S8030

(for PCB MOA)

Version 2.0a

Trademark

All registered and unregistered trademarks and company names contained in this manual are property of their respective owners including, but not limited to the following.

TYAN® is a trademark of MITAC COMPUTING TECHNOLOGY CORPORATION.
AMD® is a trademark of AMD® Corporation.
Intel® is a trademark of Intel® Corporation.
AMI, AMI BIOS are trademarks of AMI Technologies.
Microsoft®, Windows® are trademarks of Microsoft Corporation.
Nuvoton® is a trademark of Nuvoton Technology Corporation.

Notice

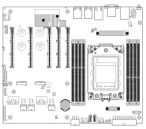
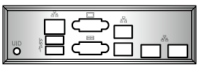
Information contained in this document is furnished by MITAC COMPUTING TECHNOLOGY CORPORATION and has been reviewed for accuracy and reliability prior to printing. MITAC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TYAN® products including liability or warranties relating to fitness for a particular purpose or merchantability. MITAC retains the right to make changes to product descriptions and/or specifications at any time, without notice. In no event will MITAC be held liable for any direct or indirect, incidental or consequential damage, loss of use, loss of data or other malady resulting from errors or inaccuracies of information contained in this document.

Contents

Before you begin…

Check the box contents!

The retail motherboard package should contain the following:

	1 x S8030 Motherboard
	2 x SATA Signal Cable
	2 x M.2 Snap Clip Kit
	1 x Rear I/O Shield
	SlimSAS 8i to 2*U.2 (NVMe) cable x 2 (Optional) FRU# FRU-CS-1230
	miniSAS HD to 4*SATA cable x3 (Optional) FRU# FRU-CS-1240
	1 x S8030 Quick reference guide

IMPORTANT NOTE:
Sales sample may not come with the accessory listed above.
Please contact your sales representative to help order accessory for your evaluation.

Chapter 1: Instruction

1.1 Congratulations

You have purchased the powerful TYAN® S8030 motherboard. The S8030 is designed to support single AMD EPYC™ 7002/7003 Series Processor, and up to 512GB RDIMM / 1,024GB LRDIMM / 2,048GB LRDIMM 3DS DDR4 memory. Leveraging advanced technology from AMDI®, the S8030 is capable of offering scalable 32 and 64-bit computing, high-bandwidth memory design, and lightning-fast PCI-E bus implementation.

The S8030 not only empowers you in today's demanding IT environment but also offers a smooth path for future application upgradeability. All of these rich feature sets provides the S8030 with the power and flexibility to meet demanding requirements for today's IT environments.

Remember to visit the TYAN® website at http://www.tyan.com. There you can find all the information on all TYAN® products as well as all the supporting documentation, FAQs, Drivers and BIOS upgrades.

1.2 Hardware Specifications

TYAN S8030 (S8030GM2NE)

Processor	**Q'ty / Socket Type**	(1) AMD Socket SP3
	Supported CPU Series	(1) AMD EPYC™ 7002/7003 Series Processor
	Configurable Thermal Design Power (cTDP) Wattage	Max up to 280W
Memory	**Supported DIMM Qty**	(8) DIMM slots
	DIMM Type / Speed	DDR4 ECC RDIMM/RDIMM 3DS/LRDIMM/LRDIMM 3DS 3200
	Capacity	Up to 512GB RDIMM/ 1,024GB LRDIMM/ 2,048GB LRDIMM 3DS *Follow latest AMD DDR4 Memory POR
	Memory channel	8 Channels per CPU
	Memory voltage	1.2V
Expansion Slots	**PCI-E**	(5) PCI-E Gen4 x16 slots
LAN	**Q'ty / Port**	(2) GbE ports + (1) GbE dedicated for IPMI

	Controller	Intel I210	
	PHY	Realtek RTL8211E	
Storage	**SATA**	**Connector**	(2) SATA, (3) SFF-8643 for (12) SATA ports
		Controller	Direct from AMD EPYC CPU
		Speed	6Gb/s
		RAID	N/A
	NVMe	**Connector (M.2)**	(2) 22110/2280 (by PCI-E Gen. 3 x4/SATA interface)
		Connector (Slim SAS)	(2) SFF-8654 for (4) NVMe ports
Graphic	**Connector type**	D-Sub 15-pin	
	Resolution	Up to 1920x1200	
	Chipset	Aspeed AST2500	
Input /Output	**USB**	(2) USB3.1 Gen1 ports (@ rear)	
	COM	(1) header	
	VGA	(1) D-Sub 15-pin VGA port (@ rear)	
	RJ-45	(2) GbE ports, (1) GbE dedicated for IPMI	
	Front Panel	(1) 2x12-pin SSI front panel header	
	SATA	(2) SATA-III connectors, (12) SATA ports from (3) Mini SAS HD connectors	
	Power	ATX 24-pin + (2) 8-pin power connectors	
System Monitoring	**Chipset**	Aspeed AST2500	
	Fan	Total (5) 4-pin headers (MOA version) / Total (4) 4-pin headers (OOY version)	
	Temperature	Monitors temperature for CPU & memory & system environment	
	Voltage	Monitors voltage for CPU, memory, chipset & power supply	
	LED	Fan fail LED indicator, Over temperature warning indicator, Fan & PSU fail LED indicator	
	Others	Watchdog timer support	
Server Management	**AST2500 iKVM**	24-bit high quality video	

	Feature	compression, Supports storage over IP and remote platform-flash, USB 2.0 virtual hub	
	AST2500 IPMI Feature	IPMI 2.0 compliant baseboard management controller (BMC), 10/100/1000 Mb/s MAC interface	
BIOS	**Brand / ROM size**	AMI, 32MB	
	Feature	Hardware Monitor, Boot from USB device/PXE via LAN/Storage, User Configurable FAN PWM Duty Cycle, Console Redirection, ACPI sleeping states S0, S5, ACPI 6.2, SMBIOS 3.2/PnP/Wake on LAN	
Physical Dimension	**Form Factor**	ATX	
	Board Dimension	12" x 9.9" (305 x 250.8mm)	
Operating System	**OS supported list**	Please refer to our AVL support lists.	
Regulation	**FCC (SDoC)**	Class A	
	CE (DoC)	Class A	
Operating Environment	**Operating Temp.**	10° C ~ 35° C (50° F~ 95° F)	
	Non-operating Temp.	- 40° C ~ 70° C (-40° F ~ 158° F)	
	In/Non-operating Humidity	90%, non-condensing at 35° C	
RoHS	**RoHS 6/6 Compliant**	Yes	
Package Contains	**Motherboard**	(1) S8030 Motherboard	
	Manual	(1) Quick Installation Guide	
	I/O Shield	(1) I/O Shield	
	Cable	**SATA**	(2) SATA signal cables

TYAN S8030 (S8030GM4NE-2T)

Processor	**Q'ty / Socket Type**	(1) AMD Socket SP3
	Supported CPU Series	(1) AMD EPYC™ 7002/7003 Series Processor
	Configurable Thermal Design Power (cTDP) Wattage	Max up to 280W

Memory	**Supported DIMM Qty**		(8) DIMM slots
	DIMM Type / Speed		DDR4 ECC RDIMM/RDIMM 3DS/LRDIMM/LRDIMM 3DS 3200
	Capacity		Up to 512GB RDIMM/ 1,024GB LRDIMM/ 2,048GB LRDIMM 3DS *Follow latest AMD DDR4 Memory POR
	Memory channel		8 Channels per CPU
	Memory voltage		1.2V
Expansion Slots	**PCI-E**		(5) PCI-E Gen4 x16 slots
LAN	**Q'ty / Port**		(2) 10GbE ports, (2) GbE ports, (1) GbE dedicated for IPMI
	Controller		Intel I210-AT, Intel X550-BT2
	PHY		Realtek RTL8211E
Storage	**SATA**	**Connector**	(2) SATA, (3) SFF-8643 for (12) SATA ports
		Controller	Direct from AMD EPYC CPU
		Speed	6Gb/s
		RAID	N/A
	NVMe	**Connector (M.2)**	(2) 22110/2280 (by PCI-E Gen. 3 x4/SATA interface)
		Connector (Slim SAS)	(2) SFF-8654 for (4) NVMe ports
Graphic	**Connector type**		D-Sub 15-pin
	Resolution		Up to 1920x1200
	Chipset		Aspeed AST2500
Input /Output	**USB**		(2) USB3.1 Gen1 ports (@ rear)
	COM		(1) header
	VGA		(1) D-Sub 15-pin VGA port (@ rear)
	RJ-45		(2) 10GbE ports, (2) GbE ports, (1) GbE dedicated for IPMI
	Front Panel		(1) 2x12-pin SSI front panel header, (2) 1x2 header
	SATA		(2) SATA-III connectors, (12) SATA ports from (3) Mini SAS HD connectors
	Power		ATX 24-pin + (2) 8-pin power

	connectors	
System Monitoring	**Chipset**	Aspeed AST2500
	Fan	Total (5) 4-pin headers (MOA version) / Total (4) 4-pin headers (OOY version)
	Temperature	Monitors temperature for CPU & memory & system environment
	Voltage	Monitors voltage for CPU, memory, chipset & power supply
	LED	Fan fail LED indicator, Over temperature warning indicator, Fan & PSU fail LED indicator
	Others	Watchdog timer support
Server Management	**AST2500 iKVM Feature**	24-bit high quality video compression, Supports storage over IP and remote platform-flash, USB 2.0 virtual hub
	AST2500 IPMI Feature	IPMI 2.0 compliant baseboard management controller (BMC), 10/100/1000 Mb/s MAC interface
BIOS	**Brand / ROM size**	AMI, 32MB
	Feature	Hardware Monitor, Boot from USB device/PXE via LAN/Storage, User Configurable FAN PWM Duty Cycle, Console Redirection, ACPI sleeping states S0, S5, ACPI 6.2, SMBIOS 3.2/PnP/Wake on LAN
Physical Dimension	**Form Factor**	ATX
	Board Dimension	12" x 9.9" (305 x 250.8mm)
Operating System	**OS supported list**	Please refer to our AVL support lists.
Regulation	**FCC (SDoC)**	Class A
	CE (DoC)	Class A
Operating Environment	**Operating Temp.**	10° C ~ 35° C (50° F~ 95° F)
	Non-operating Temp.	- 40° C ~ 70° C (-40° F ~ 158° F)
	In/Non-operating Humidity	90%, non-condensing at 35° C
RoHS	**RoHS 6/6 Compliant**	Yes
Package Contains	**Motherboard**	(1) S8030 Motherboard

	Manual	(1) Quick Installation Guide	
	I/O Shield	(1) I/O Shield	
	Cable	**SATA**	(2) SATA signal cables

1.3 Version OOY and MOA Comparison Table

Item	Version OOY	Version MOA
Total 4-pin Fan header	4	5
J31	No	Yes
J44	No	Yes
J42 System Fan Connector	Yes	Yes. Pin definitions modified.
M.2 PCIe x2 Slot (CN1/CN3)	Yes	Yes. Pin definitions modified.
Mini SAS HD Connector (J25/J26/J27)	Yes	Yes. Pin definitions modified.
Slim SAS x8 (NVME DUAL) Connector (CN2/CN4)	Yes	Yes. Pin definitions modified.

1.4 Software Specifications

For OS (operation system) support, please check with TYAN® support for latest information.

Chapter 2: Board Installation

You are now ready to install your motherboard.

How to install our products right… the first time

The first thing you should do is reading this user's manual. It contains important information that will make configuration and setup much easier. Here are some precautions you should take when installing your motherboard:

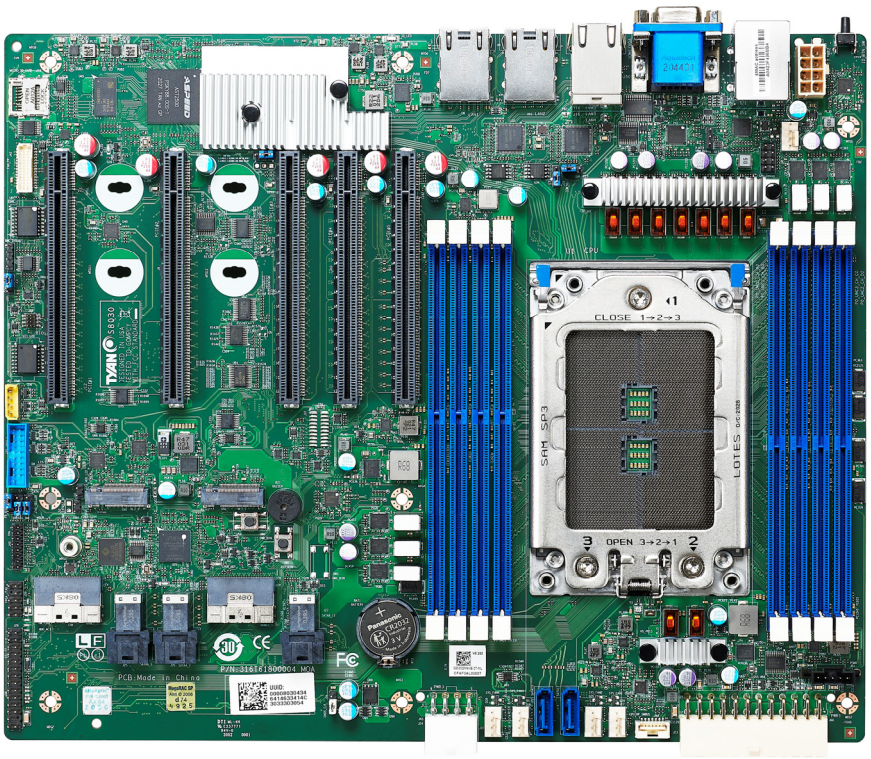
(1) Ground yourself properly before removing your motherboard from the antistatic bag. Unplug the power from your computer power supply and then touch a safely grounded object to release static charge (i.e. power supply case). For the safest conditions, MITAC recommends wearing a static safety wrist strap.
(2) Hold the motherboard by its edges and do not touch the bottom of the board, or flex the board in any way.
(3) Avoid touching the motherboard components, IC chips, connectors, memory modules, and leads.
(4) Place the motherboard on a grounded antistatic surface or on the antistatic bag that the board was shipped in.
(5) Inspect the board for damage.

The following pages include details on how to install your motherboard into your chassis, as well as installing the processor, memory, disk drives and cables.

Caution!

1. To avoid damaging the motherboard and associated components, do not use torque force greater than **5~7 kgf/cm (4.35 ~ 6.09 lb/in)** on each mounting screw for motherboard installation.
2. Do not apply power to the board if it has been damaged.

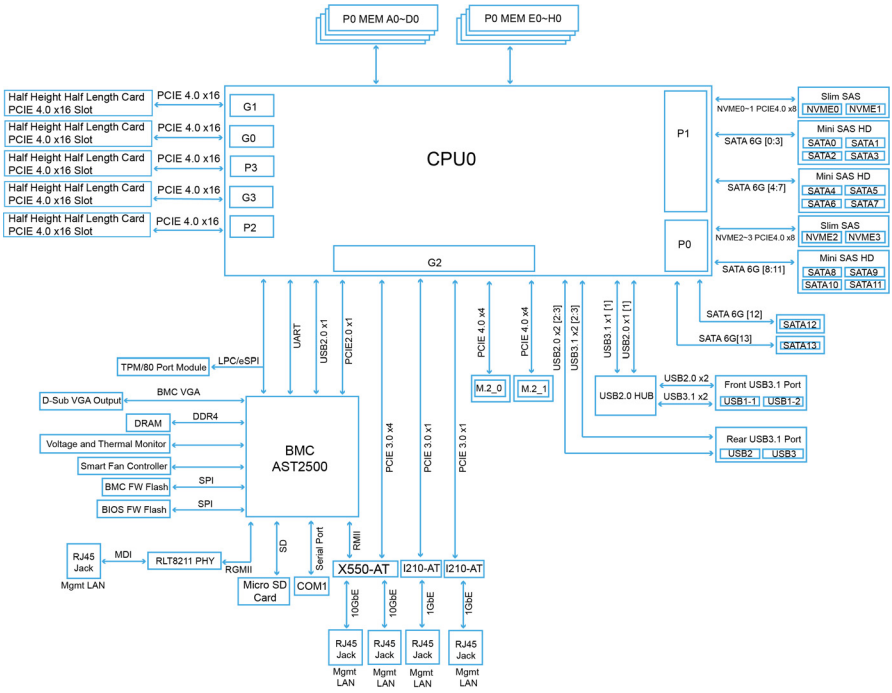
2.1 Board Image



S8030

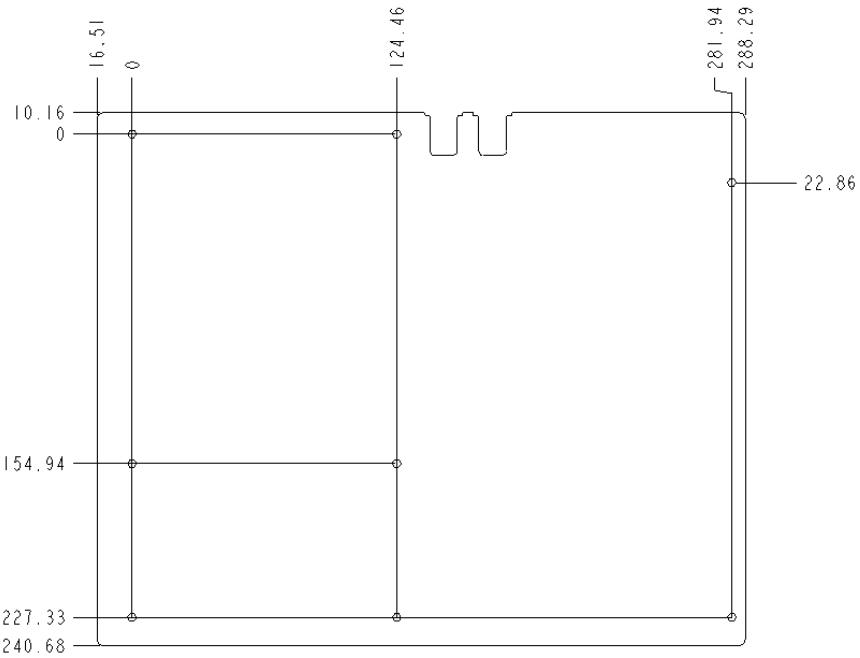
This picture is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above picture.

2.2 Block Diagram

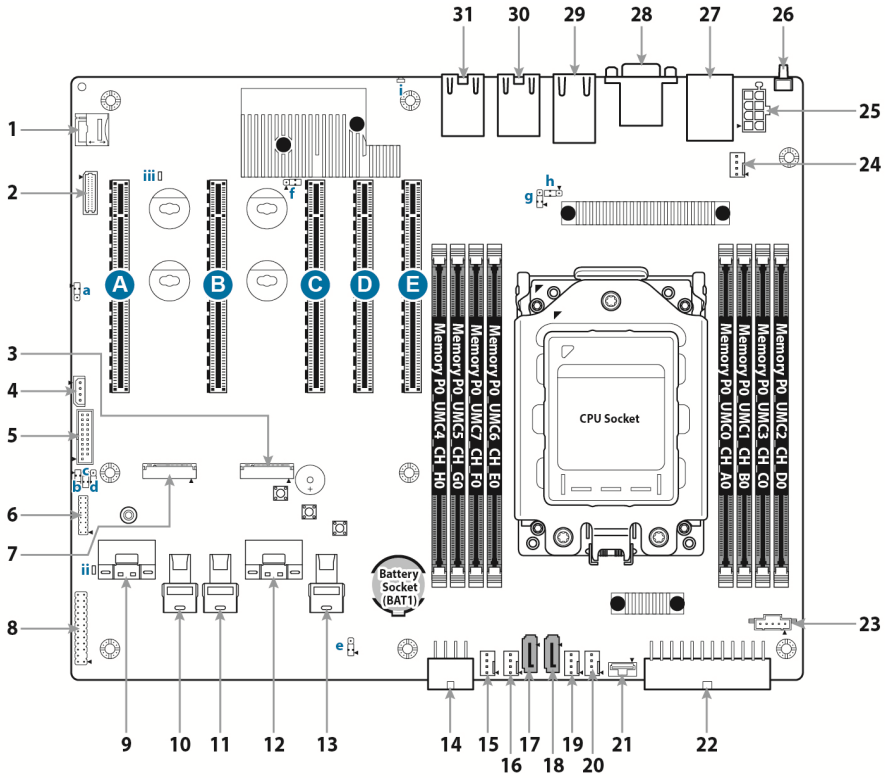


S8030 Block Diagram

2.3 Mainboard Mechanical Drawing



2.4 Board Parts, Jumpers and Connectors



This diagram is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above diagram. But for the DIMM number please refer to the above placement for memory installation. For the latest board revision, please visit our web site at http://www.tyan.com.

Jumpers & Connectors

Connectors	
1 Micro SD Connector (J19)	17 SATA Connector (J22)
2 System Fan Connector (J42)	18 SATA Connector (J14)
3 NVMe/SATA M.2 Slot (CN3)	19 System Fan Connector (J21)
4 IPMB Header (J67)	20 System Fan Connector (J17)
5 Front USB3.1 Header (J32)	21 CPU HP SMBus Connector (J44)
6 TPM Header (J40)	22 2x12pin PWR Connector (J60)
7 NVMe/SATA M.2 Slot (CN1)	23 PSMI Connector (J61)
8 Front Panel Header (J38)	24 CPU Fan Connector (J34)
9 Slim SAS 8x Connector (CN4)	25 2x4pin PWR Connector (J63)
10 Mini SAS HD Connector (J25)	26 ID Button
11 Mini SAS HD Connector (J26)	27 Stacked USB3.1x2 + IPMI LAN5 (J51)
12 Slim SAS 8x Connector (CN2)	28 COM/VGA (J50)
13 Mini SAS HD Connector (J27)	29 LAN3/LAN4 (J16)
14 2x4pin PWR Connector (J65)	30 LAN2 (U93)
15 System Fan Connector (J31)	31 LAN1 (U8)
16 System Fan Connector (J18)	
Slots	**LEDs**
A PCI-E Slot (J12)	i ID LED
B PCI-E Slot (J9)	ii HDD Active LED
C PCI-E Slot (J11)	iii BMC LED
D PCI-E Slot (J10)	
E PCI-E Slot (J13)	
Jumpers	
a BMC COM Select (J55)	e CMOS Clear (J36)
b Reset Select (J41)	f ID Button Switch (J101)
c BMC Bypass Select (J43)	g BMC COM Select (J56)
d FPGA JTAG Select (J39)	h COM Port Select (J15)

Jumper Legend

	**OPEN - Jumper OFF**	Without jumper cover
	**CLOSED - Jumper ON**	With jumper cover

J17/J18/J21/J31: System FAN Header

Pin	1	2	3	4
Signal	GND	12V	TACH	PWM

Use this header to connect the cooling fan to your motherboard to keep the system stable and reliable.
J17: SYS_FAN1 J18: SYS_FAN3
J21: SYS_FAN2 J31: SYS_FAN4

CPU_FAN (J34): CPU FAN Header

Pin	1	2	3	4
Signal	GND	12V	TACH	PWM

Use this header to connect the cooling fan to your motherboard to keep the system stable and reliable.

J38: Front Panel Pin Header

Signal	Pin	Pin	Signal
FP_PW_LED_PW	1	2	FP_CONN_PWR
NC	3	4	FP_ID_LED_PW
FP_PW_LED_GND	5	6	FP_ID_LED_L
HDD_LED_PW	7	8	BMC_HW_FAULT_L
HDD_ACT_LED_L	9	10	BMC_SYS_FAULT_L
FP_PWR_BTN_L	11	12	LAN0_LED_P
GND	13	14	LAN0_LED_L
FP_RST_BTN_JP_L	15	16	FP_SMB_DAT
GND	17	18	FP_SMB_CLK
FP_IDLED_BTN_L	19	20	FP_INTRUSION_L
SYS_AIR_INLET	21	22	LAN1_LED_P
FP_NMI_BTN_L	23	24	LAN1_LED_L

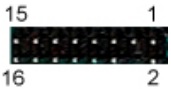
J61: PSMI Connector

Pin	Signal
1	PSMI_SMBCLK
2	PSMI_SMBDATA
3	PSMI_PMBUS_ALERT_L
4	GND
5	PSMI_VDD

J67: IPMB Pin Header

Pin	Signal
1	BMC_SMB_IPMB_5VS_DAT
2	GND
3	BMC_SMB_IPMB_5VS_CLK
4	VDD_33_DUAL

J40: LPC Debug Port and TPM Header



Signal	Pin	Pin	Signal
VDD_33_RUN	1	2	DBG_LFRAME_N
DBG_LPC0	3	4	KEY
DBG_LPC1	5	6	DBG_PLTRST_N
DBG_LPC2	7	8	GND
DBG_LPC3	9	10	DBG_CLK
DBG_SERIRQ	11	12	GND
DBG_PRES_N	13	14	VDD_33_DUAL
VDD_33_DUAL	15	16	DBG_TPM_PP_EN

J32: Front USB3.1 Header

Signal	Pin	Pin	Signal
VDD_5_USB_REAR	1	20	NC
P0_USB_0_SS_0RX_ESD_L	2	19	VDD_5_USB_REAR
P0_USB_0_SS_0RX_ESD_H	3	18	P0_USB_0_SS_1RX_ESD_L
GND	4	17	P0_USB_0_SS_1RX_ESD_H
P0_USB_0_SS_0TX_ESD_L	5	16	GND
P0_USB_0_SS_0TX_ESD_H	6	15	P0_USB_0_SS_1TX_ESD_L
GND	7	14	P0_USB_0_SS_1TX_ESD_H
USB2_HUB_ESD_DN1	8	13	GND
USB2_HUB_ESD_DP1	9	12	USB2_HUB_ESD_DN2
P0_USB3_FRONT_OC_R_N	10	11	USB2_HUB_ESD_DP2

J14/J22: 7-pin Vertical SATA Connector

PIN Define	Pin	
1	SGND0	Connects to the Serial ATA ready drives via the Serial ATA cable.
2	TX+	
3	TX-	
4	SGND1	
5	RX-	
6	RX+	
7	SGND2	

CN2 (NVME0_1) / CN4 (NVME2_3): Slim SAS 8x dual NVMe Connector

Signal Name	Pin	Pin	Signal Name
GND	A1	B1	GND
NVME[0]/[2]_RX_P0	A2	B2	NVME[0]/[2]_TX_P0
NVME[0]/[2]_RX_N0	A3	B3	NVME[0]/[2]_TX_N0
GND	A4	B4	GND
NVME[0]/[2]_RX_P1	A5	B5	NVME[0]/[2]_TX_P1
NVME[0]/[2]_RX_N1	A6	B6	NVME[0]/[2]_TX_N1
GND	A7	B7	GND
NC	A8	B8	NVME[0]/[2]_SCL
NVME[01]/[23]_WAKE[01]/[23]	A9	B9	NVME[0]/[2]_SDA
GND	A10	B10	GND
NVME[0]/[2]_CLK_DP	A11	B11	NVME[0]/[2]_PERST_L
NVME[0]/[2]_CLK_DN	A12	B12	NVME[0]/[2]_PRSNT_L
GND	A13	B13	GND
NVME[0]/[2]_RX_P2	A14	B14	NVME[0]/[2]_TX_P2
NVME[0]/[2]_RX_N2	A15	B15	NVME[0]/[2]_TX_N2
GND	A16	B16	GND
NVME[0]/[2]_RX_P3	A17	B17	NVME[0]/[2]_TX_P3
NVME[0]/[2]_RX_N3	A18	B18	NVME[0]/[2]_TX_N3
GND	A19	B19	GND
NVME[1]/[3]_RX_P0	A20	B20	NVME[1]/[3]_TX_P0
NVME[1]/[3]_RX_N0	A21	B21	NVME[1]/[3]_TX_N0
GND	A22	B22	GND
NVME[1]/[3]_RX_P1	A23	B23	NVME[1]/[3]_TX_P1
NVME[1]/[3]_RX_N1	A24	B24	NVME[1]/[3]_TX_N1
GND	A25	B25	GND
NC	A26	B26	NVME[1]/[3]_SCL

	NVME[01]/[23]_WAKE[01]/[23]	**A27**	**B27**	NVME[1]/[3]_SDA
	GND	**A28**	**B28**	GND
	NVME[1]/[3]_CLK_DP	**A29**	**B29**	NVME[1]/[3]_PERST_L
	NVME[1]/[3]_CLK_DN	**A30**	**B30**	NVME[1]/[3]_PRSNT_L
	GND	**A31**	**B31**	GND
	NVME[1]/[3]_RX_P2	**A32**	**B32**	NVME[1]/[3]_TX_P2
	NVME[1]/[3]_RX_N2	**A33**	**B33**	NVME[1]/[3]_TX_N2
	GND	**A34**	**B34**	GND
	NVME[1]/[3]_RX_P3	**A35**	**B35**	NVME[1]/[3]_TX_P3
	NVME[1]/[3]_RX_N3	**A36**	**B36**	NVME[1]/[3]_TX_N3
	GND	**A37**	**B37**	GND

J25/J26/J27: Mini SAS HD Connector

Signal	Pin	Pin	Signal
GND1	**A3**	**C3**	GND7
RXA0_DP	**B4**	**D4**	TXA0_DP
RXA0_DN	**B5**	**D5**	TXA0_DN
GND2	**A6**	**C6**	GND8
RXA1_DP	**A4**	**C4**	TXA1_DP
RXA1_DN	**A5**	**C5**	TXA1_DN
GND3	**A9**	**C9**	GND9
SGPIO_CLK	**A2**	**A1**	SIDEBAND0
SGPIO_LOAD	**B2**	**B1**	SIDEBAND1
SIDEBAND4	**C2**	**C1**	SGPIO_DATA_OUT
SIDEBAND5	**D2**	**D1**	SGPIO_DATA_IN
GND1	**B3**	**D3**	GND10
RXA2_DP	**B7**	**D7**	TXA2_DP
RXA2_DN	**B8**	**D8**	TXA2_DN
GND2	**B6**	**D6**	GND11
RXA3_DP	**A7**	**C7**	TXA3_DP
RXA3_DN	**A8**	**C8**	TXA3_DN
GND3	**B9**	**D9**	GND12

J19: Micro SD Card Connector

Pin	Signal
1	DAT2
2	DAT3
3	CMD
4	VDD(3.3V)
5	CLK
6-1	VSS
7	DAT0
8	DATA1
6-2	CD

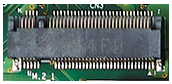
FAN_FP (J42): System Fan Connector (Reserved for Barebone)

Pin	Signal Name	Pin	Signal Name
1	SYS_FAN_T1	2	SYS_FAN_T6
3	SYS_FAN_T2	4	SYS_FAN_T7
5	SYS_FAN_T3	6	SYS_FAN_T8
7	SYS_FAN_T4	8	SYS_FAN_T9
9	SYS_FAN_T5	10	SYS_FAN_T10
11	GND	12	GND
13	BMC_PWM_BUF_FAN3	14	BMC_PWM_BUF_FAN2
15	SYS_FAN_T11	16	FAN_SDA
17	SYS_FAN_T12	18	FAN_SCL
19	VDD_33_DUAL	20	BMC_PWM_BUF_FAN4
21	VDD_33_DUAL	22	GND
23	SYS_FAN_T13	24	SYS_FAN_T15
25	SYS_FAN_T14	26	SYS_FAN_T16
27	BMC_PWM_BUF_FAN5	28	BMC_PWM_BUF_FAN6
29	BMC_PWM_BUF_FAN0	30	GND

J44: CPU HP SMBus Connector

Pin	Signal
1	3.3V_Dual
2	CPU_HP_SMBUS_CLK
3	CPU_HP_SMBUS_DATA
4	CPU_HP_ALERT
5	NC
6	NC
7	GND

CN1 / CN3: M.2 PCIe x2 Slot



Signal	Pin	Pin	Signal
GND	1	2	3.3V_RUN
GND	3	4	3.3V_RUN
PERN3	5	6	PRSNT2#
PERP3	7	8	N/C
GND	9	0	LED
PETN3	11	12	3.3V_RUN
PETP3	13	14	3.3V_RUN
GND	15	16	3.3V_RUN
PERN2	17	18	3.3V_RUN
PERP2	19	20	N/C
GND	21	22	N/C
PETN2	23	24	N/C
PETP2	25	26	N/C
GND	27	28	N/C
PERN1	29	30	12V_RUN
PERP1	31	32	12V_RUN
GND	33	34	12V_RUN
PETN1	35	36	12V_RUN(Pre-Charge)
PETP1	37	38	M2_DEVSLP
GND	39	40	I2C_M2_SCL(1.8V)
PERN0 / SATA-B+	41	42	I2C_M2_SDA(1.8V)
PERP0 / SATA-B-	43	44	N/C
GND	45	46	N/C
PETN0 / SATA-A-	47	48	N/C
PETP0 / SATA-A+	49	50	M2_PERST
GND	51	52	N/C
PE_CLK_N	53	54	M2_PEWAKE
PE_CLK_P	55	56	N/C
GND	57	58	N/C
PRSNT1#(GND)	67	68	N/C
PEDER_OC-PCIE/GND-SATA	69	70	3.3V_RUN
GND	71	72	3.3V_RUN
GND	73	74	3.3V_RUN
GND	75		

J36: Clear CMOS Jumper

 PIN1 Normal (**Default**)	You can reset the CMOS settings by using this jumper. This can be useful if you have forgotten your system/setup password, or need to clear the system BIOS setting. 1. Power off system and disconnect power connectors from the motherboard. 2. Remove the jumper from Pin_1 and Pin_2 (Default setting). 3. Move the jumper cap to close Pin_2 and Pin_3 for several seconds to Clear CMOS. 4. Put jumper cap back to Pin_1 and Pin_2 (Default setting). 5. Reconnect power connectors to the motherboard and power on system.
 PIN1 Clear CMOS	

J15: COM Port Select Jumper

 PIN1	Pin 1-2 Closed: AMD COM Port0
 PIN1	Pin 2-3 Closed: BMC Console Port1 (**Default**)

J39: FPGA JTAG Select Jumper

 PIN1	Pin 1-2 Closed: Switch to CONN
 PIN1	Pin 2-3 Closed: Switch to BMC (**Default**)

J41: Reset Select Jumper

 PIN1	Pin 1-2 Closed: FP Reset Button=System Reset (**Default**)
 PIN1	Pin 2-3 Closed: FP Reset Button=BMC Reset

J55/J56: BMC COM Select Jumper

	Pin 1-2 Closed: BMC COM Port1 (**Default**)
	Pin 2-3 Closed: BMC Console Port5

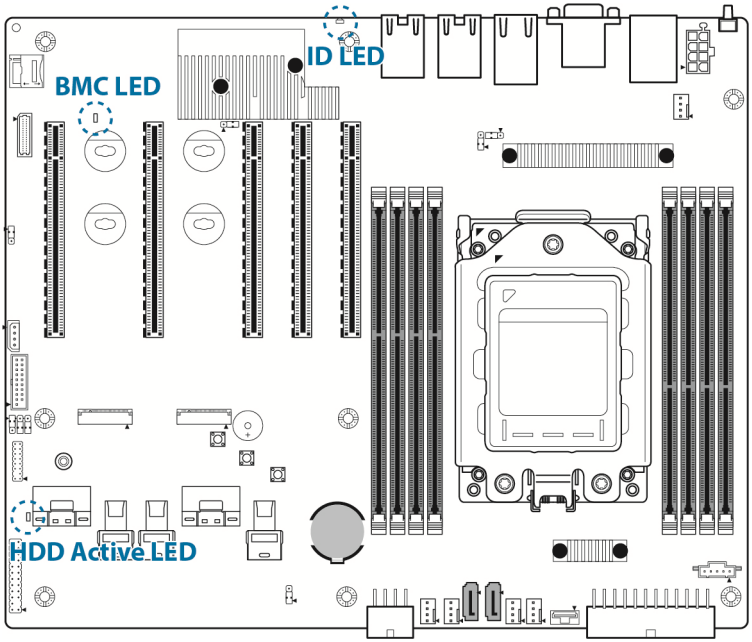
J43: Bypass BMC Jumper

	Pin 1-2 Closed: Bypass BMC
	Pin 2-3 Closed: FPGA waits for BMC ready (**Default**)

J101: ID Button Switch

	Pin 1-2 Closed: Press 5 seconds for BMC HW Reset
	Pin 2-3 Closed: Press 5 seconds for power on/off (**Default**)

2.5 LED Definitions



Location	State	Description	Note
ID LED	On	Interface shows on	The blue System Identification LED is used to help identify a system for servicing when it is installed within a high density rack or cabinet that is populated with several other similar systems.
	Off	Interface shows off	
	Blinking	N/a	
BMC LED	On	BMC initialing or inactive	BMC heartbeat LED for5 BMC activity indications.
	Off	BMC inactive	
	Blin king	BMC work normally	
HDD Active LED	On	HDD active	HDD Active LED is only for M.2 device.
	Off	HDD inactive	
	Blinking	N/A	

2.6 Installing the Processor and Heat sink

The S8030 supported AMD® processors are listed in section ***1.2 Hardware*** Specifications on page 5. Check our website at **http://www.tyan.com** for latest processor support.

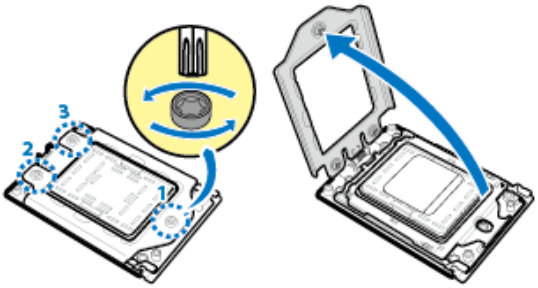
> **NOTE:** MITAC TYAN is not liable for damage as a result of operating an unsupported configuration.

Processor Installation for AMD Socket SP3

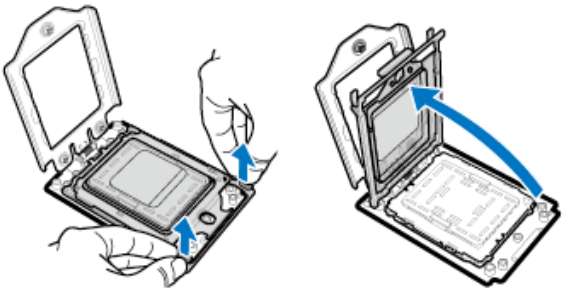
Follow the steps below to install the processors and heat sinks.
NOTE: Please save and replace the CPU protection cap when returning for service.

1. Use a T20 Torx screwdriver to loosen the screws securing the force frame in a sequential order (3→2→1).

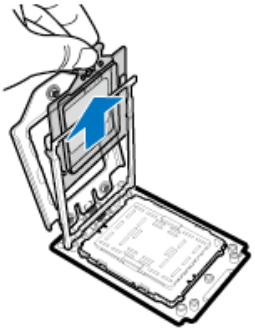
> **NOTE:** The force frame will automatically eject after the captive screws are being released.



2. By placing your both index fingers on the sides on the metal handle, pull to release the rail frame. Then lift the rail frame to its fully open position.



3. Remove the external cap from the rail frame.

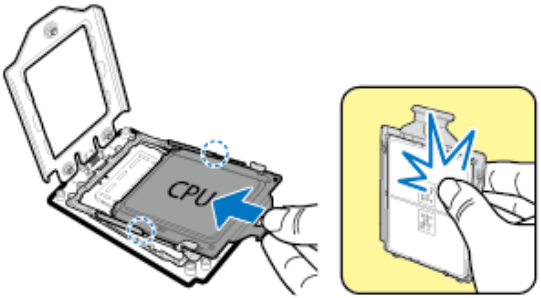


4. Align and install the carrier frame with package into the slot on the rail frame.

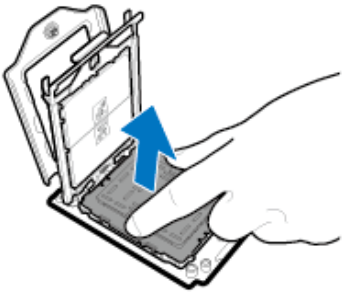
NOTE: During installation, observe the following:

■ Make sure to push the carrier frame with package towards the end of the rail frame until it clicks into place.

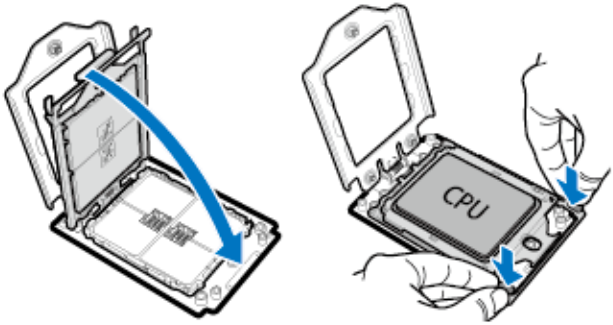
■ Do not drop the carrier frame or touch the package pad to avoid component damage.



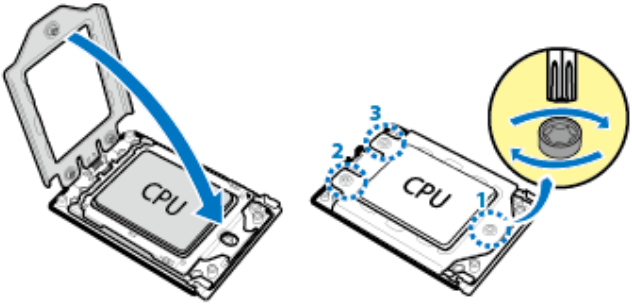
5. Using your thumb and forefinger, remove the PnP cap by lifting it up vertically.



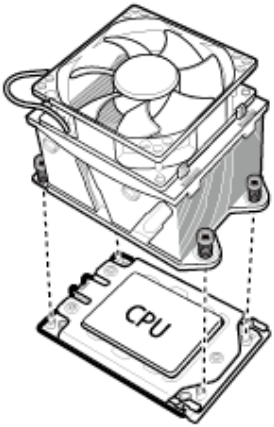
6. Carefully close the rail frame with the installed package. Then push both edges of the rail frame firmly until it locks in place.



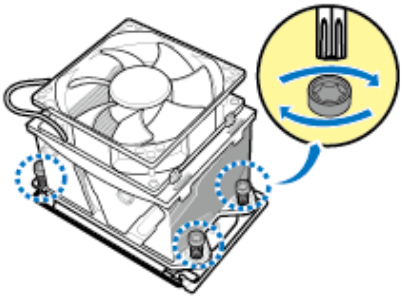
7. Close the force frame. Then use a T20 Torx screwdriver to tighten the screws to secure the force frame in a sequential order (1→2→3).



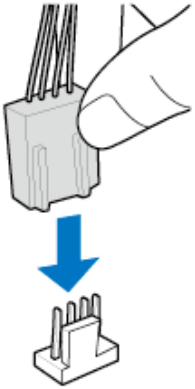
8. Align and install the CPU heatsink onto the top of the CPU socket.



9. Use a T20 Torx screwdriver to tighten the heatsink screws.



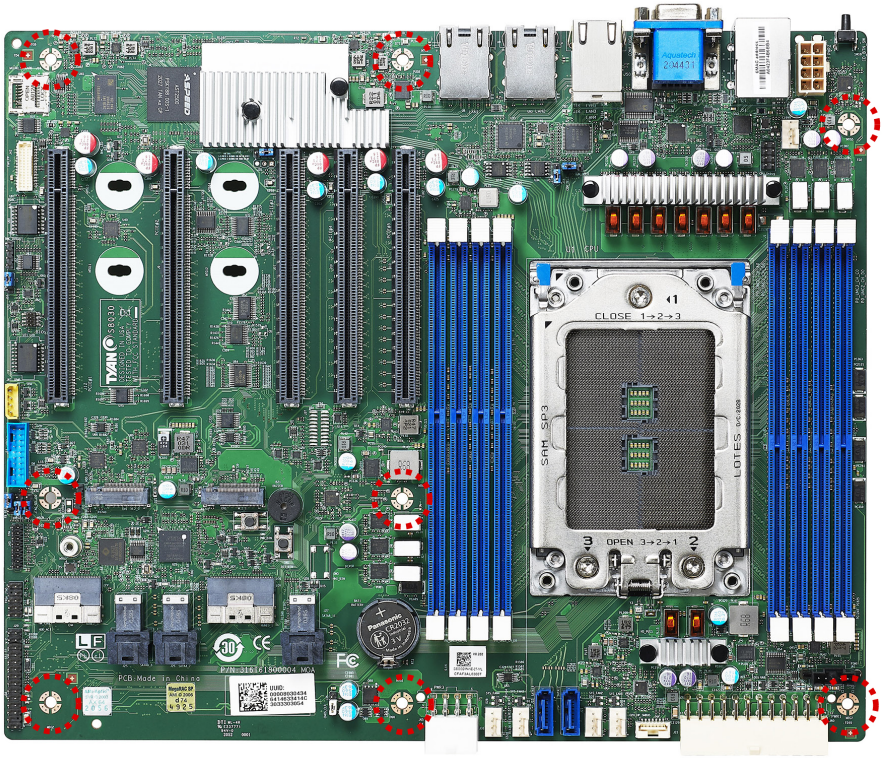
10. Connect the heatsink power cable to the mainboard connector.



NOTE: Always check with the manufacturer of the heat sink & processor to ensure that the thermal interface material is compatible with the processor and meets the manufacturer's warranty requirements.

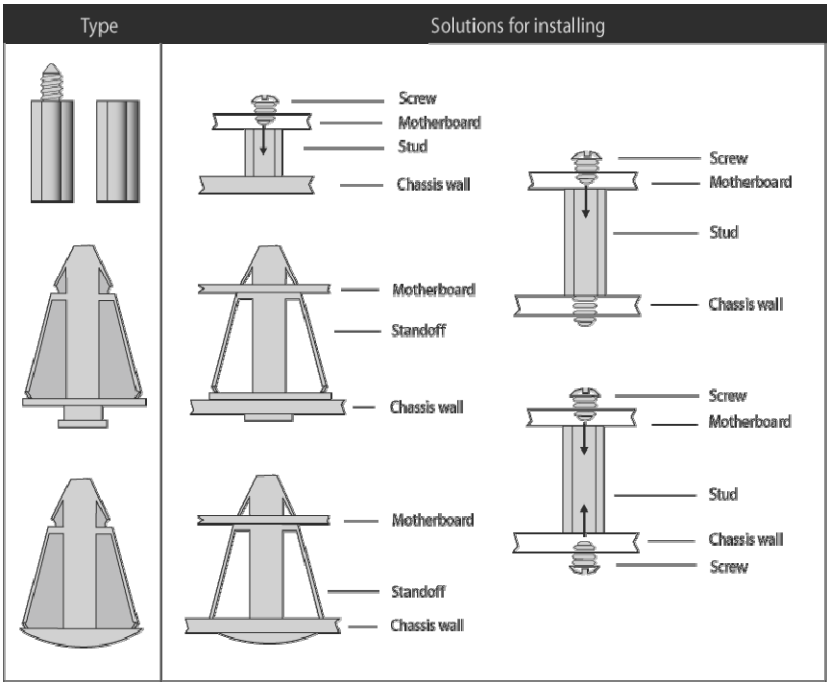
2.7 Tips on Installing Motherboard in Chassis

Before installing your motherboard, make sure your chassis has the necessary motherboard support studs installed. These studs are usually metal and are gold in color. Usually, the chassis manufacturer will pre-install the support studs. If you are unsure of stud placement, simply lay the motherboard inside the chassis and align the screw holes of the motherboard to the studs inside the case. If there are any studs missing, you will know right away since the motherboard will not be able to be securely installed.



Some chassis include plastic studs instead of metal. Although the plastic studs are usable, MITAC recommends using metal studs with screws that will fasten the motherboard more securely in place.

Below is a chart detailing what the most common motherboard studs look like and how they should be installed.

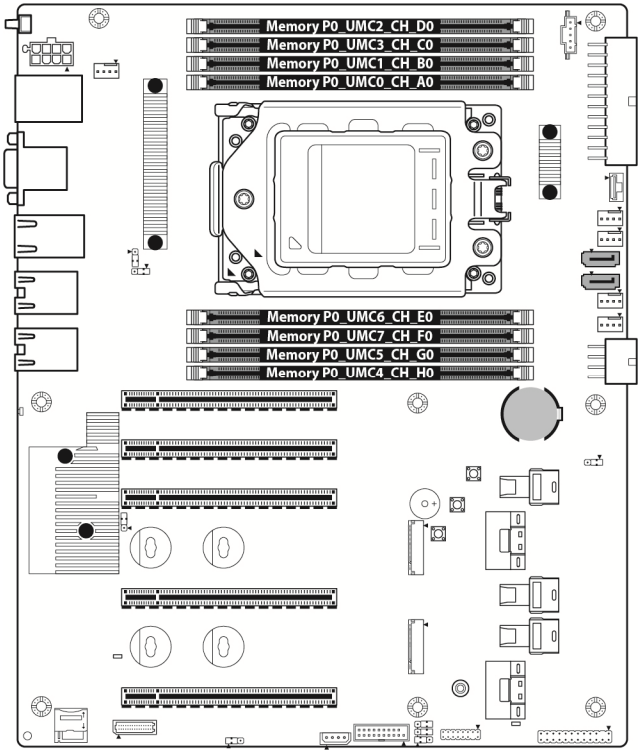

Type
Solutions for installing
Screw
Motherboard
Stud
Chassis wall
Motherboard
Standoff
Chassis wall
Motherboard
Standoff
Chassis wall
Screw
Motherboard
Stud
Chassis wall
Screw
Motherboard
Stud
Chassis wall
Screw

2.8 Installing the Memory

Before installing memory, ensure that the memory you have is compatible with the motherboard and processor. Check the TYAN Web site at http://www.tyan.com for details of the type of memory recommended for your motherboard.

- This platform supports (4)+(4) DDR4 ECC RDIMM/RDIMM 3DS/LRDIMM/ LRDIMM 3DS 3200
- Up to 512GB RDIMM / 1024GB LRDIMM / 2048GB LRDIMM 3DS are supported
- 1.2V DDR4 DIMMs are supported
- All installed memory will be automatically detected. No jumpers or settings need to be changed for memory detection.
- All memory must be of the same type and density. **Different memory types can NOT be mixed and matched on the same motherboard.**

DIMM Location



NOTE:
1. √ indicates a populated DIMM slot.
2. Use paired memory installation for max performance.
3. Populate the same DIMM type in each channel, specifically
   - Use the same DIMM size
   - Use the same # of ranks per DIMM

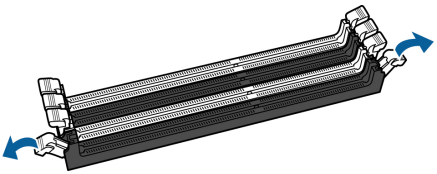
Memory Population Table

Single CPU Populated (CPU0)	Quantity of Memory Module Populated			
	1	2	4	8
P0_UMC0_CH_A0	Not Recommended			v
P0_UMC1_CH_B0				v
P0_UMC3_CH_C0			v	v
P0_UMC2_CH_D0			v	v
P0_UMC6_CH_E0				v
P0_UMC7_CH_F0				v
P0_UMC5_CH_G0			v	v
P0_UMC4_CH_H0			v	v

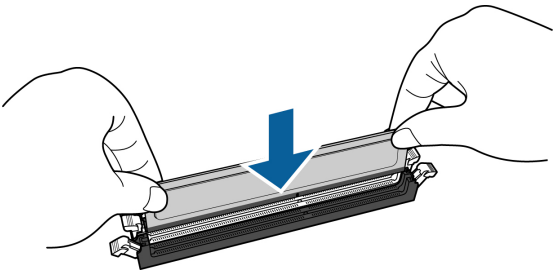
Memory Installation Procedure

Follow these instructions to install memory modules into the S8030.

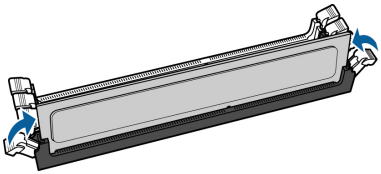
1. Unlock the clips as shown in the illustration.



2. Insert the memory module firmly into the socket by gently pressing down until it sits flush with the socket.



3. Lock the clips to secure the memory module into place.

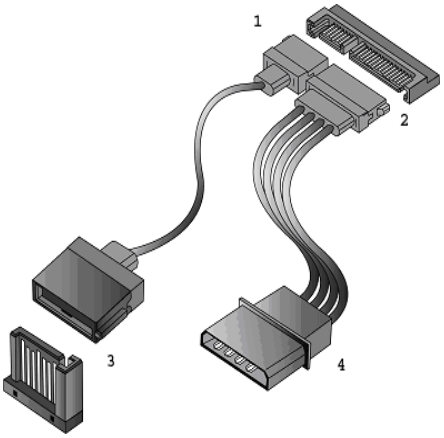


2.9 Attaching Drive Cables

Attaching Serial ATA Cables

S8030 is equipped with **two (2)** Serial ATA (SATA) channel. Connections for the drives are very simple.
There is no need to set Master/Slave jumpers on SATA drives.
If you are in need of SATA/SAS cables or power adapters please contact your place of purchase.

The following pictures illustrate how to connect an SATA drive.



1. SATA drive cable connection

2. SATA drive power connection

3. SATA cable motherboard connector

4. SATA drive power adapter

2.10 Installing Add-In Cards

Before installing add-in cards, it's helpful to know if they are fully compatible with your motherboard. For this reason, we've provided the diagrams below, showing the slots that may appear on your motherboard.

PCI-E Gen4 x16 slot

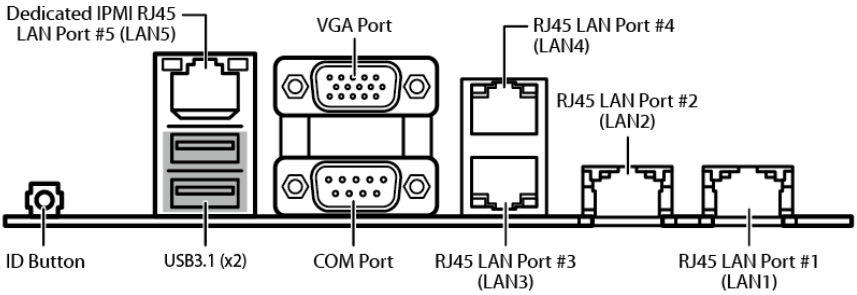
Simply find the appropriate slot for your add-in card and insert the card firmly. Do not force any add-in cards into any slots if they do not seat in place. It is better to try another slot or return the faulty card rather than damaging both the motherboard and the add-in card.

TIP: It's a good practice to install add-in cards in a staggered manner rather than making them directly adjacent to each other. Doing so allows air to circulate within the chassis more easily, thus improving cooling for all installed devices.

NOTE: You must always unplug the power connector to the motherboard before performing system hardware changes to avoid damaging the board or expansion device.

2.11 Connecting External Devices

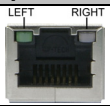
Connecting external devices to the motherboard is an easy task. The motherboard supports a number of different interfaces through connecting peripherals. See the following diagrams for the details.



NOTE: Peripheral devices can be plugged straight into any of these ports but software may be required to complete the installation.

Onboard LAN LED Color Definition

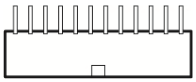
The five (5) onboard Ethernet ports have green and yellow LEDs to indicate LAN status. The chart below illustrates the different LED states.

10Mbps/100Mbps/1Gbps/10Gbps LAN Link/Activity LED Scheme			
		**Left LED**	**Right LED**
No Link		Off	Off
10Mbps	**Link**	Green	Off
	Active	Blinking Green	Off
100Mbps	**Link**	Green	Solid Green
	Active	Blinking Green	Solid Green
1Gbps	**Link**	Green	Solid Yellow
	Active	Blinking Green	Solid Yellow
10Gbps	**Link**	Green	Solid Yellow
	Active	Blinking Green	Solid Yellow

2.12 Installing the Power Supply

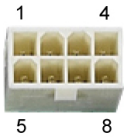
There are **three (3)** power connectors on your S8030 motherboard. The S8030 supports EPS 12V power supply.

J60: ATX 24-pin Main Power Connector



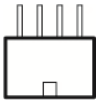
Signal	Pin	Pin	Signal
VDD_33_RUN	1	13	VDD_33_RUN
VDD_33_RUN	2	14	N12V
GND	3	15	GND
VDD_5_RUN	4	16	PS_ON_L
GND	5	17	GND
VDD_5_RUN	6	18	GND
GND	7	19	GND
PWRGD_PS	8	20	NC
VDD_5_STBY_PSU	9	21	VDD_5_RUN
VDD_12_RUN	10	22	VDD_5_RUN
VDD_12_RUN	11	23	VDD_5_RUN
VDD_33_RUN	12	24	GND

J63: CPU Power Connector (CPU / CPU FAN / Memory ABCD)



Signal	Pin	Pin	Signal
GND	1	5	P0_VDD_12_RUN
GND	2	6	P0_VDD_12_RUN
GND	3	7	P0_VDD_12_RUN
GND	4	8	P0_VDD_12_RUN

J65: 12V Power Connector (Memory EFGH / FAN_Connector / PCIE Slot)



Signal	Pin	Pin	Signal
GND	1	5	VDD_12_RUN
GND	2	6	VDD_12_RUN
GND	3	7	VDD_12_RUN
GND	4	8	VDD_12_RUN

NOTE:
You must unplug the power supply before plugging the power cables to motherboard connectors.

2.13 Finishing Up

Congratulations on making it this far! You have finished setting up the hardware aspect of your computer. Before closing up your chassis, make sure that all cables and wires are connected properly, especially IDE cables and most importantly, jumpers. You may have difficulty powering on your system if the motherboard jumpers are not set correctly.
In the rare circumstance that you have experienced difficulty, you can find help by asking your vendor for assistance. If they are not available for assistance, please find setup information and documentation online at our website or by calling your vendor's support line.

NOTE

Chapter 3: BIOS Setup

3.1 About the BIOS

The BIOS is the basic input/output system, the firmware on the motherboard that enables your hardware to interface with your software. The BIOS determines what a computer can do without accessing programs from a disk. The BIOS contains all the code required to control the keyboard, display screen, disk drives, serial communications, and a number of miscellaneous functions. This chapter describes the various BIOS settings that can be used to configure your system.

The BIOS section of this manual is subject to change without notice and is provided for reference purposes only. The settings and configurations of the BIOS are current at the time of print and are subject to change, and therefore may not match exactly what is displayed on screen.

This section describes the BIOS setup program. The setup program lets you modify basic configuration settings. The settings are then stored in a dedicated, battery-backed memory (called NVRAM) that retains the information even when the power is turned off.

To start the BIOS setup utility:

1. Turn on or reboot your system.
2. Press <**Del**> or <**F2**> during POST (**Del** on remote console) to start the BIOS setup utility.

3.1.1 Setup Basics

The table below shows how to navigate in the setup program using the keyboard.

Key	Function
Left/Right Arrow Keys	Change from one menu to the next
Up/Down Arrow Keys	Move between selections
Enter	Open highlighted section
PgUp/PgDn Keys	Change pages
+/-	Change options
ESC	Exit

3.1.2 Getting Help

Pressing [**F1**] will display a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window, press [**ESC**] or the [**Enter**] key again.

3.1.3 In Case of Problems

If you have trouble booting your computer after making and saving the changes with the BIOS setup program, you can restart the computer by holding the power button down until the computer shuts off (usually within 4 seconds); resetting by pressing CTRL-ALT-DEL; or clearing the CMOS.
The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset section unless you are absolutely sure of what you are doing. The Chipset defaults have been carefully chosen either by MITAC or your system manufacturer for best performance and reliability. Even a seemingly small change to the Chipset setup options may cause the system to become unstable or unusable.

3.1.4 Setup Variations

Not all systems have the same BIOS setup layout or options. While the basic look and function of the BIOS setup remains more or less the same for most systems, the appearance of your Setup screen may differ from the charts shown in this section. Each system design and chipset combination requires a custom configuration. In addition, the final appearance of the Setup program depends on the system designer. Your system designer may decide that certain items should not be available for user configuration, and remove them from the BIOS setup program.

NOTE: The following pages provide the details of BIOS menu. Please be noticed that the BIOS menu are continually changing due to the BIOS updating. The BIOS menu provided are the most updated ones when this manual is written. Please visit TYAN's website at http://www.tyan.com for the information of BIOS updating.

3.2 Main Menu

In this section, you can alter general features such as the date and time.
Note that the options listed below are for options that can directly be changed within the Main Setup screen.

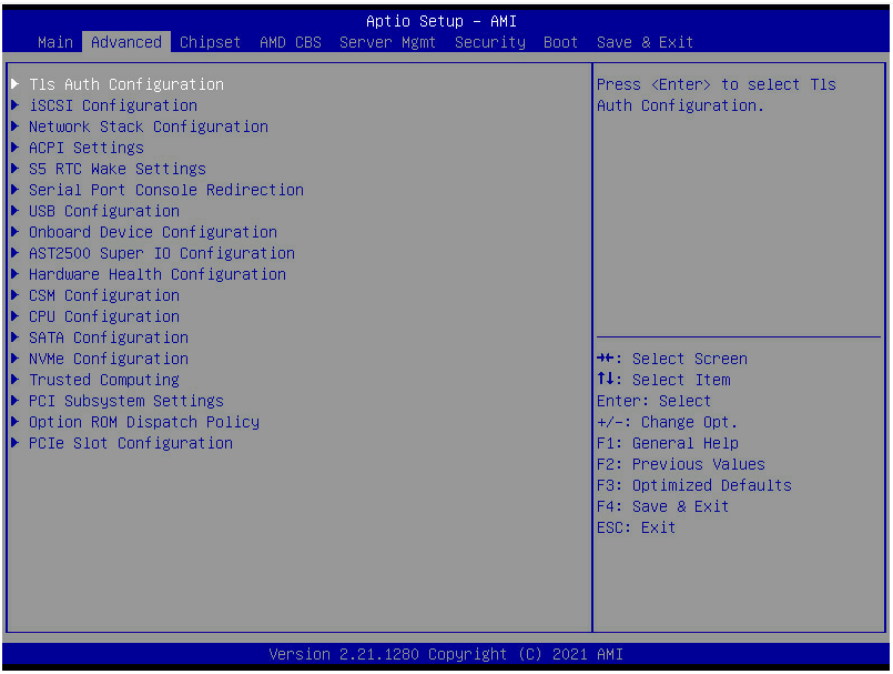
System Language
Choose the system default language.
English / Simplified Chinese / Japanese

System Date
Set the Date. Use Tab to switch between Date elements. Default Ranges:
Year: 1998-9999
Months: 1-12
Days: dependent on month

System Time
Set the Time. Use Tab to switch between Time elements.

3.3 Advanced Menu

This section facilitates configuring advanced BIOS options for your system.



T1s Auth Configuration
Press <Enter> to select T1s Auth Configuration.

iSCSI Configuration
Configure the iSCSI parameters.

Network Stack Configuration
Network Stack Settings.

ACPI Settings
System ACPI Parameters.

S5 RTC Wake Settings
Enable system to wake from S5 using RTC alarm.

Serial Port Console Redirection
Serial Port Console Redirection.

USB Configuration
USB Configuration Parameters.

Onboard Device Configuration
Onboard Device Configuration.

AST2500 Super IO Configuration
System Super IO Chip Parameters.

Hardware Health Configuration
Hardware health Configuration Parameters.

CSM Configuration
CSM configuration: Enable/Disable, Option ROM execution settings, etc.

CPU Configuration
CPU Configuration Parameters.

SATA Configuration
SATA Device Information.

NVMe Configuration
NVMe Device Options Settings.

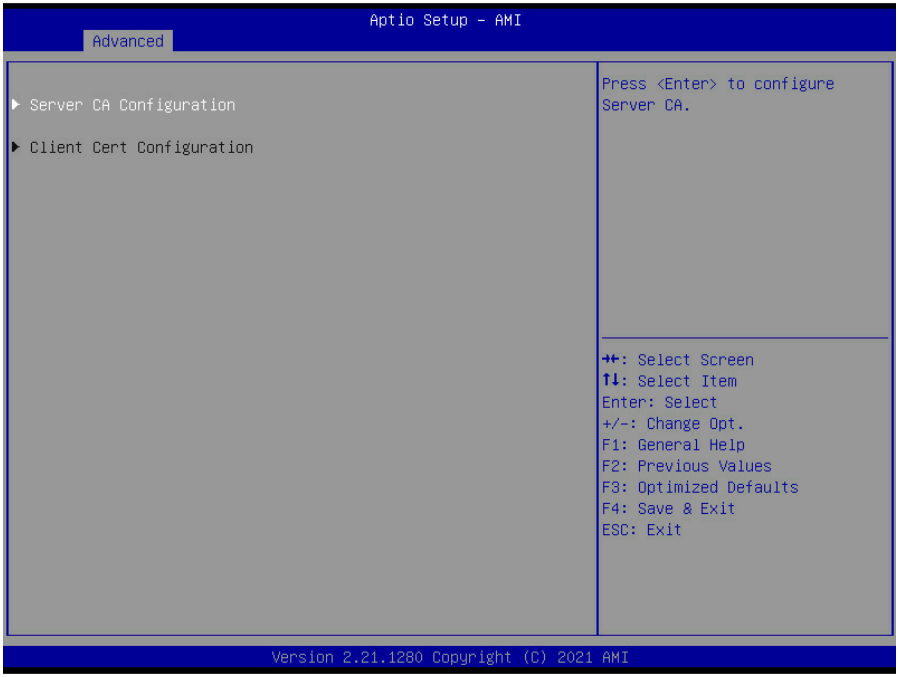
Trusted Computing
Trusted Computing Settings.

PCI Subsystem Settings
PCI, PCI-X and PCI Express Settings.

Option ROM Dispatch Policy
Option ROM Dispatch Policy.

PCIE Slot Configuration
Onboard PCIE Slot Configuration

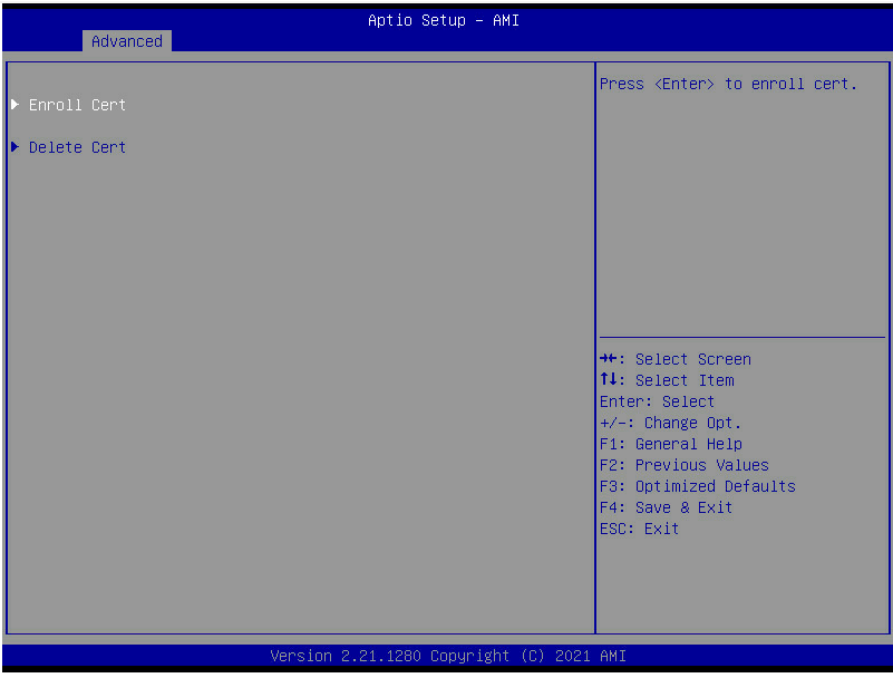
3.3.1 T1s Auth Configuration



Server CA Configuration
Press <Enter> to configure Server CA.

Client Cert Configuration
Press <Enter> to configure Client Cert.

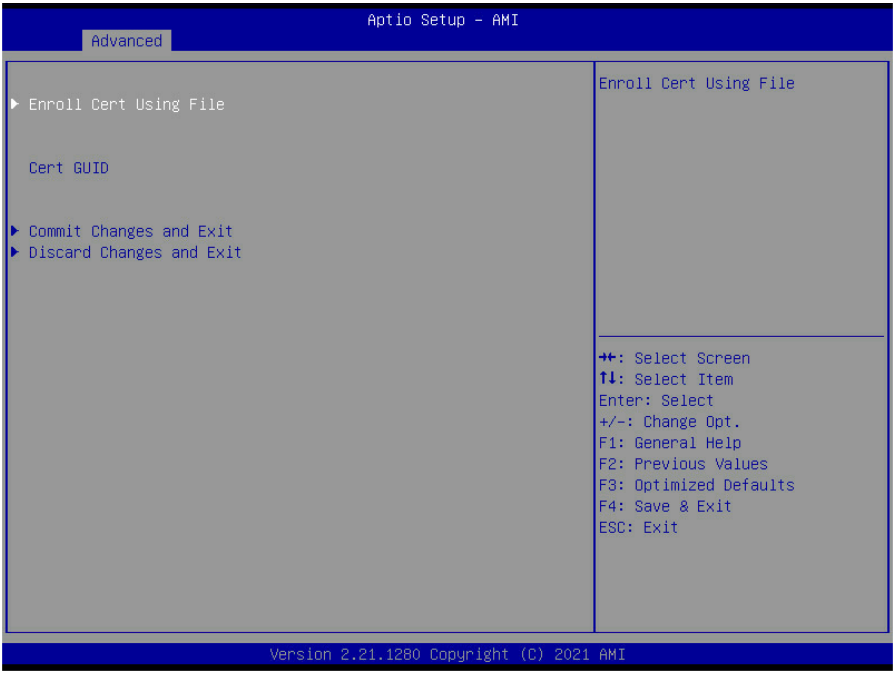
3.3.1.1 Server CA Configuration



Enroll Cert
Press <Enter> to enroll cert.

Delete Cert
Press <Enter> to delete cert.

3.3.1.1.1 Enroll Cert



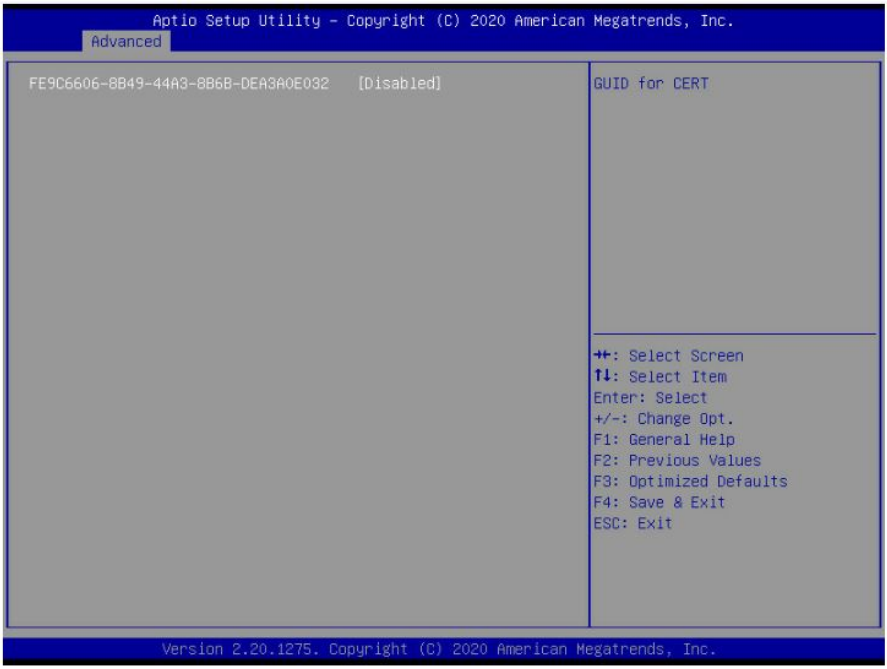
Enroll Cert Using File
Enroll Cert Using File.

Cert GUID
Input digit character in 11111111-2222-3333-4444-1234567890ab format.

Commit Changes and Exit
Commit Changes and Exit.

Discard Changes and Exit
Discard Changes and Exit.

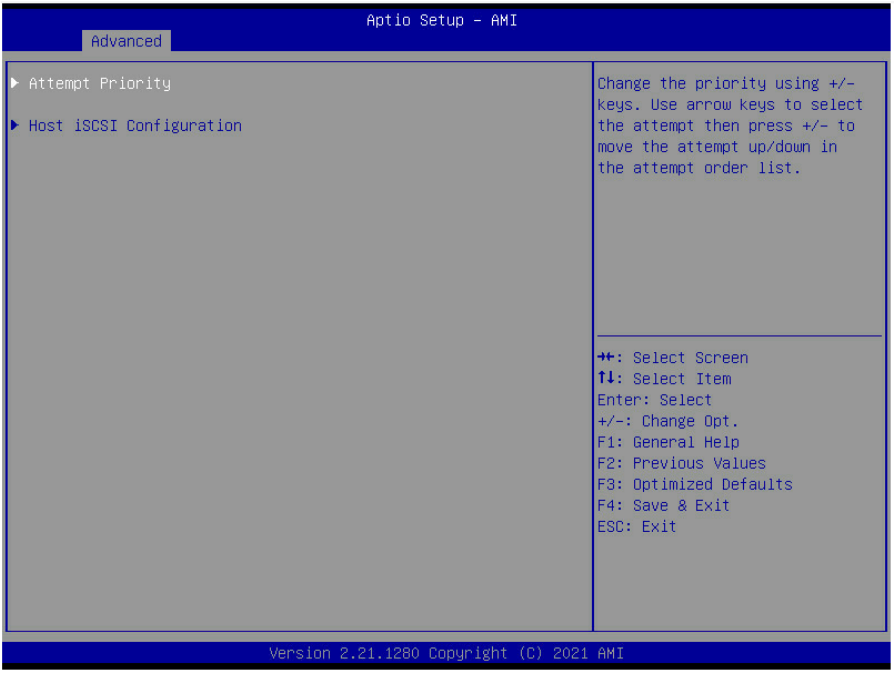
3.3.1.2 Delete Cert



FE9C6606-8849-44A3-8868-DEA3A0E0324D
GUID for CERT.

Disabled / Enabled

3.3.2 iSCSI Configuration



NOTE: Only LAN1 supports iSCSI function.

Please follow the instructions to initiate the iSCSI function.
Step 1.
Select **Advanced** → **CSM Configuration** → **Network** → [UEFI].
Step 2.
Select **Advanced** → **Network Stack Configuration** → **Network Stack** → [Enabled]
Step 3.
Save changes and reboot.

Attempt Priority
Change the priority using +/- keys. Use arrow keys to select the attempt then press +/- to move the attempt up/down in the attempt order list.

Host iSCSI Configuration
Host iSCSI Configuration.

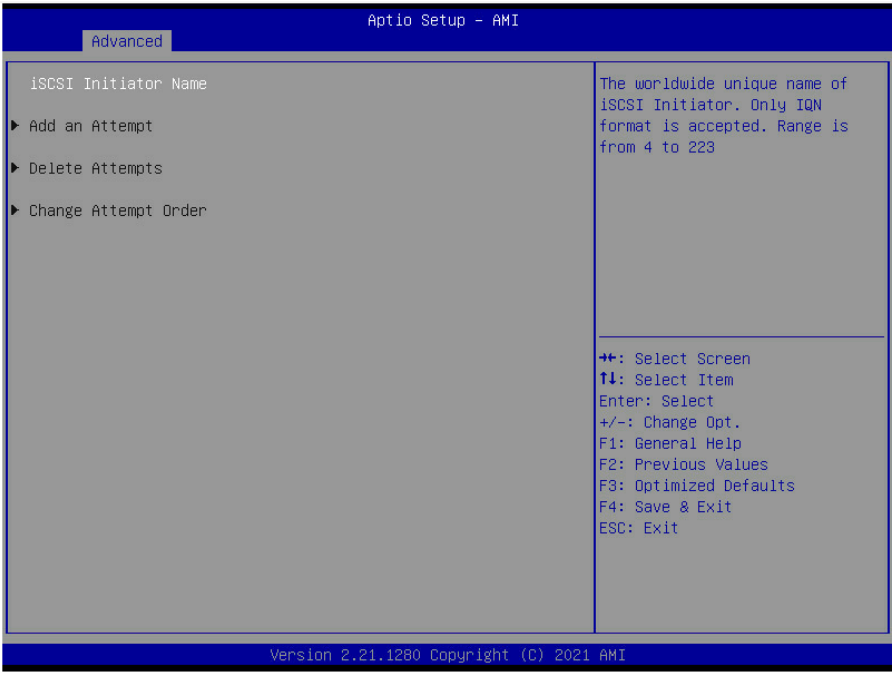
3.3.2.1 Attempt Priority

Attempt Priority
Change the priority using +/- keys. Use arrow keys to select the attempt then press +/- to move the attempt up/down in the attempt order list.

Host Attempt / Redfish Attempt

Commit Changes and Exit
Commit Changes and Exit.

3.3.2.2 Host iSCSI Configuration



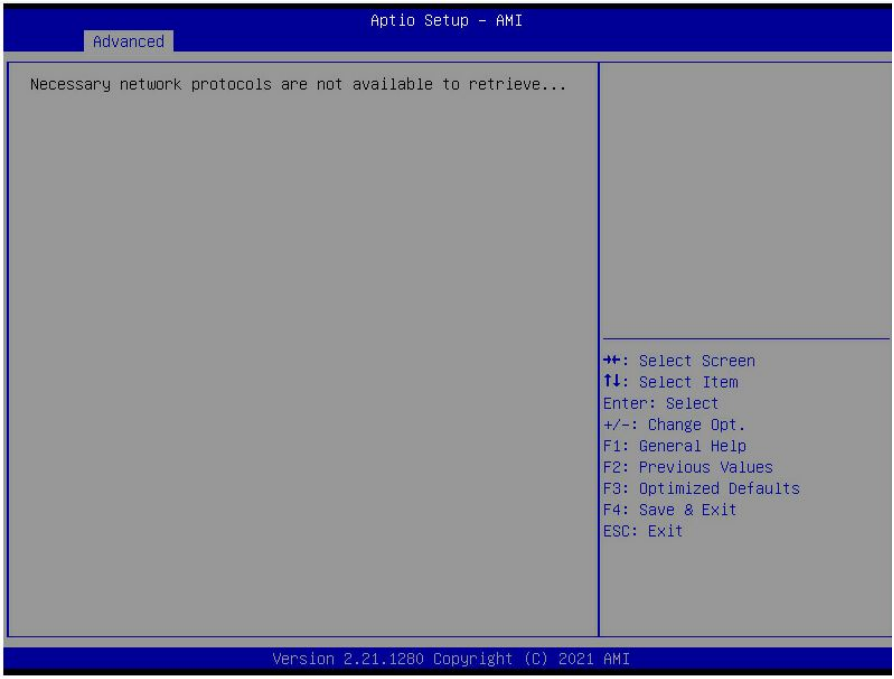
iSCSI Initiator Name
The worldwide unique name of iSCSI Initiator. Only IQN format is accepted. Enter [**iqn.xxx**]. xxx ranges from 4 to 223.

Add an Attempt
Add an attempt.

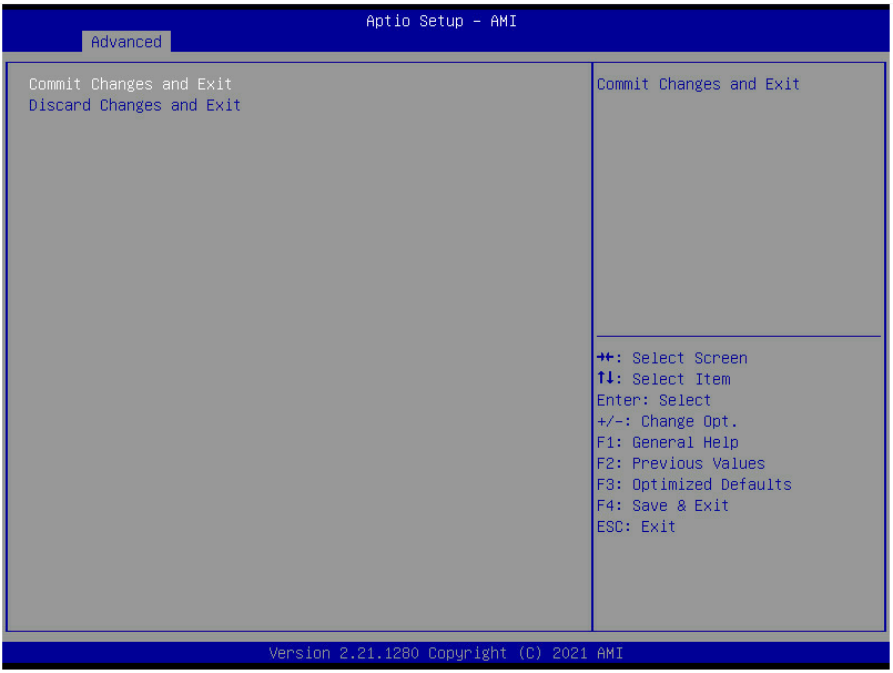
Delete Attempt
Delete one or more attempts.

Change Attempt Order
Change the priority using +/- keys. Use arrow keys to select the attempt then press +/- to move the attempt up/down in the attempt order list.

3.3.2.2.1 Add an Attempt



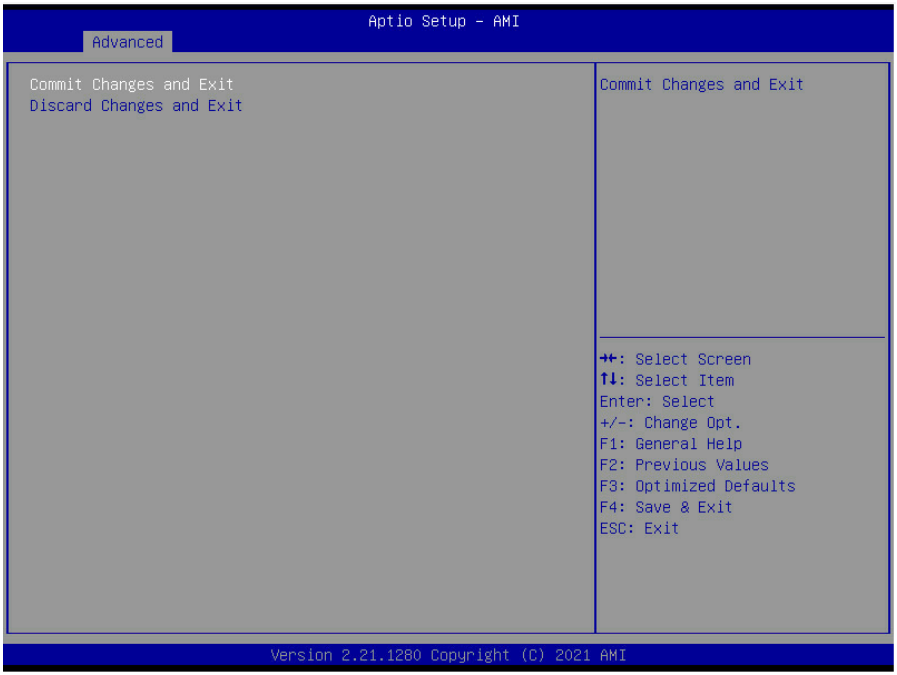
3.3.2.2.2 Delete Attempts



Commit Changes and Exit
Commit Changes and Exit.

Discard Changes and Exit
Discard Changes and Exit.

3.3.2.2.3 Change Attempt Order



Commit Changes and Exit
Commit Changes and Exit.

Discard Changes and Exit
Discard Changes and Exit.

3.3.3 Network Stack Configuration

NOTE: The BIOS will automatically read the onboard LAN controller.

Network Stack
Enable/Disable UEFI Network Stack.
Disabled / Enabled

NOTE: The following items are available when **Network Stack** is set to [Enabled].

Ipv4 PXE Support
Enable Ipv4 PXE Boot Support. If disabled IPV4 PXE boot option will not be created.
Disabled / Enabled

Ipv4 HTTP Support
Enable Ipv4 HTTP Boot Support. If disabled IPV4 HTTP boot option will not be created.
Disabled / Enabled

Ipv6 PXE Support
Enable Ipv6 PXE Boot Support. If disabled IPV6 PXE boot option will not be created.
Disabled / Enabled

Ipv6 HTTP Support
Enable Ipv6 HTTP Boot Support. If disabled IPV6 HTTP boot option will not be created.

Disabled / Enabled

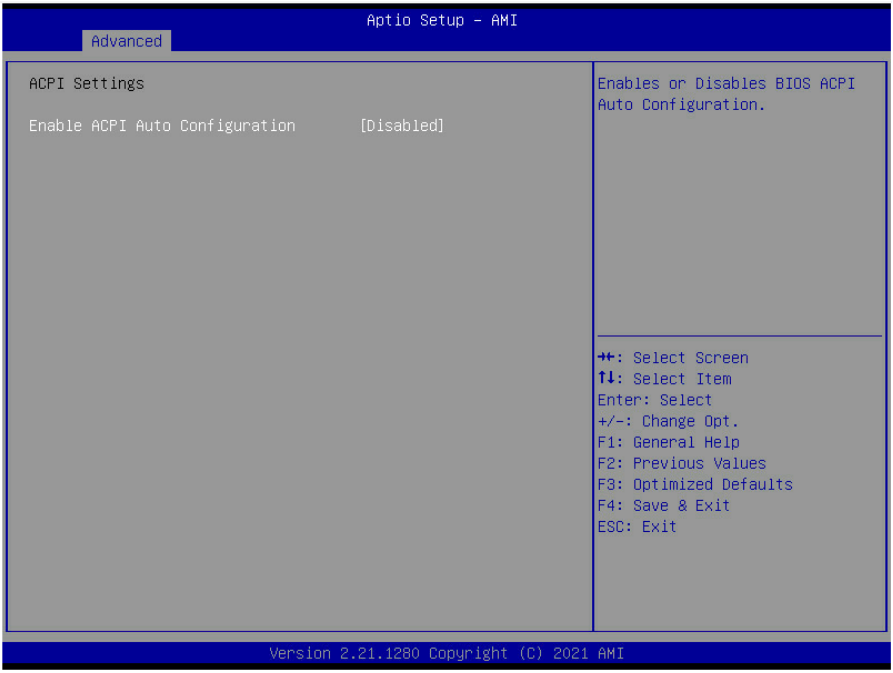
PXE boot wait time
Wait time to press ESC key to abort the PXE boot.

0

Media detect count
Number of times presence of media will be checked.

1

3.3.4 ACPI Settings



Enable ACPI Auto Configuration
Enable or disable BIOS ACPI Auto Configuration.
Disabled / Enabled

3.3.5 S5 RTC Wake Settings

Wake system from S5
Enable or disable System wake on alarm event. Select Fixed Time, system will wake on the hr:min:sec specified. Select Dynamic Time, system will wake on the current time + increase minute(s).

Disabled / Fixed Time / Dynamic Time

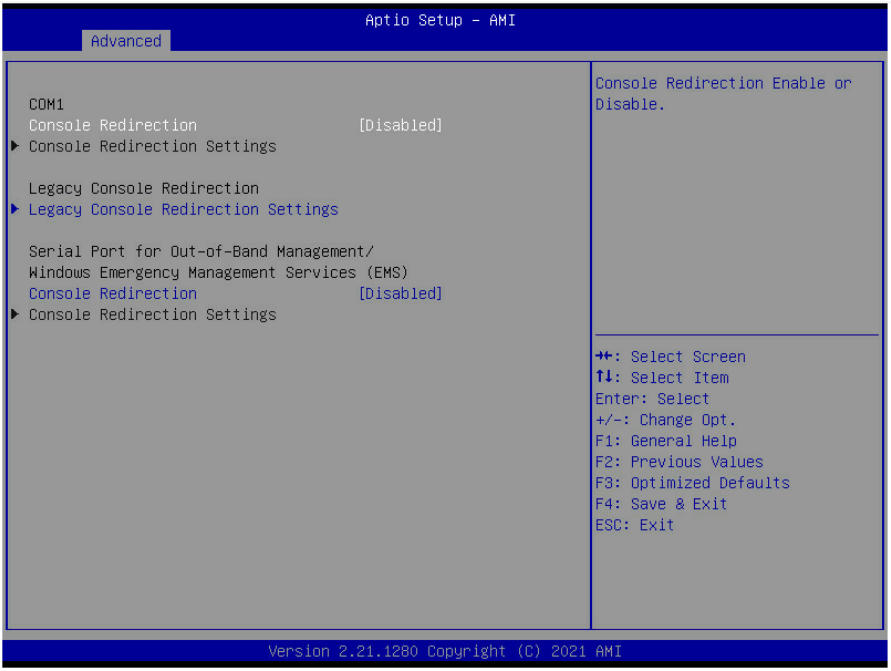
When Wake system from S5 is set to **[Fixed Time]**
Wake up hour
Select 0-23. For example enter 3 for 3am and 15 for 3pm.

Wake up minute
Select 0-59 for Minute.

Wake up second
Select 0-59 for Second.

When Wake system from S5 is set to **[Dynamic Time]**
Wake up Minute increase
1-5.

3.3.6 Serial Port Console Redirection

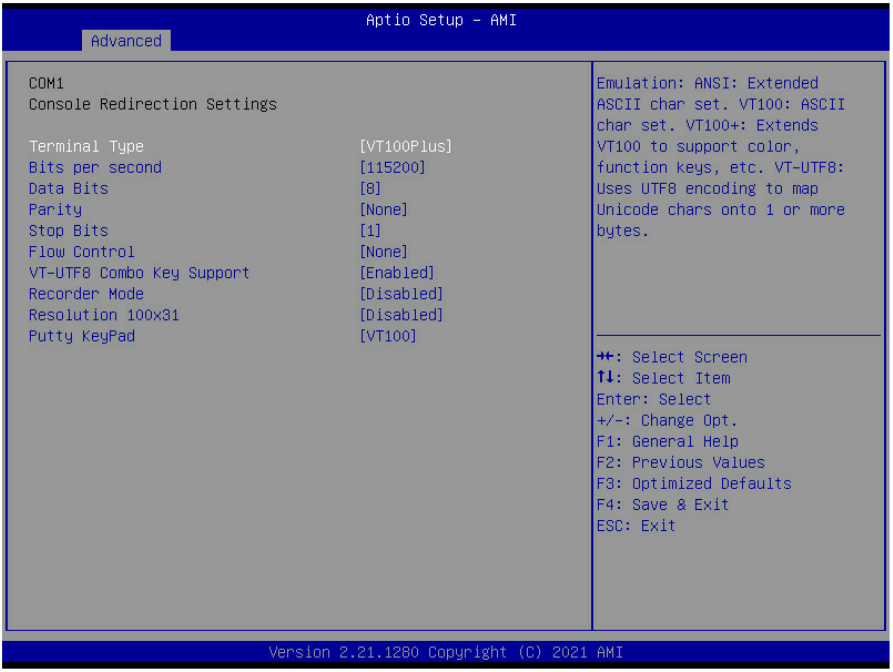


COM1 / Serial Port for Out-Of-Band Management/Windows Emergency Services (EMS)
Console Redirection
Console redirection enable or disable.
Disabled / Enabled

Legacy Console Redirection Settings
Legacy Console redirection settings.

Console Redirection Settings
The settings specify how the host computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

3.3.6.1 COM1 Console Redirection Settings



Terminal Type
Emulation: ANSI: Extended ASCII char set. VT100: ASCII char set.
VT100+: Extends VT100 to support color, function keys, etc.
VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

VT100Plus / VT100 / VT-UTF8 / ANSI

Bits per Second
Select serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

38400 / 9600 / 19200 / 57600 / **115200**

Data Bits

8 / 7

Parity
A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: parity bit is always 0. Mark and Space parity do not allow for error detection.

None / Even / Odd / Mark / Space

Stop Bits
Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

1 / 2

Flow Control
Flow Control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to restart the flow. Hardware flow control uses two wires to send start/stop signal.

None / Hardware RTS/CTS

VT-UTF8 Combo Key Support
Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

Enabled / Disabled

Recorder Mode
On this mode enabled only text will be sent. This is to capture Terminal data.

Disabled / Enabled

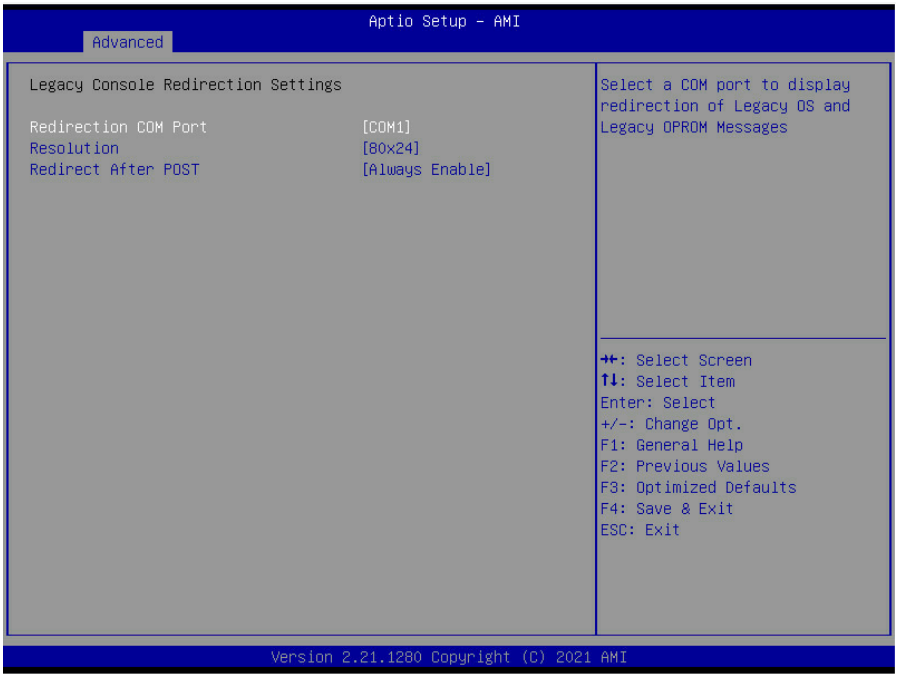
Resolution 100x31
Enable or disable extended terminal resolution.

Disabled / Enabled

Putty KeyPad
Select FunctionKey and KeyPad on Putty.

VT100 / LINUX / XTERMR6 / SCO / ESCN / VT400

3.3.6.2 Legacy Console Redirection Settings



Legacy Serial Redirection Port
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.

COM1

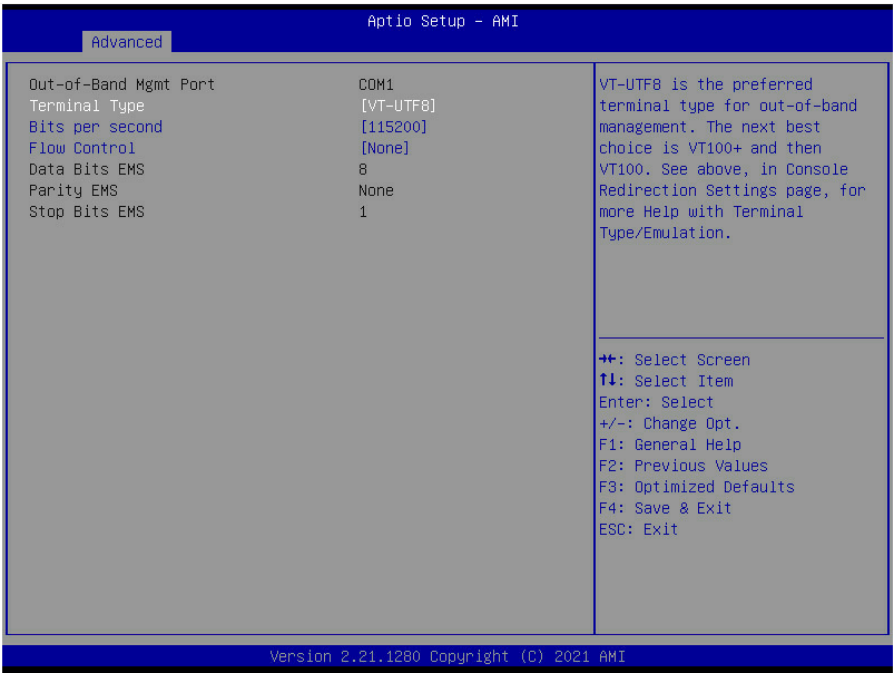
Resolution
On Legacy OS, the Number of Rows and Columns supported redirection.

80x24 / 80x25

Redirect After POST
When BootLoader is selected, then Legacy Console Redirection is disabled before booting to legacy OS, When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always Enable.

Always Enabled / BootLoader

3.3.6.3 Serial Port for Out-Of-Band Management/Windows Emergency Services (EMS) Console Redirection Settings



Out-of-Band Mgmt Port
Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

COM1

Terminal Type
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.

VT-UTF8 / VT100 / VT100Plus / ANSI

Bits per Second
Select serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

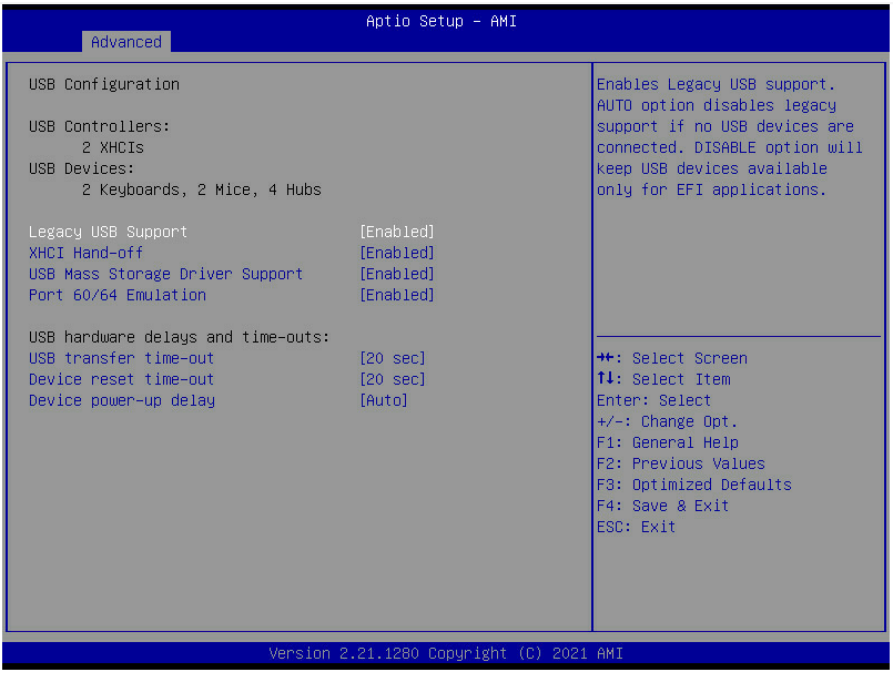
115200 / 9600 / 19200 / 57600

Flow Control
Flow Control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to restart the flow. Hardware flow control uses two wires to send start/stop signal.

None / Hardware RTS/CTS / Software Xon/Xoff

Data Bits / Parity / Stop Bits
Read only.

3.3.7 USB Configuration



Legacy USB Support
Enables USB legacy support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

Enabled / Disabled / Auto

XHCI Hand-off
This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

Enabled / Disabled

USB Mass Storage Driver Support
Enable/Disable USB Mass Storage Driver Support.

Enabled / Disabled

Port 60/64 Emulation
Enables I/O Port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

Enabled / Disabled

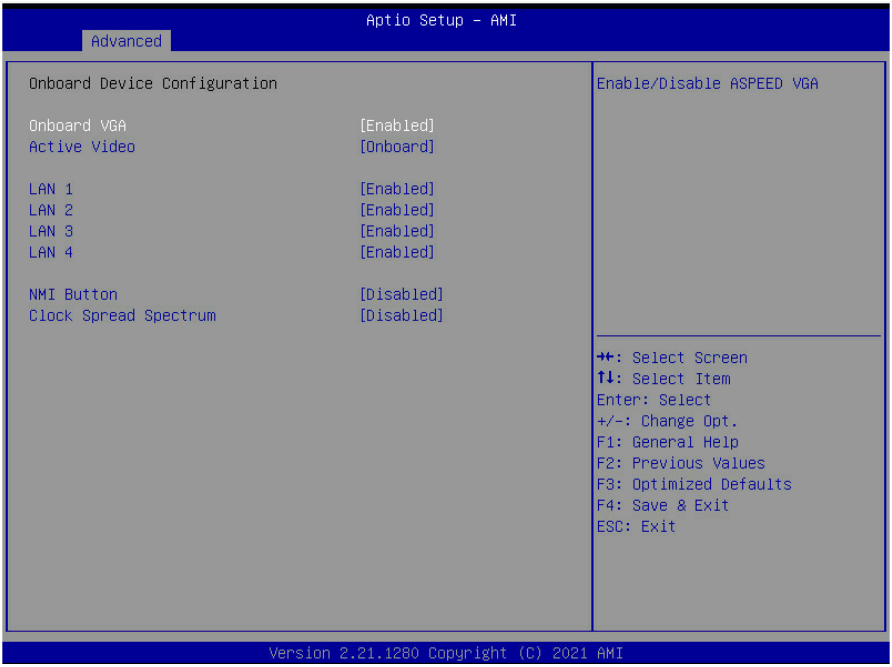
USB transfer time-out
The time-out value for Control, Bulk and Interrupt transfers.
1 sec / 5 sec / 10 sec / **20 sec**

Device reset time-out
USB mass storage device Start Unit command time-out.
10 sec / **20 sec** / 30 sec / 40 sec

Device power-up delay
Maximum time the device will take before it properly reports itself to the Host Controller. AUTO uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.
Auto / Manual
NOTE: The following item will appear when **Device power-up delay** is set to [Manual].

Device power-up delay in seconds
Delay range is 1…40 seconds, in one second increments.
5

3.3.8 Onboard Device Configuration



Onboard VGA
Enable/Disable ASPEED VGA.
Enabled / Disabled

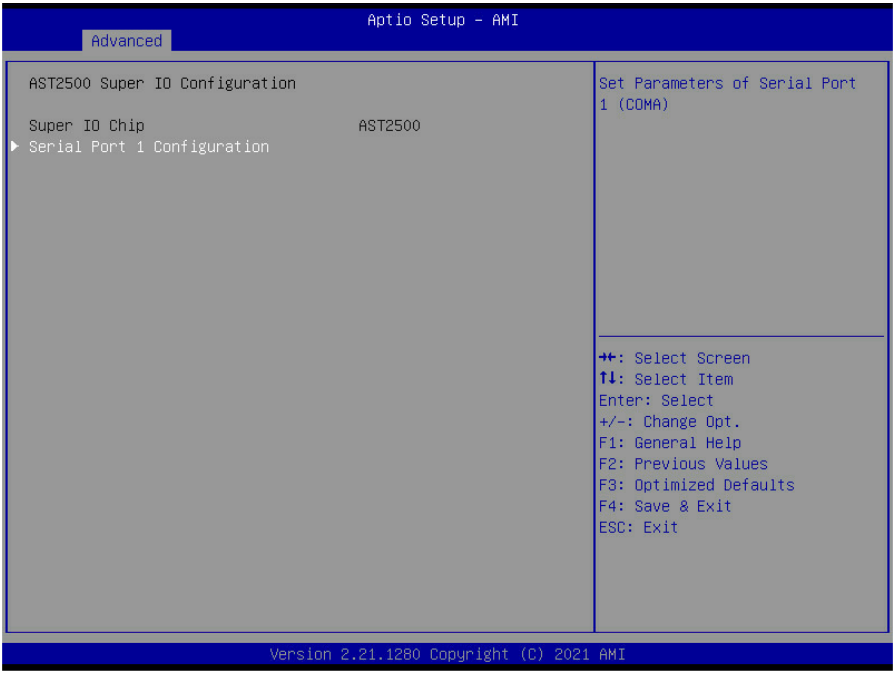
Active Video
Select between onboard or external VGA support.
Onboard / External

LAN1~LAN4
LAN Enable/Disable control function.
Enabled / Disabled

NMI Button
Enable or Disable NMI button.
Enabled / **Disabled**

Clock Spread Spectrum
Enable/Disable Clock Spread Spectrum.
Enabled / **Disabled**

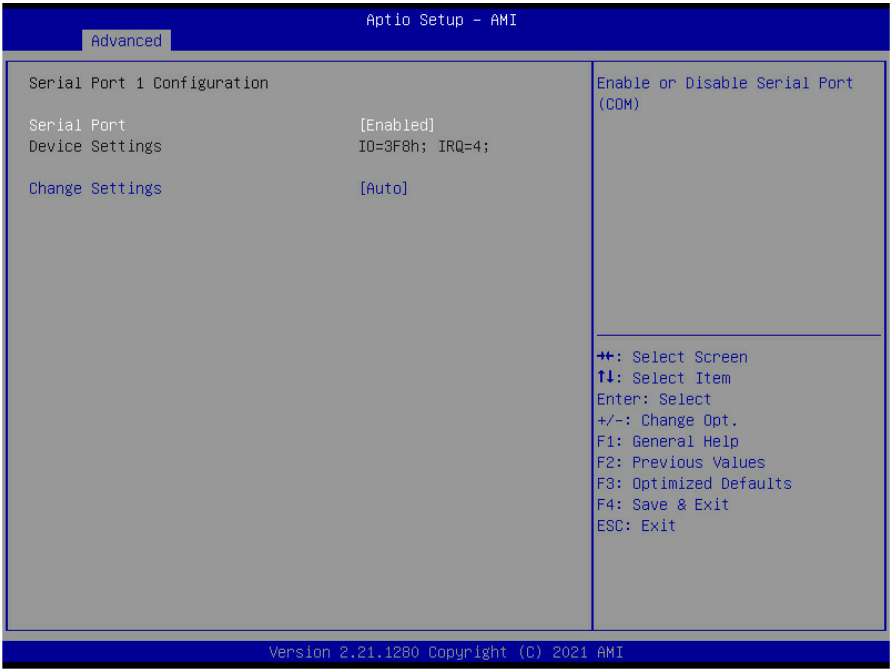
3.3.9 AST2500 Super IO Configuration



Super IO Chip
Read only.

Serial Port 1 Configuration
Set Parameters of Serial Port 1 (COMA).

3.3.9.1 Serial Port 1 Configuration

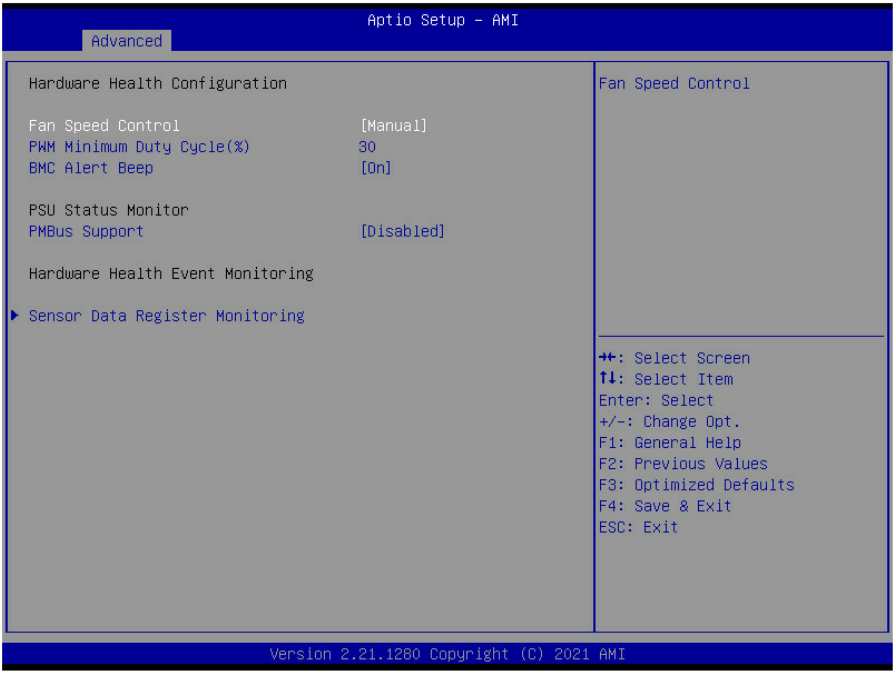


Serial Port
Enable or disable Serial Port (COM).
Enabled / Disabled

Device Settings
Read only.

Change Settings
Select an optimal setting for Super IO Device.
Auto / IO=3F8h; IRQ=4;
/ IO=3F8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
/ IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
/ IO=3E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
/ IO=2E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

3.3.10 Hardware Health Configuration



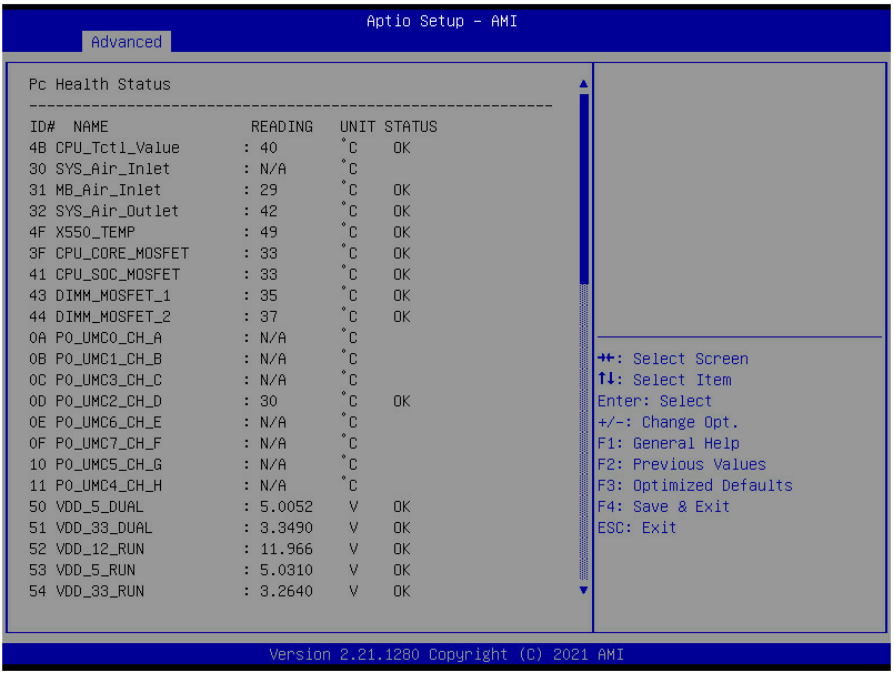
Fan Speed Control
Fan Speed Control.
Manual / Full Speed
NOTE: Change the “Fan Speed Control” BIOS setting from [Manual] to [Full Speed] when installing the Nvidia GeForce / Quardro GPU and any VGA card.

PWM Minimal Duty Cycle
PWM Minimal Duty Cycle (%).
30
NOTE: This item is available when **Fan Speed Control** is set to [Manual].

BMC Alert Beep
Enable/Disable BMC Alert Beep.
On / Off

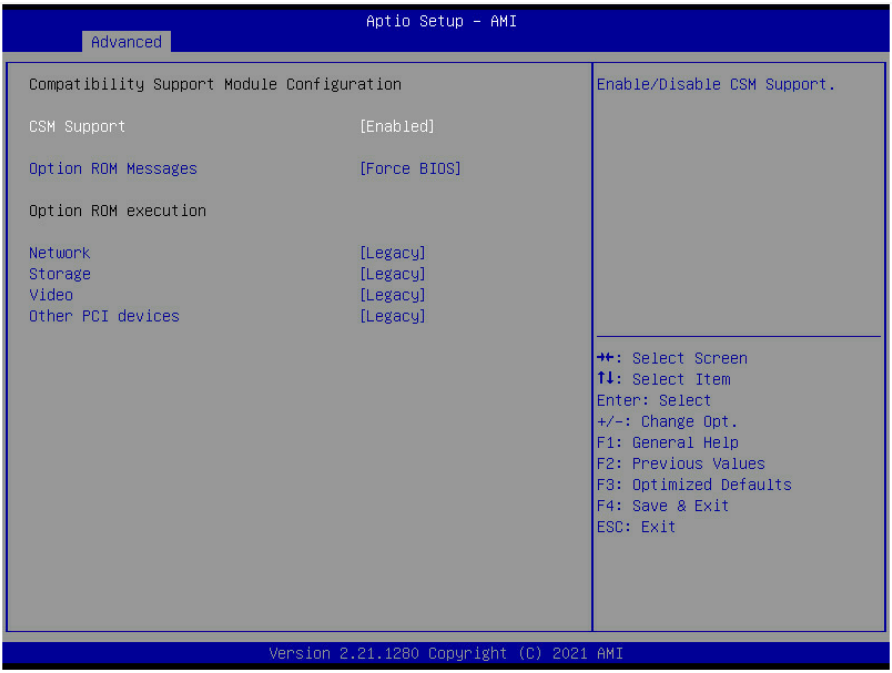
PMBus support
PSU Status Monitor support or not.
Disabled / Enabled

3.3.10.1 Sensor Data Register Monitoring



NOTE: SDR can not be modified. Read only.

3.3.11 CSM Configuration



CSM support
Enable/Disable CSM Support
Enabled / Disabled

Option ROM Messages
Set display mode for Option ROM
Force BIOS / Keep Current

Network
Controls the execution of UEFI and Legacy PXE OpROM
UEFI / **Legacy**

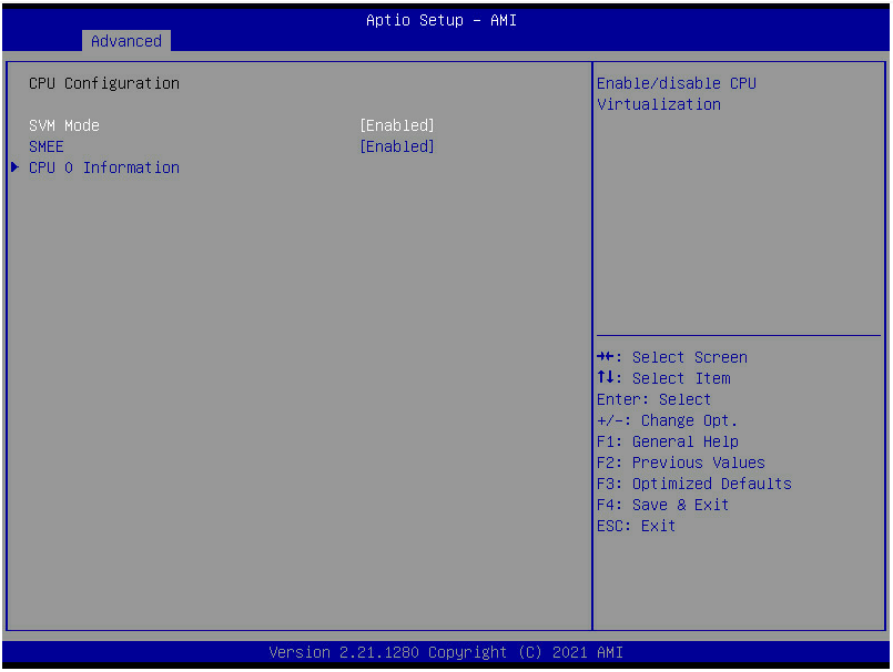
Storage
Controls the execution of UEFI and Legacy Storage OpROM
UEFI / **Legacy**

Video
Controls the execution of UEFI and Legacy Video OpROM
UEFI / **Legacy**

Other PCI devices
Determines OpRom execution policy for devices other than network, storage, or video

UEFI / **Legacy**

3.3.12 CPU Configuration

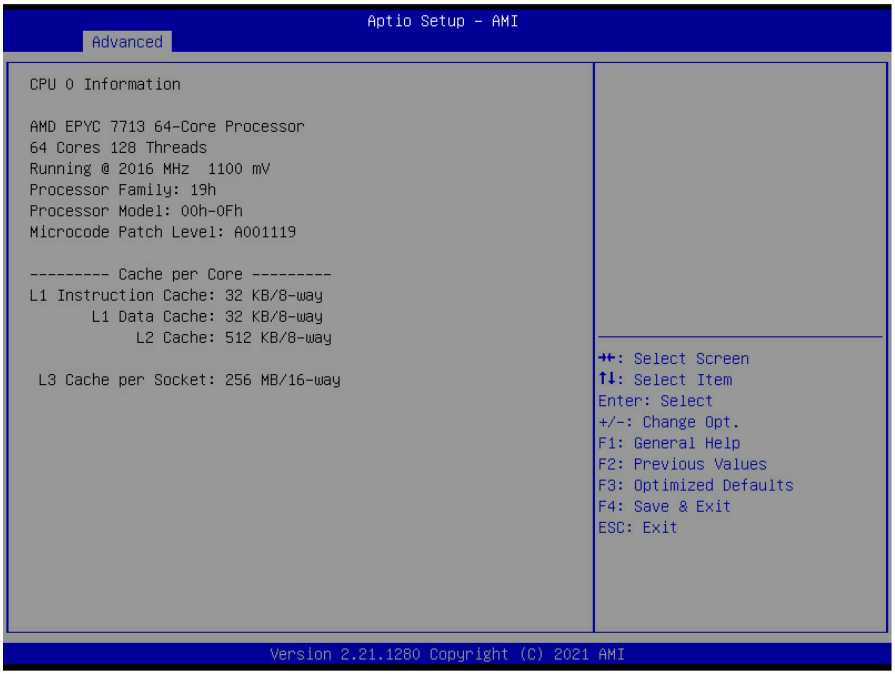


SVM Mode
Enable/disable CPU Virtualization.
Disabled / **Enabled**

SMEE
Control secure memory encryption enable.
Disabled / **Enabled**

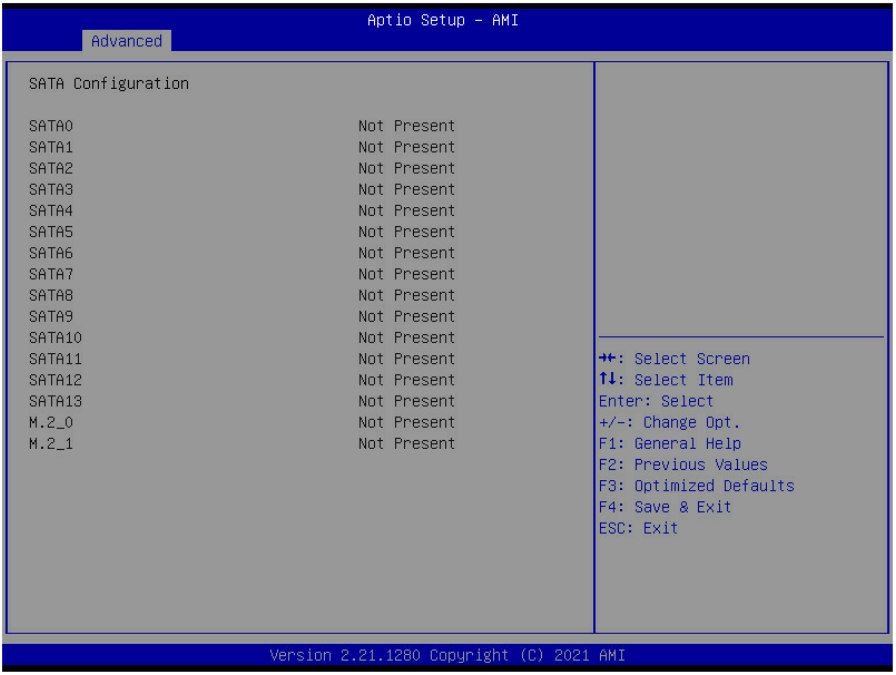
CPU 0 Information
View Information related to CPU 0.

3.3.12.1 CPU 0 Information



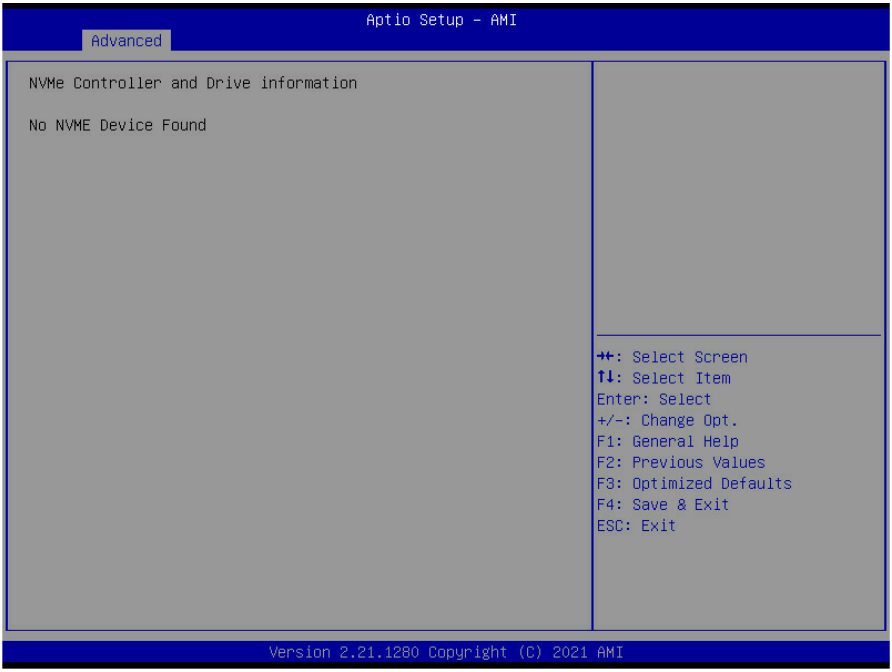
Read only.

3.3.13 SATA Configuration



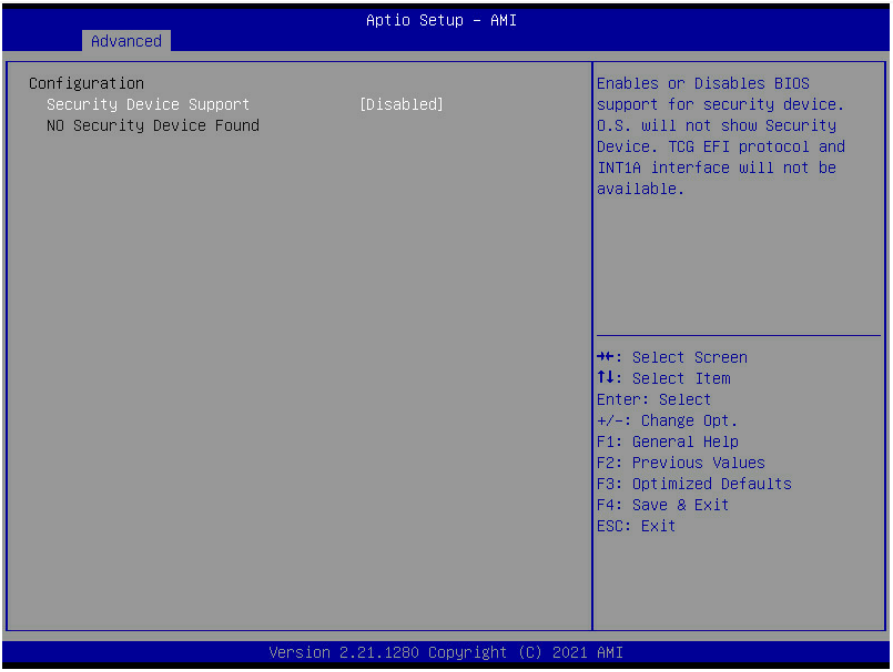
Read only.

3.3.14 NVMe Configuration



Read only.

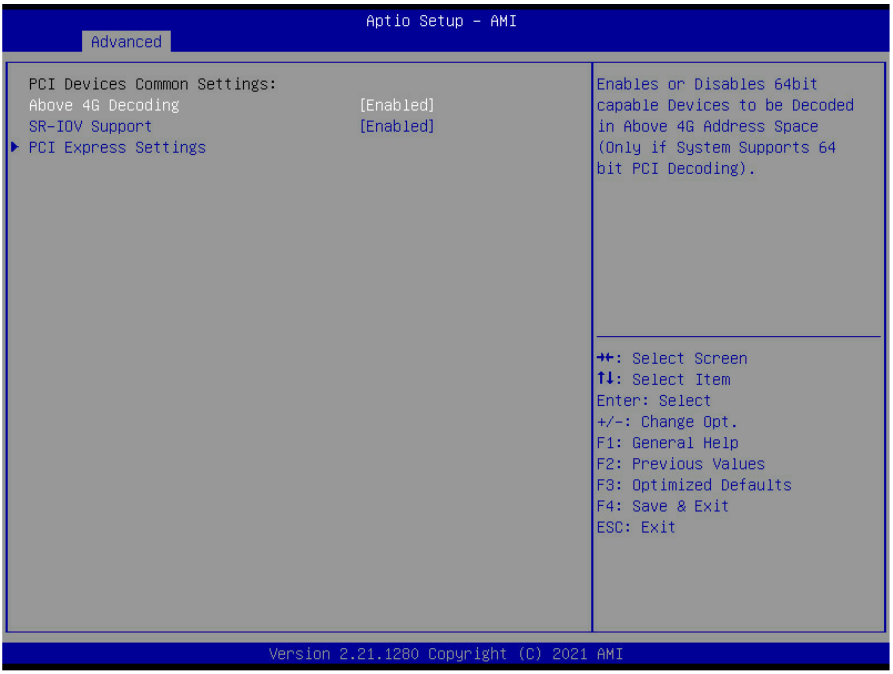
3.3.15 Trusted Computing



Security Device Support
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

Enabled / **Disabled**

3.3.16 PCI Subsystem Settings



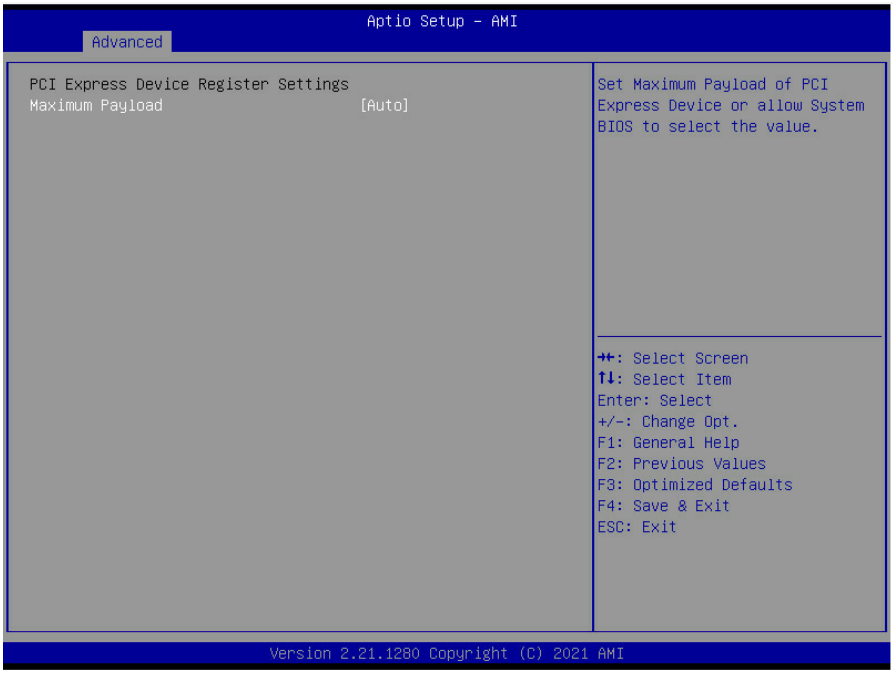
Above 4G Decoding
Enables or Disables 64bit capable Devices to be Decoded in Above 4G Address Space (Only if System Supports 64 bit PCI Decoding).

Enabled / Disabled

SR-IOV Support
If system has SR-IOV capable PCIe Devices, this option Enables or Disables Single Root IO Virtualization Support.

Enabled / Disabled

3.3.16.1 PCI Express Settings



Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Auto / 128 Bytes / 256 Bytes / 512 Bytes / 1024 Bytes / 2048 Bytes / 4096 Bytes

3.3.17 Option ROM Dispatch Policy

LAN1 (for S8030GM4NE-2T SKU only)
Enable or Disable LAN1 Option ROM.
Enabled / **Disabled**

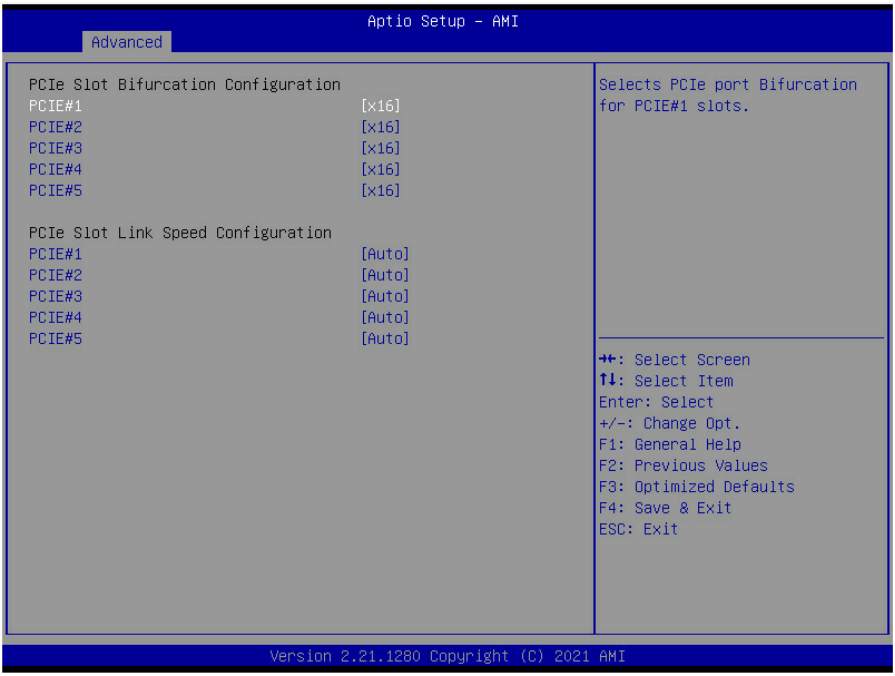
LAN2 (for S8030GM4NE-2T SKU only)
Enable or Disable LAN2 Option ROM.
Enabled / **Disabled**

LAN3
Enable or Disable LAN3 Option ROM.
Enabled / **Disabled**

LAN4
Enable or Disable LAN4 Option ROM.
Enabled / **Disabled**

PCIE#1~5
Enable or Disable Option ROM execution for selected Slot.
Enabled / Disabled

3.3.18 PCIE Slot Configuration



PCIe Slot Bifurcation Configuration

PCIE#1~PCIE#5

Selects PCIe port Bifurcation for PCIE#1~PCIE#5 slot.

x16 / x8x8 / x4x4x4x4

PCIe Slot Link Speed Configuration

PCIE#1~PCIE#5

Maximum Link Speed for PCIE#1~PCIE#5 slot.

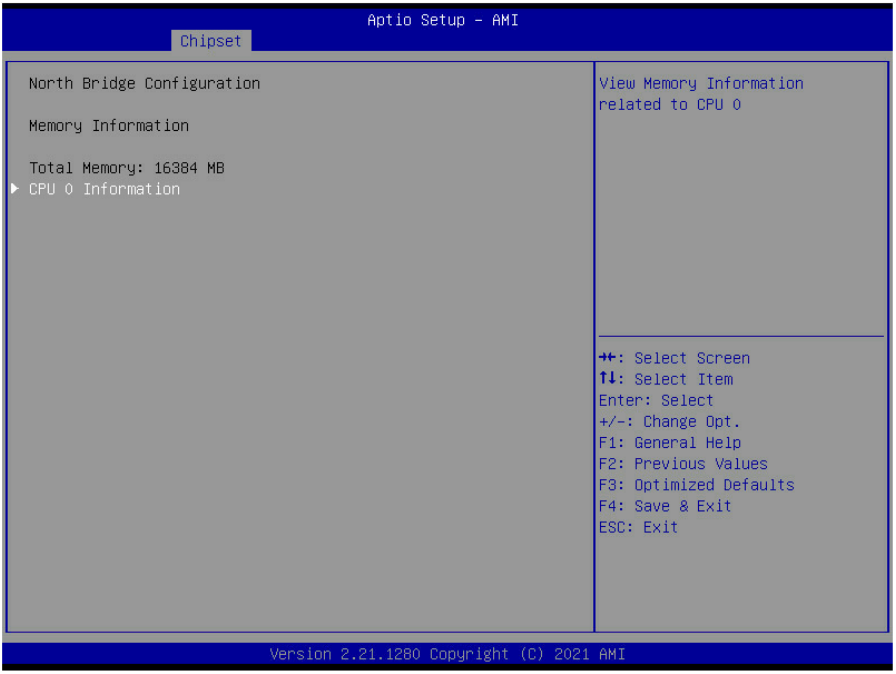
Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8GT/s) / Gen4 (16GT/s)

3.4 Chipset Menu

PCIe Compliance Mode
PCIe Link Compliance Mode.
Disabled / Enabled

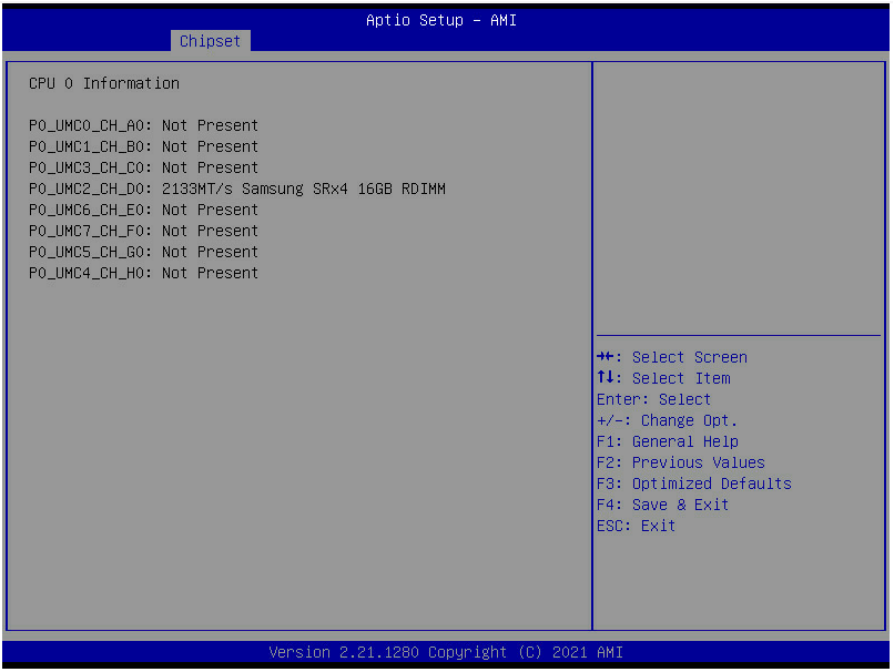
North Bridge
North Bridge Parameters

3.4.1 North Bridge Configuration



Socket 0 Configuration
View Information related to Socket 0.

3.4.1.1 Socket 0 Information



Read only.

3.5 AMD CBS

CPU Common Options
CPU Common Options.

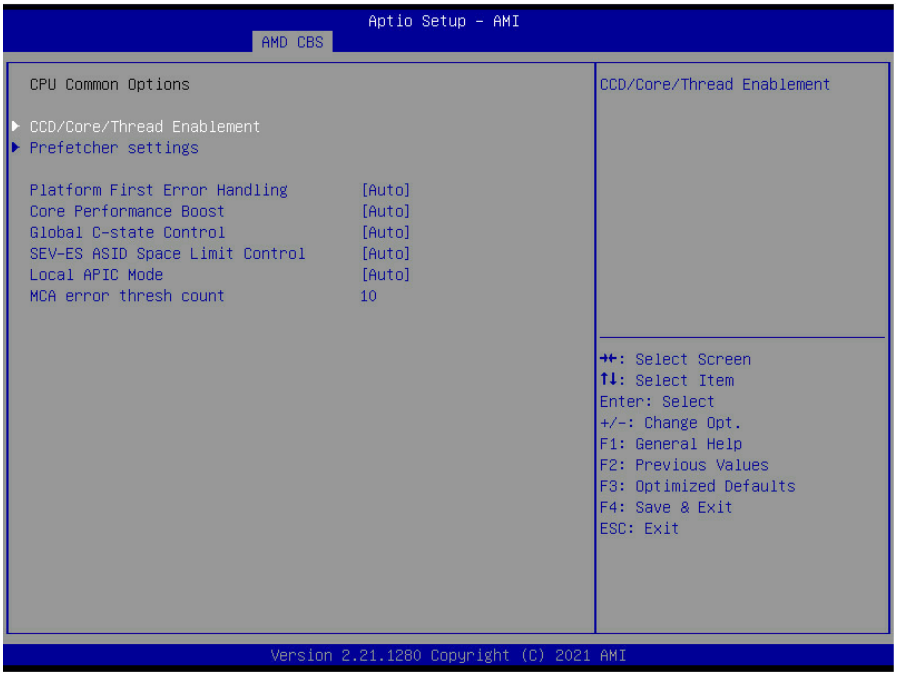
DF Common Options
DF Common Options.

UMC Common Options
UMC Common Options.

NBIO Common Options
NBIO Common Options.

FCH Common Options
FCH Common Options.

3.5.1 CPU Common Options



CCD/Core/Thread Enablement
CCD/Core/Thread Enablement.

Prefetcher Settings
Prefetcher Settings.

Platform First Error Handling
Enable/disable PFEH, cloak individual banks, and mask deferred error interrupts from each bank.

Enabled / Disabled / **Auto**

Core Performance Boost
Disable CPB.

Disabled / **Auto**

Global C-state Control
Controls IO based C-state generation and DF C-states.

Disabled / Enabled / **Auto**

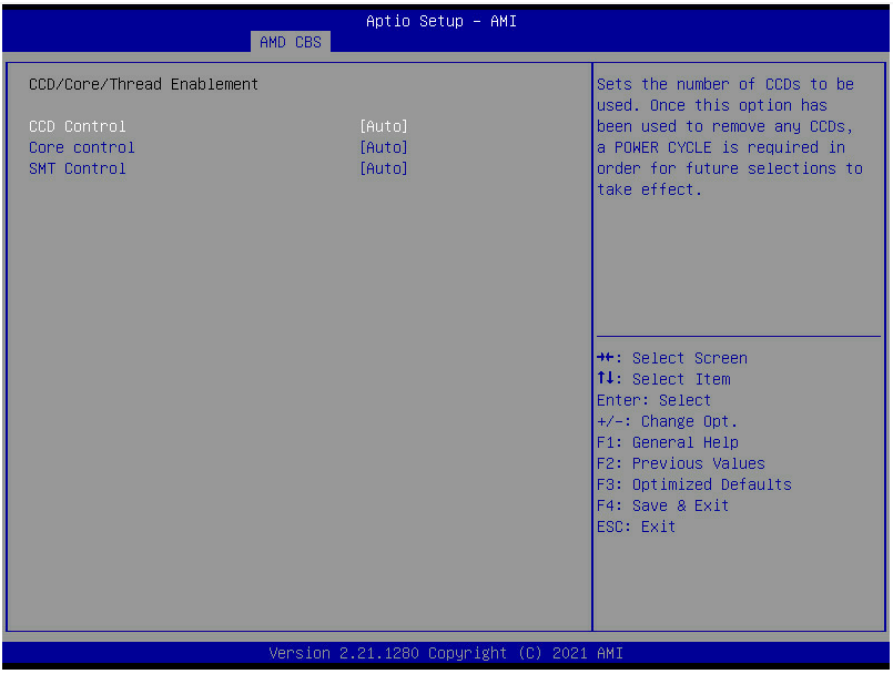
SEV-ES ASID Space Limit Control
SEV-ES ASID Space Limit Control.
Auto / Manual
NOTE: SEV-ES ASID Space Limit is available when **SEV-ES ASID Space Limit Control** is set to [Manual].

SEV-ES ASID Space Limit
ASIDs from SEV-ES ASID Space Limit to (SEV ASID Count +1) can only be used with SEV VMs. If this field is set to (SEV ASID Count +1), all ASIDs are force to be SEV-ES ASIDs. Hence, the valid values for this field is 1 --- (SEV ASID Count +1)
1

Local APIC Mode
Local APIC Mode.
xAPIC / x2APIC / **Auto**

MCA error thresh count
Default is 10, and the threshold range is from 1 to 4095.
10

3.5.1.1 CCD/Core/Thread Enablement



CCD control
Sets the number of CCDs to be used. Once this option has been used to remove any CCDs, a POWER CYCLE is required in order for future selections to take effect.

Auto / 2 CCDs / 3 CCDs / 4 CCDs / 6 CCDs

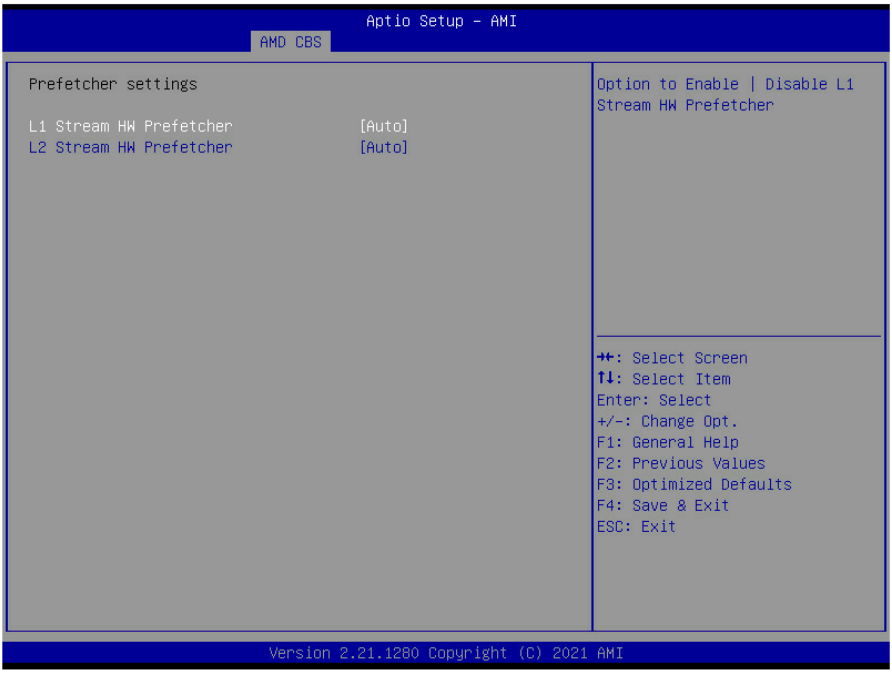
Core control
Sets the number of cores to be used. Once this option has been used to remove any cores, a POWER CYCLE is required in order for future selections to take effect.

TWO (1+1) / FOUR (2+2) / SIX (3+3) / **Auto**

SMT control
Can be used to disable symmetric multithreading. To re-enable SMT, a POWER CYCLE is needed after selecting the 'Auto' option.

Disabled / **Auto**

3.5.1.2 Prefetcher Settings



L1 Stream HW Prefetcher
Option to Enable / Disable L1 Stream HW Prefetcher.
Enabled / Disabled / **Auto**

L2 Stream HW Prefetcher
Option to Enable / Disable L2 Stream HW Prefetcher.
Enabled / Disabled / **Auto**

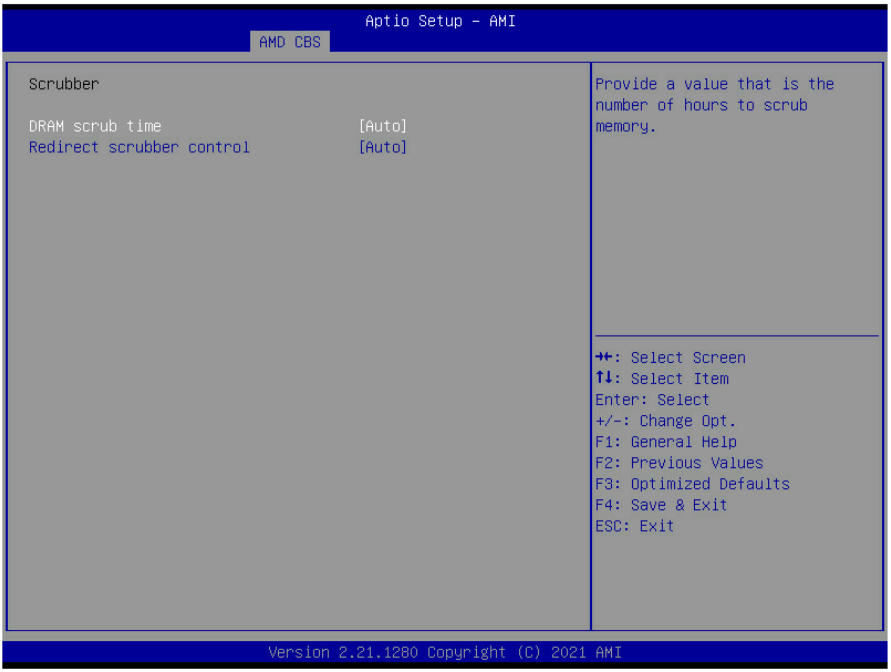
3.5.2 DF Common Options

Scrubber
Scrubber.

Memory Addressing
Memory Addressing.

ACPI
ACPI.

3.5.2.1 Scrubber



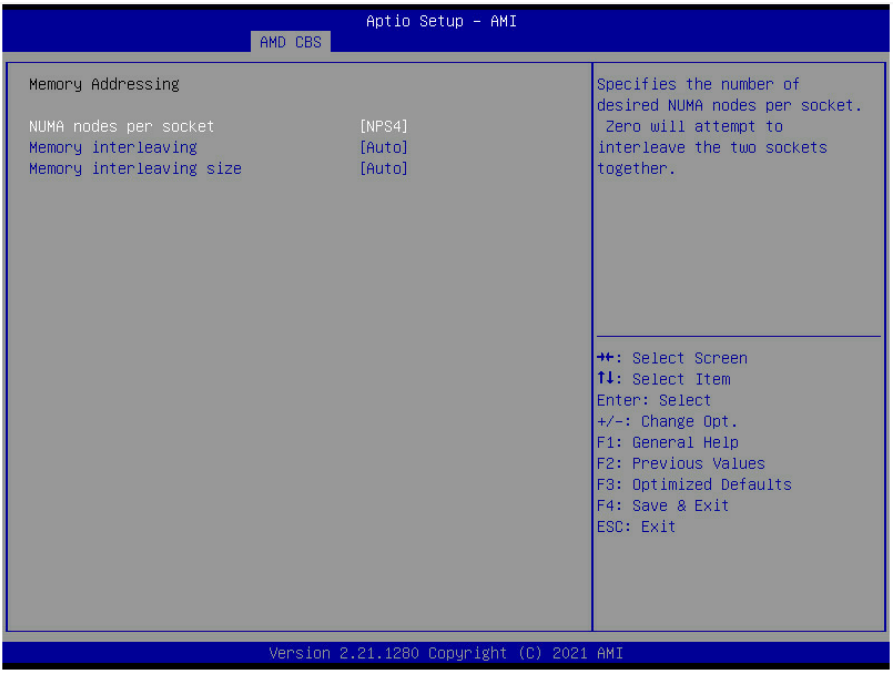
DRAM scrub time
Provide a value that is the number of hours to scrub memory.

Disabled / 1 hour / 4 hours / 8 hours / 16 hours / 24 hours / 48 hours / **Auto**

Redirect scrubber control
Redirect scrubber control.

Disabled / Enabled / **Auto**

3.5.2.2 Memory Addressing



NUMA nodes per socket
Specifies the number of desired NUMA nodes per socket. Zero will attempt to interleave the two sockets together.

NPS0 / NPS1 / NPS2 / **NPS4**

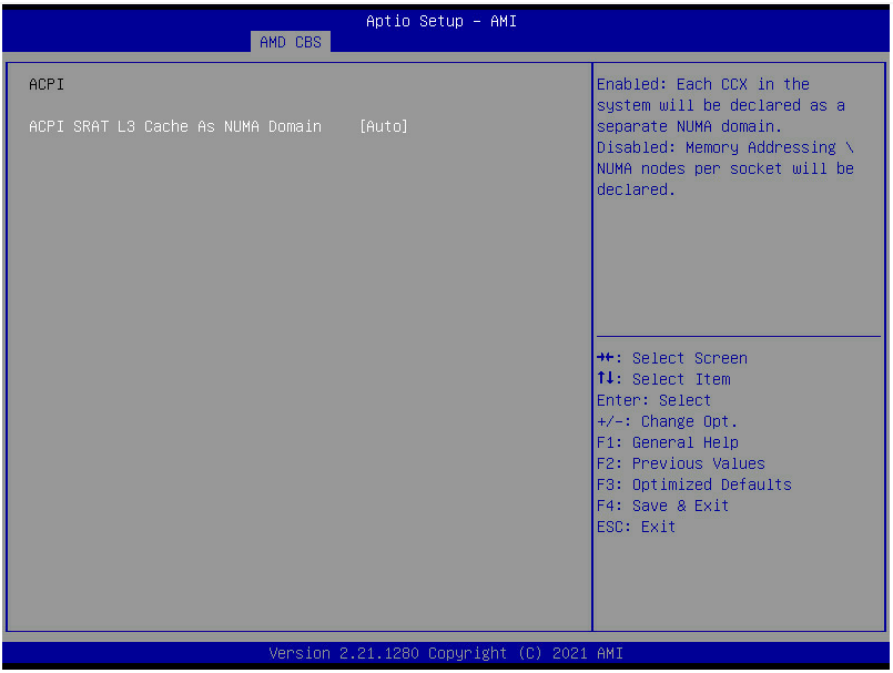
Memory interleaving
Allows for disabling memory interleaving. Note that NUMA nodes per socket will be honored regardless of this setting.

Disabled / **Auto**

Memory interleaving size
Controls the memory interleaving size. The valid value are AUTO, 256 bytes, 512 bytes, 1 Kbytes or 2Kbytes. This determines the starting address of the interleave (bit 8, 9, 10 or 11).

256 Bytes / 512 Bytes / 1 KB / 2 KB / **Auto**

3.5.2.3 ACPI



ACPI SRAT L3 Cache As NUMA Domain
Enabled: Each CCX in the system will be declared as a separate NUMA domain.
Disabled: Memory Addressing \ NUMA nodes per socket will be declared.
Disabled / Enabled / **Auto**

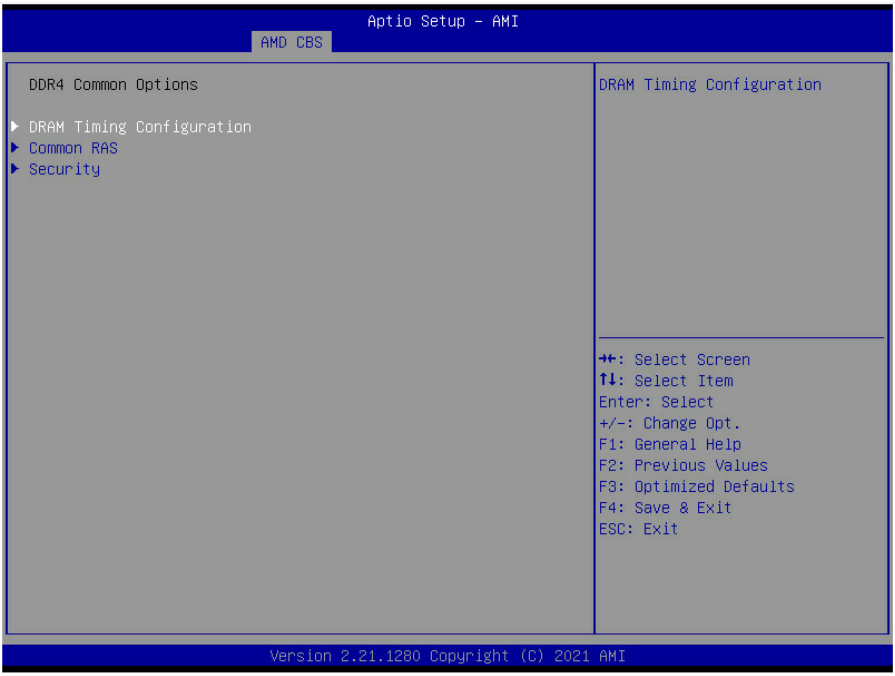
3.5.3 UMC Common Options

DDR4 Common Options
DDR4 Common Options.

DRAM Memory Mapping
DRAM Memory Mapping.

NVDIMM
NVDIMM.

3.5.3.1 DDR4 Common Options

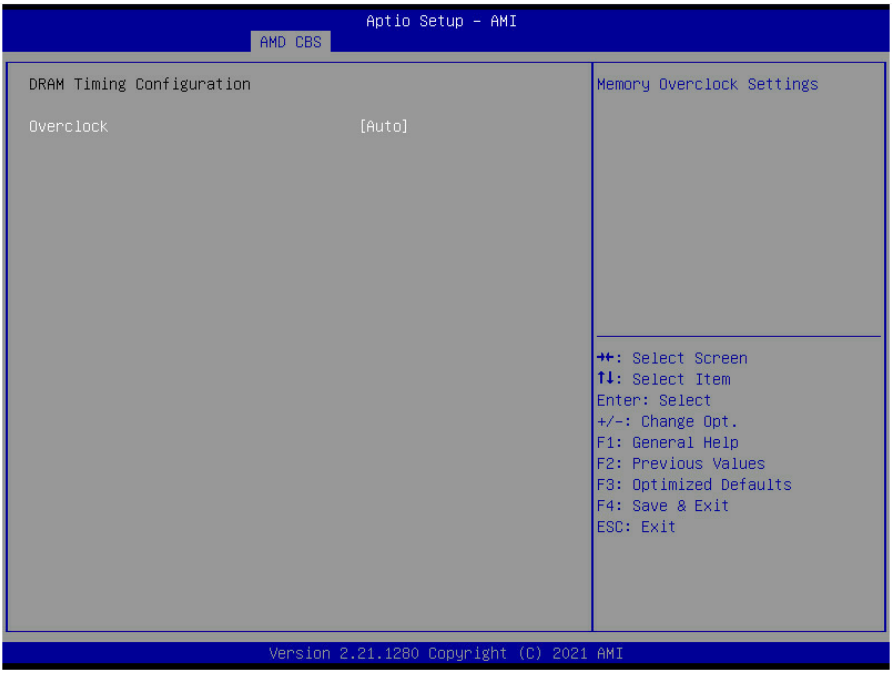


DRAM Timing Configuration
DRAM Timing Configuration.

Common RAS
Common RAS.

Security
Security.

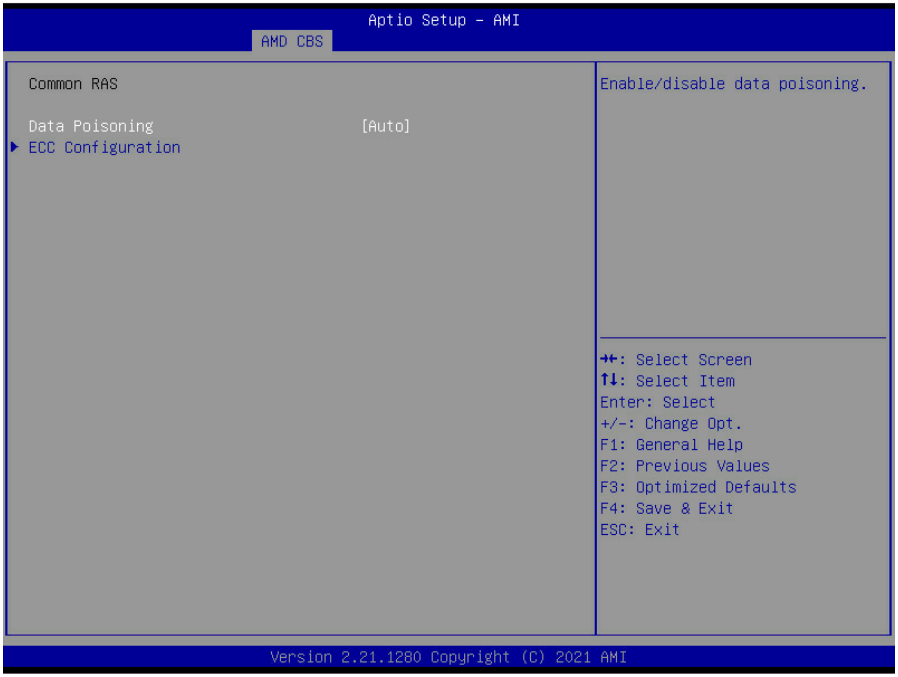
3.5.3.1.1 DRAM Timing Configuration



Overclock
Memory Overclock Settings.
Enabled / **Auto**
NOTE: The following item is available when **Overclock** is set to [Enabled].

Memory Clock Speed
Specifies the memory clock frequency.
2666MT/s / 2933MT/s / 3200MT/s / **Auto**

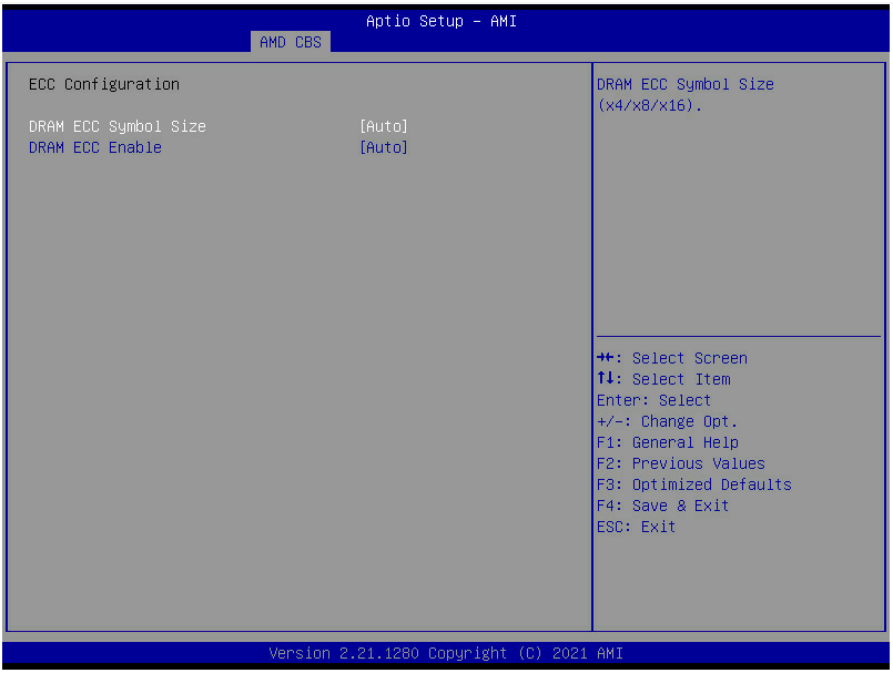
3.5.3.1.2 Common RAS



Data Poisoning
Enable/disable data poisoning:
Enabled / Disabled / **Auto**

ECC Configuration
ECC Configuration.

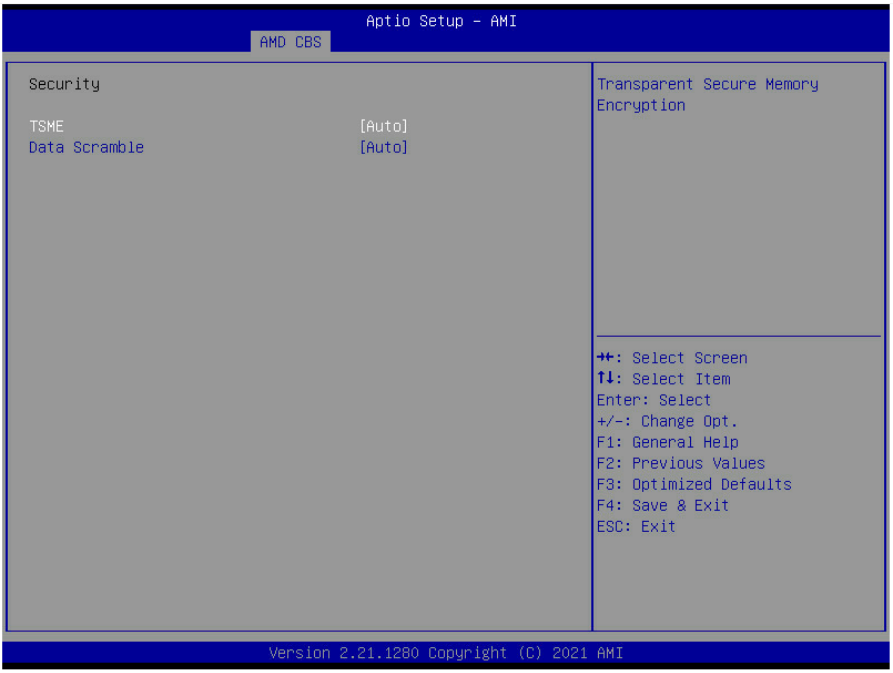
3.5.3.1.2.1 ECC Configuration



DRAM ECC Symbol Size
DRAM ECC Symbol Size (x4/x8/x16).
x4 / x8 / x16 / **Auto**

DRAM ECC Enable
Use this option to enable/disable DRAM ECC. Auto will set ECC to enable.
Enabled / Disabled / **Auto**

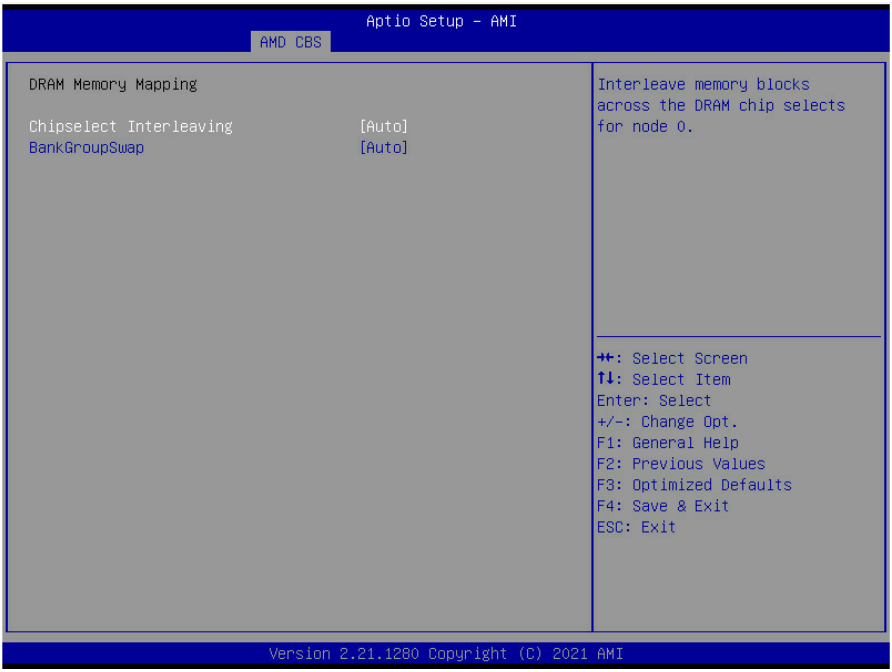
3.5.3.1.3 Security



TSME
Transparent Secure Memory Encryption.
Enabled / Disabled / **Auto**

Data Scramble
Data scrambling.
Enabled / Disabled / **Auto**

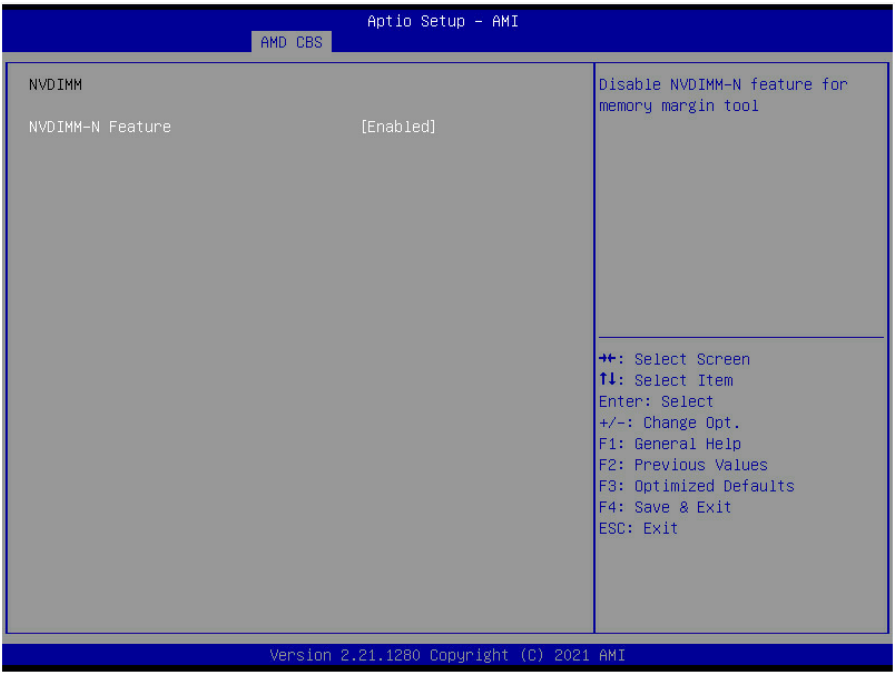
3.5.3.2 DRAM Memory Mapping



Chipselect Interleaving
Interleave memory blocks across the DRAM chip selects for node 0.
Disabled / **Auto**

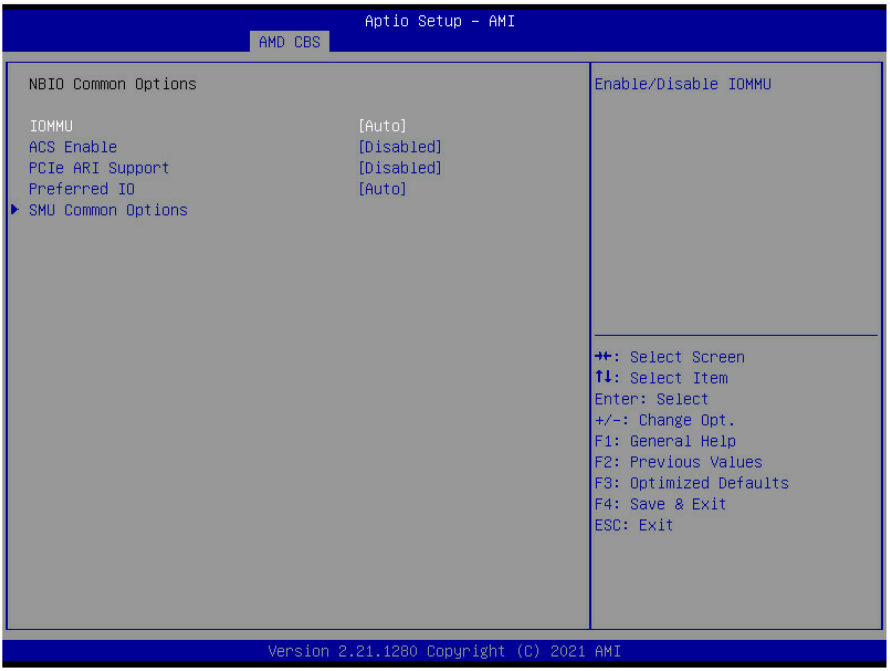
BankGroupSwap
Bank Group Swap settings.
Enabled / Disabled / **Auto**

3.5.3.3 NVDIMM



NVDIMM-N Feature
Disable NVDIMM-N feature for memory margin tool.
Disabled / **Enabled**

3.5.4 NBIO Common Options



IOMMU
Enable/Disable IOMMU.
Enabled / Disabled / **Auto**

ACS Enable
AER must be enabled for ACS enable to work.
Enabled / **Disabled** / Auto

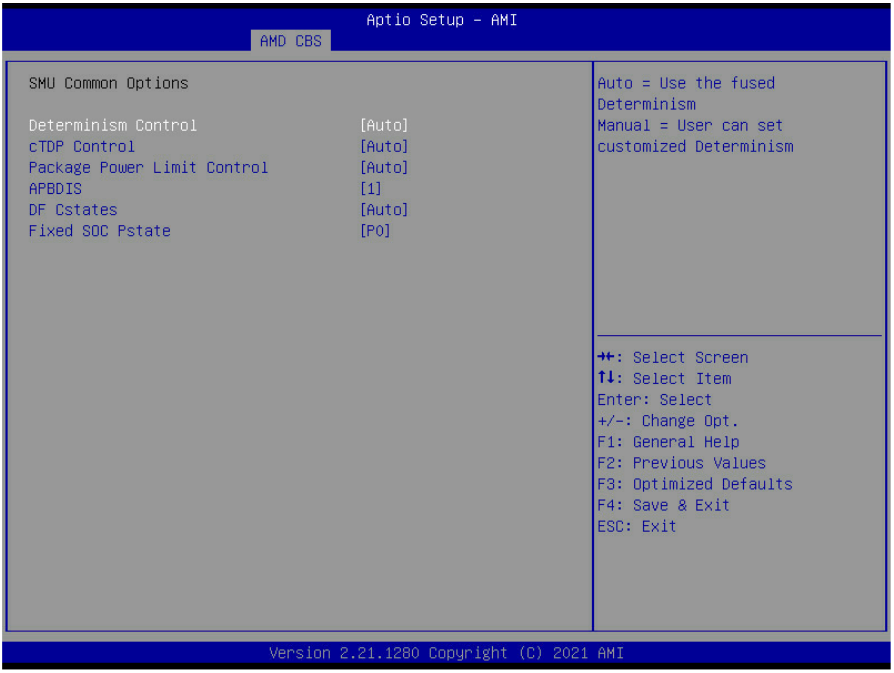
PCIe ARI Support
Enables Alternative Routing-ID Interpretation.
Enabled / **Disabled** / Auto

Preferred IO
Preferred IO Select Type.
Manual: Bus Number manually
Auto: Default
Manual / **Auto**
NOTE: The following item is available when **Preferred IO** is set to [Manual].

Preferred IO Bus
Preferred IO Bus Number 0x0-0xFF: Bus Number
0

SMU Common Options
SMU Common Options.

3.5.4.1 SMU Common Options



Determinism Control
Auto = Use the fused Determinism
Manual = User can set customized Determinism
Manual / **Auto**
NOTE: Determinism Slider is available when **Determinism Control** is set to [Manual].

Determinism Slider
Auto = Use default performance determinism settings
Power
Performance
Auto / Power / Performance

cTDP Control
Auto = Use the fused TDP
Manual = User can set customized TDP
Manual / **Auto**
NOTE: cTDP is available when **cTDP Control** is set to [Manual].

cTDP
cTDP [W] 0 = Invalid value.
0

Package Power Limit Control
Auto = Use the fused PPT
Manual = User can set customized PPT
PPT will be used as the ACIS power limit
Manual / **Auto**
NOTE: Package Power Limit is available when **Package Power Limit Control** is set to [Manual].

Package Power Limit
Package Power Limit (PPT) [W]
0

APBDIS
0 = not APBDIS (mission mode)
1 = APBDIS
0 / **1** / Auto

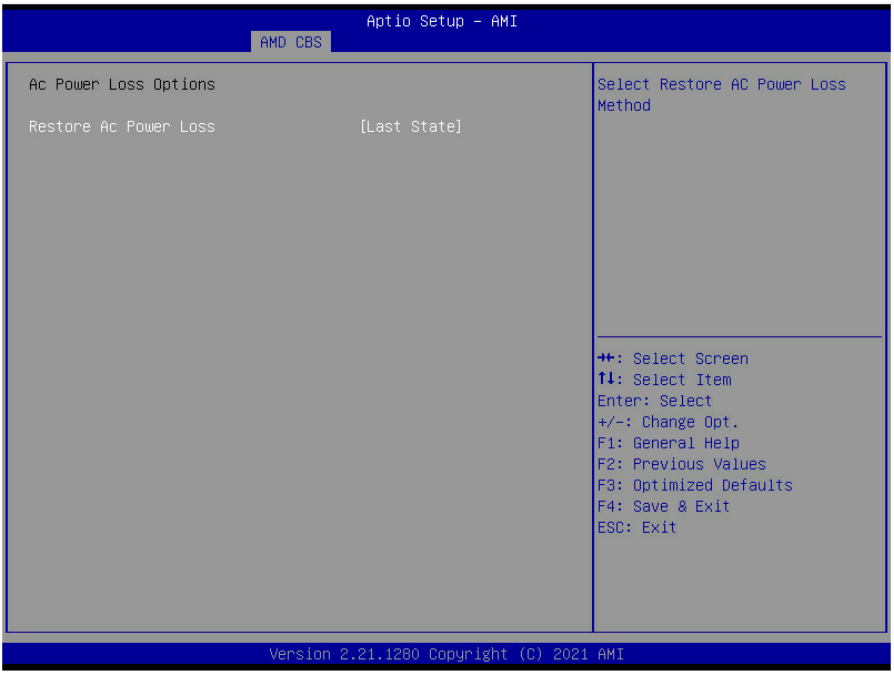
DF Cstates
Enable or Disable Data Fabric to go to a low-power state when the processor has entered Cx states.
Power
Performance
Disabled / Enabled / **Auto**

Fixed SOC Pstate
Fixed SOC Pstate.
P0 / P1 / P2 / P3 / Auto

3.5.5 FCH Common Options

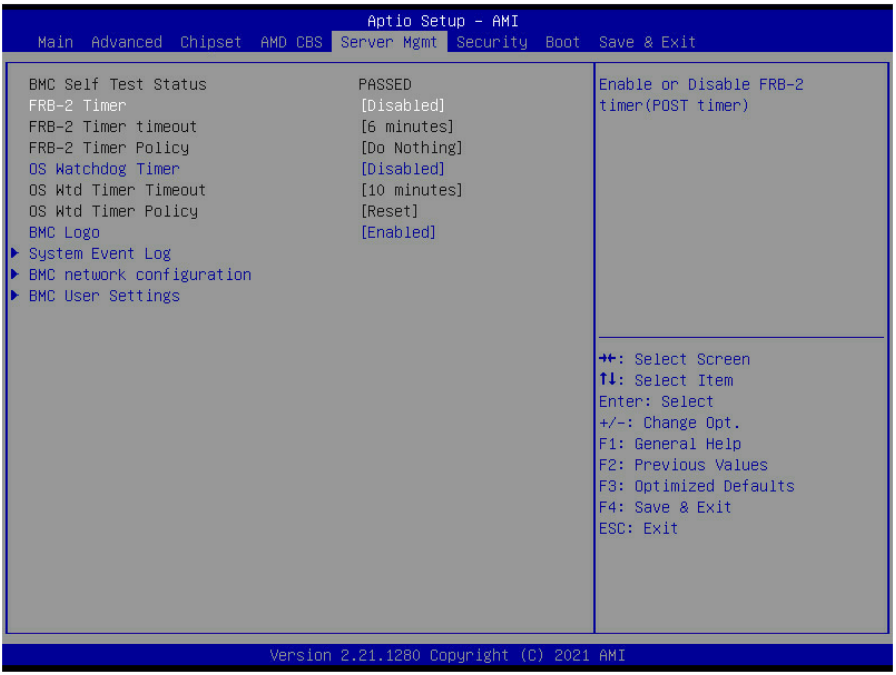
AC Power Loss Options
AC Power Loss Options.

3.5.4.1 AC Power Loss Options



Restore AC Power Loss
Select Restore AC Power Loss Method.
Power Off / Power On / **Last State**

3.6 Server Management



FRB-2 Timer
Enable or Disable FRB-2 timer (POST timer).

Enabled / **Disabled**

NOTE: The following items are available when **FRB-2 Timer** is set to [Enabled].

FRB-2 Timer timeout
Enter value Between 3 to 6 min for FRB-2 Timer Expiration value. Not available if FRB-2 Timer is disabled.

3 minutes / 4 minutes / 5 minutes / **6 minutes**

FRB-2 Timer Policy
Configure how the system should respond if the FRB-2 Timer expires. Not available if FRB-2 Timer is disabled.

Do Nothing / Reset / Power Down / Power Cycle

OS Watchdog Timer
If enabled, starts a BIOS timer which can only be shut off by Management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot Watchdog Timer policy.

Enabled / **Disabled**

NOTE: The following items are available when **OS Watchdog Timer** is set to [Enabled].

OS Wtd Timer timeout

Configure the length of the OS Boot Watchdog Timer. Not available if OS Boot Watchdog timer is disabled.

5 minutes / **10 minutes** / 15 minutes / 20 minutes

OS Wtd Timer Policy

Configure how the system should respond if the OS Boot Watchdog Timer expires. Not available if OS Boot Watchdog timer is disabled.

Do Nothing / **Reset** / Power Down / Power Cycle

BMC Logo

Enable or Disable BMC Logo.

Enabled / Disabled

System Event Log

Press <Enter> to change the SEL event log configuration.

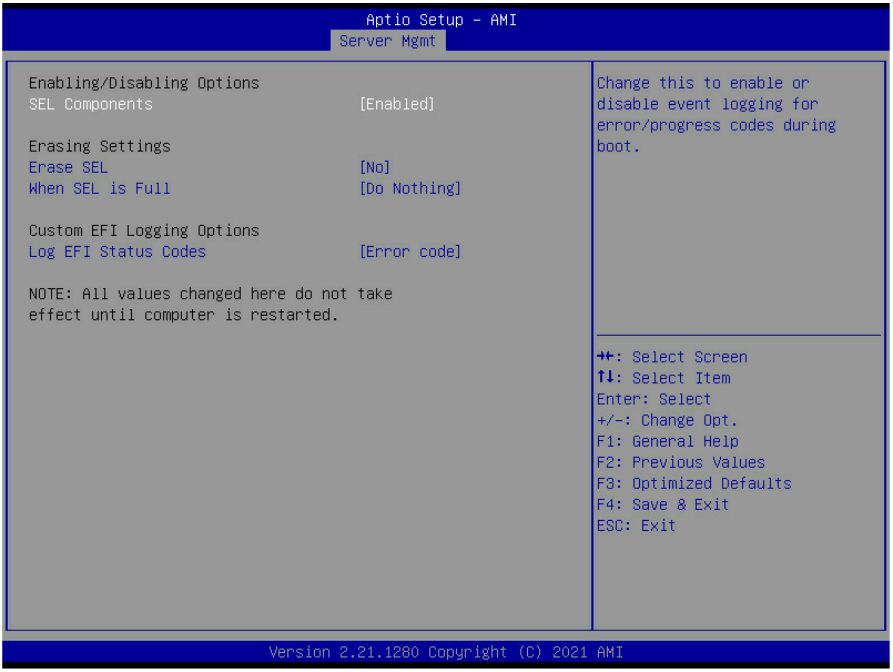
BMC network configuration

Configure BMC network parameters.

BMC User Settings

Press <Enter> to Add, Delete and Set Privilege level for users.

3.6.1 System Event Log



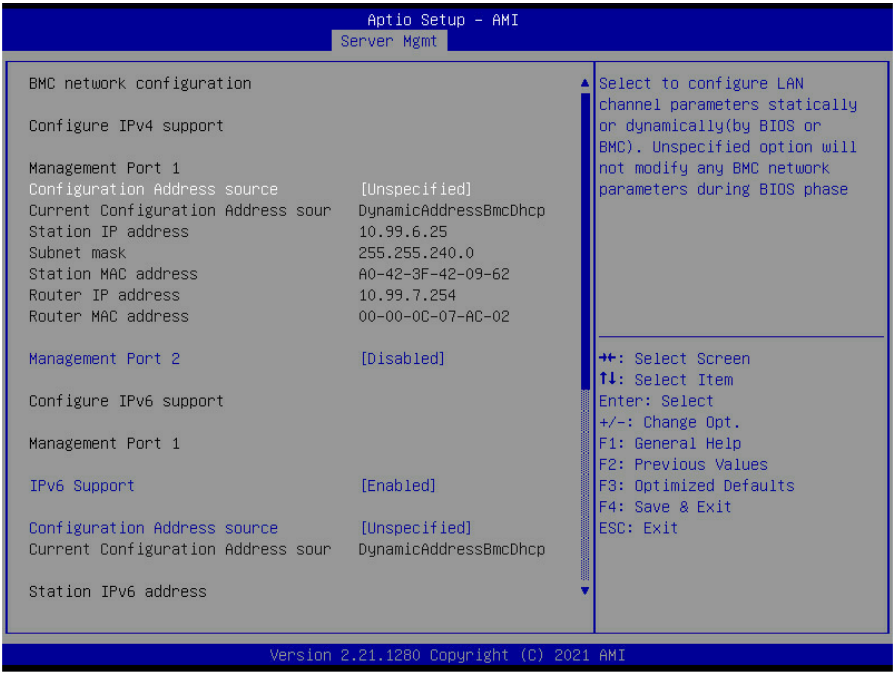
SEL Components
Change this to enable or disable all features of System Event Logging during boot.
Disabled / **Enabled**
NOTE: When **SEL Components** is set to [Disabled], the following items are read only.

Erase SEL
Choose options for erasing SEL.
No / Yes, on next reset / Yes, on every reset

When SEL is Full
Choose options for reactions to a full SEL.
Do Nothing / Erase Immediately / Delete Oldest Record

Log EFI Status Codes
Disable the logging of EFI Status Codes or log only error code or only progress code or both.
Disabled / Both / **Error Code** / Progress Code

3.6.2 BMC Network Configuration



Configuration Address Source
Select the configure LAN channel parameters statically or dynamically (by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

Unspecified / Static / DynamicBmcDhcp / DynamicBmcNonDhcp

Management Port 2
Enable/Disable BMC Share NIC.

Enabled / **Disabled**

Configure IPV6 support
Management Port 1
IPV6 Support
Enable or Disable LAN1 IPV6 Support.

Enabled / Disabled

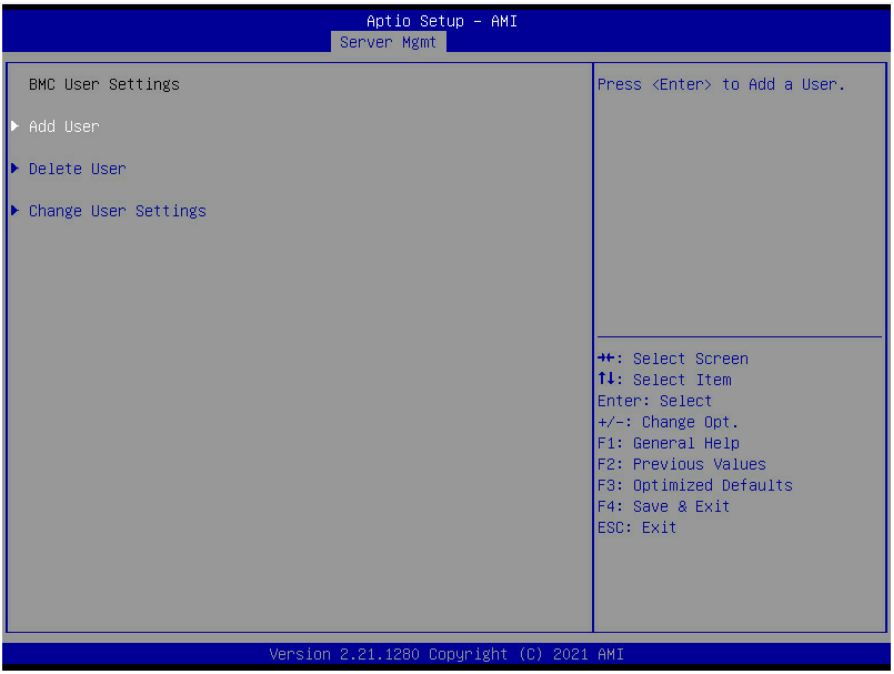
Configuration Address Source
Select the configure LAN channel parameters statically or dynamically (by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

Unspecified / Static / DynamicBmcDhcp

Management Port 2
IPV6 Support
Enable or Disable LAN2 IPV6 Support.

Enabled / **Disabled**

3.6.3 BMC User Settings

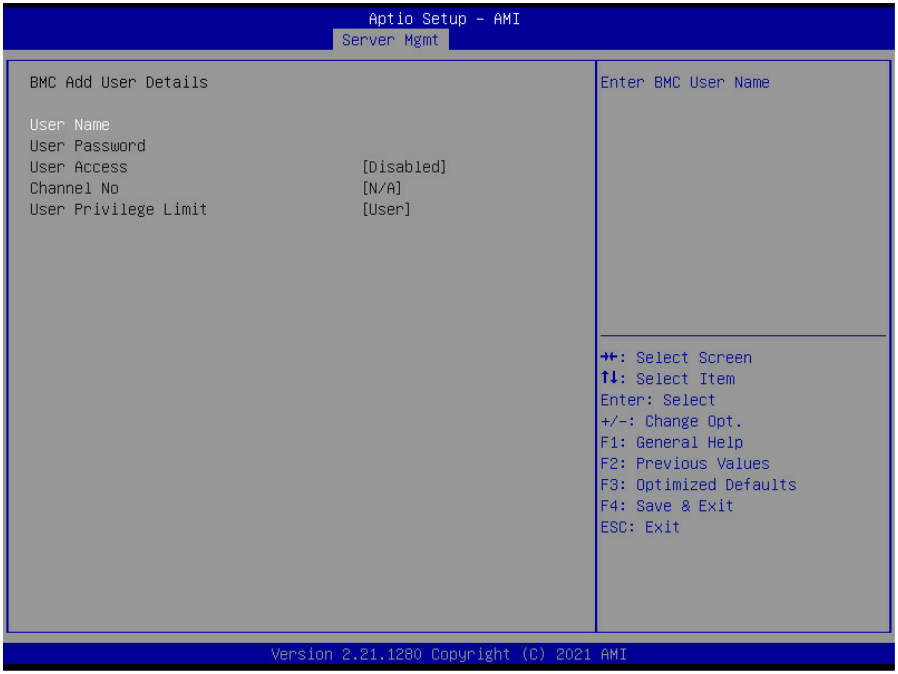


Add User
Press <Enter> to Add a user.

Delete User
Press <Enter> to Delete a user.

Change User Settings
Press <Enter> to change User Settings.

3.6.3.1 Add User



User Name
Enter BMC User Name.

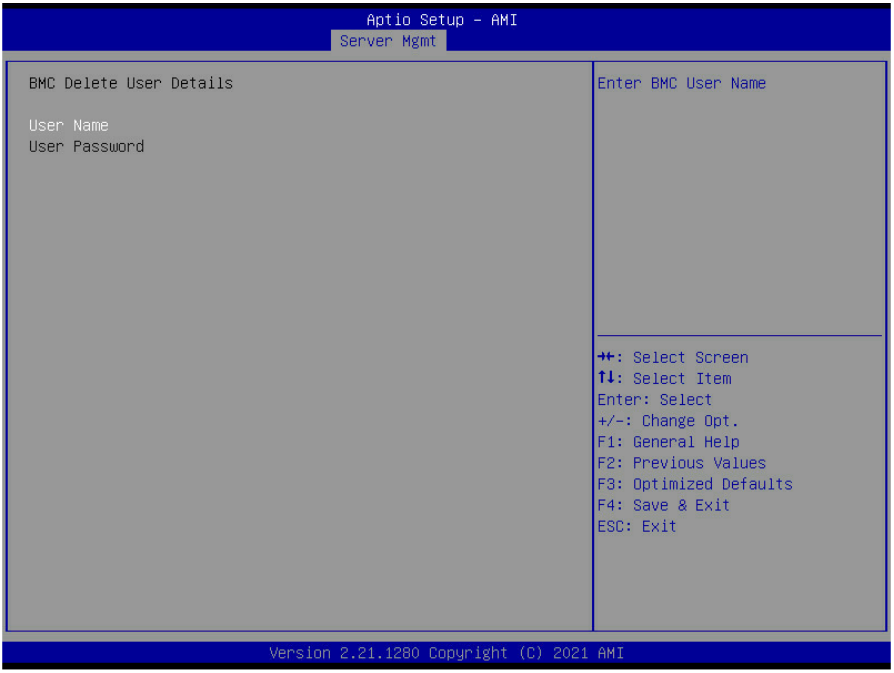
Change User Password
Enter New Password to change. Password at least 8 characters.

User Access
Enable/Disable the BMC User's Access.
Enabled / **Disabled**

Channel No
Enter BMC Channel Number.
1 – Dedicated LAN
8 – Shared LAN
N/A / 1 / 8

User Privilege Limit
Enter BMC User Privilege Limit for Selected Channel.
None / **User** / Operator / Administrator

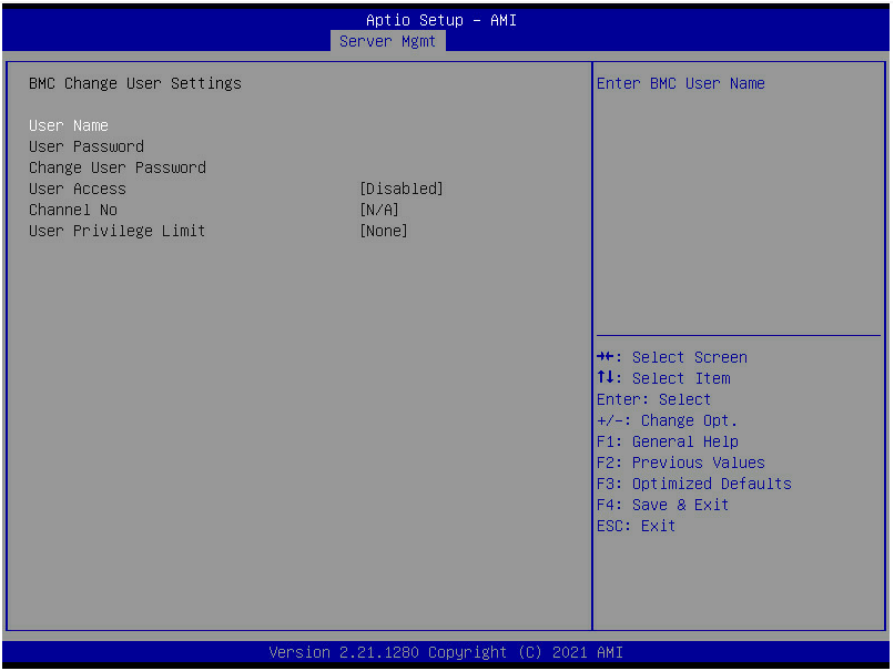
3.6.3.2 Delete User



User Name
Enter BMC User Name.

Change User Password
Enter New Password to change. Password at least 8 characters.

3.6.3.3 Change User Settings



User Name
Enter BMC User Name.

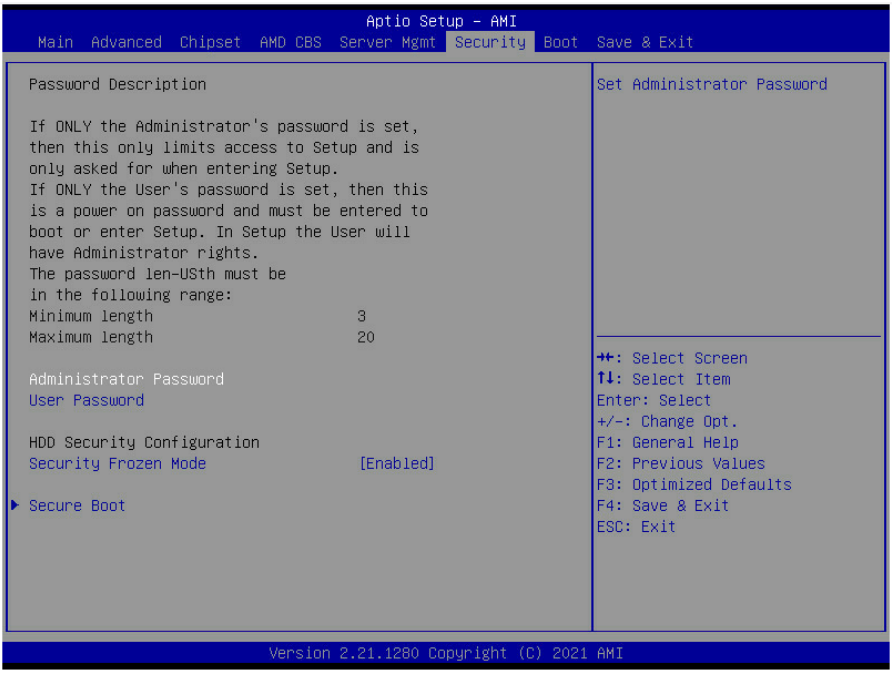
Change User Password
Enter New Password to change. Password at least 8 characters.

User Access
Enable/Disable the BMC User's Access.
Enabled / **Disabled**

Channel No
Enter BMC Channel Number.
1 – Dedicated LAN
8 – Shared LAN
N/A / 1 / 8

User Privilege Limit
Enter BMC User Privilege Limit for Selected Channel.
None / User / Operator / Administrator

3.7 Security



Administrator Password
Set administrator password in the ***Create New Password*** window. After you key in the password, the ***Confirm New Password*** window will pop out to ask for confirmation.

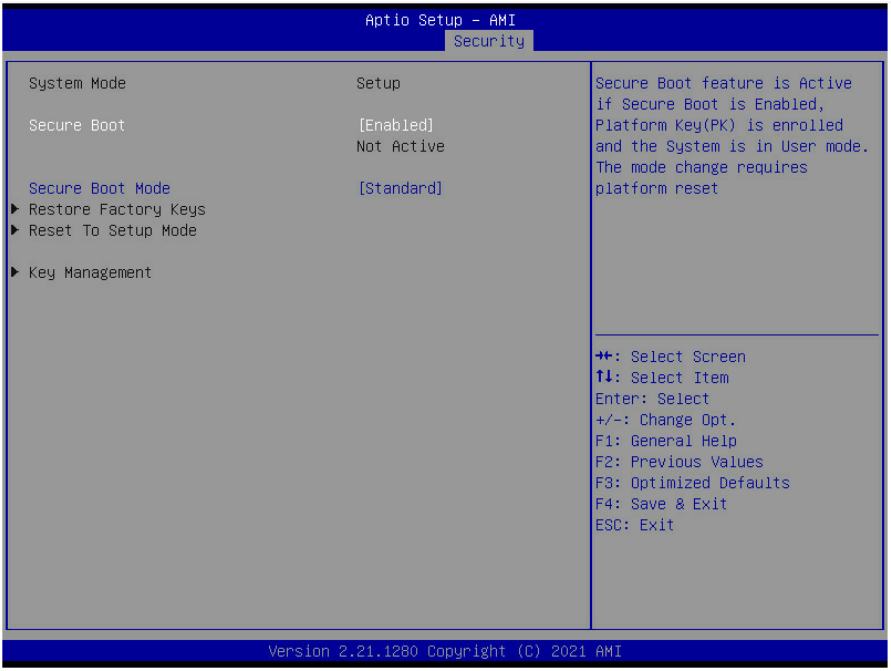
User Password
Set user password in the ***Create New Password*** window. After you key in the password, the ***Confirm New Password*** window will pop out to ask for confirmation.

Secure Frozen Mode
Disable means Hard Drive on Non-frozen mode. Enable means Hard Drive on Frozen mode.

Enabled / Disabled

Secure Boot
Secure Boot Configuration.

3.7.1 Secure Boot



Secure Boot
Secure Boot feature is Active if Secure Boot is Enabled. Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset.

Enabled / Disabled

Secure Boot Mode
Secure Boot mode selector: Standard/Custom. In Custom mode Secure Boot Variables can be configured without authentication.

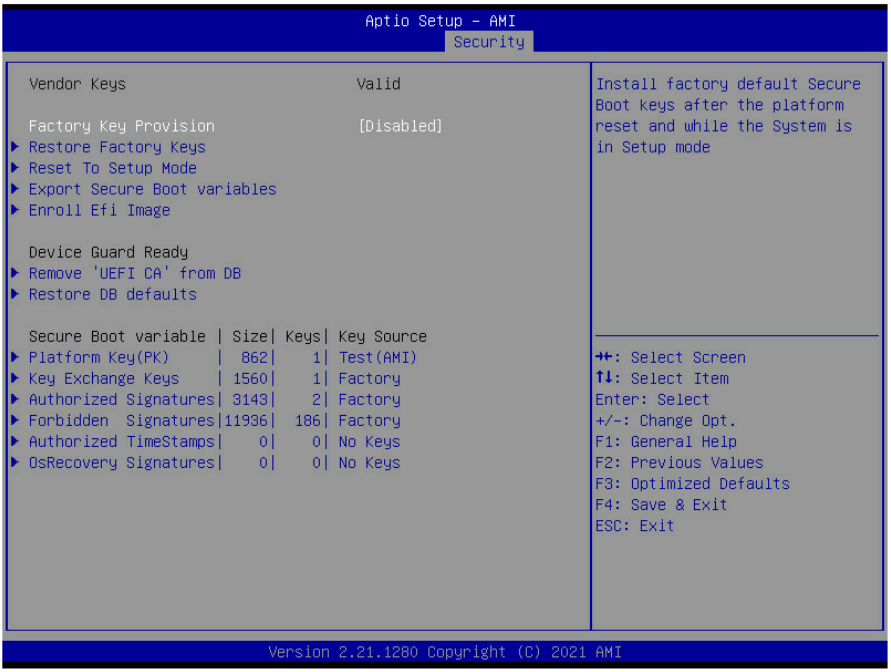
Standard / Custom

Restore Factory Keys
Force System to User Mode. Install factory default Secure Boot key databases. Press 'Yes' to proceed 'No' to cancel.

Reset to Setup Mode
Delete all Secure Boot key database from NVRAM. Deleting all variables will reset the System to Setup Mode. Press 'Yes' to proceed 'No' to cancel.

Key Management
Enables expert users to modify Secure Boot Policy variables without full authentication.

3.7.1.1 Key Management



Factory Key Provision
Install factory default Secure Boot keys after the platform reset and while the System is in Setup mode.

Enabled / **Disabled**

Restore Factory Keys
Force System to User Mode. Install factory default Secure Boot key databases. Press 'Yes' to proceed 'No' to cancel.

Reset to Setup Mode
Delete all Secure Boot key database from NVRAM. Deleting all variables will reset the System to Setup Mode.
Press 'Yes' to proceed 'No' to cancel.

Export Secure Boot variables
Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device.

Enroll Efi Image
Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db).

Remove 'UEFI CA' from DB
Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db).
Press 'Yes' to proceed 'No' to cancel.

Restore DB defaults
Restore DB variable to factory defaults.
Press 'Yes' to proceed 'No' to cancel.

Platform Key (PK)
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
    a) EFI_SIGNATURE_LIST
    b) EFI_CERT_X509 (DER)
    c) EFI_CERT_RSA2048 (bin)
    d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/C0FF Image (SHA256)
Key source: Factory, External, Mixed
Details / Export / Update / Delete

Key Exchange Keys
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
    a) EFI_SIGNATURE_LIST
    b) EFI_CERT_X509 (DER)
    c) EFI_CERT_RSA2048 (bin)
    d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/C0FF Image (SHA256)
Key source: Factory, External, Mixed
Details / Export / Update / Append / Delete

Authorized Signatures
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
    a) EFI_SIGNATURE_LIST
    b) EFI_CERT_X509 (DER)
    c) EFI_CERT_RSA2048 (bin)
    d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/C0FF Image (SHA256)
Key source: Factory, External, Mixed

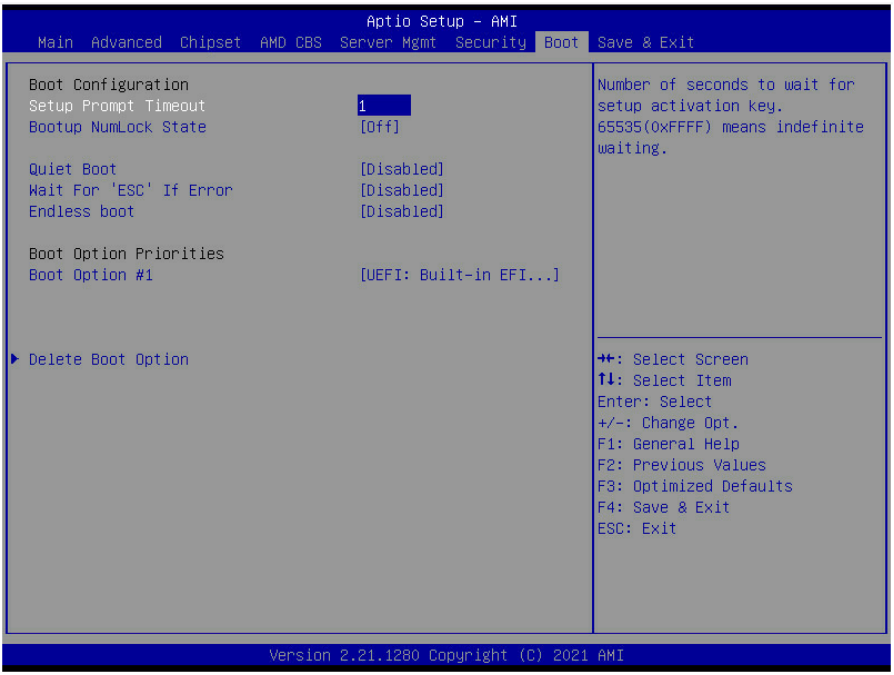
Details / Export / Update / Append / Delete

Forbidden Signatures
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
    a) EFI_SIGNATURE_LIST
    b) EFI_CERT_X509 (DER)
    c) EFI_CERT_RSA2048 (bin)
    d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/C0FF Image (SHA256)
Key source: Factory, External, Mixed
Details / Export / Update / Append / Delete

Authorized TimeStamps
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
    a) EFI_SIGNATURE_LIST
    b) EFI_CERT_X509 (DER)
    c) EFI_CERT_RSA2048 (bin)
    d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/C0FF Image (SHA256)
Key source: Factory, External, Mixed
Update / Append

OsRecovery Signatures
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
    a) EFI_SIGNATURE_LIST
    b) EFI_CERT_X509 (DER)
    c) EFI_CERT_RSA2048 (bin)
    d) EFI_CERT_SHAXXX
2. Authenticated UEFI Variable
3. EFI PE/C0FF Image (SHA256)
Key source: Factory, External, Mixed
Update / Append

3.8 Boot



Setup Prompt Timeout
Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.

1

Bootup NumLock State
Select the keyboard NumLock state.

Off / On

Quiet Boot
Enable or disable Quiet Boot option.

Enabled / **Disabled**

Wait for 'ESC' If Error
Wait for 'ESC' key to be pressed if error occurs.

Enabled / **Disabled**

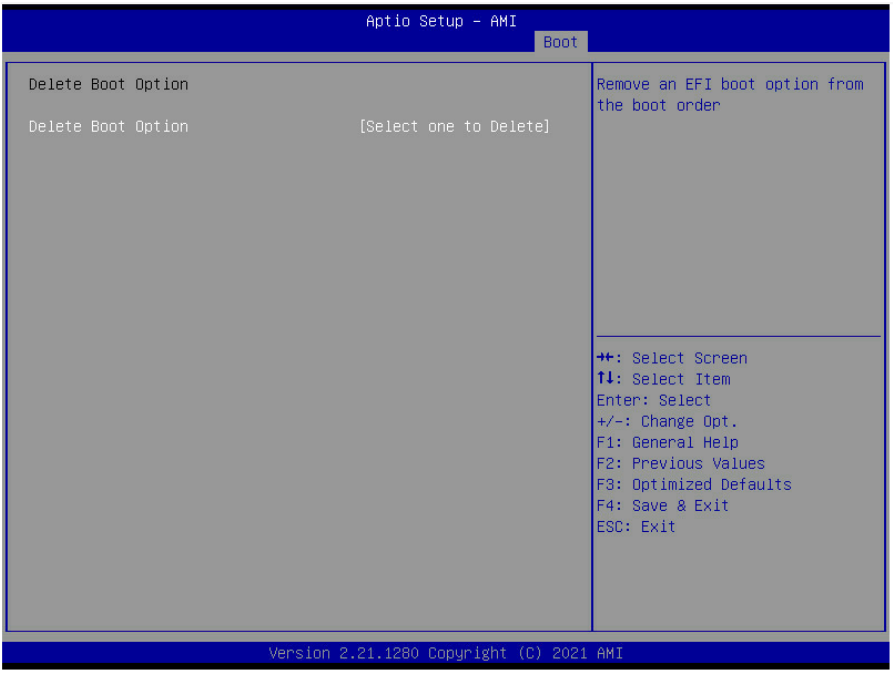
Endless Boot
Enable or disable Endless Boot.
Enabled / **Disabled**

Boot Option Priorities

Boot Option #1
Select the first/second boot device.
Device Name / Disabled

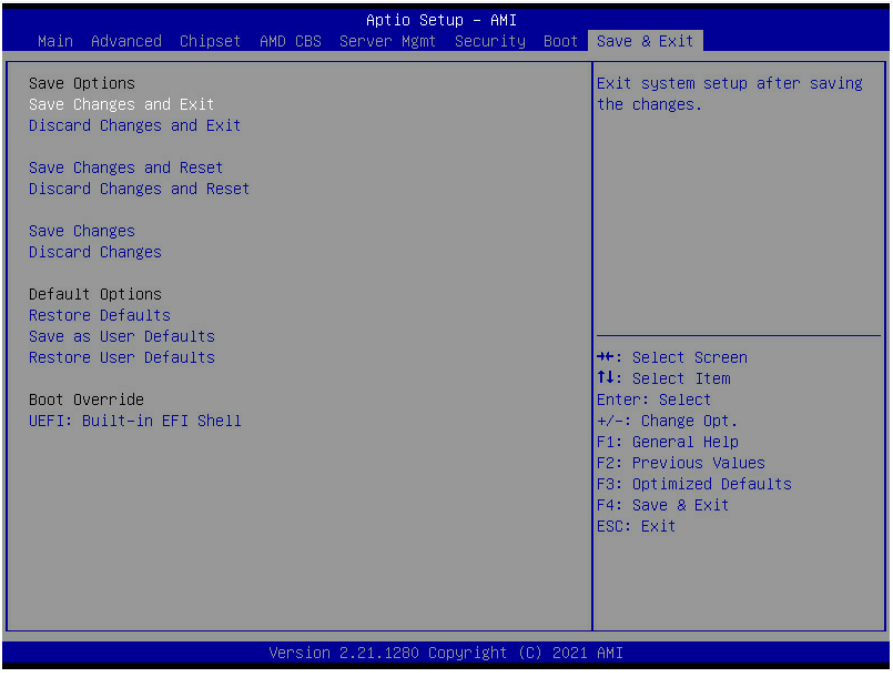
Delete Boot Option
Remove an EFI boot option from the boot order.

3.8.1 Delete Boot Option



Delete Boot Option
Remove an EFI boot option from the boot order.
Select one to Delete / UEFI: Built-in EFI Shell

3.9 Save & Exit



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save changes done so far to any of the setup options.

Discard Changes
Discard changes done so far to any of the setup options.

Restore Defaults
Restore/Load Default values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Boot Override
Read only.

Chapter 4: Diagnostics

NOTE: if you experience problems with setting up your system, always check the following things in the following order:

Memory, Video, CPU

By checking these items, you will most likely find out what the problem might have been when setting up your system. For more information on troubleshooting, check the TYAN website at http://www.tyan.com.

4.1 Flash Utility

Every BIOS file is unique for the motherboard it was designed for. For Flash Utilities, BIOS downloads, and information on how to properly use the Flash Utility with your motherboard, please check the TYAN web site at http://www.tyan.com

NOTE: Please be aware that by flashing your BIOS, you agree that in the event of a BIOS flash failure, you must contact your dealer for a replacement BIOS. There are no exceptions. TYAN does not have a policy for replacing BIOS chips directly with end users. In no event will TYAN be held responsible for damages done by the end user.

4.2 AMIBIOS Post Code (Aptio)

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	SEC errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Not used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not found

SEC Beep Codes
None

PEI Phase

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-Memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-Memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other)
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode(SMM) initialization
0x37	Post-Memory North Bridge initialization is started

Status Code	Description
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F – 0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
PEI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed
0x52	Memory initialization error. Invalid memory size or memory modules do not match
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error
0x55	Memory not installed
0x56	Invalid CPU type or speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU microcode is not found or microcode update is failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
0x5C – 0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by the DXE IPL)
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4 – 0xE7	Reserved for future AMI progress codes
S3 Resume Error Codes	
0xE8	S3 Resume Failed
0xE9	S3 Resume PPI not Found
0xEA	S3 Resume Boot Script Error
0xEB	S3 OS Wake Error
0xEC – 0xEF	Reserved for future AMI error codes

Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5 – 0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

DXE Phase

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x73	South Bridge DXE initialization (South Bridge module specific)
0x74	South Bridge DXE initialization (South Bridge module specific)
0x75	South Bridge DXE initialization (South Bridge module specific)

Status Code	Description
0x76	South Bridge DXE initialization (South Bridge module specific)
0x77	South Bridge DXE initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller initialization
0x94	PCI Bus Enumeration
0x95	PCI BUS Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console Input devices connect
0x99	Super IO initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E -0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event

Status Code	Description
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state
0x02	System is entering S2 sleep state
0x03	System is entering S3 sleep state
0x04	System is entering S4 sleep state
0x05	System is entering S5 sleep state
0x10	System is waking up from the S1 sleep state
0x20	System is waking up from the S2 sleep state
0x30	System is waking up from the S3 sleep state

Status Code	Description
0x40	System is waking up from the S4 sleep state
0xAC	System has transitioned into ACPI mode. Interrupt controller is in PIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix I: How to recover UEFI BIOS

Important Notes:

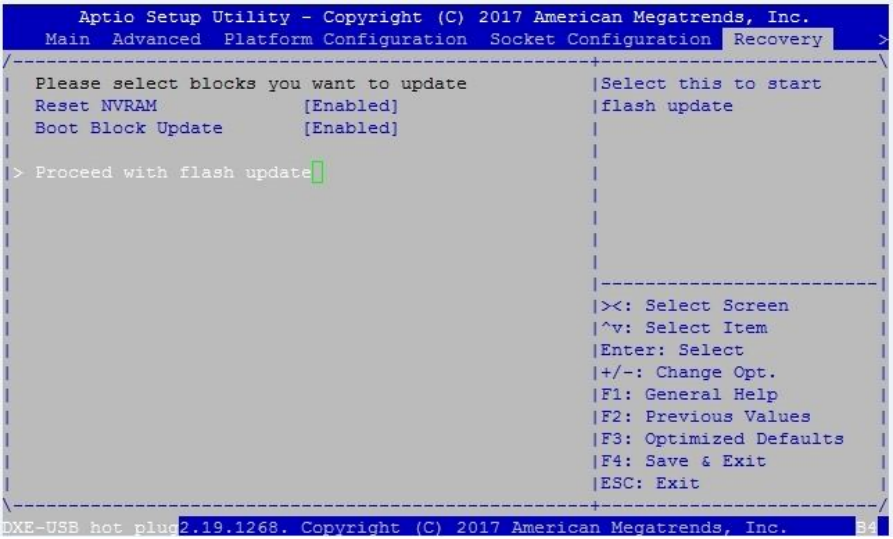
The emergency UEFI BIOS Recovery process is only used to rescue a system with a failed or corrupted BIOS image that fails to boot to an OS. It is not intended to be used as a general purpose BIOS flashing procedure and should not be used as such. Please do not shutdown or reset the system while the BIOS recovery process is underway or there is risk of damage to the UEFI recovery bootloader that would prevent the recovery process itself from working. In no event shall Tyan be liable for direct, indirect, incidental, special or consequential damages arising from the BIOS update or recovery.

The BIOS Recovery file is named xxxx.cap, where the 'xxxx' portion is the motherboard model number. Examples: 5630.cap, 7106.cap, 7109.cap, etc. Please make sure that you are using the correct BIOS Recovery file from Tyan's web site.

BIOS Recovery Process

1.Place the recovery BIOS file (xxxx.cap) in the root directory of a USB disk.
2.Ensure that the system is powered off.
3.Insert the USB disk to any USB port on the motherboard or chassis.
4.Power the system on while pressing “Ctrl” and “Home” simultaneously on the keyboard. Continue to hold these keys down until the following Tyan screen is displayed on the monitor:

5.The system will boot to BIOS setup. A new menu item will appear at the far right of the screen. Scroll to the 'Recovery' tab, move the curser to “Proceed with flash update” and press the "Enter" key on the keyboard to start the BIOS recovery process.



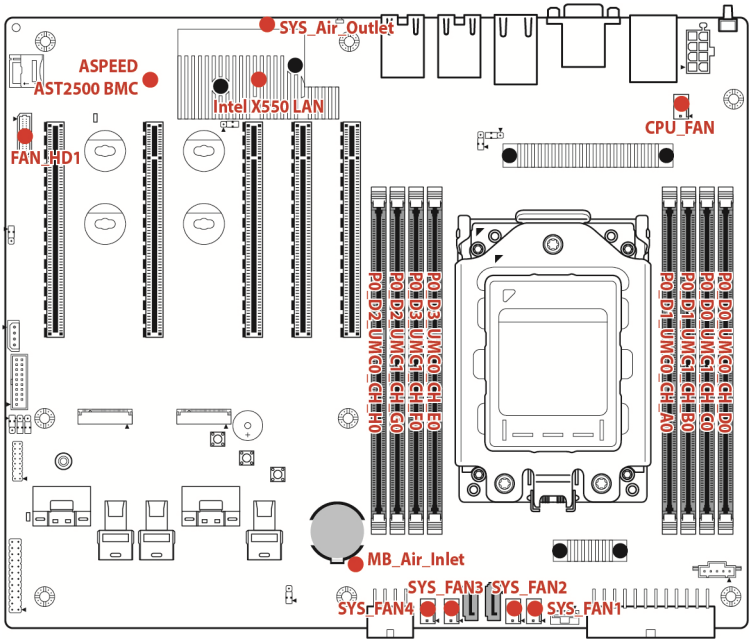
6.IMPORTANT: Do not power off or reboot the server during the BIOS recovery process. This can damage the BIOS recovery bootloader and prevent it from loading a subsequent time.
7.Wait for the BIOS recovery procedure to complete. Completion is signified with the message “Flash update completed. Press any key to reset the system” displayed on screen.
8.Remove the USB disk and reboot.

If your system does not have video output or the POST code halts at “FF” on the right-lower portion of the screen, please contact Tyan representatives for RMA service.

Appendix II: Fan and Temp Sensors

This section aims to help readers identify the locations of some specific FAN and Temp Sensors on the motherboard. A table of BIOS Temp sensor name explanation is also included for readers' reference.

Figure 1: Sensor Location

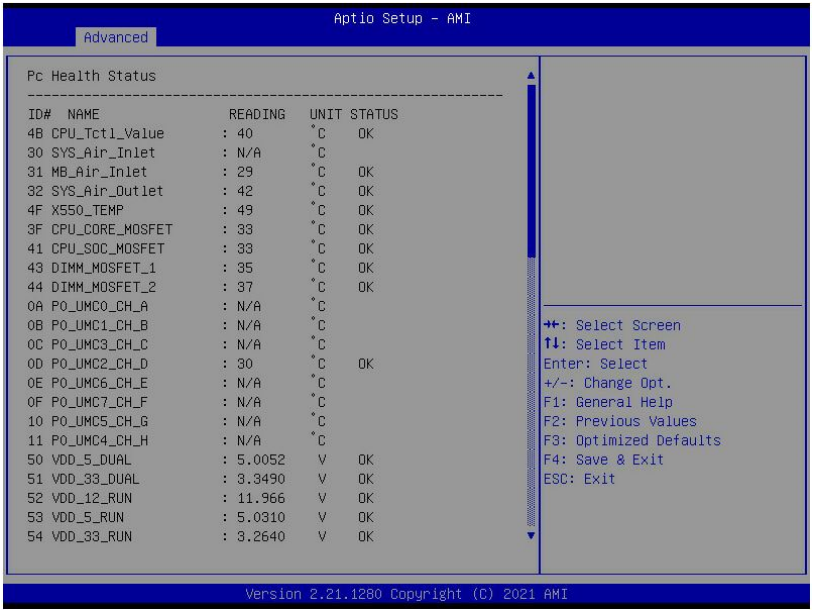


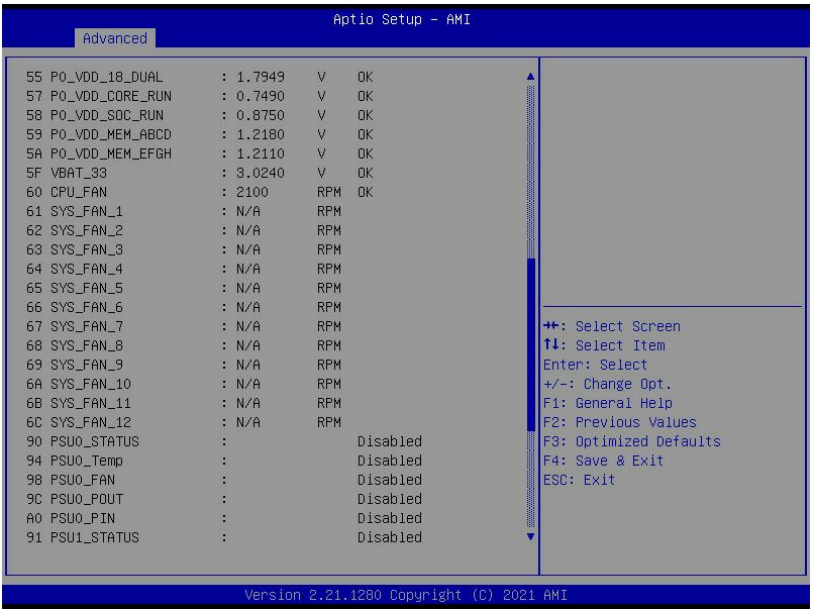
NOTE: The red spot indicates the sensor.

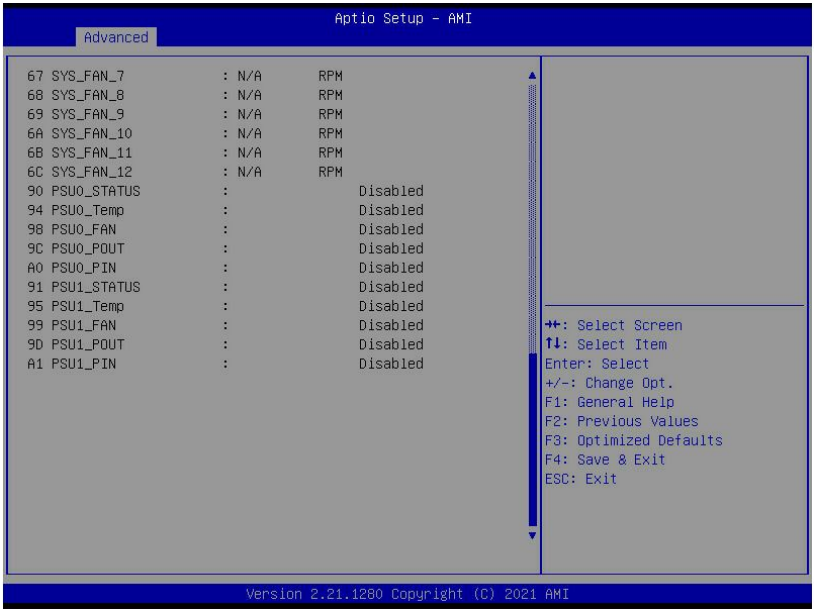
Fan and Temp Sensor Location:

1. Fan Sensor: It is located in the third pin of the fan connector, which detects the fan speed (rpm)
2. Temp Sensor: refer to Figure 1: Sensor Location. They detect the system temperature around.

BIOS Temp Sensor Name Explanation:







BIOS Temp Sensor	Name Explanation
CPU_Tctl_Value	CPU Tempterature
SYS_Air_Inlet	Sensor connected to the Front Panel
MB_Air_Inet	Temperature of the M/B Air Inlet Area
SYS_Air_Outlet	Temperature of the System Air Outlet Area
X550_Temp	Temperature of Intel LAN X550 chipset
CPU_CORE_MOSFET	Max Temperature of CPU_CORE_MOSFET
CPU_SOC_MOSFET	Max Temperature of CPU_SOC_ MOSFET
DIMM_MOSFET_1	Max Temperature of CPU DIMM Area1 MOSFET
DIMM_MOSFET_2	Max Temperature of CPU DIMM Area2 MOSFET
P0_UMC0_CH_A	Temperature of CPU0 DIMM Channel A
P0_UMC1_CH_B	Temperature of CPU0 DIMM Channel B
P0_UMC3_CH_C	Temperature of CPU0 DIMM Channel C
P0_UMC2_CH_D	Temperature of CPU0 DIMM Channel D
P0_UMC6_CH_E	Temperature of CPU0 DIMM Channel E
P0_UMC7_CH_F	Temperature of CPU0 DIMM Channel F
P0_UMC5_CH_G	Temperature of CPU0 DIMM Channel G
P0_UMC4_CH_H	Temperature of CPU0 DIMM Channel H
CPU_FAN	Fan Speed of CPU_FAN
SYS_FAN_1	Fan Speed of SYS_FAN_1
SYS_FAN_2	Fan Speed of SYS_FAN_2
SYS_FAN_3	Fan Speed of SYS_FAN_3
SYS_FAN_4	Fan Speed of SYS_FAN_4
SYS_FAN_5	Fan Speed of SYS_FAN_5

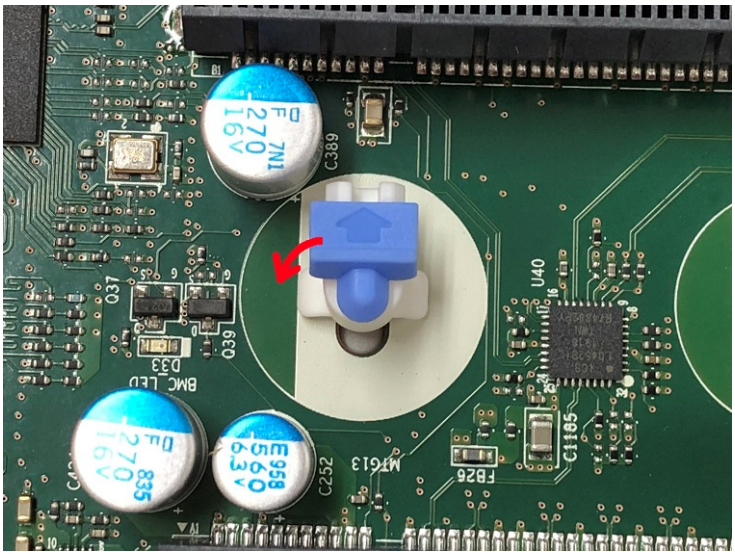
SYS_FAN_6	Fan Speed of SYS_FAN_6
SYS_FAN_7	Fan Speed of SYS_FAN_7
SYS_FAN_8	Fan Speed of SYS_FAN_8
SYS_FAN_9	Fan Speed of SYS_FAN_9
SYS_FAN_10	Fan Speed of SYS_FAN_10
SYS_FAN_11	Fan Speed of SYS_FAN_11
SYS_FAN_12	Fan Speed of SYS_FAN_12
PSU0_STATUS	Current status of PSU0
PSU0_Temp	Temperature of PSU0
PSU0_FAN	Fan Speed of PSU0
PSU1_STATUS	Current status of PSU1
PSU1_Temp	Temperature of PSU1
PSU1_FAN	Fan Speed of PSU1

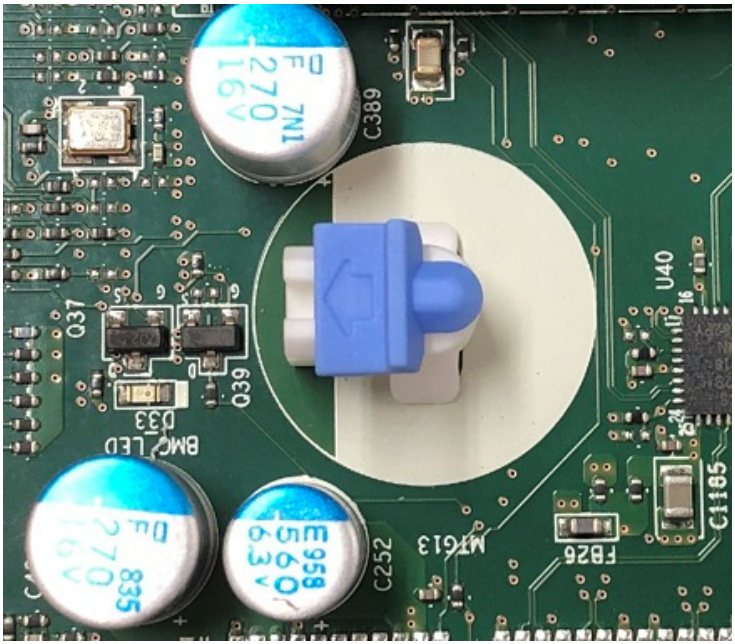
Appendix III: M.2 Latch Installation

This section provides a step-by-step demonstration on how to install a M.2 latch.

1. Take out the M.2 latch packs from the Accessory Box.

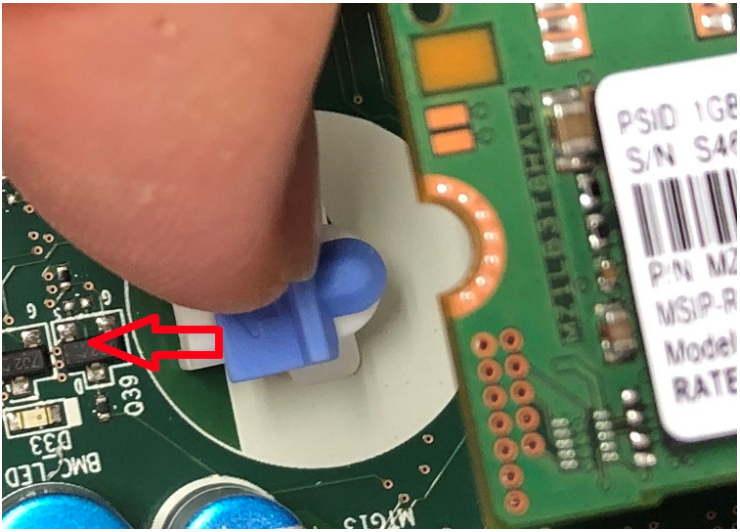
2. Insert the M.2 latch into the hole and then turn 90 degrees to the left as shown below.



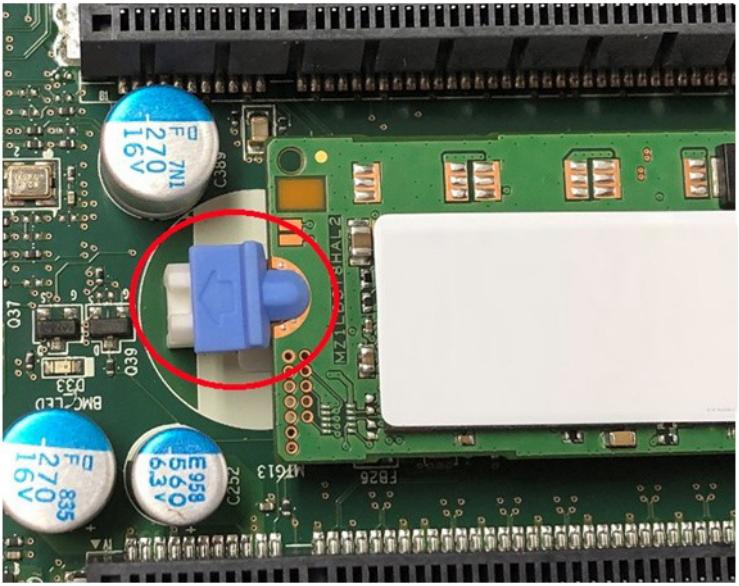


NOTE: The arrow sign on the blue knob is now turned left.

3. Push the blue knob slightly to the left as the arrow shows to lock the M.2 card in place.



4. The installation of the M.2 latch is now complete.



NOTE

Glossary

ACPI (Advanced Configuration and Power Interface): a power management specification that allows the operating system to control the amount of power distributed to the computer's devices. Devices not in use can be turned off, reducing unnecessary power expenditure.

AGP (Accelerated Graphics Port): a PCI-based interface which was designed specifically for demands of 3D graphics applications. The 32-bit AGP channel directly links the graphics controller to the main memory. While the channel runs only at 66 MHz, it supports data transmission during both the rising and falling ends of the clock cycle, yielding an effective speed of 133 MHz.

ATAPI (AT Attachment Packet Interface): also known as IDE or ATA; a drive implementation that includes the disk controller on the device itself. It allows CD-ROMs and tape drives to be configured as master or slave devices, just like HDDs.

ATX: the form factor designed to replace the AT form factor. It improves on the AT design by rotating the board 90 degrees, so that the IDE connectors are closer to the drive bays, and the CPU is closer to the power supply and cooling fan. The keyboard, mouse, USB, serial, and parallel ports are built-in.

Bandwidth: refers to carrying capacity. The greater the bandwidth, the more data the bus, phone line, or other electrical path can carry. Greater bandwidth results in greater speed.

BBS (BIOS Boot Specification): a feature within the BIOS that creates, prioritizes, and maintains a list of all Initial Program Load (IPL) devices, and then stores that list in NVRAM. IPL devices have the ability to load and execute an OS, as well as provide the ability to return to the BIOS if the OS load process fails. At that point, the next IPL device is called upon to attempt loading of the OS.

BIOS (Basic Input/Output System): the program that resides in the ROM chip, which provides the basic instructions for controlling your computer's hardware. Both the operating system and application software use BIOS routines to ensure compatibility.

Buffer: a portion of RAM which is used to temporarily store data; usually from an application though it is also used when printing and in most keyboard drivers. The CPU can manipulate data in a buffer before copying it to a disk drive. While this improves system performance (reading to or writing from a disk drive a single time is much faster than doing so repeatedly) there is the possibility of losing your data should the system crash. Information in a buffer is temporarily stored, not permanently saved.

Bus: a data pathway. The term is used especially to refer to the connection between the processor and system memory, and between the processor and PCI or ISA local buses.

Bus mastering: allows peripheral devices and IDEs to access the system memory without going through the CPU (similar to DMA channels).

Cache: a temporary storage area for data that will be needed often by an application. Using a cache lowers data access times since the information is stored in SRAM instead of slower DRAM. Note that the cache is also much smaller than your regular memory: a typical cache size is 512KB, while you may have as much as 4GB of regular memory.

Closed and open jumpers: jumpers and jumper pins are active when they are “on” or “closed”, and inactive when they are “off” or “open”.

CMOS (Complementary Metal-Oxide Semiconductors): chips that hold the basic startup information for the BIOS.

COM port: another name for the serial port, which is called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another). Parallel ports transmit the bits of a byte on eight different wires at the same time (that is, in parallel form, eight bits at the same time).

DDR (Double Data Rate): a technology designed to double the clock speed of the memory. It activates output on both the rising and falling edge of the system clock rather than on just the rising edge, potentially doubling output.

DIMM (Dual In-line Memory Module): faster and more capacious form of RAM than SIMMs, and do not need to be installed in pairs.

DIMM bank: sometimes called DIMM socket because the physical slot and the logical unit are the same. That is, one DIMM module fits into one DIMM socket, which is capable of acting as a memory bank.

DMA (Direct Memory Access): channels that are similar to IRQs. DMA channels allow hardware devices (like soundcards or keyboards) to access the main memory without involving the CPU. This frees up CPU resources for other tasks. As with IRQs, it is vital that you do not double up devices on a single line. Plug-n-Play devices will take care of this for you.

DRAM (Dynamic RAM): widely available, very affordable form of RAM which looses data if it is not recharged regularly (every few milliseconds). This refresh requirement makes DRAM three to ten times slower than non-recharged RAM such as SRAM.

ECC (Error Correction Code or Error Checking and Correcting): allows data to be checked for errors during run-time. Errors can subsequently be corrected at the same time that they're found.

EEPROM (Electrically Erasable Programmable ROM): also called Flash BIOS, it is a ROM chip which can, unlike normal ROM, be updated. This allows you to keep up with changes in the BIOS programs without having to buy a new chip. TYAN®'s BIOS updates can be found at http://**www.tyan.com**

ESCD (Extended System Configuration Data): a format for storing information about Plug-n-Play devices in the system BIOS. This information helps properly configure the system each time it boots.

Firmware: low-level software that controls the system hardware.

Form factor: an industry term for the size, shape, power supply type, and external connector type of the Personal Computer Board (PCB) or motherboard. The standard form factors are the AT and ATX.

Global timer: onboard hardware timer, such as the Real-Time Clock (RTC).

HDD: stands for Hard Disk Drive, a type of fixed drive.

H-SYNC: controls the horizontal synchronization/properties of the monitor.

HyperTransport™: a high speed, low latency, scalable point-to-point link for interconnecting ICs on boards. It can be significantly faster than a PCI bus for an equivalent number of pins. It provides the bandwidth and flexibility critical for today's networking and computing platforms while retaining the fundamental programming model of PCI.

IC (Integrated Circuit): the formal name for the computer chip.

IDE (Integrated Device/Drive Electronics): a simple, self-contained HDD interface. It can handle drives up to 8.4 GB in size. Almost all IDEs sold now are in fact Enhanced IDEs (EIDEs), with maximum capacity determined by the hardware controller.

IDE INT (IDE Interrupt): Hardware interrupt signal that goes to the IDE.

I/O (Input/Output): the connection between your computer and another piece of hardware (mouse, keyboard, etc.)

IRQ (Interrupt Request): an electronic request that runs from a hardware device to the CPU. The interrupt controller assigns priorities to incoming requests and delivers them to the CPU. It is important that there is only one device hooked up to each IRQ line; doubling up devices on IRQ lines can lock up your system. Plug-n-Play operating systems can take care of these details for you.

Latency: the amount of time that one part of a system spends waiting for another part to catch up. This occurs most commonly when the system sends data out to a peripheral device and has to wait for the peripheral to spread (peripherals tend to be slower than onboard system components).

NVRAM: ROM and EEPROM are both examples of Non-Volatile RAM, memory that holds its data without power. DRAM, in contrast, is volatile.

Parallel port: transmits the bits of a byte on eight different wires at the same time.

PCI (Peripheral Component Interconnect): a 32 or 64-bit local bus (data pathway) which is faster than the ISA bus. Local buses are those which operate within a single system (as opposed to a network bus, which connects multiple systems).

PCI PIO (PCI Programmable Input/Output) modes: the data transfer modes used by IDE drives. These modes use the CPU for data transfer (in contrast, DMA channels do not). PCI refers to the type of bus used by these modes to communicate with the CPU.

PCI-to-PCI Bridge: allows you to connect multiple PCI devices onto one PCI slot.

Pipeline burst SRAM: a fast secondary cache. It is used as a secondary cache because SRAM is slower than SDRAM, but usually larger. Data is cached first to the faster primary cache, and then, when the primary cache is full, to the slower secondary cache.

PnP (Plug-n-Play): a design standard that has become ascendant in the industry. Plug-n-Play devices require little set-up to use. Devices and operating systems that are not Plug-n-Play require you to reconfigure your system each time you add or change any part of your hardware.

PXE (Preboot Execution Environment): one of four components that together make up the Wired for Management 2.0 baseline specification. PXE was designed to define a standard set of preboot protocol services within a client with the goal of allowing networked-based booting to boot using industry standard protocols.

RAID (Redundant Array of Independent Disks): a way for the same data to be stored in different places on many hard drives. By using this method, the data is stored redundantly and multiple hard drives will appear as a single drive to the operating system. RAID level 0 is known as striping, where data is striped (or overlapped) across multiple hard drives, but offers no fault-tolerance. RAID level 1 is known as mirroring, which stores the data within at least two hard drives, but does not stripe. RAID level 1 also allows for faster access time and fault-tolerance, since either hard drive can be read at the same time. RAID level 0+1 is striping and mirroring, providing fault-tolerance, striping, and faster access all at the same time.

RAIDIOS: RAID I/O Steering (Intel)

RAM (Random Access Memory): technically refers to a type of memory where any byte can be accessed without touching the adjacent data and is often referred to the system's main memory. This memory is available to any program running on the computer.

ROM (Read-Only Memory): a storage chip which contains the BIOS; the basic instructions required to boot the computer and start up the operating system.

SDRAM (Synchronous Dynamic RAM): called as such because it can keep two sets of memory addresses open simultaneously. By transferring data alternately from one set of addresses and then the other, SDRAM cuts down on the delays associated with non-synchronous RAM, which must close one address bank before opening the next.

Serial port: called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another).

SCSI Interrupt Steering Logic (SISL): Architecture that allows a RAID controller, such as AcceleRAID 150, 200 or 250, to implement RAID on a system board-embedded SCSI bus or a set of SCSI busses. SISL: SCSI Interrupt Steering Logic (LSI) (only on LSI SCSI boards)

Sleep/Suspend mode: in this mode, all devices except the CPU shut down.

SRAM (Static RAM): unlike DRAM, this type of RAM does not need to be refreshed in order to prevent data loss. Thus, it is faster and more expensive.

SLI (Scalable Link Interface): NVIDIA SLI technology links two graphics cards together to provide scalability and increased performance. NVIDIA SLI takes advantage of the increased bandwidth of the PCI Express bus architecture, and features hardware and software innovations within NVIDIA GPUs (graphics processing units) and NVIDIA MCPs (media and communications processors). Depending on the application, NVIDIA SLI can deliver as much as two times the performance of a single GPU configuration.

Standby mode: in this mode, the video and hard drives shut down; all other devices continue to operate normally.

UltraDMA-33/66/100: a fast version of the old DMA channel. UltraDMA is also called UltraATA. Without a proper UltraDMA controller, your system cannot take advantage of higher data transfer rates of the new UltraDMA/UltraATA hard drives.

USB (Universal Serial Bus): a versatile port. This one port type can function as a serial, parallel, mouse, keyboard or joystick port. It is fast enough to support video transfer, and is capable of supporting up to 127 daisy-chained peripheral devices.

VGA (Video Graphics Array): the PC video display standard

V-SYNC: controls the vertical scanning properties of the monitor.

ZCR (Zero Channel RAID): PCI card that allows a RAID card to use the onboard SCSI chip, thus lowering cost of RAID solution

ZIF Socket (Zero Insertion Force socket): these sockets make it possible to insert CPUs without damaging the sensitive CPU pins. The CPU is lightly placed in an open ZIF socket, and a lever is pulled down. This shifts the processor over and down, guiding it into the board and locking it into place.

Technical Support

If a problem arises with your system, you should first turn to your dealer for direct support. Your system has most likely been configured or designed by them and they should have the best idea of what hardware and software your system contains. Hence, they should be of the most assistance for you. Furthermore, if you purchased your system from a dealer near you, take the system to them directly to have it serviced instead of attempting to do so yourself (which can have expensive consequences).

If these options are not available for you then TYAN can help. Besides designing innovative and quality products for over a decade, TYAN has continuously offered customers service beyond their expectations. TYAN's website (**www.tyan.com**) provides easy-to-access FAQ searches and online Trouble Ticket creation as well as Instant Chat capabilities with our Support Agents. TYAN also provides easy-to-access resources such as in-depth Linux Online Support sections with downloadable Linux drivers and comprehensive compatibility reports for chassis, memory and much more. With all these convenient resources just a few keystrokes away, users can easily find the latest software and operating system components to keep their systems running as powerful and productive as possible. TYAN also ranks high for its commitment to fast and friendly customer support through email. By offering plenty of options for users, TYAN serves multiple market segments with the industry's most competitive services to support them.

"TYAN's tech support is some of the most impressive we've seen, with great response time and exceptional organization in general" - Anandtech.com

Help Resources:

1. See the beep codes section of this manual.
2. See the TYAN website for FAQ's, bulletins, driver updates, and other information: **http://www.tyan.com**
3. Contact your dealer for help BEFORE calling TYAN.
4. Check the TYAN user group: **alt.comp.periphs.mainboard.TYAN**

Returning Merchandise for Service

During the warranty period, contact your distributor or system vendor FIRST for any product problems. This warranty only covers normal customer use and does not cover damages incurred during shipping or failure due to the alteration, misuse, abuse, or improper maintenance of products.

NOTE:
A receipt or copy of your invoice marked with the date of purchase is required before any warranty service can be rendered. You may obtain service by calling the manufacturer for a Return Merchandise Authorization (RMA) number. The RMA number Should be prominently displayed on the outside of the shipping carton and the package should be mailed prepaid. TYAN will pay to have the board shipped back to you.

Notice for the USA
Compliance Information Statement (Declaration of Conformity Procedure) DoC
FCC Part 15: This device complies with part 15 of the FCC Rules

Operation is subject to the following conditions:

This device may not cause harmful interference, and this device must accept any interference received including interference that may cause undesired operation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try one or more of the following measures:
Reorient or relocate the receiving antenna.
Increase the separation between the equipment and the receiver.
Plug the equipment into an outlet on a circuit different from that of the receiver.
Consult the dealer on an experienced radio/television technician for help.

Notice for Canada
This apparatus complies with the Class B limits for radio interference as specified in the Canadian Department of Communications Radio Interference Regulations. (Cet appareil est conforme aux norms de Classe B d'interference radio tel que specifie par le Ministere Canadien des Communications dans les reglements d'ineteference radio.)

CAUTION: Lithium battery included with this board. Do not puncture, mutilate, or dispose of battery in fire. There is danger of an explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by manufacturer. Dispose of used battery according to manufacturer instructions and in accordance with your local regulations.

Document #: D2520-200