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THE VOLTAGE REGULATOR APPLICATIONS HANDBOOK

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THE
VOLTAGE REGULATOR
APPLICATIONS HANDBOOK

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CHAPTER 1
Introduction

In spite of the common, almost universal, use of regulated power supplies in systems design, they are still one of the factors most likely to be compromised in terms of engineering effort and design time. This is due to the wide variety of system power requirements. The main purpose of this handbook, then, is to provide the power supply designer with a complete, practical reference for voltage regulators and thus contribute to a shorter, more efficient design cycle.

Monolithic voltage regulators have improved tremendously, both in performance and reliability, since 1967. One of the most significant steps was the introduction of the 3-terminal, fully protected regulator in 1969. The industry's first (and present) standard voltage regulator is the μA723. This device and its wide scope of applications is discussed in Chapter 8. In direct contrast, 3-terminal regulators, such as the Fairchild μA7800 series, are designed for specific fixed-voltage applications. These devices require very few external components, are essentially blow-out proof, and are low in cost. With these features it is difficult, if not impossible, to justify building discrete component regulators, particularly for local on-card applications.

This handbook devotes two chapters to each major regulator family. Specifically covered are the μA7800, μA78M00, μA7600, μA79E00, and the μA723. The first chapters describe the internal design of the devices and their electrical characteristics. The subsequent chapters discuss electrical and thermal considerations useful as guidelines in device application, and a brief description of the primary circuit applications. Because there are many different types of regulators, more than one circuit approach to a particular system requirement is quite likely. In such cases, a value judgement must be made to select the optimum approach for that application. Later chapters describe new regulator developments at Fairchild and list some currently available second-source devices. An aid in the successful application of voltage regulators is a selection guide covering the complete regulator line. Also included in this handbook are appendices covering switching regulator and power supply design, and a guide to the selection and operation of suitable power transistors.

A major premise of this handbook is that the reader is familiar with the basic operation of IC voltage regulators. Briefly stated: a temperature-compensated reference voltage is developed on-chip and is compared with the derived output voltage present in an error amplifier. This amplifier requires both high gain and wide bandwidth to ensure good regulation characteristics and fast transient response. It must also have low temperature drift to maintain a high order of output voltage stability under changing temperature conditions. The error amplifier drives the output stage, consisting of a Darlington pair. Also located on the chip are the necessary bias supplies, and various protection circuits.

Unless otherwise stated, line and load regulation characteristics are specified at a junction temperature of 25°C. This ensures that the specification limits represent true regulation limits unmasked by thermal effects. Therefore, to test for these characteristics, it is necessary to use a low duty cycle input signal to minimize device dissipation. Internal device heating during production testing is prevented by programming the automatic test equipment for very short test times (the entire regulator test cycle is completed in less than one second).

Throughout this book equivalent metric dimensions have been derived from the original inch dimensions.

SPECIFICATIONS AND PARAMETERS —

Some general comments on voltage regulator specifications and parameter definitions follow.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percent change in output voltage for a specified ambient temperature change.

DROPOUT VOLTAGE — The input-to-output differential voltage at which the circuit ceases to regulate against further input voltage reductions.

INPUT VOLTAGE RANGE — The range of dc input voltage within which the regulator operates to tolerance.

INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL — The range between the input and output voltages outside of which the regulator does not operate to tolerance.

LINE REGULATION — The percent change in output voltage for a specified change in input voltage.

LOAD REGULATION — The percent change in output voltage for a specified change in load current.

LONG TERM STABILITY — Output voltage stability under accelerated life test conditions measured after 1000 hours at maximum rated voltage/power dissipation.

OUTPUT NOISE VOLTAGE — The rms value of noise voltage measured at the output with a constant load current and no input ripple.

OUTPUT RESISTANCE — The resistance, at a specified value of load current, seen at the output terminal.

OUTPUT VOLTAGE RANGE — The range of regulated output voltages over which certain specifications apply.

QUIESCENT CURRENT — That part of the regulator input current not delivered to the load.

RIPPLE REJECTION — The ratio of peak-to-peak input ripple voltage to peak-to-peak output ripple voltage.

SHORT-CIRCUIT CURRENT LIMIT — The output current of the regulator measured with the output shorted to the negative supply.

STANDBY CURRENT DRAIN — The supply current drawn by the regulator under no output load and no reference voltage load.

TEMPERATURE STABILITY — The percent change in output voltage over a specified ambient temperature range.

With respect to the output voltage temperature coefficient, particularly in the case of 3-terminal regulators, the relevant temperature is the junction temperature, not the ambient temperature. This means an estimate must be made of worst-case operating junction temperatures for each application. Fortunately, these devices are well-characterized by their thermal characteristics, simplifying this task.

Operation of a regulator at, or near, its dropout voltage — or minimum permissible input-to-output voltage differential — must take into account the absolute worst-case minimum input voltage, including any ripple voltage present.

All currently used 3-terminal regulators provide internal protection to guard against the more commonly experienced failure modes. These are discussed in Chapter 2. In extraordinary situations, however, certain additional precautions are essential to avoid damage to the device. A voltage supply connected to the output which exceeds the input voltage is one such situation. If the input shorts to ground, the larger voltage supply at the output causes a reversed current flow through the regulator, probably destroying the device. If using an auxilliary supply at the output of a regulator, it may be necessary to isolate the input from a possible short with a series diode. It is also essential that the normal output voltage of the regulator be greater than the second power source.

For the 723 regulator, ripple rejection is specified over a 50 Hz to 10 kHz frequency range; but 120 Hz only for all 3-terminal regulators. Characteristic curves, however, are included to indicate the ripple rejection expected at any specific frequency up to 100 kHz. Note also that ripple rejection for the 3-terminal regulators is specified at a relatively high load current when compared to their allowed maximum. A particularly important point is that some 3-terminal devices exhibit a ripple rejection figure which degrades considerably as the load current is increased. This is due to self-heating of the monolithic chip which has an adverse effect on the regulator reference voltage. Since the chip thermal time constant is comparable to the ripple voltage period, ripple rejection is degraded. In the chip layout of Fairchild regulators, care was taken to ensure minimal thermal interaction from high dissipation areas of the chip to critical areas such as the voltage reference supply and the error amplifier input.

For fixed voltage applications, the preferred device is a 3-terminal regulator, from the 78L, 78M or 7800 series exhibiting the lowest current/power ratings consistent with worst-case requirements of the application.

The 7600 series offers the most economical means of powering small and medium size analog computing systems, and the 79E series effectively covers the needs of emitter-coupled logic systems.

The universal 723 is not only capable of giving precision regulator performance in all the above applications, but can be equally efficient in more unusual applications; e.g., both positive and negative, high voltage regulators, very high line rejection regulators, low input/output differential voltage regulators, and many others detailed in Chapter 8.

TYPE NO.	PACKAGE	MAX LOAD CURRENT A	OUTPUT VOLTAGE V	$P_{D(MAX)}$ FREE AIR W	$P_{D(MAX)}$ INF. HEAT SINK W	MAX LOAD REGULATION (ZERO TO MAX I_L)	MAX LINE REGULATION (OVER A NOMINAL V_{IN} RANGE)
78XX	TO-3	1.0	Fixed (See p 2-12)	3.5	15	1%	1%
78XXC	TO-3			3.0	15	2%	2%
78XXC	TO-220			2.0	15	2%	2%
78MXX	TO-39	0.5	Fixed (See p 2-12)	1.0	5.0	1%	1%
78MXXC	TO-39			1.0	5.0	2%	2%
78MXXC	TO-220			1.0	5.0	2%	2%
78LXXC	TO-92	0.1	Fixed	0.7	1.7	2%	2%
78LXXC	TO-39			0.8	2.8	2%	2%
79EXX	TO-3	3.0	Fixed (Negative)	3.5	15	1%	1%
79EXXC	TO-3			3.0	15	1%	1%
76XX	TO-100	0.15	Fixed/Adj	0.8	2.0	2%	2%
76XX	Power DIP			2.3	5.0	2%	2%
723	TO-100	0.15	Adjustable	0.85	2.5	0.5%	0.2%
723	TO-116			1.00		0.5%	0.2%
723C	TO-100			0.85	2.5	0.6%	0.5%
723C	TO-116			1.00		0.6%	0.5%
104	TO-100	0.025	Adjustable (Negative)	0.5		0.1%	1%
304	TO-100			0.5		0.1%	1%
105	TO-99	0.045	Adjustable	0.5		0.2%	1%
305	TO-99	0.045		0.5		0.2%	1%
305A	TO-99	0.045		0.5		0.2%	1%
376	Mini-DIP	0.025		0.45		0.2%	1%
109	TO-3	1.0	5.0	3.5	20	2%	1%
209	TO-3			3.5	20	2%	1%
309	TO-3			3.0	20	2%	1%

Table 1-1 Monolithic IC Voltage Regulators Selection Guide

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IN THIS CHAPTER:

- INTRODUCTION
- VOLTAGE REFERENCE
- ERROR AMPLIFIER
- THERMAL OVERLOAD PROTECTION
- FUNCTIONAL DESCRIPTION
- TESTING PHILOSOPHY
- CONSENSED SPECIFICATIONS
- TYPICAL PERFORMANCE CURVES
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- PACKAGING AND CONNECTION DIAGRAMS
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CHAPTER 2
7800/78M00 Positive, 3-Terminal Voltage Regulators

INTRODUCTION

The 7800 series circuits are self contained, 3-terminal regulators specifically intended for use in a wide variety of fixed output voltage applications. The combination of internal current limiting, safe area compensation, and thermal shutdown makes these devices immune to the failure modes normally associated with power regulator applications.

Two families of positive 3-terminal regulators are available differing only in their maximum output current rating.

- 78M00 series in a hermetic TO-39 package, or molded TO-220 package, rated at 0.5 A.
- 7800 series in a hermetic TO-3 package, or molded TO-220 package, rated at 1.0 A.

Since the electrical characteristics of the two families are virtually identical, only the 7800 series is described. Regulators are available in fixed output voltage options from 5 to 24 V. These options are first determined during the manufacturing process by the selection of an internal resistor matrix, RA, in the block diagram of *Figure 2-1* and, second, for an operating junction temperature range of –55 to +150°C for the 7800 or 0 to +125°C for the 7800C.

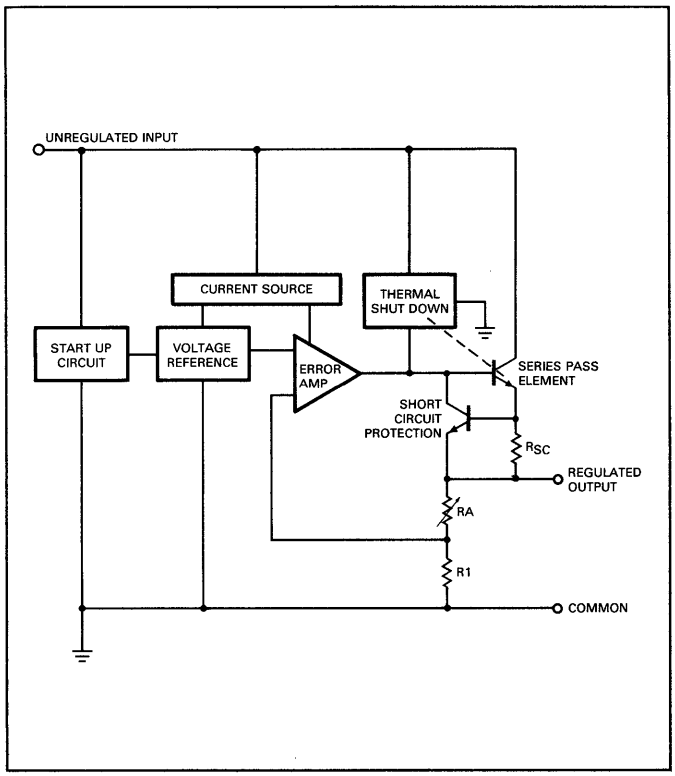


Fig. 2-1 Block Diagram of the 3-Terminal Regulator

Output voltages are specified at approximately ±4% of the nominal voltage. In applications where closer tolerance outputs are required, external components may be added allowing the output voltage to be adjusted precisely. External pass transistors may be added to increase the current handling capabilities of the regulator. These, and other applications are illustrated in Chapter 3.

VOLTAGE REFERENCE

Temperature compensated Zener diodes are normally used as reference elements in IC voltage regulators; however, these diodes exhibit breakdown voltages above 6 V, thus imposing a lower limit on the input voltage to the regulator. Zeners also require excessively tight process controls to maintain a satisfactory tolerance for any nonadjustable (3-terminal) application.

A voltage reference which does not use a Zener diode has been developed from the predictable temperature, current and voltage relationships in an emitter base junction. To obtain a temperature compensated reference voltage, the positive temperature coefficient of an emitter base voltage differential between two transistors operated at different current densities is added to the negative temperature coefficent of emitter base voltage. *Figure 2-2* shows such a reference. Transistor Q1 operates at a considerably higher current level than Q2 and the emitter base voltage differential is amplified by the voltage gain of transistor Q2.

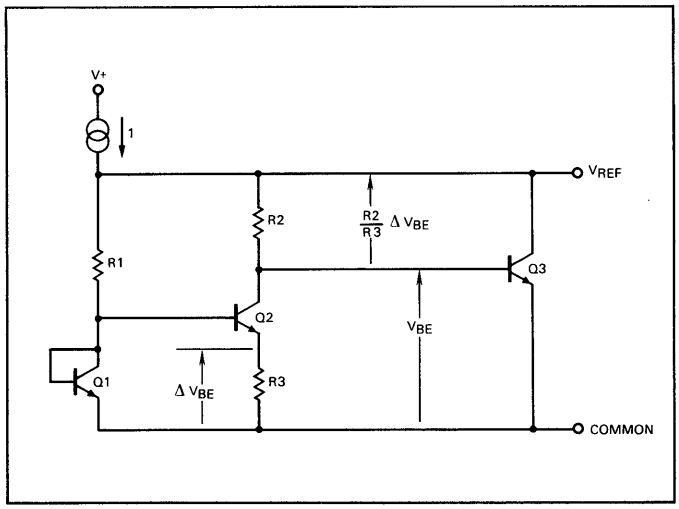


Fig. 2-2 Voltage Reference Based on Base-Emitter Voltage

The reference voltage can be expressed as follows.

$$V_{REF} = V_{BE3} + I_{CQ2}\ R2 + I_{BQ3}\ R2$$

$$V_{REF} = V_{BE3} + \frac{R2}{R3}\ (\Delta V_{BE}) + I_{BQ3}\ R2$$

$$V_{REF} = V_{BE3} + \frac{R2}{R3}\ \left(\frac{KT}{q}\ \text{Ln}\ \frac{J1}{J2}\right) + I_{BQ3}\ R2$$

$$V_{REF} \cong V_{BE3} + \frac{R2}{R3}\ \left(\frac{KT}{q}\ \text{Ln}\ \frac{R2}{R1}\right)$$

where J is current density.

By selecting the resistor ratios R2:R3 and R2:R1, a low voltage, temperature compensated reference is obtained.

Figure 2-3 shows a simplified schematic of the actual circuit used in the regulator. Transistors Q4, Q5 and Q6 are added to increase the reference level to 5 V.

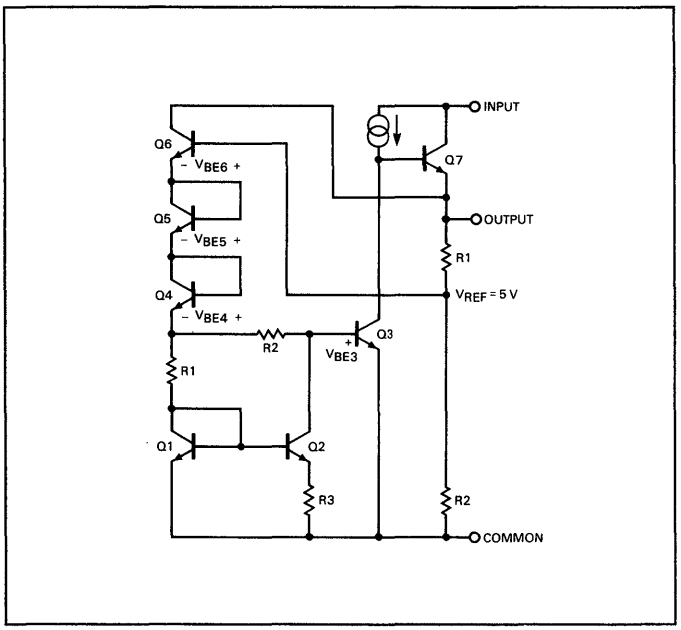


Fig. 2-3 Simplified Circuit for the Regulator

The reference then becomes:

$$V_{REF} = (V_{BE3} + V_{BE4} + V_{BE5} + V_{BE6}) + \frac{R2}{R3}\left(\frac{KT}{q}\,Ln\,\frac{R2}{R1}\right)$$

Resistors R1, R2 and R3 are selected so that the reference voltage is constant over the temperature range and also has a nominal value of 5 V at room temperature.

An extremely tight reference voltage tolerance is, therefore, obtained without special process controls. This is because base emitter characteristics are better understood and more predictable than Zener references. Also, monolithic circuits lend themselves more readily to resistor and transistor matching. An external adjustment to trim output voltage is unnecessary in most applications. An additional benefit is that this reference has low noise output compared to a Zener reference, thus eliminating the need for a large bypass capacitor to remove noise.

ERROR AMPLIFIER

An error amplifier (see *Figure 2-1)* compares the output feedback signal with the voltage reference and corrects the output by the amount of the error. The regulator circuit shown in *Figure 2-3* has the error amplifier combined with the voltage reference. The advantage is that noise at the regulator output is minimized since the amplifier and reference are no longer separate sources of noise. In *Figure 2-3,* transistor Q3 is used as the error amplifier; and at the same time, its base emitter voltage is used as part of the reference.

A current source is used as the active load to the error amplifier. A negative feedback path is provided through feedback resistors R1 and R2. If the voltage at the output increases due to a reduction in load current, that voltage change is transmitted to the base of transistor Q3. Transistor Q3, then, conducts more, effectively reducing the base drive to the output transistor by current steering. The result is a decrease in output voltage, and this tends to correct the change in output voltage due to the load current change. As the loop settles, an equilibrium value at the output is reached. The output voltage is derived using the following formula.

$$\text{Output Voltage} = V_{REF}\left(\frac{R1 + R2}{R2}\right)$$

Varying the resistor ratio R1 + R2:R2 yields different fixed output voltages.

THERMAL OVERLOAD PROTECTION

One of the benefits of including the series pass transistor on the chip is that it is then possible to incorporate both thermal and current overload protection.

Low power IC regulators usually rely on current limiting for overload protection as there is no practical way to sense junction temperature in a separate pass transistor. Excessive heating of the pass transistor, then, becomes one of the primary failure mechanisms of these solid state regulators. A thermal overload protection circuit in a monolithic regulator which contains the pass transistor limits the maximum temperature of the transistor junction. This limiting is independent of input voltage and the type of overload/degree of package heat sinking.

The base emitter junction of a transistor limiter is used to sense the temperature of the chip. The temperature limiter normally is biased below its activation threshold so that it does not affect circuit operation. If the chip temperature rises to its maximum limit due to a load fault or other conditions, the temperature limiter turns on. This removes the base drive to the output transistors and shuts down the regulator, preventing further chip heating.

FUNCTIONAL DESCRIPTION

Figure 2-4 shows the equivalent schematic diagram of the IC regulator. Transistors Q1 through Q6 and resistors R1, R2 and R3 constitute a 5 V, temperature compensated internal voltage reference for the regulator. The base emitter voltages of transistors Q3, Q4, Q5 and Q6 provide the *negative* temperature coefficient component of the output voltage. The voltage drop across R2 is the *positive* temperature coefficient component. This is derived from the differential base emitter voltages across transistors Q1 and Q2, which operate at a current ratio of $\approx$20 to 1. The output voltage of the regulator is determined by selecting a ratio from a resistor matrix which multiplies the reference voltage. The current required by the load is supplied from the input terminal through the series pass transistor Q17, driven by transistor Q16. Transistor Q3 is the gain stage providing regulation. Its effective gain is increased by the pnp transistor Q11 which acts as a buffer to drive the active collector load formed by the pnp current source transistor pair, Q8 and Q9.

The current from Q8 and Q9 is set up by the current through resistor R1. During regulator turn on, the current in R1 flows first through transistor Q13 — part of a start up circuit containing Zener diode D1, transistors Q12 and Q13, and resistors R5, R6 and R7. After the device is in regulation, Q13 is biased off and the regulator takes over setting the current in R1, which now flows through Q5 and Q10. This start up circuit is required since the regulator which eventually is to supply the current in R1 is off during initial device turn on.

Thermal limiting is accomplished by transistor Q14. The base of Q14 is clamped to $\approx$0.4 V by the resistive divider string R5, R6 and R7 in the start up circuit. As the junction temperature rises, the turn on threshold of Q14 decreases. At a junction temperature of $\approx$175°C, transistor Q14 turns on and the base current drive to the drive transistor is removed. This shuts down the pass transistor and prevents further increases in chip temperature.

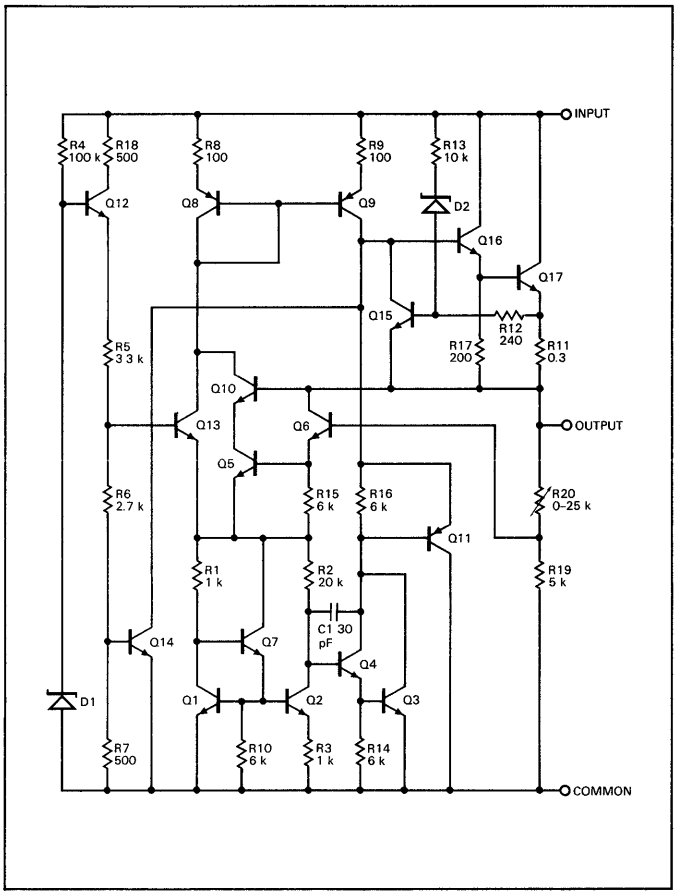


Fig. 2-4 Circuit Schematic of the 3-Terminal Regulator

Whereas this form of thermal protection is effective for *persistent* overloads which would cause excessive chip temperature, it is ineffective against *instantaneous* overloads which could result in a secondary breakdown of the pass transistor or damage to metal interconnections due to abnormally high current density. Transistor Q15 and resistor R11 protect against instantaneous overloads by limiting output current. If the output current rises to a high level, the current through R11 will turn on Q15, thus shunting base current away from the driver transistor and preventing further increases in output current.

To ensure that the output transistor operates within its forward safe area, a compensating network is included to limit the instantaneous power in the output transistor. When the voltage across the pass transistor exceeds 8 V, current through resistor R13 and diode D2 reduces the limiting current. As illustrated in *Figure 2-5,* the higher the voltage across the pass transistor, the lower the limiting current.

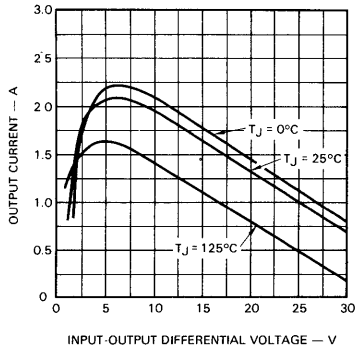


Fig. 2-5 Input-Output Differential vs Current Limit

An MOS capacitor of 30 pF is incorporated on the chip to ensure stable operation without the need for a bypass capacitor on the output.

Table 2-1 shows the typical performance characteristics of the regulator.

PARAMETER	TEST CONDITIONS (V_{OUT} = 5 V, T_J = 25°C, V_{IN} = 10 V AND I_{OUT} = 500 mA UNLESS OTHERWISE SPECIFIED)	CHARACTERISTICS 7805	78M05
OUTPUT TOLERANCE		±4%	±4%
QUIESCENT CURRENT		4.2 mA	4.5 mA
OUTPUT RESISTANCE	f = 1 kHz	20 mΩ	20 mΩ
LINE REGULATION	7 V ≤ V_{IN} ≤ 25 V	0.005%/V	.0033%/V
TEMPERATURE DRIFT	-20°C ≤ T_J ≤ 125°C	0.022%/°C	0.02%/°C
MINIMUM INPUT VOLTAGE	I_{OUT} = 1A (.5 A for 78M05)	7.0 V	7.0 V
OUTPUT NOISE VOLTAGE	10 Hz ≤ f ≤ 100 kHz	40 µV	40 µV
RIPPLE REJECTION	f = 120 Hz	78 dB	80 dB
THERMAL RESISTANCE (JUNCTION TO CASE)	TO-3 PACKAGE TO-220 PACKAGE TO-39 PACKAGE	4°C/W 4°C/W	 5°C/W 20°C/W

Table 2-1 Typical Characteristics (7805 and 78M05)

TESTING PHILOSOPHY

The 7800 series device is tested in a manner reflecting its intended usage. The input/output voltage differential used to test each device in the series takes into account all the variations in a nominal, unregulated dc source.

For example, the 7812 is tested with a 7 V input/output differential which considers the following parameters and their variations.

- Minimum device input/output differential
- Power supply ripple
- Line voltage tolerance
- Diode drop variation and source impedance variations

Table 2-2 presents the considerations resulting from the combination of all these factors and tolerances.

Therefore, not only is the 7812 tested with an additional guard band of 0.5 V (19 V total), but the input voltage range used for testing allows greater input voltage variation than found in actual use conditions. Other devices in the 7800 series are tested with the same practical considerations.

CONDENSED SPECIFICATIONS

The electrical characteristics listed below pertain specifically to the 7800 and 7800C series regulators. The 78M00 and 78M00C series have similar characteristics except that nominal and peak output currents are 200 mA and 750 mA respectively, instead of 500 mA and 2.2 A for the 7800 and 7800C.

$V_{O(max)}$ =	12.5 V
$V_{IN} - V_O$	2 V
Total	14.5 V
Line Variation = (10%)	1.4 V
Total	15.9 V
Ripple = (10%)	1.6 V
Total	17.5 V
R_S and V_d =	1.0 V
Total	18.5 V

Table 2-2 Derivation of Test Voltage

ABSOLUTE MAXIMUM RATINGS (7800, 7800C)

Input Voltage (5 V through 18 V)		35 V
(24 V)		40 V
Internal Power Dissipation (Note 1)		Internally Limited
Storage Temperature Range		−65°C to +150°C
Operating Junction Temperature Range	7800	−55°C to +150°C
	7800C	0°C to +125°C
Lead Temperature (Soldering, 60 second time limit) TO-3 Package		300°C
(Soldering, 10 second time limit) TO-220 Package		230°C

ABSOLUTE MAXIMUM RATINGS (78M00, 78M00C)

Input Voltage (5 V through 15 V)	35 V
(20 V, 24 V)	40 V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	−65°C to +200°C
Operating Junction Temperature Range	
Military (78M00)	−55°C to +175°C
Commercial (78M00C)	0°C to +175°C (TO-39), 0°C to +125°C (TO-220)
Lead Temperature (Soldering, 60 second time limit) TO-39 Package	300°C
(Soldering, 10 second time limit) TO-220 Package	230°C

NOTE 1: Thermal resistance of the packages (without a heat sink)

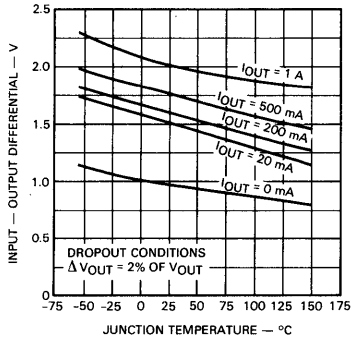
Junction-to-Case

TO-3 Package	4°C/W
TO-220 Package	(78M00) 5°C/W, (7800) 4°C/W
TO-39 Package	20°C/W

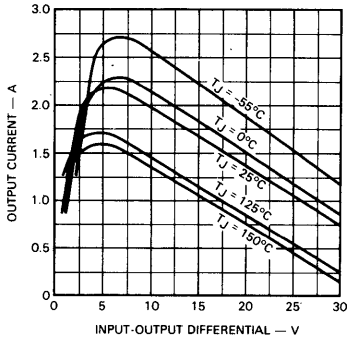
Junction-to-Ambient

TO-3 Package	35°C/W
TO-220 Package	50°C/W
TO-39 Package	150°C/W

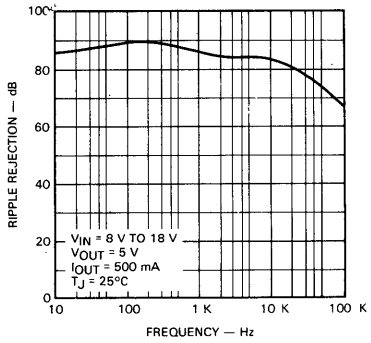
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



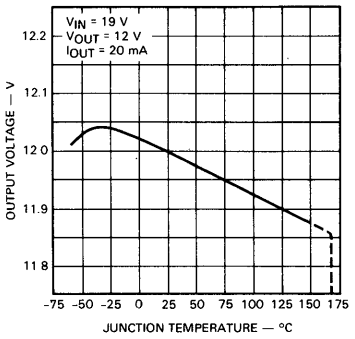
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT/OUTPUT DIFFERENTIAL VOLTAGE



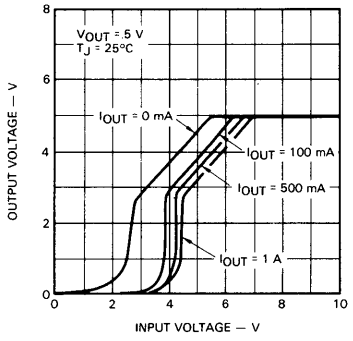
RIPPLE REJECTION AS A FUNCTION OF FREQUENCY



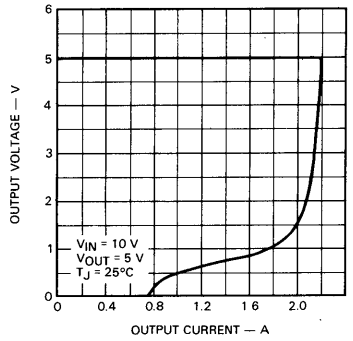
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



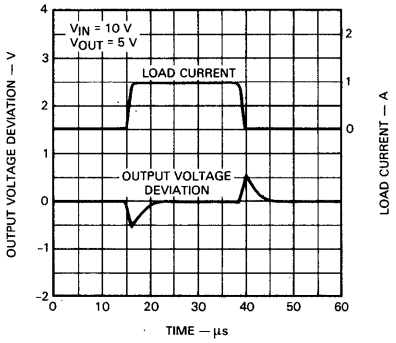
DROPOUT CHARACTERISTICS



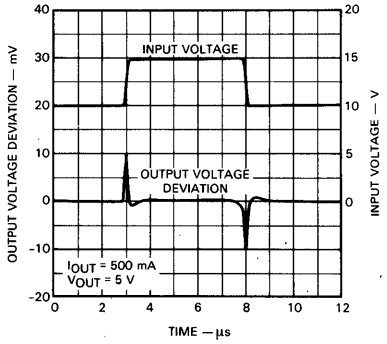
CURRENT LIMITING CHARACTERISTICS



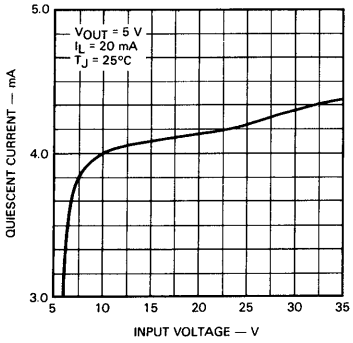
LOAD TRANSIENT RESPONSE



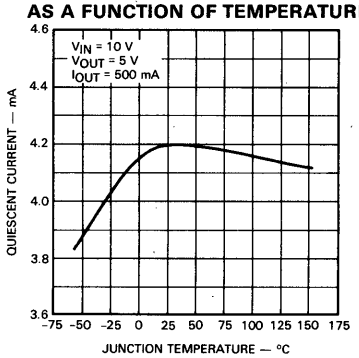
LINE TRANSIENT RESPONSE



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

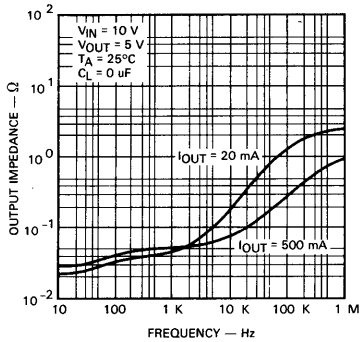


Fig. 2-6 Typical Performance Curves For 7800 Series

ELECTRICAL CHARACTERISTICS

V_{IN} = 10 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7805) 0°C ≤ T_J ≤ 125°C (7805C) unless otherwise specified

PARAMETER		CONDITIONS		7805			7805C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage		T_J = 25°C		4.8	5.0	5.2	4.8	5.0	5.2	V
Line Regulation		T_J = 25°C	7.0 V ≤ V_{IN} ≤ 25V		3.0	50		3.0	100	mV
			8.0 V ≤ V_{IN} ≤ 12 V		1.0	25		1.0	50	mV
Load Regulation		T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A		15	50		15	100	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		5.0	25		5.0	50	mV
Output Voltage		8.0 V (7.0 V for 7805C) ≤ V_{IN} ≤ 20 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		4.65		5.35	4.75		5.25	V
Quiescent Current		T_J = 25°C			4.2	6.0		4.2	8.0	mA
Quiescent Current Changes	with line	8.0 V (7.0 V for 7805C) ≤ V_{IN} ≤ 25 V				0.8			1.3	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A				0.5			0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			40		μV
Long Term Stability						20			20	mV
Ripple Rejection		f = 120 Hz, 8.0 V ≤ V_{IN} ≤ 18 V		68	78		62	78		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance		f = 1.0 kHz			17			17		mΩ
Short Circuit Current		T_J = 25°C			750			750		mA
Peak Output Current		T_J = 25°C			2.2			2.2		A
Average TC of Output Voltage		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7800)			−1.1					mV/°C
		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7800C)						−1.1		mV/°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 11 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7806) 0°C ≤ T_J ≤ 125°C (7806C) unless otherwise specified

PARAMETER		CONDITIONS		7806			7806C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage		T_J = 25°C		5.75	6.0	6.25	5.75	6.0	6.25	V
Line Regulation		T_J = 25°C	8.0 V ≤ V_{IN} ≤ 25 V			5.0			120	mV
			9.0 V ≤ V_{IN} ≤ 13 V			1.5			60	mV
Load Regulation		T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A			14			120	mV
			250 mA ≤ I_{OUT} ≤ 750 mA			4.0			60	mV
Output Voltage		9.0 V (8.0 V for 7806C) ≤ V_{IN} ≤ 21 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P≤ 15 W		5.65		6.35	5.7		6.3	V
Quiescent Current		T_J = 25°C			4.3	6.0		4.3	8.0	mA
Quiescent Current Change	with line	9.0 V (8.0 V for 7806C) ≤ V_{IN} ≤ 25 V				0.8			1.3	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A				0.5			0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			45			45		μV
Long Term Stability						24			24	mV
Ripple Rejection		f = 120 Hz, 9.0 V ≤ V_{IN} ≤ 19 V		65	75		59	75		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance		f = 1.0 kHz			19			19		mΩ
Short Circuit Current		T_J = 25°C			550			550		mA
Peak Output Current		T_J = 25°C			2.2			2.2		A
Average TC of Output Voltage		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7806)			−0.8					mV/°C
		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7806C)						−0.8		mV/°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 14 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7808) 0°C ≤ T_J ≤ 125°C (7808C) unless otherwise specified

PARAMETER		CONDITIONS		7808			7808C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage		T_J = 25°C		7.7	8.0	8.3	7.7	8.0	8.3	V
Line Regulation		T_J = 25°C	10.5 V ≤ V_{IN} ≤ 25 V		6.0	80		6.0	160	mV
			11 V ≤ V_{IN} ≤ 17 V		2.0	40		2.0	80	mV
Load Regulation		T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A		12	80		12	160	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	40		4.0	80	mV
Output Voltage		11.5 V (10.5 V for 7808C) ≤ V_{IN} ≤ 23 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		7.6		8.4	7.6		8.4	V
Quiescent Current		T_J = 25°C			4.3	6.0		4.3	8.0	mA
Quiescent Current Change	with line	11.5 V (10.5 V for 7808C) ≤ V_{IN} ≤ 25 V				0.8			1.0	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A				0.5			0.5	mA
Output Noise Voltage		T_A = 25°C, 19 Hz ≤ f ≤ 100 kHz			52			52		μV
Long Term Stability						32			32	mV
Ripple Rejection		f = 120 Hz, 11.5 V ≤ V_{IN} ≤ 21.5 V		62	72		56	72		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance		f = 1.0 kHz			16			16		mΩ
Short Circuit Current		T_J = 25°C			450			450		mA
Peak Output Current		T_J = 25°C			2.2			2.2		A
Average TC of Output Voltage		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7808)			−0.8					mV/°C
		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7808C)						−0.8		mV/°C

2

ELECTRICAL CHARACTERISTICS

V_{IN} = 19 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7812) 0°C ≤ T_J ≤ 125°C (7812C) unless otherwise specified

PARAMETER		CONDITIONS		7812			7812C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage		T_J = 25°C		11.5	12	12.5	11.5	12	12.5	V
Line Regulation		T_J = 25°C	14.5 V ≤ V_{IN} ≤ 30 V		10	120		10	240	mV
			16 V ≤ V_{IN} ≤ 22 V		3.0	60		3.0	120	mV
Load Regulation		T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A		12	120		12	240	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	60		4.0	120	mV
Output Voltage		15.5 V (14.5 V for 7812C) ≤ V_{IN} ≤ 27 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		11.4		12.6	11.4		12.6	V
Quiescent Current		T_J = 25°C			4.3	6.0		4.3	8.0	mA
Quiescent Current Change	with line	15 V (14.5 V for 7812C) ≤ V_{IN} ≤ 30 V				0.8			1.0	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A				0.5			0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			75			75		μA
Long Term Stability						48			48	mA
Ripple Rejection		f = 120 Hz, 15 V ≤ V_{IN} ≤ 25 V		61	71		55	71		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance		f = 1.0 kHz			18			18		mΩ
Short Circuit Current		T_J = 25°C			350			350		mA
Peak Output Current		T_J = 25°C			2.2			2.2		A
Average TC of Output Voltage		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7812)			−1.0					mV/°C
		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7812C)						−1.0		mV/°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 23 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7815) 0°C ≤ T_J ≤ 125°C (7815C) unless otherwise specified

PARAMETER	CONDITIONS		7815			7815C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	T_J = 25°C		14.4	15	15.6	14.4	15	15.6	V
Line Regulation	T_J = 25°C	17.5 V ≤ V_{IN} ≤ 30 V		11	150		11	300	mV
		20 V ≤ V_{IN} ≤ 26 V		3.0	75		3.0	150	mV
Load Regulation	T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A		12	150		12	150	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		4.0	75		4.0	75	mV
Output Voltage	18.5 V (17.5 V for 7815 C) ≤ V_{IN} ≤ 30 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		14.25		15.75	14.25		15.75	V
Quiescent Current	T_J = 25°C			4.4	6.0		4.4	8.0	mA
Quiescent Current Change	with line	18.5 V (17.5 V for 7815C) ≤ V_{IN} ≤ 30 V			0.8			1.0	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A			0.5			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			90			90		μV
Long Term Stability					60			60	mV
Ripple Rejection	f = 120 Hz, 18.5 V ≤ V_{IN} ≤ 28.5 V		60	70		54	70		dB
Dropout Voltage	I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance	f = 1.0 kHz			19			19		mΩ
Short Circuit Current	T_J = 25°C			230			230		mA
Peak Output Current	T_J = 25°C			2.1			2.1		A
Average TC of Output Voltage	I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7815)			−1.0					mV/°C
	I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7815C)						−1.0		mV/°C

ELECTRICAL CHARACTERISTICS

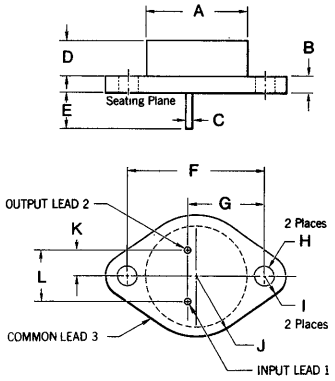
V_{IN} = 27 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7818) 0°C ≤ T_J ≤ 125°C (7818C) unless otherwise specified

PARAMETER	CONDITIONS		7818			7818C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	T_J = 25°C		17.3	18	18.7	17.3	18	18.7	V
Line Regulation	T_J = 25°C	21 V ≤ V_{IN} ≤ 33 V		15	180		15	360	mV
		24 V ≤ V_{IN} ≤ 30 V		5.0	90		5.0	180	mV
Load Regulation	T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A		12	180		12	360	mV
		250 mA ≤ I_{OUT} ≤ 750 mA		4.0	90		4.0	180	mV
Output Voltage	22 V (21 V for 7818C) ≤ V_{IN} ≤ 33 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		17.1		18.9	17.1		18.9	V
Quiescent Current	T_J = 25°C			4.5	6.0		4.5	8.0	mA
Quiescent Current Change	with line	22 V (21 V for 7818 C) ≤ V_{IN} ≤ 33 V			0.8			1.0	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A			0.5			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			110			110		μA
Long Term Stability					72			72	mV
Ripple Rejection	f = 120 Hz, 22 V ≤ V_{IN} ≤ 32 V		59	69		53	69		dB
Dropout Voltage	I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance	f = 1.0 kHz			22			22		mΩ
Short Circuit Current	T_J = 25°C			200			200		mA
Peak Output Current	T_J = 25°C			2.1			2.1		A
Average TC of Output Voltage	I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7818)			−1.0					mV/°C
	I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7818C)						−1.0		mV/°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 33 V, I_{OUT} = 500 mA, −55°C ≤ T_J ≤ 150°C (7824) 0°C ≤ T_J ≤ 125°C (7824C) unless otherwise specified

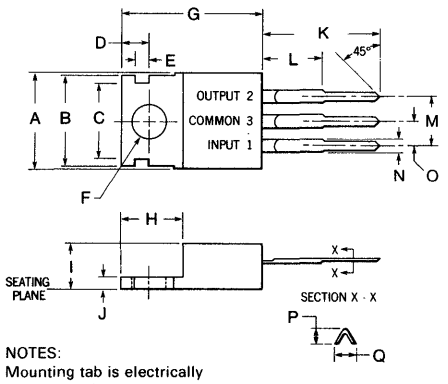
PARAMETER		CONDITIONS		7824			7824C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage		T_J = 25°C		23	24	25	23	24	25	V
Line Regulation		T_J = 25°C	27 V ≤ V_{IN} ≤ 38 V		18	240		18	480	mV
			30 V ≤ V_{IN} ≤ 36 V		6.0	120		6.0	240	mV
Load Regulation		T_J = 25°C	5.0 mA ≤ I_{OUT} ≤ 1.5 A		12	240		12	480	mV
			250 mA ≤ I_{OUT} ≤ 750 mA		4.0	120		4.0	240	mV
Output Voltage		28 V (27 V for 7824C) ≤ V_{IN} ≤ 38 V 5.0 mA ≤ I_{OUT} ≤ 1.0 A P ≤ 15 W		22.8		25.2	22.8		25.2	V
Quiescent Current		T_J = 25°C			4.6	6.0		4.6	8.0	mA
Quiescent Current Change	with line	28 V (27 V for 7824C) ≤ V_{IN} ≤ 38 V				0.8			1.0	mA
	with load	5.0 mA ≤ I_{OUT} ≤ 1.0 A				0.5			0.5	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			170			170		μV
Long Term Stability						96			96	mV
Ripple Rejection		f = 120 Hz, 28 V ≤ V_{IN} ≤ 38 V		56	66		50	66		dB
Dropout Voltage		I_{OUT} = 1.0 A, T_J = 25°C			2.0			2.0		V
Output Resistance		f = 1.0 kHz			28			28		mΩ
Short Circuit Current		T_J = 25°C			150			150		mA
Peak Output Current		T_J = 25°C			2.1			2.1		A
Average TC of Output Voltage		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 150°C (7824)			−1.5					mV/°C
		I_{OUT} = 5.0 mA, 0°C ≤ T_J ≤ 125°C (7824C)						−1.5		mV/°C



NOTES:
Leads 1 and 2 electrically isolated from case
Case is electrically connected to common
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.835	20.45	31.21
B		0.135		3.43
C	0.038	0.048	0.965	1.12
D	0.205	0.325	5.20	8.25
E	0.312		7.92	
F	1.177	1.197	29.90	30.40
G	0.655	0.675	16.64	17.15
H	0.151	0.161	3.79	3.84
I		0.188		4.78
J		0.525		13.34
K	0.205	0.225	5.20	5.71
L	0.420	0.440	9.67	10.08

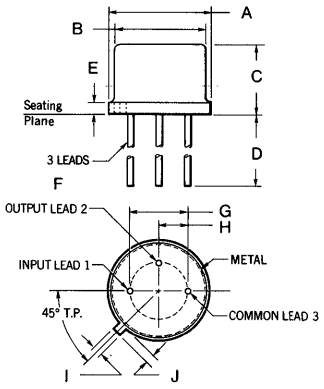
Fig. 2-7 JEDEC TO-3



NOTES:
Mounting tab is electrically connected to common
Package is molded with nickel-plated copper tab and leads
Package weight is 2.1 grams

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.395	0.410	10.03	10.41
B	0.365	0.385	9.27	9.77
C	0.300	0.320	7.62	8.13
D	0.100	0.120	2.54	3.05
E	0.040	0.060	1.02	1.52
F	0.141	0.145	3.58	3.68
G	0.575	0.600	14.6	15.24
H	0.235	0.265	5.97	6.73
I	0.160	0.190	4.06	4.83
J	0.020	0.055	0.508	1.40
K	0.500		12.70	
L		0.250		6.35
M	0.190	0.210	4.83	5.33
N	0.045	0.055	1.05	1.40
O	0.095	0.105	2.41	2.66
P	0.015	0.030	0.381	0.762
Q	0.020	0.045	0.508	1.43

Fig. 2-8 JEDEC TO-220



NOTES:
Leads are gold-plated over nickel-flash on steel
Lead 3 connected to case
Low thermal resistance
Package weight is 0.76 gram

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.350		0.370	8.51		9.39
B	0.315		0.335	8.00		8.51
C	0.240		0.260	6.10		6.60
D	0.500			12.70		
E			0.030			0.762
F	0.016		0.019	0.406		0.483
G		0.200			5.08	
H		0.100			2.54	
I	0.28		0.034	0.711		0.864
J	0.029		0.040	0.737		1.02

Fig. 2-9 JEDEC TO-39

	OUTPUT VOLTAGE	TO-3 TYPE	TO-3 PART NO.	TO-3 TYPE	TO-3 PART NO.	TO-220 TYPE	TO-220 PART NO.
7800/7800C	5 V	7805	7805KM	7805C	7805KC	7805C	7805UC
	6 V	7806	7806KM	7806C	7806KC	7806C	7806UC
	8 V	7808	7808KM	7808C	7808KC	7808C	7808UC
	12 V	7812	7812KM	7812C	7812KC	7812C	7812UC
	15 V	7815	7815KM	7815C	7815KC	7815C	7815UC
	18 V	7818	7818KM	7818C	7818KC	7818C	7818UC
	24 V	7824	7824KM	7824C	7824KC	7824C	7824UC

Fig. 2-10 Ordering Information

	OUTPUT VOLTAGE	TO-39 TYPE	TO-39 PART NO.	TO-39 TYPE	TO-39 PART NO.	TO-220 TYPE	TO-220 PART NO.
78M00/78M00C	5 V	78M05	78M05HM	78M05C	78M05HC	78M05C	78M05UC
	6 V	78M06	78M06HM	78M06C	78M06HC	78M06C	78M06UC
	8 V	78M08	78M08HM	78M08C	78M08HC	78M08C	78M08UC
	12 V	78M12	78M12HM	78M12C	78M12HC	78M12C	78M12UC
	15 V	78M15	78M15HM	78M15C	78M15HC	78M15C	78M15UC
	20 V	78M20	78M20HM	78M20C	78M20HC	78M20C	78M20UC
	24 V	78M24	78M24HM	78M24C	78M24HC	78M24C	78M24UC

Fig. 2-11 Ordering Information

NOTE: For more detailed information on the 78M00 Series Voltage Regulators — refer to the 78M00 Data Sheet.

LINEAR

CONTENTS AND SECTION SELECTOR

IN THIS CHAPTER:

- BYPASSING
- THERMAL CONSIDERATIONS
- TYPICAL APPLICATIONS

CHAPTER 3
7800/78M00 Positive, 3-Terminal Voltage Regulator Applications

BYPASSING

The monolithic 3-terminal regulator is particularly attractive in providing local on-card regulation because of the small number of external components required by the regulator. In the simplest, fixed output voltage application, a bypass capacitor of at least 0.22 μF placed across the regulator input terminals is all that is required to ensure stable operation.

The regulator output does not require bypassing for normal operation, although additional capacitance does improve the transient response of the supply. The regulator output impedance, typically less than 50 mΩ up to 1 kHz, increases as a function of frequency above 10 kHz. This is due to the gain of the regulator error amplifier rolling off above this frequency. A large tantalum capacitor of 47 μF connected across the regulator output terminals will maintain a low output impedance up to 1 MHz. If fast switching loads are to be driven, a ceramic capacitor should be placed in parallel across the tantalum to compensate for the rising impedance of the tantalum above 1 MHz. If such switching loads are distributed over a large area, the ceramic bypasses should also be distributed to minimize the isolating effects of wire inductance.

THERMAL CONSIDERATIONS

The thermal characteristics of the voltage regulator chips and packages determine that some form of heat sinking is mandatory whenever the power dissipation exceeds 1 W for the TO-39 package, 2 W for the TO-220 package, or 3 W for the TO-3 package. These basic characteristics are listed in *Table 3-1* and are shown graphically in *Figure 3-1*.

From the table, maximum permissible dissipation without a heat sink is derived by

$$\frac{T_{J\,(max)} - T_A}{\Theta_{JA}}$$

where T_A is the maximum ambient operating temperature. If the average dissipation of the device in question exceeds this figure, a heat sink will be required. The thermal resistance necessary for the heat sink may be found from

$$\Theta_{HS} = \frac{T_{J\,(max)} - T_A}{P_D} - \Theta_{JC}$$

where T_A is the maximum ambient operating temperature and P_D is the maximum average dissipation of the device in no case to exceed $P_{D(max)}$. Θ_{HS} is the thermal resistance of the heat sink to ambient, and includes the package/heat sink interface. Commercially available heat sinks are usually well characterized for this information. However, if a chassis or other convenient surface is to be used as the heat sink, use *Figure 3-2* to estimate the required surface area for a variety of commonly used materials. Surface area refers to both sides of the heat sink material.

As a further aid in determining which package/heat sink combination is best suited to a given application, the following nomograph *(Figure 3-3)* solves for Θ_{JA} from basic current, input/output voltage differential and ambient temperature information. The package thermal resistances have been

SERIES	7800	7800C	7800C	78M00	78M00C	78M00C	
PACKAGE	TO-3	TO-3	TO-220	TO-39	TO-39	TO-220	Units
Maximum Junction Temperature, $T_{J(max)}$	150	125	125	175	175	125	°C
Minimum Ambient Temperature, $T_{J(min)}$	-55	0	0	-55	0	0	°C
Thermal Resistance, Junction-to-Case, Θ_{JC}	4	4	4	20	20	5	°C/W
Thermal Resistance, Junction-to-Ambient, Θ_{JA}	35	35	50	150	150	50	°C/W
Maximum Allowable Dissipation, $P_{D\,(max)}$	15	15	15	5	5	5	W

Temperatures shown in the table are operating temperatures.

Storage temperatures are -65°C to 150°C for 7800 and 7800C,
-65°C to 200°C for 78M00 and 78M00C

Table 3-1 Basic Thermal Characteristics

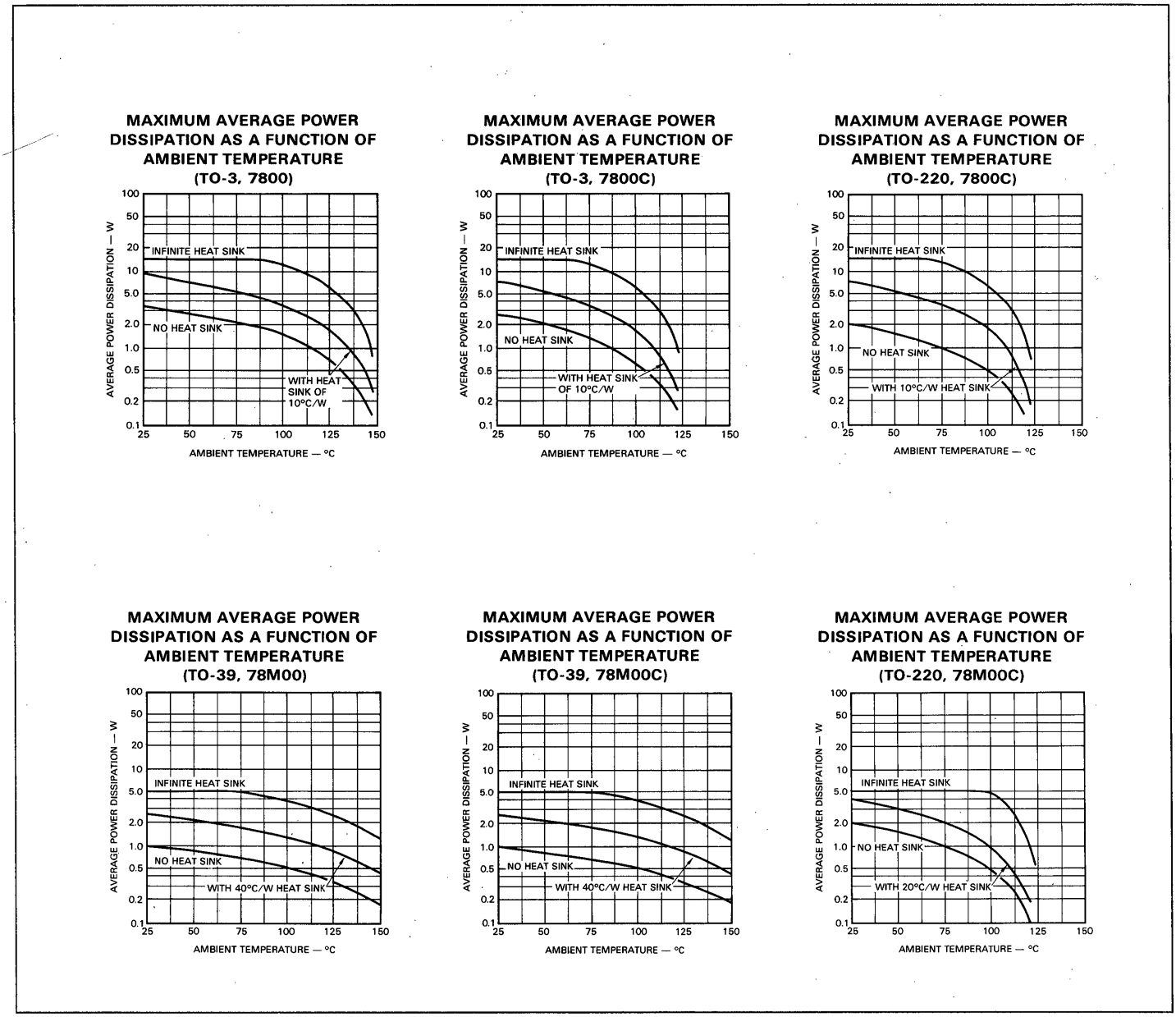


Fig. 3-1 Maximum Average Power Dissipation

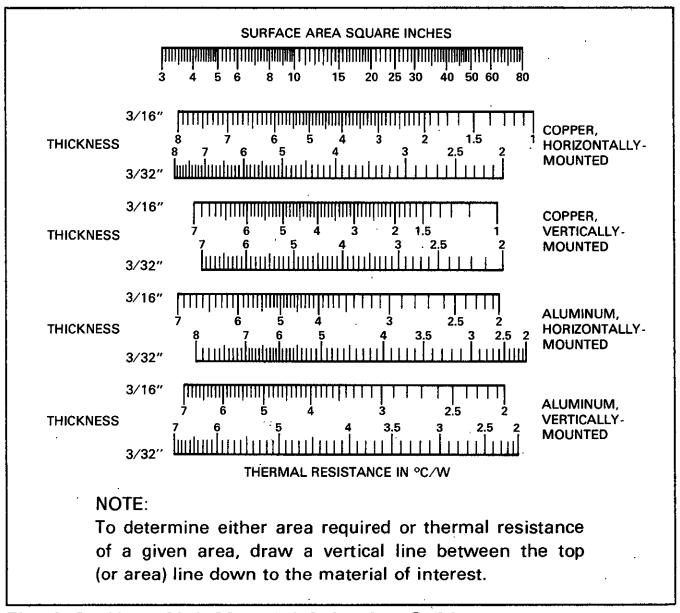


Fig. 3-2 Heat Sink Material Selection Guide

superimposed on the Θ_{JA} line E. If the required Θ_{JA} is less than Θ_{JC} for a package, then that package cannot be considered; for even if an infinite heat sink were possible, the junction temperature would exceed 125°C. If the required Θ_{JA} is greater than Θ_{JA} for a package, that package may be used without a heat sink. In all other cases a package/heat sink combination is necessary. Subtract Θ_{JC} for the preferred package from the required Θ_{JA} to arrive at the necessary heat sink thermal resistance Θ_{HS}.

The nomograph is based on a maximum junction temperature of 125°C. This will result in conservative figures for Θ_{JA} for the 78M00 and 78M00C in the TO-39 package as junction temperatures up to 175°C are permissible in these cases.

To use the nomograph, select the maximum load current on Line A and the maximum input/output voltage differential on Line D. The line joining these points intersects Line B at a point representing the maximum power dissipation. Join this Line B intersection to a point on Line C representing the maximum expected ambient temperature. Extend this line so it intersects Line E. The Line E intersection represents

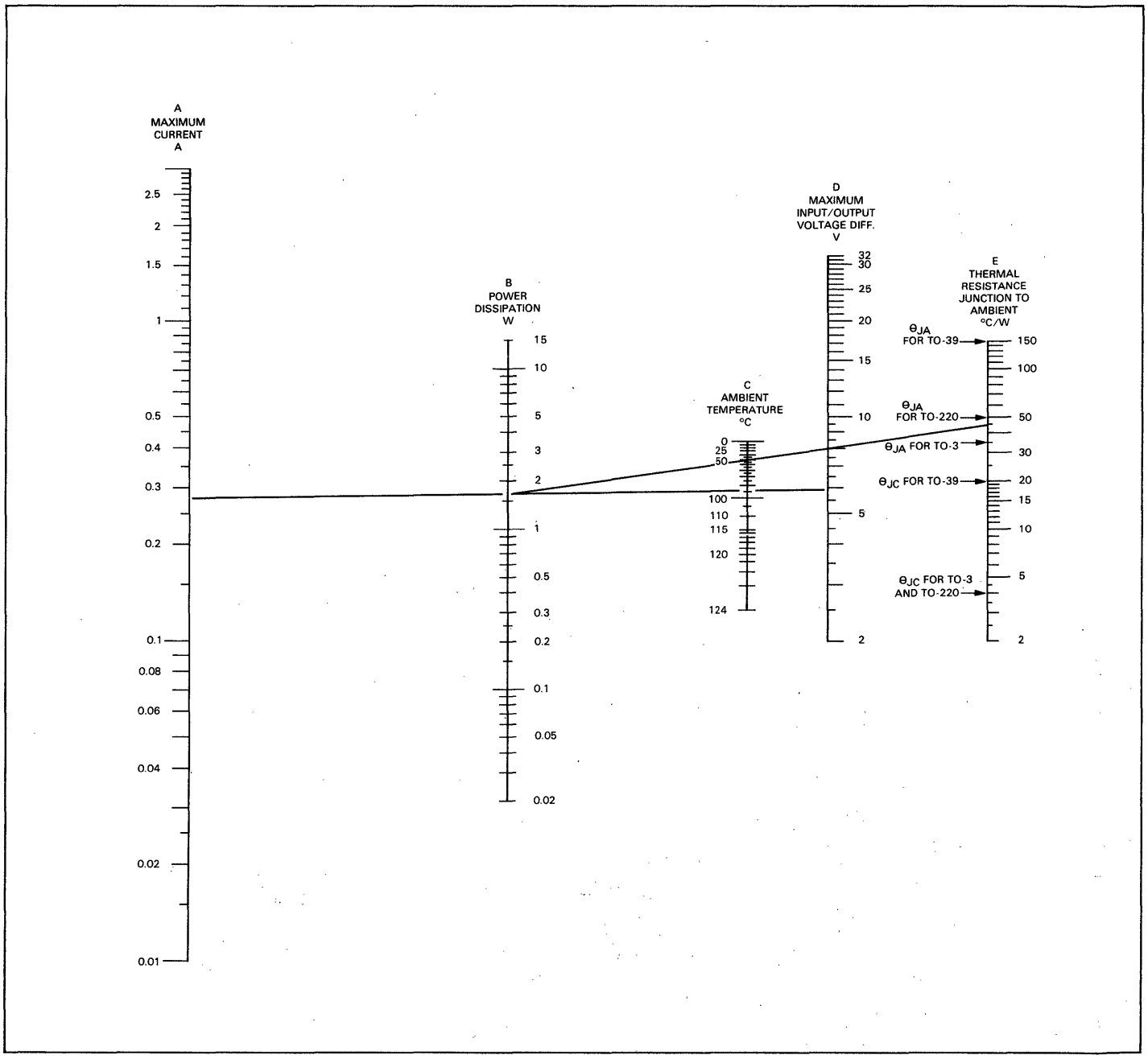


Fig. 3-3 Package/Heat Sink Nomograph

the total junction-to-ambient thermal resistance required for the particular application. If the Line E intersection falls above the junction-to-ambient thermal resistance, Θ_{JA}, no heat sink is required.

To determine the thermal resistance of a heat sink, subtract the junction-to-case thermal resistance, Θ_{JC}, of the selected package from the line E intersection:

- For TO-39, subtract 20°C/W
- For TO-3, subtract 4°C/W
- For TO-220, subtract 4°C/W

Example

Choose a regulator to supply 275 mA (max) with an input/output voltage differential of 6 V (max) at an ambient temperature of 50°C (max). Join the 275 mA point on Line A to the 6 V point on Line D. The intersection with Line B gives a power dissipation of 1.7 W. Join 1.7 W to the 50°C point on Line C and extrapolate to an intersection with Line E. This gives a total junction-to-ambient thermal resistance requirement of 45°C/W. There are three regulator package choices.

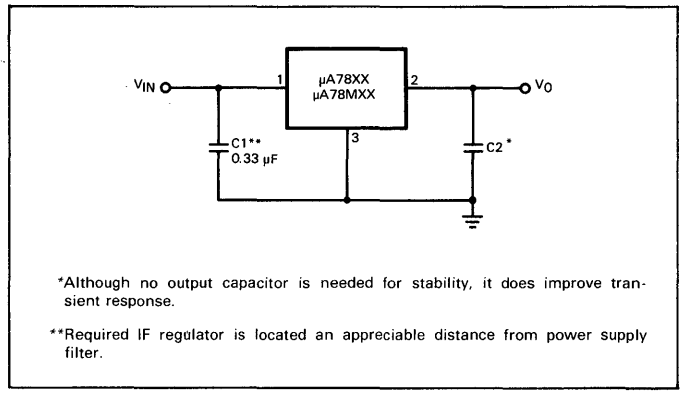
- A TO-39 package with a heat sink of 25°C/W thermal resistance (subtract 20°C/W Θ_{JC})
- A TO-220 package with a heat sink of 41°C/W thermal resistance (subtract 4°C/W Θ_{JC})
- A TO-3 package with no heat sink (45°C/W falls above Θ_{JA} for the TO-3).

TYPICAL APPLICATIONS

The versatility of the 7800 family of regulators may be increased beyond the basic 3-terminal use by the addition of external components. The following applications contain circuits which cover the range of 0.5 V to 30 V output, and output currents in excess of 10 A. Note that apart from power considerations, the 7800 and 78M00 devices are interchangeable in all applications.

Fixed Output Regulator

In this basic application, *Figure 3-4*, the last two digits of the device code specify the nominal output voltage. The insulating washer normally used when heat-sinking a power transistor may be omitted when mounting the regulator since the case of the device is at ground potential here. This is true unless circulating ground currents are a problem.



*Although no output capacitor is needed for stability, it does improve transient response.

**Required IF regulator is located an appreciable distance from power supply filter.

Fig. 3-4 Basic Fixed Output Regulator

Negative Output Voltage Regulators

If a fully floating transformer/rectifier/filter is available, the 3-terminal regulator may be used to supply a negative output voltage simply by grounding lead 2 and taking the output voltage from lead 3. In this case an insulating washer is required when mounting the regulator onto a grounded heat sink or chassis, since the case is at the same potential as the output voltage. (See *Figure 3-5a.*)

When a floating input is not available, the circuit shown in *Figure 3-5b* supplies a negative output voltage from bipolar supplies. The positive voltage source must be able to provide the base current requirements of the npn series pass device. If this current requirement is excessive, a Darlington npn series pair should be used to reduce the current requirement to acceptable levels. With this approach, very high currents can be regulated with a minimum of parts by using the full output current of the 3-terminal device and scaling the current and power capabilities of the other active devices accordingly.

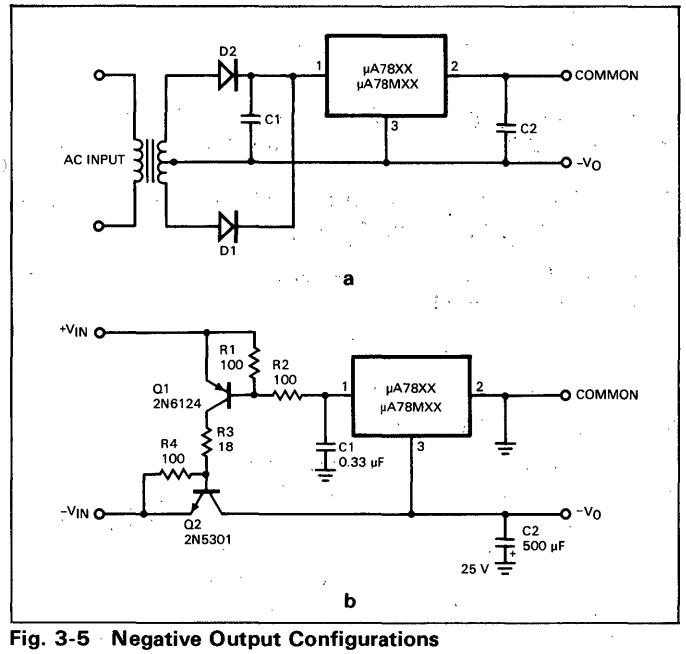


Fig. 3-5 Negative Output Configurations

Current Regulator

The circuit shown in *Figure 3-6* supplies a regulated current to a load, its value being determined by an external resistor. The minimum input/output differential in this application is (minimum regulator input/output differential voltage) + (maximum regulator output voltage). For currents up to 1 A, 0°C to 70°C, this voltage is typically 2.2 V + 5.25 V, or 7.45 V.

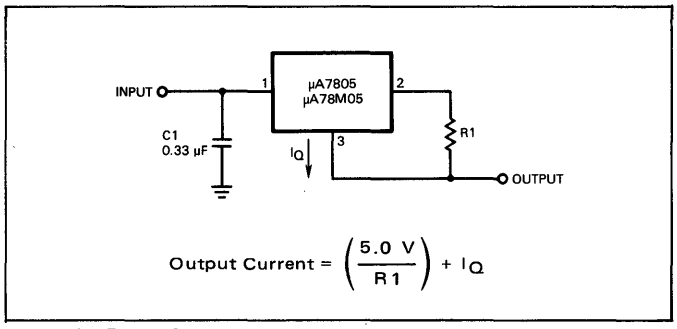


Fig. 3-6 Basic Current Regulator

High Current Voltage Regulators

Currents in excess of the output capabilities of the basic regulator can be obtained with the circuit shown in *Figure 3-7a.* The value of R1 determines the point at which Q1 begins to conduct and hence bypasses the regulator. This supply can be protected against a short circuit load by adding a short circuit sense resistor, R2, and a pnp transistor Q2, as in *Figure 3-7b.* In this circuit Q2 must be able to handle the short circuit current of the regulator, since when Q1 is bypassed, the regulator goes into its short-circuit mode.

Foldback current limiting may be provided for the external power device by adding resistors R3 and R4 (*Figure 3-7c).*

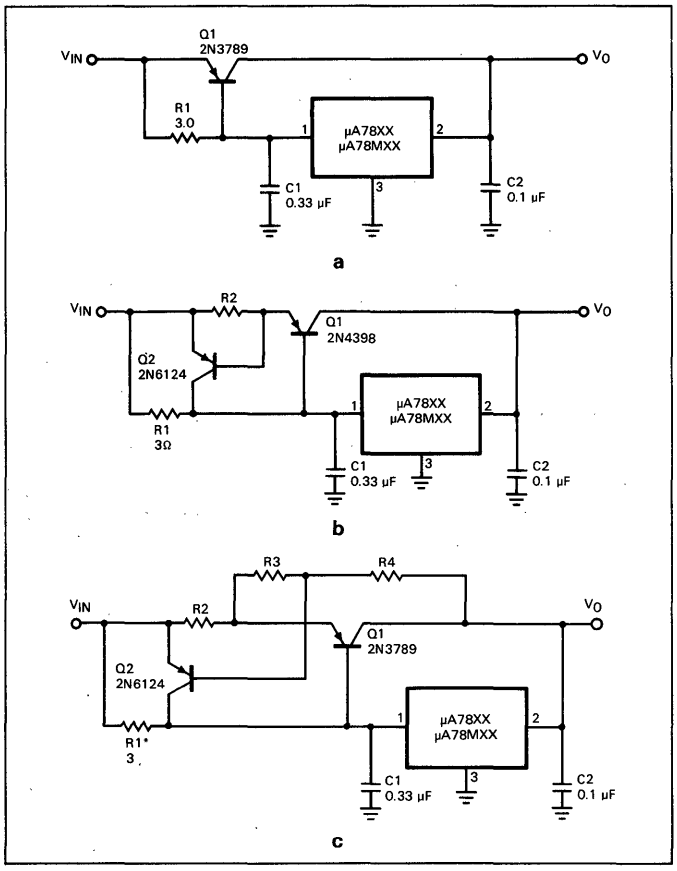


Fig. 3-7 High Current Regulators

Variable Output Voltage Regulators

In *Figure 3-8a* a voltage pedestal is developed across R2, which is then added to the normal regulated output V_{XX}, such that

$$V_O = V_{XX}\left(1+\frac{R2}{R1}\right) + I_Q R2$$

The current through R1 should be set much higher than the quiescent current I_Q to minimize the effects of the change in I_Q which occurs with a change in V_{IN}.

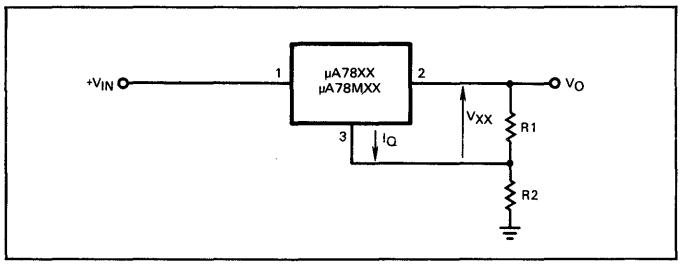


Fig. 3-8a Basic Application

A modification *(Figure 3-8b)* provides a continuously variable output in the range of 7 to 30 V. A μA741 amplifier buffers the pedestal voltage across R2 from the regulator quiescent current. This removes the interaction of I_Q and V_O.

$$V_O = V_{XX}\left(1+\frac{R2}{R1}\right), \text{ i.e. } V_O = 5\left(1+\frac{R2}{R1}\right) V.$$

Supply regulation is the same percentage per parameter change as for the basic 3-terminal device used. Care must be exercised under heavy load/short circuit conditions because it is possible for the regulator output to become reverse-biased with the internal thermal shutdown feature inoperable.

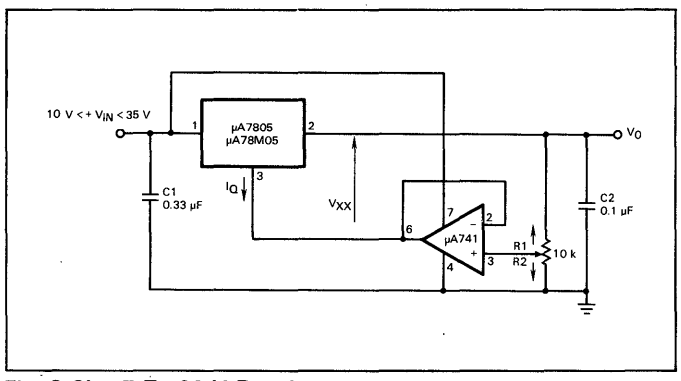


Fig. 3-8b 7-To-30 V Regulator

For adjustable outputs in the range 0.5 to 10 V, *Figure 3-8c* may be used. A negative supply, $-V_{IN}$, is required to allow adjustment to the lower output voltages.

$$V_O = V_{XX}\left(\frac{R1+R2}{11\ R1}\right) \quad \text{or } 0.45\left(1+\frac{R2}{R1}\right) V.$$

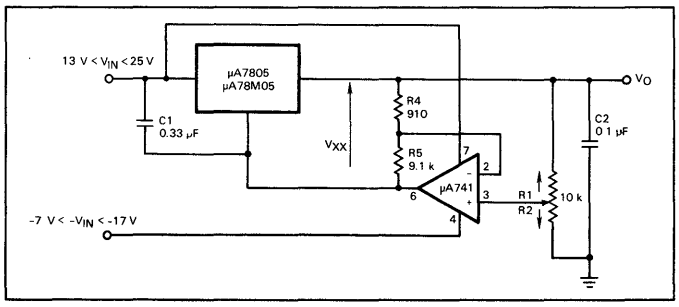


Fig. 3-8c 0.5-To-10 V Regulator

Dual Polarity Regulators

Dual polarity regulators supply both positive and negative output voltages from either positive, negative, or single floating input voltages.

In *Figure 3-9a*, a 7800 or 78M00 series regulator establishes the positive output voltage. A μA741 operational amplifier is then used as an inverting amplifier to provide the negative output voltage. It is necessary to have bipolar input supplies referenced to the common terminal. The μA741 always drives the negative output to a voltage that maintains the junction of R1 and R2 very close to zero volts,

$$-V_O = -\left(\frac{R2}{R1}\right)\left(+V_O\right)$$

As shown, in *Figure 3-9a*, with R1 = R2 = 4.7 kΩ equal bipolar output voltages will be generated. Note that the negative output will track the positive output (that is, any change occurring at the positive output will appear, inverted, at the negative output), but the positive output will not track changes generated at the negative output. This unidirectional tracking is also common to all monolithic IC tracking regulators, such as the 7600 series.

An improved, dual polarity regulator is shown in *Figure 3-9b*. Here a 7800 or 78M00 series regulator provides the total output voltage from a single, floating input. A μA741 operational amplifier with a complementary emitter follower output stage connected as a voltage follower is then used to generate a common output line at a level set by R1 and R2.

$$\frac{+V_O}{-V_O} = \frac{R1}{R2}$$

Again, with R1 = R2 = 4.7 kΩ as shown, equal positive and negative outputs are obtained. With this circuit, either output tracks changes occurring on the other. A limitation of this circuit is that the differential output current, i.e., that current which flows into or out of the common terminal, is limited to (Q1/Q2 h_{FE}) x (μA741 maximum current). However, since with the components shown, this limit is typically in excess of 750 mA, and most loads exhibit a considerable degree of balance, which minimizes the differential current, this limitation is rarely met in practice. Another improvement in performance of this circuit over that of *3.9a* is the superior line regulation on the negative output, due to the μA741 being supplied by a well regulated voltage. In *Figure 3-9a* the μA741 is supplied directly from $-V_{IN}$.

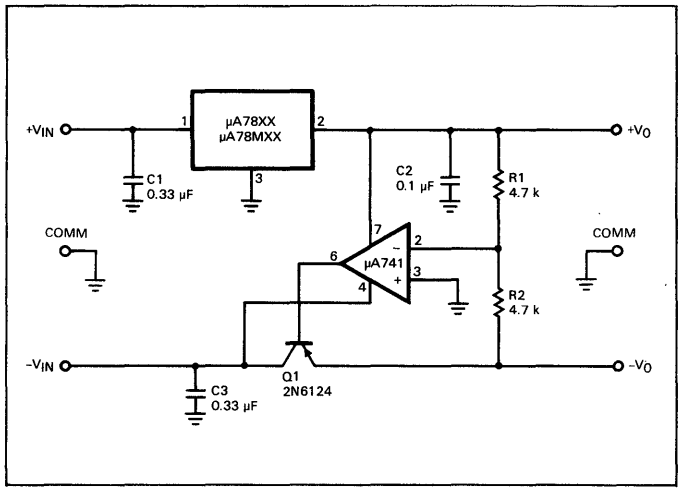


Fig. 3-9a Dual Polarity Regulator

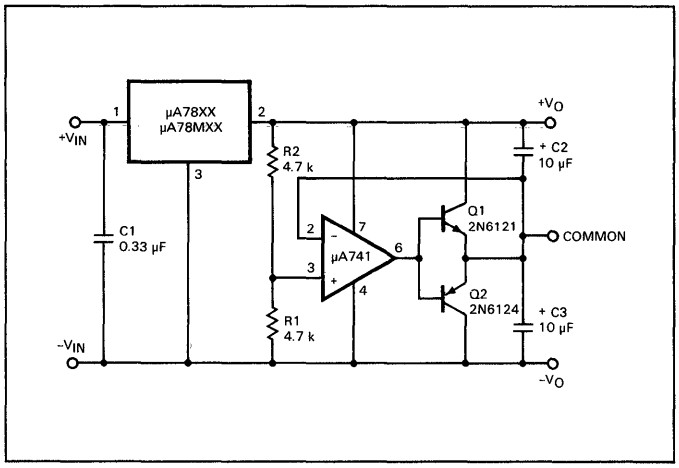


Fig. 3-9b Dual Polarity Regulator

Switching Regulators

A switching regulator may be used in those cases where the dissipation of a linear regulator is excessive. *Figure 3-10* shows that when power if first applied, current flows through R3 and the 7800 device to the output. As soon as the current generates a voltage drop sufficient to forward bias Q1's base emitter junction, Q1 is driven toward saturation. The increase in voltage at the collector applies power through L1 to the load and provides positive feedback through R1 and R2 to assure a full switching action. As the output voltage approaches the sum of the 7800 regulated output plus the voltage developed across R2, current flow through the 7800 decreases.

Input voltages in excess of the maximum input voltage rating of the regulator may be accommodated by the inclusion of a voltage dropping Zener (D1). This reduces the voltage appearing across leads 1 and 3 of the 7800 to an acceptable level.

When the base current drops below the level required to keep Q1 in saturation, the collector voltage starts to decrease and the positive feedback loop completes the switching action.

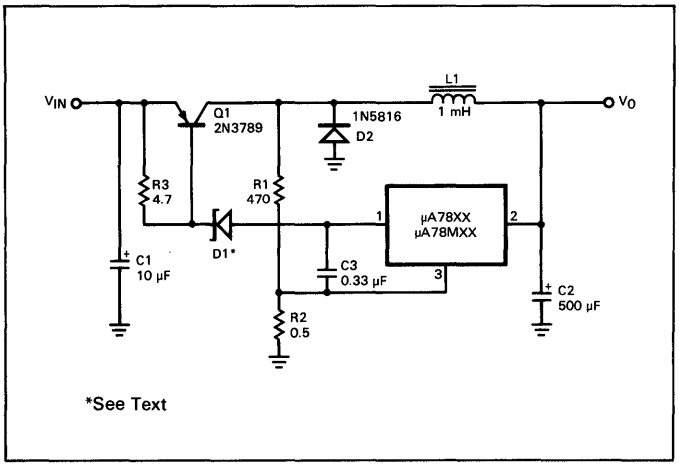
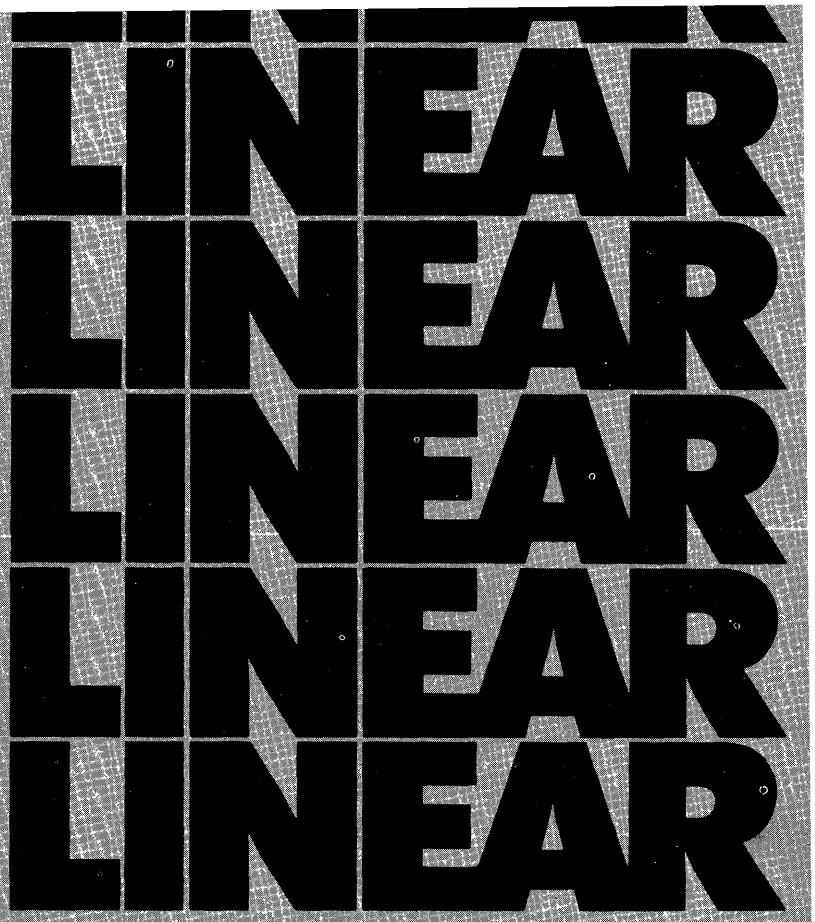


Fig. 3-10 Switching Regulator



CONTENTS AND SECTION SELECTOR

IN THIS CHAPTER:

- INTRODUCTION
- FUNCTIONAL DESCRIPTION
- TYPICAL PERFORMANCE CHARACTERISTICS
- PACKAGING AND CONNECTION DIAGRAMS

CHAPTER 4
79E00 Negative 3-Terminal Voltage Regulators

INTRODUCTION

The 79E00 series devices are 3-terminal negative voltage regulators specifically designed for emitter coupled logic (ECL) systems. Output voltages of -2.0 V (79E02) and -5.2 V (79E05) are available. Each series is capable of providing output currents to 3 A, assuming adequate heat sinking. The output voltage is internally trimmed to a ±0.5% initial tolerance, and maintains better than ±2% for normally expected combinations of line, load and temperature variations. Complete protection is built into the 79E00 series through current limiting, thermal shutdown, and output transistor safe area protection. Internal trimming is accomplished by adjusting R1, part of a resistor network, which divides the output voltage down to the voltage reference level of 1.3 V *(Figure 4-1)*. The 79E00 is available in the TO-3 package for both military and commercial operating temperature ranges.

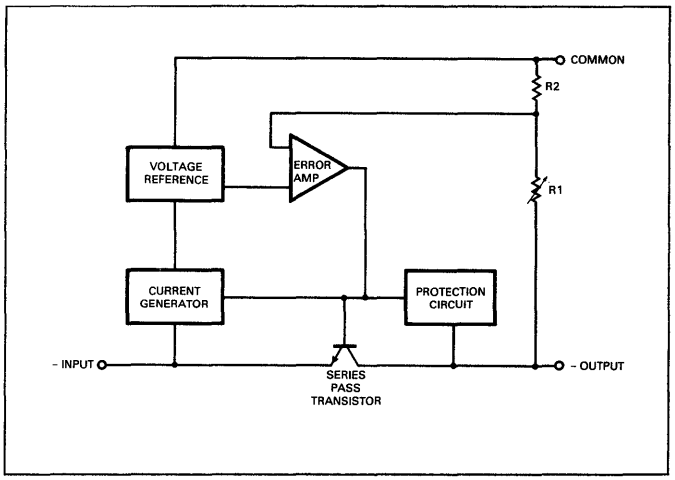


Fig. 4-1 79E00 Block Diagram

FUNCTIONAL DESCRIPTION

The equivalent schematic diagram of the 79E00 is shown in *Figure 4-2*. A forward biased diode reference circuit was selected for this regulator because of its low operating voltage when compared with a Zener reference — therefore allowing a lower input voltage to be used. The high predictability of this type of reference also helps minimize the trimming required to achieve the specified output tolerance during manufacture. A very low voltage temperature coefficient is achieved by matching the amplified positive temperature coefficient of a differential base emitter voltage to the negative temperature coefficient of a base emitter voltage.

The -1.3 V generated by the reference circuit is compared by the error amplifier to the voltage at the R27/R28 junction, which is proportional to the output voltage. The stringent performance characteristics required of the negative regulator necessitates a multistage error amplifier with an open loop gain of 100 dB. The schematic of the error amplifier (*Figure 4-2*), in fact, closely resembles that of the μA741 high performance operational amplifier. In addition to its high gain, it exhibits low offset voltage and offset voltage drift, low bias and offset currents and is frequency compensated by a single 30 pF capacitor.

The error amplifier output drives the power Darlington transistors Q23 and Q24, designed for peak currents of up to 4 A. Short circuit current limiting is provided by Q22, which begins to conduct when a sufficiently high voltage is developed across R20 by the output current, and diverts the drive current away from the base of Q23. Q21 senses the temperature of the chip and, at a junction temperature of approximately 165°C, its base emitter threshold voltage

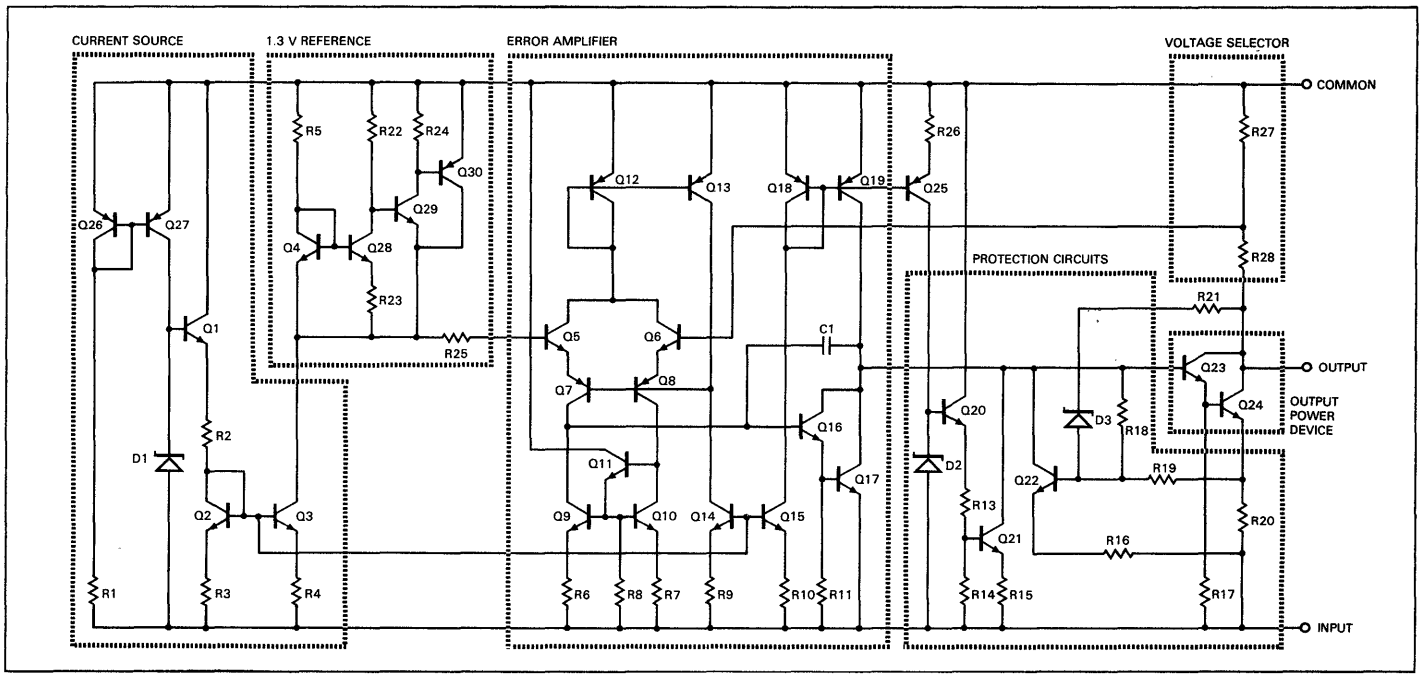


Fig. 4-2 79E00 Equivalent Schematic

equals the pre-biased voltage generated across R14. As Q21 begins to conduct, it also removes base drive from Q23 and prevents further heating of the device.

A safe area compensation circuit is also incorporated on the chip to prevent secondary breakdown of the power transistor. As the collector emitter voltage of Q24 increases, Zener diode D3 will begin conducting. The current through D3, at a level set by R21, provides a pre-biased level to the base of current sense transistor Q22. This lowers the current limit as a function of input/output differential voltage.

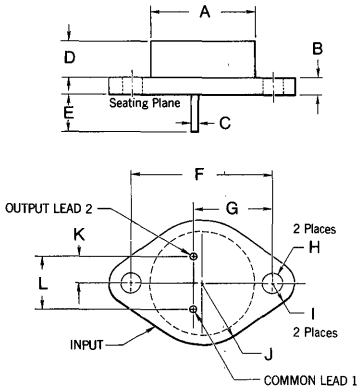
PARTS AVAILABILITY — TO-3

OUTPUT VOLTAGE	TYPE	CONDITIONS
-2.0 V -5.2 V	79E02 79E05	Operating junction temperature -55 to 150°C
-2.0 V -5.2 V	79E02C 79E05C	Operating junction temperature 0 to 150°C

Typical Performance Characteristics 79E02 and 79E05, T_J = 25°C, V_{IN} = -8.5 V, I_{OUT} = 2 A, unless otherwise noted.

PARAMETERS	CONDITIONS	TYPICAL	UNITS
INPUT VOLTAGE		-7.5 TO -15.0	V
OUTPUT VOLTAGE CHANGE	-7.5 V $\leq V_{IN} \leq$ -9.5 V 1 A $\leq I_{OUT} \leq$ 2 A 25°C $\leq T_J \leq$ 125°C	±100	mV
LINE REGULATION	-7.5 V $\leq V_{IN} \leq$ -9.5 V	2	mV
LOAD REGULATION	1 A $\leq I_{OUT} \leq$ 2 A	10	mV
OUTPUT VOLTAGE TEMPCO.	25°C $\leq T_J \leq$ 125°C	.005	%/°C
QUIESCENT CURRENT		10	mA
OUTPUT NOISE VOLTAGE	100 Hz $\leq$ f $\leq$ 100 kHz	100	μV rms
OUTPUT CURRENT, (MAX)		3	A

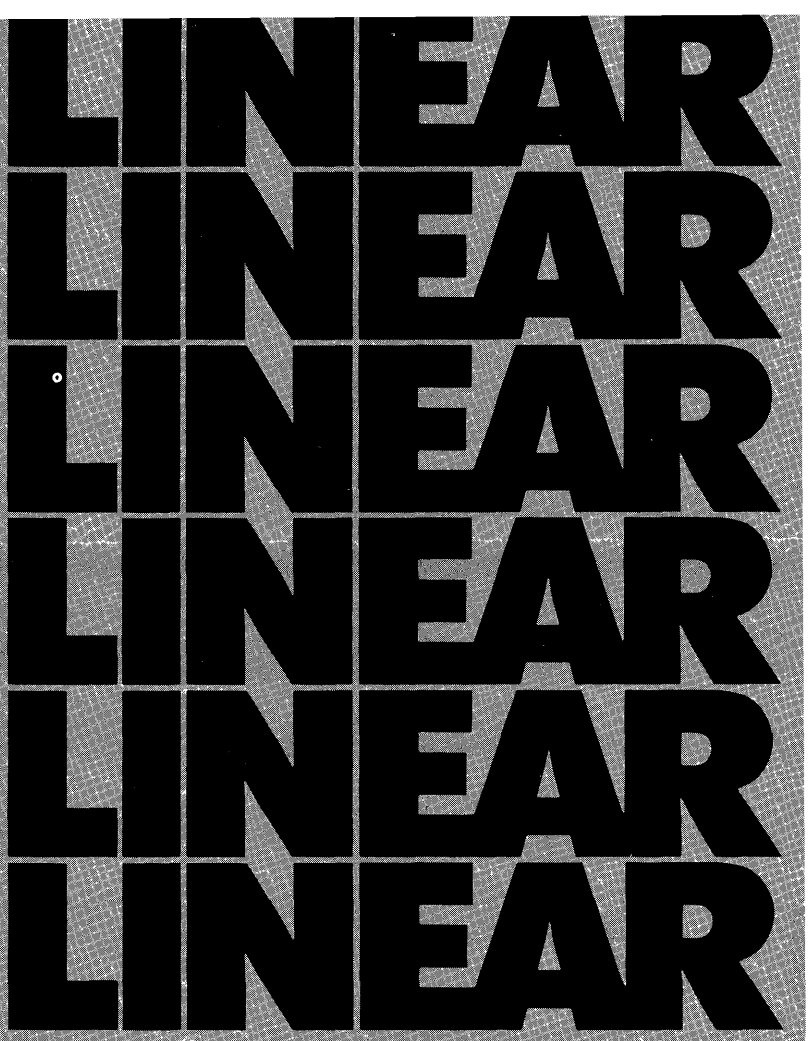
Table 4-1 Performance Characteristics of the 79E00 Regulators



NOTES:
Leads 1 and 2 electrically isolated from case
Case is electrically connected to common
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.835	20.45	31.21
B		0.135		3.43
C	0.038	0.048	0.965	1.22
D	0.205	0.325	5.20	8.26
E	0.312		7.92	
F	1.177	1.197	29.90	30.40
G	0.655	0.675	16.64	17.15
H	0.151	0.161	3.79	3.84
I		0.188		4.78
J		0.525		13.34
K	0.205	0.225	5.20	5.71
L	0.420	0.440	9.67	10.08

Fig. 4-3 JEDEC TO-3



CONTENTS AND SECTION SELECTOR

IN THIS CHAPTER:

- BYPASSING
- THERMAL CONSIDERATIONS
- TYPICAL APPLICATIONS

CHAPTER 5
79E00 Negative 3-Terminal Voltage Regulator Applications

BYPASSING

Since the 79E00 series of regulators uses an npn transistor as the internal series pass device (a configuration with voltage gain), external compensation is required. The minimum requirement to ensure stability is a 10 µF tantalum capacitor placed across the regulator output terminals.

When ECL systems are used without transmission lines, it is normal to have the complementary outputs loaded with pull down resistors, typically 510Ω to -5.2 V. In this case, logic One and logic Zero load currents are approximately 8.7 mA and 7.0 mA, respectively. However, due to the excellent matching between the complementary outputs, the power supply drain remains essentially constant regardless of the logic state or speed of operation. Small systems may be adequately bypassed by a 10 µF tantalum capacitor placed across the power supply input. The capacitor across the output of the regulator will serve this purpose in on-card regulator applications. Larger systems require ceramic capacitors distributed among the ECL devices, typically 0.01 µF to 0.1 µF every four or five packages.

ECL systems used with transmission lines have effective loads of typically 50Ω to a separate -2.0 V supply. This represents a 22 mA load current in the logic One state, and 6 mA in logic Zero state. This 16 mA differential current between the two states can produce significant load current transients. In such systems it is recommended that ceramic bypass capacitors, 0.01 µF to 0.1 µF are used every four or five ECL packages on both the -2.0 V and -5.2 V supplies. This is in addition to the 10 µF tantalum capacitor across the output of an on-card regulator.

THERMAL CONSIDERATIONS

The thermal characteristics of the 79E00 series devices are very similar to those of the 78XX series regulators in the TO-3 package, and information contained in Chapter 3 is applicable to heat sink design for 79E00 regulators as well.

A further consideration is that the case of the 79E00 regulator is at the most negative potential available, i.e., the input; therefore, an insulating washer must be used when mounting the package to a grounded heat sink.

TYPICAL APPLICATIONS

Basic 3-Terminal Regulator

Figure 5-1 illustrates the minimum external compensation necessary to ensure stability. With adequate heat sinking, the regulator has a useful output current range of 50 mA to 3 A at input/output differential voltages up to 5 V which drops to 1 A at input/output differential voltages of 15 V due to safe area compensation. The 0.47 µF input bypass capacitor is required if the regulator is located some distance from the filter capacitors of the dc supply, $-V_{IN}$.

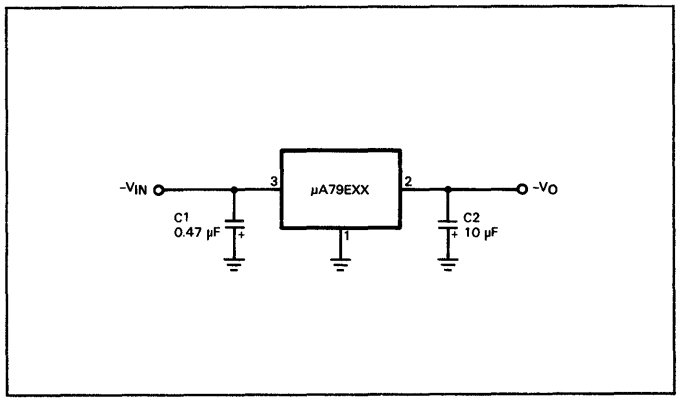


Fig. 5-1 3-Terminal Regulator

High Current Negative Voltage Regulators

Higher output current may be obtained by adding an npn bypass transistor, as in *Figure 5-2*; circuit 5-2b incorporates short circuit protection for the bypass transistor. Resistor R1 sets the point at which transistor Q1 conducts and bypasses the regulator. As shown in circuit 5-2b, resistor R2 sets the point at which Q2 begins to conduct, bypassing Q1, thus limiting the current that can be drawn by the load. With a short circuit load, Q1 is cut off and the regulator will supply its short circuit current to the load. Transistor Q2 must be capable of supplying this current to the regulator.

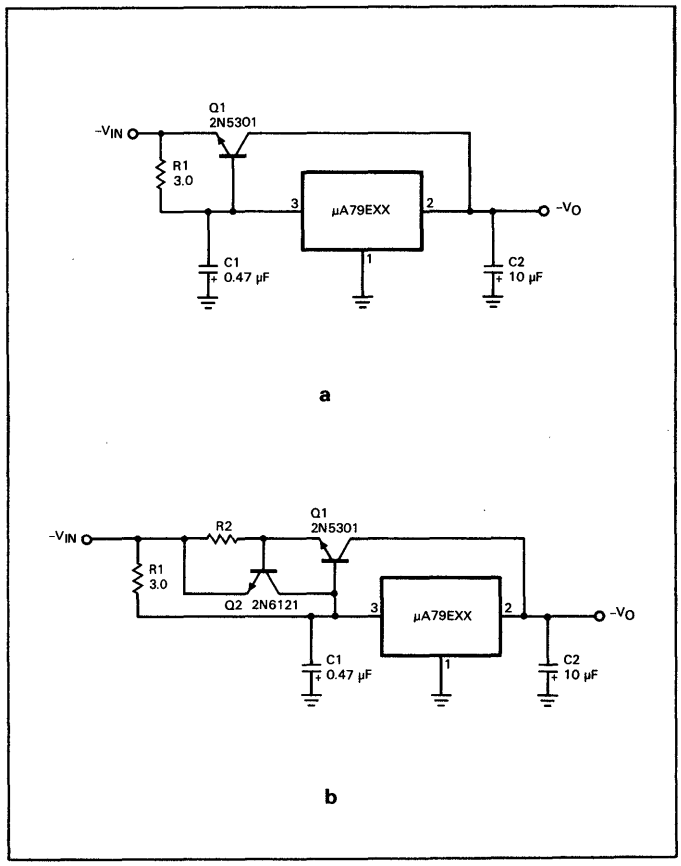


Fig. 5-2 High Current Negative Voltage Regulators

LINEAR

LINEAR

LINEAR

LINEAR

LINEAR

LINEAR

LINEAR

CONTENTS AND SECTION SELECTOR

IN THIS CHAPTER:

- INTRODUCTION
- 78L00 DESCRIPTION
- 7600 DESCRIPTION

CHAPTER 6

78L00 Low Current Positive Voltage Regulators
7600 Dual Polarity Tracking Voltage Regulators

INTRODUCTION

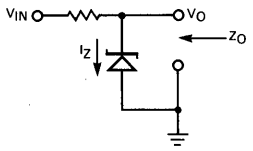
The 0.5 A (78M00), 1.0 A (7800) and negative (79E00) regulators described in previous sections fulfill a large portion of central and remote on-card power supply applications. However, as further applications demand it, Fairchild will extend the 7800 family. For example, the first such series will be the 78L00 series of positive regulators covering low current applications up to 100 mA, and the 7600 series of dual polarity tracking regulators.

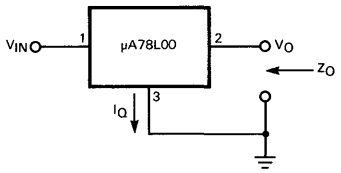
78L00 DESCRIPTION

The 78L00 series of regulators employs circuitry similar to the 78M00 series except that the series pass transistor is smaller due to the lower current handling capability required. The resulting smaller chip size enables the 78L00 to be packaged in the TO-92 case. This is a popular, low cost molded package borrowed from the discrete transistor line. It will also be available in a metal can similar to TO-39.

As with the 78M00 series, the 78L00 includes output current limiting and chip temperature limiting features. Useful output current extends to 100 mA. Initial output voltage tolerance is similar to the 78M00 series. Typical output voltage change is 1.0% with input voltage variations, and 1.0% with 5 mA to 100 mA load variation. Available output voltages include 5.0 V, 12.0 V and 15.0 V for applications in test equipment, digital panel meters, and general purpose industrial and consumer small system power supply applications. Output voltages of 2.6 V and 6.2 V are also available for low cost Zener diode/resistor combination replacement.

In this application, the 78L00 provides superior performance to the standard 400/500 mW ranges of Zener diodes (IN746 series and IN5221 series). A comparison is made in *Figure 6-1.* Note that a Zener diode/resistor combination can supply a load current of 17 mA with a quiescent current of 20 mA, whereas the 78L00 can supply up to 100 mA load current with a quiescent current of 5 mA. The effective output impedance of the 78L00 is typically two orders lower than that of the Zener diode. At I_Z = 5 mA, the temperature coefficient of the 78L00 is equal to, or better than, that of the Zener diode, and output noise voltage is reduced when using the 78L00.





V_O (nom)	Z_O(typ) I_Z = 20 mA	Z_O(typ) I_Z = 5 mA	TC(typ) I_Z = 5 mA
2.7	17	70	−1.5 to − 2.5
6.2	5	9	+1 to + 3
12	8	27	+5 to +10
15	10	40	+6 to +12
V	Ω	Ω	mV/°C

V_O (nom)	Z_O(max) I_Q = 5 mA	TC(typ) I_Q = 5 mA
2.6	0.3	±3
6.2	1.2	±3
12	2.5	±3
15	3.0	±3
V	Ω	mV/°C

NOTE: For more detailed data on the 78L00 Series devices — please refer to the 78L00 Data Sheet.

Fig. 6-1 78L00 as a Resistor/Zener Diode Replacement

7600 DESCRIPTION

The 7600 series of dual polarity tracking regulators provides positive and negative regulated output voltages at currents up to 100 mA. The principle of operation is illustrated in the block diagram, *Figure 6-3.* A temperture stabilized, negative biased reference voltage, $-V_R$, is applied to the negative error amplier, connected in a non-inverting mode such that its output,

$$-V_O = \left(\frac{R1 + R2}{R1}\right) -V_R$$

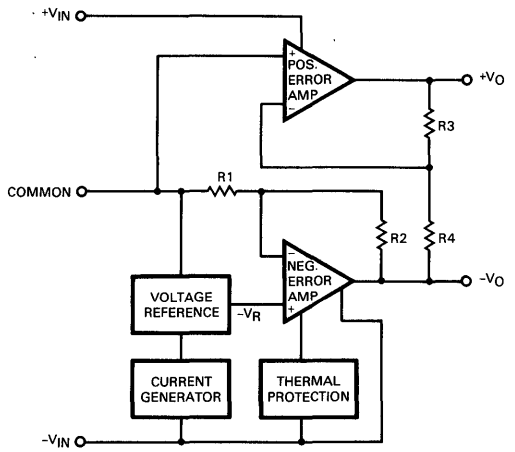
The positive error amplifier is used in an inverting mode, referenced to ground, with $-V_O$ as its input, and its output

$$+V_O = -\left(\frac{R3}{R4}\right)(-V_O)$$

Devices are available with output voltages preset to ±5 V, ±12 V, ±15 V, ±18 V, +12/−6 V, +5/−9 V, and +5/−12 V. Presetting is achieved by internally trimming resistors R2, R3 or R4 during manufacture. In addition, outputs are adjustable over a ±10% range by use of external components to shunt R1, R2, R3 or R4.

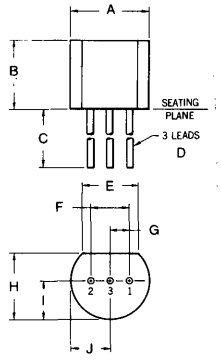
The output stage of each error amplifier is capable of supplying output current up to 150 mA and incorporates current limiting circuitry to protect the device against current overloads. If necessary, the output current may be boosted by external npn power transistors. Thermal protection is also included on the chip to shut down the negative error amplifier. This in turn, shuts down the positive error amplifier if dangerous chip temperatures are reached. Both error amplifiers are internally frequency compensated to ensure stable operation.

The 7600 devices are intended for use as on-card regulators wherever dual polarity supplies are required. External components have been reduced to a minimum; in fact, the typical application requires one 7600 regulator, two 10 µF input capacitors, and two 0.5 µF output capacitors. With their load and line regulation of ± 1%, they are well suited to supply power to operational amplifiers in precision analog systems. Other dual supply requirements include MOS systems and interface circuitry. Package availability includes the 10-lead TO-5 and the 14-lead power DIP.



NOTE:
For more detailed information of the 7600 Series Voltage Regulators – refer to the 7600 Data Sheet.

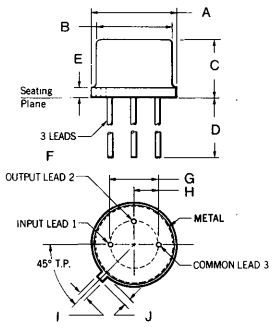
Fig. 6-2 7600 Block Diagram



NOTES:
Leads are tin-plated kovar
Package material is transfer molded thermosetting plastic
Package weight is 0.25 gram

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.175		0.205	4.45		5.20
B	0.170		0.210	4.32		5.33
C	0.500			12.70		
D	0.016		0.019	0.406		0.483
E	0.135			0.343		
F		0.100			2.54	
G		0.050			1.27	
H	0.125		0.165	3.18		4.19
I	0.080		0.105	2.03		2.67
J	0.080		0.105	2.03		2.67

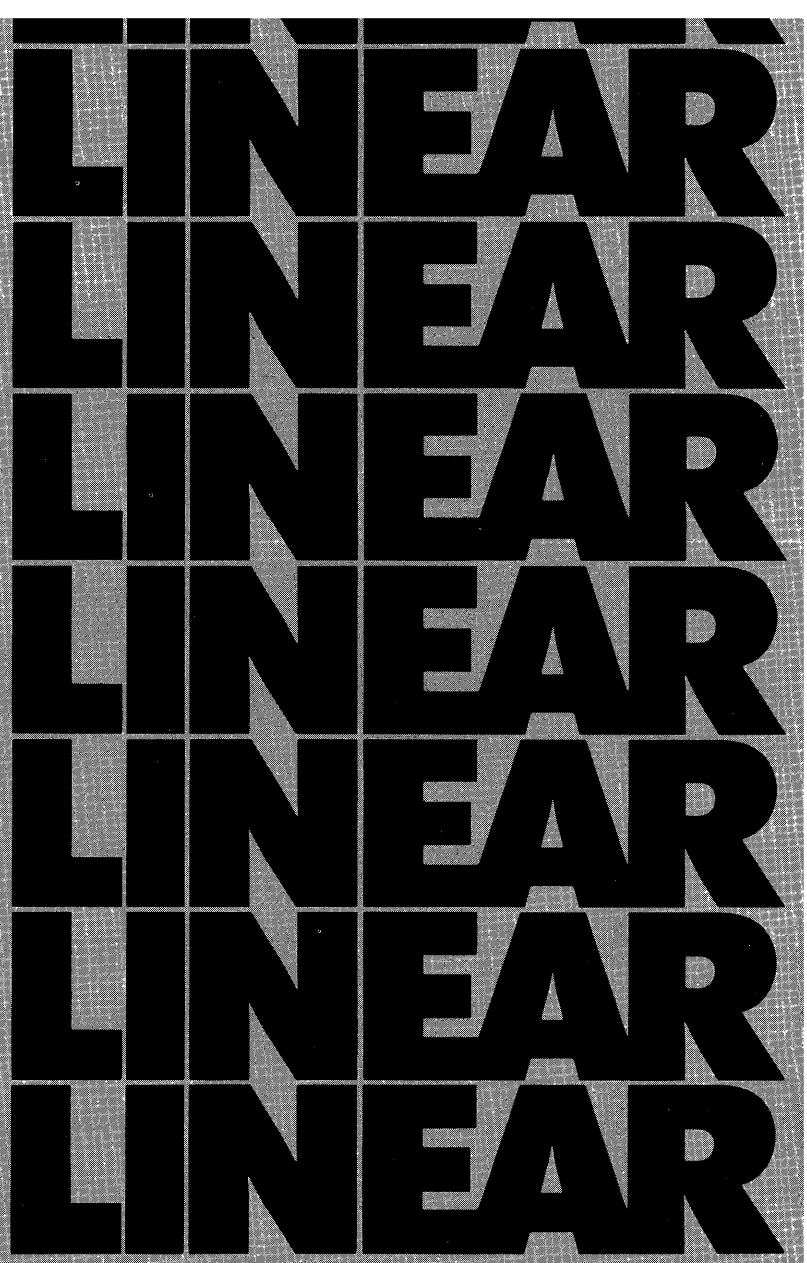
Fig. 6-3 JEDEC TO-92 (78L00)



NOTES:
Leads are gold-plated kovar
Lead 3 connected to case
Low thermal resistance
Package weight is 0.76 gram

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.350		0.370	8.51		9.39
B	0.315		0.335	8.00		8.51
C	.165		0.185	4.20		4.70
D	0.500			12.70		
E			0.030			0.762
F	0.016		0.019	0.406		0.483
G		0.200			5.08	
H		0.100			2.54	
I	0.28		0.034	0.711		0.864
J	0.029		0.040	0.737		1.02

Fig. 6-4 Low-Profile TO-39 (78L00)



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- INTRODUCTION
- FUNCTIONAL DESCRIPTION
- CONDENSED SPECIFICATIONS AND PERFORMANCE CURVES
- ELECTRICAL CHARACTERISTICS
- PACKAGING AND CONNECTION DIAGRAMS

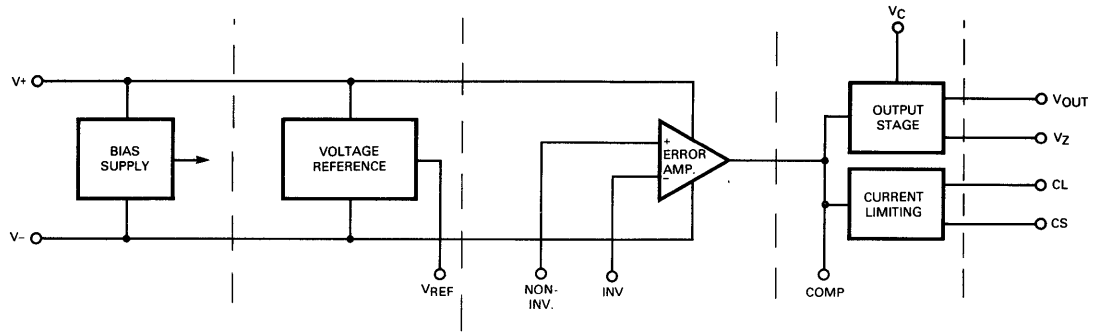
CHAPTER 7
μA723 Precision Voltage Regulator

INTRODUCTION

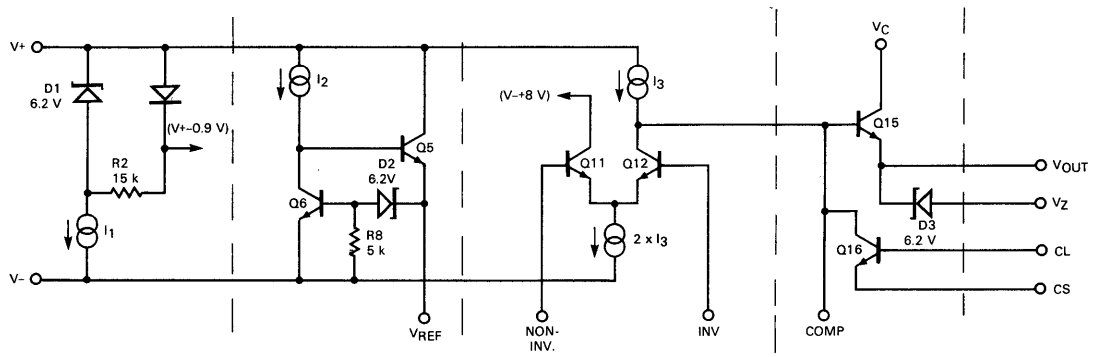
The μA723 is commonly regarded as a universal building block in power supply design. This section outlines the block diagram and those parts of the internal design which result in the flexibility required for this "universal" label.

In *Figure 7-1a* is the block diagram of the μA723 illustrating the various features which have been incorporated into the device — they are as follows.

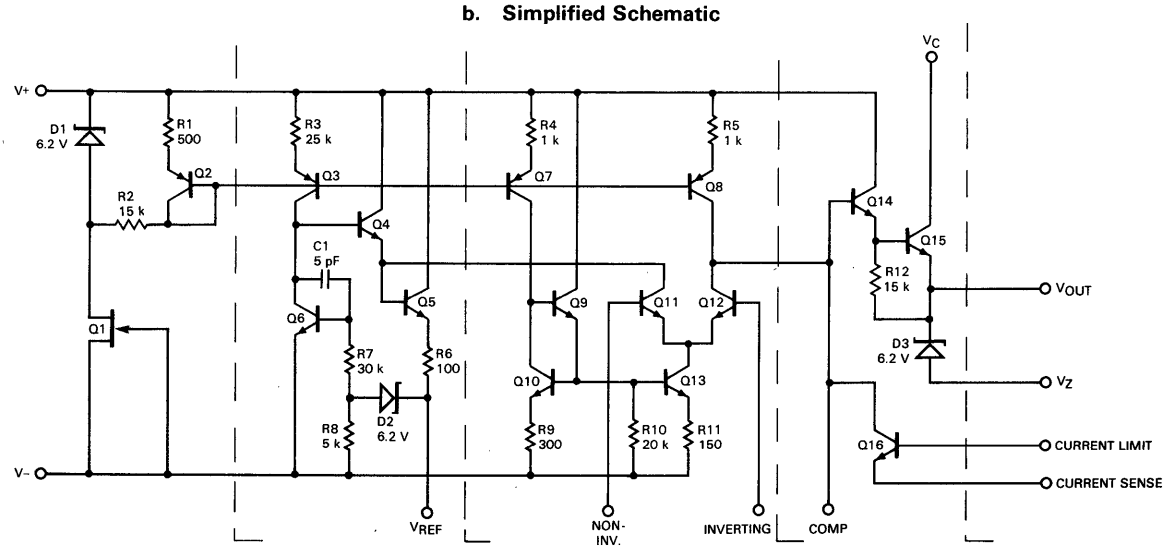
- The internally generated reference voltage is directly available in buffered form.
- Both inputs of the error amplifier are available for use with other than positive grounded configurations.
- The collector of the internal series pass device is available at a separate lead on the package (V_C).
- Voltage level shifting is available (V_Z output) through an internal Zener diode (14-lead DIP version only).



a. Block Diagram



b. Simplified Schematic



c. Equivalent Schematic

Fig. 7-1 μA723 Precision Voltage Regulator

FUNCTIONAL DESCRIPTION

Circuit operation may best be described with the aid of the simplified schematic in *Figure 7-1b.* Bias supplies for the entire circuit are obtained by first generating a stabilized voltage with respect to the V+ line across Zener diode D1, which is supplied with a constant current I_1. This voltage is then used to derive the bias voltage which controls current sources I_2 and I_3.

The basic reference element of the voltage reference supply is the Zener diode D2 which has a typical breakdown voltage of 6.2 V at 200 µA and a typical temperature coefficient of +2.4 mV/°C. Its operating current is set by R8. However, V_{REF} actually consists of D2 breakdown voltage plus the base emitter voltage of Q6. From the basic relationship between the base emitter voltage of a transistor and its collector current, it is found that the temperature coefficient of base emitter voltage is a function of collector current. Therefore, in the voltage reference supply, the temperature coefficient of Q6 base emitter voltage is set by current source I_2 to cancel the temperature coefficient of D2, giving a typical reference voltage of 7.15 V with a nominal temperature coefficient of zero. In addition to providing current for D2, transistor Q5 provides the necessary buffering to allow current to be taken from the V_{REF} terminal for certain applications.

In the error amplifier, Q11 and Q12 form a differential pair of transistors driven by a current source 2 x I_3. The active load for Q12 is a pnp current source I_3; therefore, in a balanced condition, i.e., when Q11 and Q12 base voltages are equal, Q11 and Q12 collector currents are both equal to I_3. Q11 collector is returned to a stabilized voltage source in the reference supply to maintain high line rejection in the amplifier. I_3 is set to approximately 160 µA. In operation V_{REF}, or a voltage derived from V_{REF}, is applied to the non-inverting input (Q11 base) and a voltage proportional to the desired output voltage is applied to the inverting input (Q12 base). When the feedback loop is closed via the µA723 output stage and external bypass transistors, if used, the two error amplifier inputs are forced to a condition of balance, thus defining the output voltage in terms of V_{REF} and the appropriate resistor ratios.

The output stage consists of a double emitter follower (Q14-Q15) to prevent excessive loading on Q12 collector. This, in conjunction with the high impedance of the active load (I_3), allows adequate gain to be obtained from the single stage amplifier. This also simplifies frequency compensation with a single capacitor connected from Q12 collector (COMP terminal) to either Q12 base or ground being sufficient to provide stable operation in all applications.

D3, a 6.2 V Zener diode, is available in the dual in-line package for level shifting purposes. The allowable voltage range at Q12 collector to maintain linear operation is from V_{INV} to a maximum voltage (V– plus 2 V). V_{INV} is also limited to a minimum voltage (V+ minus 1 V). In some applications the µA723 output voltage is required to be below this range, in which case D3 may be used to bring Q12 collector back into its linear region.

Q16 is available for current limiting purposes. When Q16 base emitter junction becomes forward biased at a particular level of load current by means of an external current sensing resistor, Q16 collector sinks most of the available current from the current source I_3. This tends to cut off the output stage, and limit output current.

The equivalent schematic of *Figure 7-1c* shows the implementation of these functions. Q1 is an n-channel FET made with technology compatible with normal integrated circuit components. The use of an FET has two advantages. First, the line regulation is greatly improved because the current drawn by Q1 is independent of power supply variations. Second, the power dissipation is minimized because the current drawn does not appreciably increase at large supply voltages.

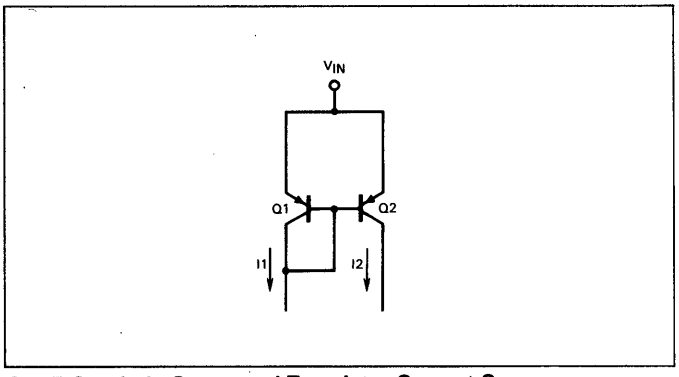


Fig. 7-2a Diode Connected Transistor Current Source

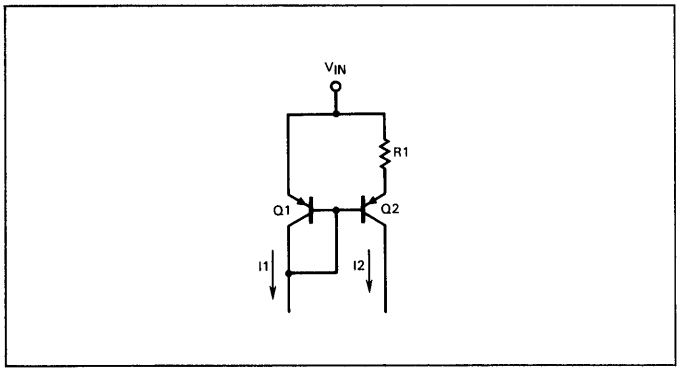


Fig. 7-2b Logarithmic Current Source

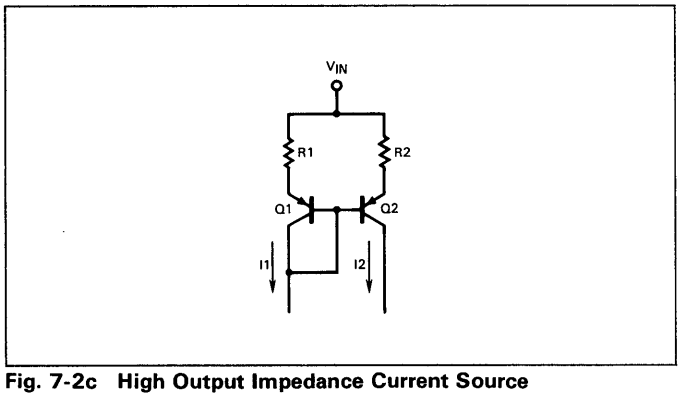


Fig. 7-2c High Output Impedance Current Source

Transistors Q2, Q7 and Q8 form the current sources previously discussed. The normal method of biasing these current sources is to use either a diode connected transistor *(Figure 7-2a)* or a logarithmic relationship as shown in *Figure 7-2b.* For this design, however, a very high output impedance is required to provide high line rejection and increase the gain of the error amplifier. In the configuration shown in *Figure 7-2c,*

$$I_{C2} = \frac{V_{BE1} + I_1 R1 - V_{BE2}}{R2}$$

In this case, a change in V_{BE} has only a small effect on the voltage across R2 and the collector current has been stabilized against changes in collector-to-emitter voltage. This then provides the necessary high output impedance.

The current source produced by Q7 is "mirrored" by Q10 and Q13 to provide a current sink of value 2 x I_3 for the error amplifier.

To achieve a low V_{REF} output impedance, transistor Q5 in *Figure 7-1b* has been replaced with a Darlington pair, Q4 and Q5. Resistor R7 and MOS capacitor C1 are included on the chip to eliminate the need for an external compensation of the voltage reference loop.

The power output transistor Q15 is a multiple device using individual emitter current balancing resistors. This technique increases the safe operating area and extends the output current capability to 150 mA.

CONDENSED SPECIFICATIONS AND PERFORMANCE CURVES

The following electrical characteristics and typical performance curves are based on the test circuit in *Figure 7-3.* Note that CL refers to Current Limit, CS to Current Sense, and the sense voltage referred to in the performance curves is the voltage difference between terminals CL and CS.

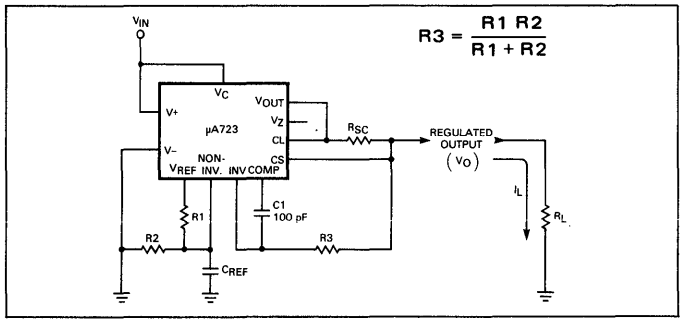


Fig. 7-3 Basic Test Circuit

Absolute Maximum Ratings

Pulse Voltage from V+ to V–, (50 ms) (723 only)	50 V
Continuous Voltage from V+ to V–	40 V
Input/Output Voltage Differential	±5 V
Voltage Between Non Inverting Input and V–	+8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation*	
Metal Can	850 mW
DIP	1000 mW
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Military (723)	-55°C to +125°C
Commercial (723C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

*Rating applies to ambient temperatures up to 25°C. Above 25°C ambient derate linearly at 6.8 mW/°C for the Metal Can. For the DIP, derate linearly at 80 mW/°C above 25°C for 723C, above 50°C for 723.

ELECTRICAL CHARACTERISTICS (See Note)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2	%V_{OUT}
	$-55°C \leqslant T_A \leqslant +125°C$, V_{IN} = 12V to V_{IN} = 15V			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15	%V_{OUT}
	$-55°C \leqslant T_A \leqslant +125°C$, I_L = 1 mA to I_L = 50 mA			0.6	%V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leqslant T_A \leqslant +125°C$		0.002	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

μA723C

ELECTRICAL CHARACTERISTICS (See Note)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1	%V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.1	0.5	%V_{OUT}
	$0°C \leqslant T_A \leqslant 70°C$, V_{IN} = 12V to V_{IN} = 15V			0.3	%V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.2	%V_{OUT}
	$0°C \leqslant T_A \leqslant 70°C$, I_L = 1 mA to I_L = 50 mA			0.6	%V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leqslant T_A \leqslant 70°C$		0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input/Output Voltage Differential		3.0		38	V

NOTE:

Unless otherwise specified, T_A = 25°C, V_{IN} = V+ = V_C = 12 V, V− = 0, V_{OUT} = 5.0 V, I_L = 1.0 mA, R_{SC} = 0, C1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

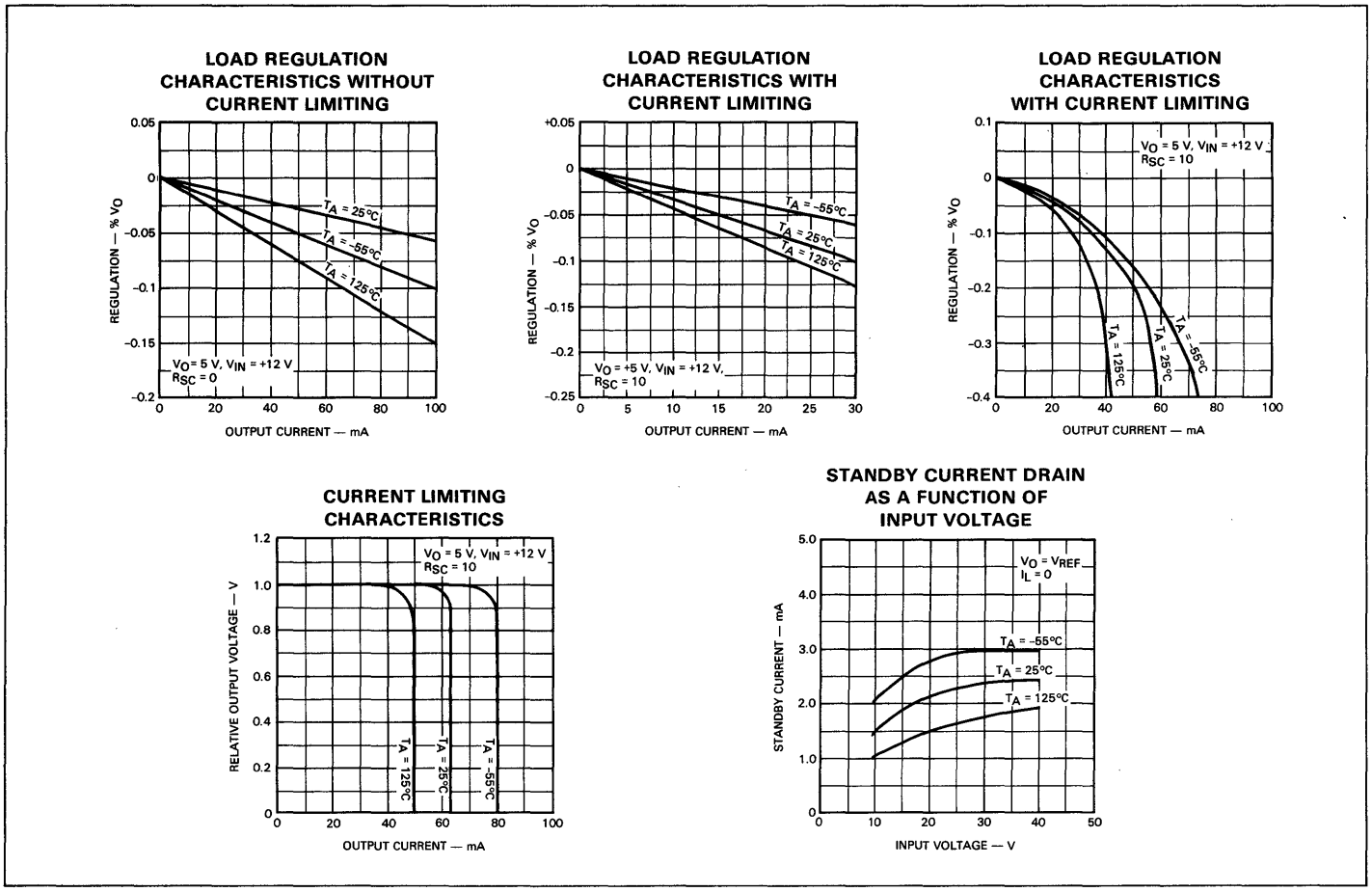


Fig. 7-4 Typical Performance Curves for 723

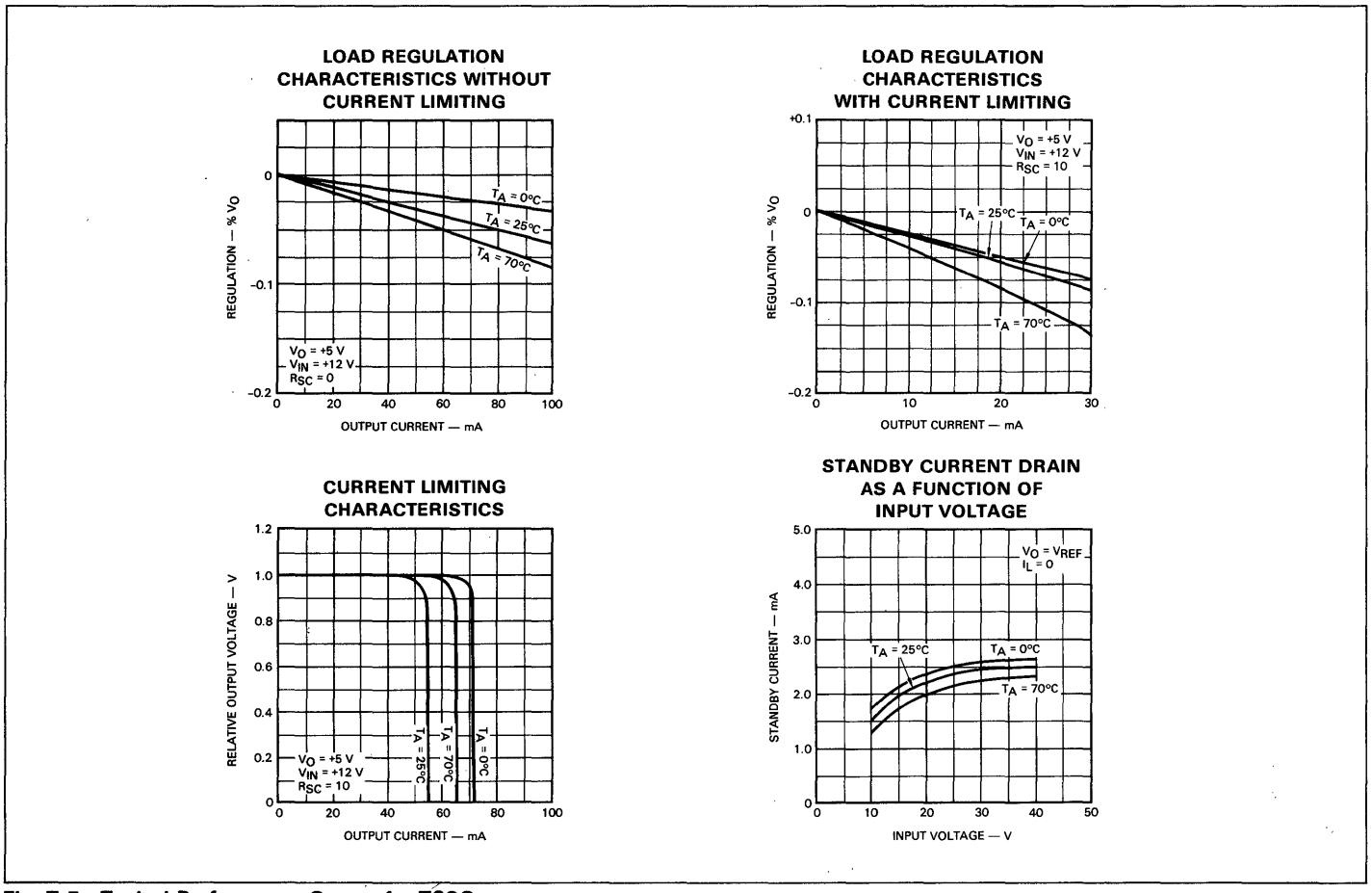


Fig. 7-5 Typical Performance Curves for 723C

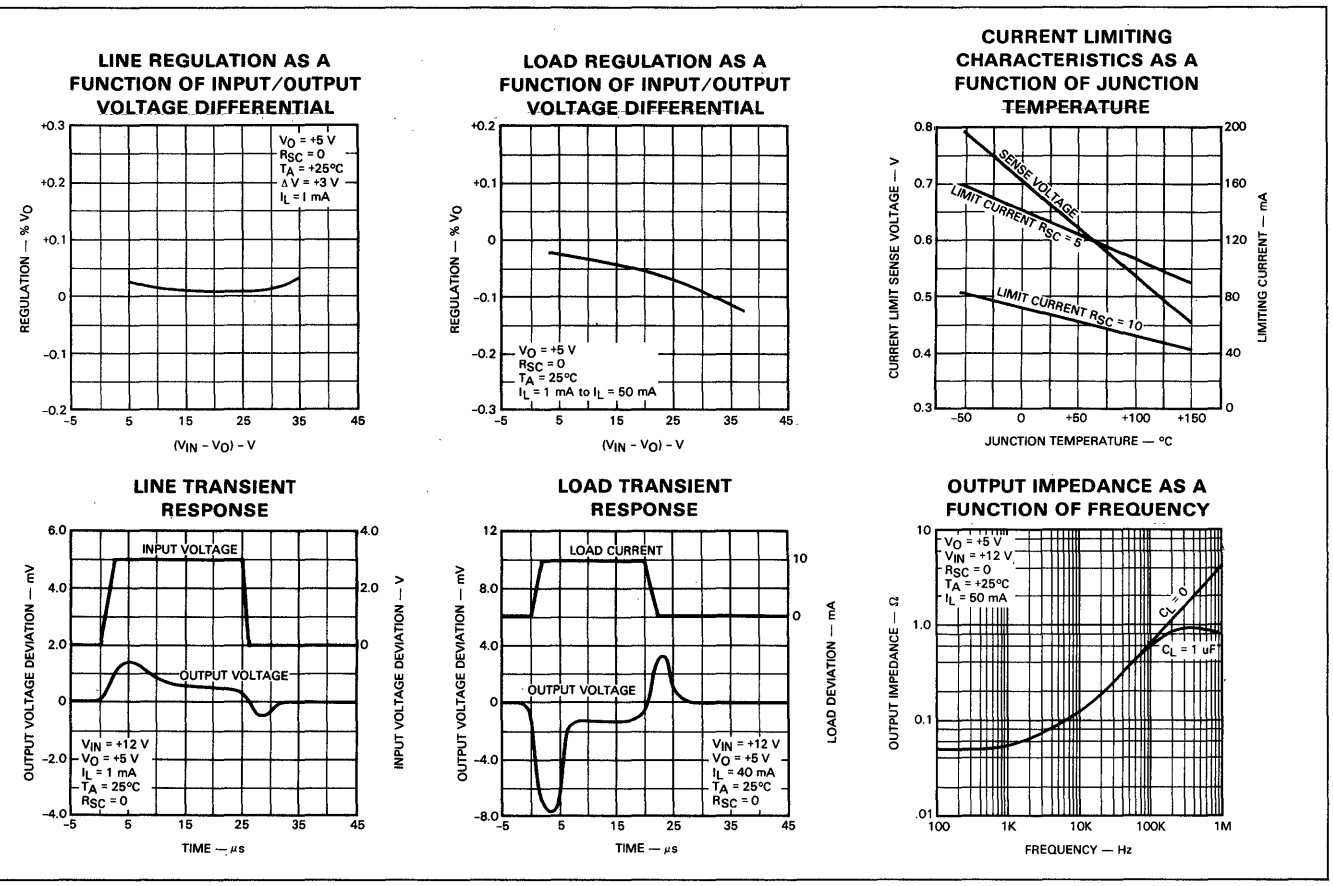
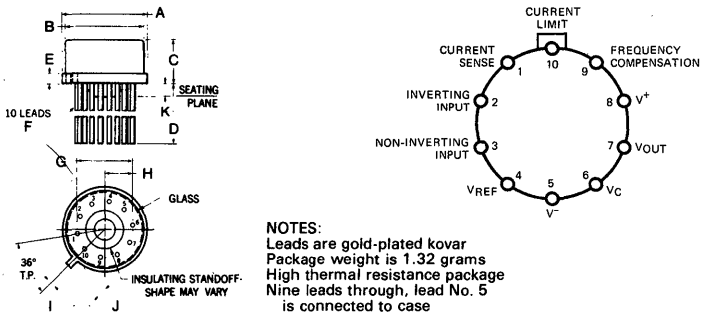


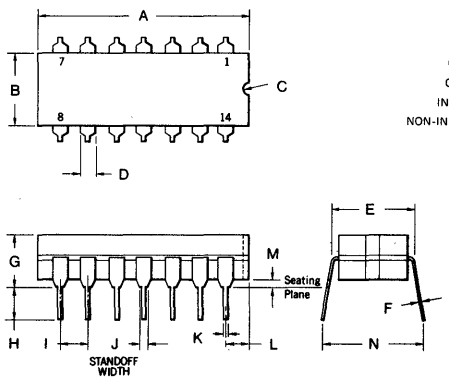
Fig. 7-6 Typical Performance Curves for 723 and 723C

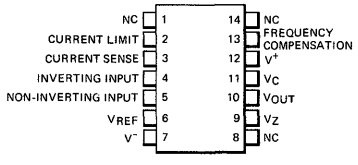


NOTES:
Leads are gold-plated kovar
Package weight is 1.32 grams
High thermal resistance package
Nine leads through, lead No. 5 is connected to case

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.335		0.370	8.51		9.40
B	0.305		0.335	7.75		8.51
C	0.165		0.185	4.19		4.70
D	0.500			12.70		
E			0.040			1.02
F	0.016		0.019	0.41		0.48
G		0.230			5.84	
H		0.115			2.92	
I	0.028		0.034	0.71		0.86
J	0.029		0.045	0.74		1.14
K			0.040			1.02

Fig. 7-7 JEDEC TO-100

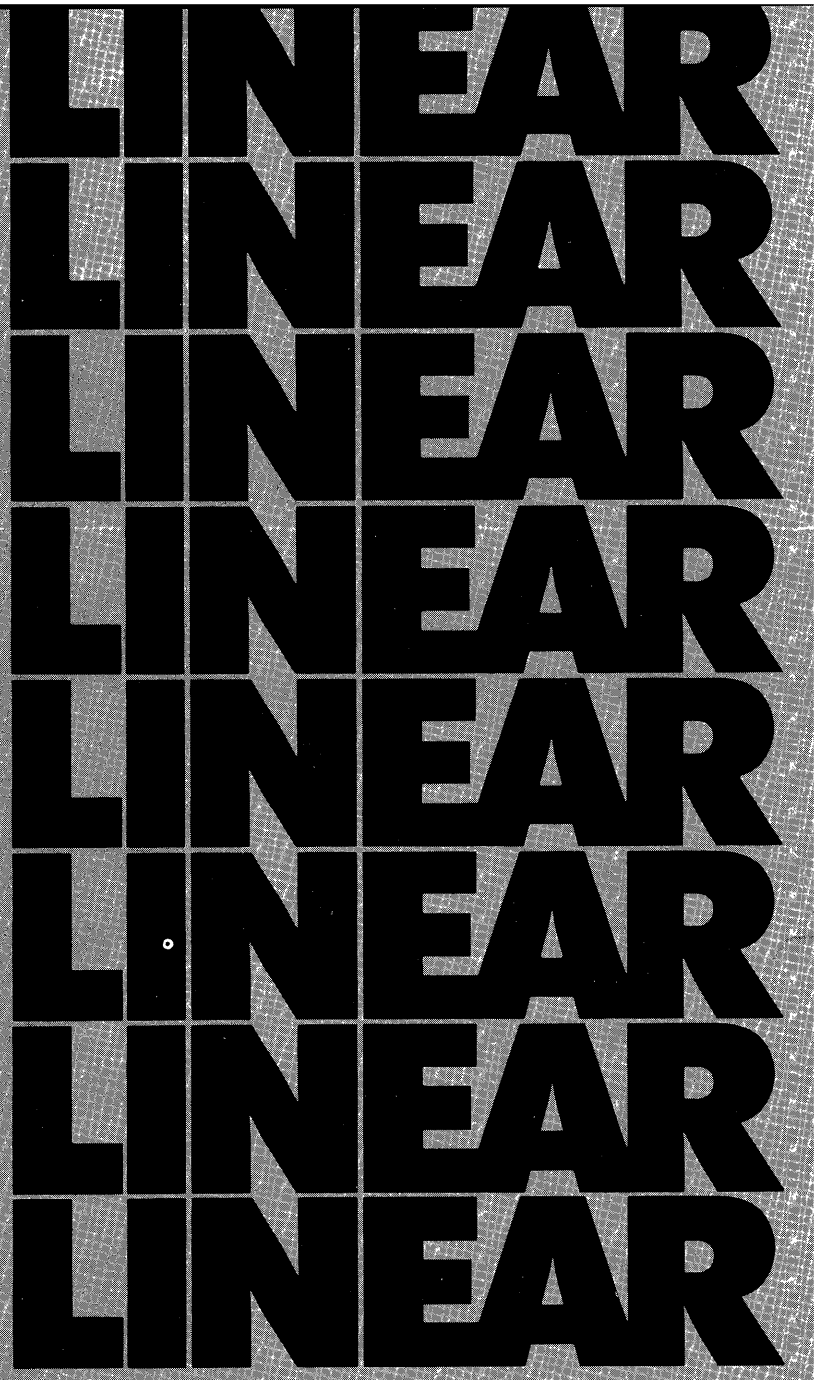




NOTES:
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.750		0.785	19.05		19.94
B	0.245		0.271	6.22		6.88
C		0.025			0.64	
D	0.045		0.065	1.14		1.65
E	0.290		0.310	7.37		7.87
F	0.009		0.011	0.229		0.279
G			0.200			5.08
H	0.100		0.165	2.54		4.19
I	0.090		0.110	2.29		2.79
J	0.027		0.037	0.69		0.94
K	0.016		0.020	0.41		0.51
L	0.065		0.095	1.65		2.41
M	0.015			0.38		
N		0.375			9.53	

Fig. 7-8 JEDEC TO-116



CONTENTS AND SECTION SELECTOR

IN THIS CHAPTER:

- FREQUENCY COMPENSATION
- THERMAL CONSIDERATIONS
- FUNCTIONAL TEST CIRCUIT
- TYPICAL APPLICATIONS

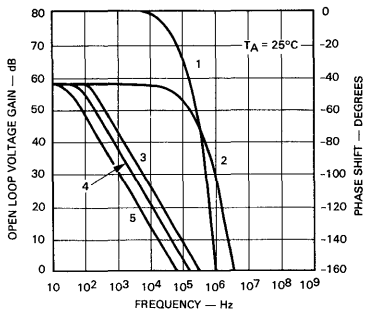
CHAPTER 8
µA723 Precision Voltage Regulator Applications

FREQUENCY COMPENSATION

The stability of any power supply configuration can be assured by two steps. First, consider the dc and ac performance of both the internal gain stage of the µA723 and all other active stages used. Then, provide the necessary compensation using standard operational amplifier techniques.

µA723 Open Loop Voltage Gain and Phase Shift as a Function of Frequency

Figure 8-1 shows the open loop frequency response of the µA723 voltage gain stage. The increase in the rate of phase shift seen in *Figure 8-1* is due to the Beta fall off of the output stage at higher frequencies. This increasing phase shift rate requires that the µA723 be compensated whether or not the device is used with external components.



1. OPEN LOOP PHASE SHIFT
2. OPEN LOOP VOLTAGE GAIN
3. GAIN WITH 5000 pF, COMP TO COMMON
4. GAIN WITH 0.01 µF, COMP TO COMMON
5. GAIN WITH 0.02 µF, COMP TO COMMON

Fig. 8-1 µA723 Open Loop Voltage Gain and Phase Shift as a Function of Frequency

Recommended frequency compensation for the unity gain is either a 5000 pF capacitor from the compensation terminal to the V– terminal or a 20 pF Miller compensation capacitor connected from the frequency compensation terminal to the inverting input. To allow proper operation when using the Miller compensation, the inverting input must be isolated from the remaining circuitry by some impedance. This is illustrated in *Figure 8-8a.*

For output voltages greater than V_{REF}, the closed loop gain will be greater than unity. If higher closed loop gains are used, the compensation capacitor can be reduced in direct proportion to the increase in gain.

When using an external series pass device, the 3 dB bandwidth of this device must also be considered, particularly since the majority of these devices have a much lower bandwidth than the µA723. For instance, if a 2N3055 is selected as the series pass device to be used in a unity gain configuration power supply, this device has a minimum f_T of 800 kHz and a maximum Beta of 70. This introduces a 3 dB point in the overall loop gain at approximately 11 kHz, which means that heavier frequency compensation of the regulator is required to assure stability. Since the first break point of 11 kHz is due to the external power device, the regulator should have less than unity gain at the second break point. The second break point is the first break point of the µA723 gain stage, which occurs at approximately 80 kHz as shown in *Figure 8-1.* Adequate compensation is provided by a 0.02 µF capacitor from the compensation terminal to common — or by a 40 pF Miller capacitor from the compensation terminal to the inverting input. As before, for any increase from unity gain, there can be a proportional reduction in the compensation capacitor. However, the value of the Miller capacitor may not be reduced in direct proportion to the standard compensation reduction; this is to allow for gain variations in the µA723 and for parasitic capacitances. Extra capacitance may be required at both the input and the output of any power supply due to the inductive effects of long lines. Adding output capacitance provides the additional benefit of reducing the output impedance occurring at higher frequencies.

THERMAL CONSIDERATIONS

µA723 Load Current Capabilities

Figure 8-2 provides a quick reference to the allowable power dissipation of the µA723 in terms of the input/output differential voltage and load current. *Figure 8-2a* is for the µA723C in the TO-100 package (10-lead metal can); *Figure 8-2b* is for the µA723/µA723C in the TO-116 package (14-lead, hermetic dual in-line); and *Figure 8-2c* refers to the MIL temperature range µA723 in the metal can package.

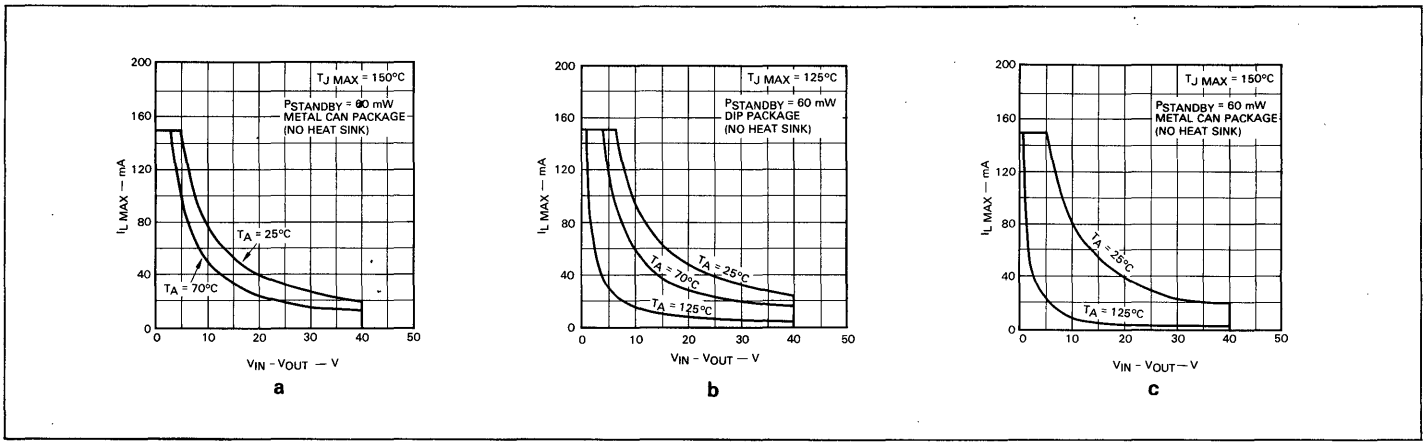


Fig. 8-2 µA723 Load Current Capabilities for Maximum Load Current as a Function of Input/Output Voltage Differential

μA723 Maximum Power Dissipation in Free Air

The previous curves are based on the free-air dissipation ratings shown in *Figure 8-3* below. The thermal derating factor is 6.8 mW/°C for the TO-100 metal can and 8 mW/°C for the TO-116 hermetic DIP. When it is necessary to heat sink the TO-100 package, a thermal resistance of 50°C/W, junction-to-case may be used.

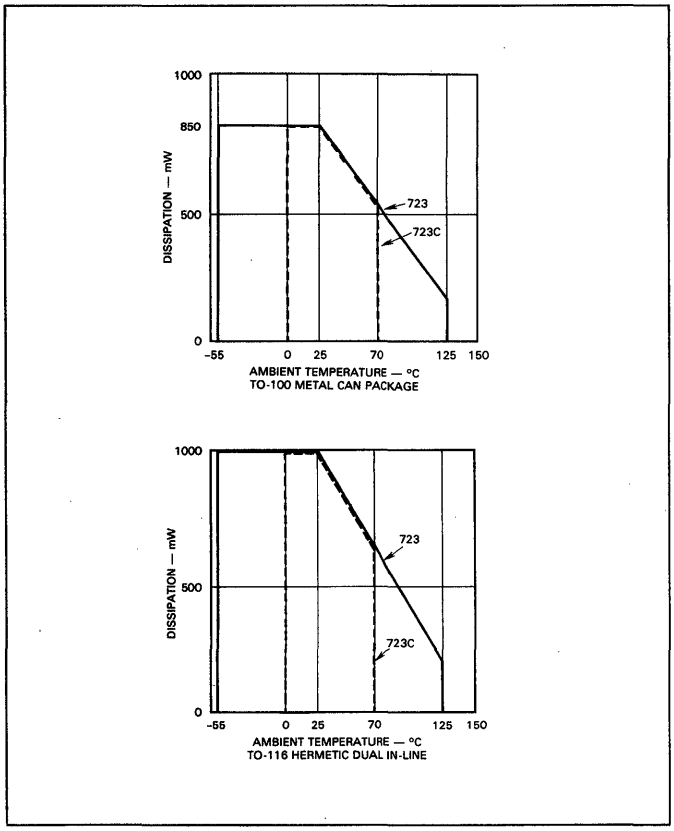


Fig. 8-3 μA723 Maximum Power Dissipation in Free Air

The relationship between power dissipation P_D, maximum ambient temperature T_A, and thermal resistance from case-to-ambient Θ_{CA}, is then:

$$P_D = \left(\frac{150°C - T_A}{50°C/W - \theta_{CA}}\right) W, \text{ or } \theta_{CA} = \left(\frac{150°C - T_A}{P_D}\right) - 50°C/W$$

These equations may be used to calculate the maximum allowable power dissipation, P_D, or the maximum allowable heat sink resistance, Θ_{CA}, from a given set of conditions.

FUNCTIONAL TEST CIRCUIT

Simplified Tester Schematic

A simplified functional test circuit for the μA723 is given in *Figure 8-4*. The output voltage is set for a nominal +5.0 V. The basic test steps are as follows.

1. Load Regulation at 50 mA, Close S1

   Measure output voltage change with S2 open and closed, (a load current change of 50 mA).

2. Line Regulation, Open S2

   Measure output voltage change resulting from a change in input voltage V_{IN}.

3. Short Circuit Current, Open S1 and S2

   Measure output current when the output is shorted to ground.

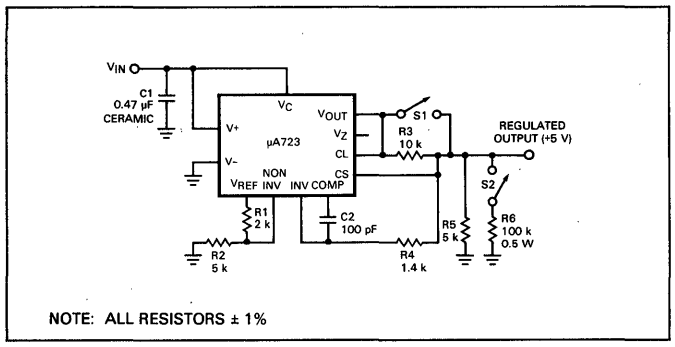


Fig. 8-4 Simplified Tester Schematic

TYPICAL APPLICATIONS

Introduction

The required output voltage for the following μA723 applications can be calculated from the equation accompanying each circuit. In all cases the resulting resistor values are assumed to include any potentiometer resistance used. In addition, *Table 8-1* is included at the end of the section and affords a quick reference for many standard output voltage requirements. The previous section on frequency compensation gives guidance to the suitable values of compensating capacitors used in the various appications. Specific transistor types are not included in this section. However, Appendix C includes a discussion of the selection of power devices and a list of preferred types.

In the following applications, the μA723 is represented in a number of ways. In those circuits where the regulator operation is very basic, the symbol of *Figure 8-5* is used. Lead functions can be identified by referring to *Figure 7-1.*

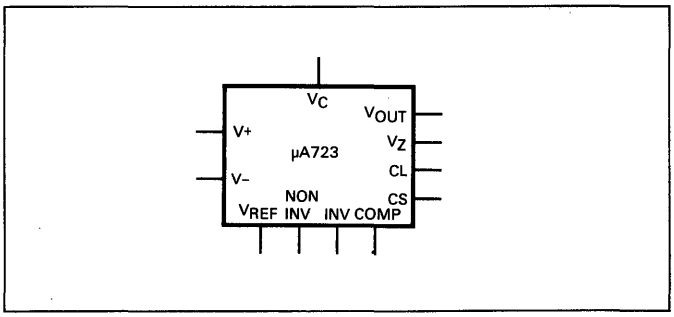


Fig. 8-5 μA723 Symbol

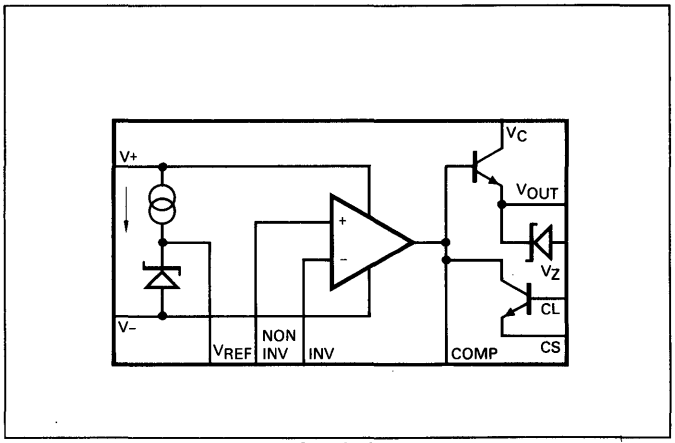


Fig. 8-6 μA723 Functional Symbol

In those applications where the circuit operation is clarified by the use of a functional schematic of the μA723, *Figure 8-6* is used. This block bears a close resemblance to the simplified schematic of *Figure 7-1.* In some cases the individual components of this block may be rearranged in order to simplify a particular schematic. The reference voltage is represented by a single Zener diode, nominal voltage 7.15 V supplied from a constant current source. The output Zener diode, V_{OUT} to V_Z, is shown only in the required applications.

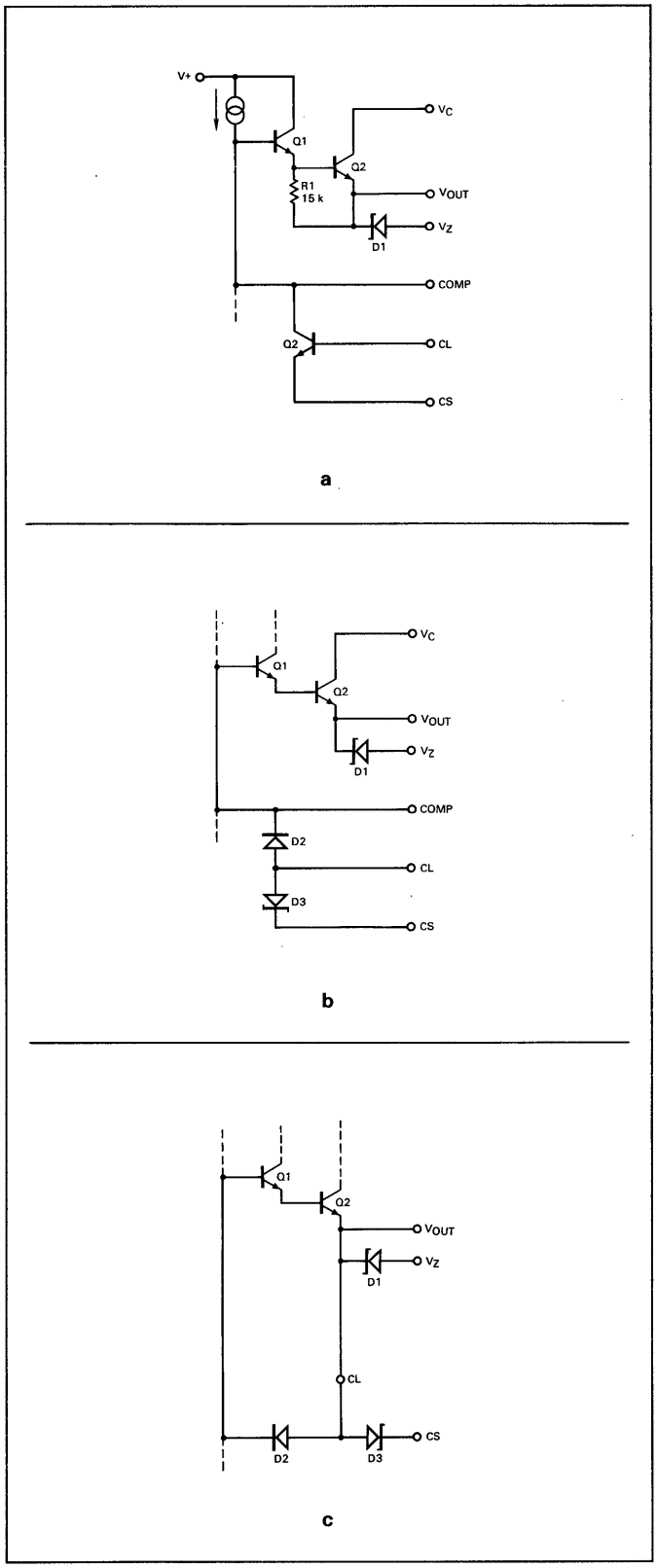


Fig. 8-7 Output Configurations

Output Configurations

Many of the applications use internal Zener diodes for level shifting or for the generation of stabilized voltages. An explanation of where these diodes exist in the μA723 circuit may help to avoid any problems arising from improper biasing.

The μA723 output stage schematic is reproduced in *Figure 8-7a.* The V_Z terminal provides direct access to a 6.2 V Zener diode whose cathode is internally connected to V_{OUT}. Provided the internal current limit transistor is not required for output short circuit protection, its base emitter junction provides another 6.2 V Zener diode (See *Figure 8-7b*). Note, however, that the anode of this diode, terminal CL, is connected internally by the collector base junction diode to the base of the output drive transistor. When using the CL – CS Zener diode, the collector base diode must always be reverse biased. Maximum permissible CL – CS Zener current is 5 mA. Correct biasing is assured in *Figure 8-7c* by interconnecting the V_{OUT} and CL terminals to provide both positive and negative 6.2 V Zener diodes referenced to the V_{OUT} terminal.

Positive Regulators, 150 mA Maximum

Figure 8-8a shows the basic low voltage configuration suitable for output voltages ranging from 2 to 7 V. The reference voltage, V_{REF}, is first divided down by R1, R2 and, if desired, potentiometer P1. Then it is applied to the non-inverting input of the error amplifier. C_{REF} may be added if ripple rejection greater than that specified for the μA723 (74 dB) is required. The presence of C_{REF} also reduces the regulated output noise voltage considerably.

Capacitor C1 provides frequency compensation. C1 is isolated from the low impedance output by R3 which also balances the error amplifier source impedances to give minimum temperature drift. To minimize component count at the expense of temperature drift, R3 may be omitted. In this case, C1 cannot be used for frequency compensation. Instead, C2 may be used from the compensation terminal to ground as shown in *Figure 8-8b.* To minimize power dissipation, the V+ and V_C terminals may be supplied separately, with V+ requiring a minimum of 9.5 V, while the V_C supply may be as low as 3 V above the regulated output voltage. The schematics shown in *Figure 8-8a* and *8-8b* have output voltages given by

$$V_O = \left(\frac{R2}{R1 + R2}\right) V_{REF} \text{ where } (R1 + R2) > 1.5\ k\Omega$$

Output voltages from 7 to 37 V are obtainable with *Figure 8-8c* in which

$$V_O = \left(\frac{R1 + R2}{R2}\right) V_{REF}$$

If the reference bypass capacitor is required in this circuit, it should be connected from the non-inverting input to ground using R3 to increase the reference source impedance and improve the effectiveness of the reference capacitance. A 150 mA output current is available with R_{SC} set to zero. When short circuit current limiting is desired, R_{SC} may be used to limit the maximum output current to

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

where V_{SENSE} (the sense voltage, or the voltage between terminals CL and CS) is given in *Figure 8-8d.* The resulting output current limit has a temperature coefficient of –0.3%/°C.

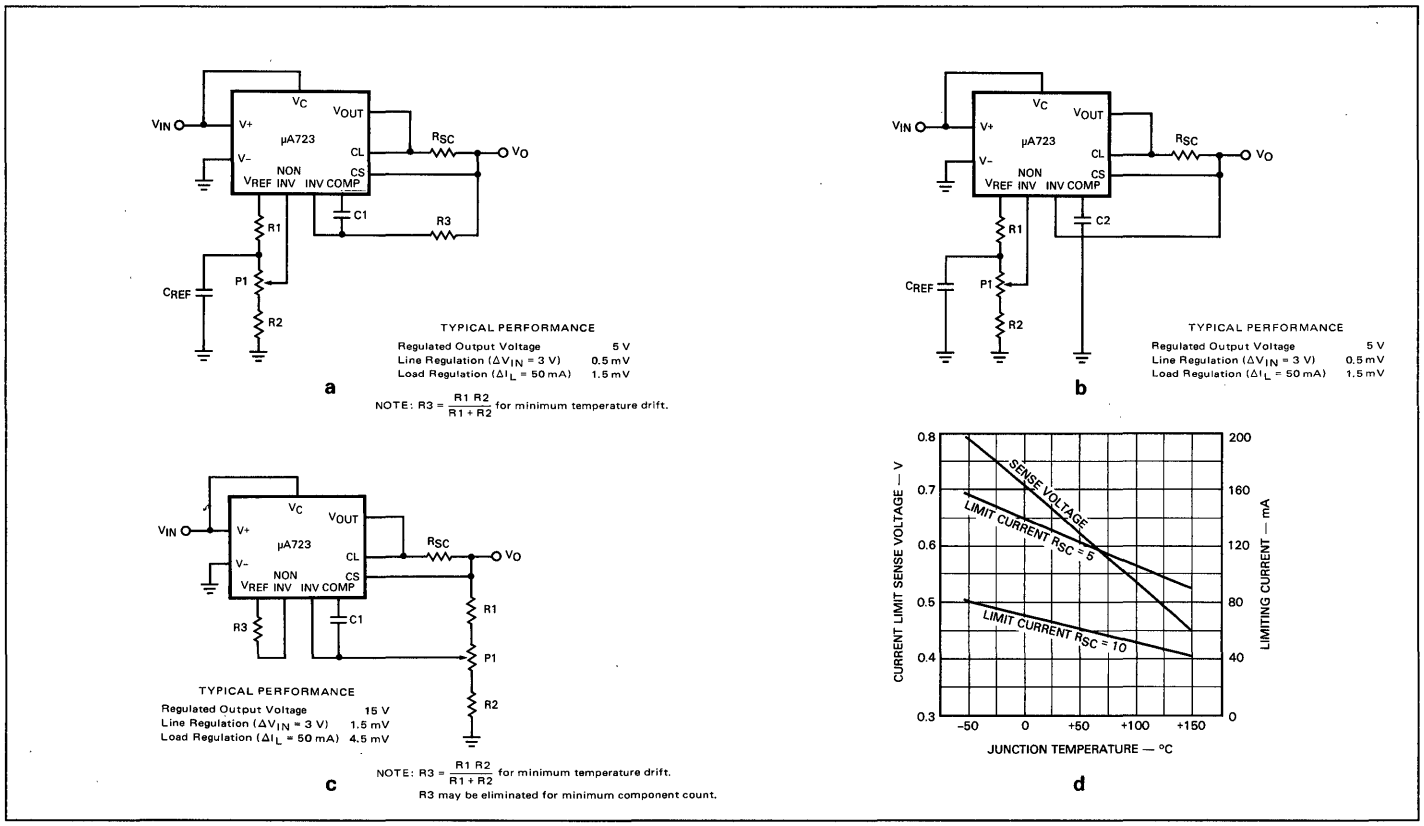


Fig. 8-8 Basic Regulator Configurations

Positive Regulators, High Output Current

In *Figure 8-9a,* an npn transistor, Q1, boosts the available output current beyond the capability of the μA723. Q1 can consist of several transistors cascaded to satisfy very high current requirements. In this circuit, one V_{BE} voltage must be added to the 3 V minimum input/output differential requirement for each transistor added. Depending on the type of transistor used for Q1, R3 should be added giving I_{CBO} compensation, and alleviating the safe area limitation of the output device. With R_{SC} set to zero the maximum output current capability is (Q1 Beta) x (150 mA). R_{SC} may be used to limit the short circuit current to any desired value up to this maximum in the same manner as outlined previously in *Figure 8-8.*

An alternate circuit is shown in *Figure 8-9b.* Using an external pnp transistor, maximum output current is again (Q1 Beta) x (150 mA). One V_{BE} should be added to the minimum input/output differential voltage requirement for each additional transistor. The circuits in *Figure 8-9* may supply outputs in the range of 2 to 37 V by selecting the appropriate feedback network. *Figure 8-9a* is shown for output voltages from 7 to 37 V, whereas *Figure 8-9b* is shown for output voltages from 2 to 7 V.

If it is required to vary the output continuously over a 10 to 1 range, it is necessary first to attenuate V_O so that V_{INV} never exceeds V_{REF} even when V_O is at its maximum value, then provide a potentiometer adjustment from V_{REF} to the non-inverting input. This is illustrated in *Figure 8-9c*, where V_O is attenuated by a ratio of 5.2:1.

Maximum permissible V_O is then 35 V (giving a V_{INV} of 6.8 V), which requires 38.6 V ≤ V_{IN} ≤ 40 V. Minimum V_O is determined by the minimum value for V_{INV}. The specified minimum V_{INV} is 2 V; however, it will be found that typically V_{INV} may be reduced to approximately 0.72 V before the circuit no longer regulates. This corresponds to a V_O of 3.7 V.

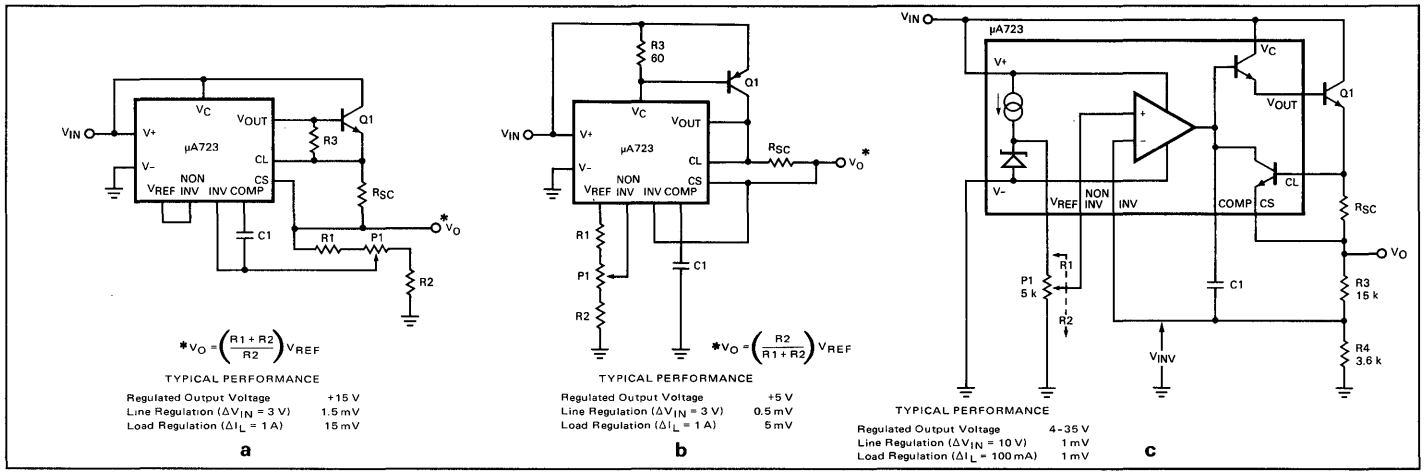


Fig. 8-9 High Current Regulators

Other 10 to 1 voltage ranges may be obtained by varying the attenuation ratio, (R3 + R4)/R4, from 5.2 to, say, 1.4. Then V_O range will be 1 V to 10 V (13.6 V ≤ V_{IN} ≤ 39 V).

Figure 8-9c,

$$V_O = V_{REF}\left(\frac{R2}{R4}\right)\left(\frac{R3 + R4}{R1 + R2}\right)$$

or, with the values of R3 and R4 as shown,

$$V_O = 5.2\ V_{REF}\left(\frac{R2}{R1 + R2}\right)$$

Positive Shunt Regulator

The µA723 may be used in a shunt regulating mode by adding an external transistor, Q1. Special attention should be paid to ensure that the series limiting resistor, R4, is capable of handling the high power dissipation inherent in this mode of operation. *Figure 8-10a* is used with the 14-lead DIP version of the µA723. When the 10-lead metal can is used, however, it is necessary to add a 6.2 V Zener diode externally, as in *Figure 8-10b.*

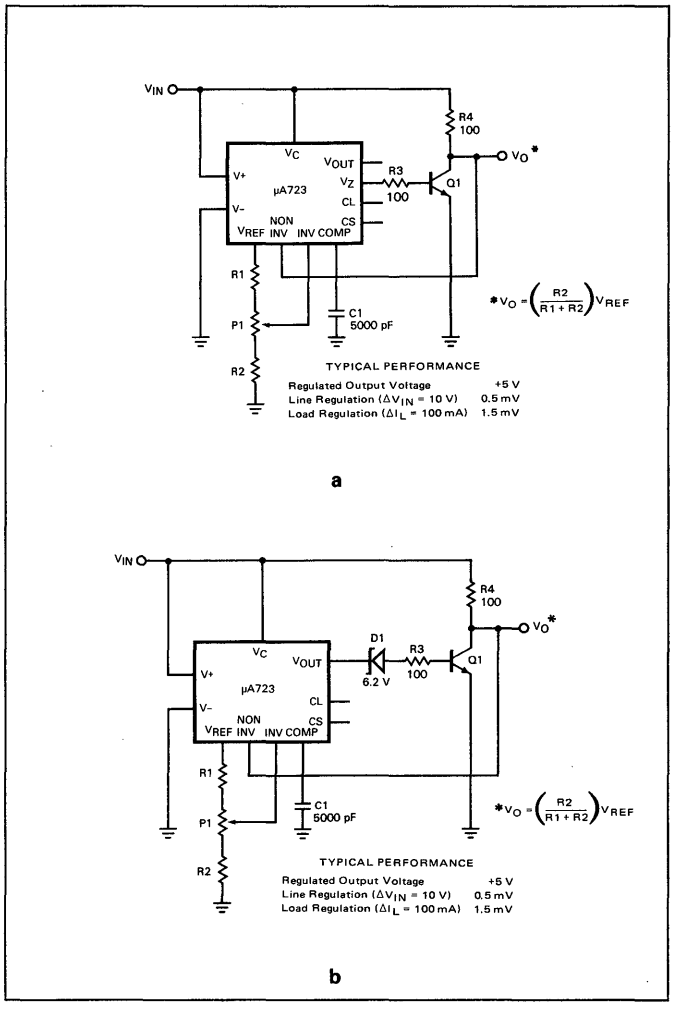


Fig. 8-10 Positive Shunt Regulators

Positive Regulators, High Line Rejection

As shown in *Figure 8-11a* and *8-11b,* the circuits each use the internal current limit transistor to preregulate the V+ supply, thereby increasing the line rejection to more than 100 dB. The CS – CL terminals provide a 6.2 V Zener diode referenced to the output voltage, which is then used to supply V+. In these applications R3 must be chosen so that the current into the CS terminal is limited to 5 mA maximum.

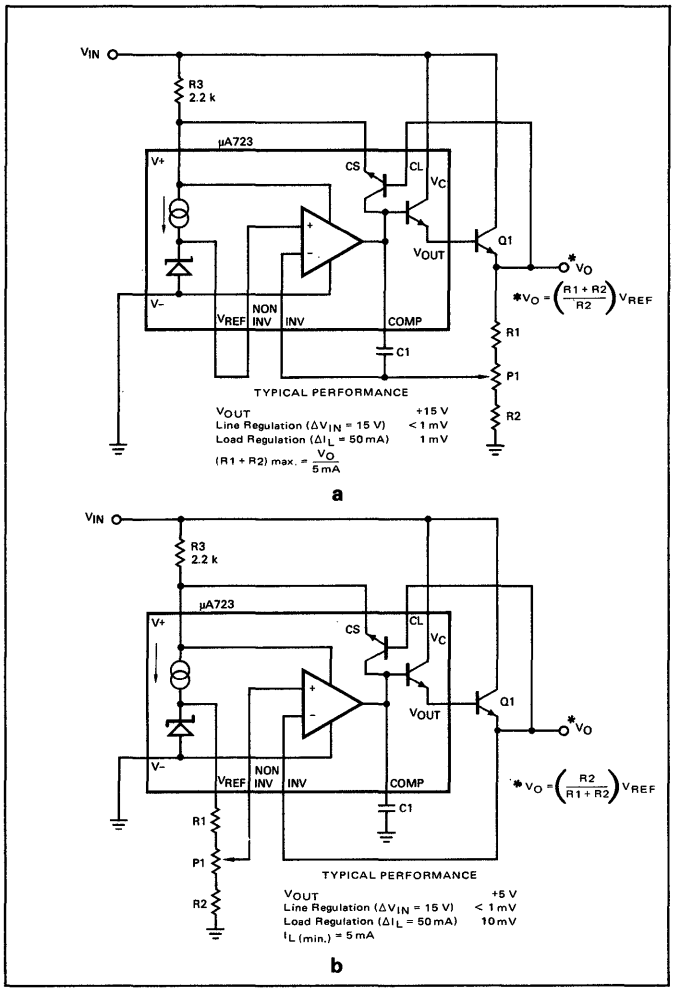


Fig. 8-11 High Line Rejection

Positive Regulators, High Input Voltage

Input voltages greater than 40 V may be applied when the µA723 is connected as shown in *Figure 8-12a.* The regulated output voltage must remain less than 38 V to protect the regulator. R3 may be replaced with a FET current source in those cases where the variation of input voltage imposes excessive power dissipation in the internal series pass device. Q2 provides short circuit protection, if required (the internal current limit transistor cannot be used in this application). The maximum input voltage is determined by the breakdown characteristics of Q1. When using the µA723 DIP version, D1 may be omitted and the V_Z terminal grounded; in this case V_{REF} must be resistively divided by two before being applied to the inverting input.

Note that in this type of application where the µA723 output stage is used as an additional inverting amplifier rather than the usual emitter follower, V_{REF} must be connected to the inverting input of the error amplifier to maintain correct phase relationships around the regulating loop, i.e., negative feedback from the output.

When using a pnp series pass device, high input voltages may be tolerated by using a Zener diode to reduce the voltage appearing across the µA723, as in *Figure 8-12b.* For example, if D1 is a 20 V Zener diode, input voltages to 60 V are permissible. D1 must be selected such that no more than 40 V is applied to the µA723 V+ and V_C terminals under maximum input voltage conditions. Similarly, the regulated output voltage must not exceed 37 V to maintain the specified input-to-output differential.

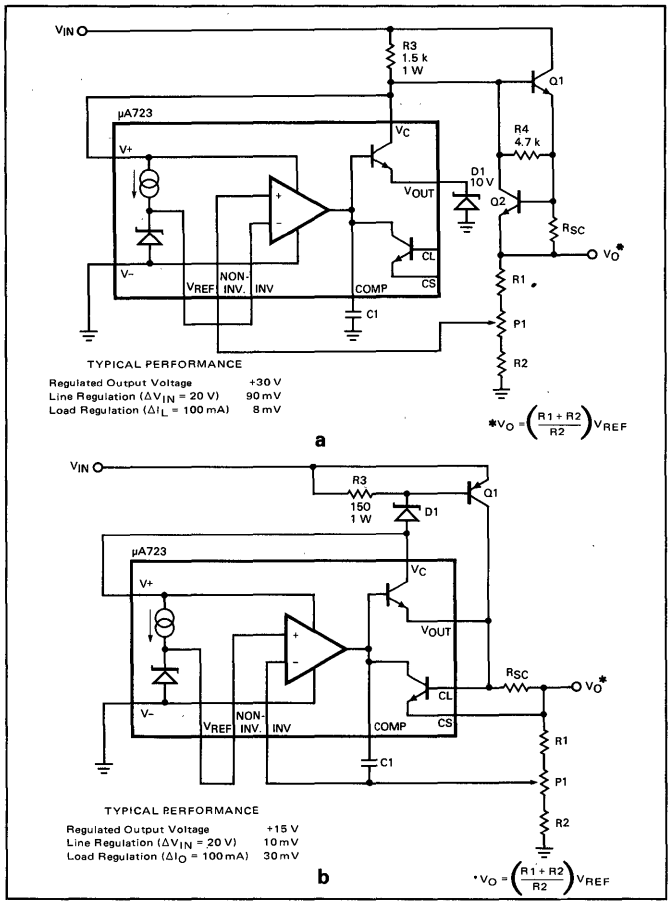


Fig. 8-12 High Input Voltage

Positive Regulator, Floating

The μA723 may be used to directly regulate hundreds of volts using the configuration shown in *Figure 8-13,* in which a floating power source is provided for the regulator by D1. The series pass transistor becomes the only limiting factor in determining the maximum voltage and current which may be controlled. The V_{REF} terminal supplies all the current drawn by the sensing resistors and the total current must not exceed 5 mA. R5 must be selected to provide sufficient current to bias D1 and to supply the μA723 standby current at the minimum input voltage condition. D2, D3 and D4 are for protection purposes; fast switching diodes should be used.

If Q1 is a high f_T device, it may be necessary to add C2 to reduce the output noise level. If V_{IN} is switched on and off, causing a very high dV_{IN}/dt to appear at the μA723 terminals, C3 may be added to ensure correct biasing throughout the circuit. In normal use when on/off switching takes place before the usual rectifier/filter supply for V_{IN}, C3 is not necessary.

It will be noted from *Figure 8-13* that

$$V_O = V_{REF}\left[\left(\frac{R2}{R1}\right) - \left(\frac{R3}{R1}\right)\left(\frac{R1+R2}{R3+R4}\right)\right]$$

If R3 and R4 are made equal,

$$V_O = \frac{V_{REF}}{2}\left(\frac{R2-R1}{R1}\right)$$

The normal minimum regulated output voltage limitation of 2 V for the μA723 does not apply to this circuit, output voltages down to zero volts being readily obtainable.

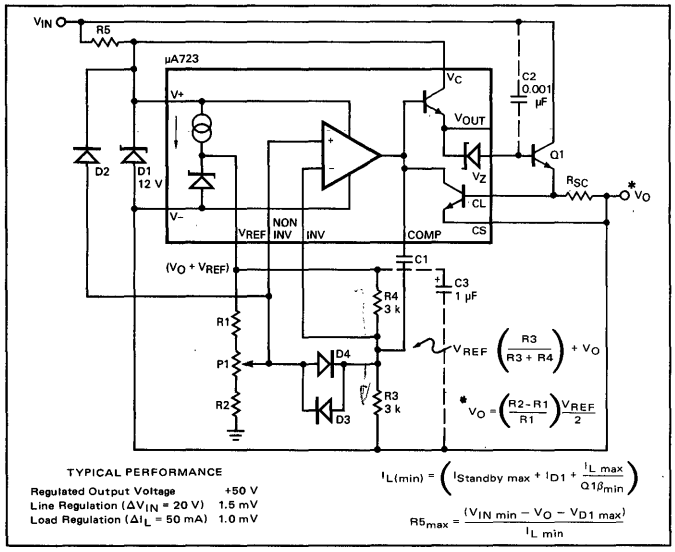


Fig. 8-13 Floating Positive Regulator

Assuming the regulator is operating correctly, then the INV input will equal the NON-INV input, i.e.,

$$(V_O + V_{REF})\left(\frac{R2}{R1+R2}\right) = (V_{REF})\left(\frac{R3}{R3+R4}\right) + V_O$$

$$V_O\left(\frac{R2}{R1+R2} - 1\right) = V_{REF}\left[\left(\frac{R3}{R3+R4}\right) - \left(\frac{R2}{R1+R2}\right)\right]$$

$$V_O = V_{REF}\left[\left(\frac{R2}{R1}\right) - \left(\frac{R3}{R1}\right)\left(\frac{R1+R2}{R3+R4}\right)\right]$$

Positive Regulators, Low Input/Output Differential

Either of the two circuits shown will allow an input-to-output voltage difference close to the saturation point of the series pass device. As in all applications, the $V_{IN(2)}$ of *Figure 8-14b*

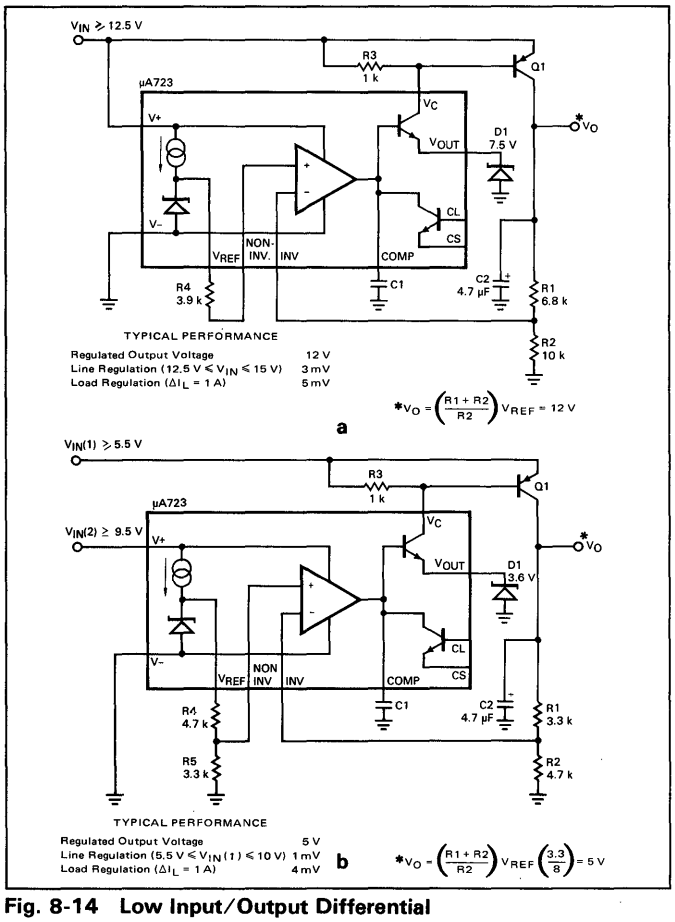


Fig. 8-14 Low Input/Output Differential

must be 9.5 V minimum. The 7.5 V Zener diode may be eliminated (See *Figure 8-14a*) when using the dual in-line package by grounding the V_Z terminal and reducing the V_{REF} to 3 V by a 4.7 kΩ/3.3 kΩ voltage divider to the non-inverting input of the μA723.

Positive Regulators, Marginal Input Voltage

The two circuits shown in *Figure 8-15* offer some relief from the 9.5 V minimum V+ voltage when regulating lower voltages. In those cases where the average voltage applied to the input is greater than the required minimum — but the negative ripple peaks are lower — a diode/capacitor peak detector will provide the solution *(Figure 8-15a). Figure 8-15b* shows one method of using a voltage doubler to assure that using a minimum of external components, the proper bias voltage is applied to the V+ terminal.

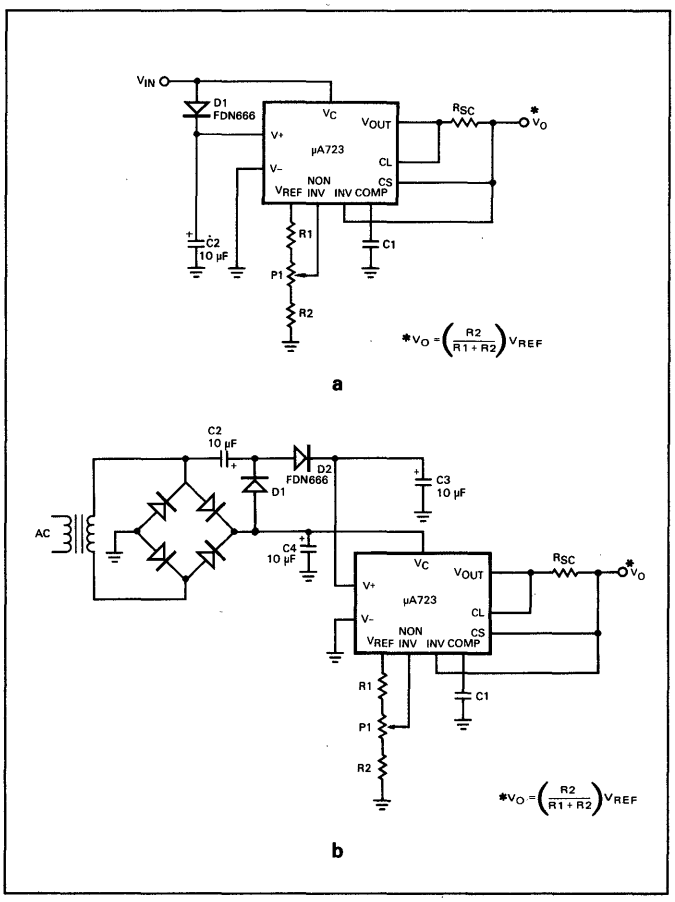


Fig. 8-15 Marginal Input Voltage

Negative Regulators, Medium/High Output Current

This configuration *(Figure 8-16a)* will regulate any negative voltage between -9.5 V and -40 V. Since the uA723 is operated between ground and the regulated output, the maximum unregulated input voltage is determined by the voltage breakdown and power dissipation capabilities of the pnp series pass device, Q1. Base current for Q1 is supplied through resistor R5 such that the minimum input-to-output differential is controlled both by the base current required by Q1 and the value of R5.

A Darlington connection may be used for Q1 to reduce the base current requirement *(Figure 8-16b)* and to increase the output current capability. Either the complementary Darlington as shown, or a standard pnp pair may be used.

For output voltages in the range -2 V to -9.5 V, the output voltage alone is insufficient to bias the μA723 in *Figure 8-16a.* This condition is satisfied in *Figure 8-16c* by an external, regulated or unregulated, positive voltage applied to the V+ and V_C terminals. The maximum limit of 40 V between the V+ and V- terminals must be observed. Maximum values for $-V_{IN(2)}$ and the input-to-output differential are determined as for *Figure 8-16a.*

In all cases, *a* through *c*, if the V_Z terminal is unavailable, then the V_{OUT} terminal may be used with a series 6.2 V Zener diode.

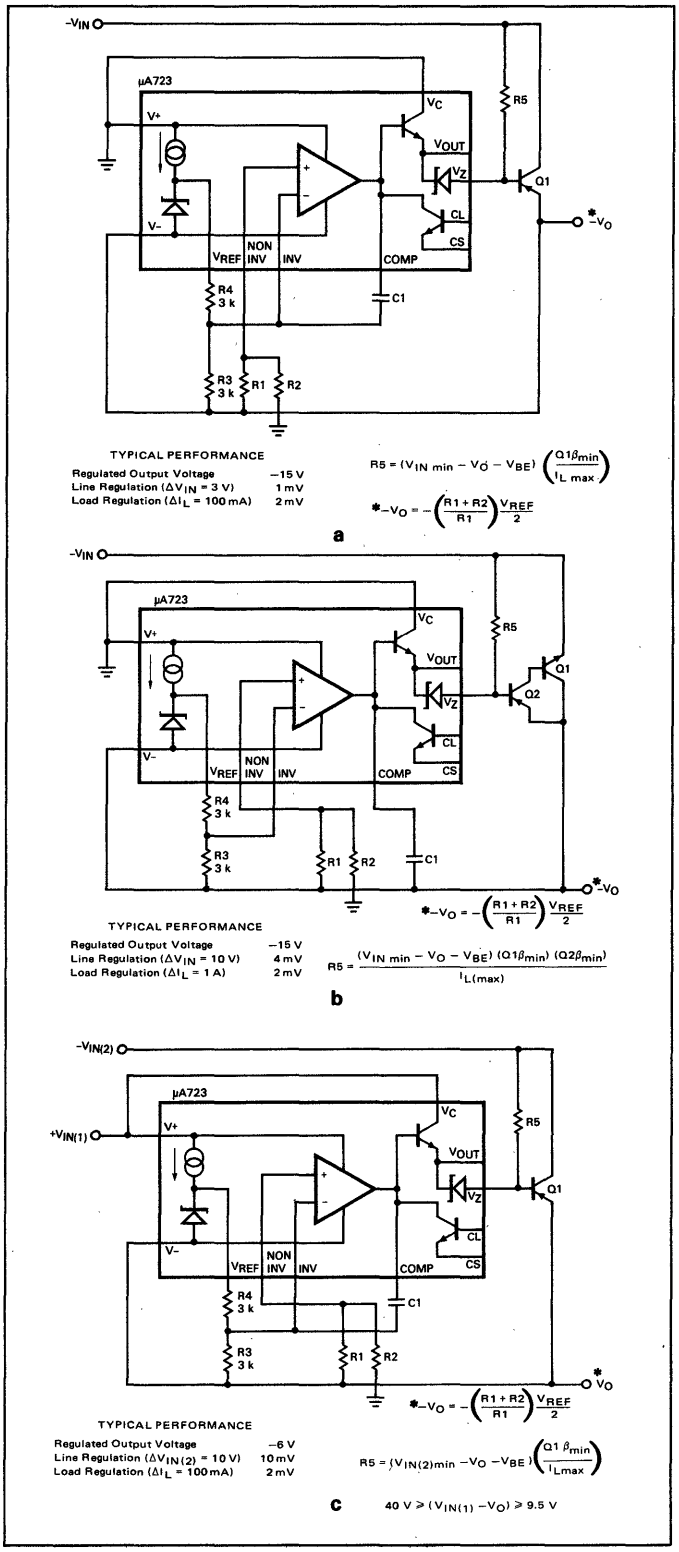


Fig. 8-16 Medium/High Output Current

Negative Shunt Regulator

For low to medium output currents the series pass transistor of the previous circuits may be omitted. However, special attention must be paid to the dissipation of D1 and R5, and the internal dissipation of the µA723. Maximum permissible current shunted to ground via the V_{OUT} terminal is 150 mA.

Figure 8-17 as shown in suitable for output voltages in the range -9.5 V to -40 V. By removing the V+ and V_C terminals from ground and supplying them with a low value positive voltage as in *Figure 8-16c,* output voltages from -2 V to -9.5 V are obtainable. Total voltage from V- to V+ of 9.5 V minimum and 40 V maximum must be observed. If the maximum current from the V_{OUT} terminal is less than 20 mA in a particular application, then D1 may be omitted and the output connected to V_Z instead of V_{OUT}.

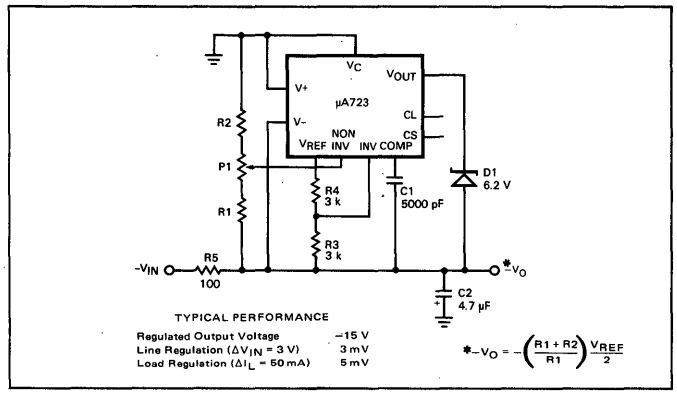


Fig. 8-17 Negative Shunt

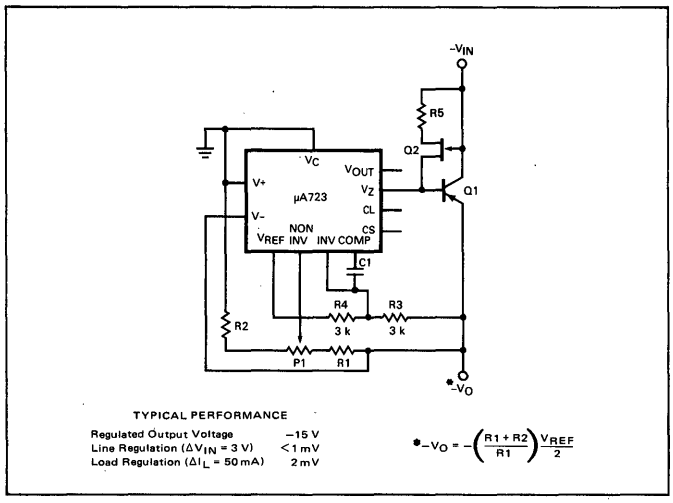


Fig. 8-18 Negative High Line Rejection

Negative Regulator, High Line Rejection

In the negative regulators with a series pass device, the only variation seen by the control circuitry under varying input conditions is the current variation caused by the fixed resistance across the series transistor's collector-base junction.

By replacing the resistor with a FET current source in *Figure 8-18,* the line rejection is greatly improved, typically exceeding 100 dB. Output voltage range is -9.5 V to -40 V, extendable down to -2 V by the addition of a positive supply as in *Figure 8-16c.* R5 and Q2 must be selected to provide sufficient base current for Q1 under worst case conditions. A good choice for Q2 would be a 2N5484 with R5 equal to zero, since its I_{DSS} (zero gate voltage drain current) of 1 to 5 mA will provide sufficient base current for Q1 in most applications.

Negative Regulator, Floating

When the desired output voltage exceeds the 40 V maximum which may be applied across the device, then a Zener diode should be used to limit the voltage, as shown *(Figure 8-19).* The actual Zener voltage selected may be between 9.5 V and 40 V with little change in performance. This circuit is the complement of *8-13.* R6 must be selected to provide sufficient current to bias D1 and to supply the µA723 standby current under minimum input voltage conditon. Select R5 according to the requirements outlined in *Figure 8-16b.*

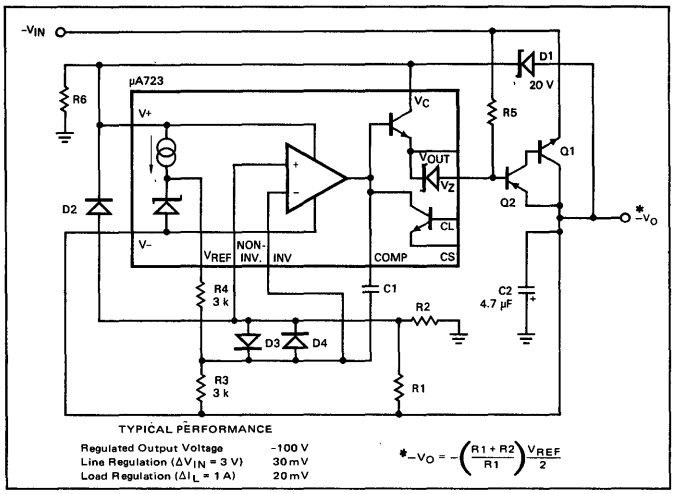


Fig. 8-19 Negative Floating

Current Regulators

In *Figure 8-20a* the regulator will force a voltage to appear across R_p which is equal to the voltage existing across R2. The resulting current is summed with the regulator's standby current, I_{SB}, and the current through R2, to provide a regulated current, I_L, into the load, R_L. Due to this summation, line regulation decreases for output currents below 10 mA.

The input voltage must be greater than I_L $R_{L(max)}$ +9.5 V to ensure sufficient voltage across the µA723. *Figure 8-20a* is shown sourcing current from a positive voltage $+V_{IN}$. V_{IN} can, of course, be grounded while returning R_L to a negative voltage. Similarly, the output terminal may be grounded or taken to a negative voltage when the V_{IN} terminal will provide a regulated current sink of magnitude I_L. In no case may the voltage from V- to V+ exceed 40 V.

$$I_L = \left(\frac{R2}{R1+R2}\right)\left(\frac{V_{REF}}{R_P}\right) + I_{SB} + I_{R2} = \left(\frac{V_{REF}}{R1+R2}\right)\left(1+\frac{R2}{R_P}\right) + I_{SB}$$

for output currents in excess of 10 mA, this approximates to:

$$I_L = \left(\frac{R2}{R1+R2}\right)\left(\frac{V_{REF}}{R_P}\right) + I_{SB} \simeq \left(\frac{3000}{R_{P(\Omega)}}\right) + I_{SB} \text{ mA}$$

with the values of R1 and R2 shown.

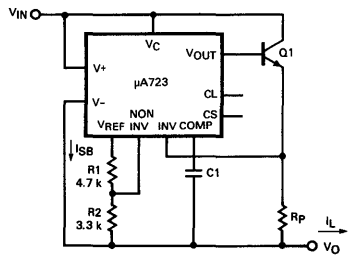
If a voltage compliance greater than 40 V is required, or if the regulation of *Figure 8-20a* is insufficient, the configuration in *Figure 8-20b* may be used. It is a precision floating current source capable of 0.05% regulation. In this circuit a floating 20 V supply (typically a half wave rectified output from a separate transformer winding of the main supply) is used to power the µA723, such that standby and reference currents do not add to the programmed output current.

$$I_L = \left(\frac{R2}{R1+R2}\right)\left(\frac{V_{REF}}{R_P}\right).$$

If P1 is adjusted so that V_{R2} = 3.0 V, as indicated in the schematic, then

$$I_L = \frac{3000}{R_{P(\Omega)}} \text{ mA}.$$

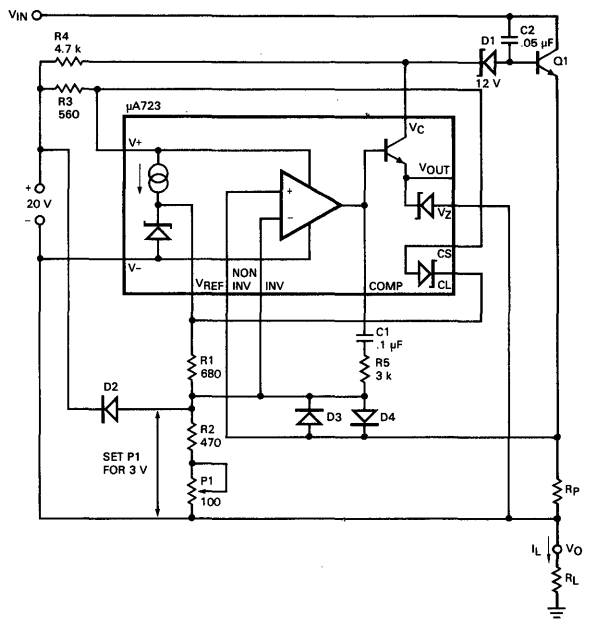
Both output current and voltage compliance are limited by the capabilities of the series pass device Q1. Diodes D2 through D4 are protection diodes which should be included whenever V_{IN} exceeds 40 V.



TYPICAL PERFORMANCE

Output Current	3.0 mA
Line Regulation (ΔV_{IN} = 5 V)	0.3 mA
Load Regulation (ΔR_L = 200 Ω)	0.2 mA

a



TYPICAL PERFORMANCE

Output Current	10 mA
Line Regulation (% of ΔV_{IN})	<.01 %
Load Regulation (ΔV_O = 10 V)	<.05 %

b

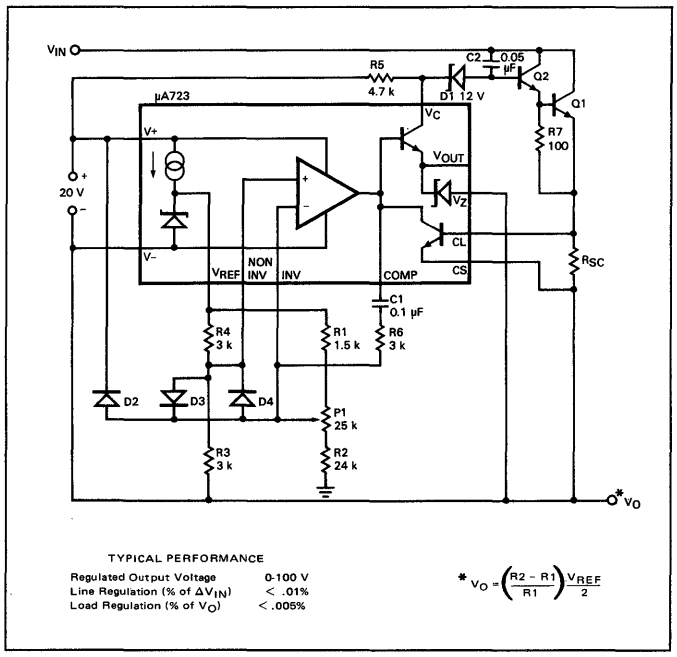
Fig. 8-20 Current Regulators

Precision Voltage Regulator

Figure 8-21 uses the same principle as the previous circuit to give a voltage output capable of 0.005% load regulation. Output voltage range is from zero volts up to the series pass device limit. Output current is also limited only by the series pass device; short circuit protection is available in this configuration by selecting R_{SC} as previously described. Protection diodes D2, D3, and D4 should be added whenever V_{IN} exceeds 40 V.

$$V_O = \left(\frac{R2-R1}{R1}\right)\frac{V_{REF}}{2}$$

With the component values shown, this gives an output voltage range of zero to 100 V.



TYPICAL PERFORMANCE

Regulated Output Voltage	0-100 V
Line Regulation (% of ΔV_{IN})	< .01%
Load Regulation (% of V_O)	< .005%

$$*V_O = \left(\frac{R2-R1}{R1}\right)\frac{V_{REF}}{2}$$

Fig. 8-21 Precision Voltage Regulator

Foldback Current Limiting

Foldback current limiting is a superior alternative to standard current limiting techniques particularly where intolerable output device power dissipation is a problem. Typically, this is a consequence of device/heat sink limitations under short circuit conditions.

In the following discussions it is assumed that a regulated output voltage is available up to a maximum output current I_M. The output current then folds back with decreasing load resistance to a value of I_{SC} (with a short-circuit load). The "knee" of the current limiting characteristic will be similar to that shown in Chapter 7 *(Figure 7-8d* and *h)* for normal current limiting. The regulation degrades considerably as I_M is approached, and in a practical regulator the useful output current may be limited to approximately 80% of I_M.

A minimum parts/cost method for providing the positive feedback required for foldback action is shown in *Figures 8-22a* and *b.* This technique introduces positive feedback by increased current flow through R1 and R2 under short circuit conditions. This forward biases the sensing transistor's base-emitter junction. The final percentage of foldback depends on the relative contributions of the voltage drop across R2, and R_{SC} to the base current of the sensing transistor. In the active region where the voltage buildup of R2 and R_{SC} provides base current to the sensing transistor, recovery of the

full output capability will take place whenever a short circuit is removed from the output. As soon as there is no voltage buildup across R_{SC} providing a portion of the base current, 100% positive feedback has been realized and a reset is required to restore normal operation once the short is removed.

In *Figures 8-22a* and *b,* the input to the current limit transistor is ($V_{RSC} + V_{R2}$), leading to

$$I_{SC} = \frac{V_{SENSE}}{R_{SC}}\left(\frac{R1 + R2}{R1}\right) - \frac{V_{IN}}{R_{SC}}\left(\frac{R2}{R1}\right) \text{ and}$$

$$I_M = I_{SC} + \frac{V_O}{R_{SC}}\left(\frac{R2}{R1}\right)$$

Design equations to give a desired I_M with approximately zero I_{SC} are

$R1\ (k\Omega) = V_{IN} - V_{SENSE}\ (V)$

$R2\ (k\Omega) = V_{SENSE}\ (V)$ (i.e. R2 = 620 Ω)

$$\text{and } R_{SC} = \frac{V_O}{I_M}\left(\frac{R2}{R1}\right), \text{ or } R_{SC} = \frac{V_O}{I_M}\left(\frac{V_{SENSE}}{V_{IN} - V_{SENSE}}\right)$$

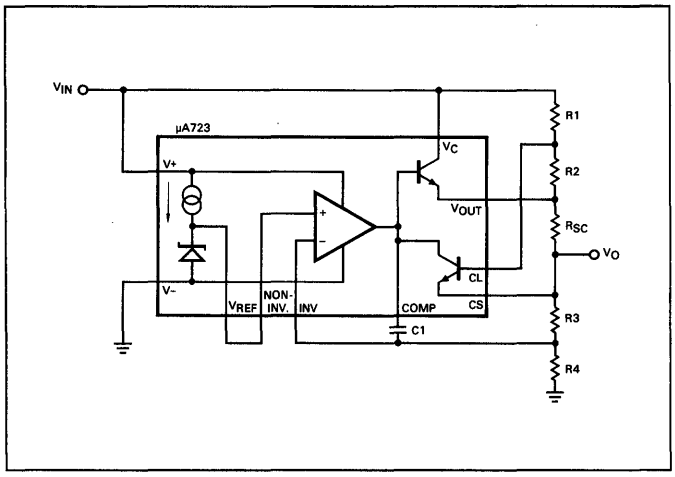


Fig. 8-22a Foldback Current Limiting Positive Regulator

In *Figure 8-22b* it is recommended to use a Darlington configuration for the bypass transistors, Q1 and Q2. This enables R5 to be a relatively high value, typically >50 K, which requires Q3 to sink a low current under short circuit conditions.

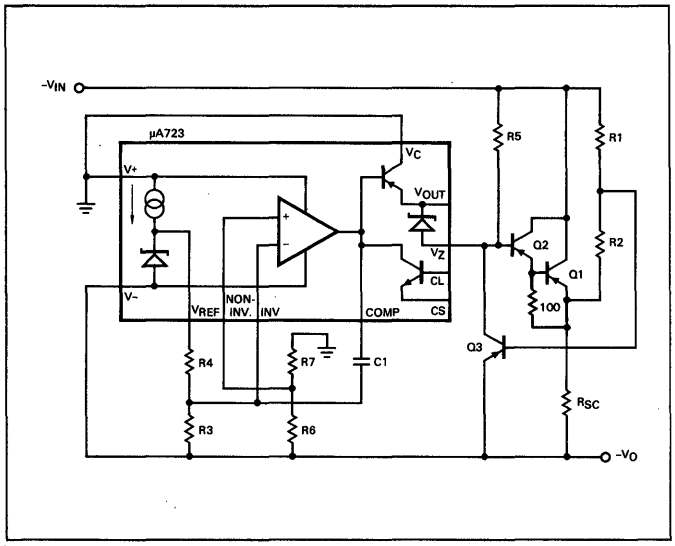


Fig. 8-22b Foldback Current Limiting Negative Regulator

As R5 is reduced the current through it increases drastically when $-V_O$ goes to zero volts, and Q3 base current increases to a point where the foldback circuit is no longer operative.

From the start of base emitter conduction of the sense transistor to the full shut off of the power supply's series pass devices requires a 2 µA base current. This represents a 10 mV increase in base emitter voltage over the base emitter zero current threshold.

The latch condition, or 100% positive feedback, is generated by any change in the input voltage which increases the voltage drop across R2 past the 10 mV window with a short circuit applied, and can only be removed by breaking the positive feedback path by some manual reset to allow the series pass devices to once more be driven in a normal fashion.

The addition of an external transistor Q1 in *Figure 8-22c* provides the same foldback limiting as *Figure 8-22a* but allows the extension of the active recovery region by several times that of the basic approach.

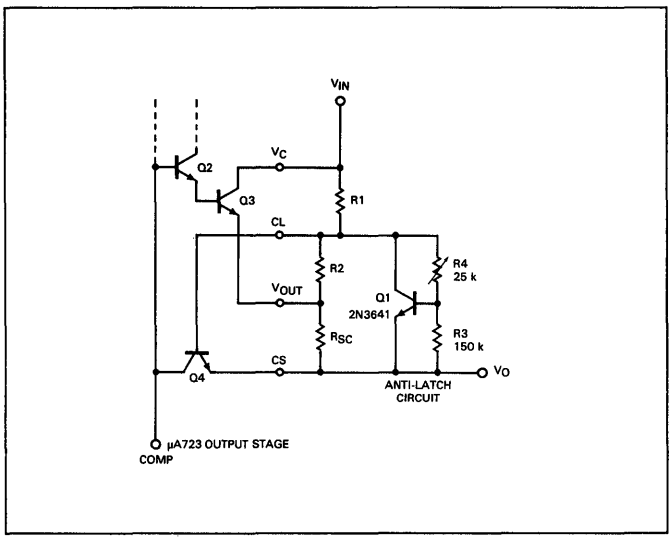


Fig. 8-22c Foldback Current Limiting (Modified)

Latch problems are due to saturation of the current sensing transistor. Because the additional circuitry shown operates as an antisaturation circuit, it bypasses base current above a value set by the voltage divider R3, R4 and the base emitter threshold of Q1. This additional transistor acts as a V_{BE} voltage regulator and, assuming a good thermal link, temperature tracks the threshold changes of the current sensing transistor, tending to keep the foldback current drive at a constant level.

Foldback resistors R1 and R2 are calculated using the equation of *Figure 8-22a*. The 2N3641 used for Q1 was selected for both high base emitter diode conductivity and reasonable Beta at 2 µA collector current.

Final adjustment under short circuit conditions occurs when R4 in *Figure 8-22c* is set just above the point of minimum output current under short circuit load and high ac line operation.

An alternate method of providing foldback current limiting is illustrated in *Figures 8-22d* and *8-22e*. Here, the base of the current limit transistor is fed from a potential divider from V_{OUT} to ground. The input to this transistor now equals ($V_{RSC} - V_{R3}$), which leads to:

$$I_{SC} = \frac{V_{SENSE}}{R_{SC}}\left(\frac{R3 + R4}{R4}\right) \text{ and } I_M = I_{SC} + \frac{V_O}{R_{SC}}\left(\frac{R3}{R4}\right)$$

To determine the resistor values required to give a short circuit current I_{SC} and a maximum output current of I_M, first determine the ratio of R3 to (R3 + R4):

$$\frac{R3}{(R3+R4)} = \alpha = \left(\frac{I_M}{I_{SC}} - 1\right) \frac{V_{SENSE}}{V_O}$$

Now set R4 (kΩ) equal to V_O (V), then

$$R3 = \left(\frac{\alpha}{1-\alpha}\right) R4 \text{ and } R_{SC} = \frac{V_{SENSE}}{I_{SC}} \left(\frac{1}{1-\alpha}\right)$$

Obviously, α must lie between zero (R3 ⟶ short circuit) and unity (when R4 ⟶ short circuit). This controls the range of the ratio I_M/I_{SC} such that its upper limit is approximately 1.5 x V_O. For a 5 V regulator, for instance, maximum value for I_M/I_{SC} is about 7.5; for a 12 V regulator it is about 18. This indicates that there is a restriction on obtaining very low short circuit currents with the figures of *8-22d* and *8-22e*. By contrast, note that *Figures 8-22a* and *b* are designed to give approximately zero short circuit current.

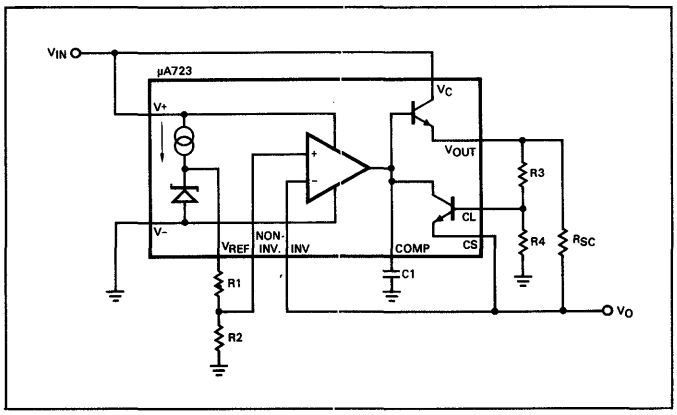


Fig. 8-22d Foldback Current Limiting Positive Regulator (Alternate Method)

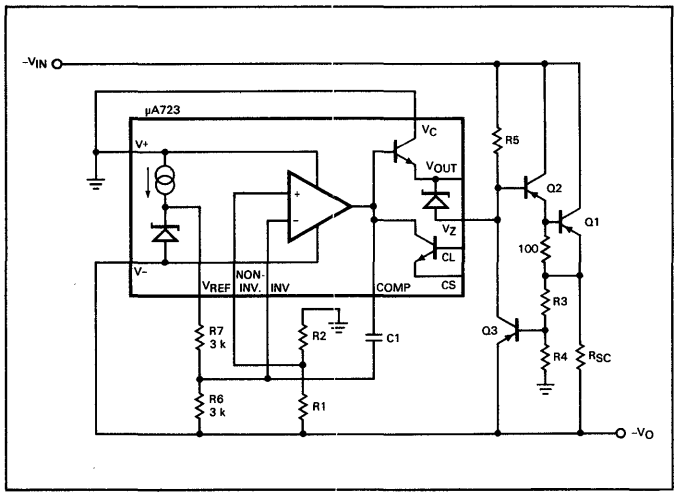


Fig. 8-22e Foldback Current Limiting Negative Regulator (Alternate Method)

Another approach to low power dissipation under short circuit condition is shown in *Figure 8-22f*. This circuit does not follow the decreasing current, decreasing voltage load line which occurs with the standard foldback technique. Instead, under a short circuit, the output voltage decreases in a normal current limiting fashion, i.e., at a constant high output current until the output voltage is below that necessary to keep the FET pinched off. As soon as the output voltage reaches the pinch off voltage, a low impedance path is established around the drivers and the output device, which turns off the compound followers.

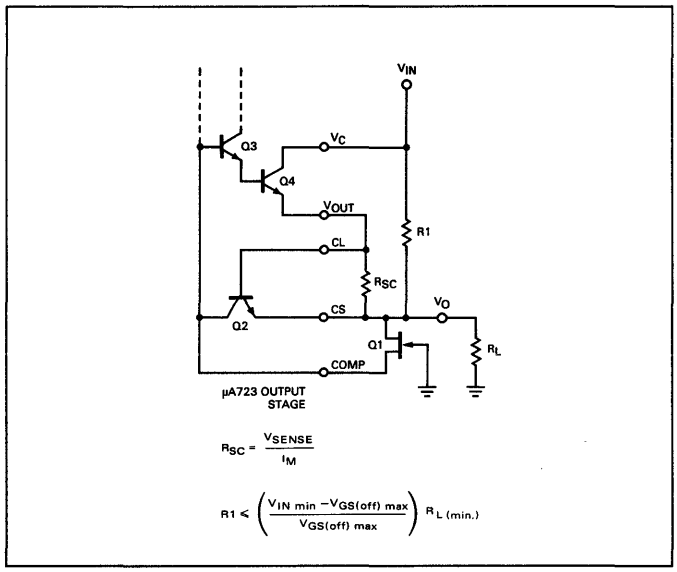


Fig. 8-22f Foldback Current Limiting (FET)

A voltage across the normal load resistor exceeding the pinch off voltage of the FET whenever the short is removed, provides recovery. Bypass resistor R1 supplies this voltage.

The FET should be selected with a maximum pinch off voltage approximately two-thirds the value of V_O. Its minimum pinch off voltage should not be so low as to demand excessive safe area requirements in the μA723 output stage.

Short Circuit Sensing, Low Loss

In high current power supplies, the 0.5 V necessary to sense the current limit point leads to a considerable power loss. In *Figure 8-23* a higher overall power supply efficiency is achieved by requiring a much lower sense voltage. The current limit point is determined by the portion of the μA777s output swing applied as positive feedback, which in turn is determined by the ratio between R1 and R2. In the example shown, the ratio is 1000-to-1. The voltage swing at the output is approximately 13 V, so the sense voltage threshold is 13 mV. When this threshold is exceeded by a voltage developed across R_{SC}, the current sense resistor, the μA777 is driven from its reset state (output high) to its active state (output low), this, in turn, shuts off the power supply by pulling the compensation terminal toward ground. The reset button restores normal operation.

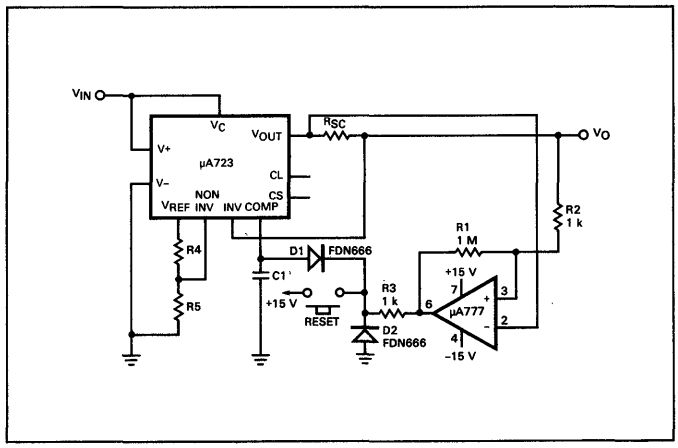


Fig. 8-23 Low Loss Short Circuit Sensing

Short Circuit Sensing, Temperature Stabilized

This circuit modification takes advantage of the internal temperature tracking which occurs in an integrated circuit. Since the current limit transistor and the internal series pass devices are at the same temperature and were fabricated at the same time, their base emitter temperature coefficients will be approximately the same. In *Figure 8-24* the current limit transistor is connected in a manner such that the temperature coefficients cancel. This is accomplished with a bridge circuit via resistors R4 and R5 which reduce the voltage drop (and therefore the temperature coefficient) to a 1 diode drop level. This voltage, appearing across R4, is balanced by an equal and opposite voltage developed across R3 by a FET current source. The current limit transistor is connected across these two voltages, plus the voltage across R_{SC} due to the output current. At room temperature the current source is adjusted by P2 such that there is zero voltage between points A and B. Therefore, at room temperature, the current limit transistor is activated when the μA723 sense voltage is developed across R_{SC}, the voltages across R3 and R4 cancelling each other.

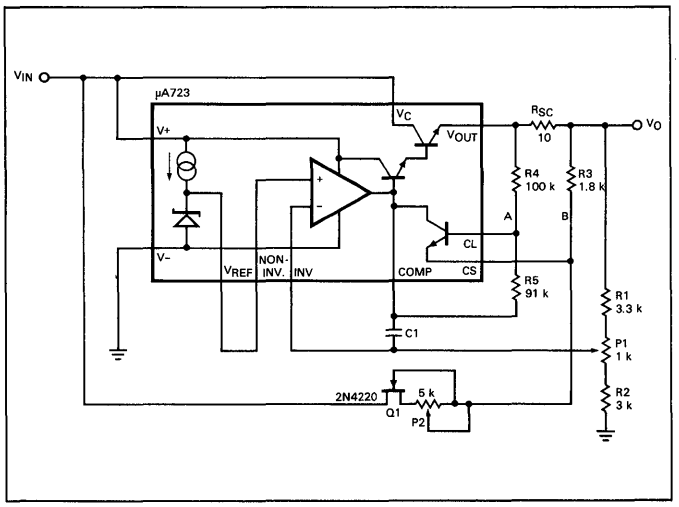


Fig. 8-24 Temperature Stabilized Short Circuit Sensing

The threshold of the current limit transistor will tend to track the voltage across R4 with temperature. Therefore, providing the current source remains constant with temperature, current limit set by R_{SC} also remains constant with temperature.

Figure 8-24 is shown for an output voltage of 15 V from a 25 V unregulated input. A higher breakdown FET will be required for use with higher input voltages.

Remote Shutdown

A μA723 regulator may be turned off by pulling down the compensation terminal, thereby shunting the drive current for the output stage to ground. The simplest method of achieving this in a positive regulator is shown in *Figure 8-25a*. When the current limiting function is required, an external transistor may be substituted (Q1 in *Figure 8-25b).* The logic input may be from any positive voltage source, e.g., TTL or CMOS, capable of driving greater than 100 uA into the CL terminal or Q1 base. Typically, R3 may be 3.0 kΩ from a 5 V TTL system, or 10 kΩ from a 10 V CMOS system.

To protect the output stage from excessive reverse base emitter voltage transients during the shutdown, D1 should be included when the output voltage V_O is greater than 10 V. R4 reduces the peak current that flows when Q1 saturates.

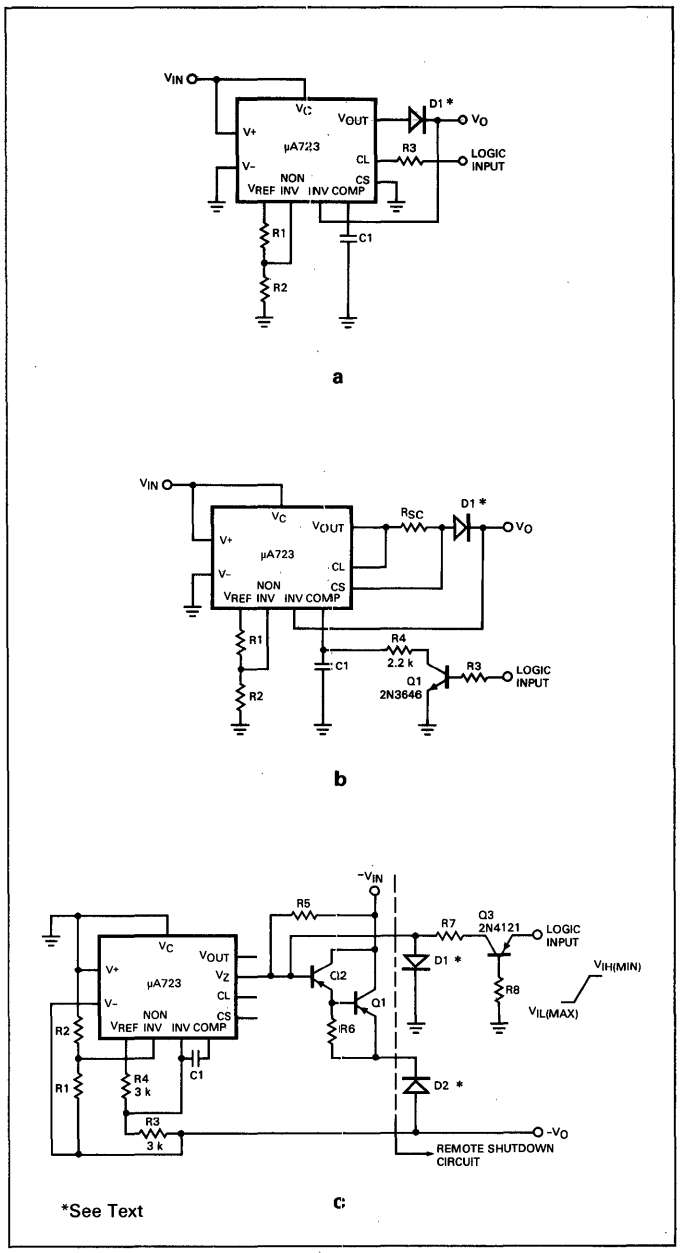


Fig. 8-25 Remote Shutdown

Remote shutdown, when applied to a negative regulator, requires the additional circuitry to the right of the dashed line in *Figure 8-25c*. In operation, a logic Low input, $V_{IL(max)}$, will hold Q3 off, disabling the shutdown circuit. A logic High input, $V_{IH(min)}$, from a TTL or CMOS gate turns Q3 on with the base drive limited by R8. Resistor R5 is calculated in the normal worst case manner for the series pass devices selected.

$$R5 = \frac{(V_{IN(min)} - V_O - 2V_{BE}^*)}{Q2I_{B(max)}}$$

*(This term becomes $3V_{BE}$ is D2 is included.)

When Q3 is turned on, D1 is forward biased at a current limited by R7. The ratio of R5 and R7 is calculated such that the output of the supply is always at ground when the logic input is High.

$$\frac{R7}{R5} = \frac{V_{IH(min)}}{V_{IN(max)}},$$

The formula shown guarantees that the junction of R5 and R7 is always positive during shutdown — R8 = 10 R7, to give a forced β of 10 for Q3, fully saturating that device. Diode D2

protects the output devices from reverse base emitter transient voltages, and should be included when the output voltage is greater than the combined base emitter breakdown voltages of the series pass devices.

Overvoltage Crowbar Protection

Figure 8-26 shows a µA723 used as a latched comparator and SCR driver. It also provides the temperature compensated reference necessary for accurate overvoltage sensing. In normal operation, P1 is adjusted so that the voltage at point A is more negative than the reference voltage, V_{REF} (typically 7.15 V). Therefore, the voltage across R2 will bias the comparator (the µA723 error amplifier) such that its output, V_{OUT} is driven toward V–, and the internal 6.2 V Zener diode is cut off. Hence no gate current is able to flow into the SCR D2, which remains in an OFF state. Diode D1 blocks the positive feedback path in this condition, therefore, no current flows through R4.

By "crowbar" action, the comparator changes its state as soon as the voltage across R2 reverses polarity, that is, as soon as the voltage at point A becomes more positive than V_{REF}. Potentiometer P1 is set so that this occurs at the desired overvoltage trip point, typically (V_O + 10%). When the comparator switches, V_{OUT} is pulled up toward V+, and the SCR is fired with gate current limited by R5. When V_{OUT} exceeds V_{REF} the positive feedback loop R4/D1 latches the comparator into its switched state.

The action of firing the SCR places a low impedance across the unregulated supply to ground, and this blows fuse F1. From the initial overvoltage to the SCR clamping takes approximately 1 µs; if required the switching action may be made slower by a capacitor from the µA723 COMP terminal to the inverting input.

Over/Under Voltage Monitoring

There are many systems where it is important that, when the regulated supply lines deviate from their nominal values, an alarm is indicated and some action, such as system shutdown or system changeover, is initiated. Such a fault detection system requires overvoltage and undervoltage monitors for both positive and negative power supplies. The µA723 may be used very effectively in this application and provides a TTL-compatible output signal.

Figure 8-27a gives an indication of an undervoltage on a positive supply line. The internal reference voltage of the µA723, V_{REF}, is used to generate a threshold voltage of 2.0 V across R4. The voltage to be monitored, V_M, is divided down by R_M and R1. The voltage across R1 is compared to the threshold voltage across R4 by the µA723 error amplifier. When V_M is at its nominal value, the output of the µA723 is in its high state, which is set at approximately 3.3 V by clamping the COMP terminal to the junction of R2 and R3 on the V_{REF} voltage divider. Current drain from V_{OUT} through R6 is nominally 15 mA.

If the monitored supply, V_M, should fall by a predetermined amount, the error amplifier changes state, and the output voltage V_O assumes its low state. R6 is able to drive one TTL load (1.6 mA at 0.4 V_{max} V_O). Positive switching action is assured by the hysteresis applied through R5. R_M is adjusted so that the voltage across R1 equals the threshold voltage (2.0 V) when V_M is at the desired undervoltage trip level.

This circuit will give an overvoltage indication on a positive supply line by interchanging the amplifier inputs as shown by the dashed lines.

Figure 8-27b performs the same functions for a negative supply line. The monitored supply voltage, $-V_M$, is referenced to V_{REF} in this circuit, to provide the level shifting from any negative input to the +2.0 V threshold voltage.

Response times for these monitor circuits are typically less than 1 µs.

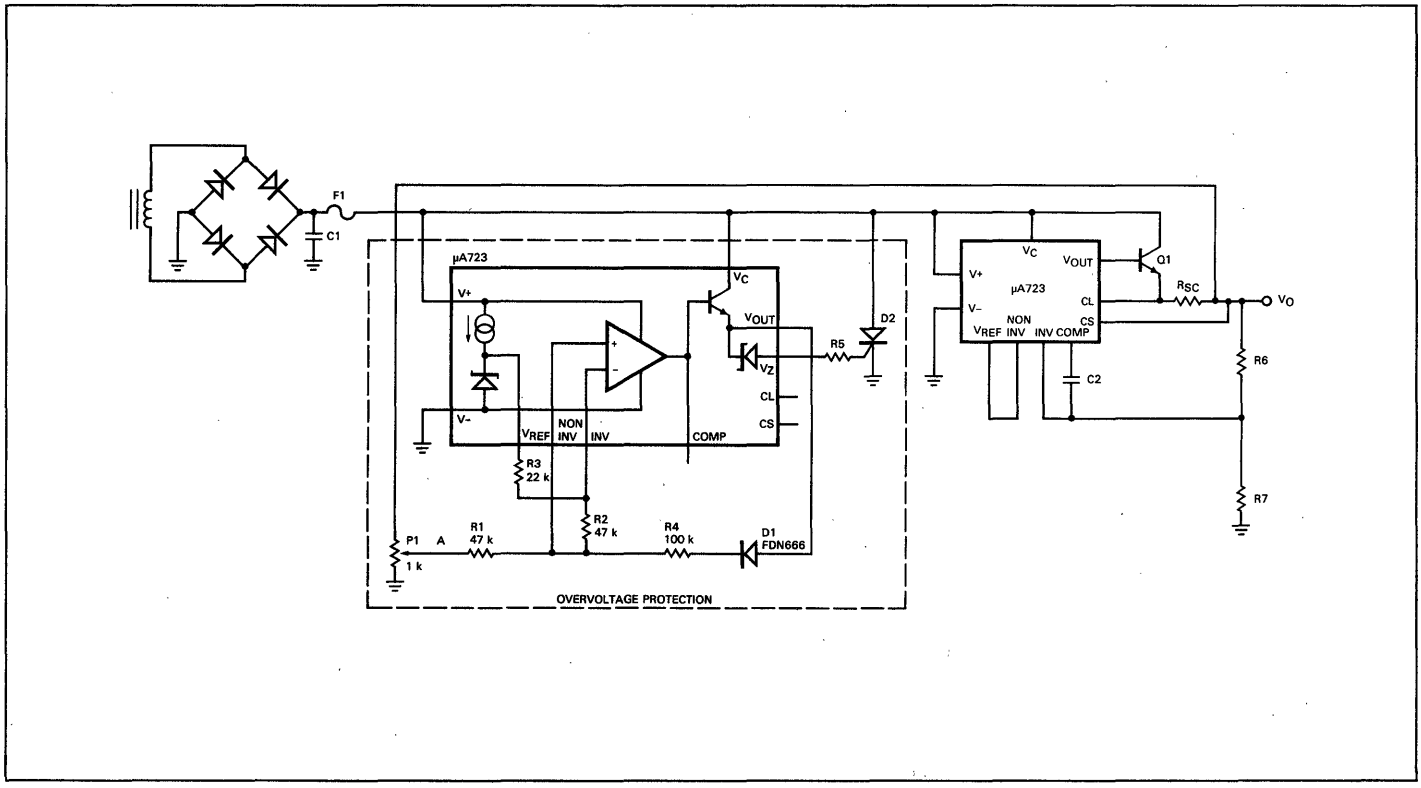


Fig. 8-26 Crowbar Protection

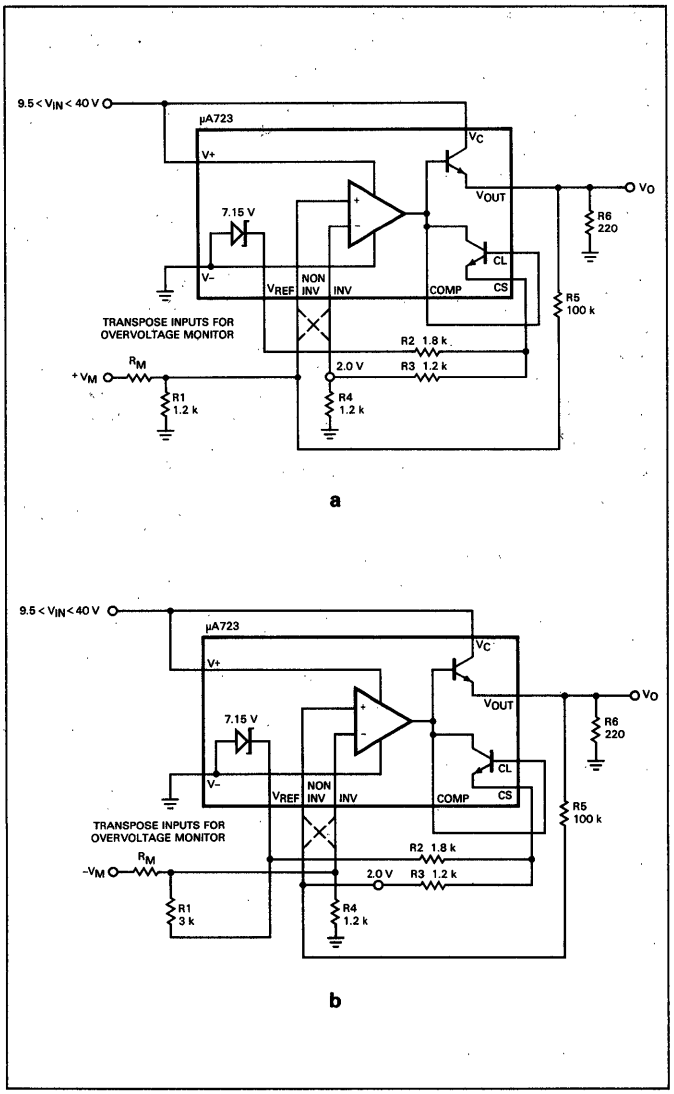


Fig. 8-27 Positive/Negative Supply Undervoltage Monitors

Switching Regulators

Figure 8-28a is a *positive* switching regulator; *Figure 8-28b* is a *negative* output version. The principles of operation of switching regulators and design equations are given in Appendix A.

Referring to *Figure 8-28a* and *Figure 8-28b,*

$$V_O = \left(\frac{R2}{R1+R2}\right)V_{REF}, \quad \text{and} \quad -V_O = -\left(\frac{R1+R2}{R1}\right)\frac{V_{REF}}{2}$$

Other gain setting configurations may be used, such as those used in the linear regulators to extend the output voltage range. R6 *(Figure 8-28a)* limits the base drive to Q2 to approximately 10 mA by using the internal current limit transistor in the μA723.

The efficiency of these circuits is typically 75% at 1 A output current, and 73% at 2 A output current. If the V_Z terminal is not available *(Figure 8-28b),* a 6.2 V Zener diode can be used in series with V_{OUT}. As in the linear negative voltage regulators, the minimum output voltage using this configuration is -9.5 V. Voltages between -2 V and -9.5 V are obtained by supplying a positive voltage to the V+ and V_C terminals such that the range of voltage applied between the V- and V+ terminals is between 9.5 V and 40 V. Values for R4, L1 and C1 are calculated from design information given in Appendix A.

One method of providing short circuit protection for the positive switching regulator is shown in *Figure 8-28c,* a modification of *Figure 8-28a.* The internal current limiting transistor is used to sense the voltage across R_{SC} in the same manner as linear regulators. For output voltages above 5 V, D2 and D3 should be added to protect the error amplifier input stage from excessive voltages during output short circuit conditions.

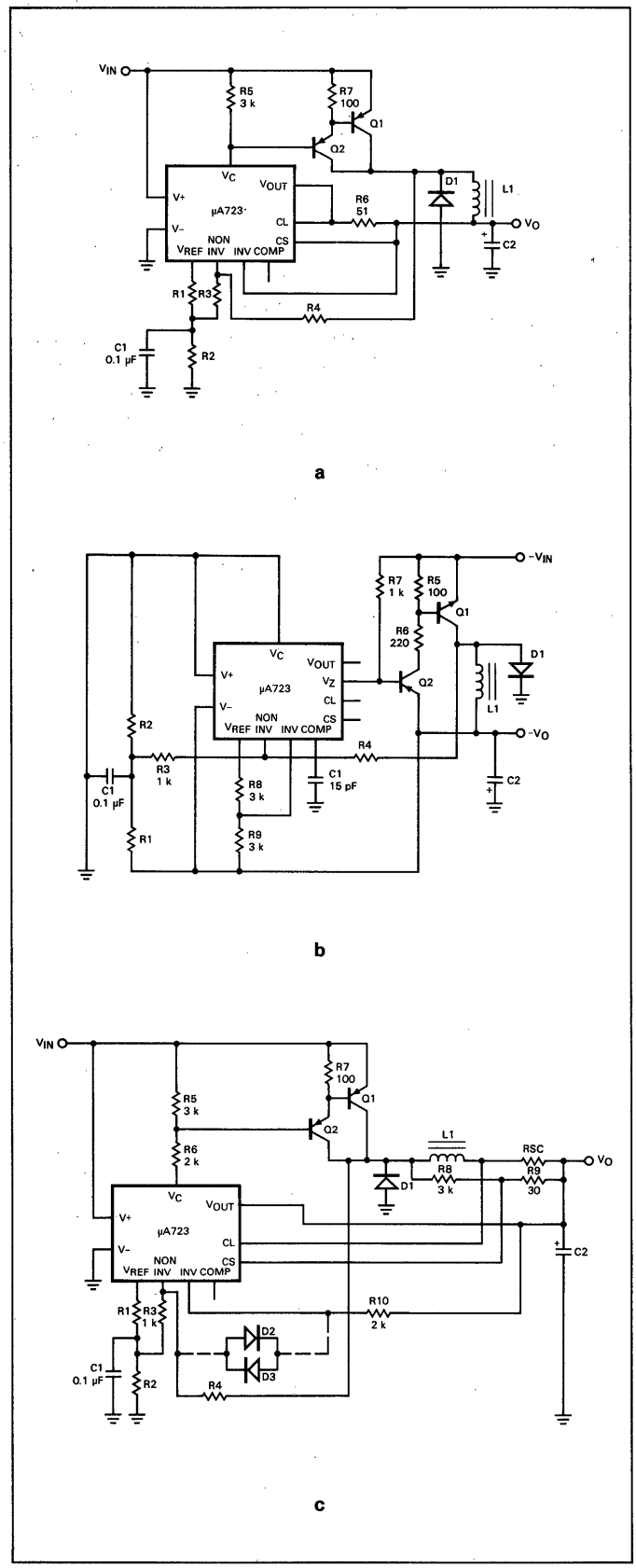


Fig. 8-28 Switching Regulators

The voltage necessary to turn on the current limiting transistor is the sum of V_{SENSE} (the V_{BE} of the current limiting transistor) and the voltage across R9. Then, as shown in the formula below,

$$V_{RSC} = V_{SENSE} + (V_{IN} - V_O)\left(\frac{R9}{R8 + R9}\right), \text{ and}$$

$$I_{LIMIT} = \left(\frac{V_{SENSE}}{R_{SC}}\right) + \frac{(V_{IN} - V_O)}{R_{SC}}\left(\frac{R9}{R8 + R9}\right)$$

R8 and R9 are included to supply positive feedback and, hence, maintain switching action even under short circuit conditions. This prevents over-dissipation if the regulator were allowed to go into a linear mode. Typically, R8 may be 3 kΩ and R9 30Ω so that to a first approximation, current limit is derived as follows:

$$I_{LIMIT} = \left(\frac{V_{SENSE}}{R_{SC}}\right) + \frac{(V_{IN} - V_O)}{100\ R_{SC}}$$

OUTPUT VOLTAGE	APPLICABLE CIRCUITS	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10%			OUTPUT VOLTAGE	APPLICABLE CIRCUITS	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10%		
	(Note 1)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
3.0	8-8 a,b (8-9a)8-9b	4.12	3.01	1.8	0.5	1.2	100	8-13 8-21	3.57	102	2.2	10	91
3.6	8-10	3.57	3.65	1.5	0.5	1.5	250		3.57	255	2.2	10	240
5.0	8-11b (8-12)	2.15	4.99	.75	0.5	2.2	−6 (Note 2)		3.57	2.43	1.2	0.5	.75
6.0	8-15 8-28a	1.15	6.04	0.5	0.5	2.7	−9	8-16	3.48	5.36	1.2	0.5	2.0
9.0	8-8c	1.87	7.15	.75	1.0	2.7	−12	8-17 8-18	3.57	8.45	1.2	0.5	3.3
12	8-9a(8-9b) (8-10)	4.87	7.15	2.0	1.0	3.0	−15	8-28b	3.65	11.5	1.2	0.5	4.3
15	8-11a 8-12 (8-28a)	7.87	7.15	3.3	1.0	3.0	−28		3.57	24.3	1.2	0.5	10
28		21.0	7.15	5.6	1.0	2.0	−45		3.57	41.2	2.2	10	33
45	8-13 8-21	3.57	48.7	2.2	10	39	−100	8-19	3.57	97.6	2.2	10	91
75		3.57	78.7	2.2	10	68	−250		3.57	249	2.2	10	240

NOTES:
1. Circuits in parenthesis may be used if R1/R2 divider is placed on opposite side of error amplifier.
2. V^+ must be connected to a +3.5 V or greater supply.

Table 8-1 Resistor Values for Standard Output Voltages

LINEAR

CONTENTS AND SECTION SELECTOR

IN THIS CHAPTER:

- INTRODUCTION
- 104 FAMILY
- TYPICAL PERFORMANCE CURVES
- ELECTRICAL CHARACTERISTICS
- PACKAGING AND CONNECTION DIAGRAM
- BASIC APPLICATIONS
- 105 FAMILY
- TYPICAL PERFORMANCE CURVES
- ELECTRICAL CHARACTERISTICS
- PACKAGING AND CONNECTION DIAGRAM
- 109 FAMILY
- TYPICAL PERFORMANCE CURVES
- ELECTRICAL CHARACTERISTICS
- PACKAGING AND CONNECTION DIAGRAM

CHAPTER 9
104, 105 and 109 Voltage Regulators

INTRODUCTION

In addition to the proprietary regulators described in previous sections, Fairchild also second sources a number of other popular regulator lines, the 104, 105 and 109 families. The 104 family devices are adjustable negative regulators, the 105 family devices are adjustable positive regulators. Both have excellent regulation characteristics but limited output current capability. The 376 regulator, based on the 105 series, is presently the only regulator available in the mini-DIP package. The 109 family is specifically for 5 V logic power supplies, and its electrical characteristics have been designed to complement the requirements of the DTL and TTL logic series. Devices in the 109 regulator family are fully protected against usual power supply failure modes. They have internal current limiting, thermal shutdown, and safe area compensation. Condensed specifications, typical performance curves, and basic applications information are as follows.

104 FAMILY

Devices in the 104 family of voltage regulators may be programmed by a single external resistor to supply any voltage from 0 V to -30 V from a single, negative unregulated supply. The basic regulator can supply up to 25 mA output current, which may be increased by the addition of external bypass transistors. Other applications include switching regulators and a floating regulator, requiring a separate bias supply, which provides 0.01% regulation at output voltages limited only by the breakdown of the external bypass device.

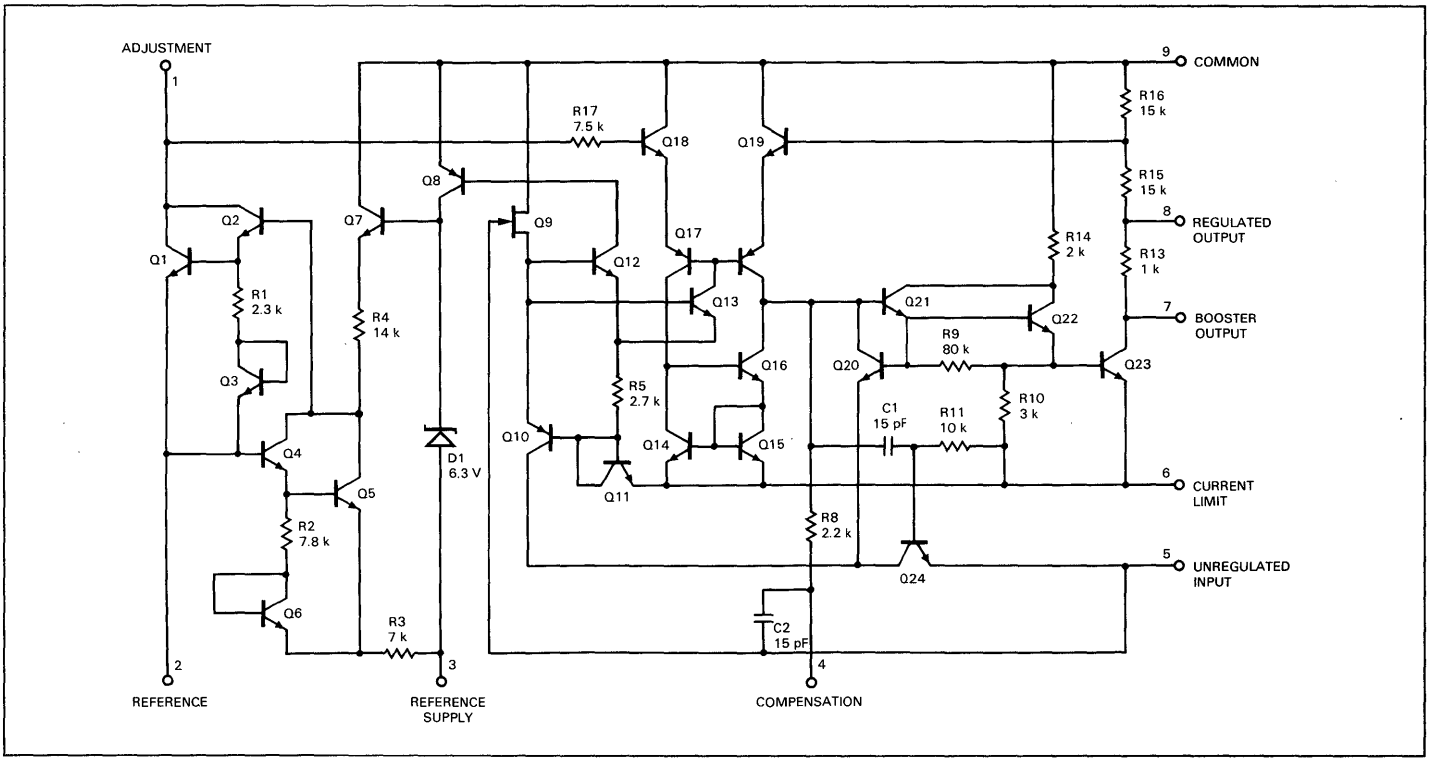


Fig. 9-1 Equivalent Circuit of the 104 Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
104	-50 V
304	-40 V
Input/Output Voltage Differential	
104	-50 V
304	-40 V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military grade (104)	-55°C to +125°C
Commercial grade (304)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

See page 9-6 for notes.

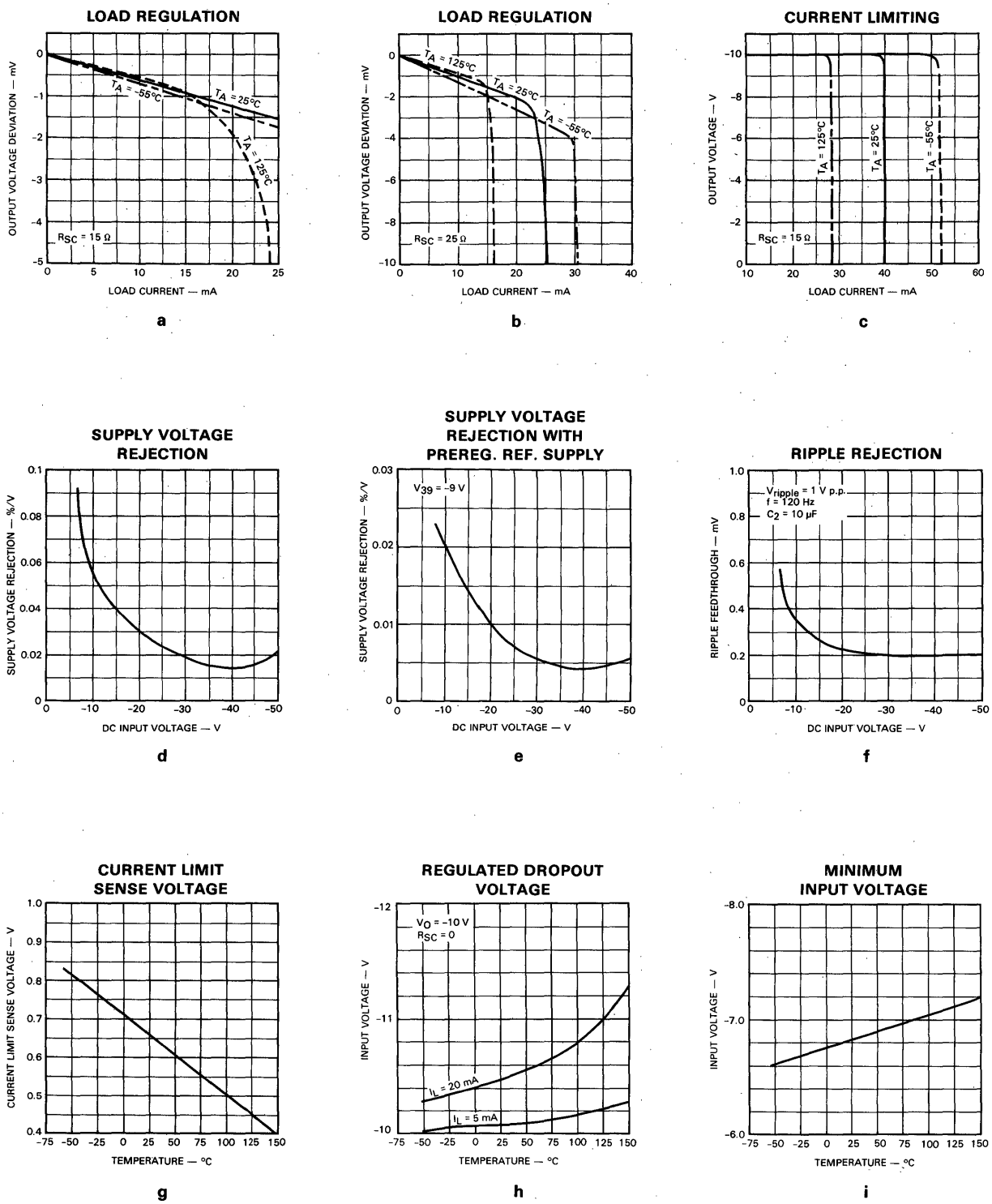


Fig. 9-2 Typical Performance Curves for 104

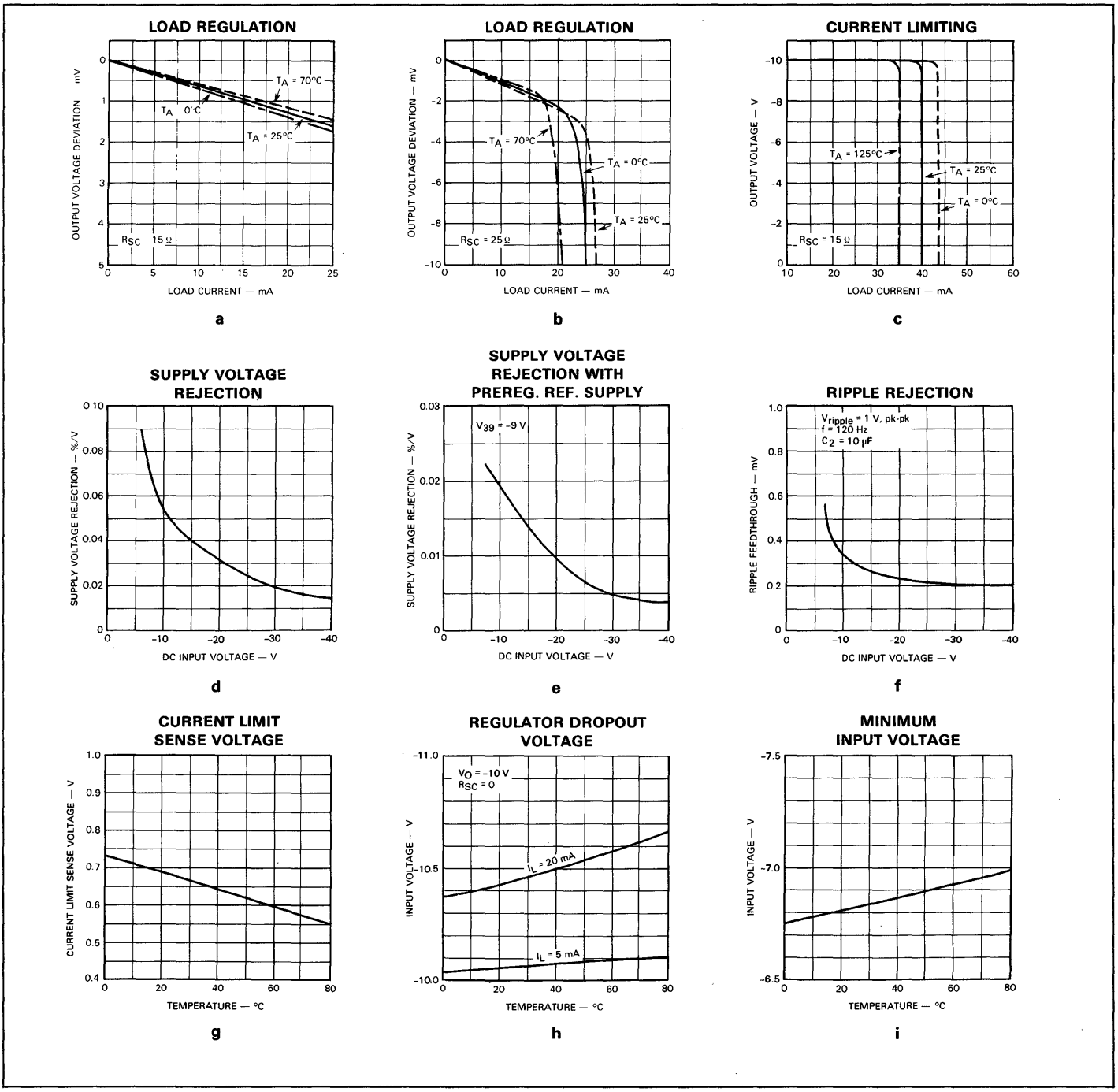


Fig. 9-3 Typical Performance Curves for 304

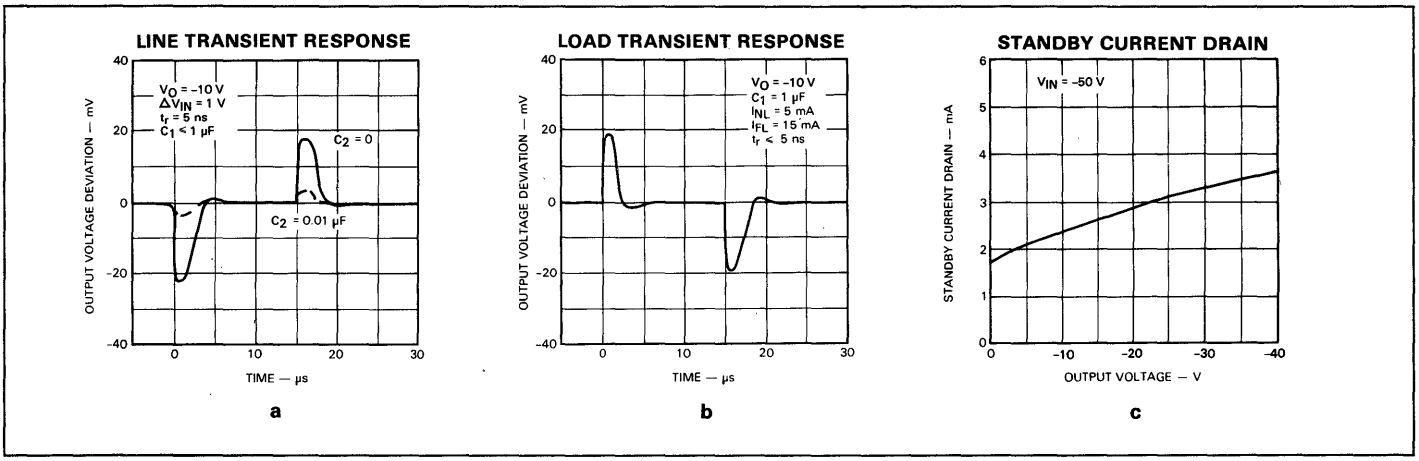


Fig. 9-4 Typical Performance Curves for 104 & 304

104

ELECTRICAL CHARACTERISTICS (V_{IN} = −50 V to −8.0 V, T_A = −55°C to 125°C, unless otherwise specified), Note 2. See Figure 9-6

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			−50		−8.0	V
Output Voltage Range			−40		−0.015	V
Output/Input Voltage Differential (Note 3)	I_L = 20 mA		2.0		50	V
	I_L = 5 mA		0.5		50	V
Load Regulation (Note 4)	$0 \leq I_L \leq 20$ mA, R_{SC} = 15 Ω			1.0	5.0	mV
Line Regulation (Note 5)	$V_O \leq -5$ V, $\Delta V_{IN} = 0.1\ V_{IN}$			0.056	0.1	%
Ripple Rejection	C_2 = 10 μF, f = 120 Hz,	$V_{IN} \geq -15$ V		0.2	0.5	mV/V
		$-7\ V \geq V_{IN} \geq -15$ V		0.5	1.0	mV/V
Output Voltage Scale Factor V_O/R_2	R1 = 2.4 kΩ		1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_O \leq -1$ V, $-55°C \leq T_A \leq 125°C$			0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, $V_O \leq -5$ V,	C2 = 0		0.007		%
		C2 = 10 μF		15		μV
Standby Current Drain	I_L = 5 mA	V_O = 0		1.7	2.5	mA
		V_O = −40 V		3.6	5.0	mA
Long Term Stability	$V_O \leq -1$ V			0.1	1.0	%

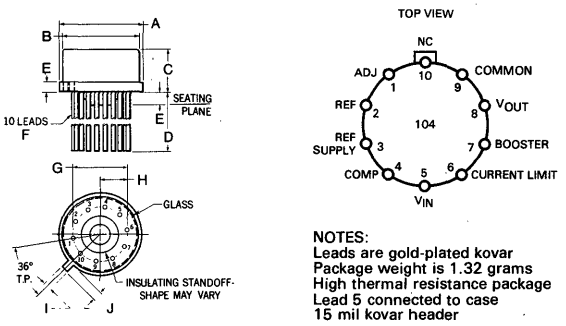
304

ELECTRICAL CHARACTERISTICS (V_{IN} = −40 V to −8.0 V, T_A = 0°C to 70°C, unless otherwise specified), Note 2. See Figure 9-6

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			−40		−8.0	V
Output Voltage Range			−30		−0.035	V
Output/Input Voltage Differential (Note 3)	I_L = 20 mA		2.0		40	V
	I_L = 5 mA		0.5		40	V
Load Regulation (Note 4)	$0 \leq I_L \leq 20$ mA, R_{SC} = 15 Ω			1.0	5.0	mV
Line Regulation (Note 5)	$V_O \leq -5$ V, $\Delta V_{IN} = 0.1\ V_{IN}$			0.056	0.1	%
Ripple Rejection	C2 = 10 μF, f = 120 Hz,	$V_{IN} < -15$ V		0.2	0.5	mV/V
		$-7\ V \geq V_{IN} \geq -15$ V		0.5	1.0	mV/V
Output Voltage Scale Factor $V_O/R2$	R1 = 2.4 kΩ		1.8	2.0	2.2	V/kΩ
Temperature Stability	$V_O \leq -1$ V, $0°C \leq T_A \leq 70°C$			0.3	1.0	%
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, $V_O \leq -5$ V,	C2 = 0		0.007		%
		C2 = 10 μF		15		μV
Standby Current Drain	I_L = 5 mA	V_O = 0		1.7	2.5	mA
		V_O = −30 V		3.6	5.0	mA
Long Term Stability	$V_O \leq -1$ V			0.1	1.0	%

NOTES:

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. When external booster transistors are used, the minimum output-input voltage differential is increased, in the worst case, by approximately 1 V.
4. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
5. With zero output, the dc line regulation is determined from the ripple rejection. Hence, with output voltages between 0 V and −5V, a dc output variation, determined from the ripple rejection, must be added to find the worst-case line regulation.



NOTES:
Leads are gold-plated kovar
Package weight is 1.32 grams
High thermal resistance package
Lead 5 connected to case
15 mil kovar header

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.335		0.370	8.51		9.40
B	0.305		0.335	7.75		8.51
C	0.165		0.185	4.19		4.70
D	0.500			12.70		
E			0.040			1.02
F	0.016		0.019	0.41		0.48
G		0.230			5.84	
H		0.115			2.92	
I	0.028		0.034	0.71		0.86
J	0.029		0.045	0.74		1.14

Fig. 9-5 Connection Diagram and Package Outline (TO-100 Package)

Basic Regulator Application (Figure 9-6)

The output voltage is proportional to R2; the exact scale factor may be set by adjusting R1. Short circuit current is set by the following equation

$$I_{SC} = \frac{V_{SENSE}}{R_{SC}}$$

C1 should be at least 1 µF, preferably solid tantalum, to prevent oscillations. A 0.01 µF capacitor may be required across the input if long leads are used from the unregulated power source. Line transient response, noise and ripple rejection may be improved by shunting R2 with a 10 µF capacitor C2, as indicated in the performance curves.

High Current Regulator

Figure 9-7 illustrates the use of external bypass transistors in the construction of a 2 A, 10 V power supply.

Floating Regulator

If V_{BIAS} in *Figure 9-8* is a pre-regulated floating supply, 0.01% regulation may be achieved with this circuit. Since terminals 8 and 9 are shorted in this application, the feedback factor of one-half ($\frac{R16}{R15+R16}$ *Figure 9-1*) no longer applies and the output voltage scale factor changes to V_O (V) = R2 (k Ω).

Switching Regulator

Figure 9-9 shows a -5 V switching regulator for output currents up to 3 A. C2 is added to reduce the transients that appear across R2 which might cause erratic switching.

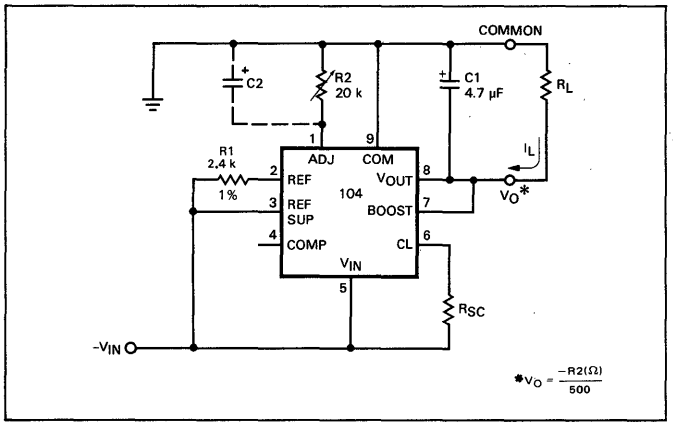


Fig. 9-6 Basic Application

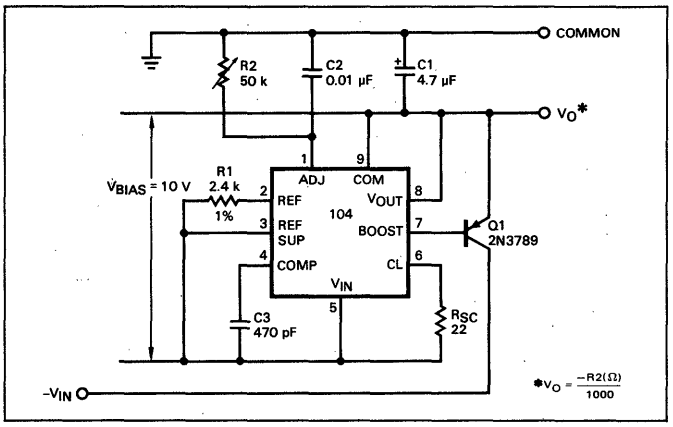


Fig. 9-8 Floating Regulator

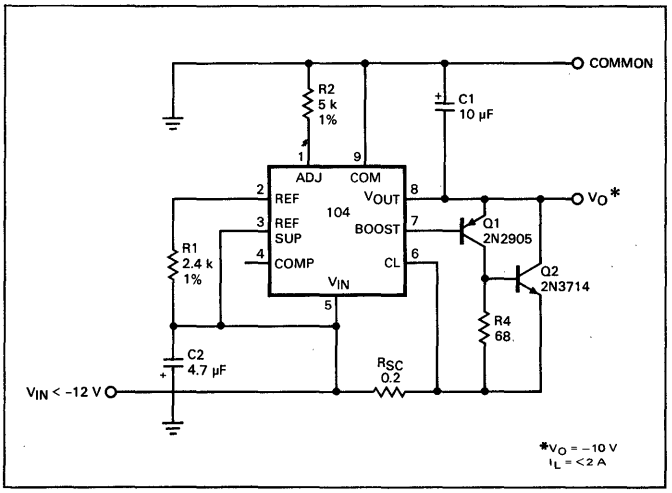


Fig. 9-7 High Current Regulator

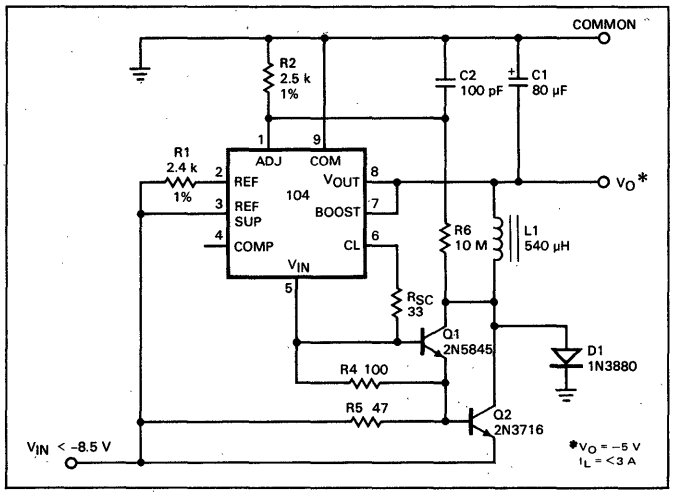


Fig. 9-9 Switching Regulator

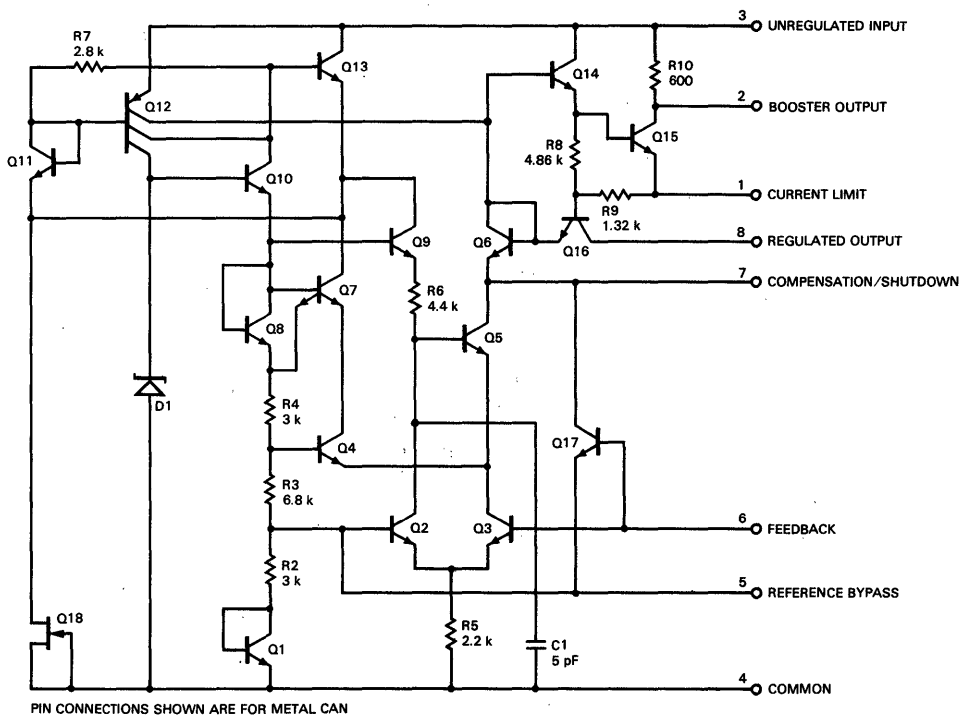


Fig. 9-10 Equivalent Circuit Of The 105 Voltage Regulator

105 FAMILY

The 105, 305, and 305A adjustable voltage regulators supply up to 45 mA at output voltages of 4.5 to 40 V (30 V for the 305). The 376, packaged in an 8-lead mini-DIP, supplies a maximum of 25 mA.

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
105, 305A	50 V
305, 376	40 V
Input/Output Voltage Differential	40 V
Internal Power Dissipation (Note 1)	
105, 305, 305A	500 mW
376	450 mW
Operating Temperature Range	
Military (105)	−55°C to +125°C
Commercial (305, 305A, 376)	0°C to +70°C
Storage Temperature Range	
Metal Can	−65°C to +150°C
Mini DIP	−55°C to +125°C
Lead Temperature	
Metal Can (Soldering, 60 seconds)	300°C
Mini DIP (Soldering, 10 seconds)	260°C

See page 9-11 for notes.

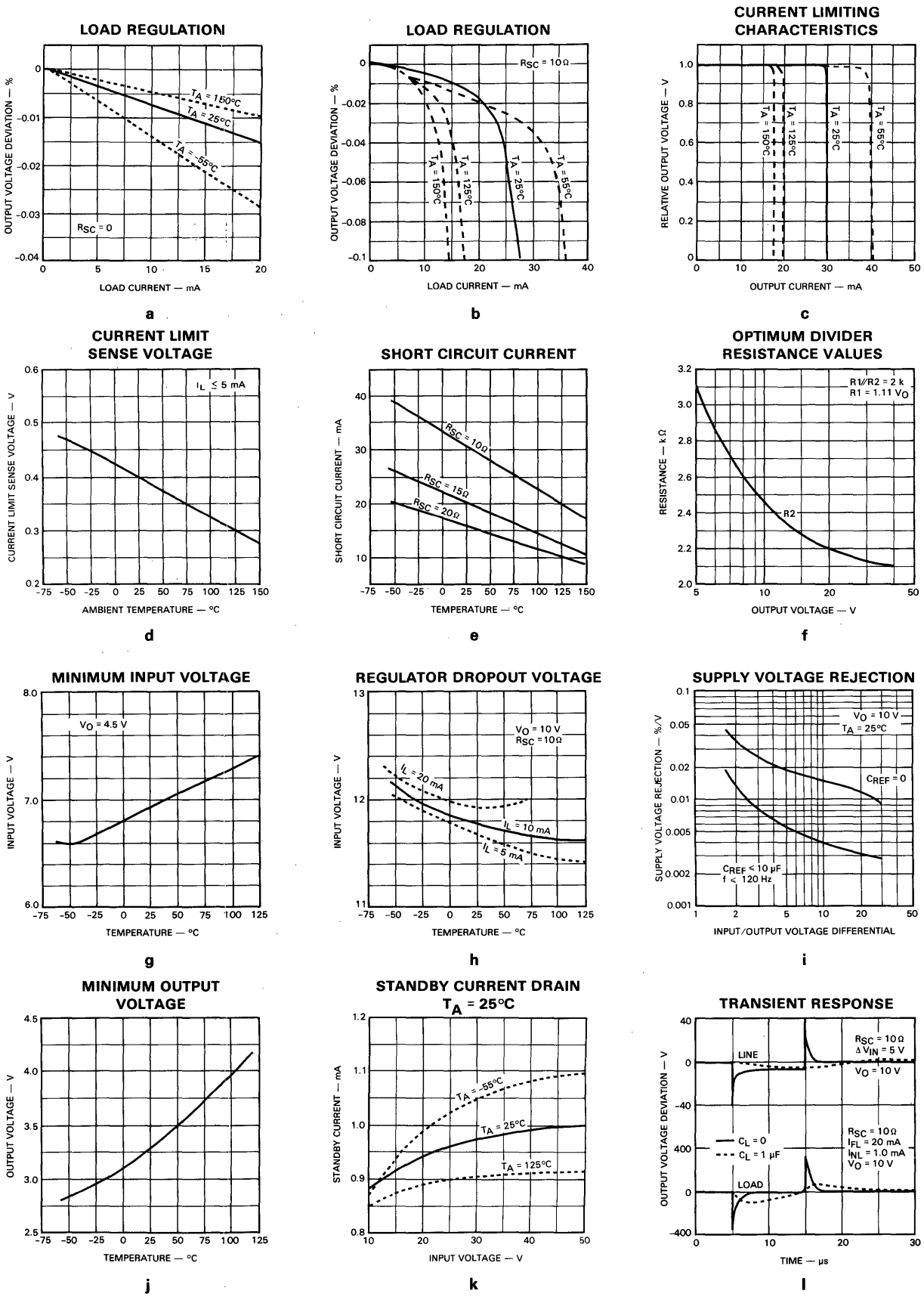


Fig. 9-11 Typical Performance Curves for 105/305/305A

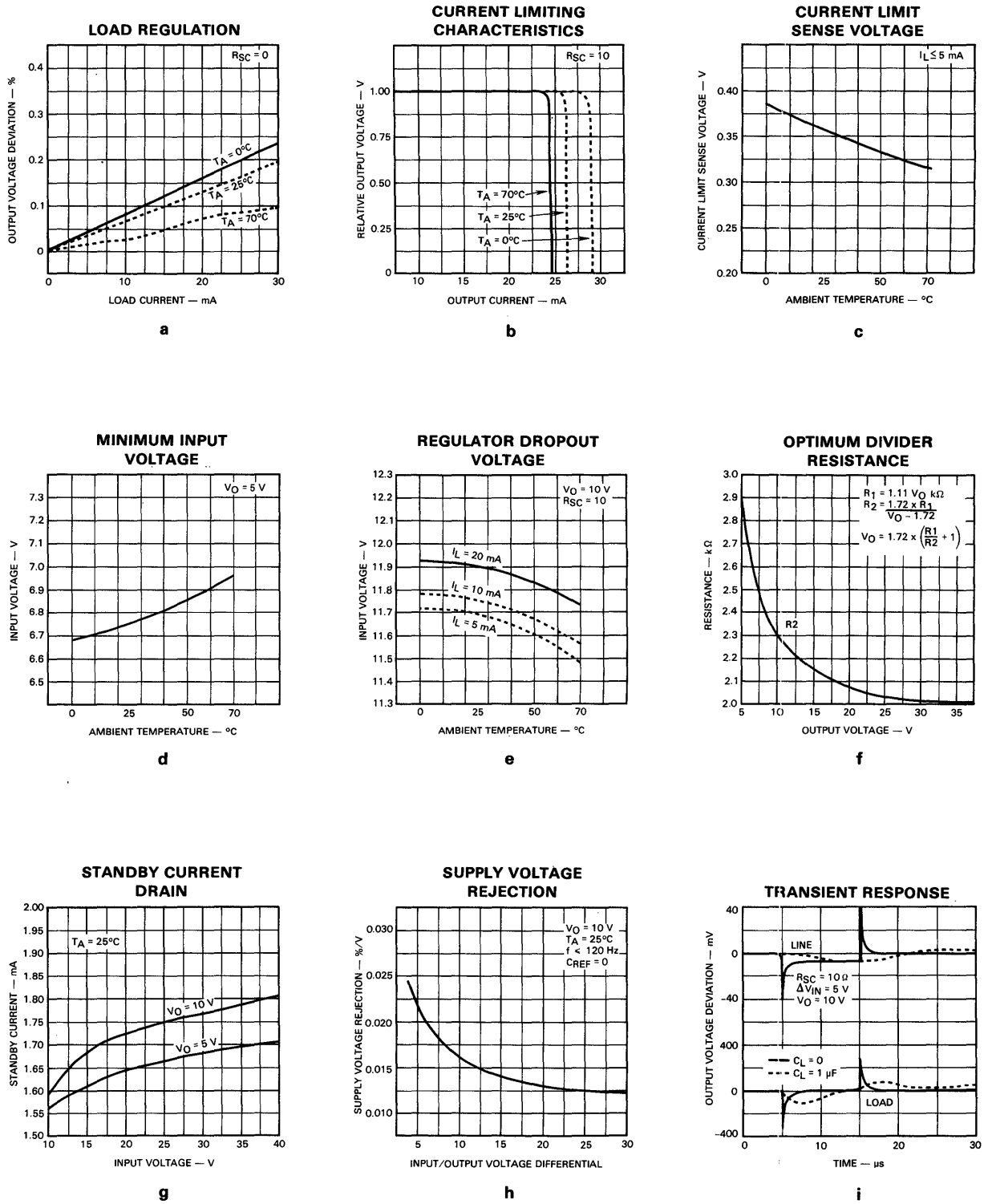


Fig. 9-12 Typical Performance Curves for 376

105

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 12$ mA	$R_{SC} = 10\Omega$, $T_A = 25°C$		0.02	0.05	%
		$R_{SC} = 10\Omega$, $T_A = 125°C$		0.03	0.1	%
		$R_{SC} = 10\Omega$, $T_A = -55°C$		0.03	0.1	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003	0.01	%/V
Temperature Stability	$-55°C \leq T_A \leq 125°C$			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu F$		0.002		%
Current Limit Sense Voltage	$R_{SC} = 10\Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	315	mV
Standby Current Drain	$V_{IN} = 50$ V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

305

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			8.5		40	V
Output Voltage Range			4.5		30	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 12$ mA	$R_{SC} = 10\Omega$, $T_A = 25°C$		0.02	0.05	%
		$R_{SC} = 15\Omega$, $T_A = 70°C$		0.03	0.1	%
		$R_{SC} = 10\Omega$, $T_A = 0°C$		0.03	0.1	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003	0.01	%/V
Temperature Stability	$0°C \leq T_A \leq 70°C$			0.3	1.0	%
Feedback Sense Voltage			1.63	1.7	1.81	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu F$		0.002		%
Current Limit Sense Voltage	$R_{SC} = 10\Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	315	mV
Standby Current Drain	$V_{IN} = 40$ V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

NOTES:

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal can and 5.6 mW/°C for the mini Dip.
2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.

305A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) Note 2

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			8.5		50	V
Output Voltage Range			4.5		40	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	$0 \leq I_L \leq 45$ mA	$R_{SC} = 0\Omega$, $T_A = 25°C$		0.02	0.2	%
		$R_{SC} = 0\Omega$, $T_A = 70°C$		0.03	0.4	%
		$R_{SC} = 0\Omega$ $T_A = 0°C$		0.03	0.4	%
Line Regulation	$V_{IN} - V_O \leq 5$ V			0.025	0.06	%/V
	$V_{IN} - V_O > 5$ V			0.015	0.03	%/V
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz			0.003		%/V
Temperature Stability	$0°C \leq T_A \leq 70°C$			0.3	1.0	%
Feedback Sense Voltage			1.55	1.7	1.85	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz	$C_{REF} = 0$		0.005		%
		$C_{REF} > 0.1\ \mu F$		0.002		%
Current Limit Sense Voltage (Note 4)	$R_{SC} = 10\Omega$, $T_A = 25°C$, $V_O = 0$ V		225	300	375	mV
Standby Current Drain	$V_{IN} = 50$ V			0.8	2.0	mA
Long Term Stability				0.1	1.0	%

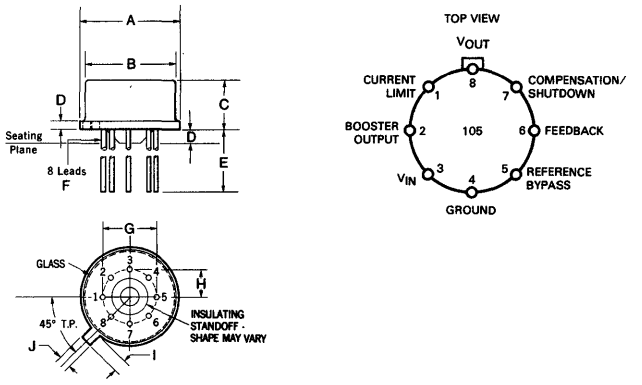
376

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 70°C$

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			9.0		40	V
Output Voltage Range			5.0		37	V
Output/Input Voltage Differential			3.0		30	V
Load Regulation	$0 \leq I_L \leq 25$ mA	$R_{SC} = 0\Omega$, $T_A = 25°C$			0.2	%
		$R_{SC} = 0\Omega$, $T_A = 70°C$			0.5	%
		$R_{SC} = 0\Omega$, $T_A = 0°C$			0.5	%
Line Regulation	$T_A = 25°C$				0.03	%/V
					0.1	%/V
Ripple Rejection	f = 120 Hz, $T_A = 25°C$				0.1	%/V
Standby Current Drain	$V_{IN} = 30$ V, $T_A = 25°C$				2.5	mA
Reference Voltage			1.60	1.72	1.80	V
Current Limit Sense Voltage				0.360		V

NOTES:

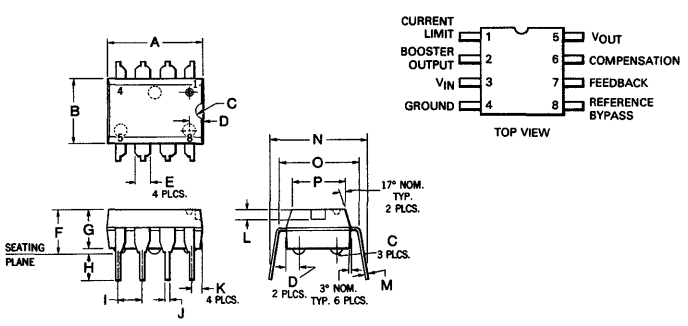
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the metal can and 5.6 mW/°C for the mini Dip.
2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. With no external pass transistor.



DIM	INCHES MIN	INCHES TYP	INCHES MAX	MILLIMETERS MIN	MILLIMETERS TYP	MILLIMETERS MAX
A	0.335		0.370	8.51		9.39
B	0.305		0.335	7.75		8.51
C	0.165		0.185	6.10		6.60
D			0.040			0.916
E	0.500			12.70		
F	0.016		0.019	0.406		0.483
G		0.200			5.08	
H		0.100			2.54	
I	0.029		0.045	0.737		1.140
J	0.028		0.034	0.711		0.864

NOTES:
Package weight 1.22 grams
Leads are gold-plated kovar
Lead 4 is connected to case

Fig. 9-13 Connection Diagram and Package Outline for 105/305/305A (TO-99 Package)



DIM	INCHES MIN	INCHES TYP	INCHES MAX	MILLIMETERS MIN	MILLIMETERS TYP	MILLIMETERS MAX
A	0.363		0.393	9.225		9.990
B	0.236		0.256	6.000		6.500
C		0.030			0.762	
D		0.050			1.270	
E	0.055		0.065	1.385		1.650
F			0.190			0.485
G	0.130		0.150	0.331		0.381
H	0.125			3.180		
I	0.090		0.110	2.282		0.279
J	0.016		0.020	0.406		0.508
K		0.039			0.989	
L		0.035			0.889	
M	0.009		0.011	0.228		2.790
N		0.375			9.520	
O	0.290		0.310	7.475		7.890
P		0.197			0.506	

NOTES:
Package weight 0.6 grams
Leads are tin or gold plated kovar

Fig. 9-14 Connection Diagram and Package Outline for 376 (Mini Dip Package)

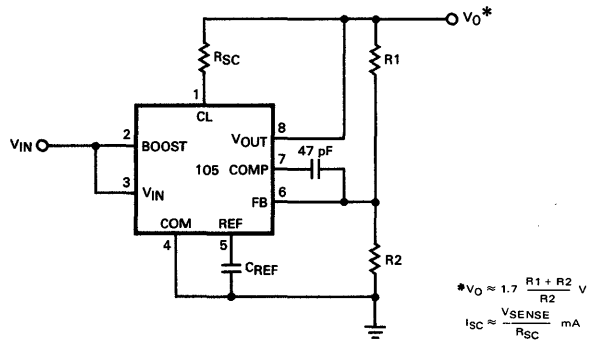


Fig. 9-15 Basic Positive Regulator and Test Circuit

109 FAMILY

The 109, 209, and 309 are 3-terminal 5 V regulators which can provide over 1 A output current with adequate heat sinking. They employ internal current limiting, thermal shutdown and safe area compensation, making them virtually indestructible.

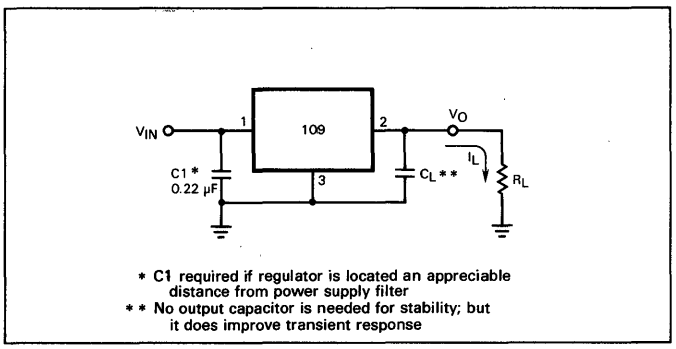


Fig. 9-16 Basic 5 V Regulator

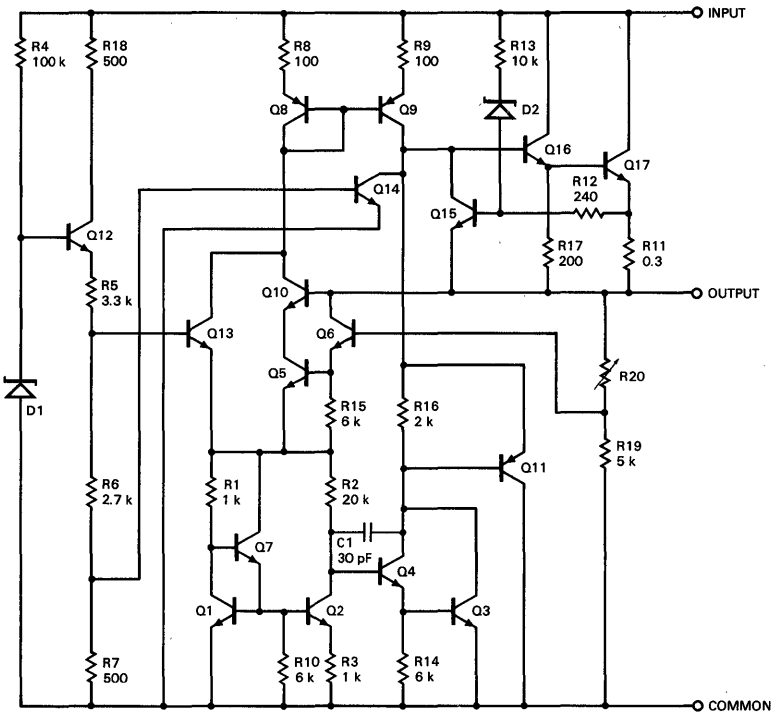


Fig. 9-17 Equivalent Circuit of the 109 Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	
109	-55°C to +150°C
209	-25°C to +150°C
309	0°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C

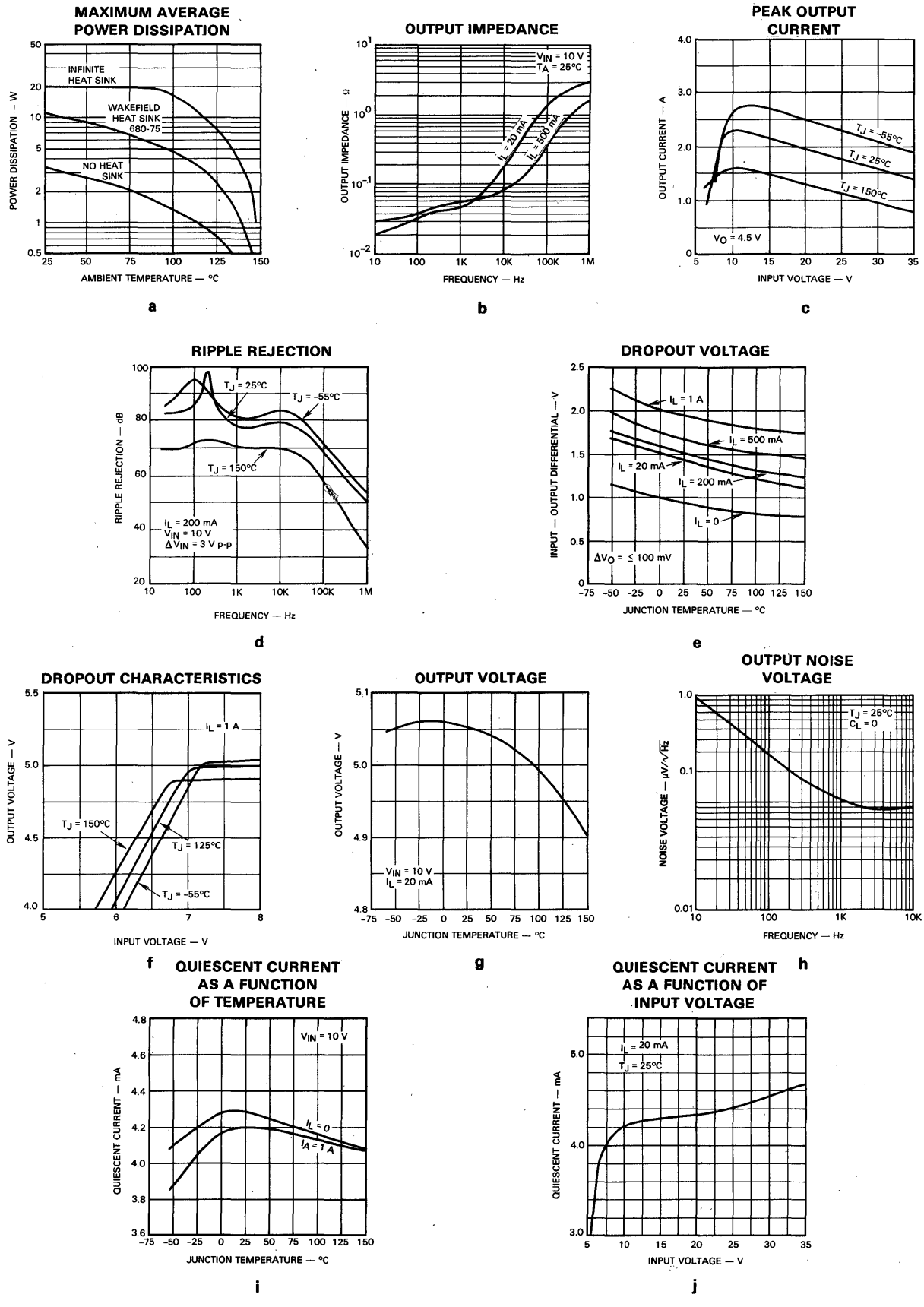


Fig. 9-18 Typical Performance Curves for 109 & 209

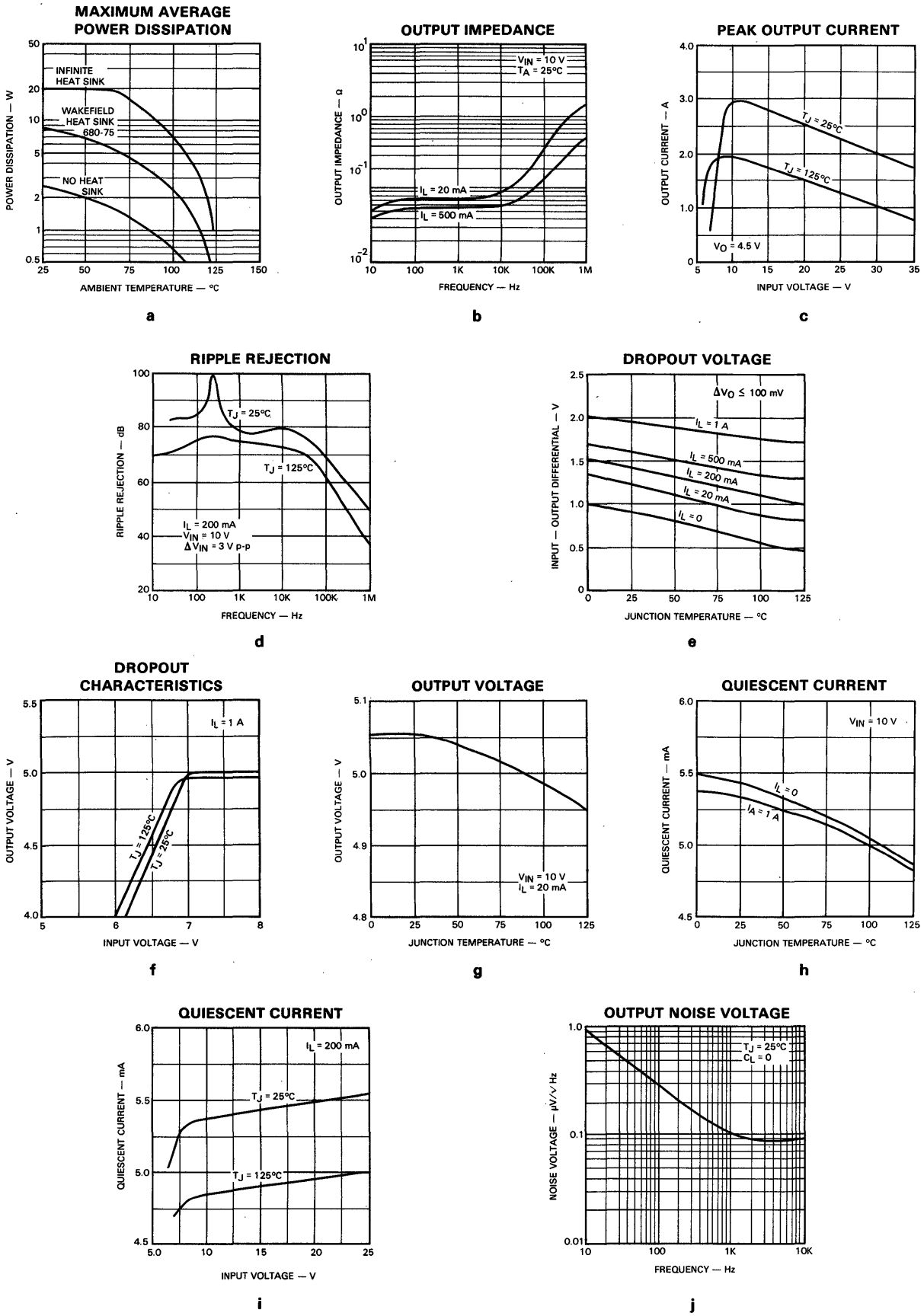


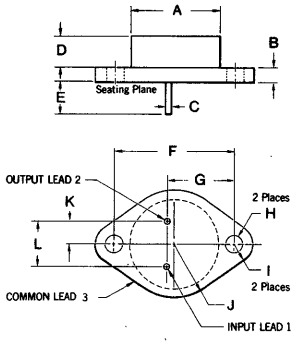
Fig. 9-19 Typical Performance Curves for 309

ELECTRICAL CHARACTERISTICS:

(T_J = −55°C to +150°C for 109, −25°C to +150°C for 209, 0°C to +125°C for 309, V_{IN} = 10 V, I_L = 0.5 A, unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage		T_J = 25°C 109, 209	4.7	5.05	5.3	V
		309	4.8	5.05	5.2	V
Line Regulation		T_J = 25°C, 7.0 V ≤ V_{IN} ≤ 25 V		4.0	50	mV
Load Regulation		T_J = 25°C, 5.0 mA ≤ I_L ≤ 1.5 A		15	100	mV
Output Voltage		109, 209 8.0 V ≤ V_{IN} ≤ 20 V, 5.0 mA ≤ I_L ≤ 1.0 A, P ≤ 20 W	4.6		5.4	V
		309 7.0 V ≤ V_{IN} ≤ 25 V, 5.0 mA ≤ I_L ≤ 1.0 A, P ≤ 20 W	4.75		5.25	V
Quiescent Current		7.0 V ≤ V_{IN} ≤ 25 V		4.2	10	mA
Quiescent Current Change	with Line	8.0 V ≤ V_{IN} ≤ 25 V			0.5	mA
	with Load	5.0 mA ≤ I_L ≤ 1.0 A			0.8	mA
Output Noise Voltage		T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40		μV
Long Term Stability		109, 209			10	mV
		309			20	mV
Thermal Resistance Junction to Case (Note 1)				3.0		°C/W

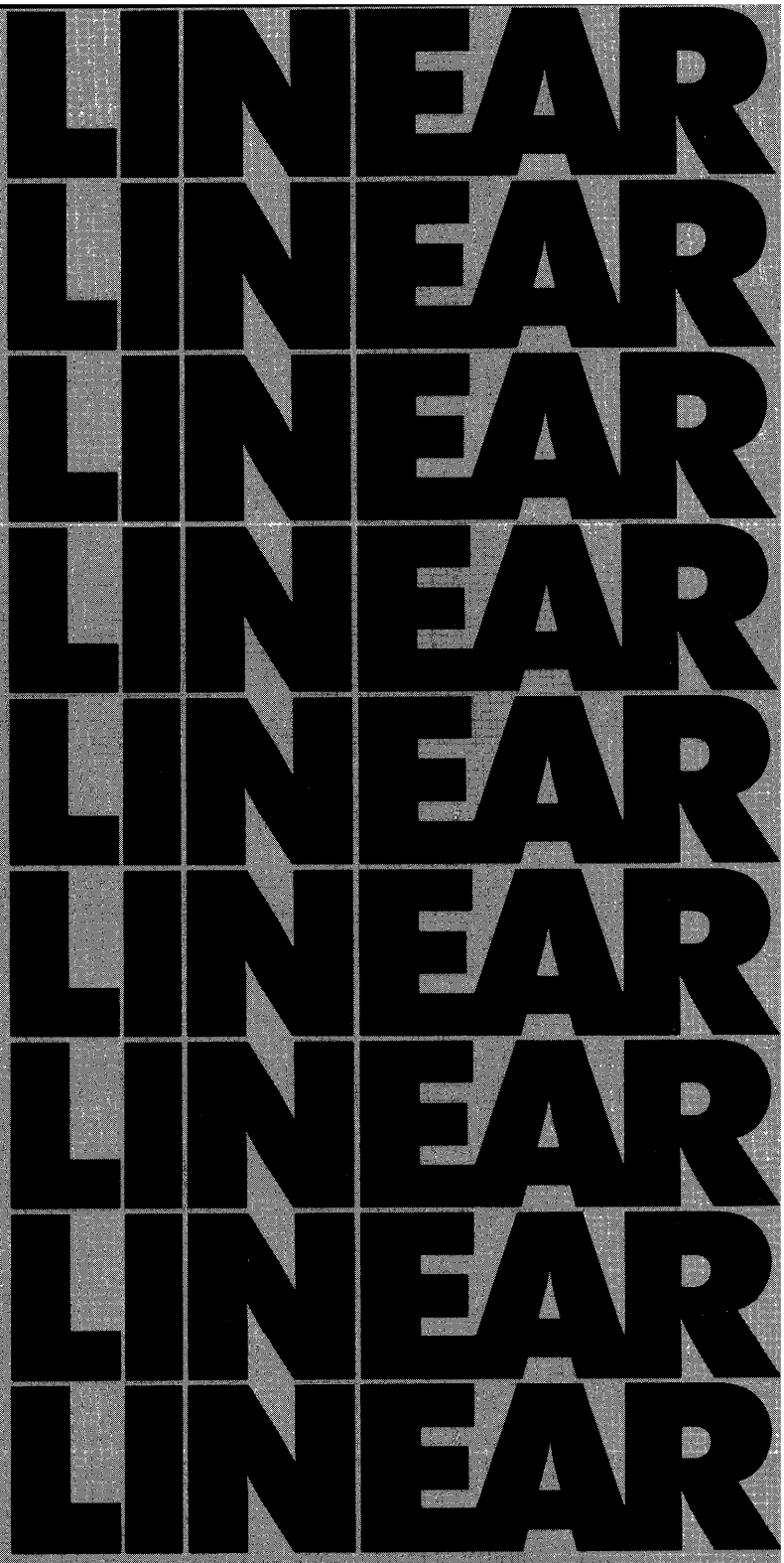
Note 1. Without a heat sink, the thermal resistance is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.



NOTES:
Leads 1 and 2 electrically isolated from case
Case is electrically connected to common
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams

	INCHES			MILLIMETERS		
DIM	MIN	TYP	MAX	MIN	TYP	MAX
A	0.805		0.835	20.45		31.21
B			0.135			3.43
C	0.038		0.048	0.965		1.12
D	0.205		0.325	5.20		8.25
E	0.312			7.92		
F	1.177		1.197	29.90		30.40
G	0.655		0.675	16.64		17.15
H	0.151		0.161	3.79		3.84
I			0.188			4.78
J			0.525			13.34
K	0.205		0.225	5.20		5.71
L	0.420		0.440	9.67		10.08

Fig. 9-20 TO-3 Outline And Connection Diagram



CONTENTS AND SECTION SELECTOR

IN THIS APPENDIX:

- INTRODUCTION
- CIRCUIT OPERATION
- DESIGN EXAMPLE
- POWER LOSSES

APPENDIX A
Switching Regulator Design

INTRODUCTION

The switching mode voltage regulator offers the advantage of high efficiency over the more common series or shunt regulation schemes. This is particularly apparent when there is a large difference between the input voltage and the regulated output voltage. Consider, for example, a voltage regulator with 28 V input and an output of 5 V at 1 A. A conventional series regulator would require a drop of 23 V across the pass transistor. Thus, 23 W are wasted, and the efficiency is only 18%. Switching regulators, however, can be simply designed to give efficiencies greater than 75% under the same input and output restrictions.

Switching regulators are also useful in applications where cost, rather than efficiency, is the prime design criterion. The designer may trade the cost of a high power series pass transistor for a slight increase in circuit complexity that allows the use of lower power switching transistors.

One area of caution when using switching regulators is the generation of electromagnetic and radio frequency interference (EMI and RFI). Solutions to these problems generally revolve around the use of feed-through low pass filters isolating the lines to the regulator, and careful mechanical design to suppress radiated interference.

CIRCUIT OPERATION

Basic Switching Regulator

Referring to *Figure A-1*, the operation of a switching regulator depends upon a duty cycle generated by switch Q1 and integrated by choke L1, capacitor C1 and freewheeling diode D1, to transfer the power efficiently from a higher input voltage to a lower output voltage at a ratio determined by the duty cycle. Diode D1 conducts during the time switch Q1 is open to provide a current path for the choke L1 to maintain current flow into capacitor C1. Conversely, when Q1 closes, the diode must recover in the shortest possible time to optimize the overall circuit efficiency.

The switch transistor Q1 is operated only in saturation or in cut-off so that power dissipation is kept to a minimum.

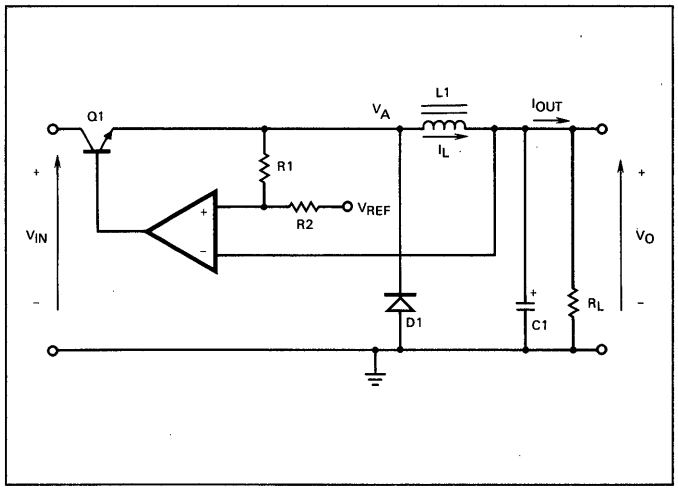


Fig. A-1 Basic Switching Regulator

When Q1 closes, the current flowing through L1 will increase linearly according to the equation shown.

$$V_{IN} - V_{OUT} = L1 \frac{\Delta I_L}{t_{on}}$$

This current supplies the load R_L and charges capacitor C1. The voltage at the non-inverting input of the error amplifier is given approximately by the following formula.

$$V'_{REF} = V_{REF} + V_{IN}\left(\frac{R1}{R2}\right) \text{(assuming R2 >> R1).}$$

V_{IN} (R1/R2) is equal to the hysteresis V_H introduced to the error amplifier to assure a switching mode of operation. When V_O reaches V'_{REF}, the error amplifier turns off transistor Q1. The current in L1 starts to decrease, causing the voltage at point A to swing negatively until D1 is forward biased. The inductor current now flows through D1, and decreases at a rate approximated by:

$$V_O = L1 \frac{\Delta I_L}{t_{off}}$$

When the inductor current falls below the load current, the output capacitor starts to discharge and V_O decreases. When V_O falls to a level slightly less than V_{REF}, the error amplifier turns Q1 back on and the cycle is repeated. The output from the regulator ripples above and below a dc level set by V_{REF}. The peak-to-peak ripple is slightly greater than V_H because inductor current continues to charge the capacitor for a short time after Q1 is switched off. The pertinent voltage and current switching waveforms are shown in *Figure A-2*.

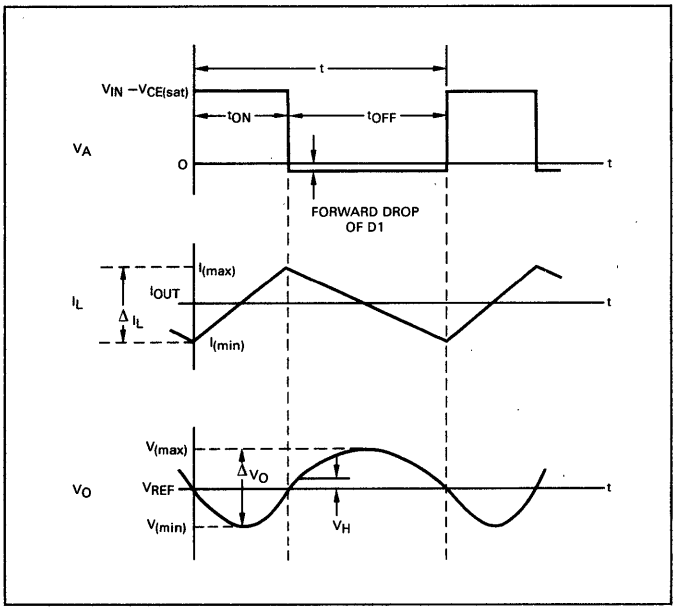


Fig. A-2 Switching Waveforms

A

DESIGN EXAMPLE

All of the elements needed to control the operation of a switching regulator are contained in IC voltage regulators; this makes them ideal for use as control circuits in switching regulators. Using the μA723 in the construction of a 5 V, 2 A regulator from a 28 V input illustrates the design of such a regulator. Maximum inductor current is 2.1 A, maximum peak-to-peak output ripple (ΔV_O) 40 mV, and the switching frequency 20 kHz.

Step 1 — Select V_H

Controlling the hysteresis provides a convenient means for trimming the operating frequency as well as supplying positive feedback to enhance switching action. A reasonable value for V_H is 10 to 20 mV below the allowable peak-to-peak value of the output ripple. If V_H = 30 mV is selected and

$$V_H = V_{IN}\left(\frac{R1}{R2}\right) \text{(where R1<<R2)}$$

then, if R1 = 1 kΩ, $R2 = \frac{28(10^3)}{30(10^{-3})} \cong 1\,M\Omega$

Step 2 — Calculate L1

L1 may be calculated using the following relationship.

$$L1 = \frac{(V_{IN}-V_O)\,t_{on}}{2(I_{MAX}-I_{OUT})}$$

where:

$$t_{on} = \left(\frac{V_O}{V_{IN}}\right)\frac{1}{f}$$

then:

$$L1 = \frac{(28-5)}{2(2.1-2)} \bullet \frac{5}{28} \bullet \frac{1}{2X10^4} = 1.025\,mH$$

Step 3 — Calculate C1

C1 may be calculated as follows.

$$C1 = \frac{(V_{IN}-V_O)\,V_O}{8Lf^2V_{IN}\,(\Delta V_O - V_H)}$$

then:

$$C1 = \frac{(28-5)5}{8(1.025X10^{-3})\,(2X10^4)^2 28\,(40-30)\,(10^{-3})}$$

$$C1 = 125\,\mu F$$

The final circuit configuration (*Figure A-3*, Positive Switching Regulator) uses L1 = 1 mH and C1 = 100 μF.

$$V_O = V_{REF}\left(\frac{R2}{R1+R2}\right) = 5.0\,V$$

This circuit is further explained in Chapter 8, (*Figure 8-25a*). The efficiency of this circuit is 75% at 1 A output and 73% at 2 A output current.

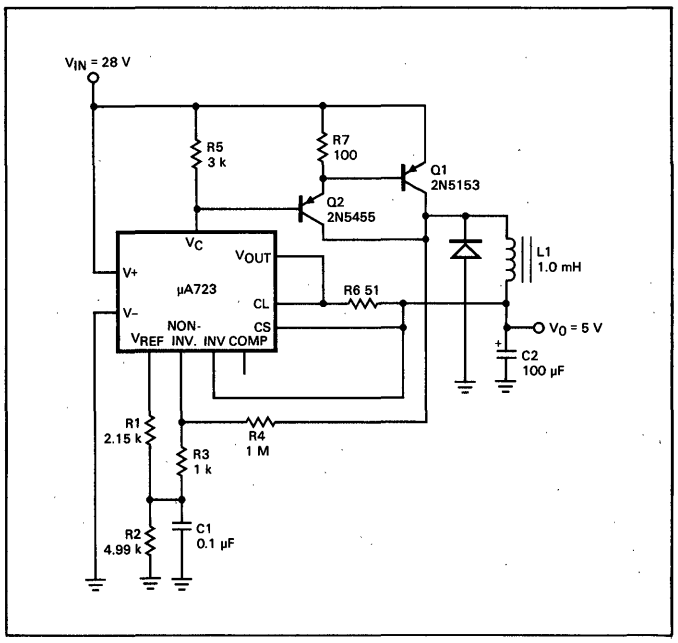


Fig. A-3 Circuit Configuration

POWER LOSSES

Power is lost in a switching regulator through conduction and switching losses.

The conduction loss in the switch transistor is a function of $V_{CE(sat)}$, I_{OUT}, and the fraction of a full cycle that the transistor is conducting. The power loss is given by:

$$\left(V_{CE(sat)}\right)\left(I_{OUT}\right)\left(\frac{t_{on}}{t_{on}+t_{off}}\right) \cong \left(V_{CE(sat)}\right)\left(I_{OUT}\right)\left(\frac{V_O}{V_{IN}}\right)$$

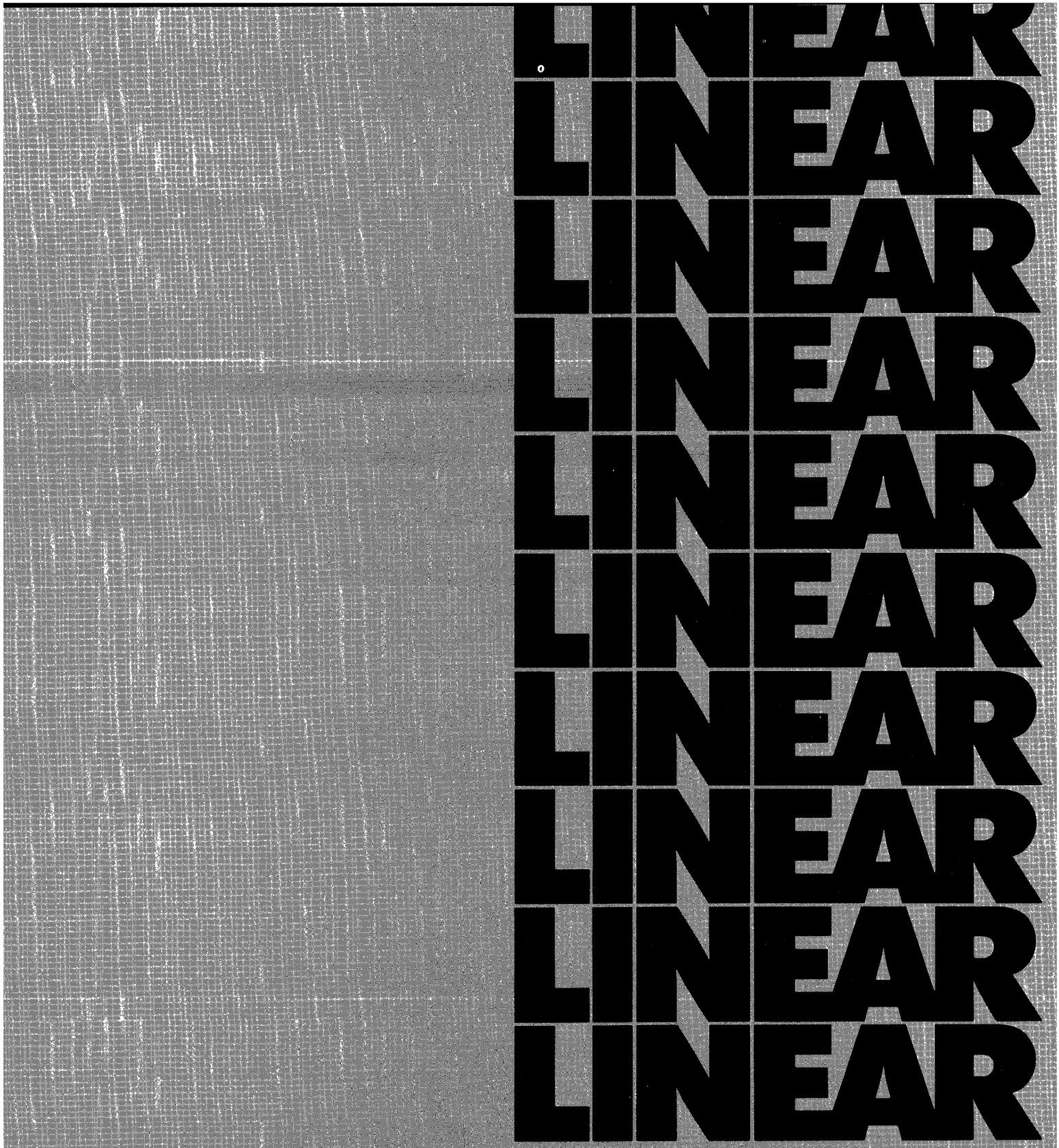
The diode D1 conducts during the time the switch transistor is off. The conduction loss of the diode is determined by the forward drop of the diode V_F, I_{OUT}, and the fraction of a cycle that the diode conducts. This conduction loss is given

$$V_F\,I_{OUT}\left(\frac{t_{off}}{t_{off}+t_{on}}\right) \cong V_F\,I_{OUT}\left(\frac{V_{IN}-V_O}{V_{IN}}\right)$$

Switching losses contribute substantially to the total power loss. The highest peak powers are dissipated when Q1 begins to turn on. Current from the transistor must remove the charge stored in D1, which is still in forward conduction. A transient current, limited primarily by the drive capability of Q1, flows for a time equal to the reverse recovery time of D1. During this interval the full input voltage appears across Q1, and the peak dissipation is quite high.

To minimize the power loss due to this current spike, D1 should be a fast recovery power diode. Ordinary power devices, not intended for switching operation, seriously degrade the regulator efficiency.

Some power is lost during the rise and fall times of the switching transistor, but this loss is negligible if high frequency switching transistors are used as bypass devices. Some power is lost due to the quiescent current in the IC regulator, and is to be considered in a detailed efficiency calculation. The greatest power losses, however, are attributable to the switching losses outlined above.



CONTENTS AND SECTION SELECTOR

IN THIS APPENDIX:

- INTRODUCTION
- DEFINITION OF TERMS
- SINGLE PHASE, HALF WAVE RECTIFIER
- HALF WAVE RECTIFIER WITH SERIES INDUCTIVE FILTER
- SINGLE PHASE, FULL WAVE RECTIFIER
- LC SECTION FILTER
- SWINGING CHOKE LC SECTION FILTER
- ELECTRICAL REFERENCES TABLE
- CAPACITIVE INPUT FILTER CHARACTERISTICS
- PRE-REGULATORS
- COMPLETE CIRCUITS

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2. Ryder, John D., "Electronic Engineering Principles," Prentice Hall, Inc., 1947, pp. 94-125.
3. Martin, Thomas L., Jr., "Electronic Circuits," Prentice Hall, Inc., 1955, pp. 506-541.
4. Seeley, Samuel, "Electron Tube Circuits," McGraw-Hill, 1958, pp. 194-230.
5. Gray, Truman, S., "Applied Electronics," John Wiley & Sons, Inc., 1954 pp. 250-277.

APPENDIX B
Power Supply Design

INTRODUCTION

In many power supply designs a means of converting an ac input voltage to a suitable dc voltage level is required. This is in addition to the voltage regulators discussed in this handbook. Appendix B discusses the performance characteristics of the most common forms of rectifier/filter combinations, and provides appropriate design equations for any output voltage and current.

DEFINITION OF TERMS

The following list covers those terms and definitions used in this Appendix.

Parameter	Definition
V_M	peak input voltage
V_O	dc output voltage
V_{pk}	transformer peak voltage
V_S	ac input voltage
F	form factor of the load current = $\frac{I_{rms}}{I_O}$
I_{ac}	effective value of all alternating components of load current, i.e., the current reading on an ac meter
I_M	peak current through each rectifier
I_O	average value of the load current, the reading on a dc meter
I_{rms}	effective value of the total load current $\sqrt{I_{ac}^2 + I_O^2}$
P_{in}	ac input power
P_O	dc output power
R_L	load resistance
R_S	total series resistance, or the source resistance plus any added resistance plus the diode series resistance
γ	ripple factor in all charts normalized as 100% equal to 1, $\gamma = (F^2-1) = \left[\left(\frac{I_{rms}}{I_O}\right)^2 - 1\right]^{1/2}$
ηR	rectification efficiency or $\frac{P_O}{P_{in}} \times 100\%$
ω	$2\pi f$ where f = line frequency

SINGLE PHASE, HALF WAVE RECTIFIER

Figure B-1 is a half wave rectifier and capacitor filter. Without the capacitor, peak current is

$$I_M = \frac{V_M}{R_S + R_L}$$

on the positive half cycle (or forward conduction cycle) of the input voltage. Some additional electrical characteristics follow.

$$I_{rms} = \frac{I_M}{2}$$

$$I_O = \frac{I_M}{\pi}$$

$$P_O = \frac{1}{\pi^2}\left(\frac{V_M^2 R_L}{(R_S+R_L)^2}\right)$$

$$\eta R = \frac{40.6}{\left(1+\frac{R_S}{R_L}\right)}$$

$$\gamma = 1.21$$

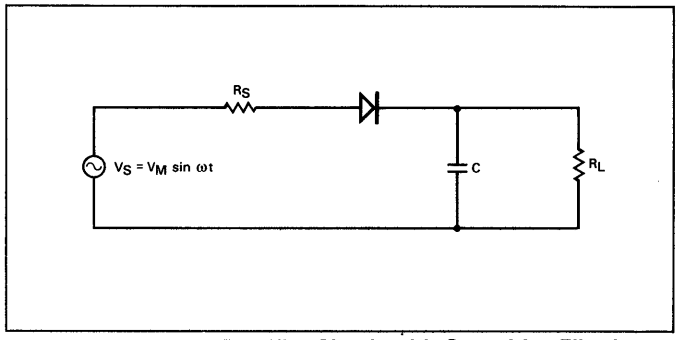


Fig. B-1 Half Wave Rectifier Circuit with Capacitive Filtering

Note that for a resistive load, the maximum ripple factor is 121% which, under most circumstances, requires filtering.

When the capacitor is added across the load resister, the ripple is reduced proportionate to the $R_L C$ product as shown in *Figure B-2*.

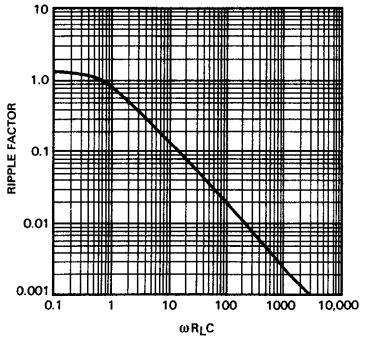


Fig. B-2 Ripple Factor vs $\omega R_L C$

One possible problem with any capacitive filter is the high peak current drawn due to the diode back-bias present throughout most of the input cycle. This is a result of the voltage stored across the filter capacitor. The rectifier conducts only during that short period of time when the input voltage exceeds the capacitor voltage by one diode drop. During conduction, the rectifier must supply the capacitor with sufficient energy to hold the ripple within specification until the next conduction cycle. *Figure B-3* is a plot of the I_M/I_O ratio versus the $R_L C$ product with the R_S/R_L ratio as a variable. Notice that the surge-to-dc ratio of current increases as a function of both increasing capacitor value and of a reduced source-to-load impedance ratio.

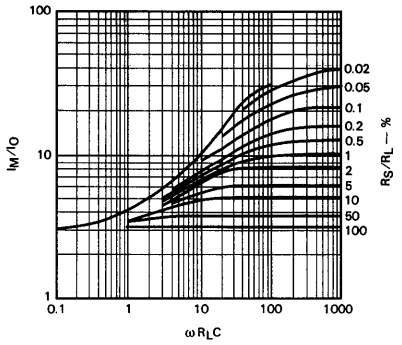


Fig. B-3 I_M/I_O vs R_LC Plot

When the ripple factor, load impedance, and ω are known, the required capacitance can be determined from *Figure B-2*. Because of the high turn on surge, an external series limiting resistor is normally needed. *Figure B-4* is a plot of the dc-to-peak voltage ratio with the filter product as the X axis and the source/load impedance ratio as the third parameter. Note that the dc output-to-peak input voltage ratio approaches unity as the filter factor goes up and also as the source-to-load impedance ratio decreases.

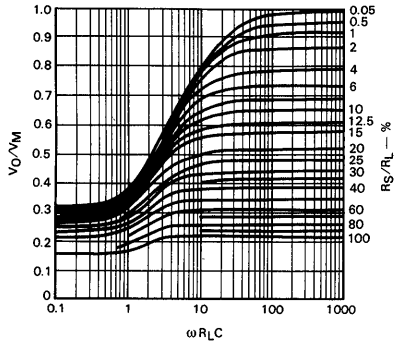


Fig. B-4 DC-to-Peak Ratio Plot

Because of the relatively large value of the filter capacitor required for a given ripple factor, the use of the half wave capacitor filter is usually limited to low current applications such as the subsidiary power supply for the µA723 in a floating regulator configuration.

HALF WAVE RECTIFIER WITH SERIES INDUCTIVE FILTER

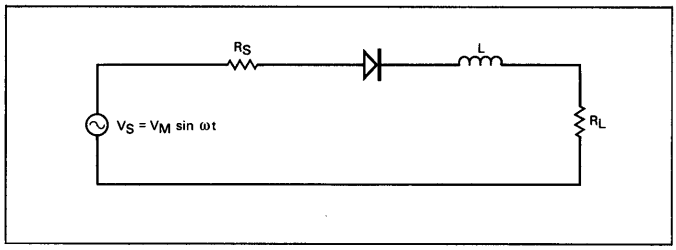


Fig. B-5 Half Wave Rectifier

Figure B-5 is a half wave rectifier with series inductive filtering. The inductor, in series with the load, prevents any rapid changes in the current flow and thus reduces the ripple factor by acting as an energy storage device. When the current flow is above the average current required, energy is stored in the inductor and, when the current is below the average, the stored energy is released. *Figure B-6* is the plot of ripple factor versus filter product for the inductor input filter.

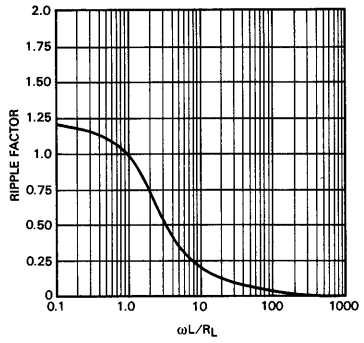


Fig. B-6 Ripple Factor vs Filter Product Plot

Because of the energy storage available with an inductor, the peak current through the rectifier is little more than the average current. However, the peak inverse voltage PIV seen by the rectifier is simply V_M, the peak input voltage. *Figure B-7* is a plot of the V_O/V_M ratio as a function of the inductive filter product.

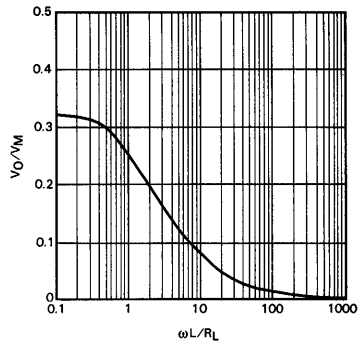


Fig. B-7 V_O/V_M Ratio Plot

SINGLE PHASE FULL WAVE RECTIFIER

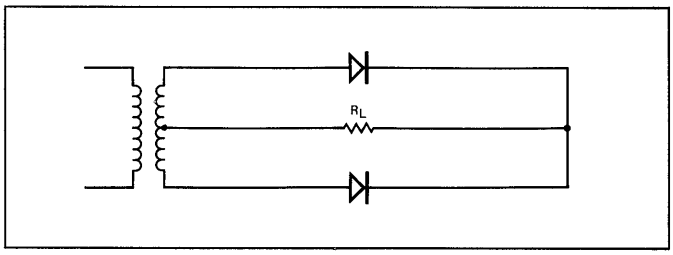


Fig. B-8 Basic Full Wave Rectifier

Figure B-8, a basic full wave rectifier, has the following electrical characteristics.

$$I_{rms} = \frac{I_M}{\sqrt{2}}$$

$$I_O = \frac{2I_M}{\pi}$$

$$P_O = \left(\frac{2}{\pi}\right)^2 \frac{V_M{}^2 R_L}{(R_S+R_L)^2}$$

$$\eta R = \frac{81.2}{\left(1+\frac{R_S}{R_L}\right)} \%$$

$$\gamma = 0.48$$

There are two interesting features. Efficiency has doubled, as can be expected when doubling the number of rectifiers. In addition, the ripple factor has decreased from 121% to 48% in comparison with the half wave circuit. Even with ripple reduction, a 48% factor is normally too high to be useful and must be filtered. *Figure B-9* is the filter product plot for both capacitive and inductive filters, assuming $R_S \ll R_L$.

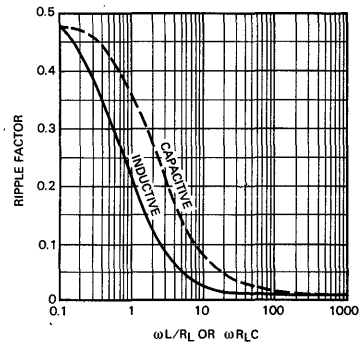


Fig. B-9 Filter Product Plot

High peak currents are always associated with capacitive filters and *Figure B-10* plots the ratio of peak-to-dc current as a function of the filter product.

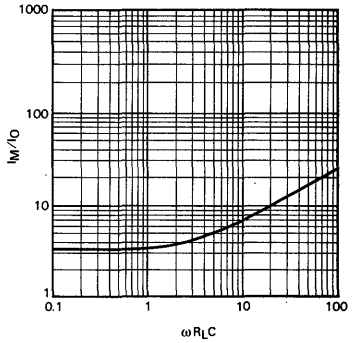


Fig. B-10 Peak-to-DC Ratio Plot

The relationship between the filter product, the R_S/R_L ratio and the dc output-to-peak input voltage is given in *Figure B-11* for the capacitive input filter. Load regulation may also be determined from *Figure B-11* by using the high and low limits for R_L.

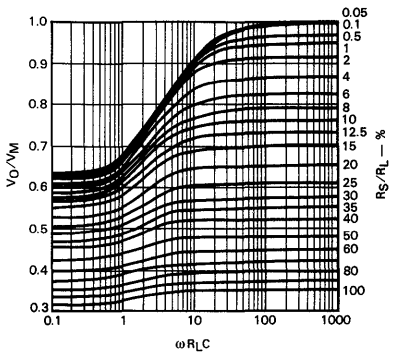


Fig. B-11 Load Regulation

Design Example

If a full wave circuit is required with the following characteristics,

$V_O = 20$ V

$I_O = 1$ A

$\gamma < 0.1$

with $R_S = 1\ \Omega$

then:

Step 1 Find the filter product from *Figure B-9* for $\gamma < 0.1. (\omega R_L C = 10)$

Step 2 Calculate R_L

$$R_L = \frac{20}{1} = 20\ \Omega$$

Step 3 Calculate C

$$C = \frac{10}{\omega R_L} = \frac{10}{120 \times 20\pi} = \frac{1}{240\pi} = 1300\ \mu F$$

Step 4 Calculate $\frac{R_S}{R_L}$

$$\frac{R_S}{R_L} = \frac{1}{20} = 5\%$$

Step 5 Find the transformer peak input voltage from the following.

V_{pk} = diode forward voltage. One diode forward voltage drop for a center tapped full wave input, two diode forward voltage drops for a full wave bridge

$$+ \frac{V_O}{V_O/V_M}$$

using the filter values from *Figure B-11.*

$V_{pk} = 0.7 + \frac{20}{0.82}$ (intersection of 5% $\frac{R_S}{R_L}$ and $\omega R_L C = 10$ from *Figure B-11.*)

$V_{pk} = 0.7 + 25.3 =$ 26 V peak or
52 V pk-pk or
18.6 V_{rms}

Step 6 Check peak diode current from *Figure B-10.* For this example at a filter product of 10, the peak current is seven times the dc current, or 7 A.

B

LC SECTION FILTER

The LC section filter is one method of reducing ripple levels without the need for single, large value filter components. The basic circuit is shown in *Figure B-12.*

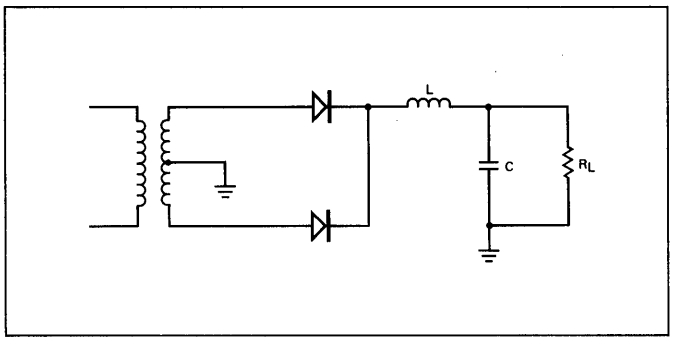


Fig. B-12 LC Filter

As a general rule, the capacitive reactance should always be less than 10% of the load resistance at the second harmonic of the incoming frequency. All the succeeding information is based upon this ratio.

The ripple factor for an L-section filter has the form:

$$\gamma = \frac{0.47}{4\omega^2 LC - 1}$$

or, if n L-section filters are cascaded, then the ripple factor is:

$$\gamma = \frac{0.47}{(4\omega^2 L1C1 - 1)\,(4\omega^2 L2C2 - 1) \cdots (4\omega^2 L_n C_n - 1)}$$

Figure B-13 is a plot of the filter factor versus the $\omega^2 LC$ product.

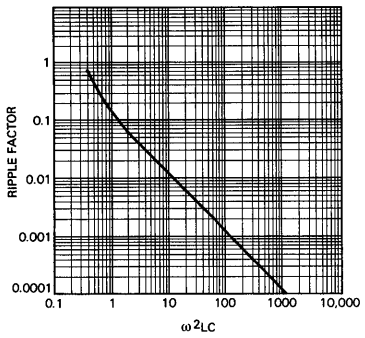


Fig. B-13 Filter Factor vs ω^2 LC

The one additional requirement is continuous current flow through the inductance. This says, in effect, that there is a critical inductor size. To assure this continuous current flow, a bleeder resistor R_K must be used at the filter output. The critical value of inductance is:

$$L_C = \frac{R_S + R_{eff}}{6\pi f}$$

where:

$$R_{eff} = \frac{R_K R_{L(max)}}{R_K + R_{L(max)}}$$

and:

$$R_K = \frac{V_O}{I_K}$$

Either I_K may be assumed to be 10% of minimum load current or, if this is not a practical value, then some reasonable minimum bleeder current is selected. Once the critical inductance is found, then the capacitor value may be determined by:

Step 1 Set $L = 2 L_C$

Step 2 Determine $\omega^2 LC$ from *Figure B-13* for the required ripple factor

Step 3 Solve for C from $\omega^2 LC = X$ where X is the product from *Figure B-13*

The peak rectifier currents depend upon the size of the inductor selected such that if $L = L_C$ then $I_M = 2\ I_L$ and if $L = 2\ L_C$ then $I_M = 1.5\ I_L$.

The transformer secondary voltage is given by:

$$V_{rms} = 1.11 \left[V_O + R_S\,(I_{L(max)} + I_K)\right]$$

and the minimum PIV for the rectifier is $1.57\ V_{O(max)}$ for a full wave bridge rectifier.

For minimum power dissipation, R_K should be as large as possible. In some cases, since the value of critical inductance is proportional to the value of the bleeder resistor, the selection of a high value results in an inductance too large to be practical. In this case, a swinging choke or a choke whose inductance decreases with increasing current flow, is needed.

Design Example

Full wave, single section, choke input filter design,

$V_O = 50$ V

$I_O = 1$ A

$I_K = 100$ mA

$R_S = 10\ \Omega$

$\gamma = 1\%$

Step 1 Calculate R_K

$$R_K = \frac{V_O}{I_K} = \frac{50\text{ V}}{100\text{ mA}} = 500\ \Omega$$

Step 2 Calculate R_{eff}

$$R_{eff} = \frac{R_K R_{L(max)}}{R_K + R_{L(max)}} = 500\ \Omega\ (R_{L(max)} = \infty)$$

Step 3 Calculate L_C

$$L_C = \frac{R_{eff} + R_S}{6\pi f} = \frac{500 + 10}{1130} = \frac{510}{1130} \cong 0.5\text{ H}$$

Step 4 Calculate C

$$\gamma = 0.01$$

then: $\omega^2 L_C C = 12$ from Figure B-13

$$C = \frac{12}{\omega^2 L_C} = \frac{12}{(120\pi)^2 0.5} =$$

$$\frac{12}{142 \times 10^3 \times 0.5} = 0.169 \times 10^{-3} = 169\ \mu F$$

Step 5 Calculate I_M

Since $L = L_C$

then $I_M = 2\ (I_O + I_K)$

$$I_M = 2 \times 1.1 = 2.2\ A$$

Step 6 Calculate voltage drop both at no load and full load

a. V_D no load = $I_K\ (R_S) = 0.1 \times 10 = 1$ V

b. V_D full load = $(I_O + I_K)\ R_S = 1.1 \times 10 = 11$ V

Step 7 Calculate transformer minimum rms voltages

$$V_{rms} = 1.11 \left[V_O + R_S\ (I_{O(max)} + I_K) \right]$$

$$V_{rms} = 1.11\ (50 + 10 \times 1.1)$$

$$V_{rms} = 1.11\ (61)$$

$$V_{rms} = 67.5\ V_{rms}$$

Step 8 Calculate maximum output voltage

$$V_{O(max)} = \frac{V_{rms}}{1.11} - I_K R_S$$

$$V_{O(max)} = \frac{67.5}{1.11} - 0.1 \times 10 = 61 - 1 = 60\ Vdc$$

Step 9 Calculate PIV rating required

$$PIV = (1.57)\ V_{O(max)}\ \text{(See Table B-1)}$$

$$PIV = 1.57 \times 60 = 94\ V$$

The transformer ratios are determined from Table B-1.

SWINGING CHOKE LC SECTION FILTER

When designing a swinging choke section filter, the inductance required at the minimum and maximum output currents can be determined as follows.

1. Find L_C (critical inductance)

$$L_C = \frac{R_S + R_{eff}}{6\pi f}$$

where, as before:

$$R_{eff} = \frac{R_K R_{L(max)}}{R_K + R_{L(max)}}$$

2. Find L2 (inductance at maximum load current)

$$L2 = \frac{R_S + R_{eff2}}{6\pi f}$$

where:

$$R_{eff2} = \frac{R_{L(min)}\ R_K}{R_{L(min)} + R_K}$$

When L_C has been determined, then the capacitor value may be calculated as before.

The condition $\omega^2 L_C \leqslant 1/4$ should be avoided due to possible filter instabilities.

B

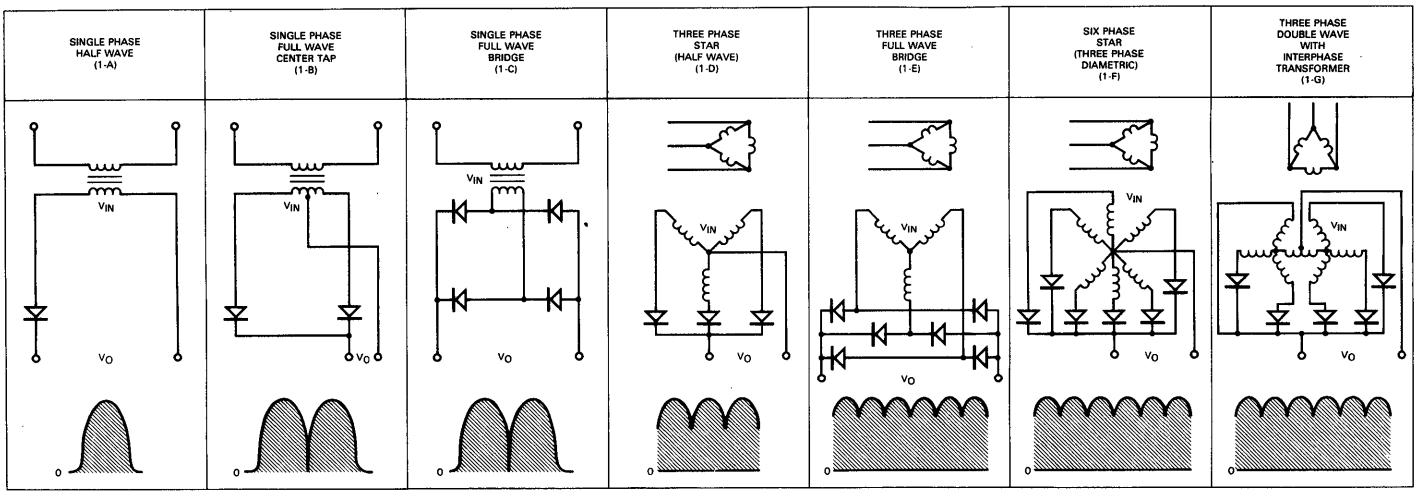


Fig. B-14 Rectifier Circuits Wave Shapes

Characteristic	Load	Single Phase Half Wave (See 1-A)	Single Phase Full Wave Center-Tap (See 1-B)	Single Phase Full Wave Bridge (See 1-C)	Three Phase Star (Half Wave) (See 1-D)	Three Phase Full Wave Bridge (See 1-E)	Six-Phase Star (Three Phase Diametric) (See 1-F)	Three Phase Double Wave With Interphase Transformer (See 1-G)
R.M.S. Input Voltage Per Transformer Leg (V_I)	Resistive & Inductive	2.22 V_O	1.11 V_O	1.11 V_O	0.855 V_O	0.428 V_O	0.741 V_O	0.855 V_O
	Capacitive	0.707 V_O	0.707 V_O	0.707 V_O	0.707 V_O	0.408 V_O	0.707 V_O	0.707 V_O
Peak Inverse Voltage Per Rectifier (P.I.V.)	R & L	3.14 V_O	3.14 V_O	1.57 V_O	2.09 V_O	1.05 V_O	2.09 V_O	2.09 V_O
	C	2.00 V_O	2.00 V_O	1.00 V_O	2.00 V_O	1.00 V_O	2.00 V_O	2.00 V_O
Average Current Through Rectifier I_F	R.L. & C	1.00 I_O	0.50 I_O	0.50 I_O	0.333 I_O	0.333 I_O	0.167 I_O	0.167 I_O
Peak Current Through Rectifier I_M	R	3.14 I_O	1.57 I_O	1.57 I_O	1.21 I_O	1.05 I_O	1.05 I_O	0.525 I_O
	L		1.00 I_O	1.00 I_O	1.00 I_O	1.00 I_O	1.00 I_O	0.500 I_O
	C	Depends on Size of Capacitor						
Transformer Total Secondary VA	Sine Wave	3.49 P_O	1.75 P_O	1.23 P_O	1.50 P_O	1.05 P_O	1.81 P_O	1.49 P_O
	Sq. Wave	3.14 P_O	1.57 P_O	1.11 P_O	1.48 P_O	1.05 P_O	1.81 P_O	1.48 P_O
Transformer Total Primary VA	Sine Wave	3.49 P_O	1.23 P_O	1.23 P_O	1.23 P_O	1.05 P_O	1.28 P_O	1.06 P_O
	Sq. Wave	3.14 P_O	1.11 P_O	1.11 P_O	1.21 P_O	1.05 P_O	1.28 P_O	1.05 P_O
% Ripple	Sine Wave Resistive Load	121%	47%	47%	17%	4%	4%	4%
Lowest Ripple Frequency	–	1 F_I	2 F_I	2 F_I	3 F_I	6 F_I	6 F_I	6 F_I
Conversion Efficiency	–	40.6%	81.2%	81.2%	97%	99.5%	99.5%	99.5%

Table B-1 Electrical Reference Table

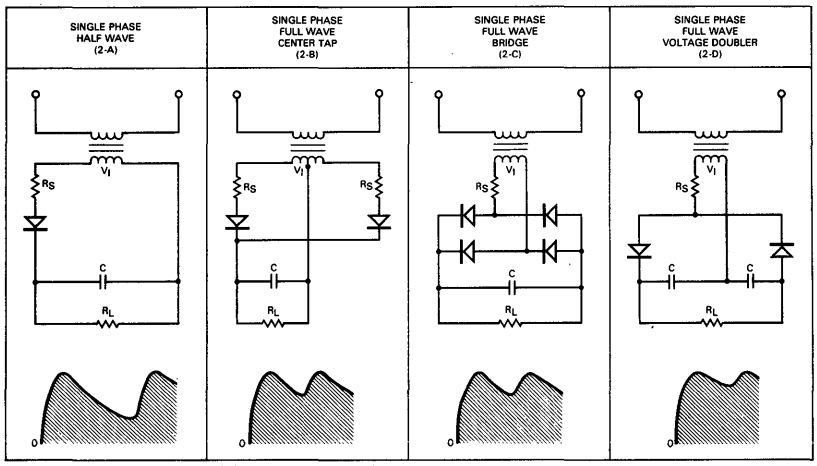


Fig. B-15 Rectifier Circuits Wave Shapes

Characteristic	Single Phase Half Wave (See 2-A)	Single Phase Full Wave Center-Tap (See 2-B)	Single Phase Full Wave Bridge (See 2-C)	Single Phase Full Wave Voltage Doubler (See 2-D)
V_I	0.910 V_O	0.825 V_O	0.805 V_O	0.552 V_O
PIV	2.56 V_O	2.34 V_O	1.14 V_O	1.56 V_O
Ripple	0.12 V_O	0.06 V_O	0.06 V_O	0.09 V_O
I_M/Rect.	7.80 I_O	4.75 I_O	4.75 I_O	3.00 I_O
I_{RMS}/Rect.	2.50 I_O	1.33 I_O	1.33 I_O	1.10 I_O
SEC VA	2.35 P_O	2.16 P_O	2.16 P_O	1.22 P_O
PRI VA	2.35 P_O	3.05 P_O	2.16 P_O	1.72 P_O

Table B-2 Capacitive Input Filter Characteristics

CAPACITIVE INPUT FILTER CHARACTERISTICS

- $R_S/R_{L(min)} = 0.02$
- $\omega CR_{L(min)} = 12$

When the voltage and current levels are known, Table B-2 can be used to select the optimum configuration and determine transformer and rectifier characteristics.

PRE-REGULATORS

Pre-regulators for use in power supplies take one of two forms.

- Fixed output circuit for use with limited output adjustment range supplies *(Figure B-16).*
- Tracking pre-regulators which maintain a fixed minimum input/output differential *(Figure B-17).*

In both cases this circuitry operates by holding the SCR gates at some dc potential which fires the forward biased (anode to cathode) device whenever the ripple voltage on the filter capacitor drops to a level sufficient to exceed the gate-to-cathode threshold of the SCR.

Two precautions are necessary when either pre-regulator circuit is used.

- The firing of the SCR is done on a dc drive basis, and represents a "soft fire" condition, i.e., no gate overdrive; this should be considered when selecting power devices.
- RFI should be considered in the application of these circuits as the SCRs operate effectively as phase control devices.

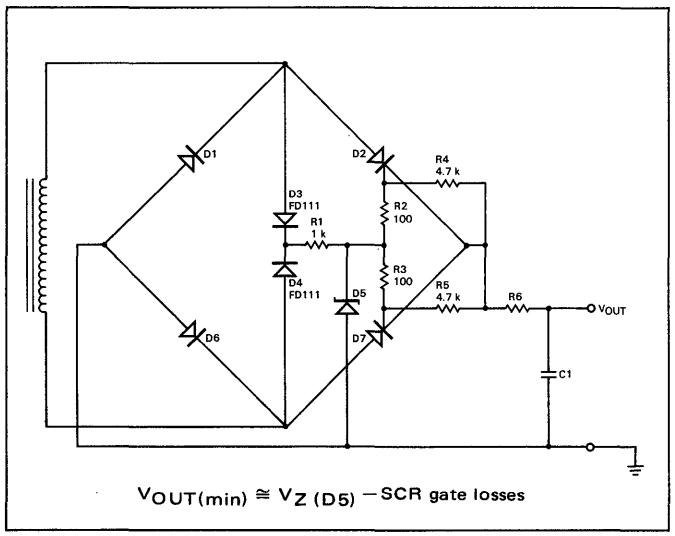


Fig. B-16 Fixed Output Circuit

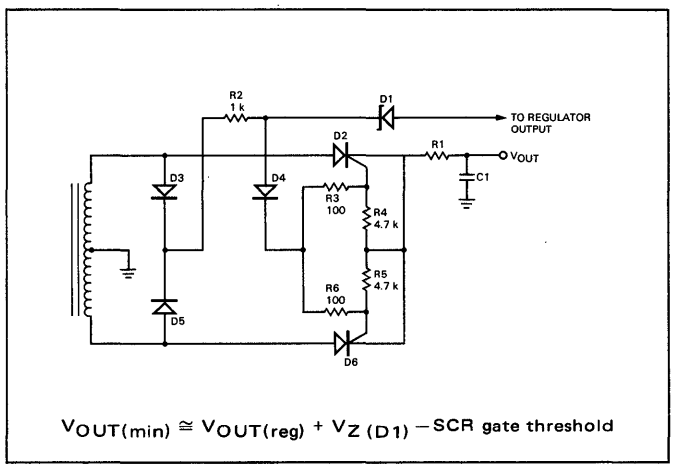


Fig. B-17 Fixed Input/Output Differential

B

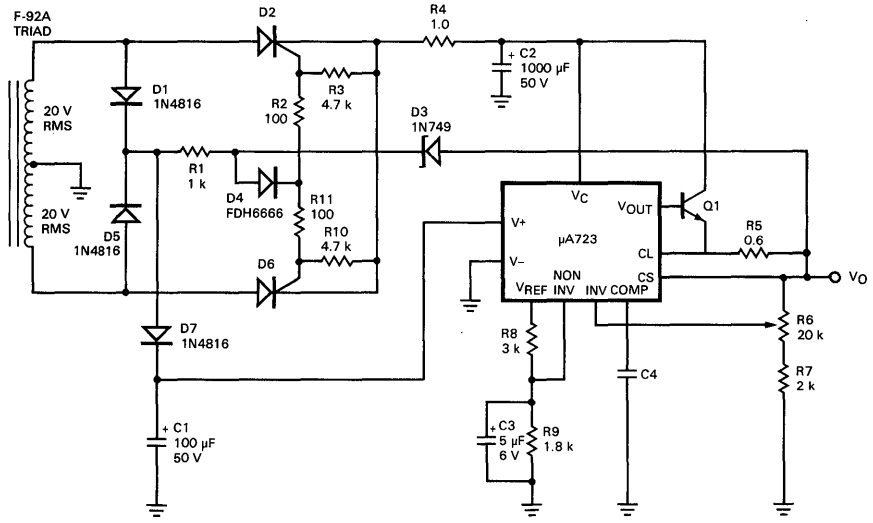
COMPLETE CIRCUITS

Two circuits are included to show combinations of several of the circuit techniques previously presented.

Figure B-18 is a grounded, tracking pre-regulator design adjustable from 3 to 25 V using the transformer shown with the minimum input/output differential set by the 1N749 Zener diode. The power for the regulator control portion is provided by a separate voltage source to insure efficient operation at low output voltages, while maintaining a voltage greater than the 9.5 V minimum specified for the μA723 internal circuitry.

Figure B-19 again provides a controlled voltage across the series pass device. But, due to the floating configuration, the device is capable of regulation from 0 to 150 V using the specified isolation transformers. In this example, the power for the integrated circuit is provided by the combination of the voltage doubler C1, C2, D1, D2 and transistor buffered Zener diode which provides approximately 20 V for the regulator.

In both *Figures B-18* and *B-19,* the maximum output capability is limited by the power components; therefore the selection of a heavy duty transformer, diodes, SCRs and output devices allows power capability expansion of the basic circuitry to fit almost any requirement.

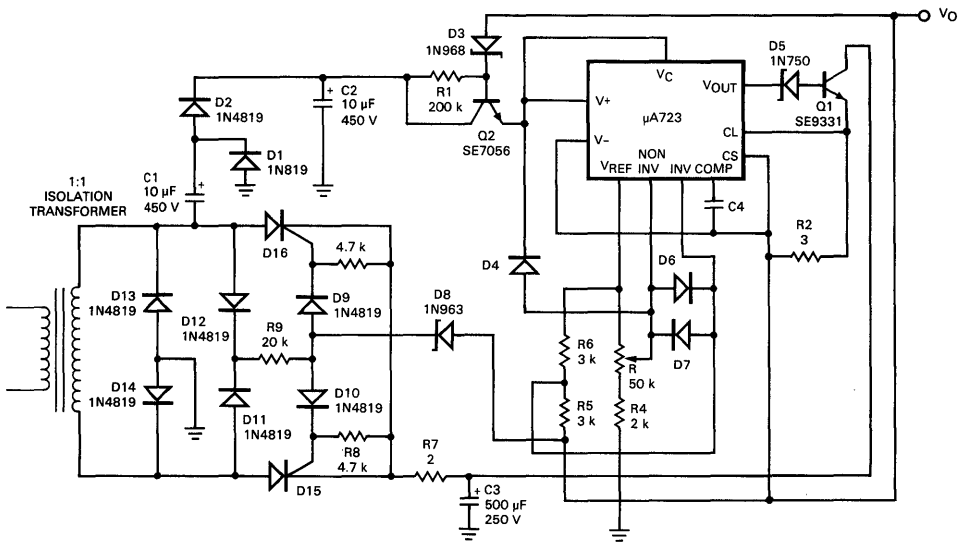


TYPICAL PERFORMANCE

V_O 3 V to 25 V (Transformer Limit)
I_{OUT} current limited at 0.8 A
Line Regulation < 1 mV any Voltage and Load
ΔV_{IN} = 95 Vrms to 125 Vrms

Load Regulation .04% of V_O
ΔI_{OUT} = 50 mA to 500 mA
Ripple and Noise = < 2 mV pk-pk over full V_O Range

Fig. B-18 Tracking Pre-Regulator

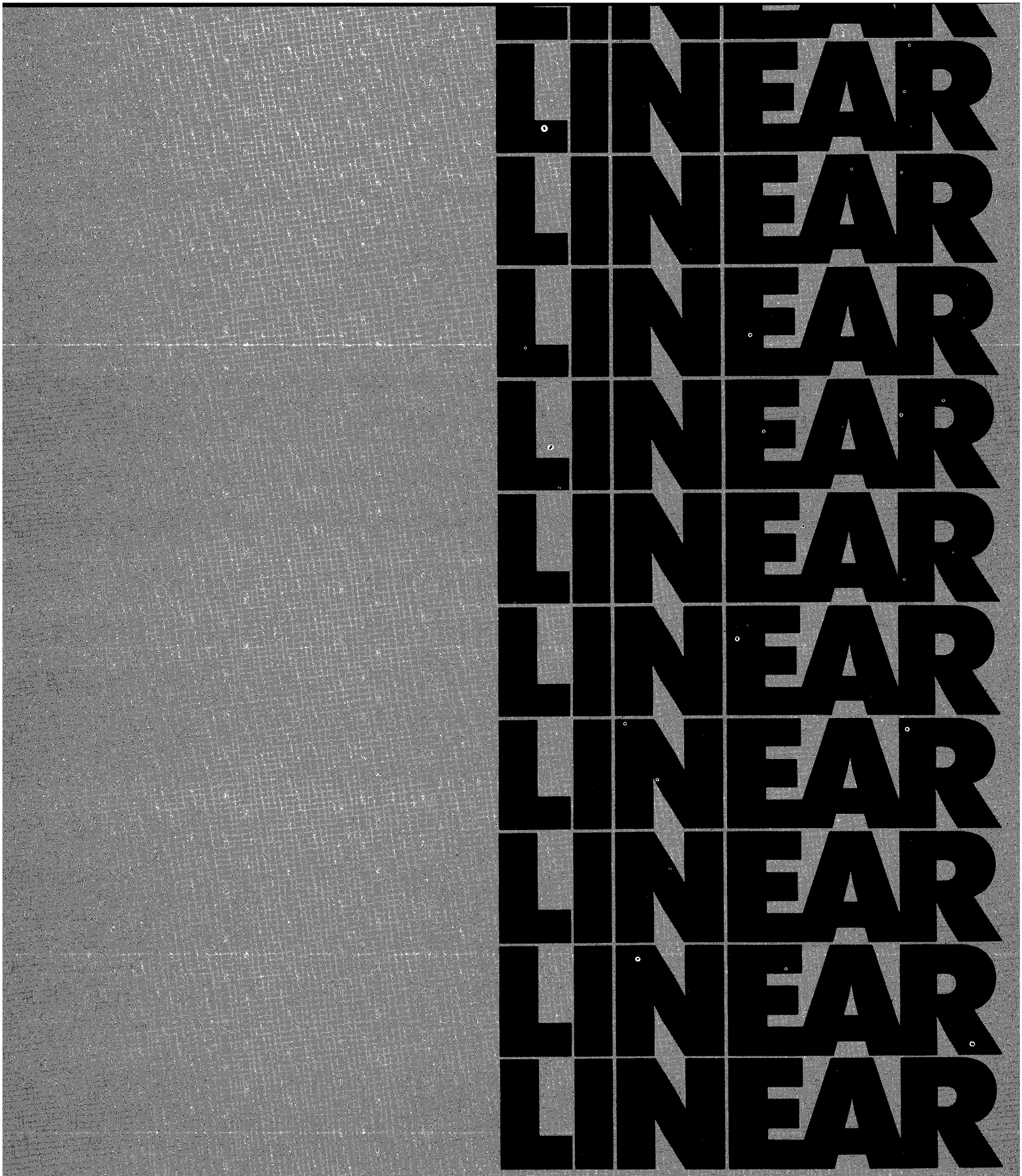


TYPICAL PERFORMANCE

V_O = 0 to +150 V_O (Transformer Limit)
I_{OUT} current limited at 170 mA
Line Regulation = 0.04% of V_O
ΔV_{IN} = 95 Vrms to 125 Vrms

Load Regulation 0.1% of V_O
ΔI_{OUT} = 15 mA to 150 mA
Ripple < 0.05% of V_O

Fig. B-19 High Voltage Tracking Regulator



CONTENTS AND SECTION SELECTOR

IN THIS APPENDIX:

- INTRODUCTION
- SAFE AREA CONSIDERATIONS
- FORWARD BIASED AREA
- REVERSE BIASED SAFE AREA
- SILICON POWER TRANSISTORS
- POWER TRANSISTOR SELECTION CHART

APPENDIX C
Power Transistors

INTRODUCTION

To assure the reliable design of a regulator involving power transistors, the designer must be fully aware of the capabilities and limitations of these components. The object of this appendix is to enhance the designer's understanding of the mechanisms affecting the performance of power transistors under conditions of high electrical and thermal stress. A selection guide of Fairchild power transistors is included. Full specifications, characteristic curves and package dimensions are available in the Fairchild Discrete Products Databook.

SAFE AREA CONSIDERATIONS

Power transistors are normally operated under high current/voltage/temperature conditions. These conditions, separately or in combination, can be destructive. Care must, therefore, be exercised to ensure that the device selected for a particular application is capable of safely withstanding all operating conditions that will be imposed. Safe area curves provide a means for determining this capability. These curves specify the limits within which each device can be safely operated without failure or degradation.

There are two basic safe area operation modes: the forward biased mode and the reverse biased mode. Bias here refers to the bias of the emitter base junction. A typical example of forward biased operation occurs during Class A operation of a power amplifier. A typical example of reverse biased operation occurs during the turn off of a hammer driver switch.

FORWARD BIASED AREA

A typical safe area plot for dc forward biased operation is shown in *Figure C-1*. Maximum permissible power dissipation P_D is shown as a function of collector-to-emitter voltage V_{CE} and case temperature T_C. Note that the plot is actually a composite of several safe areas, each corresponding to a different case temperature. This can be most easily understood by referring to *Figure C-2*, which illustrates the safe area that applies for a case temperature of 100°C. Operation at any point (any combination of voltage and power dissipation) within the area indicated is safe. For example, 30 W can be safely dissipated when case temperature is 100°C and collector voltage is 50 V.

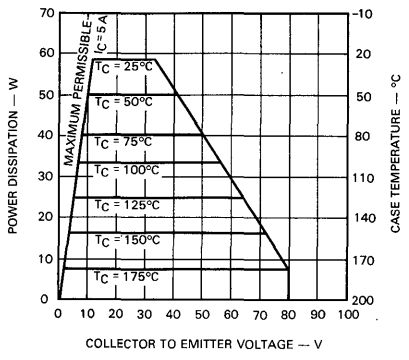


Fig. C-1 Typical Safe Area Plot

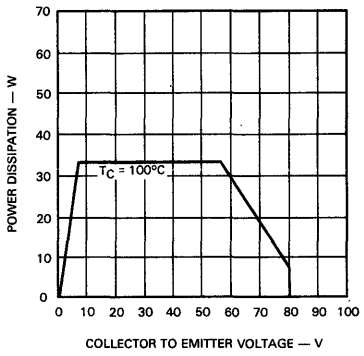


Fig. C-2 Forward Biased Safe Area, dc

Safe Area Limiting Factors

The basic factors limiting the dc forward biased safe area of a power transistor are indicated in *Figure C-3*. The left hand boundary represents the maximum rated collector current I_C. Operation to the left of this boundary may cause melting of the emitter lead wire, lifting of the lead wire bonds, or damage to the chip itself. The top boundary represents the thermal limitation. Operation above this boundary, at a specified case temperature, causes overheating of the chip which might impair reliability or, for some devices, melt the die attach solder.

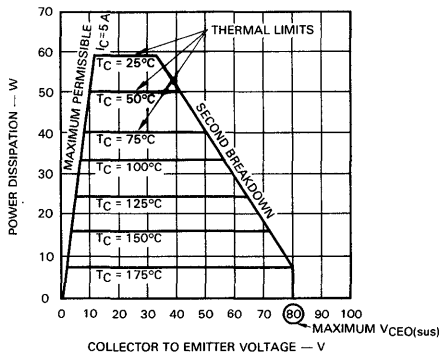


Fig. C-3 Safe Area Limiting Factors

The inclined portion of the right hand boundary represents the second breakdown. Operation to the right of this boundary causes second breakdown which might destroy the device due to localized overheating. The vertical portion of the right hand boundary represents the primary voltage breakdown limitation $V_{CEO(sus)}$. Operation to the right of this boundary results in voltage breakdown and excess current which can destroy the device.

The Thermal Limitation

The thermal limits placed on power dissipation, indicated by the upper boundaries of the safe area curves, are established to prevent overheating of the chip, and depend upon the junc-

tion-to-case thermal resistance Θ_{JC} of the device. This resistance determines how readily the heat generated in the chip during operation is conducted to the outside surface of the case (package). It is measured by comparing, at a known level of power dissipation, the temperature of the chip — specifically, the temperature of the collector base junction — with the temperature of the case. It is expressed in units of degrees centigrade (temperature difference) per watt (of power dissipation).

The industry specifies a maximum permissible junction temperature of 200°C for most power devices. Based on this limit and the Θ_{JC} value, maximum allowable power dissipation in the thermally limited region can be determined for any case temperature.

Heat Sinking

In general two types of heat sink are used. The commercial heat sink with a specified thermal resistance, and the available or added piece of metal whose thermal resistance can be determined through the use of the chart, *Figure 3-2*, Chapter 3. Note that thermal resistance decreases as the thickness of the mounting material increases.

Once the heat sink thermal resistance is known, then for any maximum ambient temperature, the maximum available power dissipation for a given device may be calculated using the following formula:

$$P_{D(max)} = \frac{T_{J(max)} - T_{A(max)}}{\Theta_{JC} + \Theta_{CHS} + \Theta_{HSA}}$$

Where:

Θ_{JC} = Thermal resistance from junction to case.

Θ_{CHS} = Thermal resistance from case to heat sink.

Θ_{HSA} = Thermal resistance from heat sink to ambient.

The Θ_{CHS} varies with the device mounting method, the use or absence of an alumina filled silicone grease to help remove the voids in the case-to-heat sink interface, the inclusion or absence of an electrical isolating mica, beryllia, or anodized aluminum washer between the device and heat sink and finally, the degree of mounting pressure which is applied through the device hold-down mechanism. Applicable package torque specifications should be observed to further minimize the case-to-heat sink thermal resistance. The results of using a silicone grease to help remove the voids in the case-to-heat sink interface is shown in Table C-1.

Thermal Resistance for TO-3 Package Outline		
Washer	Θ_{CHS} Dry °C/W	Θ_{CHS} with Silicone Grease*, °C/W
None	0.2	0.1
Mica	0.8	0.4
Anodized Al.	0.4	0.3

*Grease applied to both sides of washer.

Table C-1 Silicon Grease Characteristics

Using the above information, the maximum power dissipation available can be calculated for the following device and ambient conditions:

Power device 2N3055
Maximum ambient temperature 65°C
Heat sink thermal resistance 2.5°C/W at 10 W
(Thermal resistance decreases slightly with increasing power dissipation)
Mica washer with silicone grease

Maximum power dissipation is:

$$P_{D(max)} = \frac{200°C - 65°C}{1.5 + 0.4 + 2.4} = \frac{135}{4.4} = 30.7\ W$$

Similarly, if the heat sink thermal resistance is required for the following conditions:

$\Theta_{JC} = 3°C/W$
$T_{J(max)} = 200°C$
$T_{A(max)} = 55°C$
$P_D = 15\ W$
Anodized aluminum washer with silicone grease

then:

$$\Theta_{HSA} = \frac{T_{J(max)} - T_A}{P_D} - (\Theta_{JC} + \Theta_{CHS})$$

$$= \frac{200 - 55}{15} - (3 + 0.3) = 9.7 - 3.3 = 6.4°C/W$$

For TO-5 devices, and others without heat sinks, another thermal resistance value must be considered: case-to-ambient thermal resistance, Θ_{CA}. This resistance is typically much greater than Θ_{JC} since the mode of heat transfer is by convection and radiation into the surrounding ambient air, rather than by direct conduction. The total resistance to heat transfer out of the chip is the sum of Θ_{JC} and Θ_{CA}. This sum is junction-to-ambient thermal resistance Θ_{JA}. A typical value for a TO-5 device is 175°C/W.

The Second Breakdown Limitation

As indicated in *Figure C-3*, maximum power dissipation at relatively high voltages is limited not by thermal resistance, but by second breakdown. Second breakdown is a phenomenon wherein non-uniform current distribution in a transistor causes localized "hot spots". In a regenerative cycle, this further increases current concentration until, in the absence of controlling mechanisms, melting of the silicon in the area(s) of current concentration causes failure. Failure is characterized by a sharp decrease in collector-to-emitter voltage combined with a sharp increase in collector current. Second breakdown is so named to distinguish it from primary voltage breakdown BV_{CEO}.

The non-uniform current densities that initiate the second breakdown cycle are unavoidable. This is because forward biasing of the emitter base junction induces a transverse electric field in the base which causes current flow to concentrate in the area under the edge of the emitter periphery. Current density concentration in the area under the center of the emitter is minimal (see *Figure C-4*). As this concentrated current flows from the base through the collector base junction, localized heating is produced at a rate proportional to the product of collector voltage and current density. Note that some heat is also generated at the emitter base junction; however the voltage across the emitter base junction is usually much smaller than the voltage across the collector base junction, thus this heat is usually negligible.

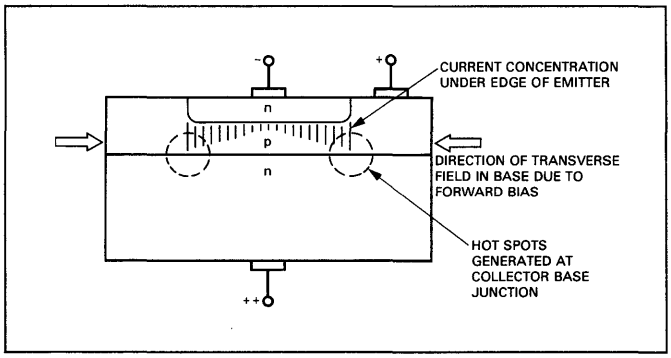


Fig. C-4 Current Concentration During Forward Bias Operation

The next step in the second breakdown cycle occurs when the heat from the collector base hot spots radiates upward, correspondingly causing hot spots at the emitter base junction. These hot spots cause localized reductions in the emitter base junction barrier, automatically developed at a junction, and must be overcome by forward bias voltage to induce current flow. This effectively increases forward bias in the hot spot areas, and this further intensifies current concentration. If unchecked, this cycle — current concentration causing hot spots which further increase current concentration — leads to thermal runaway and second breakdown (see *Figure C-5*).

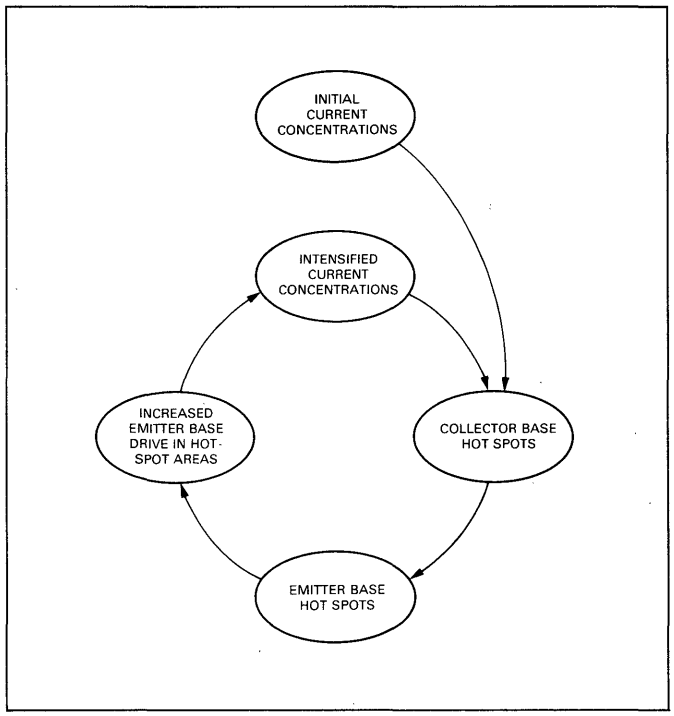


Fig. C-5 Thermal Runaway Cycle Which Causes Second Breakdown

Factors Influencing Second Breakdown Capability

Two key factors that improve the second breakdown capability of a power device are wide base widths and uniform base resistance (uniform dopant concentration). Wide base widths improve second breakdown capability in three ways. First, wide base widths reduce the intensity of the transverse electric field, thus reducing initial current concentration. Second, a wide base promotes fanning out of current before it reaches the collector base junction — tending to eliminate generation of hot spots. Third, a wide base acts to thermally isolate the emitter base junction from the hot spots generated in the collector base region, thus tending to prevent thermal runaway. Uniform base doping, such as obtained by the Fairchild Bimesar™ process utilizing epitaxial base material, improves second breakdown capability by reducing the intensity of the transverse electric field, thus reducing initial current concentration.

Fairchild Power Device Technology

Fairchild uses three basic power transistor chip technologies to span the power applications spectrum. The Bimesar process uses two epitaxial layers to form the collector and base regions, a mesa etch to define the collector base junction, and Planar processing to form the emitter base junction. This produces low cost, high current devices with excellent safe area capabilities. When compared to conventional single diffused devices, Bimesar transistors exhibit higher working voltage capabilities, lower saturation voltages, and lower leakage currents. Beta linearity is also improved and npn and pnp complementary devices are readily produced. Maximum current ratings extend to 30 A and f_T ratings to 10 MHz.

Double diffused power transistors employ base and emitter diffusions into an epitaxial collector region. Collector base and emitter base junctions are Planar passivated to ensure low leakage currents and optimum stability. Double diffused Planar epitaxial devices are primarily used in high frequency, high reliability switching and amplifying applications with f_T ratings greater than 30 MHz and maximum collector current ratings up to 30 A.

The triple diffused planar technology uses base and emitter diffusions and a heavily doped collector diffusion into a high resistivity silicon wafer. Junctions are then Planar passivated to minimize leakage currents. The high resistivity material used in these devices provides high voltage capability (to 350 V), while the heavily doped collector gives good saturation characteristics. Triple diffused Planar devices are used in high voltage switching and amplifying applications and have collector current ratings up to 15 A with f_T ratings from 10 MHz to 50 MHz.

Pulsed Operation

So far, discussion of forward biased safe area has been limited to dc operation. One other forward bias operating mode, namely, pulsed operation, must be considered. A typical safe area plot for pulsed operation is shown in *Figure C-6*. In this case, the vertical scale specifies collector current I_C, rather than power dissipation P_D. Each curve is labeled as to the duration of the on pulse — from the worst case dc condition to a minimum duration of 5 μs — and applies for a case temperature of 100°C and a duty cycle of 1%.

Very high peak power dissipation is possible during pulsed operation. In *Figure C-6*, for example, peak power of 360 W at 60 V is permissible for a pulse width of 0.1 ms, compared with maximum power of only about 115 W at 60 V for dc conditions. This high peak power capability arises from the inherent thermal capacitance of the device which enables it to absorb short bursts of energy without exceeding the maximum junction temperature or going into second breakdown. If the time between power pulses is relatively long (low duty cycle), most of the stored thermal energy is dissipated before the next power pulse arrives; thus, temperature build-up in the device is prevented. As indicated in *Figure C-6*, allowable peak power increases as pulse width decreases. This follows from the fact that total energy absorbed is equal to the product of power and time. If the time duration of the pulse decreases, peak power can increase without increasing total energy absorbed.

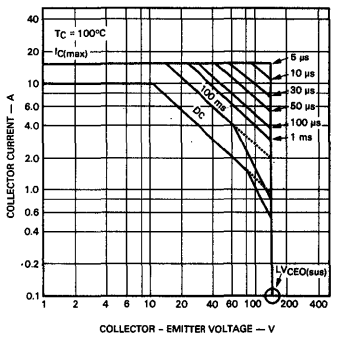


Fig. C-6 Typical Safe Area Plot for Pulsed Forward Biased Operation

REVERSE BIASED SAFE AREA

When the emitter base junction of a transistor is reverse biased, the device begins to turn off. The power which must be dissipated during turn off depends on the external circuitry, particularly the collector load. Where the load is resistive or capacitive, current quickly decays to zero while collector voltage rises to the value of the supply voltage. Power dissipated is minimal and little reverse biased safe area is required.

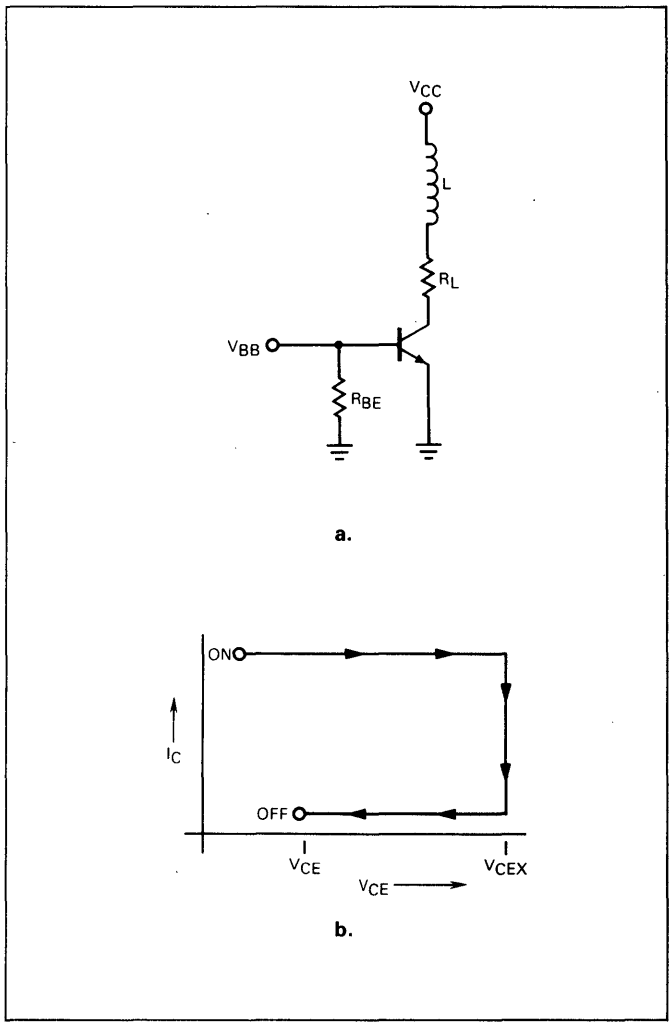


Fig. C-7 (a) Inductive Load Circuit (Unclamped); (b) V_{CE} vs I_C Load Line Traversed During Turn Off

Inductive Loads

Where the load is inductive, high levels of power dissipation may be encountered during turn off (see *Figure C-7*). Note that as soon as the device is reverse biased, the inductor attempts to maintain constant current, and in doing so, drives the transistor into breakdown BV_{CEX} forcing current to continue to flow. Collector current continues to flow, at a decreasing rate, as the stored inductive energy is discharged. When the inductive energy is fully discharged, collector voltage falls back to approximately V_{CC} and current is approximately zero (there is, of course, some leakage current). The total energy dissipated by the transistor during turn off is approximately equal to the stored energy in the inductor.

Current Concentration During Reverse Bias

Reverse biased operation is thus similar to pulsed forward biased operation, since high energy pulses of relatively short duration must be sustained. However, power capability in this mode is generally lower then in the pulsed forward biased mode. This is because the direction of the transverse electric field in the base is reversed during reverse bias. This concentrates current into a small area under the center of the emitter, rather than into the relatively large area under the emitter periphery where current concentrates during forward bias. Since current concentration tends to be greater, power capability is generally lower. Failure occurs when excessive heat build-up melts or degrades the silicon in the area of current concentration.

Factors Influencing Reverse Bias Safe Area

The reverse biased safe area of a device is improved by any change that reduces current concentration. This includes device design factors as well as circuit factors. Regarding device design, safe area is generally improved by increasing base width and/or by increasing emitter area; both changes encourage current spreading. Regarding circuit factors, safe area is improved by reducing the input circuit turn off voltage V_{BB} and/or by increasing the base emitter resistance R_{BE}; both changes reduce the intensity of the transverse base field, thus reducing current concentration. Major improvements in overall power capability can be obtained by providing a clamping circuit which, set to trigger at some value below the breakdown voltage of the transistor, shunts current away from the transistor during turn off.

Specification of Reverse Bias Safe Area

Reverse biased safe area is usually specified in terms of the total energy that can be safely dissipated during turn off. A typical rating is: E_{SB} = 8.0 mJ, I = 4 A, L = 1 mH, R_{BE} = 100Ω, and V_{BB} = −2 V. This rating means that, for the specified values of L, R_{BE}, and V_{BB}, the transistor can safely switch 4 A. E_{SB} stands for "energy of second breakdown" and is equal to the stored inductive energy ½ LI^2 which must be dissipated by the transistor during turn off (note that ½ x 1 mH x (4 A)² = 8 mJ).

SILICON POWER TRANSISTORS

The following lists of preferred power transistors are grouped by package type, from 6 W TO-5 to 200 W TO-3. Within each group, devices are listed in order of increasing breakdown voltage BV_{CEO}.

POWER TRANSISTOR SELECTION CHART

Device	Complement	LV_{CEO} V	$I_{C(max)}$ A	h_{FE} Min-Max	@	I_C A	$V_{CE(sat)}$ Max V	@	I_C A	P_D $T_C = 25°C$ W	f_T Min MHz
PNP TO-220											
2N6132	2N6129	40	7.0	20 - 100	@	2.5	1.4	@	7.0	50	2.5
2N6124	2N6121	45	4.0	25 - 100	@	1.5	0.6	@	1.5	40	2.5
2N6125	2N6122	60	4.0	25 - 100	@	1.5	0.6	@	1.5	40	2.5
2N6133	2N6130	60	7.0	20 - 100	@	2.5	1.4	@	7.0	50	2.5
2N6126	2N6123	80	4.0	20 - 80	@	1.5	0.6	@	1.5	40	2.5
2N6134	2N6131	80	7.0	20 - 100	@	2.5	1.8	@	7.0	50	2.5
NPN TO-3											
2N5067	2N4901	40	5.0	20 - 80	@	1.0	1.5	@	5.0	87.5	4.0
2N4913	2N4904	40	5.0	25 - 100	@	2.5	1.5	@	5.0	87.5	4.0
2N5301	2N4398	40	30.0	15 - 60	@	15.0	2.0	@	20.0	200.0	2.0
2N5068	2N4902	60	5.0	20 - 80	@	1.0	1.5	@	5.0	87.5	4.0
2N4914	2N4905	60	5.0	25 - 100	@	2.5	1.5	@	5.0	87.5	4.0
2N5873	2N5871	60	7.0	20 - 100	@	2.5	1.0	@	4.0	115.0	4.0
2N5877	2N5875	60	8.0	20 - 100	@	4.0	1.0	@	5.0	150.0	4.0
2N3713	2N3789	60	10.0	25 - 90	@	1.0	1.0	@	5.0	150.0	2.5
2N3715	2N3791	60	10.0	50 - 150	@	1.0	0.8	@	5.0	150.0	2.5
2N5881	2N5879	60	12.0	20 - 100	@	6.0	1.0	@	7.0	160.0	4.0
2N3055	—	60	15.0	20 - 70	@	4.0	1.1	@	4.0	117.0	0.8
2N5885	2N5883	60	20.0	20 - 100	@	10.0	1.0	@	15.0	200.0	4.0
2N5302	2N4399	60	30.0	15 - 60	@	15.0	2.0	@	20.0	200.0	2.0
2N5069	2N4903	80	5.0	20 - 80	@	1.0	1.5	@	5.0	87.5	4.0
2N4915	2N4906	80	5.0	25 - 100	@	2.5	1.5	@	5.0	87.5	4.0
2N5874	2N5872	80	7.0	20 - 100	@	2.5	1.0	@	4.0	115.0	4.0
2N5878	2N5876	80	8.0	20 - 100	@	4.0	1.0	@	5.0	150.0	4.0
2N3714	2N3790	80	10.0	25 - 90	@	1.0	1.0	@	5.0	150.0	2.5
2N3716	2N3792	80	10.0	50 - 150	@	1.0	0.8	@	5.0	150.0	2.5
2N5882	2N5880	80	12.0	20 - 100	@	6.0	1.0	@	7.0	160.0	4.0
2N5886	2N5884	80	20.0	20 - 100	@	10.0	1.0	@	15.0	200.0	4.0
2N5303	—	80	30.0	15 - 60	@	10.0	2.0	@	20.0	200.0	2.0
FT410	—	200	7.5	30 - 90	@	1.0	5.0	@	7.5	100	5.0
FT411	—	300	7.5	30 - 90	@	1.0	5.0	@	7.5	100	5.0
FT401	—	400	2.0	20 - 100	@	5.0	0.8	@	0.5	100	2.0
FT402	—	400	2.0	20 - 100	@	5.0	2.0	@	3.0	100	2.0
FT413	—	400	7.5	20 - 80	@	0.5	0.8	@	0.5	100	5.0
FT423	—	400	7.5	30 - 90	@	1.0	0.8	@	1.0	100	5.0
FT430	—	400	10.0	15 - 45	@	2.5	0.9	@	2.5	125	5.0
FT431	—	400	10.0	15 - 35	@	2.5	0.7	@	2.5	125	5.0
PNP TO-3											
2N4901	2N5067	40	5.0	20 - 80	@	1.0	1.5	@	5.0	87.5	4.0
2N4904	2N4913	40	5.0	25 - 100	@	2.5	1.5	@	5.0	87.5	4.0
2N4907	—	40	10.0	20 - 80	@	4.0	2.0	@	10.0	150.0	4.0
2N4398	2N5301	40	30.0	15 - 60	@	15.0	2.0	@	20.0	200.0	4.0
2N4902	2N5068	60	5.0	20 - 80	@	1.0	1.5	@	5.0	87.5	4.0
2N4905	2N4914	60	5.0	25 - 100	@	2.5	1.5	@	5.0	87.5	4.0
2N5871	2N5873	60	7.0	20 - 100	@	2.5	1.0	@	4.0	115.0	4.0
2N5875	2N5877	60	8.0	20 - 100	@	4.0	1.0	@	5.0	150.0	4.0
2N3789	2N3713	60	10.0	15 - —	@	3.0	1.0	@	4.0	150.0	4.0
2N4908	—	60	10.0	20 - 80	@	4.0	2.0	@	10.0	150.0	4.0
2N3791	2N3715	60	10.0	50 - 150	@	1.0	1.0	@	5.0	150.0	4.0
2N5879	2N5881	60	12.0	20 - 100	@	6.0	1.0	@	7.0	160.0	4.0
2N5883	2N5885	60	20.0	20 - 100	@	10.0	1.0	@	15.0	200.0	4.0
2N4399	2N5302	60	30.0	15 - 60	@	15.0	2.0	@	20.0	200.0	4.0
2N4903	2N5069	80	5.0	20 - 80	@	1.0	1.5	@	3.0	87.5	4.0
2N4906	2N4915	80	5.0	25 - 100	@	2.5	1.5	@	5.0	87.5	4.0
2N5872	2N5874	80	7.0	20 - 100	@	2.5	1.0	@	4.0	115.0	4.0
2N5876	2N5878	80	8.0	20 - 100	@	4.0	1.0	@	5.0	150.0	4.0
2N3790	2N3714	80	10.0	25 - 90	@	1.0	1.0	@	5.0	150.0	4.0
2N4909	—	80	10.0	20 - 80	@	1.0	2.0	@	10.0	150.0	4.0
2N3792	2N3716	80	10.0	30 - —	@	3.0	1.0	@	5.0	150.0	4.0
2N5880	2N5882	80	12.0	20 - 100	@	6.0	1.0	@	7.0	160.0	4.0
2N5884	2N5886	80	20.0	20 - 100	@	10.0	1.0	@	15.0	200.0	4.0

C

POWER TRANSISTOR SELECTION CHART

Device	Complement	LV_{CEO} V	$I_{C(max)}$ A	h_{FE} Min-Max	@	I_C A	$V_{CE(sat)}$ Max V	@	I_C A	P_D $T_C = 25°C$ W	f_T Min MHz
NPN TO-5											
2N4237	2N4234	40	1.0	30 - 150	@	0.25	0.6	@	1.00	6	2
2N5321	2N5323	50	2.0	40 - 250	@	0.50	0.8	@	0.50	10	50
2N5334	–	60	3.0	30 - 150	@	1.00	0.7	@	2.00	6	40
2N4238	2N4235	60	1.0	30 - 150	@	0.25	0.6	@	1.00	6	2
2N4895	–	60	5.0	40 - 120	@	2.00	1.0	@	5.00	7	50
2N4896	–	60	5.0	100 - 300	@	2.00	1.0	@	5.00	7	80
2N5320	2N5322	75	2.0	30 - 130	@	0.50	0.5	@	0.50	10	50
2N4239	2N4236	80	1.0	30 - 150	@	0.25	0.6	@	1.00	6	2
2N5335	–	80	3.0	30 - 150	@	1.00	0.7	@	2.00	6	40
2N4897	–	80	5.0	40 - 120	@	2.00	1.0	@	5.00	7	50
2N5336	–	80	5.0	30 - 120	@	2.00	0.7	@	2.00	6	30
2N5337	–	80	5.0	60 - 240	@	2.00	0.7	@	2.00	6	30
2N5681	2N5679	100	1.0	40 - 150	@	0.25	1.0	@	0.50	10	30
2N5338	–	100	5.0	30 - 120	@	2.00	0.7	@	2.00	6	30
2N5339	–	100	5.0	60 - 240	@	2.00	0.7	@	2.00	6	30
2N5682	2N5680	120	1.0	40 - 150	@	0.25	1.0	@	0.50	10	30
2N3440	–	250	0.1	40 - 160	@	0.02	0.5	@	0.05	10	15
2N3439	–	350	0.1	40 - 160	@	0.02	0.5	@	0.05	10	15
PNP TO-5											
2N4234	2N4237	40	1.0	30 - 150	@	0.25	0.6	@	1.00	6	3
2N5323	2N5321	50	2.0	40 - 250	@	0.50	1.2	@	0.50	10	50
2N4235	2N4238	60	1.0	30 - 150	@	0.25	0.6	@	1.00	6	3
2N5322	2N5320	75	2.0	30 - 130	@	0.50	0.7	@	0.50	10	50
2N4236	2N4239	80	1.0	30 - 150	@	0.25	0.5	@	1.00	6	3
2N5679	2N5681	100	1.0	40 - 150	@	0.25	1.0	@	0.50	10	30
2N5680	2N5682	120	1.0	40 - 150	@	0.25	1.0	@	0.50	10	30
NPN TO-66											
2N4910	2N4898	40	1.0	20 - 100	@	0.50	0.6	@	1.00	25	3
2N4231	–	40	4.0	25 - 100	@	1.50	0.7	@	1.50	35	4
2N3054	–	55	4.0	25 - 100	@	0.50	1.0	@	0.50	25	1
2N4911	2N4899	60	1.0	20 - 100	@	0.50	0.5	@	1.00	25	3
2N3766	–	60	3.0	40 - 160	@	0.50	1.0	@	0.50	20	10
2N4232	–	60	4.0	25 - 100	@	1.50	0.7	@	1.50	35	4
2N4912	2N4900	80	1.0	20 - 100	@	0.50	0.6	@	1.00	25	3
2N3767	–	80	3.0	40 - 100	@	0.50	1.0	@	0.50	20	10
2N4233	–	80	4.0	25 - 100	@	1.50	0.7	@	1.50	35	4
2N6233	–	225	5.0	25 - 125	@	1.00	0.5	@	1.00	50	20
2N6234	–	275	5.0	25 - 125	@	1.00	0.5	@	1.00	50	20
SE9051	–	275	10.0	20 - 100	@	1.00	1.0	@	5.00	50	20
2N6235	–	325	5.0	25 - 125	@	1.00	0.5	@	1.00	50	20
SE9052	–	325	10.0	20 - 100	@	1.00	1.0	@	5.00	50	20
PNP TO-66											
2N4898	2N4910	40	1.0	20 - 100	@	0.50	0.6	@	1.00	25	3
2N4899	2N4911	60	1.0	20 - 100	@	0.50	0.6	@	1.00	25	3
2N3740	–	60	1.0	30 - 100	@	0.25	0.6	@	1.00	25	4
2N4900	2N4912	80	1.0	20 - 100	@	0.50	0.6	@	1.00	25	3
2N3741	–	80	1.0	30 - 100	@	0.25	0.6	@	1.00	25	4
NPN TO-220											
2N6129	2N6132	40	7.0	20 - 100	@	2.5	1.4	@	7.0	50	2.5
2N6121	2N6124	45	4.0	25 - 100	@	1.5	0.6	@	1.5	40	2.5
2N6122	2N6125	60	4.0	25 - 100	@	1.5	0.6	@	1.5	40	2.5
2N6130	2N6133	60	7.0	20 - 100	@	2.5	1.4	@	7.0	50	2.5
SE9300	–	60	10.0	1000	@	4.0	2.0	@	4.0	70	1.0
SE9303	–	60	10.0	1000	@	4.0	2.0	@	4.0	100	1.0
2N6123	2N6126	80	4.0	20 - 80	@	1.5	0.6	@	1.5	40	2.5
2N6131	2N6134	80	7.0	20 - 100	@	2.5	2.0	@	7.0	50	2.5
SE9301	–	80	10.0	1000	@	4.0	2.0	@	4.0	70	1.0
SE9304	–	80	10.0	1000	@	4.0	2.0	@	4.0	100	1.0
SE9302	–	100	10.0	1000	@	4.0	2.0	@	4.0	70	1.0
SE9305	–	100	10.0	1000	@	4.0	2.0	@	4.0	100	1.0

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