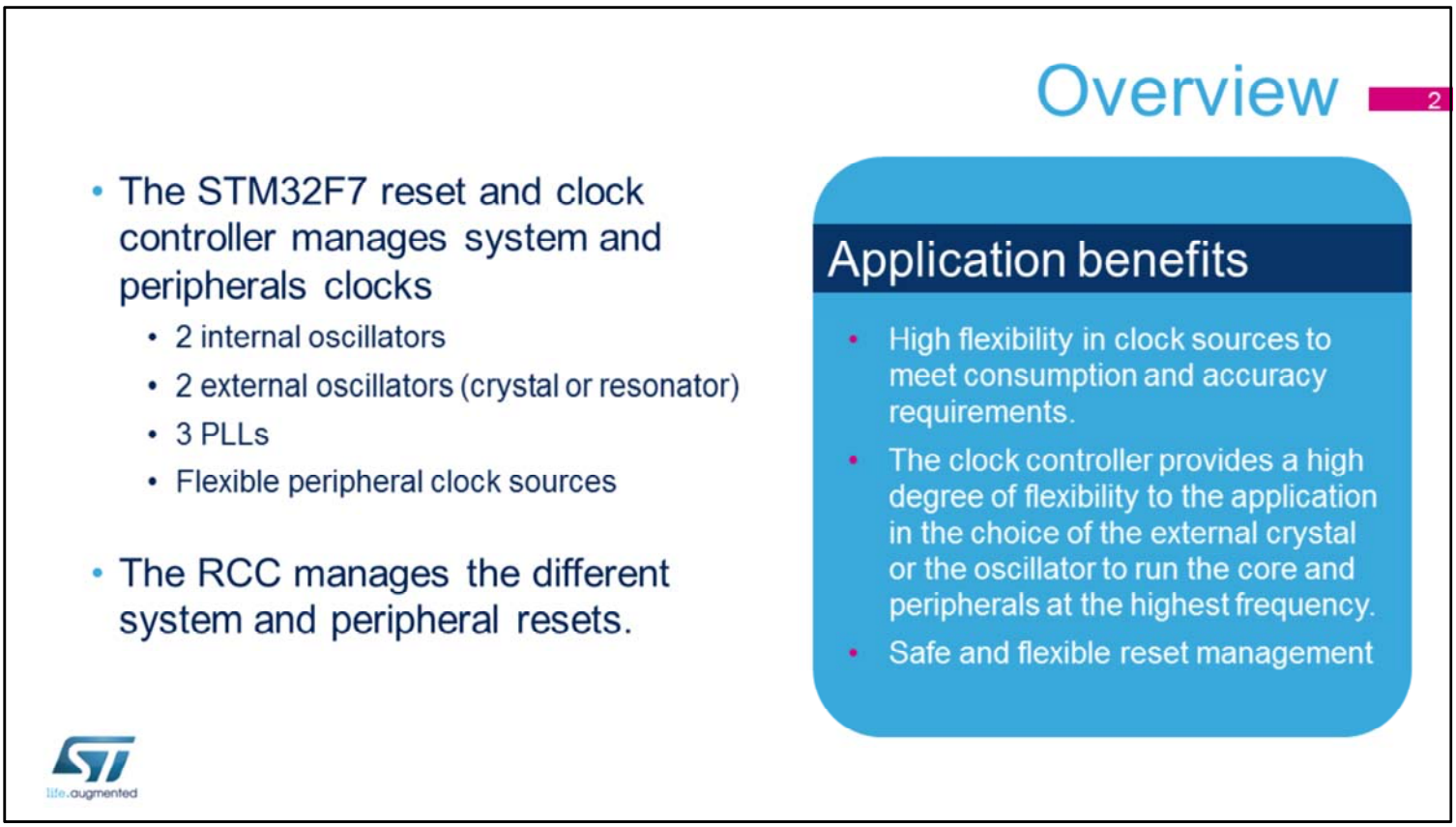
Hello, and welcome to this presentation of the STM32 Reset and Clock Controller.



The RCC controller integrated inside STM32 products manages system and peripheral clocks.
STM32F7 devices embed two internal oscillators, 2 oscillators for an external crystal or resonator, and three phase-locked loops (PLL).
Many peripherals have their own clock, independent of the system clock.
The RCC also manages the various resets present in the device.
The STM32F7 RCC provides high flexibility in the choice of clock sources, which allows the system designer to meet both power consumption and accuracy requirements.
The independent peripheral clocks allow a designer to adjust the system power consumption without impacting the communication baud rates. Finally, the RCC provides safe and flexible reset management.

Reset key features

Safe and flexible reset management without external components

- Manages three types of reset
  - System reset
  - Power reset
  - Backup domain reset
- Peripherals have individual reset control bits

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Safe and flexible reset management without any need for external components reduces application costs.
The RCC manages three types of resets: the system reset, the power reset and the backup domain reset.
The peripherals have individual reset control bits.

Reset sources

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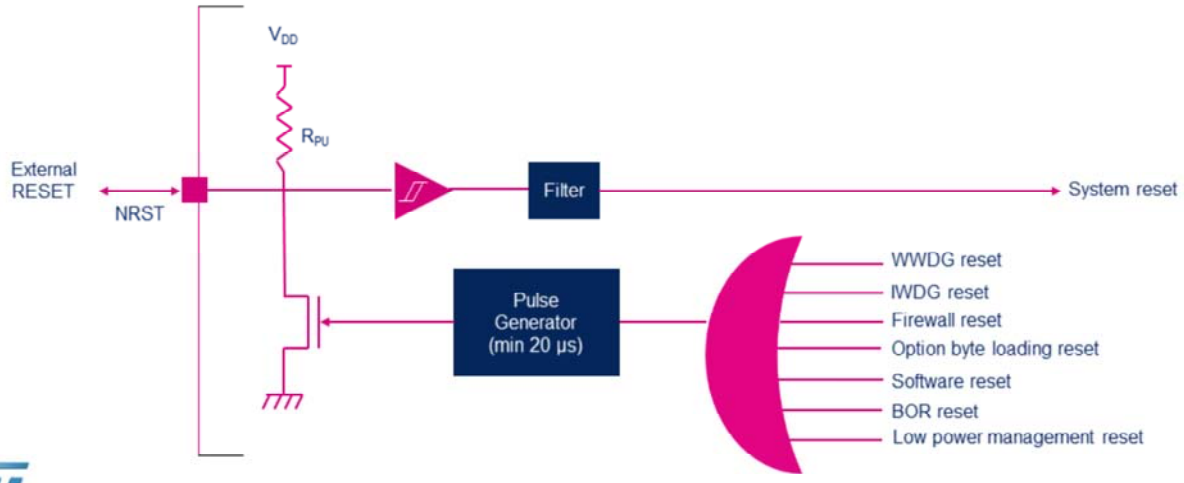
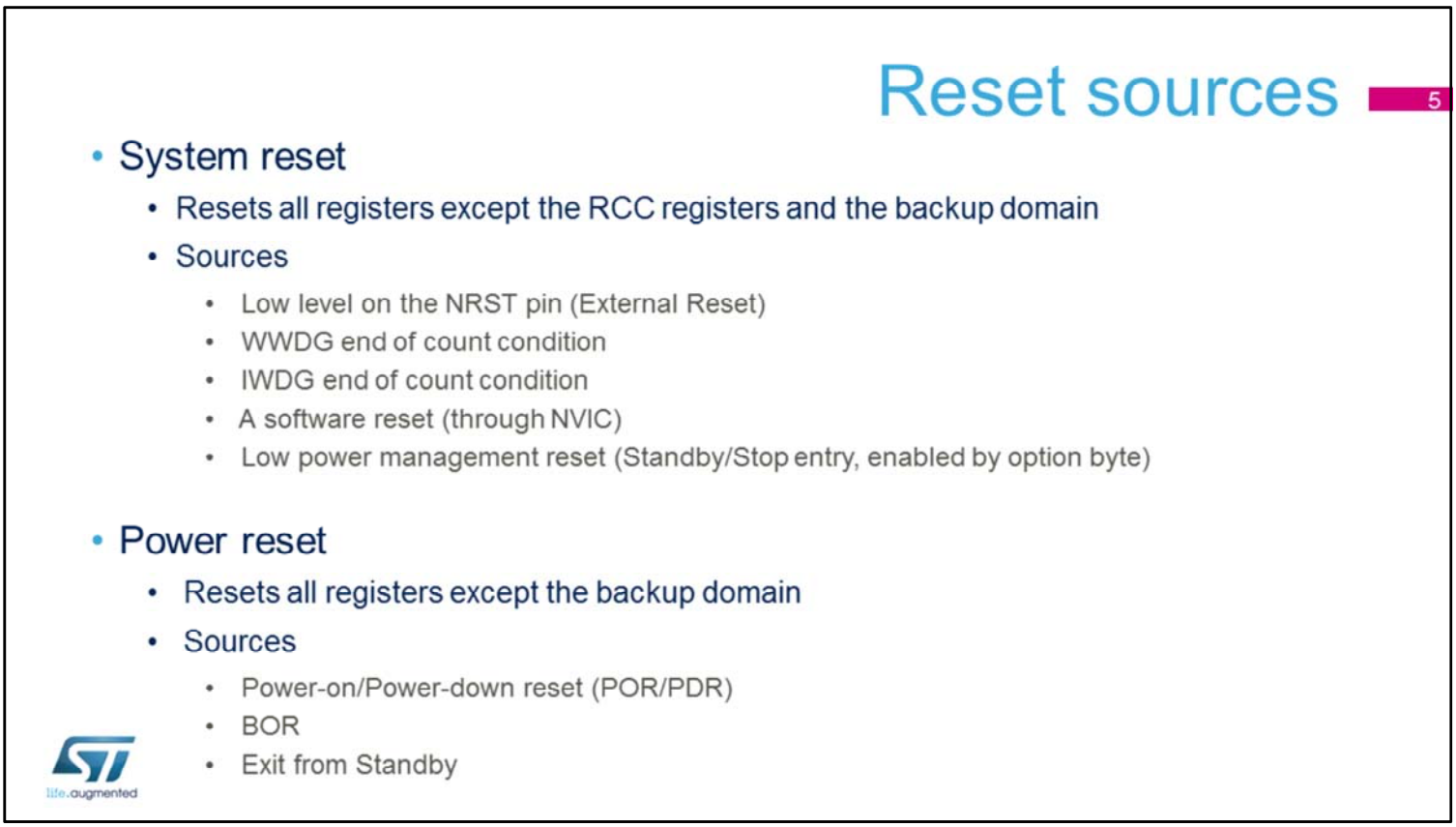
No external components needed thanks to internal filter and power monitoring

Internal reset sources can reset whole application



Here is the simplified block diagram of the system reset. All internal reset sources provide a reset signal on the NRST pin, which can be used to reset other components of the application board. In addition, no external reset circuitry is needed due to the internal glitch filter and the safe power monitoring feature which guarantees the reset of the application when VDD is below the selected threshold.

An internal pull-up on the NRST pin, allows to maintain a high level when no reset signal is driven low.



The first type of reset is the system reset, which resets all the registers except certain registers for the Reset and Clock Controller. It also does not reset the backup domain.
The system reset sources are the external reset (generated by a low level on the NRST pin), a window watchdog event, an independent watchdog event, a software event through the Nested Vectored Interrupt Controller, a low-power-mode security reset (which is generated when Stop or Standby mode is entered but is prohibited by the option byte configuration). The reset source flag can be found in the RCC Control and Status register.

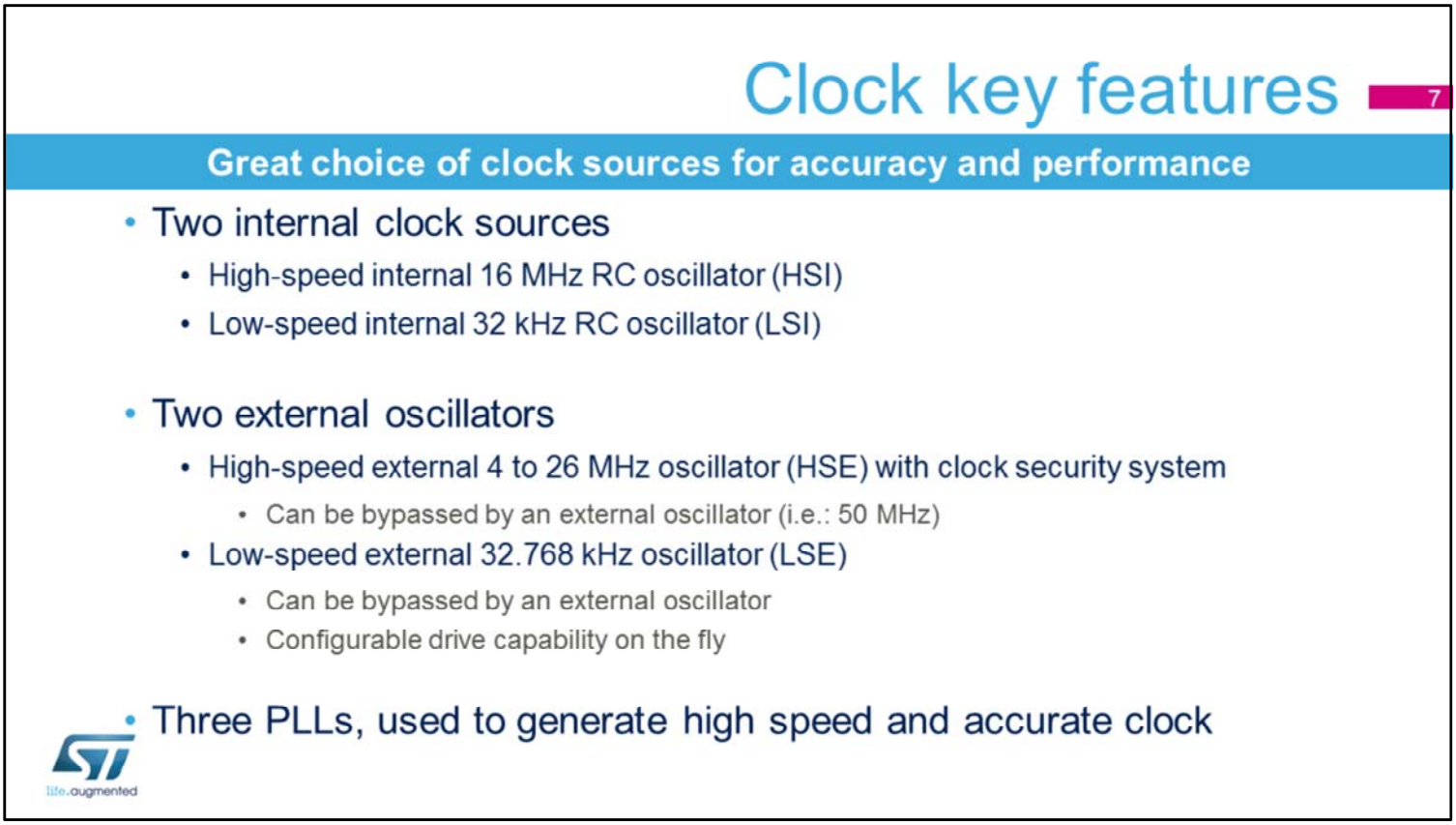
The second type of reset is the power reset. The Brown-out reset (BOR) resets all registers except those in the Backup domain powered by VBAT which contains the

RTC and the external low-speed oscillator.
When exiting Standby mode, all registers powered by the regulator are reset. When exiting Standby mode, a reset is generated.

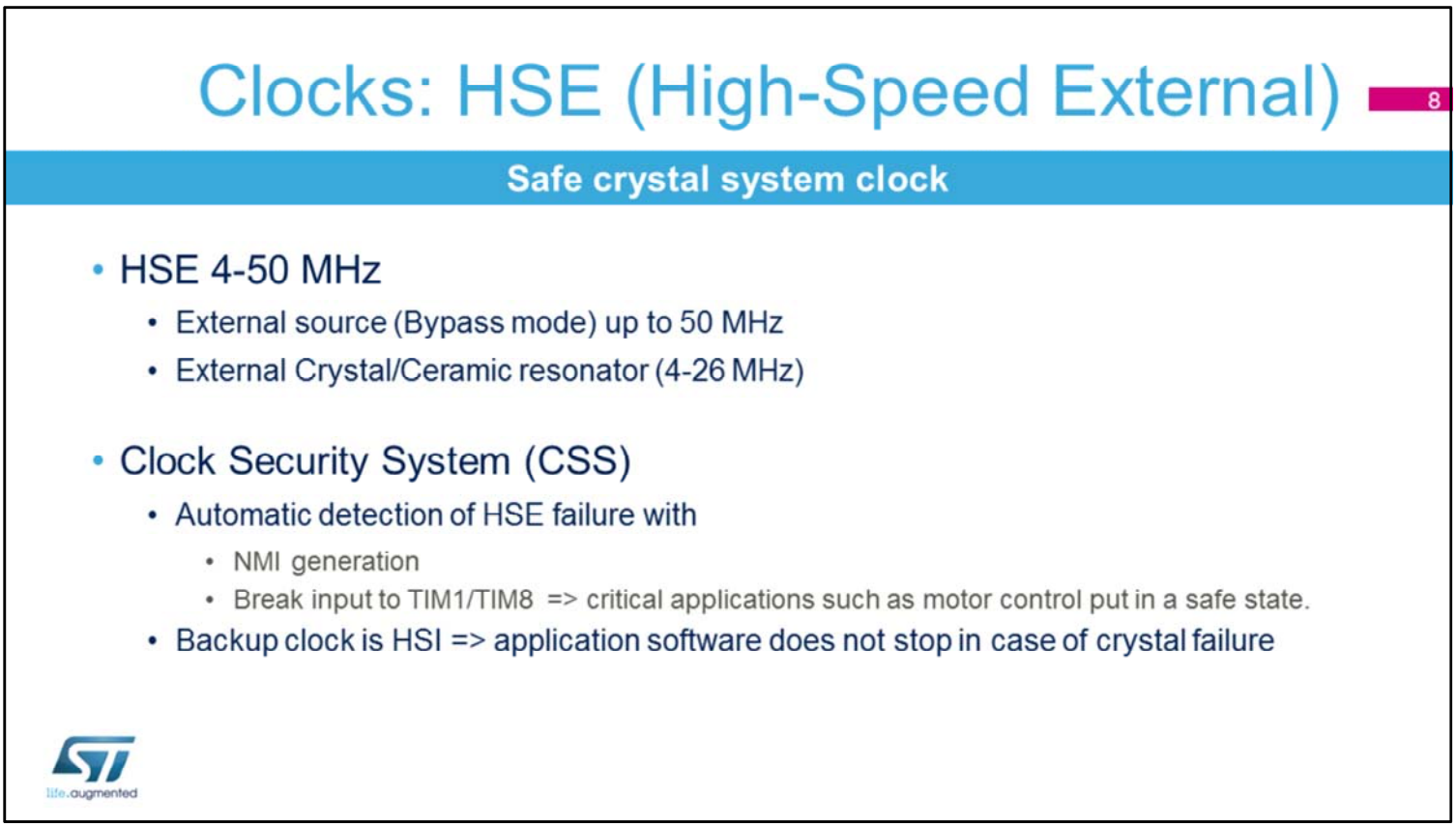
Reset sources

- Backup domain reset
  - Resets in the backup domain: RTC registers + Backup registers + RCC BDCR register
  - Sources
    - BDRST bit in RCC BDCR register set by software
    - VBAT and VDD power-on reset

The third type of reset is the backup domain reset, which resets the RTC registers, the Backup registers, and the RCC Backup Domain Control Register. This reset occurs when the BDRST bit is set in the RCC Backup Domain control register.
It also occurs when VDD and VBAT are powered on if both supplies have previously been powered off.



The RCC offers a large choice of clock sources, which can be selected depending on low-power, accuracy, and performance requirements.
STM32F7 devices embed two internal clock sources: a high-speed internal 16 MHz RC oscillator (HSI), and a low-speed internal 32 kHz RC oscillator (LSI).
STM32F7 devices embed two oscillators for use with an external crystal or resonator: a high-speed external 4 to 26 MHz oscillator (HSE) with a clock security system and a low-speed external 32.768 kHz oscillator (LSE) also with a clock security system.
STM32F7 devices embed three phase-locked loops, each with three independent outputs for clocking different peripherals at different frequencies.



The high-speed internal oscillator is a 16 MHz RC oscillator which provides 1% accuracy and fast wakeup times. The HSI is trimmed during production testing, and can also be user-trimmed.

The HSI is selected as clock at wakeup from Stop mode, and as the backup clock if an HSE failure is detected by the Clock Security System.

If an HSE failure is detected, the Clock Security System allows to put system in safe state by generating break events to critical applications such as motor control.

Clocks: LSE (Low-Speed External)

32.768 kHz configurable for low-power or high-drive
Available in all modes and in VBAT

- The LSE can be used with an external quartz or resonator, or with an external clock source in bypass mode
- LSE oscillator drive capability programmable on the fly
- The LSE can be used for RTC, U(S)ARTs, LPTIM, HDMI-CEC

LSE drive	Added consumption (µA)
Medium-low drive vs Low drive	0.02
Medium-high drive vs Medium-low drive	0.14
High drive vs Medium-high drive	0.09
High drive vs Low drive	0.23

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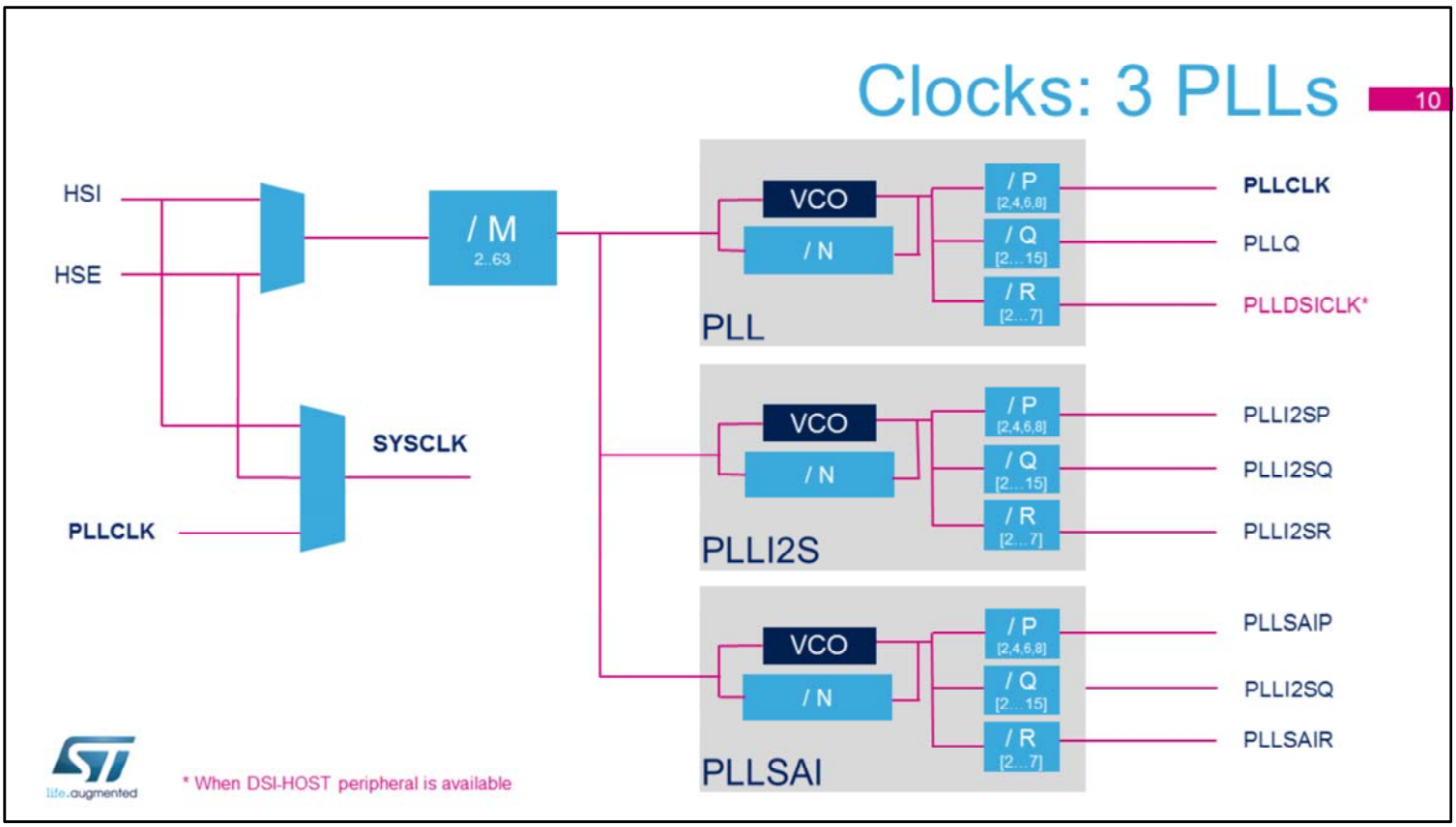
The 32.768 kHz low-speed external oscillator can be used with external quartz or resonator, or with an external clock source in bypass mode.
The oscillator driving capability is programmable. Four modes are available, from ultra-low power mode, to high-driving mode.
The LSE can be used to clock the RTC, the low-power timer, the HDMI-CEC interface, and the USARTs peripherals.



STM32F7 devices embed 3 phase-locked loops, each with 3 independent outputs. The input clock of the PLL can be selected between HSI and HSE.
The main PLL can provide the system clock.
The different PLL outputs can be used for the serial audio interfaces, USB, Random Number Generator, SDMMC peripherals and LTDC/ and DSI-HOST interfaces when available.

System clock

- Selected between HIS, HSE, or PLL
- Maximum frequency 216 MHz, APB1 & APB2 up to 54 MHz and 108 MHz respectively
- Maximum clock source frequency depends on voltage scaling:

Voltage scale	Max HCLK frequency Over-Drive OFF	Max HCLK frequency Over-Drive ON
Scale 3	144 MHz	--
Scale 2	168 MHz	180 MHz
Scale 1	180 MHz	216 MHz

The system clock is selected between the HSI, HSE and PLL output.
The maximum system clock frequency is 216 MHz. The APB1 and APB2 bus frequencies are also up to 54 MHz. and 108 MHz respectively
The maximum clock source frequency depends on the voltage scaling. The maximum system clock is reached with voltage scale 1 and when enabling Over-Drive. When Over-Drive is off, the maximum system clock frequency is 180MHz.

Peripheral clock sources summary

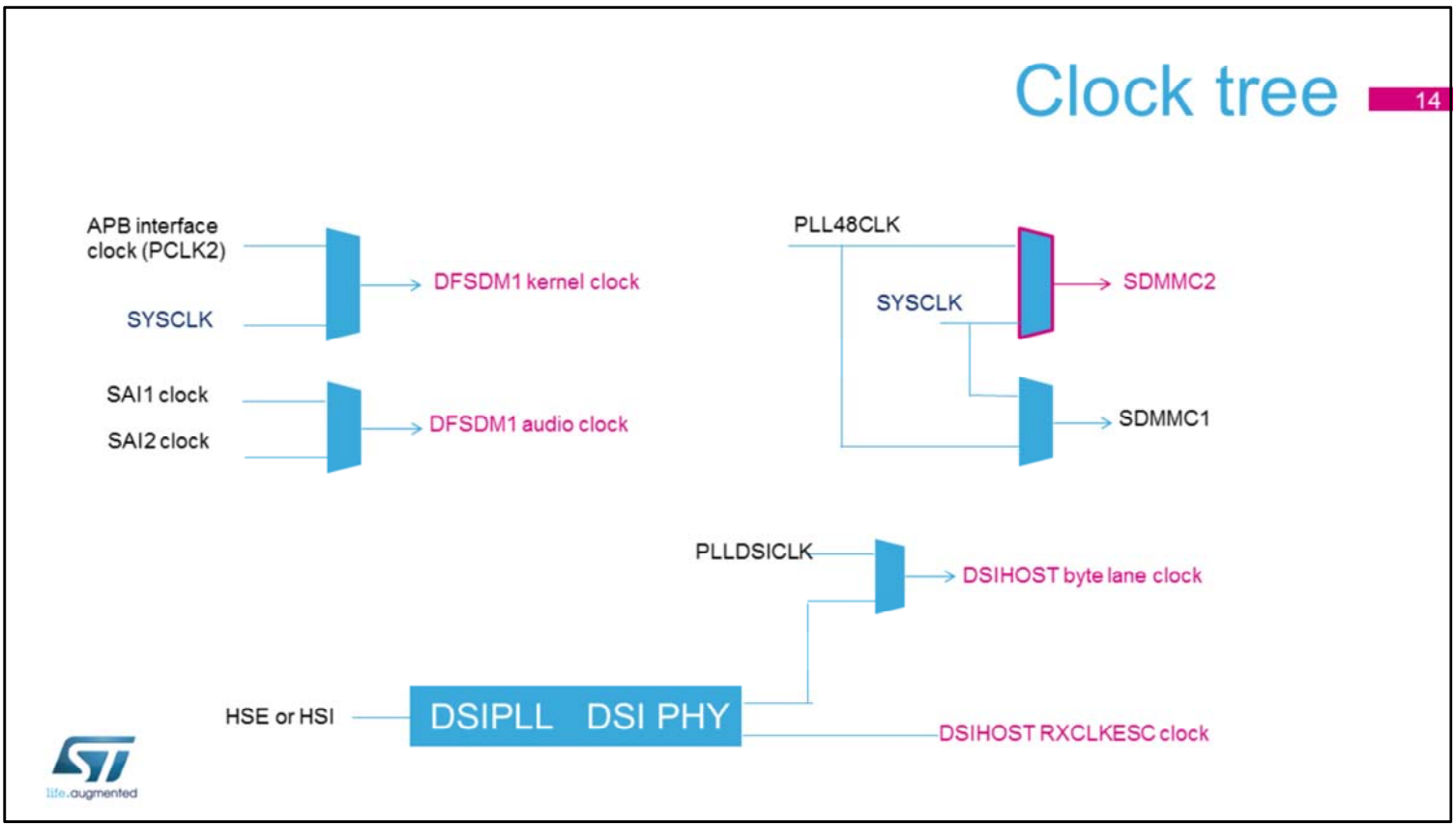
- U(S)ARTs:
  - System clock (SYSCLK)
  - HSI clock
  - LSE clock
  - PCLK1 or PCLk2 clock
- I2Cx:
  - System clock (SYSCLK)
  - HSI clock
  - PCLK1 clock
- LPTIM1:
  - LSI clock
  - LSE clock
  - HSI clock
  - APB1 clock (PCLK1)
  - External clock mapped on LPTIM1_IN1
- The HDMI-CEC clock:
  - LSE clock
  - HSI clock divided by 488
- The RTC clock:
  - LSE clock
  - LSI clock
  - HSE clock divided by 32
- The IWDG clock is always the LSI clock
- The USB OTG HS (60 MHz) clock is provided from the external PHY
- The Ethernet MAC clocks (TX, RX and RMII) which are provided from the external PHY.

Several peripherals have their own clock independent from the system clock. This is the case for the USARTs, I2Cs, low-power timer, HDMI-CEC interface, independent watchdog, USB OTG HS external PHY clock and Ethernet MAC clocks (when available in the device package). All of these clocks can be selected from the internal/external oscillators' dedicated external clock pin or bus interface clocks.

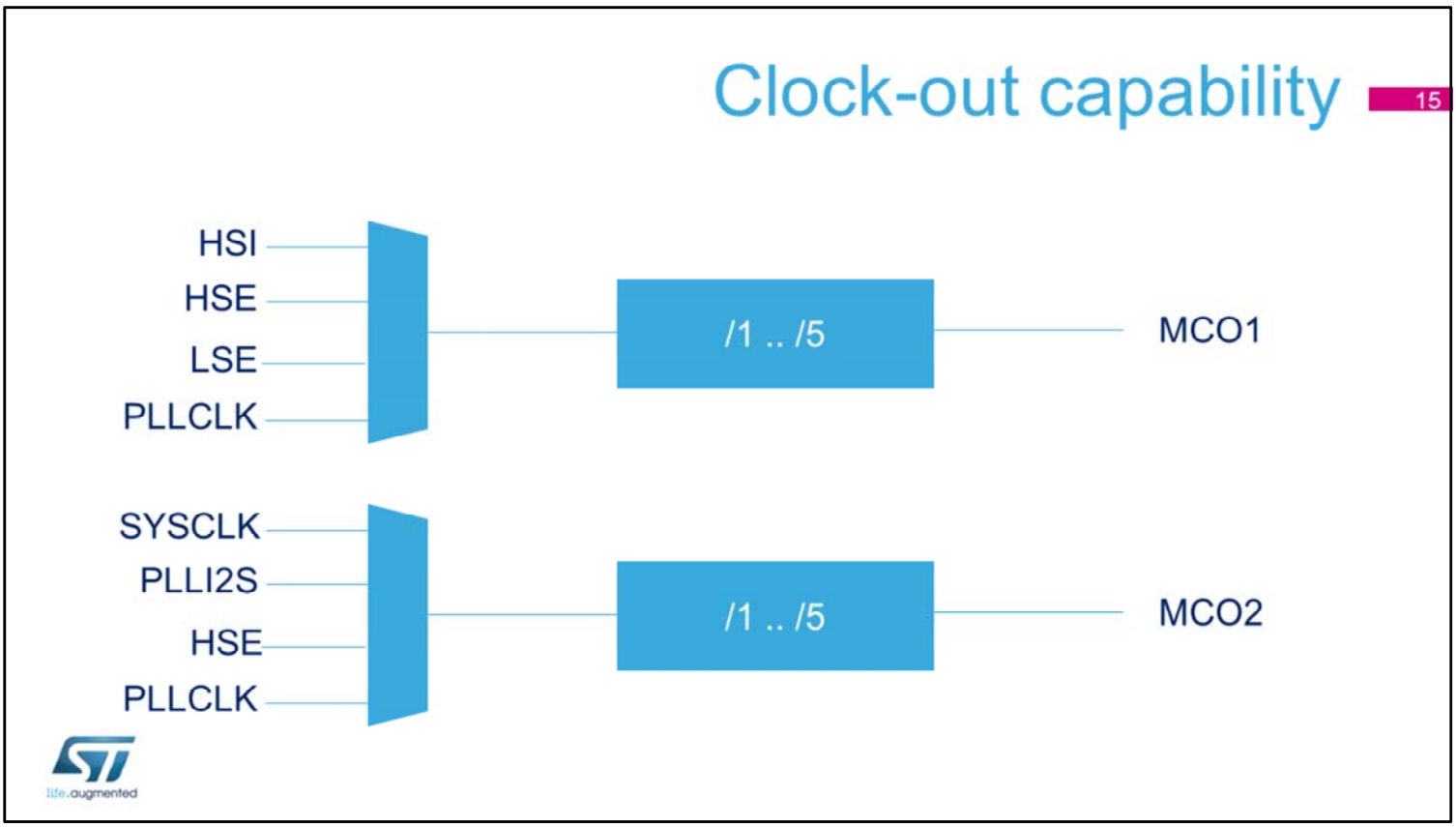
Peripheral clock sources summary

- 48 MHz clock for USB OTG FS, SDMMC1/2 and RNG:
  - Main PLL VCO (PLLQ clock)
  - or PLLSAI VCO (PLLSAI clock)
- SAI1 and SAI2 clock:
  - PLLSAI VCO (PLLSAIQ)
  - or PLLI2S VCO (PLLI2SQ)
  - or External clock mapped on the I2S_CKIN pin
  - or HSI/HSE (PLL source clock) (not available on all F7 devices)

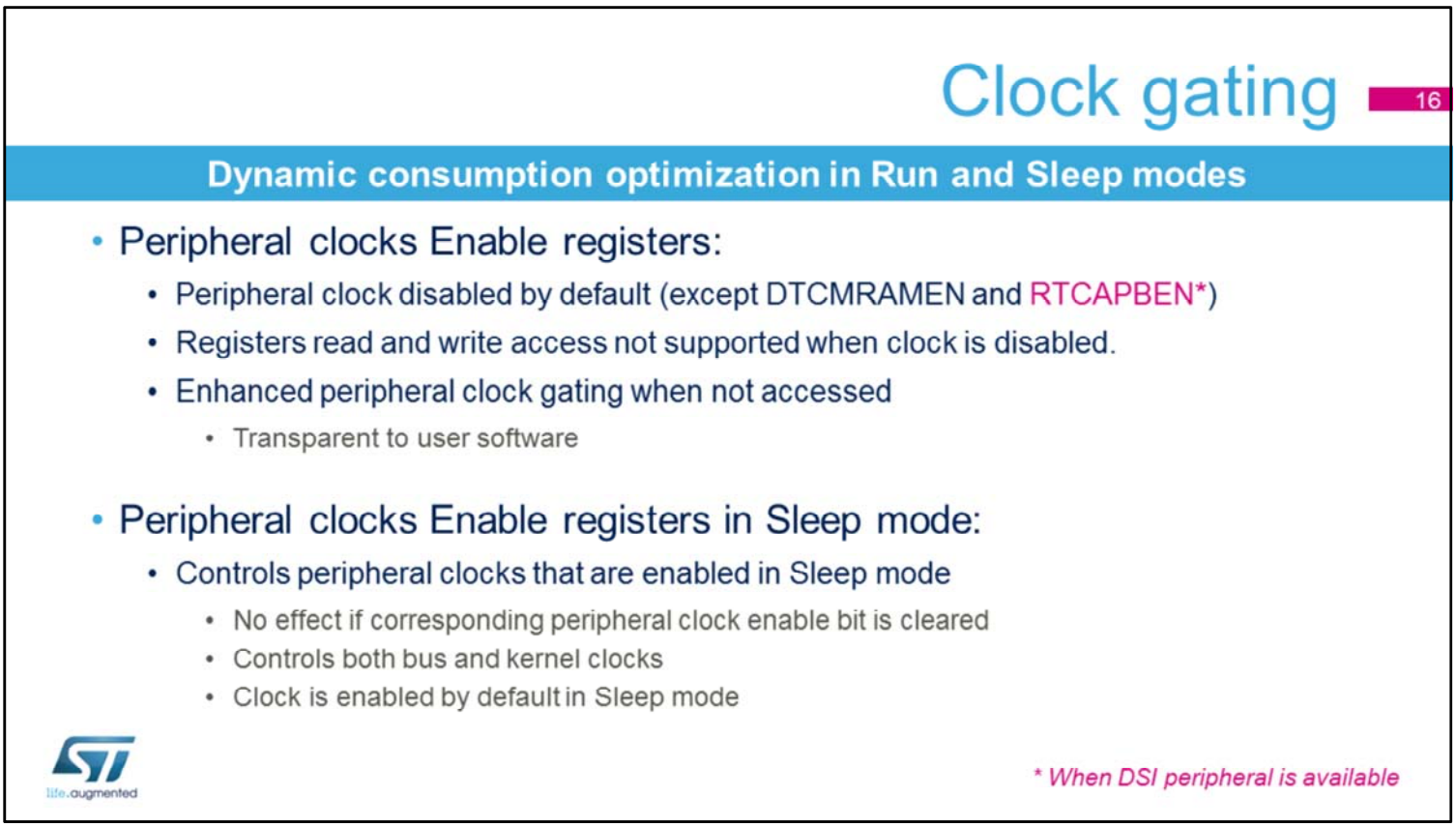
Serial audio interfaces, USB OTG FS, random number generator, and SDMMC interfaces have independent clock sources that are generated from the different PLL outputs.
In addition to PLL outputs the serial audio interfaces clock can be generated from External clock mapped on the I2S_CKIN pin or from HSI/HSE clocks if this feature is available.



Several peripherals available only on some F7 device part numbers, such as the DFSDM1 interface, the SDMMC2 interface and the DSI-HOST interface have dedicated input clock sources. The clocks are derived from PLL outputs or from system clocks.
In addition to PLL outputs, the DSI-HOST interface clock can be generated from its own PLL.



The various clocks can be output on an I/O. The Microcontroller Clock Output feature allows you to output on a pin one of these six clocks: HSI, HSE, LSE, SYSCLK, PLLCLK, and PLLI2S.



The dynamic power consumption can be optimized by using peripheral clock gating.
Each peripheral clock can be gated ON or OFF in Run and Sleep mode, except SRAM and FLASH which are always clocked in Run and Sleep modes. By default, the peripheral's clock is disabled, except the DTCMRAM clock and RTC interface clock which are enabled by default. When a peripheral's clock is disabled, the peripheral's registers cannot be read or written.
Dedicated registers allow for configuring the peripheral's clock during the Sleep mode. These control bits have no effect if the corresponding peripheral clock is disabled.

Interrupts

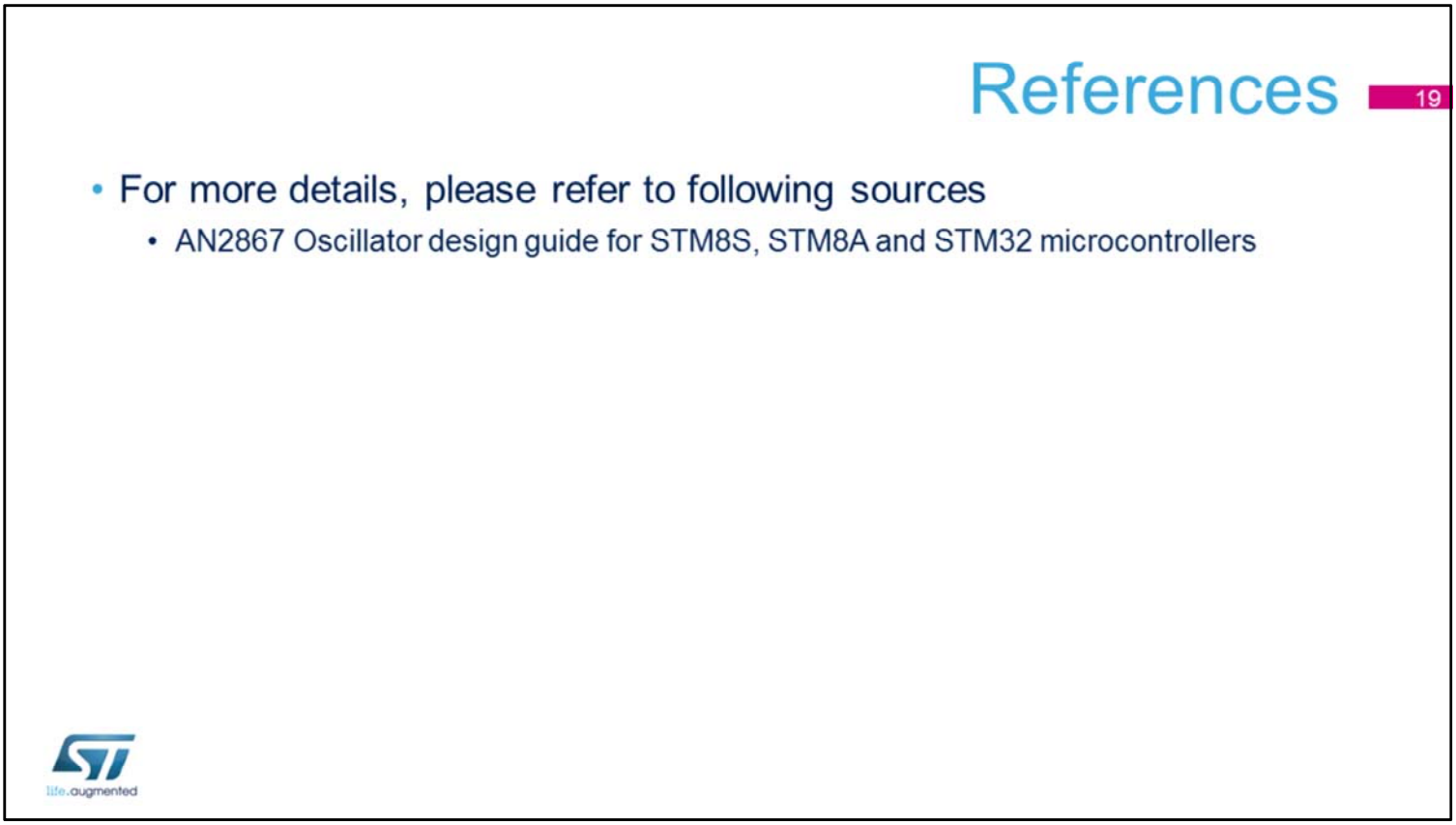
Interrupt event	Description
PLLSAI ready interrupt flag	Clock ready caused by PLLSAI lock
PLLI2S ready interrupt flag	Clock ready caused by PLLI2S lock
PLL ready interrupt flag	Clock ready caused by PLL lock
HSE ready	Clock ready caused by the HSE oscillator
HSI ready	Clock ready caused by the HSI oscillator
LSE ready	Clock ready caused by the LSE oscillator
LSI ready	Clock ready caused by the LSI oscillator

This slide lists the RCC interrupts. The PLLs ready and all oscillators ready signals can generate an interrupt.

Related peripherals

- Refer to these trainings related to this peripheral:
  - STM32F7 Power control (PWR)
  - STM32F7 Interrupts (NVIC-EXTI)

In addition to this training, you may find the Power Control and Interrupt Controller trainings useful.



For more details, please refer to application note AN2867, an oscillator design guide for STM8S, STM8A and STM32 microcontrollers .