Xtrinsic Battery Sensor ICs for Battery Monitoring and Management

AMF-AUT-T1043

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Agenda

- Intelligent Precision Battery Sensors Overview
  - Definition
  - Application Requirements
  - Family Comparison
  - Target Applications
- Hardware Features
  - Overview
  - Acquisition Channels
  - Timers, I/O and Communications
  - Operating Modes & Wakeup
- Trim & Calibration
- Hardware & Software Tools

Intelligent Precision Battery Sensors

Definition –
What is an Intelligent Battery Sensor (IBS)?

- The Intelligent Battery Sensor is a mechatronic device that fits in the terminal recess of standard batteries.
- The extremely low-resistance-shunt of the IBS provides an optimum design from shunt to signal conditioning.
- The sensor is able to measure the battery current within the whole range observable in a car from key-off to cranking.
- It also provides the voltage between the battery poles and the temperature of the negative terminal.
- Due to high acquisition frequency and a specific algorithm, the IBS is able to derive the internal resistance of the battery at the most relevant frequency range.
- The scalable microprocessor concept makes it possible to use either the sensor alone for data acquisition or complete battery diagnostics with the integrated Battery Monitoring Algorithm.

IBS: key application requirements

- Footprint
  - Essential because of the battery housing
  - Requires a single chip integration of all features
- Low power
  - Need a continuous monitoring of the battery
  - Requires typically 100 µA standby overall current consumption
- Automotive robustness
  - PHY layer needs to be automotive certified and accepted by OEMs
  - Due to space constraints, EMC/ESD requirements must be achieved with minimum amount of passive components

Algorithm for IBS: What do we want to monitor ?

- A battery is an electrochemical cell that converts stored chemical energy into electrical energy

- What are the main performances we want to observe?
  - Available capacity at a given time (Is my battery charged ?)
  - Lifetime degradation (Do I need to change my battery?)

- So a typical battery management algorithm will evaluate
  - SoC: indicates ratio between available capacity and max. capacity
  - SoH: describes the decreasing of the maximum capacity of the battery

State of Charge Evaluation: Current Integration Based

- Formula indicating SoC:

$$SoC(t) = \left(\frac{Q(t_0) + \sum_{n=0}^{\infty} \alpha\, i(n)|_{fs}}{C_r}\right) \text{x } 100$$

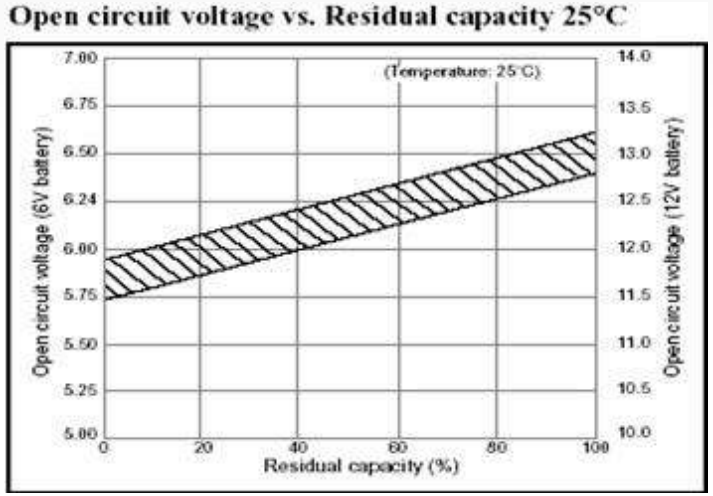
$Q(t_0)$	Initial charge of the battery
α	Efficiency factor; dependent on temperature, current and direction (charge / discharge)
C_r	Rated battery capacity; de-rated over time
fs	Sample frequency

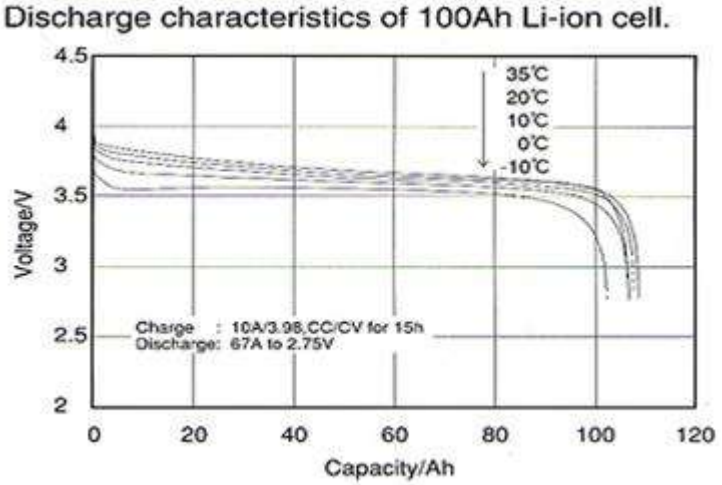
- This method is also known as Coulomb Counting
- Requirements:
  - Strongly depends on current measurement accuracy
  - Implies a known and stable time reference
  - Current must be monitored permanently, in both directions
  - Battery temperature must be known

State of Charge Evaluation: Open Circuit Voltage Based

- Another possibility is to use the relation between SoC and OCV
  - Open Circuit Voltage is defined as the voltage at the battery output, with no load current
- However, a good battery will have a very flat OCV= f(SoC) response

- Requirements
  - Very accurate voltage measurement
  - Measurement only after a given amount of time after latest charge/discharge
  - Temperature measurement





State of Health

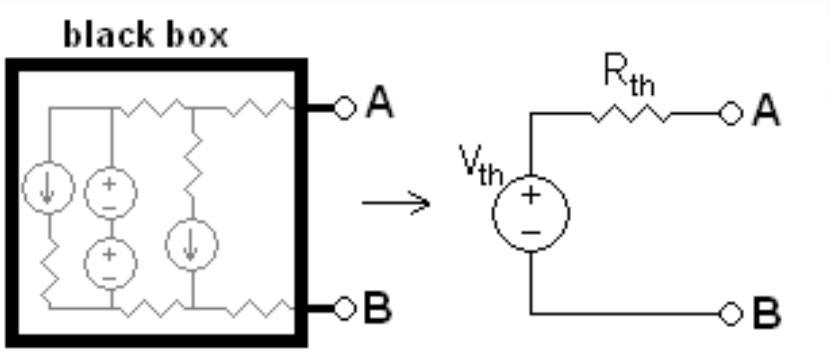
- SoH describes the decreas of the maximum capacity of the battery due to aging.

- As SoC, it can be evaluated in several ways
  - Looking at the maximum SoC reached after consecutive full charge cycles
  - Counting the number of charge/discharge cycles
  - Measuring an electrical parameter well correlated with SoH

- Generally, final algorithm will consider all these evaluations (and some more, depending on the complexity) to determine the SoH

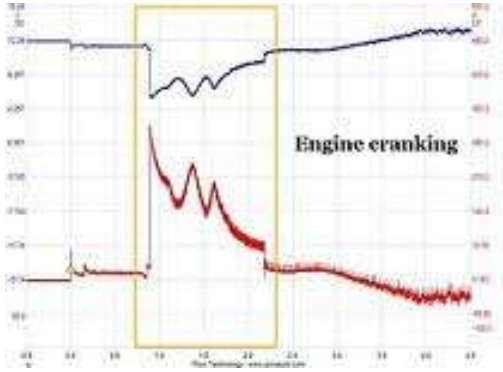
SoH estimation: Internal impedance measurement

- A battery can be modeled with a voltage source and a series impedance
- In particular, internal impedance of a battery does increase with aging
- Cranking condition is the best situation to measure this impedance



Remember Thevenin's theorem !

- Requirements
  - Synchronous measurement of V and I
  - Measure high current peaks
  - Fast sampling rates



Algorithms: summary of requirements

- Strong dependence on current measurement accuracy
- Current must be monitored permanently, in both directions
- Measure high current peaks

- Very accurate voltage measurement
- Measurement only after a given amount of time after latest charge/discharge

- Battery temperature must be known

- Implies a known and stable time reference

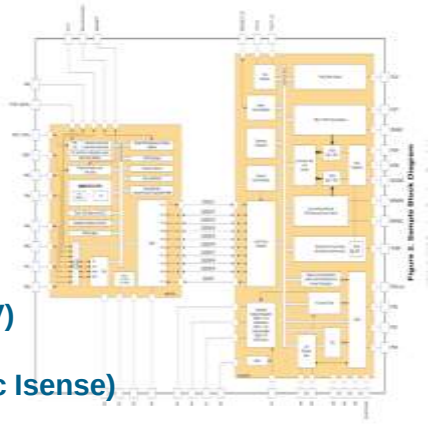
- Synchronous measurement of V and I
- Fast sampling rates (to allow cranking pulse measurements)

Freescale's Intelligent Precision Battery Sensors - Overview

EDN INNOVATION AWARD 创新奖
2011 Leading Product
Mixed Signal Category

AECQ100 Qual

MM912J637 – 12V Pb (LIN)



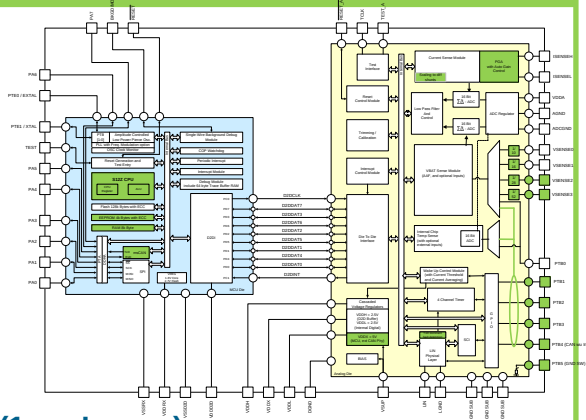
MCU S12 (16-bit)
Flash 96k/128k
Data Flash 4k
RAM 6k

Mixed-Signal Chip
LIN Physical Layer (ESD 15kV)
Watchdog
Standby Current <100µA (1sec Isense)
Vreg capability 50mA
Operating Voltage 3.5..28V
RAM Contents Guaranteed :2.5...3.5V
3x ADC (2nd Order Sigma Delta) 16bit
Current Measurement
Relative Accuracy <0.5%
Voltage Measurement
Relative Accuracy <0.2%
Temperature Measurement
Relative Accuracy <2K
Operating Temperature -40°C<Ta<125°C

48ld 7x7 QFN
w/ wet-able flanks

AECQ100 Qual

MM9Z1J638 – Multi Applications (LIN, msCAN)



MCU S12Z (32-bit ALU)
Flash 96k/128k
EEPROM 4k
RAM 8k
msCAN

Mixed-Signal Chip
LIN Physical Layer
Watchdog
Standby Current <100µA (1sec Isense)
Vreg capability 150mA
Operating Voltage 3.5..28V (Vs3:52V)
RAM Contents Guaranteed :2.5...3.5V
3x ADC (2nd Order Sigma Delta) 16bit
Current Measurement
Relative Accuracy <0.5%
Voltage Measurement
Relative Accuracy <0.15%
Temperature Measurement
Relative Accuracy <2K
Operating Temperature -40°C<Ta<125°C

48ld 7x7 QFN
w/ wet-able flanks

freescale™

Freescale Intelligent Battery Sensors – Feature Comparison

MM912J637AM2

- Application
  - 12V PB Battery (LIN)
- Supply: 12V Vreg
- Communication
  - LIN, SCI, SPI
- Just Enough MCU Performance
- Features
  - Cranking mode
  - 2nd Vsense
  - External Temp sense
- Full Temp Range
  - 40C.. 125C

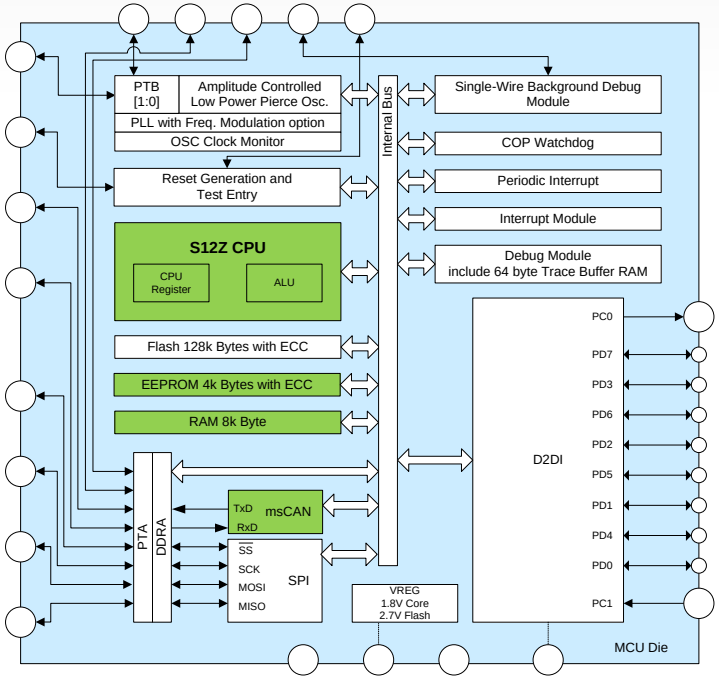
PPAP completed
SOP: 1Q13

MM9Z1J638AM2

- Applications
  - 12V Pb Battery (Lin, CAN), 14V Li-ion Battery, Multi-battery apps, HV Battery Junction Box
- Supply: 12V Vreg
- Communication
  - msCAN,LIN,SCI,SPI
- Higher MCU Performance
- Features
  - Cranking mode
  - 4 attenuated Vsense and 4 direct Voltage Pins
  - 4 External Temp sense
- Full Temp Range
  -40C.. 125C

Final Silicon, PPAP: 4Q13,
SOP: 4Q13

MCU Die - comparison ‘637 vs. ‘638



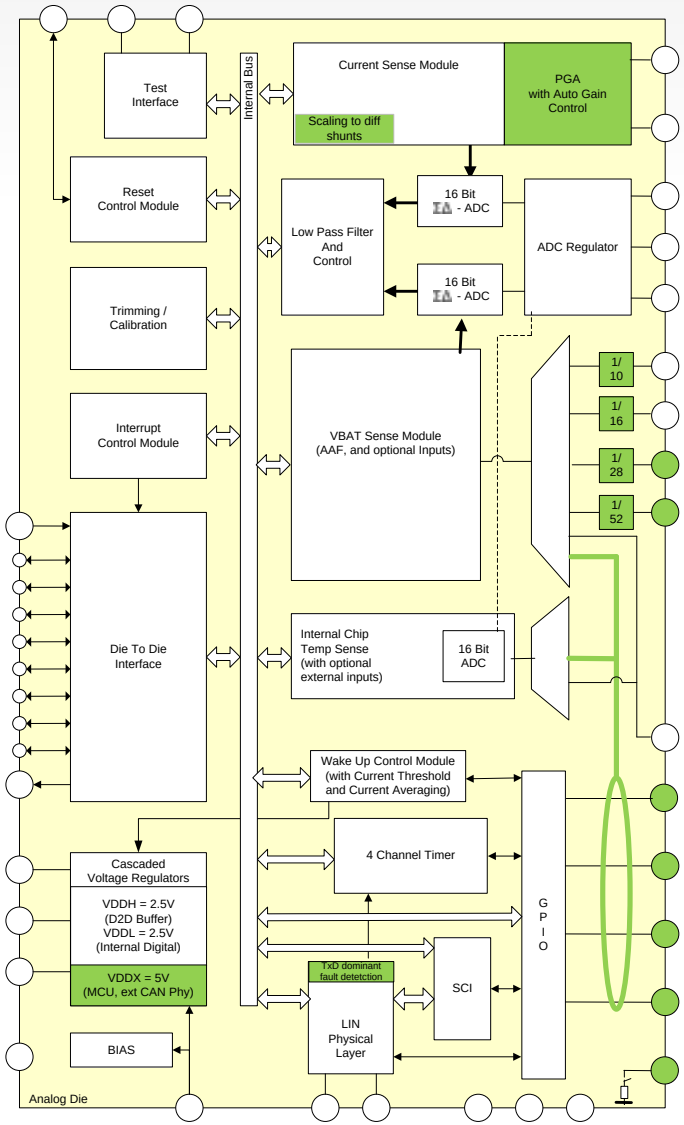
Legend:

Change vs. previous version, Validated on previous silicon /pizza mask

No Change vs. previous version, AEC Q100 qualified

	MCU (637)	MCU (638)	benefit/impact
CPU core	S12I	S12Z	More performance. New compiler, minor SW adoptions needed mainly on linker level. Peripheral SW modules can be reused
Clock Freq	up to 32MHz	up to 50MHz Bus Freq (100MHz CPU)	More performance.
Addressing	paging	linear addressing	simple S/W, faster access
Data Flash/ EEPROM	4k Dataflash with ECC	4k EEPROM with ECC	True EEPROM. Different EEPROM Driver & Data Storage System, Different Flash SW driver (only relevant if programming feature available in boot loader)
RAM	6k	8k with ECC	Extended to 8k, added ECC feature
GPI0 Port A	Yes	**Yes**	added msCAN module
msCAN	no	**Yes**	

Analog Die - comparison ‘637 vs. ‘638



	Analog Die (637)	Analog Die (638)	benefit/impact
Vsense	2 inputs, with attenuation	Extend to 4 inputs with attenuation, and 4 direct inputs without attenuation (external resistor divider)	Extended sense capabilities
Vsup, Vsense max rating	42V	Vsense3 rated 65V, for truck application	Higher rating for truck application
PGA	8 different gains, auto gain switching	Reduced to 4 gains, changed layout to improve noise, auto gain switching	Better accuracy
External Temp sense	1 ext. channel	up to 5 ext channels. Routed via port B	Extended sense capabilities. ADC cross check.
VDDX	5V - 50mA	capability extended to 150mA	CAN phy consumption
Vdda	2.5V, capability less than 2mA	VDD a extended up to 4mA	account for additional ext Temp sensors.
LIN	LIN IP for LIN 2.0 - 2.1 and J2602-1	Latest LIN IP	Added TxD dominant fault detection
GPI0 Port B	4 input ouput ports	Port B extended to 5 pins	Includes CAN wake up, ext Vsense and external T° sense
CAN Wake up	No msCAN	CAN wake up via PTB	

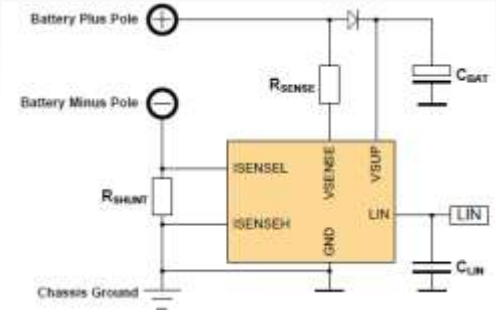
Legend:

Change vs. previous version, Validated on previous silicon /pizza mask

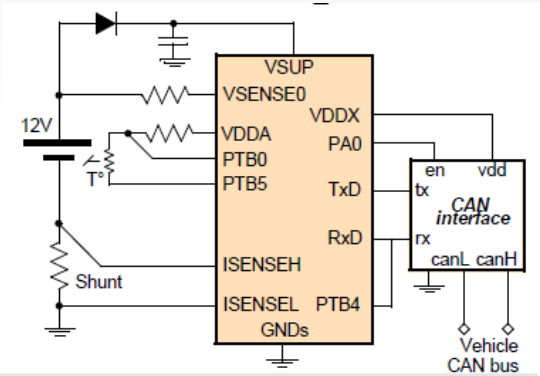
No Change vs. previous version, AEC Q100 qualified

freescale™

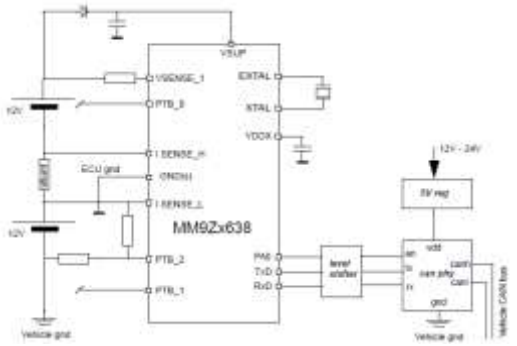
Target Applications



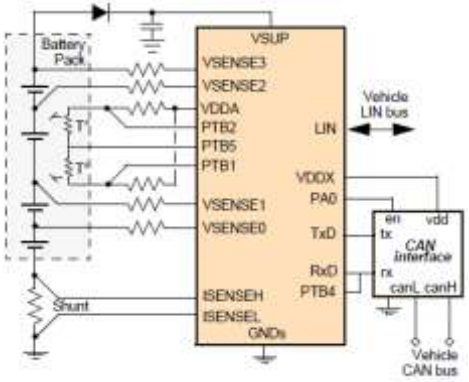
12V PB Battery (LIN)



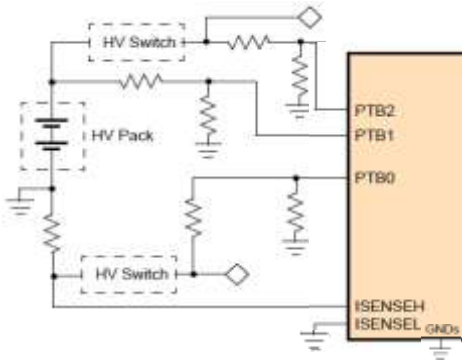
12V PB Battery (CAN)



Multi- Battery



Multiple Cells



HV Battery Junction Box

i.e. 14V 4 cell Li-ion

Hardware Features

Overview

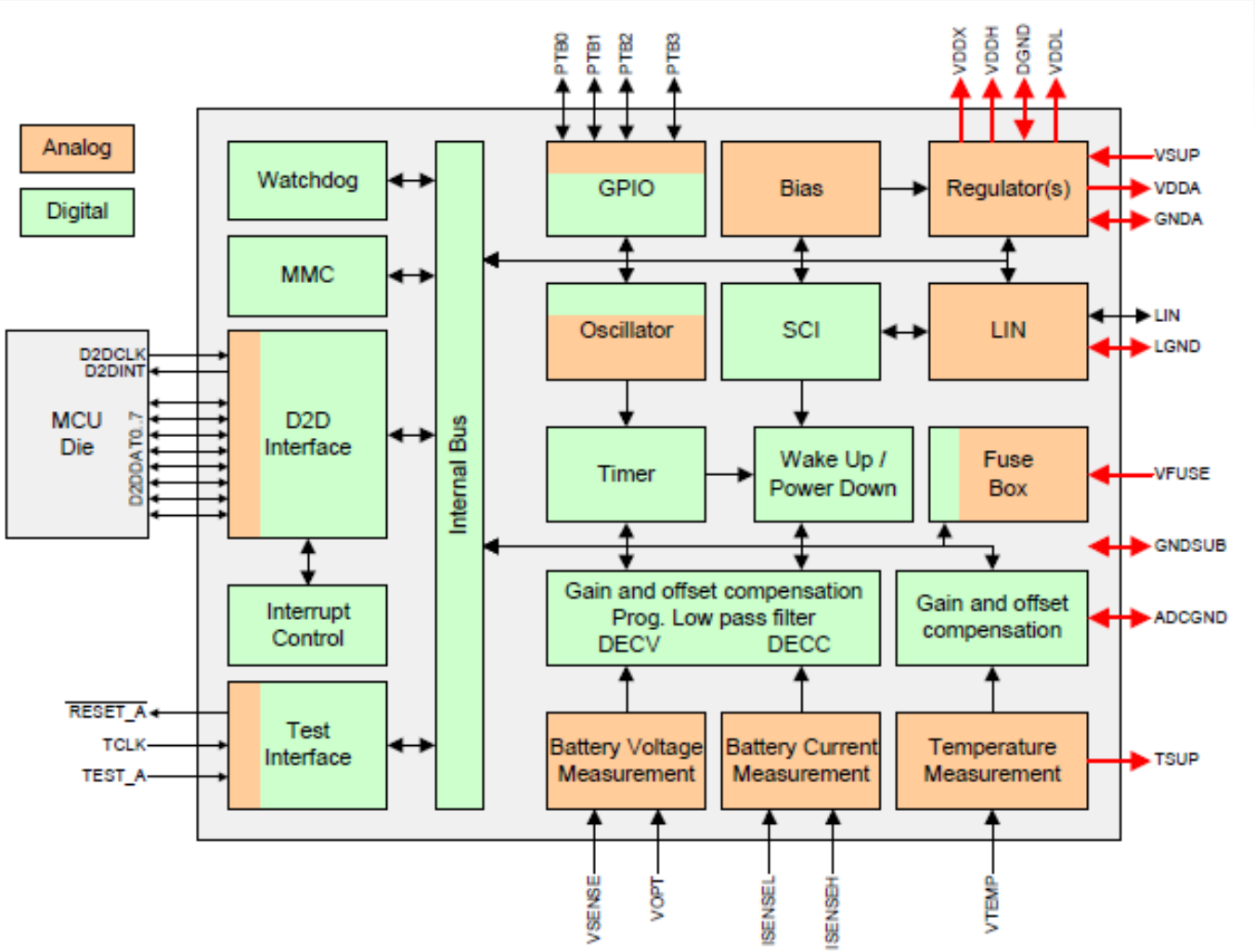
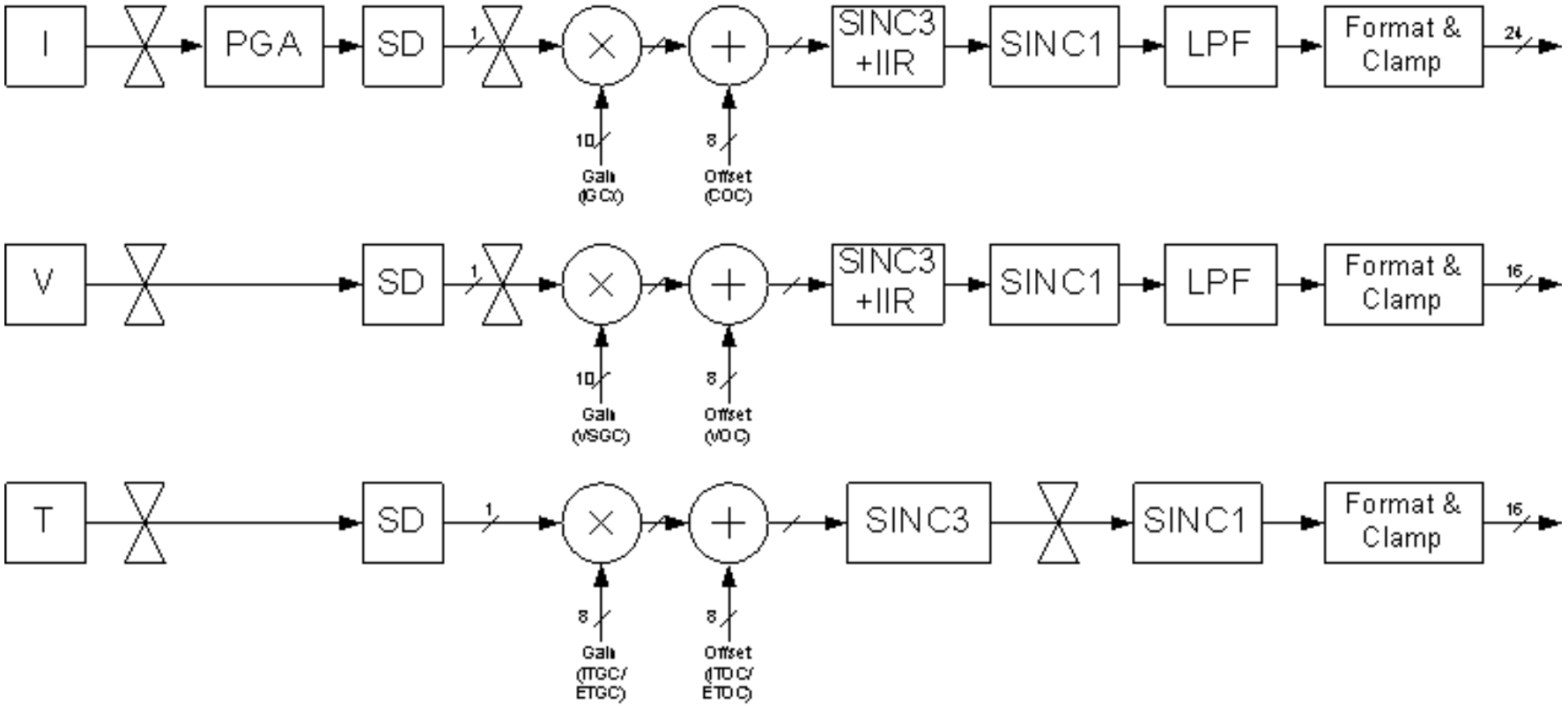


Figure 14. Analog Die Block Overview

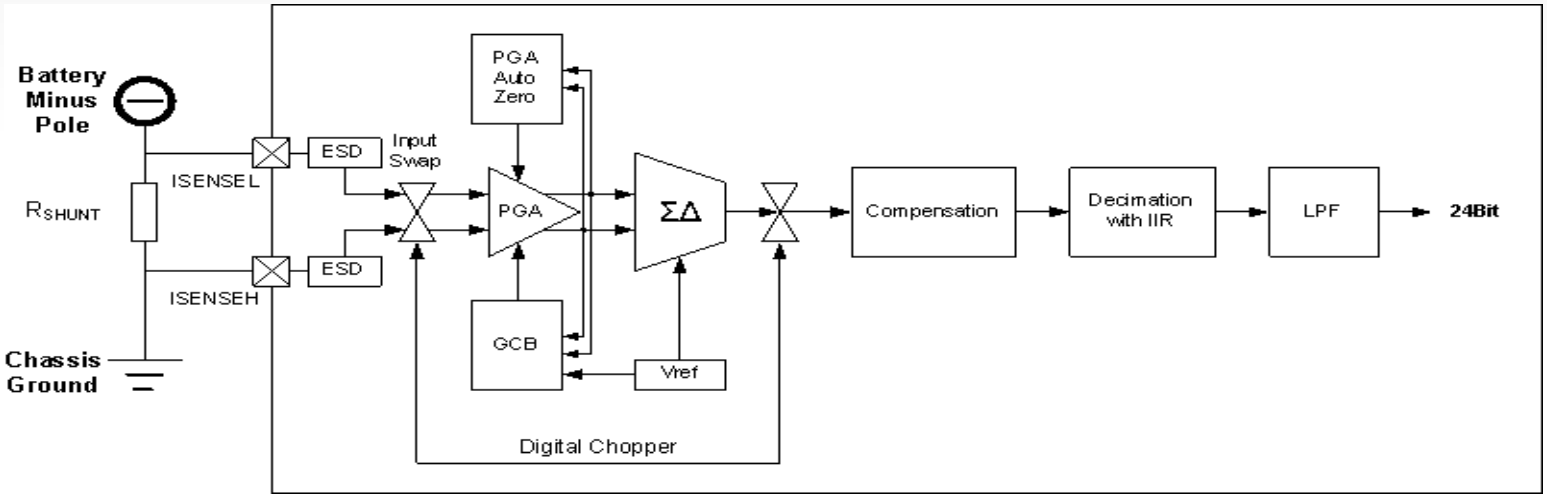
Acquisition channels

Measurement Channels Structure Overview

Same V and I channel structures allow synchronization between voltage and current measurement



Current Measurement



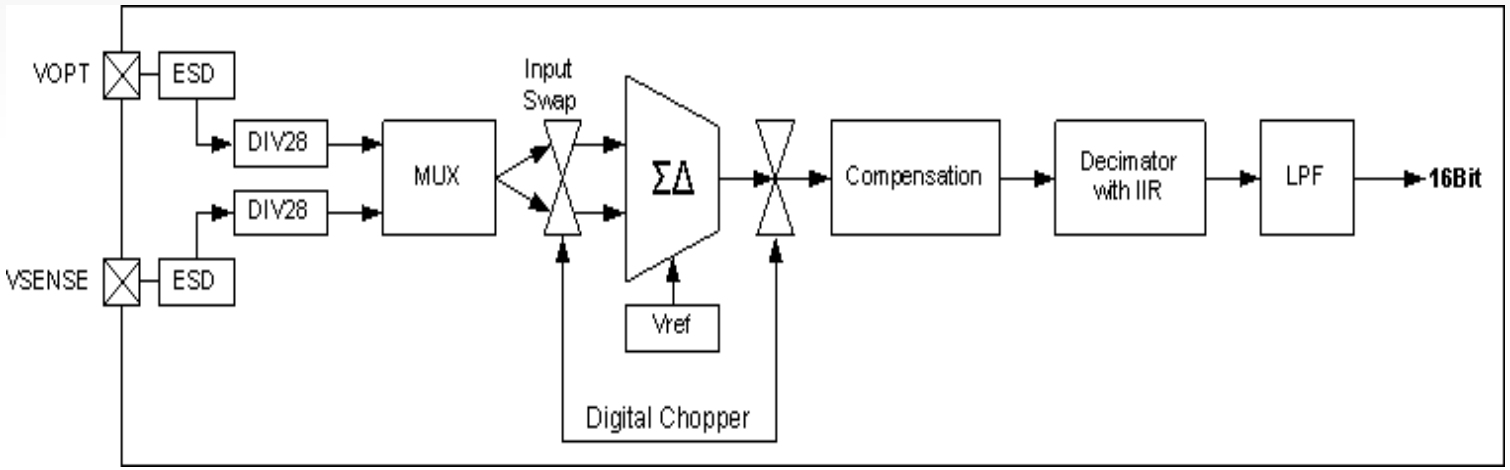
Feature Summary:

- Dedicated 16-bit Sigma Delta (ΣΔ) ADC
- Programmable Gain Amplifier (PGA) with 8 programmable gain factors
- Gain Control Block (GCB) for automatic gain adjustment
- Simultaneous sampling with voltage channel
- Gain and offset compensation
- Optional chopper mode with moving average
- SINC3 + IIR stage
- Programmable Low Pass Filter (LPF), configuration shared with voltage measurement channel
- Shunt open detect sensing feature
- Triggered sampling during low power mode with programmable wake up conditions

Ratings	Symbol	Min	Typ	Max	Unit
Gain Error	$I_{GAINERR}$				
with temperature based gain compensation adjustment[19], [20]		-0.5	+/-0.1	0.5	%
with default gain compensation		-1.0		1.0	
Offset Error[21], [22]	$I_{OFFSETERR}$			0.5	µV
Resolution	I_{RES}		0.1		µV
ISENSEH, ISENSEL					
terminal voltage	V_{INC}	-300		300	mV
differential signal voltage range	V_{IND}	-200		200	
Wake-up Current Threshold	$I_{RESWAKE}$		0.2		µV
Resistor Threshold for OPEN Detection	R_{OPEN}	0.8	1.25	1.8	MOhm

Ratings	Symbol	Min	Typ	Max	Unit
Frequency Attenuation[40],[41]					
<100 Hz (f_{PASS})				3.0	dB
>500 Hz (f_{STOP})		40			
Signal Update Rate[42]	$f_{IUPDATE}$	0.5		8.0	kHz
Signal Path Match with Voltage Channel	$t_{IVMATCH}$			1.0	µs
Gain Change Duration (Automatic GCB active)	t_{GC}			14	µs

Voltage Measurement



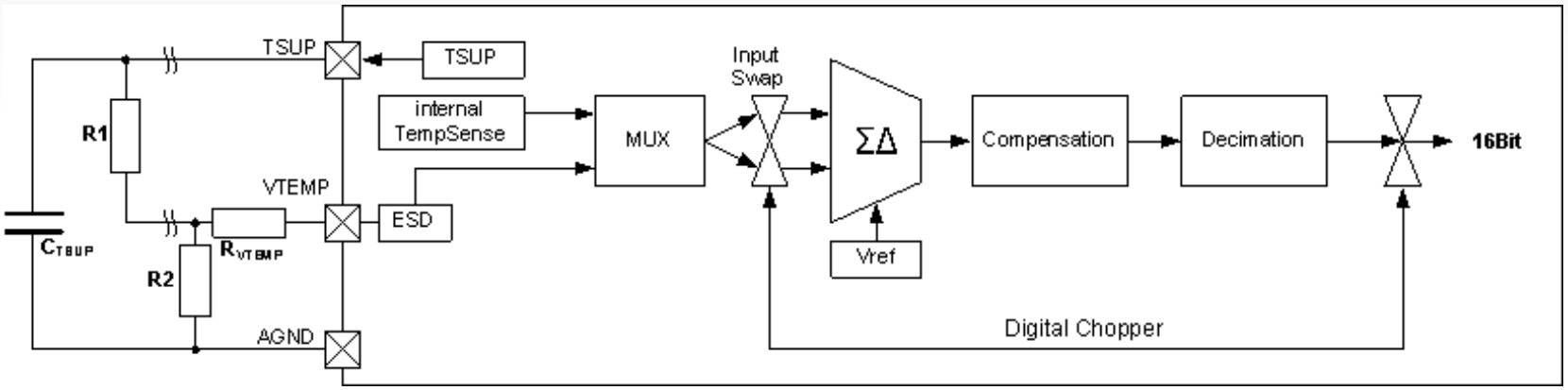
Feature Summary:

- Dedicated 16-bit Sigma Delta (ΣΔ) ADC
- Fixed high precision divider
- Optional external voltage input "VOPT"
- Simultaneous sampling with current channel
- Gain and offset compensation
- Optional chopper mode with moving average
- SINC3 + IIR Stage
- Programmable Low Pass Filter (LPF), configuration shared with current measurement channel

Ratings	Symbol	Min	Typ	Max	Unit
Measurement Range	V_{RANGE}				
$3.5\ V \le V_{SUP} < 5.0\ V$		0.5		20	V
$5.0\ V \le V_{SUP} \le 28\ V$		0.5		28	
Gain Error[24]	$V_{GAINERR}$				
$18\ V < V_{IN} \le 28\ V$		-0.5		0.5	
$3.5\ V \le V_{IN} \le 18\ V$		-0.4		0.4	%
$3.5\ V \le V_{IN} < 5.0\ V$[25]		-0.25		0.25	
$5.0\ V \le V_{IN} \le 18\ V$[25],[27]		-0.15		0.15	
Offset Error[26]	$V_{OFFSETERR}$	-1.5		1.5	mV
Resolution with R_{VSENSE} = 2.2 kOhm	V_{RES}			0.5	mV

Ratings	Symbol	Min	Typ	Max	Unit
Frequency attenuation[43],[44]					
95...105Hz (f_{PASS})				3.0	dB
>500Hz (f_{STOP})		40			
Signal update rate[45]	$f_{VUPDATE}$	0.5		8.0	kHz
Signal path match with Current Channel	$f_{IVMATCH}$			1.0	µs

Temperature Measurement



Feature Summary:

- Internal on chip temperature sensor
- Optional external temperature sensor input (VTEMP)
- Dedicated 16-bit Sigma Delta ADC
- Programmable gain and offset compensation
- Optional external sensor supply (TSUP) with selectable capacitor
- Optional measurement during low power mode to trigger recalibration

Ratings	Symbol	Min	Typ	Max	Unit
Measurement Range	T_{RANGE}	-40		125	°C
Accuracy	T_{ACC}				
-40 °C ≤ T_A ≤ 60 °C[29]		-2.0		2.0	K
-40 °C ≤ T_A ≤ 125 °C		-3.0		3.0	
Resolution	T_{RES}		8.0		mK
TSUP Voltage Output, 10 µA ≤ I_{TSUP} ≤ 100 µA	V_{TSUP}	1.1875	1.25	1.3125	V
TSUP Capacitor with ECAP = 1	C_{TSUP}	209	220	231	pF
Max Calibration Request Interrupt Temperature Step	$T_{CALSTEP}$	-25		25	K

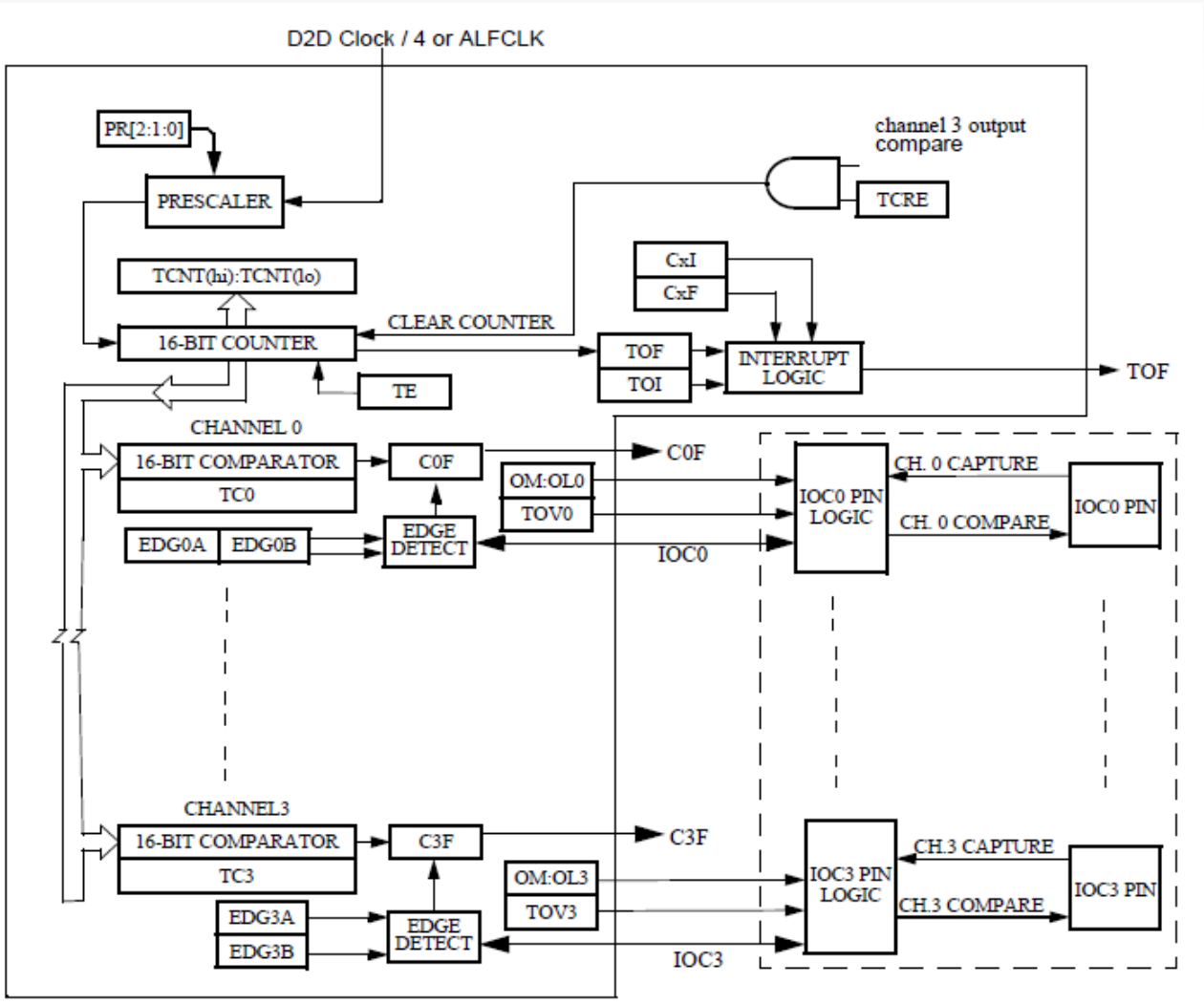
Ratings	Symbol	Min	Typ	Max	Unit
Signal Update Rate[46]	$f_{TUPDATE}$	1.0		4.0	kHz

Timers, I/O & Communications

Timers – 4 channel 16-bit timer module

- General purpose timer
- 4 independent channels
- Input capture
- Output compare
- Interrupts
  - 1 per channel
  - Timer overflow
- Clock prescaler (1-128)
- 16-bit counter
- Normal mode clock:
  - D2DCLK / 4 (8 MHz max.)
- Low power mode clock:
  - ALFCLK (0.125 – 1 kHz)

- Optional Timer counter reset on channel 3 ouput compare event
- Optional wake-up over PTB0-3 (GPIO)



Timers – life time counter

- Flexible up-counter running in normal and low power mode
- ALWAYS based on ALFCLK
- Overflow interrupt and wake-up

Table 275. Module Memory Map

Offset[228]	Name		7	6	5	4	3	2	1	0
0x38	LTC_CTL (hi)	R	0	0	0	0	0	0	0	0
	Life Time Counter control register	W	LTCIEM							LTCEM
0x39	LTC_CTL (lo)	R	LTCIE	0	0	0	0	0	0	LTCE
	Life Time Counter control register	W								
0x3A	LTC_SR	R	LTCOF	0	0	0	0	0	0	0
	Life Time Counter status register	W	1 = clear							
0x3B	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x3C	LTC_CNT1 Life Time Counter Register	R	LTC[31:0]							
		W								
		R								
		W								
0x3E	LTC_CNT0 Life Time Counter Register	R								
		W								
		R								
		W								

GPIO – General purpose input output

- 4 pins (PTB0-3)
  - PTB0-2
    - 5V
    - Input / output
  - PTB3
    - High voltage capable (42 V)
    - Input only
- Wake up detection
- SCI Rx/Tx
- Timer 0-3 IC/OC
- LIN Tx/Rx
- PIN direct control
- Optional pull-up (PTB0-2)
- Optional pull-down (PTB3)

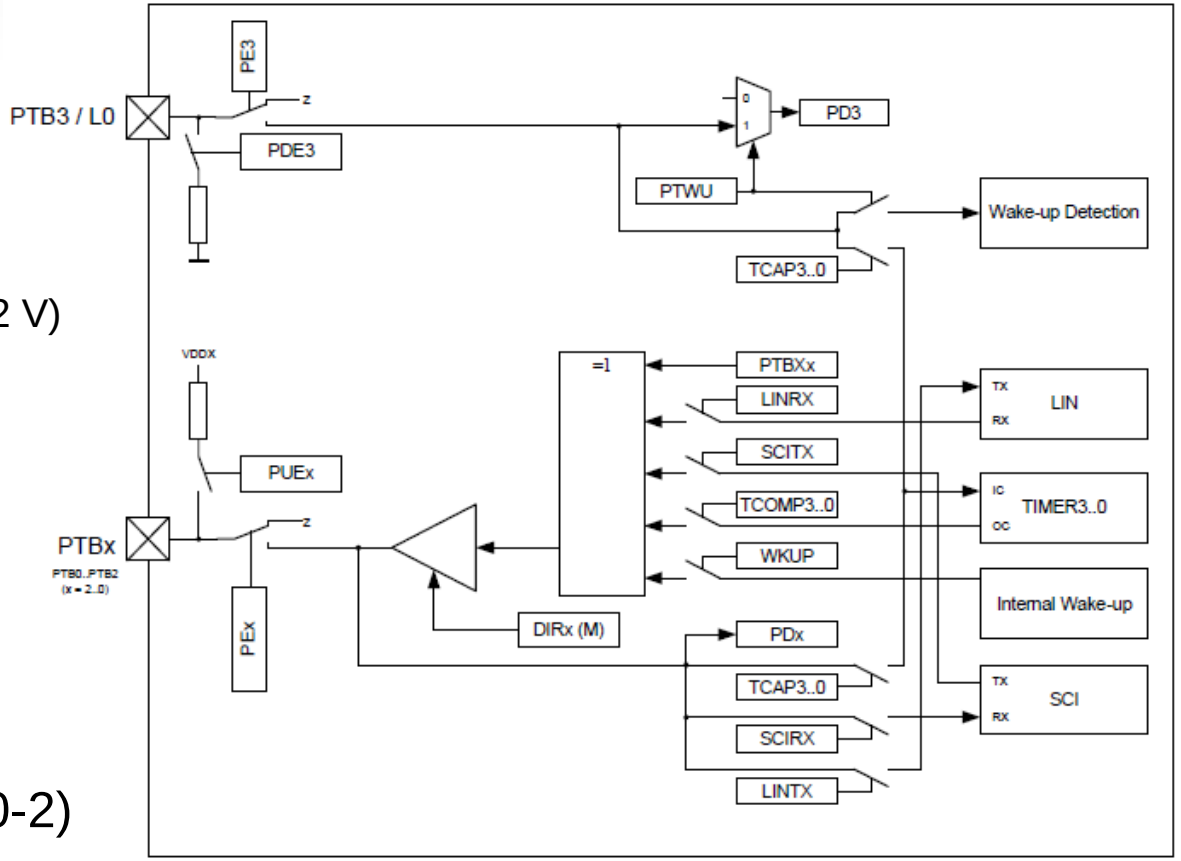


Figure 42. General Purpose I/O - Block Diagram

Interrupts

- Common vector on S12 for all analog die interrupts
  - INT_VECT register shows individual source
- Interrupt mask register for each source
- All interrupts are nestable
- Fixed priorities

Table 95. Interrupt Vector / Priority

IRQ	Description	IRQ	Priority
-	No interrupt pending or wake-up from Stop mode	0x00	-
UVI	Under-voltage interrupt or wake-up from Cranking mode	0x01	1 (highest)
HTI	High temperature interrupt	0x02	2
LTI	LIN driver over-temperature interrupt	0x03	3
CH0	TIM channel 0 interrupt	0x04	4
CH1	TIM channel 1 interrupt	0x05	5
CH2	TIM channel 2 interrupt	0x06	6
CH3	TIM channel 3 interrupt	0x07	7
TOV	TIM timer overflow interrupt	0x08	8
ERR	SCI error interrupt	0x09	9
TX	SCI transmit interrupt	0x0A	10
RX	SCI receive interrupt	0x0B	11
CVMI	Acquisition interrupt	0x0C	12
LTC	Life time counter interrupt	0x0D	13
CAL	Calibration request interrupt	0x0E	14 (lowest)

Window watchdog

- Can be used as conventional or window watchdog
- Clocking based on low power oscillator (independent from S12 MCU)
- Active after reset or wake-up
- Disabled during low power mode
  - During stop mode, the S12 watchdog can be used instead (inactive by default)
- Configurable timeout (4ms – 2048ms)

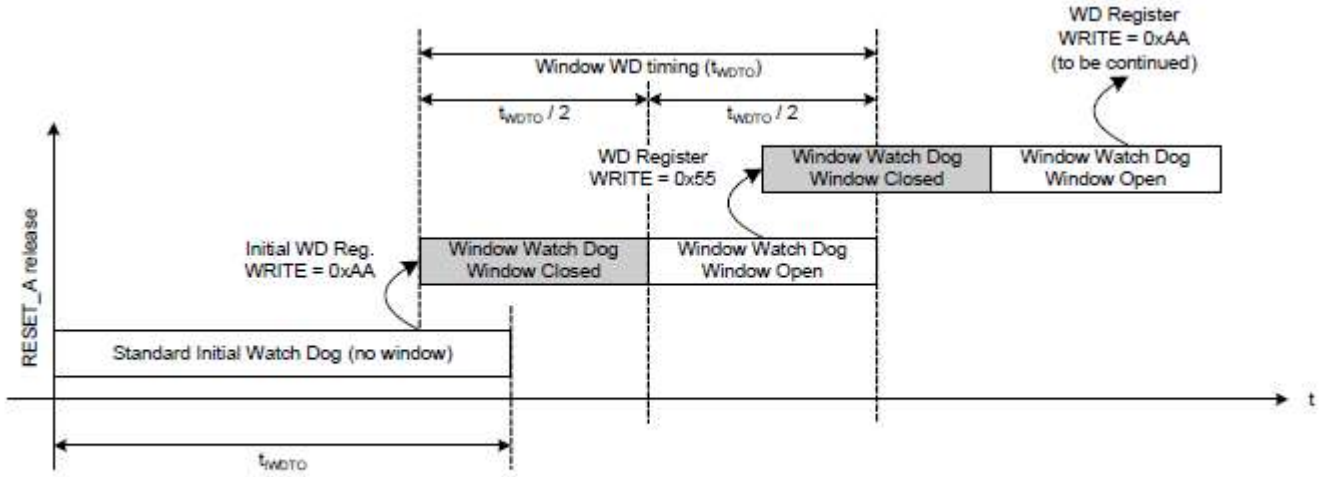


Figure 39. MM912_637 Analog Die Watchdog Operation

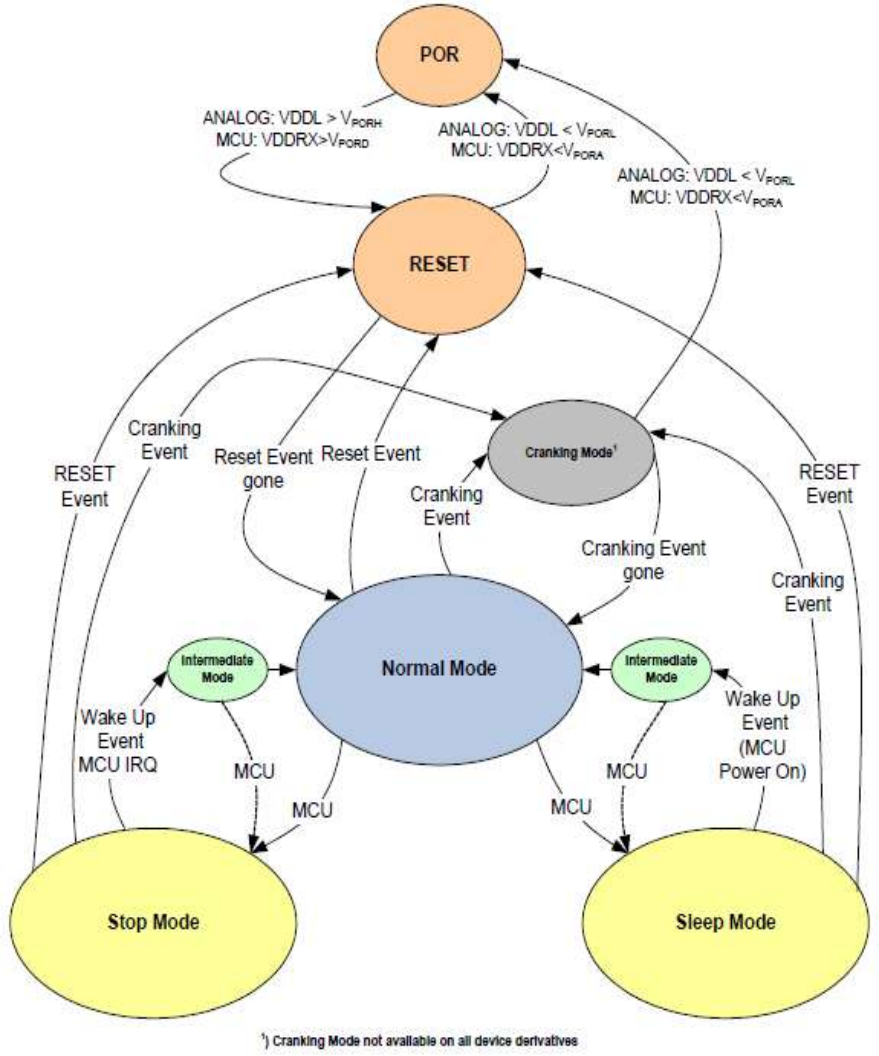
Serial Communication Interface - SCI

- Digital part of serial communication (e.g. for LIN)
- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver wake-up by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity
- Single wire mode

Operating Modes & Wakeup

Operating modes- overview

- **Normal Mode**
  - All device modules active
  - MCU fully supplied, D2DCLK active analog die clock source
  - Window Watchdog clocked on independent clock
- **Stop Mode**
  - MCU in low power mode, MCU-Regulator Supply reduced current capability, D2D interface supply disabled (VDDH=OFF)
  - Unused Analog Blocks disabled, watchdog disabled
  - Optional : wake-up capabilities
  - Optional: Current and temperature measurements
- **Sleep Mode**
  - MCU powered down (VDDH and VDDX = OFF)
  - Unused Analog Blocks disabled
  - Watchdogs = OFF
  - Optional : wake-up capabilities
  - Optional: Current and temperature measurements
- **Intermediate Mode**
  - Transition from Stop/Sleep to normal mode
- **Reset Mode**
  - Reset state (driven by both analog and MCU)
- **Power On Reset Mode**
  - Indicate a loss of internal state
- **Cranking Mode**
  - Special Mode implemented to guarantee the RAM content being valid though very low power conditions.



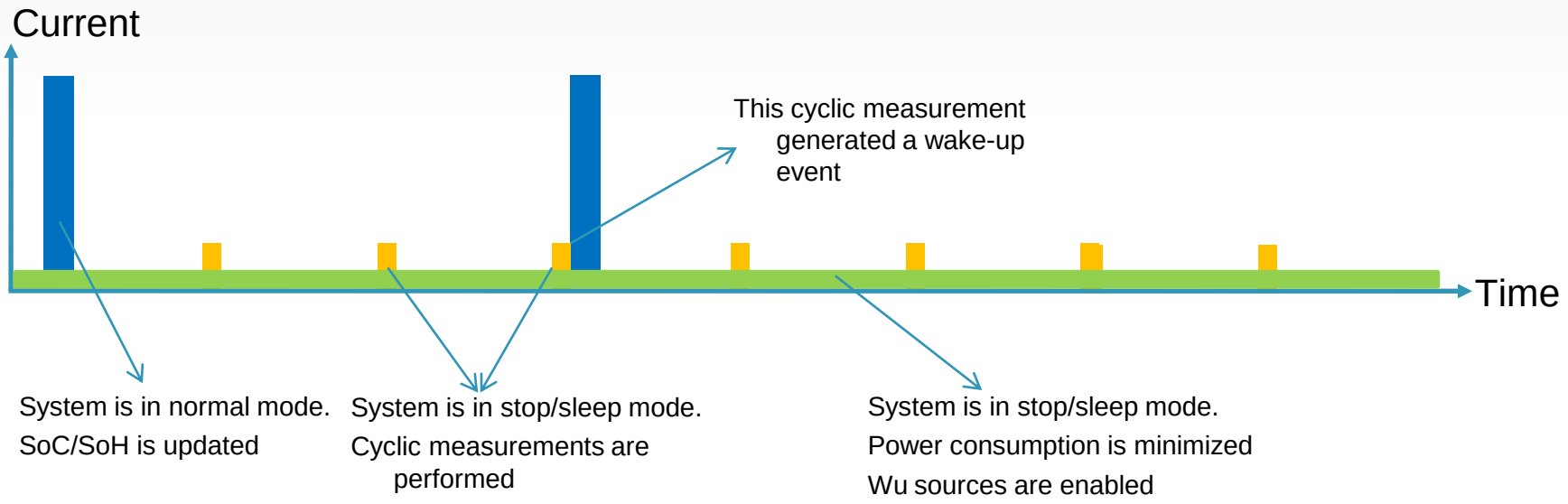
[1]) Cranking Mode not available on all device derivatives

Differences between sleep- and stop mode (SW perspective)

- Differences between sleep- and stop mode:
  - Starting point for the software after wake-up
  - Current consumption (different values for analog and MCU die)

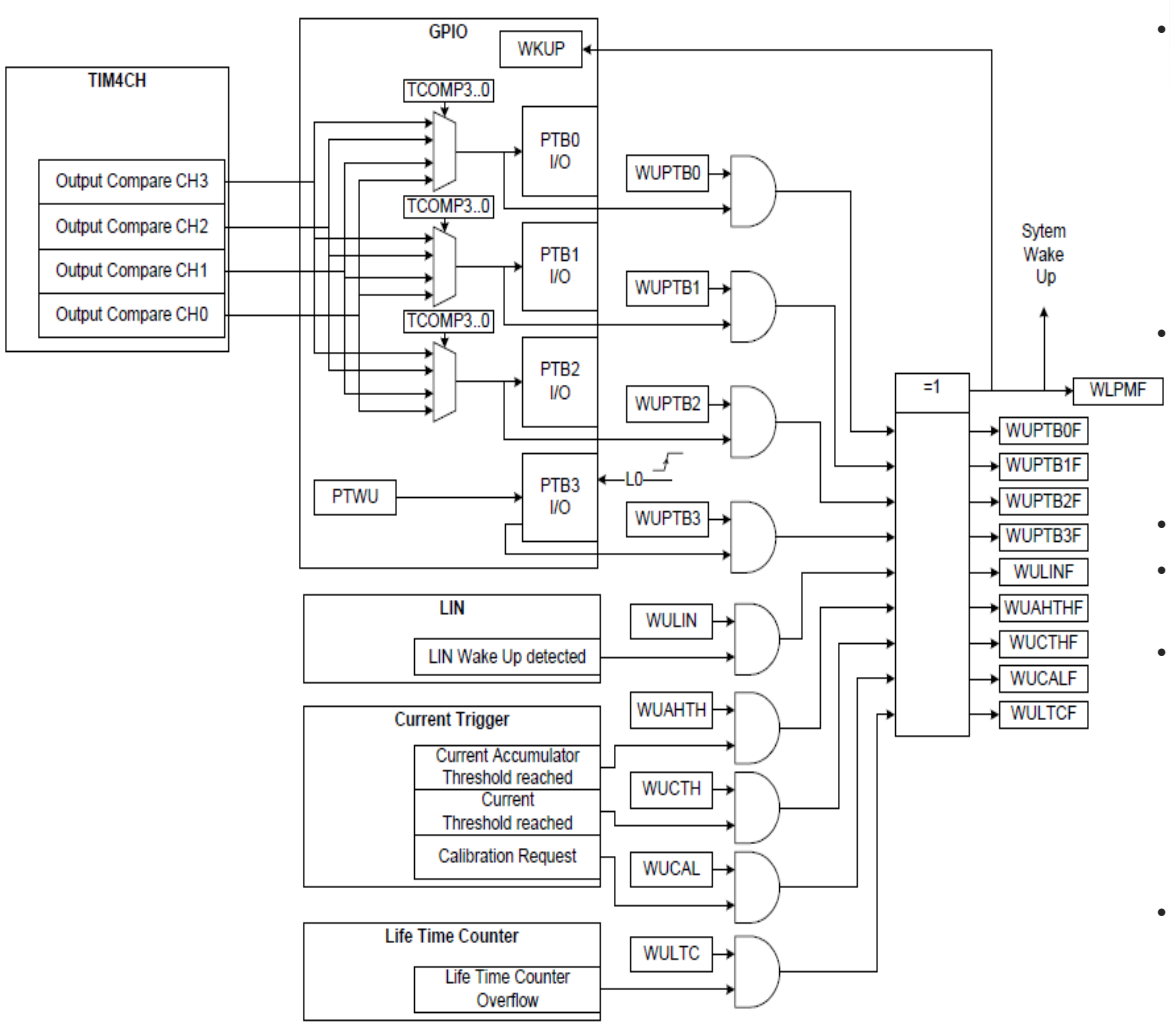
- Sleep mode
  - MCU is not powered (disconnected from the supply)
  - First instruction is fetched from power-on reset vector
  - All hardware and software initialization code is executed
  - Longer wake-up time but less current consumption compared to sleep mode (see next slides for details)
- Stop mode
  - MCU is in stop mode but still supplied
  - First instruction is fetched from the wake-up ISR. After the ISR, the first instruction after the STOP command (to go to stop mode) is executed in the main program
  - No software initialization, minor hardware initialization (mainly wait for PLL-lock)
  - Faster wake-up but more current consumption compared to sleep mode

Typical mode transitions in the application



- Device is put into stop/sleep mode most of the time to decrease current
- Regularly, the system wakes-up and performs updates of SoC/SoH
- Cyclic measurements allow coulomb counting and detect any activity in the car (typically every second)

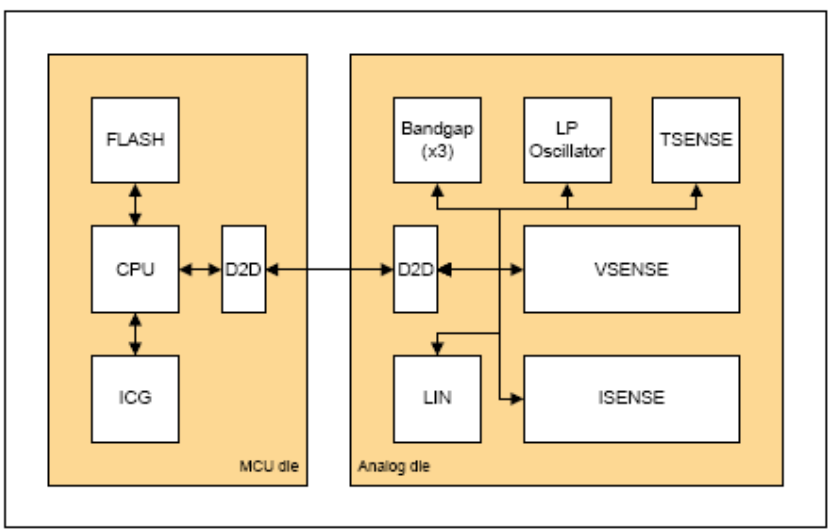
Wake-up Sources overview



- **Cyclic Current Acquisition / Calibration Temperature Check**
  - Three wake-up conditions are implemented.
    - **Current Threshold Wake-Up**
    - **Current AmpHour Threshold Wake-Up**
    - **Calibration Request Wake-Up**
- **Timed wake-up**
  - Programmable wake up timer with integrated 4 Channel Timer Module available during both low power modes
- **Wake Up from LIN/CAN**
- **Wake Up on Pin : PBT3/L0 with pin 0 to 1 transition (rising edge)**
- **Wake Up on Life Time Counter Overflow**
  - The life time counter can be configured to run during low power mode, Once the counter overflows with the life time counter wake up enabled, a wake up is issued.
- **General Wake Up Indicator**
  - To indicate the system has been woken up after power up

Trim and Calibration

Trimming and Calibration Overview



- Factory Stored Trimming
  - Trimming will use factory measured and calculated values stored in a special Microcontroller Information Register to be loaded into specific registers in the MCU and analog die at system power up.
- Calibration
  - Calibration will be done during operation of the system using internal references or specific measurement procedures.

Factory Stored Trimming

- **Microcontroller Chip**
  - **Internal Oscillator Trimming (ICG)**
    - Optimum trim value is determined during Final Test and stored into the Information register block of the MCU FLASH memory. During power on of the microcontroller, the trim value will be automatically stored into the MCU trimming register.

- **Analog Chip**
  - **Low Power Oscillator Trimming**
  - **Band gap Reference Trimming (BGAP)**
  - **Temperature Sense Module Trimming (TESENE)**
  - **LIN Slope Control Trimming**

Trim information is determined during Final Test and stored into the MCU FLASH memory.

On device every power up, the corresponding trim value needs to be copied into the desired register.

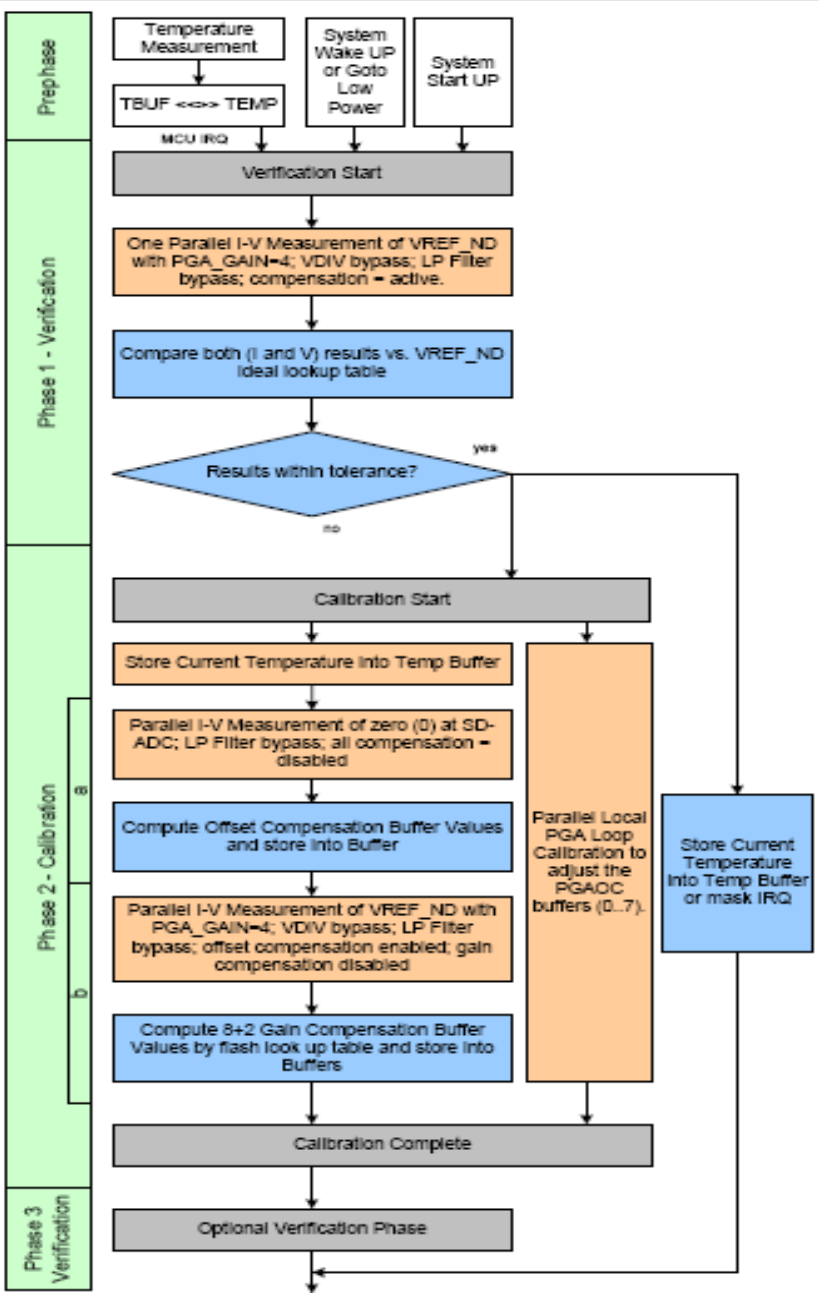
Calibration - Periodic Adjustment during Operation

- Voltage and Current Sense Calibration have to be performed during system operation

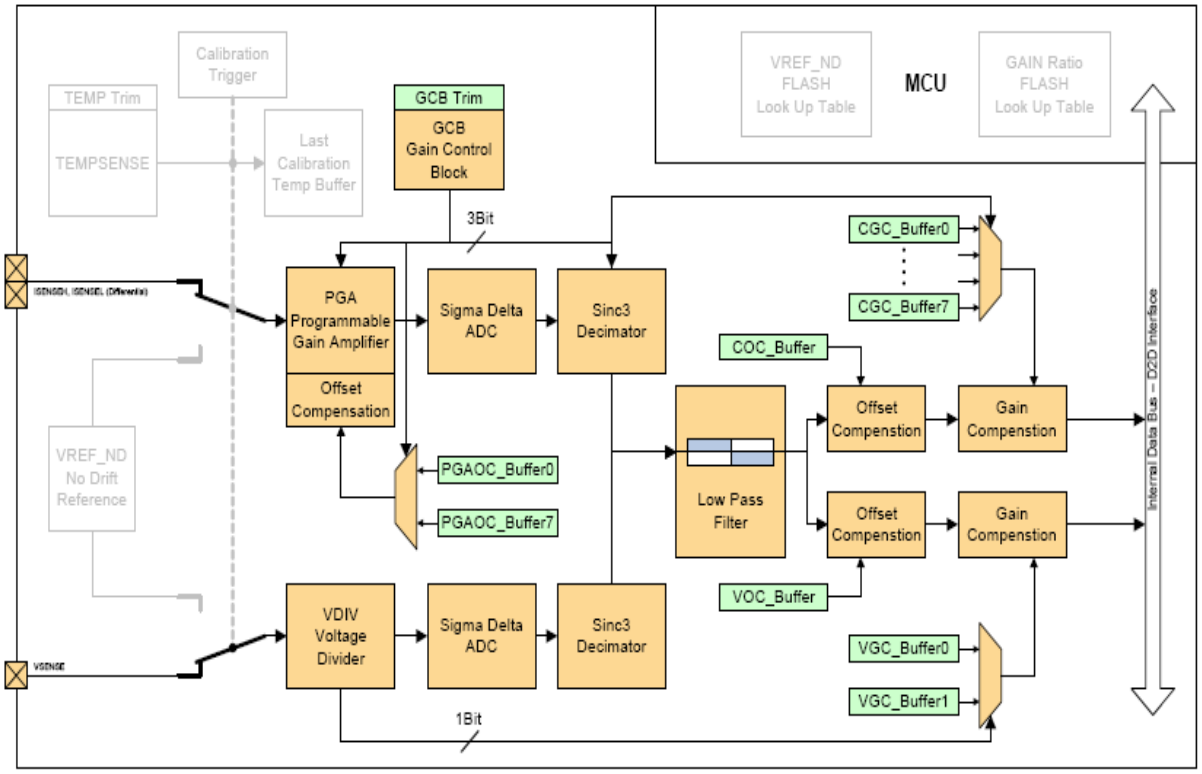
- Initiators for re-calibration would be
  - A system power up occurred (to be initiated by the MCU)
  - On a regular basis before or after low power mode - based on application software flow.
  - The junction temperature measurement result significantly differs from the “last calibration temperature buffer content. The analog die constantly compares the “last calibration temperature buffer” vs. the current temperature measurement and issues an interrupt once a significant difference is detected.
  - A significant temperature change was detected during low power current sense2. The analog die compares the “last calibration temperature buffer” vs. the temperature measurement and issues a wake up once a significant difference is detected.

Calibration - Periodic Adjustment during Operation

- General Calibration Flow
  - The current and voltage measurement calibration can be divided into 3 phases:
    - Phase 1 - Verification Phase: One parallel (I/V) acquisition of the VREF_ND reference is done in order to identify an existing inaccuracy. Based on the application flow, phase 1 could be skipped by immediately performing phase 2 calibration after trigger.
    - Phase 2 - Calibration Phase: Once Phase 1 identified an inaccuracy, the actual calibration phase would perform a parallel offset compensation measurements (I/V) followed by one gain compensation measurement.
    - Optional Phase 3 - Verification phase: To ensure effective calibration, an additional verification phase can be performed (1 measurement).



Voltage / Current sense Module Calibration - Normal Acquisition Flow

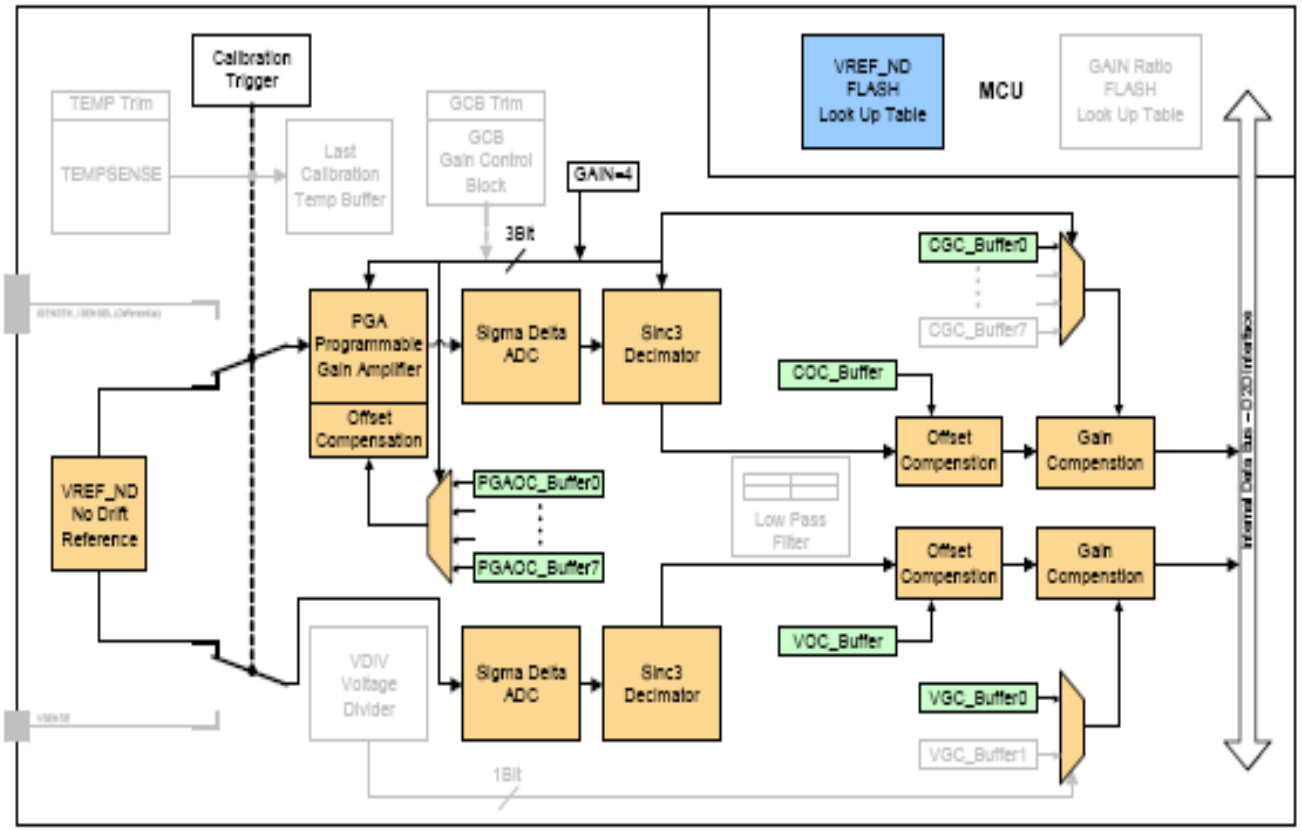


- During a regular acquisition the differential ISENSE(L/H) will be routed through the Programmable Gain Amplifier (PGA).
- The amplified signal is converted by the Sigma Delta converter and decimated in the SINC3 decimator. In a similar procedure, the VSENSE signal is routed through the voltage divider stage followed by the Sigma Delta ADC and SINC3 decimator.
- Both signals are processed by the same programmable low pass filter, offset- and gain compensation stage in serial.
- For both chains, the Offset and Gain Compensation is based on the content of the COC/VOC and CGC/VGC buffers located in the analog die logic.
- Once a trigger calibration event occurs, a calibration sequence has to be initiated by the microcontroller.

1. TEMPSENSE - Current temperature measurement result located in the ADC result register.
2. LAST CALIBRATION BUFFER - At the start of a calibration sequence (Phase 2), the current temperature (TEMPSENSE) is stored into the buffer to memorize the calibration temperature. This value is used during low power current sense to wake up on any significant temperature change and during normal mode to issue an interrupt on the same temperature change.
3. VREF_ND - Non Drift Voltage reference. Very stable voltage reference implementation to compensate any temperature, lifetime or similar effect.
4. VREF_ND FLASH LOOK UP TABLE - This table stores all ideal results for the measurement results of the VREF_ND acquisition of both chains in 20 °C increments in the MCU flash memory. The values have been calculated during final HOT and COLD test (and interpolation).
5. PGA OFFSET COMPENSATION - In order to eliminate any PGA offset effect, an local compensation is performed based on the current gain setting.
6. GAIN RATIO FLASH LOOK UP TABLE - This look up table is used to compute the correct gain compensation buffer values based on the result of the smallest value measured.

Verification Phase (Phase 1)

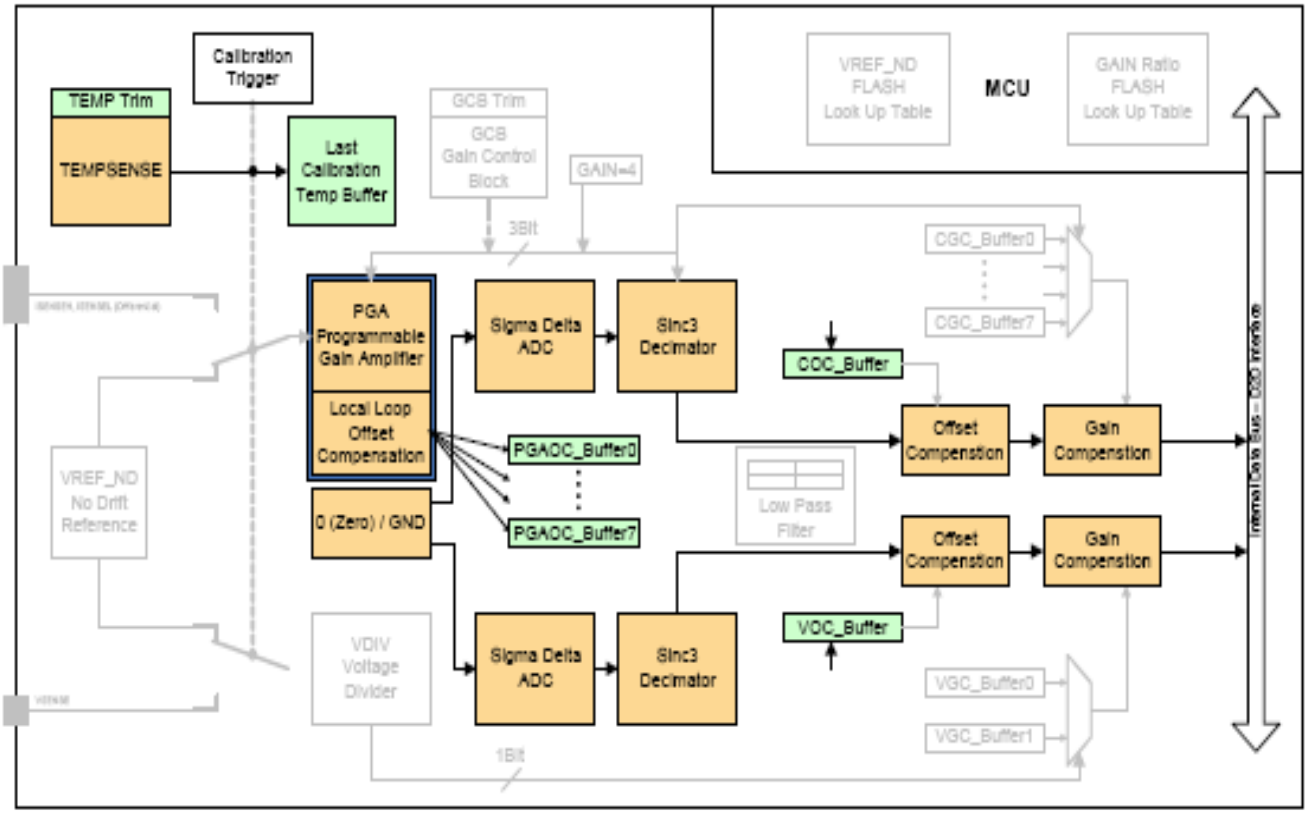
- Once a calibration trigger event has occurred, phase 1 verification is executed to do a single acquisition to evaluate the accuracy of the compensation.



1. The PGA is set to the minimum gain (4); current offest gain compensation are set to Buffer 0
2. The Voltage Divider is bypassed (accuracy is guaranteed by implementation); voltage offset and gain compensation are set to buffer 0
3. The PGA offset is calibrated using PGAOC_Buffer0.
4. The No-Drift-Voltage reference is connected to the input of the PGA and VSENSE-Sigma Delta ADC.
5. A full parallel acquisition is performed with the low pass filter bypassed. Offset and gain compensation are done with the buffers described under 1. and 2.
6. Both (current and voltage) acquisition results are compared to the VREF_ND reference look up table value for the actual temperature.
7. If the comparison shows a significant difference, a calibration sequence (phase 2) is necessary.
8. If the comparison is within limits, the actual temperature should be copied into the calibration temperature buffer to avoid reoccurring trigger interrupts.

Offset Calibration Phase (Phase2a)

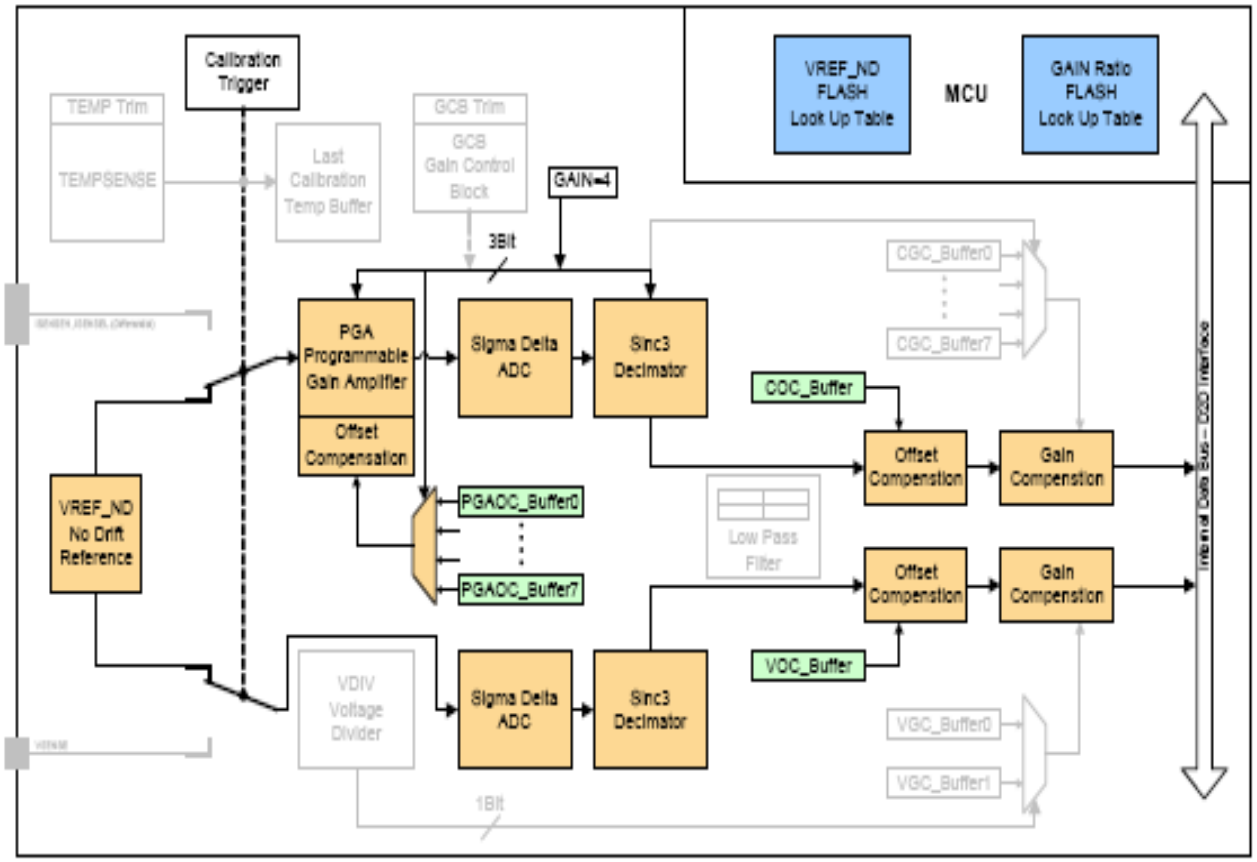
- Once phase 1 has detected a significant mismatch in calibration, a phase 2 calibration sequence has to be performed to adjust the gain and offset compensation buffers. Phase 2 can be divided into phase 2a to calibrate the offset compensation buffers and phase 2b for the gain compensation buffers. Both, 2a and 2b, will require one acquisition each.



1. The PGA is bypassed; current offset and gain compensation are disabled.
2. The Voltage Divider is bypassed; voltage offset and gain compensation are disabled.
3. Both current and voltage Sigma Delta ADC inputs are set to 0 (zero).
4. A full parallel acquisition is performed with the low pass filter bypassed.
5. Both (current and voltage) acquisition results are used to compute the offset compensation buffers for the current and voltage chain.
6. In parallel, the PGA is performing a local loop offset compensation calibration, updating the PGAOC Buffers 0..7.

Gain Calibration Phase (Phase2b)

- Once all offset compensation buffers have been computed in phase 2a, phase 2b will use one acquisition to compute the gain correction buffers.

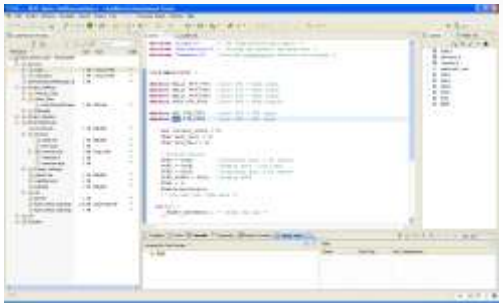


1. The PGA is set to the minimum gain (4); current offset compensation is enabled and gain compensation is disabled.
2. The Voltage Divider is bypassed (accuracy is guaranteed by implementation); voltage offset compensation is enabled and gain compensation is disabled.
3. The PGA offset is calibrated using PGAOC_Buffer0.
4. The No-Drift-Voltage reference is connected to the input of the PGA and VSENSE-Sigma Delta ADC.
5. A full parallel acquisition is performed with the low pass filter bypassed.
6. Both (current and voltage) acquisition results are compared to the VREF_ND reference look up table value for the actual temperature. The difference is used to compute the gain compensation buffer 0 for the current and voltage chain.
7. The remaining gain compensation buffers are calculated using the factory trimmed Gain Ratio Look Up Table stored in the microcontroller flash memory.

Hardware and Software Tools

Development Tools Overview

- Compilers
  - CodeWarrior
  - Cosmic
- IDE
  - CodeWarrior v10.3 (Eclipse based)
  - Cosmic Win IDEA
  - Eclipse
- Programmers
  - P&E PROGS12Z
- Debugger
  - CW & P&E S12Z Debugger
  - Cosmic Zap Debugger
- Debug Interface
  - P&E USB Multilink Debug Interface
  - Cyclone Pro Programmer
  - 3rd Party Debug Interfaces (iSYSTEM/Lauterbach)

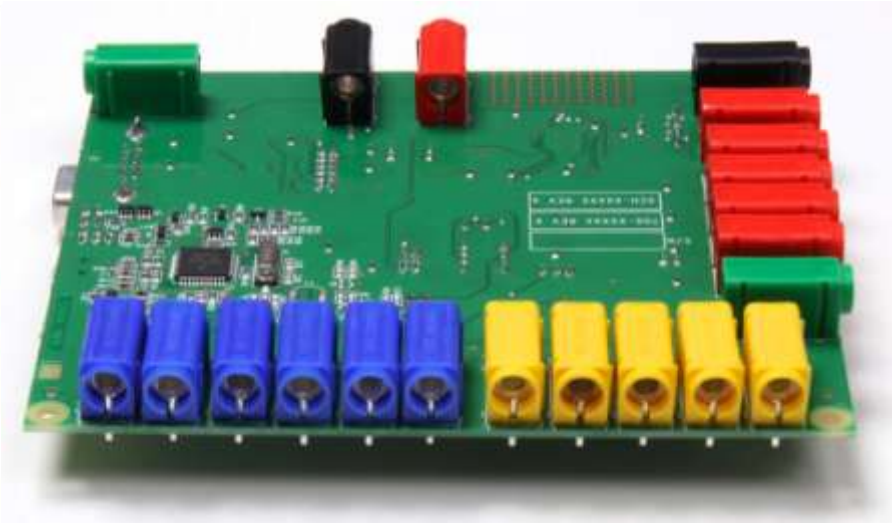


Hardware

- Standard EVB - KIT9Z1J638EVM
  - **Status: available**

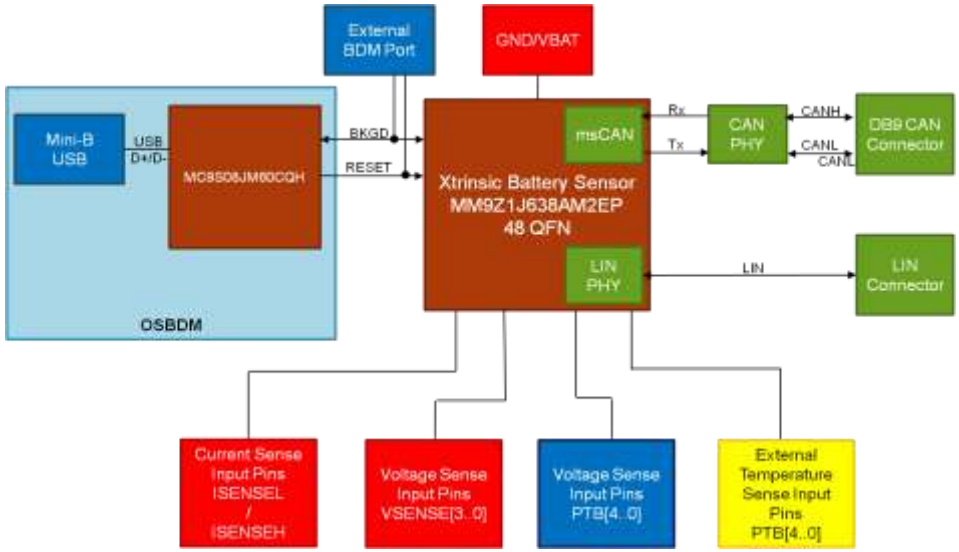
KIT912J637EVME

KIT9Z1J638EVM



KIT9Z1J638EVM – Hardware Features

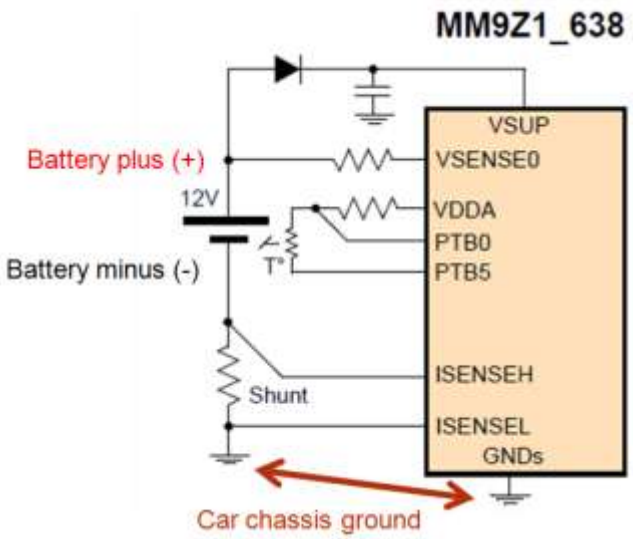
- MM9Z1_638 Xtrinsic Battery Sensor in a 48-QFN package with wet able flank.
- On-board BDM connection via open source OSBDM circuit using the MC9S08JM60 microcontroller .See www.pemicro.com/osbdm for OSBDM source code
- High-speed CAN interface
- LIN interface
- Customizable GPIOs for voltage and temperature sensing
- LED indicators
- Support for USB Multilink Interface BDM



Block diagram of the KIT9Z1J638EVM design with the primary components

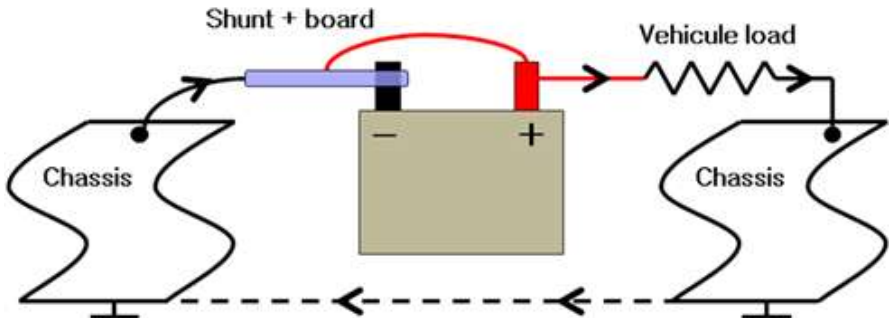
12V Lead Acid IBS Application with MM9Z1_638

Datasheet 12V Application

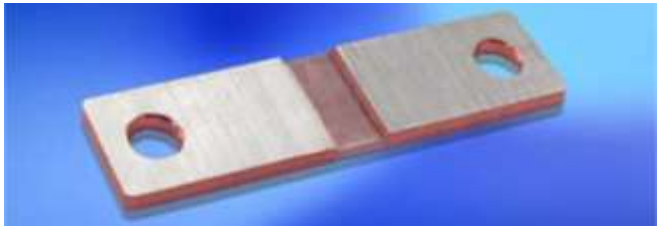


Measured current
=
Vehicle current
+
IC current

Application diagram

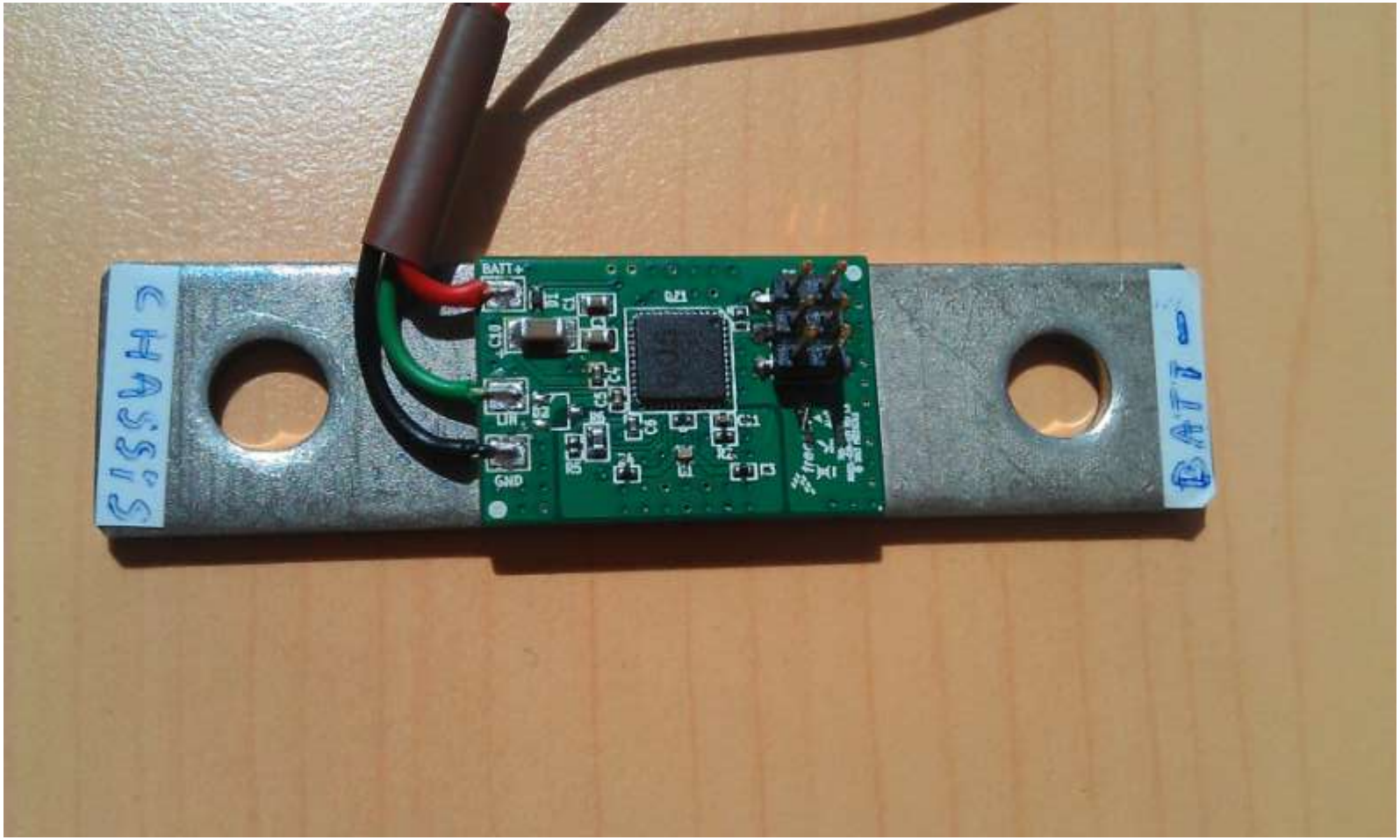


Precision shunt



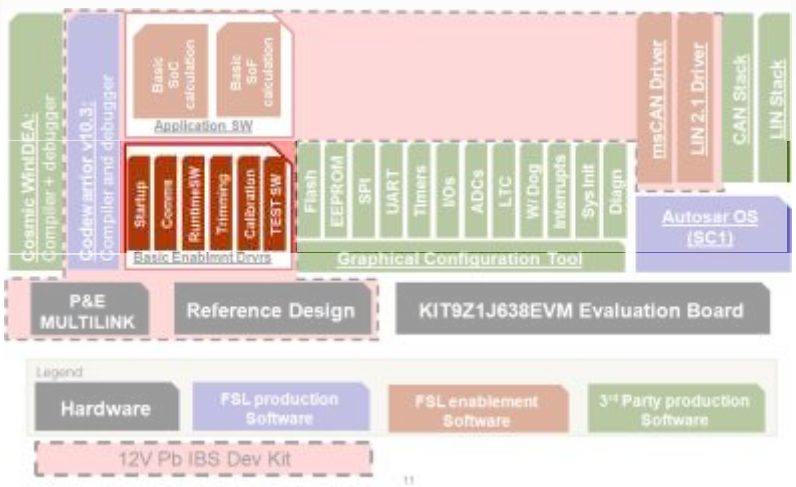
- **Resistance value : 100µΩ +/-5%**
- **Manufacturer : Isabellenhütte**
- **PCB is soldered on it**
- **PCB matches the shunt shape**

Final HW Solution (PCB + Shunt)



12V Lead Acid IBS – Basic Enablement Drivers

- QuIBS+Z startup
  - MCU die init, analog die init
  - Measurement channel setup for evaluation
- Communication
  - LIN 1.3 slave driver
  - LIN 2.1 slave driver
  - SPI
  - CAN
  - 2-wire serial (UART)
- Runtime SW
  - Flash/ EEPROM SW
  - TIMERs SW
  - STOP / SLEEP mode SW , using wake up from LTC, LIN or L0-PTB3
- Startup trimming
  - Complete startup trimming procedure as described in datasheet
  - Including temperature based gain compensation
- Module calibration
  - Test for IBS module calibration (like at end-of-line at customer)
  - On-Chip & external (in Excel) calculation of compensation values
  - Storage of compensation values in DFLASH
- Test software
  - LIN Master/Slave test using DEMO9S08DZ60 board



Availability

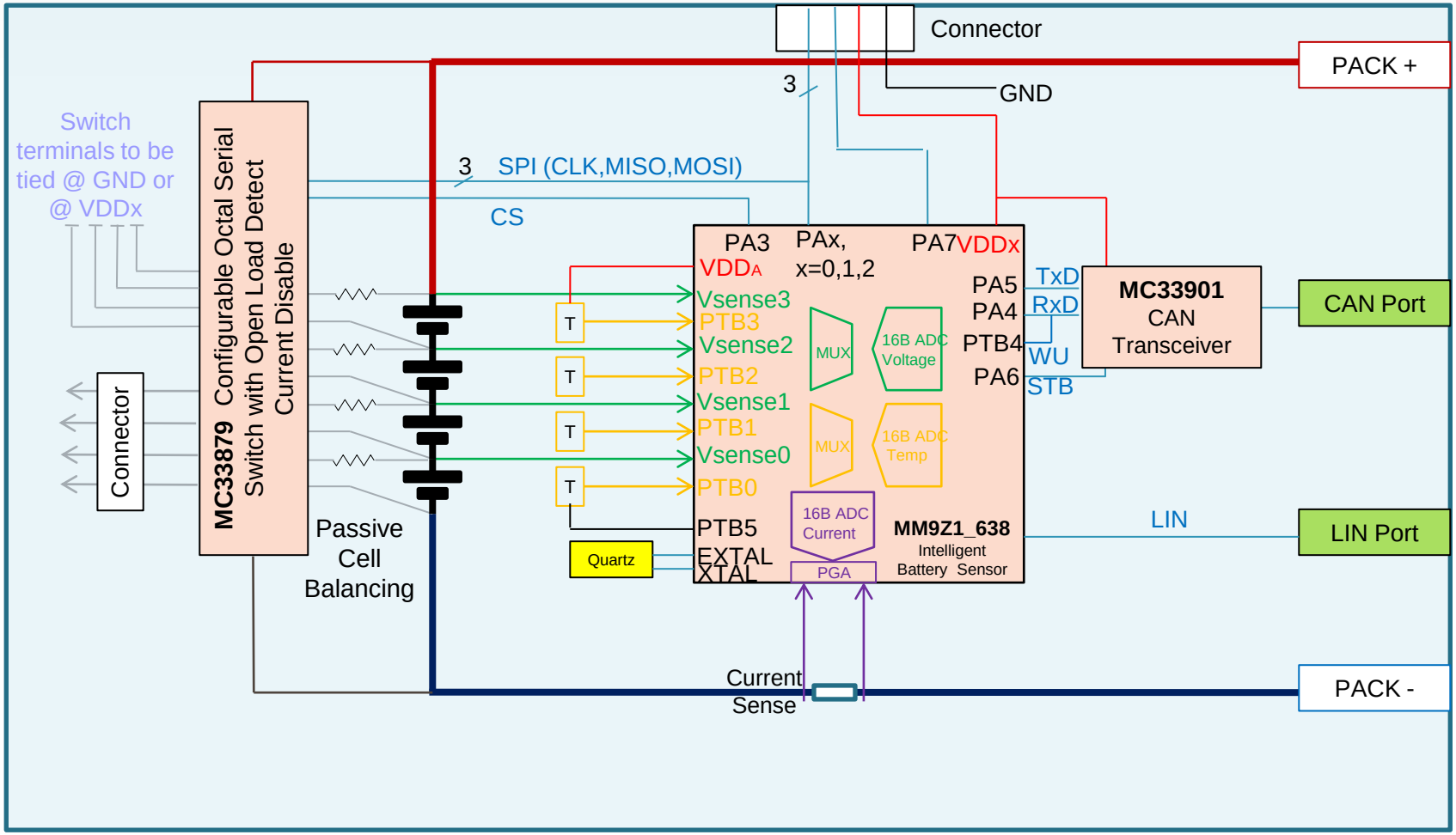
- 12V PB IBS- Development Kits (Example SW) :
  - Development Kit (1st Milestone): Available Now
    - Reference Design HW (LIN Only)
    - LIN 2.1 Driver
    - msCAN Driver
  - Development Kit (Final Milestone): Available Now
    - Basic Enablement Drivers
    - Basic SoC Calculation
    - Basic SoF Calculation

- AUTOSAR OS (FSL Production SW): Available Now
- CAN Stack (3rd Party Production SW): Available Now
- LIN Stack (3rd Party Production SW) : Available Now

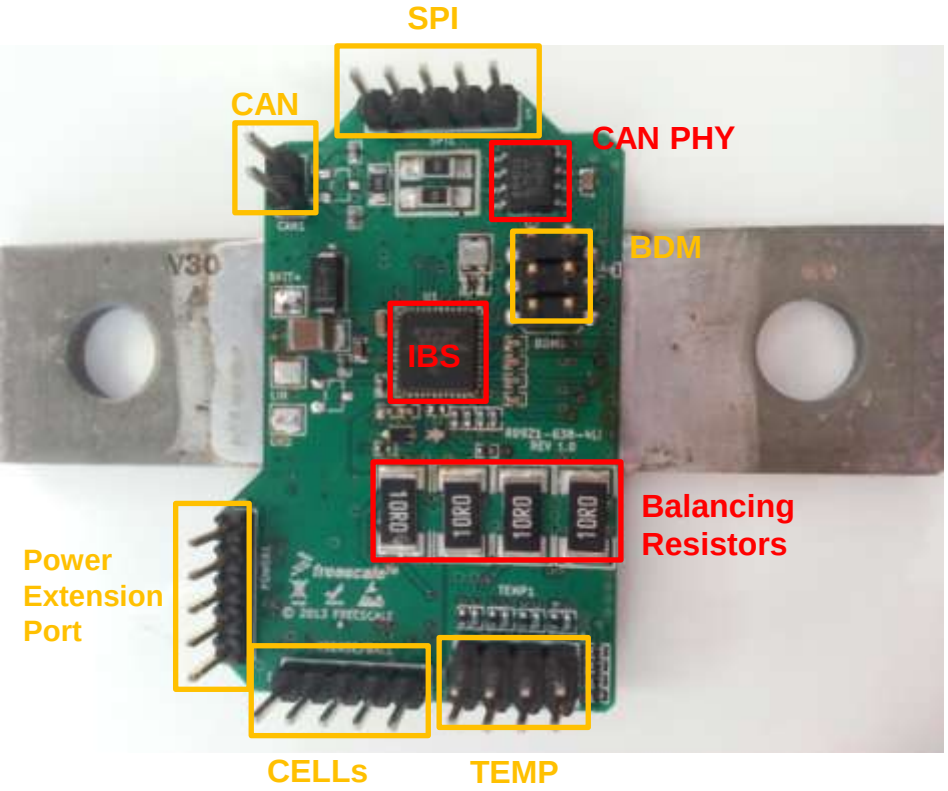
- Low-level Drivers (3rd Party Production SW) Beta Release : Q1 2014

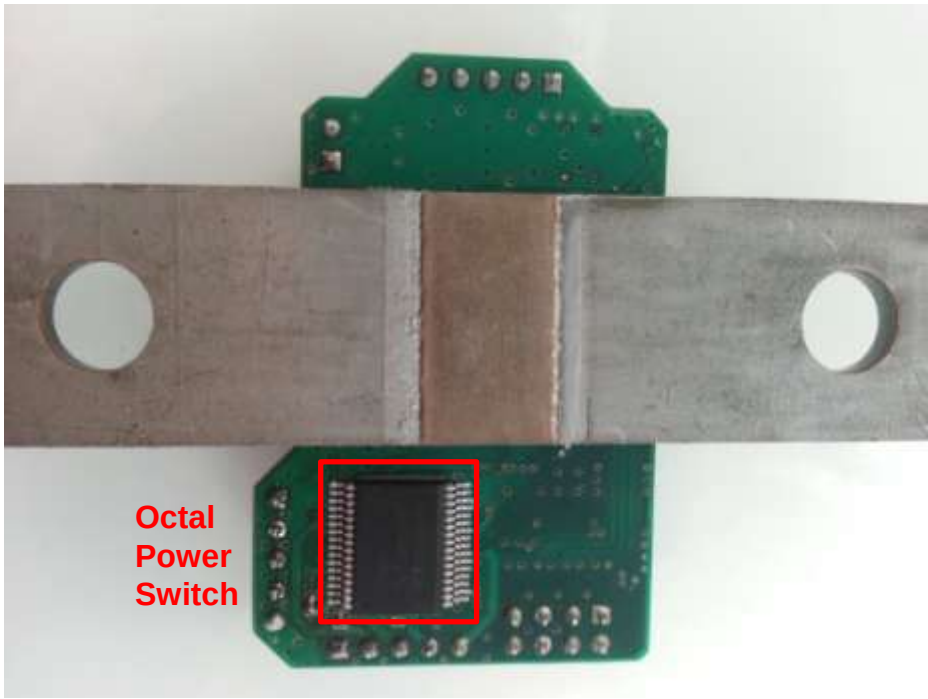
- P & E Multilink : Available Now
- Cosmic WinIDEA (3rd Party Production SW) : Available Now
- CodeWarrior 10.3 (FSL Production SW) : Available Now

14V 4 cells Li-ion BMS application with MM9Z1_638



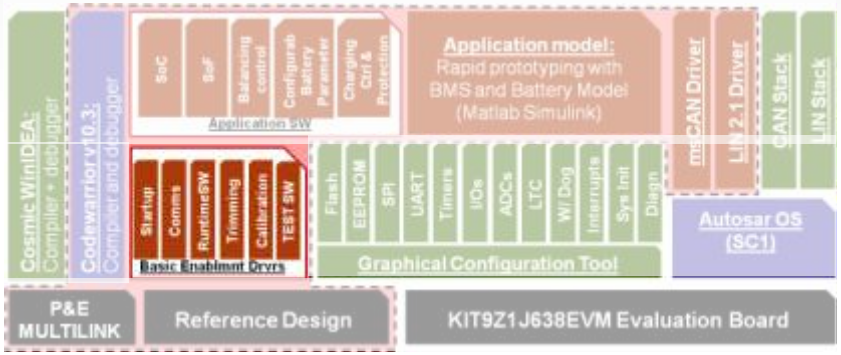
Final HW Solution (PCB + Shunt)





14V 4 cells Li-ion BMS – Basic Enablement Drivers

- Startup
  - MCU die init, analog die init
  - Measurement channel setup (current, 4 voltage, 4 temperature channels)
- Communication
  - LIN 1.3 slave driver
  - LIN 2.1 slave driver
  - SPI
  - CAN
  - 2-wire serial (UART)
- Runtime SW
  - EEPROM SW
  - TIMERs SW
  - STOP / SLEEP mode SW , using wake up from LTC, LIN or L0-PTB3
- Startup trimming
  - Complete startup trimming procedure as described in datasheet
  - Including temperature based gain compensation
- Module calibration
  - Test for IBS module calibration (like at end-of-line at customer)
  - On-Chip & external (in Excel) calculation of compensation values
  - Storage of compensation values in DFLASH
- Test software
  - LIN Master/Slave test using DEMO9S08DZ60 board



Availability

- 14V 4 cells Li-ION BMS Development Kit :
  - Development Kit (1st Milestone): Available Now
    - Reference Design HW
    - Basic Enablement Drivers
    - LIN 2.1 Driver
    - msCAN Driver
    - SoC Appl (Basic)
  - Development Kit (2nd Milestone): Available Now
    - SoC Appl (Full)
    - Balancing Appl SW
    - Charge ctrl Appl SW
  - Development Kit (Final Milestone): Oct 2013
    - SoF Appl
    - Battery parameter configuration
    - Matlab Models
- AUTOSAR OS (FSL Production SW): Available Now
- CAN Stack (3rd Party Production SW): Available Now
- LIN Stack (3rd Party Production SW) : Available Now
- Low-level Drivers (3rd Party Production SW) Beta Release : Q1 2014
- P& E Multilink : Available Now
- Cosmic WinIDEA (3rd Party Production SW) : Available Now
- CodeWarrior 10.3 (FSL Production SW) : Available Now

Useful Links

- **Compilers / Debugger / Debugging Interface:**
  - CodeWarrior 10.3 (eclipse based) – http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=CW-MCU10&fsrch=1
  - Cosmic WinIDEA and Zap – http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=CDPW-S12Z-NLA&fsrch=1 http://cosmic-software.com/s12z_des.php
  - P&E USB Multilink Debug Interface - http://www.pemicro.com/index.cfm
  - D-Bug12XZ - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=S12ZVM&fpsp=1&tab=Design_Tools_Tab#

- **FSL HW:**
  - EVB – http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KIT912J637EVME&fr=gtl

- **FSL SW Drivers and Libraries:**
  - LIN drivers – http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=S12ZVM&fpsp=1&tab=Design_Tools_Tab# in near future will be also added to www.freescale.com/LIN
  - NVM Drivers: http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=S12ZVM&fpsp=1&tab=Design_Tools_Tab#

- **FSL Tools:**
  - FreeMASTER Run time debugger – www.freescale.com/FreeMASTER
  - Rappid - http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=RAPPIDTOOLBOX
  - Processor Expert – www.freescale.com/processorexpert

Intelligent Precision Battery Sensors

- Embedded **MCU + Precision Analog** solutions in a single device
- **Highly Integrated** to allow BOM optimization
- Designed to **reduce SW complexity** and **current consumption** compared to existing solutions
- **AECQ-100 qualified**, meets **Automotive Robustness** and **Zero defect Quality** levels
- Samples available
- EVBs available
- Product Demonstrator available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