P4080PCIe Development Platform Quick Started Guide

About this Document

This document describes how to connect to the P4080PCIe card and verify its basic operation.

Contents

Required Reading

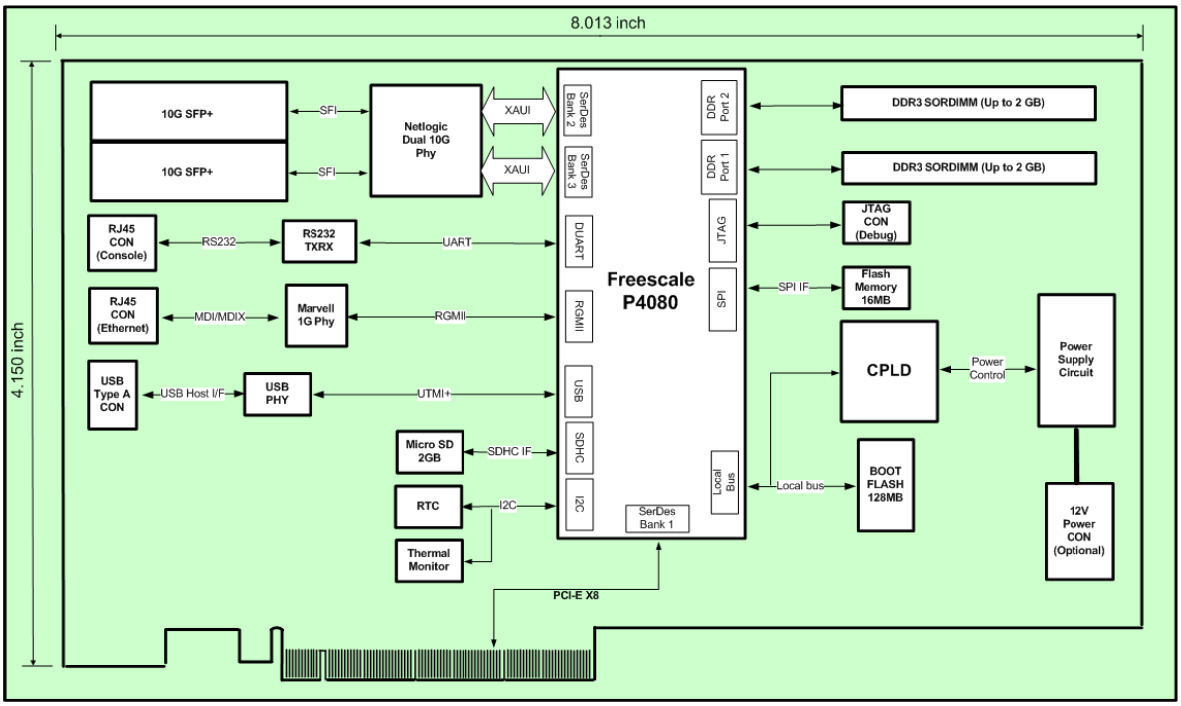
It is assumed that the reader is familiar with the P4080 microprocessor and P4080 Board Support Package (BSP).

1 About the P4080PCIe Development platform

The P4080PCIe board consists of four main blocks.

- CPU: Freescale's QorIQ P4080 multi-core processor with the e500mc core controls the 10G Ethernet, Management, Console and USB ports.
- CPLD: The Altera EPM1270 controls the power sequence, reset, control signals and MDIO/I2C/SPI interface.
- Power: Multiple power modules provide power conversion for various on board circuits.
- Netlogic AEL2020 dual 10G PHY for 10G Ethernet ports.

2 Getting to Know the P4080PCIe Development Board



Ethernet Port: RGMII, Management Port, J4

- The P4080 is connected with a single port PHY (88E1111TFBGA) through the RGMII interface.
- This port is used as the management port for the appliance.
- The J4 connector is a dual RJ45 connector that is accessible through the front panel.
- The RJ45 connector has bi-color LEDs: Green and Yellow.

DDR2/DDR3 DRAM Controller

- The P4080 supports 32 bit DDR2/DDR3 memory; however, on the P4080PCIe board only DDR3 is supported.
- The P4080PCIe utilizes two ECC Registered SORDIMM memory modules from ATP (P/N: XW1348E2GS-F-IM).
- Each of the memory modules is 2G Bytes

Serial Interface

- Serial Interface 0, UART1, Console Port, J4
- Serial interface 0 is a RS232 level serial interface that is used as the console port for the Appliance. The J4 connector is a dual RJ45 connector that is accessible through the front panel.
- The default setting for this port is: 115200 baud, 8 data bit, no stop bits and even parity.

USB 2.0

- The P4080 supports USB 2.0.
- The P4080PCIe utilizes a type A USB connector on the USB Interface for data storage.
- Connector CON1 is accessible through the front panel.
- The USB interface is designed to operate in host mode.
- The P4080PCIe is designed a self-powered device and as such it does not draw power from the USB port.

Micro SD (Optional)

- The P4080 supports a Micro SD interface.
- The capacity of the Super Talent Micro SD (P/N: MSD2GST_R) on the P4080PCIe board is 2G Bytes.

Thermal Monitor

- A thermal monitor is implemented on the P4080PCIe to monitor the junction temperature of the P4080.
- The Thermal Monitor P/N is ADT7461AARMZ.

External RTC

- An external system real time clock is implemented on the P4080PCIe. The RTC P/N is DS3232S#
- This RTC is battery powered.

SPI Flash Memory

- The P4080 has a SPI Interface. The SPI flash memory used on P4080PCIe is 16M Bytes from Spansion(P/N: S25FL128P0XNFI00). This flash memory can be used to store board info.

NETLOGIC PHY

- The AEL2020 Netlogic PHY has the following integrated peripherals:
    - XAUI ports
        - CML serial interface
        - XAUI Ports and CML Ports
        - The 2 XAUI ports are connected to the P4080, and the 2 high speed CML ports are connected to a 10G SFP+ module.
    - 10G SFP+ Transceiver (optional)
        - The PHY can access the SFP+ registers through I2C bus.
        - Two types of SFP+ modules could be used on the P4080PCIe: SR (shot range) and LR (long range).

3 Web Contents

Please refers to http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=P4080PCIE for the latest P4080PCIe documents and software.
Table 1 Website Contents lists a sample of the documents available on www.freescale.com.

Documentation
• N710 PCIE Adapter Users Guide and SW Release Notes
• Niagara 710B Hardware Specification
• Niagara 710 and 711 U-boot & Linux Upgrade Instructions
• N710 P4080 PCIE Adapter Software Proto Release Notes
Software Development Tools
• P4080 SDK2.3
• One Convergency P4080PCIe patch, P4080-PCIE-PRODUCTION-09-20-2011.tgz
• FSL-Adapter-TestPlan-1.2.doc
• Niagara710_Hardware_spec_rev03.pdf
• Release-notes.pdf

Table 1 Website Contents

4 Getting Started

This section describes how to use the P4080PCIe board and the components in the kit. This section also describes the PC requirements to develop applications using the P4080PCIe board.

Unpacking the Kit

The P4080PCIe is shipped with the items listed below:

- P4080PCIe card with Fan (1)
- Cat 5 cable (1)
- Console cable (1)
- Custom Power Supply (1)
- Power Cable – US (1)
- Screws for Bracket (2)

5 Basic Setup Procedures

The steps to getting started with the board are:

1. Setup the x86 host to run a Linux environment.
2. Insert the P4080PCIe board into an open PCIe slot on the host.
3. Connect a power source to the P4080PCIe board.
4. Connect to the Ethernet and console port on the P4080PCIe board.
5. Power on the board.

6. Boot Linux and login.

These steps are described in detail in the following sections.

Host Setup

The x86 host can run either Microsoft Environment or Linux environment. For illustration, Ubuntu 10.04 is used in this document.

Configure Host IP address

Assuming the host x86 machine has two Ethernet interfaces. Eth0 is for a production network (green LAN), and eth1 is for a lab network (red LAN). The Linux command needed to configure the host IP address for the eth1 interface is shown below:

```
$ sudo ifconfig eth1 192.168.2.1 netmask 255.255.255.0
```

Install TFTP daemon (optional)

One is free to use any tftp server they like. The command to use tftpd-hpa is shown below:

```
$ sudo aptitude install tftpd-hpa
[sudo] password for user:
Reading package lists... Done
Building dependency tree
Reading state information... Done
Reading extended state information
Initializing package states... Done
The following NEW packages will be installed:
  tftpd-hpa
```

Install terminal console software

The Minicom terminal console is used as an example in this document. Minicom should be pre-loaded with the ubuntu release. Alternatively, one can install minicom by running the following command:

```
$ sudo aptitude install minicom
```

6 Setting Up the P4080BPIe Board

Unpack the P4080PCIe card from the box.

Option 1: Standalone Mode

Connect the provided customer power supply (P/N SA-125A0IV) to the P4080PCIe's 6 pins power cable receptacle.

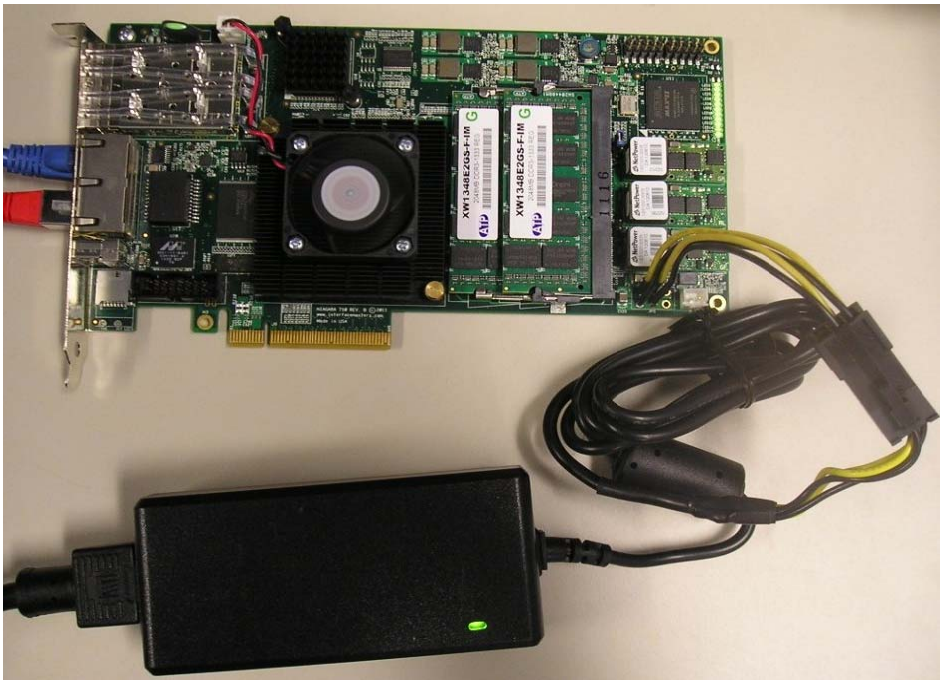


Figure 1 P4080PCIe standalone mode

Option 2: PCIe Mode

Insert the P4080PCIe to any open PCIe x8 or x16 slot as shown in Figure 2 P4080PCIe in a PCIe x8 slot

Figure 2 P4080PCIe in a PCIe x8 slot.

Connect the 5V power supply cable to a 6 pins PCI Express power cable receptacle. The receptacle usually labeled with “PCI”.

Connect Terminal access with an RS232 Cable

Connect the P4080PCIe console cable between the P4080PCIe console port and the x86 host serial, as shown in Figure 3 P4080PCIe wiring.

If your x86 host does not have a RS232 serial port, you may want to use a USB to serial cable (shown below). Check your linux console message for the correct serial port assignment.

```
[ 4011.742274] ftdi_sio ttyUSB0: FTDI USB Serial Device converter now disconnected from ttyUSB0
[ 4011.742310] ftdi_sio 2-3:1.0: device disconnected
[ 4014.280043] usb 2-4: new full speed USB device using ohci_hcd and address 6
[ 4014.507870] usb 2-4: configuration #1 chosen from 1 choice
[ 4014.516015] ftdi_sio 2-4:1.0: FTDI USB Serial Device converter detected
[ 4014.516074] usb 2-4: Detected FT232RL
[ 4014.516080] usb 2-4: Number of endpoints 2
[ 4014.516086] usb 2-4: Endpoint 1 MaxPacketSize 64
[ 4014.516091] usb 2-4: Endpoint 2 MaxPacketSize 64
[ 4014.516096] usb 2-4: Setting MaxPacketSize 64
[ 4014.518825] usb 2-4: FTDI USB Serial Device converter now attached to ttyUSB0
```

Serial port configuration: 115200baud, No parity, 8 data bit, 1 stop bit.

```
$ sudo minicom
```

Press CTRL-A, O, for minicom configuration

```
+-----------------------------------------+
| Filenames and paths                     |
| File transfer protocols                 |
| Serial port setup                       |
| Modem and dialing                       |
| Screen and keyboard                     |
| Save setup as dfl                       |
| Save setup as..                         |
| Exit                                    |
+-----------------------------------------+
```

Select “Serial port setup” for Serial Device selection and configuration.

```
+-----------------------------------------------------------------------+
| A -    Serial Device      : /dev/ttyUSB0                              |
| B - Lockfile Location     : /var/lock                                 |
| C -   Callin Program      :                                           |
| D -  Callout Program      :                                           |
| E -    Bps/Par/Bits       : 115200 8N1                                |
| F - Hardware Flow Control : Yes                                       |
| G - Software Flow Control : No                                        |
|                                                                       |
|    Change which setting?                                              |
+-----------------------------------------------------------------------+
```

Ethernet cable connection

Connect the P4080PCIe management port to the Host Ethernet port, as shown in Figure 3 P4080PCIe Wiring.

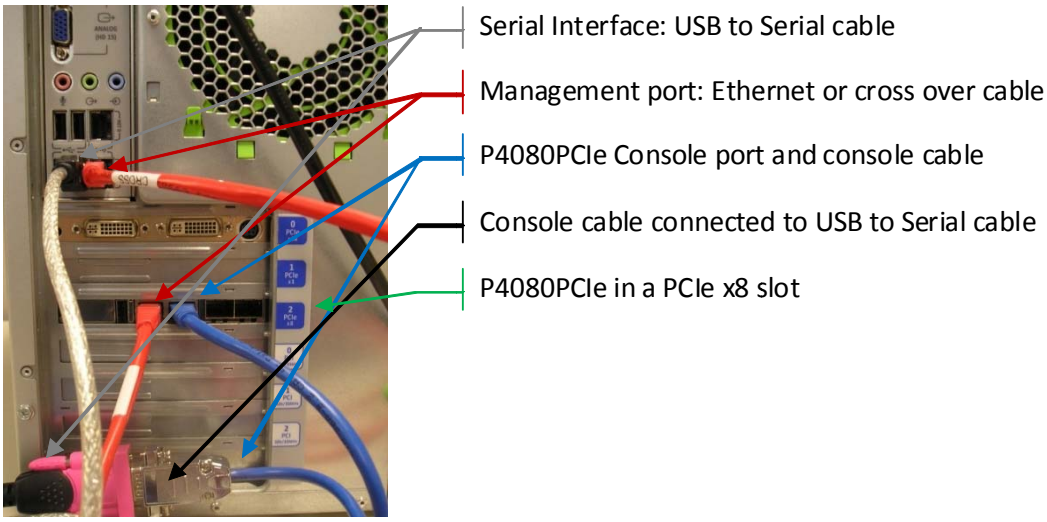


Figure 3 P4080PCIe Wiring.

7 Linux Boot Process

Invoke the terminal console software

Type in the following command to invoke the terminal console:

$ sudo minicom

Power-on the P4080PCIe unit to start the boot up process. The console will display a countdown message from 3 to 0 on the terminal. Press the enter key during the countdown to abort normal auto boot, which should get you to a command prompt: "=>".

```
U-Boot MPS N710 2010.12 (Sep 20 2011 - 13:24:26)

CPU0: P4080E, Version: 2.0, (0x82080020)
Core: E500MC, Version: 2.0, (0x80230020)
Clock Configuration:
       CPU0:1333.333 MHz, CPU1:1333.333 MHz, CPU2:1333.333 MHz, CPU3:1333.333 M
       CPU4:1333.333 MHz, CPU5:1333.333 MHz, CPU6:1333.333 MHz, CPU7:1333.333 M
       CCB:666.667 MHz,
       DDR:666.667 MHz (1333.333 MT/s data rate) (Asynchronous), LBC:83.333 MHz
       FMAN1: 500 MHz
       FMAN2: 500 MHz
       PME: 333.333 MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
Sys ID: 0x0711, Board Version 0x 0, CPLD Ver: 0x0336-bit Addressing
Reset Configuration Word (RCW):
       00000000: 10600000 00000000 20201820 0000cccc
       00000010: 08402200 3c3c2000 de800000 61000000
       00000020: 00300000 00000000 00000000 008b0000
       00000030: 00000000 00000000 00000000 00000000
I2C:   ready
DRAM:  Initializing....using SPD
Detected RDIMM(s)
Detected RDIMM(s)
CS2 is disabled.
CS3 is disabled.
CS2 is disabled.
CS3 is disabled.
Implementing recommended DDR3 Init sequence
Enabling controller 0
Enabling controller 1
2 GiB left unmapped
```

```
    DDR: 4 GiB (DDR3, 64-bit, CL=8, ECC on)
       DDR Controller Interleaving Mode: cache line
       DDR Chip-Select Interleaving Mode: CS0+CS1
Testing 0x00000000 - 0x7fffffff
Testing 0x80000000 - 0xffffffff
Remap DDR 2 GiB left unmapped

Relocating u-boot to 0x7ff30000
POST memory PASSED
FLASH: 128 MiB
L2:    128 KB enabled
Corenet Platform Cache: 2048 KB enabled
p4080_erratum_serdes8 enable Bank3
p4080_erratum_serdes8 enable Bank2
p4080_erratum_serdes9 reset Bank2
p4080_erratum_serdes9 reset Bank3
MMC:  FSL_ESDHC: 0
EEPROM: N710 v2
PCIe1: Endpoint,  with errors.  Clearing.  Now 0x00000000
Setting up PCIE Outbound Regions
        Region 0:
        bus start = 0x0
        bus end = 0x20000000
        phys_start = 0xc00000000
Outbound memory range: 0:20000000
PCICSRBAR @ 0xff000000
PCI reg:0 0000000c00000000:0000000000000000 0000000020000000 00000000
PCI reg:1 0000000ffe000000:00000000ff000000 0000000001000000 00000100
x8, regs @ 0xfe200000
fsl_pci_config_unlock CFG_READY
PCIe1: Bus 00 - 00
In:    serial
Out:   serial
Err:   serial
Net:   Fman: Uploading microcode version 101.8.0.
Dtsec: PHY is Marvell MV88E1111 (1410cc2)
AEL2020 Config Phy
AEL2020 Config Phy ERRATUM_SERDES9
        AEL2020 FM1 Phy
...waiting for ael2020 reset to clear
AEL2020 1.C001 = 0x2
10GE Port 0 SFP Module NOT Detected, TX Not Enabled
Fman: Uploading microcode version 101.8.0.
AEL2020 Config Phy
AEL2020 Config Phy ERRATUM_SERDES9
        AEL2020 FM2 Phy
...waiting for ael2020 reset to clear
AEL2020 1.C001 = 0x1
10GE Port 1 SFP Module NOT Detected, TX Not Enabled
FM1@DTSEC2, FM1@TGEC1, FM2@TGEC1
ADT7461 Detected
STTS2002 SPD 0 Detected
STTS2002 SPD 1 Detected
Setting up MX CP Bridge with Local Device Side PCIE window 0x8000000
N710 Booted from Primary Flash Bank 0

=>
```

Setup and verify the Ethernet port between the P4080PCIe and the Host PC

To setup and verify a working Ethernet port between the P4080PCIe and the Host, type the following commands at the uboot prompt “=>”.

```
=> setenv ethact FM1@DTSEC2
=> setenv serverip 192.168.2.1
=> setenv gatewayip 192.168.2.1
=> setenv ipaddr 192.168.2.10
=> ping $serverip
```

Normal Linux boot

The default uboot has the following pre-defined environment variables (the command *pri* prints the environment settings):

```
=> pri
…
bootargs=root=/dev/ram console=ttyS0,115200
bootcmd=bootm 0xe8020000 0xe9300000 0xe8800000
bootdelay=3
…
```

If you did interrupt the countdown for the boot process, type the following command to boot with pre-loaded linux image from the flash memory.

```
=> bootm
```

If you did not intercept the boot process, P4080PCIe will boot with pre-loaded linux image from the flash memory and the following data should match the boot log.

```
## Booting kernel from Legacy Image at e8020000 ...
   Image Name:   Linux-2.6.34.6
   Created:      2011-08-16   5:13:17 UTC
   Image Type:   PowerPC Linux Kernel Image (gzip compressed)
   Data Size:    3369364 Bytes = 3.2 MiB
   Load Address: 00000000
   Entry Point:  00000000
   Verifying Checksum ... OK
## Loading init Ramdisk from Legacy Image at e9300000 ...
   Image Name:   uboot initramfs rootfs
   Created:      2011-08-16   5:48:42 UTC
   Image Type:   PowerPC Linux RAMDisk Image (gzip compressed)
   Data Size:    19255434 Bytes = 18.4 MiB
   Load Address: 00000000
   Entry Point:  00000000
   Verifying Checksum ... OK
## Flattened Device Tree blob at e8800000
   Booting using the fdt blob at 0xe8800000
   Uncompressing Kernel Image ... OK
   Loading Ramdisk to 2eda2000, end 2ffff08a ... OK
   Loading Device Tree to 00ff3000, end 00fff9b7 ... OK
Using P4080 N710 machine description
Memory CAM mapping: 256/256/256 Mb, residual: 3328Mb
Linux version 2.6.34.6 (bhagya@localhost.localdomain) (gcc version 4.5.1 (Sourcery G++ Lite
20101Found initrd at 0xeeda2000:0xeffff08a
No /soc@ffe000000/qman@318000 property 'fsl,qman-fqd', using lmb_alloc(0000000000200000)
No /soc@ffe000000/qman@318000 property 'fsl,qman-pfdr', using lmb_alloc(0000000001000000)
Qman ver:0a01,01,01
No /soc@ffe000000/bman@31a000 property 'fsl,bman-fbpr', using lmb_alloc(0000000001000000)
Bman ver:0a02,01,00
pme: No /soc@ffe000000/pme@316000 property 'fsl,pme-pdsr', using lmb_alloc(0x0000000001000000)
pme: No /soc@ffe000000/pme@316000 property 'fsl,pme-sre', using lmb_alloc(0x0000000000a00000)
USDPAA region at f8000000:4000000
CPU maps initialized for 1 thread per core
bootconsole [udbg0] enabled
setup_arch: bootmem
Found FSL PCI host bridge at 0x0000000ffe200000. Firmware bus number: 0->0
PCI host bridge /pcie@ffe200000  ranges:
 MEM 0x0000000c00000000..0x0000000c1fffffff -> 0x00000000e0000000
  IO 0x0000000ff8000000..0x0000000ff800ffff -> 0x0000000000000000
P4080_EP:: Before writing, read from BAR0 d1000000
Setting CCSR size as 0xff000000
P4080_EP:: Value read from BAR0 first time is ff000000
P4080_EP:: BAR address after host enumeration d1000000
/pcie@ffe200000: PCICSRBAR @ 0xdf000000
Inbound RAM test memory physical address is 0x6aac70, inbound_ram_test[3] is 4
P4080_EP: USDPAA shared memory start: f8000000
P4080_EP: Updated TAR value with USDPAA shared memory is: f8000
/pcie@ffe200000: DMA window size is 0xdf000000
P4080 N710 board from Interface Masters and MPS
arch: exit
```

```
Zone PFN ranges:
  DMA      0x00000000 -> 0x00030000
  Normal   empty
  HighMem  0x00030000 -> 0x00100000
Movable zone start PFN for each node
early_node_map[1] active PFN ranges
    0: 0x00000000 -> 0x00100000
MMU: Allocated 1088 bytes of context maps for 255 contexts
PERCPU: Embedded 9 pages/cpu @c3010000 s16276 r8192 d12396 u65536
pcpu-alloc: s16276 r8192 d12396 u65536 alloc=16*4096
pcpu-alloc: [0] 0 [0] 1 [0] 2 [0] 3 [0] 4 [0] 5 [0] 6 [0] 7
Built 1 zonelists in Zone order, mobility grouping on.  Total pages: 1040384
Kernel command line: root=/dev/ram console=ttyS0,115200
PID hash table entries: 4096 (order: 2, 16384 bytes)
Dentry cache hash table entries: 131072 (order: 7, 524288 bytes)
Inode-cache hash table entries: 65536 (order: 6, 262144 bytes)
Placing 64MB software IO TLB between c3149000 - c7149000
software IO TLB at phys 0x3149000 - 0x7149000
Memory: 3940836k/4194304k available (6808k kernel code, 253468k reserved, 256k data, 420k bss,
2)Kernel virtual memory layout:
  * 0xfff67000..0xfffff000  : fixmap
  * 0xffc00000..0xffe00000  : highmem PTEs
  * 0xffbea000..0xffc00000  : early ioremap
  * 0xf1000000..0xffbea000  : vmalloc & ioremap
Hierarchical RCU implementation.
RCU-based detection of stalled CPUs is enabled.
NR_IRQS:512 nr_irqs:512
mpic: Setting up MPIC " OpenPIC  " version 1.2 at ffe040000, max 8 CPUs
mpic: ISU size: 256, shift: 8, mask: ff
mpic: Initializing for 256 sources
clocksource: timebase mult[5ffffff] shift[22] registered
Console: colour dummy device 80x25
Mount-cache hash table entries: 512
mpic: requesting IPIs...
Processor 1 found.
Processor 2 found.
Processor 3 found.
Processor 4 found.
Processor 5 found.
Processor 6 found.
Processor 7 found.
Brought up 8 CPUs
NET: Registered protocol family 16

e500 family performance monitor hardware support registered
N710 CPLD Reset Control mapped to 0xf1048008
clkc0csr mapped to 0xf104c000
PCI: Probing PCI hardware
bio: create slab <bio-0> at 0
vgaarb: loaded
SCSI subsystem initialized
usbcore: registered new interface driver usbfs
usbcore: registered new interface driver hub
usbcore: registered new device driver usb
Bman err interrupt handler present
Bman portal initialised, cpu 0
Bman portal (slave) initialised, cpu 1
Bman portal (slave) initialised, cpu 2
Bman portal (slave) initialised, cpu 3
Bman portal (slave) initialised, cpu 4
Bman portal (slave) initialised, cpu 5
Bman portal (slave) initialised, cpu 6
Bman portal (slave) initialised, cpu 7
Bman: reserved bpid 0, seeded 256 items
Bman: reserved bpid 7
Bman: reserved bpid 8
Bman: reserved bpid 9
Bman portals initialised
Qman err interrupt handler present
Qman portal initialised, cpu 0
```

```
Qman portal (slave) initialised, cpu 1
Qman portal (slave) initialised, cpu 2
Qman portal (slave) initialised, cpu 3
Qman portal (slave) initialised, cpu 4
Qman portal (slave) initialised, cpu 5
Qman portal (slave) initialised, cpu 6
Qman portal (slave) initialised, cpu 7
Qman portals initialised
Switching to clocksource timebase
NET: Registered protocol family 2
IP route cache hash table entries: 32768 (order: 5, 131072 bytes)
TCP established hash table entries: 131072 (order: 8, 1048576 bytes)
TCP bind hash table entries: 65536 (order: 7, 524288 bytes)
TCP: Hash tables configured (established 131072 bind 65536)
TCP reno registered
UDP hash table entries: 512 (order: 2, 16384 bytes)
UDP-Lite hash table entries: 512 (order: 2, 16384 bytes)
NET: Registered protocol family 1
RPC: Registered udp transport module.
RPC: Registered tcp transport module.
RPC: Registered tcp NFSv4.1 backchannel transport module.
Trying to unpack rootfs image as initramfs...
Freeing initrd memory: 18804k freed
Setting Freescale static PAMU/IOMMU configuration
Freescale PowerQUICC MII Bus: probed
MII Addr 8 read PhyID 0x0
phy_scan_fixups
phy_scan_fixups
mdio_bus mdio@ffe4e1120: /soc@ffe000000/fman@400000/mdio@e1120/p4080ds-mdio0 has invalid PHY
addsmdio_bus mdio@ffe4e1120: /soc@ffe000000/fman@400000/mdio@e1120/p4080ds-mdio1 has invalid PHY
addsmdio_bus mdio@ffe4e1120: /soc@ffe000000/fman@400000/mdio@e1120/p4080ds-mdio2 has invalid PHY
addsmdio_bus mdio@ffe4e1120: /soc@ffe000000/fman@400000/mdio@e1120/p4080ds-mdio3 has invalid PHY
addsFreescale XGMAC MDIO Bus: probed
mdio_bus mdio: /soc@ffe000000/fman@400000/mdio@f1000/p4080ds-xmdio1 has invalid PHY address
mdio_bus mdio: /soc@ffe000000/fman@400000/mdio@f1000/p4080ds-xmdio3 has invalid PHY address
Freescale P4080DS MDIO Bus: probed
MII Addr 0 read PhyID 0x1410cc2
phy_scan_fixups
phy_scan_fixups
Freescale P4080DS MDIO Bus: probed
MII Addr 1 read PhyID 0x3429081
phy_scan_fixups
phy_scan_fixups
Freescale P4080DS MDIO Bus: probed
MII Addr 0 read PhyID 0x3429081
phy_scan_fixups
phy_scan_fixups
audit: initializing netlink socket (disabled)
type=2000 audit(1.148:1): initialized
highmem bounce pool size: 64 pages
NTFS driver 2.1.29 [Flags: R/O].
JFFS2 version 2.2. (NAND) .. 2001-2006 Red Hat, Inc.
msgmni has been set to 1205
alg: No test for cipher_null (cipher_null-generic)
alg: No test for ecb(cipher_null) (ecb-cipher_null)
alg: No test for digest_null (digest_null-generic)
alg: No test for compress_null (compress_null-generic)
alg: No test for stdrng (krng)
io scheduler noop registered
io scheduler deadline registered
io scheduler cfq registered (default)
Generic non-volatile memory driver v1.1
ePAPR hypervisor byte channel console driver
ehv-bc: no hypervisor found
Serial: 8250/16550 driver, 4 ports, IRQ sharing enabled
serial8250.0: ttyS0 at MMIO 0xffe11c500 (irq = 36) is a 16550A
console [ttyS0] enabled, bootconsole disabled
console [ttyS0] enabled, bootconsole disabled
serial8250.0: ttyS1 at MMIO 0xffe11c600 (irq = 36) is a 16550A
serial8250.0: ttyS2 at MMIO 0xffe11d500 (irq = 37) is a 16550A
```

```
serial8250.0: ttyS3 at MMIO 0xffe11d600 (irq = 37) is a 16550A
brd: module loaded
loop: module loaded
nbd: registered device at major 43
Freescale hypervisor management driver
fsl-hv: no hypervisor found
Freescale USDPAA shared memory driver
st: Version 20081215, fixed bufsize 32768, s/g segs 256
fe8000000.flash: Found 1 x16 devices at 0x0 in 16-bit bank
 Amd/Fujitsu Extended Query Table at 0x0040
fe8000000.flash: CFI does not contain boot bank location. Assuming top.
number of CFI chips: 1
RedBoot partition parsing not available
fsl_espi ffe110000.spi: at 0xf11be000 (irq = 53)
m25p80 spi32766.0: s25sl12801 (16384 Kbytes)
Creating 4 MTD partitions on "spi32766.0":
0x000000000000-0x000000100000 : "u-boot"
0x000000100000-0x000000600000 : "kernel"
0x000000600000-0x000000700000 : "dtb"
0x000000700000-0x000001000000 : "file system"
MII Addr 0 read PhyID 0xffffffff
MII Addr 1 read PhyID 0xffffffff
MII Addr 2 read PhyID 0xffffffff
MII Addr 3 read PhyID 0xffffffff
MII Addr 4 read PhyID 0xffffffff
MII Addr 5 read PhyID 0xffffffff
MII Addr 6 read PhyID 0xffffffff
MII Addr 7 read PhyID 0xffffffff
MII Addr 8 read PhyID 0xffffffff
MII Addr 9 read PhyID 0xffffffff
MII Addr 10 read PhyID 0xffffffff
MII Addr 11 read PhyID 0xffffffff
MII Addr 12 read PhyID 0xffffffff
MII Addr 13 read PhyID 0xffffffff
MII Addr 14 read PhyID 0xffffffff
MII Addr 15 read PhyID 0xffffffff
MII Addr 16 read PhyID 0xffffffff
MII Addr 17 read PhyID 0xffffffff
MII Addr 18 read PhyID 0xffffffff
MII Addr 19 read PhyID 0xffffffff
MII Addr 20 read PhyID 0xffffffff
MII Addr 21 read PhyID 0xffffffff
MII Addr 22 read PhyID 0xffffffff
MII Addr 23 read PhyID 0xffffffff
MII Addr 24 read PhyID 0xffffffff
MII Addr 25 read PhyID 0xffffffff
MII Addr 26 read PhyID 0xffffffff
MII Addr 27 read PhyID 0xffffffff
MII Addr 28 read PhyID 0xffffffff
MII Addr 29 read PhyID 0xffffffff
MII Addr 30 read PhyID 0xffffffff
MII Addr 31 read PhyID 0xffffffff
Fixed MDIO Bus: probed
Intel(R) PRO/1000 Network Driver - version 7.3.21-k5-NAPI
Copyright (c) 1999-2006 Intel Corporation.
e1000e: Intel(R) PRO/1000 Network Driver - 1.0.2-k2
e1000e: Copyright (c) 1999 - 2009 Intel Corporation.
cpu0/0: > WARNING (FM-PCD) [drivers/net/dpa/NetCommSw/Peripherals/FM/Pcd/fm_kg.c:1644 KgConfig]:
cpu0/0: numOfSchemes was defined 0 by user, re-defined by driver to FM_PCD_KG_NUM_OF_SCHEMES
cpu0/0:
cpu0/0: > WARNING (FM-PCD) [drivers/net/dpa/NetCommSw/Peripherals/FM/Pcd/fm_kg.c:1644 KgConfig]:
cpu0/0: numOfSchemes was defined 0 by user, re-defined by driver to FM_PCD_KG_NUM_OF_SCHEMES
cpu0/0:
Freescale FM module (Aug 16 2011:10:41:35)
cpu0/0: fsl_mac: FSL FMan MAC API based driver ()
mac_probe, get phy config
mac-api.c init()
mac-api.c init() res64 0xffe4e2000, remap 0xf9384000
cpu0/0: fsl_mac: ffe4e2000.ethernet: FMan dTSEC version: 0x08240101
cpu0/0: fsl_mac: ffe4e2000.ethernet: FMan MAC address: 00:0c:bd:00:dc:32
```

```
setup_xgmac
mac_probe, get phy config
mac-api.c init()
mac-api.c init() res64 0xffe4f0000, remap 0xf9390000
Calling FM_MAC_ConfigResetOnInit
cpu0/0: FmResetMac 10G Mac reset
cpu0/0: Applying 10G tx-ecc error workaround (FMAN11) ...
cpu0/0: done.
cpu0/0: fsl_mac: ffe4f0000.ethernet: FMan XGEC version: 0x0001032c
cpu0/0: fsl_mac: ffe4f0000.ethernet: FMan MAC address: 00:0c:bd:00:dc:33
setup_xgmac
mac_probe, get phy config
mac-api.c init()
mac-api.c init() res64 0xffe5f0000, remap 0xf93a8000
Calling FM_MAC_ConfigResetOnInit
cpu0/0: FmResetMac 10G Mac reset
cpu0/0: Applying 10G tx-ecc error workaround (FMAN11) ...
cpu0/0: done.
cpu0/0: fsl_mac: ffe5f0000.ethernet: FMan XGEC version: 0x0001032c
cpu0/0: fsl_mac: ffe5f0000.ethernet: FMan MAC address: 00:0c:bd:00:dc:34
cpu0/0: fsl_dpa: FSL DPAA Ethernet driver ()
cpu0/0: fsl_dpa: ethernet.27: dpaa_eth.c:1744:dpa_bp_create() eth%d: Using private BM buffer
pooscpu0/0: Using dynamic RX QM frame queues
cpu0/0: Using dynamic TX QM frame queues
cpu0/0: fsl_oh: FSL FMan Offline Parsing port driver ()
ehci_hcd: USB 2.0 'Enhanced' Host Controller (EHCI) Driver
fsl-ehci fsl-ehci.0: Freescale On-Chip EHCI Host Controller
fsl-ehci fsl-ehci.0: new USB bus registered, assigned bus number 1
fsl-ehci fsl-ehci.0: irq 44, io base 0xffe210000
fsl-ehci fsl-ehci.0: USB 2.0 started, EHCI 1.00
hub 1-0:1.0: USB hub found
hub 1-0:1.0: 1 port detected
fsl-ehci fsl-ehci.1: Freescale On-Chip EHCI Host Controller
fsl-ehci fsl-ehci.1: new USB bus registered, assigned bus number 2
fsl-ehci fsl-ehci.1: can't setup
fsl-ehci fsl-ehci.1: USB bus 2 deregistered
fsl-ehci fsl-ehci.1: init fsl-ehci.1 fail, -110
fsl-ehci: probe of fsl-ehci.1 failed with error -110
ohci_hcd: USB 1.1 'Open' Host Controller (OHCI) Driver
Initializing USB Mass Storage driver...
usbcore: registered new interface driver usb-storage
USB Mass Storage support registered.
rtc-ds3232 2-0068: rtc core: registered ds3232 as rtc0
adt7461_probe called
adt7461 2-004c: adt7461 ADT7461 found
Thermal Device ADT7461 IRQ 16 was detected
ADT7461 Procfs setup successful
EDAC MC: Ver: 2.1.0 Aug 16 2011
Freescale(R) MPC85xx EDAC driver, (C) 2006 Montavista Software
EDAC PCI0: Giving out device to module 'MPC85xx_edac' controller 'mpc85xx_pci_err': DEV
'ffe2000)MPC85xx_edac acquired irq 17 for PCI Err
MPC85xx_edac PCI err registered
sdhci: Secure Digital Host Controller Interface driver
sdhci: Copyright(c) Pierre Ossman
mmc0: SDHCI controller on ffe114000.sdhc [ffe114000.sdhc] using DMA
caam ffe300000.crypto: device ID = 0x0a10020000000000
caam ffe300000.crypto: job rings = 4, qi = 1
alg: No test for authenc(hmac(sha1),cbc(aes)) (authenc-hmac-sha1-cbc-aes-caam)
caam ffe300000.crypto: authenc-hmac-sha1-cbc-aes-caam
alg: No test for authenc(hmac(sha256),cbc(aes)) (authenc-hmac-sha256-cbc-aes-caam)
caam ffe300000.crypto: authenc-hmac-sha256-cbc-aes-caam
alg: No test for authenc(hmac(sha1),cbc(des3_ede)) (authenc-hmac-sha1-cbc-des3_ede-caam)
caam ffe300000.crypto: authenc-hmac-sha1-cbc-des3_ede-caam
alg: No test for authenc(hmac(sha256),cbc(des3_ede)) (authenc-hmac-sha256-cbc-des3_ede-caam)
caam ffe300000.crypto: authenc-hmac-sha256-cbc-des3_ede-caam
alg: No test for authenc(hmac(sha1),cbc(des)) (authenc-hmac-sha1-cbc-des-caam)
caam ffe300000.crypto: authenc-hmac-sha1-cbc-des-caam
alg: No test for authenc(hmac(sha256),cbc(des)) (authenc-hmac-sha256-cbc-des-caam)
caam ffe300000.crypto: authenc-hmac-sha256-cbc-des-caam
fsl-pme ffe316000.pme: ver: 0x00100201
```

```
sample_db: starting pme2 sample DB initialisation
sample_db: db for pme ver 2.1 or greater
sample_db: pme2 sample DB initialised
Freescale pme2 db driver
Freescale pme2 scan driver
fsl-pme2-scan: device pme_scan registered
IPv4 over IPv4 tunneling driver
GRE over IPv4 tunneling driver
TCP cubic registered
Initializing XFRM netlink socket
NET: Registered protocol family 10
IPv6 over IPv4 tunneling driver
NET: Registered protocol family 17
NET: Registered protocol family 15
rtc-ds3232 2-0068: setting system clock to 2011-09-10 14:33:54 UTC (1315665234)
Freeing unused kernel memory: 256k init
Mounting /proc and /sys
Starting the hotplug events dispatcher udevd
Synthesizing initial hotplug events
mmc0: new high speed SD card at address 0002
mmcblk0: mmc0:0002 00000 1.86 GiB
 mmcblk0: p1
Setting the hostname to p4080
Mounting filesystems
Starting syslogd and klogd
Running sysctl
Setting up networking on loopback device:

Warning: no IPADDR is set, please set this from the ltib
config screen, or directly in /etc/rc.d/rc.conf.
IP address setup bypassed

Starting inetd:
Starting the port mapper:
Starting the dropbear ssh server:
Starting the boa webserver:


        Welcome to the LTIB Embedded Linux Environment

!!!!! WARNING !!!!!!!

The default password for the root account is: root
please change this password using the 'passwd' command
and then edit this message (/etc/issue) to remove this message

p4080 login:
```

Login to Linux with the userid “root” and password “root” should be used to log into the P4080PCIe board.

```
p4080 login: root
Password: root
[root@p4080 /root]#
```

Reset the P4080PCIe board

The P4080PCIe’s CPLD supports reset to current bank or alternate memory bank.

Software Reset:

- In u-boot prompt, issue “n710_cpld” or “n710_cpld altbank” to reset the P4080PCIe board.

Hardware Reset:

- Power On Reset (PORST) is map to JP2. One can reset the P4080PCIe board by shorting the jumper J2.

8 Revision History

Table 10. Document Revision History

Rev.	Date	Substantive Changes(s)
0.0	10/2011	Initial release.

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