National Semiconductor

400022

F100K ECL Logic

Databook and Design Guide

F100K ECL
DATABOOK

1989 Edition

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Introduction

National's F100K ECL family has gained acceptance as the standard subnanosecond logic and memory family used in high-speed, next generation systems. Utilizing the advanced Isoplanar-Z process, F100K circuits offer specification of DC and AC parameters over a $-4.2V$ to $-4.8V$ V_{EE} at 0°C to 85°C case temperature, full voltage and temperature compensation, and ease-of-use features, providing a high performance, cost-effective ECL logic family.

F100K Data Book

Product Index and Selection Guide

The Product Index is a numerical list of all device types contained in this book. The Selection Guide groups the products by function.

F100K Design Guide—Section 5

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Alpha-Numeric Index

Alpha-Numeric Index (Continued)

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F100K Product Selection Guide

Gates

Function	Device	Inputs/ Gate	No. of Gates	Leads
OR/NOR/Exclusive OR				
Triple 5-Input OR/NOR	100101	5	3	24
Quint 2-Input OR/NOR	100102	2	5	24
Dual Input OR/NOR	11C01	4/5	2	16
Quint Exclusive OR/NOR	100107	2	5	24
AND/NAND				
Quint 2-Input AND/NAND	100104	2	5	24
OR-AND/OR-AND-INVERT				
Triple 2-Wide OA/OAI	100117	2	3	24
5-Wide 5, 4, 4, 4, 2 OA/OAI	100118	5/4/4/4/2	1	24

Flip-Flops

Function	Device	Clock Edge	Direct Set	Direct Clear	Complementary Outputs	Leads
Triple D Flip-Flop	100131	⎍	Yes	Yes	Yes	24
Triple J-K Flip-Flop	100135	⎍	Yes	Yes	Yes	24
Hex D Flip-Flop	100151	⎍	No	Yes	Yes	24
750 MHz D Flip-Flop	11C06	⎍	No	No	Yes	16
Master-Slave D Flip-Flop	11C70	⎍	Yes	Yes	Yes	16
Low Power Hex D Flip-Flop	100351	⎍	No	Yes	Yes	24

Latches

Function	Device	Enable Inputs	Complementary Outputs	Direct Set	Direct Clear	Leads
Triple D Latch	100130	4(L)	Yes	Yes	Yes	24
Hex D Latch	100150	2(L)	Yes	No	Yes	24
Quad 2-Input Mux/Latch	100155	2(L)	Yes	No	Yes	24
Mask-Merge Latch	100156	1(L)	No	No	No	24
Quint 100K-to-10K Latch	100175	2(L)	No	No	Yes	24
Low Power Hex D Latch	100350	2(L)	Yes	No	Yes	24

Multiplexers/Demultiplexers/Decoders

Function	Device	Enable Inputs	Complementary Outputs	Leads
Multiplexers				
Dual 8-Input	100163		No	24
Triple 4-Input	100171	1(L)	Yes	24
Quad 2-Input Mux/Latch	100155	2(L)	Yes	24
16-Input	100164		No	24
Decoders/Demultiplexers				
Dual 1 of 4/Single 1 of 8	100170	2(L) & 2(L)	No	24

Translators

Function	Device	Enable Inputs	Latch	Complementary	Leads
Hex TTL-to-100K ECL	100124	1(H)	No	Outputs	24
Hex 100K ECL-to-TTL	100125		No	Inputs	24
Octal Bidirectional ECL/TTL	100128	1(H)	Yes		24
Quint 100K-to-10K	100175	2(H)	Yes		24
Low Power Hex TTL-to-100K ECL	100324	1(H)	No	Outputs	24
Low Power Hex 100K ECL-to-TTL	100325		No	Inputs	24

Registers/Shift Registers

Function	Device	Clock Inputs	Complementary Outputs	Leads
Shift Registers				
4-Bit Bidirectional Shift Reg	100136	⎍	Yes	24
8-Bit Shift Register	100141	⎍	No	24

Buffers/Drivers/Receivers

Function	Device	Output Polarity	25Ω Drive	Output Cut-Off	Leads
Buffers/Inverters					
9-Bit Inverter	100121	Inverting	No	No	24
9-Bit Buffer	100122	Non-Inverting	No	No	24
Drivers/Bus Drivers					
Quad Line Driver	100112	Differential	No	No	24
Quad Line Driver	100113	Differential	No	No	24
Low Skew Quad Driver	100115	Differential	No	No	16
Hex Bus Driver	100123	Non-Inverting	Yes	Yes	24
9-Bit Backplane Driver	100126	Non-Inverting	No	No	24
Receivers/Transceivers					
Quint Differential Line Receiver	100114	Differential	No	No	24
Quint Full Duplex Line Transceiver	100250	Differential	No	No	24

Counters/Prescalers

Function	Device	Parallel Entry	Reset	Up/Down	Leads
Counters					
4-Bit Binary Counter	100136	S	S/A	Yes	24
1 GHz Divide-by-Four Counter	11C05		No	No	16
Prescalers					
650 MHz Prescaler	11C90		No	No	16
650 MHz Prescaler	11C91		No	No	16

Arithmetic Operators

Function	Device	Features	Leads
High Speed 6-Bit Adder	100180		24
Carry Lookahead	100179		24
4-Bit Binary/BCD ALU	100181	8 Logic/8 Arithmetic Ops	24
9-Bit Wallace Tree Adder	100182	Expandable	24
2 x 8-Bit Recode Multiplier	100183		24
Dual 9-Bit Parity Checker/Generator	100160	Expandable	24
9-Bit Comparator	100166	Expandable	24
8-Input Priority Encoder	100165	Dual 4-Bit/Single 8-Bit	24
8-Bit Shift Matrix	100158	Barrel Shift, Backfill	24
4-Bit Mask-Merge/Latch	100156	Bit-Selectable Merge	24
4 x 4-Bit Content Addressable Memory	100142		24

Memories

Function	Device	Leads
Register Files/RAMs		
16 x 4-Bit RAM	100145	24
16 x 4-Bit RAM	10145A	16
16 x 4-Bit RAM	10402	16
1024 x 1-Bit RAM	100415	16
1024 x 1-Bit RAM	10415	16
256 x 4-Bit RAM	100422	24
256 x 4-Bit RAM	10422	24
Specialty Memories		
4 x 4-Bit Content Addressable Memory	100142	24

Section 1

Family Overview

Section 1 Contents

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Family Overview

Introduction

Systems designers have found that Emitter Coupled Logic (ECL) circuits offer significant advantages to high-speed systems. These advantages include high switching rates with moderate power consumption, low propagation delays with moderate edge rates, and the ability to drive low impedance transmission lines. Most F100K devices have 50 kΩ pull-down resistors on all the inputs.

The F100K ECL family is the realization of refinements made on ECL design to produce a family of ultrafast logic and memory components. These components are capable of providing ultimate performance for packaged SSI/MSI, are easy to use, and cost effective.

F100K ECL has been accepted as the standard subnanosecond logic and memory family used in high-speed, next generation systems. The advance into complex LSI and gate arrays is fully supported by the F100K SSI/MSI parts.

Design Philosophy

F100K was designed to meet four key requirements: high speed at reduced power, high level of on-chip integration, flexible logic functions, and optimum I/O pin assignment.

Subnanosecond Gate Delays

The subnanosecond internal gate delays of F100K are obtained by the use of ECL design techniques and the advanced Isoplanar-Z process. Many circuit approaches were carefully considered prior to selecting the optimum gate configuation for the F100K family. The emitter-follower current-switch (E^2CL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability; the CML gate has low noise margins. The 2-½D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and voltage compensation characteristics that lead to the loss of system noise immunity.

The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

- High fan-out capability
- Simultaneous complementary outputs
- Excellent AC characteristics
- Compatibility with existing ECL logic and memories
- Internal series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

In order to ease drive requirements all circuit inputs were designed to have similar loading characteristics; i.e., buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than three unit loads. Full compensation was selected for the F100K Family to provide improved switching characteristics. Full compensation results in relatively constant signal levels and thresholds and in improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter AC window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system AC performance due solely to full compensation *(Figure 1-1)*. And, the improved speed has been achieved at reduced power. Power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a −4.5V V_{EE} power supply. F100K is specified at a V_{EE} power supply of −4.2V to −4.8V, but a −5.2V ±10% power supply can be used to interface with 2 ns ECL families.

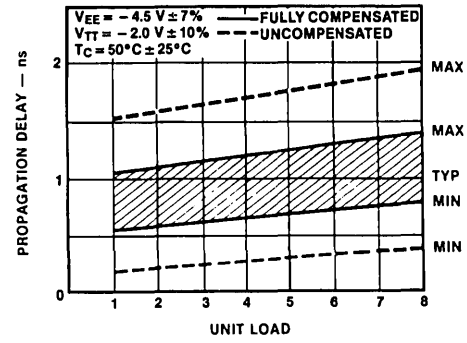

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FIGURE 1-1. Comparison of Propagation Delays

High On-Chip Integration

Higher on-chip integration is made possible by using the 24-pin package to increase the number of signal pins by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximize the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve the system needs presently requiring 25 functions in the ECL 10K family.

Flexibility and Pin Assignment

F100K was planned to minimize to total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system

performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and to ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the DIP package to ease system design and to provide low-inductance connections to the chip.
- Provide two V_{CC} pins, one for the internal circuit and one for the output buffers, to minimize noise coupling.
- Locate inverting outputs of logically independent gates adjacent to each other. This provides the ability to wire AND-OR-Invert functions with ease.
- Locate common pins such as common Reset and common Clock at pin number 22 and Address or control inputs at pins 19 and 20 for flatpaks. This is to maximize use of Computer Aided Design (CAD) for board layouts.
- When feasible, mode control pins are used to create multipurpose devices.

Process Technology

The F100K ECL family is fabricated using an advanced isoplanar technology called FAST-Z. Devices in the family that feature higher performance and sizes of 1.25 microns are fabricated with a scaled FAST-Z Fineline process. These processes make possible subnanosecond logic delays and very highly controlled switching characteristics for consistent device-to-device high-speed performance.

The technology can best be described by reviewing the evolution of the transistor structure from the conventional planar and the original Isoplanar II processes to the FAST-Z and FAST-Z Fineline processes *(Figure 1-2)*. The top view shows the area needed for each structure; the dashed area is the center of the isolation region.

As in all Isoplanar technologies, the FAST-Z processes selectively grow a thick oxide between devices instead of the P+ region that is present in the planar process. The oxide needs no separation from the base-collector regions, resulting in a substantial reduction in device and chip size. The base and emitter ends terminate in the oxide wall. The mask openings can therefore overlap onto the isolation oxide making them self-aligned in that direction. This overlap feature means that base and emitter masking does not have to meet the extremely close tolerances that might otherwise be necessary. In addition, the FAST-Z transistor contacts are defined on a single mask layer making them self-aligned in the other direction.

Both the self-alignment feature and the ability to overlap the mask openings onto the isolation oxide provide improved process control. The need to meet extremely close tolerances that otherwise might be necessary is therefore avoided.

The FAST-Z "walled emitter" structures provide a reduction in transistor silicon area of 400 percent as compared to the planar structure. The collector-substrate therefore is also reduced by 400 percent. The collector-base area is reduced by 540 percent. These area reductions, combined with the shallower junctions achieved by well controlled ion implantation processes, provide significantly reduced capacitance and resistance values within the FAST-Z transistor structure. This, is turn, allows higher speeds.

Compensation Network

The heart of F100K is fully compensated ECL.[1] The basic gate consists of three blocks—the current switch, the output emitter-followers, and the reference or bias network *(Figure 1-3)*. The current switch allows both conjunctive and disjunctive logic. The output emitter-followers provide high drive capability through impedance transformation and allows for increased logic swing. The bias network sets DC

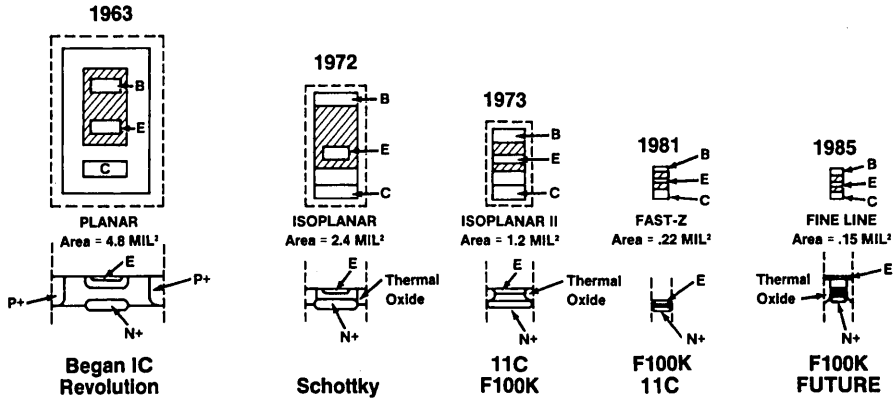

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FIGURE 1-2. Evolution of Bipolar Transistor Structures

thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary collector nodes of the current switch and driving the current source with a temperature insensitive bias network[2] *(Figure 1-4)*.

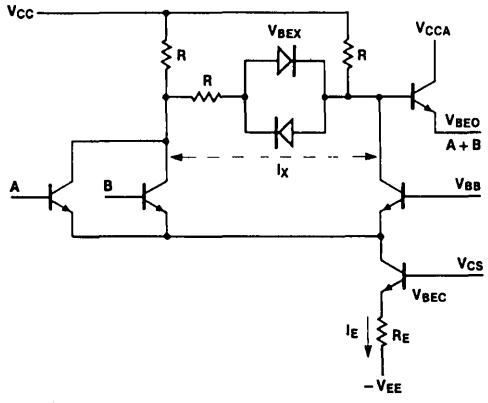

FIGURE 1-4. Temperature Compensation

As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS}, is independent of temperature, the switch curent increases with temperature due to the temperature dependence of V_{BEC}. The combination of temperature controlled current, I_E, and the cross-connect branch current, I_X, forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BEO} tracking coefficient.[3]

The schematic for the reference network displays a V_{BE1} amplifier in the bottom left corner *(Figure 1-5)*. Two base-emitter junctions are operated at different current densities, J1 and J2. The resulting voltage difference, V_{BE1} minus V_{BE2}, appears across R1 and is amplified by the ratio R2/R1. Note that R2 is used twice, once to generate V_{CS} and once to generate V_{BB}. The different current densities, J1 and J2, result in a positive temperature tracking coefficient across R2, which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4}. The V_{CS} and the V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon[1, 2] (approximately 1300 mV).[4] R_X in the V_{BE} amplifier compensates for process variations of β and ΔV_{BE}.[5] Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

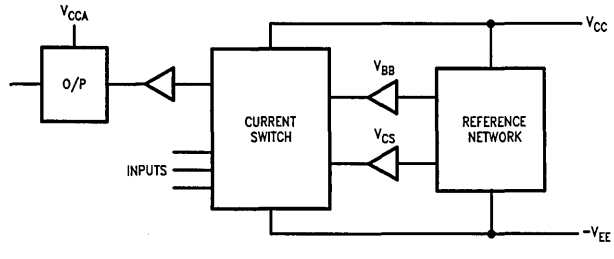

FIGURE 1-3. ECL Gate

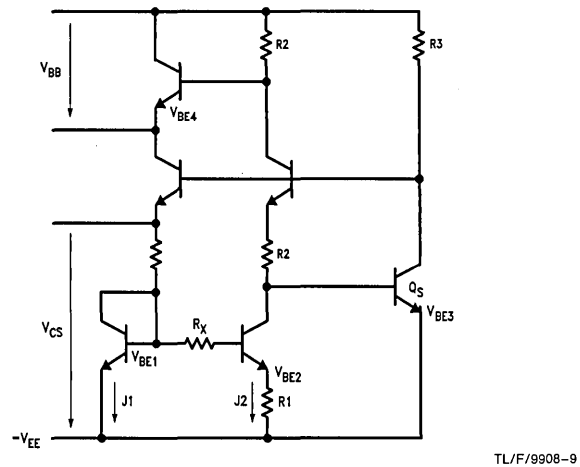

FIGURE 1-5. Reference Network

Characteristics

F100K compatibility with existing ECL logic families and memories permit direct interface with slower logic families and ensures immediate memory availability. The typical logic swing is 800 mV *(Figure 1-6)* and all voltage levels are specified with a 50Ω load to −2V at all outputs to provide transmission line drive capability. However, the inherently low output impedance *(Figure 1-7)* and maximum specified output current, 50 mA, make 25Ω drive possible at any or all outputs. Alternately, of course, higher termination impedances or other termination schemes are also useful.

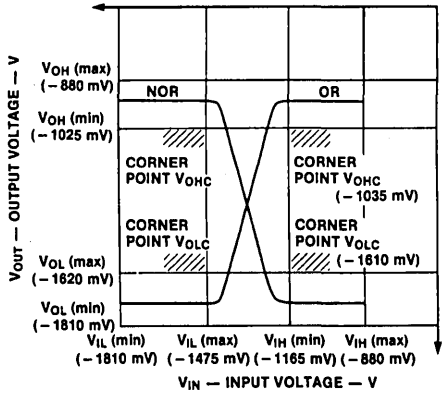

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FIGURE 1-6. Transfer Characteristics

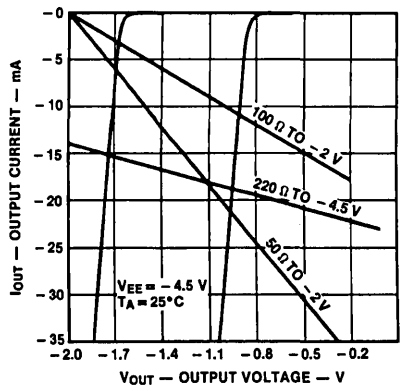

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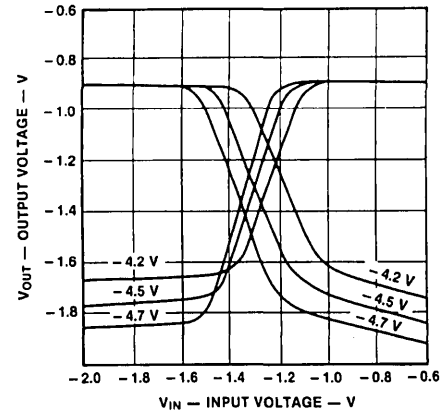
FIGURE 1-7. Output Characteristics vs Output Terminations

F100K exhibits relatively constant output levels and thresholds over the 0°C to +85°C specified temperature range and −4.2V to −4.8V specified voltage range *(Figure 1-8)*. V_{EE} power supply current is also constant over the specified voltage range *(Figure 1-9)*; therefore:

Uncompensated ECL



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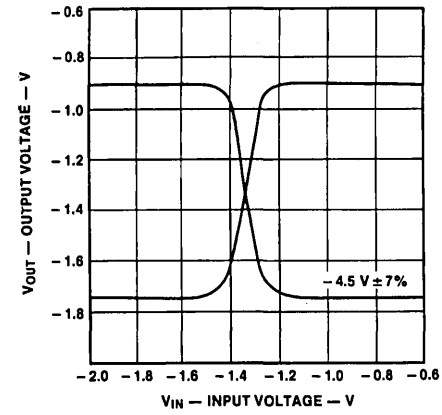
Fully Compensated ECL



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Uncompensated ECL

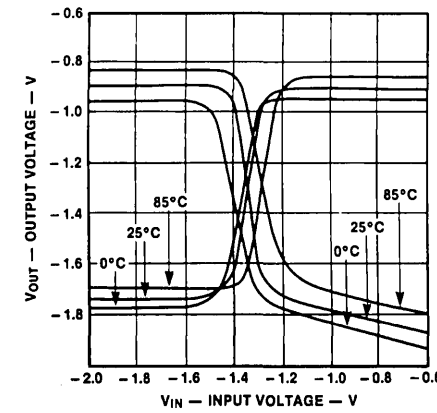

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FIGURE 1-8. Transfer Characteristics

Fully Compensated ECL

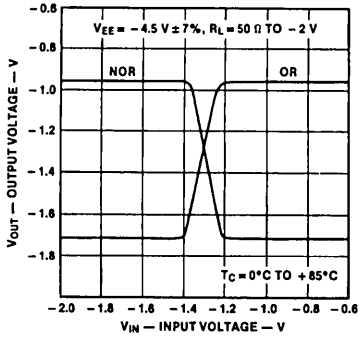

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FIGURE 1-8. Transfer Characteristics (Continued)

- Propagation delay is relatively constant versus power supply voltage variations thus tightening the AC window.
- Power dissipation is a linear function of the supply voltage, reducing worst-case power consumption.

The typical propagation delay of an SSI gate function driving a 50Ω transmission line is 0.75 ns, including package, with a power dissipation of 40 mW resulting in a speed-power product of 30 pJ. For optimized MSI functions, the internal gates can dissipate < 10 mW with average propagation delay of < 0.5 ns, giving a power-speed product of < 5 pJ.

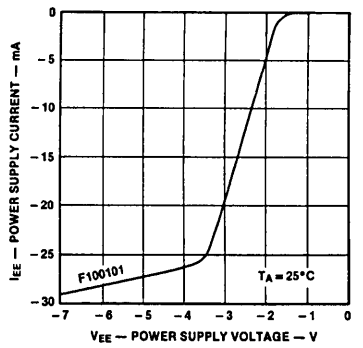

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FIGURE 1-9. Change in I_{EE} vs Change in V_{EE}

F100K has a tighter AC window over the wide range of environmental conditions; thus, the system timing requirements are eased and maximum system clock rates are increased. At the sacrifice of AC performance, the small-signal input impedance was conservatively designed to be positive-real over the frequency range encountered by any circuit input. This provides adequate damping to insure AC stability within the system.

System Aspects

F100K provides high-density digital functions that outperform all other families on the market today. How does this increased circuit performance and higher on-chip density improve system performance?

Propagation delay and transition times vary (AC windows) when functions are operated at the extremes of the specified environmental ranges. With F100K, these variations are reduced and more predictable system timing is achieved.

For synchronous machines and very high speed asynchronous systems, timing and its predictability are of utmost importance. Due to F100K constant supply current versus power supply voltage and because of nearly constant levels and thresholds with respect to temperature, voltage variations and gradients, speed skews are minimized.

Not only timing but also maximum system clock rate is affected by the tighter AC window. Thus, with F100K the system designer can use a higher speed value in his worst-case calculations. This can be translated into higher possible system clock rates. Therefore, a machine can perform at up to twice the frequency, solely due to the F100K compensation features. Noise immunity will be of utmost importance in next generation computers, since much of the noise generated within the system is inversely proportional to the switching transition time of the circuits. The F100K transition time is typically 0.7 ns as compared to 2.0 ns in other ECL families and should therefore increase system crosstalk by the same ratio.

F100K combats the increased system noise by maintaining a virtually invariant noise immunity with variations and gradients in power supply voltage, ambient and junction temperatures. The variation in junction temperatures is much larger than in earlier computer systems because of the mixture of LSI and SSI functions on the same boards.

Features

F100K ECL logic components are designed to be used in high-speed, low-noise systems and offer significant advantages over other logic families. Some of the important features and advantages are summarized below.

Low Propagation Delay

F100K ECL features gate delays that are typically 0.75 ns (750 picoseconds) with counters, registers and flip-flops operating in the 400–500 MHz range. When compared to other logic families such as Schottky TTL or slower ECL families, system performance can be doubled or tripled. Tighter AC distribution helps system timing requirements and increases system clock rates.

Moderate Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughout delays. Slower rise times minimize ringing and reflections on interconnection wiring and simplify physical design. The typical edge rate for F100K ECL is 1V/ns, only about 80% of the edge rate of Schottky TTL. It can be shown that for ECL circuits, the natural rise and fall times are approximately equal to the propagation delay. This relationship is considered optimum for use in high-speed systems.

Wired-OR Capability

ECL outputs can be wired together where wiring rules permit, to form the positive logic-OR function, thus achieving an extra level of gating at no parts count expense. Data bussing and party line operations are facilitated by this features.

Complementary Outputs

A majority of F100K ECL logic elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

A significant advantage to complementary outputs is that, since both the true and complement logic functions are available, I_{CC} imbalance can be minimized either by using both outputs in the design or merely terminating unused outputs. In this way, the constant current characteristic of ECL is not compromised and power supply noise is minimized.

Low Output Impedance, High Current Capacity

As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds.

Characteristic impedances of normal wiring and printed circuit interconnections generally fall in the 50Ω to 250Ω range. With these low impedance lines and fast transitions, the signals are attenuated by the voltage divider action between the circuit output impedance and the characteristic impedance of the interconnection.

Voltage mode circuits have a HIGH state output impedance of from 50Ω to 150Ω and thus exhibit an output *stepped* characteristic, first reaching about 50% of final value and later reaching the final value in another *step*. F100K ECL output impedances under 10Ω insure a complete, full valued, signal into a transmission line. Also, F100K ECL outputs are specified to drive a 50Ω load (some devices are specified to drive a 25Ω load). Outputs are capable of supply 50 mA or more and can thus support the quiescent current required for passive terminations.

Convenient Data Transmission

The complementary high-current outputs of F100K ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancellation and minimizing crosstalk between subsystems.

High Common-Mode Noise Rejection

Differential line receivers provide common-mode noise rejection of 1V or more for induced and ground noise. Differential receiving requires less signal swing than single ended and thus allows more reliable interpretation of low signal swings.

Constant Supply Current

The supply current drain of F100K ECL elements is governed by one or more internal constant current sources supplying operating current for differential switches and level shifting networks. Since the current drain is the same regardless of the state of the switches, F100K ECL circuits present constant currents loads to power supplies *(see Complementary Outputs)*.

Low Power Loss in Stray Capacitance

Energy is consumed each time a capacitor is charged or discharged so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and F100K ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance may be an order of magnitude less than that of TTL.

Low Noise Generation

In ECL systems, power supply lines are not subjected to the large current spikes common with TTL designs. Inherently, ECL is a constant current family without the totem-pole structures found in TTL circuits which generate the large current spikes. Since ECL voltage swings are much smaller than TTL, the current spikes caused by charging and discharging stray capacitances are much smaller with ECL than with TTL of comparable edge rates.

Low Crosstalk

Induced noise signals are proportional to signal swings and edge rates. The lower swing and slower edge rate of F100K ECL results in low levels of crosstalk.

System Benefits

The National F100K ECL Family offers improvements over other ECL families such as voltage and temperature compensation, higher integration levels, improved packaging, planned pinouts, lower propagation delay and more complementary outputs. These improvements offer measurable advantages to the design(er) of high-performance systems.

Easier Engineering

Designers have increased confidence that designs realized in F100K will operate with good margins over voltage and temperature variations in prototypes, production models and field installations. Less effort need be expended doing detailed voltage and temperature calculations and testing. With noncompensated ECL, noise margins cannot be guaranteed unless both the receiving and transmitting circuit operate at the same temperature and V_{EE}. This can cause a problem when attempting to transfer a breadboard or prototype system to production.

Since output swings and input thresholds remain almost constant over temperature and V_{EE} variations, complex control systems for power supply levels and more-than-adquate cooling are not necessary with F100K. This results in a more economical and better operating system.

Circuit Design

F100K ECL benefits from sound, well-engineered circuit designs. All input pins exhibit *positive/real* input impedance to eliminate system oscillations. Input buffering is used to reduce loads on lines which drive multiple internal gates.

High Performance

The regulation and control of DC and AC parameters achieved by F100K ECL assures that signal timing and propagation delays in critical paths are relatively insensitive to changes or gradients of temperature and supply voltage. Guardbands can be narrower, yet provide a higher degree of confidence due to the elimination of skew between output levels at one location and input threshold at another.

The consistency of response and security of noise margins permit operation at higher clock rates and thus increase system performance.

Easier Debugging

With F100K, debugging of systems can proceed more rapidly than with uncompensated ECL. When a cabinet or enclosure is opened for access in debugging, the resultant change in thermal conditions has almost no effect on F100K signal swings, propagation delays, edge rates or noise margins.

Flexibility

F100K is designed to operate at −4.5V for reduced power dissipation. If compatibility with other ECL families is a requirement, F100K will operate between −4.2V and −5.7V due to the unique voltage compensation features. When operating at voltages other than −4.5V, AC and DC parameters will vary slightly from specified values.

Fan-In/Fan-Out

All F100K ECL outputs are specified to drive 50Ω transmission lines; this makes them suitable for driving very-high fan-out loads. In addition, some F100K outputs are specified to drive 25Ω lines, which would be the case if a 50Ω party-line bus terminated at both ends were being driven.

System Design

F100K ECL was designed to be the ultimate standard packaged IC logic family. System design constraints were considered and the F100K family was designed for overall ease of system design and use while making the maximum use of the very fast propagation delay available.

Packaging

The initial package selected for the F100K family was a 24-pin Flatpak, 0.375 inches square, with leads on 50-mil centers, 6 leads per side. This package was chosen because its electrical characteristics minimized performance degradations of the circuit and its small footprint optimized board packing density. For customers who desire to use conventional through-hole assembly technology, the 24-pin ceramic dual in-line package is available as well. By utilizing the available F100K packages, and high chip complexities within the family, the user can achieve system densities two to three times higher than that possible with other ECL logic families.

A 28-pin plastic leaded chip carrier package is now in development for the F100K family. This package is approximately 0.490 inches square, with J-bend leads on 50-mil centers, 7 leads per side. This package, which features better electrical characteristics than the Flatpak, will improve the AC performance of a typical F100K device by an average of 200–300 ps as compared with the Flatpak. The leadframe has been designed with extra thermal paths which will provide junction-ambient thermal resistances of approximately 45°C/Wt in air flow of 500 linear feet per minute.

For information on thermal resistance please see section on Power Distribution and Thermal Considerations.

F100K ECL Mil/Aero Product Line

To help meet the growing need for higher speed components in many of todays military and aerospace applications, National Semiconductor has introduced a new line of military processed F100K ECL products. The new F100K ECL product line is processed to an extensive flow developed to meet the requirements of many military applications. This new process flow was designed to provide military system designers with the most reliable, highest quality 100K ECL products available.

The excellent AC characteristics of F100K ECL, recognized as the standard for commercial subnanosecond logic, are now available for next generation military applications. The AC and DC electrical characteristics (specified with an operating case temperature range of 0°C to +85°C) of the military product line, are identical to the characteristics specified in the data sheets of their commercial counterparts. The military system designer can now work with the same high speed tools as the commercial world to assure a continued edge in technology.

FEATURES

National's new F100K ECL Mil/Aero Product Line is the fastest military processed logic family available today. The excellent AC characteristics of ECL circuits will enable military system designers to overcome the speed limitations which have for so long hindered next generation design considerations. Some of the features and advantages are summarized below:

***Maintains Commercial Electrical Characteristics**—Mil/Aero F100K ECL devices will maintain the same AC and DC characteristics specified in their commercial equivalent data sheets. The additional processing will not affect the electrical performance of the military products. All of the features discussed in the Family Overview section of this book, System Considerations, Power Distribution and Thermal Considerations, and Testing Techniques can be applied for military applications without modifications or special considerations.

***SCD Support**—To fully support the needs of our military customers, National Semiconductor will accept Source Control Drawings (SCDs) submitted for review. This review shall be based upon the basic Mil/Aero F100K ECL product datasheet described in Table I format. For any additional testing, processing or special requirements, please contact your local sales office for further information.

***Two Package Types**—The entire Mil/Aero F100K ECL product line will be available in both 24-Pin 400 mil CDIP and 24-Pin Quad FLATPAK packages. Both packages are hermetically sealed and subjected to the entire military process flow. Both packages offer excellent thermal characteristics for system design considerations.

***Highest Performance**—F100K ECL is currently the only subnanosecond military processed logic family available. Typical gate delays of 0.75 ns allow system designers to use components up to several times faster than other logic families. The improved performance of F100K ECL opens the door to next generation, high performance military systems.

MILITARY PROCESSING

In order to help contractors meet many of the strict processing and test requirements imposed by the military, National Semiconductor has developed a special military process flow (Table I). National subjects 100% of the F100K ECL Mil/Aero Logic Family to this process flow.

Internal circuit design limitations, necessary for achieving the high performance of the F100K ECL logic family, currently prevent these devices from qualifying to all of the requirements of MIL-STD-883. National employs many of the industry-accepted MIL-STD-883 methods as identified in Table I as part of the Mil/Aero F100K ECL Process Flow.

TABLE I. Mil/Aero F100K ECL Process Flow

Process	MIL-STD-883	
	Method	Condition
*Internal Visual Inspection	2010	Test Condition B
Quality Assurance Sample Testing		
Internal Visual Inspection	2010	Test Condition B
*Stabilization Bake	1008	Test Condition C
*Temperature Cycling	1010	Test Condition C
*Constant Acceleration	2001	Test Condition E
*Pre-Burn-In Electrical Parameters		100% DC Test @ 25°C
*Burn-In	1015	160 hrs @ 125°C or Equivalent Unless Otherwise Specified
*Post Burn-In Electrical Parameters		100% DC test @ 25°C
Percent Defective Allowable (PDA)		5%
*AC Electrical Parameters		100% AC Test @ 25°C per Table I Specification
Quality Assurance Sample Testing		
DC Tests @ 25, 85, 0°C LTPD 2%		
AC Tests @ 25, 85, 0°C LTPD 2%		
*Seal (Hermiticity)		
(a) Fine	1014	Test Condition B
(b) Gross	1014	Test Condition C
Quality Assurance Sample Testing (Flatpak only)		
Seal		
(a) Fine	1014	Test Condition B
(b) Gross	1014	Test Condition C
*External Visual Inspection	2009	
Quality Assurance Sample Testing		
External Visual LTPD 2%		

*—Devices are subjected to 100% testing per applicable test method.

In addition to the above tests National Semiconductor also performs periodic quality assurance and reliability inspection tests. These tests are performed on a lot-by-lot, quarterly (die-related tests), and semi-annual (package related tests) basis. Testing is performed on a random sampling of devices, from randomly selected lots. Test data is available for review upon request.

The majority of National Semiconductor's F100K ECL Logic Family is now available in the expanded military process flow version. The remainder will become available based on the individual device demand and function. Please contact the factory or local sales office for the latest listing of available military processed F100K ECL devices.

Definitions of Symbols and Terms

AC Switching Parameters

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency): The maximum repetition rate at which clock pulses may be applied to sequential circuit. Above this frequency the device may cease to function.

t_{AA} (Address Access Time): 50% points of address input pulse to data output pulse.

t_{ACS} (Chip Select Access Time): 50% points of select pulse to data output pulse/leading edges.

t_h (Hold Time): The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{RCS} (Chip Select Recovery Time): Data output pulse/trailing edges.

t_S (Setup Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_S (Release Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized.

t_{TLH} (Transition Time, LOW to HIGH): The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW): The time between two specified reference points on a waveform which is changing from HIGH to LOW.

t_w (Pulse Width): The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_W (Write Pulse Width): 50% points of write enable input pulse.

t_{WHA} (Address Hold Time): 50% points of address pulse to trailing edge of write enable pulse.

t_{WHCS} (Chip Select Hold Time): 50% points of trailing edges of chip select pulse to write enable pulse.

t_{WHD} (Data Hold Time after Write): 50% points of trailing edges of data input pulse to write enable pulse.

t_{WR} (Write Recovery Time): 50% points of trailing edges of write enable pulse to data output pulse.

t_{WS} (Write Disable Time): 50% points of leading edges of write enable pulse to data output pulse.

t_{WSA} (Address Setup Time): 50% points of address pulse to leading edge of write enable pulse.

t_{WSCS} (Chip Select Setup Time): 50% points of leading edges of chip select pulse to write enable pulse.

t_{WSD} (Data Setup Time Prior to Write): 50% points of leading edges of data input pulse to write enable pulse.

Currents

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional curent flow *out of* a device lead.

I_{EE} (Power Supply Current): The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

I_{IH} (Input Current HIGH): The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst case DC input load that a device presents to a driving element.

I_{IL} (Input Current LOW): The current flowing into a device lead with the specified V_{IL} applied to the input.

Voltages

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage): The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground): This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CS} (Current Source Voltage): The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage): This potential is the system power supply voltage and it is the most negative potential in the system.

V_{IH} (Input Voltage HIGH): The range of input voltages that represents a logic HIGH level in the system.

$V_{IH\ (Max)}$: The most positive V_{IH}.

$V_{IH\ (Min)}$: The most negative V_{IH}. This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW): The range of input voltages that represents a logic LOW level in the system.

$V_{IL\ (Max)}$: The most positive V_{IL}. This value represents the guaranteed input LOW threshold for the device.

$V_{IL\ (Min)}$: The most negative V_{IL}.

V_{OH} (Output Voltage HIGH): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the output.

$V_{OH\ (Max)}$: The most positive V_{OH} under the specified input and loading conditions.

$V_{OH\ (Min)}$: The most negative V_{OH} under the specified input and loading conditions.

V_{OHC}: The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

$V_{OL\ (Max)}$: The most positive V_{OL} under the specified input and loading conditions.

$V_{OL\ (Min)}$: The most negative V_{OL} under the specified input and loading conditions.

V_{OLC}: The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin): Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and $V_{IH\ (Min)}$.

V_{NL} (LOW Level Noise Margin): Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between $V_{IL\ (Max)}$ and V_{OLC}.

References

1. H.H. Muller, W.K. Owens, and P.W.J. Verhofstadt, "Fully Compensated Emitter-Coupled Logic: Eliminating the Drawbacks of Conventional ECL", *IEEE Journal of Solid-State Circuits*, October 1973, pp. 362–367.
2. R.R. Marley, "On-Chip Temperature Compensation for ECL", *Electronic Products*, March 1, 1971.
3. V.A. Dhaka, J.E. Muschinske, and W.K. Owens, "Subnanosecond Emitter-Coupled Logic Gate Circuit Using Isoplanar II", *IEEE Journal of Solid-State Circuits*, October 1973, pp. 368–372.
4. R.J. Widlar, "New Developments in IC Voltage Regulators", *ISSCC Digital Technical Papers*, February 1970, pp. 157–159.
5. W.K. Owens, "Temperature Compensated Voltage Regulator Having Beta Compensating Means", United States Patent, No. 3,731,648, December 25, 1973.

Section 2

F100K Datasheets

Section 2 Contents

National Semiconductor

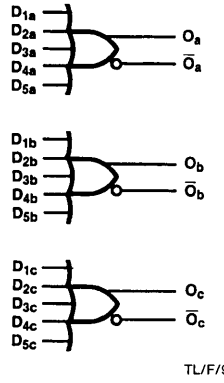
F100101
Triple 5-Input OR/NOR Gate

General Description

The F100101 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

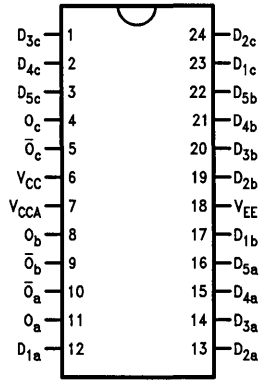
Logic Symbol



TL/F/9835–3

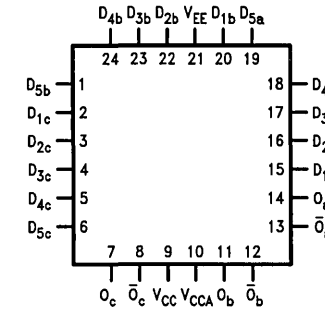
Connection Diagrams

24-Pin DIP



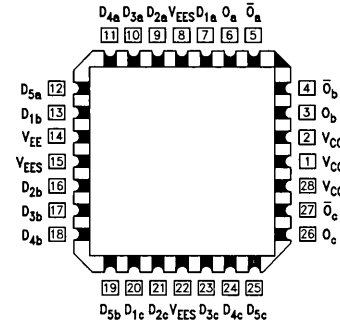
TL/F/9835–1

24-Pin Quad Cerpak



TL/F/9835–2

28-Pin PCC (Preliminary)



TL/F/9835–4

Pin Names	Description
D_{na}, D_{nb}, D_{nc}	Data Inputs
O_a, O_b, O_c	Data Outputs
$\overline{O}_a$, $\overline{O}_b$, $\overline{O}_c$	Complementary Data Outputs

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to --2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−38	−26	−18	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	1.15	0.50	1.15	0.55	1.30	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.20	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.50	0.95	0.50	0.95	0.55	1.10	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.10	ns	

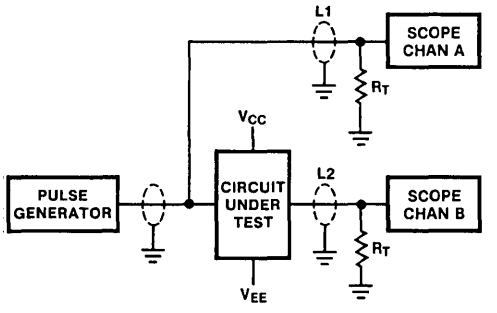


FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

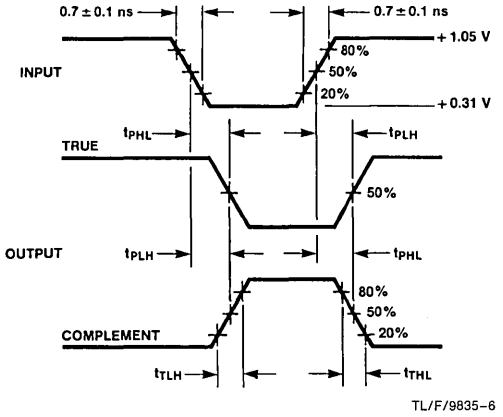


FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

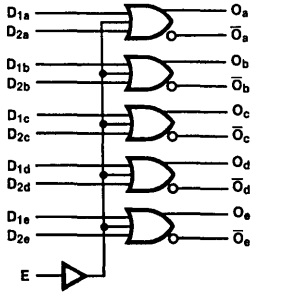
F100102
Quint 2-Input OR/NOR Gate

General Description

The F100102 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

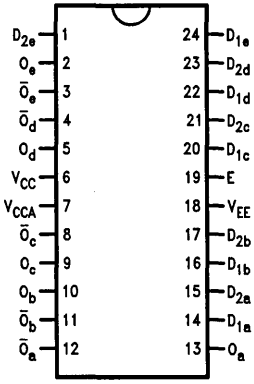
Logic Symbol



TL/F/9836-3

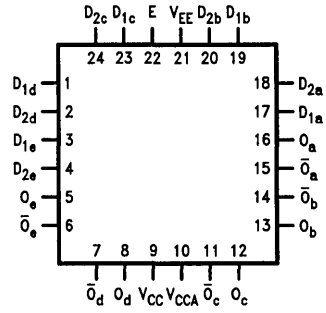
Connection Diagrams

24-Pin DIP



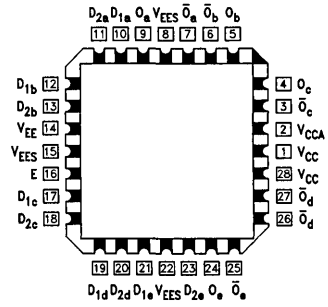
TL/F/9836-1

24-Pin Quad Cerpak



TL/F/9836-2

28-Pin PCC (Preliminary)



TL/F/9836-4

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
E	Enable Input
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

TABLE 1. F100102 Truth Table

D_{1X}	D_{2X}	E	O_X	$\overline{O}_X$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current Data Enable			 350 300	μA	V_{IN} = $V_{IH(Max)}$
I_{EE}	Power Supply Current	−80	−55	−38	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

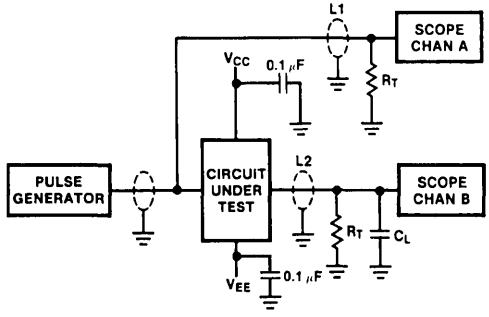
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.35	0.45	1.15	0.45	1.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.95	2.15	0.95	2.15	0.95	2.20	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.20	ns	

Cerpak AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

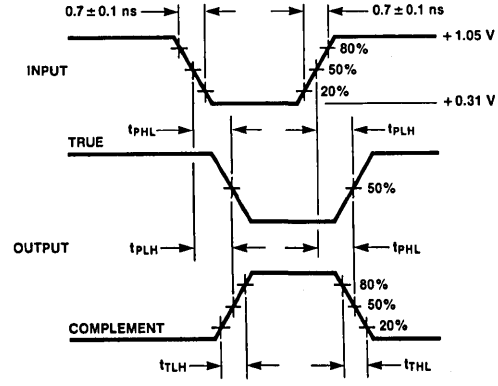
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.15	0.45	0.95	0.45	1.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.95	1.95	0.95	1.95	0.95	2.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.10	ns	



TL/F/9836–5

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9836–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

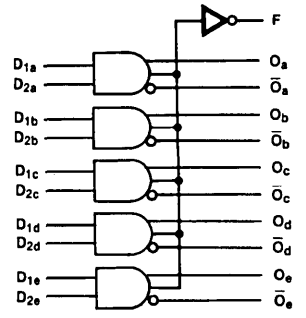
F100104
Quint AND/NAND Gate

General Description

The F100104 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

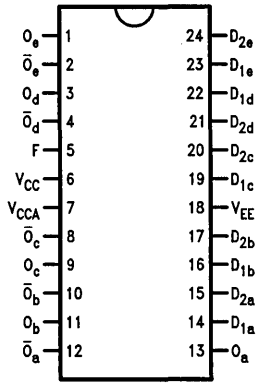
Logic Symbol



TL/F/9837–3

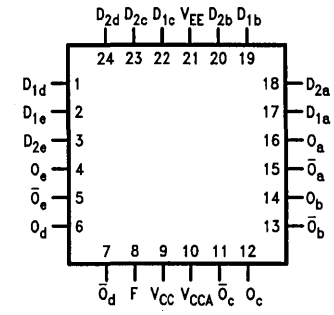
Connection Diagrams

24-Pin DIP



TL/F/9837–1

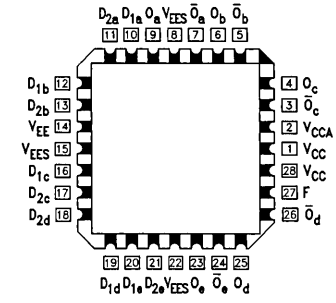
24-Pin Quad Cerpak



TL/F/9837–2

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

28-Pin PCC (Preliminary)



TL/F/9837–4

Logic Equation

$$F = \overline{(D_{1a} \bullet D_{2a}) + (D_{1b} \bullet D_{2b}) + D_{1c} \bullet D_{2c}) + (D_{1d} \bullet D_{2d}) + (D_{1e} \bullet D_{2e})}.$$

2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current D_{2a}–D_{2e} D_{1a}–D_{1e}			 250 350	 μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−96	−66	−46	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

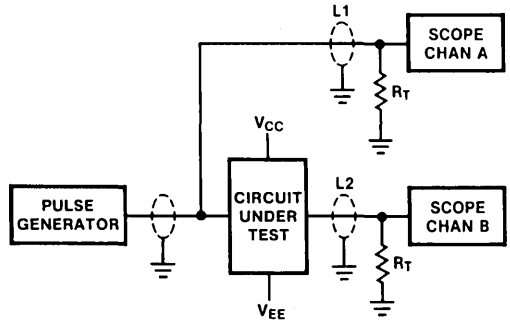
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{ne} to O, $\overline{O}$	0.40	1.75	0.40	1.65	0.40	1.75	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.00	2.60	1.00	2.60	1.15	3.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.70	0.35	1.55	0.35	1.70	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

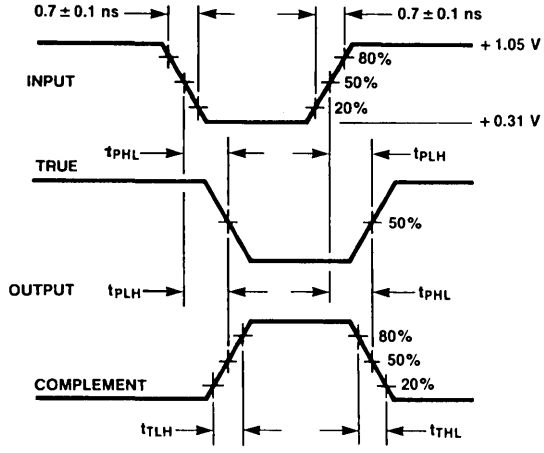
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{ne} to O, $\overline{O}$	0.40	1.55	0.40	1.45	0.40	1.55	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.00	2.40	1.00	2.40	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.35	1.60	0.35	1.45	0.35	1.60	ns	



TL/F/9837–5

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



TL/F/9837–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

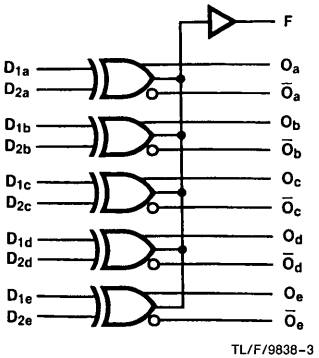
F100107
Quint Exclusive OR/NOR Gate

General Description

The F100107 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs.

Ordering Code: See Section 6

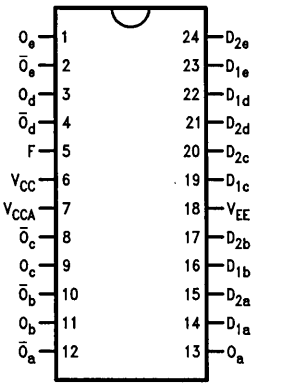
Logic Symbol



TL/F/9838-3

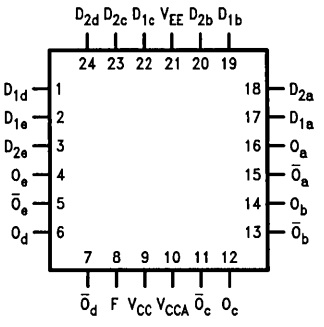
Connection Diagrams

24-Pin DIP



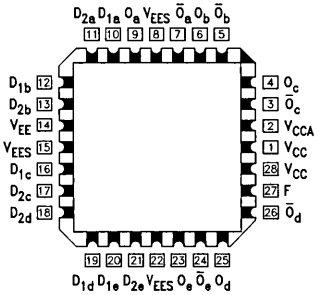
TL/F/9838-1

24-Pin Quad Cerpak



TL/F/9838-2

28-Pin PCC (Preliminary)



TL/F/9838-4

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
F	Function Output
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

Logic Equation

$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$.

2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current D_{2a}–D_{2e} D_{1a}–D_{1e}			 250 350	 μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−96	−66	−46	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

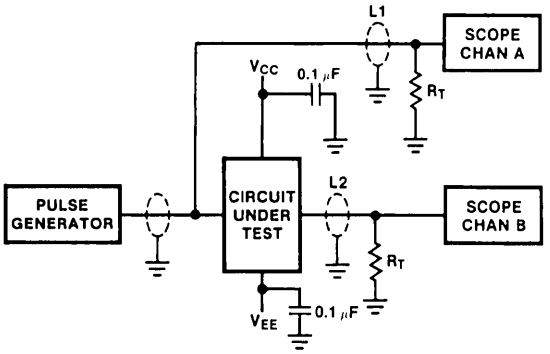
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.55	1.90	0.55	1.80	0.55	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.75	1.15	2.75	1.15	3.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.65	0.45	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{2a}–D_{2e} to O, $\overline{O}$	0.55	1.70	0.55	1.60	0.55	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_{1a}–D_{1e} to O, $\overline{O}$	0.55	1.50	0.55	1.40	0.55	1.50	ns	
t_{PLH} t_{PHL}	Propagation Delay Data to F	1.15	2.55	1.15	2.55	1.15	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.55	0.45	1.70	ns	

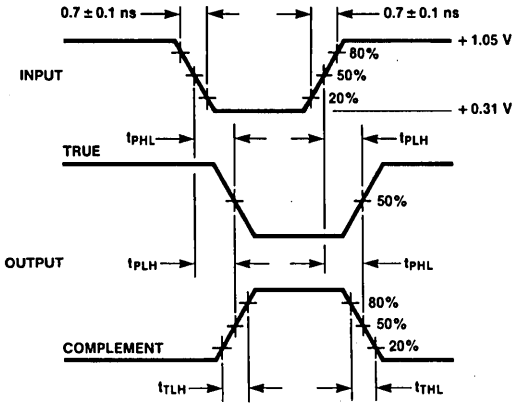


TL/F/9838–5

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



TL/F/9838–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

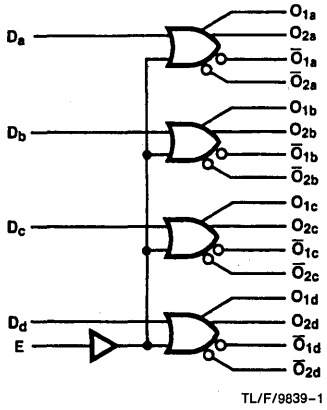
F100112
Quad Driver

General Description

The F100112 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

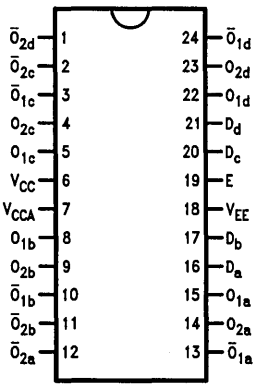
Logic Symbol



TL/F/9839–1

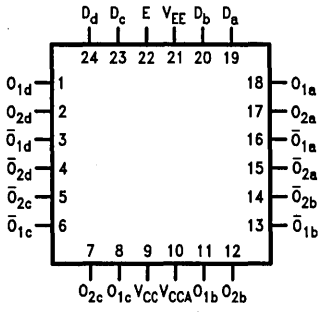
Connection Diagrams

24-Pin DIP



TL/F/9839–2

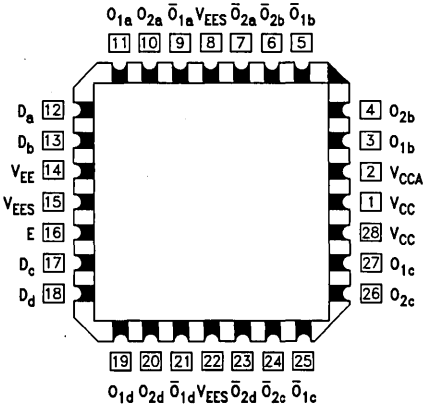
24-Pin Quad Cerpak



TL/F/9839–3

Pin Names	Description
D_a–D_d	Data Inputs
E	Enable Input
O_{na}–O_{nd}	Data Outputs
$\overline{O}_{na}$–$\overline{O}_{nd}$	Complementary Data Outputs

28-Pin PCC (Preliminary)



TL/F/9839–4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current Data Enable			 550 450	 μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−106	−73	−51	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

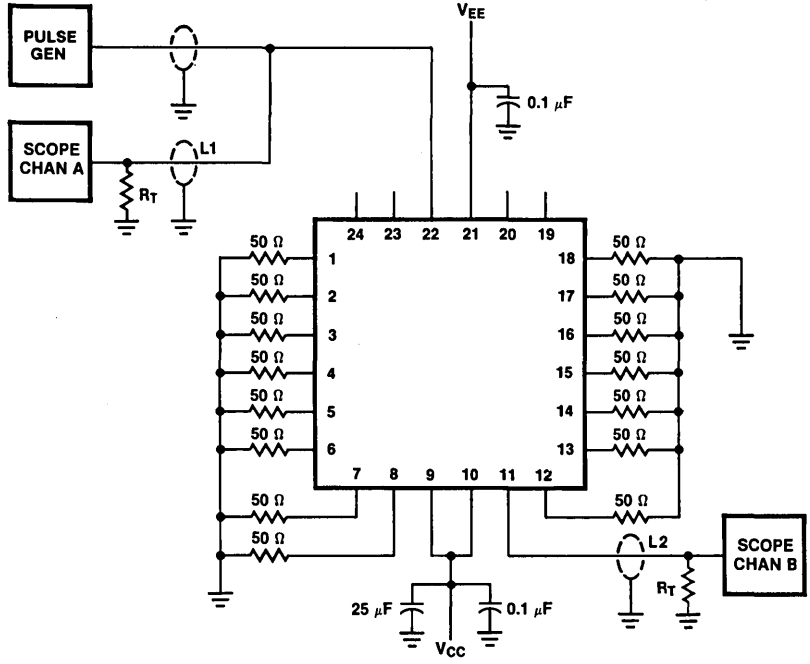
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.50	0.55	1.40	0.45	1.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.65	2.00	0.65	1.90	0.65	2.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

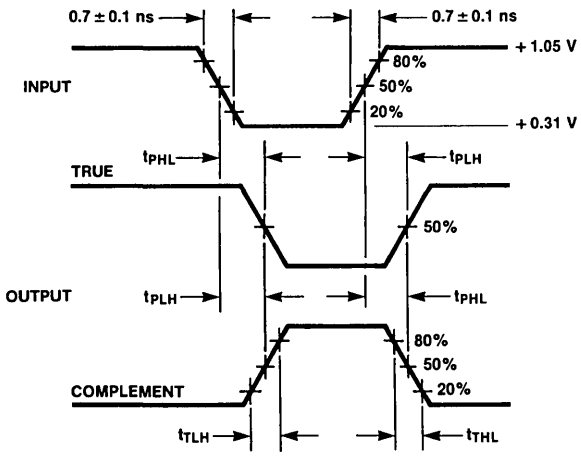
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.30	0.55	1.20	0.45	1.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.65	1.80	0.65	1.70	0.65	1.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	



TL/F/9839–5

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9839–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

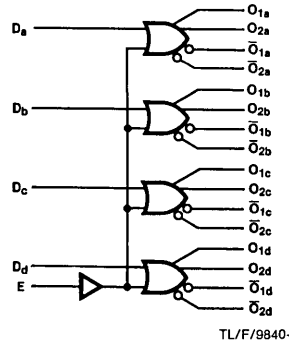
F100113
Quad Driver

General Description

The F100113 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

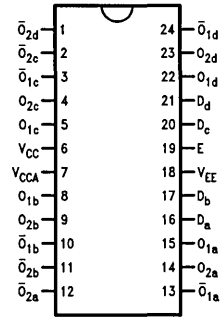
Logic Symbol



TL/F/9840-3

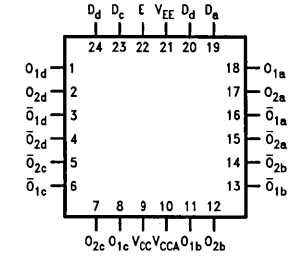
Connection Diagrams

24-Pin DIP



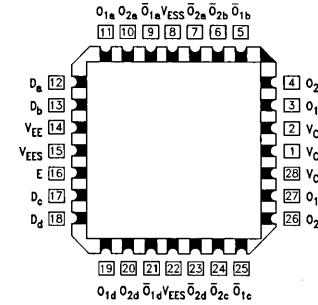
TL/F/9840-1

24-Pin Flatpak



TL/F/9840-2

28-Pin PCC (Preliminary)



TL/F/9840-4

Pin Names	Description
D_A–D_d	Data Inputs
E	Enable Input
O_{na}–O_{nd}	Data Outputs
$\overline{O}_{na}$–$\overline{O}_{nd}$	Complementary Data Outputs

2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current Data Enable			 550 350	μA	V_{IN} = $V_{IH\ (max)}$
I_{EE}	Power Supply Current	−116	−80	−56	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

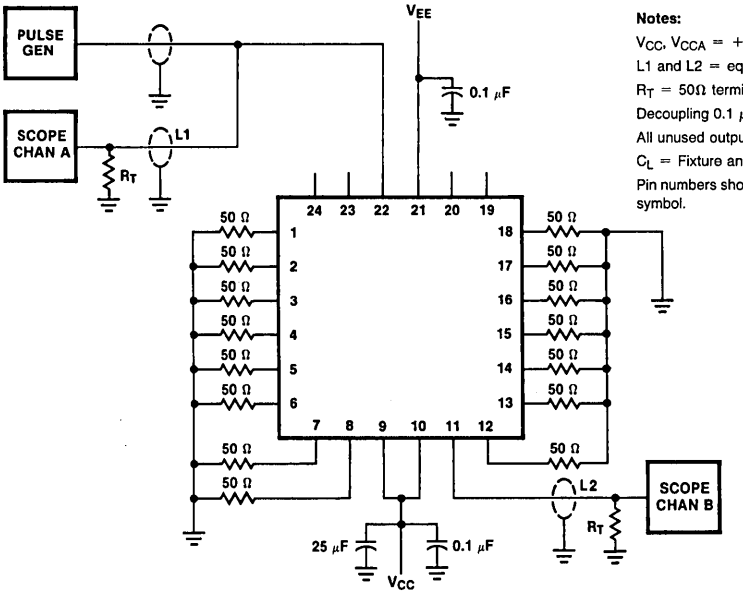
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.40	0.45	1.35	0.45	1.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.55	1.90	0.55	1.90	0.55	1.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.20	0.45	1.15	0.45	1.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.55	1.70	0.55	1.70	0.55	1.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V.

L1 and L2 = equal length 50Ω impedance lines.

R_T = 50Ω terminator internal to scope.

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.

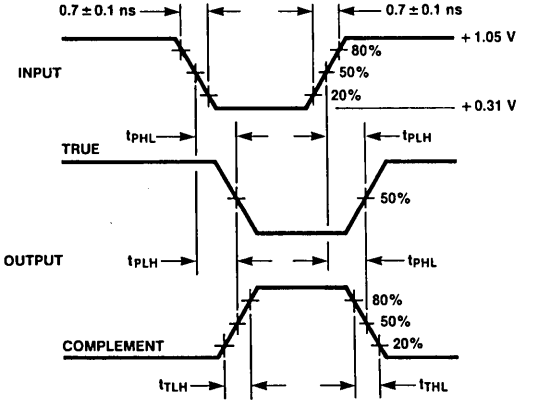
All unused outputs are loaded with 50Ω to GND.

C_L = Fixture and stray capacitance ≤ 3 pF.

Pin numbers shown are for flatpak; for DIP see logic symbol.

TL/F/9840–5

FIGURE 1. AC Test Circuit



TL/F/9840–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

F100114
Quint Differential Line Receiver

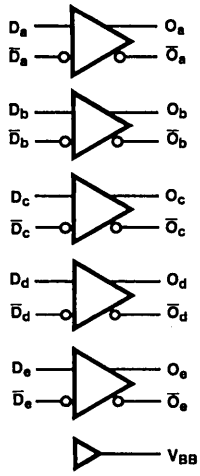
General Description

The F100114 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single-ended reception. When used in single-ended operation the apparent input threshold of the true inputs is 25 mV to 30 mV higher (positive) than the threshold of the complementary inputs. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors.

Active current sources provide common-mode rejection of 1.0V in either the positive or negative direction. A defined output state exists if both inverting and non-inverting inputs are at the same potential between V_{EE} and V_{CC}. The defined state is logic HIGH on the $\overline{O}_a$–$\overline{O}_e$ outputs.

Ordering Code: See Section 6

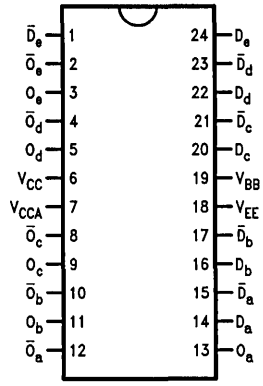
Logic Symbol



TL/F/9841-3

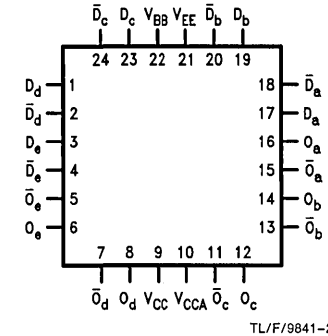
Connection Diagrams

24-Pin DIP



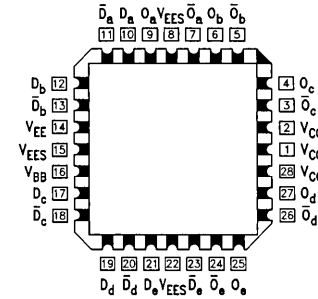
TL/F/9841-1

24-Pin Quad Cerpak



TL/F/9841-2

28-Pin PCC (Preliminary)



TL/F/9841-4

Pin Names	Description
D_a–D_e	Data Inputs
$\overline{D}_a$–$\overline{D}_e$	Inverting Data Inputs
O_a–O_e	Data Outputs
$\overline{O}_a$–$\overline{O}_e$	Complementary Data Outputs

2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −250 μA	
V_{IH}	Single-Ended Input HIGH Voltage	−1165			mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage			−1475	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB})	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{BB}	Output Reference Voltage	−1396	−1320	−1244	mV	I_{VBB} = −250 μA	
V_{IH}	Single-Ended Input HIGH Voltage	−1150			mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage			−1490	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB})	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{BB}	Output Reference Voltage	−1396	−1320	−1244	mV	I_{VBB} = −250 μA	
V_{IH}	Single-Ended Input HIGH Voltage	−1150			mV	Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage			−1490	mV	Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB})	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing
V_{CM}	Common Mode Voltage			1.0	V	Permissible ±V_{CM} with Respect to V_{BB}
I_{IH}	Input HIGH Current			50	μA	V_{IN} = $V_{IH\ (Max)}$, D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = $V_{IL\ (Min)}$
I_{CBO}	Input Leakage Current	−10			μA	V_{IN} = V_{EE}, D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = $V_{IL\ (Min)}$
I_{EE}	Power Supply Current	−106	−73	−51	mA	D_a–D_e = V_{BB}, $\overline{D}_a$–$\overline{D}_e$ = $V_{IL\ (Min)}$

Ceramic Dual-In-Line Package AC Electrical Characteristics

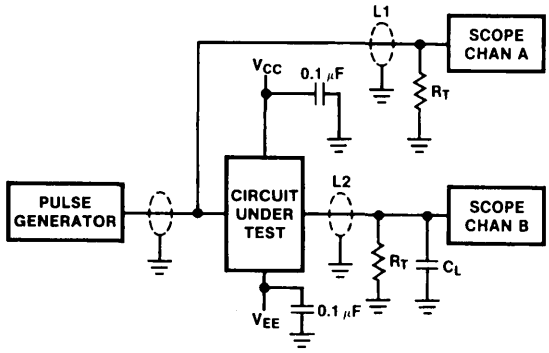
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.90	0.60	2.00	0.70	2.40	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	1.30	0.45	1.20	0.45	1.40	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.55	1.70	0.60	1.80	0.70	2.20	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.55	1.20	0.45	1.10	0.45	1.30	ns	

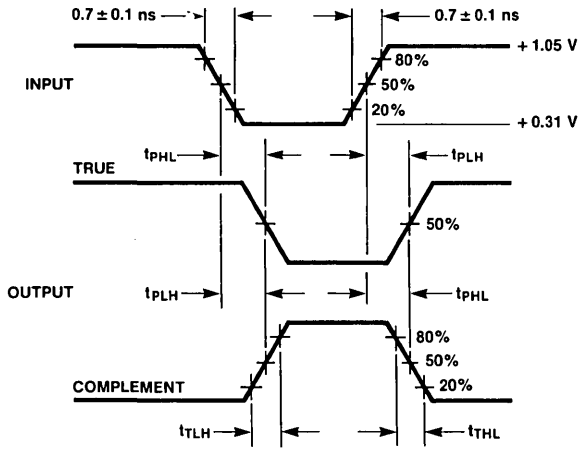


TL/F/9841–5

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



TL/F/9841–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

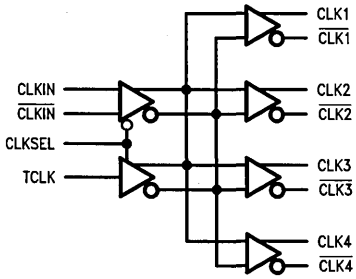
ADVANCE INFORMATION

F100115
Low-Skew Quad Driver

General Description

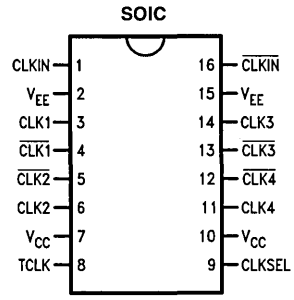
The F100115 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing.

Logic Diagram



TL/F/9842–2

Connection Diagram



TL/F/9842–1

Pin Names	Description
CLKIN, $\overline{CLKIN}$	Differential Clock Inputs
CLK_{1-4}, $\overline{CLK}_{1-4}$	Differential Clock Outputs
TCLK	Test Clock Input
CLKSEL	Clock Input Select

2

National Semiconductor

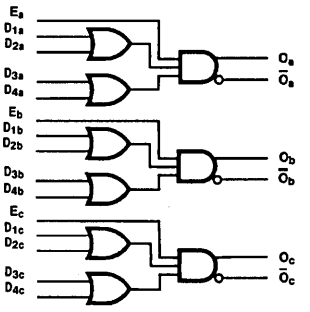
F100117
Triple 2-Wide OA/OAI Gate

General Description

The F100117 is a monolithic triple 2-wide OR/AND gate with true and complement outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

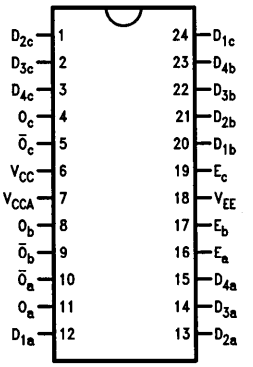
Logic Symbol



TL/F/9843–3

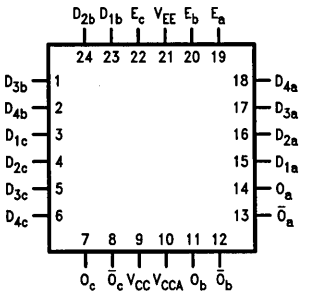
Connection Diagrams

24-Pin DIP



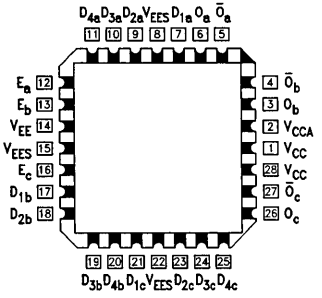
TL/F/9843–1

24-Pin Quad Cerpak



TL/F/9843–2

28-Pin PCC (Preliminary)



TL/F/9843–4

Pin Names	Description
D_{na}–D_{nc}	Data Inputs
E_a–E_c	Enable Inputs
O_a–O_c	Data Outputs
$\overline{O}_a$–$\overline{O}_c$	Complementary Data Outputs

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			260	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−79	−54	−37	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

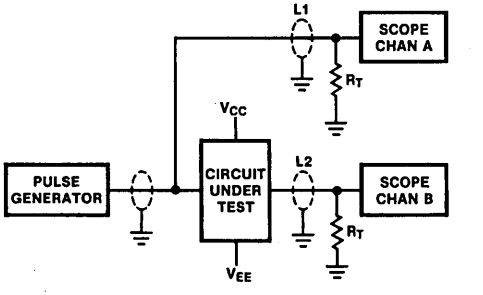
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.60	0.90	2.50	0.90	2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.40	0.45	1.30	0.45	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.30	0.45	1.20	0.45	1.30	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

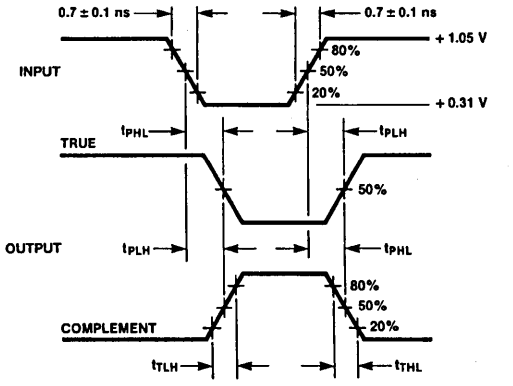
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.90	2.40	0.90	2.30	0.90	2.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Enable to Output	0.45	1.20	0.45	1.10	0.45	1.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.20	0.45	1.10	0.45	1.20	ns	



TL/F/9843–5

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9843–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

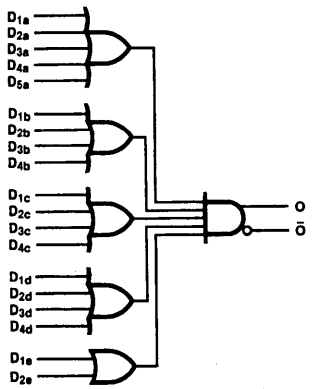
F100118
5-Wide 5, 4, 4, 4, 2 OA/OAI Gate

General Description

The F100118 is a monolithic 5-wide 5, 4, 4, 4, 2 OR/AND gate with true complementary outputs. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

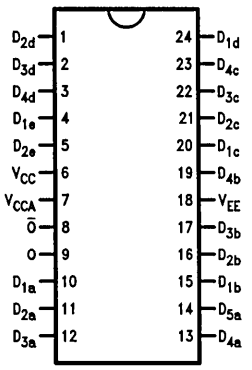
Logic Symbol



TL/F/9844-3

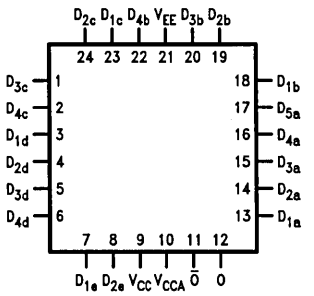
Connection Diagrams

24-Pin DIP



TL/F/9844-1

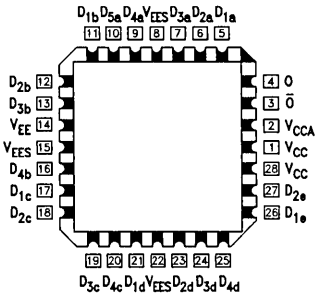
24-Pin Quad Cerpak



TL/F/9844-2

Pin Names	Description
D_{na}–D_{ne}	Data Inputs
O, $\bar{O}$	Data Outputs

28-Pin PCC (Preliminary)



TL/F/9844-4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−92	−69	−42	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

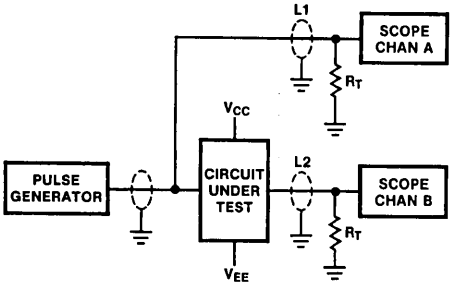
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.85	2.50	0.95	2.50	0.95	2.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.85	2.30	0.95	2.30	0.95	2.50	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	



TL/F/9844–5

FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

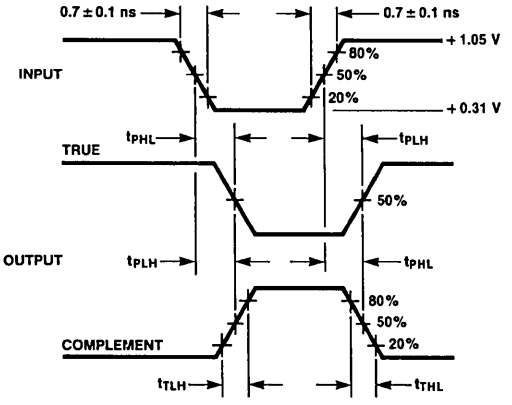
L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9844–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

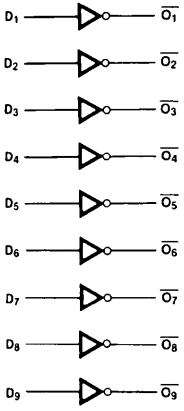
F100121
9-Bit Inverter

General Description

The F100121 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

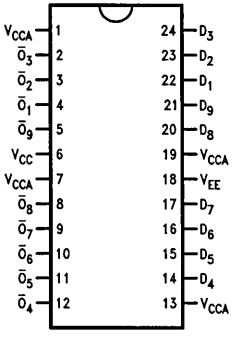


TL/F/9845–3

Pin Names	Description
D_1–D_9	Data Inputs
$\overline{O}_1$–$\overline{O}_9$	Data Outputs

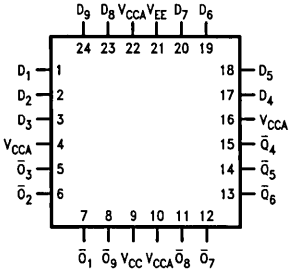
Connection Diagrams

24-Pin DIP



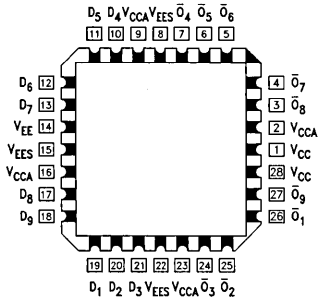
TL/F/9845–1

24-Pin Quad Cerpak



TL/F/9845–2

28-Pin PCC (Preliminary)



TL/F/9845–4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−96	−70	−46	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

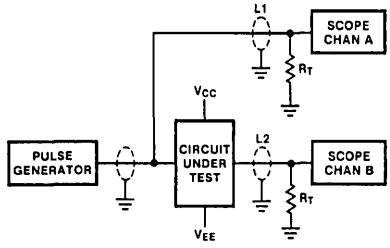
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.60	0.45	1.45	0.45	1.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.40	ns	

Cerpak AC Characteristics

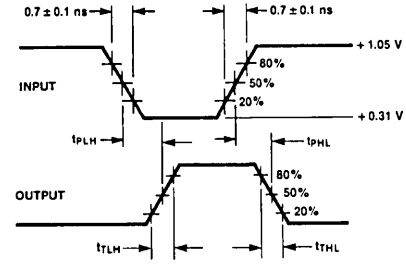
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.40	0.45	1.25	0.45	1.40	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.30	ns	



TL/F/9845–5

FIGURE 1. AC Test Circuit



TL/F/9845–6

FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope.

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.

All unused outputs are loaded with 50Ω to GND.

C_L = Fixture and stray capacitance ≤ 3 pF.

National Semiconductor

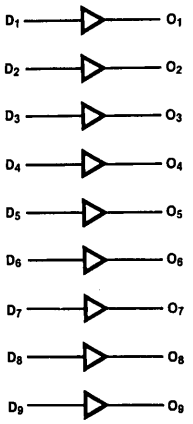
F100122
9-Bit Buffer

General Description

The F100122 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Ordering Code: See Section 6

Logic Symbol

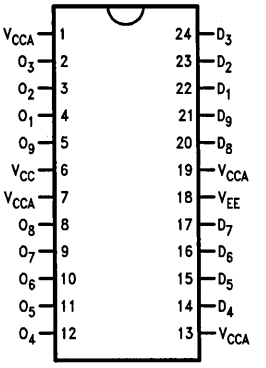


TL/F/9846-3

Pin Names	Description
D_1, D_9	Data Inputs
O_1, O_9	Data Outputs

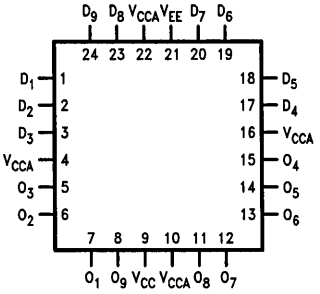
Connection Diagrams

24-Pin DIP



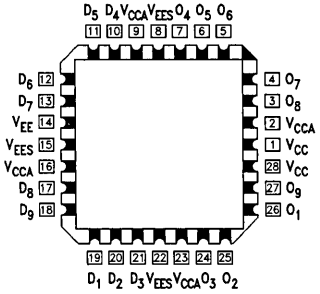
TL/F/9846-1

24-Pin Quad Cerpak



TL/F/9846-2

28-Pin PCC (Preliminary)



TL/F/9846-4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−96	−70	−46	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

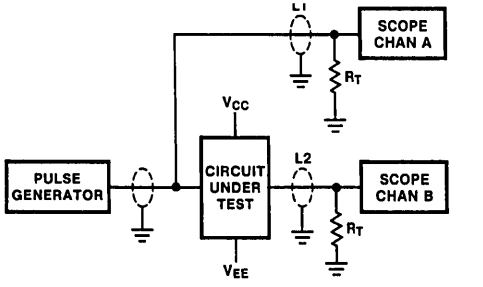
V_{EE} = −2.4V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.60	0.45	1.45	0.45	1.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.40	ns	

Cerpak AC Electrical Characteristics

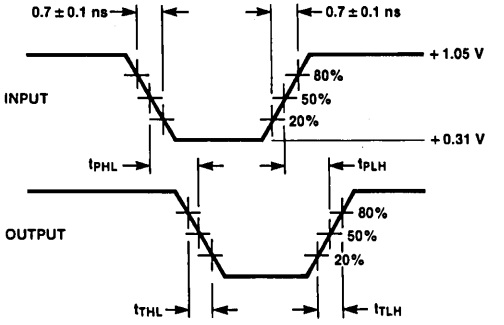
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.45	1.40	0.45	1.25	0.45	1.40	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.30	ns	



TL/F/9846–5

FIGURE 1. AC Test Circuit



TL/F/9846–6

FIGURE 2. Propagation Delay and Transition Times

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

National Semiconductor

F100123
Hex Bus Driver

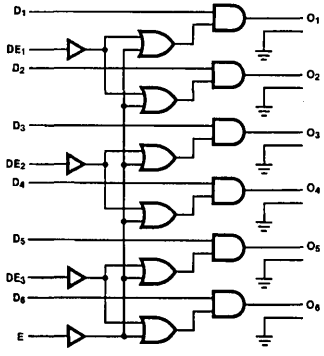
General Description

The F100123 is a monolithic device containing six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its respective ground connection. Transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (D_1–D_6) and the OR of two select inputs (E and either DE_1, DE_2 or DE_3). Enabling of data is possible in multiples of two, i.e., 2, 4 or all 6 paths. All inputs have 50 kΩ pull-down resistors.

The output voltage LOW level is designed to be more negative than normal ECL outputs (cut off state). This allows an emitter-follower output transistor to turn off when the termination supply is −2.0V and thus present a high impedance to the data bus.

Ordering Code: See Section 6

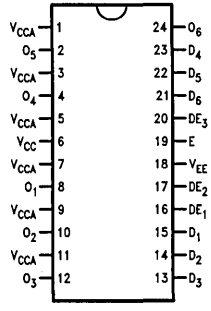
Logic Symbol



TL/F/9847–2

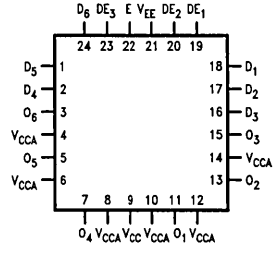
Connection Diagrams

24-Pin DIP



TL/F/9847–1

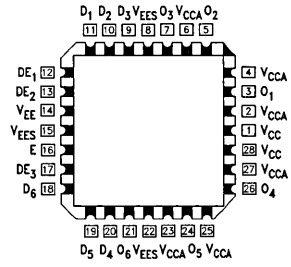
24-Pin Quad Cerpak



TL/F/9847–3

Pin Names	Description
D_1–D_6	Data Inputs
DE_1–DE_3	Dual Enable Inputs
E	Common Enable Input
O_1–O_6	Data Outputs

28-Pin PCC (Preliminary)



TL/F/9847–4

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage Cut-Off State			−2200	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.3V
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage Cut-Off State			−2200	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.3V
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 25Ω to −2.0V
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.0V
V_{OL}	Output LOW Voltage Cut-Off State			−2200	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 25Ω to −2.3V
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current Common Enable Data and Dual Enable			 330 260	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−235	−170	−113	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.00 1.00	4.30 2.40	1.95 1.00	4.30 2.40	2.00 1.10	4.60 2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Dual Enable to Output	2.30 1.40	4.70 3.00	2.00 1.40	4.70 3.00	2.30 1.40	5.10 3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay Common Enable to Output	2.60 1.50	5.40 3.20	2.50 1.50	5.30 3.30	2.80 1.50	5.80 3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.70 0.45	2.10 1.40	0.70 0.45	1.80 1.30	0.70 0.45	2.20 1.40	ns	

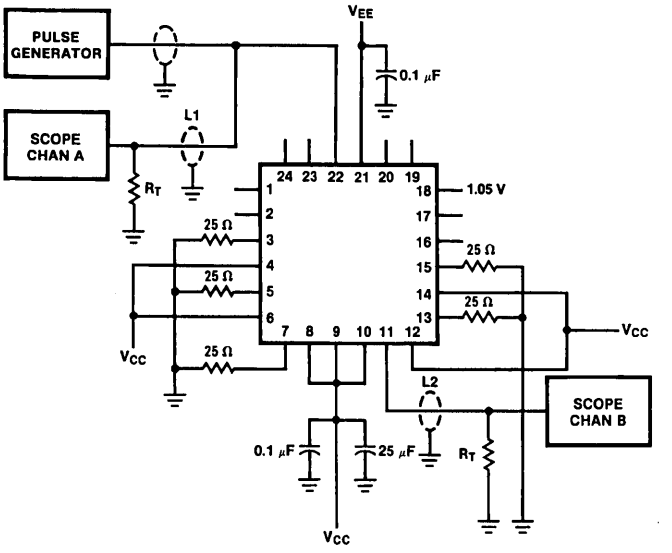
Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	2.00 1.00	4.10 2.20	1.95 1.00	4.10 2.20	2.00 1.10	4.40 2.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay Dual Enable to Output	2.30 1.40	4.50 2.80	2.00 1.40	4.50 2.80	2.30 1.40	4.90 3.20	ns	
t_{PLH} t_{PHL}	Propagation Delay Common Enable to Output	2.60 1.50	5.20 3.00	2.50 1.50	5.10 3.10	2.80 1.50	5.60 3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.70 0.45	2.00 1.30	0.70 0.45	1.70 1.20	0.70 0.45	2.10 1.30	ns	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

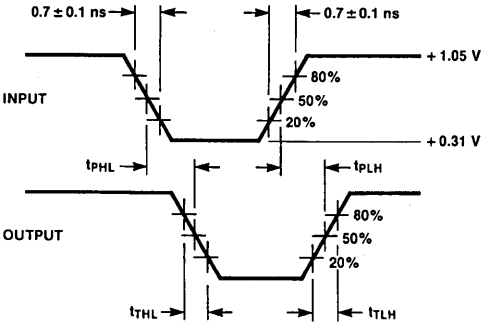
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

TL/F/9847–5

FIGURE 1. AC Test Circuit



TL/F/9847–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

F100124
Hex TTL-to-ECL Translator

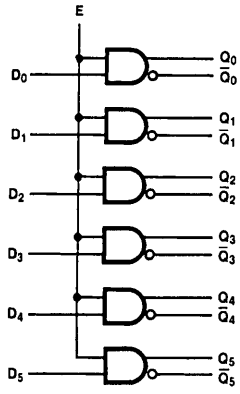
General Description

The F100124 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable input (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated. All inputs have 50 kΩ pull-down resistors.

When the circuit is used in the differential mode, the F100124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

Ordering Code: See Section 6

Logic Symbol

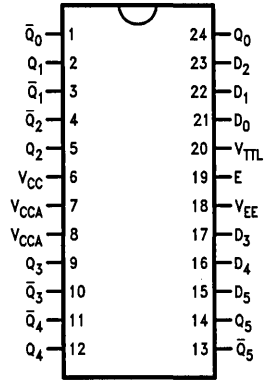


TL/F/9848–3

Pin Names	Description
D_0–D_5	Data Inputs
E	Enable Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

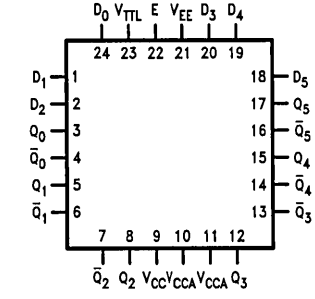
Connection Diagrams

24-Pin DIP



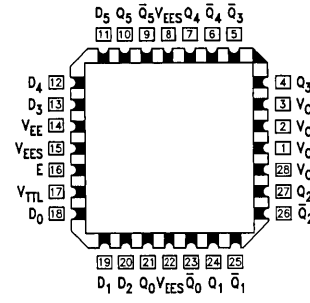
TL/F/9848–1

24-Pin Quad Cerpak



TL/F/9848–2

28-Pin PCC (Preliminary)



TL/F/9848–4

2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	+6.0V to −0.5V
Input Voltage (DC)	−0.5V to V_{TTL}
Output Current (DC Output HIGH)	−50 mA
Operating Range (V_{EE}) (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs
V_{CD}	Input Clamp Diode Voltage	−1.5			V	I_{IN} = −10 mA
I_{IH}	Input HIGH Current Data Enable			 20 120	 μA	V_{IN} = +2.4V, All Other Inputs V_{IN} = GND
	Input HIGH Current Breakdown Test, All Inputs			1.0	mA	V_{IN} = +5.5V, All Other Inputs = GND
I_{IL}	Input LOW Current Data Enable	 −1.6 −9.6			mA	V_{IN} = +0.4V, All Other Inputs V_{IN} = V_{IH}
I_{EE}	V_{EE} Power Supply Current	−140	−96	−52	mA	All Inputs V_{IN} = +4.0V
I_{TTL}	V_{TTL} Power Supply Current		44	75	mA	All Inputs V_{IN} = GND

Ceramic Dual-In-Line Package AC Electric Characteristics

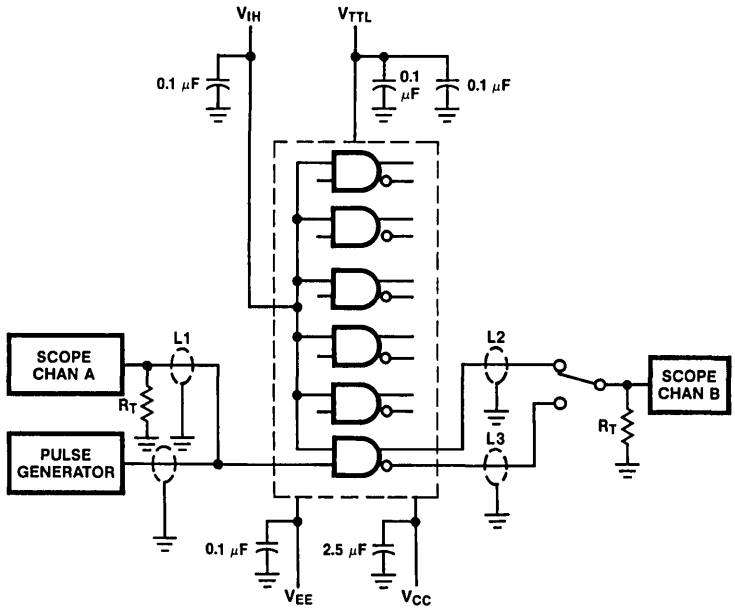
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	3.00	0.50	2.90	0.50	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	



TL/F/9848–5

FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V, V_{TTL} = +7.0V, V_{IH} = +6.0V

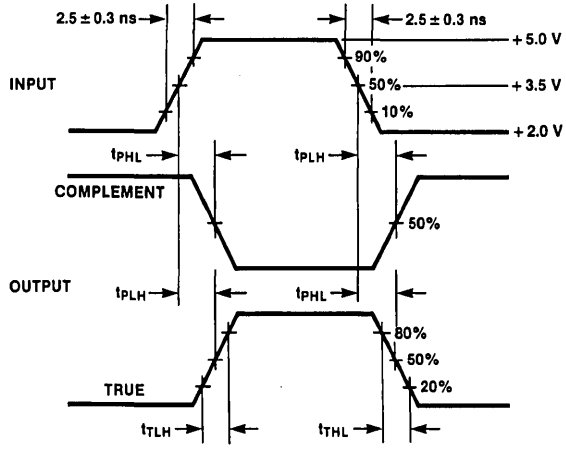
L1, L2 and L3 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9848–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

F100125
Hex ECL-to-TTL Translator

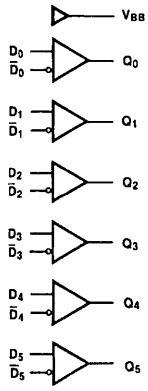
General Description

The F100125 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation or for use in Schmitt trigger applications. All inputs have 50Ω pull-down resistors; therefore, the outputs will go LOW when the inputs are left unconnected.

When used in the differential mode, the inputs have a common mode rejection of +1V, making this device tolerant of ground offsets and transients between the signal source and the translator. The V_{EE} and V_{TTL} power may be applied in either order.

Ordering Code: See Section 6

Logic Symbol

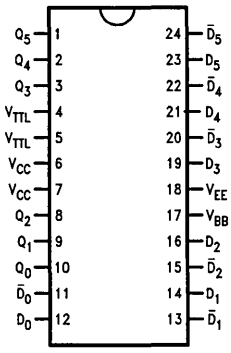


TL/F/9849-3

Pin Names	Description
D_0–D_5	Data Inputs
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs
Q_0–Q_5	Data Outputs

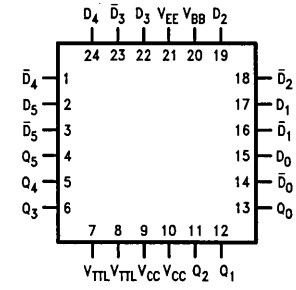
Connection Diagrams

24-Pin DIP



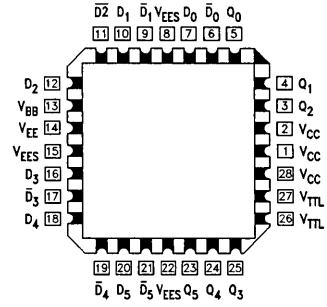
TL/F/9849-1

24-Pin Quad Cerpak



TL/F/9849-2

28-Pin PCC (Preliminary)



TL/F/9849-4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	+6.0V to −0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −2.1 mA
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)
V_{BB}	Output Reference Voltage	−1396	−1320	−1244	mV	I_{VBB} = −2.1 mA
V_{IH}	Single-Ended Input HIGH Voltage	−1150		−880	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1490	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)
V_{BB}	Output Reference Voltage	−1396	−1320	−1244	mV	I_{VBB} = −2.1 mA
V_{IH}	Single-Ended Input HIGH Voltage	−1150		−880	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})
V_{IL}	Single-Ended Input LOW Voltage	−1810		−1490	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20 mA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage			1.0	V	Permissible ±V_{CM} with Respect to V_{BB}	
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH\ (Max)}$, D_0–D_5 = V_{BB}, $\overline{D}_0$–$\overline{D}_5$ = $V_{IL\ (Min)}$	
I_{IL}	Input LOW Current	0.5			μA	V_{IN} = $V_{IL\ (Min)}$, D_0–D_5 = V_{BB}	
I_{OS}	Output Short-Circuit Current	−100		−40	mA	V_{OUT} = GND*	
I_{EE}	V_{EE} Power Supply Current	−85	−60	−40	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current		75	115	mA	D_0–D_5 = V_{BB}	

*Test one output at a time.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.50	0.90	3.70	1.00	4.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 1V to 2V, 2V to 1V	0.50	2.60	0.50	2.60	0.50	2.60	ns	

Cerpak AC Electrical Characteristics

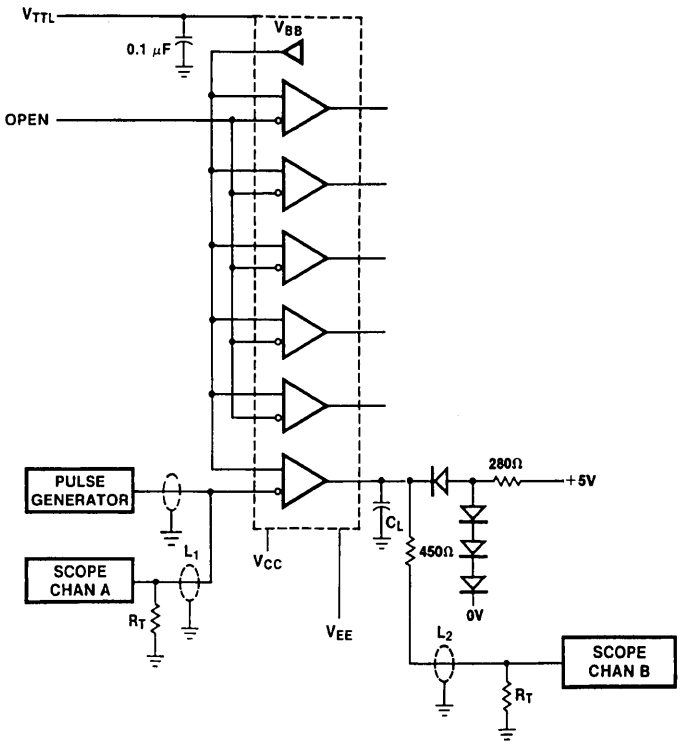
V_{EE} = −4.2V to −4.8V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 1V to 2V, 2V to 1V	0.50	2.50	0.50	2.50	0.50	2.50	ns	

Truth Table

Inputs		Outputs
D_n	$\overline{D}_n$	Q_n
L	H	L
H	L	H
L	L	U
H	H	U
Open	Open	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
U = Undefined



TL/F/9849–5

FIGURE 1. AC Test Circuit

Notes:

V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V

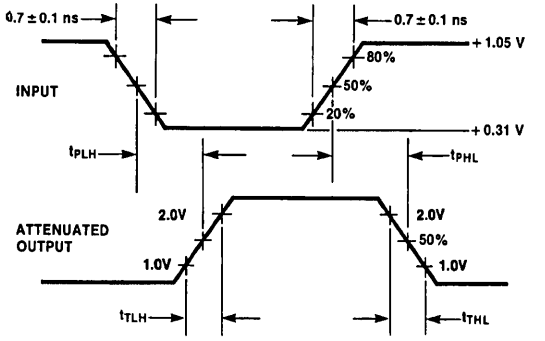
L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}

All unused outputs are loaded with 500Ω to GND

C_L = Fixture and stray capacitance = 15 pF



TL/F/9849–6

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

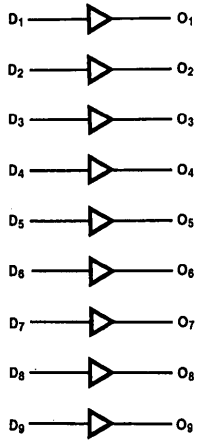
F100126
9-Bit Backplane Driver

General Description

The F100126 contains nine independent, high-speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus-oriented systems where minimal output loading or bus isolation is desired. The output transition times are longer to minimize noise when used as a backplane driver. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

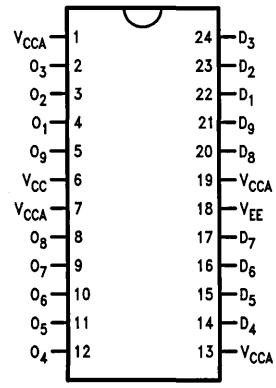


TL/F/9850-3

Pin Names	Description
D_1–D_9	Data Inputs
O_1–O_9	Data Outputs

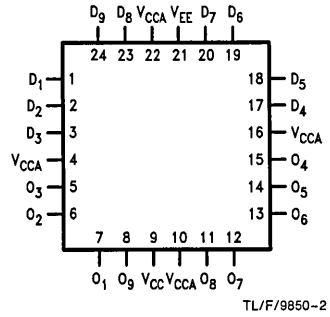
Connection Diagrams

24-Pin DIP



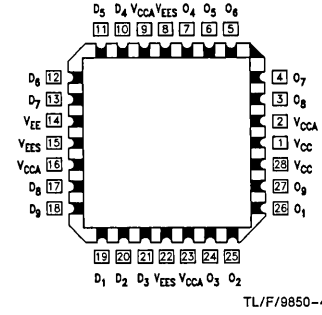
TL/F/9850-1

24-Pin Quad Cerpak



TL/F/9850-2

28-Pin PCC (Preliminary)



TL/F/9850-4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−96	−70	−46	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

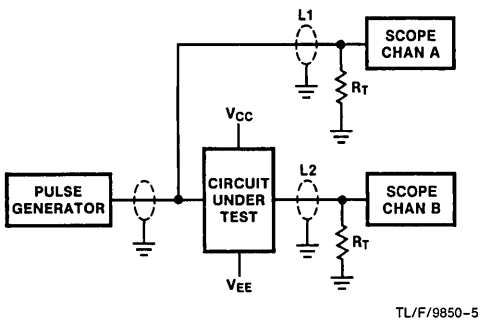
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.05	2.75	1.05	2.75	1.05	2.75	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.15	3.40	1.15	3.40	1.05	3.40	ns	

Cerpak AC Electrical Characteristics

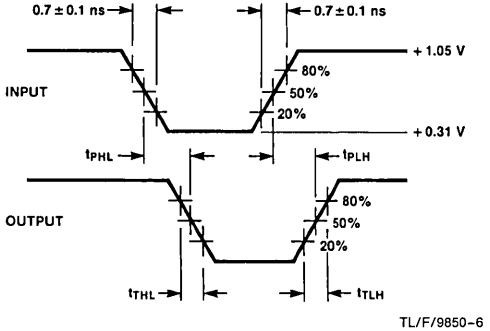
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.05	2.55	1.05	2.55	1.05	2.55	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.15	3.30	1.15	3.30	1.05	3.30	ns	



TL/F/9850–5

FIGURE 1. AC Test Circuit



TL/F/9850–6

FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

National Semiconductor

F100128
ECL/TTL Bi-Directional Translator

General Description

The F100128 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the F100128 transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

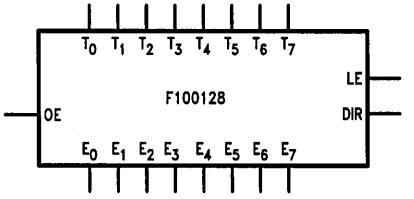
The F100128 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads.

Features

- Bi-directional translation
- ECL high impedance outputs
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs

Ordering Code: See Section 6

Logic Symbol



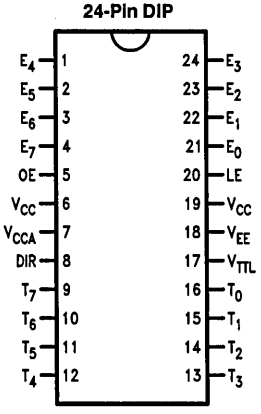
TL/F/9851-3

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

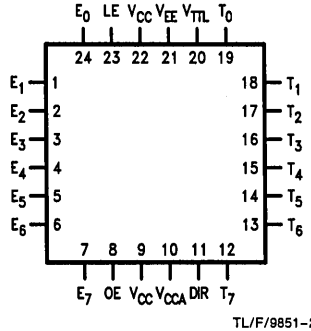
Connection Diagrams

24-Pin DIP



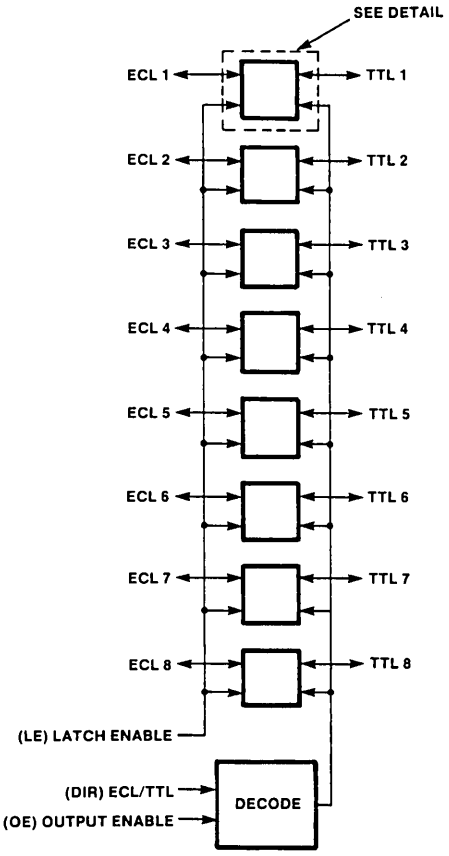
TL/F/9851-1

24-Pin Quad Cerpak



TL/F/9851-2

Functional Diagram



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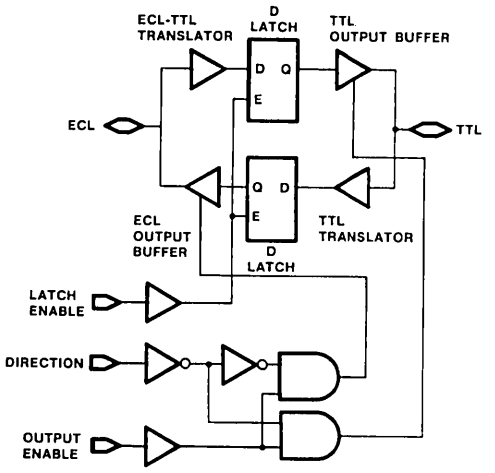
Detail



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Truth Table

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	
L	L	H	Input	Z	1, 3
L	H	H	LOW (Cut-Off)	Input	2, 3
H	L	L	L	L	1, 4
H	L	L	H	H	1, 4
H	L	H	X	Latched	1, 3
H	H	L	L	L	2, 4
H	H	L	H	H	2, 4
H	H	H	Latched	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature	+150°C
Case Temperature under Bias	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	+6.0V to −0.5V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 2)	−0.5V to +7.0V
TTL Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature	0°C to +85°C
Supply Voltage (Note 1)	
V_{EE}	−5.7V to −4.2V
V_{TTL}	+4.5V to +5.5V

Note 1: Parametric values specified at V_{EE} = −4.2V to −4.8V.

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	−1020		−870	mV	V_{EE} = −4.2V, 50Ω to −2V
		−1025	−955	−880	mV	V_{EE} = −4.5V, 50Ω to −2V
		−1035		−880	mV	V_{EE} = −4.8V, 50Ω to −2V
V_{OL}	Output Low Voltage	−1810		−1605	mV	V_{EE} = −4.2V, 50Ω to −2V
		−1810	−1705	−1620	mV	V_{EE} = −4.5V, 50Ω to −2V
		−1830		−1620	mV	V_{EE} = −4.8V, 50Ω to −2V
	Cutoff Voltage					OE or DIR Low,
			−2000	−1930	mV	V_{EE} = −4.2V, 50Ω to −2V
			−2000	−1950	mV	V_{EE} = −4.5V, 50Ω to −2V
			−2000	−1950	mV	V_{EE} = −4.8V, 50Ω to −2V
V_{OHC}	Output High Voltage Corner Point High	−1030			mV	V_{EE} = −4.2V, 50Ω to −2V
		−1035			mV	V_{EE} = −4.5V, 50Ω to −2V
		−1045			mV	V_{EE} = −4.8V, 50Ω to −2V
V_{OLC}	Output Low Voltage Corner Point Low			−1595	mV	V_{EE} = −4.2V, 50Ω to −2V
				−1610	mV	V_{EE} = −4.5V, 50Ω to −2V
				−1610	mV	V_{EE} = −4.8V, 50Ω to −2V
V_{IH}	Input High Voltage	2.0			V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input Low Voltage			0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input High Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input Low Current			−1.0	mA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage			−1.2	V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−250	−175	−125	mA	LE Low, OE and DIR High

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output Low Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input High Voltage	−1150 −1165 −1165		−870 −880 −880	mV mV mV	V_{EE} = −4.2V V_{EE} = −4.5V V_{EE} = −4.8V
V_{IL}	Input Low Voltage	−1810 −1810 −1810		−1475 −1475 −1490	mV mV mV	V_{EE} = −4.2V V_{EE} = −4.5V V_{EE} = −4.8V
I_{IH}	Input High Current			200	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input Low Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low			−1.0	mA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−60		−225	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current		155 90 120	200 120 160	mA mA mA	TTL Outputs Low TTL Outputs High TTL Outputs in TRI-STATE

Cerpak TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.0 1.1	3.3 3.7	1.0 1.1	3.3 3.7	1.0 1.4	3.3 4.3	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	2.2 2.0	4.6 4.3	2.2 2.0	4.6 4.3	2.7 2.4	5.4 5.0	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.4	4.5	1.4	4.5	1.5	5.0	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.0	4.0	1.0	4.0	1.0	4.0	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.0	3.5	1.0	3.5	1.0	4.0	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6		1.0		1.6		ns	*Figures 1 & 2*

Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.5 2.0	6.5 5.5	2.5 2.0	6.5 5.5	3.0 2.0	8.0 6.0	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.0 2.5	7.5 6.5	3.0 2.5	7.5 6.5	3.5 3.0	9.5 7.0	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.0 4.0	7.5 9.5	3.0 4.0	7.5 9.5	3.5 4.5	8.5 10.0	ns	*Figures 3 & 4*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.0 2.5	9.5 8.0	3.0 2.5	9.5 8.0	3.5 3.5	11.0 10.0	ns	*Figures 3 & 4*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.5 2.5	10.0 8.5	2.5 2.5	10.0 8.5	3.0 3.5	10.0 10.0	ns	*Figures 3 & 4*
t_{set}	E_n to LE	1.5		1.5		1.5		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	3.5		3.5		3.5		ns	*Figures 3 & 4*

Ceramic Dual-In-Line Package TTL-to-ECL AC Electrical Characteristics

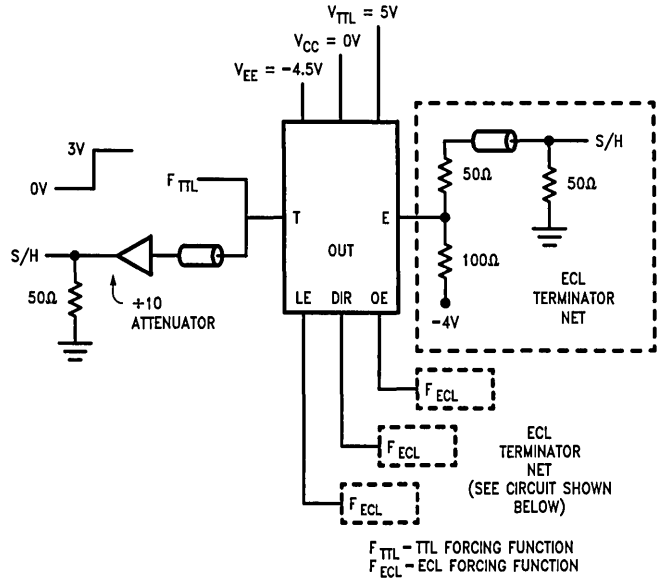
V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	1.0 1.1	3.3 3.7	1.0 1.1	3.3 3.7	1.0 1.4	3.3 4.3	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	2.2 2.0	4.6 4.3	2.2 2.0	4.6 4.3	2.7 2.4	5.4 5.0	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.4	4.5	1.4	4.5	1.5	5.0	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.0	4.0	1.0	4.0	1.0	4.0	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.0	3.5	1.0	3.5	1.0	4.0	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6		1.0		1.6		ns	*Figures 1 & 2*

Ceramic Dual-In-Line Package ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.5 2.0	6.5 5.5	2.5 2.0	6.5 5.5	3.0 2.0	8.0 6.0	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.0 2.5	7.5 6.5	3.0 2.5	7.5 6.5	3.5 3.0	9.5 7.0	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.0 4.0	7.5 9.5	3.0 4.0	7.5 9.5	3.5 4.5	8.5 10.0	ns	*Figures 3 & 4*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.0 2.5	9.5 8.0	3.0 2.5	9.5 8.0	3.5 3.5	11.0 10.0	ns	*Figures 3 & 4*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.5 2.5	10.0 8.5	2.5 2.5	10.0 8.5	3.0 3.5	10.0 10.0	ns	*Figures 3 & 4*
t_{set}	E_n to LE	1.5		1.5		1.5		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	3.5		3.5		3.5		ns	*Figures 3 & 4*



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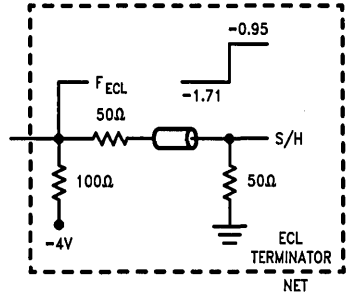
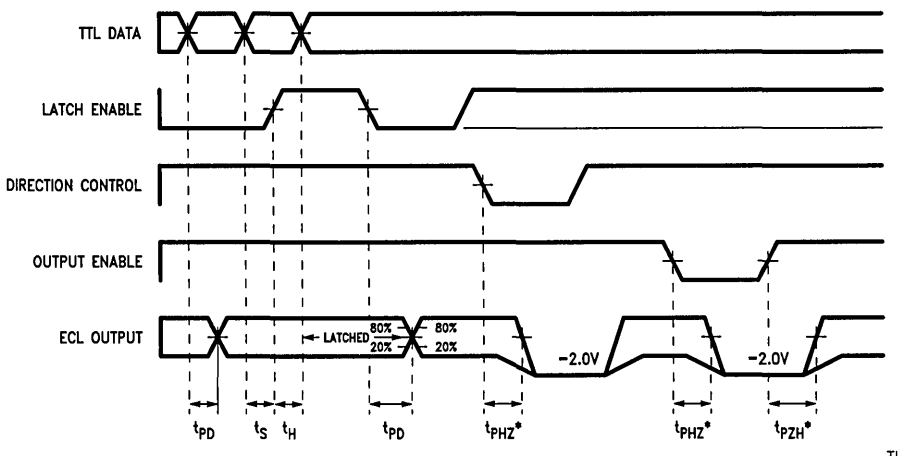


TL/F/9851–12

FIGURE 1. TTL to ECL AC Test Circuit



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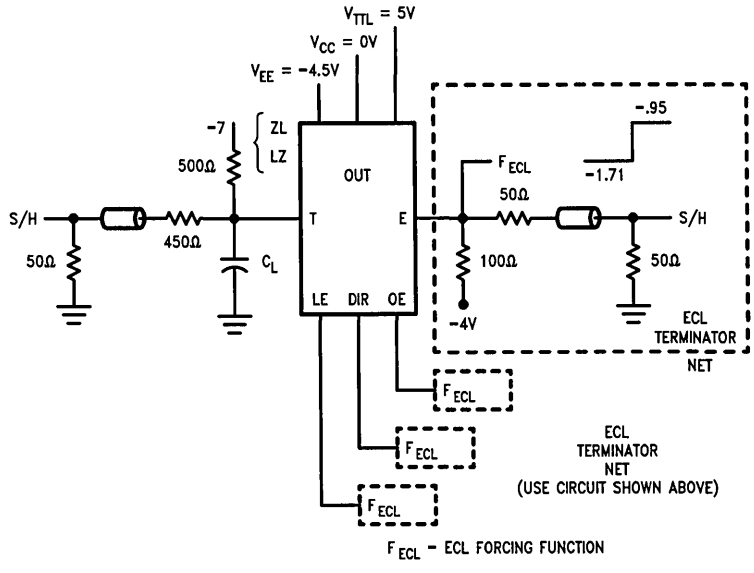
*ECL cut-off transitions use 50% point between V_{OH} and V_{OL}.

FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times



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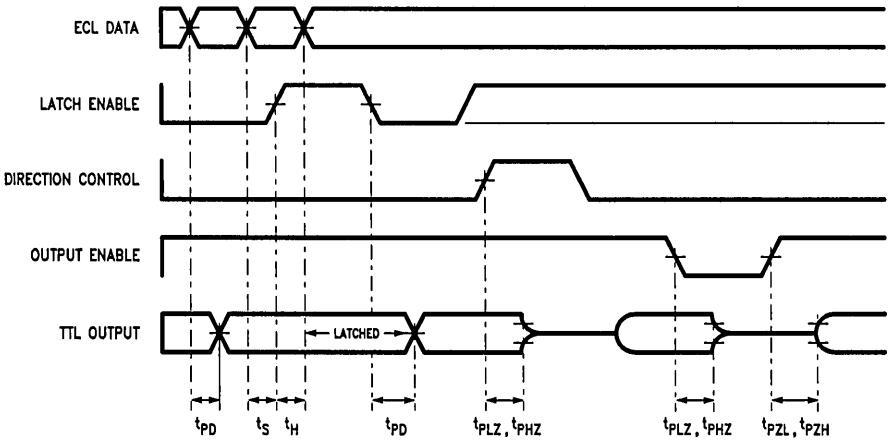
C_L = 50 pF including stray and jig capacitance.

Note: 50Ω to ground termination **must be included** on ECL I/O pins **not** monitored by a 50Ω scope to prevent oscillatory feedback.

FIGURE 3. ECL-to-TTL AC Test Circuit



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ZL and ZH are measured to 1.5V.
HZ is measured to V_{OH} −300 mV.
LZ is measured to V_{OL} +300 mV.

FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times

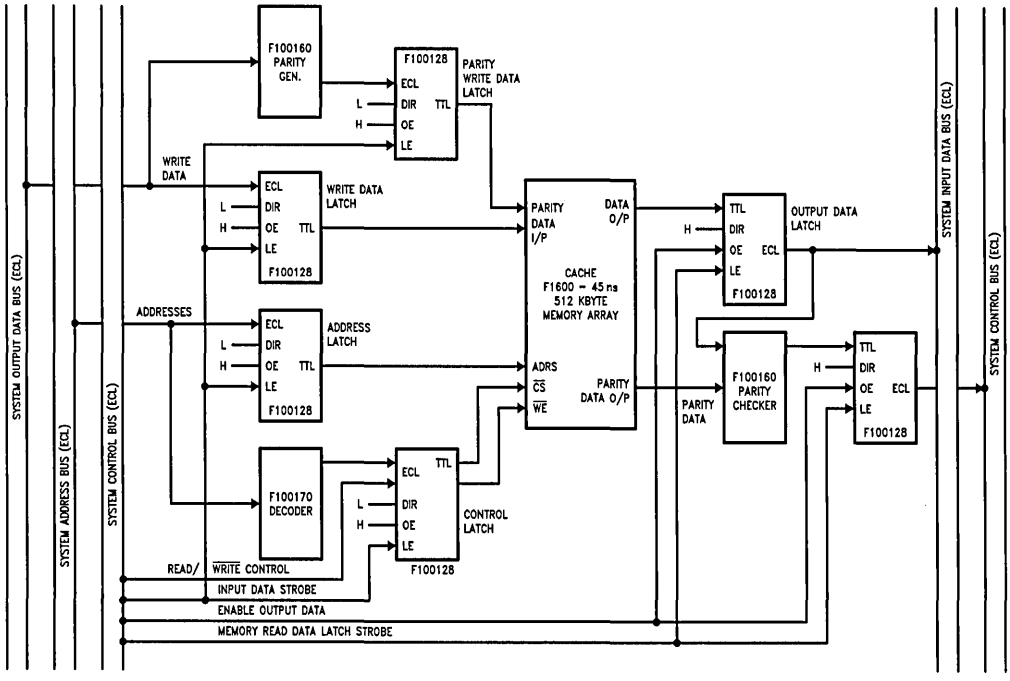

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FIGURE 5. Applications Diagram—MOS/TTL SRAM Interface Using F100128 ECL–TTL Latched Translator

National Semiconductor

F100130
Triple D Latch

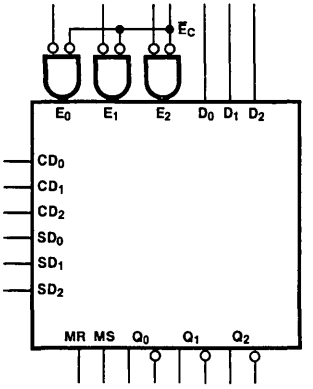
General Description

The F100130 contains three D-type latches with true and complement outputs and with Common Enable ($\overline{E}_C$), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable ($\overline{E}_n$), Direct Set (SD_n) and Direct Clear (CD_n) inputs. The Q output follows its Data (D) input when both $\overline{E}_n$ and $\overline{E}_C$ are LOW (transparent mode). When either $\overline{E}_n$ or $\overline{E}_C$ (or both) are HIGH, a latch stores the last valid data present on its D_n input before $\overline{E}_n$ or $\overline{E}_C$ goes HIGH.

Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs. The individual CD_n and SD_n also override the Enable inputs. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

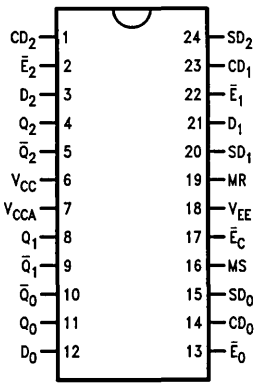
Logic Symbol



TL/F/9852-3

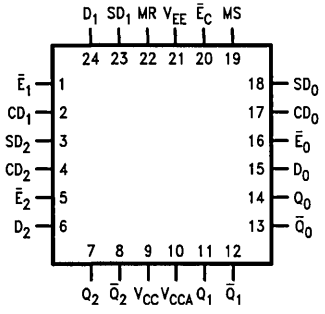
Connection Diagrams

24-Pin DIP



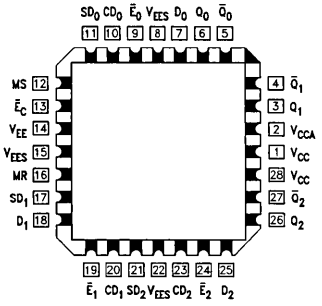
TL/F/9852-1

24-Pin Quad Cerpak



TL/F/9852-2

28-Pin PCC (Preliminary)



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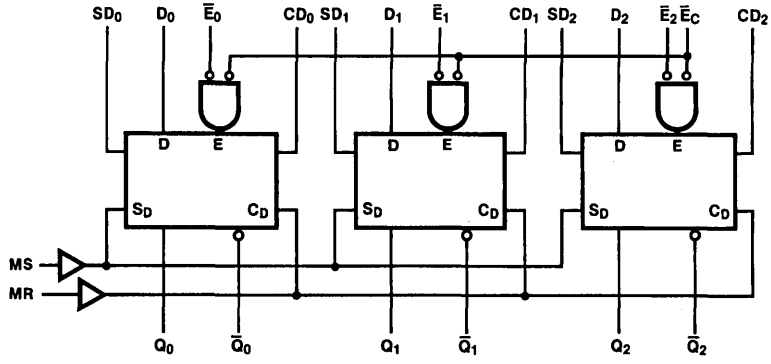
Pin Names	Description
CD_0–CD_2	Individual Direct Clear Inputs
SD_0–SD_2	Individual Direct Set Inputs
$\overline{E}_0$–$\overline{E}_2$	Individual Enable Inputs (Active LOW)
$\overline{E}_C$	Common Enable Input (Active LOW)
D_0–D_2	Data Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

2

Logic Diagram



TL/F/9852–5

Truth Tables (Each Latch)

Latch Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
L	L	L	L	L	L
H	L	L	L	L	H
X	H	X	L	L	Latched*
X	X	H	L	L	Latched*

Asynchronous Operation

Inputs					Outputs
D_n	$\overline{E}_n$	$\overline{E}_C$	MS SD_n	MR CD_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

*Retains data presented before $\overline{E}$ positive transition
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current					
	D_n			350		
	CD_n, SD_n			530	μA	V_{IN} = $V_{IH\ (Max)}$
	$\overline{E}_n$			240		
	$\overline{E}_C$, MR, MS			450		
I_{EE}	Power Supply Current	−149	−106	−74	mA	Inputs Open

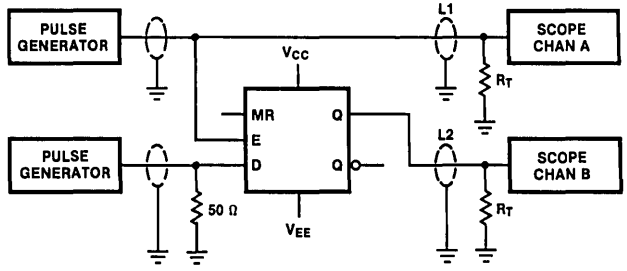
Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.80	0.50	1.70	0.50	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	2.10	0.75	2.00	0.75	2.10	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	2.00	0.60	1.75	0.60	2.00	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*
t_s	Setup Time								
	D_0–D_2	0.90		0.70		0.90			
	CD_n, SD_n (Release Time)	1.20		1.10		1.40		ns	*Figures 3* and *4*
	MR, MS (Release Time)	1.90		1.90		2.00			
t_h	Hold Time D_0–D_2	0.60		0.60		0.80		ns	*Figure 4*
$t_{pw}(L)$	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
$t_{pw}(H)$	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.50	1.60	0.50	1.50	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_C$ to Output	0.65	1.90	0.75	1.80	0.75	1.90	ns	
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n, $\overline{E}_n$ to Output	0.50	1.80	0.60	1.55	0.60	1.80	ns	*Figures 1, 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.30	1.10	2.20	1.10	2.40	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_2 CD_n, SD_n (Release Time) MR, MS (Release Time)	 0.80 1.10 1.80		 0.60 1.00 1.80		 0.80 1.30 2.00		ns	*Figures 3* and *4*
t_h	Hold Time D_0–D_2	0.50		0.50		0.70		ns	*Figure 4*
t_{pw}(L)	Pulse Width LOW $\overline{E}_n$, $\overline{E}_C$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw}(H)	Pulse Width HIGH CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3*



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9852–6

FIGURE 1. AC Test Circuit

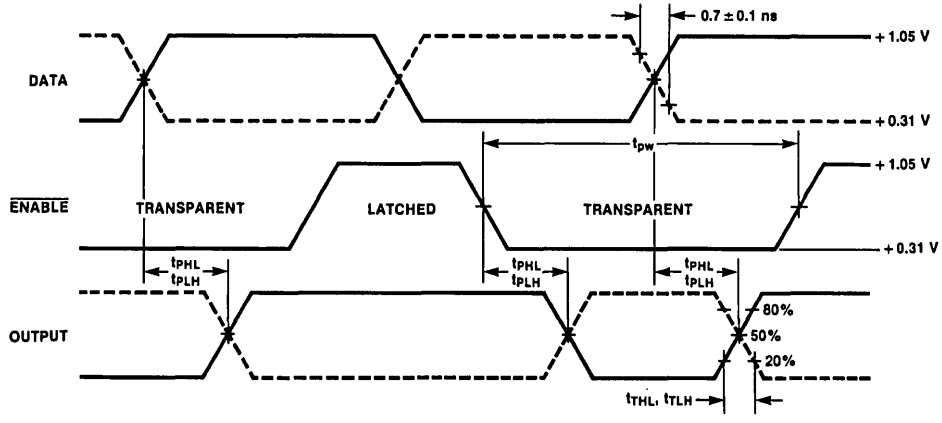


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FIGURE 2. Enable Timing

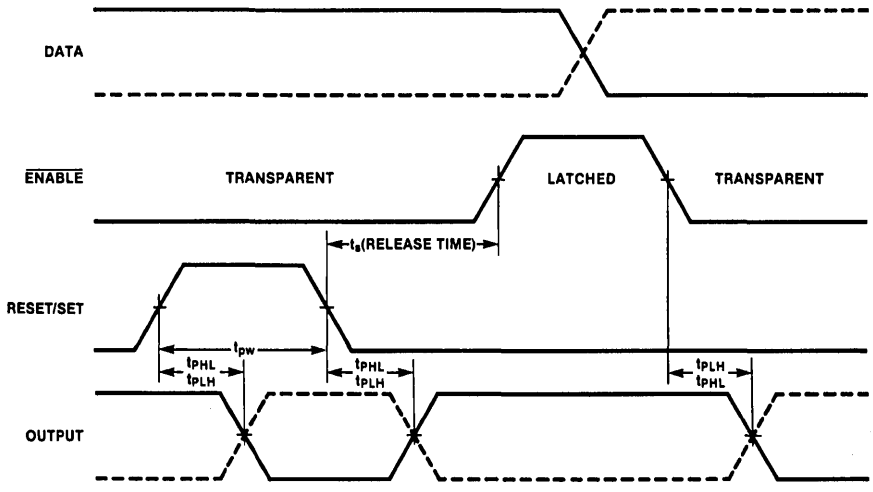

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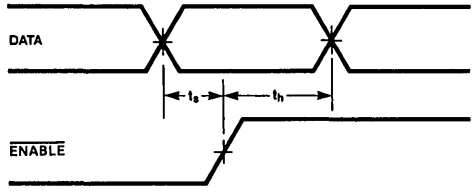
FIGURE 3. Reset Timing



Notes:
t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

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FIGURE 4. Data Setup and Hold Time

National Semiconductor

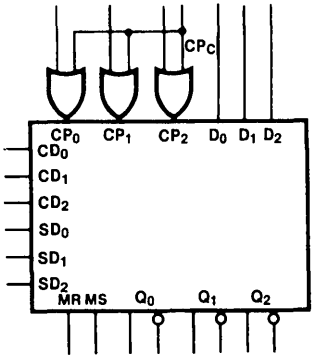
F100131
Triple D Flip-Flop

General Description

The F100131 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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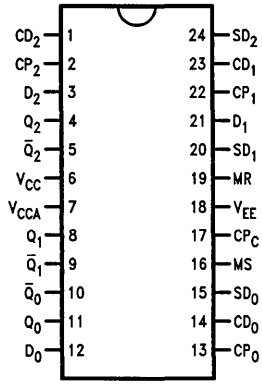
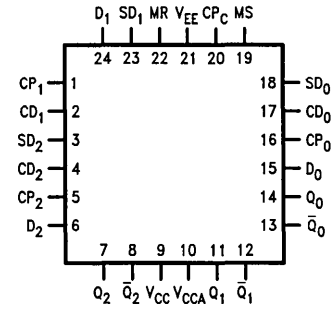
Connection Diagrams

24-Pin DIP



TL/F/9853-1

24-Pin Quad Cerpak



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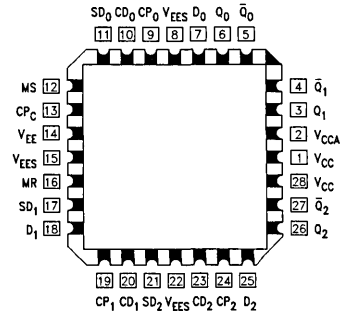
Pin Names	Description
CP_0–CP_2	Individual Clock Inputs
CP_C	Common Clock Input
D_0–D_2	Data Inputs
CD_0–CD_2	Individual Direct Clear Inputs
SD_n	Individual Direct Set Inputs
MR	Master Reset Input
MS	Master Set Input
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

28-Pin PCC (Preliminary)



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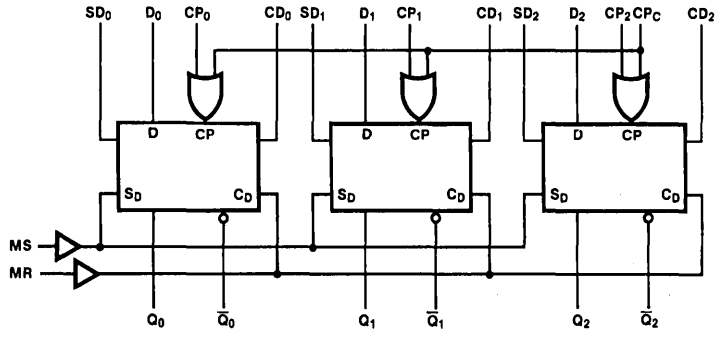
Logic Diagram



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Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t+1)$
L	↗	L	L	L	L
H	↗	L	L	L	H
L	L	↗	L	L	L
H	L	↗	L	L	H
X	L	L	L	L	Qn(t)
X	H	X	L	L	Qn(t)
X	X	H	L	L	Qn(t)

Asynchronous Operation

Inputs					Outputs
D_n	CP_n	CP_C	MS SD_n	MR CD_n	$Q_n(t+1)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t+1 = Time after CP Positive Transition
↗ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current CP_n, D_n MS, MR, CP_C CD_n, SD_n			 240 450 530	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−149	−106	−74	mA	Inputs Open

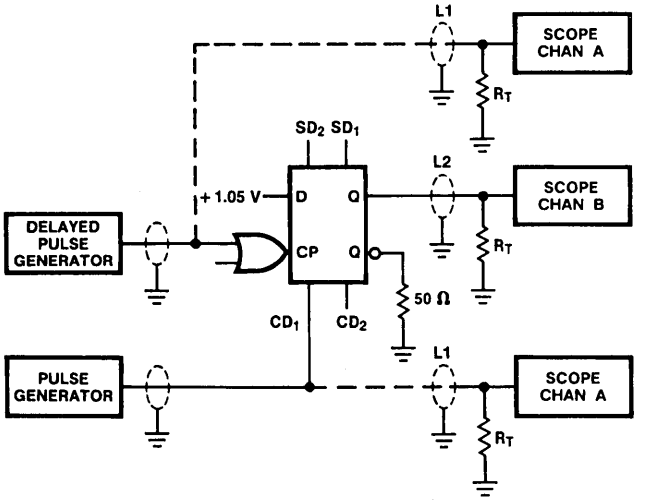
Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	325		325		325		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.40	0.75	2.15	0.70	2.30	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.20	0.70	2.00	0.70	2.20	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.90	0.70	1.70	0.70	1.80	ns	CP_n, CP_C = L	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.70	2.10	0.70	2.00	0.70	2.20		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.70	1.10	2.60	1.10	2.70	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.05	3.05	1.05	2.95	1.05	3.05		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.20	0.45	1.80	0.45	1.90	ns	*Figures 1, 3* and *4*	
t_s	Setup Time D_n CD_n, SD_n (Release Time) MS, MR (Release Time)	 0.90 1.50 2.50		 0.70 1.30 2.30		 0.90 1.50 2.50		ns	*Figure 5* *Figure 4*	
t_h	Hold Time D_n	0.60		0.60		0.80		ns	*Figure 5*	
$t_{pw}(H)$	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figures 3* and *4*	

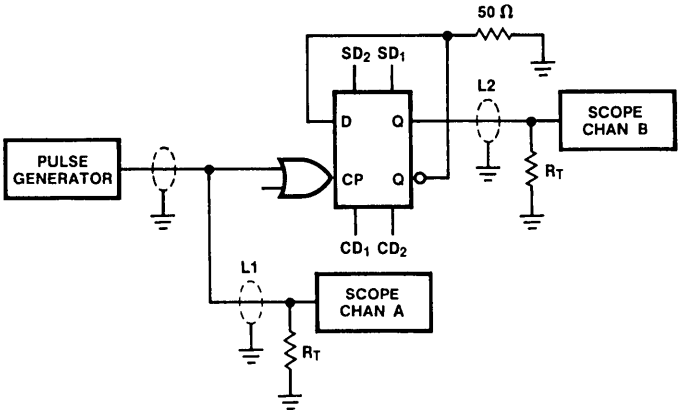
Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions	
		Min	Max	Min	Max	Min	Max			
f_{max}	Toggle Frequency	350		350		350		MHz	*Figures 2* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_C to Output	0.75	2.20	0.75	1.95	0.70	2.10	ns	*Figures 1* and *3*	
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.00	0.70	1.80	0.70	2.00	ns		
t_{PLH} t_{PHL}	Propagation Delay CD_n, SD_n to Output	0.70	1.70	0.70	1.50	0.70	1.60	ns	CP_n, CP_C = L	*Figures 1* and *4*
t_{PLH} t_{PHL}		0.70	1.90	0.70	1.80	0.70	2.00		CP_n, CP_C = H	
t_{PLH} t_{PHL}	Propagation Delay MS, MR to Output	1.10	2.50	1.10	2.40	1.10	2.50	ns	CP_n, CP_C = L	
t_{PLH} t_{PHL}		1.05	2.85	1.05	2.75	1.05	2.85		CP_n, CP_C = H	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.00	0.45	1.60	0.45	1.70	ns	*Figures 1, 3* and *4*	
t_s	Setup Time D_n	0.80		0.60		0.80		ns	*Figure 5*	
	CD_n, SD_n (Release Time)	1.40		1.20		1.40			*Figure 4*	
	MS, MR (Release Time)	2.40		2.20		2.40				
t_h	Hold Time D_n	0.50		0.50		0.70		ns	*Figure 5*	
t_{pw}(H)	Pulse Width HIGH CP_n, CP_C, CD_n, SD_n, MR, MS	2.00		2.00		2.00		ns	*Figure 3* and *4*	



TL/F/9853–6

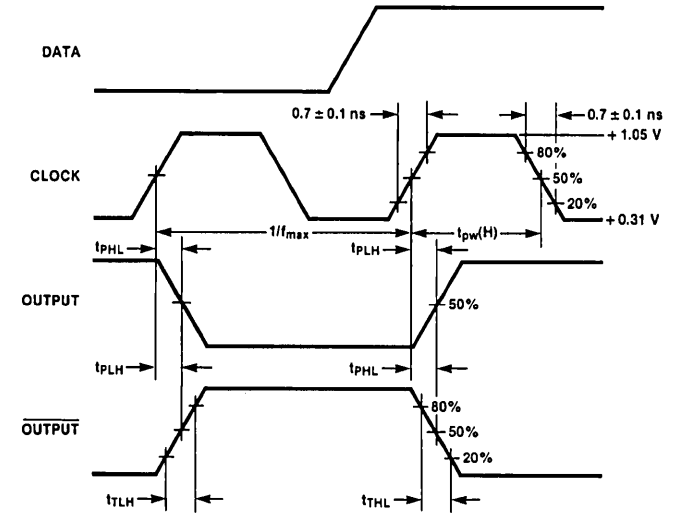
FIGURE 1. AC Test Circuit



TL/F/9853–7

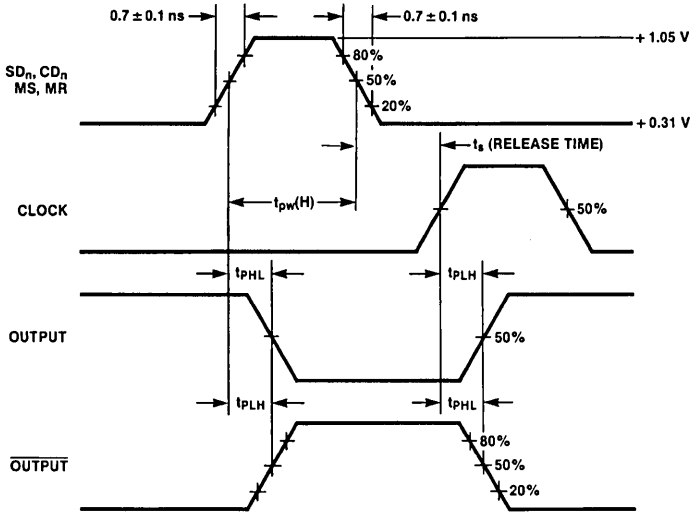
FIGURE 2. Toggle Frequency Test Circuit

Note:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



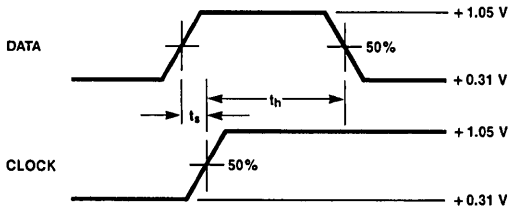
TL/F/9853–8

FIGURE 3. Propagation Delay (Clock) and Transition Times



TL/F/9853–9

FIGURE 4. Propagation Delay (Resets)



TL/F/9853–10

FIGURE 5. Data Setup and Hold Time

Note:

t_s is the minimum time before the transition of the clock that information must be present at the data input.
t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

National Semiconductor

F100135
Triple J-K Flip-Flop

General Description

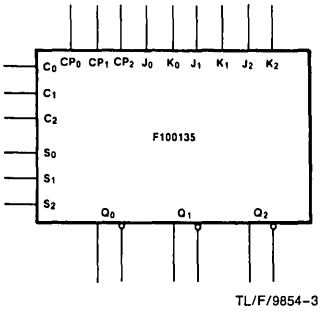
The F100135 contains three J-K, edge-triggered master-slave flip-flops with true and complement outputs. All have individual Clock (CP_n), Clear (C_n), and Set (S_n) inputs. Clocking occurs on the rising edge of CP_n. All inputs have 50 kΩ pull-down resistors.

Features

- Toggle frequency 750 MHz Typical
- Propagation delay 2.2 ns max
- Outputs specified to drive a 50Ω load

Ordering Code: See Section 6

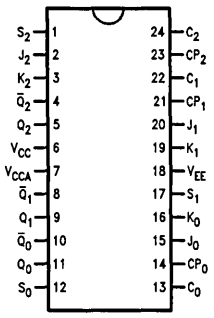
Logic Symbol



TL/F/9854–3

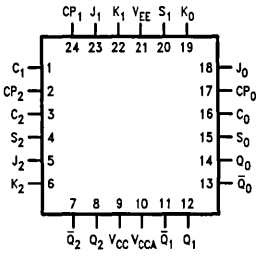
Connection Diagrams

24-Pin DIP



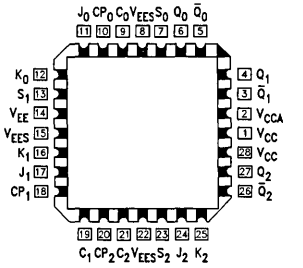
TL/F/9854–1

24-Pin Quad Cerpak



TL/F/9854–2

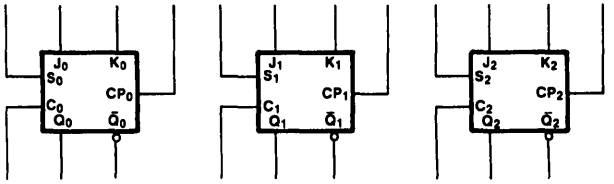
28-Pin PCC (Preliminary)



TL/F/9854–4

Pin Names	Description
J_0–J_2	J Inputs
K_0–K_2	K Inputs
S_0–S_2	Direct Set Inputs
C_0–C_2	Direct Clear Inputs
CP_0–CP_2	Clock Inputs
Q_0–Q_2	Data Outputs
$\overline{Q}_0$–$\overline{Q}_2$	Complementary Data Outputs

Logic Diagram



TL/F/9854–5

Truth Tables (Each Flip-Flop)

Synchronous Operation

Inputs					Outputs
J_n	K_n	CP_n	S_n	C_n	$Q_n(t+1)$
L	L	⌐‾	L	L	$Q_n(t)$
L	H	⌐‾	L	L	L
H	L	⌐‾	L	L	H
H	H	⌐‾	L	L	$\overline{Q_n(t)}$
X	X	H	L	L	$Q_n(t)$
X	X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs					Outputs
J_n	K_n	CP_n	S_n	C_n	Q_n
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t = Time before CP Positive Transition
t + 1 = Time after CP Positive Transition
⌐‾ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			350	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−195	−150	−90	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

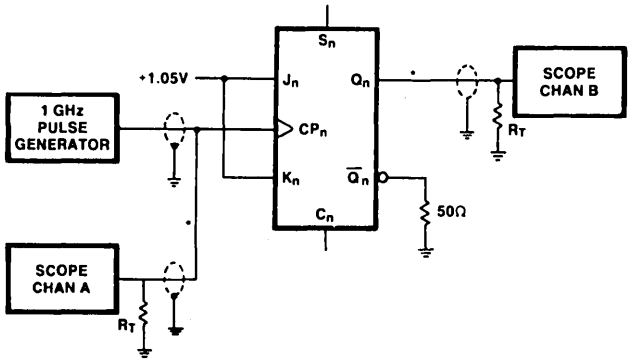
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	600		600		600		MHz	*Figure 1*
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.20	0.70	2.00	0.70	2.20	ns	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay C_n, S_n to Output	0.90	1.80	0.90	2.00	0.90	2.40	ns	CP_n = L, CP_n = H
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.40	0.30	1.40	0.30	1.40	ns	
t_S	Setup Time J_n, K_n to CP_n C_n, S_n (Release Time)	0.90 1.50		0.70 1.30		0.90 1.50		ns	*Figures 2* and *3*
t_H	Hold Time J_n, K_n to CP_n	0.80		0.80		0.80		ns	
t_{pw}(H)	Pulse Width HIGH CP_n, C_n, S_n	2.00		2.00		2.00		ns	

Cerpak AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	650		650		650		MHz	*Figure 1*
t_{PLH} t_{PHL}	Propagation Delay CP_n to Output	0.70	2.00	0.70	1.80	0.70	2.00	ns	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay C_n, S_n to Output	0.90	1.60	0.90	1.80	0.90	2.20	ns	CP_n = L, CP_n = H
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.30	1.30	0.30	1.30	0.30	1.30	ns	
t_S	Setup Time J_n, K_n to CP_n C_n, S_n (Release Time)	0.80 1.40		0.60 1.20		0.80 1.40		ns	*Figures 2* and *3*
t_H	Hold Time J_n, K_n to CP_n	0.70		0.70		0.70		ns	
t_{pw}(H)	Pulse Width HIGH CP_n, C_n, S_n	2.00		2.00		2.00		ns	



TL/F/9854–6

FIGURE 1. Toggle Frequency Test Circuit

Notes:

$V_{CC} = V_{CCA} = +2V$

$V_{EE} = -2.5V$

* = equal electrical length 50Ω lines

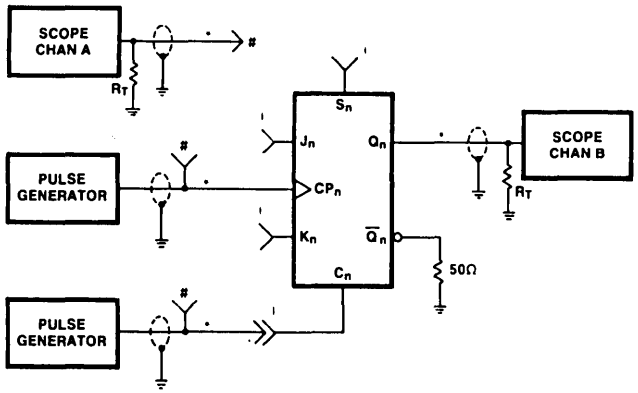
R_T = 50Ω termination

Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Load all unused outputs with 50Ω to GND

Set pulse generator output level for 740 mV p-p at a frequency of 10 MHz as measured at the clock input pin of the device under test. Do not readjust this voltage for frequencies up to f_{max}. The pad isolates the generator output for D.U.T. input impedance variations. Signal voltage measured at the D.U.T. input will vary as input impedance varies with frequency.



TL/F/9854–7

FIGURE 2. AC Test Circuit

Notes:

$V_{CC} = V_{CCA} = +2V$

$V_{EE} = -2.5V$

Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND

R_T = 50Ω termination

Load all unused outputs with 50Ω to GND

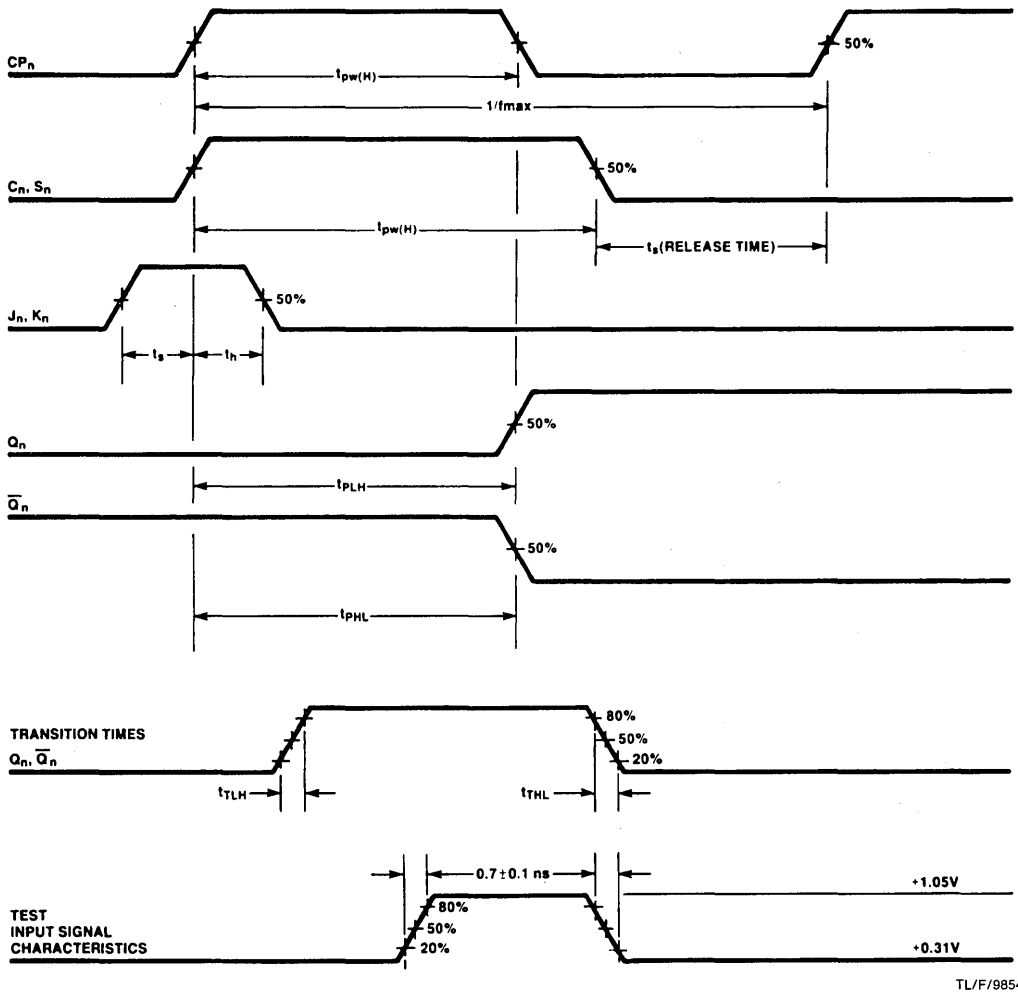
C_L = Fixture and stray capacitance ≤ 3 pF

* = equal electrical length 50Ω lines

= Connect Scope CHAN A to pulse generator as required

† = Connect pulse generator to input under test; else connect input to voltage source set to +1.05 volts for logic HIGH or +0.31 volts for logic LOW

Consult truth table for appropriate logical condition



TL/F/9854–8

FIGURE 3. Propagation Delays and Setup and Hold Time

National Semiconductor

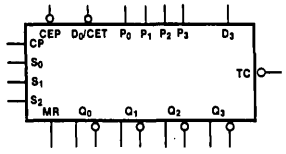
F100136
4-Stage Counter/Shift Register

General Description

The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable ($\overline{CEP}$, $\overline{CET}$) inputs are provided for ease of cascading in multistage counters. One Count Enable ($\overline{CET}$) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count ($\overline{TC}$) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the $\overline{TC}$ output repeats the Q_3 output. The dual nature of this $\overline{TC}/Q_3$ output and the $D_0/\overline{CET}$ input means that one interconnection from one stage to the next higher stage serves as the link for multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

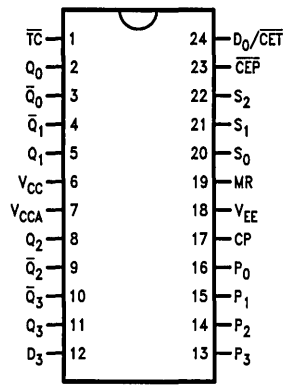
Logic Symbol



TL/F/9855-3

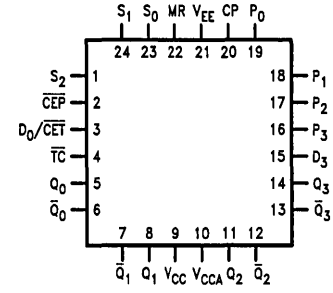
Connection Diagrams

24-Pin DIP



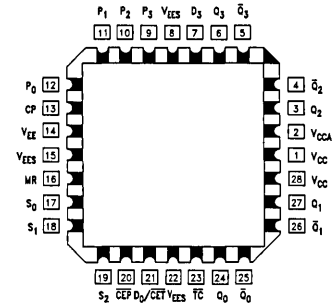
TL/F/9855-1

24-Pin Quad Cerpak



TL/F/9855-2

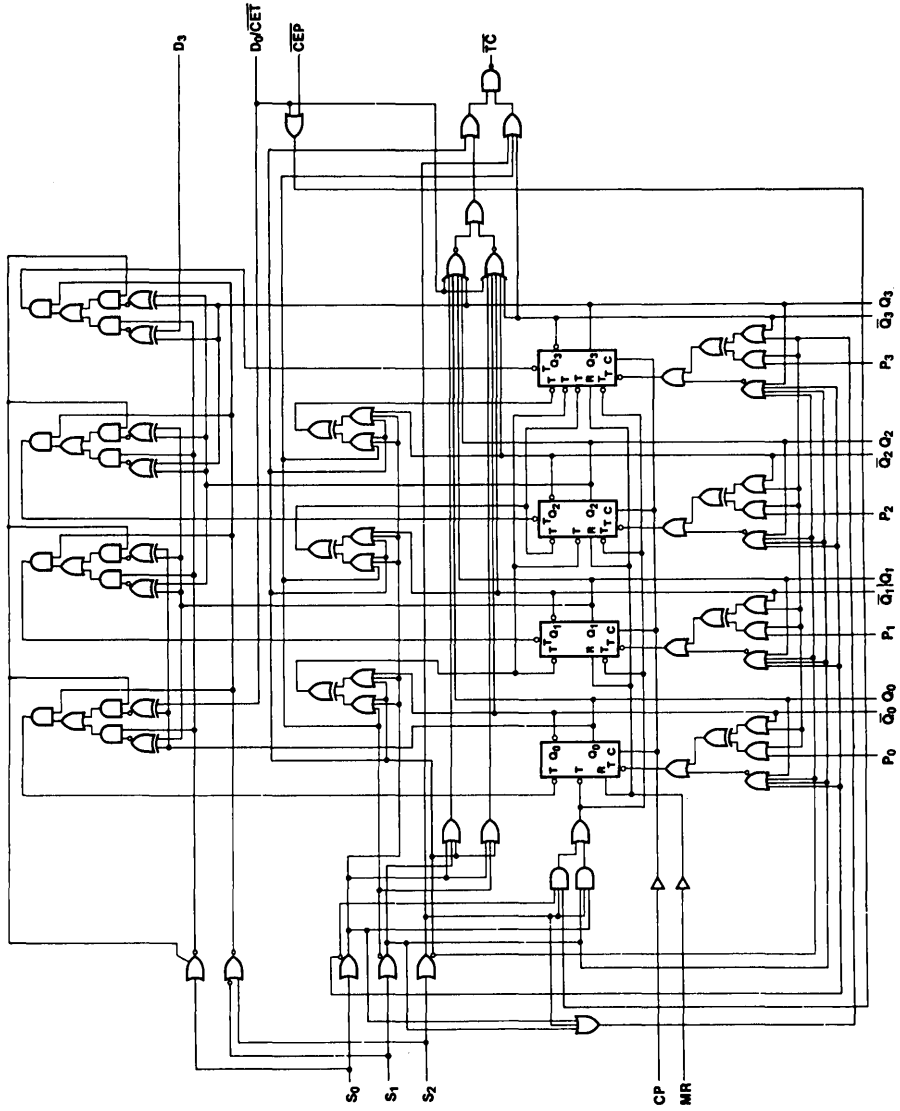
28-Pin PCC (Preliminary)



TL/F/9855-4

Pin Names	Description
CP	Clock Pulse Input
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)
$D_0/\overline{CET}$	Serial Data Input/Count Enable Trickle Input (Active LOW)
S_0–S_2	Select Inputs
MR	Master Reset Input
P_0–P_3	Preset Inputs
D_3	Serial Data Input
$\overline{TC}$	Terminal Count Output
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

Logic Diagram



TL/F/9855-5

Function Select Table

S_2	S_1	S_0	Function
L	L	L	Parallel Load
L	L	H	Complement
L	H	L	Shift Left
L	H	H	Shift Right
H	L	L	Count Down
H	L	H	Clear
H	H	L	Count Up
H	H	H	Hold

Truth Table

Inputs								Outputs					
MR	S_2	S_1	S_0	$\overline{CEP}$	$D_0/\overline{CET}$	D_3	CP	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	Mode
L	L	L	L	X	X	X	↗	P_0	P_1	P_2	P_3	L	Preset (Parallel Load)
L	L	L	H	X	X	X	↗	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	L	Invert
L	L	H	L	X	X	X	↗	Q_1	Q_2	Q_3	D_3	D_3	Shift Left
L	L	H	H	X	X	X	↗	D_0	Q_0	Q_1	Q_2	Q_3*	Shift Right
L	H	L	L	L	L	X	↗	(Q_{0-3}) minus 1				①	Count Down
L	H	L	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	①	Count Down with $\overline{CEP}$ not active
L	H	L	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Down with $\overline{CET}$ not active
L	H	L	H	X	X	X	↗	L	L	L	L	H	Clear
L	H	H	L	L	L	X	↗	(Q_{0-3}) plus 1				②	Count Up
L	H	H	L	H	L	X	X	Q_0	Q_1	Q_2	Q_3	②	Count Up with $\overline{CEP}$ not active
L	H	H	L	X	H	X	X	Q_0	Q_1	Q_2	Q_3	H	Count Up with $\overline{CET}$ not active
L	H	H	H	X	X	X	X	Q_0	Q_1	Q_2	Q_3	H	Hold
H	L	L	L	X	X	X	X	L	L	L	L	L	Asynchronous Master Reset
H	L	L	H	X	X	X	X	L	L	L	L	L	
H	L	H	L	X	X	X	X	L	L	L	L	L	
H	L	H	H	X	X	X	X	L	L	L	L	L	
H	H	L	L	X	L	X	X	L	L	L	L	L	
H	H	L	L	X	H	X	X	L	L	L	L	H	
H	H	L	H	X	X	X	X	L	L	L	L	H	
H	H	H	L	X	X	X	X	L	L	L	L	H	
H	H	H	H	X	X	X	X	L	L	L	L	H	

① = L if Q_0–Q_3 = LLLL
H if Q_0–Q_3 ≠ LLLL

② = L if Q_0–Q_3 = HHHH
H if Q_0–Q_3 ≠ HHHH

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW-to-HIGH Transition

*Before the clock, $\overline{TC}$ is Q_3
After the clock, $\overline{TC}$ is Q_2

2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current					
	P_n, S_n			180		
	$\overline{CEP}$			200		
	MR			240	μA	V_{IN} = $V_{IH\ (Max)}$
	D_3			280		
	CP			390		
	$D_0/\overline{CET}$			530		
I_{EE}	Power Supply Current	−283	−195	−136	mA	Inputs Open

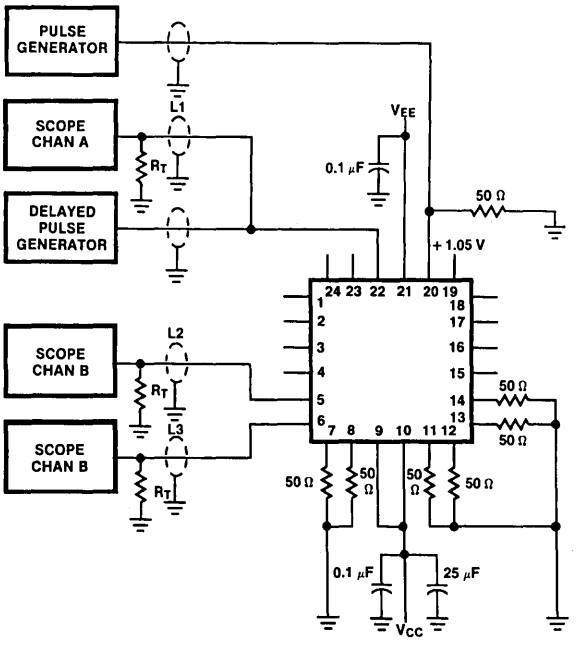
Ceramic Dual-In-Line Package AC Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	2.10	0.85	2.10	0.85	2.25	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.80	1.90	4.60	1.90	5.20	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.95	1.35	2.95	1.20	3.10	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.80	2.20	4.80	2.20	5.30	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.20	1.40	3.20	1.40	3.50	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	0.90	3.80	1.00	3.80	1.00	4.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time								
	D_3	1.20		1.20		1.20			
	P_n	1.70		1.70		1.70			
	$D_0/\overline{CET}$, $\overline{CEP}$	1.45		1.45		1.45		ns	*Figure 6*
	S_n	3.30		3.30		3.30			
	MR (Release Time)	2.60		2.60		2.60			
t_h	Hold Time								
	D_3	0.20		0.20		0.20			
	P_n	0.10		0.10		0.10			
	$D_0/\overline{CET}$, $\overline{CEP}$	0.20		0.20		0.20		ns	*Figure 6*
	S_n	−0.90		−0.90		−0.90			
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	250		250		250		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	0.85	1.90	0.85	1.90	0.85	2.05	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{TC}$	1.90	4.60	1.90	4.40	1.90	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Q_n, $\overline{Q}_n$	1.20	2.75	1.35	2.75	1.20	2.90	ns	*Figures 1* and *4*
t_{PLH} t_{PHL}	Propagation Delay MR to $\overline{TC}$	2.20	4.60	2.20	4.60	2.20	5.10	ns	
t_{PLH} t_{PHL}	Propagation Delay $D_0/\overline{CET}$ to $\overline{TC}$	1.40	3.00	1.40	3.00	1.40	3.30	ns	*Figures 1* and *5*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{TC}$	0.90	3.60	1.00	3.60	1.00	4.10	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n MR (Release Time)	 1.10 1.60 1.35 3.20 2.50		 1.10 1.60 1.35 3.20 2.50		 1.10 1.60 1.35 3.20 2.50		ns	*Figure 6*
t_h	Hold Time D_3 P_n $D_0/\overline{CET}$, $\overline{CEP}$ S_n	 0.10 0 0.10 −1.00		 0.10 0 0.10 −1.00		 0.10 0 0.10 −1.00		ns	*Figure 6*
$t_{pw}(H)$	Pulse Width HIGH CP, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1, L2 and L3 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

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FIGURE 1. AC Test Circuit

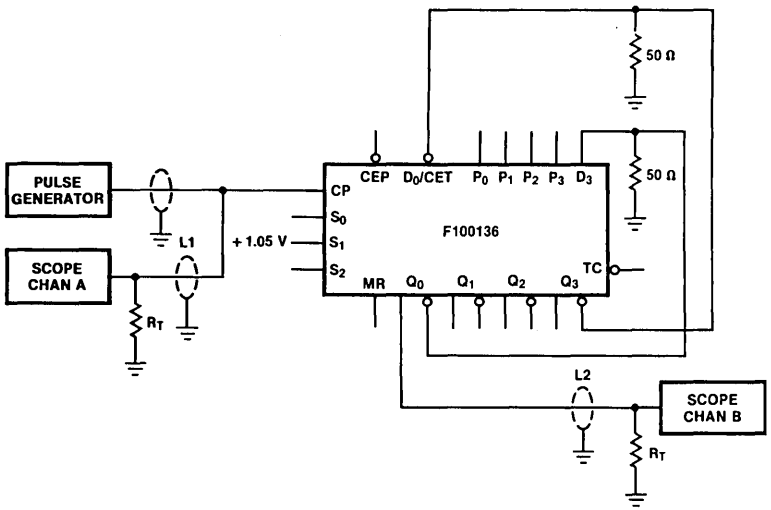

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FIGURE 2. Shift Frequency Test Circuit (Shift Left)

Notes:

For shift right mode, +1.05V is applied at S_0.

The feedback path from output to input should be as short as possible.

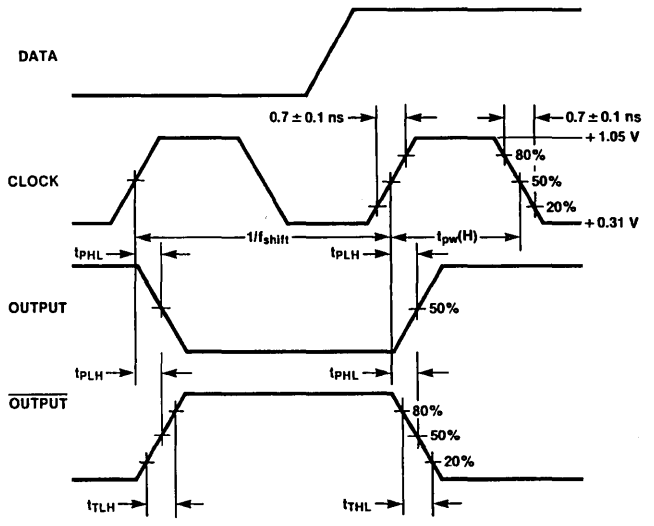

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FIGURE 3. Propagation Delay (Clock) and Transition Times

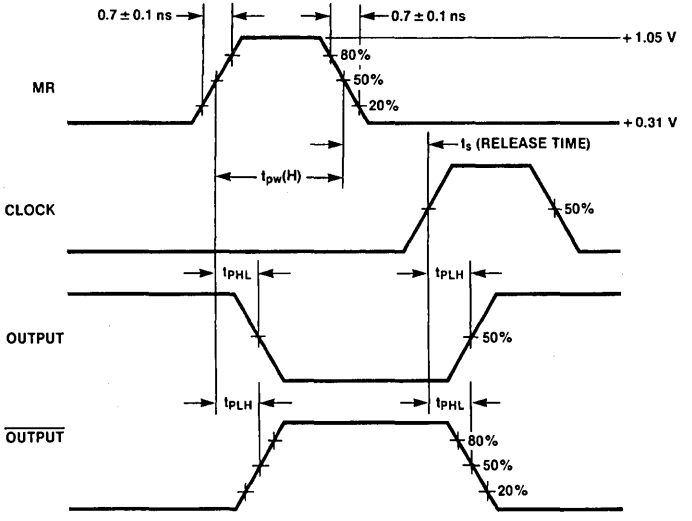

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FIGURE 4. Propagation Delay (Reset)

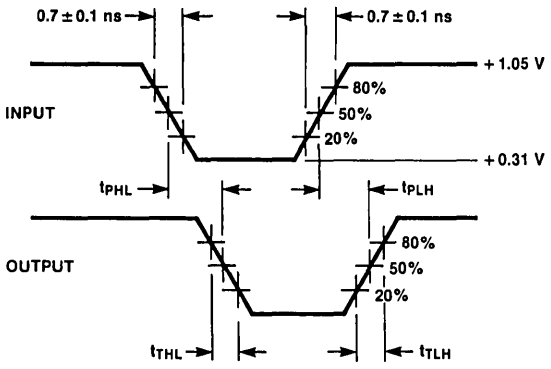

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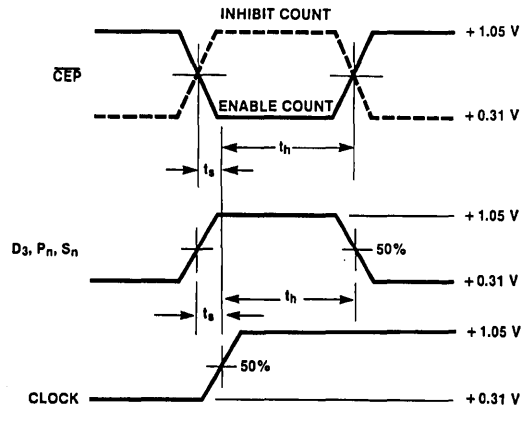
FIGURE 5. Propagation Delay (Serial Data, Selects)



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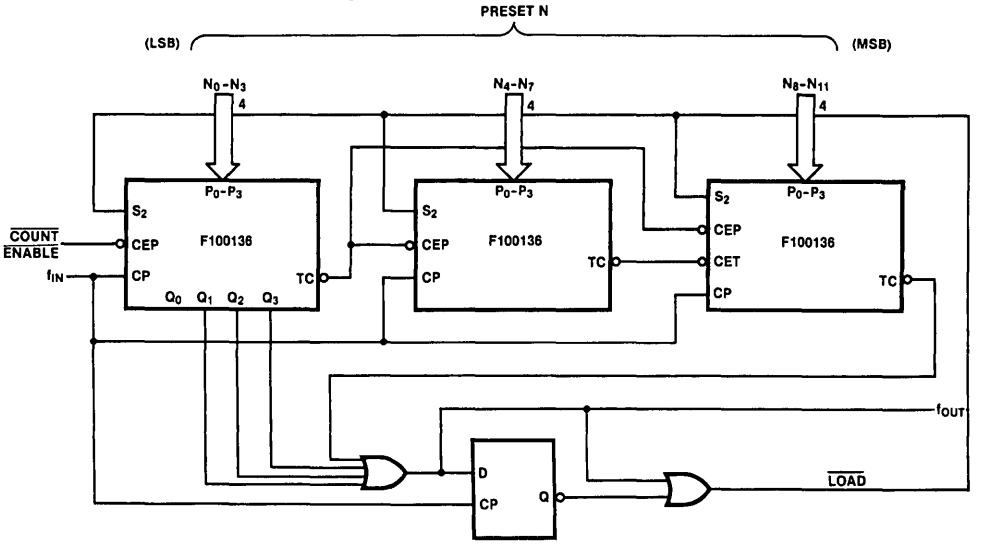
Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.
t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time

Applications

3-Stage Divider, Preset Count Down Mode



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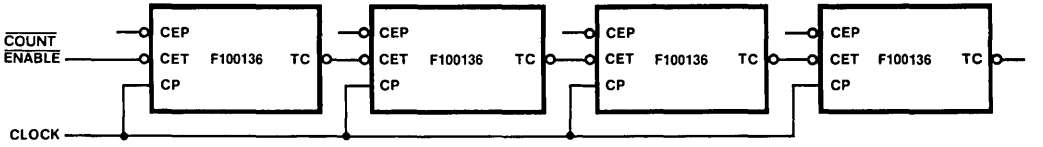
Note:

If $S_0 = S_1 = S_2$ = LOW, then T_C = LOW

Slow Expansion Scheme



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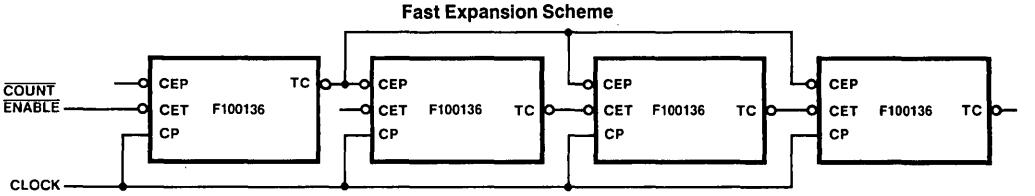
Fast Expansion Scheme



TL/F/9855–15

National Semiconductor

F100141
8-Bit Shift Register

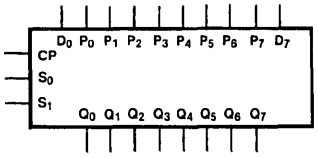
General Description

The F100141 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1, which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

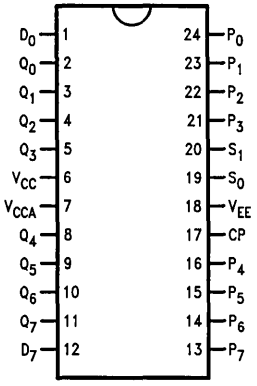
Logic Symbol



TL/F/9856–1

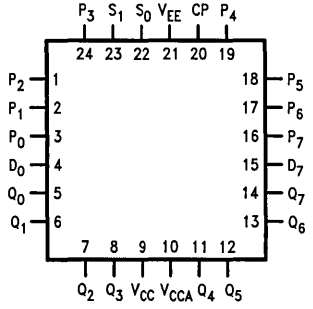
Connection Diagrams

24-Pin DIP



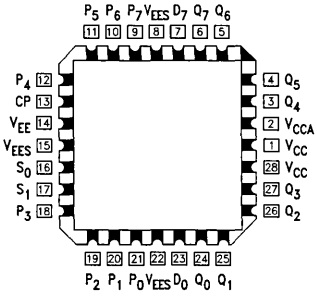
TL/F/9856–2

24-Pin Quad Cerpak



TL/F/9856–3

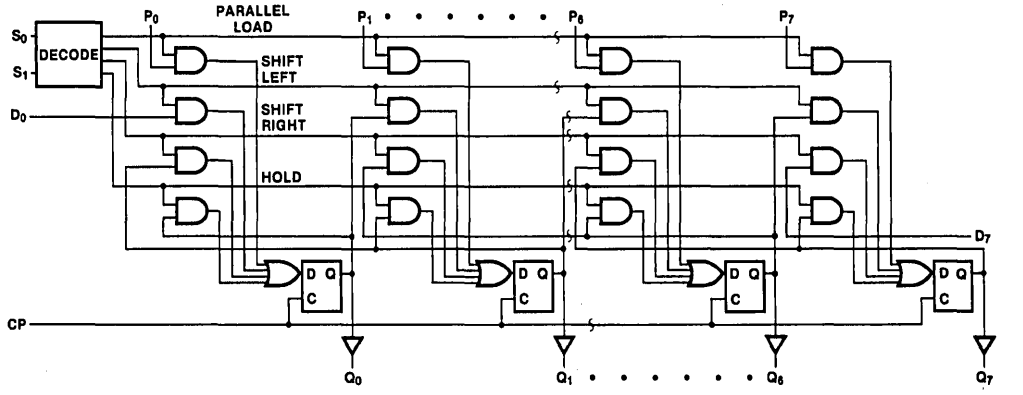
28-Pin PCC (Preliminary)



TL/F/9856–4

Pin Names	Description
CP	Clock Input
S_0, S_1	Select Inputs
D_0, D_7	Serial Inputs
P_0–P_7	Parallel Inputs
Q_0–Q_7	Data Outputs

Logic Diagram



TL/F/9856–5

Truth Table

Function	Inputs					Outputs							
	D_7	D_0	S_1	S_0	CP	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Load Register	X	X	L	L	↗	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0
Shift Left	X	L	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	L
Shift Left	X	H	L	H	↗	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	H
Shift Right	L	X	H	L	↗	L	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Shift Right	H	X	H	L	↗	H	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
Hold	X	X	H	H	X	No Change							
Hold	X	X	X	X	H								
Hold	X	X	X	X	L								

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current D_n, P_n, S_n CP			 220 550	 μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−238	−170	−119	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

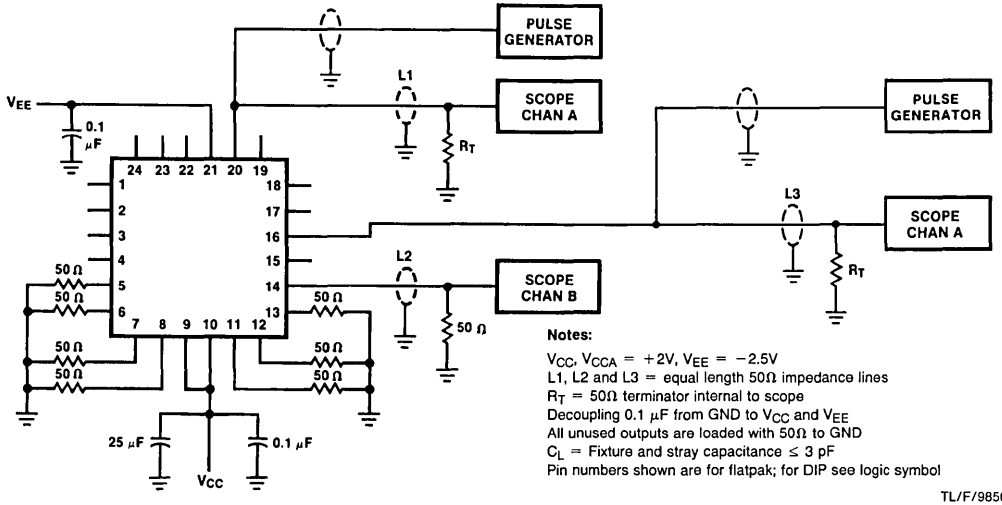
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	275		275		255		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	2.40	1.10	2.30	1.10	2.50	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	
t_s	Setup Time D_n, P_n S_n	 0.85 2.20		 0.85 2.20		 0.85 2.20		ns	*Figure 4*
t_h	Hold D_n, P_n S_n	 0.60 0.10		 0.60 0.10		 0.60 0.10		ns	
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{shift}	Shift Frequency	300		300		280		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP to Output	0.90	2.20	1.10	2.10	1.10	2.30	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	
t_s	Setup Time D_n, P_n S_n	 0.75 2.10		 0.75 2.10		 0.75 2.10		ns	*Figure 4*
t_h	Hold D_n, P_n S_n	 0.50 0		 0.50 0		 0.50 0		ns	
t_{pw}(H)	Pulse Width HIGH CP	2.00		2.00		2.00		ns	*Figure 3*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

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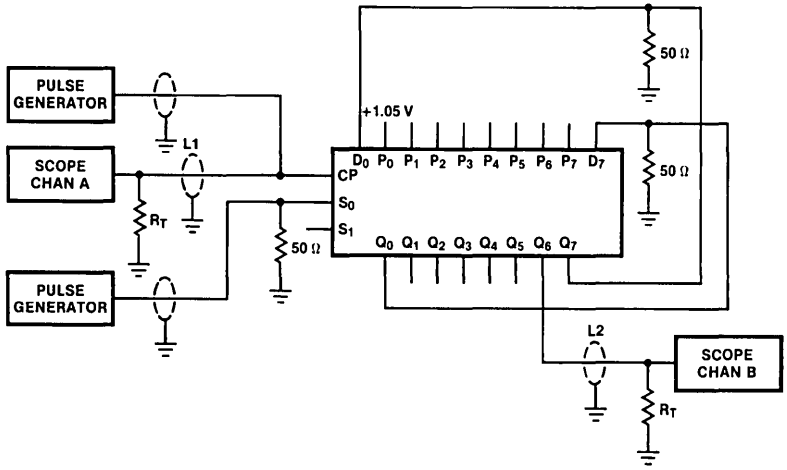
FIGURE 1. AC Test Circuit



Notes:

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For shift right mode pulse generator connected to S_0 is moved to S_1.
Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.
The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

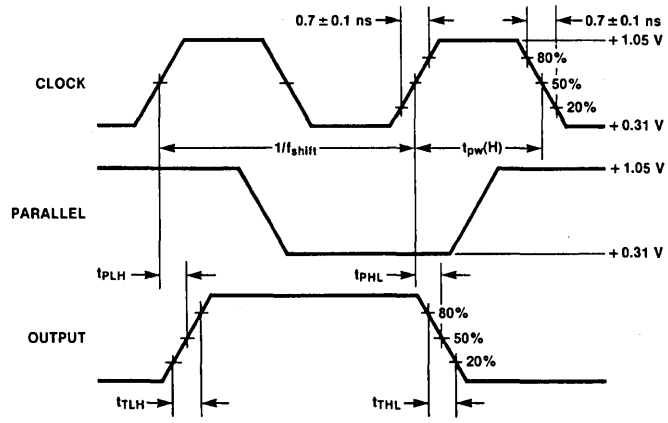

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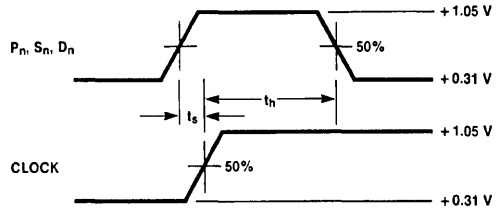
FIGURE 3. Propagation Delay and Transition Times



TL/F/9856–9

FIGURE 4. Setup and Hold Times

Note:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

National Semiconductor

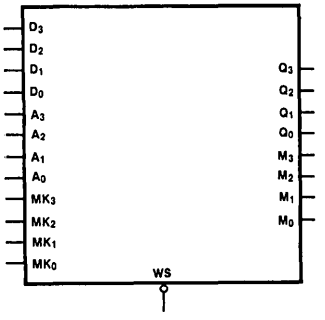
F100142
4 x 4-Bit Content Addressable Memory

General Description

The F100142 is a 4 word by 4-bit Content Addressable Memory (CAM). Reading is accomplished when an address select input (A_0, A_7, A_2, A_3) is LOW and the write strobe input ($\overline{WS}$) is HIGH. The corresponding stored word appears on the data outputs (Q_0–Q_3). Writing can be performed to individual bits of a word or to the whole word. (A LOW on an address select input enables a 4-bit word.) A LOW on a bit mask input (MK_0, MK_1, MK_2, MK_3) enables a bit within all four 4-bit words. Write data is presented on the data inputs (D_0, D_1, D_2, D_3) and is latched into the addressed bit latch when the write strobe input ($\overline{WS}$) is LOW. Hence, the bit mask inputs are used to selectively store data bit-wise within an addressed word. During writing, the data input word is simultaneously compared to each of the stored memory words. A search/compare is performed by placing a LOW on the bit mask inputs and presenting a data pattern to the data inputs. Corresponding to the bit mask inputs, the match outputs (M_0–M_3) go LOW if a data bit of the pattern matches the respective stored bit. A HIGH on any bit mask input forces a LOW on the respective match output. Each input has a 50 kΩ (typical) pull-down resistor to V_{EE}.

Ordering Code: See Section 6

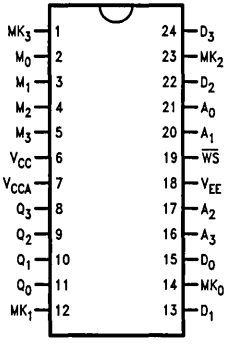
Logic Symbol



TL/F/9857–3

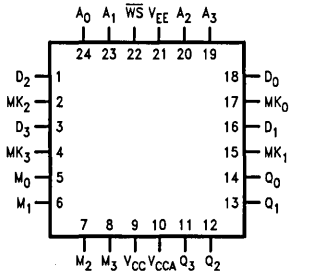
Connection Diagrams

24-Pin DIP



TL/F/9857–1

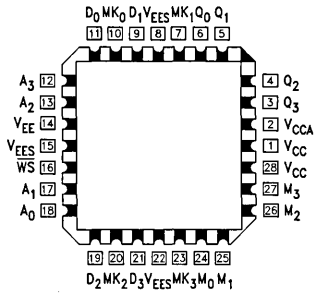
24-Pin Quad Cerpak



TL/F/9857–2

Pin Names	Description
MK_0–MK_3	Data Mask Inputs
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WS}$	Write Strobe Input
M_0–M_3	Match Outputs
Q_0–Q_3	Data Outputs

28-Pin PCC (Preliminary)



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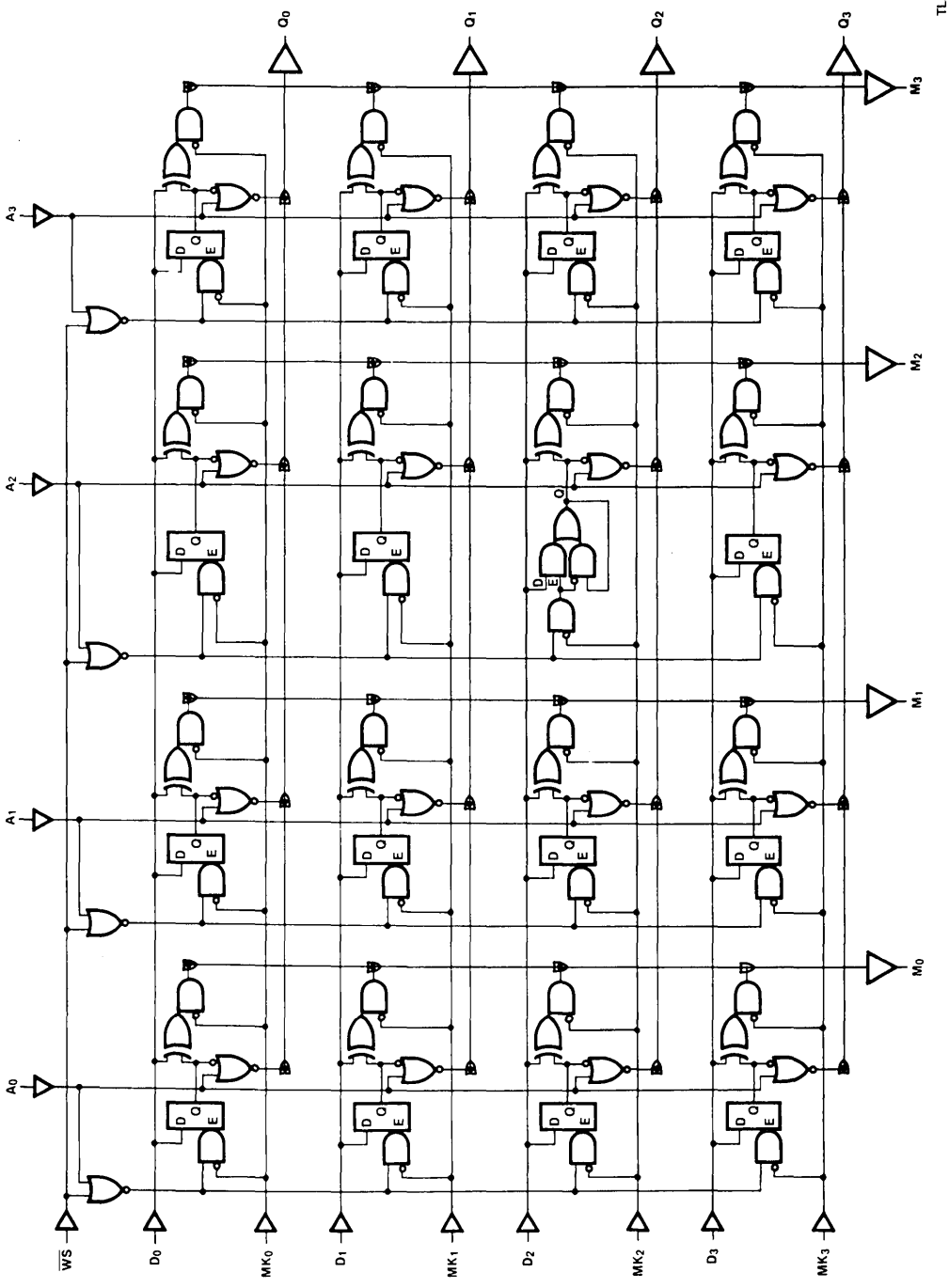
Logic Diagram



TL/F/9857–5

Truth Table

Operation	Inputs				Flip-Flop	Outputs	
	$\overline{WS}$	A_I	D_J	MK_J	Q_{IJ}	M_I	Q_J
	$\overline{WS}$	A_0 A_1 A_2 A_3	D_0 D_1 D_2 D_3	MK_0 MK_1 MK_2 MK_3		M_0 M_1 M_2 M_3	Q_0 Q_1 Q_2 Q_3
Write Disabled	X X	H L	X X	X H	NC NC	X L	L $Q_{ij}n-1$
Write	L L	L L	H L	L L	H L	L L	H L
Read	H H	L L	X X	X X	H L	X X	H L
Match Masked	H	X	X	H	NC	L	X
Match Not Satisfied	H H H H	L H H L	H H L L	L L L L	L L H H	H H H H	L L L H
Match Satisfied	H H H H	L H H L	H H L L	L L L L	H H L L	L L L L	H L L L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change from Previous State
$\overline{WS}$ = Write Strobe
A_i = Address for ith Word
D_j = Data for jth Bit
MK_j = Data Mask for jth Bit
H = Mask
Q_{ij} = Cell State for ith Word, jth Bit
M_i = Match Output of ith Word
L = True
Q_j = Data Output of jth Bit
Q_{n-1} = Previous Cell State

2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			200	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−288	−190	−114	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

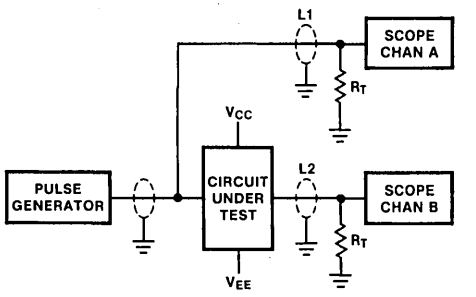
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.40	1.20	4.30	1.20	4.50	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.70	1.60	3.60	1.60	3.80	ns	*Figure 5*
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.90	1.20	3.90	1.20	4.00	ns	
t_{DD}	Data In to New Data Out	1.70	4.40	1.70	4.40	1.70	4.60	ns	*Figure 2*
t_{WD}	Write to New Data Out	2.50	5.40	2.50	5.20	2.30	5.10	ns	
t_{AM}	Address to Match	2.50	4.60	2.50	4.60	2.50	4.90	ns	
t_{MD}	Mask to Data	2.20	4.90	2.20	4.80	2.20	5.00	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.90	2.80	4.80	2.80	5.10	ns	
t_W	Write Pulse Width	1.30		1.30		1.30		ns	*Figuro 1*
t_{AS}	Address Setup before Write Time	1.40		1.40		1.40		ns	
t_{AH}	Address Hold after Write Time	1.40		1.40		1.40		ns	
t_{DS}	Data In Setup before Write Time	0.60		0.60		0.60		ns	
t_{DH}	Data In Hold after Write Time	1.10		1.10		1.10		ns	
t_{MH}	Mask In Hold Write Time	2.50		2.50		2.50		ns	
t_{MS}	Mask In Setup Write Time	1.10		1.10		1.10		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	*Figure 2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{AD}	Address to Data Out	1.20	4.20	1.20	4.10	1.20	4.30	ns	*Figures 2* and *3*
t_{DM}	Data In to Match Out Time	1.60	3.50	1.60	3.40	1.60	3.60	ns	*Figure 5*
t_{MM}	Mask In to "Enable Partial" Match Out Time	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{DD}	Data In to New Data Out	1.70	4.20	1.70	4.20	1.70	4.40	ns	*Figure 2*
t_{WD}	Write to New Data Out	2.50	5.20	2.50	5.00	2.30	4.90	ns	
t_{AM}	Address to Match	2.50	4.40	2.50	4.40	2.50	4.70	ns	
t_{MD}	Mask to Data	2.20	4.70	2.20	4.60	2.20	4.80	ns	
t_{WSM}	$\overline{WS}$ to Match	2.80	4.70	2.80	4.60	2.80	4.90	ns	
t_W	Write Pulse Width	1.20		1.20		1.20		ns	*Figure 1*
t_{AS}	Address Setup before Write Time	1.30		1.30		1.30		ns	
t_{AH}	Address Hold after Write Time	1.30		1.30		1.30		ns	
t_{DS}	Data In Setup before Write Time	0.50		0.50		0.50		ns	
t_{DH}	Data In Hold after Write Time	1.00		1.00		1.00		ns	
t_{MH}	Mask In Hold Write Time	2.40		2.40		2.40		ns	
t_{MS}	Mask In Setup Write Time	1.00		1.00		1.00		ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	*Figure 2*

Switching Waveforms

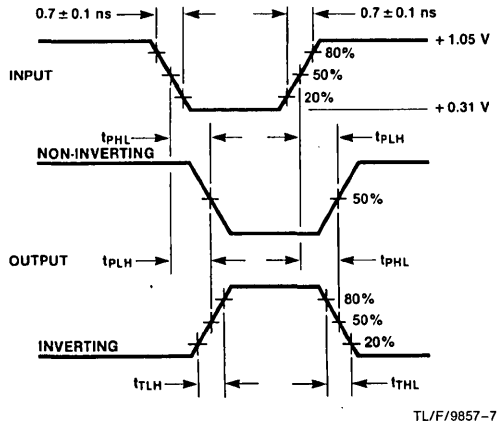


TL/F/9857–6

FIGURE 1. AC Test Circuit

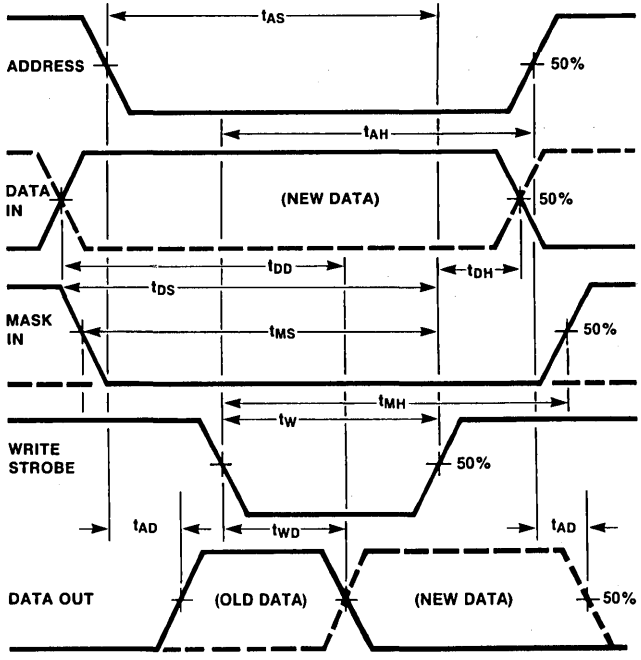
Note:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1, L2 and L3 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9857–7

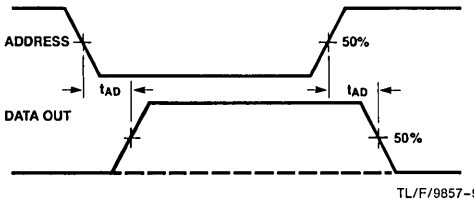
FIGURE 2. Output Rise and Fall Times and Waveforms



TL/F/9857–8

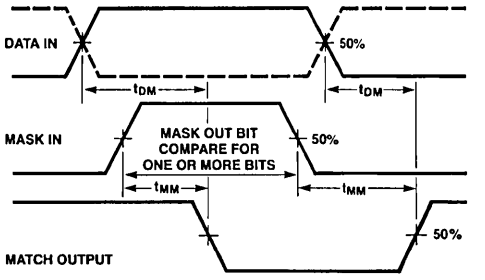
FIGURE 3. Write Mode and Read/Write Mode Waveforms

Switching Waveforms (Continued)



TL/F/9857–9

FIGURE 4. Read Mode Waveforms

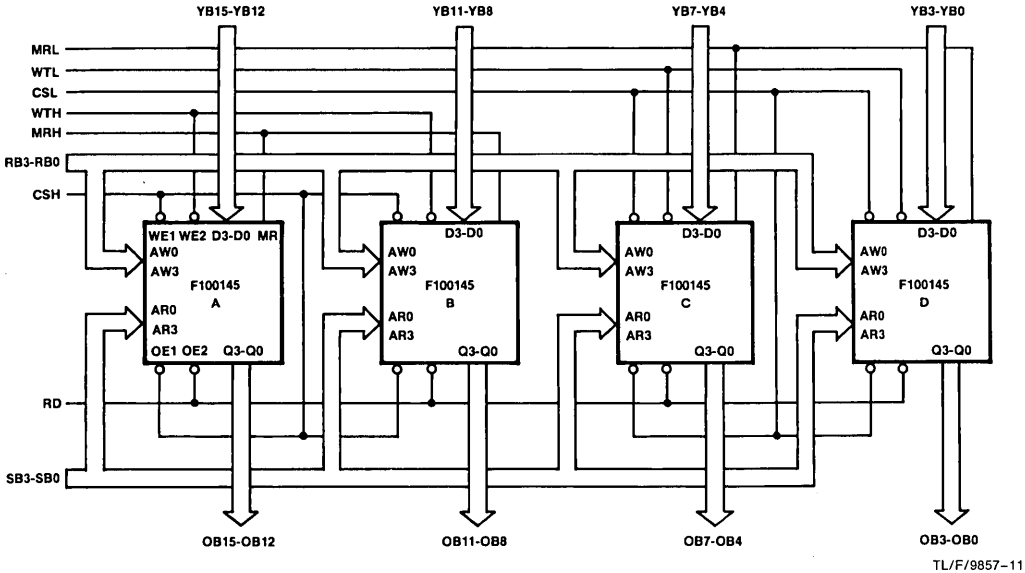


TL/F/9857–10

FIGURE 5. Search Mode Waveforms

Application

The F100142 is an ideal choice for the register file unit of a bit-slice processor. *Figure 5* shows the configuration of four F100145s into a 16 x 16 register file. The write enbles (WE_1, WE_2) and output enables (OE_1, OE_2) are configured to allow access to one array of sixteen 16-bit registers or two arrays of sixteen 8-bit registers. Simultaneous read and write addressing is made possible with separate buses. Also, reading and then writing to the same address is easily and efficiently done by tying one write enable to an output enable.



TL/F/9857–11

FIGURE 5. 16 x 16 Register File (Two 16 x 8 Register Files)

National Semiconductor

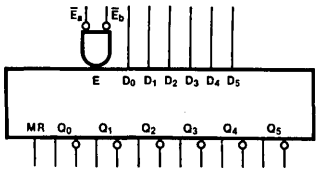
F100150
Hex D Latch

General Description

The F100150 contains six D-type latches with true and complement outputs, a pair of common Enables ($\overline{E}_a$ and $\overline{E}_b$), and a common Master Reset (MR). A Q output follows its D input when both $\overline{E}_a$ and $\overline{E}_b$ are LOW. When either $\overline{E}_a$ or $\overline{E}_b$ (or both) are HIGH, a latch stores the last valid data present on its D input before $\overline{E}_a$ or $\overline{E}_b$ went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

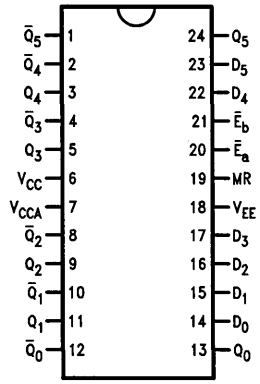
Logic Symbol



TL/F/9858–3

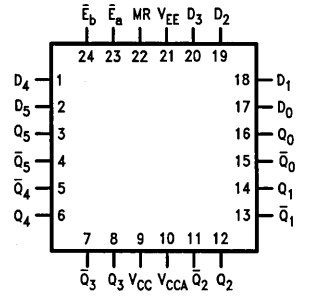
Connection Diagrams

24-Pin DIP



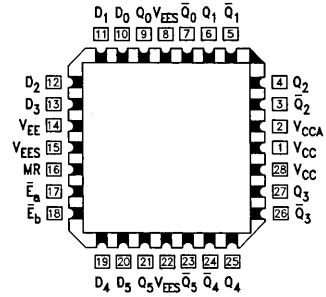
TL/F/9858–1

24-Pin Quad Cerpak



TL/F/9858–2

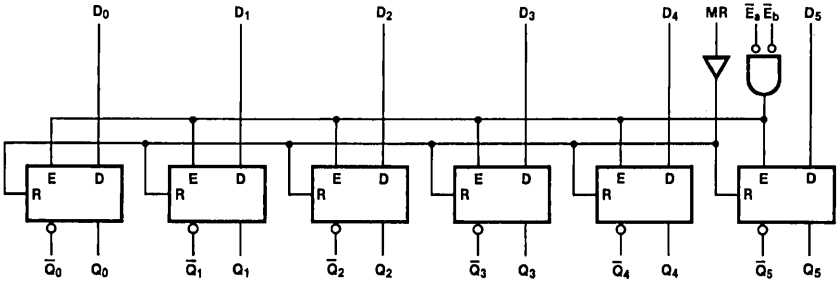
28-Pin PCC (Preliminary)



TL/F/9858–4

Pin Names	Description
D_0–D_5	Data Inputs
$\overline{E}_a$, $\overline{E}_b$	Common Enable Inputs (Active LOW)
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

Logic Diagram



TL/F/9858–5

Truth Tables (Each Latch)

Latch Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
L	L	L	L	L
H	L	L	L	H
X	H	X	L	Latched*
X	X	H	L	Latched*

*Retains data present before $\overline{E}$ positive transition

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Asynchronous Operation

Inputs				Outputs
D_n	$\overline{E}_a$	$\overline{E}_b$	MR	Q_n
X	X	X	H	L

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current MR D_n $\overline{E}_a$, $\overline{E}_b$			 450 340 520	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−159	−113	−79	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

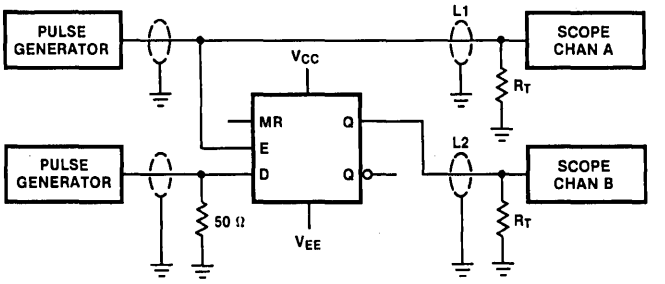
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.45	1.50	0.50	1.40	0.50	1.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	2.05	0.75	1.85	0.75	2.05	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.40	0.90	2.40	0.90	2.60	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.70 2.10		 0.70 2.10		 0.70 2.10		ns	*Figures 3* and *4*
t_h	Hold Time, D_0–D_5	0.70		0.70		0.70		ns	*Figure 4*
t_{pw}(L)	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw}(L)	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output (Transparent Mode)	0.45	1.30	0.50	1.20	0.50	1.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_a$, $\overline{E}_b$ to Output	0.75	1.85	0.75	1.65	0.75	1.85	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.80	2.20	0.90	2.20	0.90	2.40	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.60 2.00		 0.60 2.00		 0.60 2.00		ns	*Figures 3* and *4*
t_h	Hold Time, D_0–D_5	0.60		0.60		0.60		ns	*Figure 4*
t_{pw}(L)	Pulse Width LOW $\overline{E}_a$, $\overline{E}_b$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw}(L)	Pulse Width HIGH, MR	2.00		2.00		2.00		ns	*Figure 3*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9858–6

FIGURE 1. AC Test Circuit

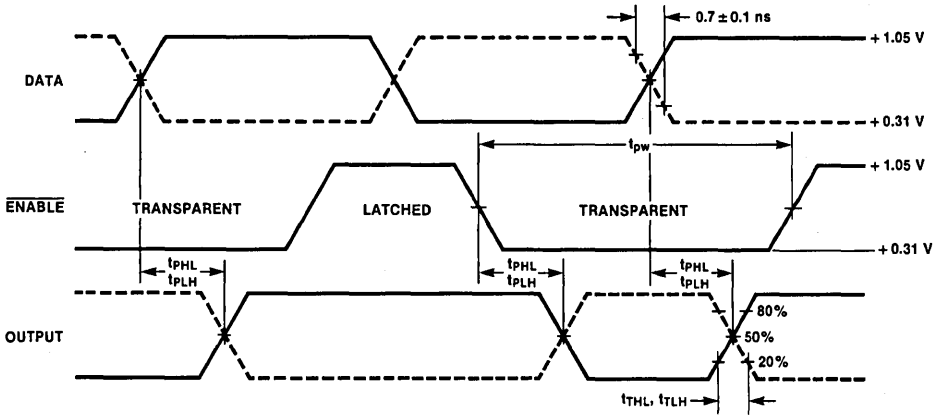


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FIGURE 2. Enable Timing

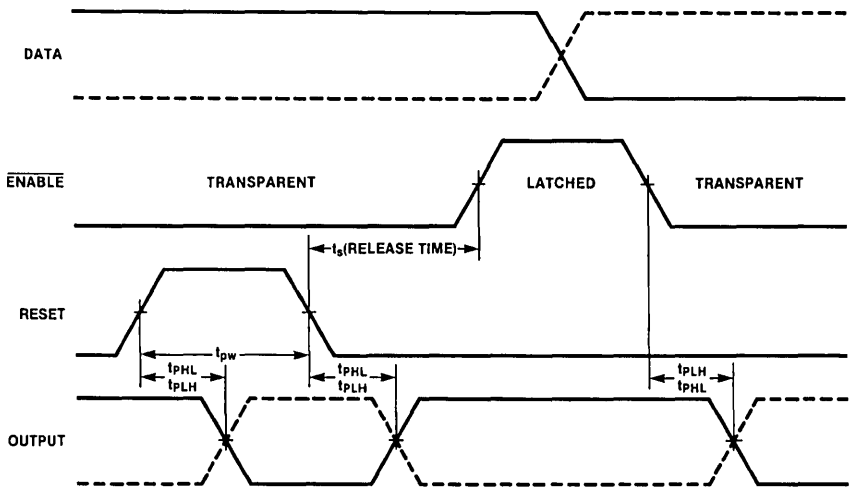

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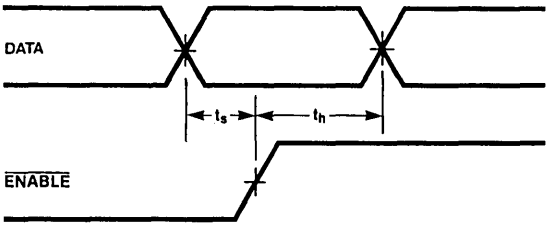
FIGURE 3. Reset Timing



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Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time

National Semiconductor

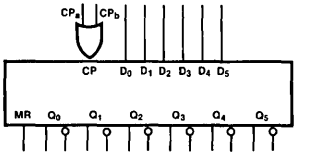
F100151
Hex D Flip-Flop

General Description

The F100151 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

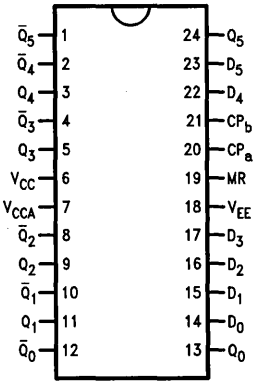
Logic Symbol



TL/F/9859-3

Connection Diagrams

24-Pin DIP



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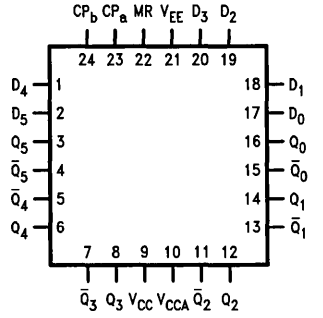
24-Pin Quad Cerpak

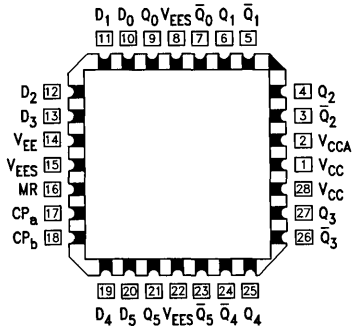


TL/F/9859-2

Top View

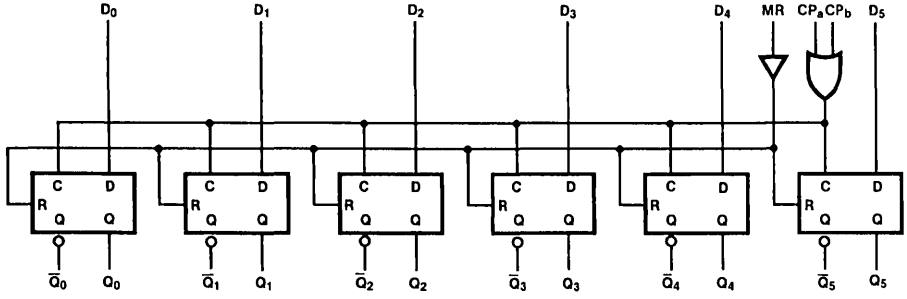
Pin Names	Description
D_0–D_5	Data Inputs
CP_a, CP_b	Common Clock Inputs
MR	Asynchronous Master Reset Input
Q_0–Q_5	Data Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Complementary Data Outputs

28-Pin PCC (Preliminary)



TL/F/9859-4

Logic Diagram



TL/F/9859–5

Truth Table (Each Flip-flop)

Synchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
L	↗	L	L	L
H	↗	L	L	H
L	L	↗	L	L
H	L	↗	L	H
X	H	↗	L	$Q_n(t)$
X	↗	H	L	$Q_n(t)$
X	L	L	L	$Q_n(t)$

Asynchronous Operation

Inputs				Outputs
D_n	CP_a	CP_b	MR	$Q_n(t+1)$
X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
t = Time before CP positive transition
t+1 = Time after CP positive transition
↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current MR D_0–D_5 CP_a, CP_b			 450 225 520	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−210	−155	−98	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

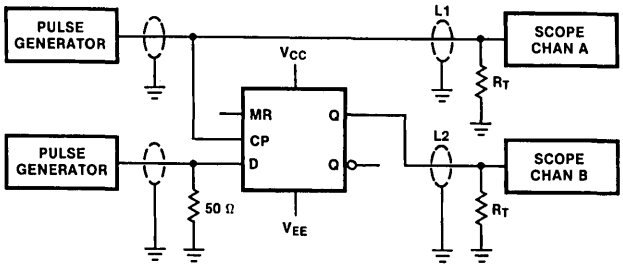
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.20	0.80	2.20	0.90	2.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.90	1.30	3.00	1.20	3.10	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	*Figures 1* and *3*
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.70 2.30		 0.70 2.30		 0.70 2.60		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0–D_5	0.70		0.70		0.70		ns	*Figure 5*
t_{pw}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

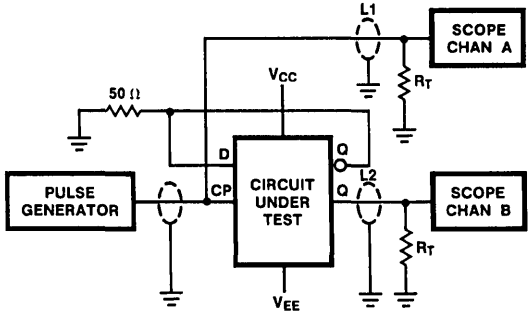
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
f_{max}	Toggle Frequency	375		375		375		MHz	*Figures 2* and *3*
t_{PLH} t_{PHL}	Propagation Delay CP_a, CP_b to Output	0.80	2.00	0.80	2.00	0.90	2.20	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay MR to Output	1.20	2.70	1.30	2.80	1.20	2.90	ns	*Figures 1* and *4*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.60	0.45	1.70	ns	*Figures 1* and *3*
t_s	Setup Time D_0–D_5 MR (Release Time)	 0.60 2.20		 0.60 2.20		 0.60 2.50		ns	*Figure 5* *Figure 4*
t_h	Hold Time D_0–D_5	0.60		0.60		0.60		ns	*Figure 5*
t_{pw}(H)	Pulse Width HIGH CP_a, CP_b, MR	2.00		2.00		2.00		ns	*Figures 3* and *4*



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/9859–6

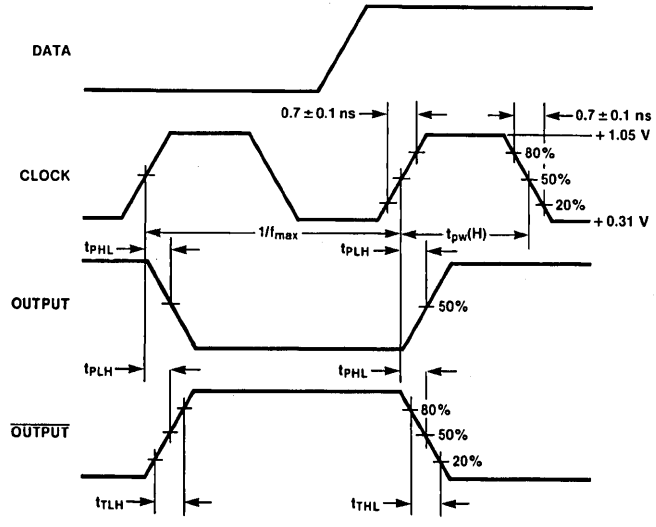
FIGURE 1. AC Test Circuit



Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Jig and stray capacitance ≤ 3 pF

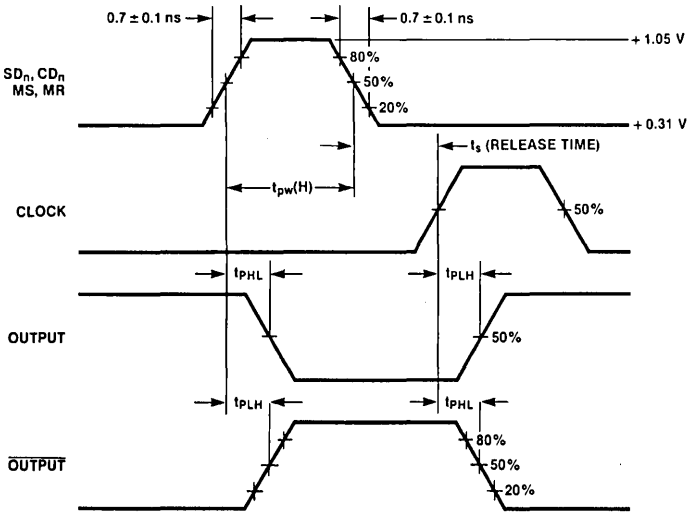
TL/F/9859–7

FIGURE 2. Toggle Frequency Test Circuit



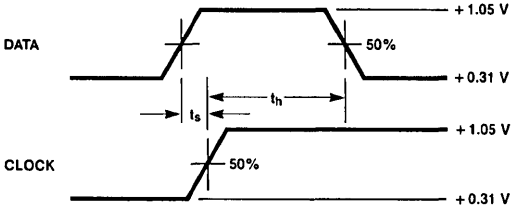
TL/F/9859–8

FIGURE 3. Propagation Delay (Clock) and Transition Times



TL/F/9859–9

FIGURE 4. Propagation Delay (Reset)



TL/F/9859–10

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time

National Semiconductor

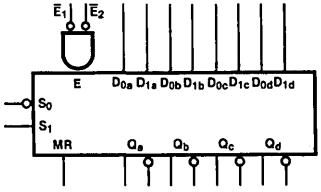
F100155
Quad Multiplexer/Latch

General Description

The F100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

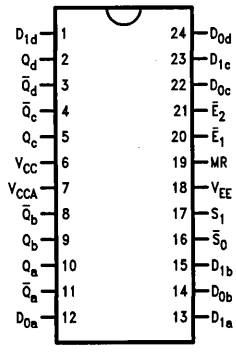
Logic Symbol



TL/F/9860–3

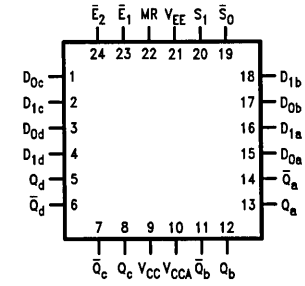
Connection Diagrams

24-Pin DIP



TL/F/9860–1

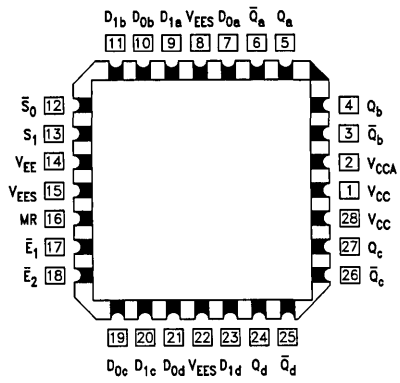
24-Pin Quad Cerpak



TL/F/9860–2

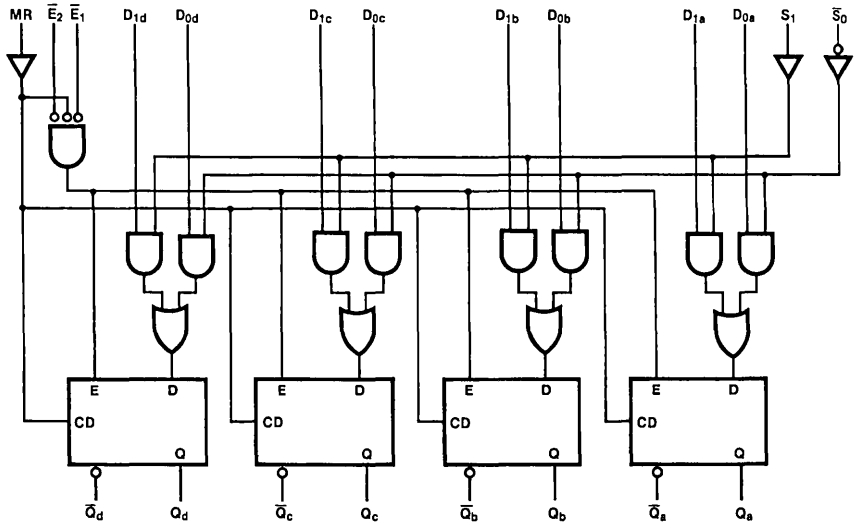
Pin Names	Description
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_2	Select Inputs
MR	Master Reset
D_{na}–D_{nd}	Data Inputs
Q_a–Q_d	Data Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Complementary Data Outputs

28-Pin PCC (Preliminary)



TL/F/9860–4

Logic Diagram



TL/F/9860–5

Operating Mode Table

Controls				Outputs
$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	Q_n
H	X	X	X	Latched*
X	H	X	X	Latched*
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

*Stores data present before $\overline{E}$ went HIGH
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Truth Table

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1x}	D_{0x}	$\overline{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched*	
L	X	H	X	X	X	X	Latched*	

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current $\overline{S}_0$, S_1 $\overline{E}_1$, $\overline{E}_2$ D_{na}–D_{nd} MR			 220 350 340 430	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−133	−95	−66	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristic

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.50	1.90	0.60	1.85	0.50	1.90	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$ S_1 to Output (Transparent Mode)	1.50	3.50	1.50	3.40	1.50	3.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.90	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	3.00	0.90	2.90	0.90	3.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	2.30	0.60	2.20	0.45	2.30	ns	*Figures 1* and *2*
t_S	Setup Time D_{na}–D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 0.90 2.40 1.50		 0.90 2.40 1.50		 0.90 2.70 1.50		ns	*Figure 4* *Figure 3*
t_H	Hold Time D_{na}–D_{nd} $\overline{S}_0$, S_1	 0.40 −0.70		 0.40 −0.70		 0.40 −0.70		ns	*Figure 4*
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics

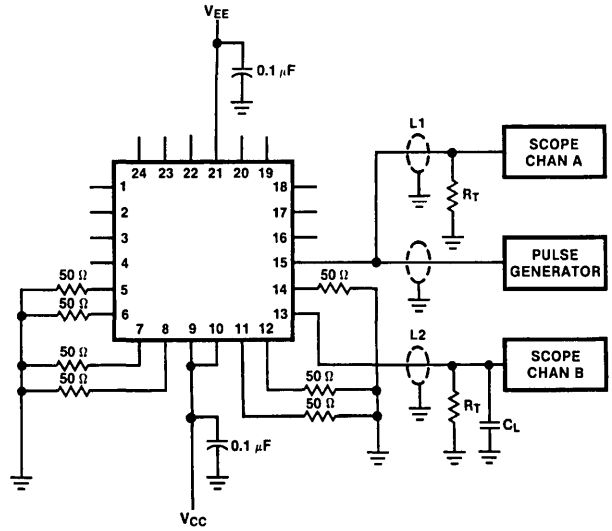
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.50	1.70	0.60	1.65	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_1$, S_1 to Output (Transparent Mode)	1.50	3.30	1.50	3.20	1.50	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.90	2.30	1.00	2.20	1.00	2.30	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND (Continued)

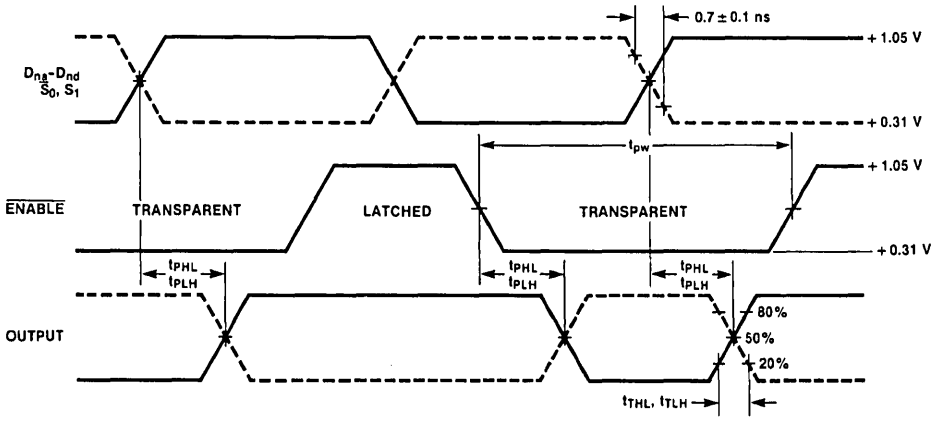
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.90	2.80	0.90	2.70	0.90	2.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.60	2.20	0.60	2.10	0.45	2.20	ns	*Figures 1* and *2*
t_S	Setup Time D_{na}–D_{nd} $\overline{S}_0$, S_1 MR (Release Time)	 0.80 2.30 1.40		 0.80 2.30 1.40		 0.80 2.60 1.40		ns	 *Figure 4* *Figure 3*
t_H	Hold Time D_{na}–D_{nd} $\overline{S}_0$, S_1	 0.30 −0.80		 0.30 −0.80		 0.30 −0.80		ns	*Figure 4*
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*



TL/F/9860–6

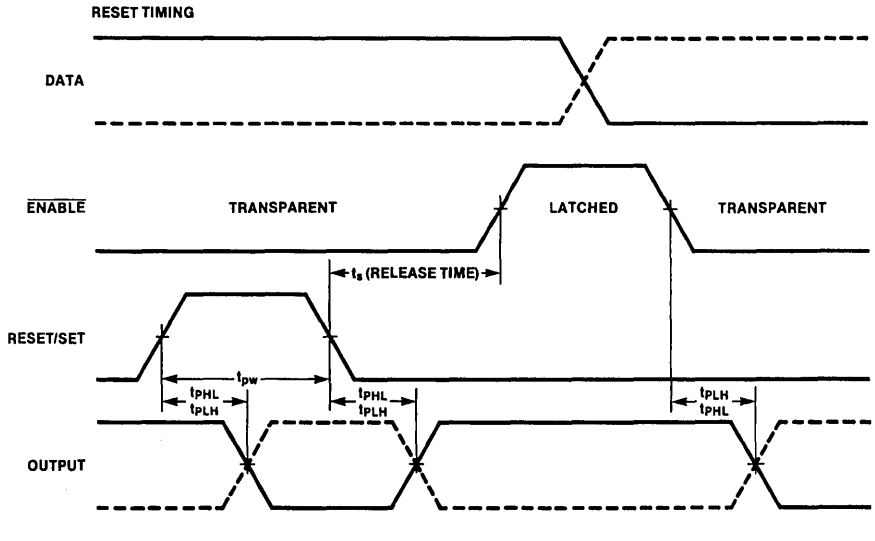
FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol



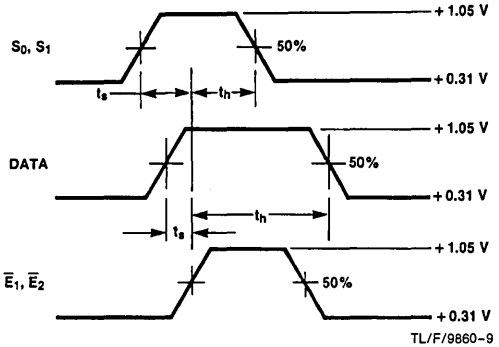
TL/F/9860–7

FIGURE 2. Enable Timing



TL/F/9860–8

FIGURE 3. Reset Timing



TL/F/9860–9

FIGURE 4. Data Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

National Semiconductor

F100156
Mask-Merge/Latch

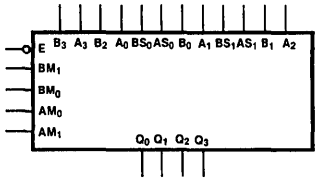
General Description

The F100156 merges two 4-bit words to form a 4-bit output word. The AM_n enable allows the merge of A into B by one, two or three places (per the AS_n value) from the left. The BM_n enable similarly allows the merge of B into A from the left (per the BS_n value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable ($\overline{E}$) input. All inputs have a 50 kΩ (typical) pull-down resistor tied to V_{EE}.

Ordering Code: See Section 6

Logic Symbol

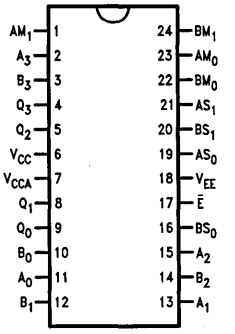


TL/F/9861-3

Note:
When $\overline{E}$ is HIGH, Q_n outputs do not change.
When $\overline{E}$ is LOW, Q_n = A or B depending on which is selected.

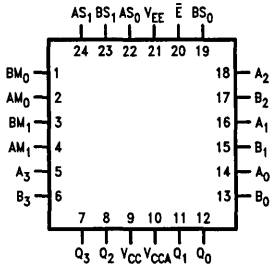
Connection Diagrams

24-Pin DIP



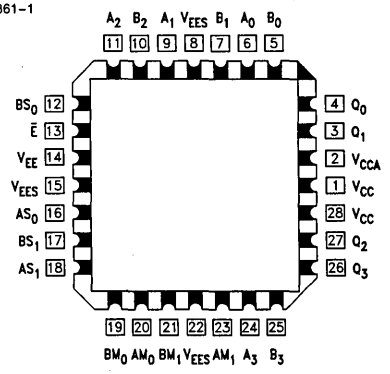
TL/F/9861-1

24-Pin Quad Cerpak



TL/F/9861-2

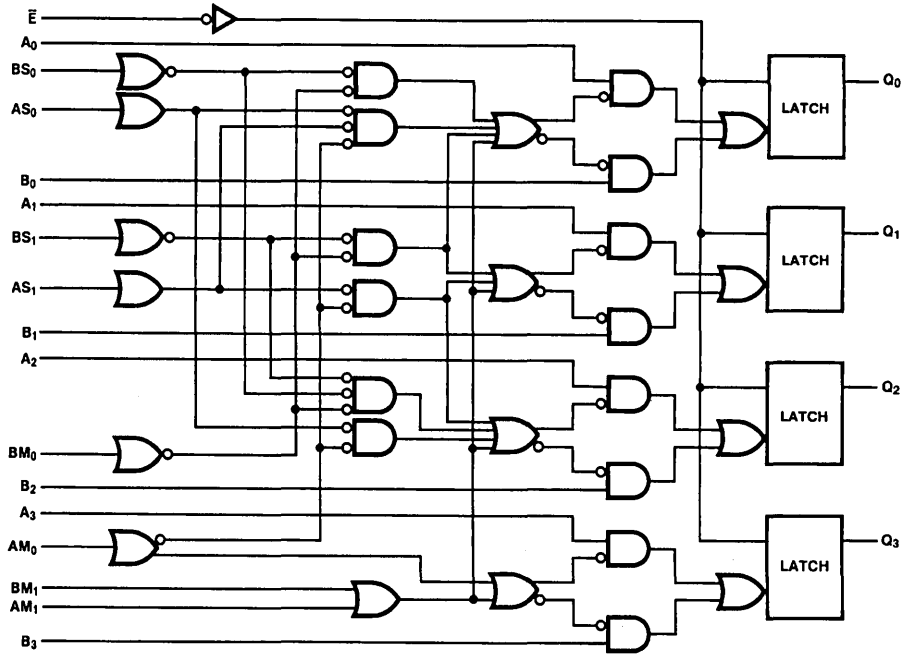
28-Pin PCC (Preliminary)



TL/F/9861-4

Pin Names	Description
$\overline{E}$	Latch Enable Input (Active LOW)
A_0–A_3	A Data Inputs
B_0–B_3	B Data Inputs
AM_0, AM_1	A Merge Enable Inputs
BM_0, BM_1	B Merge Enable Inputs
AS_0, AS_1	A Address Inputs
BS_0, BS_1	B Address Inputs
Q_0–Q_3	Data Outputs

Logic Diagram



TL/F/9861–5

Truth Table

Inputs									Outputs				Remarks
Merge Enables				Addresses									
BM_1	BM_0	AM_1	AM_0	BS_1	BS_0	AS_1	AS_0	$\overline{E}$	Q_0	Q_1	Q_2	Q_3	
X	X	H	X	X	X	X	X	L	B_0	B_1	B_2	B_3	Select B
H	X	X	X	X	X	X	X	L	B_0	B_1	B_2	B_3	
L	L	L	L	X	X	X	X	L	A_0	A_1	A_2	A_3	Select A
L	L	L	H	X	X	L	L	L	B_0	B_1	B_2	B_3	Merge A → B
L	L	L	H	X	X	L	H	L	A_0	B_1	B_2	B_3	
L	L	L	H	X	X	H	L	L	A_0	A_1	B_2	B_3	
L	L	L	H	X	X	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	L	L	L	X	X	L	A_0	A_1	A_2	A_3	Merge B → A
L	H	L	L	L	H	X	X	L	B_0	A_1	A_2	A_3	
L	H	L	L	H	L	X	X	L	B_0	B_1	A_2	A_3	
L	H	L	L	H	H	X	X	L	B_0	B_1	B_2	A_3	
L	H	L	H	L	L	L	H	L	A_0	B_1	B_2	B_3	Merge A → B
L	H	L	H	L	L	H	L	L	A_0	A_1	B_2	B_3	
L	H	L	H	L	L	H	H	L	A_0	A_1	A_2	B_3	
L	H	L	H	L	H	H	L	L	B_0	A_1	B_2	B_3	Merge A → B then Merge B → A
L	H	L	H	L	H	H	H	L	B_0	A_1	A_2	B_3	
L	H	L	H	H	L	H	H	L	B_0	B_1	A_2	B_3	
L	H	L	H	H	H	H	H	L	B_0	B_1	B_2	B_3	B Address ≥ A Address
L	H	L	H	H	H	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	H	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	H	L	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	H	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	H	L	L	L	B_0	B_1	B_2	B_3	
L	H	L	H	L	L	L	L	L	B_0	B_1	B_2	B_3	
X	X	X	X	X	X	X	X	H	Q_0	Q_1	Q_2	Q_3	Latch

Before Start	At Start	After End	At End

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current A_n, B_n, BM_n, AM_n, BS_n, AS_n, $\overline{E}$			265	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−235	−161	−107	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

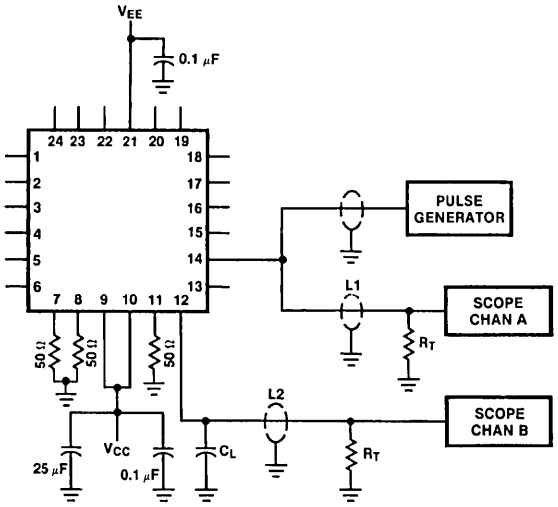
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.90	0.50	1.80	0.50	2.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.50	1.00	2.40	1.00	2.50	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.70	1.20	3.70	1.20	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.90	0.45	1.80	0.45	1.90	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.80 2.90		0.80 2.90		0.80 2.90		ns	*Figure 3*
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.10 0.80		2.10 0.80		2.10 0.80		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to Outputs (Transparent Mode)	0.45	1.70	0.50	1.60	0.50	1.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Outputs	1.00	2.30	1.00	2.20	1.00	2.30	ns	
t_{PLH} t_{PHL}	Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode)	1.20	3.50	1.20	3.50	1.20	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.70	0.45	1.80	ns	
t_S	Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n	0.70 2.80		0.70 2.80		0.70 2.80		ns	*Figure 3*
t_H	Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n	2.00 0.70		2.00 0.70		2.00 0.70		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*



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Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit

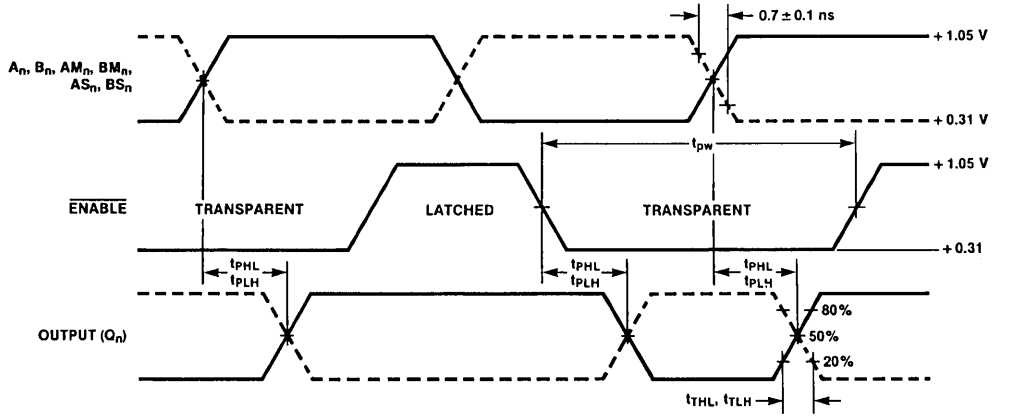

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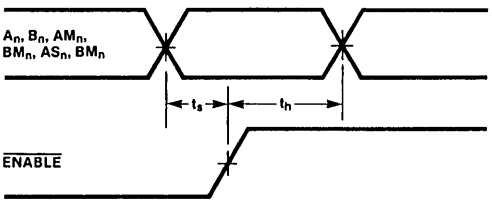
FIGURE 2. Enable Timing



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Notes:
t_s is the minimum time before the transition of the enable that information must be present at the designated input.
t_h is the minimum time after the transition of the enable that information must remain unchanged at the designated input.

FIGURE 3. Data Setup and Hold Times

National Semiconductor

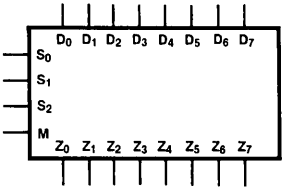
F100158
8-Bit Shift Matrix

General Description

The F100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (S_n) are internally decoded and define the number of places which an 8-bit word present at the inputs (D_n) is shifted to the left and presented at the outputs (Z_n). A Mode Control input (M) is provided which, if LOW, forces LOW all outputs to the right of the one that contains D_7. This operation is sometimes referred to as *LOW backfill*. If M is HIGH, an end-around shift is performed such that D_0 appears at the output to the right of the one that contains D_7. This operation is commonly referred to as *barrel shifting*. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol

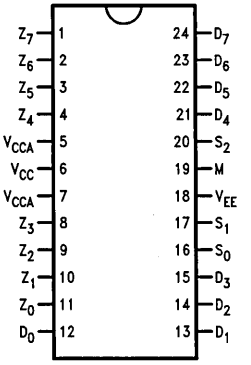


TL/F/9862–3

Pin Names	Description
D_0–D_7	Data Inputs
S_0–S_2	Select Inputs
M	Mode Control Input
Z_0–Z_7	Data Outputs

Connection Diagrams

24-Pin DIP



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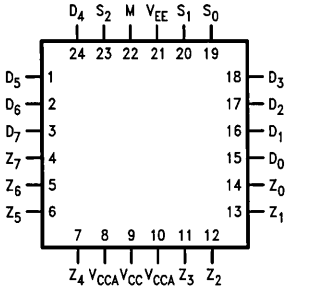
24-Pin Quad Cerpak



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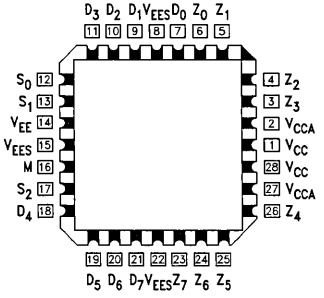
28-Pin PCC (Preliminary)



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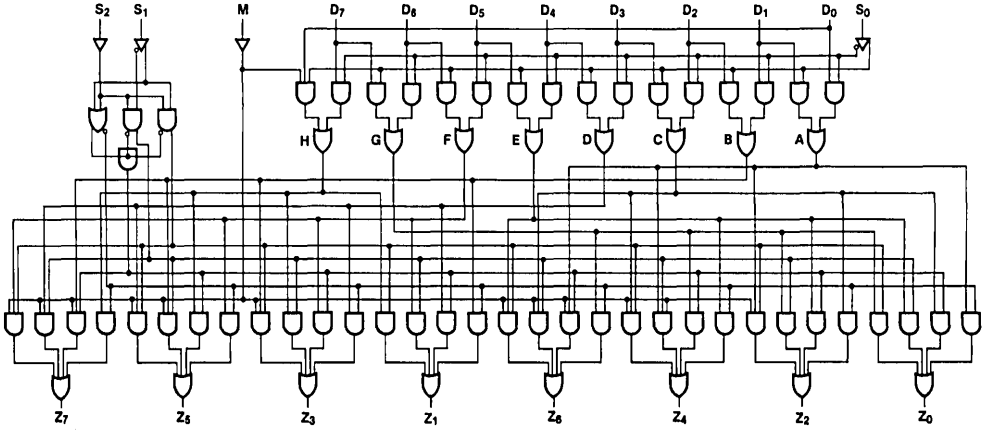
Logic Diagram



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Truth Table

Inputs				Outputs							
M	S_0	S_1	S_2	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
X	L	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
L	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	L
L	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	L	L
L	H	H	L	D_3	D_4	D_5	D_6	D_7	L	L	L
L	L	L	H	D_4	D_5	D_6	D_7	L	L	L	L
L	H	L	H	D_5	D_6	D_7	L	L	L	L	L
L	L	H	H	D_6	D_7	L	L	L	L	L	L
L	H	H	H	D_7	L	L	L	L	L	L	L
H	H	L	L	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0
H	L	H	L	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_1
H	H	H	L	D_3	D_4	D_5	D_6	D_7	D_0	D_1	D_2
H	L	L	H	D_4	D_5	D_6	D_7	D_0	D_1	D_2	D_3
H	H	L	H	D_5	D_6	D_7	D_0	D_1	D_2	D_3	D_4
H	L	H	H	D_6	D_7	D_0	D_1	D_2	D_3	D_4	D_5
H	H	H	H	D_7	D_0	D_1	D_2	D_3	D_4	D_5	D_6

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			220	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−205	−140	−95	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

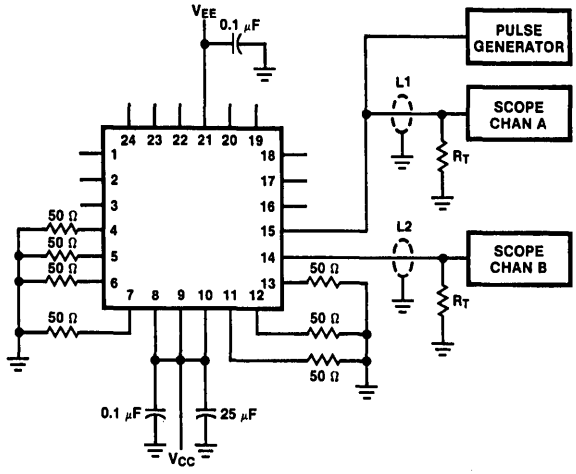
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.80	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.20	1.25	4.20	1.15	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.20	1.70	4.20	1.70	4.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.30	0.50	2.30	0.50	2.30	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to Output	1.10	2.60	1.10	2.50	1.10	2.60	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.15	4.00	1.25	4.00	1.15	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to Output	1.70	4.00	1.70	4.00	1.70	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	2.20	0.50	2.20	0.50	2.20	ns	

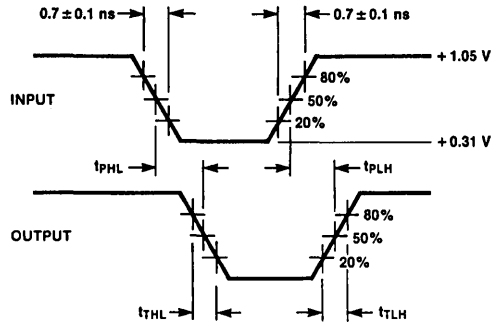


TL/F/9862–6

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V.
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.
Pin numbers shown are for flatpak; for DIP refer to logic symbol.

FIGURE 1. AC Test Circuit



TL/F/9862–7

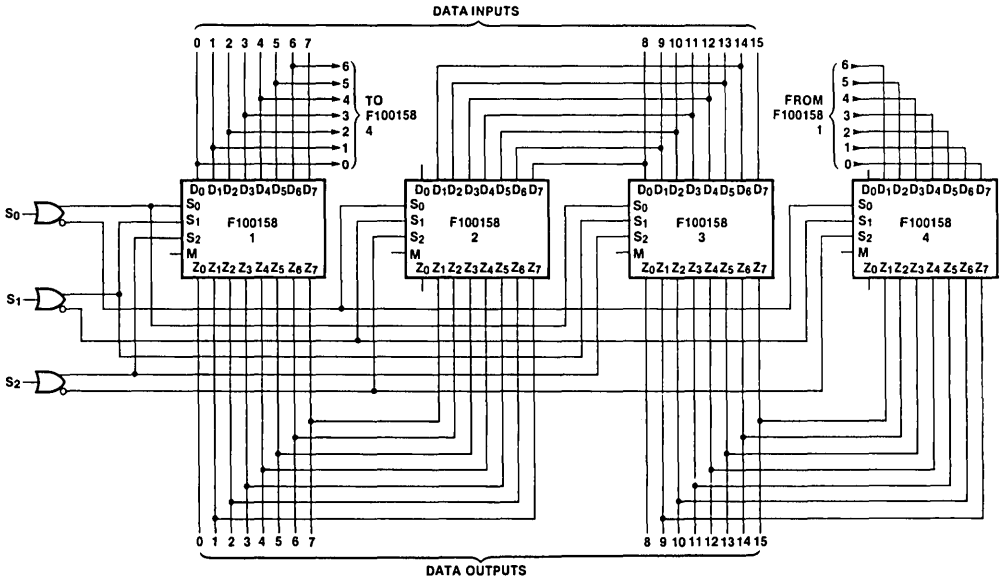
FIGURE 2. Propagation Delay and Transition Times

Applications

The following technique uses two ranks of F100158s to shift a 64-bit word from 0 to 63 places. Although two stage delays are required (one for each rank), the total shift takes only about 4 ns. This technique performs a bit shift on each 8-bit byte in the first rank and then a modulo-8 byte shift on the 64-bit word in the second rank.

Basic 16-Bit 0–7 Place Shifter

Figure 3 shows the basic 0–7 place shift technique which can be expanded to accommodate any word length. Each 8-bit byte requires a pair of F100158s operating in the LOW backfill mode. The address lines for each pair of ICs are driven out of phase by three OR gates. Inputs for the two ICs are taken from two bytes transposed in order; outputs are transposed and emitter-OR tied. One device shifts right from location 0 and the other shifts left from location 7. The bits shifted off one pair are picked up by the next pair of F100158s or—in the case of the last one in the rank—returned to the first device. The net result is a 0–7 place shift of the entire word.



TL/F/9862–8

FIGURE 3. Basic 16-Bit 0–7 Place Shifter

Applications (Continued)

Expanding to 64-Bit Word and 64-Place Shift

The basic 0–7 place shift technique can be expanded to accommodate a 64-bit word shifted from 0 to 63 places, however, two ranks of F100158s are required *(Figure 4)*. The first rank is identical to the one illustrated in *Figure 3* except it contains a total of 16 devices. The second rank consists of eight additional F100158s connected in the modulo-8 configuration shown in *Figure 5*.

The modulo-8 rank is used to simulate an 8-bit simultaneous shift since the F100158 cannot shift in 8-bit jumps. The modulo-8 configuration is achieved by wiring the first rank and the output device to the second rank as illustrated in *Figure 5*. The LSB of each output byte in the first rank is wired to one of the eight inputs of the first F100158 in the second rank. The next least significant bit of each first-rank F100158 pair, however, is connected to the inputs of the second F100158 in the second rank. The other first-ranked outputs are connected in a similar fashion to the remainder of the second-rank inputs. Ultimately, the outputs of the second rank must then be connected to reform the final usable 64-bit word so that the bits are again ordered from 0–63.

The effect is that each single-location shift in the second rank appears to be an eight place shift in the final word due to the way the inputs and outputs of the second rank are connected. The combination of the two ranks produces the 64-place shift of the entire word.

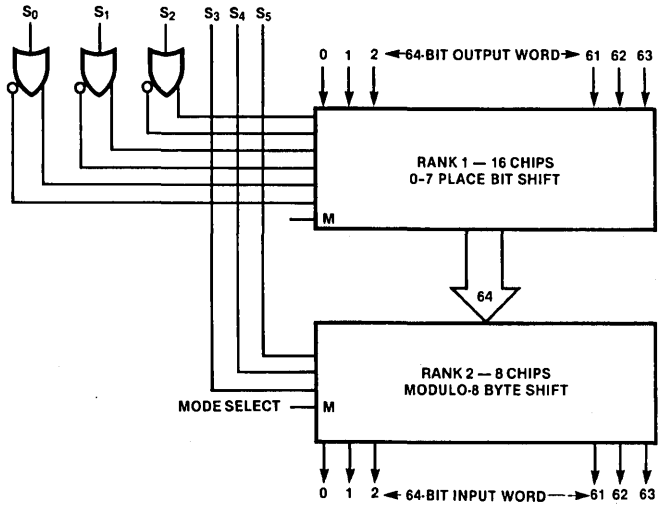


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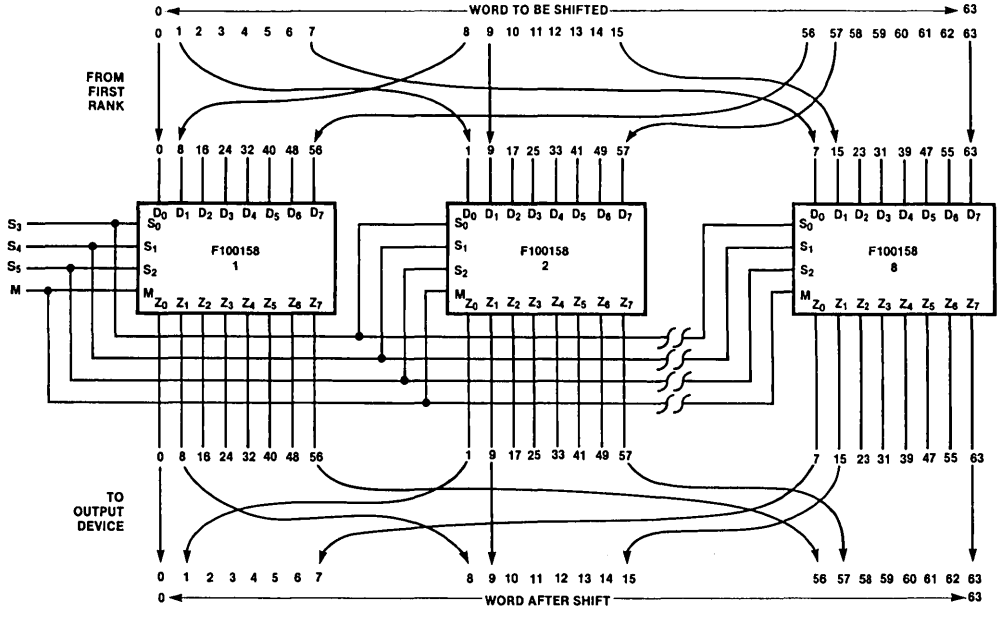
FIGURE 4. 64-Bit 0–63 Place Barrel Shifter

Applications (Continued)



TL/F/9862–10

FIGURE 5. Modulo-8 Shift

National Semiconductor

F100160
Dual Parity Checker/Generator

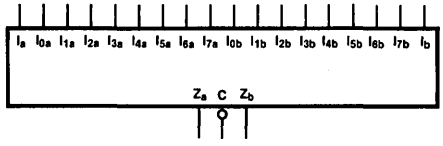
General Description

The F100160 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits.

The F100160 also has a Compare ($\overline{C}$) output which allows the circuit to compare two 8-bit words. The $\overline{C}$ output is LOW when the two words match, bit for bit. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

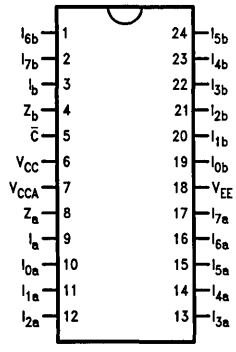
Logic Symbol



TL/F/9863-3

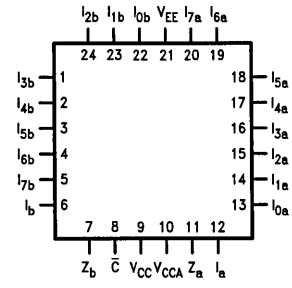
Connection Diagrams

24-Pin DIP



TL/F/9863-1

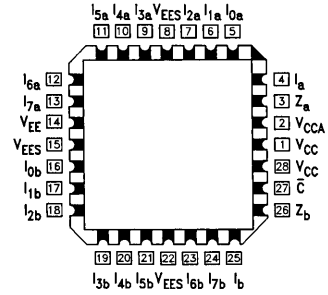
24-Pin Quad Cerpak



TL/F/9863-2

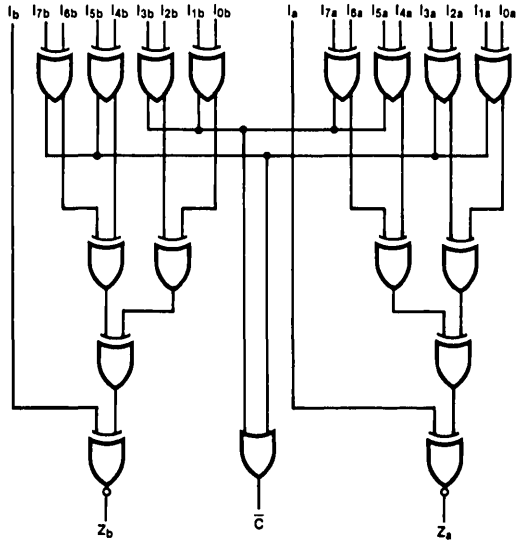
Pin Names	Description
I_a, I_b, I_{na}, I_{nb}	Data Inputs
Z_a, Z_b	Parity Odd Outputs
$\overline{C}$	Compare Output

28-Pin PCC (Preliminary)



TL/F/9863-4

Logic Diagram



TL/F/9863–5

Truth Table (Each Half)

Sum of HIGH Inputs	Output Z
Even	HIGH
Odd	LOW

Comparator Function

$$\overline{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current I_a, I_b I_{na}, I_{nb}			 340 240	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−115	−82	−57	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

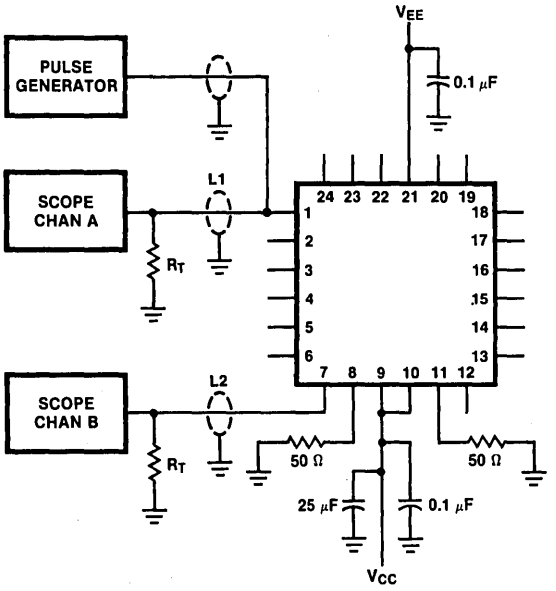
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.30	4.30	1.30	4.10	1.30	4.30	ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.20	3.30	1.20	3.10	1.20	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.60	0.50	1.50	0.50	1.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.50	0.45	1.60	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

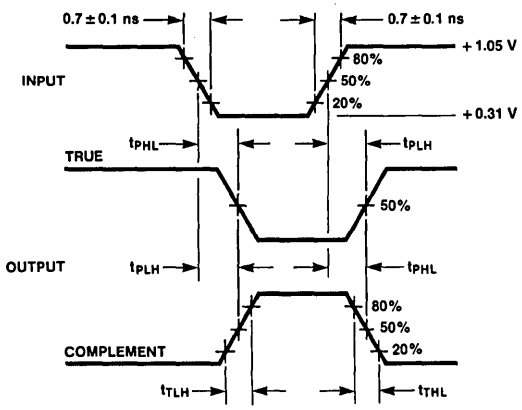
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to Z_a, Z_b	1.30	4.10	1.30	3.90	1.30	4.10	ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	Propagation Delay I_{na}, I_{nb} to $\overline{C}$	1.20	3.10	1.20	2.90	1.20	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay I_a, I_b to Z_a, Z_b	0.50	1.40	0.50	1.30	0.50	1.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	



TL/F/9863–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9863–7

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

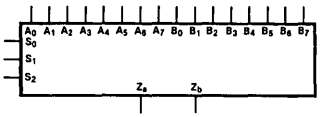
F100163
Dual 8-Input Multiplexer

General Description

The F100163 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b respectively). The same bit (0–7) will be selected for both the Z_a and Z_b output. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

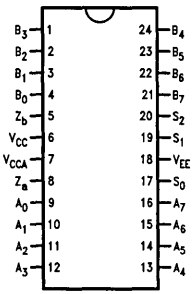
Logic Symbol



TL/F/9864–3

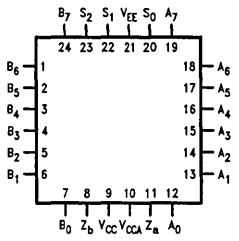
Connection Diagrams

24-Pin DIP



TL/F/9864–1

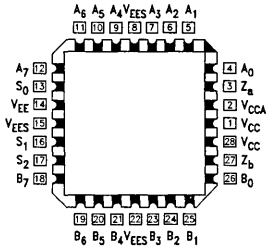
24-Pin Quad Cerpak



TL/F/9864–2

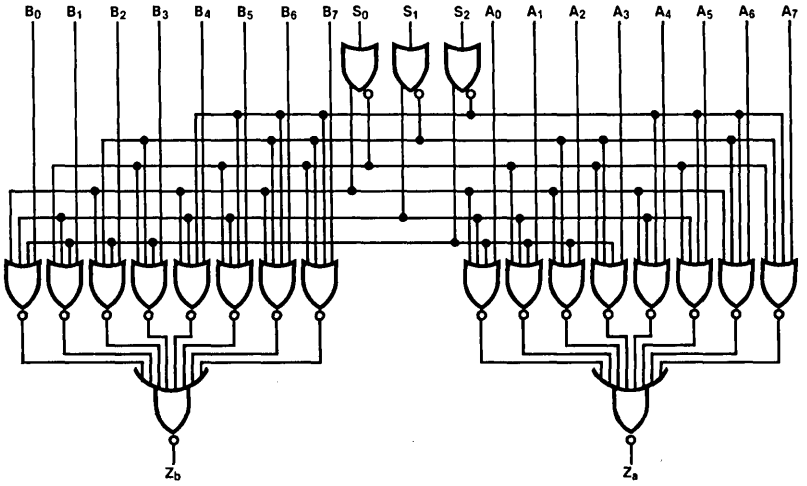
Pin Names	Description
S_0–S_2	Data Select Inputs
A_0–A_7	A Data Inputs
B_0–B_7	B Data Inputs
Z_a, Z_b	Data Outputs

28-Pin PCC (Preliminary)



TL/F/9864–4

Logic Diagram



TL/F/9864–5

Truth Table

Inputs											Outputs
Select			Data								
S_2	S_1	S_0	A_7 B_7	A_6 B_6	A_5 B_5	A_4 B_4	A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	Z_a Z_b
L L	L L	L L								L H	L H
L L	L L	H H							L H		L H
L L	H H	L L						L H			L H
L L	H H	H H					L H				L H
H H	L L	L L				L H					L H
H H	L L	H H			L H						L H
H H	H H	L L		L H							L H
H H	H H	H H	L H								L H

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current S_n A_n, B_n			 265 340	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−153	−110	−76	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

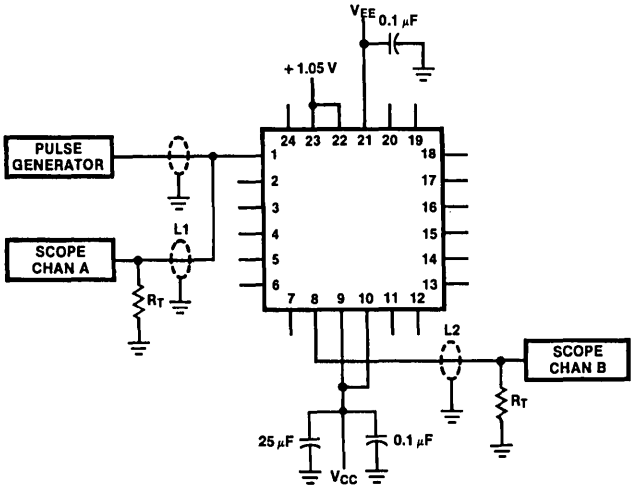
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.55	1.65	0.60	1.70	0.65	1.80	ns	
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.10	2.80	1.10	2.80	1.20	3.10	ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.85	0.55	1.80	0.50	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

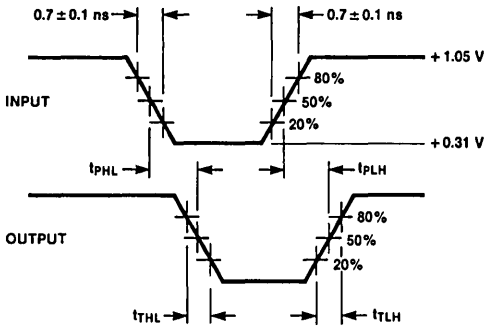
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_7, B_0–B_7 to Output	0.55	1.45	0.60	1.50	0.65	1.60	ns	
t_{PLH} t_{PHL}	Propagation Delay S_0–S_2 to Output	1.10	2.60	1.10	2.60	1.20	2.90	ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.50	1.75	0.55	1.70	0.50	1.70	ns	



TL/F/9864–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9864–7

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

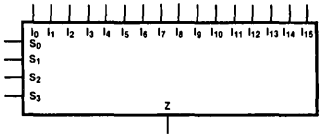
F100164
16-Input Multiplexer

General Description

The F100164 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0–S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

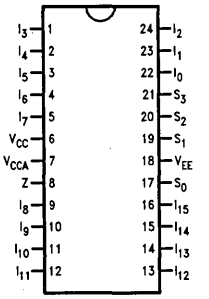
Logic Symbol



TL/F/9865–3

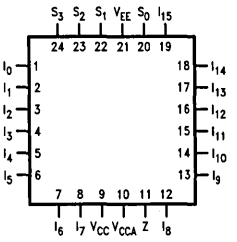
Connection Diagrams

24-Pin DIP



TL/F/9865–1

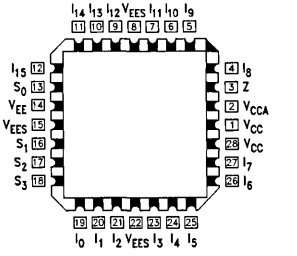
24-Pin Quad Cerpak



TL/F/9865–2

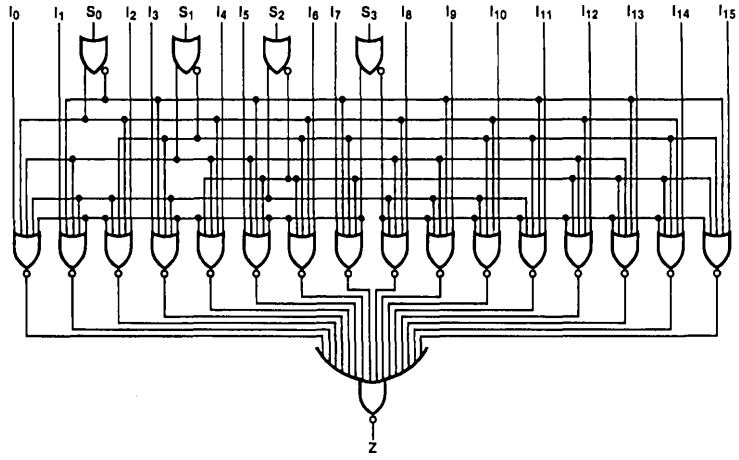
Pin Names	Description
I_0–I_{15}	Data Inputs
S_0–S_3	Select Inputs
Z	Data Output

28-Pin PCC (Preliminary)



TL/F/9865–4

Logic Diagram



TL/F/9865–5

Truth Table

Select Inputs				Output
S_0	S_1	S_2	S_3	Z
L	L	L	L	I_0
H	L	L	L	I_1
L	H	L	L	I_2
H	H	L	L	I_3
L	L	H	L	I_4
H	L	H	L	I_5
L	H	H	L	I_6
H	H	H	L	I_7
L	L	L	H	I_8
H	L	L	H	I_9
L	H	L	H	I_{10}
H	H	L	H	I_{11}
L	L	H	H	I_{12}
H	L	H	H	I_{13}
L	H	H	H	I_{14}
H	H	H	H	I_{15}

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current					
	I_n			280		
	S_0, S_1			240	μA	V_{IN} = $V_{IH\ (Max)}$
	S_2, S_3			200		
I_{EE}	Power Supply Current	−105	−70	−49	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

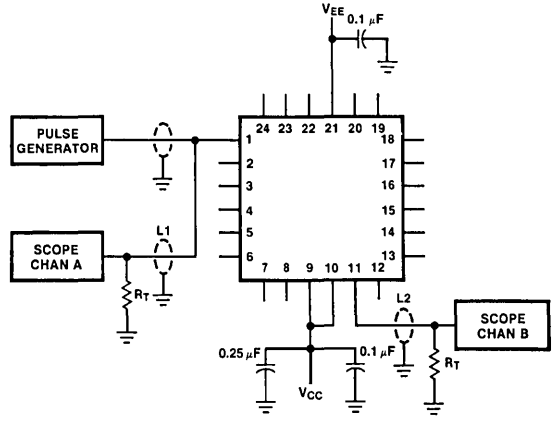
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.80	2.20	0.90	2.35	0.90	2.55	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.45	3.10	1.45	3.20	1.55	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.10	2.45	1.10	2.50	1.20	2.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

Cerpak AC Electrical Characteristics

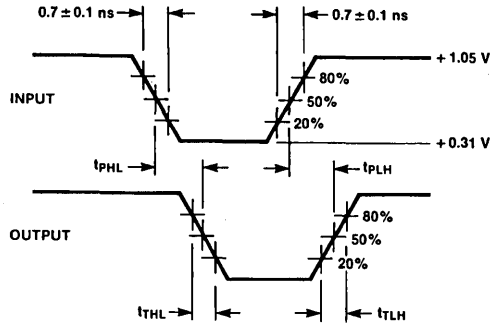
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_{15} to Output	0.80	2.00	0.90	2.15	0.90	2.35	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	1.45	2.90	1.45	3.00	1.55	3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay S_2, S_3 to Output	1.10	2.25	1.10	2.30	1.20	2.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	



TL/F/9865–6

FIGURE 1. AC Test Circuit



TL/F/9865–7

FIGURE 2. Propagation Delay and Transition Times

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

National Semiconductor

F100165
Universal Priority Encoder

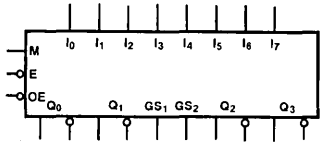
General Description

The F100165 contains eight input latches with a common Enable ($\overline{E}$) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control (M) input is LOW, and as a single 8-input encoder when M is HIGH. In the 8-input mode, Q_0, Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0, Q_1 and GS_1 operate with I_0–I_3. Q_2, Q_3 and GS_2 operate with I_4–I_7. A GS output goes LOW when its pertinent inputs are all LOW.

Inputs are latched when $\overline{E}$ goes HIGH. A HIGH signal on the Output Enable ($\overline{OE}$) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the $\overline{OE}$ input of the next lower priority group. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

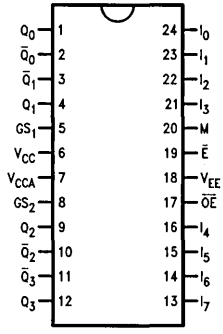
Logic Symbol



TL/F/9866-3

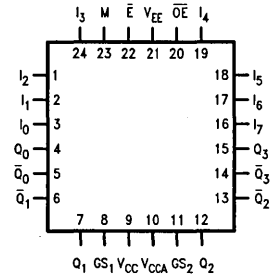
Connection Diagrams

24-Pin DIP



TL/F/9866-1

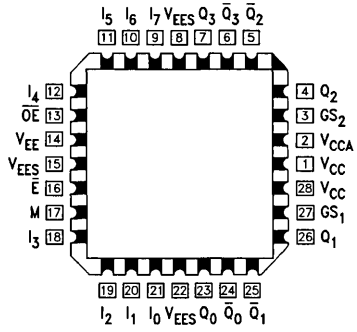
24-Pin Quad Cerpak



TL/F/9866-2

Pin Names	Description
I_0–I_7	Data Inputs
$\overline{E}$	Enable Input (Active LOW)
$\overline{OE}$	Output Enable Input (Active LOW)
M	Mode Control Input
GS_1–GS_2	Group Signal Outputs
Q_0–Q_3	Data Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complementary Data Outputs

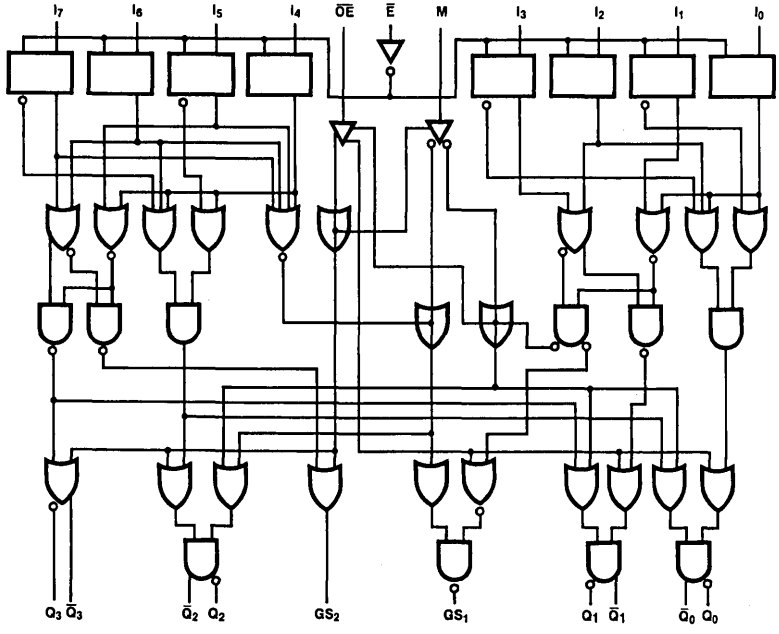
28-Pin PCC (Preliminary)



TL/F/9866-4

2

Logic Diagram



TL/F/9866-5

Truth Table

Inputs											Outputs					
$\overline{E}$	$\overline{OE}$	M	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Q_0	Q_1	Q_2	Q_3	GS_1	GS_2
L	L	L	H	X	X	X					L	L			H	
L	L	L	L	H	X	X					H	L			H	
L	L	L	L	L	H	X					L	H			H	
L	L	L	L	L	L	H					H	H			H	
L	L	L	L	L	L	L					L	L			L	
L	L	L					H	X	X	X			L	L		H
L	L	L					L	H	X	X			H	L		H
L	L	L					L	L	H	X			L	H		H
L	L	L					L	L	L	H			H	H		H
L	L	L					L	L	L	L			L	L		L
L	L	H	H	X	X	X	X	X	X	X	L	L	L	L	H	H
L	L	H	L	H	X	X	X	X	X	X	H	L	L	L	H	H
L	L	H	L	L	H	X	X	X	X	X	L	H	L	L	H	H
L	L	H	L	L	L	H	X	X	X	X	H	H	L	L	H	H
L	L	H	L	L	L	L	H	X	X	X	L	L	H	L	H	H
L	L	H	L	L	L	L	L	H	X	X	H	L	H	L	H	H
L	L	H	L	L	L	L	L	L	H	X	L	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	H	H	H	H	L	H	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H
X	H	X	X	X	X	X	X	X	X	X	L	L	L	L	H	H
H	L	L	X	X	X	X	X	X	X	X	Given by I_0–I_7 when $\overline{E}$ was LOW and M = L					
H	L	H	X	X	X	X	X	X	X	X	Given by I_0–I_7 when $\overline{E}$ was LOW and M = H					

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			230	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−200	−140	−77	mA	Inputs Open

Ceramic Dual-In-Line Package AC Characteristics

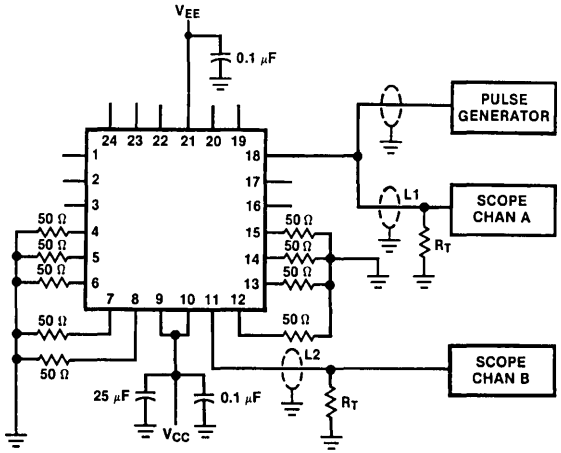
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Condition
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$ (Transparent Mode)	1.10	4.10	1.10	4.10	1.10	4.60	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to GS_1–GS_2 (Transparent Mode)	1.30	3.90	1.30	3.90	1.30	4.20	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.00	3.00	1.00	3.00	1.10	3.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1–GS_2	1.10	2.60	1.10	2.60	1.20	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	0.90	3.60	1.00	3.60	1.00	3.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.50	4.70	1.50	4.60	1.50	5.00	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.40	0.45	1.50	ns	*Figures 1*, *2* and *3*
t_S	Setup Time I_0–I_7	1.00		0.90		1.00		ns	*Figure 4*
t_H	Hold Time I_0–I_7	1.20		1.20		1.20		ns	
t_{pw}(L)	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*

Cerpak AC Electrical Characteristics

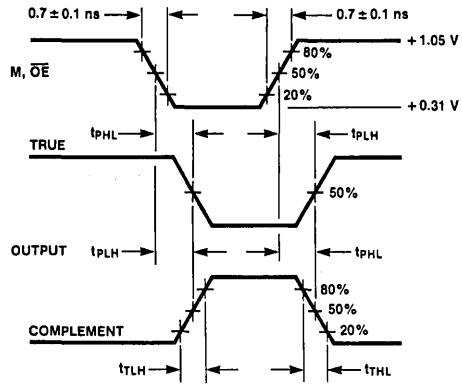
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$ (Transparent Mode)	1.10	3.90	1.10	3.90	1.10	4.40	ns	*Figures 1* and *3*
t_{PLH} t_{PHL}	Propagation Delay I_0–I_7 to GS_1–GS_2 (Transparent Mode)	1.30	3.70	1.30	3.70	1.30	4.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	1.00	2.80	1.00	2.80	1.10	3.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}$ to GS_1–GS_2	1.10	2.40	1.10	2.40	1.20	2.60	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Q_0–Q_3, $\overline{Q}_0$–$\overline{Q}_3$	0.90	3.40	1.00	3.40	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_0–Q_3, $\overline{Q}_0$–Q_3	1.50	4.50	1.50	4.40	1.50	4.80	ns	*Figures 1* and *3*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.40	0.45	1.30	0.45	1.40	ns	*Figures 1, 2* and *3*
t_S	Setup Time I_0–I_7	0.90		0.80		0.90		ns	*Figure 4*
t_H	Hold Time I_0–I_7	1.10		1.10		1.10		ns	
t_{pw}(L)	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 3*



TL/F/9866–6

FIGURE 1. AC Test Circuit



TL/F/9866–7

FIGURE 2. Propagation Delay (M, $\overline{OE}$) and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

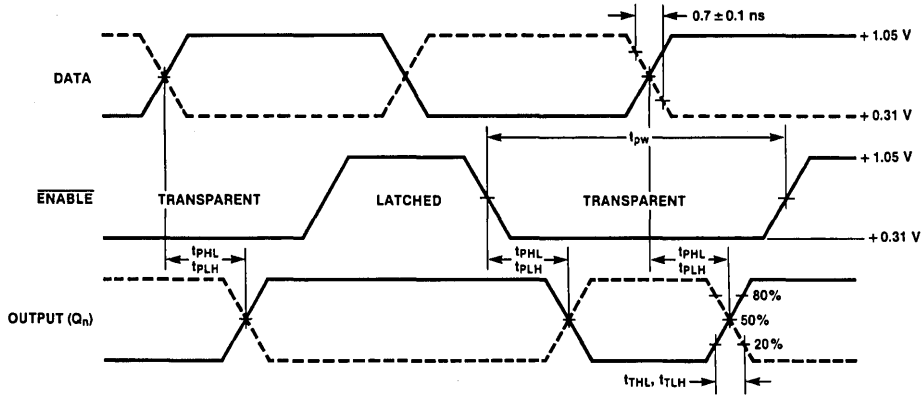
R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

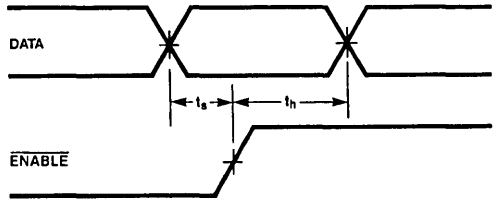
C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9866–8

FIGURE 3. Enable Timing



TL/F/9866–9

FIGURE 4. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

National Semiconductor

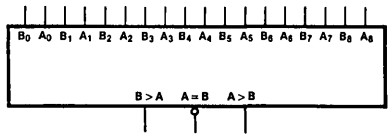
F100166
9-Bit Comparator

General Description

The F100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to, the other. Other functions can be generated by the wire-OR of the outputs. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

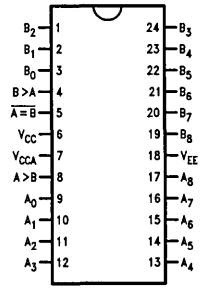
Logic Symbol



TL/F/9867–3

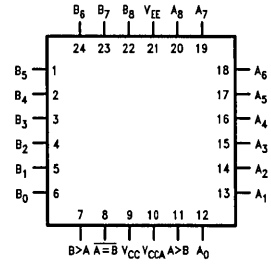
Connection Diagrams

24-Pin DIP



TL/F/9867–1

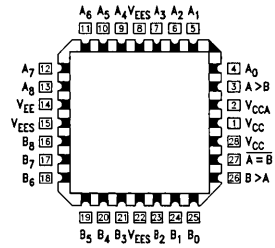
24-Pin Quad Cerpak



TL/F/9867–2

Pin Names	Description
A_0–A_8	A Data Inputs
B_0–B_8	B Data Inputs
A > B	A Greater than B Output
B > A	B Greater than A Output
$\overline{A = B}$	Complement A Equal to B Output (Active LOW)

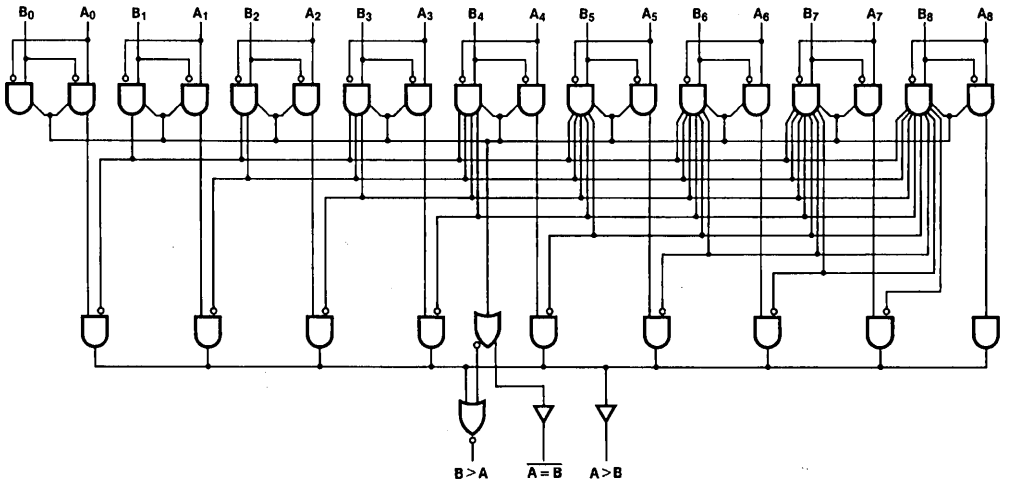
28-Pin PCC (Preliminary)



TL/F/9867–4

2

Logic Diagram



TL/F/9867–5

Truth Table

Inputs									Outputs		
A_8B_8	A_7B_7	A_6B_6	A_5B_5	A_4B_4	A_3B_3	A_2B_2	A_1B_1	A_0B_0	A > B	B > A	$\overline{A = B}$
H L									H	L	H
L H									L	H	H
$A_8 = B_8$	H L								H	L	H
$A_8 = B_8$	L H								L	H	H
$A_8 = B_8$	$A_7 = B_7$	H L							H	L	H
$A_8 = B_8$	$A_7 = B_7$	L H							L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	H L						H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	L H						L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	H L					H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	L H					L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	H L				H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	L H				L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	H L			H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	L H			L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	H L		H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	L H		L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	H L	H	L	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	L H	L	H	H
$A_8 = B_8$	$A_7 = B_7$	$A_6 = B_6$	$A_5 = B_5$	$A_4 = B_4$	$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
Blank = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			250	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−238	−170	−119	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

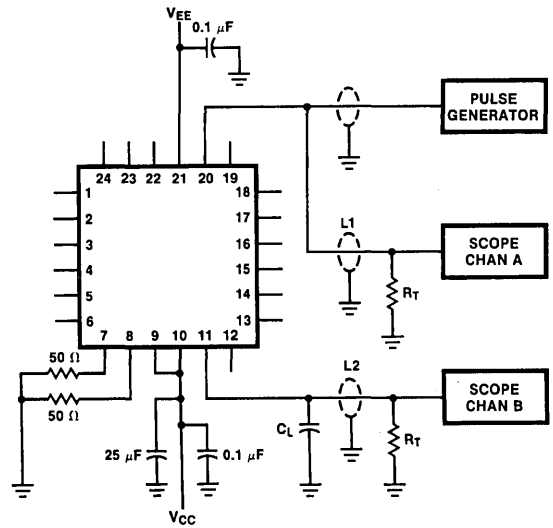
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.40	3.50	1.40	3.50	1.40	3.90	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.55	0.45	1.50	0.45	1.50	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

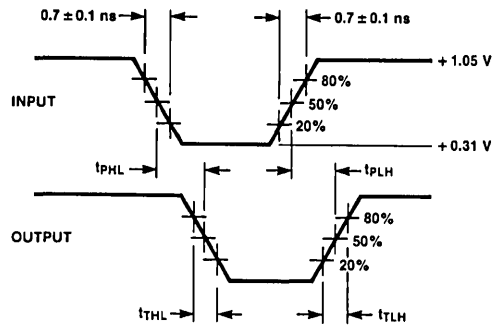
Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.40	3.30	1.40	3.30	1.40	3.70	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.45	0.45	1.40	0.45	1.40	ns	



TL/F/9867–6

FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9867–7

FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

F100170
Universal Demultiplexer/Decoder

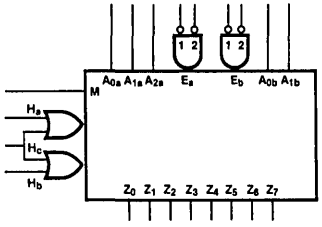
General Description

The F100170 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable ($\overline{E}$) inputs. Pin assignments for the $\overline{E}$ inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables ($\overline{E}_{1a}$ to $\overline{E}_{1b}$, $\overline{E}_{2a}$ to $\overline{E}_{2b}$). Signals applied to auxiliary inputs H_a, H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a}, A_{1a} and A_{0b}, A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a}, A_{1a}, A_{2a} with A_{0b} and A_{1b} LOW or open. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

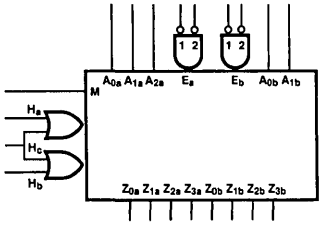
Logic Symbols

Single 1-of-8 Application



TL/F/9868–4

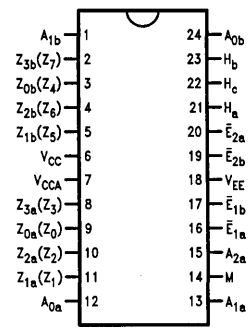
Dual 1-of-4 Application



TL/F/9868–5

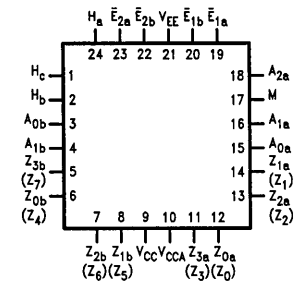
Connection Diagrams

24-Pin DIP



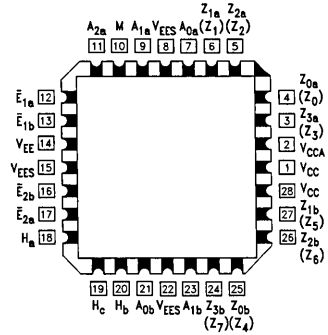
TL/F/9868–1

24-Pin Quad Cerpak



TL/F/9868–2

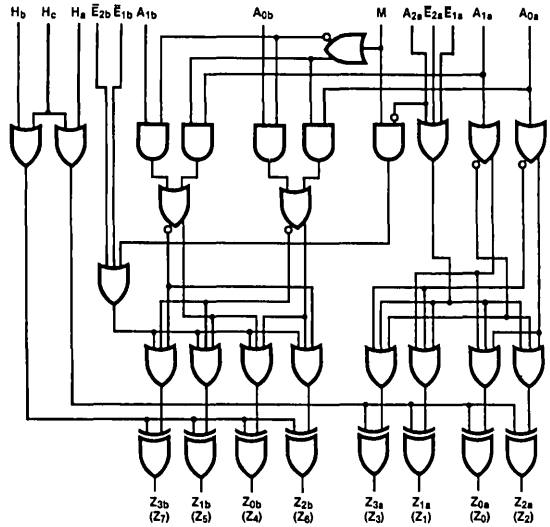
28-Pin PCC (Preliminary)



TL/F/9868–3

Pin Names	Description
A_{na}, A_{nb}	Address Inputs
$\overline{E}_{na}$, $\overline{E}_{nb}$	Enable Inputs
M	Mode Control Input
H_a	Z_0–Z_3 ($\overline{Z}_{0a}$–$\overline{Z}_{3a}$) Polarity Select Input
H_b	Z_4–Z_7 ($\overline{Z}_{0b}$–$\overline{Z}_{3b}$) Polarity Select Input
H_c	Common Polarity Select Input
Z_0–Z_7	Single 1-of-8 Data Outputs
Z_{na}, Z_{nb}	Dual 1-of-4 Data Outputs

Logic Diagram



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Note: (Z_n) for 1-of-4 applications.

Truth Tables

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)

Inputs				Active HIGH Outputs (H_a and H_b Inputs HIGH)				Active LOW Outputs (H_a and H_b Inputs LOW)			
$\overline{E}_{1a}$ $\overline{E}_{1b}$	$\overline{E}_{2a}$ $\overline{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L	H	H	H	H
X	H	X	X	L	L	L	L	H	H	H	H
L	L	L	L	H	L	L	L	L	H	H	H
L	L	L	H	L	H	L	L	H	L	H	H
L	L	H	L	L	L	H	L	H	H	L	H
L	L	H	H	L	L	L	H	H	H	H	L

Single 1-of-8 Mode (M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW)

Inputs					Active HIGH Outputs* (H_c Input HIGH)							
$\overline{E}_1$	$\overline{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
*for H_c = LOW, output states are complemented
$\overline{E}_1$ = $\overline{E}_{1a}$ and $\overline{E}_{1b}$ wired; $\overline{E}_2$ = $\overline{E}2_{2a}$ and $\overline{E}_{2b}$ wired

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current H_c, A_{0a} A_{1a}, A_{2a} All Others			310 250	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−153	−109	−76	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.90	2.30	0.90	2.20	0.90	2.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	1.00	2.80	1.00	2.70	1.00	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	1.00	3.00	1.00	2.90	1.00	3.00	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.50	3.90	1.60	3.80	1.60	3.90	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_{na}$, $\overline{E}_{nb}$ to Output	0.90	2.10	0.90	2.00	0.90	2.10	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_{na}, A_{nb} to Output	1.00	2.60	1.00	2.50	1.00	2.70	ns	
t_{PLH} t_{PHL}	Propagation Delay H_a, H_b, H_c to Output	1.00	2.80	1.00	2.70	1.00	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay M to Output	1.50	3.70	1.60	3.60	1.60	3.70	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.70	ns	

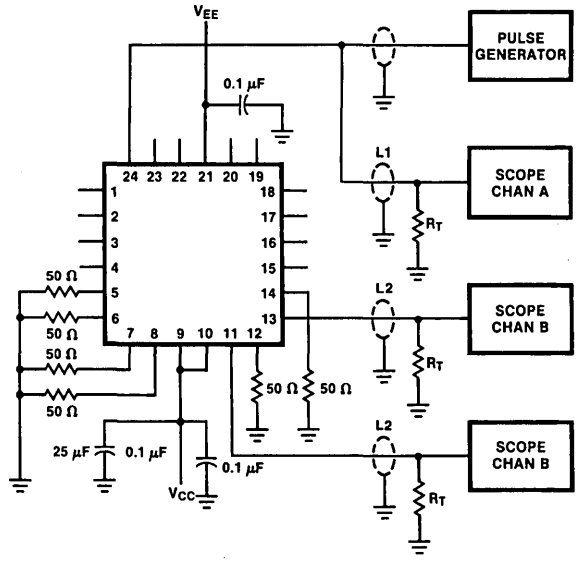

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FIGURE 1. AC Test Circuit

Notes:
V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

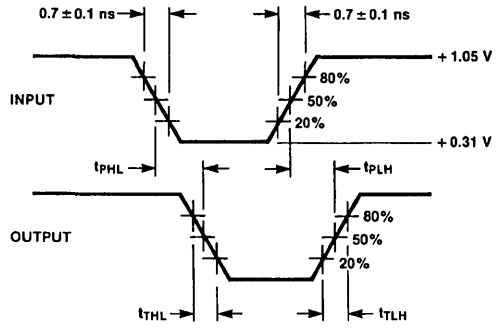

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FIGURE 2. Propagation Delay and Transition Times

National Semiconductor

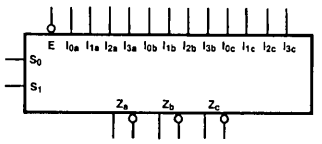
F100171
Triple 4-Input Multiplexer with Enable

General Description

The F100171 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input ($\overline{E}$) forces all true outputs LOW (see Truth Table). All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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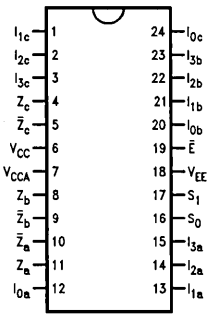
Connection Diagrams

24-Pin DIP



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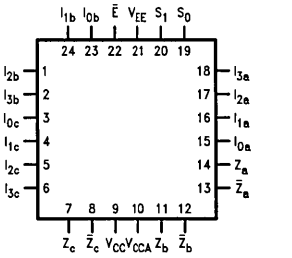
24-Pin Quad Cerpak



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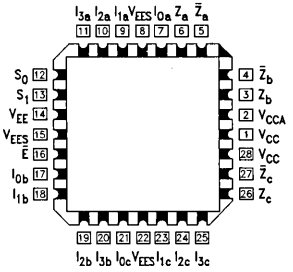
Pin Names	Description
I_{0x}–I_{3x}	Date Inputs
S_0, S_0	Select Inputs
$\overline{E}$	Enable Input (Active LOW)
Z_a–Z_c	Data Outputs
$\overline{Z}_a$–$\overline{Z}_c$	Complementary Data Outputs

28-Pin PCC (Preliminary)



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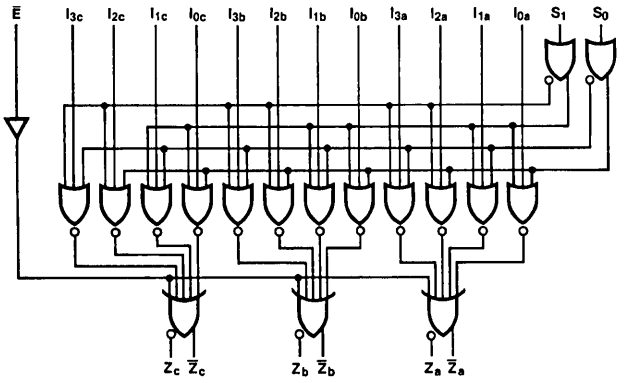
Logic Diagram



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Truth Table

Inputs			Outputs
$\overline{E}$	S_0	S_1	Z_n
L	L	L	I_{0x}
L	H	L	I_{1x}
L	L	H	I_{2x}
L	H	H	I_{3x}
H	X	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current I_{0x}–I_{3x} S_0, S_1, $\overline{E}$			340 300	μA	V_{IN} = $V_{IH\ (max)}$
I_{EE}	Power Supply Current	−114	−80	−56	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

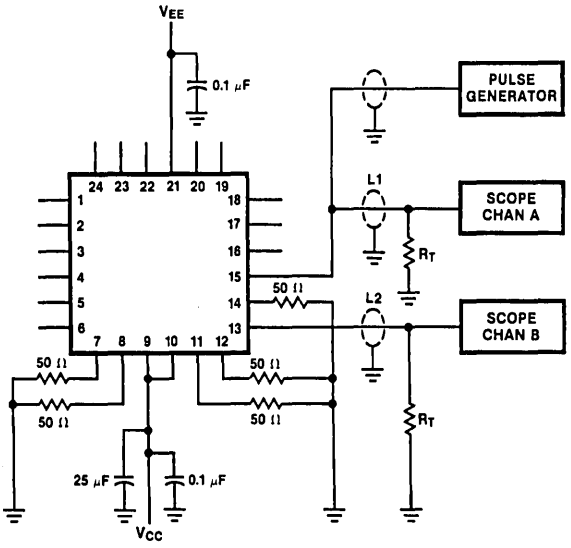
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.70	0.45	1.60	0.50	1.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.40	0.90	2.60	1.00	3.00	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.40	0.65	2.30	0.75	2.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.60	0.45	1.60	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_{0x}–I_{3x} to Output	0.45	1.50	0.45	1.40	0.50	1.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_0, S_1 to Output	0.90	2.20	0.90	2.40	1.00	2.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Output	0.65	2.20	0.65	2.10	0.75	2.20	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.50	0.45	1.50	ns	



TL/F/9869-6

FIGURE 1. AC Test Circuit

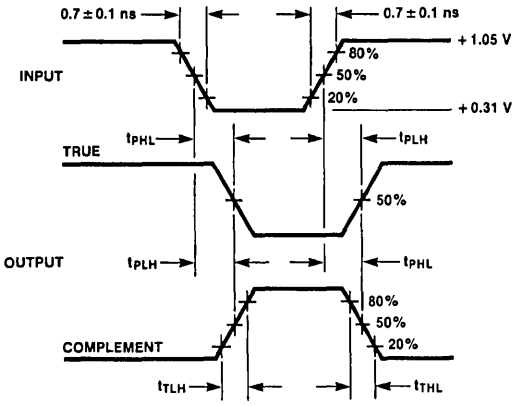


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FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

National Semiconductor

F100175
Quint Latch 100K In/10K Out

General Description

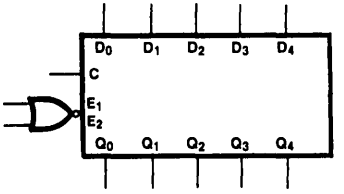
The F100175 is a 5-bit latch with temperature and voltage compensated 100K compatible inputs and voltage compensated 10K compatible outputs. Each latch has one data input and one output. All five latches share a common clear input and two enable inputs. All inputs have 50 kΩ pull-down resistors.

Features

- Outputs specified to drive a 50Ω load
- Available in 16-pin ceramic DIP
- 100K compatible inputs/10K compatible outputs

Ordering Code: See Section 6

Logic Symbol

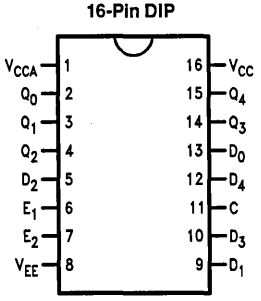


TL/F/9870-2

Pin Names	Description
D_0–D_4	100K Data Inputs
E_1, E_2	100K Enable Inputs
C	100K Common Clear Input
Q_0–Q_4	10K Data Outputs

Connection Diagram

16-Pin DIP



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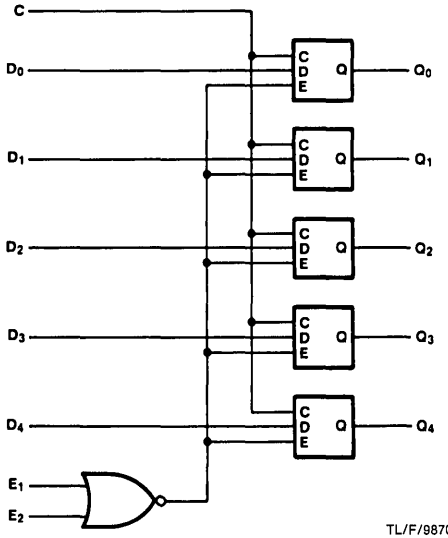
Logic Diagram



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Truth Table

Inputs				Output
D_n	E_1	E_2	C	Q_n
H	L	L	X	H
L	L	L	X	L
X	H	X	L	Q_{n-1}
X	X	H	L	Q_{n-1}
X	H	X	H	L
X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias (T_A)	−55°C to +125°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage	−8V
Input Voltage (DC)	−5.2V to +0V
Output Current (DC Output HIGH)	−55 mA
Operating Range	−5.72V to −4.68V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.72V	−5.2V	−4.68V
Ambient Temperature (T_A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = V_{CCA} = GND, T_A = 0°C to +75°C (Notes 1, 2)

Symbol	Parameter	Temp	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	T_A = 0°C	−1000		−840	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
		T_A = +25°C	−960		−810	mV		
		T_A = +75°C	−900		−720	mV		
V_{OL}	Output LOW Voltage	T_A = 0°C	−1870		−1665	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	
		T_A = +25°C	−1850		−1650	mV		
		T_A = +75°C	−1830		−1625	mV		
V_{OHC}	Output HIGH Voltage	T_A = 0°C	−1020			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	
		T_A = +25°C	−980			mV		
		T_A = +75°C	−920			mV		
V_{OLC}	Output LOW Voltage	T_A = 0°C			−1645	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	
		T_A = +25°C			−1630	mV		
		T_A = +75°C			−1605	mV		
V_{IH}	Input HIGH Voltage		−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage		−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input HIGH Current				290		V_{IN} = $V_{IH\ (Max)}$	
I_{IL}	Input LOW Current		0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{EE}	V_{EE} Supply Current		−125	−90	−50	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4*.

DC Electrical Characteristics

V_{EE} = −4.68V, V_{CC} = V_{CCA} = GND, T_A = 0°C to +75°C (Notes 1, 2)

Symbol	Parameter	Temp	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	T_A = 0°C	−1000		−840	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	
		T_A = +25°C	−960		−810	mV		
		T_A = +75°C	−900		−720	mV		
V_{OL}	Output LOW Voltage	T_A = 0°C	−1870		−1665	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	
		T_A = +25°C	−1850		−1650	mV		
		T_A = +75°C	−1830		−1625	mV		
V_{OHC}	Output HIGH Voltage	T_A = 0°C	−1020			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
		T_A = +25°C	−980			mV		
		T_A = +75°C	−920			mV		
V_{OLC}	Output LOW Voltage	T_A = 0°C			−1645	mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	
		T_A = +25°C			−1630	mV		
		T_A = +75°C			−1605	mV		
V_{IH}	Input HIGH Voltage		−1150		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage		−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input HIGH Current				290		V_{IN} = $V_{IH\ (Max)}$	
I_{IL}	Input LOW Current		0.50			μA	V_{IN} = $V_{IL\ (Min)}$	
I_{EE}	V_{EE} Supply Current		−125	−90	−50	mA	Inputs Open	

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4*.

DC Electrical Characteristics

$V_{EE} = -5.72V$, $V_{CC} = V_{CCA} = GND$, $T_A = 0°C$ to $+75°C$ (Notes 1, 2)

Symbol	Parameter	Temp	Min	Typ	Max	Units	Conditions	
V_{OH}	Output HIGH Voltage	$T_A = 0°C$	−1000		−840	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	
		$T_A = +25°C$	−960		−810	mV		
		$T_A = +75°C$	−900		−720	mV		
V_{OL}	Output LOW Voltage	$T_A = 0°C$	−1870		−1665	mV	$V_{IN} = V_{IH}$ (Max) or V_{IL} (Min)	
		$T_A = +25°C$	−1850		−1650	mV		
		$T_A = +75°C$	−1830		−1625	mV		
V_{OHC}	Output HIGH Voltage	$T_A = 0°C$	−1020			mV	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V
		$T_A = +25°C$	−980			mV		
		$T_A = +75°C$	−920			mV		
V_{OLC}	Output LOW Voltage	$T_A = 0°C$			−1645	mV	$V_{IN} = V_{IH}$ (Min) or V_{IL} (Max)	
		$T_A = +25°C$			−1630	mV		
		$T_A = +75°C$			−1605	mV		
V_{IH}	Input HIGH Voltage		−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage		−1810		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input HIGH Current				290		$V_{IN} = V_{IH}$ (Max)	
I_{IL}	Input LOW Current		0.50			μA	$V_{IN} = V_{IL}$ (Min)	
I_{EE}	V_{EE} Supply Current		−125	−90	−50	mA	Inputs Open	

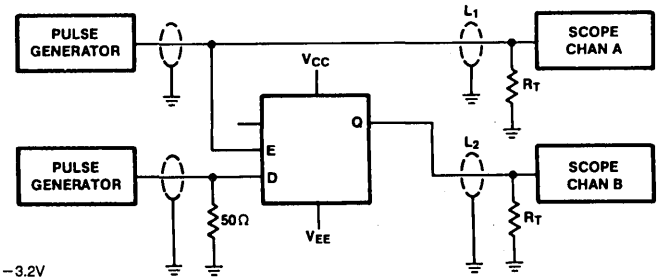
Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4.*

AC Electrical Characteristics

$V_{EE} = -5.2V \pm 10\%$, $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_A = 0°C$		$T_A = +25°C$		$T_A = +75°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PDLH} t_{PDHL}	Propagation Delay Data to Output	1.10	2.60	1.10	2.75	1.10	3.00	ns	*Figures 1 & 2*
t_{PDLH} t_{PDHL}	Propagation Delay Enable to Output	1.20	3.40	1.20	3.50	1.20	3.75	ns	*Figures 1 & 3*
t_{PDHL}	Propagation Delay Clear to Output	1.30	3.20	1.30	3.20	1.30	3.20	ns	*Figures 1, 3 & 4*
t_S	Setup Time D_0–D_4		2.50		2.50		2.50	ns	*Figures 1 & 5*
t_H	Hold Time D_0–D_4		0.50		0.50		0.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	1.10	3.25	1.20	3.25	1.20	3.50	ns	*Figures 1, 2, 3 & 4*



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Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −3.2V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μf from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

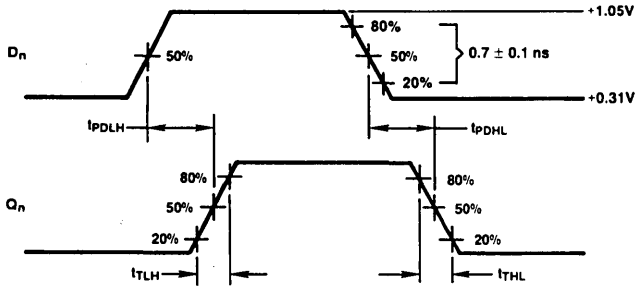

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FIGURE 2. Data Propagation Delay @ T_A = +25°C

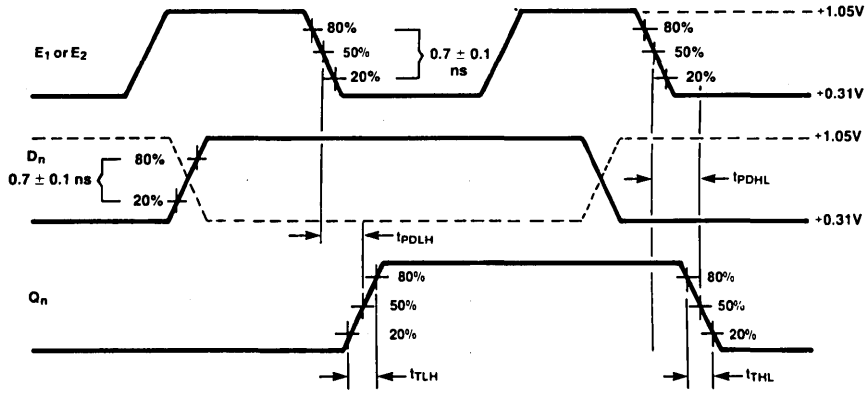

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FIGURE 3. Enable Propagation Delay @ T_A = +25°C

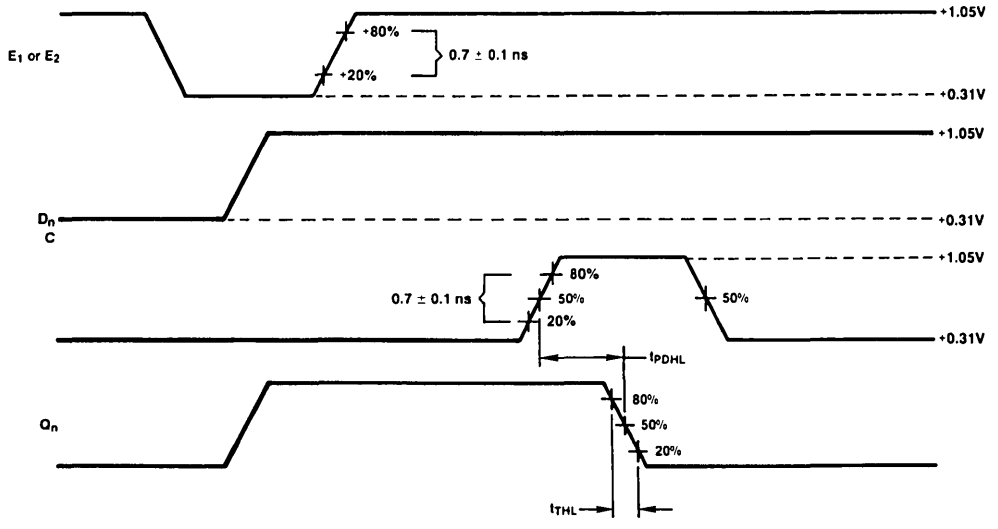

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FIGURE 4. Clear Propagation Delay @ $T_A = +25°C$

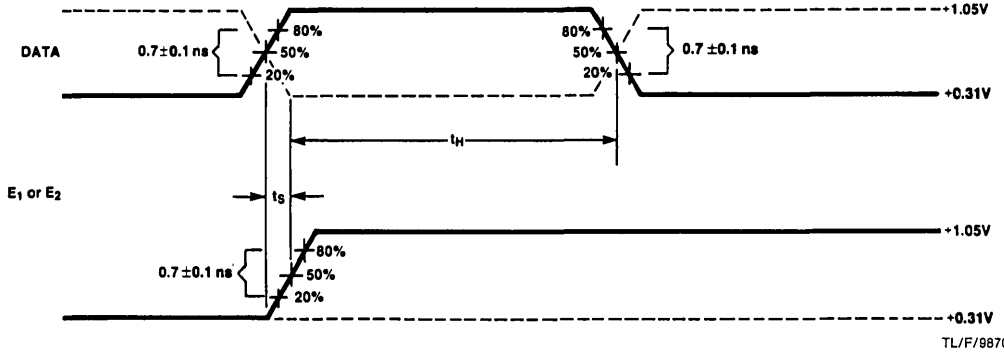

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FIGURE 5. Data Setup and Hold Time

National Semiconductor

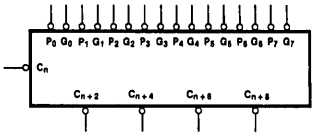
F100179
Carry Lookahead Generator

General Description

The F100179 is a high-speed Carry Lookahead Generator intended for use with the F100180 6-bit fast Adder and the F100181 4-bit ALU. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 6

Logic Symbol



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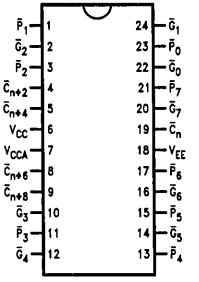
Connection Diagrams

24-Pin DIP



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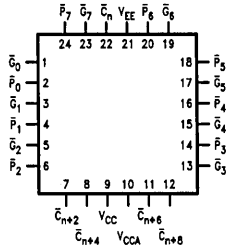
24-Pin Quad Cerpak



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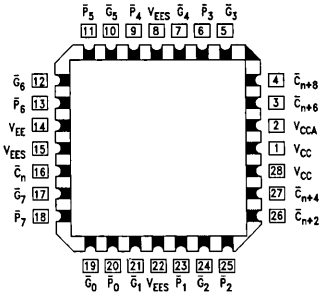
Pin Names	Description
$\overline{C}_n$	Carry Input (Active LOW)
$\overline{P}_0$–$\overline{P}_7$	Carry Propogate Inputs (Active LOW)
$\overline{G}_0$–$\overline{G}_7$	Carry Generate Inputs (Active LOW)
$\overline{C}_n + 2$, $\overline{C}_n + 4$ $\overline{C}_n + 6$, $\overline{C}_n + 8$	Carry Outputs

28-Pin PCC (Preliminary)



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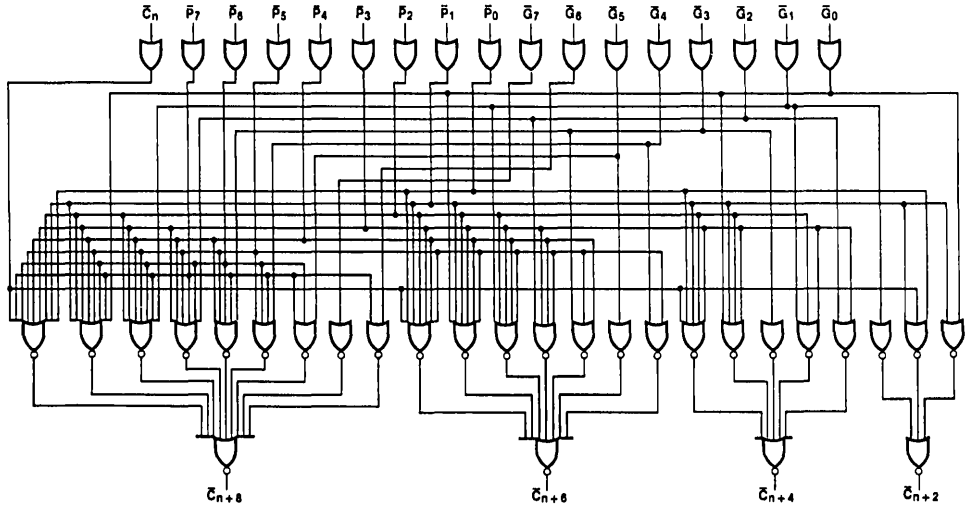
Logic Diagram



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Truth Tables

$\overline{C}_{n+2}$ Output

Inputs					Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{C}_{n+2}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

$\overline{C}_{n+2} = \overline{G}_1 \bullet (\overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

$\overline{C}_{n+4}$ Output

Inputs									Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{C}_{n+4}$
X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	L	X	X	L	L
X	X	X	L	X	X	L	X	L	L
X	L	X	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	L
All other combinations									H

$\overline{C}_{n+4} = \overline{G}_3 \bullet (\overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$
$\bullet (\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$

Truth Tables (Continued)

$\overline{C}_{n+6}$ Output

Inputs												Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{G}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{C}_{n+6}$
X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations													H

$$\overline{C}_{n+6} = \overline{G}_5 \bullet (\overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

$\overline{C}_{n+8}$ Output

Inputs																Output
$\overline{C}_n$	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$\overline{G}_4$	$\overline{P}_4$	$\overline{G}_5$	$\overline{P}_5$	$\overline{G}_6$	$\overline{P}_6$	$\overline{G}_7$	$\overline{P}_7$	$\overline{C}_{n+8}$
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	L
X	X	X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	L
X	X	X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	L
X	X	X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	L
X	X	X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	L
X	X	X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	L
X	L	X	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	X	L	L
All other combinations																	H

$$\overline{C}_{n+8} = \overline{G}_7 \bullet (\overline{P}_7 + \overline{G}_6) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{G}_5) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{G}_4) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{G}_3) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{G}_2) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{G}_1) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0) \bullet (\overline{P}_7 + \overline{P}_6 + \overline{P}_5 + \overline{P}_4 + \overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{P}_0 + \overline{C}_n)$$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current $\overline{C}_N$, $\overline{G}_0$–$\overline{G}_7$ $\overline{P}_0$–$\overline{P}_7$			 250 340	 μA	 V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−220	−150	−100	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

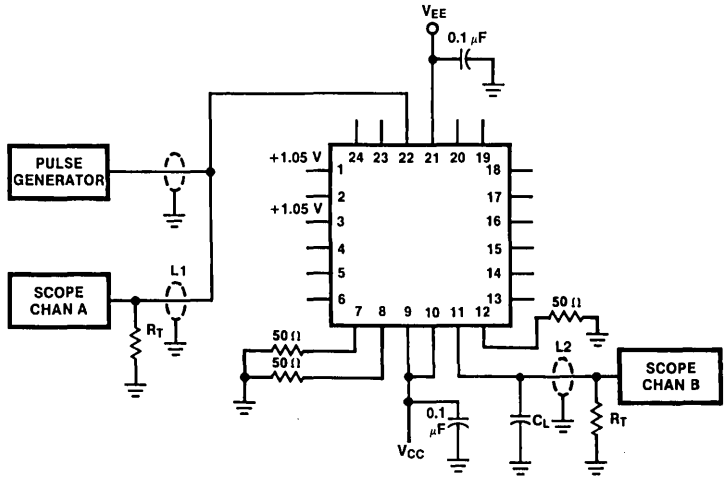
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.90	1.10	2.90	1.10	3.00	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.80	0.45	1.80	0.45	1.80	ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$, $\overline{G}_0$–$\overline{G}_7$, $\overline{P}_0$–$\overline{P}_7$ to $\overline{C}_{n+x}$	1.10	2.70	1.10	2.70	1.10	2.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	

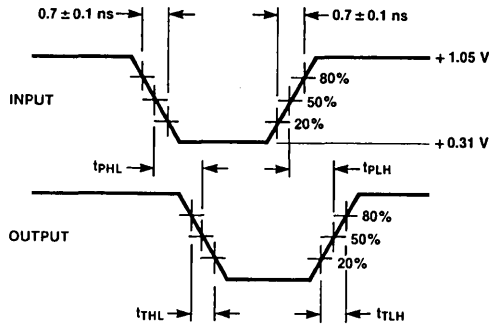


TL/F/9871–6

FIGURE 1. AC Test Circuit

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

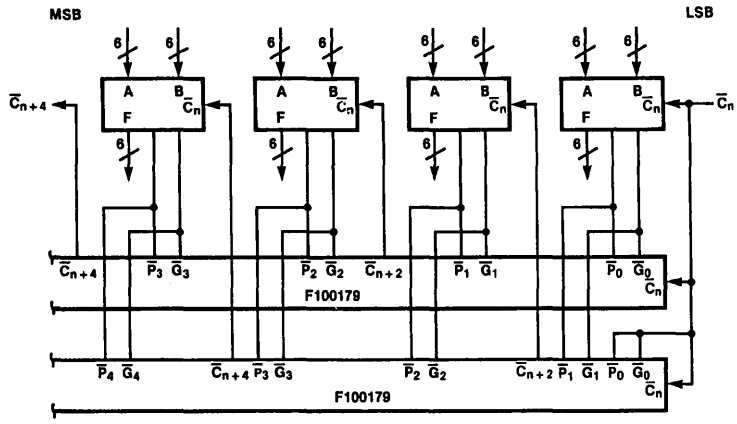


TL/F/9871–6

FIGURE 2. Propagation Delay and Transition Times

Applications

Fast Adder and Carry Lookahead



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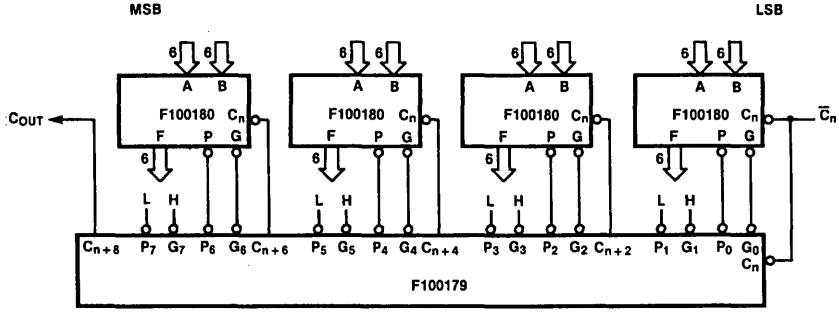
24-Bit Adder Using One Carry Lookahead



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National Semiconductor

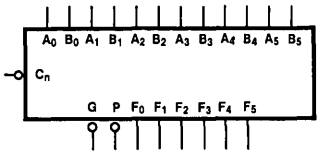
F100180
High-Speed 6-Bit Adder

General Description

The F100180 is a high-speed 6-bit adder capable of performing a full 6-bit addition of two operands. Inputs for the adder are active-LOW Carry, Operand A, and Operand B; outputs are Function, active-LOW Carry Generate, and active-LOW Carry Propagate. When used with the F100179 Full Carry Lookahead as a second order lookahead block, the F100180 provides high-speed addition of very long words. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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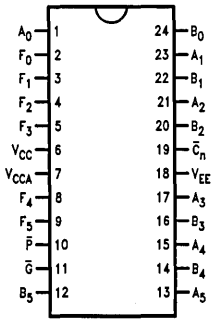
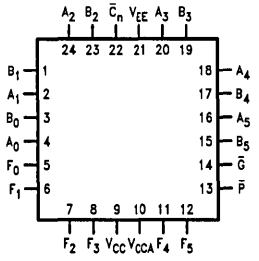
Connection Diagrams

24-Pin DIP



TL/F/9872-1

24-Pin Quad Cerpak



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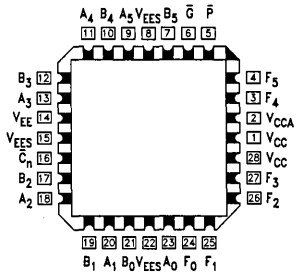
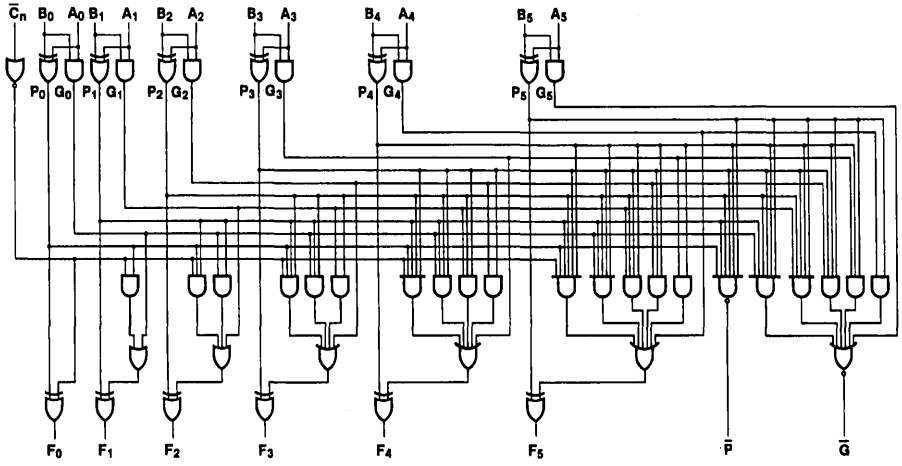
Pin Names	Description
A_0–A_5	Operand A Inputs
B_0–B_5	Operand B Inputs
$\overline{C}_n$	Carry Input (Active LOW)
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
F_0–F_5	Function Outputs

28-Pin PCC (Preliminary)



TL/F/9872-4

Logic Diagram



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Logic Equations

$P_i = A_i \oplus B_i$

$G_i = A_i B_i$

$i = 0, 1, 2, 3, 4, 5$

$F_0 = P_0 \oplus C_n$

$F_1 = P_1 \oplus (G_0 + P_0 C_n)$

$F_2 = P_2 \oplus (G_1 + P_1G_0 + P_1P_0C_n)$

$F_3 = P_3 \oplus (G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n)$

$F_4 = P_4 \oplus (G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n)$

$F_5 = P_5 \oplus (G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1G_0 + P_4P_3P_2P_1P_0C_n)$

$\overline{P} = \overline{P_0P_1P_2P_3P_4P_5}$

$\overline{G} = \overline{G_5 + P_5G_4 + P_5P_4G_3 + P_5P_4G_3G_2 + P_5P_4P_3P_2G_1 + P_5P_4P_3P_2P_1G_0}$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current All Inputs			220	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−290	−195	−135	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

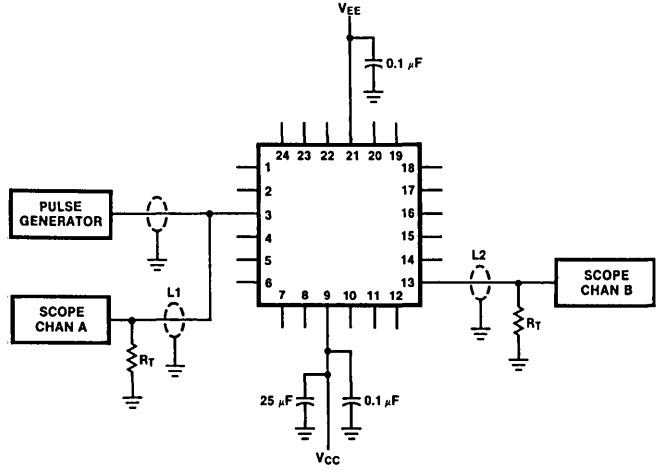
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.70	1.10	4.60	1.10	4.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$	1.00	3.00	1.00	3.00	1.00	3.30	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{G}$	1.40	3.90	1.40	3.80	1.40	3.90	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.10	4.00	1.10	3.90	1.10	4.00	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.40	ns	

Cerpak AC Electrical Characteristics

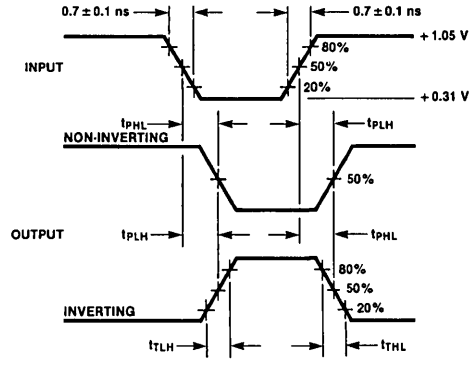
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	1.10	4.50	1.10	4.40	1.10	4.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$	1.00	2.80	1.00	2.80	1.00	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{G}$	1.40	3.70	1.40	3.60	1.40	3.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.10	3.80	1.10	3.70	1.10	3.80	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.30	0.45	2.20	0.45	2.30	ns	



TL/F/9872–6

FIGURE 1. AC Test Circuit



TL/F/9872–7

FIGURE 2. Propagation Delay and Transition Times

Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

National Semiconductor

F100181
4-Bit Binary/BCD Arithmetic Logic Unit

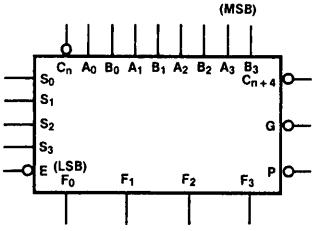
General Description

The F100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (S_n) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable ($\overline{E}$) input LOW makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F_n outputs and to the ripple Carry output, $\overline{C}_{n+4}$. Group Carry Lookahead Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are also provided, which are independent of the Carry input $\overline{C}_n$. The $\overline{P}$ output goes LOW when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, $\overline{G}$ goes LOW when the sum of A and B is greater than fifteen (nine for BCD) in a plus mode, or when their difference is greater than zero in a minus mode. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

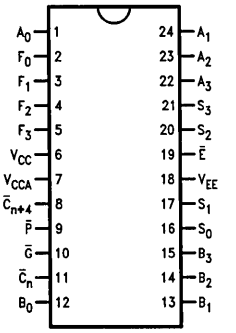
Logic Symbol



TL/F/9873–4

Connection Diagrams

24-Pin DIP



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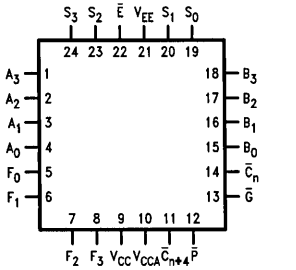
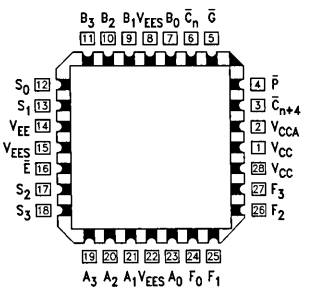
24-Pin Quad Cerpak



TL/F/9873–2

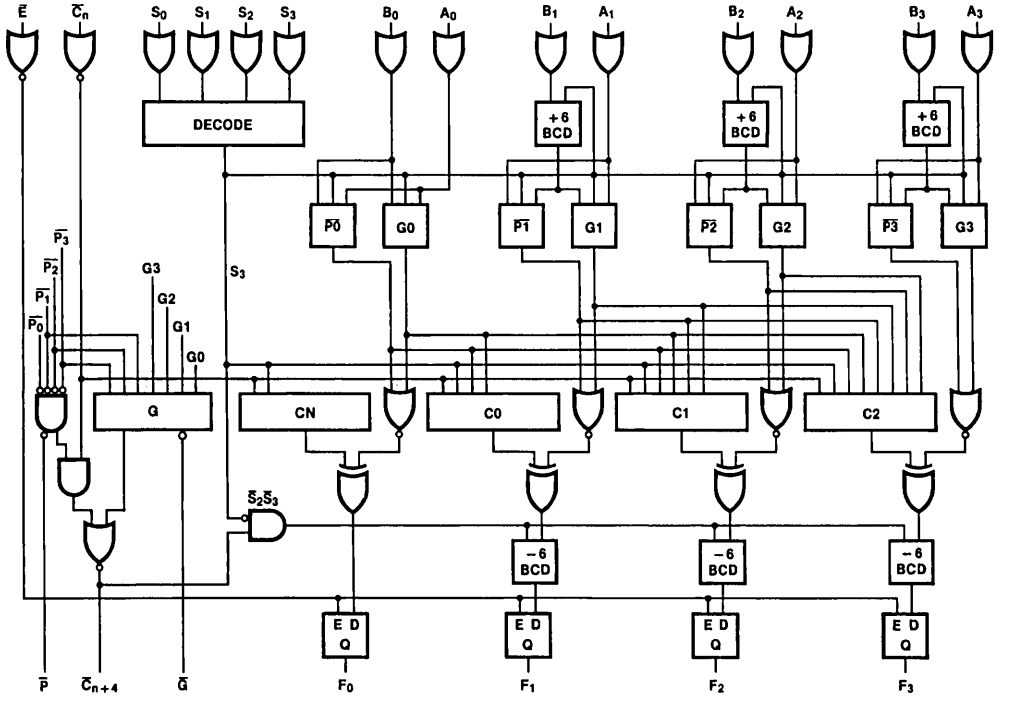
Pin Names	Description
A_0–A_3	Word A Operand Inputs
B_0–B_3	Word B Operand Inputs
$\overline{C}_n$	Carry Input (Active LOW)
S_0–S_3	Function Select Inputs
$\overline{E}$	Latch Enable Input (Active LOW)
$\overline{P}$	Carry Lookahead Propagate Output (Active LOW)
$\overline{G}$	Carry Lookahead Generate Output (Active LOW)
$\overline{C}_{n+4}$	Carry Output
F_0–F_3	Function Outputs

28-Pin PCC (Preliminary)



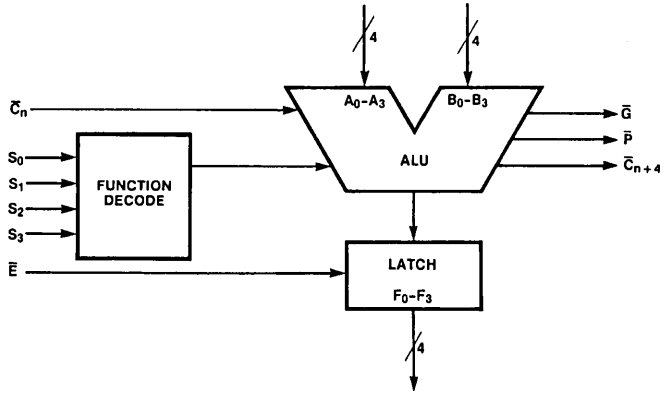
TL/F/9873–3

Logic Diagram



TL/F/9873–5

Block Diagram



TL/F/9873–6

Functional Description

There are two modes of operation: Arithmetic and Logic. The S_3 input controls these two modes:

S_3 = LOW for Arithmetic mode

S_3 = HIGH for Logic mode

The arithmetic mode includes decimal and binary arithmetic operations. S_2 is the control input: with S_3 = LOW,

S_2 = LOW for Decimal Arithmetic (BCD)

S_2 = HIGH for Binary Arithmetic

DECIMAL ARITHMETIC OPERATION

Addition

F = A plus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically performs the "+6" and "−6" logic correction internally.

Subtraction

F = A minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the nines complement of B and adds "+6". A "−6" adjustment is made if the subtraction algorithm calls for it. If there is a carry out, the result is a positive number. With no carry out, the result is a negative number expressed in its nines complement form. Therefore, to perform a subtraction with results in the tens complement form, an initial carry should be forced into the lowest order bit, i.e., set $\overline{C}_n$ = LOW.

(tens complement of B) = (nines complement of B) + 1

F = B minus A plus C_n. Operation is similar to and results are the same as F = A minus B plus C_n.

BINARY ARITHMETIC OPERATION

Addition

F = A minus B plus C_n. Arguments A and B are directly applied to the inputs.

Subtraction

F = A minus B plus C_n. Arguments A and B are directly applied to the inputs. The circuit automatically takes the ones complement of B (by inverting B internally). If there is a carry out the result is a positive number. With no carry out, the result is a negative number expressed in its ones complement form. Therefore, to perform a subtraction with results in the twos complement form, an initial carry should forced into the lowest order bit, i.e., set $\overline{C}_n$ = LOW.

(twos complement of B) = (ones complement of B) + 1

F = B minus A plus C_n. Operation is similar and results are the same as F = A minus B plus C_n.

Function Table

S_3	S_2	S_1	S_0	F_n Function	G_n (n = 0 to 3)	P_n (n = 0 to 3)	Outputs		
					Internal Signals		$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	L	F_n = A plus B plus C_n (BCD)	A_nD_n	$A_n + D_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	L	H	F_n = A minus B plus C_n (BCD)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	L	F_n = B minus A plus C_n (BCD)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	L	H	H	F_n = 0 minus B plus C_n (BCD)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
L	H	L	L	F_n = A plus B plus C_n (Binary)	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	L	H	F_n = A minus B plus C_n (Binary)	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	L	F_n = B minus A plus C_n (Binary)	$\overline{A}_nB_n$	$\overline{A}_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
L	H	H	H	F_n = 0 minus B plus C_n (Binary)	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	L	L	L	$F_n = A_nB_n + \overline{A}_n\overline{B}_n$	A_nB_n	$A_n + B_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	L	H	$F_n = A_n\overline{B}_n + \overline{A}_nB_n$	$A_n\overline{B}_n$	$A_n + \overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}$	$\overline{P}$
H	L	H	L	$F_n = A_n + B_n$	A_n	$\overline{B}_n$	$\overline{C}_{n+4}$	$\overline{G}_x$	$\overline{P}$
H	L	H	H	$F_n = A_n$	A_n	H	$\overline{C}_{n+4}$	$\overline{G}$	L
H	H	L	L	$F_n = \overline{B}_n$	L	B_n	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	L	H	$F_n = B_n$	L	$\overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	H	L	$F_n = A_nB_n$	L	$\overline{A}_n + \overline{B}_n$	$\overline{C}_{n+4}$	H	$\overline{P}$
H	H	H	H	F_n = LOW	L	H	$\overline{C}_n$	H	L

H = HIGH Voltage Level

L = LOW Voltage Level

$$\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$$

$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

$$\overline{C}_{n+4} = \overline{G} \bullet (\overline{P} + \overline{C}_n)$$

Arithmetic Operations

$$F_n = \overline{G_n + \overline{P}_n} \oplus C_i \quad i = 0 \text{ to } 3$$

Logic Operations

$$F_n = G_n + \overline{P}_n$$

Internal Equations for Carry Lookahead

(i = 0, 1, 2, 3)

$$C_0 = C_n + S_3$$

$$C_1 = G_0 + P_0C_n + S_3$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_n + S_3$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n + S_3$$

Internal Equations for +6 Logic

$$D_0 = B_0$$

$$D_1 = \overline{B}_1$$

$$D_2 = B_1B_2 + \overline{B}_1\overline{B}_2$$

$$D_3 = B_1 + B_2 + B_3$$

$$\overline{G}_x = \overline{G_3P_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current S_n, $\overline{E}$ All Others			350 250	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−300	−210	−130	mA	Inputs Open

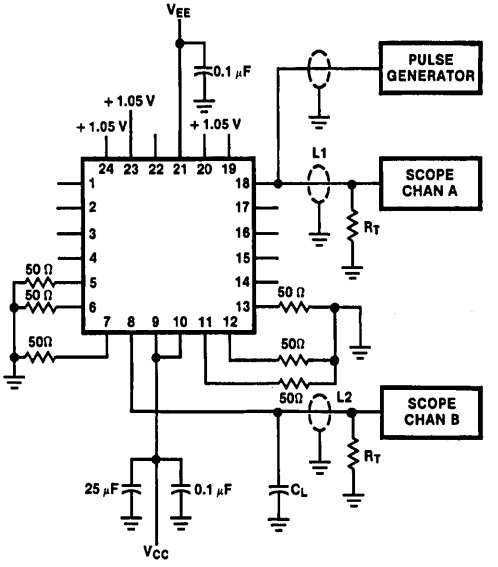
Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.90	2.10	6.80	2.30	7.40	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.70	1.40	4.40	1.40	4.70	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.50	2.00	6.50	2.10	6.80	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	5.10	1.60	5.20	1.60	5.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	3.00	1.40	3.00	1.40	3.10	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.80	1.50	8.60	1.50	9.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.40	2.00	5.90	2.00	6.50	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	10.10	2.80	8.50	2.90	8.70	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.40	0.90	3.60	1.10	3.80	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.70	0.45	2.60	0.45	2.70	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	 7.60 8.70 4.80		 7.60 8.50 5.00		 8.10 9.60 5.30		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	 0.10 0.60 0.60		 0.10 0.60 0.60		 0.10 0.60 0.60		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*

Cerpak AC Electrical Characteristics V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to F_n	2.00	6.70	2.10	6.60	2.30	7.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{P}$, $\overline{G}$	1.40	4.50	1.40	4.20	1.40	4.50	ns	
t_{PLH} t_{PHL}	Propagation Delay A_n, B_n to $\overline{C}_{n+4}$	2.00	6.30	2.00	6.30	2.10	6.60	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to F_n	1.60	4.90	1.60	5.00	1.60	5.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay $\overline{C}_n$ to $\overline{C}_{n+4}$	1.30	2.80	1.40	2.80	1.40	2.90	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to F_n	1.40	8.60	1.50	8.40	1.50	8.80	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{P}$, $\overline{G}$	1.70	7.20	2.00	5.70	2.00	6.30	ns	
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{C}_{n+4}$	2.70	9.90	2.80	8.30	2.90	8.50	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to F_n	1.00	3.20	0.90	3.40	1.10	3.60	ns	*Figures 1* and *2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.60	0.45	2.50	0.45	2.60	ns	*Figures 1* and *2*
t_s	Setup Time A_n, B_n S_n $\overline{C}_n$	 7.50 8.60 4.70		 7.50 8.40 4.90		 8.00 9.50 5.20		ns	*Figure 3*
t_h	Hold Time A_n, B_n S_n $\overline{C}_n$	 0 0.50 0.50		 0 0.50 0.50		 0 0.50 0.50		ns	
$t_{pw}(L)$	Pulse Width LOW $\overline{E}$	2.00		2.00		2.00		ns	*Figure 2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

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FIGURE 1. AC Test Circuit

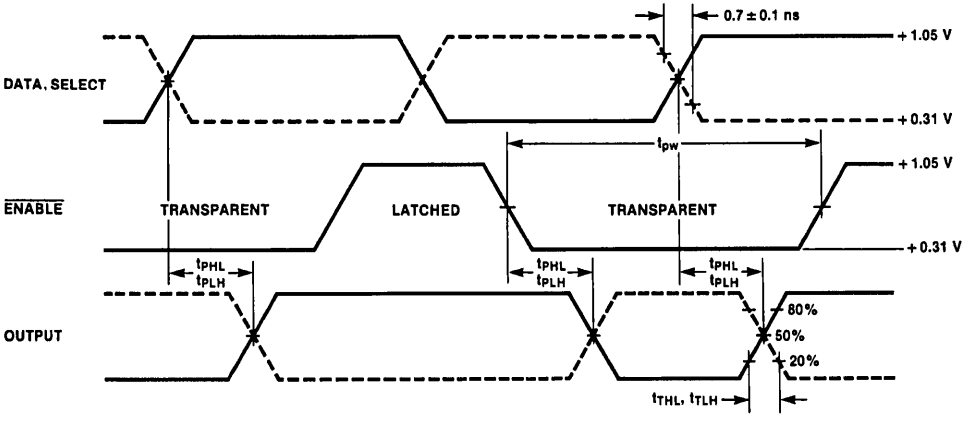

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FIGURE 2. Enable Timing

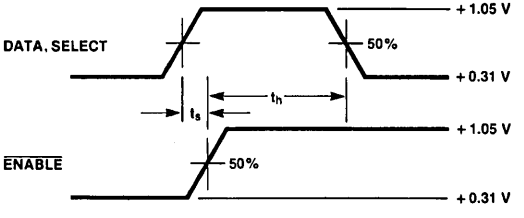

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FIGURE 3. Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

National Semiconductor

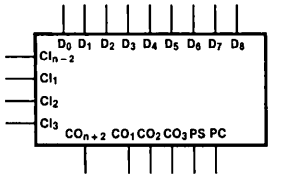
F100182
9-Bit Wallace Tree Adder

General Description

The F100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The F100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the F100183 Recode Multiplier, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the F100182 assists in performing parallel multiplication of two signed numbers to produce a signed twos complement product. See F100183 data sheet for additional information. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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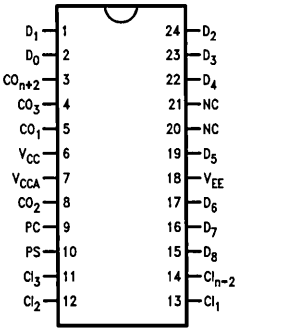
Connection Diagrams

24-Pin DIP



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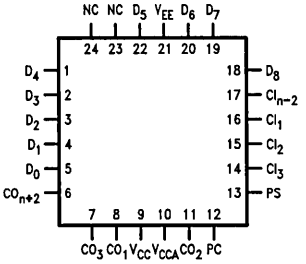
24-Pin Quad Cerpak



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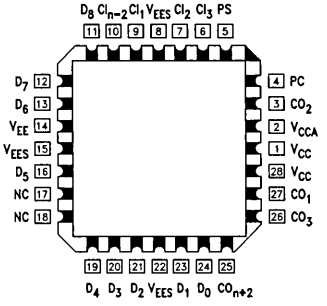
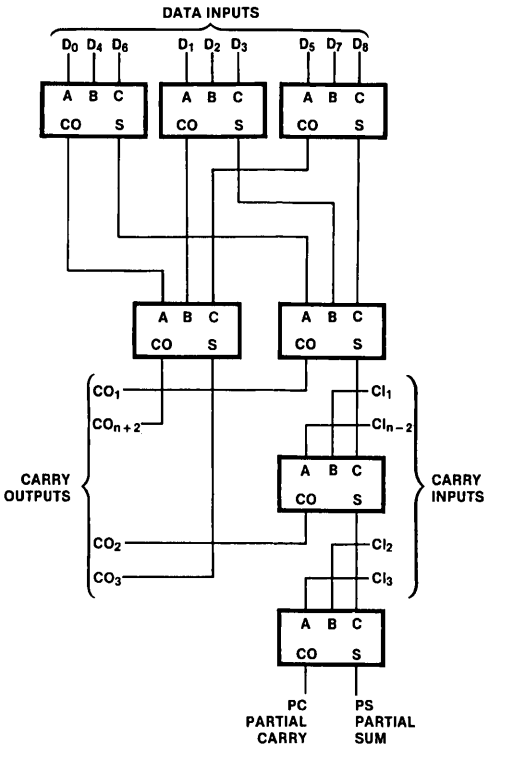
28-Pin PCC (Preliminary)



TL/F/9874–4

Pin Names	Description
D_0–D_8	Data Inputs
CI_1–CI_3, CI_{n-2}	Carry Inputs
CO_1–CO_3, CO_{n+2}	Carry Outputs
PS	Partial Sum Output
PC	Partial Carry Output

Logic Diagram



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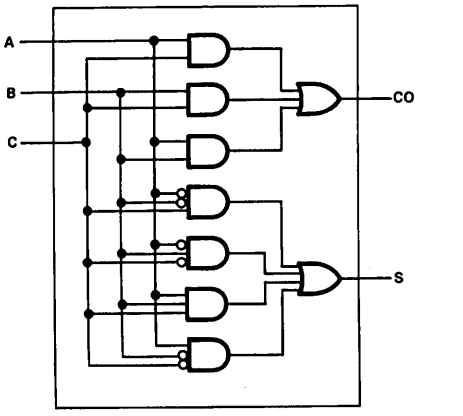
Adder Logic Diagram



TL/F/9874–6

Adder Truth Table

Inputs			Outputs	
A	B	C	S	CO
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current CI_1–CI_3, CI_{n-2} D_1, D_3, D_4, D_5, D_6, D_8			300	μA	V_{IN} = $V_{IH\,(Max)}$
	D_0, D_2, D_7			250		
I_{EE}	Power Supply Current	−260	−180	−125	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

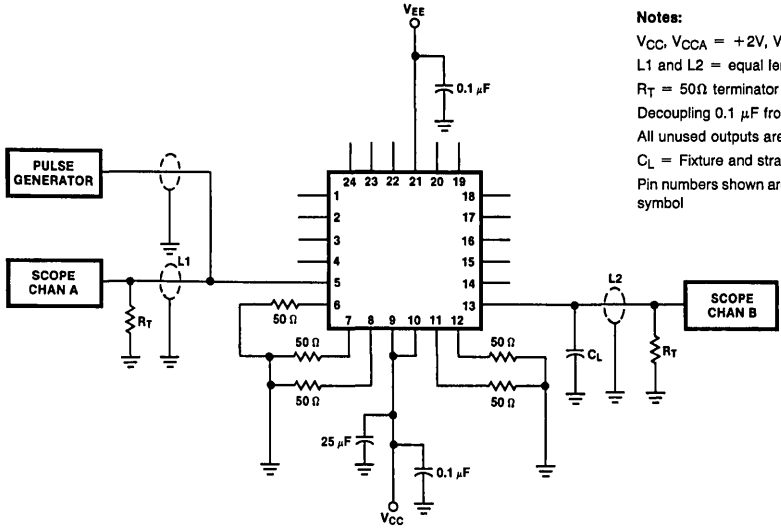
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.50	1.40	4.50	1.50	4.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.80	1.30	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.20	2.20	6.10	2.30	6.40	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.70	1.40	4.70	1.50	5.00	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.20	2.50	7.20	2.70	7.40	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.50	1.00	3.40	1.10	3.70	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.50	1.50	4.45	1.60	4.60	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.30	0.80	3.20	0.90	3.60	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.60	0.45	1.60	0.45	1.60	ns	*Figures 1* and *2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_{n+2}	1.40	4.30	1.40	4.30	1.50	4.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_1	1.30	4.60	1.30	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_2	2.20	6.00	2.20	5.90	2.30	6.20	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to CO_3	1.30	4.50	1.40	4.50	1.50	4.80	ns	
t_{PLH} t_{PHL}	Propagation Delay D_n to PS, PC	2.50	7.00	2.50	7.00	2.70	7.20	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to CO_2	1.00	3.30	1.00	3.20	1.10	3.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay CI_{n-2}, CI_1 to PS, PC	1.50	4.30	1.50	4.25	1.60	4.40	ns	
t_{PLH} t_{PHL}	Propagation Delay CI_3, CI_2 to PS, PC	0.80	3.10	0.80	3.00	0.90	3.40	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	1.50	0.45	1.50	0.45	1.50	ns	*Figures 1* and *2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

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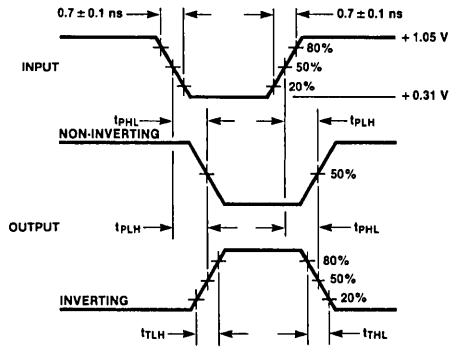
FIGURE 1. AC Test Circuit

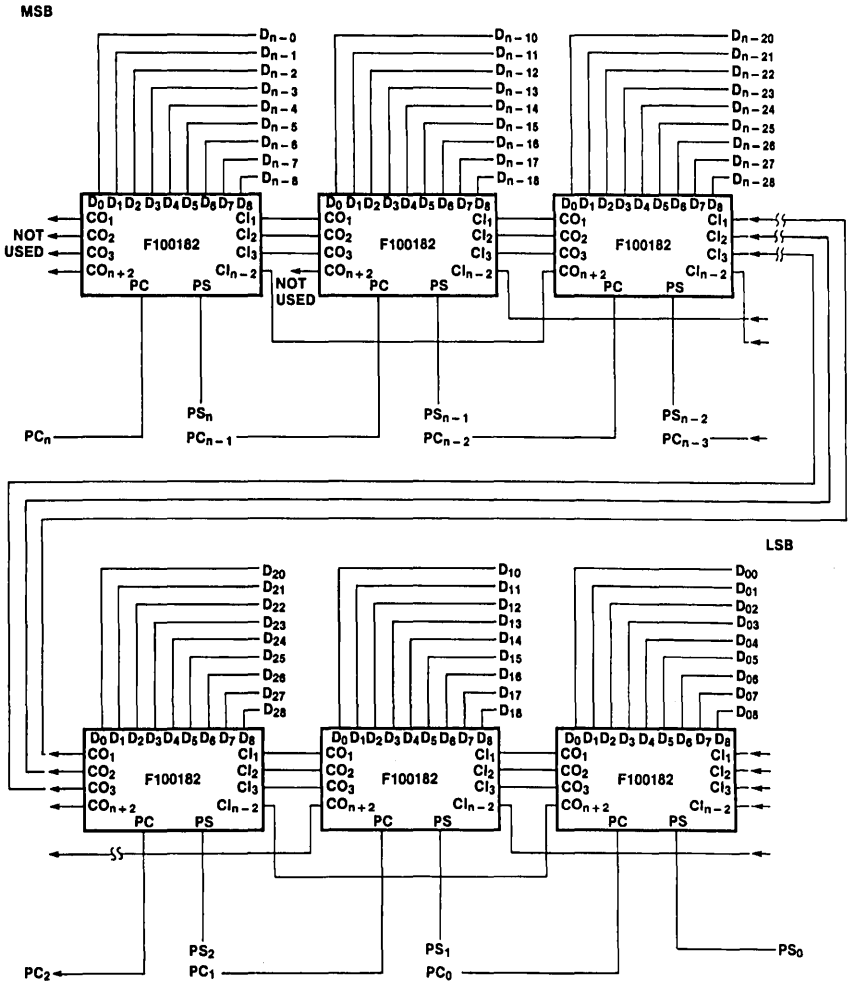


TL/F/9874–8

FIGURE 2. Propagation Delay and Transition Times

Application

Typical Horizontal Interconnection of 9-Bit Wallace Tree Adders F100182



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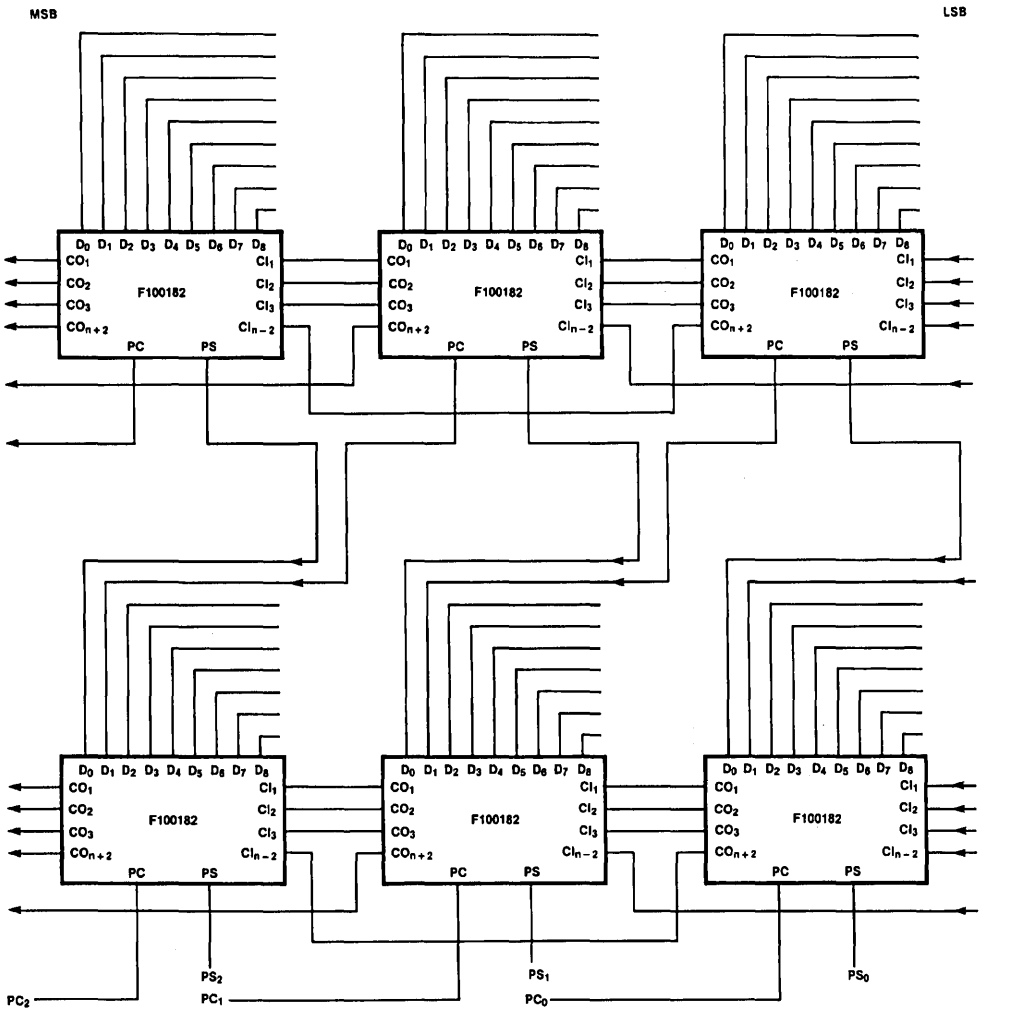
Application (Continued)

16-Bit Vertical Expansion of Wallace Tree Adders



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National Semiconductor

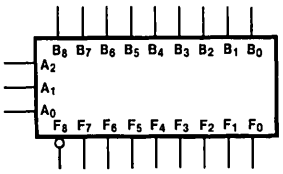
F100183
2 x 8-Bit Recode Multiplier

General Description

The F100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication. In conjunction with the F100182 Wallace Tree Adder, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the F100183 performs parallel multiplication of two signed numbers in twos complement form to produce a signed twos complement product. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 6

Logic Symbol



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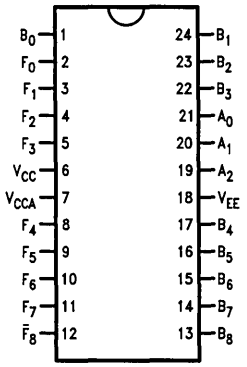
Connection Diagrams

24-Pin DIP



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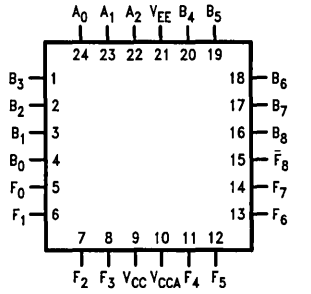
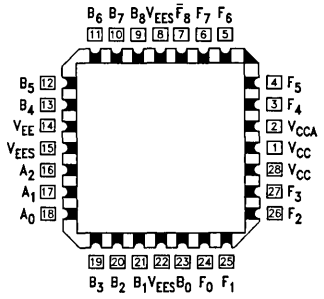
24-Pin Quad Cerpak



TL/F/9875-2

Pin Names	Description
A_0–A_2	Multiplier (Recode) Inputs
B_0–B_8	Multiplicand Inputs
F_0–F_7	Partial Product Outputs
$\overline{F}_8$	Sign Extension Output

28-Pin PCC (Preliminary)



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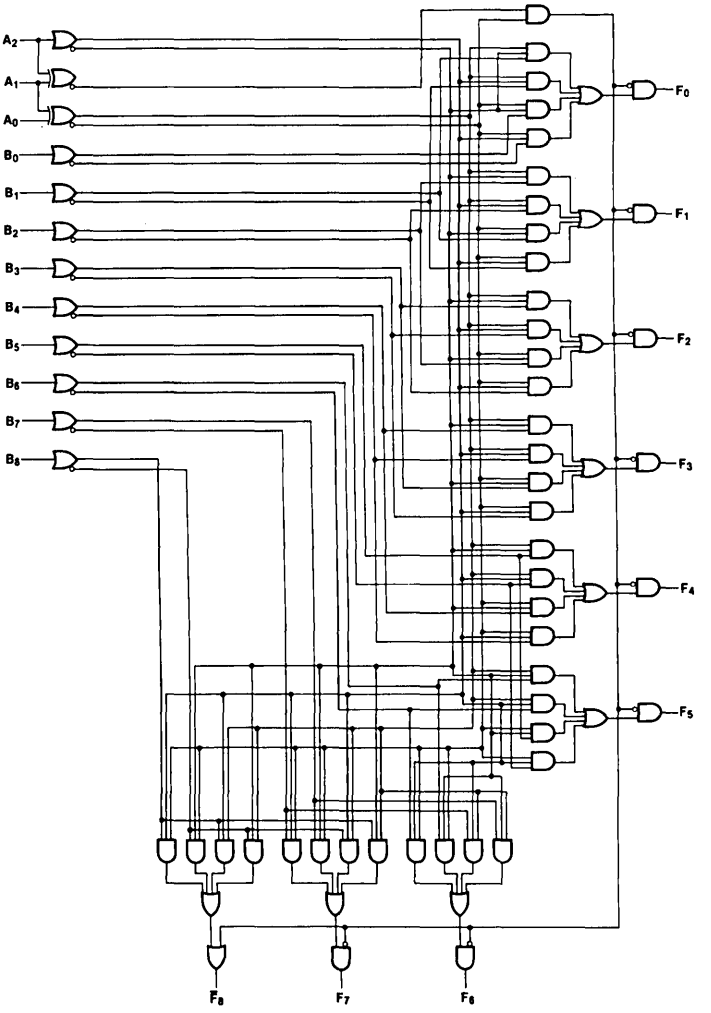
Logic Diagram



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Truth Table

Inputs			Recode Mode	Outputs								
A_2	A_1	A_0		$\overline{F}_8$	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
L	L	L	0	H	L	L	L	L	L	L	L	L
L	L	H	+1	$\overline{B}_8$	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
L	H	L	+1	$\overline{B}_8$	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
L	H	H	+2	$\overline{B}_8$	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
H	L	L	−2	B_8	$\overline{B}_7$	$\overline{B}_6$	$\overline{B}_5$	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$	$\overline{B}_0$
H	L	H	−1	B_8	$\overline{B}_8$	$\overline{B}_7$	$\overline{B}_6$	$\overline{B}_5$	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$
H	H	L	−1	B_8	$\overline{B}_8$	$\overline{B}_7$	$\overline{B}_6$	$\overline{B}_5$	$\overline{B}_4$	$\overline{B}_3$	$\overline{B}_2$	$\overline{B}_1$
H	H	H	0	H	L	L	L	L	L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620			
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605			
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1595			
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620			
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V
V_{OLC}	Output LOW Voltage			−1610			
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL\ (Min)}$	

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current B_0–B_8 A_0 A_1 A_2			 215 215 285 310	μA	V_{IN} = $V_{IH\ (Max)}$
I_{EE}	Power Supply Current	−250	−170	−115	mA	Inputs Open

Ceramic Dual-In-Line Package AC Electrical Characteristics

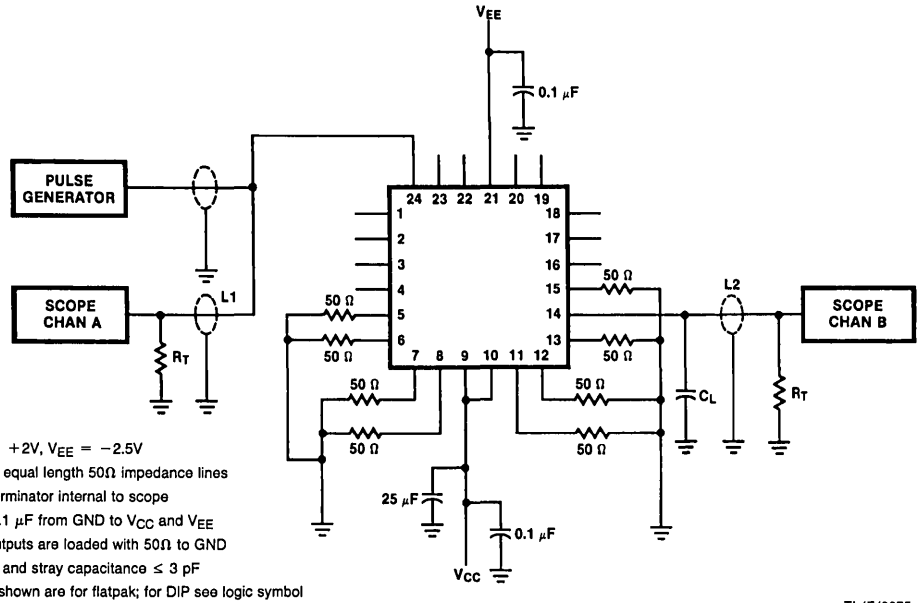
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to F_0–F_7	1.10	3.90	1.10	3.80	1.10	4.20	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to $\overline{F}_8$	0.90	3.20	1.00	3.10	1.00	3.60	ns	
t_{PLH} t_{PHL}	Propagation Delay B_0–B_8 to F_0–F_7	0.80	2.20	0.90	2.15	0.90	2.50	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay B_8 to $\overline{F}_8$	0.80	2.00	0.90	2.00	0.90	2.50	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.50	0.45	2.40	0.45	2.60	ns	*Figures 1* and *2*

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to F_0–F_7	1.10	3.70	1.10	3.60	1.10	4.00	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay A_0–A_2 to $\overline{F}_8$	0.90	3.00	1.00	2.90	1.00	3.40	ns	
t_{PLH} t_{PHL}	Propagation Delay B_0–B_8 to F_0–F_7	0.80	2.00	0.90	1.95	0.90	2.30	ns	*Figures 1* and *2*
t_{PLH} t_{PHL}	Propagation Delay B_8 to $\overline{F}_8$	0.80	1.80	0.90	1.80	0.90	2.30	ns	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.45	2.40	0.45	2.30	0.45	2.50	ns	*Figures 1* and *2*



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V

L1 and L2 = equal length 50Ω impedance lines

R_T = 50Ω terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

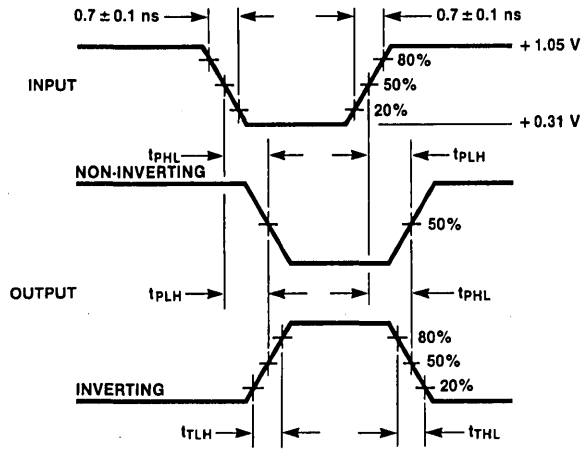
All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

TL/F/9875–6

FIGURE 1. AC Test Circuit



TL/F/9875–7

FIGURE 2. Propagation Delay and Transition Times

Application

F100183 is a 2 x 8-bit recode multiplier that performs parallel multiplication using twos complement arithmetic. In multiplying, the multiplier is partitioned into recode groups, then each recode group operates on the multiplicand to provide a partial product at the same time. The F100183, 2 x 8-bit recode multiplier provides partial products in 3.6 ns.

The F100182, 9-Bit Wallace Tree Adder combines the partial products to obtain the partial sum and partial carries in an additional 10.7 ns. Then the Carry Lookahead generator and 6-bit adder combine the results of a 16 x 16-bit multiply for a total of 24.3 ns. The propagation delays and package count for implementing various size multipliers are listed in Tables I and II.

Multiplication of twos complement binary numbers is accomplished by first obtaining all the partial products. Then the weighted partial products are added together to yield the final result. In the Wallace Tree method of multiplication the sign bit is treated the same as the rest of the bits to obtain a signed result.

TABLE I. Propagation Delay Summation*

Array Size	Recode Multiplier 100183	Wallace Tree Adder 100182	High-speed Adder 100180	Carry Lookahead 100179		Total (Max) Delay
16 x 16	3.6	10.7	7.3	2.7	=	24.3 ns
17 x 17 thru 24 x 24	3.6	21.4	7.3	2.7	=	35.0 ns
25 x 25 thru 48 x 48	3.6	21.4	7.3	5.4	=	37.7 ns
49 x 49 thru 72 x 72	3.6	21.4	7.3	8.1	=	40.4 ns
73 x 73	3.6	32.1	7.3	10.8	=	53.8 ns

*Worst case, Flatpak

Application (Continued)

TABLE II. Package Count

	100102 100117	100183	100182	100180	100179		Total
16 x 16	6	16	32	6	2	=	62
18 x 18	7	27	38	6	2	=	70
24 x 24	9	36	60	8	2	=	115
32 x 32	11	64	96	11	4	=	186
36 x 36	13	80	116	12	4	=	225
64 x 64	24	256	328	22	6	=	634

For a quick review of the twos complement number format see Table III. Note that subtraction is accomplished by adding the negative number. An example of changing from a positive number to a negative number is shown.

1011 negative number-5

0100 bits inverted
+0001 add one
0101 Results 5

TABLE III. Twos Complement Format

Sign Bit	Magnitude 2^2	2^1	2^0	Decimal Number
0	1	1	1	+7
0	1	1	0	+6
0	1	0	1	+5
0	1	0	0	+4
0	0	1	1	+3
0	0	1	0	+2
0	0	0	1	+1
0	0	0	0	+0
1	1	1	1	−1
1	1	1	0	−2
1	1	0	1	−3
1	1	0	0	−4
1	0	1	1	−5
1	0	1	0	−6
1	0	0	1	−7
1	0	0	0	−8

Multiplication Algorithm

In the multiplication algorithm used, the multiplier ($Y_n \ldots Y_0$) is partitioned into recode groups and each recode group operates on the multiplicand ($X_n \ldots X_0$) as in *Figure 4.* The F100183, 2 x 8-bit recode multiplier partitions the multiplier ($X_n \ldots X_0$) into groups of eight and the multiplicand ($Y_n \ldots Y_0$) into groups of two. Each recode group is two bits wide but requires three bits to determine the partial products. Table IV lists the significance of the various recode groups. The partial product is ±0, ±multiplicand, or ±two times the multiplicand. A forced zero is required to establish the least significant bit of the first recode group. By connecting recode multipliers in parallel the partial products are available at the same time. The weighted partial products ($A_n \ldots A_0$, $B_n \ldots B_0$) . . . are added together using F100182, 9-bit Wallace Tree Adders. The results of the partial sum and partial carry are combined together using Carry Lookahead generators and 6-bit adders. An example of using recode multiplication is shown in *Figure 3:* multiplier (117_{10}) 01110101 times multiplicand (105_{10}) 01101001. The first recode group 010 requires adding the multiplicand; the second recode group 010 also requires adding the multiplicand; the third group 110 requires subtracting the multiplicand (the same as inverting each digit and adding 1); the fourth group 011 requires adding twice the multiplicand. Combining the results of four groups, 12285_{10}, we have the correct answer.

TABLE IV. Recode Product

Recode Group Y_{I+1}	Y_I	Y_{I-1}	Recode Value	Partial Product
0	0	0	+0	Add zero
0	0	1	+1	Add multiplicand
0	1	0	+1	Add multiplicand
0	1	1	+2	Add twice the multiplicand
1	0	0	−2	Subtract twice the multiplicand
1	0	1	−1	Subtract the multiplicand
1	1	0	−1	Subtract the multiplicand
1	1	1	−0	Subtract zero

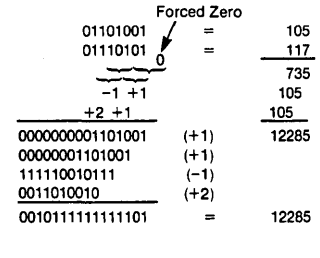


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FIGURE 3. Recode Multiplication Example

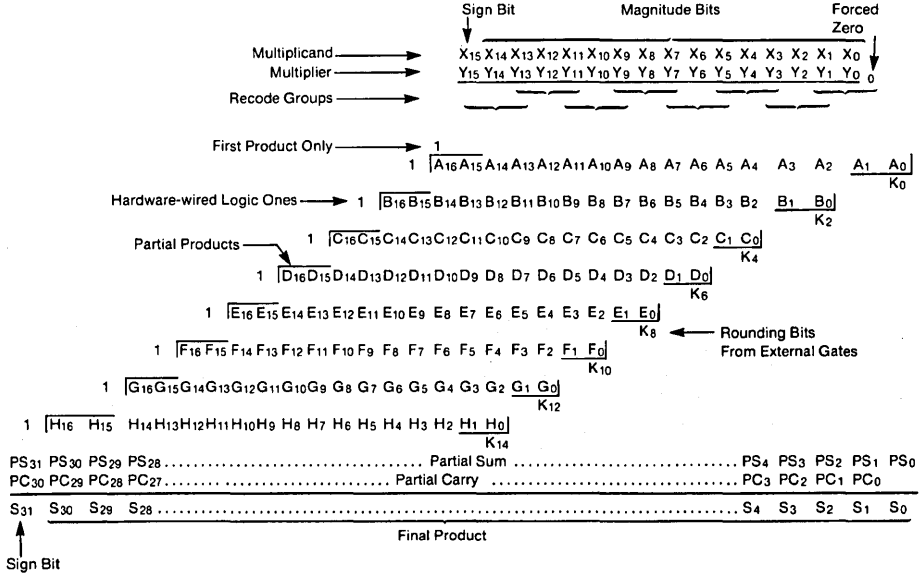

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FIGURE 4. 16 x 16 Multiply

Hardware Implementation

For the hardware implementation of the F100183 recode multiplier the sign bit is connected to the B_8 input, and B_7 through B_0 are the magnitude bits. Two extend the word length greater than eight bits, the B_0 and B_8 inputs of adjacent devices are connected together (see *Figure 7*). The device outputs F_0 through F_7 are used as the partial products; these correspond to A_0 through A_7, or A_8 through A_{15}, or B_0 through B_7, etc. To reduce the hardware, the $\overline{F}_8$ bit (A_{16} in *Figure 7*) is used as the sign bit of the partial product. The sign bits are extended by using hardware wired logic "1s". The ones are located in front of each partial product with an extra "1" at the sign bit of the first partial product as in *Figure 4*. The logic "1s" are wired as inputs into the Wallace Tree Adders as shown in *Figure 6*. If the recode group requires the multiplicand to be added, then the F100183 outputs the correct partial products to be added. But when the recode group requires that the multiplicand be subtracted, then the F100183 outputs the ones complement. External gates are required to generate a "1" to be added to the ones complement to complete the twos complement for the partial product *(Figure 7)*. These external gates generate the rounding bits, $K_0 \ldots K_n$, which are input to the Wallace Tree Adder. *Figures 4, 6* and *7* show the location. An example of multiplication which has the rounding bits and the hardware wired logic "1s" is shown in *Figure 5*.

The weighted partial products are added together using F100182, 9-bit Wallace Tree Adders as shown in *Figure 6*. The output is a partial sum and partial carry which can be reduced to the final product using Carry Lookahead and 6-bit adders. See *Figure 8*.

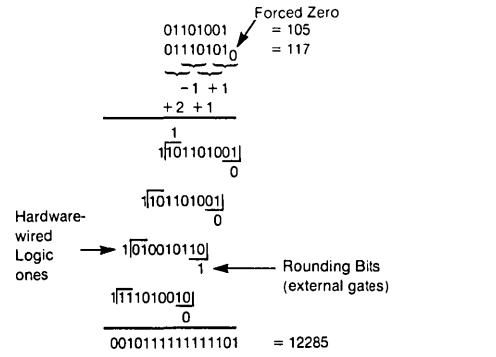

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FIGURE 5. Example of Multiplication Using Rounding Bits

Hardware Implementation (Continued)

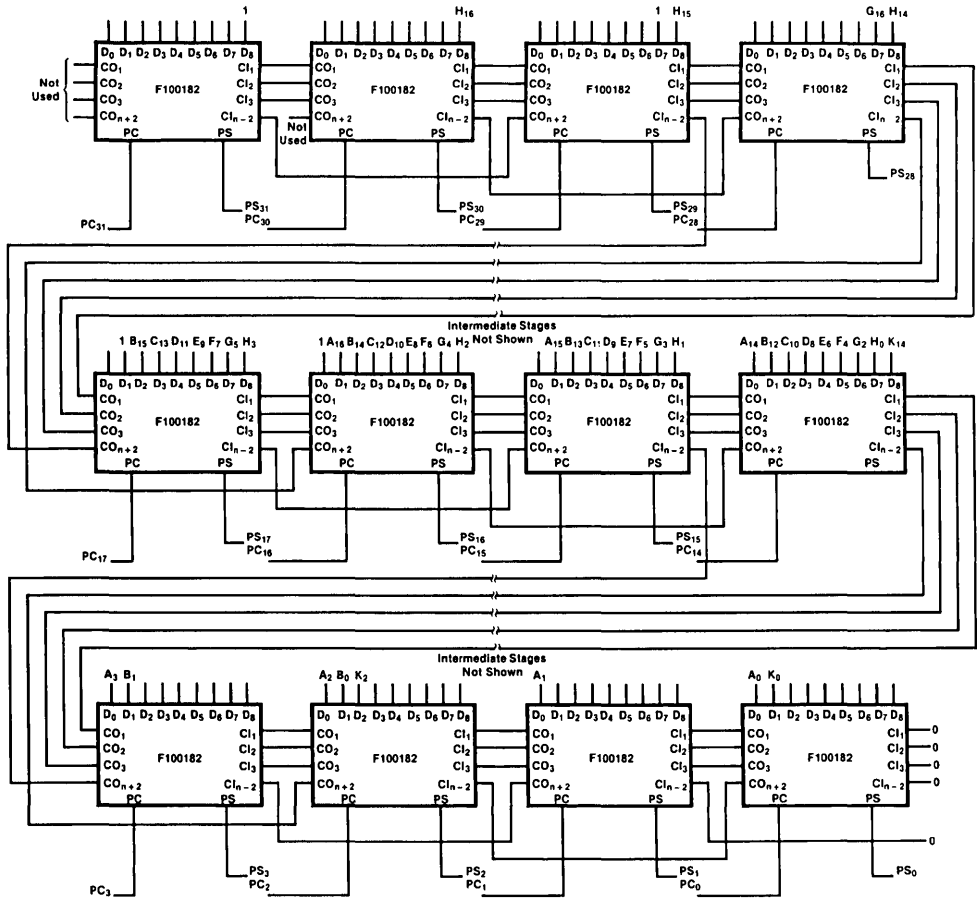

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FIGURE 6. F100182 Hook-up for 16 x 16 Multiplier

Hardware Implementation (Continued)

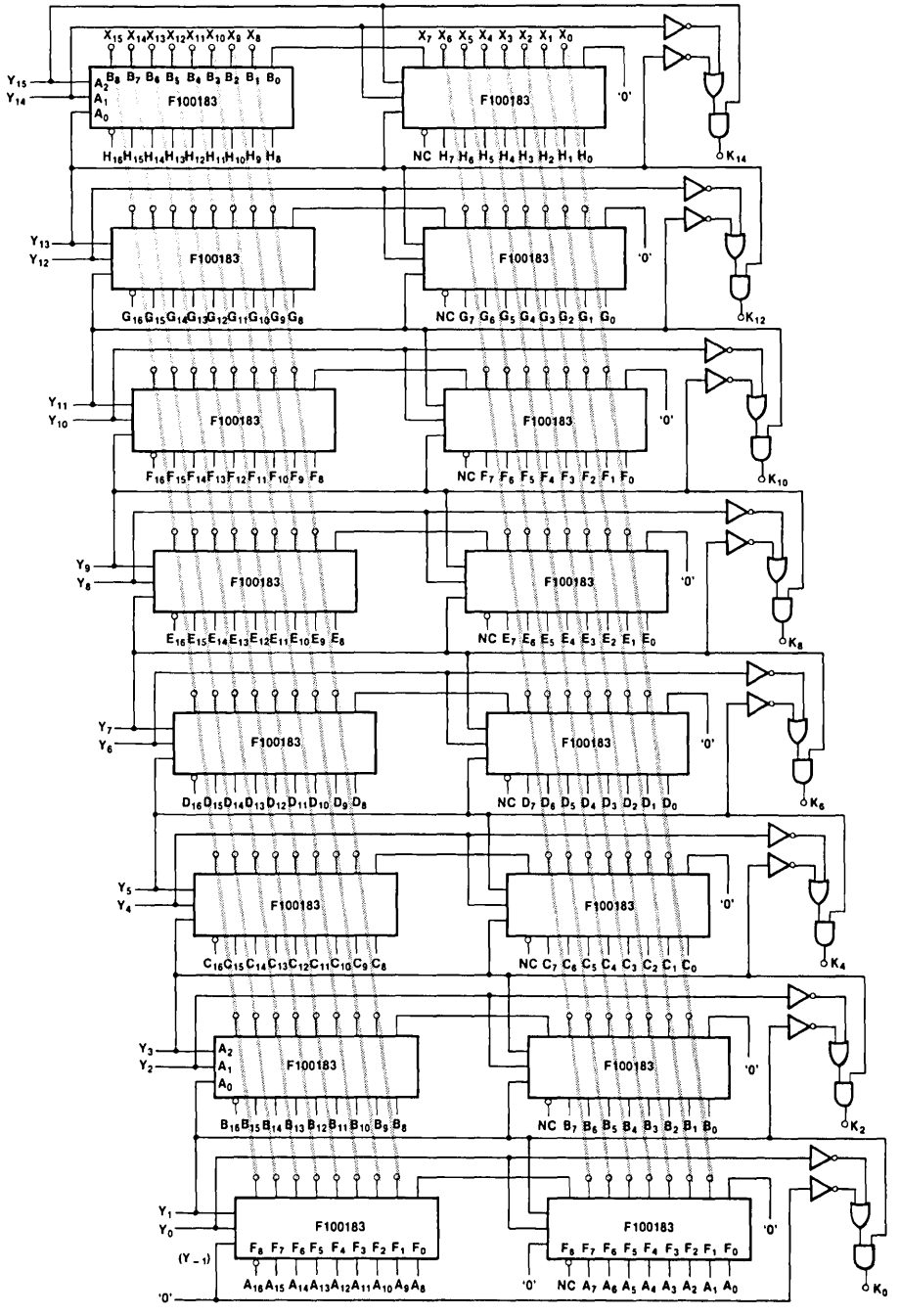

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FIGURE 7. F100183 Hook-Up for 16 x 16 Multiplier

Hardware Implementation (Continued)

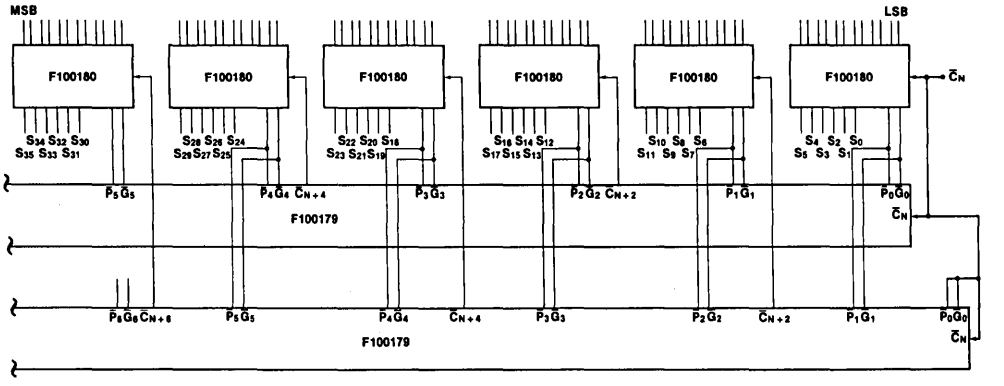

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FIGURE 8. Final Summation for 16 x 16 Multiplier

National Semiconductor

F100250
Quint Line Transceiver

General Description

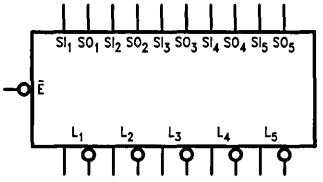
The F100250 is a quint line transceiver capable of simultaneously transmitting and receiving differential mode signals on a twisted pair line. Each transceiver has a signal input S_{IN}, a signal output S_{OUT} and two differential line inputs/outputs L and $\overline{L}$. Signals received from the lines L and $\overline{L}$ can be stored in an internal latch. The line outputs are designed to drive twisted pair lines. The $\overline{ENABLE}$ input is common to all five transceivers.

Features

- Full duplex operation
- Common mode noise immunity of ±1V

Ordering Code: See Section 6

Logic Symbol



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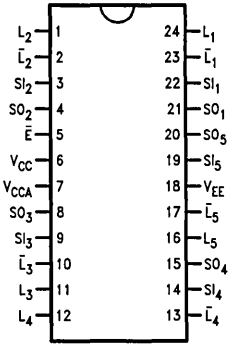
Pin Names	Description
$\overline{E}$	Common Enable
S_{In}	100K Signal Inputs
S_{On}	100K Signal Outputs
L_n, $\overline{L}_n$	Differential Line Inputs/Outputs

Connection Diagrams

24-Pin DIP



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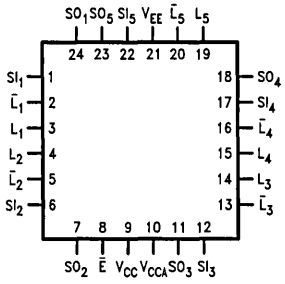
24-Pin Quad Cerpak



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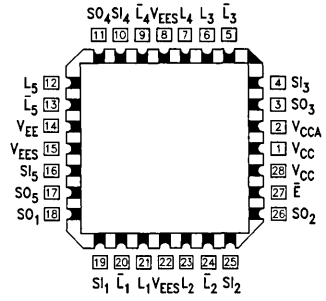
28-Pin PCC (Preliminary)



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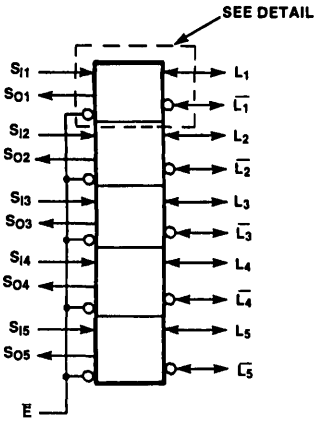
2

Logic Diagram



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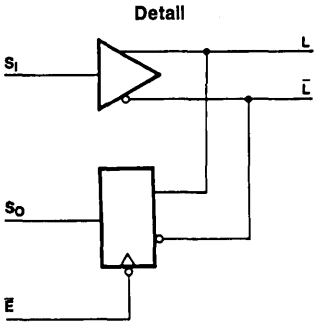

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Truth Table

$\overline{E}$	S_{IA}	S_{IB}	S_{OA}	S_{OB}	L	$\overline{L}$
H	X	X	$S_{OA}(n-1)$	$S_{OB}(n-1)$	*	*
L	L	L	L	L	U_L	U_H
L	L	H	H	L	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	L	L	H	$(U_L + U_H)/2$	$(U_L + U_H)/2$
L	H	H	H	H	U_H	U_L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
n−1 = Previous State
* = Dependent on S_{IA} and S_{IB}

$U_L \approx -1.27V$
$U_H \approx -0.27V$
$(U_L + U_H)/2 \approx -0.77V$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Case Temperature under Bias (T_C)	0°C to +85°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
Operating Range (Note 2)	−5.7V to −4.2V

DC Electrical Characteristics

V_{EE} = −4.2V to −4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{IH}	Input HIGH Current	S_{In} Enable			200 250	μA μA	V_{IN} = $V_{IH(Max)}$
I_{EE}	Power Supply Current		−280	−267	−180	mA	Inputs Open

DC Electrical Characteristics

V_{EE} = −4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1025	−955	−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810	−1705	−1620	mV		
V_{OHC}	Output HIGH Voltage	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{KH}	Line Output HIGH Voltage	−370		−220	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1400		−1090	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1020		−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1810		−1605	mV		
V_{OHC}	Output HIGH Voltage	−1030			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1595	mV		
V_{KH}	Line Output HIGH Voltage	−350		−200	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1300		−990	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1150		−870	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

DC Electrical Characteristics

V_{EE} = −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions (Note 4)	
V_{OH}	Output HIGH Voltage	−1035		−880	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	Loading with 50Ω to −2.0V
V_{OL}	Output LOW Voltage	−1830		−1620	mV		
V_{OHC}	Output HIGH Voltage	−1045			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$	
V_{OLC}	Output LOW Voltage			−1610	mV		
V_{KH}	Line Output HIGH Voltage	−400		−250	mV	No Load	
V_{KL}	Line Output LOW Voltage	−1500		−1190	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$	
V_{IH}	Input HIGH Voltage	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	−1830		−1490	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = $V_{IL(Min)}$	

Note 1: Unless specified otherwise on individual data sheet.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

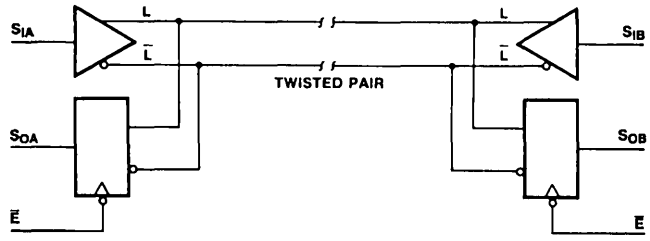
V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_I to S_O	2.0	6.0	2.0	6.2	2.0	6.2	ns	Figures 4 and *8*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to S_O	1.4	2.9	1.2	2.7	1.2	2.7	ns	*Figures 5* and *8*
t_{PLH} t_{PHL}	Propagation Delay S_I to L, $\overline{L}$	1.2	2.9	1.2	2.7	1.2	2.7	ns	*Figures 2, 3* and *7*
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_O	1.0	4.0	1.0	4.3	1.0	4.3	ns	
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	2.0	0.5	2.0	0.5	2.0	ns	
t_S	Setup Time L, $\overline{L}$	1.3		1.3		1.5		ns	*Figure 6*
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	

Cerpak AC Electrical Characteristics

V_{EE} = −4.2V to −4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_I to S_O	2.0	6.0	2.0	6.0	2.0	6.0	ns	*Figures 4* and *8*
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to S_O	1.4	2.5	1.4	2.5	1.4	2.5	ns	*Figures 5* and *8*
t_{PLH} t_{PHL}	Propagation Delay S_I to L, $\overline{L}$	1.2	2.5	1.2	2.5	1.2	2.5	ns	*Figures 2, 3* and *7*
t_{PLH} t_{PHL}	Propagation Delay L, $\overline{L}$ to S_O	1.0	4.1	1.0	4.1	1.0	4.1	ns	
t_{THL} t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.5	1.9	0.5	1.9	0.5	1.9	ns	
t_S	Setup Time L, $\overline{L}$	1.3		1.3		1.5		ns	*Figure 6*
t_H	Hold Time L, $\overline{L}$	1.3		1.3		1.5		ns	



TL/F/9876–5

FIGURE 1. Interconnection of Two F100250 Circuits

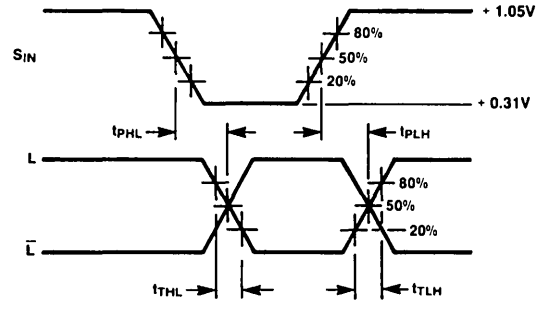


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FIGURE 2. S_I to Differential Line

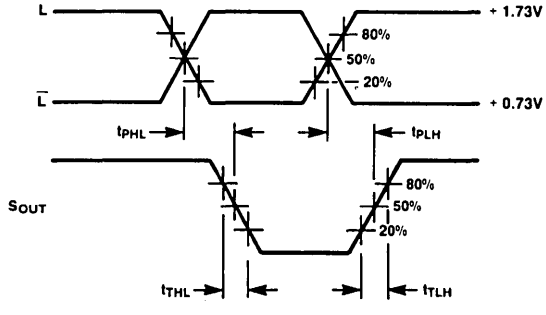

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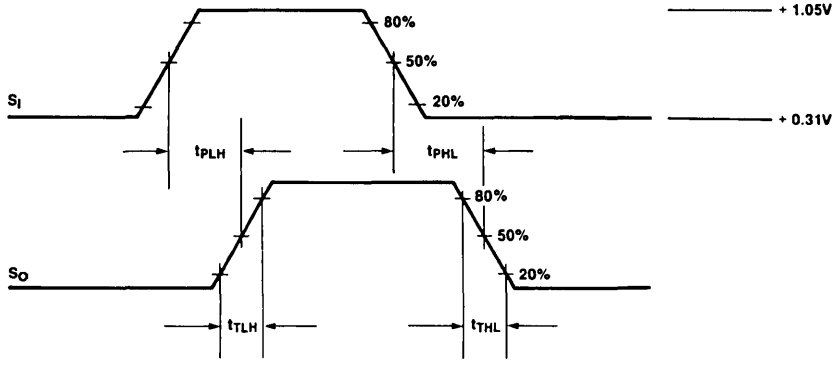
FIGURE 3. Differential Line to S_O



TL/F/9876–10

FIGURE 4. S_I to S_O

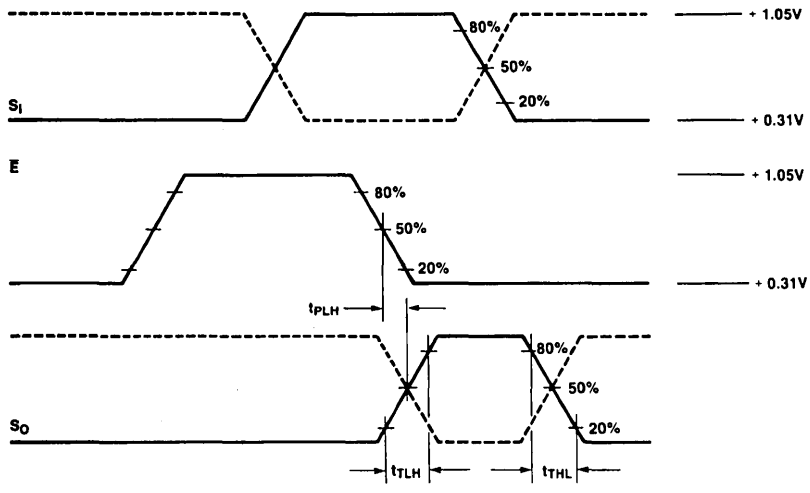


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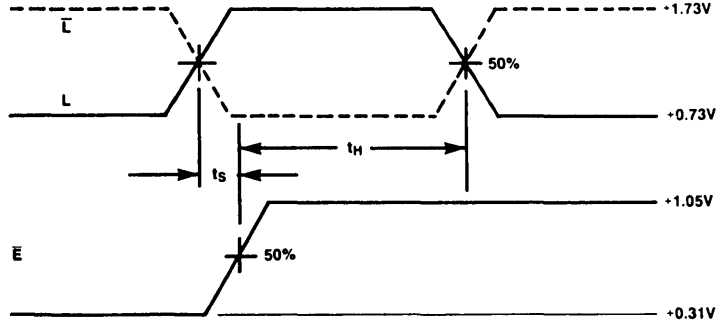
FIGURE 5. $\overline{E}$ to S_O



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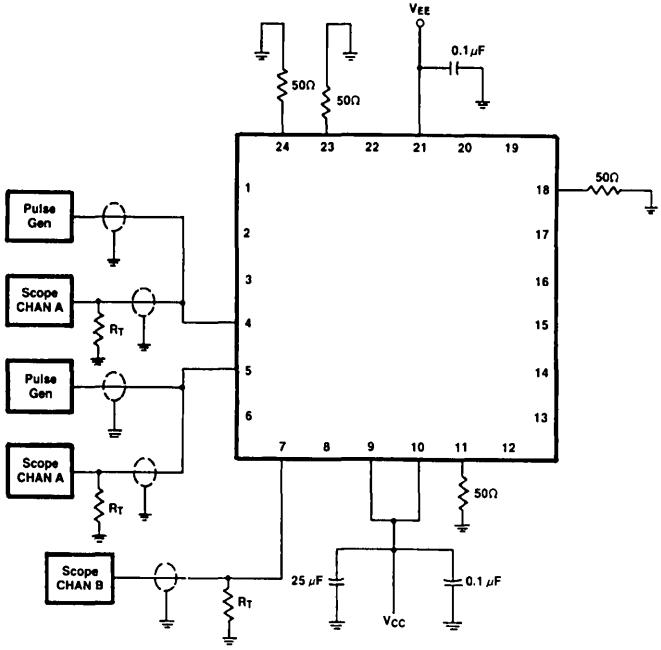
Notes:

t_S is the minimum time before the transition of the clock that information must be present at the data input.

t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Line Data Setup and Hold Time



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.

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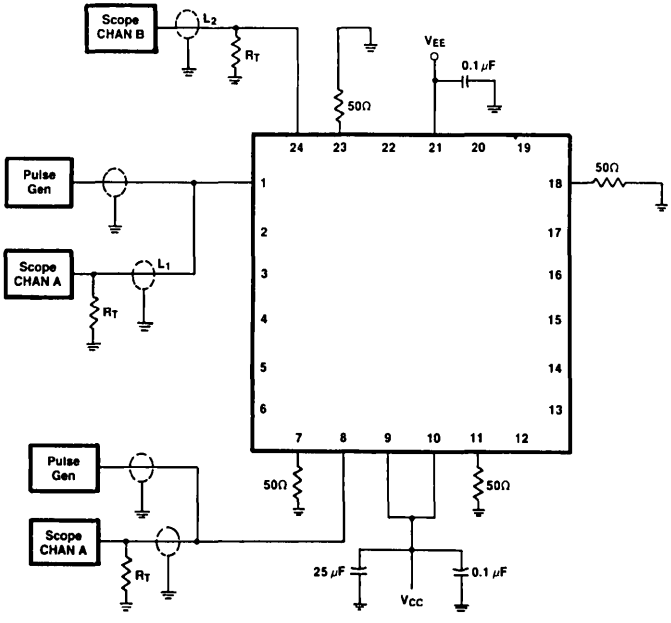
FIGURE 7. AC Test Circuit Differential Line to S_O



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines.
R_T = 50Ω terminator internal to scope.
Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
All unused outputs are loaded with 50Ω to GND.
C_L = fixture and stray capacitance ≤ 3 pF.
All differential line outputs on AC fixture should be cut open as close to the DUT as possible.

TL/F/9876–14

FIGURE 8. AC Test Circuit S_I to S_O and $\overline{E}$ to S_O

National Semiconductor

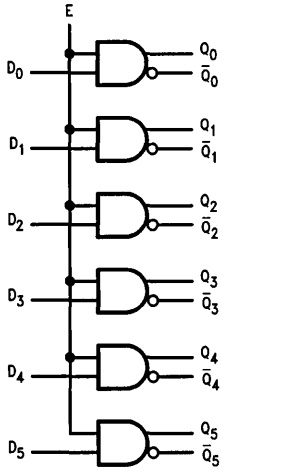
ADVANCE INFORMATION

F100324
Low Power Hex TTL-to-ECL Translator

General Description

The F100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The F100324 is pin and function compatible with the F100124 with similar AC performance but features power dissipation roughly half of the F100124 to ease system cooling requirements.

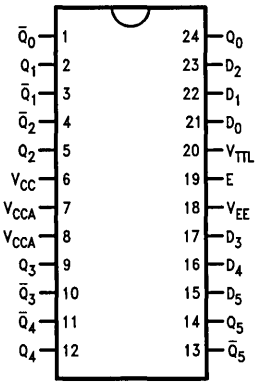
Logic Diagram



TL/F/9878-4

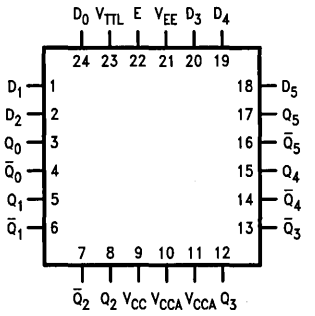
Connection Diagrams

24-Pin DIP



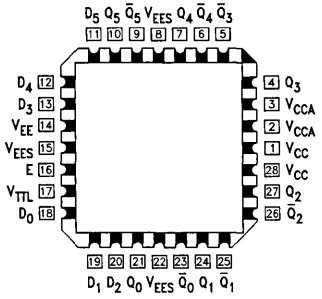
TL/F/9878-1

24-Pin Quad Cerpak



TL/F/9878-2

28-Pin PCC



TL/F/9878-3

National Semiconductor

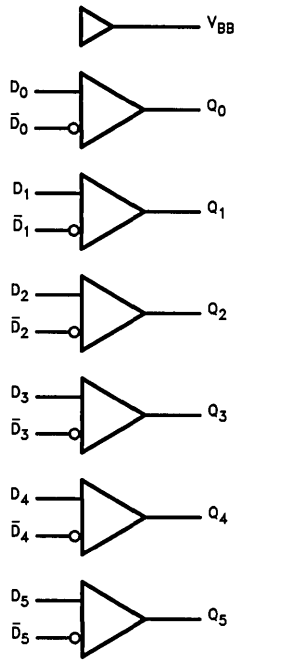
ADVANCE INFORMATION

F100325
Low Power Hex ECL-to-TTL Translator

General Description

The F100325 is a hex translator, designed to convert 100K ECL logic levels to TTL logic levels. The F100325 is pin and function compatible with the F100125 with similar AC performance but features power dissipation roughly half of the F100125 to ease system cooling requirements.

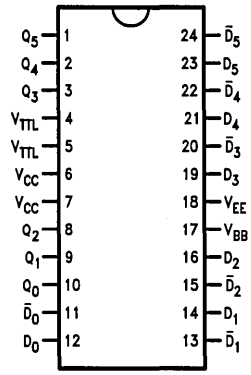
Logic Diagram



TL/F/9879-4

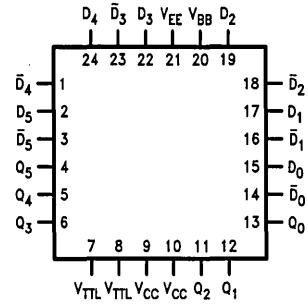
Connection Diagrams

24-Pin DIP



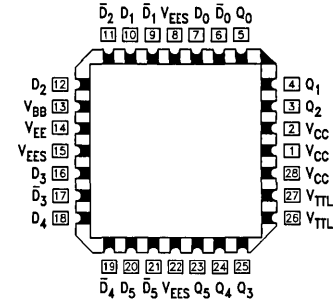
TL/F/9879-1

24-Pin Quad Cerpak



TL/F/9879-2

28-Pin PCC



TL/F/9879-3

National Semiconductor

ADVANCE INFORMATION

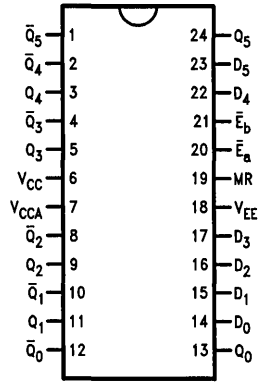
F100350
Low Power Hex D-Latch

General Description

The F100350 contains six D-type latches with true and complement outputs. The F100350 is pin and function compatible with the F100150 with similar AC performance but features power dissipation roughly two-thirds of the F100150 to ease system cooling requirements.

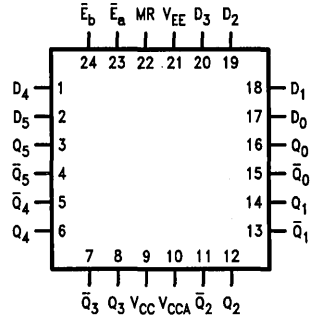
Connection Diagrams

24-Pin DIP



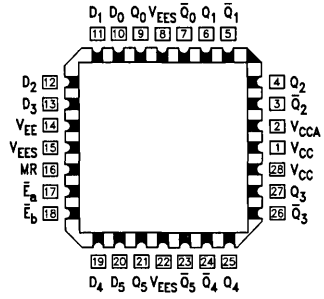
TL/F/9884-1

24-Pin Quad Cerpak



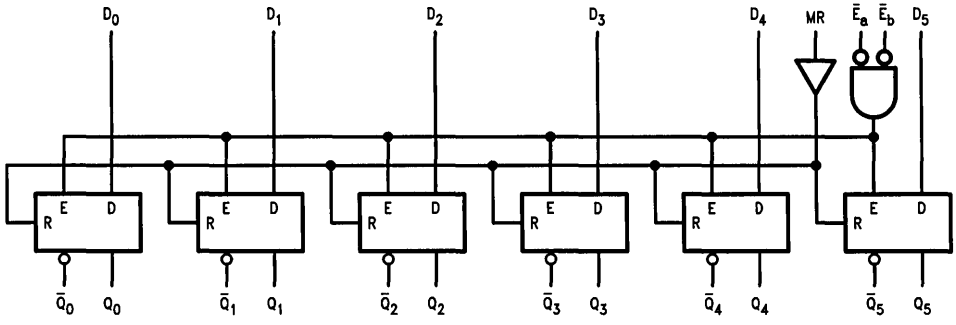
TL/F/9884-2

28-Pin PCC



TL/F/9884-3

Logic Diagram



TL/F/9884-4

National Semiconductor

ADVANCE INFORMATION

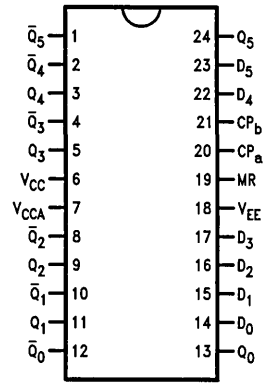
F100351
Low Power Hex D Flip-Flop

General Description

The F100351 contains six D-type flip-flops with true and complement outputs. The F100351 is pin and function compatible with the F100151 with similar AC performance but features power dissipation roughly two-thirds of the F100150 to ease system cooling requirements.

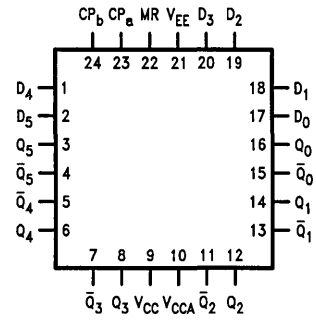
Connection Diagrams

24-Pin DIP



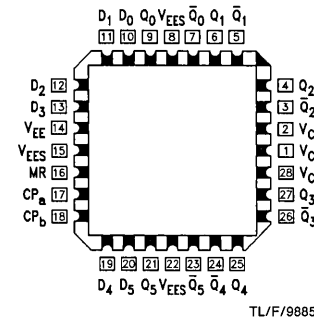
TL/F/9885-1

24-Pin Quad Cerpak



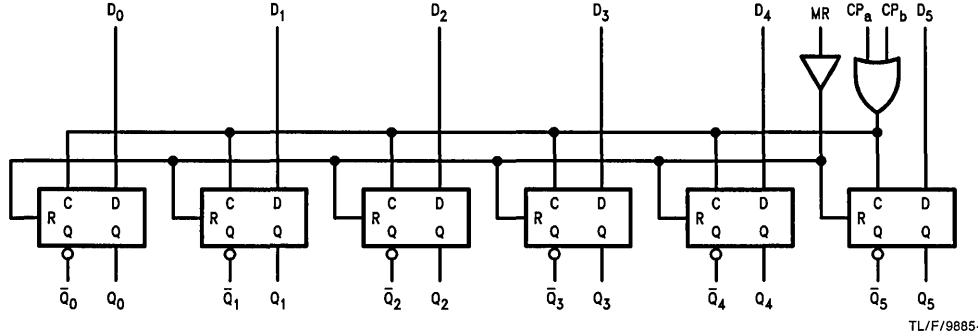
TL/F/9885-2

28-Pin PCC



TL/F/9885-3

Logic Diagram



TL/F/9885-4

2

Section 3

11C Datasheets

Section 3 Contents

National Semiconductor

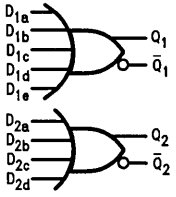
11C01
Dual 5-4 Input OR/NOR Gate

General Description

The 11C01 is a voltage-compensated ECL dual 5-4 input OR/NOR gate. The circuit has standard internal voltage compensation with DC parameters identical to 10K ECL devices.

Ordering Code: See Section 6

Logic Symbol

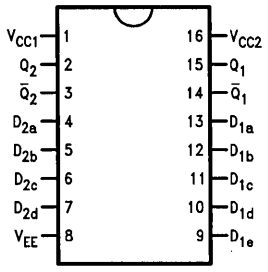


TL/F/9888–2

Pin Names	Description
D_{1a}–D_{1e}, D_{2a}–D_{2d}	Data Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

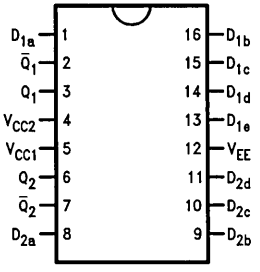
Connection Diagrams

16-Pin DIP



TL/F/9888–1

16-Pin Flatpak



TL/F/9888–3

Truth Tables

In					Out	
D_{1a}	D_{1b}	D_{1c}	D_{1d}	D_{1e}	Q_1	$\overline{Q}_1$
L	L	L	L	L	L	H
H	X	X	X	X	H	L
X	H	X	X	X	H	L
X	X	H	X	X	H	L
X	X	X	H	X	H	L
X	X	X	X	H	H	L

In				Out	
D_{2a}	D_{2b}	D_{2c}	D_{2d}	Q_2	$\overline{Q}_2$
L	L	L	L	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.5V to −4.75V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{EE})	−5.5	−5.2	−4.75	V
Ambient Temperature (T_A)	0		+75	°C

DC Electrical Characteristics

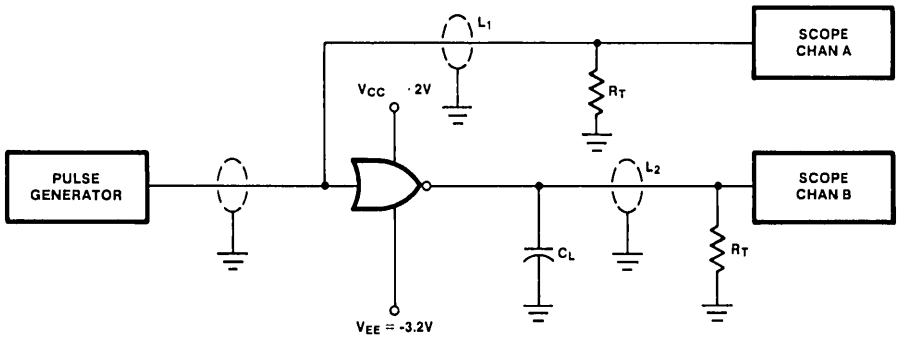
V_{EE} = −5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions	
V_{OH}	Output Voltage HIGH	−1000 −960 −900		−840 −810 −720	mV	0°C +25°C +75°C	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ per Truth Table	Loading is 50Ω to −2.0V
V_{OL}	Output Voltage LOW	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C +25°C +75°C		
V_{OHC}	Output Voltage HIGH	−1020 −980 −920			mV	0°C +25°C +75°C	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ per Truth Table	
V_{OLC}	Output Voltage LOW			−1645 −1630 −1605	mV	0°C +25°C +75°C		
V_{IH}	Input Voltage HIGH	−1145 −1105 −1045		−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs	
V_{IL}	Input Voltage LOW	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs	
I_{IH}	Input Current HIGH			350	μA	+25°C	V_{IN} = $V_{IH(Max)}$	
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = $V_{IL(Min)}$	
I_{EE}	Power Supply Current	−30	−24		mA	+25°C	Inputs and Outputs Open	

AC Electrical Characteristics

V_{EE} = −5.2V, T_A = +25°C

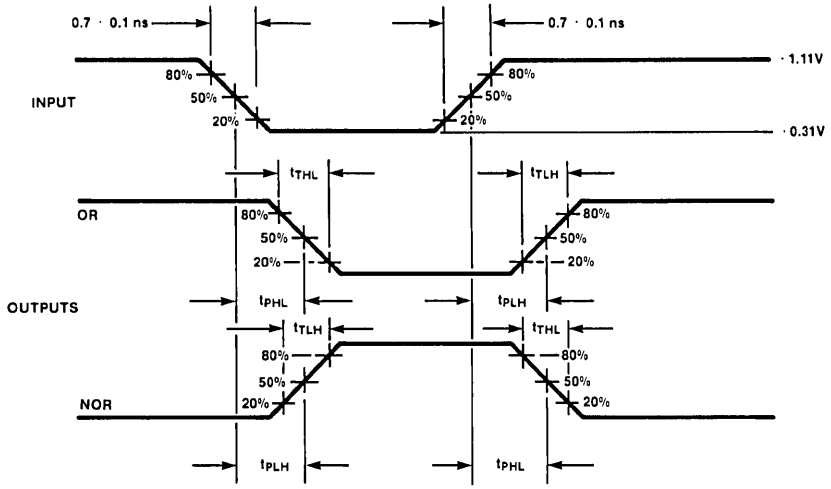
Symbol	Parameter	Flatpak			DIP			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
t_{PLH}	Propagation Delay LOW to HIGH	0.45	0.7	0.95	0.60	0.90	1.15	ns	See *Figure 1*
t_{PHL}	Propagation Delay HIGH to LOW	0.45	0.7	0.95	0.60	0.90	1.15	ns	
t_{TLH}	Output Transition Time LOW to HIGH (20% to 80%)		0.7	0.95		0.90	1.15	ns	
t_{THL}	Output Transition Time HIGH to LOW (80% to 20%)		0.7	0.95		0.90	1.15	ns	



TL/F/9888–4

Notes:

L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω Termination of scope
Decoupling 0.1 μF from GND to V_{EE} and V_{CC}
$C_L \leq 3$ pF



TL/F/9888–5

Notes:

Jig setup with no circuit under test
$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$

FIGURE 1. Switching Circuit and Waveforms

National Semiconductor

11C05
1 GHz Divide-By-Four Counter

General Description

The 11C05 is an ECL Divide-By-Four Counter with a maximum operating frequency above 1 GHz over the 0°C to +75°C temperature range. The input may be DC or AC (capacitively) coupled to the signal source. The emitter follower outputs (Q and $\overline{Q}$) are capable of driving 50Ω lines. The outputs are voltage-compensated and provide standard ECL output levels.

Ordering Code: See Section 6

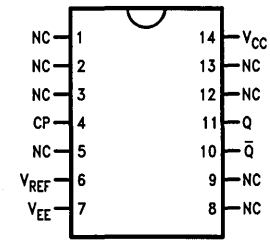
Logic Symbol

TL/F/9889–1

Pin Names	Description
CP	Clock Input
V_{REF}	Reference Input
Q, $\overline{Q}$	Counter Outputs

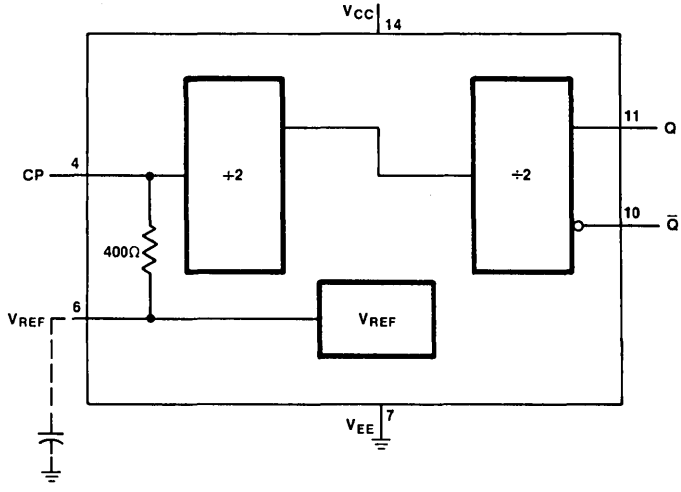
Connection Diagram

14-Pin DIP



TL/F/9889–2

Logic Diagram



TL/F/9889–3

Absolute Maximum Ratings

Above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.5V to −4.75V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})			
Commercial	−5.25V	−5.0V	−4.75V
Military	−5.5V	−5.0V	−4.75V
Ambient Temperature (T_A)			
Commercial	0°C		+75°C
Military	−55°C		+125°C

Commercial DC Electrical Characteristics

V_{EE} = 5.0V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1060 −1025 −980	−995 −960 −910	−910 −880 −830	mV mV mV	0°C +25°C +75°C	V_{IN} = V_{IH} or V_{IL}, Loading 50Ω to −2V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV	0°C to +75°C	
V_{IH}	Input Voltage HIGH	−2.45 −2.50 −2.60			V V V	0°C +25°C +75°C	Guaranteed Input HIGH
V_{IL}	Input Voltage LOW			−3.25 −3.30 −3.40	V V V	0°C +25°C +75°C	Guaranteed Input LOW
I_{EE}	Power Supply Current	−90	−65		mA	+25°C	Input Open
V_{EE}	Supply Voltage Range	−5.25	−5.0	−4.75	V	0°C to +75°C	
V_{REF}	Input Reference Voltage		−2.9		V	+25°C	

Military DC Electrical Characteristics

V_{EE} = −5.0V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1100 −980 −910	−1030 −910 −820	−950 −820 −720	mV mV mV	−55°C +25°C +125°C	V_{IN} = V_{IH} or V_{IL}, Loading 100Ω to −2V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV	−55°C to +125°C	
V_{IH}	Input Voltage HIGH	−2.35 −2.50 −2.70			V V V	−55°C +25°C +125°C	Guaranteed Input HIGH
V_{IL}	Input Voltage LOW			−3.15 −3.30 −3.50	V V V	−55°C +25°C +125°C	Guaranteed Input LOW
I_{EE}	Power Supply Current	−90	−65		mA	+25°C	Input Open
V_{EE}	Supply Voltage Range	−5.5	−5.0	−4.75	V	−55°C to +125°C	
V_{REF}	Input Reference Voltage		−2.9		V	+25°C	

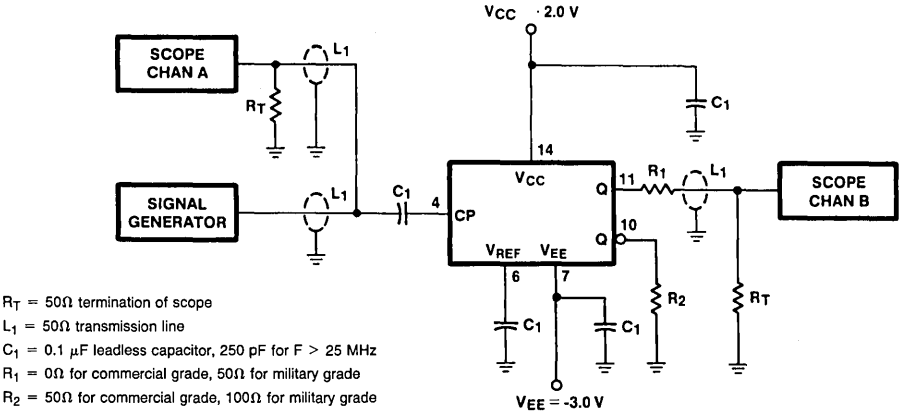
Commercial and Military AC Electrical Characteristics

V_{EE} = −5V, V_{CC} = GND, T_A −55°C to +125°C unless otherwise noted

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
f_{COUNT}	Maximum Sinusoidal Input Frequency	1000			MHz	0°C to +75°C	AC Coupled 800 mV Peak-to-Peak Input (Note 2)
		950				−55°C to +125°C	
f_{COUNT}	Minimum Sinusoidal Input Frequency		25		MHz		
SR_{MIN}	Slew Rate of Squareware		50		V/μs	(Note 1)	

Note 1: Very low frequency operation is possible as long as sufficient slew rate of the input pulse edges is maintained.

Note 2: Input drive shall not exceed 1.5V peak-to-peak max.

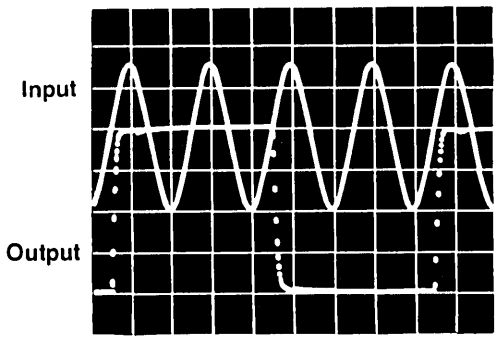


R_T = 50Ω termination of scope
L_1 = 50Ω transmission line
C_1 = 0.1 μF leadless capacitor, 250 pF for F > 25 MHz
R_1 = 0Ω for commercial grade, 50Ω for military grade
R_2 = 50Ω for commercial grade, 100Ω for military grade

TL/F/9889–4

FIGURE 1. AC Test Circuit

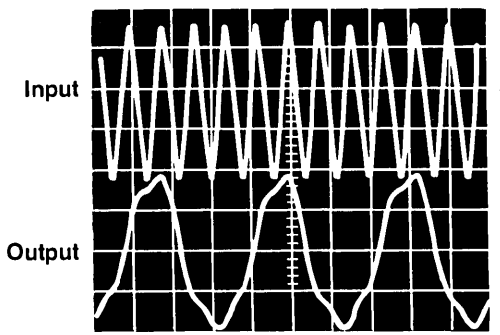
Horizontal Scale = ns/div
Vertical Scale = 200 mV/div



TL/F/9889–5

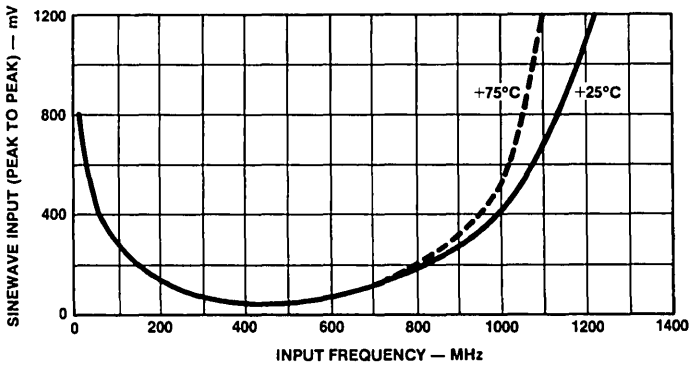
25 MHz Operation

Horizontal Scale = 1 ns/div
Vertical Scale = 200 mV/div



TL/F/9889–6

1.2 GHz Operation



TL/F/9889–7

FIGURE 2. AC Input Requirements

Note: Trigger amplitudes refer to the circuit end of the input cable as opposed to the signal generator end.

A DC coupled input should be designed to provide specified V_{IH} and V_{IL} levels. For AC coupling, an external resistor may or may not be necessary depending on the application. If an input signal is always present, only the capacitor is required because an internal 400Ω resistor connected between CP and V_{REF} centers the AC signal about mid-threshold. For applications in which an input signal is not always present, AC coupling requires that an external 10 KΩ resistor be connected between CP and V_{EE}. This offsets the input sufficiently to avoid extreme sensitivity to noise when no signal is present. Otherwise, noise triggering can lead to oscillation at about 450 MHz. For best operation, both outputs should be equally loaded.

National Semiconductor

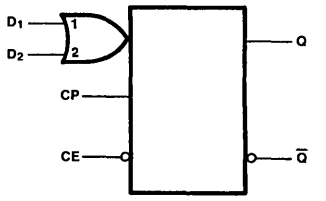
11C06
750 MHz D-Type Flip-Flop

General Description

The 11C06 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 750 MHz. Designed primarily for high-speed prescaling, it can also be used in any application which does not require preset inputs. The circuit is voltage-compensated, which makes input thresholds and output levels insensitive to V_{EE} variations. Complementary Q and $\overline{Q}$ outputs are provided, as are two Data inputs, Clock and Clock Enable inputs. The 11C06 is pin-compatible with the Motorola MC1690L but is a higher-frequency replacement.

Ordering Code: See Section 6

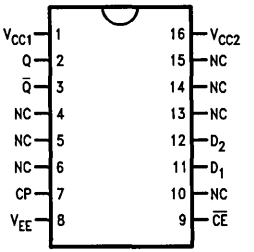
Logic Symbol



TL/F/9890-3

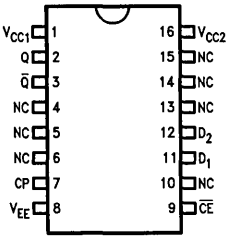
Connection Diagrams

16-Pin DIP



TL/F/9890-1

16-Pin Flatpak



TL/F/9890-2

Pin Names	Description
D_n	Data Input
CP	Clock Input
$\overline{CE}$	Clock Enable (Active LOW)
Q, $\overline{Q}$	Outputs

Truth Table

$\overline{CE}$	CP	D	Q_n
L	L	X	Q_{n-1}
L	H	X	Q_{n-1}
L	⌐	L	L
L	⌐	H	H
H	X	X	Q_{n-1}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW to HIGH Transition
Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.7V	−5.2V	−4.7V
Ambient Temperature (T_A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$ per Truth Table Loading 50Ω to −2V
		−960		−810	mV	+25°C	
		−900		−720	mV	+75°C	
V_{OL}	Output Voltage LOW	−1870		−1635	mV	0°C	
		−1850		−1620	mV	+25°C	
		−1830		−1595	mV	+75°C	
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$ for D_n Inputs Loading 50Ω to −2V
		−980			mV	+25°C	
		−920			mV	+75°C	
V_{OLC}	Output Voltage LOW			−1615	mV	0°C	
				−1600	mV	+25°C	
				−1575	mV	+75°C	
V_{IH}	Input Voltage HIGH	−1135		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs
		−1095		−810	mV	+25°C	
		−1035		−720	mV	+75°C	
V_{IL}	Input Voltage LOW	−1870		−1500	mV	0°C	Guaranteed Input Voltage LOW for All Inputs
		−1850		−1485	mV	+25°C	
		−1830		−1460	mV	+75°C	
I_{IH}	Input Current HIGH						V_{IN} = $V_{IH\ (Max)}$
	Clock Input			250	μA	+25°C	
	Data Input			270	μA	+25°C	
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = $V_{IH\ (Min)}$
I_{EE}	Power Supply Current	−59	−40		mA	+25°C	All Inputs Open

AC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND, T_A = +25°C

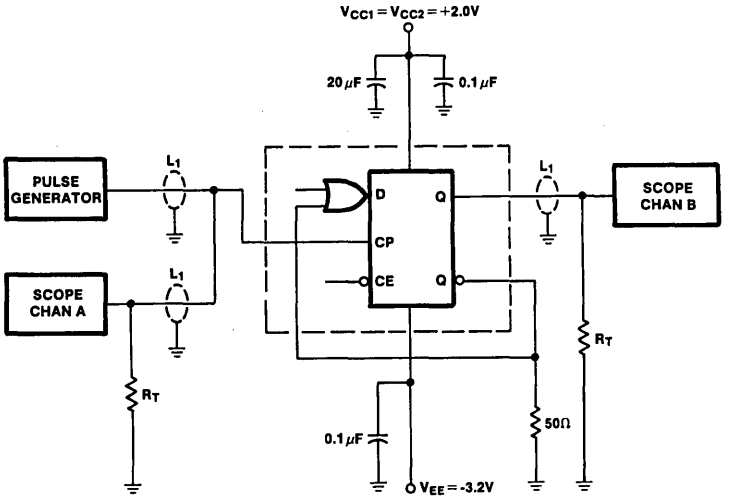
Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PHL}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	See *Figure 1*
t_{PHL}	Propagation Delay (CP-Q)	0.7	1.0	1.2	ns	
t_{TLH}	Transition Time 20% to 80%	0.5	0.8	1.0	ns	
t_{THL}	Transition Time 80% to 20%	0.5	0.8	1.0	ns	
t_S	Set-up Time		0.2		ns	
t_H	Hold Time		0.2		ns	
$f_{TOG\ (MAX)}$	Toggle Frequency (CP)	650	750		MHz	See *Figure 2*, Note

Note: The device is guaranteed for f_{TOG} (CP) ≥ 600 MHz, f_{TOG}(CE) ≥ 550 MHz over the 0°C to +75°C temperature range.

Functional Description

While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times.

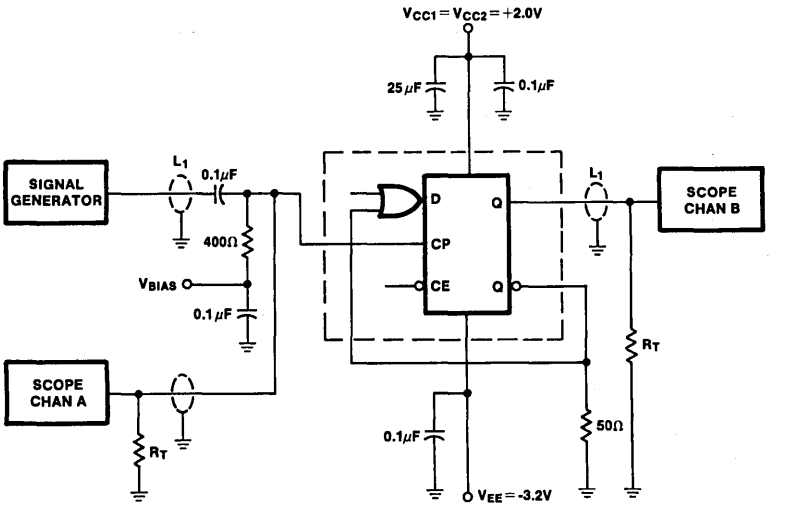
The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual-In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should go HIGH while CP is still HIGH.



TL/F/9890–4

R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
All input transition times are 2.0 ns ±0.2 ns

FIGURE 1. Propagation Delay (CP to Q)

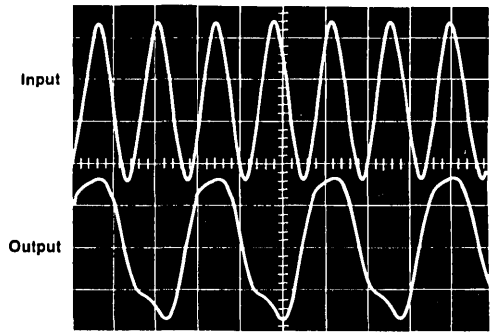


TL/F/9890–5

R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
Adjust V_{BIAS} for +0.7V baseline of 800 mV peak-to-peak sinewave input.
All input transition times are 2.0 ns ±0.2 ns

FIGURE 2. Toggle Frequency Test Circuit

Typical Waveforms



700 MHz Operation

TL/F/9890–6

Horizontal Scale = 1.0 ns/div
Vertical Scale = 200 mV/div

National Semiconductor

11C70
Master-Slave D-Type Flip-Flop

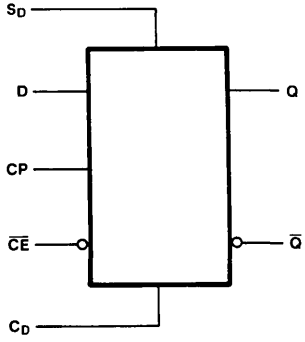
General Description

The 11C70 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 650 MHz. Designed primarily for communications and instrumentation, it can also be used in other digital applications and is fully compatible with 10K ECL. Asynchronous Direct Set and Direct Clear inputs are provided which override the clock.

The circuit is voltage-compensated, which makes output levels and input thresholds insensitive to V_{EE} variations. This also allows operation with ECL supply voltage V_{EE} of $-5.2V$ or with TTL supply V_{CC} of $+5.0V$. Each input has an internal 50 kΩ pull-down resistor, which allows unused inputs to be left open. Open emitter-follower outputs accommodate a variety of loading and terminating schemes. The 11C70 is pin-compatible with the Motorola MC1670 but is a higher-frequency replacement.

Ordering Code: See Section 6

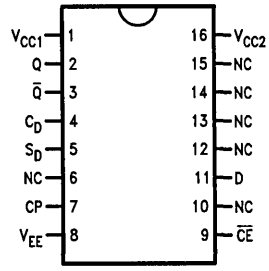
Logic Symbol



TL/F/9891–2

Connection Diagram

16-Pin DIP



TL/F/9891–1

Pin Names	Description
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse
D	Data Input
Q, $\overline{Q}$	Outputs
S_D	Direct Set
C_D	Direct Clear

Truth Table

Inputs					$Q_t + 1$	Operation
S_D	C_D	D	$\overline{CE}$	CP		
H	L	X	X	X	H	Direct Set
L	H	X	X	X	L	Direct Clear
H	H	X	X	X	—	Intermediate
L	L	X	H	⌐	Q_t	Disable Clock
L	L	H	L	⌐	H	Clocked Set
L	L	L	L	⌐	L	Clocked Clear

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW to HIGH Transition
t, t+1 = Time Before and After Clock Positive Transition

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Supply Voltage (V_{EE})	−5.7V	−5.2V	−4.7V
Ambient Temperature (T_A)	0°C		+75°C

DC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output Voltage HIGH	−1000 −960 −900		−840 −810 −720	mV mV mV	0°C +25°C +75°C	V_{IN} = V_{IHA} or V_{ILB} per Truth Table Loading 50Ω to −2V
V_{OL}	Output Voltage LOW	−1870 −1850 −1850		−1665 −1620 −1595	mV mV mV	0°C +25°C +75°C	
V_{OHC}	Output Voltage HIGH	−1020 −980 −920			mV mV mV	0°C +25°C +75°C	V_{IN} = V_{IHB} or V_{ILA} for D Input Loading 50Ω to −2V
V_{OLC}	Output Voltage LOW			−1615 −1600 −1575	mV mV mV	0°C +25°C +75°C	
V_{IH}	Input Voltage HIGH	−1135 −1095 −1035		−840 −810 −720	mV mV mV	0°C +25°C +75°C	Guaranteed Input Voltage HIGH for All Inputs
V_{IL}	Input Voltage LOW	−1870 −1850 −1830		−1500 −1485 −1460	mV mV mV	0°C +25°C +75°C	Guaranteed Input Voltage LOW for All Inputs
I_{IH}	Input Current HIGH Clock Input Data Input S_D and C_D			 250 270 550	 μA μA μA	+25°C	V_{IN} = V_{IHA}
I_{IL}	Input Current LOW	0.5			μA	+25°C	V_{IN} = V_{IHB}
I_{EE}	Power Supply Current	−48			mA	+25°C	All Inputs Open

AC Electrical Characteristics

V_{EE} = −5.2V, V_{CC} = GND, T_A = +25°C

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH}, t_{PHL}	Propagation Delay (CP-Q)		1.1	1.4	ns	See *Figures 3* and *4*
t_{PLH}, t_{PHL}	Propagation Delay (S_D-$\overline{Q}$, C_D-Q)		1.3	1.7	ns	
t_{TLH}	Transition Time 20% to 80%		0.9	1.3	ns	
t_{THL}	Transition Time 80% to 20%		0.9	1.3	ns	
$f_{TOG\ (MAX)}$	Toggle Frequency (CP)	550	650		MHz	See *Figure 2*

Note: This device is guaranteed for $f_{TOG(max)} \geq$ 500 MHz over the 0°C to +75°C temperature range.

Functional Description

Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times. While the clock is LOW, the slave is in a HOLD condition and information present on the D input is gated into the master. When the clock goes HIGH, it locks the master into its present state, making it insensitive to the D input, causing the new information to appear on the outputs.

The CP and $\overline{CE}$ inputs are logically identical, but physical constraints associated with the Dual In-Line package make the $\overline{CE}$ input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, $\overline{CE}$ should be HIGH while CP is still HIGH.

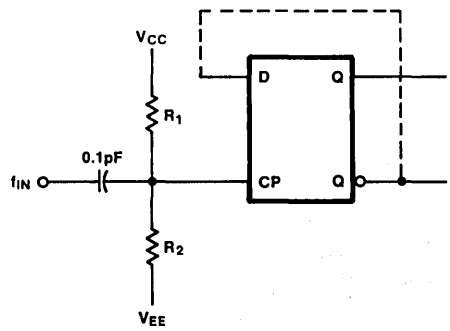
A HIGH signal on S_D or C_D will override the clocked inputs and force Q or $\overline{Q}$, respectively, to go HIGH. If both C_D and S_D are HIGH, the two output voltages will be somewhere between the HIGH and LOW levels and thus, cannot be usefully defined.

When the input signals for the 11C70 come from other ECL circuits, either 11CXX series or 10K types, these circuits will automatically provide appropriate signal swings, provided, of course, that these circuits are operated within their ratings and that due consideration is given to terminations appropriate to the particular application, as discussed in the F100K ECL Design Guide (Section 5 of Databook).

For applications where the clock signal comes from a circuit type other than ECL (in high frequency prescaling, for example) it is generally necessary to use external components to shift the signal levels and center them about the 11C70 input threshold region. A typical biasing scheme is shown in *Figure 1*. Resistors R1 and R2 are chosen such that the quiescent voltage at the CP input is −1.3V with respect to the V_{CC} terminal of the 11C70. Also indicated is the coupling from $\overline{Q}$ back to the D input to make a simple toggle. The clock source should be designed to provide a signal swing in the range of 400 mV to 1200 mV, peak-to-peak, over the specified frequency and temperature range. To avoid saturating the input transistor, and thus limiting the frequency capability, the positive peak of the clock should not be more positive than −0.4V with respect to V_{CC}.

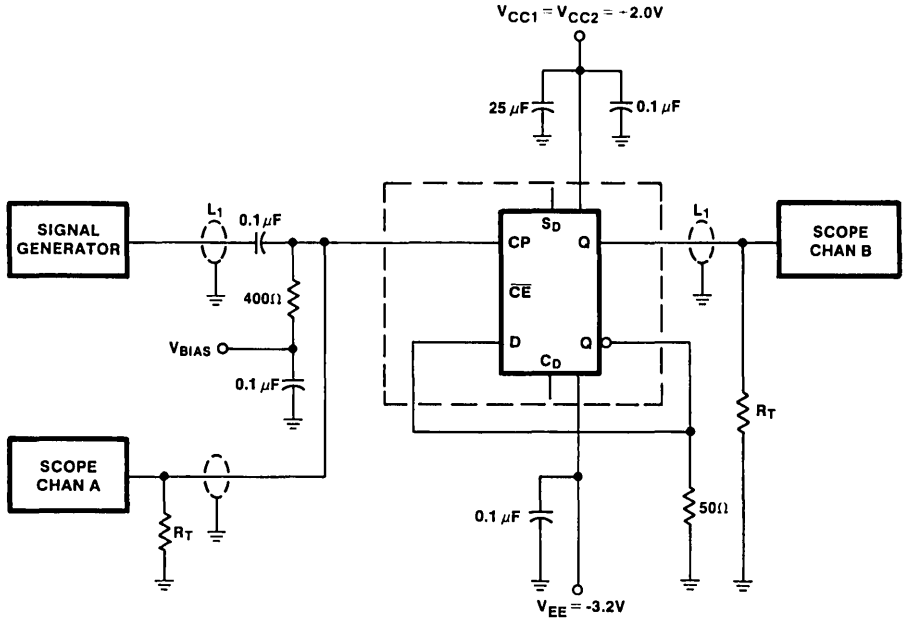
The 11C70 outputs have no internal pull-down resistors. When driving a microstrip line terminated at the far end by a resistor returned to −2V (w.r.t. V_{CC}), the quiescent I_{OH} current in the line performs the pull-down function when the output starts to go LOW. For series termination or for short unterminated lines, a 270Ω resistor to V_{EE} will provide adequate pull-down current. The outputs switch slightly faster when both outputs are equally loaded than if only one output is loaded. Equal and opposite changes in Q and $\overline{Q}$ load currents tend to cancel the effects of the small inductance of the V_{CC} pin.

The test arrangements illustrate the use of split power supplies, with a 2V V_{CC} and −3.2V V_{EE}. This is done as a matter of instrumentation convenience, since it allows the outputs to be connected via 50Ω cables directly to the sampling scope inputs, which have 50Ω internal terminations. By thus avoiding the use of probes, test correlation problems between supplier and user are minimized. In actual applications, only a single power supply is needed, and ground can be assigned to V_{CC}, as in ECL systems or to V_{EE} side as in TTL systems. RF bypass capacitors are recommended in either case.



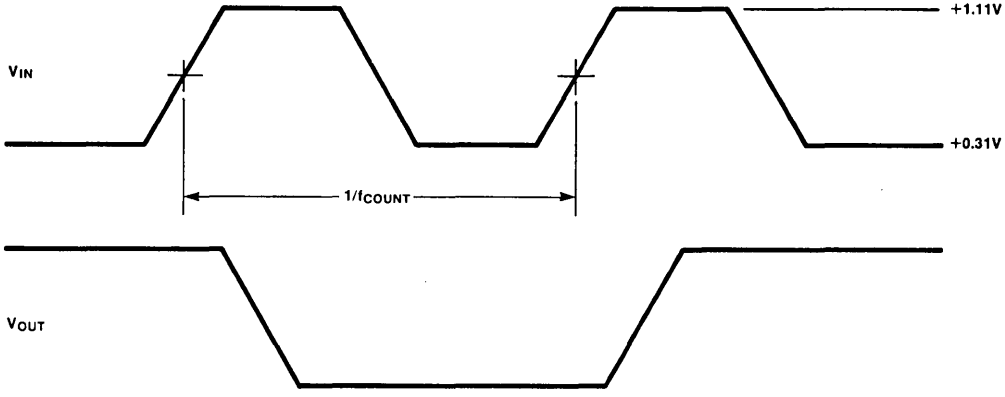
TL/F/9891–3

FIGURE 1. Input Biasing for AC Coupled Triggering



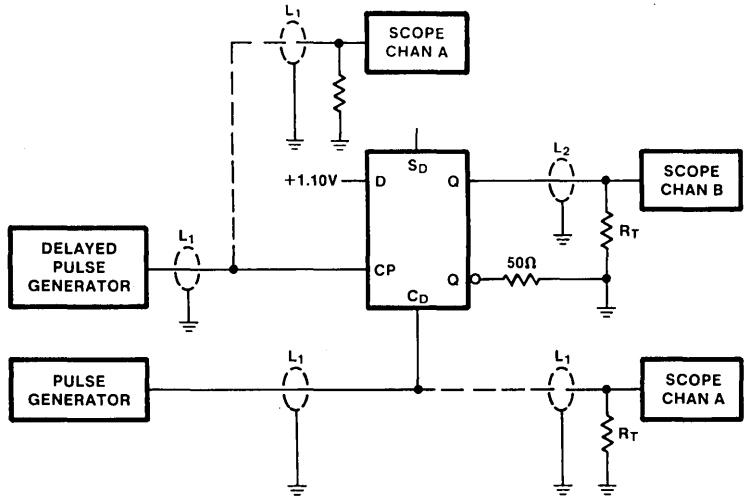
TL/F/9891–4

R_T = 50Ω termination of scope
L_1 = 50Ω impedance lines
Adjust V_{BIAS} for ±0.7V baseline of 800 mV peak-to-peak sinewave input



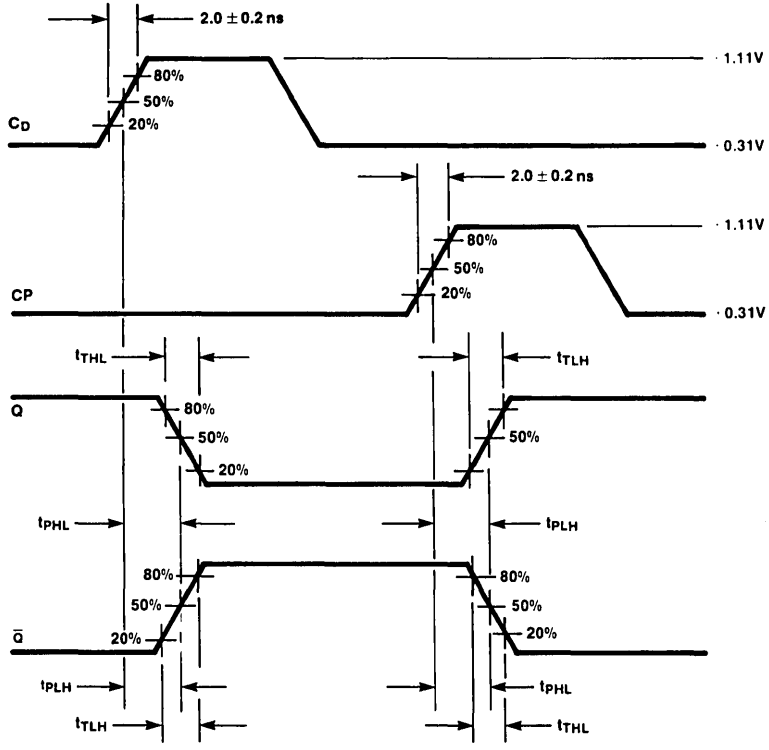
TL/F/9891–5

FIGURE 2. Toggle Frequency Test Circuit



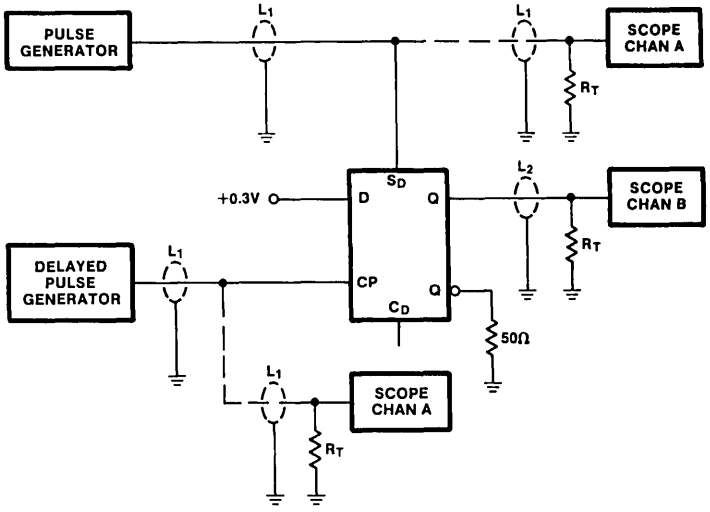
TL/F/9891–6

$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$
$R_T = 50\Omega$ termination of scope
L_1, L_2 = equal 50Ω impedance lines
All input transition times are 2.0 ns ±0.2 ns



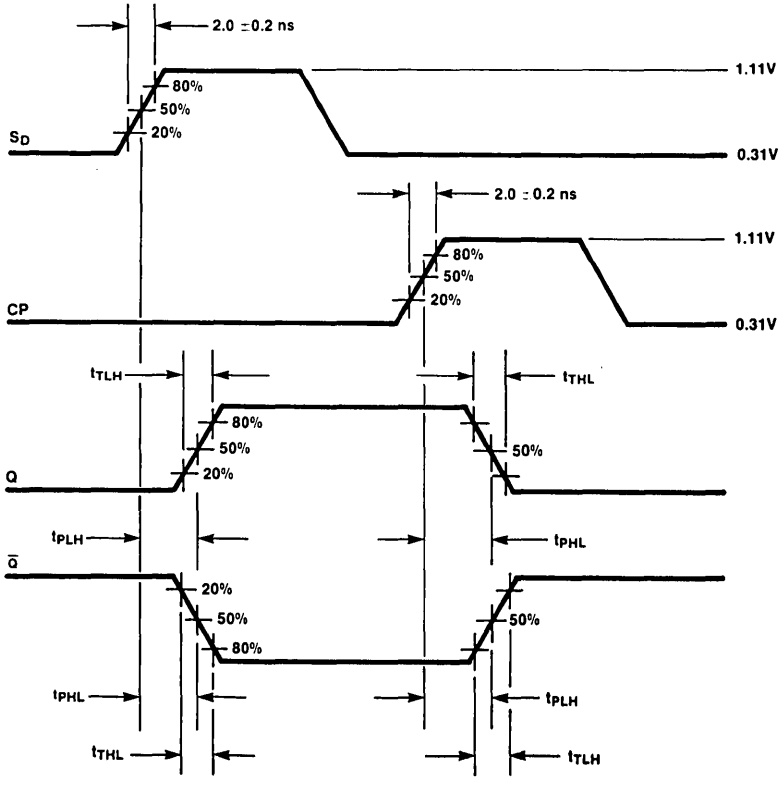
TL/F/9891–7

FIGURE 3. Propagation Delay and C_D Test Circuit



TL/F/9891–8

$V_{CC1} = V_{CC2} = +2.0V$
$V_{EE} = -3.2V$
$R_T = 50\Omega$ termination of scope
L_1, L_2 = equal 50Ω impedance lines
All input transition times are 2.0 ns ±0.2 ns



TL/F/9891–9

FIGURE 4. Propagation Delay and S_D Test Circuit

National Semiconductor

11C90/11C91
650 MHz Prescalers

General Description

The 11C90 and 11C91 are high-speed prescalers designed specifically for communication and instrumentation applications. All discussions and examples in this data sheet are applicable to the 11C91 as well as the 11C90.

The 11C90 will divide by 10 or 11 and the 11C91 by 5 or 6, both over a frequency range from DC to typically 650 MHz. The division ratio is controlled by the Mode Control. The divide-by-10 or -11 capability allows the use of pulse swallowing techniques to control high-speed counting modulos by lower-speed circuits. The 11C90 may be used with either ECL or TTL power supplies.

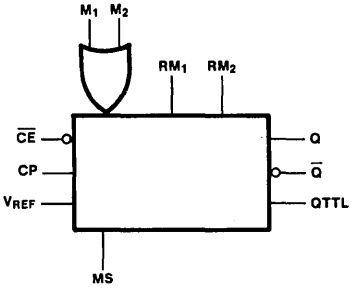
In addition to the ECL outputs Q and $\overline{Q}$, the 11C90 contains an ECL-to-TTL converter and a TTL output. The TTL output operates from the same V_{CC} and V_{EE} levels as the counter, but a separate pin is used for the TTL circuit V_{EE}. This minimizes noise coupling when the TTL output switches and also allows power consumption to be reduced by leaving the separate V_{EE} pin open if the TTL output is not used.

To facilitate capacitive coupling of the clock signal, a 400Ω resistor (V_{REF}) is connected internally to the V_{BB} reference. Connecting this resistor to the Clock Pulse input (CP) automatically centers the input about the switching threshold. Maximum frequency operation is achieved with a 50% duty cycle.

Each of the Mode Control inputs is connected to an internal 2 kΩ resistor with the other end uncommitted (RM_1 and RM_2). An M input can be driven from a TTL circuit operating from the same V_{CC} by connecting the free end of the associated 2 kΩ resistor to V_{CCA}. When an M input is driven from the ECL circuit, the 2 kΩ resistor can be left open or, if required, can be connected to V_{EE} to act as a pull-down resistor.

Ordering Code: See Section 6

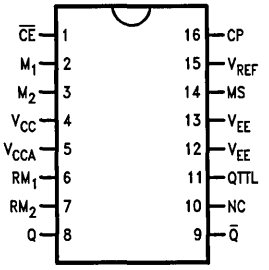
Logic Symbol



TL/F/9892–2

Connection Diagram

16-Pin DIP



TL/F/9892–1

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input
M_n	Count Modulus Control Input
MS	Asynchronous Master Set Input
Q, $\overline{Q}$	ECL Outputs
QTTL	TTL Output
RM_n	2 kΩ Resistor to M_n
V_{REF}	400Ω Resistor to V_{BB}

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Supply Voltage Range	−7.0V to GND
Input Voltage (DC)	V_{EE} to GND
Output Current (DC Output HIGH)	−50 mA
Operating Range	−5.7V to −4.7V
Lead Temperature (Soldering, 10 sec.)	300°C

Recommended Operating Conditions

	Min	Typ	Max
Ambient Temperature (T_A)			
Commercial	0°C		+75°C
Military	−55°C		+125°C
Supply Voltage (V_{EE})			
Commercial	−5.7V	−5.2V	−4.7V
Military	−5.7V	−5.2V	−4.7V

TTL Input/Output Operation

DC Electrical Characteristics

Over Operating Temperature and Voltage Range unless otherwise noted, Pins 12 and 13 = GND

Symbol	Parameter	Min	Typ (Note 3)	Max	Units	Conditions
V_{IH}	Input HIGH Voltage M_1 and M_2 Inputs		4.1		V	Guaranteed Input HIGH Threshold Voltage (Note 4), $V_{CC} = V_{CCA} = 5.0V$
V_{IL}	Input LOW Voltage M_1 and M_2 Inputs		3.3		V	Guaranteed Input LOW Threshold Voltage (Note 4), $V_{CC} = V_{CCA} = 5.0V$
V_{OH}	Output HIGH Voltage QTTL Output	2.3	3.3		V	$V_{CC} = V_{CCA} =$ Min, $I_{OH} = -640\ \mu A$
V_{OL}	Output LOW Voltage QTTL Output		0.2	0.5	V	$V_{CC} = V_{CCA} =$ Min, $I_{OL} = 20.0$ mA
I_{IL}	Input LOW Current M_1 and M_2 Inputs		−2.3	−5.0	mA	$V_{CC} = V_{CCA} =$ Max, $V_{IN} = 0.4V$, Pins 6, 7 = V_{CC}
I_{SC}	Output Short Circuit Current	−20	−35	−80	mA	$V_{CC} = V_{CCA} =$ Max, $V_{OUT} = 0.0V$, Pin 14 = V_{CC}

AC Electrical Characteristics

$V_{CC} = V_{CCA} = 5.0V$ Nominal, V_{EE} = GND, $T_A = +25°C$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to QTTL	6	10	14	ns	See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to QTTL		12	17	ns	
t_s	Mode Control Setup Time	4	2		ns	
t_h	Mode Control Hold Time	0	−2		ns	
t_{TLH}	Output Rise Time (20% to 80%)		10		ns	
t_{THL}	Output Fall Time (80% to 20%)		2		ns	
f_{MAX}	Count Frequency	550 600	650 650		MHz	−55°C to +125°C 0°C to +75°C Clock Input AC Coupled 350 mV Peak-to-Peak Sinewave (Note 5)

ECL Operation—Commercial Version

DC Electrical Characteristics

$V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output HIGH Voltage Q and $\overline{Q}$	−1060 −1025 −980	−995 −960 −910	−905 −880 −805	mV	0°C +25°C +75°C	Load = 50Ω to −2V
V_{OL}	Output LOW Voltage Q and $\overline{Q}$	−1820	−1705	−1620	mV	0°C to +75°C	
V_{IH}	Input HIGH Voltage	−1135 −1095 −1035		−840 −810 −720	mV	0°C +25°C +75°C	Guaranteed Input HIGH Signal (Note 6)
V_{IL}	Input LOW Voltage	−1870 −1850 −1830		−1500 −1485 −1460	mV	0°C +25°C +75°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input (Note 1) MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110 −119	−75		mA	0°C to +75°C	Pins 6, 7, 13 not connected
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	0°C to +75°C	
V_{REF}	Reference Voltage	−1550		−1150	mV	+25°C	$V_{RM_1} = V_{RM_2} = -5.2V$ $I_N = -10.0\ \mu A$

AC Electrical Characteristics

$T_A = 0°C$ to +75°C, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	0°C Typ	+25°C Min	+25°C Typ	+25°C Max	+75°C Typ	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to Q	1.8	1.3	2.0	3.0	2.5	ns	Output: R_L = 50Ω to −2.0V Input: $t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20% to 80%) See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to Q	3.7		4.0	6.0	4.5	ns	
t_s	Setup Time, M to CP	2.0	4.0	2.0		2.0	ns	
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	
t_{TLH}	Output Rise Time (20% to 80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80% to 20%)	1.0		1.0	2.0	1.0	ns	
f_{MAX}	Maximum Clock Frequency	650	600	650		625	MHz	AC Coupled Input 350 mV Peak-to-Peak. f_{MAX} is Guaranteed to be 575 MHz Min at 0°C to +75°C.

ECL Operation—Military Version

DC Electrical Characteristics

$V_{CC} = V_{CCA} = GND, V_{EE} = -5.2V$

Symbol	Parameter	Min	Typ	Max	Units	T_A	Conditions
V_{OH}	Output HIGH Voltage Q and $\overline{Q}$	−1100 −980 −910	−1030 −910 −820	−900 −820 −670	mV	−55°C +25°C +125°C	Load = 100Ω to −2V
V_{OL}	Output LOW Voltage Q and $\overline{Q}$	−1820	−1705	−1620	mV	−55°C to +125°C	
V_{IH}	Input HIGH Voltage	−1190 −1095 −975		−905 −810 −690	mV	−55°C +25°C +125°C	Guaranteed Input HIGH Signal (Note 6)
V_{IL}	Input LOW Voltage	−1890 −1850 −1800		−1525 −1485 −1435	mV	−55°C +25°C +125°C	Guaranteed Input LOW Signal
I_{IH}	Input HIGH Current CP Input (Note 1) MS Input M_1 and M_2 Input			 400 400 250	 μA	 +25°C +25°C +25°C	$V_{IN} = V_{IHA}$
I_{IL}	Input LOW Current	0.5			μA	+25°C	$V_{IN} = V_{ILB}$
I_{EE}	Power Supply Current	−110	−75		mA	+25°C	Pins 6, 7, 13 not connected
			−119		mA	−55°C to +125°C	
V_{EE}	Operating Supply Voltage Range	−5.7	−5.2	−4.7	V	−55°C to +125°C	
V_{REF}	Reference Voltage	−1550		−1150	mV	+25°C	$V_{RM_1} = V_{RM_2} = -5.2V$ $I_N = -10.0\ \mu A$

AC Electrical Characteristics

$T_A = -55°C$ to $+125°C$, $V_{CC} = V_{CCA} = GND$, $V_{EE} = -5.2V$

Symbol	Parameter	−55°C Typ	+25°C Min	+25°C Typ	+25°C Max	+125°C Typ	Units	Conditions
t_{PLH} t_{PHL}	Propagation Delay, (50% to 50%) CP to Q	1.5	1.3	2.0	3.0	3.0	ns	Output: $R_L = 50\Omega$ to −2.0V Input: $t_{ri} = t_{fi} = 2.0 \pm 0.1$ ns (20% to 80%) See *Figure 1*
t_{PLH}	Propagation Delay, (50% to 50%) MS to Q	3.5		4.0	6.0	5.0	ns	
t_s	Setup Time, M to CP	2.0	4.0	2.0		2.0	ns	
t_h	Hold Time, M to CP	−2.0	0.0	−2.0		−2.0	ns	
t_{TLH}	Output Rise Time (20% to 80%)	1.0		1.0	2.0	1.0	ns	
t_{THL}	Output Fall Time (80% to 20%)	1.0		1.0	2.0	1.0	ns	
f_{MAX}	Maximum Clock Frequency	700	600	650		600	MHz	AC Coupled Input 350 mV Peak-to-Peak. f_{MAX} is Guaranteed to be 550 MHz Min at −55°C to +125°C.

Note 1: Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

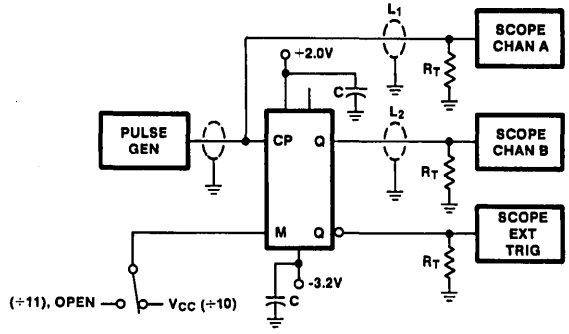
Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Typical limits are at $V_{CC} = 5.0V$ and $T_A = +25°C$.

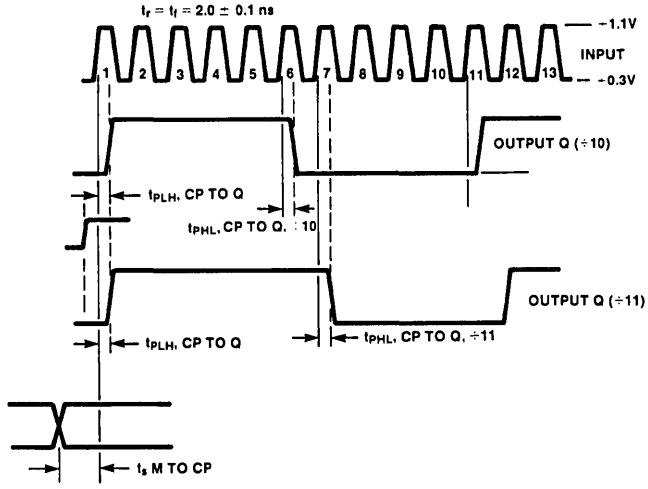
Note 4: The M_1 and M_2 threshold specifications are normally referenced to the V_{CC} potential, as shown in the ECL operation tables. Using V_{EE} (GND) as the reference, as in normal TTL practice, effectively makes the threshold vary directly with V_{CC}. Threshold is typically 1.3V below V_{CC} (e.g., +3.7V at $V_{CC} = +5V$). A signal swing about threshold of ±0.4V is adequate, which gives the state V_{IH} and V_{IL} values. The internal 2 kΩ resistors are intended to pull TTL outputs up to the required V_{IH} range, as discussed in the Functional Description and shown in *Figure 5.*

Note 5: TTL Output Signal swing is guaranteed at f_{MAX} over temperature range.

Note 6: M_1 or M_2 can be tied to V_{CC} for fixed divide-by-ten operation.



TL/F/9892-3



TL/F/9892-4

Conditions:

V_{CC} = +2.0V
V_{EE} = −3.2V
R_T = 50Ω (scope input impedance)
C_L = Jig and stray capacitance < 5.0 pF
l_1 = L_2 = equal 50Ω impedance lines
C = 0.1 pF

Note 7: Use high impedance to test QTTL.
Connect pin 13 to V_{EE}.

Note 8: For High frequency test use AC coupled input as in *Figure 3*.
Adjust input amplitude to 350 mV peak-to-peak.

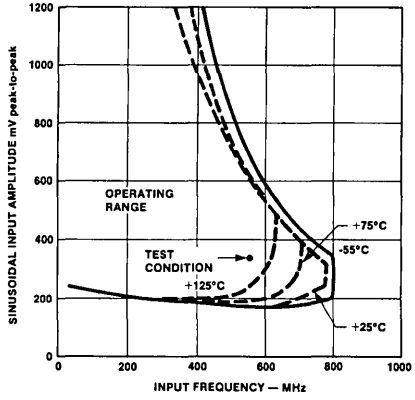
FIGURE 1. AC Test Circuit

Functional Description

The 11C90 contains four ECL Flip-Flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the Flip-Flops operate as a synchronous shift counter driving the fourth Flip-Flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

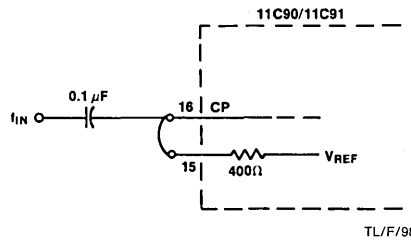
The feedback logic is such that the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a setup time before the clock that follows the HHLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the 11C90 output as its active edge. This gives an allowable delay of ten clock periods, minus the CP to Q delay of the 11C90 and the M to CP setup time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the previously mentioned delay and setup time.

Capacitively coupled triggering is simplified by the 400Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the CP input, as shown in *Figure 3*, the clock is automatically centered about the input threshold. A clock duty cycle of 50% provides the fastest operation, since the Flip-Flops are Master-Slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no maximum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in the graph labeled *Figure 2*. When the CP or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in *Figure 4*. Other ECL termination methods are discussed in the F100K ECL Design Guide (Section 5 of Databook).



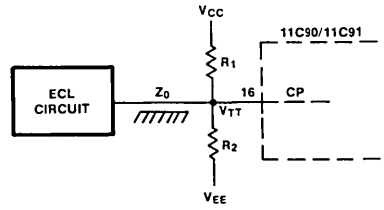
TL/F/9892-5

FIGURE 2. AC Coupled Triggering Characteristics



TL/F/9892-10

FIGURE 3. Capacitively Coupled Clocking



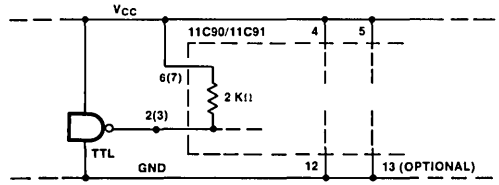
TL/F/9892-11

$Z_O\Omega$	50	75	100
$R_1\Omega$	80.6	121	162
$R_2\Omega$	130	196	261

V_{EE} = −5.2V, V_{CC} = 0V, V_{TT} = −2.0V

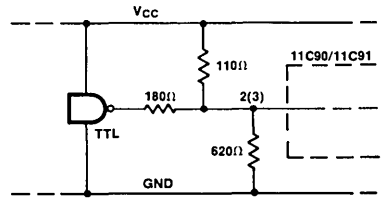
FIGURE 4. Clocking by ECL Source via Terminated Line

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 kΩ resistor can be used to pull the TTL output up as shown in *Figure 5*. Some types of TTL outputs will only pull up to within two diode drops of V_{CC}, which is not high enough for 11C90 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in *Figure 6*.



TL/F/9892-12

FIGURE 5. Using Internal Pull-Up with TTL Source



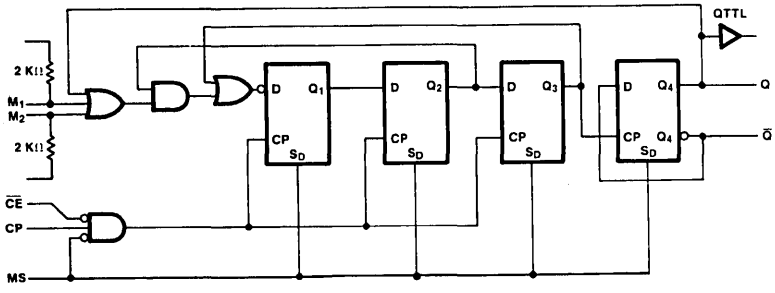
TL/F/9892-13

FIGURE 6. Faster Low Impedance TTL to ECL Interface

Functional Description (Continued)

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270Ω to 510Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and RF bypass capacitors are recommended to prevent crosstalk.

Logic Diagram 11C90



TL/F/9892-6

Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

Count Sequence Table 11C90

	Q_1	Q_2	Q_3	Q_4(QTTL)	
	H	H	H	H	÷11
÷10	L	H	H	H	
	L	L	H	H	
	L	L	L	H	
	H	L	L	H	
	H	H	L	H	
	L	H	H	L	
	L	L	H	L	
	L	L	L	L	
	H	L	L	L	
	H	H	L	L	

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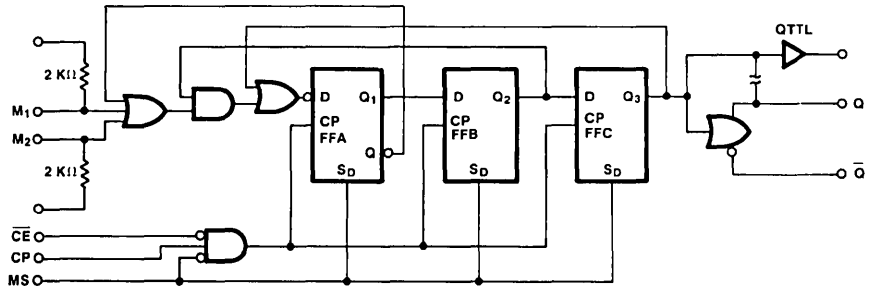
Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C90

Inputs				Output Response
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	X	÷10
L	L	X	H	÷10

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Logic Diagram 11C91



TL/F/9892–8

Count Sequence Table 11C91

	Q_1	Q_2	Q_3(QTTL)	
	H	H	H	÷6
÷5	L	H	H	
	L	L	H	
	L	L	L	
	H	L	L	
	H	H	L	

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Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C91

Inputs				Output Response
MS	$\overline{CE}$	M_1	M_2	
H	X	X	X	Set HIGH
L	H	X	X	Hold
L	L	L	L	÷6
L	L	X	H	÷5
L	L	H	X	÷5

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Section 4

10K and 100K Memory Datasheets

This section contains first page only of datasheets previously found in the F100K ECL Databook. For complete information on these and other ECL memory devices, refer to the National Memory Databook (Lit# 400088).

Section 4 Contents

National Semiconductor

10145A
16 x 4 Register File (Random Access Memory)

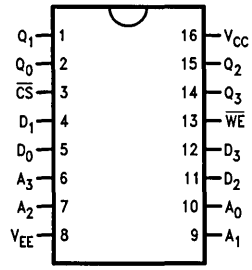
General Description

The 10145A is a high-speed 64-bit Random Access Memory organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data bussing are facilitated by the output disabling features of the Chip Select (CS) and Write Enable (WS) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Connection Diagram

16-Pin Ceramic Dual-in-Line Package



TL/D/9742–2

Top View

Order Number 10145ADC
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-In

Pin Names

$\overline{CS}$	Chip Select
A_0–A_3	Address
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enables
Q_0–Q_3	Data Outputs

National Semiconductor

10402 16 x 4-Bit Register File (Random Access Memory)

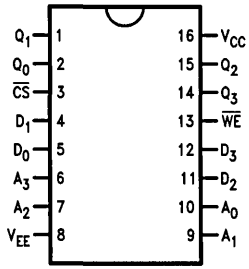
General Description

The 10402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) inputs.

A HIGH signal on $\overline{CS}$ prevents read and write operations and forces the outputs to the LOW state. When $\overline{CS}$ is LOW, the $\overline{WE}$ input controls chip operations. A HIGH signal on $\overline{WE}$ disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on $\overline{WE}$ forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, i.e., the memory is non-inverting.

Connection Diagrams

16-Pin Ceramic Dual-In-Line Package



TL/D/9640-2

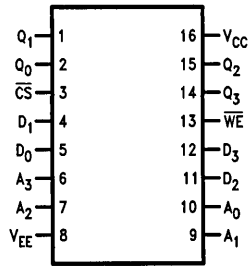
Top View

Order Number 10402DC
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Flatpack



TL/D/9640-3

Top View

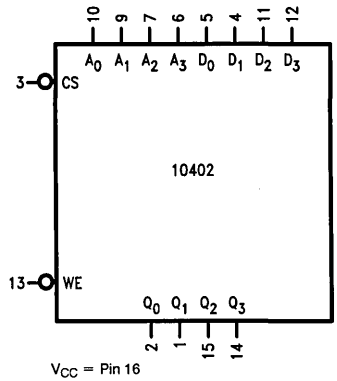
Order Number 10402FC
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Pin Names

$\overline{CS}$	Chip Select Input
A_0–A_3	Address Inputs
D_0–D_3	Data Inputs
$\overline{WE}$	Write Enable Input
Q_0–Q_3	Data Outputs



V_{CC} = Pin 16
V_{EE} = Pin 8

TL/D/9640-1

FIGURE 1. Logic Symbol

National Semiconductor

10415 1024 x 1-Bit Static Random Access Memory

General Description

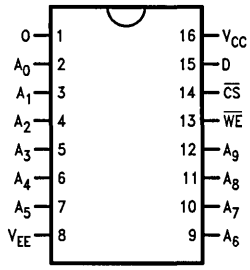
The 10415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-LOW Chip Select line.

Features

- Address access time—10 ns max
- Chip select access time—5 ns max
- Open-emitter output for easy memory expansion
- Power dissipation—0.92 mW/Bit Typ
- Power dissipation decreases with increasing temperature
- Polyimide die coat for alpha immunity

Connection Diagrams

16-Pin Ceramic Dual-In-Line Package



TL/D/9641-2

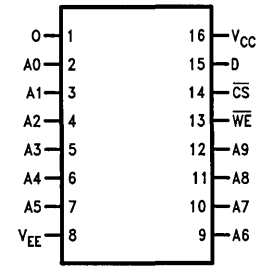
Top View

Order Number 10415DC10
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

16-Pin Ceramic Flatpack



TL/D/9641-11

Top View

Order Number 10415FC10
See NS Package Number W16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

National Semiconductor

10422 256 x 4-Bit Static RAM 10 ns, 7 ns, 5 ns

General Description

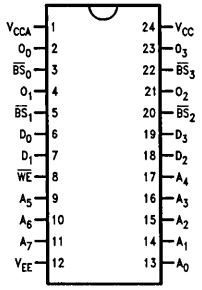
The 10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control, and buffer storage applications. The device features full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as four active-LOW Bit Select lines.

Features

- Address access time—5 ns/7 ns/ 10 ns Max
- Bit select access time—4 ns/5 ns/5 ns Max
- Four bits can be independently selected
- Open-emitter outputs for easy memory expansion
- Polyimide die coat for alpha immunity

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



TL/D/9642-2

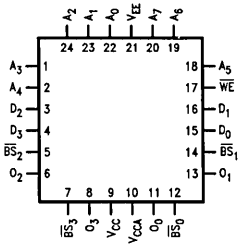
Top View

Order Number 10422DC5, 10422DC7 or 10422DC10
See NS Package Number J24E*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-in

24-Pin Flatpak



TL/D/9642-3

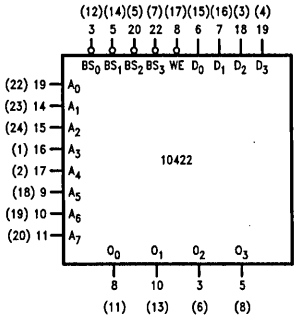
Top View

Order Number 10422FC5, 10422FC7 or 10422FC10
See NS Package Number W24B*

*For most current package information, contact product marketing.

Optional Processing
QR = Burn-in

Logic Symbol



TL/D/9642-1

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

Symbol	Description
$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0$–$\overline{BS}_3$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

National Semiconductor

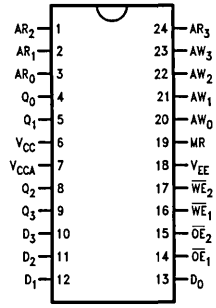
100145 16 x 4-Bit Register File Random Access Memory

General Description

The 100145 is a 64-bit register file organized as 16 words of four bits each. Separate address inputs for Read (AR_n) and Write (AW_n) operations reduce overall cycle time by allowing one address to be setting up while the other is being executed. Operating speed is also enhanced by four output latches which store data from the previous read operation while writing is in progress. When both Write Enable ($\overline{WE}$) inputs are LOW, the circuit is in the Write mode and the latches are in a Hold mode. When either $\overline{WE}$ input is HIGH, the circuit is in the Read mode, but the outputs can be forced LOW by a HIGH signal on either of the Output Enable ($\overline{OE}$) inputs. This makes it possible to tie one $\overline{WE}$ input and one $\overline{OE}$ input together to serve as an active-LOW Chip Select ($\overline{CS}$) input. When this wired $\overline{CS}$ input is HIGH, reading will still take place internally and the resulting data will enter the latches and become available as soon as the $\overline{CS}$ signal goes LOW, provided that the other $\overline{OE}$ input is LOW. A HIGH signal on the Master Reset (MR) input overrides all other inputs, clears all cells in the memory, resets the output latches, and forces the outputs LOW.

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



TL/D/9638-1

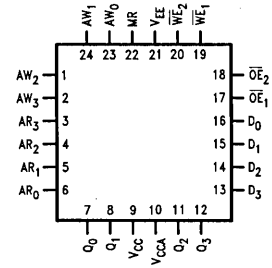
Top View

Order Number 100145DC
See NS Package Number J24E*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

24-Pin Ceramic Flatpak



TL/D/9638-2

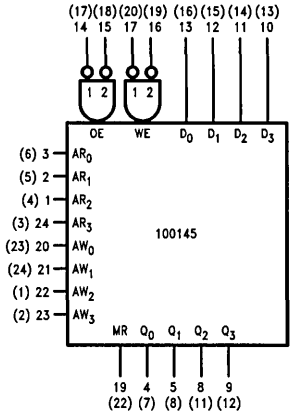
Top View

Order Number 100145FC
See NS Package Number W24B*

Optional Processing QR = Burn-In

*For most current package information, contact product marketing.

Logic Symbol



TL/D/9638-3

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

AR_0–AR_3	Read Address Inputs
AW_0–AW_3	Write Address Inputs
$\overline{WE}_1$, $\overline{WE}_2$	Read Enable Inputs (Active LOW)
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)
D_0–D_3	Data Inputs
MR	Master Reset Input
Q_0–Q_3	Data Outputs

4

National Semiconductor

100415 1024 x 1-Bit Random Access Memory

General Description

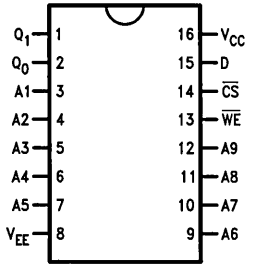
The 100415 is a 1024-bit read/write Random Access Memory (RAM), organized as 1024 words by one bit per word and designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as an active-LOW Chip Select line.

Features

- Address access time—10 ns max
- Chip select access time—5.0 ns max
- Open-emitter output for easy memory expansion
- Power dissipation—0.79 mW/bit typ
- Power dissipation decreases with increasing temperature
- Polyamide die coat for alpha immunity

Connection Diagrams

16-Pin Ceramic Flatpak

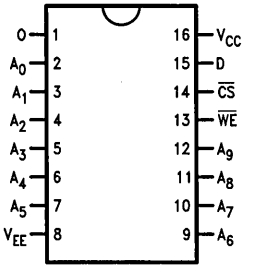


TL/D/9639–11

Top View

Order Number 100415FC10
See NS Package Number W16A*

16-Pin Ceramic Dual-In-Line Package



TL/D/9639–2

Top View

Order Number 100415DC10
See NS Package Number J16A*

*For most current package information, contact product marketing.

Optional Processing QR = Burn-In

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{CS}$	Chip Select Input (Active LOW)
A_0–A_9	Address Inputs
D	Data Input
O	Data Output

National Semiconductor

100422 256 x 4-Bit Static RAM 10 ns, 7 ns, 5 ns

General Description

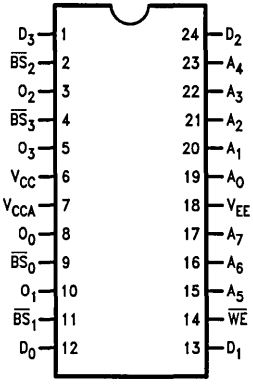
The 100422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device features full on-chip address decoding, separate Data Input and non-inverting Data Output lines, as well as four active-LOW Bit Select lines.

Features

- Address access time—5 ns/7 ns/10 ns max
- Bit select access time—4 ns/5 ns/5 ns max
- Four bits can be independently selected
- Open-emitter outputs for easy memory expansion
- Polyimide die coat for alpha immunity

Connection Diagrams

24-Pin Ceramic Dual-In-Line Package



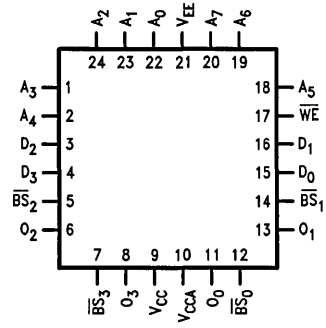
TL/D/9643-2

Top View

Order Number 100422DC5, 100422DC7 or 100422DC10
See NS Package Number J24E*

*For most current package information, contact product marketing.

24-Pin Ceramic Flatpak



TL/D/9643-3

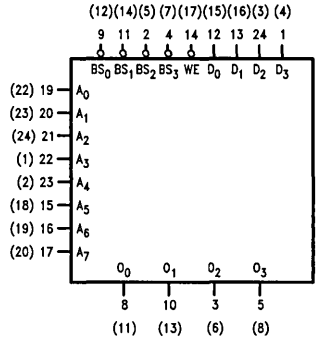
Top View

Order Number 100422FC5, 100422FC7 or 100422FC10
See NS Package Number W24B*

*For most current package information, contact product marketing.

Optional Processing, QR = Burn-In

Logic Symbol



TL/D/9643-1

V_{CC} = Pin 6 (9)
V_{CCA} = Pin 7 (10)
V_{EE} = Pin 18 (21)
( ) = Flatpak

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS_0}$–$\overline{BS_3}$	Bit Select Inputs (Active LOW)
A_0–A_7	Address Inputs
D_0–D_3	Data Inputs
O_0–O_3	Data Outputs

4

Section 5

Design Guide

Section 5 Contents

National Semiconductor

Chapter 1
Circuit Basics

Introduction

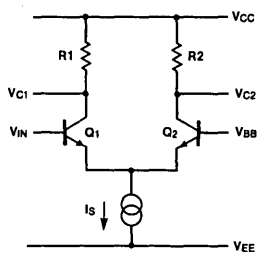
ECL circuits, except for the simplest elements, are schematically formidable and many of the specified parameters are relatively unfamiliar to system designers. The relationships between external parameters and internal circuitry are best determined by individually examining the fundamental subcircuits of a simple element. System variables such as supply voltage tolerances and temperature have predictable effects on circuit parameters, thus allowing a systematic evaluation of noise margins.

Basic ECL Switch

At the bottom of every ECL circuit, literally and figuratively, is a current source. In the basic ECL switch *(Figure 1-1)*, a logic operation consists of steering the current through either of two return paths to V_{CC}; the state of the switch can be detected from the resultant voltage drop across R1 or R2. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish the charging and discharging of all of the parasitic capacitances at the desired switching rate.

Required Input Signal

The voltage swing required to control the state of the switch is relatively small due to the exponential change of emitter current with base-emitter voltage and to the differential mode of operation. For example, starting from a condition where the two base voltages are equal, which causes the current to divide equally between Q1 and Q2, an increase of V_{IN} by 125 mV causes essentially all of the current to flow through Q1. Conversely, decreasing V_{IN} by 125 mV causes essentially all of the current to flow through Q2. Thus the minimum signal swing required to accomplish switching is 250 mV centered about V_{BB}. The signal swing is made larger (approximately 750 mV) to provide noise immunity and to allow for differences between the V_{BB} of one circuit and the output voltage levels of another circuit driving it.



TL/F/9905–1

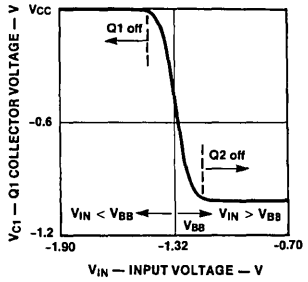
FIGURE 1-1. Basic ECL Switch

Transition Region

If the voltage at the collector of Q1 is monitored while varying V_{IN} above and below the value of V_{BB}, the relationship between V_{C1} and V_{IN} appears as shown in *Figure 1-2*. Note that the horizontal axis of the graph is centered on V_{BB}; this emphasizes the importance of V_{BB} in fixing the location of the transition region. The shape of the transition (or threshold) region is governed by the transistor characteristics and the value of current to be switched. Both of these factors are determined by the circuit designer. The shape of the transition region is essentially invariant over a broad range of conditions, due to the matching of transistor characteristics inherent with IC technology and because the transistors are at the same temperature. The inherent matching of IC resistors assures equal voltage swings at the two collectors.

Emitter-Follower Buffers

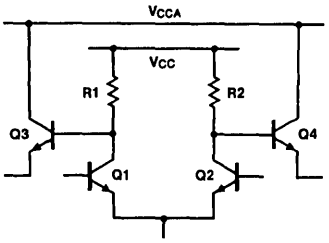
In *Figure 1-2*, V_{C1} ranges from V_{CC} (ground) when Q1 is off to approximately −0.90V when Q1 is conducting all of the source current. To make these voltage levels compatible with the voltages required to drive the input of another current switch, emitter followers are added as shown in the buffered current switch *(Figure 1-3)*. In addition to translating V_{C1} and V_{C2} downward, the emitter followers also isolate the collector nodes from load capacitance and provide current gain. Since the output impedance of the emitter followers is low (approximately 7Ω), ECL circuits can drive transmission lines—coaxial cables, twisted pairs, and etched circuits—having characteristic impedances of 50Ω or more.



TL/F/9905–2

FIGURE 1-2. V_{C1}–V_{IN} Transition Region

Emitter-Follower Buffers (Continued)



TL/F/9905–3

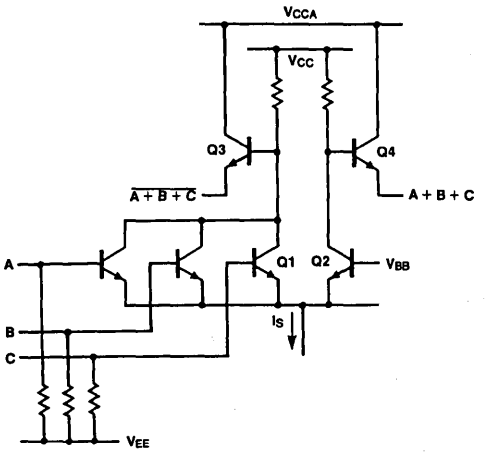
FIGURE 1-3. Buffered Current Switch

In this buffered current switch, the collectors of Q3 and Q4 return to a separate ground lead, V_{CCA}. This separation insures that any changes in load currents during switching do not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire and package lead. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution.

For internal functions of complex circuits where loading is minimal, the buffer transistors are scaled down to maintain high switching speeds with modest source currents. For service as output buffers, the emitter followers are designed for a maximum rated output current of 50 mA. For standardization of testing, detailed specifications on guaranteed min/max output levels apply when an output is loaded with 50Ω returned to −2V. The emitter followers have no internal pull-down resistors; consequently, there is maximum design flexibility when optimizing line terminations and using wired-OR techniques for combinatorial logic or data bussing.

Multiple Inputs

The buffered switch of *Figure 1-3* is essentially an ECL line receiver circuit with the bases of both Q1 and Q2 available for receiving differential signals. With one input connected to the V_{BB} terminal, the switch can receive a signal transmitted in a single-ended mode or it can act as a buffer or logic inverter. To perform the OR and NOR of two or more functions, additional transistors are connected in parallel with Q1 as indicated in *Figure 1-4*. When any input is HIGH, its associated transistor conducts the source current and Q2 is turned off; this causes the collector of Q1 to go LOW and the collector of Q2 to go HIGH, with the emitters of Q3 and Q4 following the collectors of Q1 and Q2 respectively. When two or more inputs are HIGH, the results are the same. Thus, with a HIGH level defined as a True or logic "1" signal, Q3 provides the NOR of the inputs while Q4 simultaneously provides the OR. In addition to the logic design flexibility afforded by the availability of both the assertion and negation, the Q3 and Q4 outputs can drive both conductors of a differential pair for data transmission. Also shown in *Figure 1-4* are the pull-down resistors, nominally 50 kΩ, connected between ECL inputs and the negative supply. These resistors serve the purpose of holding unused inputs in the LOW state by sinking I_{CBO} current and preventing the build-up of charge on input capacitances. Accordingly, most non-essential ECL inputs are designed to be active HIGH. When such inputs are not used, the pull-down resistors eliminate the need for external wiring to hold them LOW.



TL/F/9905–4

FIGURE 1-4. Input Expansion by Parallel Transistors

Power Conservation, Complementary Functions

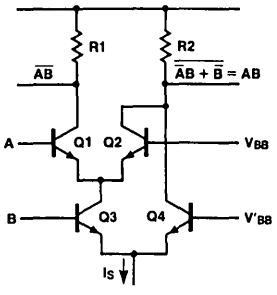
Power dissipation in an ECL circuit is due in part to the output load currents and in part to the internal operating currents. Load currents depend on system design factors and are discussed in Chapter 5. In the basic switch *(Figure 1-1)*, power dissipation is fixed by the source current and the supply voltage, whether the circuit is in a quiescent or transient state. There is no mechanism for causing a current spike such as occurs in TTL circuits, and thus the power dissipation is not a function of switching frequency.

A distinct advantage of the ECL switch is the ease of forming both the assertion and negation of a function without additional time delay or complexity. This is very significant in complex MSI functions, since it helps to maximize the efficiency of the internal logic while minimizing chip area and power consumption. Since most 100K ECL devices have complementary outputs, the system designer has similar opportunities to reduce package count and power consumption while enhancing logic efficiency and reducing throughput times.

Series Gating, Wired-AND

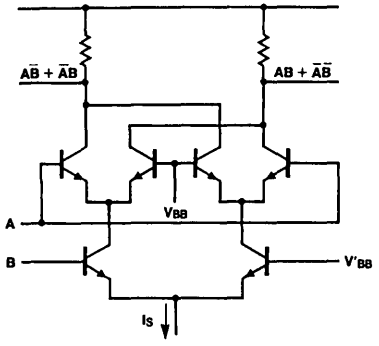
Quite often in ECL elements, the circuitry required to generate functions is much simpler than the detailed logic diagrams suggest. In addition to readily available complementary functions and the wired-OR option, other techniques providing high performance with low part count are series gating and wired collectors. These are illustrated in principle by the simplified schematics of *Figures 1-5* and *1-6*.

Series Gating, Wired-AND (Continued)



TL/F/9905–5

FIGURE 1-5. Series/Parallel Gating



TL/F/9905–6

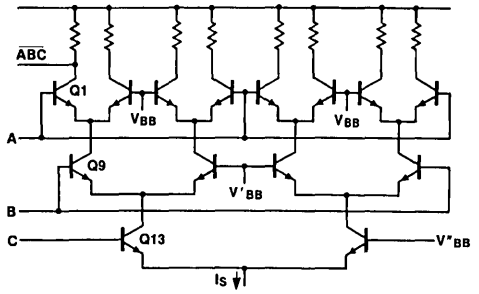
FIGURE 1-6. Exclusive-OR/NOR

In *Figure 1-5*, if both A and B are HIGH, then Q1 and Q3 conduct and I_S flows through R1, making the collector of Q1 go LOW, thereby achieving the NAND of A and B. Connecting the collectors of Q2 and Q4 to the same load resistor provides the AND of A and B. If the collectors of Q3 and Q4 were interchanged, a different pair of functions of A and B would be produced. Similarly, a third functional pair is achieved by interchanging the collectors of Q1 and Q2. For Q3 and Q4 to operate at a lower voltage level than Q1 and Q2, the voltage level of B is translated downward from the normal ECL levels and V'_{BB} is similarly translated downward from the V_{BB} voltage. In the slightly more complex circuit in *Figure 1-6*, another pair of transistors is added to obtain the Exclusive-OR and Exclusive-NOR functions.

Connecting transistors in series is not limited to two levels of decision making; three levels are shown in the simplified schematic of an octal decoding tree *(Figure 1-7)*. If the three input signals are all HIGH, Q1 conducts through Q9 and Q13 to make the collector of Q1 LOW. In all, there are eight possible paths through which the source current can return to the positive supply. A LOW signal at the collector of any one of the transistors in the top row represents a unique combination of the three input signals. This 1-of-8 decoding circuit illustrates very clearly how ECL design techniques make the most efficient use of components and power to generate complex functions. This same set of switches, with the upper collectors wired in two sets of four collectors each, generates the binary sum and its complement of the three input signals.

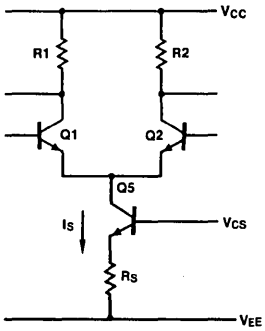
The Current Source, Output Regulation

All elements of the F100K circuits use a transistor current source illustrated in *Figure 1-8*. Source current is determined by an internally generated reference voltage V_{CS}, the emitter resistor R_S and the base-emitter voltage of Q5. The reference voltage is designed to remain fixed with respect to the negative supply V_{EE}, which makes I_S independent of supply voltage.



TL/F/9905–7

FIGURE 1-7. Octal Decoding Tree



TL/F/9905–8

FIGURE 1-8. Constant Current Source for a Switch

Regulating the current source (I_S) simplifies system design because output voltage and switching parameters are not sensitive to V_{EE} changes. Output voltage levels are determined primarily by the voltage drops across R1 and R2 resulting from the collector currents of Q1 and Q2. Since the collector current of the conducting transistor (Q1 or Q2) is determined by I_S and the transistor α, the voltage drop across the collector load resistor is not sensitive to V_{EE} variations. For example, a 1V change in V_{EE} changes the output level V_{OL} by only 30 mV.

Switching parameters are affected by transistor characteristics, the collector resistor (R1 or R2), stray capacitances, and the amount of current being switched. In other forms of ECL where source currents change with V_{EE}, switching parameters are directly affected. This sensitivity is essentially eliminated in F100K circuits by regulating I_S against V_{EE} changes.

Power dissipation in an ECL switch is the product of I_S and V_{EE}. By holding I_S constant with V_{EE}, incremental changes in dissipation are linear with V_{EE} changes. In non-regulated ECL, I_S increases with V_{EE} causing switch dissipation to change more rapidly with V_{EE}.

Threshold Regulation

As previously discussed, the input threshold region of an ECL switch is centered on the internal reference V_{BB}. In F100K circuits, the on-chip bias driver holds V_{BB} constant with respect to V_{CC}, thus minimizing changes in input thresholds with V_{EE}. For a V_{EE} change of 1V, for example, V_{BB} changes by approximately 25 mV.

With output voltage levels and input thresholds regulated, F100K circuits tolerate large differences in V_{EE} between a driving and a receiving circuit and still maintain good noise margins. For example, a driving circuit operated with −4.2V and receiving circuit operated with −5.7V experience a LOW state noise margin loss of only 30 mV to 40 mV compared to the ideal case of both circuits with V_{EE} = −4.5V. This insensitivity to V_{EE} simplifies the design of system power distribution and regulation.

Temperature Compensation

In F100K circuits, input thresholds are made insensitive to temperature by regulating V_{BB}. Output voltage levels are made insensitive to temperature by a correction factor designed into the current source and by a simple network connected between the bases of the output transistors as shown in *Figure 1-9*.

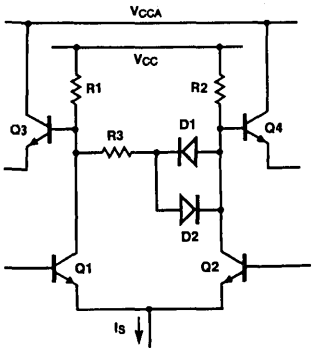


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FIGURE 1-9. Temperature Compensation

With Q1 conducting and Q2 off, most of the source current flows through R1, while a small amount flows through R2, D1 and R3. If the chip temperature increases, the source current is made to increase, causing an increase in the voltage drop of sufficient magnitude across R1 to offset the decrease in base-emitter voltage of Q3. The voltage drop across R1 increases with temperature at the rate of approximately 1.5 mV/°C, while the voltage drop across D1 decreases at the same rate. This means that there is a net voltage increase of 3 mV/°C across the series combination of R2 and R3. This increase is equally divided between the two resistors since R3 is equal to R2 (and R1); thus the voltage at the base of Q4 goes negative by 1.5 mV/°C, offsetting the decrease in the base-emitter voltage of Q4. When Q2 is on and Q1 is off, the same relationships apply except that most of the current flows through R2, and D2 conducts instead of D1. F100K change rates for V_{OH}, V_{BB}, and V_{OL} are approximately 0.06, 0.08 and 0.1 mV/°C, respectively.

The stabilization of output levels against changes in temperature provides significant advantages to both the user and manufacturer. In testing, an extended thermal stabilization period is not required, nor is an elaborate air cooling arrangement necessary to obtain correlation of test results between user and supplier. In a system, the output signal swing of a circuit does not depend on its temperature, therefore temperature differences do not cause a mismatch in signal levels between various locations. With temperature gradients thus eliminated as a system constraint, the design of the cooling system is greatly simplified.

Noise Margins

The most conservative values of ECL noise margins are based on the DC test conditions and limits listed on the data sheets. Acceptance limits on V_{OH} and V_{OL} are identified on a symbolic waveform in *Figure 1-10*, with the boundaries of the input threshold region also identified. The HIGH-state noise margin is usually defined as the difference between $V_{OH(Min)}$ and $V_{IH(Min)}$, with the LOW-state margin defined as the difference between $V_{OL(Max)}$ and $V_{IL(Max)}$. These two differences are identified as V_{NH} and V_{NL} respectively. The worst case input and output test points are also identified on the OR gate transfer function shown in *Figure 1-11*. The transition region indicated by the solid line is applicable when the internal reference V_{BB} has the design center value of −1.32V for F100K circuits. The transition regions indicated by the dashed lines represent the lot-to-lot displacement resulting from the normal production tolerances on V_{BB}, which amount to ±40 mV for F100K circuits. Using F100K circuit values as an example, the dashed curve on the right correlates with a V_{BB} value of −1.280V, and the input test voltage $V_{IH(Min)}$ is −1.165V, for a net difference of 115 mV. Similarly, the dashed curve on the left applies when V_{BB} is −1.360V with $V_{IL(Max)}$ specified as −1.475V, which also gives a net difference of 115 mV. The points V_{OHC} and V_{OLC} are commonly referred to as the *corner points* because of their location on the transfer function of worst case circuits.

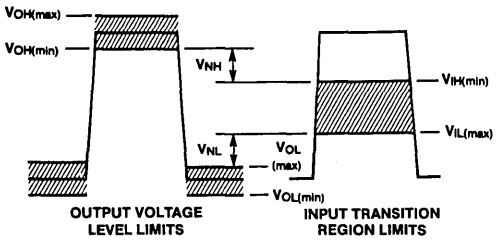

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FIGURE 1-10. Identifying Specification Limits on Input and Output Voltage Levels

In actual system operation, the noise margins V_{NH} and V_{NL} are quite conservative because of the way $V_{IH(Min)}$ and $V_{IL(Max)}$ are defined. From the transfer function of *Figure 1-11*, for example, $V_{IH(Min)}$ is defined as a value of input voltage which causes a worst-case output to decrease from $V_{OH(Min)}$ to V_{OHC} This change in V_{OH} amounts to only 10 mV for F100K circuits. Thus, if a worst case OR gate has a quiescent input of $V_{OH(Min)}$, a superimposed negative-going disturbance of amplitude V_{NH} causes an output change of only 10 mV, assuming that the time duration of the disturbance is sufficient for the OR gate to respond fully. In

Noise Margins (Continued)

contrast, a system fault does not occur unless the superimposed noise at the OR input is of sufficient amplitude to cause the output response to extend into the threshold region(s) of the load(s) driven by the OR gate. In general, noise becomes intolerable when it propagates through a string of gates and arrives at the input of a regenerative circuit (flip-flop, counter, shift register, etc.) with sufficient amplitude to reach the V_{BB} level.

The critical requirement for propagating either a signal or noise through a string of gates is that each output must exhibit an excursion to the V_{BB} level of the next gate in the string, assuming, of course, that the time duration is sufficient to allow full response. If the excursion at the input of a particular gate either falls short or exceeds V_{BB}, the effect on its output response is magnified by the voltage gain of the gate. On the voltage transfer function of a gate, the slope in the transition region is not, strictly speaking, constant. However, for input signal excursions of about ±50 mV on either side of V_{BB}, a value of 5.5 may be used for the voltage gain. For example, if the noise (or signal) excursion at the input of a gate falls short of V_{BB} by 20 mV, the gate output response is 110 mV less. Another useful relationship is that if the input voltage of a gate is equal to V_{BB}, the output voltage is also equal to V_{BB}, within perhaps 30 mV.

To determine the combined effects of circuit and system parameters on noise propagation through a string of gates, refer to *Figure 1-12*. The voltages V_1 and V_2 represent differences in ground potential, while V_3 and V_4 are V_{EE} differences. The output of gate A is in the quiescent LOW state and V_{PL} is a positive-going disturbance voltage. Now, how large can V_{PL} be without causing propagation through gate C? For a starting point, assume all three gates are identical with typical parameters; V_{EE} is −4.5V, the ground drops are zero, and there are no temperature gradients. Voltage parameters of F100K circuits are used. With typical circuits and the idealized environment, the maximum tolerable value of V_{PL} for propagation is the difference between the nominal V_{BB} of −1.320V and nominal V_{OL} of −1.705V, or 385 mV. The following steps treat each non-ideal factor separately and the required reduction in V_{PL} is calculated.

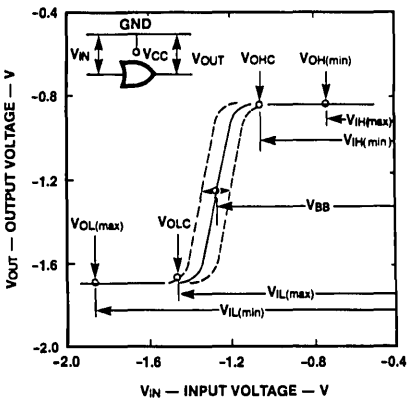

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FIGURE 1-11. Location of Test Points and Threshold on a Transfer Function

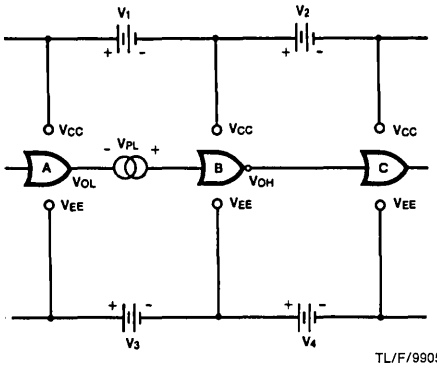

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FIGURE 1-12. Arrangement for Noise Propagation Analysis

Non-Typical V_{BB} of Gate B: Specifications provide for V_{BB} variations of ±40 mV. If the V_{BB} of gate B is 40 mV more negative than nominal, V_{PL} must be reduced by the same amount.

$\Delta V_{PL} = -40$ mV

$V_{PL} = 385 - 40 = 345$ mV

Non-Typical V_{OL} of Gate A: V_{OL} limits are −1.620V to −1.810V corresponding to the $\pm 3\sigma$ points on the distribution. Statistically, this means that 98% of the circuits have V_{OL} values of −1.650V or lower. Since this value differs from the nominal V_{OL} by 55 mV, V_{PL} must be reduced accordingly.

$\Delta V_{PL} = -55$ mV

$V_{PL} = 345 - 55 = 290$ mV

Difference in Ground (V_{CC}) Potential between Gates A and B: Since the V_{CC} lead of Gate B is the reference potential for input voltages, V_1 in the polarity shown effectively makes the V_{OL} of Gate A more positive. Minimizing ground drops is one of the system designer's tasks *(Chapter 5)* and its effect on noise margins emphasizes its importance. For this analysis, a value of 30 mV is assumed.

$\Delta V_{PL} = 30$ mV

$V_{PL} = 290 - 30 = 260$ mV

Difference in V_{EE} between Gates A and B: In the polarity shown, V_3 reduces the supply voltage for Gate A since it is assumed that Gate B has V_{EE} of −4.5V. The indicated polarities of V_1 and V_3 seem to be in conflict if it is assumed that V_3 represents only ohmic drops along the V_{EE} bus. Since V_3 may, however, be caused by the use of different power supplies or regulators as well as by ohmic drops, the polarities may exist as indicated. In any actual situation, the designer can usually predict the directions of supply current flow by observation of the physical arrangement. As mentioned earlier, a 1V change in V_{EE} causes a V_{OL} change 30 mV, or 3%. Assuming a value of 0.5V for V_3 and adding the 30 mV of V_1, the net reduction in supply voltage for Gate A is 0.53V. Using 3% of this reduction as the change in V_{OL} gives a positive V_{OL} shift of 16 mV, which is a reduction of noise margin.

$\Delta V_{PL} = -16$ mV

$V_{PL} = 260 - 16 = 244$ mV

If the net supply voltage of Gate A is assumed to be −4.5V, then V_1 and V_3 cause Gate B to have a greater supply voltage. This, in turn, causes the V_{BB} of Gate B to go more negative at the rate of 25 mV/V of V_{EE} change, or 2.5%.

Noise Margins (Continued)

Thus, for the same values of V_1 and V_3, the required reduction of V_{PL} is only 13 mV instead of the 16 mV computed above.

Non-Typical V_{BB} of Gate B: This was considered earlier for its effect at the input of Gate B. It must also be considered for its effect on the excursions of the output voltage of Gate B. Since the net input voltage of Gate B ($V_{OL} + V_{PL}$) reaches the V_{BB} level of Gate B, the output excursion also extends to the V_{BB} level and perhaps 30 mV beyond (more negative). This means that the output excursion of Gate B could be 90 mV more negative than the nominal V_{BB} of Gate C. This excess excursion must be divided by the voltage gain of Gate B to determine exactly how much V_{PL} must be reduced as compensation.

$\Delta V_{PL} = -90/5.5 = -16$ mV

$V_{PL} = 244 - 16 = 228$ mV

Non-Typical V_{BB} of Gate C: The V_{BB} of Gate C could be 40 mV more positive than the nominal value of −1.320V. Dividing by the voltage gain of Gate B gives the necessary reduction of V_{PL}.

$\Delta V_{PL} = -40/5.5 = -7$ mV

$V_{PL} = 228 - 7 = 221$ mV

Difference in V_{CC} Potential between Gates B and C: For the polarity shown, V_2 makes the net voltage at the C input more negative with respect to the V_{CC} lead of Gate C. Assume 30 mV for V_2 as was done for V_1.

$\Delta V_{PL} = -30/5.5 = -5.0$ mV

$V_{PL} = 217 - 5 = 212$ mV

Difference in V_{EE} between Gates B and C: In the polarity shown, V_4 reduces the supply voltage for Gate C, as does V_2. As previously mentioned, V_{BB} changes with V_{EE} at a rate of 25 mV/V, or 2.5%. Assuming a value of 0.5V for V_4, as was done for V_2, adding V_2 gives a net V_{EE} reduction of 0.53V. This makes the V_{BB} of Gate C about 13 mV more positive, with respect to its own V_{CC} lead. This must be divided by the gain of Gate B to determine the effect on the permissible value of V_{PL}.

$\Delta V_{PL} = -13/5.5 \cong -2$ mV

$V_{PL} = 212 - 2 = 210$ mV

At this point the more conservatively defined V_{NL} *(Figure 1-10)* should be evaluated and compared with V_{PL}. Subtracting the values of $V_{OL(Max)}$ and $V_{IL(Max)}$, a value of 145 mV for V_{NL} is obtained.

The primary advantage of using V_{NH} and V_{NL} as the limits of tolerable noise is that they provide for simultaneous appearance of noise on inputs and outputs. Whatever the system designer's preference regarding noise margin definitions, the important factor is to recognize that the ΔV_{CC} and ΔV_{EE} between devices decrease the noise margins and therefore should be minimized.

References

1. Marley, R.R., "On-Chip Temperature Compensation for ECL", *Electronic Products*, (March 1, 1971).
2. Marley, R.R., "Design Considerations of Temperature Compensated ECL," *IEEE International Convention*, (March, 1971).
3. Widlar, R.J., "Local IC Regulator for Logic Circuits," *Computer Design*, (May, 1971).
4. Widlar, R.J., "New Developments in IC Voltage Regulators," *ISSCC Digest of Technical Papers*, (February, 1970).
5. Muller, H.H., Owens, W.K., Verhofstadt, P.W.J., "Fully Compensated ECL," *ISSCC Digest of Technical Papers*, (February, 1973).

National Semiconductor

Chapter 2
Logic Design

Introduction

The F100K family comprises SSI, MSI, LSI, gate arrays, RAMs and PROMs. This chapter covers basic gates and flip-flops, as well as applications using MSI. Gate arrays and LSI are covered in separate publications and memory applications are included in the Bipolar Memory Data Book.

National F100K ECL logic symbols use the positive logic or "active-HIGH" option of MIL-STD-806B. Logic '1' is the more positive voltage, nearest ground (typically −0.955V). Logic '0' or "active LOW" is the more negative level, nearest V_{EE} (typically −1.705V).

OR/NOR Gates

The most basic F100K ECL circuit is the OR/NOR gate *(Figure 2-1)*. If the input (A or B) voltages are more negative than the reference voltage V_{BB}, Q1 and Q2 are cut off (non-conducting) and Q3 conducts, holding the collector of Q3 LOW. Since the base of Q4 is LOW, the pull-down resistor or terminator connected to its emitter makes the OR output LOW. The base of Q5 is HIGH (near ground) and its emitter pulls the NOR output HIGH. If either input is more positive than V_{BB}, Q1 or Q2 conducts and Q3 is cut off. This makes the base of Q4 HIGH, resulting in a HIGH at the OR output. At the same time, the base of Q5 is LOW and the pull-down resistors or terminator pulls the NOR output LOW. Detailed information concerning F100K ECL circuit basics may be found in Chapter 1.

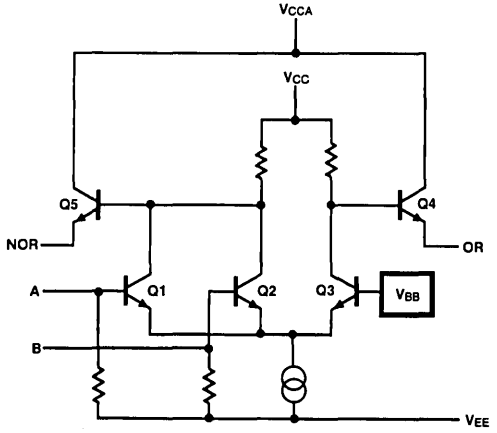

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FIGURE 2-1. Basic ECL Gate

The F100K family includes two OR/NOR-gate devices. The F100101 is a triple 5-input OR/NOR and the F100102 is a quint 2-input OR/NOR with common enable. One element of the F100102 is shown in *Figure 2-2*; the corresponding truth table is Table 2-1.

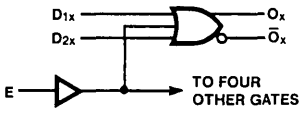

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FIGURE 2-2. F100102 OR/NOR Gate

TABLE 2-1. F100102 Truth Table

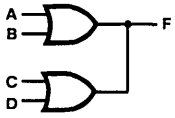
D_{1x}	D_{2x}	E	O_x	$\overline{O}_x$
L	L	L	L	H
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Wired-OR Function

A wired-OR function can be implemented simply by connecting the appropriate outputs external to the package (see *Figure 2-3*). Each output is buffered so that the internal logic is not affected by the wire-OR. This is a positive logic OR, not to be confused with a DTL wired-AND or the internal series gating used for some ECL functions. This wired-OR is especially useful in implementing data busses. For further information see Chapter 4.

Wired-OR Function (Continued)



$F = (A + B) + (C + D)$
$= A + B + C + D$
$= \overline{\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}}$

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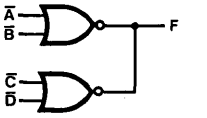

$F = \overline{\overline{A} + \overline{B}} + \overline{\overline{C} + \overline{D}}$
$= AB + CD$

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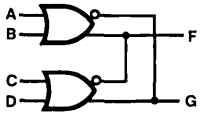

$G = (\overline{A+B}) + (C+D)$
$= (\overline{A}\,\overline{B}) + C + D$
$F = A+B + \overline{C+D}$
$= A+B + (\overline{C}\,\overline{D})$

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FIGURE 2-3. Wired-OR Function

AND Function

The positive logic AND function is directly available in F100K ECL (F100104). There are two other approaches which can be taken to solve the problem of implementing an AND.

The first solution is indicated in *Figure 2-4*. A positive logic OR gate can be redrawn as a negative logic AND gate. To take advantage of this requires active-LOW input terms; but, since practically every F100K circuit provides complementary outputs, this should not be a problem.

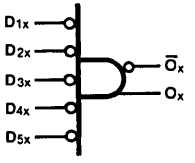

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FIGURE 2-4. F100101 Redrawn as AND/NAND Gate

The second possible solution is to use devices in a manner other than that intended, at the cost of package efficiency. The F100117 may be used as a triple 3-input AND/NAND by connecting only one input on each of the OR gates. The F100179 may be used as a single 9-input AND gate by connecting the inputs to $\overline{C}_n$ and $\overline{G}_7$ through $\overline{G}_0$. The $\overline{P}_n$ inputs are left open (LOW) and the output is taken from $\overline{C}_{n+8}$.

OR-AND, OR-AND-Invert Gates

The F100117 is a triple 2-wide OR-AND, OR-AND-Invert Gate. The logic diagram and truth table for one section of the F100117 are shown in *Figure 2-5* and Table 2-2, respectively. The F100118 5-wide OA/OAI has OR inputs of 5, 4, 4, 4, and 2.

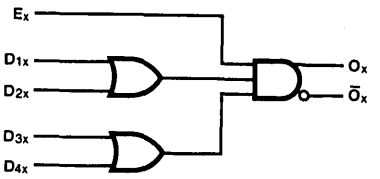

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FIGURE 2-5. F100117 OA/OAI Gate

TABLE 2-2. F100117 Truth Table

E_x	D_{1x}	D_{2x}	D_{3x}	D_{4x}	O_x	$\overline{O}_x$
H	H	X	H	X	H	L
H	X	H	X	H	H	L
X	L	L	X	X	L	H
X	X	X	L	L	L	H
L	X	X	X	X	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Exclusive-OR/Exclusive-NOR Gate

The F100107 is a quint exclusive OR/NOR gate. In addition to providing the exclusive-OR/exclusive-NOR of the five input pairs, a comparison output is available. If the five pairs of inputs are identical, bit by bit, then the common output will be LOW.

Flip-Flops and Latches

Flip-flops and latches are treated together due to their similarity. The only difference is that latch outputs follow the inputs whenever the enable is LOW, whereas a flip-flop changes output states only on the LOW-to-HIGH clock transition.

The advantage of an edge-triggered flip-flop is that the outputs are stable except while the clock is rising; a latch has better data-to-output propagation delay while the enable is kept active.

Both latches and flip-flops are available three to a package with individual as well as common controls and six to a package with only common controls. There are a total of four parts as indicated below.

	Triple w/Individual Controls	Hex w/Common Controls
Flip-Flops	F100131	F100151
Latches	F100130	F100150

Figure 2-6 shows the equivalent logic diagram of ⅓ of an F100131. The internal clock is the OR of two clock inputs, one common to the other two flip-flops. The OR clock input permits common or individual control of the three flip-flops. In addition, one input may be used as a clock input and the other as an active-LOW enable.

Flip-Flops and Latches (Continued)

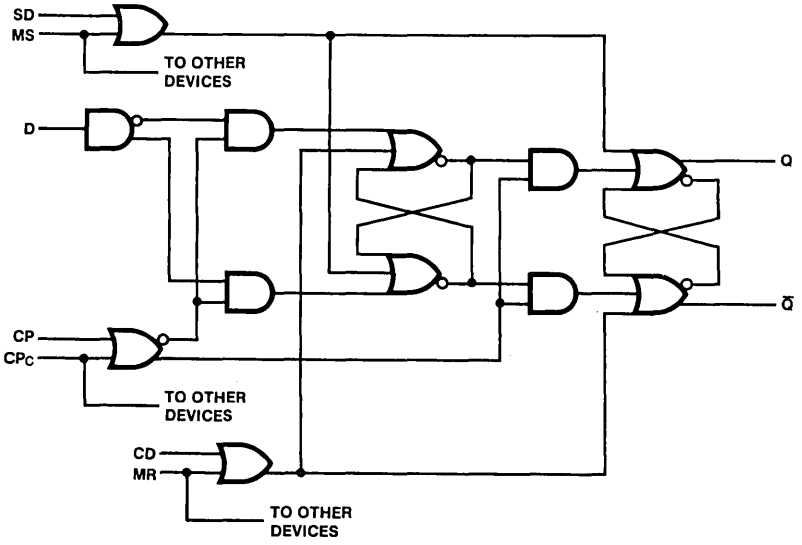

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FIGURE 2-6. F100131 D Flip-Flop

When the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master, causing the new information to appear at the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

The Clear and Set Direct for each flip-flop are the OR of two inputs, one common to the other two flip-flops. The output levels of a flip-flop are unpredictable if both the Set and Clear Direct inputs are active.

The outputs of all F100K flip-flops and latches are buffered. This means that they can be OR-wired; noise appearing on the outputs cannot affect the state of the internal latches.

Table 2-3 is the truth table for the F100131 flip-flop. The truth table for the F100130 latch is similar except the enables are active LOW whereas the F100131 clocks are edge triggered.

TABLE 2-3. F100131 Truth Table

D_n	CP_n	CP_c	MS SD_n	MR CD_n	$Q_{n(t+1)}$
L	⌐	L	L	L	L
H	⌐	L	L	L	H
L	L	⌐	L	L	L
H	L	⌐	L	L	H
X	H	X	L	L	$Q_n(t)$
X	X	H	L	L	$Q_n(t)$
X	X	X	H	L	H
X	X	X	L	H	L
X	X	X	H	H	U

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
U = Undefined
t, t + 1 = Time before and after CP positive transition

If eight flip-flops are desired, such as for pipeline register applications, the F100141 Shift Register can be used. Neither reset nor complementary outputs are available. The Select inputs may be used to mechanize a clock enable as shown in *Figure 2-7*.

Flip-Flops and Latches (Continued)

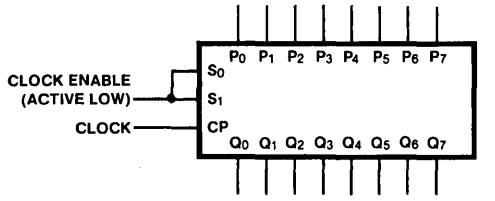

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FIGURE 2-7. F100141 as Octal D Flip-Flop

Counters

The F100136 operates either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register. It has three Select inputs which determine the mode of operation as shown in Table 2-4. In addition, a Terminal Count output, and two Count Enables are provided for easy expansion to longer counters. A detailed truth table for the F100136 is included in the specification sheet. To achieve the highest possible speed, complementary outputs should be equally terminated, i.e., if Q_2 is used, $\overline{Q}_2$ should be equally terminated even if not used. If neither output of a particular stage is used, then both outputs can be left open.

TABLE 2-4. F100136 Function Select Table

S_0	S_1	S_2	Function
L	L	L	Load
L	L	H	Count Down
L	H	L	Shift Left
L	H	H	Count Up
H	L	L	Complement
H	L	H	Clear
H	H	L	Shift Right
H	H	H	Hold

H = HIGH Voltage Level
L = LOW Voltage Level

VARIABLE MODULUS COUNTERS

An F100136 can act as a programmable divider by presetting it via the parallel inputs, counting down to minimum and then presetting it again to start the next cycle. *Figure 2-8* shows a one-stage counter capable of dividing by 2 to 15. S_0 and S_1 are unconnected (therefore LOW) and the counter thus is in either the Count Down or Parallel Load mode, depending on whether S_2 is HIGH or LOW, respectively. $\overline{CEP}$ and $\overline{CET}$ are also LOW, enabling counting when S_2 is HIGH. Immediately after the counter is preset to N, which must be greater than one, the $\overline{LOAD}$ signal goes HIGH and the F100136 starts counting down on the next clock. When it counts down to one, the $\overline{LOAD}$ signal goes LOW and presetting will occur on the next clock rising edge. Generating the $\overline{LOAD}$ signal on the count of one, rather than zero, makes up for the clock pulse used in presetting.

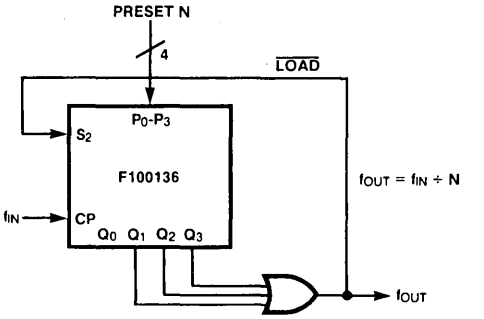

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FIGURE 2-8. 1-Stage Counter

A 3-stage programmable divider is shown in *Figure 2-9*. The $\overline{TC}$ output of the first stage enables counting in the upper stages, while the $\overline{TC}$ output of the second stage also enables counting in the third stage. The D-input signal to the flip-flop is normally HIGH and thus $\overline{Q}$ is normally LOW. When both the second and third stage counters have counted down to zero, the $\overline{TC}$ output of the third stage goes LOW. When the first stage subsequently counts down to one, the D signal goes LOW, as does $\overline{LOAD}$. Presetting thus occurs on the next clock and $\overline{Q}$ goes HIGH to end the $\overline{LOAD}$ signal and permit counting to resume on the next clock.

In *Figure 2-8*, the maximum clock frequency is determined by the sum of the propagation delays from CP to Q and the OR gate, plus the setup time from S to CP. The maximum frequency is approximately 220 MHz for typical units or 170 MHz for worst-case units. In *Figure 2-9* the critical path is CP to Q of the first stage plus both OR gates, plus the S to CP set-up time of the counters. Typical and worst-case maximum frequencies are 190 MHz and 140 MHz respectively.

INTERCONNECTING COUNTERS

The terminal count and count enable connections provide an easy method of interconnecting the F100136 counter to achieve longer counts. *Figure 2-10* shows a method that uses few connections but has a drawback. The counters are fully synchronous, since the clock arrives at all devices at the same time; the only drawback is that the count enables have to "trickle" down the chain. This results in a lower maximum counting rate since it drastically increases the set-up time from enable to clock.

Figure 2-11 shows a method for partially overcoming these drawbacks. The enable to clock set-up is now one $\overline{CET}$ to $\overline{TC}$ propagation delay plus one $\overline{CEP}$ to CP set-up. The count speed is thus increased. This is best seen by assuming that all stages except the second are at terminal count. At the next clock pulse, the second counter reaches terminal count and the first stage exits terminal count. The command to suppress counting in the third and fourth (and subsequent) stages arrives very quickly (via $\overline{CEP}$). The terminal count from the second stage propagates via $\overline{TC}$ and $\overline{CEP}$ to the high order stages, but has a full 15 counts to do so.

Counters (Continued)

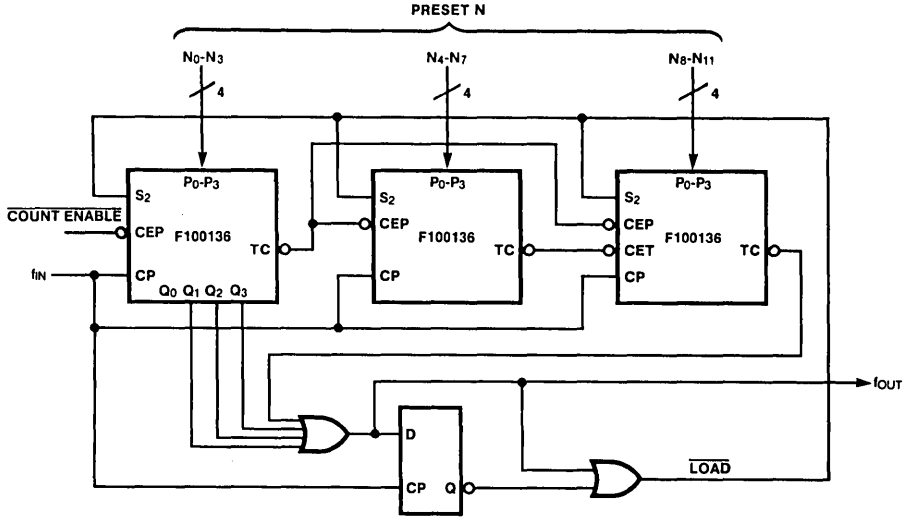

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FIGURE 2-9. 3-Stage Programmable Divider

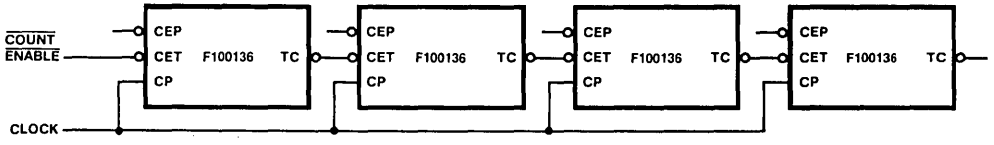

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FIGURE 2-10. Slow Expansion Scheme

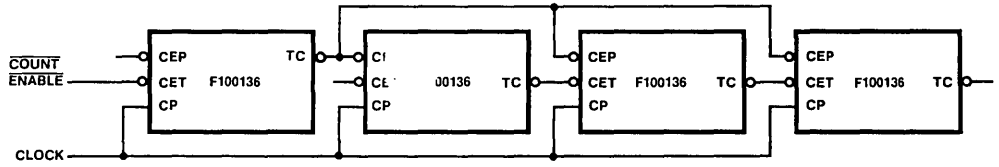

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FIGURE 2-11. Fast Expansion Scheme

Counters (Continued)

DECODING OUTPUTS

Since the complementary outputs from each stage are available, it is an easy matter to decode any value. (Clearly, if many values needed to be decoded one would choose a decoder chip.) *Figure 2-12* shows an F100136 and ⅓ F100101 interconnected to decode 1001 (NINE). Both complementary outputs of NINE are available and there is a spare input on the decoding gate.

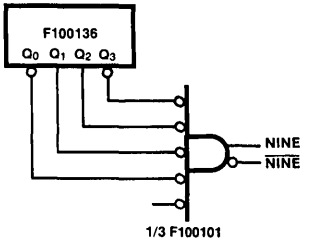

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FIGURE 2-12. Decoding States of F100136

Shift Registers

The F100141 is an 8-bit universal shift register. It can be used for parallel-to-serial or serial-to-parallel conversion and it will shift left or right. The truth table is shown in Table 2-5.

TABLE 2-5. F100141 Truth Table

S_1	S_0	CP	Mode
L	L	⌐	Parallel Load
L	H	⌐	Shift Left ($Q_0 \rightarrow Q_7$)
H	L	⌐	Shift Right ($Q_7 \rightarrow Q_0$)
H	H	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 2-13 shows the F100141 used as a 7-bit serial-to-parallel converter. When Initialize (INIT) becomes active, the next clock pulse presets the register to '10000000', and Register-Full (REG-FULL) becomes inactive. Each time a data bit becomes available, Data-Available (DATA-AVAIL) must be made active during one clock LOW-to-HIGH transition. This clocks the bit into the register moves the flag bit closer to Q_0. When the seventh data bit is entered, the flag bit reaches Q_0 and REG-FULL becomes active. The seven data bits may be removed at this time (Q_1 to Q_7) and the conversion is complete.

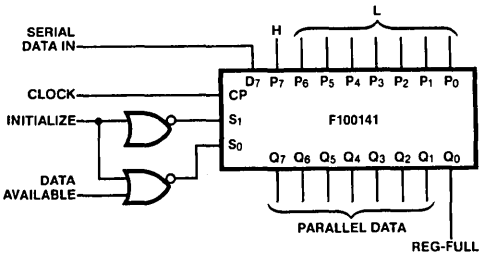

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FIGURE 2-13. Serial-to-Parallel Conversion

Table 2-6 summarizes the control inputs and corresponding F100141 modes for this circuit.

TABLE 2-6. Select Inputs Truth Table

INIT	DATA-AVAIL	S_1	S_0	Mode
L	L	H	H	Hold
L	H	H	L	Shift Right
H	L	L	L	Preset
H	H	L	L	(Illegal)

H = HIGH Voltage Level
L = LOW Voltage Level

Figure 2-15 shows a parallel-to-serial converter using the F100136 counter. *Figure 2-14* shows the associated timing diagram. Each time the external device has taken a bit of data, it makes the signal Serial-Data-Accept (SERIAL-DATA-ACPT) HIGH. The shift register shifts right which makes the next bit available and the counter counts up. The Serial-Data-Accept term must be synchronized with the clock. The counter counts to eight after the eighth data bit has been accepted and Parallel-Data-Request (PARALLEL-DATA-RQST) becomes active HIGH. When the device supplying data makes the next byte available, Parallel-Data-Ready (PARALLEL-DATA-RDY) goes HIGH. On the next clock pulse the shift register loads the new data byte and the counter clears to zero. Table 2-7 shows the operating mode as a function of the control inputs.

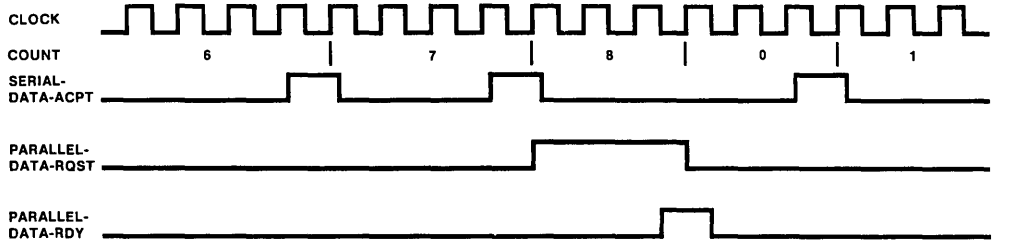

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FIGURE 2-14. Timing Diagram Parallel-to-Serial Converter

Shift Registers (Continued)

TABLE 2-7. Parallel-to-Serial Converter Truth Table

PARALLEL-DATA-RDY	SERIAL-DATA-ACPT	Shift Register			Counter			
		S_1	S_0	Mode	S_0	S_1	S_2	Mode
L	L	H	H	Hold	H	H	H	Hold
L	H	H	L	Shift Right	L	H	H	Count Up
H	L	L	L	Load	H	L	H	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

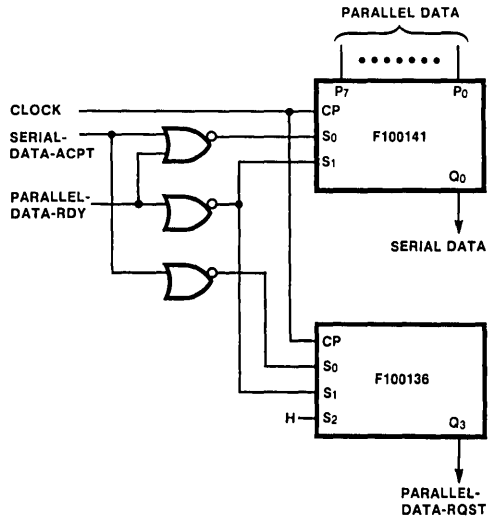

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FIGURE 2-15. Parallel-to-Serial Converter

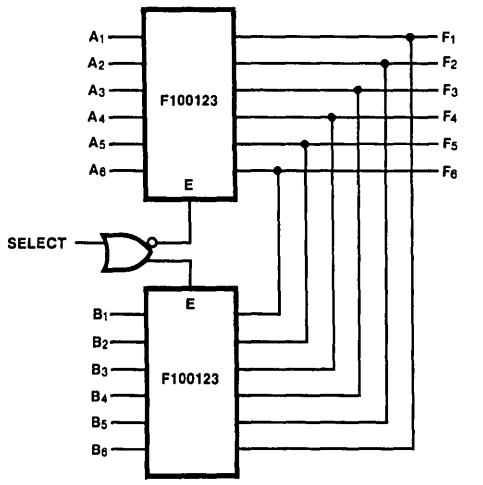

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FIGURE 2-16. Wired-OR Multiplexer

Multiplexers

Multiplexers send one of several inputs to a single output. The function can be implemented with standard gates or bus drivers and the wired-OR connection. *Figure 2-16* shows the F100123 Hex Bus Driver used as a wired-OR multiplexer. The F100123 devices could be in physically different parts of the system, since they can drive double-terminated busses.

The F100155 is a quad 2-input multiplexer with transparent latches. The device has two select terms and can accept data from either, neither, or both (OR) sources.

The F100163 is a dual 8-input multiplexer with common selects. The F100164 is a single 16-input multiplexer.

The F100163 and F100164 do not feature complementary outputs or an enable for wired-ORing. The F100171 is a triple 4-input multiplexer with enable and complementary outputs.

Figure 2-17 shows an F100164 multiplexer and F100136 connected to convert 16-bit parallel data to single-bit serial data. A gate is added to provide complementary serial data. If the input data is stable, then the output data is stable from 6.4 ns after a clock until 2.5 ns after the next clock. This would insure valid data 50% of the time at a clock rate of 100 MHz. Terminal Count on the counter can be used as a term to indicate the last bit is being transmitted. This can be used as a clock enable to the register containing the parallel data. The propagation delay through the register is masked by the propagation delay through the counter.

Multiplexers (Continued)

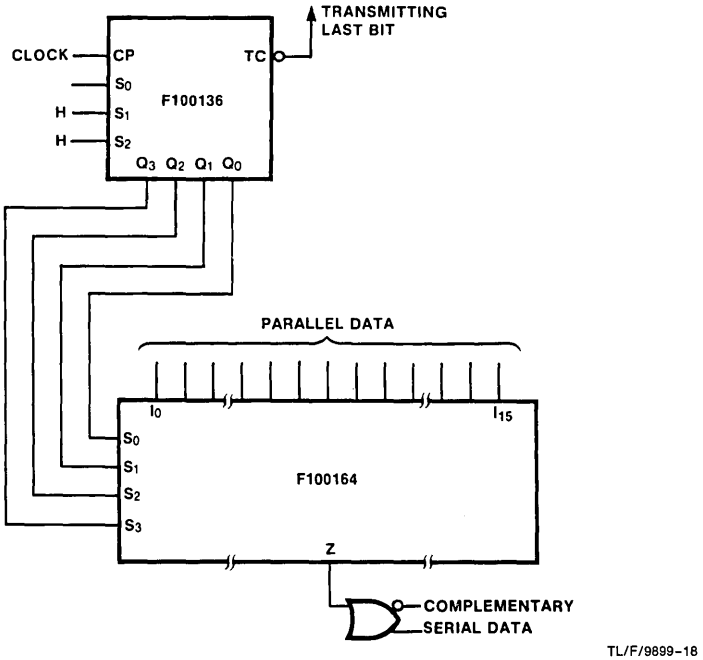

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FIGURE 2-17. Parallel-to-Serial Data Transmission

Decoder

The F100170 is a universal demultiplexer/decoder. It can function as either a dual 1-of-4 decoder or as a single 1-of-8 decoder. The outputs can be either active HIGH or active LOW.

If the M input is LOW, then the F100170 is configured as a dual 1-of-4 decoder. Both A_{2a} and H_c must be LOW. Table 2-8 is a truth table for each half of the F100170; the two halves are completely independent. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_x is made LOW.

TABLE 2-8. Dual 1-of-4 Mode Truth Table

Inputs				Active-HIGH Outputs (H_a and H_b Inputs HIGH)			
$\bar{E}_{1a}$ $\bar{E}_{1b}$	$\bar{E}_{2a}$ $\bar{E}_{2b}$	A_{1a} A_{1b}	A_{0a} A_{0b}	Z_{0a} Z_{0b}	Z_{1a} Z_{1b}	Z_{2a} Z_{2b}	Z_{3a} Z_{3b}
H	X	X	X	L	L	L	L
X	H	X	X	L	L	L	L
L	L	L	L	H	L	L	L
L	L	L	H	L	H	L	L
L	L	H	L	L	L	H	L
L	L	H	H	L	L	L	H

M = A_{2a} = H_c = LOW
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE 2-9. Single 1-of-8 Mode Truth Table

Inputs					Active-HIGH Outputs (H_c Input HIGH)							
$\bar{E}_1$	$\bar{E}_2$	A_{2a}	A_{1a}	A_{0a}	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7
H	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H

M = HIGH;
A_{0b} = A_{1b} = H_a = H_b = LOW
E_1 = E_{1a} and E_{1b} Wired; E_2 = E_{2a} and E_{2b} Wired
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

If the M input is HIGH, then the F100170 is configured as a single 1-of-8 decoder. A_{0b}, A_{1b}, H_a, and H_b must all be LOW. Table 2-9 is a truth table for the F100170 in single 1-of-8 mode. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_C is mode LOW.

Figure 2-18 and Table 2-10 show a universal decimal decoder and the decode table, respectively. The sense of the outputs can be easily modified. The entire decoder may be enabled with a LOW at the Function input.

Decoder (Continued)

TABLE 2-10. Output Selection

A_0–A_3 Weighted Input	Selected Output per Input Code				
	8421	5421	Excess 3	Excess 3 Gray	2421
0	0	0	3	2	0
1	1	1	4	6	1
2	2	2	5	7	2
3	3	3	6	5	3
4	4	4	7	4	4
5	5	8	8	12	11
6	6	9	9	13	12
7	7	10	10	15	13
8	8	11	11	14	14
9	9	12	12	10	15

Figure 2-19 shows a scheme to decode five lines with a 1-of-32 decoder. Inputs A_0, A_1, and A_2 are connected to the address select inputs of all four decoders in parallel. Both the true and complement of the two high order addresses are formed and then ANDed together at the decoder enable inputs.

Figure 2-20 shows a 1-of-64 decoder which uses the LOW outputs of one F100170 to enable one-of-eight F100170 devices whose address inputs are connected together. The unused enable inputs may be used to enable all 64 outputs. The 64 outputs may be either active HIGH or LOW. The propagation delay from address to any output is 4.5 ns maximum.

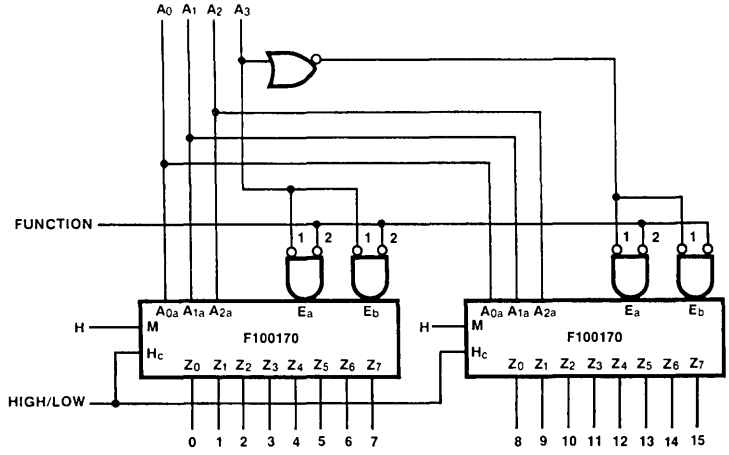

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FIGURE 2-18. Universal Decimal Decoder

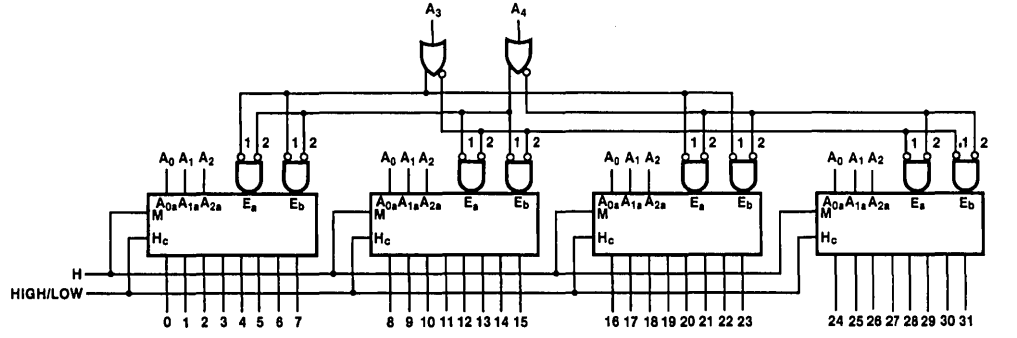

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FIGURE 2-19. 1-of-32 Decoder

Decoder (Continued)

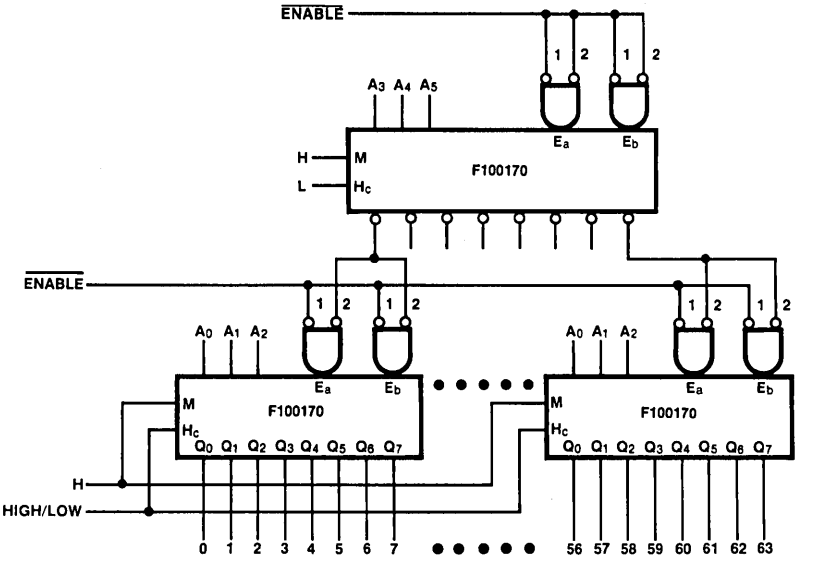

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FIGURE 2-20. 1-of-64 Decoder

Register File

The F100145 is a 16 x 4 register file with typical Read access time of 5.5 ns. It has separate addresses for Read (AR_n) and Write (AW_n) operations. This reduces effective cycle time by allowing one address to be setting up while the other is being used.

Internal output latches are present which store data from a prevous Read while a Write is in progress. Any time a Write is not in progress, the data in the latches are updated from the array.

Active-LOW output enables are available, allowing the F100145 to be OR-wired for easy expansion. A HIGH on the Master Reset (MR) input, which overrides all other inputs, resets the output latches, forces the outputs LOW, and clears all cells in the memory.

Figure 2-21 indicates a method of connecting one or more F100145 devices with F100136 devices to form a very fast FIFO. This FIFO can be expanded horizontally (to form wider words) by merely adding more register files. The inputs and outputs must be synchronized to a common clock.

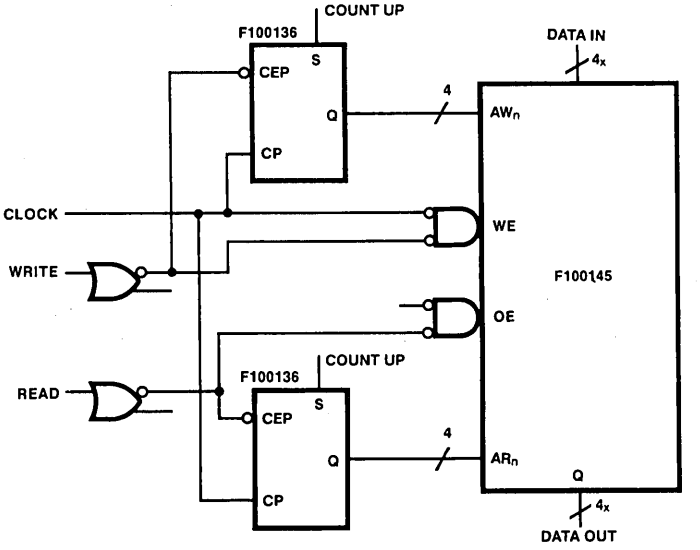

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FIGURE 2-21. FIFO Diagram

Register File (Continued)

During the first half of the clock cycle, data are written into the FIFO in the case of a WRITE command, or presented on the outputs in the case of a READ command. During the second half of the cycle, either the Write or Read (or neither) address is updated. In addition, the data at the current Read address is accessed in case it will be used during the next cycle. This means that Read data is available very early in the cycle.

The FIFO timing diagram is shown in *Figure 2-22*. The minimum timing of the LOW portion of the clock may be determined as follows. The Write pulse width is 4 ns typical and the data set-up to trailing edge of Write is 6 ns typical. Assuming the Write data are available at the beginning of the period, the 6 ns would be the longest path.

The worst case for the HIGH portion of the clock is when a Read is followed by a Read. In this case, the counter must be incremented and the data read from a new location. This is 1.6 ns + 5.5 ns typical. Allowing for non-typical devices, clock skew, and interconnection delays could bring these numbers to 10 ns each, for a total (Read or Write) cycle time of 20 ns. Since a Read and a Write are required to move one piece of data through the FIFO, the actual transfer rate is 25 M words/second.

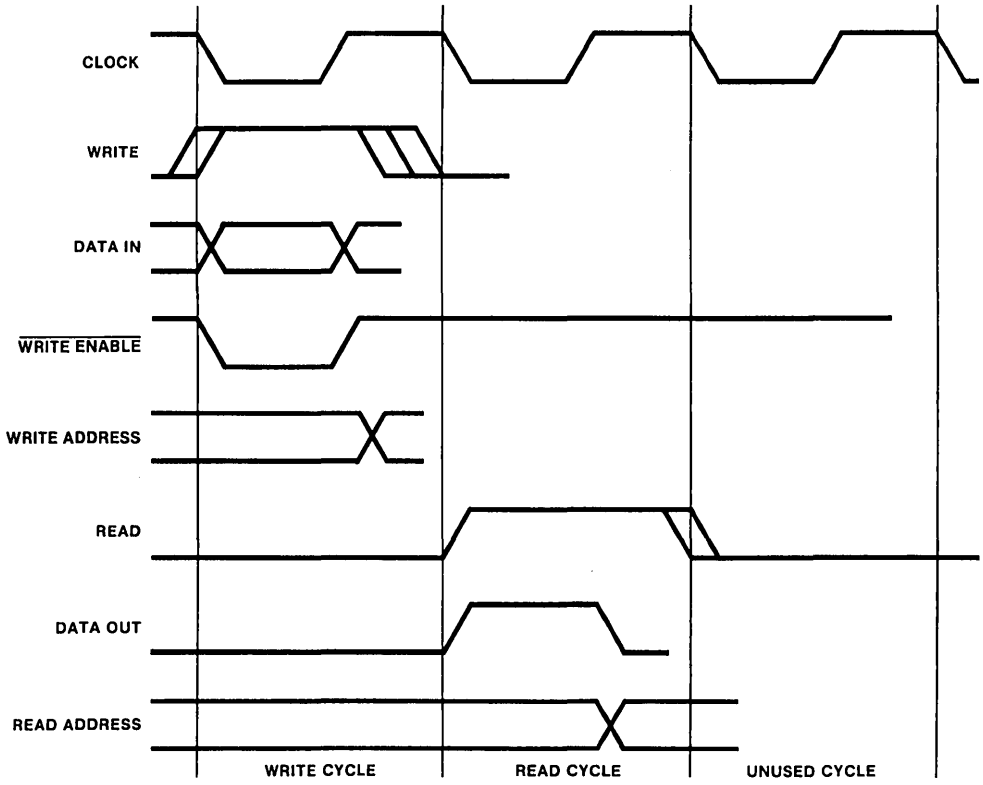

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FIGURE 2-22. FIFO Timing

Comparators

The F100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates either A > B, A < B, or $\overline{A = B}$.

The unequal outputs are active HIGH so that expansion is simple, *Figure 2-23* indicates how two 64-bit words may be compared in 5.4 ns typical. If desired, the $\overline{A = B}$ outputs of the first rank may be OR-wired to obtain an active-LOW $\overline{A = B}$ in 2.7 ns typical.

The F100107 Quint Exclusive-OR/NOR may be used as a 5-bit identity comparator with a propagation delay of 2.0 ns typical. The F100160 Parity Checker/Generator may also be used as an identity comparator.

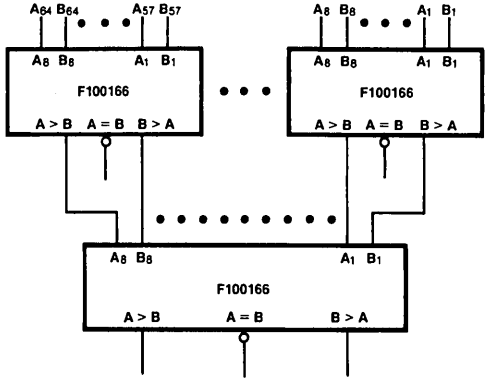

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FIGURE 2-23. 64-Bit Magnitude Comparator

Parity Generator/Checker

The F100160 is a dual 9-bit parity checker/generator. The output (of each section) is HIGH when an even number of inputs are HIGH. Thus, to generate odd parity on eight bits, the ninth input would be held HIGH. One of the nine inputs on each half has a shorter propagation (I_a, I_b) delay and is thus preferred for expansion.

Figure 2-24 shows how to build a 16-bit parity checker using a single F100160. The typical propagation delay from the longest input is 4.05 ns. This circuit can be turned into a parity generator by replacing "P" at input I_b with a LOW or HIGH for even or odd parity, respectively.

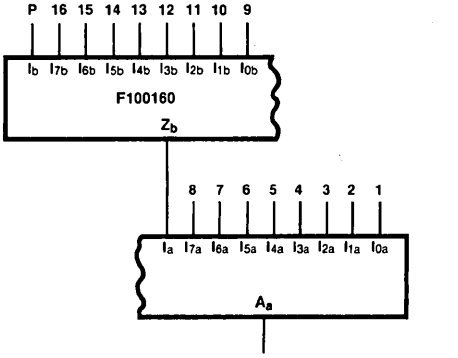

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FIGURE 2-24. 16-Bit Parity Checker/Generator

Arithmetic Logic Unit

The F100181 is a 4-bit binary/BCD ALU with a typical propagation delay of 4.5 ns. Output latches are provided to reduce system package count. When the latches are not required, they may be made transparent. Table 2-11 summarizes the functions available in the F100181. Table 2-12 is a summary of add times as a function of word width using the F100181 and, optionally, the F100179 Lookahead Carry Generator. These are calculated using maximum times for flatpak at 25°C from the data sheets and assume zero interconnection times. Further, it is assumed that the S (function select) inputs are available very early; their delay paths are ignored. The F100181 specification sheet indicates how the parts are interconnected.

TABLE 2-11. F100181 Functions

S_3	S_2	S_1	S_0	Function	Note
L	L	L	L	A Plus B BCD	
L	L	L	H	A Minus B BCD	
L	L	H	L	B Minus A BCD	
L	L	H	H	O Minus A BCD	
L	H	L	L	A Plus B Binary	
L	H	L	H	A Minus B Binary	
L	H	H	L	B Minus A Binary	
L	H	H	H	O Minus B Binary	
H	L	L	L	Identity	$F = A \bullet B + \overline{A} \bullet \overline{B}$
H	L	L	H	XOR	$F = A \bullet \overline{B} + \overline{A} \bullet B$
H	L	H	L	OR	$F = A + B$
H	L	H	H	A	$F = A$
H	H	L	L	Inverse	$F = \overline{B}$
H	H	L	H	B	$F = B$
H	H	H	L	AND	$F = A \bullet B$
H	H	H	H	Zero	F = LOW

H = HIGH Voltage Level
L = LOW Voltage Level

Arithmetic Logic Unit (Continued)

TABLE 2-12. Summary of Add Times Using F100181

Bits	Ripple Carry	1 F100179 Lookahead Carry	2 F100179 Lookahead Carries
8	11.3	n/a	n/a
16	16.9	11.9	n/a
32	28.1	14.7	14.6
64	50.5	n/a	17.4

Ripple Carry = (A or B to C_{n+4}) + (C_n to F) + ((D − 2)C_n to C_{n+4}) where D = number of 100181 devices

16-Bit, 1 Lookahead = (A or B to P or G) + (C_n to F) + (t_P of 100179)

32-Bit, 1 Lookahead = (A or B to P or G) + (C_n to F) + (t_P of 100179) + (C_n to C_{n+4} of last stage)

32-Bit, 2 Lookaheads = (A or B to P or G) + (C_n to F) + ($2t_p$ of 100179)

64-Bit, 2 Lookaheads = (A or B to P or G) + (C_n to F) + ($2t_P$ of 100179) + (C_n to C_{n+4} of last stage)

Multipliers

The F100182 Wallace Tree Adder and F100183 Recode Multiplier can be combined to build extremely fast parallel multipliers. The F100183 data sheet has detailed applications information; Table 2-13 is a summary of delay times and package counts for various operand sizes. The times are typical and do not include interconnection delays.

TABLE 2-13. Multiplier Summary

Operand Size	Delay (ns)	Device Count
16 × 16	16	62
24 × 24	22	115
32 × 32	24	186
64 × 64	26	634

TTL/F100K Interfacing

The F100124 is a hex translator, designed to convert TTL logic levels to F100K ECL logic levels. A common Enable input (E_C), when LOW, holds all true outputs LOW. Complementary outputs are available on each translator, allowing the circuits to be used as inverting, non-inverting, or differential translators. The TTL inputs present the loading factors indicated in Table 2-14.

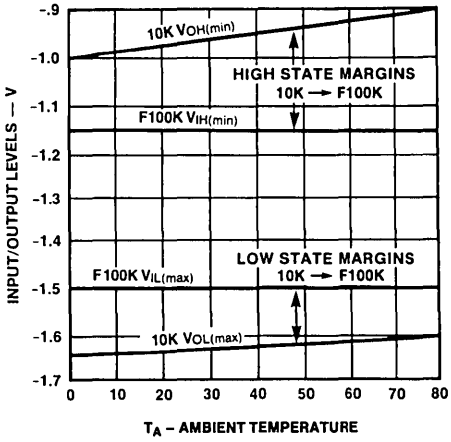
TABLE 2-14. F100124 Input Loading

Load	Current	Standard TTL Unit Loads
HIGH	50 μA	1.25
HIGH (Enable)	300 μA	7.5
LOW	−3.2 mA	2
LOW (Enable)	−16.0 mA	10

The F100125 is a hex F100K ECL-to-TTL translator. Differential inputs allow each circuit to be used as an inverting, non-inverting, or differential translator. An internal reference voltage generator provides V_{BB} for single-ended operation. The outputs of the F100125 have a fan-out of 50 standard TTL Unit Loads (U.L.) in the HIGH state and 12.5 in the LOW state.

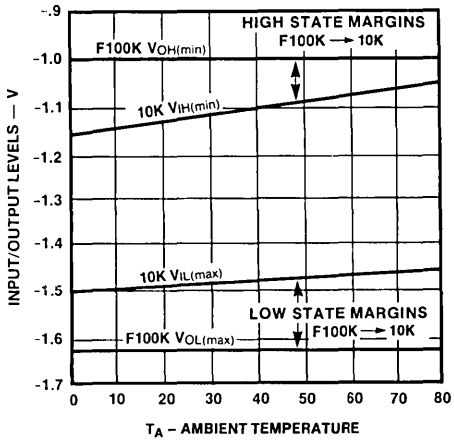
10K/F100K Interfacing

The problem caused by mixing 10K ECL and F100K ECL is illustrated in *Figures 2-25* and *2-26*. 10K output levels and input thresholds vary with temperature whereas F100K levels and thresholds remain essentially constant. This means that the noise margins vary with temperature, even if the temperatures of the driving and receiving circuits track. Perhaps the worst case is shown in *Figure 2-26*, which illustrates F100K driving 10K.



TL/F/9899-26

FIGURE 2-25. 10K ECL Driving 100K ECL



TL/F/9899-27

FIGURE 2-26. 100K ECL Driving 10K ECL

10K/F100K Interfacing (Continued)

At +75°C, the high margins are seen to be less than 100 mV. Clearly this would not represent acceptable DC margins in any real system.

If the use of 10K ECL in an F100K system is unavoidable, it is recommended that all interfacing be done differentially. This is illustrated in *Figure 2-27* which is applicable for either direction.

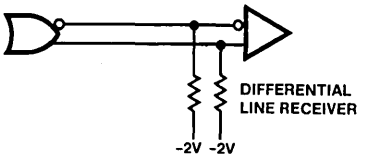


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FIGURE 2-27. Interfacing 10K and 100K

National Semiconductor

Chapter 3
Transmission Line Concepts

Introduction

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

Simplifying Assumptions

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

Characteristic Impedance

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal charge or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad (3\text{-}1)$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in Henries, C_0 in Farads.

Propagation Velocity

Propagation velocity ν and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$\nu = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \qquad (3\text{-}2)$$

Equations 3-1 and *3-2* provide a convenient means of determining the L_0 and C_0, of a line when delay, length and impedance are known. For a length *l* and delay T, δ is the ratio T/*l*. To determine L_0 and C_0, combine *Equations 3-1* and *3-2*.

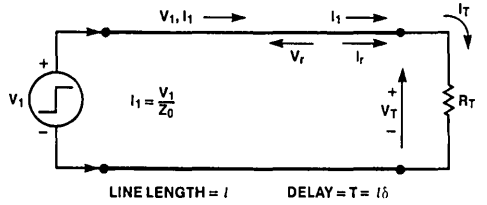
$$L_0 = \delta Z_0 \qquad (3\text{-}3)$$

$$C_0 = \frac{\delta}{Z_0} \qquad (3\text{-}4)$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1-3]

Termination and Reflection

A transmission line with a terminating resistor is shown in *Figure 3-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.



TL/F/9900–1

FIGURE 3-1. Assigned Polarities and Directions for Determining Reflections

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated by V_r and I_r in *Figure 3-1*, starts to return toward the generator. Applying

Termination and Reflection (Continued)

Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \qquad (3\text{-}5)$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

$$\text{thus} \quad I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \qquad (3\text{-}6)$$

$$\text{also} \quad I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1\left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r\left(\frac{1}{R_T} + \frac{1}{Z_0}\right) \qquad (3\text{-}7)$$

$$V_r = V_1\left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1$$

The term in parenthesis is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between −1 and +1 respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 3-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r \qquad (3\text{-}8)$$

then $V_T = V_1 (1 + \rho_L)$.

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 3-8* gives

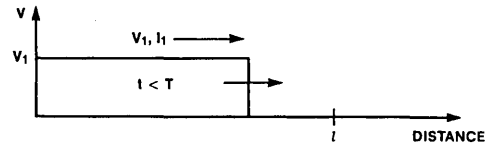
$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right) V_1 \qquad (3\text{-}9)$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r in *Figure 3-1* correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 3-7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence, I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, i.e., R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 3-2* for both cases of mismatch between R_T and Z_0.

The incident wave is shown in *Figure 3-2a*, before it has reached the end of the line. In *Figure 3-2b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 3-2c*, the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.



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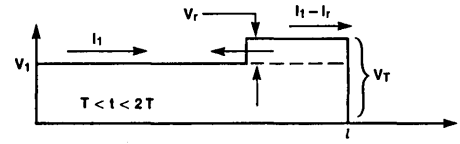
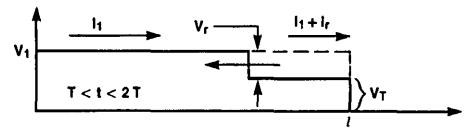
a. Incident Wave



TL/F/9900–3

b. Reflected Wave for $R_T > Z_0$



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c. Reflected Wave for $R_T < Z_0$

FIGURE 3-2. Reflections for $R_T \neq Z_0$

Source Impedance, Multiple Reflections

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \qquad (3\text{-}10)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

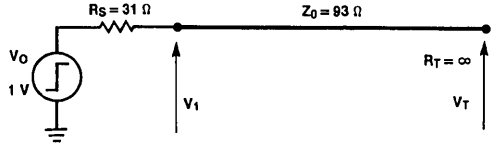
$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \qquad (3\text{-}11)$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 3-3*. The source is a step function of 1V amplitude occurring at time t_0. The initial value of V_1 starting down the line is 0.75V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 3-3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 3-3)* to 13Ω increases ρ_S to −0.75V, and the effects are illustrated in *Figure 3-4*. The initial value of V_T is 1.8V with a reflection of 0.9V from the open end. When this reflection reaches the source, a reflection of 0.9V × −0.75V starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9V × −0.75V starts back toward the source. This negative increment is again multiplied by −0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V'_T = (1 + \rho_L) V_1 - (1 + \rho_L) V_1 \rho^2_L \rho^2_S = (1 + \rho_L) V_1 (1 - \rho^2_L \rho^2_S). \qquad (3\text{-}12)$$

The factor $(1 - \rho^2_L \rho^2_S)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.



TL/F/9900–5

$$\rho_S = \frac{31 - 93}{31 + 93} = -0.5 \qquad \rho_L = \frac{\infty - 93}{\infty + 93} = +1$$

$$\text{Initially: } V_1 = \frac{Z_0}{Z_0 + R_S} \cdot V_0 = \frac{93}{124} \cdot 1 = 0.75V$$

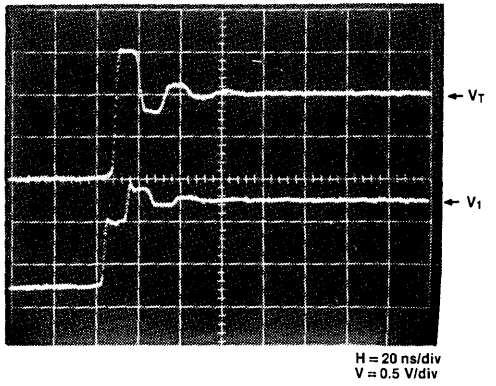


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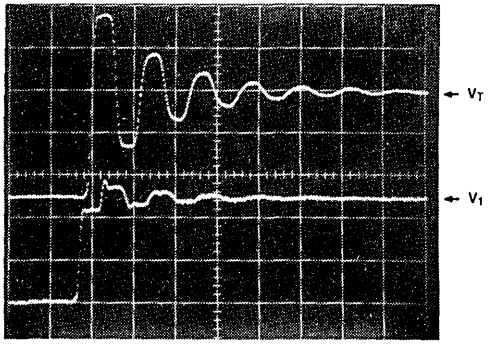
FIGURE 3-3. Multiple Reflections Due to Mismatch at Load and Source



TL/F/9900–7

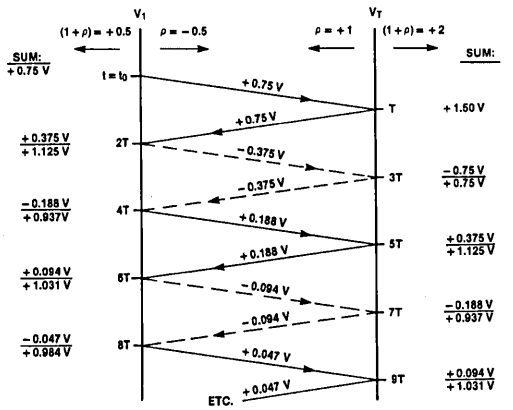
FIGURE 3-4. Extended Ringing when R_S of *Figure 3-3* is Reduced to 13Ω

Lattice Diagram

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 3-3* is shown in *Figure 3-5*.

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and (1 + ρ) at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1V, as they must with a 1V source driving an open-ended line.

Lattice Diagram (Continued)



TL/F/9900–8

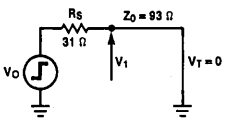
FIGURE 3-5. Lattice Diagram for the Circuit of *Figure 3-3*

Shorted Line

The open-ended line in *Figure 3-3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of −1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 3-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 3-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75V, which is inverted at the shorted end and returned toward the source as −0.75V. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a −0.37V net change in V_1. Concurrently, a reflected voltage of +0.37V (−0.75V times ρ_S of −0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

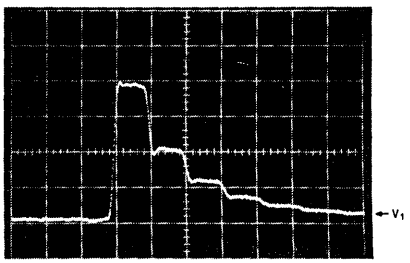
When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 3-6c*. The amplitude decreases by 50% with each successive occurrence as it did in *Figure 3-6b*.



TL/F/9900–9

$\rho_S = -0.5$ $\quad \rho_L = \dfrac{0 - 93}{0 + 93} = -1$

a. Reflection Coefficients for Shorted Line



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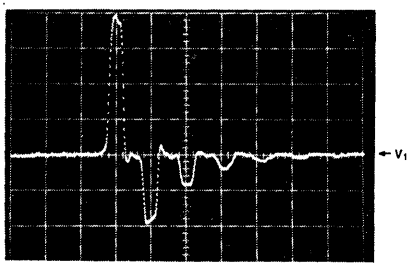
b. Input Pulse Duration ≫ Line Delay



TL/F/9900–11

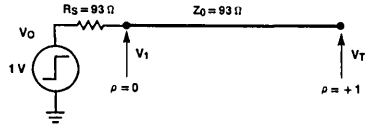
c. Input Pulse Duration < Line Delay

FIGURE 3-6. Reflections of Long and Short Pulses on a Shorted Line

Series Termination

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 3-7* shows a 93Ω line driven from a 1V generator through a source impedance of 93Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

An ECL output driving a series terminated line requires a pull-down resistor to V_{EE}, as indicated in *Figure 3-8*. The resistor R_0 shown in *Figure 3-8* symbolizes the output resistance of the ECL gate. The relationships between R_0, R_S, R_E and Z_0 are discussed in Chapter 4.



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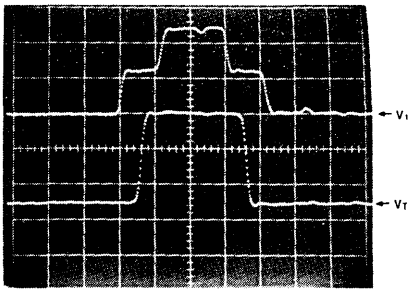
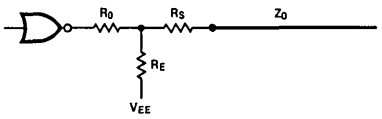


TL/F/9900–13

FIGURE 3-7. Series Terminated Line and Waveforms

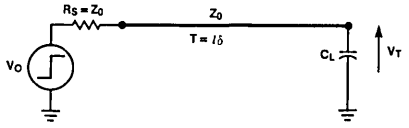


TL/F/9900–14

FIGURE 3-8. ECL Element Driving a Series Terminated Line

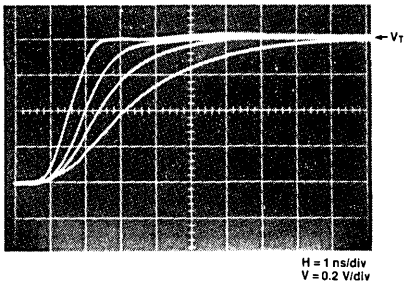
Extra Delay with Termination Capacitance

Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 3-9* shows how the output waveform changes with increasing load capacitance. *Figure 3-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.



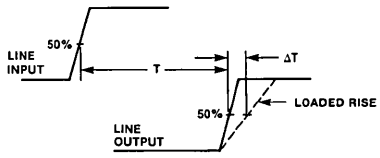
TL/F/9900–15

a. Series Terminated Line with Load Capacitance



TL/F/9900–16

b. Output Rise Time Increase with Increasing Load Capacitance

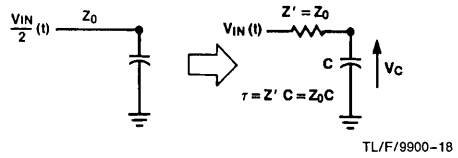


TL/F/9900–17

c. Extra Delay ΔT Due to Rise Time Increase

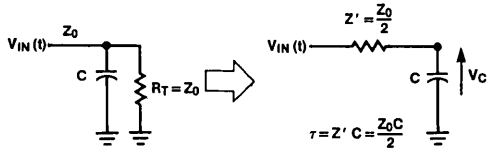
FIGURE 3-9. Extra Delay with Termination Capacitance

Extra Delay with Termination Capacitance (Continued)



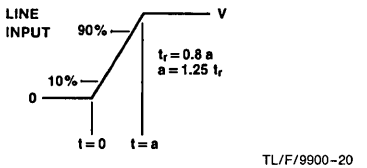
TL/F/9900–18

a. Thevenin Equivalent for Series Terminated Case



TL/F/9900–19

b. Thevenin Equivalent for Parallel Terminated Case



TL/F/9900–20

$$v_{in}(t) = \frac{V}{a}[\,tu(t) - (t-a)u(t-a)]$$

$$u(t) = \frac{0 \text{ for } t < O}{1 \text{ for } t > O}$$

$$u(t-a) = \frac{0 \text{ for } t < a,}{1 \text{ for } t > a}$$

$$V_{IN}(S) = \frac{V}{as^2}(1 - e^{-as})$$

$$V_C(S) = \frac{V}{ar} \bullet \frac{1}{s^2(s + 1/\tau)}(1 - e^{-as})$$

$$v_c(t) = \frac{V}{a}[t - \tau(1 - e^{-t/\tau})]\,u(t)$$

$$- \frac{V}{a}[(t-a)$$

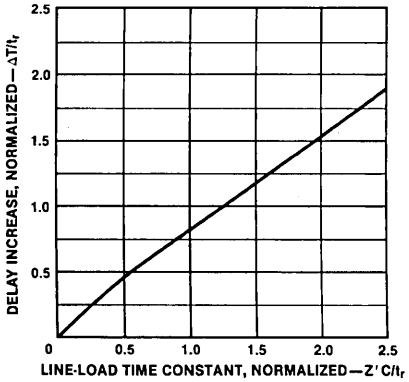
$$- \tau(1 - e^{-\frac{t-a}{\tau}})]\,u(t-a)$$

c. Equations for Input and Output Voltages

FIGURE 3-10. Determining the Effect of End-of-Line Capacitance

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 3-10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant τ, defined in *Figure 3-10a* and *3-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 3-11*, based on measured values, shows the increase in delay to the 50% point as a function of the Z′C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 3-10a*, Z′ is equal to 100Ω; the ratio Z′C/t_r is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z′ would be 50Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.



TL/F/9900–21

FIGURE 3-11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to T_r

Distributed Loading Effects on Line Characteristics

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 3-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 3-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 3-12b*, the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at $\approx -10\%$) for half its duration. This is about the same reflection that would occur if the 93Ω line had a middle section with an impedance reduced to 75Ω.

With a number of capacitors distributed all along the line of *Figure 3-12a*, the combined reflections modify the observed input waveform as shown in the top trace of *Figure 3-12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T >$ Z_0). This analogy is strengthened by observing the effect of reducing R_T from 93Ω to 75Ω, which leads to the middle waveform of *Figure 3-12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 3-12c* the source resistance R_S is reduced from 93Ω to 75Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

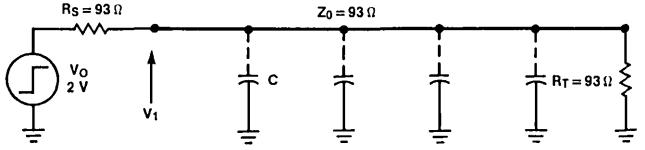
The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as *l*, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 3-1* to determine the reduced line impedance Z_0.

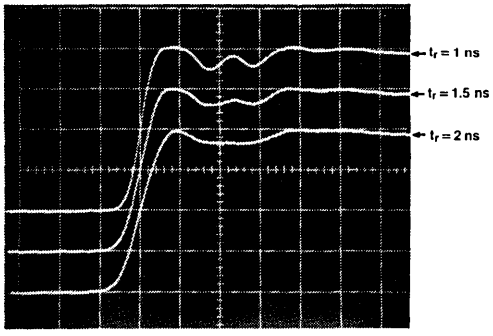
$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}} \qquad (3\text{-}13)$$

$$Z'_0 + \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$



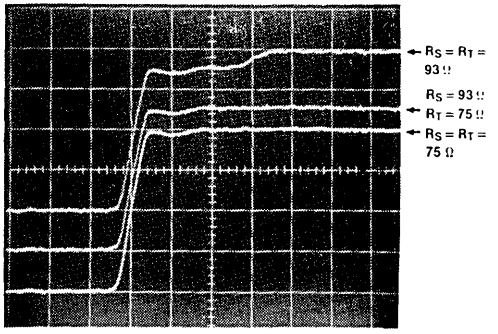
TL/F/9900–22

a. Arrangement for Observing Capacitive Loading Effects



TL/F/9900–23

b. Capacitive Reflections Merging as Rise Time Increases



TL/F/9900–24

c. Matching the Altered Impedance of a Capacitively Loaded Line

FIGURE 3-12. Capacitive Reflections and Effects on Line Characteristics

Distributed Loading Effects on Line Characteristics (Continued)

In the example of *Figure 3-12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance $/C_0$ is 60 pF. (Note that the ratio C_D/C_0 is the same as $C_L//C_0$.) The calculated value of the reduced impedance is thus

$$Z'_0 = \frac{93}{\sqrt{1+\frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\Omega \qquad (3\text{-}14)$$

This correlates with the results observed in *Figure 3-12c* when R_T and R_S are reduced to 75Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 3-2*.

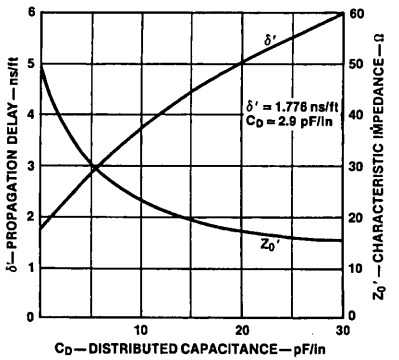
$$\delta' = \sqrt{L_0 (C_0 + C_D)} = \sqrt{L_0 C_0}\sqrt{1+\frac{C_D}{C_0}} = \delta\sqrt{1+\frac{C_D}{C_0}} \qquad (3\text{-}15)$$

The line used in the example of *Figure 3-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 3-15*.

$$/\delta' = /\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5\text{ ns} \qquad (3\text{-}16)$$

Equation 3-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

A plot of Z' and δ' for a 50Ω line as a function of C_D is shown in *Figure 3-13*. This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.



TL/F/9900–25

FIGURE 3-13. Capacitive Loading Effects on Line Delay and Impedance

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 3-9*.[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z'_0 - Z_0}{Z'_0 + Z_0} \qquad (3\text{-}17)$$

Mismatched Lines

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5% to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 3-14* and analyzed in the lattice diagram of *Figure 3-15*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 3-14*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \qquad (3\text{-}18)$$

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3 V_1 \qquad (3\text{-}19a)$$

$$V_2 = (1 + \rho_{12}) V_1 = +1.3 V_1 \qquad (3\text{-}19b)$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \qquad (3\text{-}20)$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$V_{2r} = \rho_{23} V_2 = -0.41 V_2 = (-0.41)(1.3) V_1 = -0.53 V_1 \qquad (3\text{-}21a)$$

$$V_3 = (1 + \rho_{23}) V_2 = 0.59 V_2 = (0.59)(1.3) V_1 = 0.77 V_1 \qquad (3\text{-}21b)$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$V_4 = (1 + \rho_L) V_3 = (1 + \rho_L)(1 + \rho_{23}) V_2 = (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) V_1 = (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12})\frac{V_0}{2} \qquad (3\text{-}22)$$

$$V_4 = (1 + \rho_{23})(1 + \rho_{12}) V_O$$

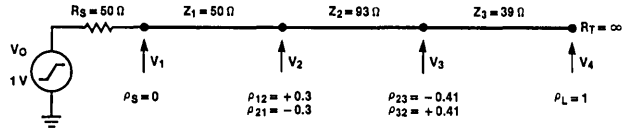
Thus, *Equation 3-22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

Mismatched Lines (Continued)

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 3-15* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 3-15)*.

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 3-16* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 3-16*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.



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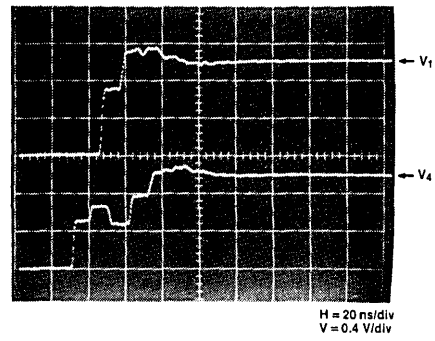

TL/F/9900–27

FIGURE 3-14. Reflections from Mismatched Lines

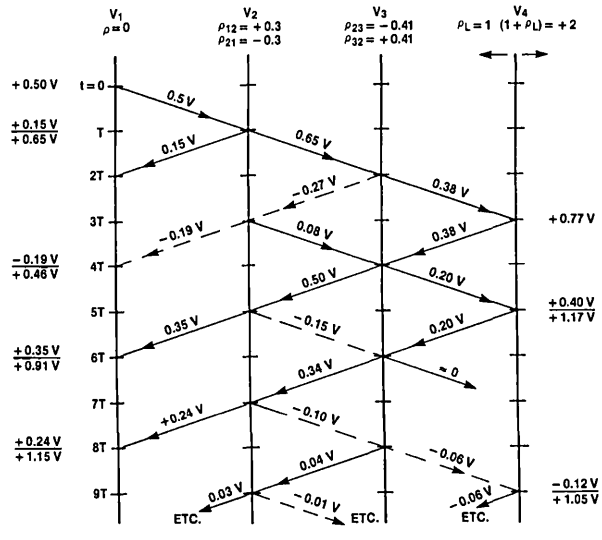

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FIGURE 3-15. Lattice Diagram for the Circuit of *Figure 3-14*

Mismatched Lines (Continued)

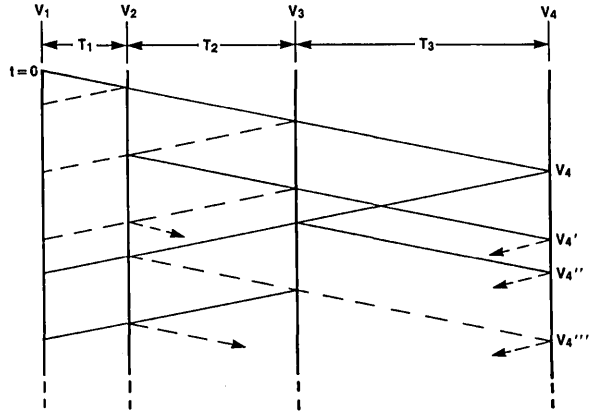

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FIGURE 3-16. Lattice Diagram for Three Lines with Delay Ratios 1:2:3

Rise Time versus Line Delay

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 3-17*, which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 3-17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1V. At time T later, V_T rises to 0.5V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of -0.4V, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 3-17c*, the input rise time (0% to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

The input rise time is increased to 4T in *Figure 3-17d*, with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 3-17e*, which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 3-17d* can be calculated by starting with the 1V input ramp.

$$V_1 = \frac{1}{t_r} \bullet t \quad \text{for } 0 \le t \le 4T \tag{3-23}$$

$$= 1V \quad \text{for } t \ge 4T$$

The reflection from the end of the line is

$$V_r = \frac{\rho_L (t - 2T)}{t_r}; \tag{3-24}$$

the portion of the reflection that appears at the input is

$$V'_r = \frac{(1 + \rho_S)\,\rho_L (t - 2T)}{t_r}; \tag{3-25}$$

the net value of the input voltage is the sum.

$$V'_1 = \frac{t}{t_r} + \frac{(1 + \rho_S) + \rho_L (t - 2T)}{t_r} \tag{3-26}$$

The peak value of the input voltage in *Figure 3-17d* is determined by substituting values and letting t equal 4T.

$$V'_1 = 1 + \frac{(0.8)(-0.5)(4T - 2T)}{t_r} \tag{3-27}$$

$$= 1 - 0.4\,(0.5) = 0.8V$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

Rise Time versus Line Delay (Continued)

$V'_{1(t)} = V_{1(t)}$
for $0 < t < 2T$

$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)}$
for $2T < t < 4T$

$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)}$ (3-28)
for $4T < t < 6T$

$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)} + (1 + \rho_S)\,\rho_S^2\rho_L^3\,V_{1(t-6T)}$
for $6T < t < 8T$, etc.

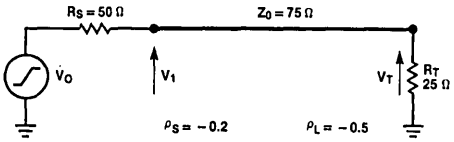
The voltage at the output end of the line is expressed in a similar manner.

$V_{T(t)} = 0$
for $0 < t < T$

$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)}$
for $T < t < 3T$

$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t-3T)}$ (3-29)
for $3T < t < 5T$

$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L V_{1(t-3T)} + (1 + \rho_L)\,\rho_S^2\rho_L^2\,V_{1(t-5T)}$
for $5T < t < 7T$, etc.



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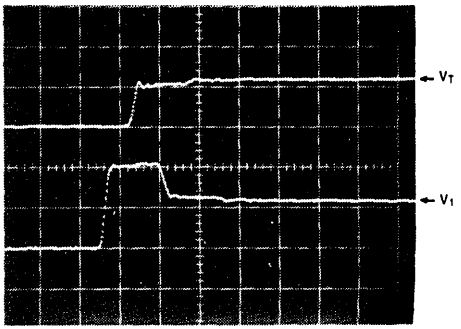
a. Test Arrangement for Rise Time Analysis



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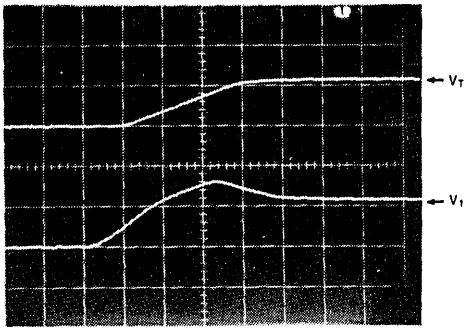
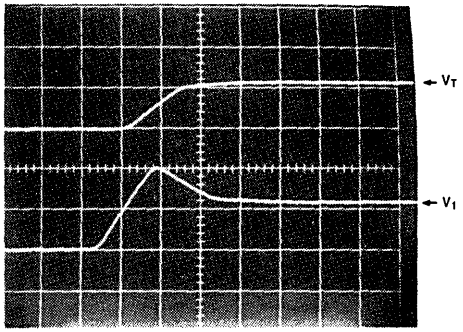
b. Line Voltages for $t_r \ll T$



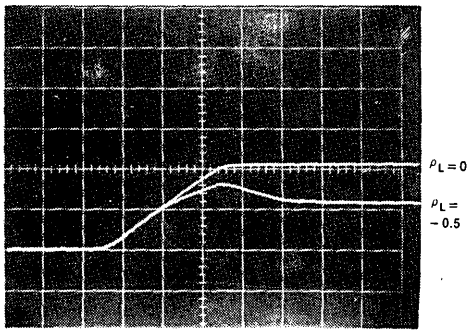
TL/F/9900–33

d. Line Voltages for $t_r = 4T$



TL/F/9900–32

c. Line Voltages for $t_r = 2T$



TL/F/9900–34

e. Input Voltage with and without Reflection

FIGURE 3-17. Line Voltages for Various Ratios of Rise Time to Line Delay

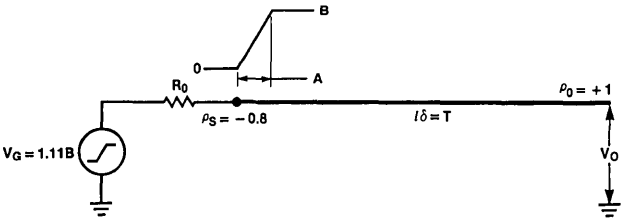
Ringing

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 3-18*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is +1 and the source reflection coefficient is assumed to be −0.8, i.e., $R_0 = Z_0/9$.

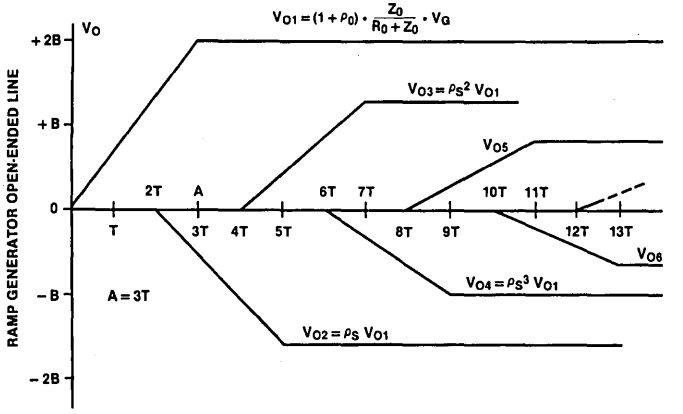
Figure 3-18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_O rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by −0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to −1.6B at time 2T + A.

The negative-going increment also generates a reflection of amplitude −0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T + A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.



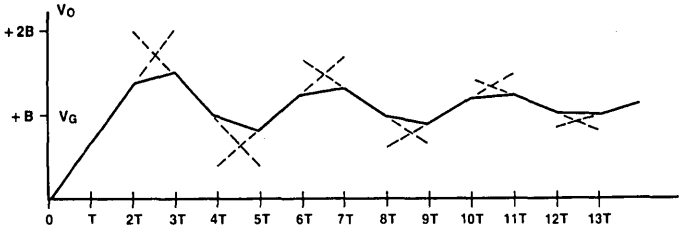
TL/F/9900–35

a. Ramp Generator Driving Open-Ended Line



TL/F/9900–36

b. Increments of Output Voltage Treated Individually



TL/F/9900–37

c. Net Output Signal Determined by Superposition

FIGURE 3-18. Basic Relationships Involved in Ringing

Ringing (Continued)

In *Figure 3-18c*, the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (i.e., 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 3-18c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 3-18*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

Summary

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, i.e., at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

References

1. Metzger, G. and Vabre, J., *Transmission Lines with Pulse Excitation*, Academic Press, (1969).
2. Skilling, H., *Electric Transmission Lines*, McGraw-Hill, (1951).
3. Matick, R., *Transmission Lines for Digital and Communication Networks*, McGraw-Hill, (1969).
4. Millman, J. and Taub, H., *Pulse Digital and Switching Waveforms*, McGraw-Hill, (1965).
5. "Time Domain Reflectometry", *Hewlett-Packard Journal*, Vol. 15, No. 6, (February 1964).
6. Feller, A., Kaupp H., and Digiacoma, J., "Crosstalk and Reflections in High-Speed Digital Systems", *Proceedings, Fall Joint Computer Conference*, (1965).

National Semiconductor

CHAPTER 4
System Considerations

Introduction

All of National's ECL input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Specific guidelines and recommendations are based on assumed worst-case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

PC Board Transmission Lines

Strictly speaking, transmission lines are not always required for F100K ECL but, when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 4-1*. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards. Other board construction techniques are wire wrap, stitch weld and discrete wired.

Stripline, *Figure 4-1b*, is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 14 layers have been used in ECL systems.

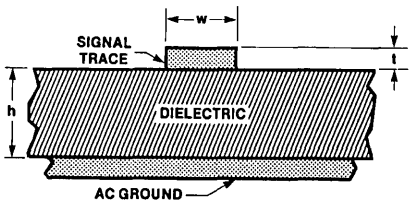
Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 4-1a*, the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 4-1c*.

Microstrip

Equation 4-1 relates microstrip characteristic impedance to the dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\,\epsilon_r + 0.67}}\right) \ln\left(\frac{4h}{0.67\,(0.8\,w + t)}\right) = \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \ln\left(\frac{5.98\,h}{0.8\,w + t}\right) \quad \textbf{(4-1)}$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air.



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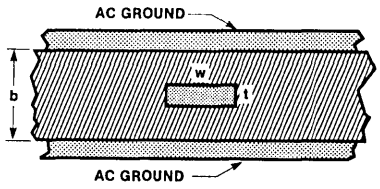
a. Microstrip



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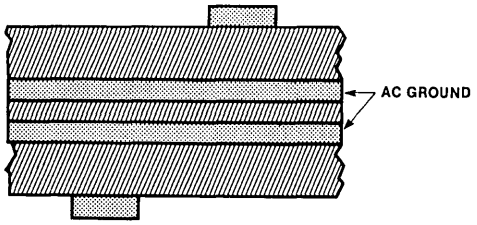
b. Stripline



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c. Composite Microstrip

FIGURE 4-1. Transmission Lines on Circuit Boards

PC Board Transmission Lines (Continued)

Equation 4-1 was developed from the impedance formula for a wire over ground plane transmission line, Equation 4-2.

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4h}{d}\right) \qquad \textbf{(4-2)}$$

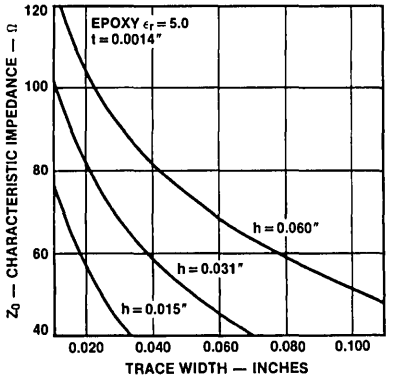
where d = wire diameter, h = distance from ground to wire center.

Comparing Equation 4-1 and 4-2, the term 0.67 (0.8 w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip ϵ_e, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.016 \bullet \sqrt{\epsilon_e}\ \text{ns/ft} \qquad \textbf{(4-3)}$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.016 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.04.



TL/F/9901–4

FIGURE 4-2. Microstrip Impedance Versus Trace Width, G-10 Epoxy

Using ϵ_r = 5.0 in Equation 4-1, *Figure 4-2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 4-3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, (Equation 3-15).

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

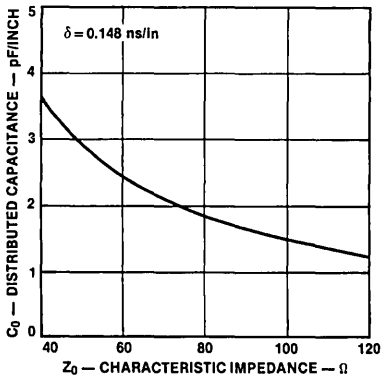


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FIGURE 4-3. Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

Stripline

Stripline conductors are totally embedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. Equation 4-4 is used to calculate stripline impedances.[1,2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4b}{0.67\,\pi\,(0.8\,w + t)}\right) \qquad \textbf{(4-4)}$$

where b = distance between ground planes, w = trace width, t = trace thickness, w/(b-t) < 0.35 and t/b < 0.25.

Figure 4-4 shows stripline impedance as a function of trace width, using Equation 4-4 and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 4-5*.

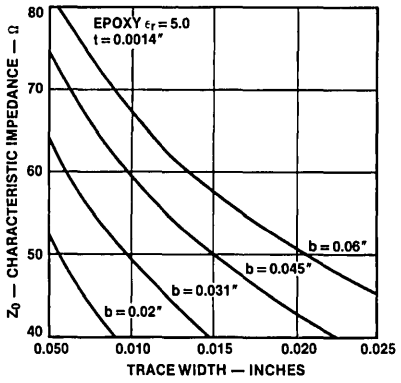

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FIGURE 4-4. Stripline Impedance Versus Trace Width, G-10 Epoxy

PC Board Transmission Lines (Continued)

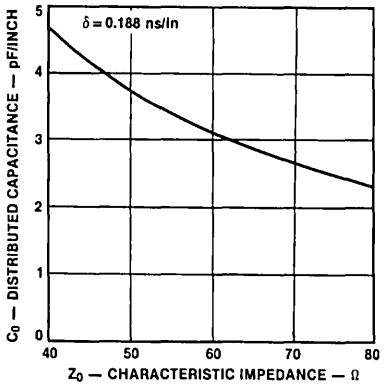

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FIGURE 4-5. Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy

Wire Wrap

Wire-wrap boards are commercially available with three voltage planes, positions for several 24-pin Dual-In-Line Packages (DIP), terminating resistors, and decoupling capacitors. The devices are mounted on socket pins and interconnected with twisted pair wiring. One wire at each end of the twisted pair is wrapped around a signal pin, the other around a ground pin. The #30 insulated wire is uniformly twisted to provide a nominal 93Ω impedance line. Positions for Single-In-Line Package (SIP) terminating resistors are close to the inputs to provide good termination characteristics.

Stitch Weld

Stitch-weld boards are commercially available with three voltage planes and buried resistors between planes. The devices are mounted on terminals and interconnected with insulated wires that are welded to the backside of the terminals. The insulated wires are placed on a controlled thickness over the ground plane to provide a nominal impedance of 50Ω. The boards are available for both DIPs and flatpaks. Use of flatpaks can increase package density and provide higher system performance.

Discrete Wired

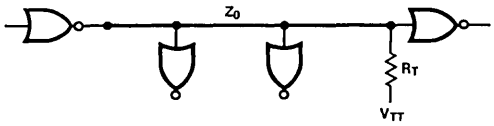
Custom Multiwire* boards are available with integral power and ground planes. Wire is placed on a controlled thickness above the ground plane to obtain a nominal impedance line of 55Ω. Then holes are drilled through the wire and board. Copper is deposited in the drilled holes by an additive-electrolysis process which bonds each wire to the wall of the holes. Devices are soldered on the board to make connection to the wires.

*Multiwire is a registered trademark of the Multiwire Corporation.

Parallel Termination

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 4-6a*. F100K circuits do not have internal pull-down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A −2V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE} supply can provide the Thevenin equivalent of a single resistor to −2V if a separate termination supply is not available, *Figure 4-6b*. The average power dissipation in the Thevenin equivalent resistors is about 10 times the power dissipation in the single resistor returned to −2V, as shown in *Figures 5-10* and *5-13*. For either parallel termination method, decoupling capacitors are required between the supply and ground (Chapter 6).

a. Parallel Termination



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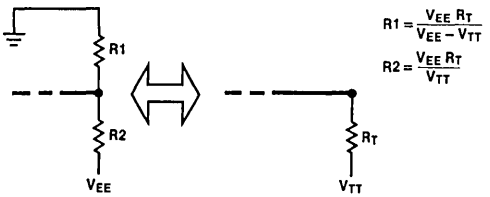
b. Thevenin Equivalent of R_T and V_{TT}



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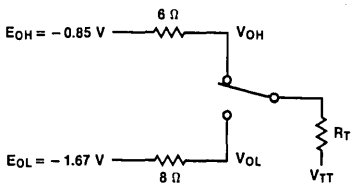
c. Equivalent Circuit for Determining Approximate V_{OH} and V_{OL} Levels



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d. F100K Output Characteristic with Terminating Resistor R_T Returned to V_{TT} = −2.0V

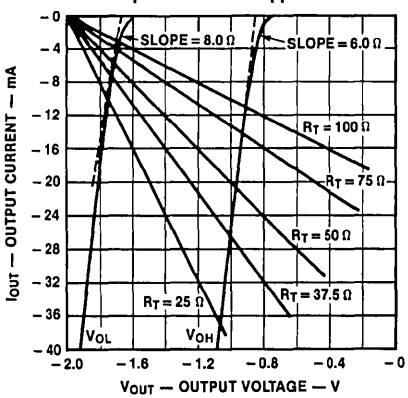

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FIGURE 4-6. Parallel Termination

PC Board Transmission Lines (Continued)

F100K output transistors are designed to drive low-impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50Ω load returned to −2V. This gives nominal output levels of −0.955V at 20.9 mA and −1.705V at 5.9 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base-emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50Ω load, the effective source resistance is approximately 6Ω in the HIGH state and 8Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in *Figure 4-6c*. The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6Ω and 8Ω respectively. The values shown for E_{OH} and E_{OL} are −0.85V and −1.67V respectively.

The linearized portion of the F100K output characteristic can be represented by two equations:

For V_{OH}: $V_{OUT} = -850 - 6\ I_{OUT}$
For V_{OL}: $V_{OUT} = -1670 - 8\ I_{OUT}$

where I_{OUT} is in mA, V_{OUT} is in mV.

If the range of I_{OUT} is confined between 8 mA to 40 mA for V_{OH}, and 2 mA to 16 mA for V_{OL}, the output voltage can be estimated within ±10 mV *(Figure 4-6d)*.

An ECL output can drive two or more lines in parallel, provided the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75Ω terminations to −2V (*Figure 4-6d*) give output levels of approximately −1.000V and −1.716V. Noise margins are thus 35 mV less in the HIGH state and 11 mV more in the LOW state, compared to 50Ω load conditions. Conversely, a single 75Ω load to −2V causes noise margins 38 mV greater in the HIGH state and 11 mV less in the Low state, compared to a 50Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_O. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ.

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad \textbf{(4-5)}$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2R_T}{R_T + Z_0} \qquad \textbf{(4-6)}$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst-case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging Equation 4-5.

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad \textbf{(4-7)}$$

Using 15% reflection limits as examples, the range of the R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \quad 1.35 > \frac{R_T}{Z_0} > 0.74 \qquad \textbf{(4-8)}$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ±10% allow Z_0 tolerance limits of +22% and −19%; R_T tolerances of ±5% allow Z_0 tolerance limits of +28% and −23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter-follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0. Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product $I_{OH}\ Z_0$.

If the $I_{OH}\ Z_0$ product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH}\ Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge such as the one shown in *Figure 4-14*. In the output-LOW state the emitter follower is essentially nonconducting for V_{OL} values more positive than about −1.55V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of *Figure 4-6c*, an upper limit on the value of R_T can be developed.

$$\Delta V = I_{OH} Z_0 > 1.55 - |V_{OH}|$$

$$\left(\frac{E_{OH} - V_{TT}}{R_0 + R_T}\right) Z_0 > 1.55 - \left|\frac{V_{TT}\ R_0 = E_{OH} R_T}{R_0 + R_T}\right|$$

$$R_T < \frac{(E_{OH} - V_{TT})\ Z_0 - (1.55 - |V_{TT}|)\ R_0}{1.55 - |E_{OH}|} \qquad \textbf{(4-9)}$$

For a V_{TT} of −2V, R_0 of 6Ω and E_{OH} of −0.85V, Equation 4-9 reduces to

$R_T < 1.64\ Z_0 + 3.86\Omega$

For $Z_0 = 50\Omega$, the emitter follower cuts off during a negative-going transition if R_T exceeds 86Ω. Changing the voltage level criteria to −1.60V to insure continuous conduction in the emitter follower gives an upper limit of 77Ω for a 50Ω line. For a line terminated at the receiving end with a resistance to −2V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 50%. This insures a satisfactory negatve-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

Input Impedance

The input impedance of ECL circuits is predominately capacitive. A single-function input has an effective value of about 1.5 pF for F100K flatpak, as determined by its effect on reflected and transmitted signals on transmission lines.

Input Impedance (Continued)

In practical calculations, a value of 2 pF should be used. Approximately one third of this capacitance is attributed to the internal circuitry and two thirds to the flatpak pin and internal bonding.

For F100K flatpak circuits, multiple input lines may appear to have up to 3 pF to 4 pF but never more. For example, in the F100102, an input is connected internally to all five gates, but because of the philosophy of buffering these types of inputs in the F100K family this input appears as a unit load with a capacitance of approximately 2 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive-LOW output can be taken as 2 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 3. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figure 4-3* and *4-5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ (Equation 4-3) by the line impedance Z_0.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figure 4-10)*. The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

Series Termination

Series termination requires a resistor between the driver and transmission line, *Figure 4-7*. The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to a full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In *Figure 4-7*, one load is shown connected at point D, aways from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated line *(Figure 4-10)*.

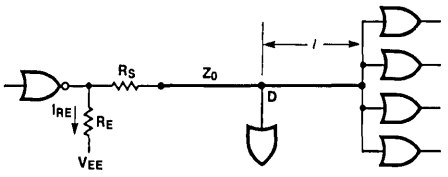

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FIGURE 4-7. Series Termination

The signal at the end has a slower rise time that the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product line impedance and load capacitance is discussed in Chapter 3.

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E *(Figure 4-7)*, which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical switch which opens to initiate the negative-going swing. At this instant, Z_O acts as a linear resistor returned to V_{OH}. Thus the components form a simple circuit of R_E, R_S and Z_0 in a series, connected between V_{EE} and V_{OH}. The initial current in this series circuit must be sufficient to introduce a 0.38V transient into the line, which then doubles at the load end to give 0.75V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + P_S + Z_0} \geq \frac{0.38}{Z_0} \qquad \textbf{(4-10)}$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should be ignored when calculating R_E.

Increasing the minimum signal swing into the line by 30% to 0.49V insures sufficient pull-down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.49}{Z_0} \qquad \textbf{(4-11)}$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.955V and $V_{EE} = -4.5V$. The value of R_S is equal to Z_0 minus R_0 (R_0 averages 7Ω). Inserting these values and rearranging Equation 4-11 gives the following.

$$R_E \leq 5.23\, Z_0 + 7\Omega \qquad \textbf{(4-12)}$$

Power dissipation in R_E is listed in *Figure 5-14*. The power dissipation in R_E is greater than in R_T of a parallel termination to −2V, but still less than the two resistors of the Thevenin equivalent parallel termination, see *Figure 5-10, 5-13* and *5-14*.

The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of

Series Termination (Continued)

inputs, with a worst-case value of 265 μA for simple gate inputs. The voltage drop subtracts from the HIGH-state noise margin as outlined in *Figure 4-8a*.

However, there is more HIGH-state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50Ω load to −2V. This makes V_{OH} more positive; the increase ranges from 43 mV for a 50Ω line to 82 mV for a 100Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH-state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_0 (= Z_0)$ gives the allowed load input current (Ix in *Figure 4-8a*). This works out to 0.86 mA for a 50Ω line, 0.92 mA for a 75Ω line and 0.82 mA for a 100Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 1.86 mA, 1.59 mA and 1.32 mA for 50Ω, 75Ω and 100Ω lines respectively.

An ECL output can drive more than one series terminated line, as suggested in *Figure 4-8b*, if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_0. This voltage drop decreases the HIGH-state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application.

The appropriate R_E value can be determined using Equation 4-13 for $V_{EE} = -4.5V$.

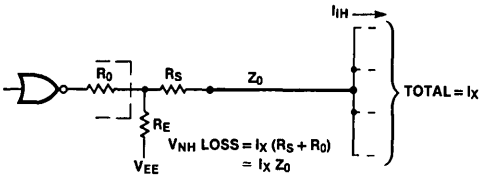
$$\frac{1}{R_E} \geq \frac{1}{6.23\,Z_1 - R_{S1}} + \frac{1}{6.23\,Z_2 - R_{S2}} + \frac{1}{6.23\,Z_3 - T_{S3}} \qquad \textbf{(4-13)}$$

Circuits with multiple outputs (such as the F100112) provide an alternate means of driving several lines simultaneous *(Figure 4-8c)*. Note, each output should be treated individually when assiging load distribution, line impedance, and R_E value.

Unterminated Lines

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately −0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments if the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 3, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines that on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, *(Figure 4-9a)* making V_{OH} higher and V_{OL} lower.



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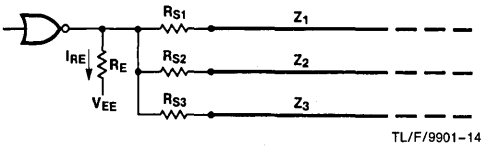
a. Noise Margin Loss Due to Load Input Current



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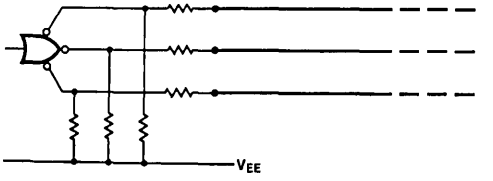
b. Driving Several Lines from one Output



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c. Using Multiple Output Element for Load Sharing

FIGURE 4-8. Loading Considerations for Series Termination

For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

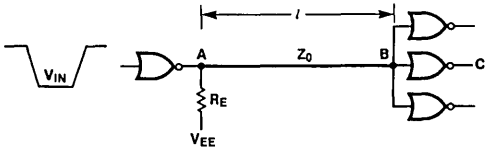
For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 3 and incorporating the effects of load capacitance on line delay.

$$t_r = 2T' = 2\ell\delta' = 2\ell\delta\sqrt{1 + \frac{C_L}{\ell C_0}}$$

Solving this expression for the line length (ℓ):

$$\ell_{max} = \frac{1}{2}\sqrt{\left(\frac{C_L}{C_0}\right)^2 + \left(\frac{t_r}{\delta}\right)^2} - \frac{C_L}{2C_0} \qquad \textbf{(4-14)}$$

Unterminated Lines (Continued)



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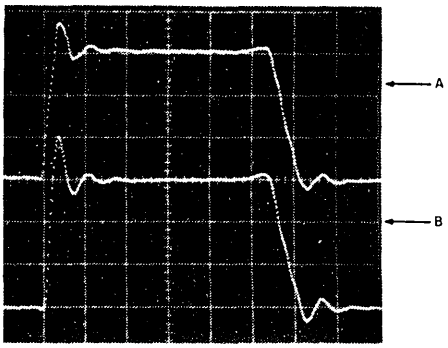
a. Unterminated Line



H = 10 ns/div
V = 0.3 V/div

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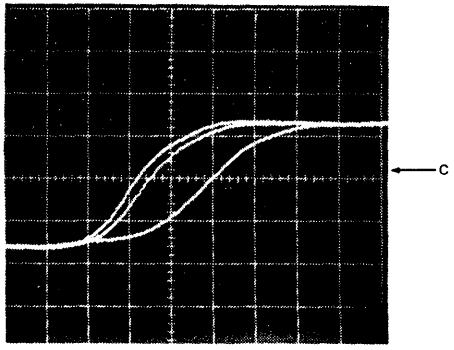
b. Line Voltages Showing Stair-step Trailing Edges



H = 1 ns/div
V = 0.3 V/div

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c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E: 330Ω, 510Ω, 1 kΩ

FIGURE 4-9. Effect on R_E Value on Trailing-Edge Propagation

The shorter the rise time, the shorter the premissible line length. For F100K ECL, the minimum rise time from 20% to 80% is specified as 0.5 ns. Using this rise time and 2 pF per fan-out load, calculated maximum line lengths for G-10 epoxy microstrip are listed in *Figure 4-10a*. The length (ℓ) in the table is the distance from the terminating resistor to the input of the device(s). For F100K ECL the case described in *Figure 4-10a* is the only one calculated, since all other combinations are approximately the same. For other combinations of rise time, impedance, fan-out or line characteristics (δ and C_0), maximum lengths are calculated using Equation 4-14. For the convenience of those who are also using 10K ECL, maximum recommended lengths of unterminated lines are listed in *Figure 4-10b* to *4-10e*.

FIGURE 4-10. Maximum Worst-Case Line Lengths for Unterminated Lines

Z_0	Number of Fan-Out Loads			
	1	2	3	4
50	1.37*	1.13	0.95	0.81
62	1.33	1.07	0.87	0.70
75	1.25	0.95	0.75	0.61
90	1.18	0.85	0.66	0.53
100	1.15	0.82	0.61	0.49

*Length in inches.
Unit load = 2 pF, δ = 0.148 ns/inch

FIGURE 4-10a. F100K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

Z_0	Number of Fan-Out Loads				
	2	3	4	6	8
50	4.15*	3.75	3.45	2.85	2.45
62	3.95	3.50	3.15	2.55	2.10
75	3.75	3.25	2.85	2.25	1.85
90	3.55	3.00	2.60	2.00	1.60
100	3.45	2.85	2.45	1.85	1.45

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/in.

FIGURE 4-10b. 10K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

Z_0	Number of Fan-Out Loads				
	1	2	4	6	8
50	4.40*	3.65	2.60	1.90	1.40
62	4.30	3.45	2.30	1.60	1.15
75	4.20	3.20	2.05	1.40	0.95
90	4.05	2.95	1.75	1.05	0.65
100	3.90	2.80	1.60	0.90	0.50

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/in.

FIGURE 4-10c. 10K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Concentrated Loading

Z_0	Number of Fan-Out Loads				
	2	3	4	6	8
50	3.30*	3.00	2.70	2.25	2.90
62	3.15	2.80	2.50	2.00	1.65
75	3.00	2.60	2.25	1.80	1.45
90	2.80	2.40	2.05	1.55	1.25

*Length in inches.
Unit load = 3 pF, δ = 0.188 ns/in.

FIGURE 4-10d. 10K Maximum Worst-Case Line Lengths for Unterminated Stripline, Distributed Loading

Unterminated Lines (Continued)

Z_0	Number of Fan-Out Loads				
	1	2	4	6	8
50	3.45*	2.85	2.00	1.50	1.10
62	3.40	2.70	1.80	1.30	0.90
75	3.30	2.55	1.60	1.10	0.75
90	3.15	2.35	1.40	0.85	0.50
100	3.10	2.20	1.25	0.70	0.40

*Length in inches.
Unit load = 3 pF, δ = 0.188 ns/in.

FIGURE 4-10e. 10K Maximum Worst-Case Line Lengths for Unterminated Stripline, Concentrated Loading

A load capacitance concentrated at the end of the line restricts line length more than a distributed load does. Maximum recommended lengths for fiberglass epoxy dielectric and a 0.5 ns rise time are listed in *Figure 4-10* for microstrip. For line impedances not listed, linear interpolation can be used to determine appropriate line lengths. Appropriate line lengths for dielectric materials with a different propagation constant δ can be determined by multiplying the listed values by the fiberglass epoxy δ and then dividing by the δ of the other material. For example, a line length for a material which has a microstrip δ of 0.1 ns/inch is determined by multiplying the length given in the microstrip table (for a desired impedance and load) by 0.148 and dividing by 0.1.

Resistor R_E must provide the current for the negative-going signal at the driver output. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 4-9b*. The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 4-9c* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330Ω. Changing R_E to 510Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 kΩ produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial negative-going step of 0.6V at the driving end of the line. This gives an upper limit on the value of R_E, as shown in Equation 4-15.

$$\text{initial step} = \Delta \ell \bullet Z_0 = \frac{(V_{OH} - V_{EE})\, Z_0}{R_E + Z_0} \geq 0.6$$

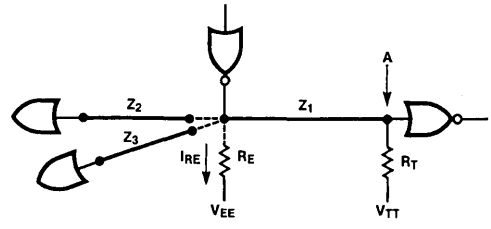
$$R_E = \leq 6.25\, Z_0 \qquad \textbf{(4-15)}$$

An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from Equation 4-15, using the parallel impedance of the two or more lines for Z_0.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 4-11a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case unterminated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 4-11b*. The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current through R_T and the negative-going signal swing was discussed earlier in connection with parallel termination.

The bottom trace in *Figure 4-11* shows the effect of connecting two stubs to the driver output. The steps in trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increas-

a. Multiple Lines



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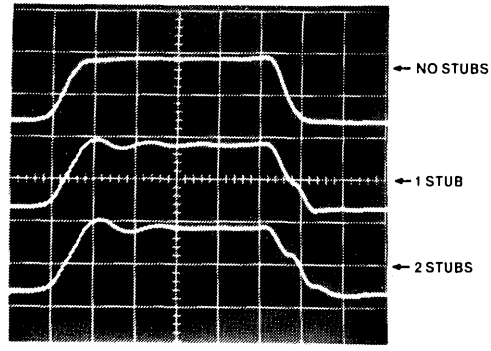
b. Waveforms at Termination Point A



H = 5 ns/div
V = 0.5 V/div

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c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output

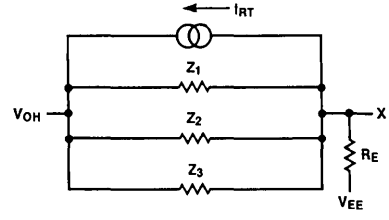

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FIGURE 4-11. Driving Terminated and Unterminated Lines in Parallel

Unterminated Lines (Continued)

es the switching time of the cirucit connected to point A. If this extra delay cannot be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 4-11a*. The initial negative-going step at point A should be about 0.7V to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7V. If the driver output is treated as a switch that opens to initiate the negative-going signal, the equivalent circuit of *Figure 4-11c* can be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T. Using Z' to denote the parallel impedance of the transmission lines and ΔV for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

$$R_E = \left(|V_{EE}| - |V_{OH}| - \Delta V|\right) \bullet \left(\frac{Z'}{|\Delta V| - |I_{RT}|Z'}\right)$$

For a sample calculation, assume that R_T and the line impedances are each 100Ω, V_{OH} is −0.955V, ΔV is 0.750V, V_{EE} is −4.5V and V_{TT} is −2V. I_{RT} is thus 10.45 mA and the calculated value of R_E is 232Ω. In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

Again, the foregoing example is based on worst-case stub lengths (the longest permissible). With shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.

The many combinations of line impedance and load make it practically impossible to define just with stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figure 4-10*.

Data Bussing

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 4-12)*. Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. *For calculating the modified delay of the line (Chapter 3) the capacitance of a LOW (unselected) driver output should be taken as 2 pF.*

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedance less than 100Ω, the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH-state noise margin. This loss can be eliminated if necessary by

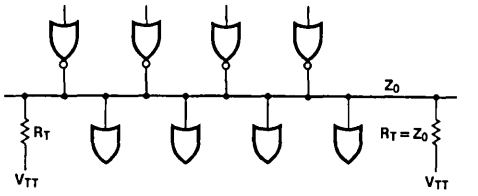

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FIGURE 4-12. Data Bus or Party Line

using multiple output gates (F100112) and paralleling two outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100Ω line terminated at both ends represents a net 50Ω DC load, which is the same as the data sheet condition for V_{OL}. If one worst-case output were conducting all the current, the V_{OL} would be −1.705V. If another output with identical DC characteristics shares the load current equally, the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW-state noise margin is specified greater than the HIGH-state margin to allow for V_{OL} shift when outputs are paralleled.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, i.e., the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

Wired-OR

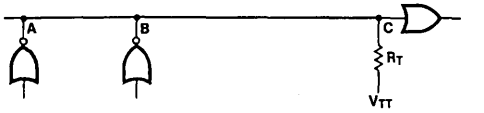
In general-purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net re-

Wired-OR (Continued)

sult is a "V" shaped negative glitch whose amplitude and duration depend on three factors: current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about one inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra wiring time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 4-13*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.



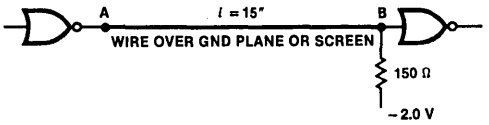
TL/F/9901–23

FIGURE 4-13. Relative to Wired-OR Propagation

Backplane Interconnections

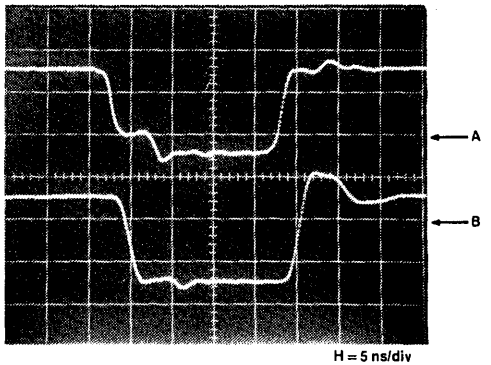
Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment, and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

For single-wire transmission through the backplane, a ground plane or ground screen (Chapter 5) should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 4-14* illustrates the effects of impedance variations with a 15-inch wire parallel terminated with 150Ω to −2V. *Figure 4-14b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane.



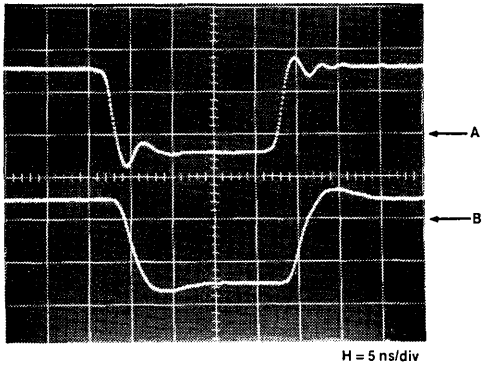
TL/F/9901–24

a. Wire over Ground Plane or Screen



TL/F/9901–25

b. Wire in Contact with Ground Plane



TL/F/9901–26

c. Wire Spaced 1/8" from Ground Screen

FIGURE 4-14. Parallel Terminated Backplane Wire

Backplane Interconnections (Continued)

The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH-state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

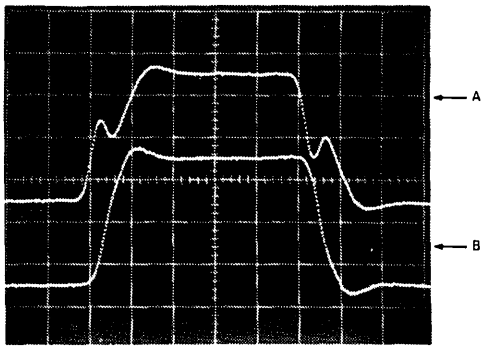
Figure 4-14c shows waveforms for a similar arrangement, but with the wire about 1/8 inch from a ground screen. The impedance of the wire is greater than 150Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200Ω constant impedance line were terminated with 150Ω.

Series source resistance can also be used with single wire interconnections to absorb reflection. *Figure 4-15a* shows a 16-inch wire with a ground screen driven through a source resistance of 100Ω. The waveforms *(Figure 4-15b)* show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from the PC board transmission line. *Figure 4-16a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan-out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 4-16b*. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 4-16c* shows the signals at the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 4-16a* is a case of mismatched transmission lines, discussed in Chapter 3.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall time (Chapter 3), further increasing the effective propagation delay.

TL/F/9901–27

a. Wire over Ground Screen

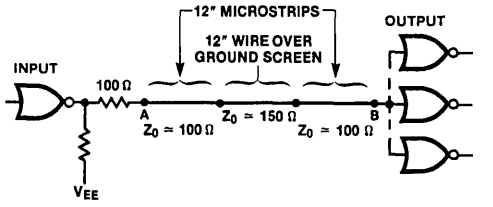


TL/F/9901–28

b. Series Terminated Waveform

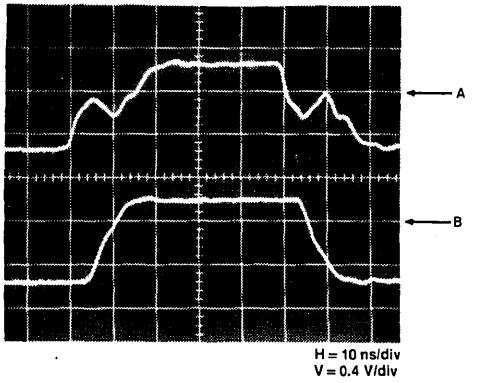
FIGURE 4-15. Series Terminated Backplane Wire

Backplane Interconnections (Continued)



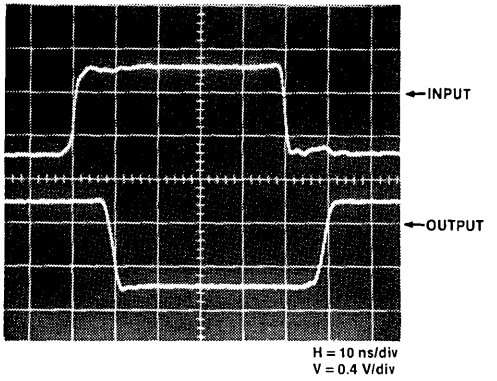
TL/F/9901–29

a. Backplane Wire Interconnecting PC Board Lines



TL/F/9901–30

b. Signals into the First Microstrip and at the Loads



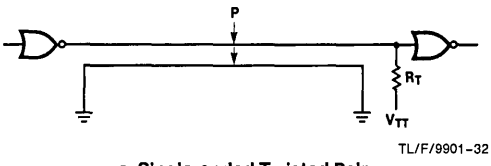
TL/F/9901–31

c. Input to Driving Gate and Output of Load Gate

FIGURE 4-16. Signal Path with Sequence of Microstrip, Wire, Microstrip

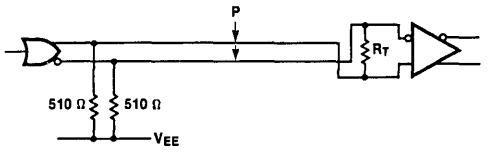
Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 4-17a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

*Teflon is a registered trademark of E.I. du Pont de Nemours Company.



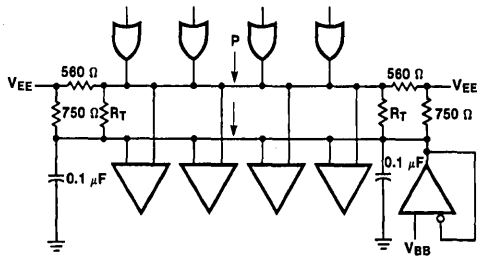
TL/F/9901–32

a. Single-ended Twisted Pair



TL/F/9901–33

b. Differential Transmission Reception



TL/F/9901–34

c. Backplane Data Bus

FIGURE 4-17. Twisted Pair Connections

Differential line driving and receiving complementary gates as the driver and an F100114 line receiver is illustrated in *Figure 4-17b*. Differential operation provides high noise immunity, since common mode input voltages between −0.55V and −3.0V are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, interconnections using shielded twisted pair are recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 4-17c*. Only one driver should be enabled at a given time; the other outputs must be in the V_{OL} state. The V_{BB} reference voltage is available on pin 22 of the flatpak and pin 19 of the dual-in-line package for the F100114.

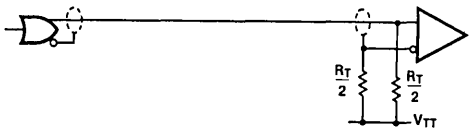
In the differential mode, a twisted pair can send high-frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise effects on time jitter.[3]

Backplane Interconnections (Continued)

Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 4-18a,* 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 4-18b, c,* the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 4-18c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.

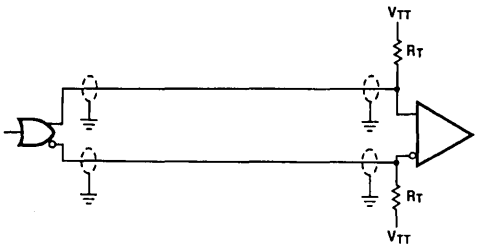
TL/F/9901–35

a. Single-Ended Coaxial Transmission



TL/F/9901–36

b. Differential Coaxial Transmission



TL/F/9901–37

c. Differential Transmission with Grounded Shields

FIGURE 4-18. Coaxial Cable Connections

References

1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," *IEEE Transaction on Electronic Computers*, Vol. EC-16 (April, 1967).
2. Harper, C. A., *Handbook of Wiring, Cabling and Interconnections for Electronics.* New York: McGraw-Hill, 1972.
3. True, K. M., "Transmission Line Interface Elements," *The TTL Applications Handbook,* Chapter 14 (August 1973), pp. 14-1–14-14.

National Semiconductor

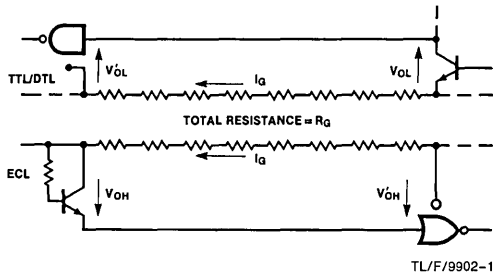
Chapter 5
Power Distribution and Thermal Considerations

Introduction

High-speed circuits generally consume more power than similar low-speed circuits. At the system level, this means that the power supply distribution system must handle the larger current flow; the larger power dissipation places a greater demand on the cooling system. The direct current (DC) voltage drop along ground busses affects noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F100K circuits, but they require consideration to obtain the performance available from the family.

Logic Circuit Ground, V_{CC}

The positive potential V_{CC} and V_{CCA} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in *Chapter 1*. This effect for TTL/DTL circuits, as well as for ECL circuits, is illustrated in *Figure 5-1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW-state noise margin of the TTL/DTL circuits and the HIGH-state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. For tabulation of ground currents in ECL, the designs must include termination currents as well as I_{EE} operating currents. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.



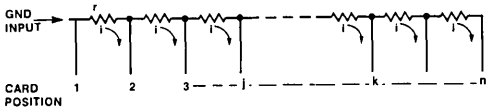
TL/F/9902-1

TTL/DTL	ECL
$V'_{OL} = V_{OL} = +I_G R_G$	$V'_{OH} = V_{OH} + I_G R_G$

$I_G R_G = (V'_{OL} - V_{OL})$ = Noise Margin Decrease = $I_G R_G = (V'_{OH} - V_{OH})$

FIGURE 5-1. Effect of Ground Resistance on Noise Margins

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 5-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.



TL/F/9902-2

r = Incremental Bus Resistance between Positions
i = Average Ground Current per Card

FIGURE 5-2. Ground Shift Along a Row of PC Cards

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current (i) per card, and an incremental bus resistance (r) between card positions, the bus voltage drops between the various positions can be determined as follows:

between positions 1 and 2: $v_{1-2} = (n-1)\,ir$

between positions 1 and 3: $v_{1-3} = (n-1)\,ir + (n-2)\,ir$

between positions 1 and 4: $v_{1-4} = (n-1)\,ir + (n-2)\,ir + (n-3)\,ir$

between 1 and n:

$$v_{1-n} = ir\{(n-1) + (n-2) + (n-3) + \ldots + [n-(n-1)]\}$$
$$= ir[1 + 2 + 3 + \ldots + (n-1)]$$
$$v_{1-n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in Equation 5-1.

$$v_{1-15} = ir \sum_{1}^{14} n = ir\,(1 + 2 + 3 + \ldots + 13 + 14) = 105\,ir \quad (5\text{-}1)$$

5

Logic Circuit Ground, V_{CC} (Continued)

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j-k} = (n - j)\,ir + [n - (j + 1)]\,ir + [n - (j + 2)]\,ir + \ldots + \{n - [j + (k\text{-}j\text{-}1)]\}\,ir$$

$$= (k - j)\,nir - ir\{j + (j + 1) + (j + 2) + \ldots + [j + (k\text{-}j\text{-}1)]\} \quad (5\text{-}2)$$

$$v_{j-k} = (k - j)\,nir - ir\sum_{j}^{k-1} n = ir\left[(k - j)\,n - \sum_{j}^{k-1} n\right]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j-k} = ir\,[(9 - 4)\,15 - (4 + 5 + 6 + 7 + 8)] \quad (5\text{-}3)$$
$$= ir\,(75 - 30) = 45\,ir$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10-15} = ir\,[(15 - 10)15 - (10 + 11 + 12 + 13 + 14)] \quad (5\text{-}4)$$
$$= ir\,(75 - 60) = 15\,ir$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross-sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential transmission and reception method i.e., twisted pair, should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

Conductor Resistances

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 5-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and, hence, areas is: as gauge numbers increase, resistance doubles with every third gauge number; e.g., the resistance per foot of #10 wire is 1 mΩ, for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships follow.

AWG B & S Gauge	Resistance mΩ Per Foot	Cross-Sectional Area Square Inches
#2	0.156	5.213×10^{-2}
#6	0.395	2.062×10^{-2}
#10	0.999	8.155×10^{-3}
#12	1.588	5.129×10^{-3}
#18	6.385	1.276×10^{-3}
#22	16.14	5.046×10^{-4}
#26	40.81	1.996×10^{-4}
#30	103.2	7.894×10^{-5}

FIGURE 5-3. Resistance and Cross-Sectional Area of Several Sizes of Annealed Copper Wire

Copper resistivity = $\rho = 1.724 \times 10^{-6}\ \Omega$cm @ 20°C

Resistance of a conductor = $\rho\frac{l}{A} = \rho\frac{l}{tw}$

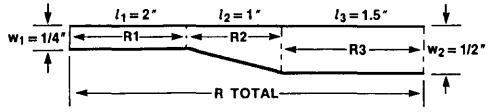
where: l = length t = thickness w = width

Sheet resistance $\rho_S = \frac{\rho}{t}\ \Omega$ per $\frac{l}{w}$

The length/width ratio (l/w) is dimensionless; therefore, the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares," then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$\rho(\Omega\text{in.}) = \rho(\Omega\text{cm}) \div 2.54 = 6.788 \times 10^{-7}\ \Omega$in.

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 5-4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.



TL/F/9902–3

FIGURE 5-4. Conductor of Uniform Thickness but Non-Uniform Cross Section

Sheet resistance = $\rho_S = \frac{\rho}{t}$

$= 5.657 \times 10^{-4}\ \Omega$ per square

The number of squares S for the rectangular sections are as follows.

$$S1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1}\ln\left(\frac{w_2}{w_1}\right) = 4 \ln 2 = 2.77 \text{ squares} \quad (5\text{-}5)$$

$$\text{Total } R = R_1 + R_2 + R_3 = \rho_s(S_1 + S_2 + S_3)$$
$$= 7.51\ \text{m}\Omega$$

Conductor Resistances (Continued)

As another example, assume that a 1 oz. trace must carry a 200 mA current six inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{I} = \frac{0.01}{0.2} = 0.05\Omega$$

$$0.05 = \rho_s \frac{l}{w} \qquad (5\text{-}6)$$

$$\frac{w}{l} = 20\,\rho_s$$

$$w = 120\,\rho_s = (120)\,5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

$\therefore$ minimum trace width, w = 68 mils

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50A current.

$$\rho_s = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square}$$

$$V = IR - (50)\,(3.364 \times 10^{-5})\,\frac{36}{1.25} \qquad (5\text{-}7)$$

$$= 0.0484 = 48.4 \text{ mV}$$

Sheet resistances for various copper thicknesses are listed in *Figure 5-5*. Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 5-6* and resistance per foot as a function of width is shown in *Figure 5-7*.

Weight or Thickness	Sheet Resistance Ω per Square	Thickness	Sheet Resistance Ω per Square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

FIGURE 5-5. Sheet Resistance for Various Thicknesses of Copper

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	Weight, %	in.
0.0007	0.0178	½	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 −0.0002
0.0028	0.0715	2	+10	+0.0007 −0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

FIGURE 5-6. Thickness and Tolerances for Copper Cladding

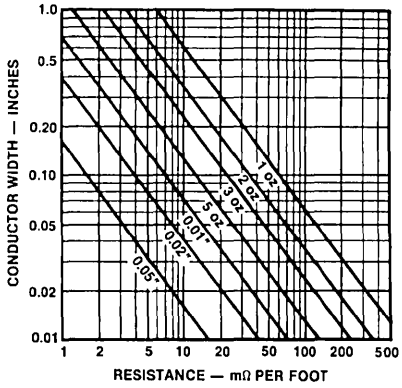


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FIGURE 5-7. Conductor Resistance vs Thickness and Width

Temperature Coefficient

The resistances in *Figures 5-3, 5-5,* and *5-7*, as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature (T) can be determined as follows.

$$R_T = R_{20°C}\,[1 + 0.004\,(T + 20°C)]$$

At 55°C: (5-8)

$$R = R_{20°C}\,[1 + 0.004\,(55°C - 20°C)] = 1.14\,R_{20°C}$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 5-8* illustrates the ohmic heating effect of various current densities.[1]

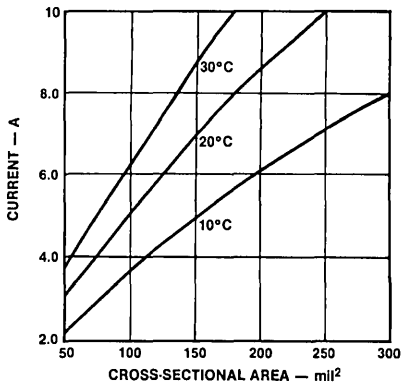

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FIGURE 5-8. Temperature Rise with Current Density in PC Board Traces

Distribution Impedance

Power busses should have low AC impedance, as well as low DC resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 5-9*. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377\,d}{\sqrt{\epsilon}\,h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar®* or Teflon®* dielectric ($\epsilon = 2.3$) two mils thick, impedance of the flat conductor pair is only 0.5Ω. Power line impedance can be reduced by periodically connecting RF-type capacitors across the line.

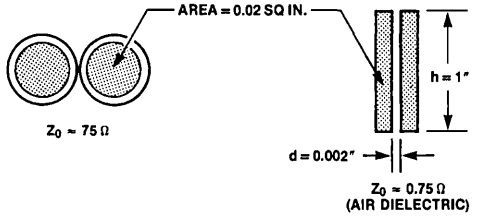

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FIGURE 5-9. Effect of Geometry on Power Bus Impedance

*Mylar and Teflon are registered trademarks of E.I. du Pont de Nemours Company.

Ground on PC Cards

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low-impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CCA} pins of the IC packages, through the output transistors, then into the loads and the stray capacitances. These stray capacitances exist from an output to V_{EE}, output to ground, and to other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every one to two IC packages. Additional capacitors may be needed for multiple output devices. These capacitors should be ceramic, monolithic or other RF types in the 0.01 μF to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, in a 50Ω terminator I_{OL} is 5.9 mA, I_{OH} is 20.9 mA. Then signal change will cause about 15 mA current change and, as this current change propagates along the signal trace, a current of −15 mA advances along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. The 15 mA current change can be reduced by terminating the complementary output of the signal. Then a signal change will direct the current from true output to the complement output reducing the Δ currents in the ground plane. When it is necessary to interrupt the ground plane, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

Not enough emphasis can be placed on the requirement for a good ground. All input signals are referenced to internal V_{BB} and the V_{BB} is referenced to V_{CC} (ground). Any variation from one side of the board to the other affects the noise margins. To help eliminate some of the variations a separate V_{CCA} is provided on F100K ECL circuits to power the output drivers and leave the V_{CC} going to internal circuitry unaffected.

Backplane Construction

In order to take complete advantage of the speeds inherent in F100K ECL it is desirable to construct the backplane as a multilayer printed circuit board. Generally, two internal layers are devoted to ground and V_{EE} and the signals occupy the outside layers. Where power densities are very high, it may be necessary to supplement the power layers with external busses (see Backplane Interconnections, *Chapter 4*).

If it is necessary to use wires to augment the interconnection provided by the traces, less critical signals should use the wires. The wires will exhibit an impedance which can be calculated with the wire-over-ground formula

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \text{Log}_{10} \frac{4h}{d} \qquad (5\text{-}9)$$

where d is diameter, h is distance to ground, and ϵ is dielectric constant.

Bear in mind that if the ground plane is buried inside the board, then both h and ϵ are made up of multiple components.

Termination Supply, V_{TT}

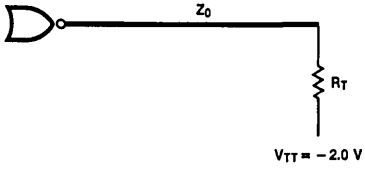
A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A−2V V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. *Figure 5-10* shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to −2V. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cy-

Termination Supply, V_{TT} (Continued)

cle values are useful in determining the current drain on the −2V supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

DC regulation of the −2V supply is not critical; a variation of ±5% causes a change in output levels of ±12 mV for 50Ω terminations or ±7 mV for 100Ω terminations.

The high frequency characteristics of the V_{TT} distribution are extremely important. Ideally, a solid voltage plane should be devoted to V_{TT}. If this is not feasible, the V_{TT} distribution should form a grid using orthogonal traces. In any case, decoupling capacitors to ground should be used to reduce the high frequency impedance.



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R_T Ω	I_{avg} mA	$P_{D\,(avg)}$ mW	
		IC Output	Resistor
50	14	14	13
62	11	12	11
75	9.3	9.5	9.1
90	8.1	8.2	7.9
100	7.3	7.3	7.1
150	5.0	4.9	5.0

FIGURE 5-10. Average Current and Power Dissipation for Parallel Termination to −2V

If the terminators used are in Single In-line Packages (SIP) or Dual-In-line Packages (DIP) as opposed to discrete resistors, particular attention must be given to decoupling in order to maintain a solid V_{TT} voltage inside the package. This is necessary to avoid crosstalk due to mutual inductance to V_{TT}. SIPs have been developed which have multiple V_{TT} connections and on-board decoupling capacitors.

V_{EE} Supply

The value of V_{EE} is not critical for F100K since all circuits in the family operate over the range of −4.2V to −5.7V. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should used 1 μF to 10 μF decoupling capacitors near the points where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than −4.5V, the current drain varies as shown in *Figure 5-11* and *5-12* for SSI and MSI elements respectively. These graphs are made from data from the F100101 and F100179.

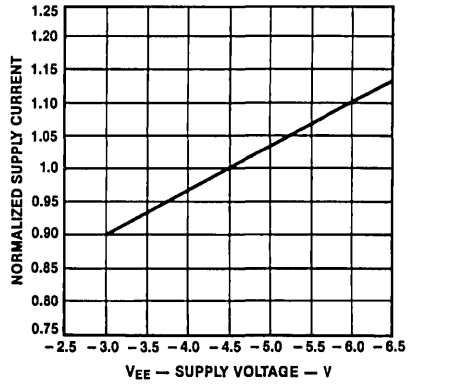

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FIGURE 5-11. Supply Current vs Supply Voltage for F100101

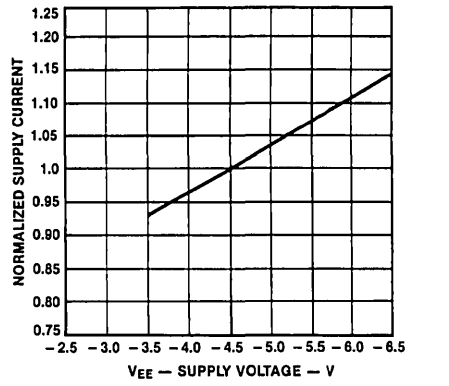

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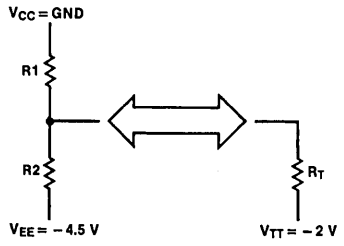
FIGURE 5-12. Supply Current vs Supply Voltage for F100179

Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull-down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in *Figure 5-13* for several representative values of equivalent resistance. The average values apply for 50% duty cycle. Peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in *Figure 5-10*. Average dissipation and I_{EE} current for several values of pull-down resistance to V_{EE} are listed in *Figure 5-14*. The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from Equation 4-12. Peak current values are approximately 12% greater than average values.

Figures 5-10, 13 and *14* show that the Thevenin equivalent parallel termination method leads to ten times as much dissipation in the resistors as in the single resistor returned to −2V. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to −2V.

V_{EE} Supply (Continued)



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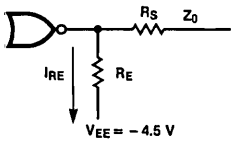
R_T Ω	$R_{1\Omega}$ = 1.80 R_T	$R_{2\Omega}$ = 2.25 R_T	I_{EE} (avg) mA	P_D (avg) mW Resistors
50	90	113	28.2	109
62	112	140	22.7	87.9
75	135	169	18.8	72.7
82	148	185	17.2	66.5
90	162	203	15.7	60.5
100	180	225	14.1	54.5
120	216	270	11.7	45.4
150	270	338	9.4	36.3

FIGURE 5-13. Series Divider for Thevenin Equivalent Terminations



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Z_0 Ω	R_E Ω	I_{EE} (avg) mA	P_D (avg) mW	
			IC Output	R_E
50	269	9.8	12.9	25.8
62	331	7.9	10.4	20.6
75	399	6.5	8.6	16.8
90	477	5.4	7.1	13.9
100	530	4.9	6.5	12.7
120	634	4.1	5.4	10.6
150	791	3.2	4.2	8.1

FIGURE 5-14. Average Current and Power Dissipation Using Pull-Down Resistor to V_{EE}

Thermal Considerations

System cooling requirements for ECL circuits are based on three considerations: (1) the need to minimize temperature gradients between circuits communicating in the single-ended mode, (2) the need to control the temperature environment of each circuit to assure that the parameters stay within guaranteed limits, and (3) the need to insure that the maximum rated junction temperature is not exceeded.

Temperature gradients are of no practical concern with F100K circuits since they are temperature compensated; their output voltage levels and input thresholds change very little with temperature, as discussed in *Chapter 1*. With uncompensated ECL circuits, output voltage levels and input thresholds vary with temperature. This causes a loss of noise margin when driving and receiving circuits are operating at different temperatures. Loss of HIGH-state noise margin occurs when the receiving circuit is at the higher temperature, amounting to approximately 1 mV/°C of temperature gradient. When the driving circuit is at the higher temperature, the LOW-state margin decreases by approximately 0.5 mV/°C of gradient. The system designer must consider noise margin loss, due to temperature gradients.

Each DC parameter limit on the F100K data sheets applies over the entire 0°C to +85°C case temperature. For uncompensated ECL circuits, parameter limits have different values for different ambient temperatures. Further, ambient temperature specifications are based on a minimum air flow rate of 400 linear feet per minute. Thermal equilibrium must be established for incoming test results of uncompensated ECL circuits to be valid. The time required to attain equilibrium can vary considerably, depending on the internal dissipation of the particular IC type and details of the thermal arrangement. Normally, an adequate waiting time is three to five minutes after power is applied.

The maximum rated junction temperature of F100K circuits is +150°C. An individual IC junction temperature can be determined by multiplying power dissipation by the junction-to-air thermal resistance θ_{JA} and adding the result to the ambient air temperature. The power dissipation is V_{EE} times I_{EE}, from the data sheet, plus the dissipation in the output transistors from *Figure 5-10* or *5-14*. Thermal resistance is shown in *Figure 5-15* as a function of cooling air flow rate. This figure applies when the IC is mounted on a board with the air flowing in a plane parallel to the board and perpendicular to the long axis of the IC package. When air temperature, flow rate and package power dissipation are known, junction temperature is determined as follows.

$$T_J = T_A + P_D\theta_{JA} \qquad (5\text{-}10)$$

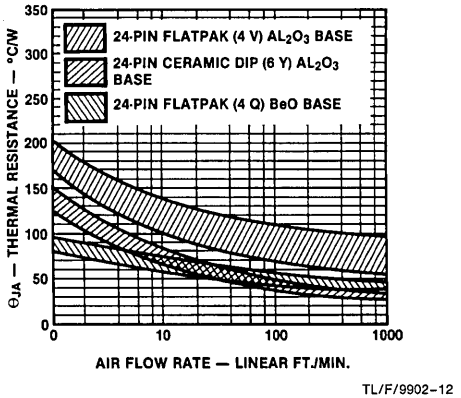

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FIGURE 5-15. Junction-to-Air Thermal Resistance vs Air Flow Rate

Thermal Considerations (Continued)

Conversely, when the maximum rate junction temperature (+150°C), the package power dissipation, and the air temperature are known, the minimum flow rate can be determined by first determining the maximum thermal resistance.

$$\text{Maximum } \theta_{JA} = \frac{(150° - T_A)}{P_D} \quad (5\text{-}11)$$

For this value of θ_{JA} the minimum flow rate is determined from *Figure 5-15.*

When the system designer plans to depend on natural convection for cooling, it is recommended that thermal tests be conducted to determine actual conditions. The effectiveness of natural convection for cooling varies greatly. For instance, on a densely packed logic board in a horizontal attitude in still air, the effective ambient temperature for an IC varies with its position. An IC in the middle of the board is subjected to air that is partially heated by surrounding ICs. Additionally, the temperature of the board rises due to heat flow through the component leads. These effects can cause a much higher junction temperature than might be expected.

Reference

1. Harper, C.A., Editor, *Handbook of Wiring, Cabling and Interconnecting for Electronics*, McGraw-Hill, 1972.

National Semiconductor

Chapter 6
Testing Techniques

Introduction

The purpose of this chapter is to assist personnel involved with incoming inspection and qualification testing, by discussing the various methods and techniques used in testing ECL devices.

Testing includes verifying functionality, checking DC parametric limits and measuring AC performance. These tasks are particularly difficult for ECL devices in light of the broad range of products: RAMs, PROMs, gate arrays, and logic circuits. Correlation between supplier and user is extremely important. Recognizing the differences between high-volume instantaneous testing, as performed by the supplier, and the user's concern for long term performance in a given operating environment, National guarantees the data sheet limits as specified, although testing may be performed by alternate methods.

Tester Selection

Although many makes and types of automatic test systems are available and in use today, not all are capable of testing ECL RAMs, PROMs, logic and gate arrays.

Logic and gate array testers require DC Accuracy, subnanosecond AC test capability, and the ability to change software for each device. Software capability and the number of test pins available are major considerations in choosing a gate array tester. Functional, DC and threshold tests are successfully performed on automatic test equipment, but subnanosecond propagation delays are difficult to measure accurately.

The use of dedicated testers to perform high-volume memory testing is very common. Testers containing hardware addressing capability are usually the most efficient. Although basic DC testing is similar for any device type, RAM and PROM functional testing usually require special addressing capabilities to test for pattern sensitivity. The pattern generators and output comparators must have minimum skew to obtain maximum tester accuracy. Functional and AC tests are performed simultaneously; then, DC and threshold tests are performed.

The following considerations must be taken into account when selecting a tester.

Noise

Since the voltage swing on ECL input and output levels is only about 800 mV, it is very important that the power supplies and voltage drivers be extremely clean and free of spikes, hum, or any other type of noise.

DC Resolution

The threshold measurements ($V_{IH\ (Min)}$, $V_{IL\ (Max)}$) require that input voltage be extremely accurate and repeatable, i.e., if the $V_{IL\ (Max)}$ is specified as -1.475V, a voltage source of -1.475 ± 5 mV is not adequate to accurately test the part. Ideally, the driver and the output comparators should have an accuracy of ± 1 mV.

Current Capability

Since ECL is noted for high current requirements, power supplies for V_{EE} should be capable of supplying current with a 25% reserve over the highest powered parts. This reserve should be included because power supplies tend to get noisy when approaching the current clamp. Some ECL LSI parts dissipate over 4.5W; therefore, with a V_{EE} of -4.5V, the power supply must provide well over 1A.

Edge Rates

When testing edge-triggered sequential logic parts such as flip-flops and shift registers, it is important that the rise and fall times of the clock pulses be fast, clean and free from overshoot. If the clock edges are not adequate, the deficiency can be overcome using a Schmitt trigger as shown in *Figure 6-1*.

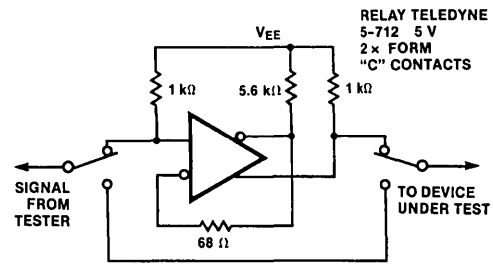

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FIGURE 6-1. Typical Schmitt Trigger Circuit

The 68Ω resistor provides hysteresis by positive feedback, thus improving the edge rates. When energized, the relay provides a path to bypass the Schmitt trigger, so the input currents of the device under test can be measured.

Functional Testing

The functional operation and truth table for all device types are checked using automatic test equipment. For memory devices, pattern sensitivity and AC characteristics are also tested automatically. Functional testing is usually performed before DC testing. Logic parts are functionally tested in all modes of operation. The inputs are driven using typical V_{IH} and V_{IL} values. The outputs are compared against relaxed V_{OH} and V_{OL} limits. The V_{IH}, V_{IL}, V_{OH} and V_{OL} limits are tested during DC testing.

DC Testing

An automatic tester is used to test all DC parameters listed on the individual data sheet for each input and output. The device may have to be preconditioned to obtain the correct output logic state. The cable length should be kept to a minimum to insure signal integrity.

Threshold Measurements

Threshold measurement on an automatic tester is probably the most difficult DC test and the test most prone to oscillation. When testing, take one input at a time to threshold; all other inputs remain at full V_{IH} or V_{IL} levels. For example, to test a flip-flop, make sure the output is LOW before test, take the data pin to HIGH threshold, and apply the clock pulse. Verify that the HIGH has been transferred to the output. Next, apply LOW threshold to the data input and clock it through; use hard levels on the clock (full V_{IH} and V_{IL}). Check that the output pin goes LOW.

Bench Testing

Occasionally, it is necessary to obtain data not easily available from an automatic tester. This is accomplished by testing devices in a universal test board. The typical test circuit board is double-clad copper. All input/output pins go to single-pole, triple-throw switches so that V_{IH}, V_{IL} or a 50Ω terminating resistor can be connected. Leadless 0.05 μF capacitors decouple all pins to V_{CC} (+2V) at the socket pins. Access to the device under test is made via banana sockets to the X-Y plotter.

V_{IH}/V_{OUT} Plot—The input ramp supply is 0V to −2V varied by a multi-turn potentiometer. The input voltage (V_{IN}) versus output voltage (V_{OUT}) is plotted on an X-Y recorder using the test setup shown in *Figure 6-2*.

V_{OUT}/I_{OUT} Plot—The output voltage (V_{OUT}) versus output current (I_{OUT}) can be plotted using the test setup shown in *Figure 6-3*.

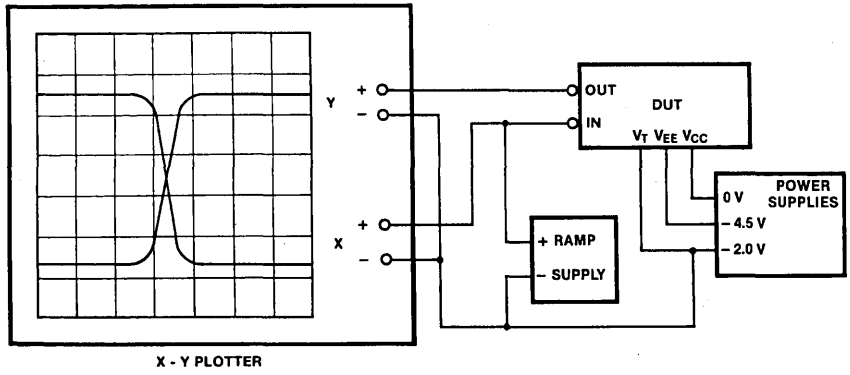

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FIGURE 6-2. V_{IN}/V_{OUT} Transfer Characteristics

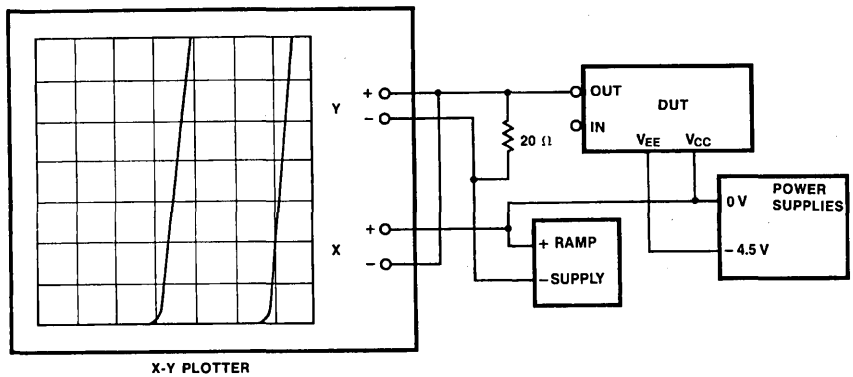

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FIGURE 6-3. V_{OUT}/I_{OUT} Characteristics

AC Testing

Because few automatic measurements systems have sufficient accuracy to perform subnanosecond testing, AC testing of ECL is one of the most difficult tests to accomplish. To obtain subnanosecond accuracy usually requires special test fixtures and equipment. The physical location of the test fixture, the input driver and the output comparator is very important.

Depending upon the accuracy and repeatability of the automatic tester, a bench setup may be required for correlation. Comparing an air line with known propagation delay to the test setup is recommended.

AC Test Fixtures

Test fixture design plays a pivotal role in insuring that undistorted waveforms are applied to the Device Under Test (D.U.T.) and that the device output can be monitored correctly.

Board Construction and Layout

ECL AC bench test fixtures are built on a double-clad printed circuit board or on a multilayer printed circuit board with semi-rigid coax, *Figures 6-4* and *6-5*. The power planes are shorted at the device and brought out to banana sockets with the decoupling capacitors at the device. Transmission lines of 50Ω are maintained from soldered-on BNC or SMA connectors to the D.U.T. Sense lines from the D.U.T. output and input pins to the connectors must be of electrically equal length. For input pins, care must be taken to insure that the force and sense lines are brought directly to the point that makes contact with the D.U.T. For output pins, only the output sense lines are used to monitor the signals. The force lines are disconnected at the device to minimize signal distortion. Special care must be taken to minimize crosstalk and stray capacitance in the area of the D.U.T. For correlation, flatpaks are not tested in sockets but are clamped to the traces of a multilayer PC board. Dual in-line devices are plugged into individual pin sockets instead of normal test sockets. Due to equipment limitations and for correlation, the amplitude, offset, rise and fall time are set up with no device in the test socket.

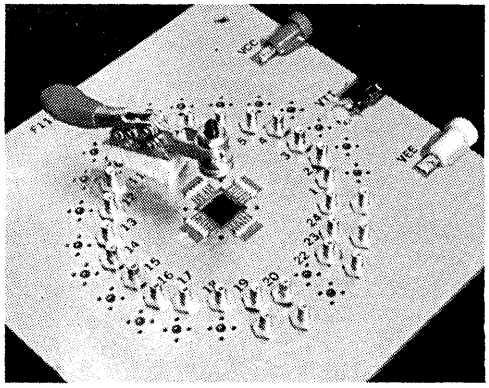

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FIGURE 6-4. Multilayer Test Fixture (Top View)

The bench test fixture to measure toggle frequency utilizes the principles described in the preceding paragraph except that the feedback path between the output and data input is as short as possible.

Output Termination

All outputs should be terminated with 50Ω ±1% resistors. This is especially important for complementary outputs.

When bench testing, the device is offset by +2V; V_{EE} is −2.5V; V_{CC}, V_{CCA} is +2V. Then the 50Ω input impedance of the sampling oscilloscope acts as the termination resistor to 0V. The input and output coaxial cable to the oscilloscope should be cut to exactly the same electrical length.

Decoupling

Not enough emphasis can be put on the importance of good decoupling on the D.U.T. because oscillations can give erroneous test results. A sampling scope should be used to make sure that oscillation is not occurring.

The value of capacitors used depends on the type of tester used and the frequency of test. Some testers use pulse test; in other words, for each individual test in a program, V_{EE} is powered up and down. On this type of tester, electrolytic-type (i.e., large value) capacitors cannot be used because of the time constant needed to charge the capacitor.

Always start with the minimum decoupling needed to achieve good results, perhaps merely a capacitor between V_{CC} and V_{EE}. Capacitors should be placed as close as possible to the D.U.T. to eliminate as much inductance as possible. Only low-inductance capacitors should be used; leadless monolithic ceramic capacitors are very effective.

There are no rigid decoupling rules, and each device type may have its own decoupling requirements. A typical decoupling technique that works well on most F100K devices is to place 0.01 μF to 0.1 μF monolithic ceramic capacitors in the following locations.

- If no offset is used:
  between V_{EE} (−4.5V) and V_{CC}, V_{CCA} (0V)
  between V_{TT} (−2V) and ground (0V)
- If +2V offset is used:
  between V_{CC}, V_{CCA} (+2V) and ground (0V)
  between V_{EE} (−2.5V) and ground (0V)
- In most cases, V_{CCA} and V_{CC} should be shorted as close to the D.U.T. as possible. However, if the V_{CCA} and V_{CC} pins are physically separated, individual decoupling capacitors may be necessary.
- For DC test only place a 0.001 μF capacitor:
  between an input pin and V_{EE}
  between an output pin and V_{CCA}

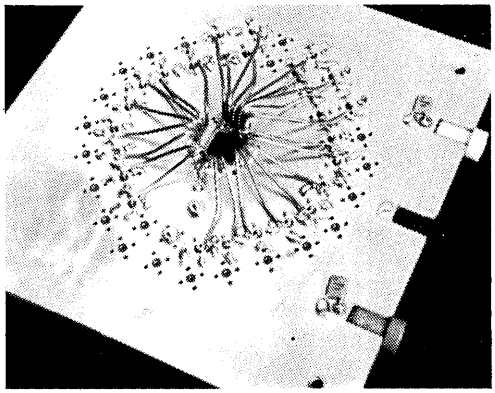

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FIGURE 6-5. Multilayer Test Fixture (Bottom View)

AC Test Fixtures (Continued)

Decoupling problems will appear mainly at threshold test. If certain outputs fail, try the decoupling technique, described in the preceding paragraph, on those outputs and the associated inputs. With testers that use the power-hold method, such as the Sentry®, large electrolytics can be used in parallel with smaller (0.01 μF) disk capacitors for the high-frequency bypass.

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Chapter 7
Quality Assurance and Reliability

Introduction

F100K ECL is manufactured to strict quality and reliability standards. Product conformance to these standards is insured by careful monitoring of the following functions: (1) incoming quality inspection, (2) process quality control, (3) quality assurance, and (4) reliability.

Incoming Quality Inspection

Purchased piece parts and raw materials must conform to purchase specifications. Major monitoring programs are the inspection of package piece parts, inspection of raw silicon wafers, and inspection of bulk chemicals and materials. Two other important functions of incoming quality inspection are to provide real-time feedback to vendors and in-house engineering, and to define and initiate quality improvement programs.

Package Piece Parts Inspection

Each shipment of package piece parts is inspected and accepted or rejected based on AQL sampling plans. Inspection tests include both inherent characteristics and functional use tests. Inherent characteristics include physical dimensions, color, plating quality, material purity, and material density. Functional use tests for various package piece parts include die attach, bond pull, seal, lid torque, salt atmosphere, lead fatigue, solderability, and mechanical strength. In these tests, the piece parts are sent through process steps that simulate package assembly. The units are then destructively tested to determine whether or not they meet the required quality and reliability levels.

Silicon Wafer Inspection

Each shipment of raw silicon wafers is accepted or rejected based on AQL sampling plans. Raw silicon wafers are subjected to non-destructive and destructive tests. Included in the testing are flatness, physical dimensions, resistivity, oxygen and carbon content, and defect densities. The test results are used to accept or reject the lot.

Bulk Chemical and Material Inspection

Bulk chemicals and materials play an important role in any semiconductor process. To insure that the bulk chemicals and materials used in processing F100K wafers are the highest quality, they are stringently tested for trace impurities and particulate or organic contamination. Mixtures are also analyzed to verify their chemical make-up.

Incoming inspection is only the first step in determining the acceptability of bulk chemicals and materials. After acceptance, detailed documentation is maintained to correlate process results to various vendors and to any variations found in mixture consistency.

Process Quality Control

Process quality is maintained by establishing and maintaining effective controls for monitoring the wafer fabrication process, reporting the results of the monitors, and initiating valid measurement techniques for improving quality and reliability levels.

Methods of Control

The process quality control program utilizes the following methods of control: (1) process audits, (2) environmental monitors, (3) process monitors, (4) lot acceptance inspections, (5) process qualifications, and (6) process integrity audits. These methods of control, defined below, characterize visually and electrically the wafer fabrication operation.

Process Audit—Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.

Environmental Monitor—Monitors concerning the process environment, i.e., water purity, air temperature/humidity, and particulate count.

Process Monitor—Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variables data.

Lot Acceptance—Lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, requiring special attention.

Process Qualification—Complete distributional analysis is run to specified tolerance averages and standard deviations. These qualifications are typically conducted on deposition and evaporation processes, i.e., epi, aluminum, vapox, and backside gold.

Process Integrity Audit—Special audits conducted on oxidation and metal evaporation processes (CV drift—oxidation; SEM evaluation—metal evaporation).

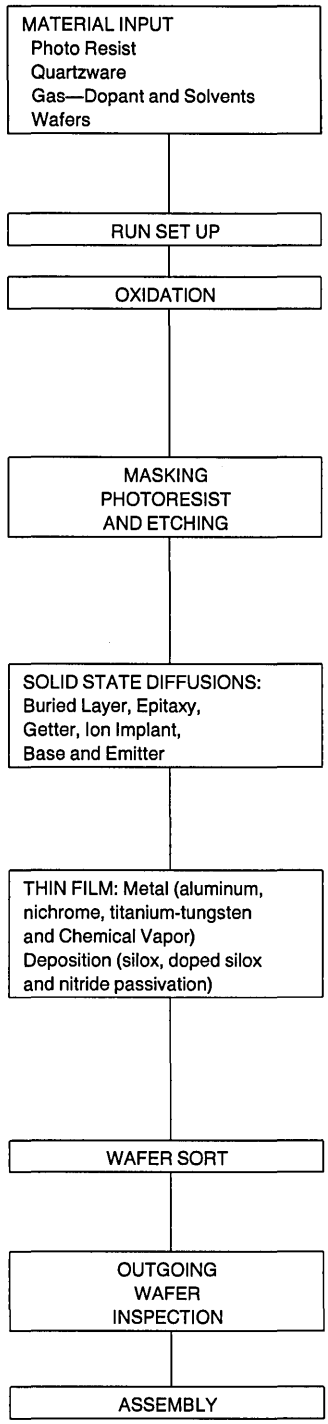
Data Reporting

Process quality control data is recorded on an attribute or variable basis as required; control charts are maintained on a regular basis. This data is reviewed at periodic intervals and serves as the basis for judging the acceptability of specific processes. Summary data from the various process quality control operations are relayed to cognizant line, engineering and management personnel in real time so that, if appropriate, the necessary corrective actions can be immediately taken.

Process Flow

Figure 7-1 shows the integration of the various methods of control into the wafer fabrication process flow. The process flow chart contains examples of the process quality controls and inspections utilized in the manufacturing operation.

Process Quality Control (Continued)



Process Controls (Examples)

- A. Environmental
- B. Chemical supplies
- C. Substrate examination (resistivity, flatness, thickness, crystal perfection, etc.)
- D. Photoresist evaluation
- E. Mask inspections

- A. Process audit

- A. Process audit/qualification
- B. Environmental
- C. Process monitors (thickness, pinhole and crack measurements)
- D. C V Plotting
- E. Calibration

- A. Process audits
- B. Environmental
- C. Visual examinations
- D. Photoresist evaluation (preparation, storage, application, baking, development and removal)
- E. Etchant controls
- F. Exposure controls (intensity, uniformity)

- A. Process audits/qualification
- B. Environmental
- C. Temperature profiling
- D. Quartz cleaning
- E. Calibration
- F. Electrical tests (resistivity, breakdown voltages, etc.)

- A. Process audits/qualification
- B. Environmental
- C. Visual examinations
- D. Epitaxy controls (thickness, resistivity cleaning, visual examination)
- E. Metallization controls (thickness, temperature cleaning, SEM, C V plotting)
- F. Glassivation controls (thickness, dopant concentration, pinhole and crack measurements)

- A. Process audit
- B. Environmental
- C. Visual examinations

- A. Process audit
- B. Inspection

FIGURE 7-1. Process Flow Chart

Quality Assurance

To assure that all product shipped meets both internal National specifications for standard product and customer specifications in the case of negotiated specs, a number of QA inspections throughout the assembly process flow *(Figure 7-2)* are required. A flow, much more detailed than the one presented in *Figure 7-2*, governs the assembly of the devices and the performance of the environmental, mechanical and electrical tests.

Reliability

A number of programs, among them qualification testing, reliability monitoring, failure analysis, and reliability data collection and presentation, are maintained.

Qualification Programs

All products receive reliability qualification prior to the product being released for shipment. Qualification is required for (1) new product designs, (2) new fabrication processes or (3) new packages or assembly processes. Stress tests are run and the results are evaluated against existing reliability levels. These results must be better than or equal to current product for the new product to receive qualification.

New Product Designs—Receive, as a minimum, +125°C operating life tests. Readouts are normally scheduled at 168 hours, 1168 hours and 2168 hours. The samples stressed are electrically good units from initial wafer runs. Additional life testing, consisting of high-temperature operating life test, 85/85 humidity bias tests and bias pressure pot (BPTH) tests, may be run as deemed necessary. Redesigns of existing device layouts are considered to be new product designs, and full qualification is necessary.

New Fabrication Processes—Qualifications are designed to evaluate the new process against the current process. Stress tests consist of operating life test, high-temperature operating life test, 85/85 humidity bias test and/or biased

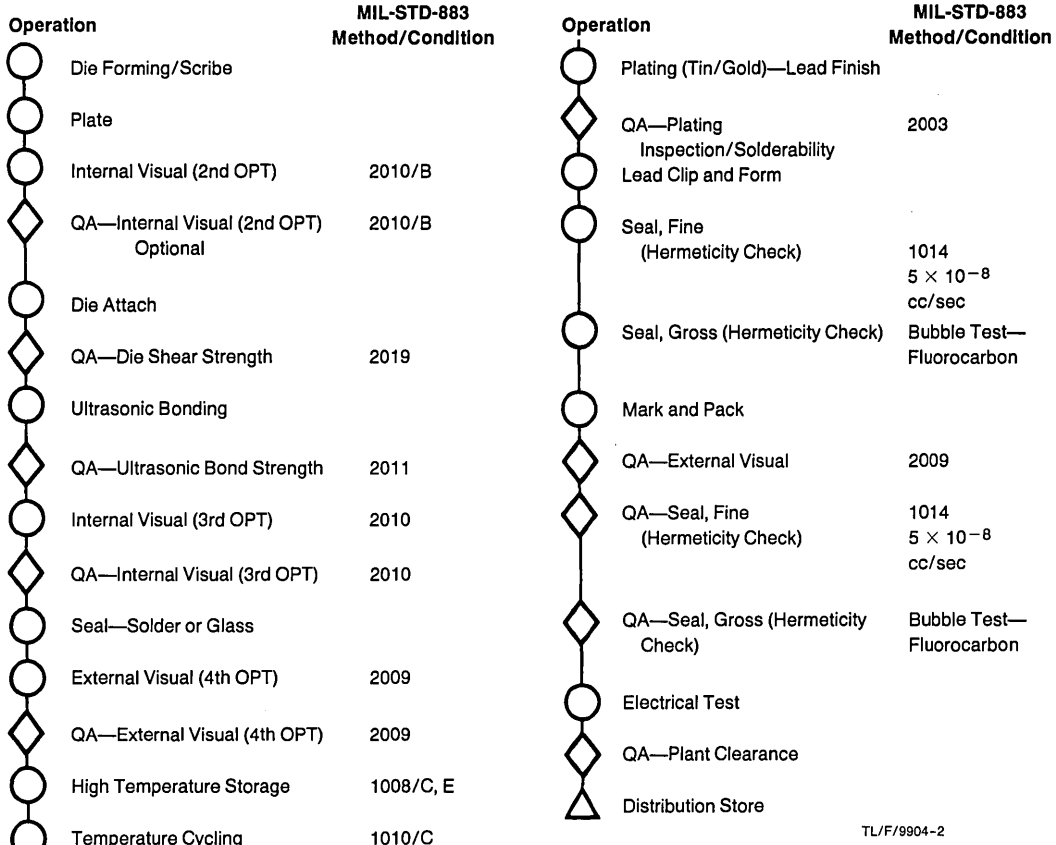


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FIGURE 7-2. Generalized Process Flow

Reliability (Continued)

pressure pot (BPTH) test. In addition, package environment tests may be performed. Evaluations are performed on various products throughout the development stages of the new process. Units stressed are generally from split wafer runs. All processing is performed as a single wafer lot up to the new process steps, where the lot is split for the new and the current process steps. Then the wafers are recombined, and again processed as a single wafer lot. This allows for controlled evaluation of the new process against the standard process. Both significant modifications to existing process and transferring existing products to new fabrication plants are treated as a new process.

New Packages or Assembly Processes—Qualifications are performed for new package designs, changes to existing piece parts, changes in piece part vendors, and significant modification to assembly process methods. In general, samples from three assembly runs are stressed to a matrix shown in Table 7-1. In addition, +100°C operating life tests, 85/85 humidity bias tests, biased pressure pot (BPTH) tests and unbiased pressure pot tests are performed.

Reliability Monitors

Reliability testing of mature products is performed to establish device failure rates, and to identify problems occurring in production. Samples are obtained on a regular basis from production. These units are stressed with operating life tests or package environmental tests. The results of these tests are summarized and reported on a monthly basis. When a problem is identified, the respective engineering group is notified, and production is stopped until corrective action is taken.

Current testing levels are in excess of 14,000 units per year stressed with operating life tests, and 23,000 units per year stressed with package environmental tests.

Failure Analysis

Failure analysis is performed on all units failing reliability stress tests. Failure analysis is offered as a service to support manufacturing and engineering, and to support customer returns and customer requested failure studies. The failure analysis procedure used has been established to provide a technique of sequential analysis. This technique is based on the premise that each step of analysis will provide information of the failure without destroying information to be obtained from subsequent steps. The ultimate purpose is to uncover all underlying failure mechanisms through complete, in-depth, defect analysis. The procedure places great emphasis on electrical analysis, both external before decapsulation, and internal micro-probing. Visual examinations with high magnification microscopes or SEM analysis are used to confirm failure mechanisms. Results of the failure analysis are recorded and, if abnormalities are found, reported to engineering and/or manufacturing.

Data Collection and Presentation

Product reliability is controlled by first stressing the product, and then feeding back results to manufacturing and engineering. This feedback takes two forms. There is a formal monthly Reliability Summary distributed to all groups. The summary shows current product failure rates, highlights problem areas, and shows the status of qualification and corrective action programs. Less formal feedback is obtained by including reliability personnel at all product meetings, which gives high visibility to the reliability aspects of various products. As a customer service, product reliability data is compiled and made available upon request.

TABLE 7-1. Package Environmental Stress Matrix

Test	MIL-STD-883	
	Method	Condition
GROUP B		
Subgroup 1 Physical Dimensions	2016	
Subgroup 2 Resistance to Solvents	2015	
Subgroup 3 Solderability	2003	Soldering Temperature of 260 ±10°C
Subgroup 5 Bond Strength (1) Thermocompression (2) Ultrasonic or Wedge	2011	 (1) Test Condition C or D (2) Test Condition C or D
GROUP C		
Subgroup 2 Temperature Cycling Constant Acceleration Seal (a) Fine (b) Gross Visual Examination End-Point Electrical Parameters	 1010 2001 1014	 Test Condition C (−65°C to +150°C) Test Condition E (30 kg), Y_1 Orientation and X_1 Orientation Test Condition D (20 kg) for Packages over 5 gram weight or with Seal Ring Greater than 2 inches

Reliability (Continued)

TABLE 7-1. Package Environmental Stress Matrix (Continued)

Test	MIL-STD-883	
	Method	Condition
GROUP D		
Subgroup 1		
Physical Dimensions	2016	
Subgroup 2		
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)
Seal	1014	As Applicable
(a) Fine		
(b) Gross		
Lid Torque	2024	As Applicable
Subgroup 3		
Thermal Shock	1011	Test Condition B (−55°C to +125°C) 15 Cycles Minimum
Temperature Cycling	1010	Test Condition C (−65°C to +150°C) 100 Cycles Minimum
Moisture Resistance	1004	
Seal	1014	
(a) Fine		
(b) Gross		
Visual Examination		
End-Point Electrical Parameters		
Subgroup 4		
Mechanical Shock	2002	Test Condition B (1500g, 0.5 ms)
Vibration, Variable Frequency	2007	Test Condition A (20g)
Constant Acceleration	2001	Same as Group C, Subgroup 2
Seal		
(a) Fine		
(b) Gross		
Visual Examination		
End-Point Electrical Parameters		
Subgroup 5		
Salt Atmosphere	1009	Test Condition A Minimum (24 Hours)
Seal	1014	As Applicable
(a) Fine		
(b) Gross		
Visual Examination		
Subgroup 6		
Internal Water-Vapor Content	1018	
Subgroup 7		
Adhesion of Lead Finish	2025	

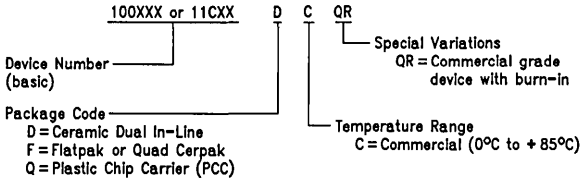
Section 6

Ordering Information and Physical Dimensions

Section 6 Contents

ORDER INFORMATION

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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For most current packaging information, contact product marketing.

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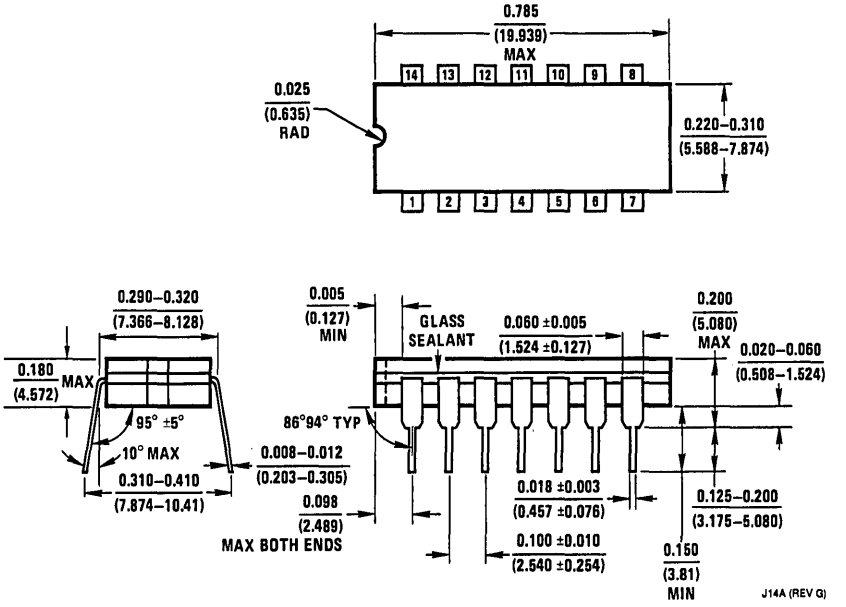
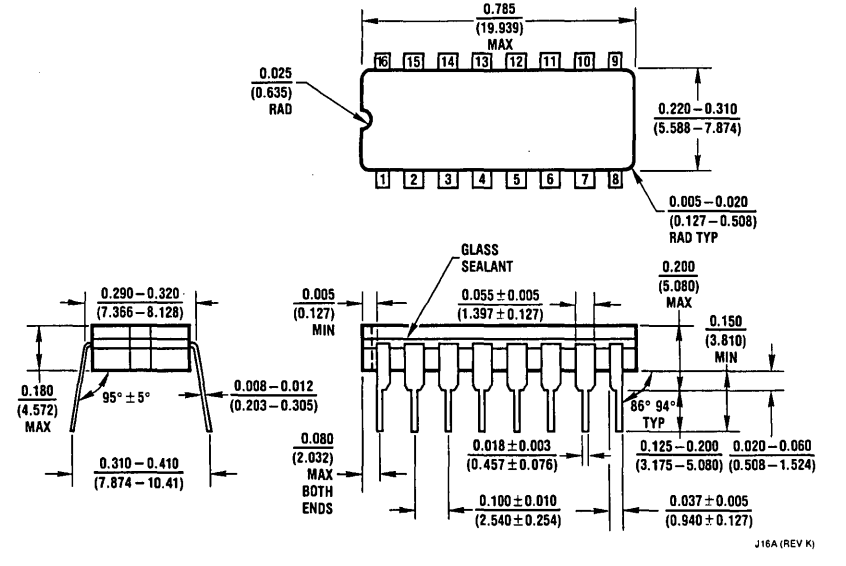
All dimensions are in inches (millimeters)

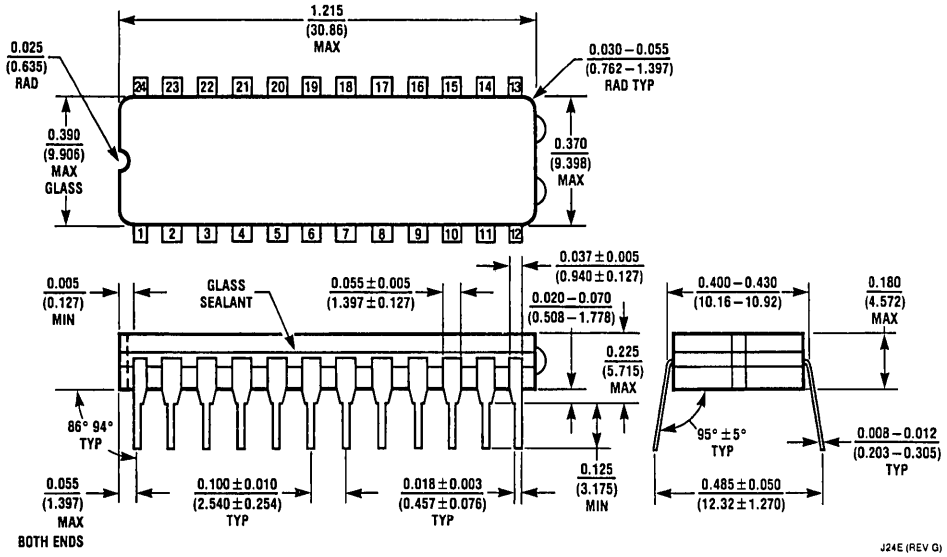
14 Lead Ceramic Dual In-Line Package (D)
NS Package Number J14A



16 Lead Ceramic Dual In-Line Package (D)
NS Package Number J16A

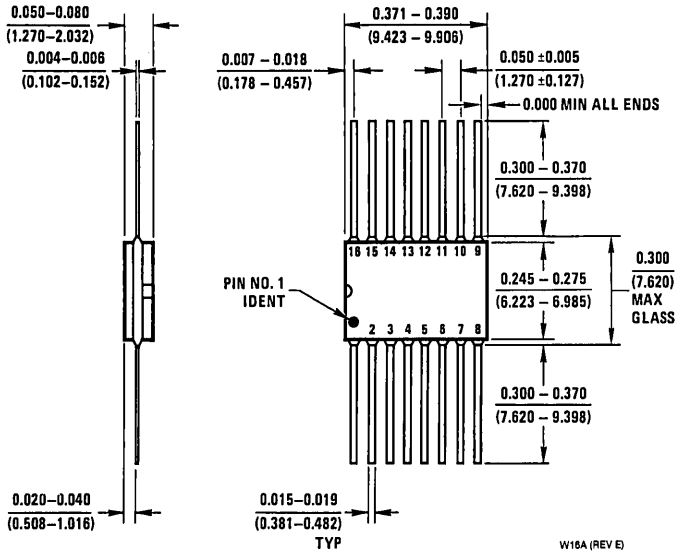


24 Lead Ceramic Dual In-Line Package (0.400" Wide) (D)
NS Package Number J24E



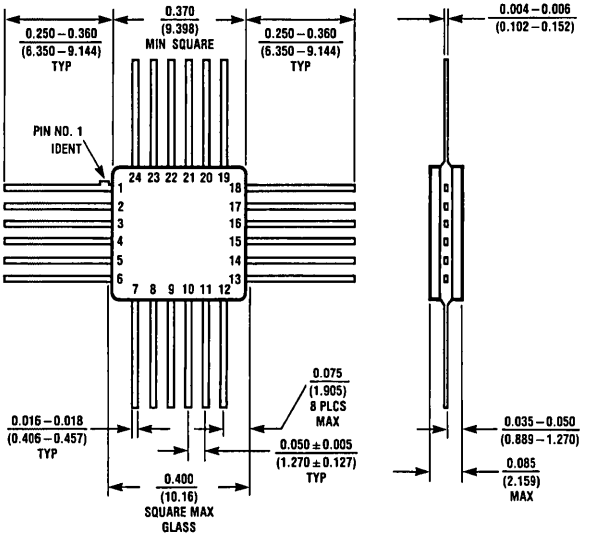
J24E (REV G)

16 Lead Ceramic Flatpak (F)
NS Package Number W16A



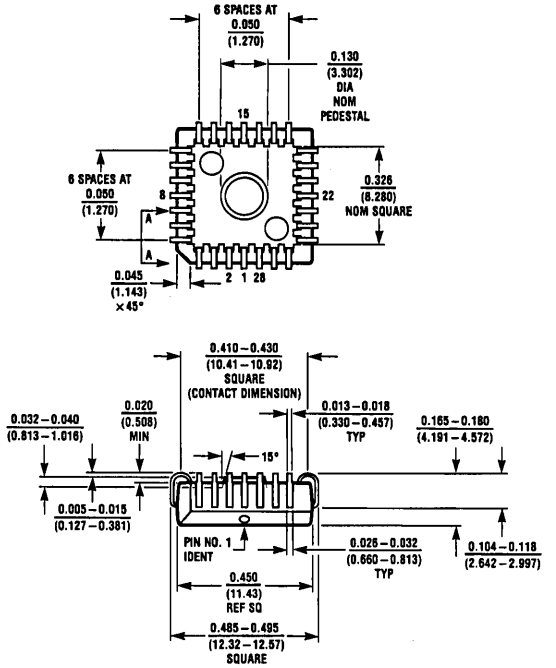
W16A (REV E)

24 Lead Quad Cerpak (F)
NS Package Number W24B



W24B (REV C)

28 Lead Plastic Chip Carrier (Q)
NS Package Number V28A



V28A (REV G)

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