coolaudio

2048-Stage Low Voltage Operation Low Noise BBD

V3208D

1. General Description

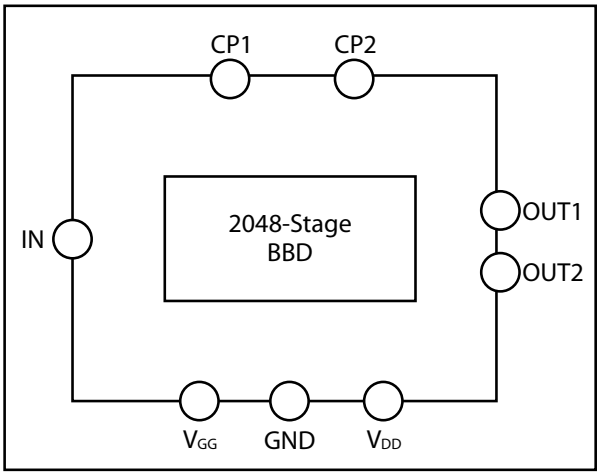
The V3208D is a 2048-stage low voltage operation (VDD = 5 V) BBD that provides a signal delay of up to 102.4 ms at clock frequency 10 KHz and is suitable for use as reverberation effect of audio equipments such as portable stereo and radio cassette recorders which need low voltage and long delay time since S/N is 71 dB in spite of many stages.

Features

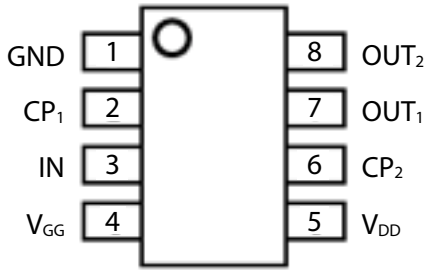
- Variable delay of audio signals: 10.24 ms ~ 102.4 ms.
- Wide power supply voltage: 4 ~ 10 V.
- No insertion noise: Li = 0 dB typ.
- Wide dynamic range: S/N = 71 dB.
- N Channel silicon gate process.
- DIP8

2. Block Diagram And Pin Description

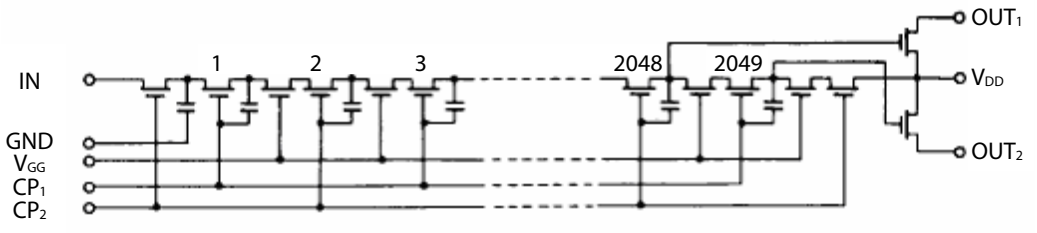
2.1 Block Diagram



2.2 Pin Configurations



2.3 Circuit Diagram



2.4 Pin Description

Pin No.	Pin Name	Description
1	GND	Ground
2	CP1	The second clock input
3	IN	Analog signal input
4	VGG	Bias voltage input (14/15 VDD)
5	VDD	Power
6	CP2	The first clock input
7	OUT1	Signal output, delayed 4096 times
8	OUT2	Signal output, delayed 4097 times

3. Electrical Parameter

3.1 Absolute Maximum Ratings

(Tamb = 25 °C, All voltage referenced to Vss, unless otherwise specified)

Characteristic	Symbol	Min.	Max.	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_i	-0.3	11	V
Output Voltage	V_O	-0.3	11	V
Operation Ambient Temp.	T_{opr}	-20	60	°C
Storage Temp.	T_{stg}	-55	125	°C
Soldering Temp	T_L		245	°C

3.2 Operating Condition

(Tamb = 25 °C , VDD = 2.5 V, fosc = 3.579545 MHz, unless otherwise specified)

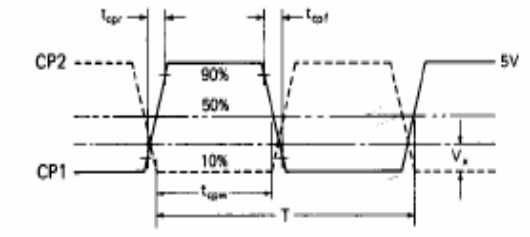
Parameter	Symbol	Min	Typ	Max	Unit
Drain Supply Voltage	VDD	4	5	10	V
Gate Supply Voltage	VGG		14/15 VDD		V
Clock Voltage High	Vcph				V
Clock Voltage Low	Vcpl	0		+0.5	V
Clock frequency	Fcp	10		100	KHz
Clock Pulse Width	Tcpw			0.5 T	
Clock Rise Time	Tcpr			500	Ns
Clock fall Time	Tcpf			500	Ns
Clock Input Cap.	Ccp			2800	Pf
Clock Cross Point	Vx	0		0.3 V_{CPH}	v

3.3 Electrical Characteristics

(Ta = 25 °C, V_{DD} = V_{CPH} = 5 V, V_{CPL} = 0 V, V_{GG} = 14/15 V_{DD}, R_L = 100 kΩ)

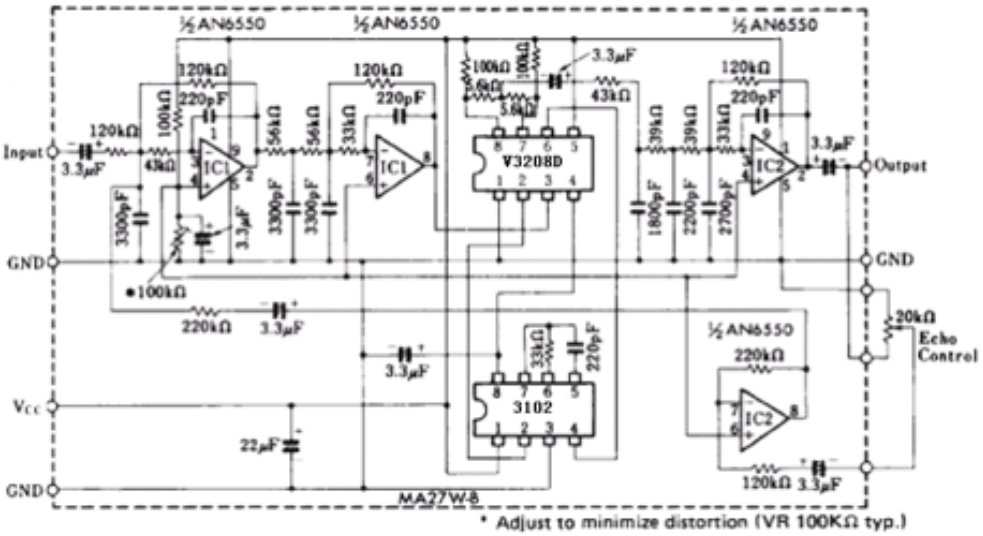
Parameter	Symbol	Min	Typ	Max	Unit
Signal Delay time	to	10.24		102.4	Ms
Input Signal Freq. fcp = 40 kHz, Output Attenuation ≤ 3 dB	fi	10			kHz
Input Signal Swing THD = 2.5%	Vi		0.36		Vrms
Insertion Loss fcp = 40 kHz, fi = 1 kHz	Li	-4	0	4	dB
Total Harm. Dist. fcp = 40 kHz, fi = 1 kHz, Vi = 0.25 Vrms	THD		0.8	2.5	%
Output Noise Voltage tcp = 100 kHz, Weighted by “A” curve	Von			0.25	mVrms
Signal to Noise Ratio tcp = 100 kHz, Weighted by “A” curve	S/N		71		dB

3.4 Clock Pulse Waveform



T = 1/fCP (Clock Period)

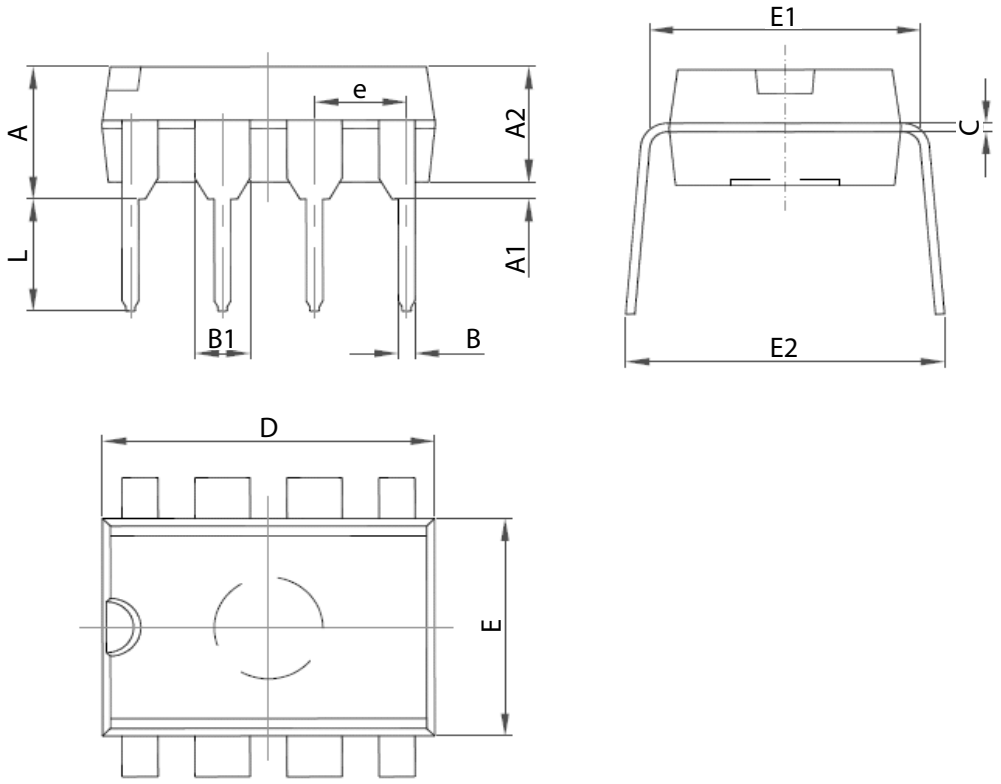
4. Typical Application Circuit



* Adjust to minimize distortion (VR 100KΩ typ.)

5. Package Information

5.1 DIP8 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100 (BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354