MOTOROLA

MC3468

Specifications and Applications Information

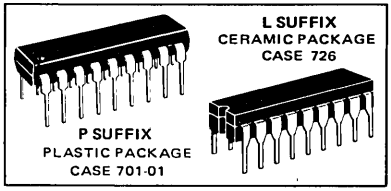
MAGNETIC TAPE
MEMORY READ AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

LSI MAGNETIC MEMORY READ SUBSYSTEM

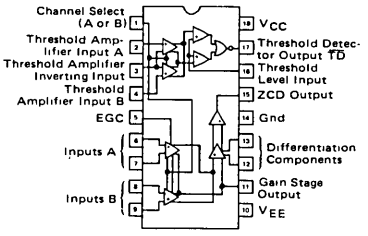
The MC3468 READ Subsystem when used with the MC3467 triple preamplifier provides the interface between magnetic tape heads and digital logic. This system is well suited for open-reel and cartridge magnetic tape systems. The MC3468 performs peak detection, and threshold detection functions as required for NRZI, Phase-Encoded or Group-Encoded recording formats. The device consists of: 1) Input Multiplex function, 2) Gain Stage with Electronic Gain Control (EGC), 3) Active Differentiation Amplifier, 4) Zero Crossing Detector (ZCD), 5) Threshold Detector Amplifier with Multiplexed Inputs and 6) Threshold Detector.

- Complete READ Function in One LSI Device
- Two Pair of Differential Inputs Allow Logically Controlled Selection of Input Filter or Tape Head Configuration
- Low Recovered Error Rate
- Input/Outputs are Low Power Schottky TTL Compatible

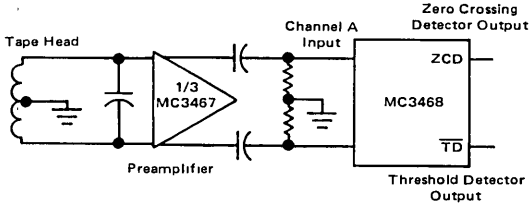


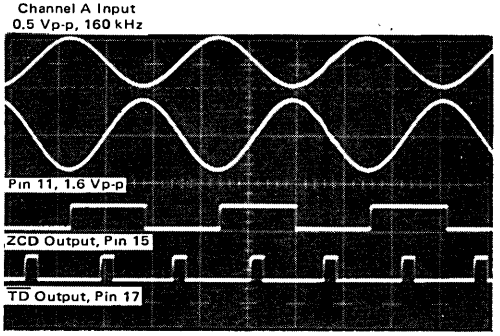
L SUFFIX
CERAMIC PACKAGE
CASE 726

P SUFFIX
PLASTIC PACKAGE
CASE 701-01



MC3468 TYPICAL APPLICATION AND WAVEFORMS





MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages			
Positive Supply Voltage	V_{CC}	+7.0	V
Negative Supply Voltage	V_{EE}	−8.0	V
Pin Voltages			
EGC Voltage (Pin 5)	$V_{I(EGC)}$	−5.0 to +7.0	V
Threshold Voltage (Pin 16)	$V_{I(T)}$	+1.0 to −3.5	V
ZCD Output (Pin 15)	$V_{O(ZCD)}$	+7.0	V
Channel Select A/B Input (Pin 1)	$V_{I(CS)}$	+7.0 to −2.0	V
Threshold Output $\overline{TD}$ (Pin 17)	$V_{O(\overline{TD})}$	+7.0	V
Differential Input Voltage			
Threshold Amplifier	$V_{ID(T)}$	±5.0	V
Gain Amplifier	V_{ID}	±5.0	V

MAXIMUM RATINGS (continued)

Rating	Symbol	Value	Unit
Common Mode Input Voltage			
Threshold Amplifier	$V_{IC(T)}$	±5 0	V
Gain Amplifier	V_{IC}	±5 0	V
Amplifier Output Short Circuit Duration (Ground Pin 11)	t_S	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE						
Power Supply Voltage Range @ T_A = 25°C						
Positive Supply Voltage		V_{CCR}	4.75	5.0	5.25	V
Negative Supply Voltage		V_{EER}	−5.5	−6.0	−7.0	V
Positive Supply Current (V_{CC} = +5.25 V)	7-13	I_{CC}	–	35	45	mA
Negative Supply Current (V_{EE} = −7.0 V)	7-13	I_{EE}	–	30	45	mA
Channel Select Input Voltage — Low Logic State		$V_{IL(CS)}$	–	–	0 8	V
Channel Select Input Voltage — High Logic State		$V_{IH(CS)}$	2.0	–	–	V
Channel Select Input Current — Low Logic State ($V_{IL(CS)}$ = 0, V_{CC} = 5.25 V)	6	$I_{IL(CS)}$	–	–	−100	μA
Channel Select Input Current — High Logic State ($V_{IH(CS)}$ = V_{CC} = 5.25 V)	6	$I_{IH(CS)}$	–	–	10	μA
GAIN AMPLIFIER SECTION						
Voltage Gain (Unbalanced @ Max Gain) (e_i = 100 mV_{p-p}, f = 1.0 kHz	1, 14	A_V	6.5	7.5	8.5	V/V
Voltage Gain (Unbalanced @ Min Gain) ($V_{I(EGC)}$ = V_{CC}, e_i = 800 mV_{p-p})	1, 14	A_{VS}	–	0.05	0.1	V/V
Operating EGC Current (V_{EGC} = 0 to +5.25 V)	1, 15	$I_{I(EGC)}$	–	–	6.0	mA
Maximum Differential Input Voltage (T_A = 25°C)		V_{IDR}	0.8	–	–	Vpp
Common Mode Rejection Ratio ($V_{I(EGC)}$ = 0, V_{CM} = 1.0 Vpp, f = 100 kHz, T_A = 25°C)	3	CMRR	40	80	–	dB
Bandwidth (−3.0 dB, T_A = 25°C)	1	BW	–	15	–	MHz
Input Resistance		r_i	30	60	–	kΩ
Channel Isolation (f = 100 kHz, e_i ≈ 800 mV_{p-p})	2, 16		40	60	–	dB
Input Bias Current	4	I_{IB}	–	5.0	15	μA
Input Common Mode Voltage Range		V_{ICR}	±1.0	±1.5	–	V
Output Resistance (Pin 11) (T_A = 25°C)		r_o	–	15	30	Ohms
Output Sink Current (Pin 11)	5	I_{OS-}	1.2	2.1	–	mA
Output Voltage Swing (Pin 11) (f = 1.0 kHz, e_i = 800 mV_{p-p})	1	V_{OR}	2.25	3.0	–	Vpp
Output Offset Voltage (T_A = 25°C)		V_{OO}	–	±400	–	mV

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, T_A = 0 to +70°C unless otherwise noted) (Continued)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Timing Distortion (I = 1.0 mA, A = 1.5 Vpp, f = 100 kHz, T_A = 25°C)	12		–	1.0	3.0	%
Zero Cross Detector – High Level Output Current (V_{OH} = 5.5 V)	8	$I_{OH(ZCD)}$	–	–	150	μA
Zero Cross Detector – Low Level Output (I_{OL} = 8.0 mA)	9	$V_{OL(ZCD)}$	–	–	0.50	V
Differentiator Output Sink Current (Pins 12 and 13)	5	$I_{O(D)-}$	1.0	1.4	–	mA
Differentiator Output Resistance (Unbalanced) (T_A = 25°C)		$r_{o(D)}$	–	20	–	Ohms
THRESHOLD AMPLIFIER SECTION						
Differential Voltage Gain (e_i = 200 mV)		A_{VD}	4.25	5.0	5.75	V/V
Maximum Differential Input Voltage Without Distortion (T_A = 25°C)		$V_{IDR(T)}$	–	–	400	mVpp
Maximum Differential Input Voltage Before Timing Shift (T_A = 25°C)		$V_{IDR(T)}$	–	–	1.4	Vpp
Maximum Threshold Voltage (Linear Operation)		$V_{IR(T)}$	–	–	−1.0	V
Threshold Voltage Required to Disable Threshold Comparators ($V_{\overline{TD}}$ > 2.7 V, T_A = 25°C)		$V_{I(T)}$	–	−2.0	−2.5	V
Bandwidth (−3.0 dB, T_A = 25°C)		BW	–	15	–	MHz
Input Resistance		$r_{i(INT)}$	25	50	–	kΩ
Threshold Amplifier Bias Current	4	$I_{IB(T)}$	–	5.0	15	μA
Channel Isolation Ratio (f = 100 kHz)	2		40	60	–	dB
Threshold Detector Output Voltage – Low Logic State (I_{OL} = 8.0 mA, Pin 17)	10	$V_{OL(T)}$	–	–	0.50	V
Threshold Detector Output Current – High Logic State (V_{OH} = 5.5 V, Pin 17)	11	$I_{OL(T)}$	–	–	150	μA
Threshold Voltage Input Current (Pin 16)		I_{THC}	–	25	50	μA

DESCRIPTION OF FUNCTION

Input Multiplex – Input multiplexing allows logic-controlled (TTL compatible) selection of either of a pair of differential gain stages. Two separate tracks or one track processed through different filter networks for different recording formats can be selected (e.g., Phase Encoded/NRZI, Group-Coded/PE).

Gain Stage – The gain stage is controlled by Electronic Gain Control (EGC) and differential outputs are provided for the active differentiator and a single output is available for the threshold function. The EGC range is from essentially zero to 7.5 (unbalanced).

Active Differentiation – Active differentiation requires minimum external passive component count. The procedure for selecting component values insures linear operation and optimum zero-crossing detector performance for excellent noise rejection.

Zero Crossing Detector (ZCD) – The zero-crossing detector generates an output transition corresponding to the peak of the incoming signal to the MC3468. Careful attention has been paid to avoid timing distortion between the outputs of the active differentiator and the inputs of the zero crossing comparator. The output is open collector Schottky TTL.

Threshold Amplifier and Detector – The gain stage output is ac coupled or differentiated into the Threshold Amplifier multiplexer. This allows logic-controlled (TTL compatible) selection of either of a pair of single-ended to differential gain stages. Thus, the possibility of selecting between a differentiated or straight capacitive coupled signal for thresholding. The select line is the same as for the Gain Stage multiplexing. The unbalanced gain of the threshold amplifier is 5. An inverting input is available for balancing the input signal to minimize the effects of offset current. The differential outputs of the threshold amplifier are compared to an external threshold in the threshold comparators. An output signal is provided whenever the signal exceeds the threshold setting in the positive or negative direction. The output is open collector Schottky TTL.

The versatility of the MC3468 facilitates the design of dual mode (NRZI/PE, Group/PE) tape drives with the ability of dynamically switch gain, active differentiator components, and thresholds for different recording speeds or interchanged tapes.

Note: For proper operation a dc path must be provided for all inputs of all amplifiers.

4

MC3468 BLOCK SCHEMATIC

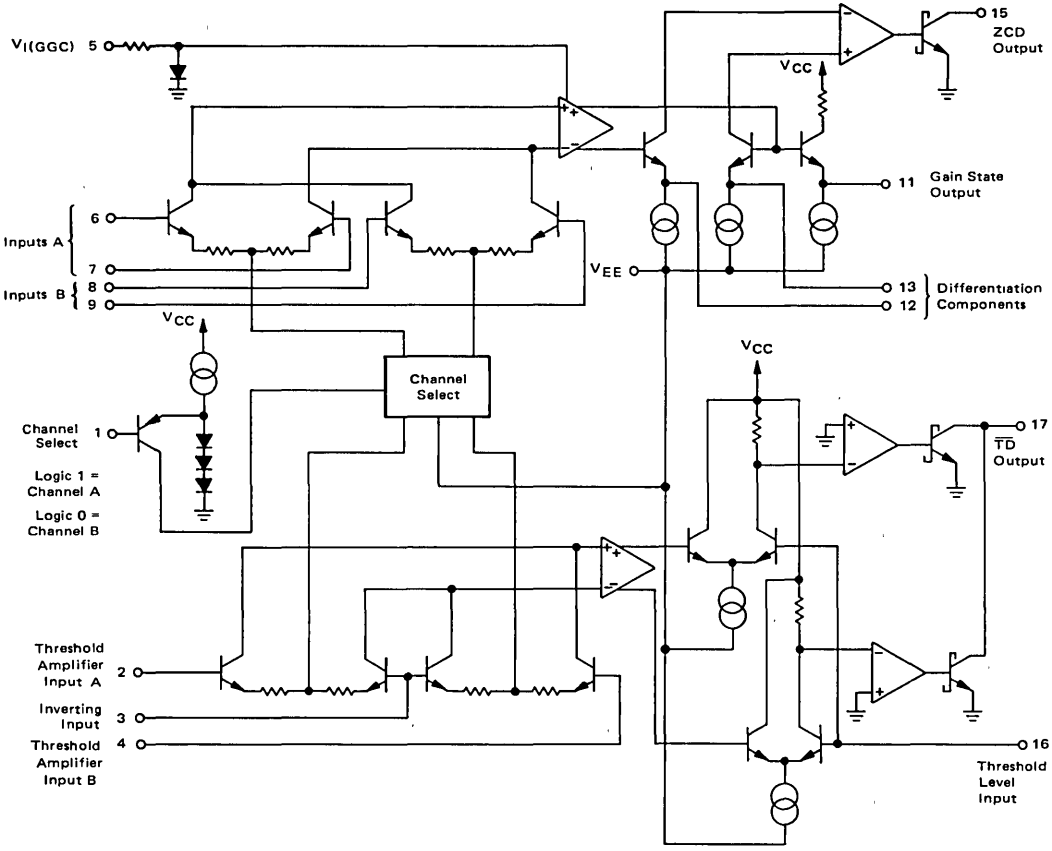


FIGURE 1 – VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING (A Input Shown)

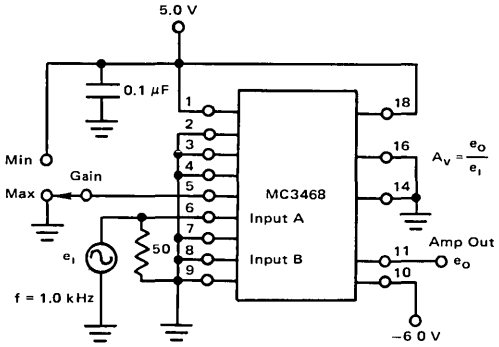


FIGURE 2 – CHANNEL ISOLATION RATIO (B Inputs Shown)

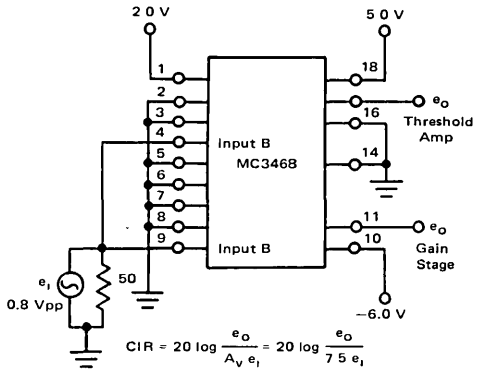


FIGURE 3 – COMMON MODE REJECTION RATIO (CMRR)

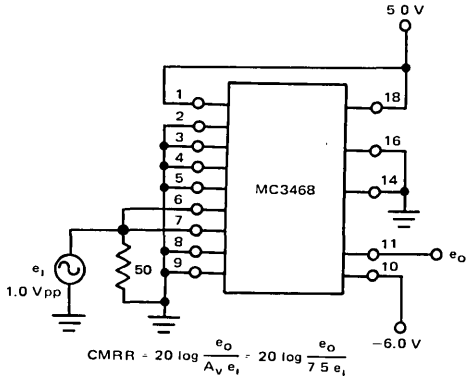


FIGURE 4 – INPUT BIAS CURRENT TEST CIRCUIT

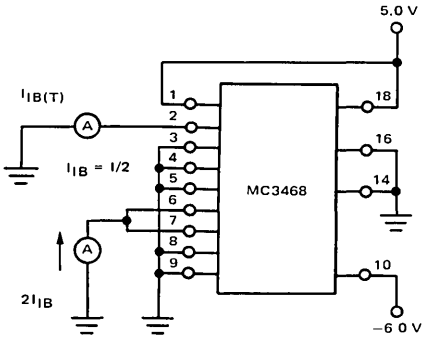


FIGURE 5 – AMPLIFIER OUTPUT AND DIFFERENTIATOR OUTPUT SINK CURRENT TEST CIRCUIT

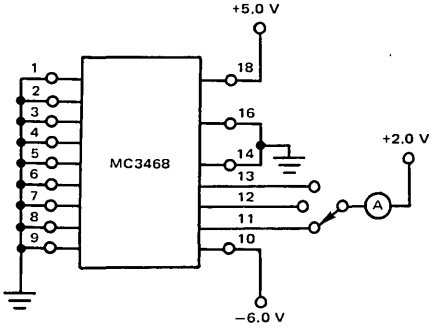


FIGURE 6 – CHANNEL SELECT INPUT CURRENT TEST CIRCUIT

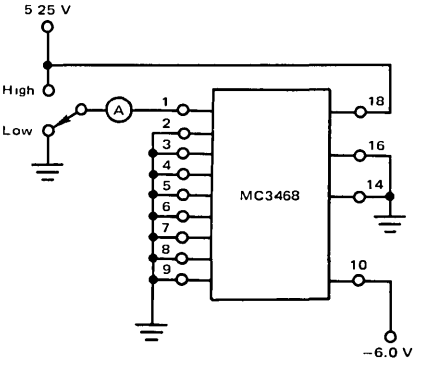


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FIGURE 7 – POSITIVE AND NEGATIVE SUPPLY CURRENT TEST CIRCUIT

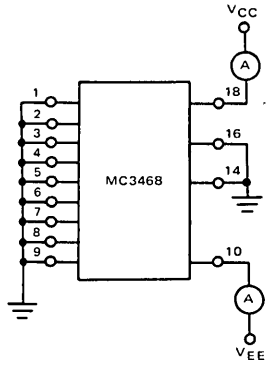


FIGURE 8 – ZERO CROSS DETECTOR OUTPUT CURRENT HIGH LOGIC STATE TEST CIRCUIT

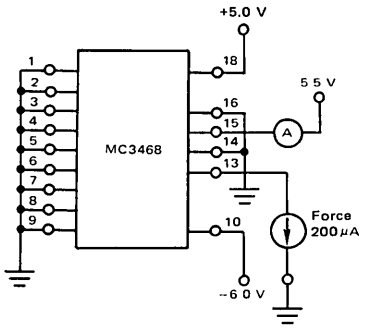


FIGURE 9 – ZERO CROSSING DETECTOR OUTPUT VOLTAGE LOW LOGIC STATE TEST CIRCUIT

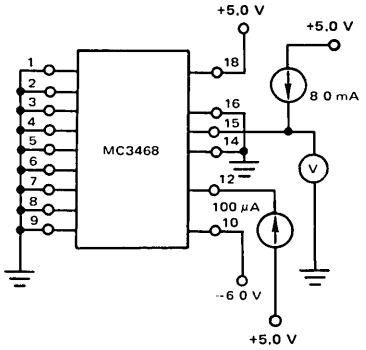


FIGURE 10 – THRESHOLD DETECTOR OUTPUT VOLTAGE – LOW LOGIC STATE TEST CIRCUIT

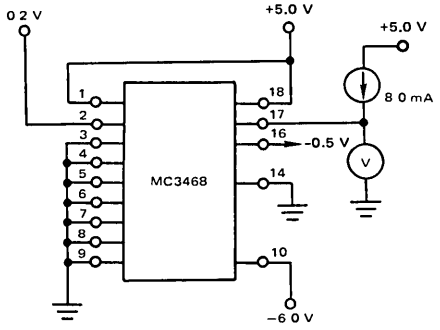


FIGURE 11 – THRESHOLD DETECTOR OUTPUT CURRENT – HIGH LOGIC STATE TEST CIRCUIT

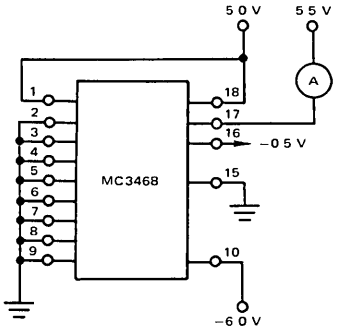
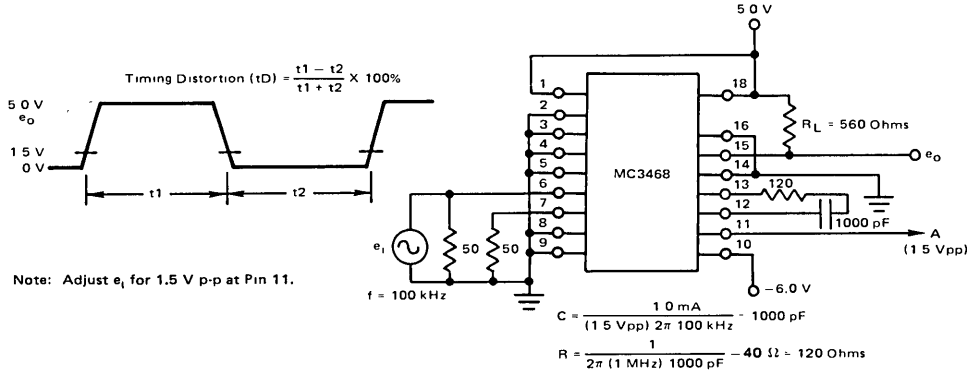


FIGURE 12 – TIMING DISTORTION $T_A = 25^oC$



TYPICAL PERFORMANCE CURVES

FIGURE 13 – NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

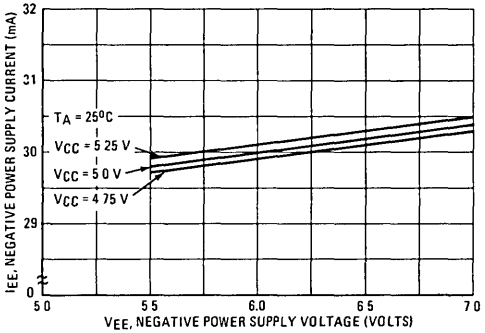


FIGURE 14 – NORMALIZED VOLTAGE GAIN versus EGC INPUT VOLTAGE

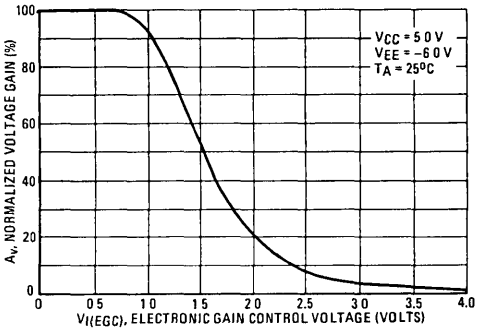


FIGURE 15 – ELECTRONIC GAIN CONTROL INPUT CURRENT versus VOLTAGE

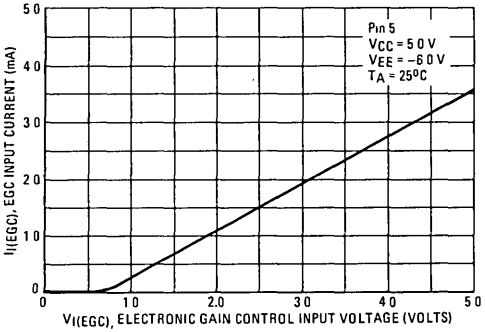


FIGURE 16 – CHANNEL ISOLATION RATIO versus FREQUENCY

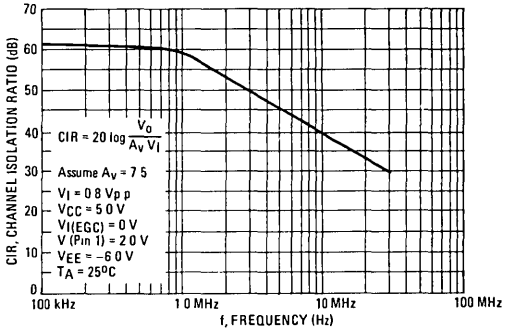
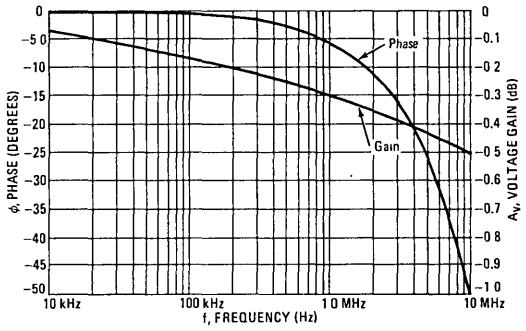


FIGURE 17 – GAIN AND PHASE versus FREQUENCY FROM Pins 6, 7 to Pins 12, 13



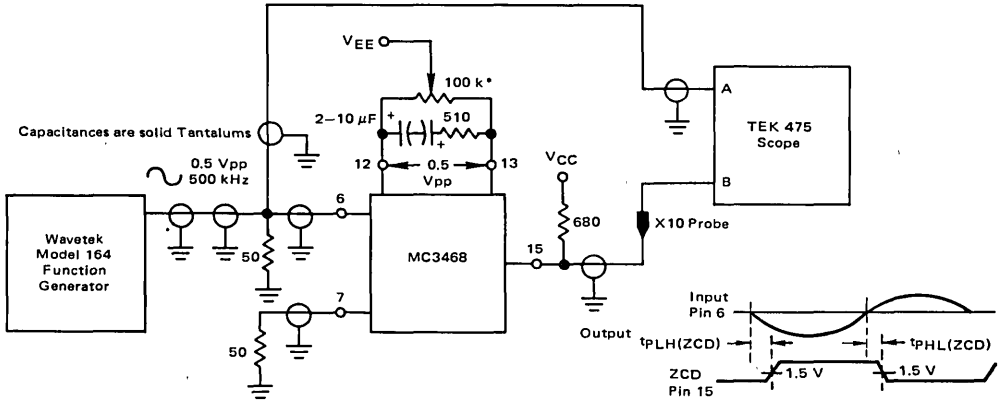
SYSTEM PARAMETERS

The following system parameters are characteristic of not only the device but external component values and circuit layout. Detailed test circuits and measured parameters are provided only as a guide to expected system performance. These parameters are not readily measureable on a production volume basis.

FIGURE 18 – TEST CIRCUIT FOR MEASURING PROPAGATION DELAYS

From Gain Stage Input to Zero Crossing Detector Output

(Pin 6 to Pin 15) (Subtract 8 ns from measurement for probe and cable delays)

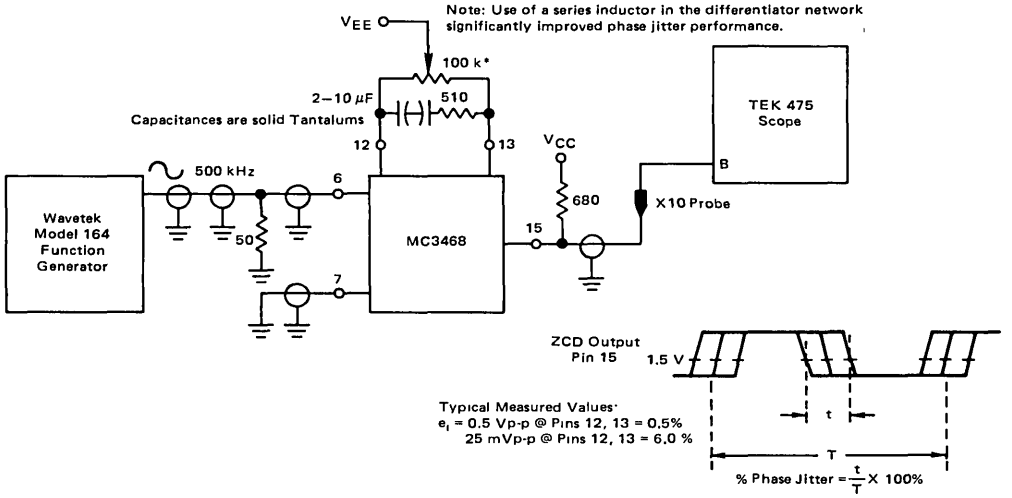


Note: Symmetry is adjusted @ 50 kHz and 50 mVpp

*Adjust 100 k per Figure 21, Part II

Typical Measured Values $t_{PLH(ZCD)}$ = 40 ns, $t_{PHL(ZCD)}$ = 50 ns

FIGURE 19 – TEST SETUP FOR MEASURING PHASE JITTER

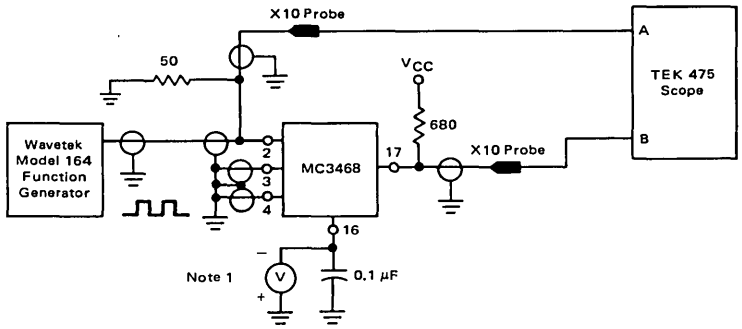


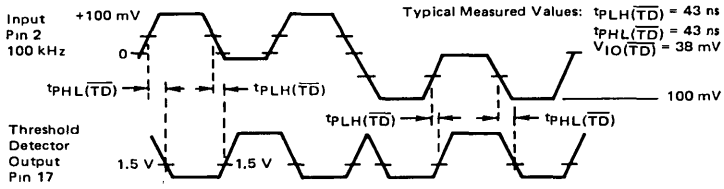
Typical Measured Values:
e_i = 0.5 Vp-p @ Pins 12, 13 = 0.5%
25 mVp-p @ Pins 12, 13 = 6.0 %

$$\% \text{ Phase Jitter} = \frac{t}{T} \times 100\%$$

Note: The jitter window, t, is defined as the 3 σ points on a Gussion curve.

FIGURE 20 – TEST SETUP FOR THRESHOLD AMPLIFIER DELAY AND THRESHOLD COMPARATOR EQUIVALENT OFFSET MEASUREMENTS



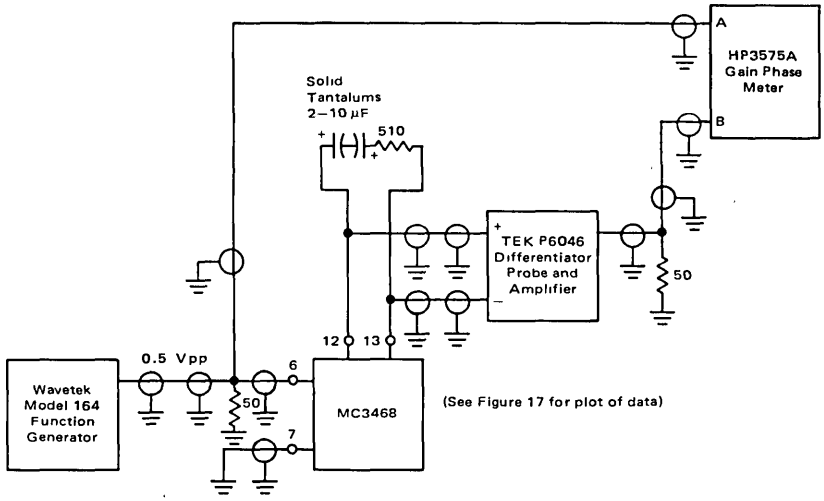


Notes: 1. For Delay measurements, V is fixed at −250 mV; for equivalent comparator offset voltage measurements, V is adjusted until Pin 17 goes low. The voltage, V, is the equivalent offset, $V_{IO(\overline{TD})}$.

2. Some compensation is possible using a resistor from Pin 3 to ground.

FIGURE 21 – TEST SETUP FOR GAIN AND PHASE versus FREQUENCY (5 kHz to 1 MHz) FROM INPUT TO DIFFERENTIATOR (Pin 6, 7 to Pin 12, 13)

Actual Test Measurements (Calibrate Instrumentation for Phase Compensation)



DESIGN SUGGESTIONS

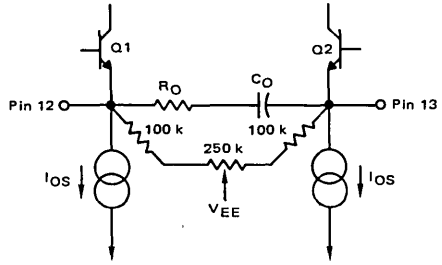
Gain Stage Bias Current

One must consider supplying 15 μA of bias current to the Gain Stage when designing a filter network. A good design value for the equivalent resistance from each input leg to ground is 5 kΩ.

II Adjusting Peak Shift to Zero (See Figure 22)

The worst peak shift observed on the ZCD output occurs for the smallest slew rate provided by the Active Differentiator at the ZCD inputs. In Turn, the Active Differentiator produces the smallest slew rate when the gain-bandwidth product applied at its inputs is the smallest. Current source, resistors, and diode imbalances will exhibit the maximum peak shift under this condition. Using the resistor network shown, these imbalances are adjusted out for the worst case condition.

FIGURE 22 – PEAK SHIFT NETWORK



Note: The 100 kΩ resistors should be close to the IC to suppress noise.

MC3468 APPLICATIONS INFORMATION

MC3468 For NRZI Encoded Magnetic Tape

NRZI Encoding was one of the first popular recording formats and is formalized as an American National Standard for the purpose of facilitating the interchange of magnetic tapes. Although the Phase-Encoded format is now more widely accepted than NRZI, vast libraries of NRZI tapes still exist. Computers will be reading these tapes for years to come, and in some cases, re-writing them in phase-encoded format. Thus, the ability of the tape drive electronics to read both NRZI and PE tapes is a feature often sought in new designs.

For NRZI recording, the magnetic surface of the tape is magnetized to saturation in one direction or the other each time a logical "1" is to be recorded. The magnetization remains unchanged for a logical "0". The resulting signal from the read head for a typical NRZI data stream is shown in Figure 23. The NRZI data stream consists of a continuum of Fourier components up to a maximum frequency of $5f_H$, where f_H is numerically equal to one-half the maximum flux changes per second (FCPS). For long strings of zeroes, the lowest Fourier component could theoretically be near dc, but on a typical tape a long interval with no "1's" is not allowed. Consequently, most of the energy in the pulse train is around f_H and its harmonics (up to the fifth). A suitable corner frequency for ac coupling from the preamplifier is 60 Hz, although for high speed systems it could be considerably higher (1/10 fH). The -3 dB frequency of a low pass filter is usually placed at a frequency greater than f_H. In most systems, this low pass filter must do more than provide a roll-off for high-frequency transients. It also equalizes the read amplifier chain and differentiation network for linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated either as part of the ac coupling between the preamplifier and amplifier or as part of the differentiation network.

The American National Standard specifies that NRZI be recorded at 800 BPI (Bits Per Inch) on open reel magnetic tape. Typical read/write tape speeds range from 12.5 to 300 IPS (Inches Per Second). Examples 1 and 4 show MC3468 NRZI designs.

MC3468 For Phase-Encoded (PE) Magnetic Tape

Of the numerous methods for encoding digital data on magnetic tape, phase encoding is currently most popular. As shown in Figure 23, data is represented by transitions occurring in the middle of a "data cell". A low-to-high flux transition (toward the magnetization level representing erased tape) is defined as a logical "one" and a high-to-low transition is defined as a logical "zero". For consecutive "one's" or "zero's" phase transitions are introduced as needed at the "data cell" borders. Phase transitions are not required when the encoded data consists of "one-zero" patterns.

The read head signal resulting from mixed data streams consists of two fundamental frequencies, f_H and f_L which represent most of the harmonic content (with some energy at harmonics up to the fifth). These are numerically equal to $\frac{FCPI}{2} \times IPS$ and $\frac{FCPI \times IPS}{4}$ (where FCPI is maximum flux changes per inch and IPS is tape speed in inches per second). In high-speed, low-level systems, the amplitude of these read head signals is only a few millivolts and conditioning with a preamplifier such as the MC3467 followed by a passive bandpass filter is required. The bandpass characteristic sets the lower −3 dB frequency below f_L and the upper −3 dB frequency above f_H. In most systems, the bandpass filter must do more than filter out noise. The low-pass portion also equalizes the read amplifier chain and differentiation network for a linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated as part of the filter between the preamplifier and amplifier or as part of the differentiation network.

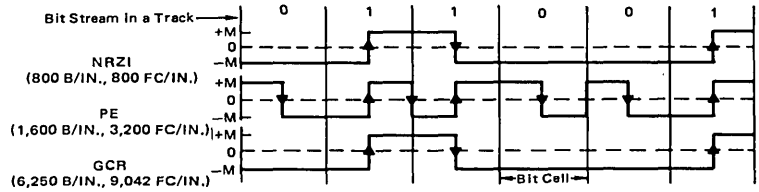
The American National Standard specifies that PE data be recorded at 1600 BPI (Bits Per Inch) on open reel magnetic tape. Typical read/write tape speeds range from 6.25 to 200 IPS (Inches Per Second). Cartridges use 1600 BPI and have tape speeds of 30 IPS for read/write. Examples 2, 3, and 4 show MC3468 designs for PE systems.

MC3468 For Group Code Recorded (GCR) Magnetic Tape

Basically, Group-Coded Recording (GCR) is a high density recording scheme which uses the NRZI convention for "1's" and "0's", but adds the restriction that flux changes occur at least once in every three bit cells (Figure 23). The read head signal resulting from mixed data streams consists primarily of Fourier components from f_L to $3f_L = f_H$ and their harmonics up to the fifth. The frequencies f_L and f_H are numerically equal to $\frac{FCPI \times IPS}{2}$ and $\frac{FCPI \times IPS}{6}$, respectively (where FCPI is maximum flux changes per inch and IPS is tape speed in inches per second). The amplitude of the read head signals is only a few millivolts or less and conditioning with a preamplifier such as the MC3467 followed by a passive bandpass filter is required. The bandpass characteristic sets the lower −3 dB frequency below f_L and the upper −3 dB frequency above f_H. The bandpass filter must do more than filter out noise. The low pass portion equalizes the read amplifier chain and differentiation network for linear phase versus frequency response. Once the transfer function of this equalization filter is known, it may be incorporated as part of the filter between the preamplifier and amplifier or as part of the differentiation network.

The proposed American National Standard specifies that GCR data be recorded at 9042 FCPI (Flux Changes Per Inch). Because of the data format, the usable data density is 6250 BPI rather than 9042 BPI. The "6250 BPI" is a throughput specification and should not be used in read amplifier calculations. The original GCR concept was intended for high speed drives (200 IPS). However, it is also being applied to lower speed (125 IPS) systems. Examples 5 and 6 illustrate the use of the MC3468 in GCR systems.

FIGURE 23 – MOST POPULAR MAGNETIC TAPE RECORDING FORMATS



CIRCUIT OPERATION

4

(See Figure 24 for component wiring and Figures 25 and 26 for Timing Diagrams)

The operation of the MC3468 is similar for NRZI, PE, and GCR data formats. The preamplifier and filtered signal is applied differentially to either Channel A or B Gain Stages. The Gain Stage output differentially feeds an Active Differentiator and a single-ended output is available for straight capacitive or differentiated (active or passive) coupling into either Channel A or B inputs to the Threshold Amplifier.

For the circuit configuration shown, the Active Differentiator output leads the input by almost 90°. The Active Differentiator output is applied to a Zero-Crossing Detector, which goes low for positive levels and high for negative levels, changing state at the zero crossings. The Threshold Circuit amplifies the Gain Stage output and compares positive and negative signals to a threshold level. When the level is exceeded, the $\overline{TD}$ output is low. From the waveforms, it is seen that the ZCD output makes a transition approximately in the middle of the period when $\overline{TD}$ is low. Wiring ZCD "anded" with TD to the set input and $\overline{ZCD}$ "anded" with TD to the "reset" input of the R-S type flip-flop reconstructs the data stream encoded on the tape. This circuit works for zero clip (zero threshold) operation, but has the disadvantage that timing distortion results from capacitive loading. Digital circuits for reconstructing the data stream which utilize pipe-line delays to overcome capacitive loading timing distortion are shown in Figure 27.

FIGURE 24 – TYPICAL MC3468 COMPONENT HOOKUP

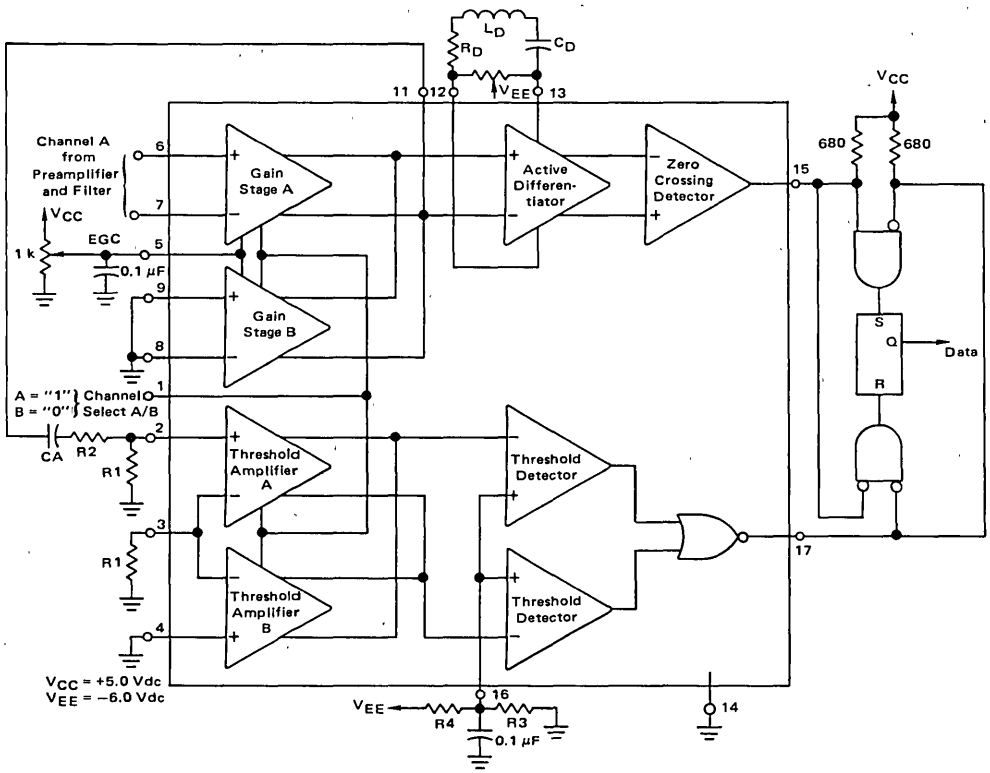


FIGURE 25 – WAVEFORMS SHOWING MC3468 OPERATION FOR NRZI DATA

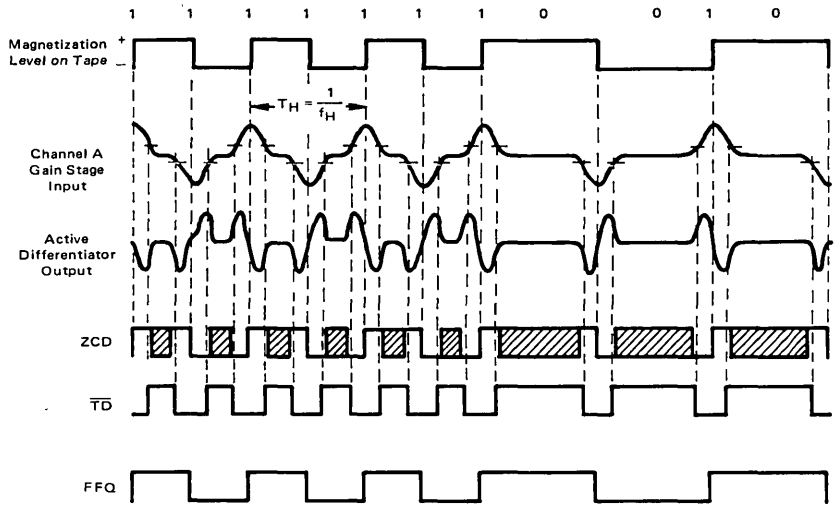


FIGURE 26 – TIMING DIAGRAM WAVEFORMS SHOWING MC3468 OPERATION FOR PHASE-ENCODED DATA

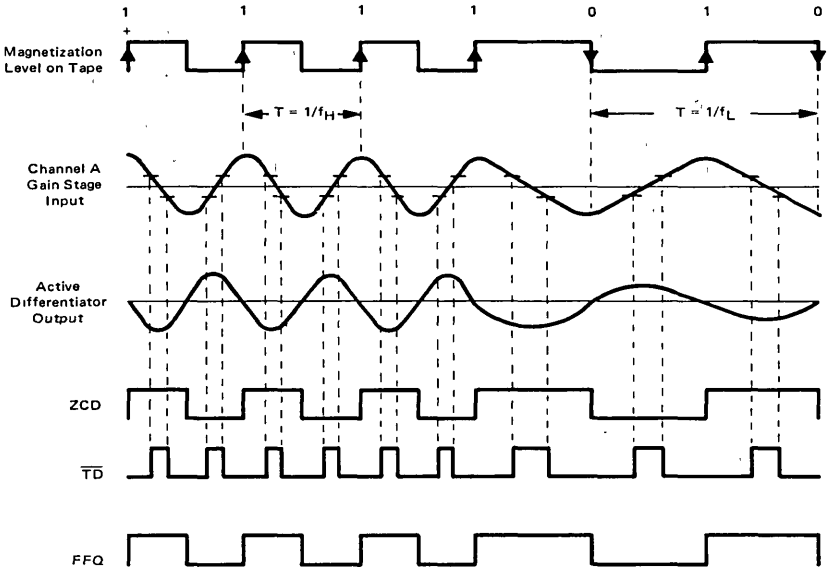
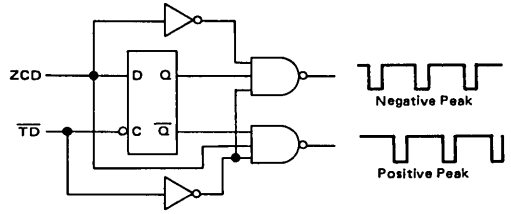
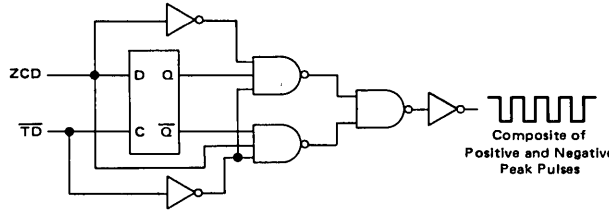


FIGURE 27 – OTHER DIGITAL CIRCUITS FOR RECONSTRUCTING DATA STREAMS FROM THE MC3468

1) Dual Output Circuit (Pipeline Delay for Negative Edge Must Be the Same for Both Outputs)



2) Single Output Circuit (Operation Independent of Capacitive Loading Effects on Delays)



4

Group Delay Distortion

The ultimate purpose of the magnetic read amplifier chain in Figure 28 is to produce a digital signal with transitions corresponding to the peaks of a read head signal. Because the active and passive elements in the chain exhibit phase characteristics, there will be a "pipe-line" delay between peaks at the read head and the digital output from the zero-crossing detector. Variations in this delay with frequency or amplitudes cause timing distortion which translates directly into increasing error rates. The primary consideration in the read chain implementation is to equalize the read chain for almost flat delay over the frequencies and amplitudes of required operation. Figure 28 depicts one of several possible read chain configurations which can be equalized for best-flat time delay performance.

The determination of the component values is relatively straight forward provided the active elements have negligible phase characteristics in the frequency range of operation. Below 1 MHz, the MC3467/MC3468 read chain active elements have negligible phase characteristics. Although phase effects start showing above 1 MHz, phase versus frequency is linear (constant time delay).

Other read chain configurations have a band-pass filter between the preamplifier and Gain Stage. It is possible to move some of the poles of the filter into the active differentiator. The technique suggested in Figure 28 transfers poles into the active differentiator to minimize component count. The insertion loss of the technique is also less than an equalization filter ahead of the READ amplifier.

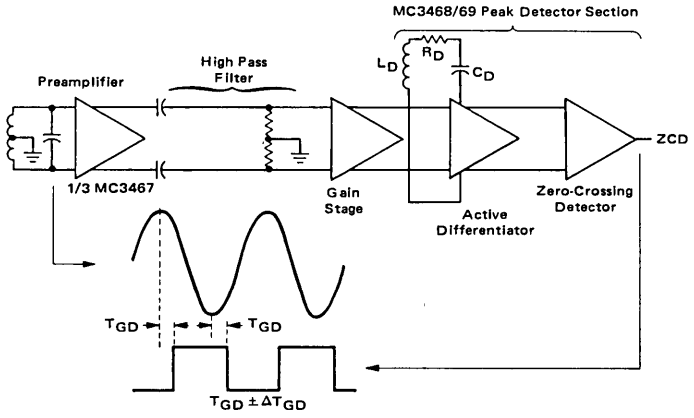


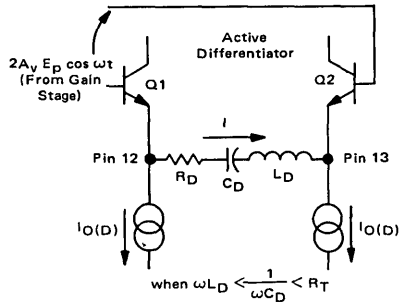
FIGURE 28 – GROUP DELAY DISTORTION THROUGH READ CHAIN

Determining R_D, C_D, and L_D For the Active Differentiator

For the equalized read chain shown in Figure 28, C_D, R_D and L_D are determined respectively in that order. The phase characteristics of the active elements are assumed to be negligible.

An active differentiator is formed by R_D, C_D and L_D coupling the emitters of a differential amplifier having current sources I_{OD} in each leg. If a differential voltage $A_V E_p \cos \omega t$ is applied to the Active Differentiator, the resulting current through R_D and C_D is:

$$I = \frac{2A_V E_p}{\sqrt{R_T{}^2 + \left(\frac{1}{\omega C_D} + \omega L_D\right)^2}} \cos\left\{\omega t - \arctan\left(\frac{-1/\omega C_D}{R_T}\right)\right\}$$



$I \cong 2A_V E_p C_D \omega \sin \omega t$

where $2A_V E_p$ is the product of the differential input to the Gain Stage E_p and its unbalanced gain, A_V.
where R_T is the total of R_D and the output impedances of Q1 and Q2. The combined output impedances of Q1 and Q2 is 40 Ohms.

This condition is approximated for $\frac{1}{R_T C_D} = \omega_C = 3\omega_H$ (where ω_H is the maximum applied frequency of appreciable Fourier content).

The peak value of I (i.e., $2A_V E_p C_D \omega$) is important. As I approaches $I_{O(D)}$, the transistor Q2 turns off and the waveform at Pin 12 distorts. The circuit no longer behaves as a differentiator and peak distortion results.

For best zero crossing detector performance, it is essential that I be maximized. A design value of I which results in good noise performance and minimum peak shift is 900 microamperes.[1]

$$I = 2A_V E_p C_D \omega = 900 \times 10^{-6}$$

Rearranging the equation for I,

$$\boxed{C_D = \frac{900 \times 10^{-6}}{2A_V E_p \omega}}$$

Also, solving $\omega_C = \frac{1}{R_T C_D}$ for R_T,

$$R_T = \frac{1}{\omega_C C_D}$$

Assuming the output impedance of Q1 and Q2 combined is 40 Ohms,

$$\boxed{R_D = \frac{1}{\omega_C C_D} - 40}$$

where $\omega_C = 3\,\omega_H$.

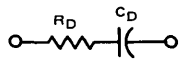
As shown in Table 1, the addition of an inductor, L_D, significantly improves phase linearity versus frequency as well as providing a roll off for high frequency noise. This optimum solution requires the following relationships:

$$\frac{2}{R_T C_D} = \frac{R_T}{L_D}$$

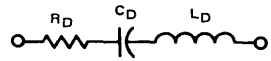
rearranging, $\boxed{L_D = \frac{R_T{}^2 C_D}{2}}$

[1] For optimum zero-crossing detector performance, dI/dt should be as large as possible at zero-crossing. Motorola guarantees a minimum $I_{O(D)}$ of 1.0 mA.

TABLE 1 – PHASE LINEARITY (CONSTANT TIME DELAY) PERFORMANCE FOR RC versus RLC ACTIVE DIFFERENTIATOR NETWORK



$\omega_C = \frac{1}{R_D C_D} = 3\omega_H$



$\omega_n = \frac{\sqrt{2}}{R_D C_D} = \frac{1}{\sqrt{LC}}$

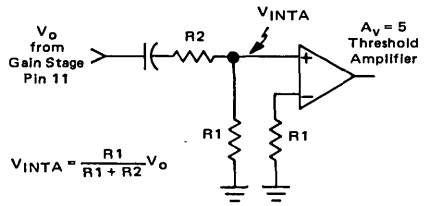
$\frac{\omega}{\omega_C}$	θ	$\Delta\theta$	$\frac{\omega}{\omega_n}$	θ	$\Delta\theta$
1.0	+45.00		1.0	0	
0.9	+48.01	+3.01	0.9	+8.49	+8.49
0.8	+51.34	+3.33	0.8	+17.65	+9.16
0.7	+55.01	+3.67	0.7	+27.26	+9.61
0.6	+59.04	+4.03	0.6	+37.03	+9.77
0.5	+63.43	+4.39	0.5	+46.69	+9.66
0.4	+68.20	+4.77	0.4	+56.04	+9.35
0.3	+73.30	+5.10	0.3	+65.00	+8.96
0.2	+78.69	+5.39	0.2	+73.58	+8.58
0.1	+84.29	+5.60	0.1	+81.87	+8.29

4

Threshold Considerations

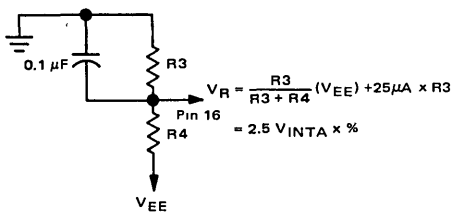
The threshold circuitry is used in read after write systems to insure that good data was written, to set up gain during an ID burst, and sometimes to indicate a minimum signal voltage for invalid data. Optimum thresholding requires a large swing at the threshold amplifier inputs. A good design value for V_{INTA} is 1.0 Vp-p, and should not exceed 1.4 Vp-p. If it does, a timing shift results. Internal clipping is provided for all signals greater than 400 mVp-p. The distortion resulting from clipping has no effect on thresholding because only peaks are clipped.

As shown in Figure 24, the Gain Stage output at Pin 11 is ac coupled to the threshold amplifier so that voltage offsets do not influence thresholding. An attenuator, R1/R2, is often required in the ac coupling networks because the gain stage output is between 1.6 Vp-p and 2.4 Vp-p for optimum zero-crossing-detector performance.



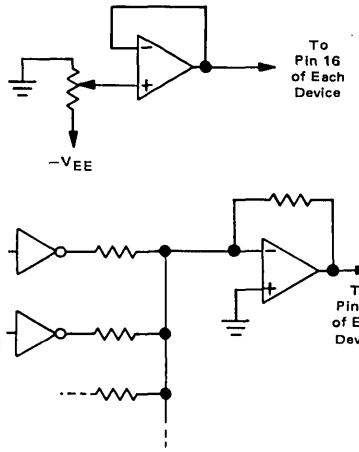
The magnitude of R1 should be less than 5 kΩ to minimize the effects of Threshold Amplifier Bias current (I_{THA} = 15 μA). Also, R1 + R2 must be greater than 3 kΩ because the minimum output sink current (I_{OS}) of the Gain Stage is 1.5 mA. A resistance equal to R1 should be wired to ground from the – leg of the Threshold Amplifier (minimize offset bias current effects).

Note that only the selected amplifier input contributes to bias current. Each output of the Threshold Amplifier is 5 V_{INTA}, and is applied to its resepctive Threshold comparator. Each comparator sees 2.5 V_{INTA}. Thresholding is based on a percentage of the nominal voltage applied to the comparators, 2.5 V_{INTA}. Both positive and negative references are derived from V_{EE} as follows:



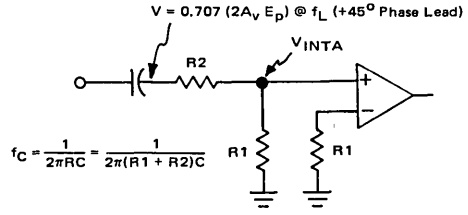
R3 should be less than 1 kΩ to minimize the effects of Threshold Comparator Bias Current (I_{THC} = 50 μA). A 0.1 μF decoupling capacitor is required for transients.

The following circuits are useful for multi-channel and/or dynamic threshold switching applications.



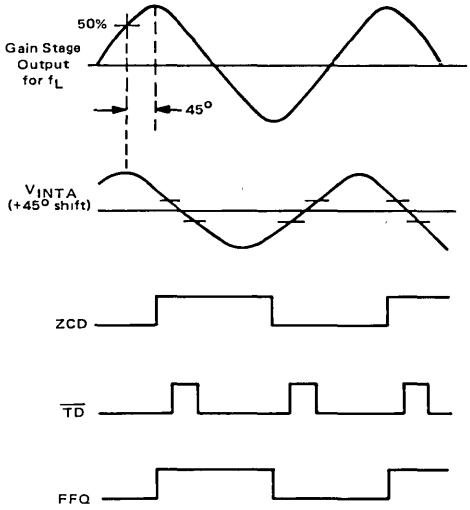
Base Line Shift in PE Systems

In phase-encoded recording, the read signal may not make symmetrical transitions about the zero bias level. A lower amplitude signal with a low frequency component is often superimposed. Although a highpass filter attenuates some of this component, its frequency is often close to the –3 dB frequency of the filter and may be only –6 dB down from signal amplitudes. This baseline shift has no adverse effects on the performance of the Active Differentiator. However, the Threshold Detector is sensitive to the unequal signal peaks. Signal-to-noise ratio can be improved by performing a passive differentiation into the Threshold Amplifier. With the corner frequency, f_C, placed at f_L, the f_L signal is attenuated –3 dB; the $f_H = 2f_L$ signal is for all practical purposes unattenuated. Figure 29 shows the 45° phase lead introduced by passive differentiation. Note that this technique is not directly applicable to high thresholds because the ZCD transitions fall outside the thresholding window. However, the threshold window can be delayed to overcome this drawback.



The design of the attenuator, R1/R2, follows as described previously. Example 3 shows a typical application of passive differentiation to overcome base-line shift.

FIGURE 29 – RESULTING OPERATION FOR PASSIVE DIFFERENTIATION INTO THRESHOLD AMPLIFIER



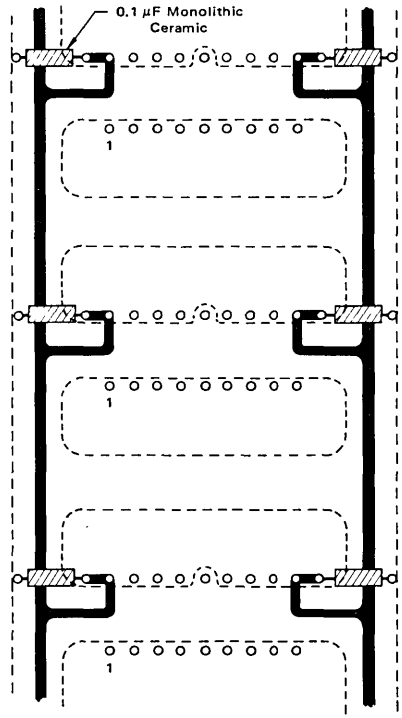
Board Layout and Testing Considerations

An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 30.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in 3-dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC, also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients. One from V_{CC} to ground and one from V_{EE} to ground for each IC package. Keep lead lengths to ¼ inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible. The lead on Pin 15 will radiate and can couple back into the active differentiator. This will result in excessive phase jitter. The tell-tale behavior is a ringing at Pin 11 corresponding to the transitions at Pin 15. To overcome this coupling problem, keep the lead on Pin 15 short and isolated from the other Input/Output lines to the MC3468. Preferably, put it over or next to a ground plane. For long distance runs, use a twisted pair or coaxial cable.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test set-ups must be calibrated at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 30 – POWER AND GROUND DISTRIBUTION FOR MC3468 PRINTED CIRCUIT BOARD LAYOUT



Note: Dotted Lines Outline Ground Plane on Back Side of Printed Circuit Board

4

EXAMPLES

Example #1 (See Figure 24 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: NRZI
Recording Density: 800 BPI (800 FCPI)
Tape Speed: 200 IPS
Signal into Gain Stage

$$E_{pp} = 0.3 \text{ to } 0.6 \text{ Vp-p @ } 80 \text{ kHz}$$

Threshold: 25% of minimum voltage peaks

The voltage from the Gain Stage is designed for 1.6 Vp-p at Pin 11.

$$\frac{1.6}{0.6} = A_v = 2.7$$

Set the EGC for a gain of 2.7, unbalanced.

The maximum p-p voltage to the Threshold Amplifier, V_{INTA}, is designed for 1 Volt. The required attenuation factor is $\frac{1}{1.6}$.

$$\frac{V_{INTA}}{V_O} = \frac{R1}{R1 + R2} = \frac{1}{1.6}$$

$$R1 + R2 \geq 3 \text{ k}\Omega \text{ and } R1 \leq 5 \text{ k}\Omega \text{ (See text)}$$

These constraints are satisfied when R1 = 4.7 kΩ and R2 = 3 kΩ. This is an optimum solution for a minimum coupling capacitor value.

Now consider the minimum voltage applied to the Threshold Amplifier

$$V_{INTA(MIN)} = \frac{1}{1.6} \times 2.7 \times 0.3 = 0.5 \text{ Vp-p}$$

The threshold comparator reference voltage, V_R, is set at 25% of $2.5 V_{INTA(MIN)}$

$$V_R = 0.25 \times 2.5 \times 0.5 \cong 300 \text{ mV}$$

$$-300 \times 10^{-3} = \frac{R3}{R3 + R4}(-6)$$

$$R3 \leq 1 \text{ k}\Omega \text{ (See text)}$$

Let R3 = 470 Ω; then R4 ≅ 10 kΩ

The values of R_D and C_D are determined from the equations given in the text.

$$C_D = \frac{900 \times 10^{-6}}{2A_v E_p \omega} = \frac{900 \times 10^{-6}}{A_v E_{pp} \omega}$$

$$= \frac{900 \times 10^{-6}}{2.7 \times 0\,6 \times 2\pi \times 80 \times 10^3}$$

$$C_D \cong 1000 \text{ pF}$$

Assume $f_c = 3f$

$$R_D = \frac{1}{\omega C C_D} - 40 = \frac{1}{2\pi \times 3 \times 80 \times 10^3 \times 10^{-9}} - 40$$

$$R_D = 670 - 40 \cong 600 \ \Omega$$

$$L_D = \frac{R_T^2 C_D}{2} = \frac{(670)^2 \times 10^{-9}}{2} = 224 \ \mu\text{H}$$

Example #2 (See Figure 24 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Phase-Encoded
Recording Density: 1600 BPI (3200 FCPI)
Tape Speed: 200 IPS
Signal Into Gain Stage

$$E_{pp} = 0.2 \text{ Vp-p @ } 320 \text{ kHz}$$
$$0.4 \text{ Vp-p @ } 160 \text{ kHz}$$

Threshold: 25% of minimum voltage peaks

The voltage from the Gain Stage is designed for 1.6 Vp-p at Pin 11.

$$\frac{1.6}{0.4} = A_v = 4$$

Set the EGC for a gain of 4, unbalanced.

The maximum p-p voltage to the Threshold Amplifier, V_{INTA}, is designed for 1 Volt. The required attenuation factor is $\frac{1}{1.6}$.

$$\frac{V_{INTA}}{V_O} = \frac{R1}{R1 + R2} = \frac{1}{1.6}$$

$$R1 + R2 \geq 3 \text{ k}\Omega \text{ and } R1 \leq 5 \text{ k}\Omega \text{ (See text)}$$

These constraints are satisfied when R1 ≅ 4.7 kΩ and R2 ≅ 3 kΩ. This is an optimum solution for a minimum coupling capacitor value. Now consider the minimum voltage applied to the Threshold Amplifier.

$$V_{INTA(MIN)} = \frac{1}{1.6} \times 4 \times 0.2 = 0.5 \text{ Vp-p}$$

The threshold comparator reference voltage, V_R, is set at 25% of $2.5 V_{INTA(MIN)}$

$$V_R = 0.25 \times 2.5 \times 0.5 \cong 300 \text{ mV}$$

$$-300 \times 10^{-3} = \frac{R3}{R3 + R4}(-6)$$

$$R3 \leq 1 \text{ k}\Omega \text{ (See text)}$$

Let R3 = 470 Ω; then R4 ≅ 10 kΩ

The values of R_D and C_D are determined from the equations given in the text.

$$C_D = \frac{900 \times 10^{-6}}{2A_v E_{pp}} = \frac{900 \times 10^{-6}}{A_v E_p} = \frac{900 \times 10^{-6}}{4 \times 0.4 \times 2\pi \times 160 \times 10^3}$$

$$C_D \cong 560 \text{ pF}$$

Assume $f_C = 3f_H$

$$R_D = \frac{1}{\omega C C_D} - 40$$

$$= \frac{1}{2\pi \times 3 \times 320 \times 10^3 \times 5.6 \times 10^{-10}} - 40$$

$$R_D = 295 \text{ ohms} - 40 \cong 250 \ \Omega$$

$$L_D = \frac{R_T^2 C_D}{2} = \frac{(295)^2 \times 560 \times 10^{-12}}{2} = 24 \ \mu\text{H}$$

Example #3 (See Figure 24 for Component Hookup)

Same as Example #2, but consider base-line shift.

In addition to ac coupling between the Gain Stage and Threshold, a passive differentiation is performed to attenuate the lower frequencies producing base-line shift. This improves signal-to-noise ratio. The corner frequency is chosen at f_L = 160 kHz where the attenuation is 0.707 (−3 dB) and the phase angle is +45°.

$$f_L = \frac{1}{2\pi C (R1 + R2)} = 160 \times 10^3$$

For C = 200 pF

$$R1 + R2 \cong 5 \text{ k}\Omega$$

$$\text{Now } \frac{R1}{R1 + R2} = \frac{1}{1.6 \times 0.707} = 0.9$$

Let R1 = 4.7 kΩ, then R2 = 470 Ω

Example #4 (See Figure 31 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Dual Mode (Phase-Encoded/NRZI)
Recording Density: 1600 BPI (3200 FCPI) for PE mode and 800 BPI (800 FCPI) for NRZI mode
Tape Speed: 200 IPS
Signal Into Gain Stage

Same as Examples 1 and 2

Threshold: 25% of minimum voltage peaks

NOTE: Consider base-line shift for PE mode.

This tape drive performs either the NRZI or the PE functions of Examples #1 and #3, under control of the SEL A/B line. Using the Gain Stage and Threshold Amplifier Channel A, Channel B inputs, the hook-up for a single track is implemented as shown in Figure 31. Note that an electronic switch is required for Gain switching when the mode is changed. This particular design did not require the threshold voltage to be switched, although in a typical system it probably would be.

It is necessary to electronically switch differentiator components. A low impedance MOSFET switch is shown.

Example #5 (See Figure 24 for Component Hookup)

Tape Drive Type: Open Reel
Encoding: Group Code
Recording Density: 6250 BPI, 9042 FCPI
Tape Speed: 200 IPS
Signal Into Gain Stage

E_{pp} = 0.1 Vp-p @ 900 kHz = f_H

E_{pp} = 0.3 Vp-p @ 300 kHz = f_L

Considerations for setting Gain Stage EGC, coupling (passive differentiation for base-line shift or straight ac) into the Threshold Amplifier, and Threshold setting are similar to the previous examples. For Group-coded data the EGC setting can be electronically locked during the ID burst in conjunction with Threshold setting. (See Figure 32.)

Values for C_D and R_D

$$C_D = \frac{900 \times 10^{-6}}{2A_v E_p \omega}$$

$$= \frac{900 \times 10^{-6}}{A_v E_{pp} \omega} = \frac{900 \times 10^{-6}}{5.3 \times 0.3 \times 2\pi \times 300 \times 10^3}$$

$C_D \cong 300$ pF

Assume $f_C = 3f_H$

$$R_D = \frac{1}{\omega_C C_D} - 40 = \frac{1}{2\pi \times 3 \times 900 \times 10^3 \times 300 \times 10^{-12}} - 40$$

$R_D = 200 - 40 = 160$ Ohms

$$L_D = \frac{R_T^2 C_D}{2} = \frac{(200)^2 \times 300 \times 10^{-12}}{2} = 6\ \mu H$$

Example #6 (See Figure 24 for Component Hookup)

Same as Example #5 except 125 IPS tape speed.

Signal Into Gain Stage

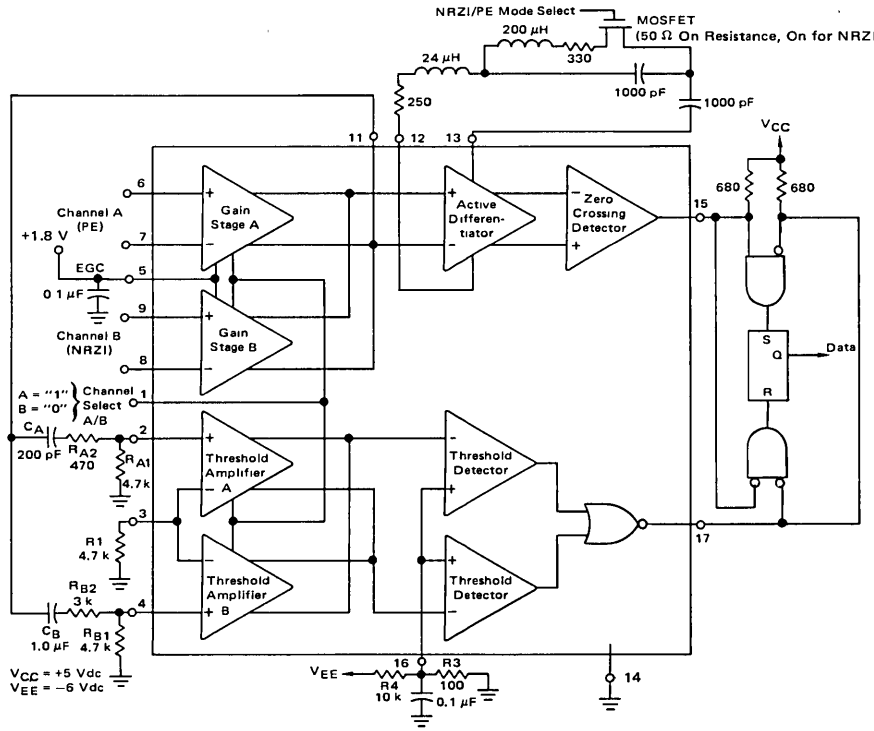
E_{pp} = 0.3 Vp-p @ 565 kHz

E_{pp} = 0.6 Vp-p @ 188 kHz

C_D = 300 pF, R_D = 250 Ω

L_D = 12.6 μH

FIGURE 31 – MC3468 COMPONENT HOOKUP FOR DUAL MODE PE/NRZI EXAMPLE #4



4

FIGURE 32 – APPLICATIONS CIRCUITS

Digital Attenuator for Setting MC3468 Gain Stage Automatically During ID Burst