AN3114
Application note

How to use the STM8AL3Lxx, STM8L152xx and STM8L162xx LCD controllers

Introduction

This application note describes techniques for connecting the LCD controller available in the medium density STM8AL3Lxx devices, medium density STM8L152xx devices, medium+ density STM8L152xx devices, and high density STM8L152xx/STM8L162xx devices, to liquid crystal displays (LCD), for driving alphanumeric characters and for converting ASCII characters to LCD segment control codes.

It explains how to select the LCD glass best suited for your application, and how to configure the LCD controller to take into account key parameters such as contrast, power consumption, number of used pixels, operating frequency range, and blinking.

A brief description of the LCD segment drive firmware embedded on the STM8L1526-EVAL and STM8L1528-EVAL evaluation boards is also provided.

For more information, please refer to the STM8L05xx, STM8L15xx, STM8L162x, STM8AL31xx and STM8AL3Lxx microcontroller family reference manual (RM0031).

Table 1. Applicable products

Product family	Part numbers
Microcontrollers	– STM8L152x4, STM8L152x6, STM8L152x8 – STM8L162R8, STM8L162M8 – STM8AL3L4x, STM8AL3L6x

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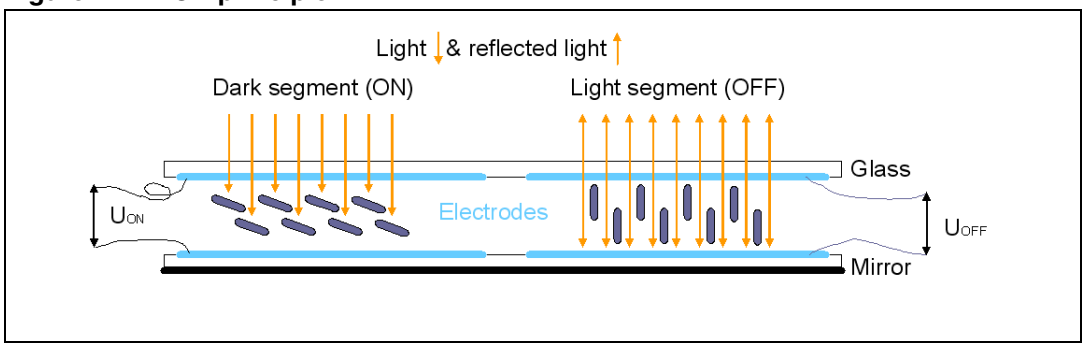
1 LCD solution

1.1 Definitions

- **LCD** (liquid crystal display): a passive display panel with terminals driving LCD segments.
- **LCD segment** (Pixel[i][j]): the smallest viewing element (a single bar or dot that is used to help create a character on an LCD display)
- **Segment line** (SEG[j]): segment terminal
- **Common** (COM[i]): electrical connection terminal connected to several LCD segments (denotes how many LCD segments (pixels) are connected to a segment line)
- **Duty ratio**: number defined as 1 / (number of common terminals on an LCD display)
- **Bias**: indicates the number of voltage levels used when driving an LCD. It is defined as 1 / (number of voltage levels used driving a LCD display - 1)
- **Von**: the RMS voltage applied to the LCD segment that creates an ON pixel which is typically at 90% of the contrast level
- **Vth (LCD threshold voltage):** the RMS voltage across an LCD pixel when contrast reaches a 10% level
- **Voff:** the RMS voltage across an LCD pixel when contrast reaches a 0% level
- **Frame**: one period of the waveforms written to a segment line
- **Frame rate**: the number of frames per second, that is, the number of times the LCD segments are energized per second
- **Boost circuit**: contrast controller circuit

1.2 LCD principle

Figure 1. LCD principle



An LCD panel is composed of many layers. A liquid crystal is filled between two of them (glass plates), that are separated by thin spacers coated with transparent electrodes which contain orientation layers.

The orientation layer usually consists of a polymer (e.g. polyimide) which has been unidirectionally rubbed using, for instance, a soft tissue. As a result, the liquid crystal molecules are fixed with their alignment more or less parallel to the plates, in the direction of rubbing. The crystal alignment directions at the surface of the two plates are perpendicular so that the molecules between the two plates undergo a homogeneous twist deformation in alignment to form a helix.

If no electric field is applied, the birefringent liquid crystal molecules keep their helical structure and rotate linearly polarized light waves passing through the plates. The transmitted light wave is then allowed through a crossed exit polarizer. As a result, the modulator has a bright appearance. On the other hand, if an AC voltage of a few volts is applied, the resulting electric field forces the liquid crystal molecules to align themselves along the field direction and the twist deformation (the helix) is unwound. In this case, the polarization of the incident light is not rotated by the crystal molecules and the crossed exit polarizer blocks the light wave. As a result, the modulator appears dark.

The inverse switching behavior can be obtained with parallel polarizers. It must also be noted that gray scale modulation is easily achieved by varying the voltage between the crystal molecule reorientation threshold (reorientation is resisted by the elastic properties of liquid crystals) and the saturation field.

LCDs are sensitive to root mean square voltage levels. With a low root mean square voltage applied to it, an LCD is practically transparent (the LCD segment is then inactive or off). To turn an LCD segment on, causing the LCD segment to turn dark (from light gray to opaque black), an LCD RMS voltage greater than the LCD threshold voltage V_{th} is applied to the LCD. The LCD RMS voltage is the RMS voltage across the capacitor C in *Figure 2*, which is equal to the potential difference between the SEG and COM values.

The LCD threshold voltage V_{th} depends on the quality of the liquid used in the LCD and the temperature. The optical contrast is defined by the difference in transparency of an LCD segment that is on (dark) and an LCD segment that is off (transparent). The optical contrast depends on the difference between the RMS voltage on an on LCD segment (V_{on}) and the RMS voltage on an off LCD segment (V_{off}). The higher the difference between $V_{on(RMS)}$ and $V_{off(RMS)}$, the higher the optical contrast. The optical contrast also depends on the level of V_{on} versus the LCD threshold voltage V_{th}. If V_{on} is lower or close to the threshold voltage V_{th}, the LCD is completely or almost transparent. If V_{off} is close or higher than the threshold voltage V_{th}, the LCD is completely black.

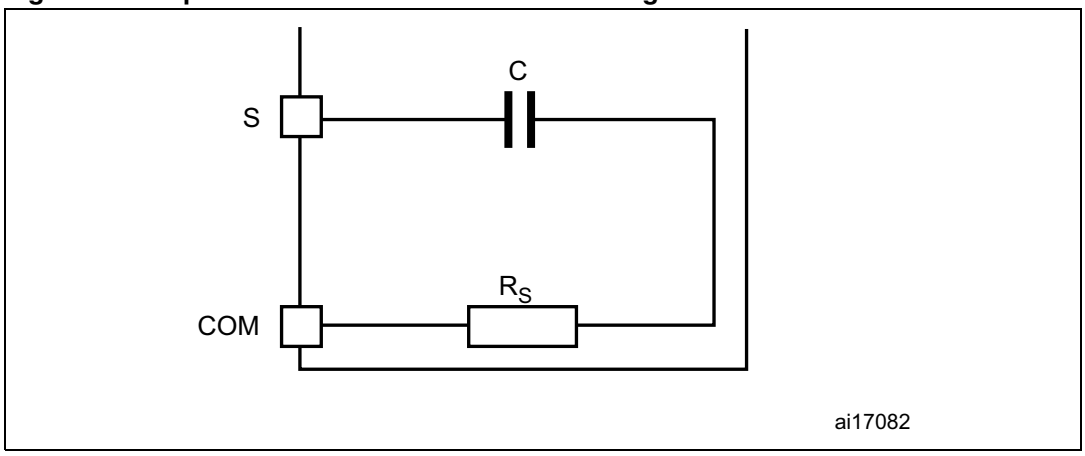
The discrimination ratio (D) specifies the contrast levels that the LCD panel can achieve. It is defined as follows:

$$D = V_{ON(RMS)} / V_{OFF(RMS)}$$

To prevent the electrolytic process (DC voltage applied on LCD or the temperature effect on the performance of the LCD panel...) from occurring and consequently ensure a longer LCD lifetime, the applied LCD voltage must also alternate to obtain a zero DC value.

Note: The DC value should never be higher than 100 mV (refer to the LCD manufacturer's datasheet), otherwise, the LCD lifetime may be shortened. The typical frequency ranges from 30 to 100 Hz. If a lower frequency is used, the LCD flickers. If a larger frequency is used, the power consumption increases.

Figure 2. Equivalent electrical schematic of a segment line



1.3 Selecting an LCD glass

To select the LCD glass best suited for your application among the wide range of products available on the market, the following criteria must be taken into account:

1. The information to display on the LCD glass. It is a combination of alphanumeric symbols and various useful predefined symbols such as digits, bells, low-battery symbol, arrows, antenna, and progress bar.
2. The typical electrooptical characteristics required for the LCD to operate: operating temperature, storage temperature, and operating voltage, which affect the LCD contrast.
3. The number of pixels required to achieve the desired display on the LCD.
4. When the multiplex of the LCD panel increases (quadruplex, octaplex...), the discrimination ratio and the contrast decrease (please refer to the discrimination ratio calculation for each backplane LCD). So, to provide a better contrast and a greater separation between Von(RMS) and Voff(RMS), the LCD voltages must be increased.

1.4 Typical applications

The LCD controller can be used in many embedded applications. They can be classified as follows:

1. **Home appliances**: refrigerator, microwave oven, coffee maker, washing machine, thermostat, battery management, security system, baby alarm, and clock radio, etc.
2. **Medical**: spirometer, glucose meter, pressure meter, temperature reader, nurse call system, medical pump, and pulse oximeter, etc.
3. **Automotive**: dashboard, audio system, tire pressure sensor, battery vehicle display, iPod adapter, etc.
4. **Industrial:** data acquisition, pressure meter, portable instruments, gasoline pumps, air conditioner, payment systems, gas detection, etc.

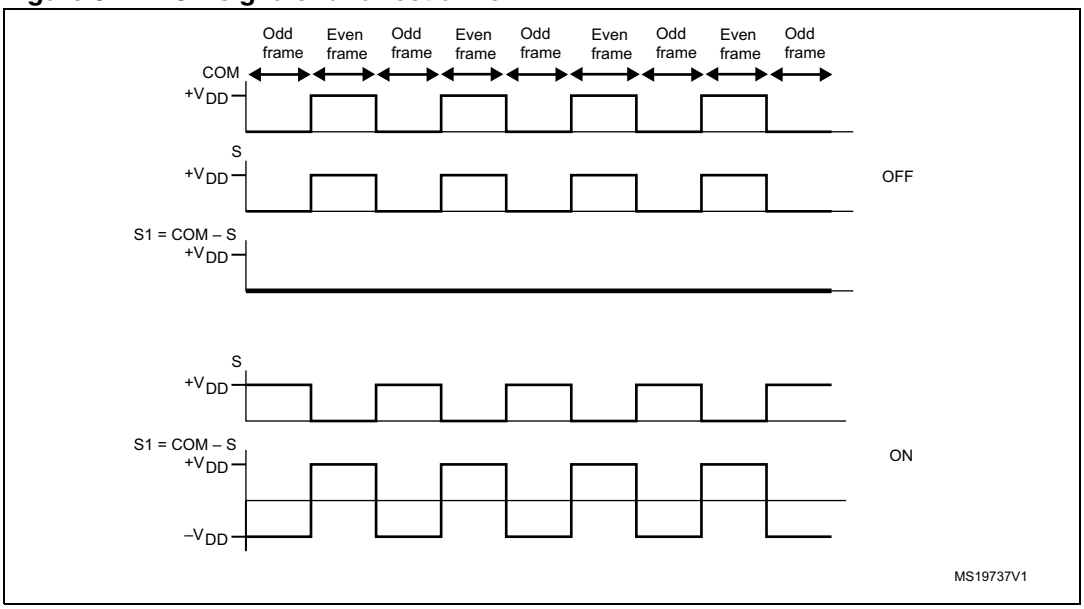
2 LCD controller drive signals

2.1 Single backplane LCD drive

In a single backplane drive, each LCD segment is connected to a segment line (Sx) and to a backplane (common line) common to all the segment lines. A display using S LCD segments is driven with S+1 MCU output lines (S segments + 1common). The backplane is driven with a COM signal between 0 and V_{DD} with a duty cycle of 50%.

When switching on an LCD segment, a signal with opposite polarity to COM is sent to the corresponding Segment line. When the non-inverted COM signal-to-segment signal is sent to the Segment line, the LCD segment is off. Using an MCU, the I/O operates in output mode at either logic 0 or 1.

Figure 3. LCD signals for direct drive



Discrimination ratio calculation for the single backplane LCD:

COM - S [ON] = (0-VDD) +(VDD-0) = 0 => VDC = 0

COM - S [OFF] = (0-0) + (0-0) = 0 => VDC = 0

$$V_{ON(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{(-VDD)^2 + (VDD)^2}{2}} = VDD$$

$$V_{OFF(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{(0)^2 + (0)^2}{2}} = 0$$

$$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}} = \frac{VDD}{0} = \infty$$

2.2 Duplex LCD drive

In a duplex drive, two backplanes are used instead of one. Each LCD segment line (Sx) is connected to two LCD segments, which other side is connected to one of the two backplanes or common lines (refer to *Figure 4*). Thus, only (S/2)+2 MCU pins are necessary to drive an LCD with S segments.

Three different voltage levels have to be generated on the backplanes: 0, VDD/2 and VDD. The Segment line voltage levels are 0 and VDD only. *Figure 5* shows typical backplane, segment lines and LCD waveforms. The intermediate voltage VDD/2 is only required for the backplane voltages. When one backplane is active (0 V during an odd frame and VDD during an even frame), the other is inactive (V_{DD}/2).

Figure 4. Basic segment lines connection in duplex mode

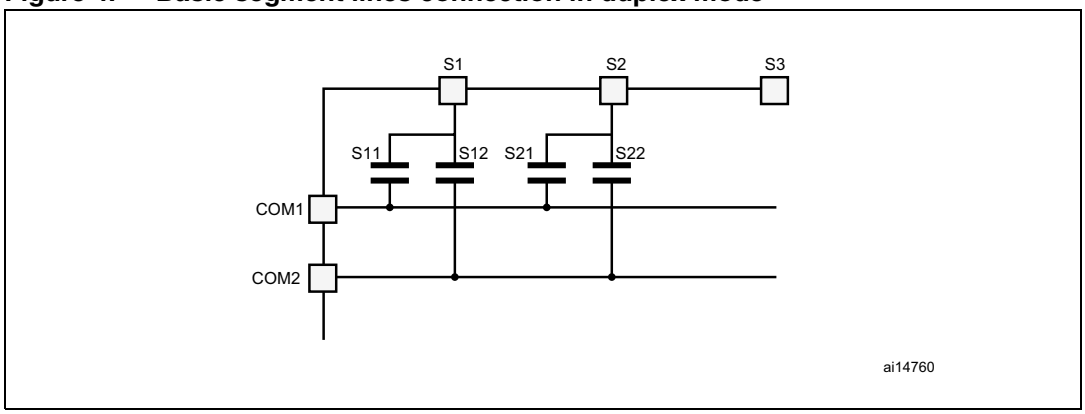
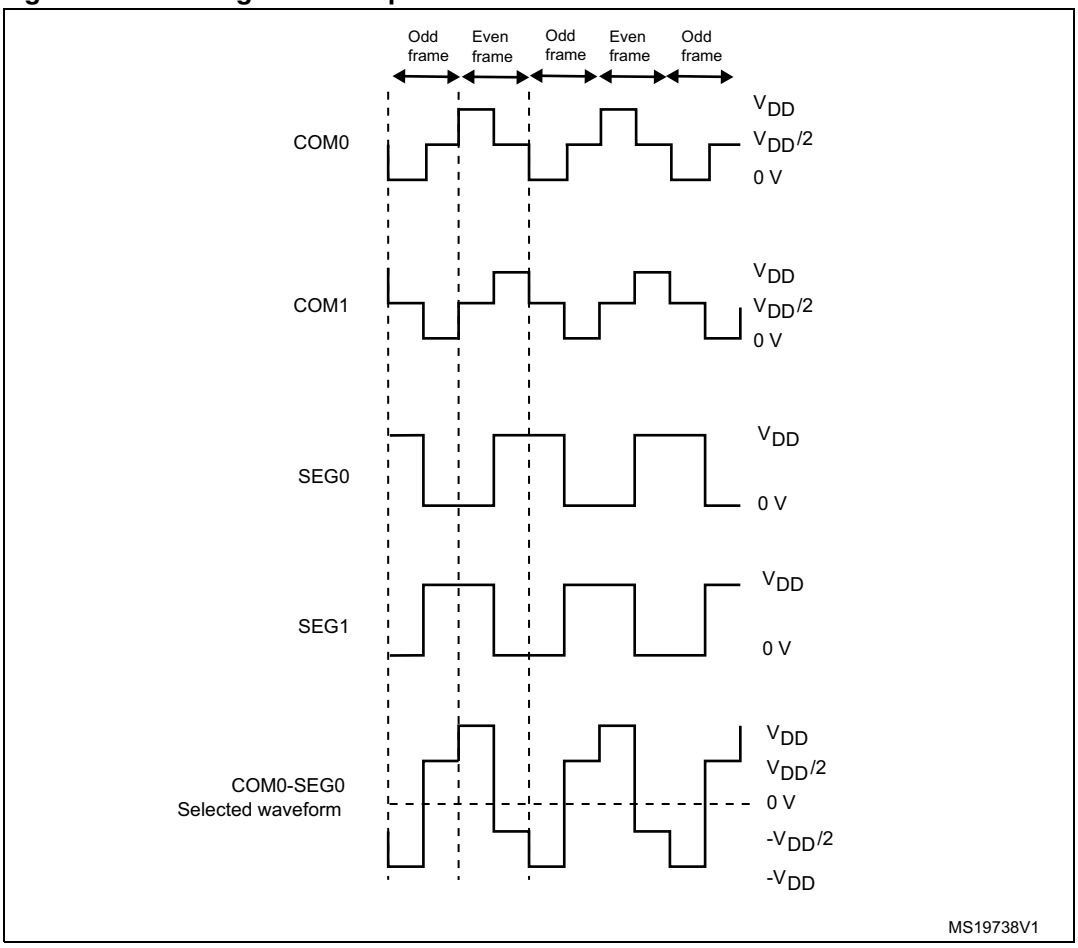


Figure 5. LCD signals for duplex mode



Discrimination ratio calculation for duplex mode:

COM0 - SEG0 [ON] = (0 - VDD) + (VDD/2 - VDD) + (VDD - 0) + (VDD/2 - 0) => VDC = 0

COM0 - SEG0 [OFF] = (0 - 0) - (VDD/2 - VDD) + (0 - 0) + (VDD/2 - 0) => VDC = 0

$$V_{ON(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{\left((VDD)^2 + \left(\frac{VDD}{2}\right)^2 + \left(\frac{-VDD}{2}\right)^2 + (-VDD)^2\right)}{4}} = 0{,}790VDD$$

$$V_{OFF(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{\left((0)^2 + \left(\frac{VDD}{2}\right)^2 + (0)^2 + \left(\frac{-VDD}{2}\right)^2\right)}{4}} = 0{,}353VDD$$

$$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}} = \frac{0{,}790VDD}{0{,}353VDD} = 2{,}237$$

2.3 Quadruplex LCD drive

In a quadruplex LCD drive, four backplanes are used. Each LCD pin is connected to four LCD segments, which other side is connected to one, two or four backplanes. Consequently, only (S/4)+4 MCU pins are necessary to drive an LCD with S LCD segments (pixels). For example, to drive an LCD with 112 LCD segments (28 ×4), only 32 I/O ports are required (28 I/O ports to drive the segment lines and 4 I/O ports to drive the backplanes).

Four different voltage levels have to be generated on the common lines: 0, $V_{DD}/3$, $2V_{DD}/3$ and V_{DD}. The Segment line voltage levels are also 0, $V_{DD}/3$, $2V_{DD}/3$ and V_{DD}. The LCD segment is inactive if the RMS voltage applied is below the LCD threshold voltage V_{th}, and is active if the LCD RMS voltage is above the threshold. *Figure 7.* shows typical backplane, Segment lines and LCD waveforms. The intermediate voltage $V_{DD}/3$ and $2V_{DD}/3$ are required for backplane voltages. When a backplane or COM is active (0 V during an odd frame and V_{DD} during an even frame), the others are made inactive by applying to them $2V_{DD}/3$ during an odd frame and $V_{DD}/3$ during an even frame.

Figure 6. Basic LCD segment lines connection in quadruplex mode

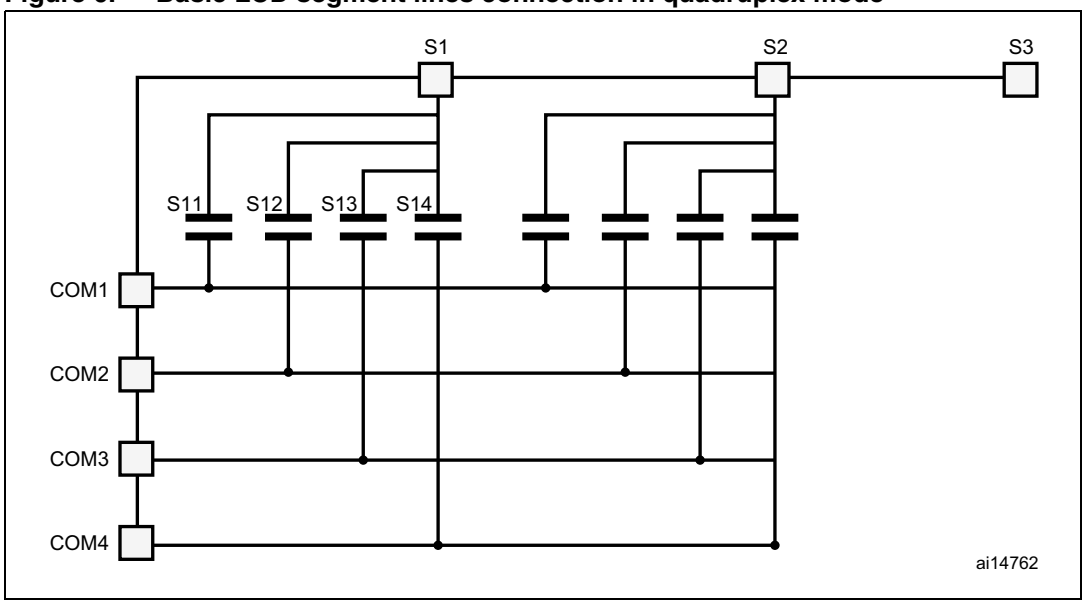
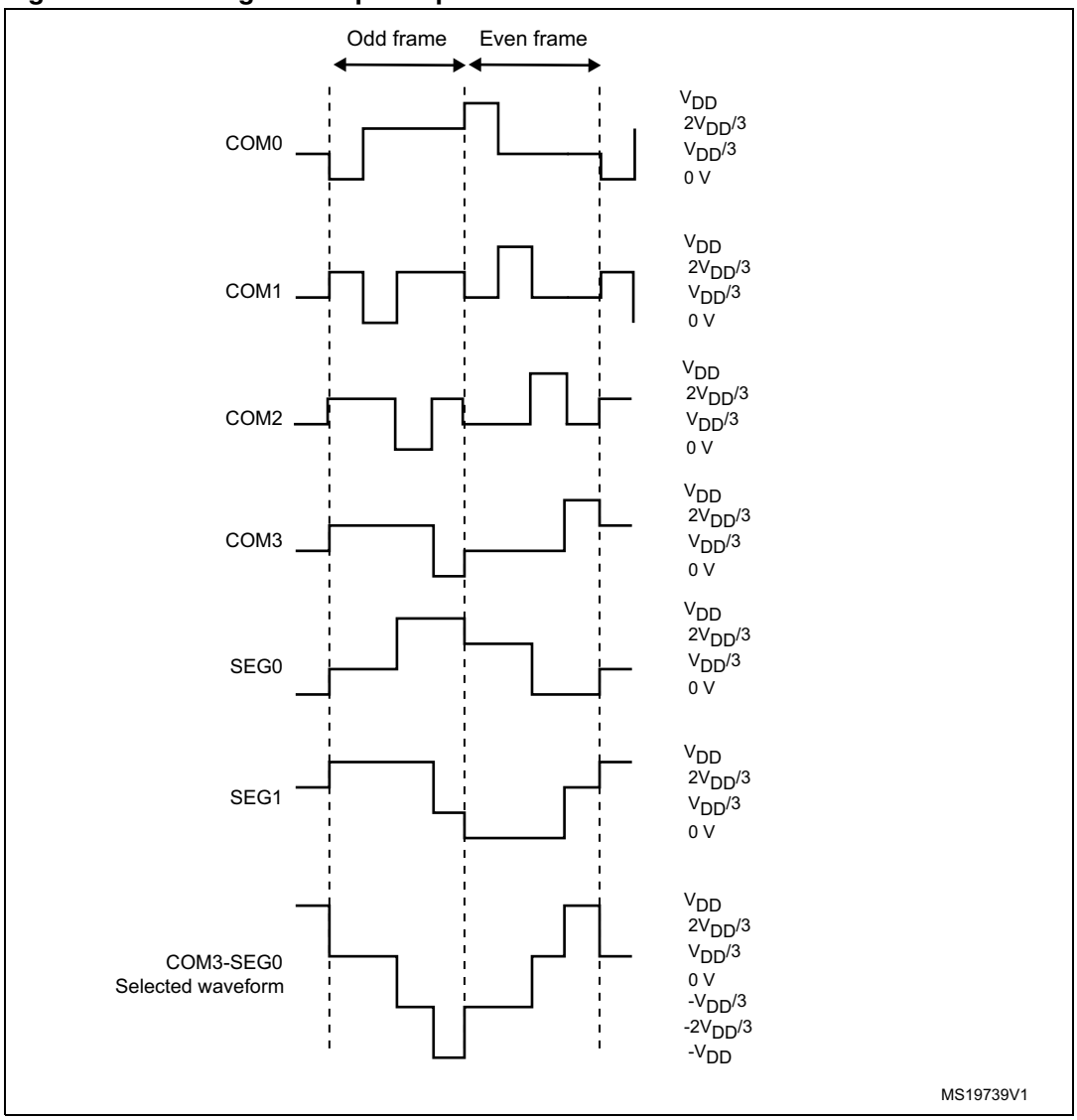


Figure 7. LCD signals in quadruplex mode



Discrimination ratio calculation for quadruplex mode:

COM3 - SEG0 [ON] = (2VDD/3 - VDD/3) + (2VDD/3 - VDD/3) + (2VDD/3 - VDD/3) + (0 - VDD) + (VDD/3 - 2VDD/3) + (VDD/3 - 2VDD/3) + (VDD/3 - 2VDD/3) + (VDD - 0) => VDC = 0

COM3 - SEG0 [OFF] = (2VDD/3 - VDD/3) + (2VDD/3 - VDD/3) + (2VDD/3 - VDD/3) + (0 - 0) + (VDD/3 - 2VDD/3) + (VDD/3 - 2VDD/3) + (VDD/3 - 2VDD/3) + (0 - 0) => VDC = 0

$$V_{ON(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{3\left(\frac{VDD}{3}\right)^2 + (VDD)^2 + 3\left(\frac{-VDD}{3}\right)^2 + (-VDD)^2}{8}} = 0{,}577VDD$$

$$V_{OFF(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{4\left(\frac{VDD}{3}\right)^2 + 4\left(\frac{-VDD}{3}\right)^2}{8}} = 0{,}333VDD$$

$$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}} = \frac{0{,}\dot{3}95}{0{,}176} = 1{,}732$$

2.4 Octaplex LCD drive

In an octaplex LCD drive, eight backplanes are used. Each segment line is connected to eight LCD segments, which other side is connected to one, two, four or eight of the eight backplanes. Consequently, only (S/8)+8 MCU pins are necessary to drive an LCD with S LCD segments. This mode is available only in medium+ and high density STM8L152xx/STM8L162xx devices. For example, to drive an LCD with 320 LCD segments (40 ×8), only 48 I/O ports are required (40 I/O ports to drive the segment lines and 8 I/O ports to drive the backplanes).

Five different voltage levels have to be generated on the common lines: 0, $V_{DD}/4$, $V_{DD}/2$, $3V_{DD}/4$ and V_{DD}. The Segment line voltage levels are also 0, $V_{DD}/4$, $V_{DD}/2$, $3V_{DD}/4$ and V_{DD}. The LCD segment is inactive if the RMS voltage is below the LCD threshold voltage V_{th}, and is active if the LCD RMS voltage applied is above the threshold. *Figure 9* shows typical backplane, Segment lines and LCD waveforms. The intermediate voltages $V_{DD}/4$, and $3V_{DD}/4$ are required for backplane voltages. When a backplane or COM is active (0 V during an odd frame and V_{DD} during an even frame), the others are made inactive by applying to them $3V_{DD}/4$ during an odd frame and $V_{DD}/4$ during an even frame.

Figure 8. Basic LCD segment lines connection in octaplex mode

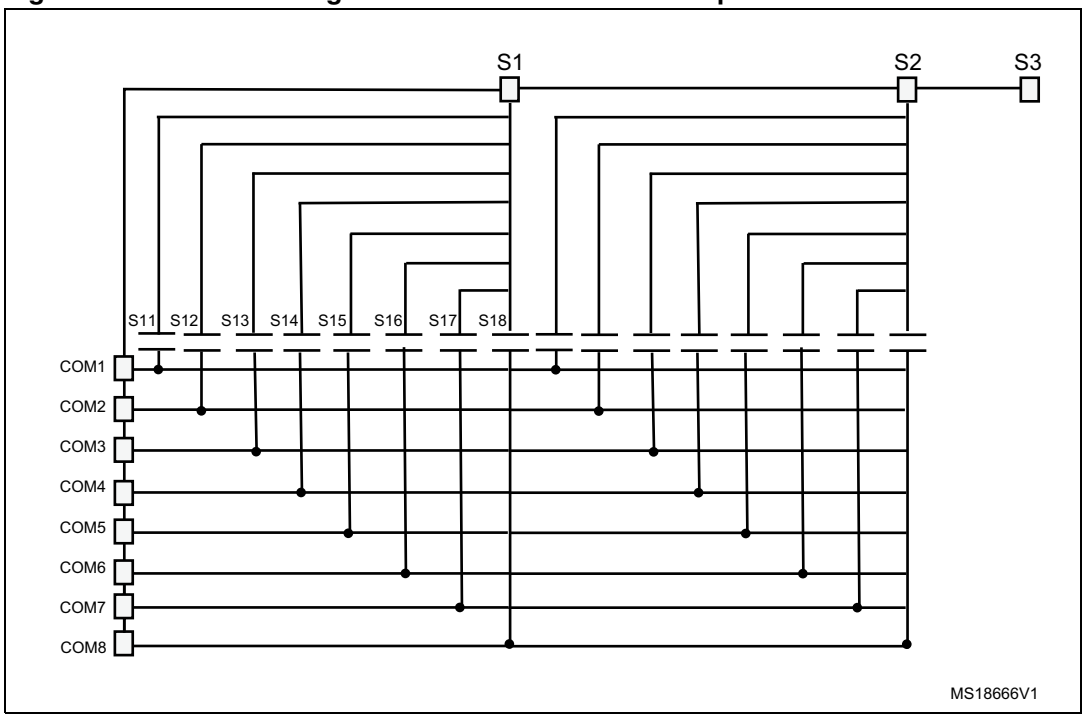
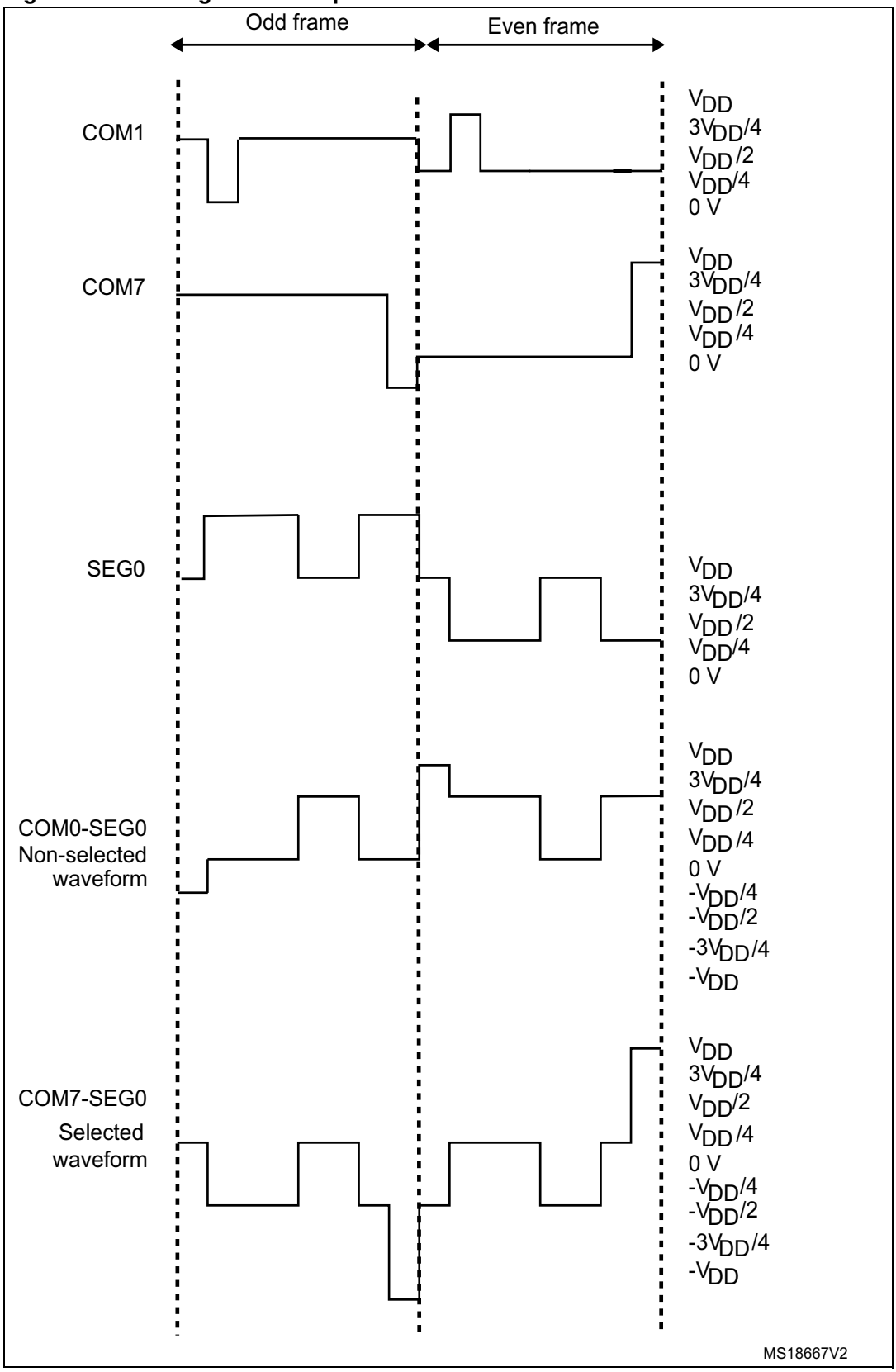


Figure 9. LCD signals in octaplex mode



Discrimination ratio calculation for octaplex mode:

COM0 - SEG0 [ON] = (0 -VDD) + 3 (3VDD/4-VDD) + 2 (3VDD/4 - VDD/2) + 2 (3VDD/4 - VDD) + (VDD - 0) + 3 (VDD/4 - 0) + 2 (VDD/4 - VDD/2) + 2 (VDD/4 - 0) => VDC = 0

COM0 - SEG0 [OFF] = 4 (3VDD/4-VDD) + 2 (3VDD/4 - VDD/2) + 2 (3VDD/4 - VDD) + 4 (VDD/4 - 0) + 2 (VDD/4 - VDD/2) + 2 (VDD/4 - 0) => VDC = 0

$$V_{ON(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{7\left(\frac{VDD}{4}\right)^2 + (VDD)^2 + 7\left(\frac{-VDD}{4}\right)^2 + (-VDD)^2}{16}} = 0{,}423VDD$$

$$V_{OFF(RMS)} = \sqrt{\frac{\sum_{n} V(Si)^2}{n}} = \sqrt{\frac{8\left(\frac{VDD}{4}\right)^2 + 8\left(\frac{-VDD}{4}\right)^2}{16}} = 0{,}25VDD$$

$$D = \frac{V_{ON(RMS)}}{V_{OFF(RMS)}} = \frac{0{,}423VDD}{0{,}25VDD} = 1{,}692$$

3 Integrated LCD controller

3.1 Benefits of integrated LCD controllers

The medium density STM8AL3Lxx devices, medium density STM8L152xx devices, medium+ density STM8L152xx devices, and high density STM8L152xx/STM8L162xx integrate an LCD control module that offers various advantages, including its overall design optimized to achieve an immediate reduction in component count and board space saving, and thus reducing the total system cost and power consumption.

The LCD controller is composed of three main blocks (see *Figure 10: Medium density LCD controller block diagram* and *Figure 11: Medium+ and high density LCD controller block diagram*):

- The frequency generator
- The common/segments driver
- The contrast controller

Figure 10. Medium density LCD controller block diagram

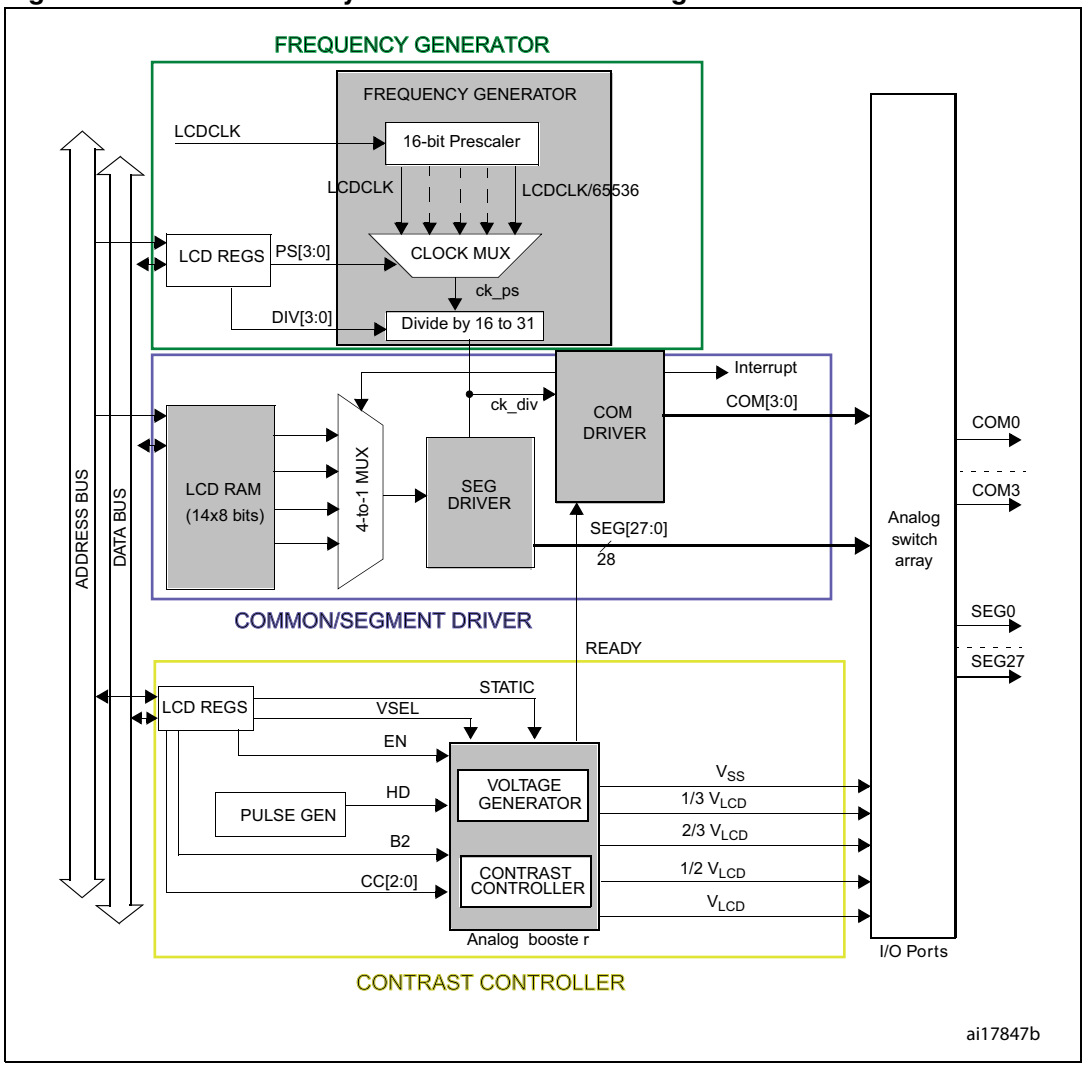
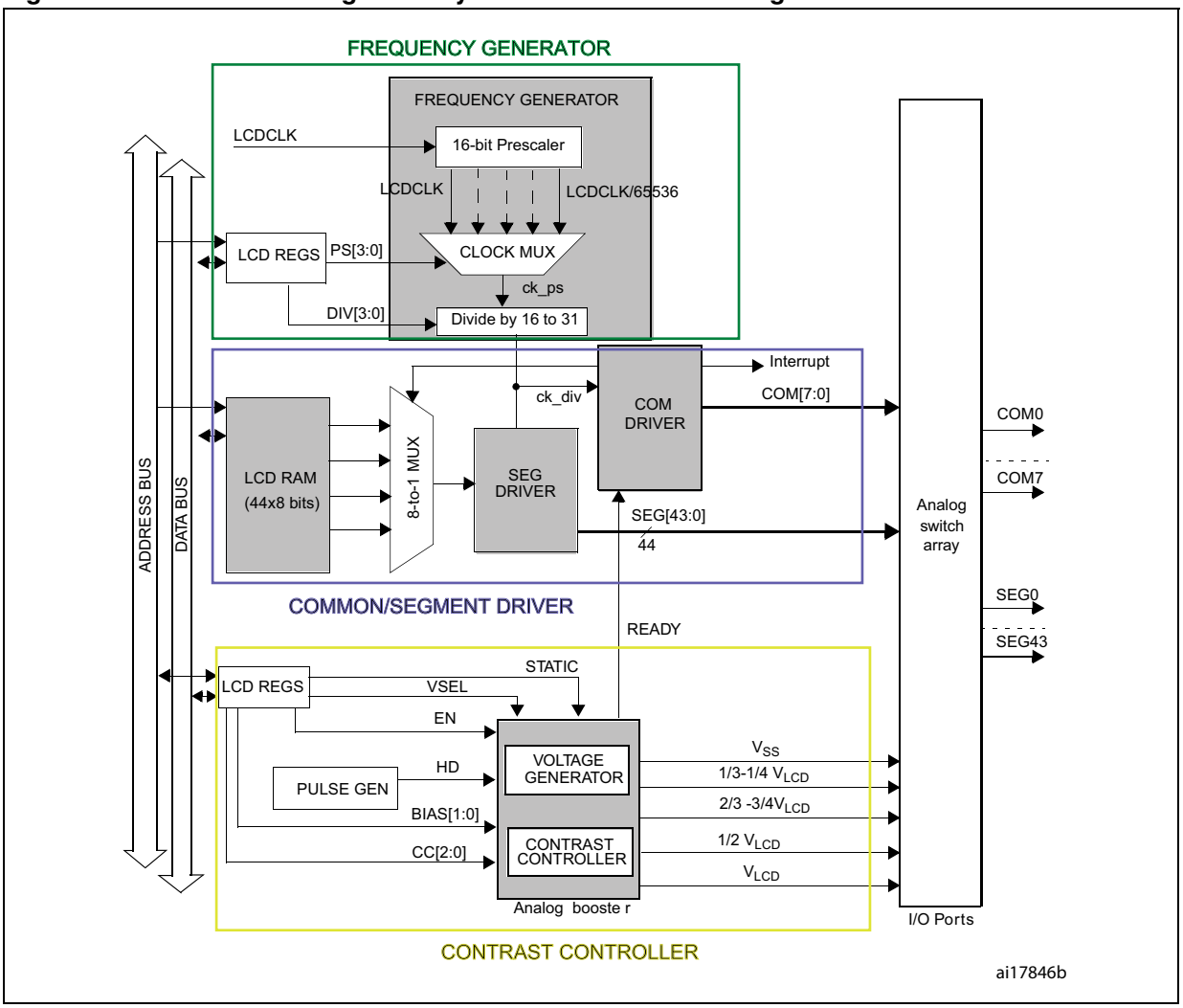


Figure 11. Medium+ and high density LCD controller block diagram



3.1.1 Frequency generator block

The first block of the LCD controller is the frequency generator. It consists of a 16-bit ripple counter prescaler and a programmable clock divider with a divider factor ranging from 16 to 31. It generates the LCD frequency, ck_div, starting from the input clock frequency, f_{LCDCLK}. The 16-bit prescaler divides f_{LCDCLK} by 1 up to 65536. The value can be configured through the PS[3:0] bits in the LCD_FRQ register. If a finer resolution rate is required, a second divider can be used to further divide fck_ps by a factor of 16 to 31. This second factor is configured through the DIV[3:0] bits in the LCD_FRQ register. fck_div is given by the following equation:

$$f_{ck\_div} = \frac{f_{CLKLCD}}{2^{PS} \times (16 + DIV)}$$

f_{frame} is the operating frequency. It should be evaluated by taking into account the operating frequency of the LCD device used in application. This range is typically from 30 to 100 Hz. It is a compromise between power consumption and an acceptable refresh rate.

To generate f_{frame} in the LCD operating frequency range using the prescaler and the divider, the LCDCLK input clock must be in the range of 16.384 KHz to 500 KHz. For more details, refer to section *Clock control* of the reference manual (RM0031). $f_{frame}$is given by the following equation:

$$f_{frame} = f_{ck\_div} \times duty$$

where the duty can be static, 1/2, 1/3, 1/4 or 1/8.

3.1.2 Common/segments drive block

The second block of the LCD controller is the common/segments drive. It contains the timing circuitry which allows to generate the appropriate waveforms to drive the common and the segments lines. Refer to the reference manual RM0031 (section 17.3.3 *Common driver*) for additional details.

This block also contains the LCD_RAM registers which bits correspond to the individual pixels to be displayed on the LCD device.

In addition to the common/segments drive block features, a blink prescaler allows to select the blink frequency. This frequency is defined by setting the BLINKF[2:0] bits of the LCD_CR1 register from 0 to 7. Refer to the reference manual RM0031 (section 17.3.2 *Frequency generator*) for additional details.

3.1.3 LCD contrast controller block

The last block is the contrast controller. It plays a key role in the LCD controller since it allows to adjust the contrast to the optimal value depending on the trade-off between the power consumption and a satisfactory contrast level for the application.

The contrast depends on the V_{LCD} voltage level which either internally generated by the booster or externally provided on the Vlcd pin.

External V_{LCD} voltage source

The external V_{LCD} voltage source is selected by setting the V_{SEL} bit to ‘1’ in the LCD_CR2 register. When the external source is used to generate V_{LCD}, the contrast is controlled by varying the dead time (up to seven phase periods) between each couple of frames where the COM and SEG values are low simultaneously.

Internal V_{LCD} voltage source

The internal booster is selected by clearing the V_{SEL} bit in LCD_CR2. In this case, the contrast is controlled by adjusting V_{LCD} by software. In medium density STM8L152xx, and STM8AL3Lxx devices, the adjustment is from 2.6 to 3.3 V. In medium+ and high density STM8L152xx and STM8L162xx devices, the eight-step adjustment is from 2.6 to 3.5 V. Please refer to the product datasheets.

Generation of the LCD voltage levels

The internal booster includes two resistive networks, one with low value resistors (R_L) and one with high value resistor (R_H) which are respectively used to increase the current during transitions and to reduce consumption in static state (see *Figure 12*).

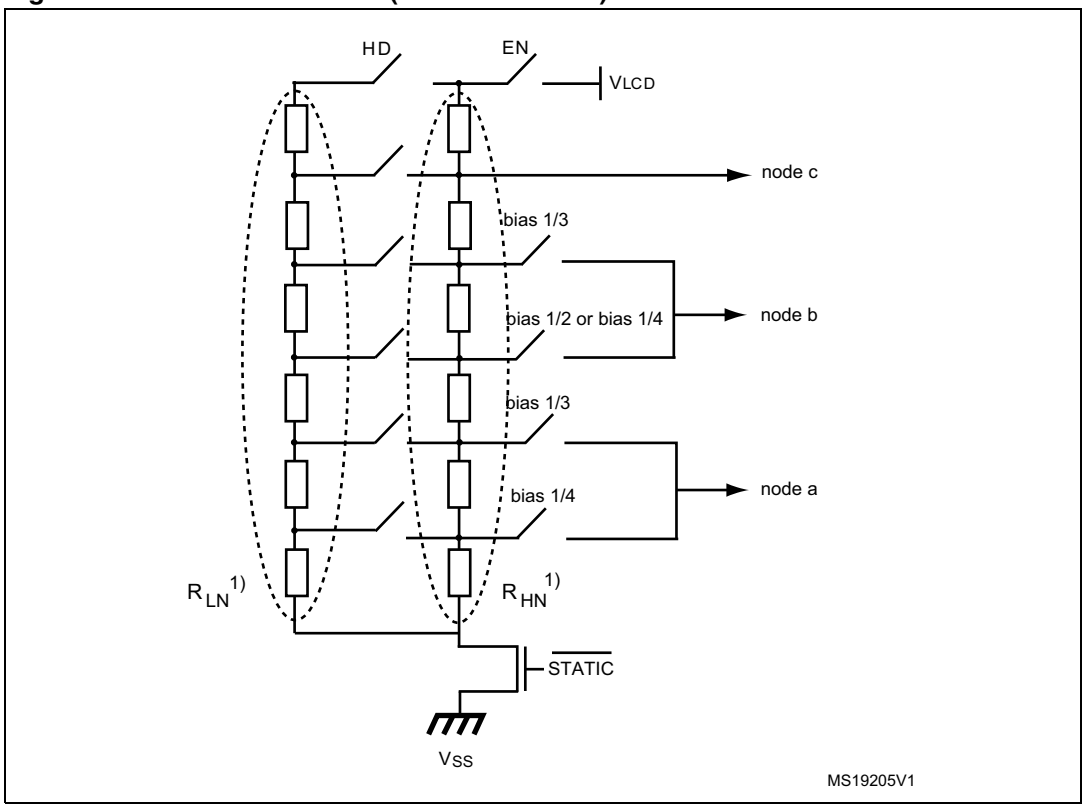
- The EN switch follows the rules below:
  - When the LCDEN bit in the LCD_CR3 register is set, the EN switch is closed.
  - When clearing the LCDEN bit in the LCD_CR3, the EN switch is open at the end of the even frame in order to avoid a medium voltage level different from 0 during the frame.

The PON[2:0] (Pulse ON duration) bits in the LCD_CR2 register configure the time during which R_L is enabled (see *Figure 10* and *Figure 11*) through a HD (high drive) when the levels of common and segment lines change. A short drive time decreases power consumption, but displays with high internal resistance may need a longer drive time to achieve a satisfactory contrast.

The R_L divider can be always switched on using the HD bit in the LCD_CR2 register.

- The R_L divider is enabled when the HD signal is set only for a short period of time when the levels of common and segment lines change. This time can be programmed through the Pulse ON bits (PON[2:0]) of the LCD_CR2 register. The HD signal follows the rules described below:
  - If the HD bit and the PON[2:0] bits in the LCD_CR2 are reset, then the HD signal is open.
  - If the HD bit in the LCD_CR2 register is reset and the PON[2:0] bits in the LCD_CR2 are different from 00, then the HD signal is closed during the number of pulses defined in the PON[2:0] bits.
  - If the HD bit in the LCD_CR2 register is 1, then the HD signal is always closed.

Figure 12. Resistive network (internal booster)



- In case of 1/2 bias, one voltage level (1/2 V_{LCD}) is generated and node b voltage is 1/2 V_{LCD}.
- In case of 1/3 bias, two intermediate voltage levels (1/3 V_{LCD}, 2/3 V_{LCD}) are generated:
  - node a is 1/3 V_{LCD}
  - node b is 2/3 V_{LCD}
- In case of 1/4 bias (medium+ and high density STM8L152xx and STM8L162xx devices only), three intermediate voltage levels (1/4 V_{LCD}, 1/2 V_{LCD} and 3/4 V_{LCD}) are generated:
  - node a is 1/4 V_{LCD}
  - node b is 1/2 V_{LCD}
  - node c is 3/4 V_{LCD}.

3.2 Optimizing power consumption

When the LCD controller operates in run mode, decreasing the power consumption results in a lower contrast. As a consequence, the contrast adjustment methods described in *Section 3.1.3* can also be used to adjust the power consumption.

When the internal booster is used, the power consumption can be reduced by minimizing the period of time during which the R_L divider is enabled (drive time). However, the drive time to achieve a satisfactory contrast may be longer with a high internal resistance.

However, the STM8AL3Lxx, STM8L152xx, and STM8L162xx microcontrollers allow the LCD controller to operate in all low power modes except for Halt mode.

4 Displaying alphanumeric characters on the LCD glass

This section explains how to connect the LCD controller to an LCD glass to display alphanumeric characters. It is based on the following examples:

- STM8L1526-EVAL evaluation board using Pacific Display devices PD-878 and medium density STM8L152xx microcontroller
- STM8L1528-EVAL evaluation board using the custom LCD HXO5002B and high density STM8L152xx/STM8L162xx microcontroller

4.1 PD-878 LCD glass used on STM8L1526-EVAL

The PD-878 LCD glass mounted on the STM8L1526-EVAL is an eight multiplexed digit display from Pacific Display devices, the PD-878 (see *Figure 13*).

Depending on the type of LCD glass which is used, the user can select the LCD mode by configuring the duty cycle. Each segment line can control up to four pixels. The integrated LCD controller available in medium density STM8L152xx/STM8AL3Lxx devices can control up to 112 LCD segments that can be divided between alphanumeric symbols and several predefined symbols including digit, bell, low-battery symbol, arrows (left, up, right, and down), antenna, and progress bar. Since the LCD glass has in total 128 LCD segments (only alphanumeric characters) controlled through four COM and 32 segment lines, some of the segment lines of the LCD glass are not connected in the standard configuration (see *Figure 14*).

Alphanumeric characters are displayed using 16 LCD segments. *Figure 15* shows the LCD segments and reference letters for an alphanumeric character.

Figure 13. Layout for the PD-878

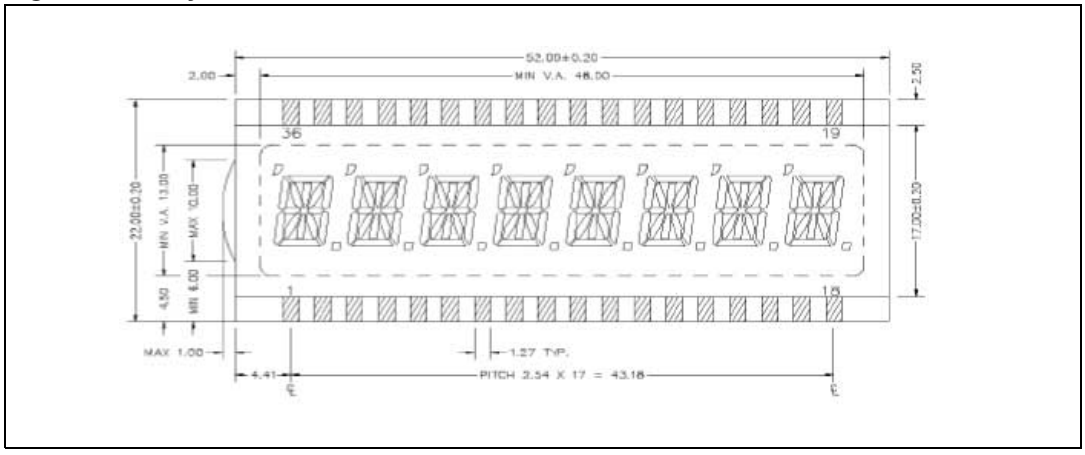
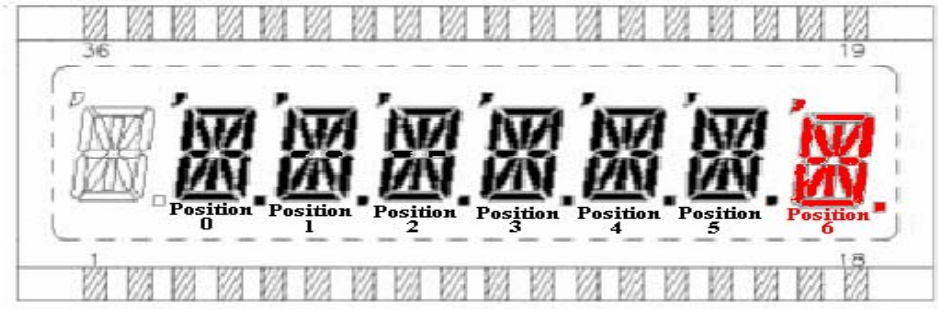
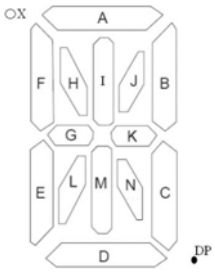


Figure 14. LCD segments used on the STM8L1526-EVAL



Note: Only the black alphanumeric characters are used by this application note firmware to display the time. The red alphanumeric (position 6) is connected on the evaluation board STM8L1526-EVAL but not used, and the white alphanumeric is not connected.

Figure 15. Reference letters for an alphanumeric character on the PD-878



4.2 Custom LCD glass HXO5002B used on STM8L1528-EVAL

The custom LCD glass HXO5002B mounted on the STM8L1528-EVAL is designed specially for the LCD controller available in medium+ density STM8L152xx devices, high density STM8L152xx/STM8L162xx devices. It is a combination of alphanumeric symbols and various useful predefined symbols such as dot matrix, low-battery symbol, arrows (left, up, right, and down), ST logo... *Figure 16* shows the layout for the custom LCD HXO5002B.

The operating LCD mode is 1/8 duty and 1/4 bias. Each segment line can control up to eight pixels. The integrated LCD controller can control up to 320 LCD segments that can be divided between alphanumeric symbols (7 x 16 pixels), dot matrix (10 x 19 pixels), low-battery symbol (4 pixels), arrows (4 pixels), antenna (6 pixels), ST logo (1 pixel) and 3 pixels for mA, µa and nA signs. In total, 320 LCD segments are controlled through eight COM and 40 segment lines. Each segment line of the LCD glass is connected in the standard configuration. *Figure 17* shows the reference segment lines for the custom LCD HXO5002B.

Figure 16. Layout for the custom LCD HXO5002B

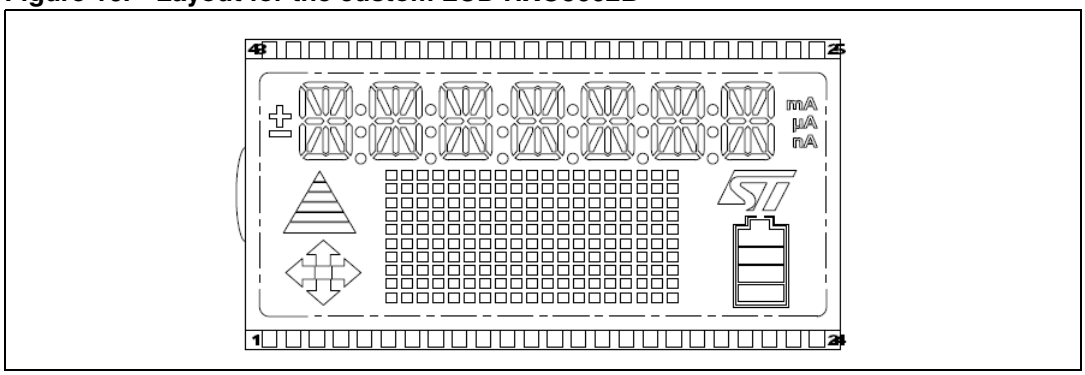
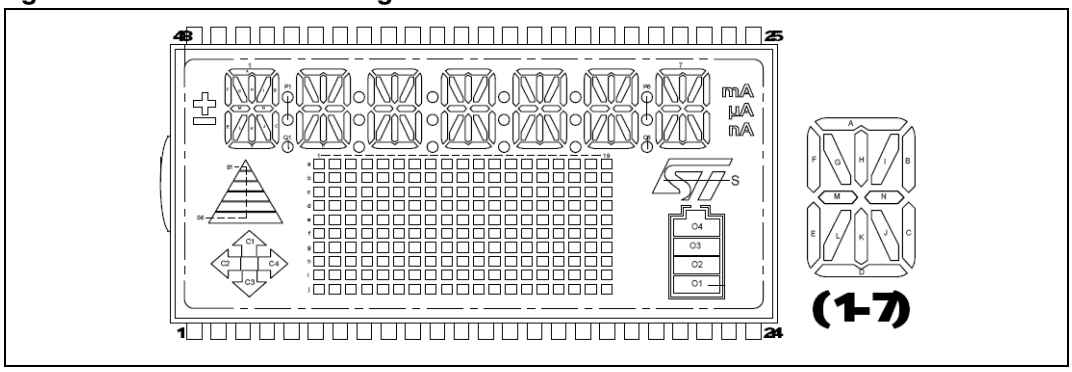


Figure 17. Reference LCD segments for the custom LCD HXO5002B



4.3 Connecting the LCD glass PD-878 to the LCD controller available in medium density STM8L152xx/STM8AL3Lxx/ devices

To display an alphanumeric character on the LCD glass display PD-878 available on STM8L1526-EVAL, four common lines (COM) and four segment lines (SEG) are required. *Table 2* shows the correspondence between each LCD segment and the reference letter on the LCD glass.

Table 2. Reference letter for an alphanumeric character on LCD

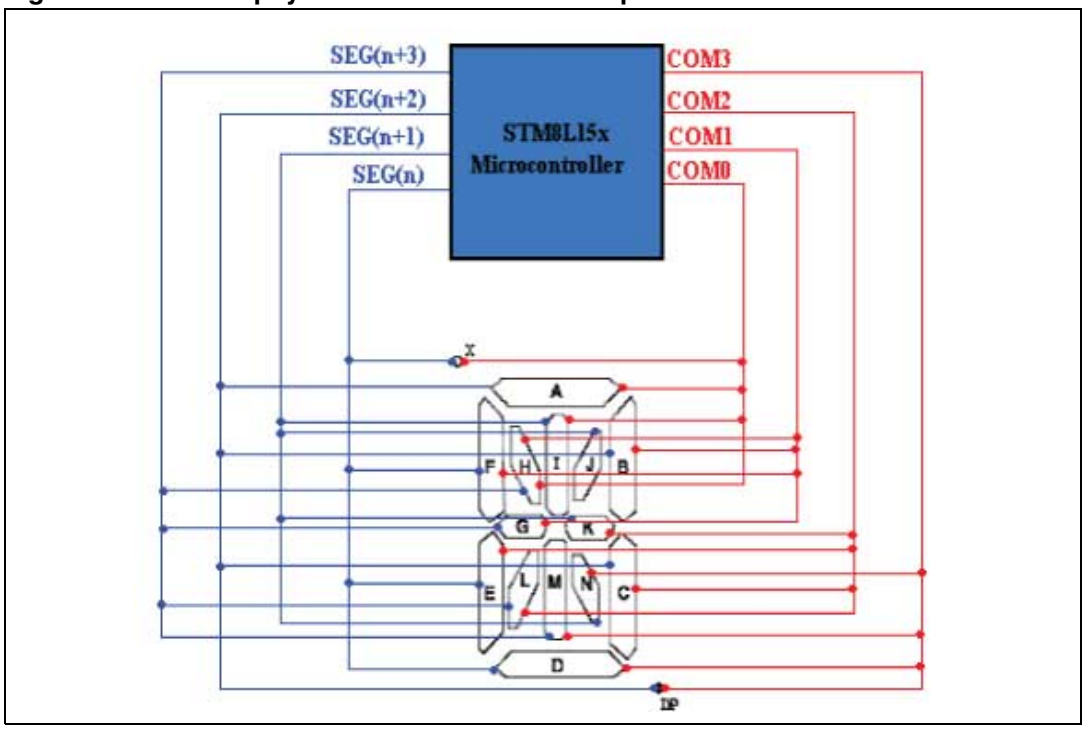
Couple (COM/SEG)	LCD segment in LCD RAM	Reference letter for an alphanumeric character
COM0/SEG(n)	LCD segment(n)	X
COM0/SEG(n+1)	LCD segment(n+1)	I
COM0/SEG(n+2)	LCD segment(n+2)	A
COM0/SEG(n+3)	LCD segment(n+3)	H
COM1/SEG(n)	LCD segment(n+28)	F
COM1/SEG(n+1)	LCD segment(n+1+28)	J
COM1/SEG(n+2)	LCD segment(n+2+28)	B
COM1/SEG(n+3)	LCD segment(n+3+28)	G
COM2/SEG(n)	LCD segment(n+56)	E
COM2/SEG(n+1)	LCD segment(n+1+56)	K
COM2/SEG(n+2)	LCD segment(n+2+56)	C
COM2/SEG(n+3)	LCD segment(n+3+57)	L
COM3/SEG(n)	LCD segment(n+84)	D
COM3/SEG(n+1)	LCD segment(n+1+84)	N
COM3/SEG(n+2)	LCD segment(n+2+84)	DP
COM3/SEG(n+3)	LCD segment(n+3+84)	M

Note: "n" values can be (0, 4, 8, 12, 16, 20, 24) respectively for alphanumeric character position (6, 5, 4, 3, 2, 1 and 0).

The LCD segments are individually controlled by setting or clearing the corresponding bit of the LCD data registers (LCD_RAM[13:0]). The LCD controller module handles the encoding of the physical drive waveforms to the LCD glass.

The physical connections between each of the 16 segment digits, the segment lines and the common lines must be performed as shown in *Figure 18*.

Figure 18. PD-878 physical connection for an alphanumeric character



To be able to make an efficient LCD software driver and optimize LCD alphanumeric character coding in terms of code density, the matrix shown in *Figure 19* has been chosen.

Figure 19. PD-878 segment driver matrix

```
                COM0     COM1     COM2     COM3
SEG(n)     { X ,      F ,      E ,      D  }
SEG(n+1)   { I ,      J ,      K ,      N  }
SEG(n+2)   { A ,      B ,      C ,      DP }
SEG(n+3)   { H ,      G ,      L ,      M  }

n ={0,4,8,12,16,20,24}
```

Each matrix M element corresponds to one bit on the LCD_RAM[13:0] registers. To enable SEG(i) connected to COM(j), the “M[i][j]” element must be set to 1 and to disable it the “M[i][j]” element must be set to 0.

The following structure provided in the LCD firmware allows to translate alphanumeric characters from ASCII to LCD_RAM[13:0] registers:

```
bit[15:0] = Nibble[3:0] = {LCD_RAM[13:10], LCD_RAM[10:7],
LCD_RAM[6:3], LCD_RAM[3:0]};
```

Bit[15:0] are the 16 matrix terms arranged so that each nibble is related to one or several LCD_RAM registers. The relation between the nibbles and the LCD_RAM registers is conditioned by the LCD digit which is accessed. *Table 3* summarizes the correspondence between LCD_RAM register bits (nibble) and LCD character.

Table 3. LCD_RAM bits versus LCD PD-878 characters

LCD RAM	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LCD_RAM0	Character1				Character0			
LCD_RAM1	Character3				Character2			
LCD_RAM2	Character5				Character4			
LCD_RAM3	Character0				Character6			
LCD_RAM4	Character2				Character1			
LCD_RAM5	Character4				Character3			
LCD_RAM6	Character6				Character5			
LCD_RAM7	Character1				Character0			
LCD_RAM8	Character3				Character2			
LCD_RAM9	Character5				Character4			
LCD_RAM10	Character0				Character6			
LCD_RAM11	Character2				Character1			
LCD_RAM12	Character4				Character3			
LCD_RAM13	Character6				Character5			

Displaying a “W” on the LCD glass

The LCD segments B, C, E, F, L, and N must be activated to display the “W” letter (see *Figure 20*). These segments must then be transferred from the LCD_RAM registers to the LCD glass. Use the matrix described in *Figure 19* to know which bits of the LCD_RAM registers must be set.

The firmware structure provides the value 0x05D2 for Nibble[3:0], corresponding to:

- Nibble[0] = 0x0 = 0000b
- Nibble[1] = 0x5 = 0101b
- Nibble[2] = 0xD = 1101b
- Nibble[3] = 0x2h = 0010b.

To display ‘W’ on position three on the LCD glass, the LCD_RAM registers must be programmed as follows:

- Nibble[0] in the MSB bits for LCD_RAM1 register
- Nibble[1] in the LSB bits for the LCD_RAM5 register
- Nibble[2] in the MSB bits for the LCD_RAM8 register
- Nibble[3] in the LSB bits for the LCD_RAM12 register

Note: All upper case letters and number are converted from ASCII characters to LCD_RAM registers format. The LCD letters and numbers map are stored in two Flash tables (LetterMap and NumberMap) as constants which are used when translating the ASCII characters to LCD RAM registers.

Figure 20. Letter “W” displayed on the PD-878

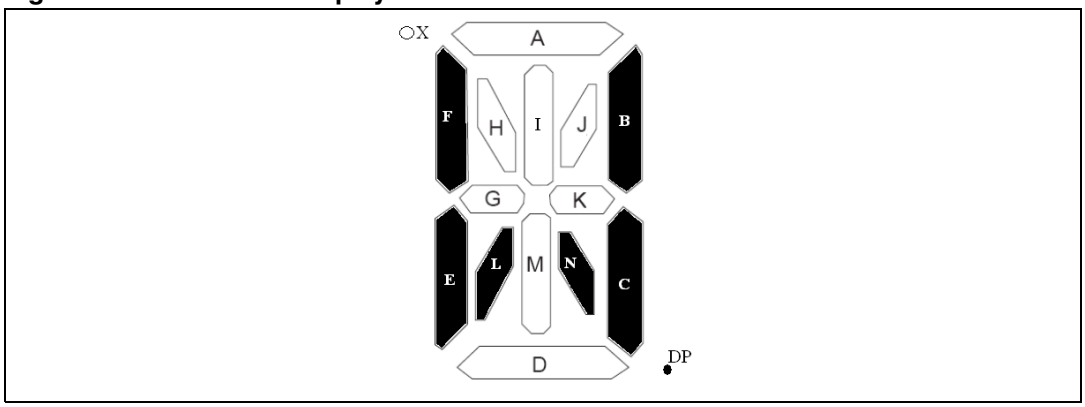


Figure 21. Displaying “W” on the matrix for the PD-878

```
          COM0    COM1    COM2    COM3
SEG(n)    { 0 ,     1 ,     1 ,     0 }
SEG(n+1)  { 0 ,     0 ,     0 ,     1 }
SEG(n+2)  { 0 ,     1 ,     1 ,     0 }
SEG(n+3)  { 0 ,     0 ,     1 ,     0 }

        Ox  0       5       D       2
```

4.4 Connecting the custom LCD glass HXO5002B to the LCD controller available in medium+ density STM8L152xx and high density STM8L152xx/STM8L162xx devices

To display an alphanumeric character on the custom LCD glass display HXO5002B available in medium+ density STM8L152xx and high density STM8L152xx/STM8L162xx devices, six common lines (COM) and three segment lines (SEG) are required. The selected COM from the eight available COM in medium+ and high density STM8L152xx/STM8L162xx devices used on the STM8L1528-EVAL are COM0, COM1, COM4, COM5, COM6 and COM7. *Table 4* shows the correspondence between the LCD controller available in medium+ density STM8L152xx and high density STM8L152xx/STM8L162xx device segment lines, the LCD segment in the LCD RAM and the reference letter for each alphanumeric character on the LCD glass.

Table 4. Reference letter for an alphanumeric character on custom LCD HXO5002B

Couple (COM/SEG)	LCD segment in LCD RAM	Reference letter for an alphanumeric character
COM0/SEG(n)	LCD segment(n)	-
COM0/SEG(n+1)	LCD segment(n+1)	D
COM0/SEG(n+2)	LCD segment(n+2)	Q
COM1/SEG(n)	LCD segment(n+40)	-
COM1/SEG(n+1)	LCD segment(n+1+40)	K
COM1/SEG(n+2)	LCD segment(n+2+40)	L
COM4/SEG(n)	LCD segment(n)	I
COM4/SEG(n+1)	LCD segment(n+1)	A
COM4/SEG(n+2)	LCD segment(n+2)	G
COM5/SEG(n)	LCD segment(n+40)	B
COM5/SEG(n+1)	LCD segment(n+1+40)	H
COM5/SEG(n+2)	LCD segment(n+2+40)	F
COM6/SEG(n)	LCD segment(n+80)	C
COM6/SEG(n+1)	LCD segment(n+1+80)	M
COM6/SEG(n+2)	LCD segment(n+2+80)	P
COM7/SEG(n)	LCD segment(n+120)	J
COM7/SEG(n+1)	LCD segment(n+1+120)	N
COM7/SEG(n+2)	LCD segment(n+2+120)	E

Note: 1 "n" values can be (25, 28, 33, 36, 39 and 42) respectively for alphanumeric character numbers (7, 6, 4, 3, 2 and 1).

2 This reference table covers all alphanumeric character, except the alphanumeric character number 5 that is managed by the segment (24, 31 and 32).

In medium+ and high density STM8L152xx/STM8L162xx devices, the LCD RAM is accessed through two pages, each activated by the PAGE_COM bit in the LCD_CR4 register:

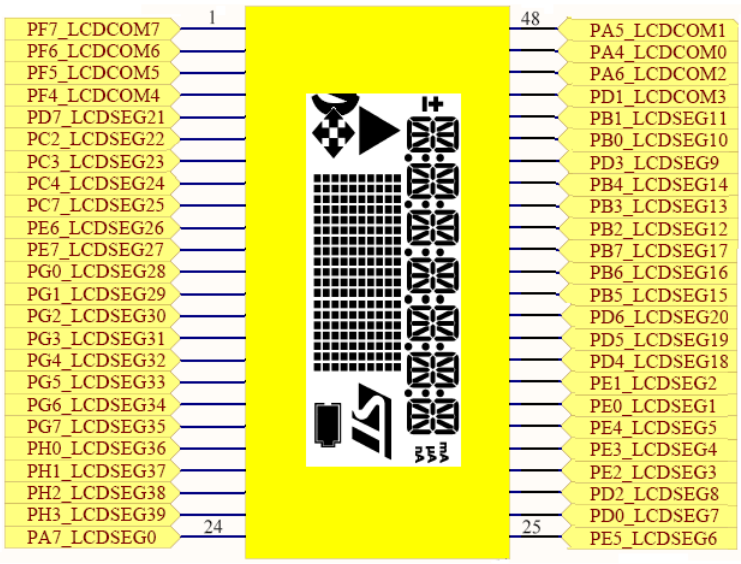
– When PAGE_COM = 0: the LCD RAM register address gives access to the first LCD RAM page, selecting COM0, 1, 2 and 3.
– When PAGE_COM = 1: the LCD RAM register address gives access to the second LCD RAM page, selecting COM4, 5, 6 and 7.

The LCD segments are individually controlled by selecting the dedicated page and setting or clearing the corresponding bit of the LCD data registers (LCD_RAM[21:0]).

The LCD controller module handles the encoding of the physical drive waveforms to the custom LCD Glass HXO5002B.

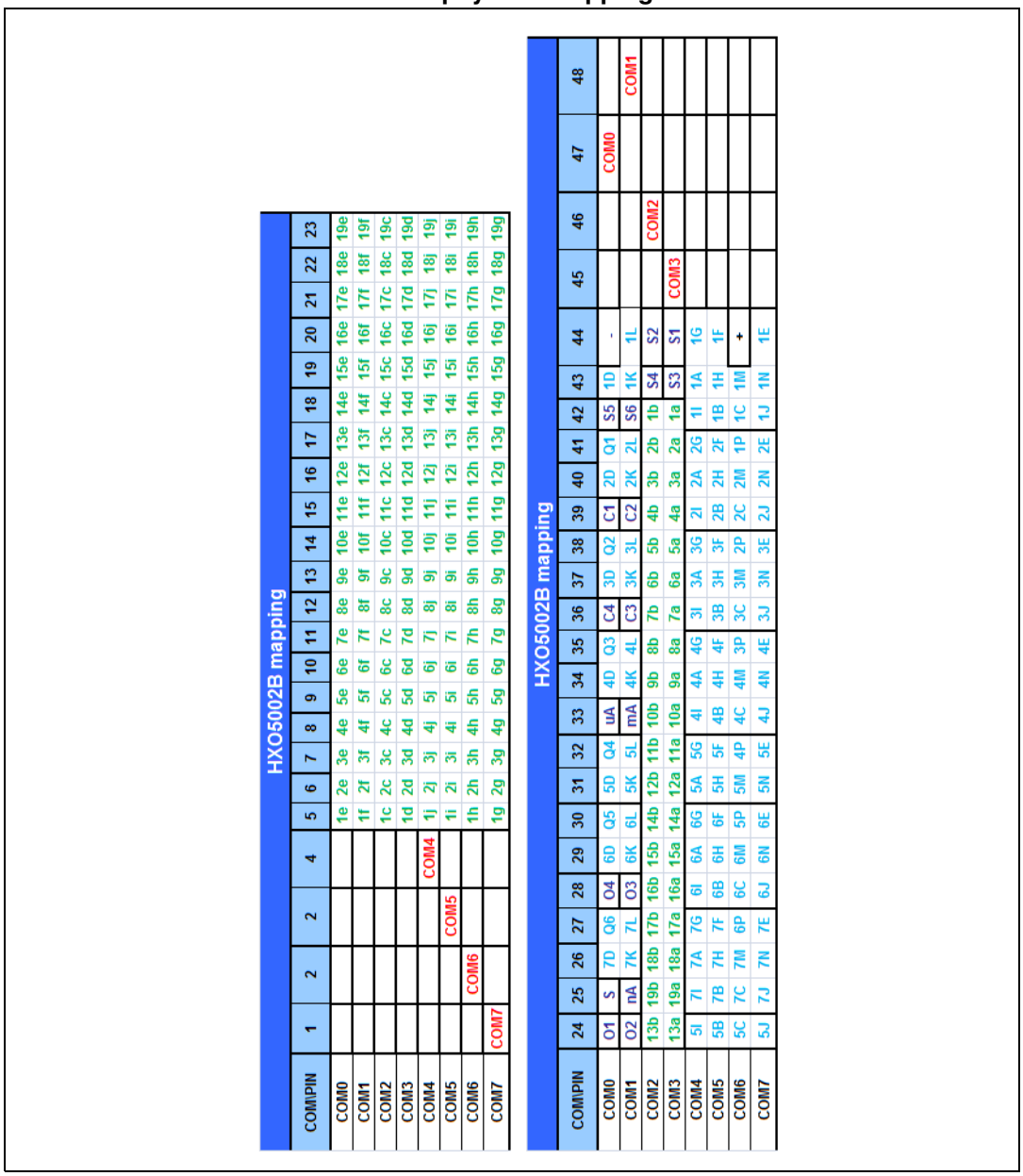
The physical connections between custom LCD HXO5200B and the LCD controller available on the medium+ density STM8L152xx devices and on high density STM8L152xx/STM8L162xx devices must be performed as shown in *Figure 22*.

Figure 22. HXO5002B LCD daughterboard



The physical connections between each pixel, the segment lines and the common lines must be performed as shown in *Table 5*.

Table 5. Custom LCD HXO5002B physical mapping



HXO5002B mapping

COM\PIN	1	2	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
COM0				1e	2e	3e	4e	5e	6e	7e	8e	9e	10e	11e	12e	13e	14e	15e	16e	17e	18e	19e
COM1				1f	2f	3f	4f	5f	6f	7f	8f	9f	10f	11f	12f	13f	14f	15f	16f	17f	18f	19f
COM2				1c	2c	3c	4c	5c	6c	7c	8c	9c	10c	11c	12c	13c	14c	15c	16c	17c	18c	19c
COM3				1d	2d	3d	4d	5d	6d	7d	8d	9d	10d	11d	12d	13d	14d	15d	16d	17d	18d	19d
COM4			COM4	1j	2j	3j	4j	5j	6j	7j	8j	9j	10j	11j	12j	13j	14j	15j	16j	17j	18j	19j
COM5			COM5	1i	2i	3i	4i	5i	6i	7i	8i	9i	10i	11i	12i	13i	14i	15i	16i	17i	18i	19i
COM6		COM6		1h	2h	3h	4h	5h	6h	7h	8h	9h	10h	11h	12h	13h	14h	15h	16h	17h	18h	19h
COM7	COM7			1g	2g	3g	4g	5g	6g	7g	8g	9g	10g	11g	12g	13g	14g	15g	16g	17g	18g	19g

HXO5002B mapping

COM\PIN	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
COM0	O1	S	7D	Q6	O4	6D	Q5	5D	Q4	uA	4D	Q3	C4	3D	Q2	C1	2D	Q1	S5	1D	-			COM0	
COM1	O2	nA	7K	7L	O3	6K	6L	5K	5L	mA	4K	4L	C3	3K	3L	C2	2K	2L	S6	1K	1L				COM1
COM2	13b	19b	18b	17b	16b	15b	14b	12b	11b	10b	9b	8b	7b	6b	5b	4b	3b	2b	1b	S4	S2		COM2		
COM3	13a	19a	18a	17a	16a	15a	14a	12a	11a	10a	9a	8a	7a	6a	5a	4a	3a	2a	1a	S3	S1	COM3			
COM4	5I	7I	7A	7G	6I	6A	6G	5A	5G	4I	4A	4G	3I	3A	3G	2I	2A	2G	1I	1A	1G				
COM5	5B	7B	7H	7F	6B	6H	6F	5H	5F	4B	4H	4F	3B	3H	3F	2B	2H	2F	1B	1H	1F				
COM6	5C	7C	7M	6P	6C	6M	5P	5M	4P	4C	4M	3P	3C	3M	2P	2C	2M	1P	1C	1M	+				
COM7	5J	7J	7N	7E	6J	6N	6E	5N	5E	4J	4N	4E	3J	3N	3E	2J	2N	2E	1J	1N	1E				

The following *Table 6* summarizes the correspondence between LCD_RAM register bits and each LCD character in the custom LCD glass HXO5200B.

Table 6. LCD_RAM bits versus custom LCD HXO5002B characters

LCD RAM	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
First page (PAGE_COM bit = 0)								
LCD_RAM0	7D	S	Q5	6D	O4	Q4	5D	O1
LCD_RAM1	C4	Q1	2D	C1	-	1D	S5	Q6
LCD_RAM2	3e	2e	1e	Q3	4D	uA	Q2	3D
LCD_RAM3	O3	5L	5K	O2	7e	6e	5e	4e
LCD_RAM4	1L	1K	S6	7L	7K	nA	6L	6K
LCD_RAM5	4K	mA	3L	3K	C3	2L	2K	C2
LCD_RAM6	7f	6f	5f	4f	3f	2f	1f	4L
LCD_RAM7	18b	19b	14b	15b	16b	11b	12b	13b
LCD_RAM8	7b	2b	3b	4b	S2	S4	1b	17b
LCD_RAM9	3c	2c	1c	8b	9b	10b	5b	6b
LCD_RAM10	16a	11a	12a	13a	7c	6c	5c	4c
LCD_RAM11	S1	S3	1a	17a	18a	19a	14a	15a
LCD_RAM12	9a	10a	5a	6a	7a	2a	3a	4a
LCD_RAM13	7d	6d	5d	4d	3d	2d	1d	8a
LCD_RAM14	15e	14e	13e	12e	11e	10e	9e	8e
LCD_RAM15					19e	18e	17e	16e
LCD_RAM16	15f	14f	13f	12f	11f	10f	9f	8f
LCD_RAM17					19f	18f	17f	16f
LCD_RAM18	15c	14c	13c	12c	11c	10c	9c	8c
LCD_RAM19					19c	18c	17c	16c
LCD_RAM20	15d	14d	13d	12d	11d	10d	9d	8d
LCD_RAM21					19d	18d	17d	16d

Color key for first page:

= Pixels connected to COM0 (M[i][0])

= Pixels connected to COM1 (M[i][1])

= Pixels connected to COM2 (M[i][2])

= Pixels connected to COM3 (M[i][3])

Table 6. LCD_RAM bits versus custom LCD HXO5002B characters (continued)

Second page (PAGE_COM bit = 1)								
LCD_RAM0	7A	7I	6G	6A	6I	5G	5A	5I
LCD_RAM1	3I	2G	2A	2I	1G	1A	1I	7G
LCD_RAM2	3j	2j	1j	4G	4A	4I	3G	3A
LCD_RAM3	6B	5F	5H	5B	7j	6j	5j	4j
LCD_RAM4	1F	1H	1B	7F	7H	7B	6F	6H
LCD_RAM5	4H	4B	3F	3H	3B	2F	2H	2B
LCD_RAM6	7i	6i	5i	4i	3i	2i	1i	4F
LCD_RAM7	7M	7C	5P	6M	6C	4P	5M	5C
LCD_RAM8	3C	1P	2M	2C	+	1M	1C	6P
LCD_RAM9	3h	2h	1h	3P	4M	4C	2P	3M
LCD_RAM10	6J	5E	5N	5J	7h	6h	5h	4h
LCD_RAM11	1E	1N	1J	7E	7N	7J	6E	6N
LCD_RAM12	4N	4J	3E	3N	3J	2E	2N	2J
LCD_RAM13	7g	6g	5g	4g	3g	2g	1g	4E
LCD_RAM14	15j	14j	13j	12j	11j	10j	9j	8j
LCD_RAM15					19j	18j	17j	16j
LCD_RAM16	15i	14i	13i	12i	11i	10i	9i	8i
LCD_RAM17					19i	18i	17i	16i
LCD_RAM18	15h	14h	13h	12h	11h	10h	9h	8h
LCD_RAM19					19h	18h	17h	16h
LCD_RAM20	15g	14g	13g	12g	11g	10g	9g	8g
LCD_RAM21					19g	18g	17g	16g

Color key for second page:

= Pixels connected to COM4 (M[i][4])

= Pixels connected to COM5 (M[i][5])

= Pixels connected to COM6 (M[i][6])

= Pixels connected to COM7 (M[i][7])

To be able to make an efficient LCD software driver and optimize the LCD character coding in terms of code density, the matrix shown in *Figure 23* has been chosen.

Figure 23. HXO5002B segment driver matrix

```
              COM0    COM1    COM4    COM5    COM6    COM7
SEG(n)     { 0 ,     0 ,     I ,     B ,     C ,     J }
SEG(n+1)   { D ,     K ,     A ,     H ,     M ,     N }
SEG(n+2)   { Q ,     L ,     G ,     F ,     P ,     E }
n = {25, 28, 33, 36, 39, 42}
```

Each matrix M element corresponds to one bit on the LCD_RAM[13:0] registers. To enable SEG(i) connected to COM(j), the “M[i][j]” element must be set to 1 and to disable it the “M[i][j]” element must be set to 0.

The following structure provided in the LCD firmware enables to translate alphanumeric characters from ASCII into LCD_RAM[21:0]:

```
bit[17:0] = Nibble[5:0] = {LCD_RAM[13:10], LCD_RAM[10:7],
LCD_RAM[6:3], LCD_RAM[3:0],LCD_RAM[10:7], LCD_RAM[13:10]};
```

bit[17:0] are the 18 matrix terms arranged so that each nibble is related to LCD_RAM register and to COMi in the selected page. The relation between the nibbles and the LCD_RAM registers is conditioned by the LCD digit being accessed. Refer to *Table 6* for the correspondence between LCD_RAM register bits (nibble) and LCD character.

Displaying a character “A” on the custom LCD glass HXO5002B

The LCD segments A, B, C, E, F, M and N must be activated to display the “A” letter (see *Figure 24*). These segments must then be transferred from the LCD_RAM registers to the LCD glass. Use the matrix described in *Figure 23* to know which bits of the LCD_RAM registers must be set.

The firmware structure provides the value 0x002536 for Nibble[5:0] corresponding to:

- Nibble[0] = 0x0 = 000b
- Nibble[1] = 0x0 = 000b
- Nibble[2] = 0x2 = 010b
- Nibble[3] = 0x5 = 101b
- Nibble[4] = 0x3 = 011b
- Nibble[5] = 0x6 = 110b

To display “A” on position five on the LCD glass, the LCD_RAM registers must be programmed as follows:

- Nibble[0] in LCD_RAM0[0:2] bits: page0 COM0
- Nibble[1] in LCD_RAM3[4:6] bits: page0 COM1
- Nibble[2] in LCD_RAM0[0:2] bits: page1 COM4
- Nibble[3] in LCD_RAM3[4:6] bits: page1 COM5
- Nibble[4] in LCD_RAM7[0:2] bits: page1 COM6
- Nibble[5] in LCD_RAM10[4:6] bits: page1 COM7

Note: All upper case letters and numbers are converted from ASCII characters to LCD_RAM register format. The LCD letter and number maps are stored in two Flash tables (LetterMap and NumberMap) as constants which are used when translating the ASCII characters to LCD RAM registers. For more details, refer to stm8l1528_eval_glass_lcd.c driver.

Figure 24. Letter “A” displayed on the custom LCD HXO5002B

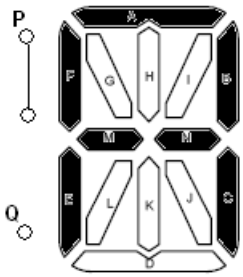


Figure 25. Displaying “A” on the matrix for the custom LCD HXO5002B

```
             COM0    COM1     COM4    COM5    COM6     COM7
SEG(n)     { 0 ,     0 ,      0 ,     1 ,     1 ,      0 }
SEG(n+1)   { 0 ,     0 ,      1 ,     0 ,     1 ,      1 }
SEG(n+2)   { 0 ,     0 ,      0 ,     1 ,     0 ,      1 }
  ------------------------------------------------------------
          =  0       0        2       5       3        6 hex
```

5 LCD segment drive firmware

To facilitate the development of customer applications, ST provides a firmware to drive the LCD segments.

This firmware runs on the STM8L1526-EVAL and STM8L1528-EVAL evaluation boards, which provide all the hardware features to interface with an LCD glass.

- STM8L1528-EVAL set-up
  - Make sure that the LCD glass daughterboard (MB905) is mounted in LCD position.
- STM8L1526-EVAL set-up
  - JP7 jumper on the Key position
  - Make sure that the LCD glass daughterboard (MB821) is mounted in LCD position.

For more details, please refer to the evaluation board user manuals.

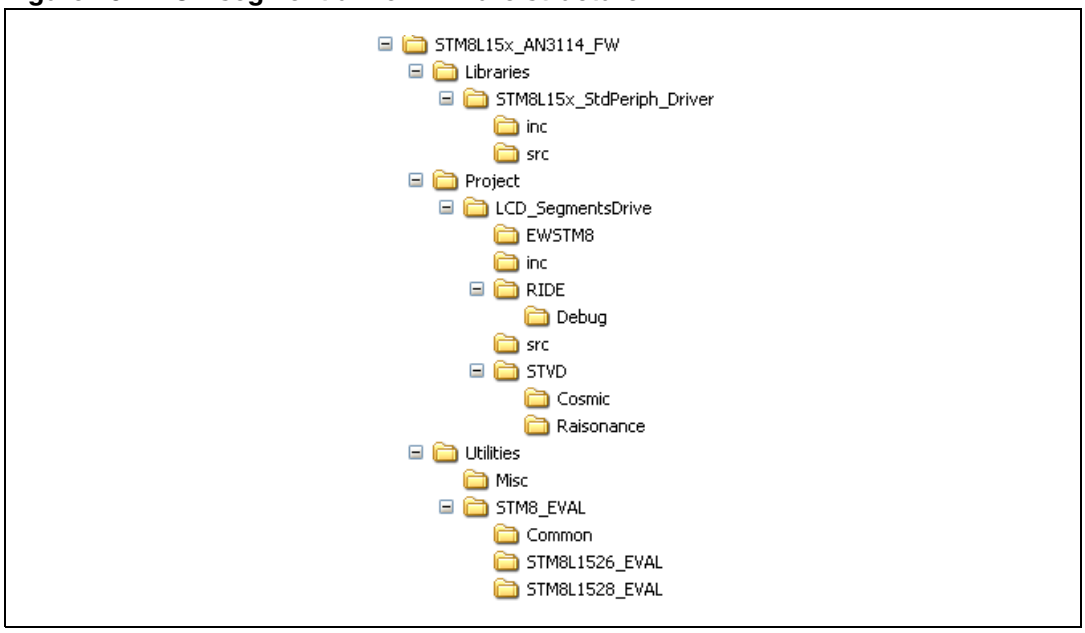
5.1 Firmware package description

The LCD segment drive firmware package contains both projects, one running on STM8L1528-EVAL and the other on STM8L1526-EVAL, and each project provides the LCD glass library and the firmware described in this section.

The firmware package contains the following directories (see *Figure 26*):

- ***Libraries*** directory
- ***Project*** directory
- ***Utilities*** directory

Figure 26. LCD segment drive firmware structure



5.1.1 Libraries directory

The ***Libraries*** directory contains the subdirectories and files that make up the core of the LCD segment drive firmware:

- ***inc*** subdirectory contains the firmware library header files.
- ***src*** subdirectory contains the firmware library source files.

5.1.2 Projects directory

The ***Projects*** directory includes the ***LCD_SegmentsDrive*** subdirectory, which contains the subdirectories and files that make up the core of the LCD glass interface application example:

- ***inc*** subdirectory contains the example header files.
- ***src*** subdirectory contains the example source files.
- ***project*** subdirectory contains the projects used to compile the firmware files.

5.1.3 Utilities directory

The ***Utilities*** directory contains the subdirectories and files used to control the STM8L1526-EVAL and STM8L1528-EVAL board hardware.

5.2 Firmware description

The real-time clock (RTC) provides a set of continuously running counters that can be used to implement a clock-calendar function. The counters values can be written to set the current time of the system. After the evaluation board is powered up, the default time (00:00:00) is displayed on the LCD glass and the first digit of the hour field can be changed.

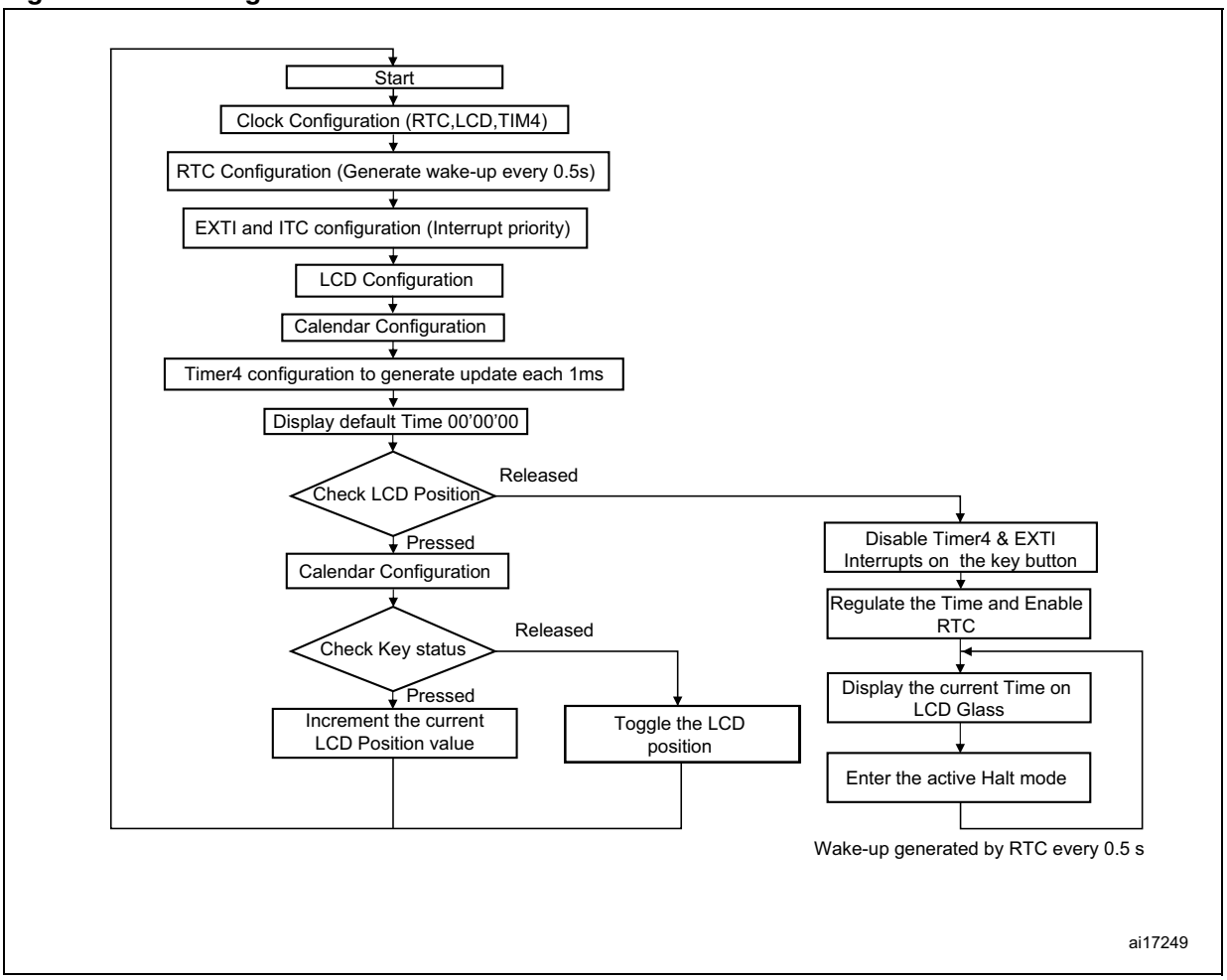
To set the time:

1. Press the **Key** button to increment the active digit. When the **Key** button is released the selected value is stored and the next digit can be changed. The digit allowed values depend on the corresponding field (hour, minute or seconds).
2. Repeat these two steps for the six digits.

Once all the digits are set, the RTC calendar registers are configured, and the current time is displayed on the LCD. The application enters Active-halt mode and is woken up by the RTC wakeup interrupt to display the current time. It then goes back to the Active-halt mode. This operation is repeated infinitely.

Note: Time setting is made only once after the application startup. The application must be restarted to modify the time.

Figure 27. LCD segment drive software flowchart



Note: STM8L1528-EVAL: before displaying the default time, the "STM" string is displayed on the LCD dot matrix and the ST logo segment is ON.

5.2.1 LCD controller setup

The following steps are recommended to configure the LCD controller:

1. Enable the LCD clock.
2. Configure the RTC clock source.
3. Configure the duty ratio and the bias.
4. Configure the frame frequency in the operating frequency range of the LCD glass, that is between 20 and 85 Hz.
5. Configure the voltage source.
6. Configure the port mask registers according to the pins used as segment lines.
7. If the internal voltage source is selected, then adjust the contrast using the contrast bits.
8. If the external voltage source is selected, then adjust the contrast using the dead time bits.
9. The contrast can be adjusted also using the pulse on duration bits.
10. Enable the LCD controller.

In this application, the LCD controller is configured as follows:

- LCD clock source frequency

  f_{LCDCLK} = LSE frequency = 32.768 KHz
- Prescaler factor = 2
- Divider factor = 18 (16 + 2)
- Mode = 1/4 Duty, 1/3 Bias applies to medium density STM8L152xx devices (PD-878 LCD Glass) and Mode = 1/8 Duty, 1/4 Bias applies to high density STM8L152xx/STM8L162xx devices (HXO5002B custom LCD glass)
- LCD clock frequency

  The LCD clock frequency, f_{frame}, is given by the equation below:

$$f_{frame} = f_{ck\_div} \times duty = \frac{f_{LCDCLK}}{2^{PS} \times (16 + DIV)} \times duty$$

As a result, if f_{ck_div} equals 228 Hz, f_{frame} = 57Hz for PD-878 LCD glass and f_{frame} = 28.5 Hz for custom LCD glass HXO5002B.

6 Conclusion

The LCD segment drive firmware allows to develop an LCD glass based application with the minimum firmware and hardware resources.

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
22-Jan-2010	1	Initial release.
02-Aug-2011	2	Added: – Support for the medium+ and high density STM8L152x/STM8L162x devices – How to use the custom LCD HXO5002B available on STM8L1528-EVAL – *Section 1.1: Definitions* – Discrimination ratio calculation Updated: – All data regarding generation of LCD voltage
08-Nov-2012	3	Document updated to include STM8AL3Lxx devices. Added: *Table 1: Applicable products*.

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