RF Analyzer Tutorial

2019.1

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Agenda

> Installation

> Quick Generation and Acquisition

> ZCU111 and ZCU1275 Setup

> Bitstream Generation

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Installation

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Installation Procedure

> **Double click on Setup_RF_Analyzer_1.5.exe**
>> You may have to right-click → Run as administrator

> **Select the folder where you want RF Analyzer to be installed**

> **Click next on the following screens, then Install**

> **The LabVIEW runtime will install automatically if necessary**

> **Restart your computer to complete the installation**

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Quick Generation and Acquisition

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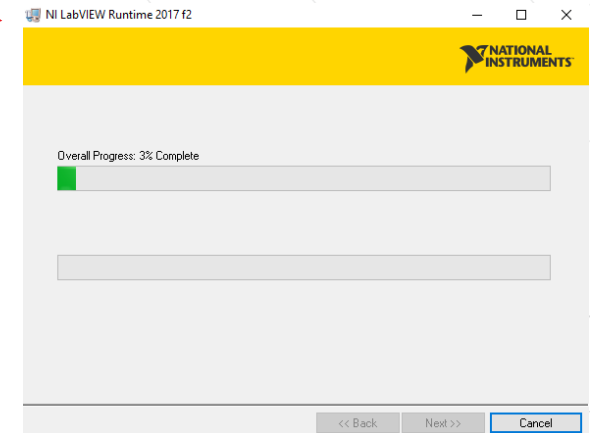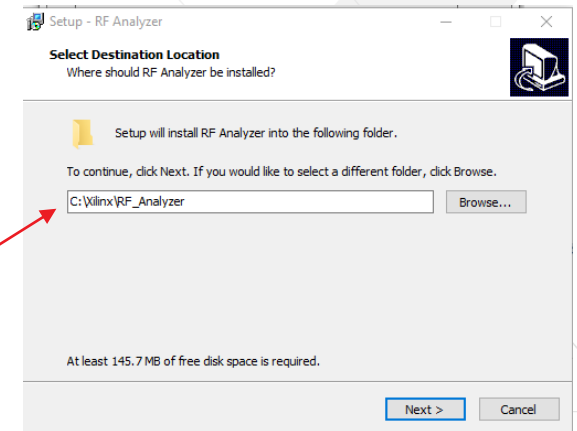
Select the Vivado Path

> **The first time the tool is invoked after installation, you must first select the installation path of Vivado or the stand-alone HW Server**
>> The tool requires hw_server to communicate with the board via JTAG

> **Select the folder where Vivado or the HW Server is installed**
>> In the example shown below, the path is *C:\Xilinx\Vivado\2019.1*

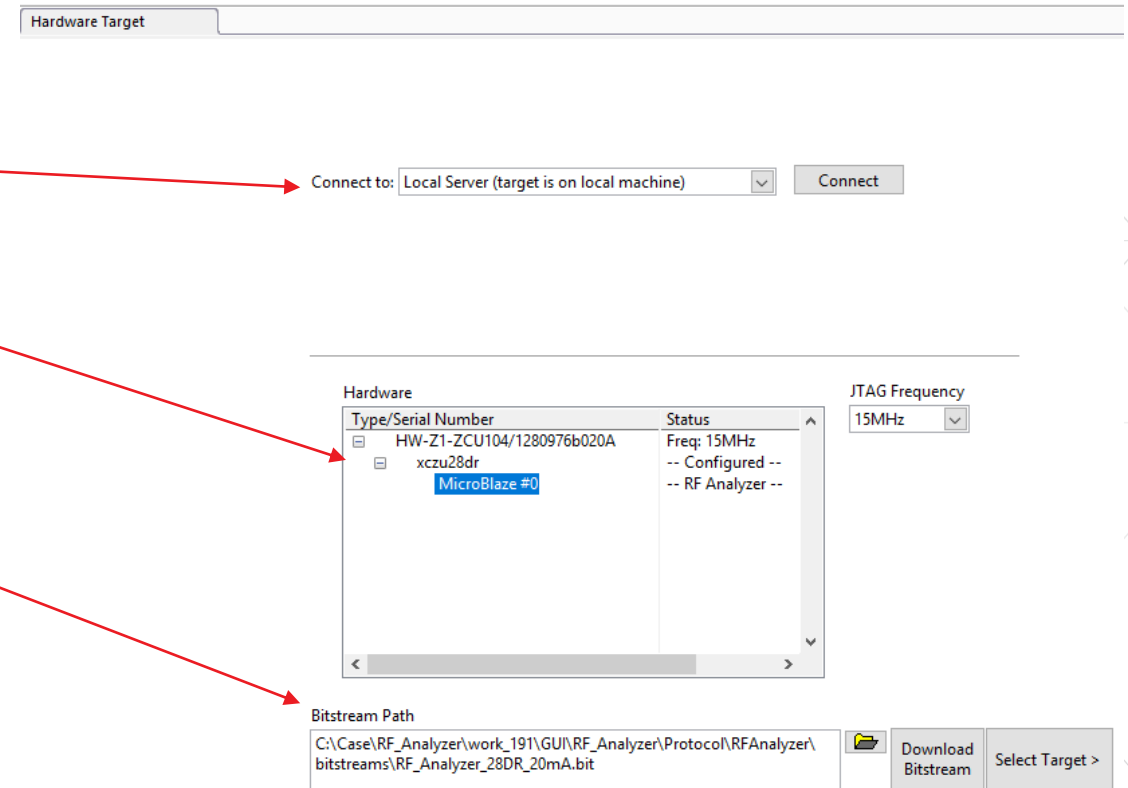**XILINX.**
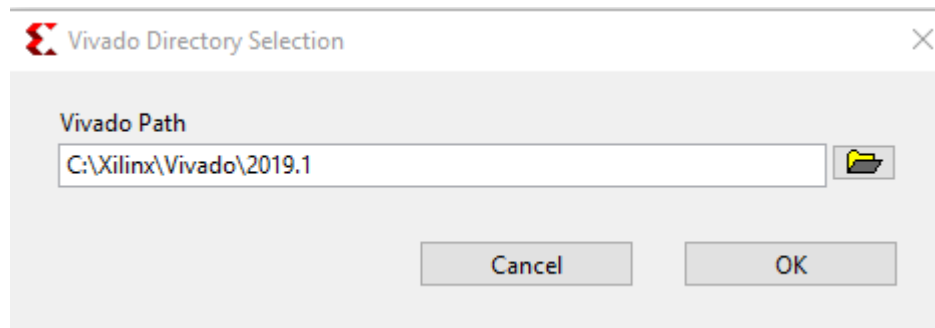
Start screen, Hardware target

> **Similarly to Vivado HW manager, the RF Analyzer start screen allows you to:**
>> Select the connection (Local or Remote)
>> Detects cables and JTAG chain
>> Configure the device
>> Select the target

> **Pre-built bitstreams are located under *<install_directory>*/Protocol/RFAnalyzer/ bitstreams**
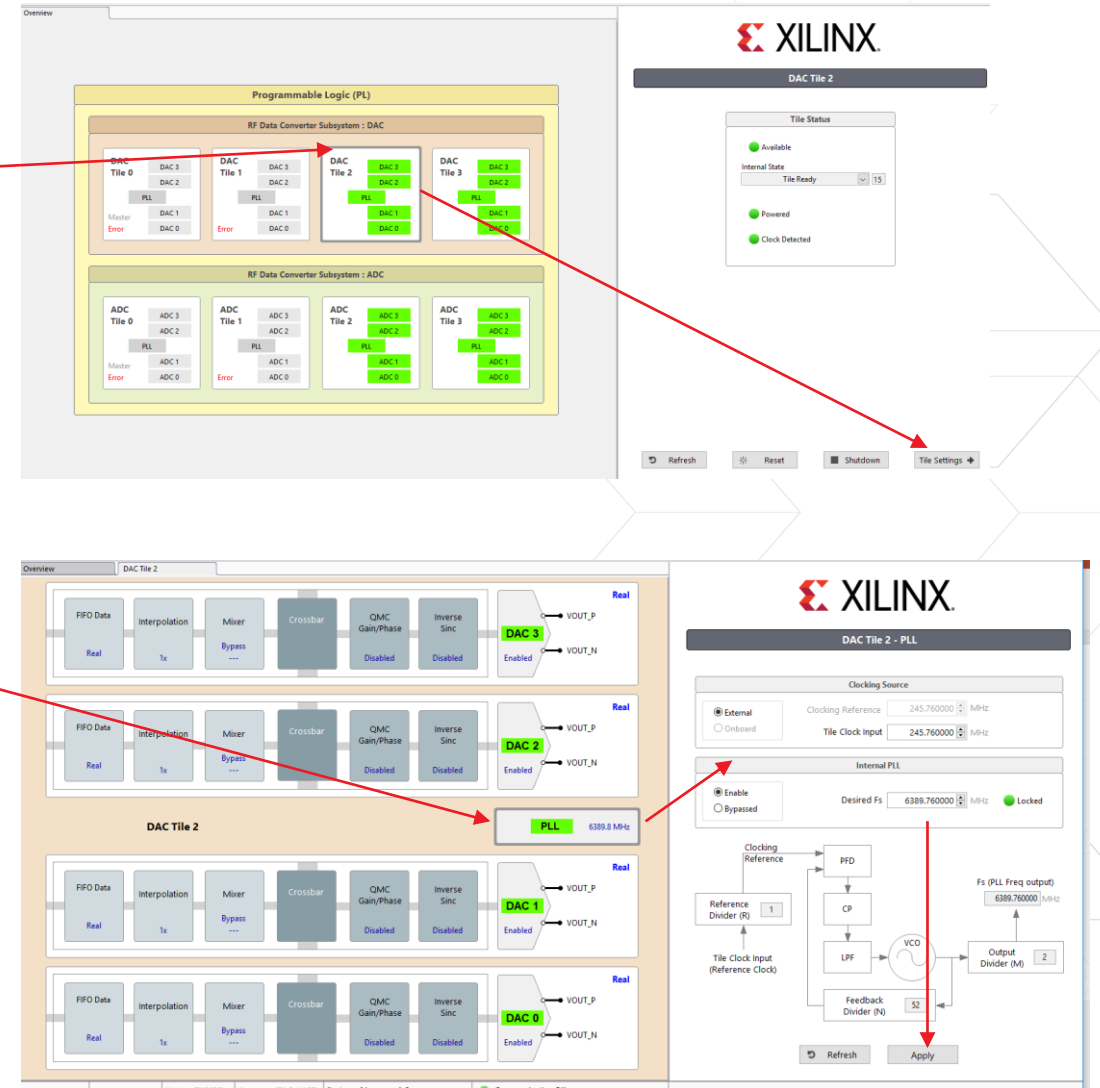
> **To return to this screen, you can select "File->Hardware Target"**

Clock Configuration

> **If the IP and the board clock are configured differently, you can modify the IP PLL configuration**

> **Select the desired tile**

> **Click "Tile Settings"**

> **Select the PLL**

>

> **Configure the PLL according to your board**

> **Click Apply**

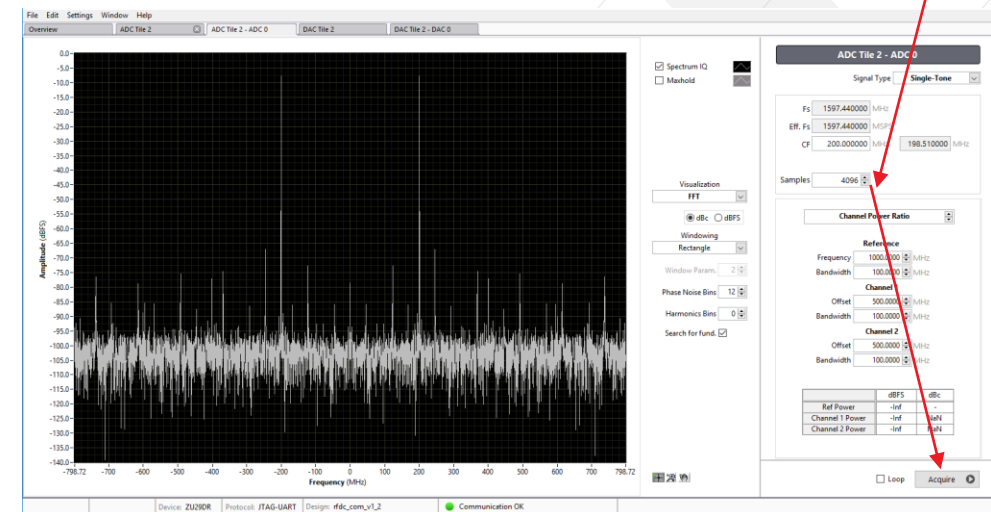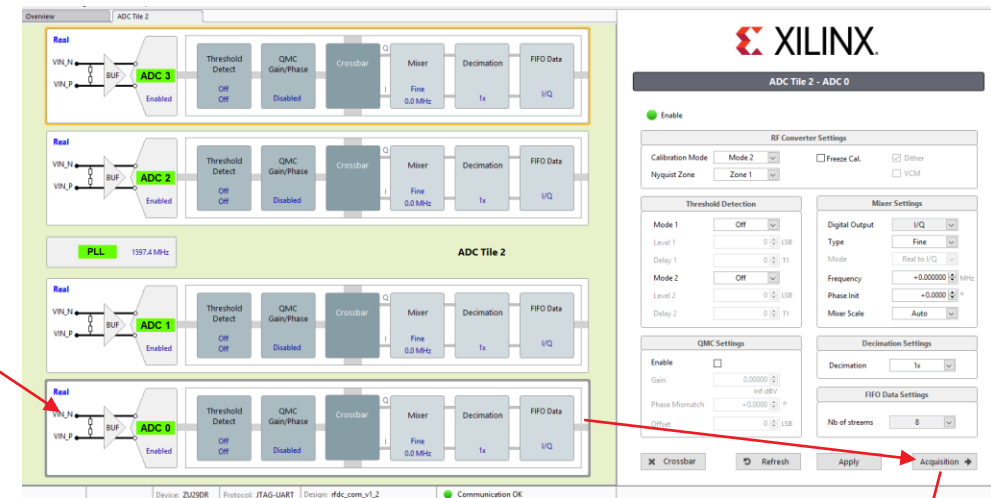Note: external clocks should already be configured on the board

Generation

> **Select the desired channel**

> **Click Generation**

> **Select the frequency tone**

> **Select the number of samples**

> **Click Generate**
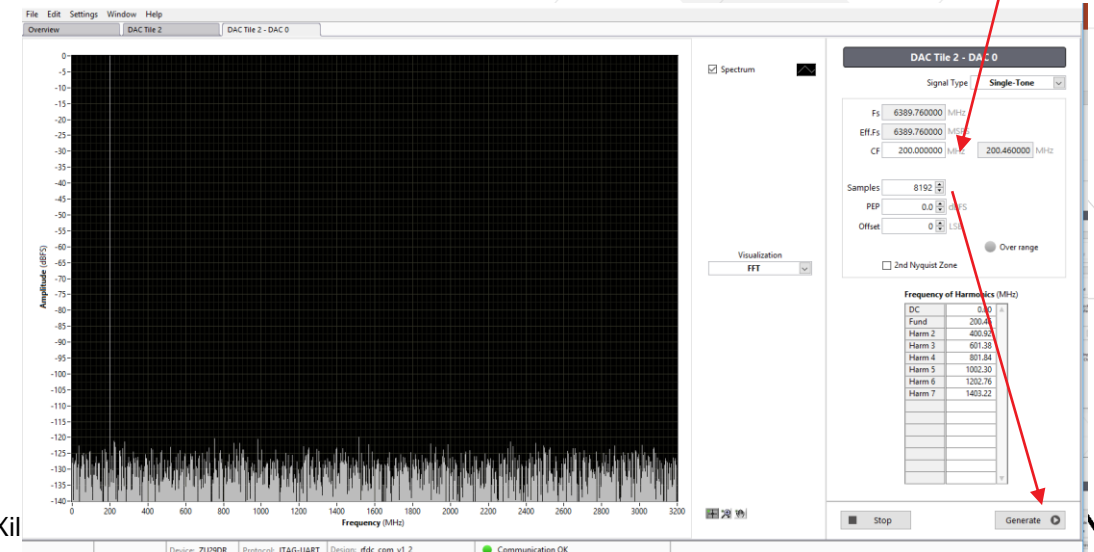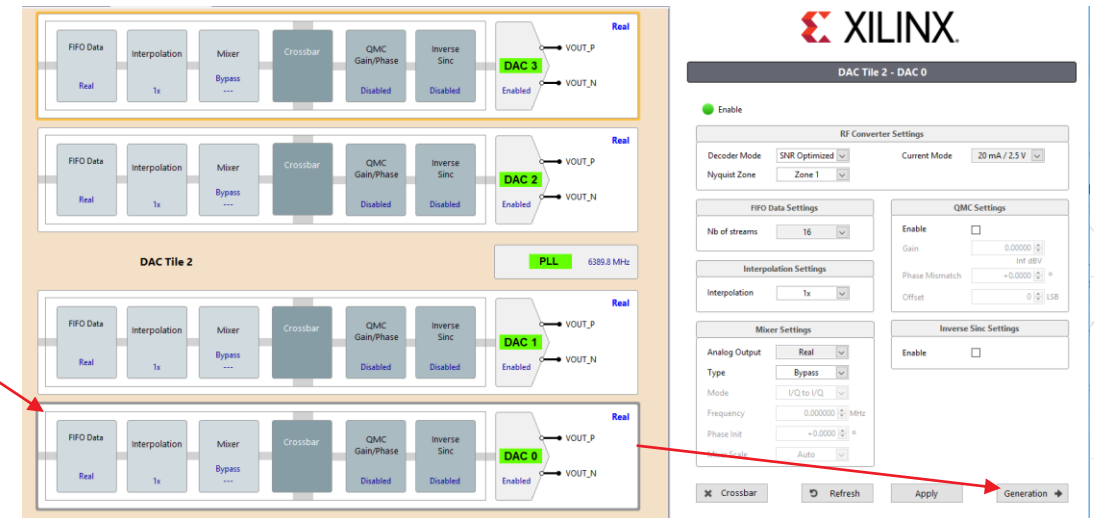
Acquisition

> **Select the desired channel**

> **Click Acquisition**

> **Select the number of samples**

> **Click Acquire**

Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit and Zynq UltraScale+ RFSoC ZCU1275 Characterization Kit Setup
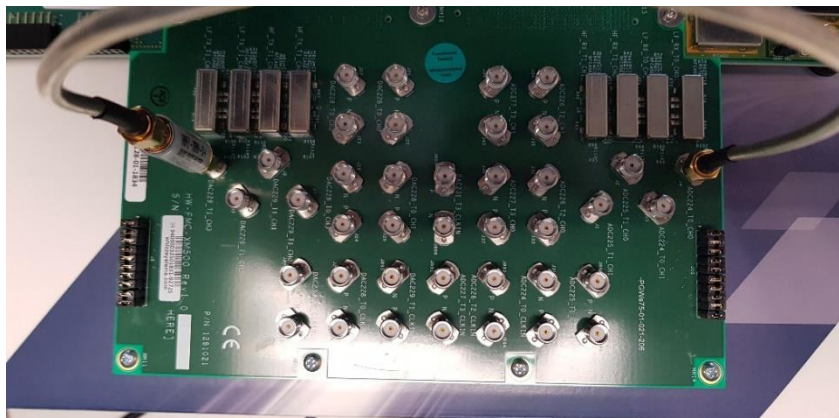
Clock Programming – SCUI

> **External clocks can be programmed with the System Controller GUI (SCUI) application**

> **For a ZCU1275 board, the SCUI can be found at:**
  https://www.xilinx.com/products/boards-and-kits/zcu1275.html#documentation

> **For a ZCU111 board, the SCUI can be found at:**
  https://www.xilinx.com/products/boards-and-kits/zcu111.html#documentation

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ZCU111 Board Setup

> **Connect the JTAG cable**

> **Connect DAC 229 Tile 1 Channel 3 to ADC 224 Tile 0 Channel 0**
>> An optional filter can be used.

> **Generate/Acquire waveforms as per slide 6 to 10**
>> With the above connection in place (as shown in the picture below), DAC tile 1 channel 3 is connected to ADC tile 0 channel 0 (see next slide)

> **For more information, please see:**
https://www.xilinx.com/products/boards-and-kits/zcu111.html#overview

ZCU111 GUI setup

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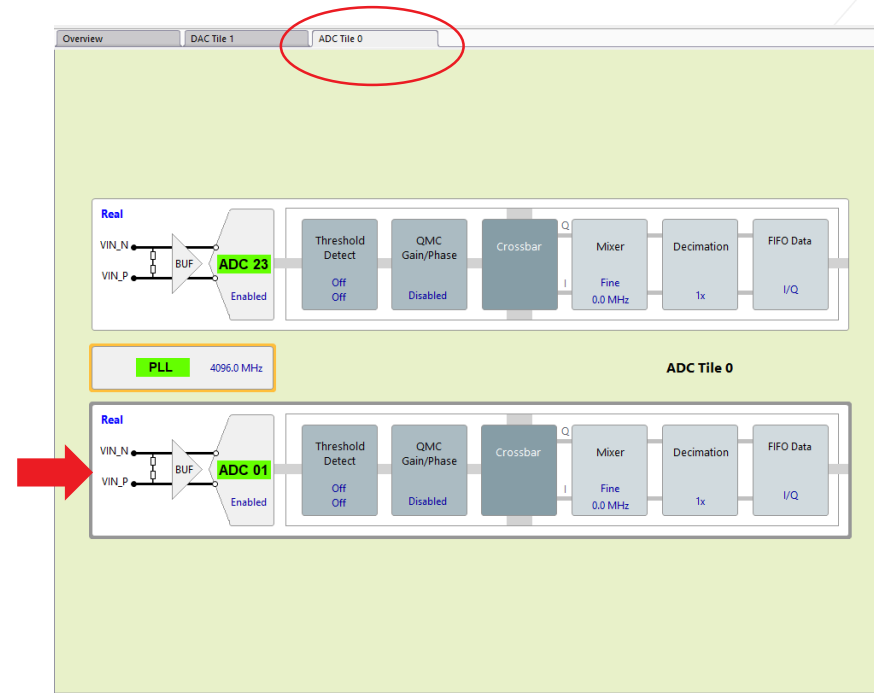
ZCU1275 Board Setup

> **Connect the bullseyes cable to the clock module output**
>> Bullseye 19/20 and 1/2 connect to ADC/DAC clocks

> **Connect the DAC/ADC bullseyes together via DC blocks.**

> **Generate/Acquire waveforms as per slide 6 to 10.**
>> Connector 17/18 match DAC/ADC Tile 0 or 2, Channel 0
>> Connector 15/16 match DAC/ADC Tile 0 or 2, Channel 1

> **For more information, please see:**
https://www.xilinx.com/products/boards-and-kits/zcu1275.html#overview
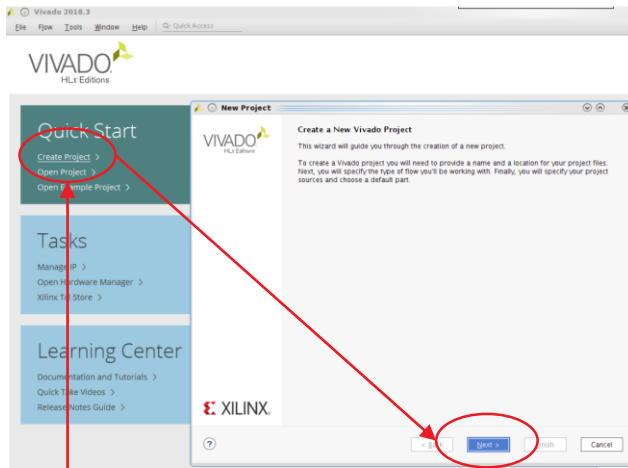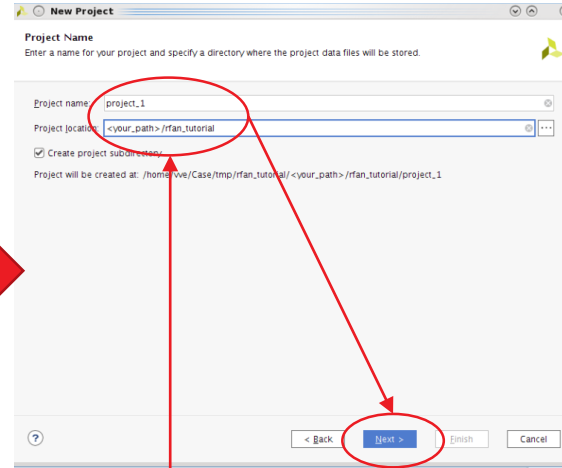
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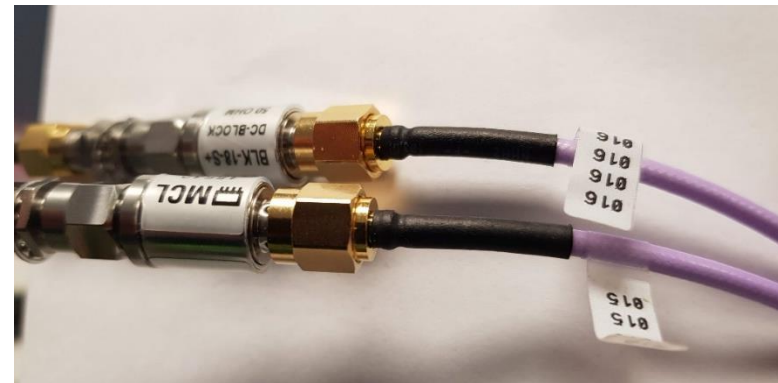
Bitstream Generation

Steps Overview

> **Create a Vivado project**

> **Customize the RF DC IP**

> **Generate the RF DC IP example design**

> **Generate the bitstream**
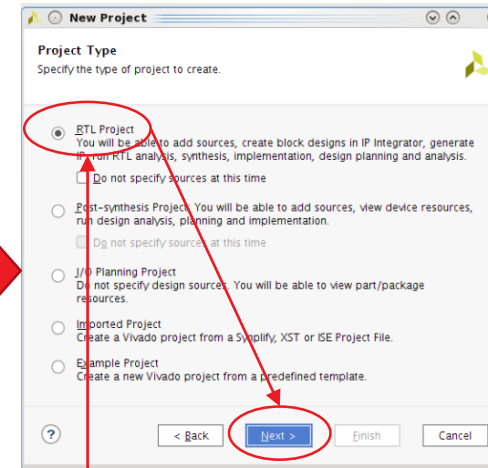 **Note:** pre-built bitstreams are also available under *<install_directory>*/Protocol/RF_Analyzer/bitstreams

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Create a Vivado Project

> **Open Vivado**

> **Click "Create Project"**

> **Click Next**

> **Enter the project name and location**

> **Click Next**

> **Select "RTL Project"**

> **Click Next**
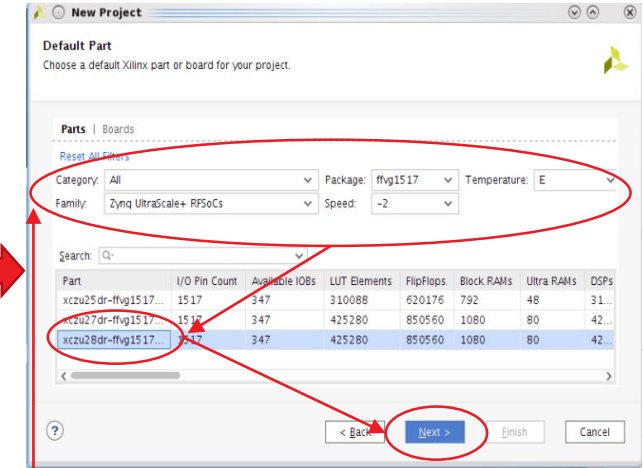
> **Use the filters to find your device**

> **Select the device**

> **Click Next and Finish**

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Add and Customize RF Data Converter IP
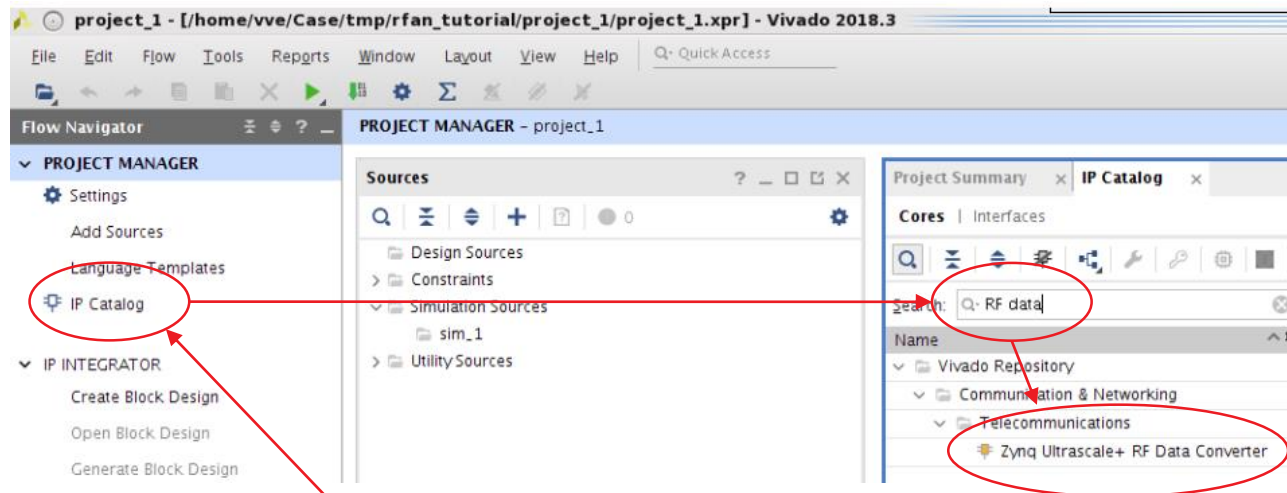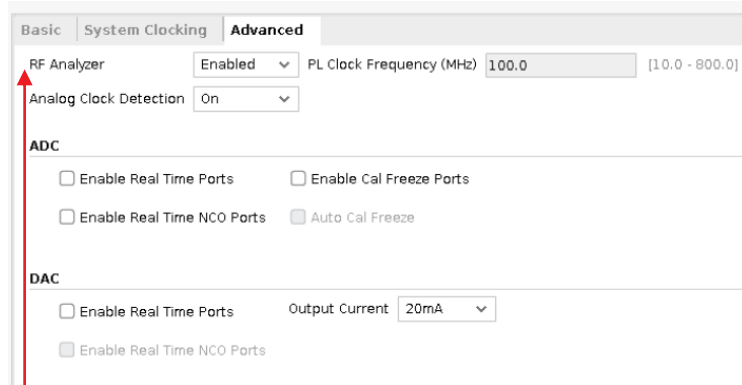

> **Click on IP Catalog**

> **Find the RF Data Converter IP**
>> You can use the search field

> **Double click on the IP**
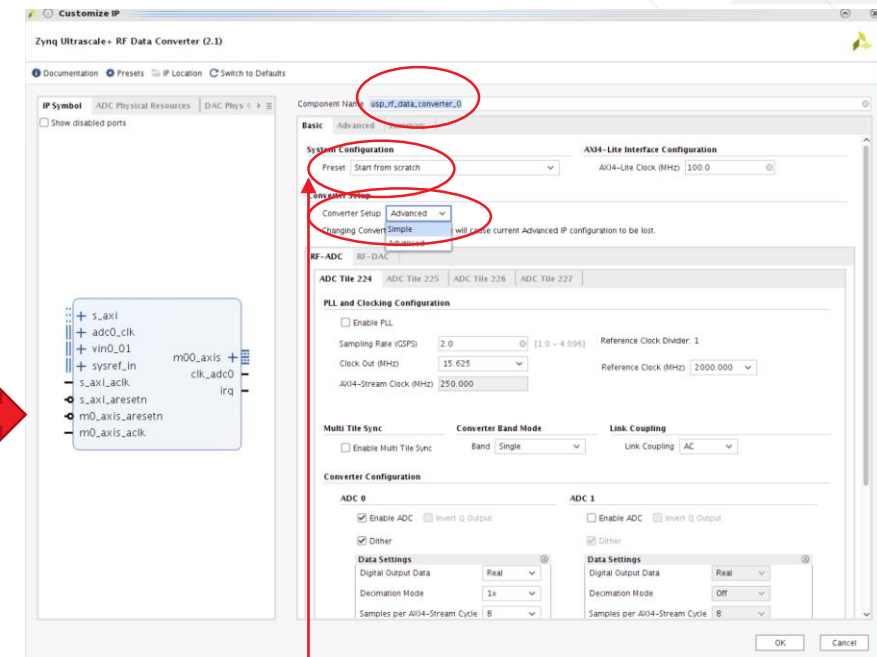
> **Configure the IP as per your board requirement**

> **Be aware of limitations, see (Answer Record 71746)**

> **To speed up the configuration, "Predefined Configuration" or "Simple" Setup can be used**
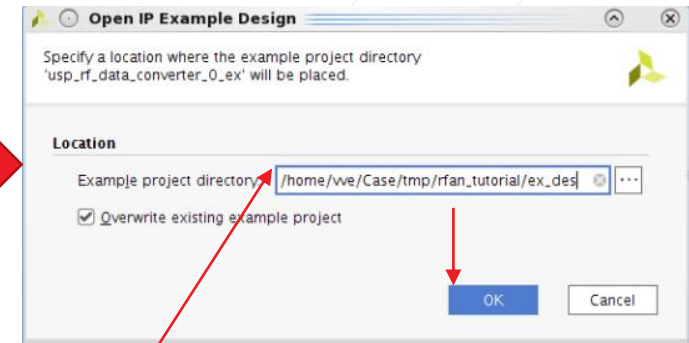
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Generate the RF Data Converter IP Example Design

> In the Advanced mode tab, enable RF Analyzer.

> Click "OK"

> You can skip the IP generation on the next screen
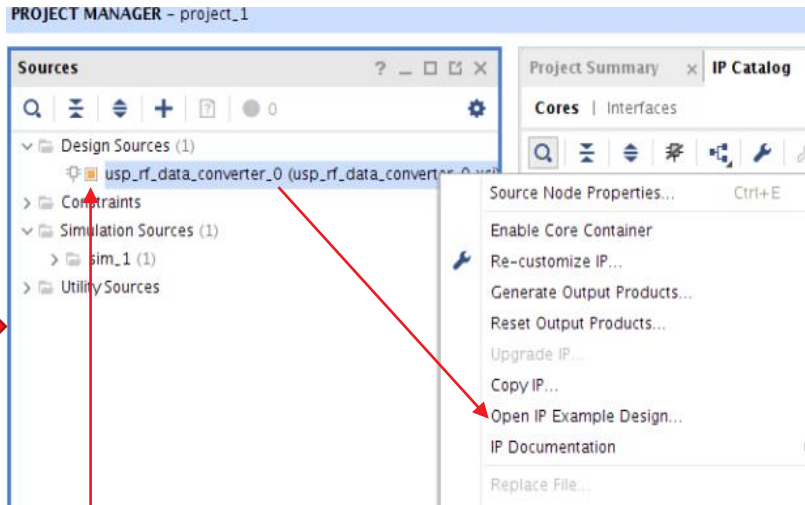
> In the Source window, select the IP
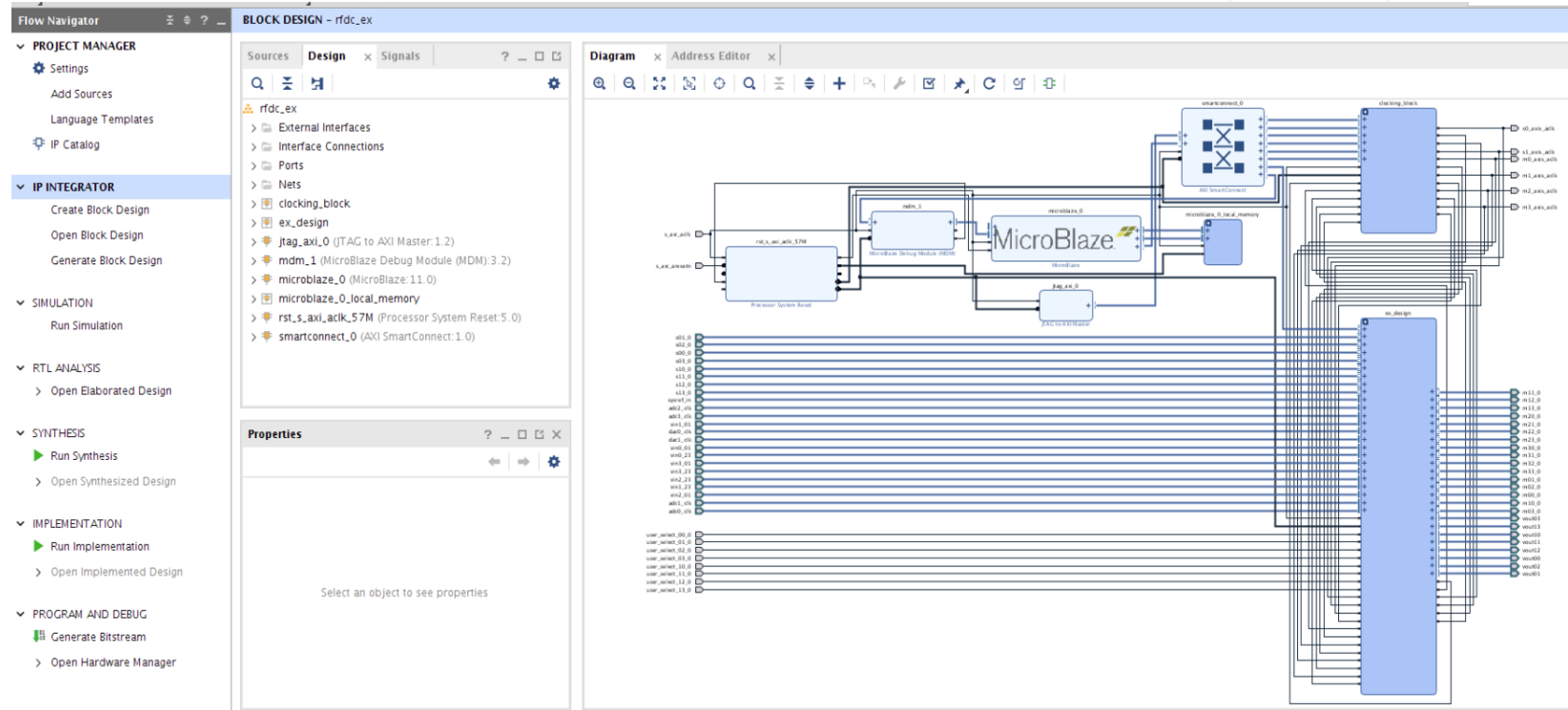
> Right-click and select "Open IP Example Design"

> Select the path where the example project will be created

> Click OK

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Generate the Bitstream

> The example project will create an IP Integrator design

> You may have to zoom-fit to see the full IP Integrator design

> Click "Generate Bitstream"

> Once generated, the bitstream will be found at

<example_design_path>\ip_name\ip_name.runs\impl_1

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