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Business Excellence

Quality at work

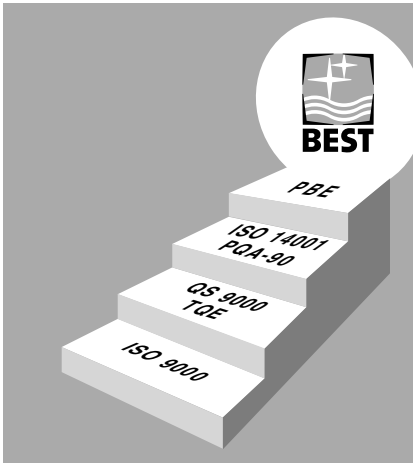
Philips has long recognized the vital importance of high quality in electronic components, and its crucial effect on the viability and economics of finished equipment. This is especially true for semiconductors, which often perform critical circuit functions, such as handling high frequencies, and transmitting high-speed digital data, often in hostile environments.
To achieve the improvements that have made our products amongst the most reliable available, we fully cooperate with our major customers to improve products and processes, to refine test methods to match applications, and to ensure correct applications conditions. Feedback of data on quality levels achieved on customer assembly lines and in service is a vital and continuing part of this cooperation, because it measures the quality that really matters; the quality experienced by our customers which, in turn, directly influences their reputation in the market.

BEST (Business Excellence through Speed and Teamwork)

The company-wide BEST program is the Philips way to Business Excellence. The program was launched in July 1999. It is an extension of the PQA-90 program and incorporates the Philips Business Excellence (PBE) model as the frame of reference for assessing improvement in overall business performance.

From ISO 9000 to Business Excellence

ISO 9000 certificates for Philips Semiconductors manufacturing centres were achieved as early as 1990. The sales organizations and headquarters were certified some years later.
With the Ford TQE award and QS-9000 certifications the customer requirements in the quality systems were enhanced. ISO 14001 shows our dedication to the environment.
Subsequently the Philips PQA-90 program set the road to quality excellence. Almost all eligible units were granted the PQA award before 1999.
Now, Business Units and Accountable Units are being assessed on business excellence to the in the BEST program.



From ISO 9000 to Business Excellence.

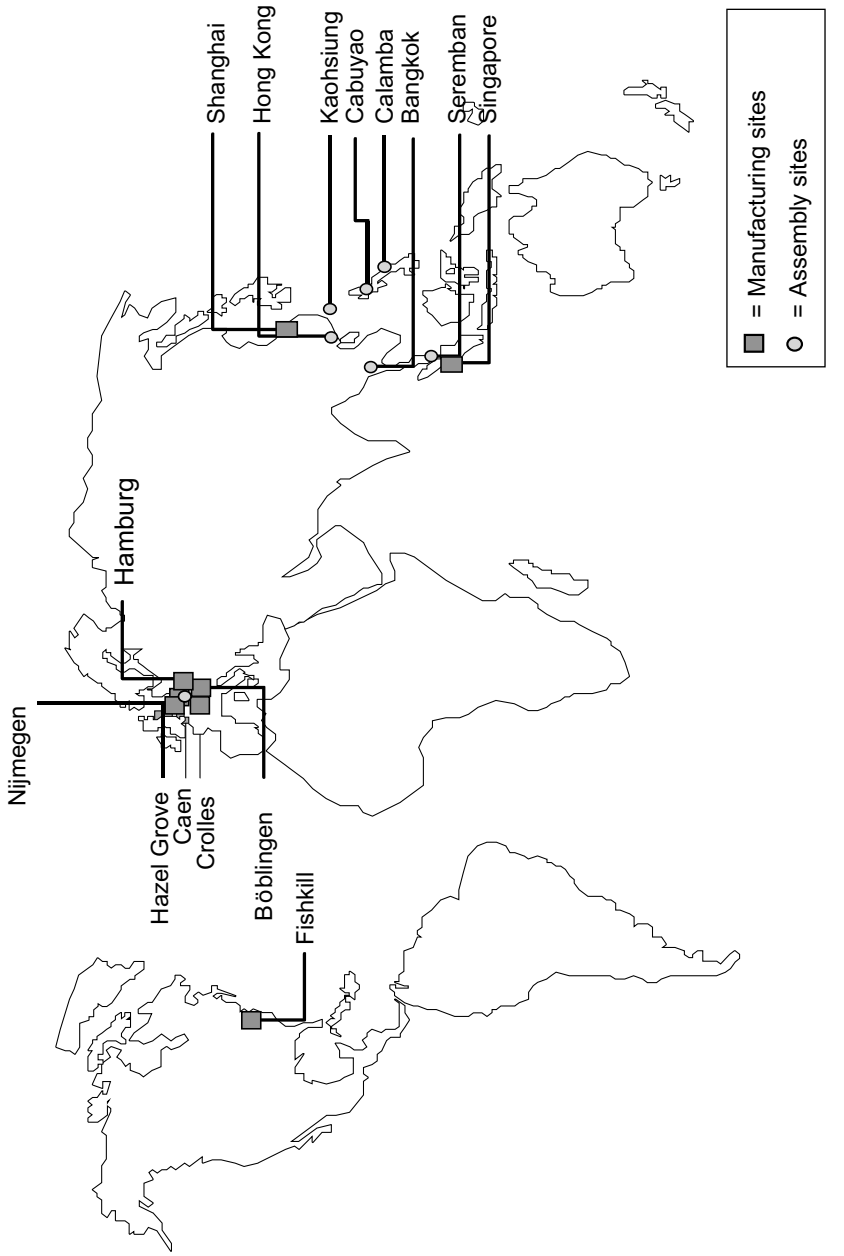
Business Excellence Policy

For over a decade, Philips Semiconductors management used to issue a yearly business excellence policy outlining the goal for the year and deploy the same via town meetings, posters, etc. From 2002, we started a fresh and alternative approach for policy deployment. The CEO of PD Semiconductors, launched a one page summary of the strategy on the divisional Intranet, with a call for action, urging everybody to contribute in translating the strategy in to action. This one page document spelled out where the PD is going, why and how it will get there in a coherent and concise way. Clear "Top Must Do " targets were set and deployed.

Product/Manufacturing centres

Location of Product /Manufacturing centre	Business Unit served		
	Multimarket semiconductors	Consumer Businesses	Communications Businesses
Europe:			
France: Caen		✔	✔
Germany: Böblingen	✔	✔	✔
Germany: Hamburg	✔	✔	✔
The Netherlands: Nijmegen	✔	✔	✔
Switzerland: Zürich		✔	✔
UK: Hazel Grove	✔		
UK: Southampton		✔	
USA:			
Fishkill, New York	✔	✔	✔
Sunnyvale, California			✔
Asia-Pacific:			
China: Guangdon / Jilin	✔		
China: Hong Kong	✔		
Malaysia: Seremban	✔		
Philippines: Cabuyao	✔		
Philippines: Calamba	✔	✔	✔
Taiwan: Kaohsiung	✔	✔	✔
Taiwan: Taipei		✔	
Thailand: Bangkok	✔	✔	✔

Global manufacturing, assembly and test



France: Caen

Built in 1957, Philips Semiconductors factory at Caen, near the D-day landing beaches in Normandy, occupies 5680 square meters of production facilities, including over 2755 square meters of cleanrooms. It has a workforce of around 1200 people.

Philips Semiconductors Caen focuses on the development and prototyping for Sb-SiP concept (Silicon based-System in Package) and the Pics process, through a pilot wafer fab and an assembly pilot line. The IC test and finishing areas are organized as part of the worldwide Assembly and Test Operations (ATO). The site also supports 11 PL, BCT and MST Consumer, Communications and Multi Market Businesses associated with Systems, Applications, Quality Support, Software and RF competences.

The site is certified to ISO 9001, ISO 14001, ISO TS 16949 for Pilot Line Epsilon, ATO and two PL/MST.

The Plant Quality Manager is Joel Porterie, who works closely with the Quality Representatives of the Business Lines and Support. He is also responsible for safety and environmental matters and Infrastructure.

Address :
Philips Semiconductors, 2, rue de la Girafe,
B.P. 5120, 14079 Caen Cedex 5, France.

The Quality Managers are:
Joel PORTERIE,
Plant, Quality Safety and Environment Manager
Tel. (33) 2 31 45 21 46 Fax. (33) 2 31 45 21 77
E-mail: joel.porterie@philips.com

Jean-Emmanuel Gillet, MC/BL Cordless
Tel. (33) 2 31 45 61 89 Fax. (33) 2 31 45 22 80
E-mail: jean-emmanuel.gillet@philips.com

Bruno Perennou, MST TV Front end
Tel.(33) 2 31 45 39 54 Fax (33) 2 31 45 21 65
E-mail:Bruno.perennou@philips.com

Corinne Taglione, ATO
Tel. (33) 2 31 45 30 17 Fax. (33) 2 31 45 22 14
E-mail: corinne.taglione@philips.com

Vincent Civita, Pilot Line Epsilon
Tel. (33) 2 31 45 38 62 Fax. (33) 2 31 45 22 90
E-mail: vincent.civita@philips.com

Eric Quessandier, –Sb-SiP Organisation
Quality Manager
Tel. (33) 2 31 45 31 78
Email : eric.quessandier@philips.com

Pascal Roquet, MST RF Quality Manager
Tel. (33) 2 31 45 23 39 Fax. (33) 2 31 45 39 70
E-mail : pascal.roquet@philips.com

Lelia Devinoy Cbic CAEN Quality Manager
Tel. (33) 2 31 45 60 11 Fax. (33) 2 31 45 62 30
E-mail : lelia.devinoy@philips.com

François Quinones, MST ACB Quality Manager
Tel. (33) 2 31 45 61 24 Fax. (33) 2 31 45 38 80
E-mail : francois.quinones@philips.com

Jean-François Fouillard, Quality System Manager
Tel. (33) 2 31 45 31 40 Fax. (33) 2 31 45 21 77
E-mail : jean-francois.fouillard@philips.com

Germany: Böblingen

Situated in Böblingen, southern Germany, Philips Semiconductors GmbH Böblingen (PSB), formerly known as SMST, has been a 100% Philips subsidiary since January 1st 1999.

The main wafer fab covers 12,180 square meters, of which 6584 square meters are cleanroom (with class 1 in the production area).
The background cleanroom class is 1000.
The facility employs around 700 people and the technical manufacturing capacity is 22,000 wafers (200 mm) per month. The manufacturing line has a capacity for structures down to 0.32 micron. Currently the following processes, with derivatives, are qualified at PSB:

- SC 075, 100, 150, 175
- High-voltage options SC 175
- LCOS
- Automotive and optics applications
- Embedded Logic.

PSB is the Philips single source for Embedded logic devices, and offers product design and test support for Embedded Logic products. Process development is performed for process derivatives, such as shrink versions and high voltage sapplications. PSB has a long history of quality achievements and was certified according to ISO 9001 in 1995 and QS-9000 as well as ISO 14001 in 1998. As the first Philips fab PSB achieved the new TS 16949 in 2001. A TQM concept based on empowerment, achievement bonuses, teamwork and individual motivation has long been established to ensure continuous improvement. Today it is extended through BEST/PBE, for which PSB received the “Finalist” award of the German Ludwig-Erhard-Prize and was “Recognized for Excellence” by the EFQM in 2004.

The Quality Manager is Karl-Heinz Saremski.
E-mail: karl-heinz.saremski@philips.com
Philips Semiconductors Böblingen,
Schickardstrasse 25, 71034 Böblingen.
Tel.: (49) 70 31 18 4669
Fax: (49) 70 31 18 54 00

Germany: Hamburg

With a wide variety of activities from design and test development to manufacturing and marketing, Philips Semiconductors GmbH has locations in Hamburg, Böblingen, Nürnberg and Starnberg and is the second largest semiconductors manufacturer in Germany.

The Philips Semiconductors Hamburg site hosts various businesses, wafer fabs and test facilities for discrete semiconductors and ICs.

With their headquarters located in Hamburg, BL-Identification, BL-Car Infotainment Systems and BL-General Applications Products are responsible for the worldwide development, quality management, logistics and marketing of their products; other Business Lines are also represented on-site through business segments and/or supporting activities.

The Consumer Business Innovation Center-Hamburg defines, provides and maintains cutting edge solutions in the area of Video, Display and RF processing. In the Discrete Wafer Fab and the IC Foundry Hamburg, discrete semiconductors and ICs for a wide variety of applications are produced using a range of technologies. Products are also tested on-site, with IC Test Operations being organized as a part of the worldwide Assembly Test Organization (ATO). Philips Semiconductors Hamburg employs about 2300 people spread over two locations. The site holds ISO 9001, ISO / TS 16949, OHSAS 18001 and ISO 14001 registrations.

Business Line General Applications Products (BL-GA)

BL-GA is a multi-site activity with headquarters in Hamburg. With wafer fab, wafer test, development, marketing, logistics and quality management in Hamburg, the BL is also responsible for the diode activity in Nijmegen and cooperates with significant parts of the assembly activities in Guangdong, China (PSG), Hong Kong, China (EDL), Cabuyao, Philippines (PSPI) and Seremban, Malaysia (PSS). The Business Line has been assessed and meets the QS-9000 requirements.

Product portfolio:
- Low-frequency small-signal transistors
- Switching-, Schottky- and zener-diodes
- Semiconductor sensors for temperature and magnetic-field measurements.

Quality Manager: Horst Waschkewitz
Tel.: (49) 40 5613 2662
Fax: (49) 40 5613 3093
E-mail: horst.waschkewitz@philips.com

Business Line Car Entertainment Solutions (BL-Car)
BL-Car is a TS-16949 certified, fabless multi-site organization with headquarters in Hamburg, and additional locations in Nijmegen, Southampton, Eindhoven and Tokyo. The business segments are:
- Car Radio
- Digital Car Radio

With the product portfolio:
- Car Radio Frontend and Tuning
- Voltage Regulators and Audio Power Amplifiers
- Digital Reception Frontend
- Storage
- Control
- Car Digital Sound Processor
- Digital Radio and Satellite Reception

Quality Manager is Karl-Heinz Greßmann.
Tel.: (49) 40 5613 2752
Fax: (49) 40 5613 3548
E-mail: karl-heinz.gressmann@philips.com

Business Line Identification (BL-ID)
BL-ID is a fabless multi-site activity with headquarters in Hamburg (Germany), and additional locations in Gratkorn (Austria) and Caen (France). BL-ID employs about 310 personnel supporting its three Market Sector Teams:
- Contactless and Embedded Security
- Transportation and Logistics
- Car access & immobilizers

As technology and innovation leader in the area of identification, BL-ID provides a broad portfolio of chip based identification technologies for smart cards, Near Field Communication (NFC) contactless (RFID) applications, car immobilization and tire pressure monitoring.

In addition to ISO / TS 16949, BL ID fulfils several quality and security management requirements, such as: EUROPAY CQM, Common Criteria (security) and EMV. These are mandatory for specific market segments such as banking, e-business, pay-TV and automotive.

Quality Manager: Manfred Horst
Tel.: (49) 40 5613 2625
Fax: (49) 40 5613 3554
E-mail: manfred.horst@philips.com

Consumer Business Innovation Center Hamburg (CBIC-H)
CBIC-H is a development center of the Consumer Business Cluster of Philips Semiconductors. CBIC-H provides system solutions to Business Lines in the domains of TV, PC, Multimedia and Automotive applications. It has ISO 9001, ISO / TS 16949 certification (with BL-Car), ISO 14001 certified with green flagship designs. A CMMI level 2 compliant deployment program is in place.

The activity range includes:
- IC Design
- IP Development
- SW Development
- Test Development and Product Engineering
- Customer Complaint Handling
- Reliability Monitoring and Failure Analysis

Quality Manager: Dieter Paxa
Tel.: (49) 40 5613 1880
Fax: (49) 40 5613 3392
E-mail: dieter.paxa@philips.com

IC Foundry Hamburg (ICFH)
The ICFH wafer fab is a high-volume production center that provides Philips Semiconductors with Bipolar, BiCMOS, CMOS and Passive Integration services for automotive, monitor, identification, audio, TV and protection applications. Its wafer fab capacity is around 10k wafer-starts (150 mm) a week, with dimensions down to 0.4 micron. Cleanroom facilities occupy about 4000 square meters.

The activity range includes:
- Production
- Fab engineering
- Product engineering
- Process development
- Foundry service.

Quality Manager: Adolf Belka
Tel.: (49) 40 5613 3069
Fax: (49) 40 5613 3239
E-mail: adolf.belka@philips.com

Quality Systems & Sustainability Manager:
Jens Meyer
Tel.: (49) 40 5613 2305
Fax: (49) 40 5613 2686
E-mail: jens.meyer@philips.com

ATO-Hamburg
ATO-Hamburg belongs to the Assembly & Test Organization (ATO) with headquarters in Singapore. ATO-Hamburg is the test-innovation-center for business lines located in Hamburg for wafer- and package-test and supports the local wafer fabs with quick test data feedback via monitor wafer test. ATO-Hamburg is the bare-die center of competence of the BU-ATO.
The activity range includes:
- Wafer testing
- Wafer treatment
- Package testing.

Quality Manager: Maren Jutta Steffen
Tel.: (49) 40 5613 1505
Fax: (49) 40 5613 3113
E-mail: maren.jutta.steffen@philips.com

Automotive Innovation Center (AIC)
The Automotive Innovation Center focuses on advanced development, system studies and technical market studies on automotive electronic systems. Activities are done in close co-operation with worldwide automotive industry, in consortia with standardization boards. The AIC as a competence center has a broad background on automotive architectures, technologies and standards. Among other areas the AIC focuses especially on:
- In vehicle network architectures (In car connectivity)
- Smart Sensor System

Quality Manager: Hannes Wolff
Tel.: (49) 40 5613 2690
Fax.; (49) 40 5613 3524
Email: hannes.wolff@philips.com

Design Technology Center (DTC)
DTC-Hamburg belongs to the Chief Technology Office (CTO) with headquarter in Eindhoven. DTC-H defines and provides world-class methods, tools and flows in (Design for) Test Technology, such that products (ICs) can be tested in the most efficient and effective way, enabling Philips Semiconductors to deliver high quality ICs in time. For 20 years DTC-H has worked in the field of research and development of EDA methods and software tools for Computer Aided Test.
To be able to fulfill today's and future business requirements DTC-H has build a strictly process oriented, learning organization in accordance to Quality Management Systems specified in international and industrial standards.

Quality Manager: Peter Koch
Tel.: (49) 40 5613 3348
Fax: (49) 40 5613 2706
E-mail: peter-cat.koch@philips.com

Philips Semiconductors GmbH

Site Lokstedt	Site Hausbruch
Stresemannallee 101	Georg-Heyken-Str.1
D-22529 Hamburg	D-21147 Hamburg,
P.O.Box 54 02 40	D-22502 Hamburg,
Germany	Germany.

Business Excellence Manager: Michael Küchler
Tel.: (49) 40 5613 2324
Fax:. (49) 40 5613 6 2324
E.mail: michael.kuechler@philips.com

Site Programme Manager TQM: Lewe Petersen
Tel.: (49) 40 5613 2744
Fax: (49) 40 5613 2914
E-mail: lewe.petersen@philips.com

The Netherlands: Eindhoven

Headquarters
Eindhoven houses the headquarters of Philips Semiconductors at the High Tech Campus site. The headquarters of Semiconductors (Building HTC60) houses the Executive Management Team, the Chief Technology Office (CTO), and several staff departments – including Purchasing, Human Resource Management (HRM), Legal, Supply Chain Management (SCM) and Information Communication Technology (ICT).

Personnel at the Campus headquarters building – approximately 340

Management of the Consumer, Communications and MultiMarket semiconductor businesses, and the manufacturing operation are also located in Eindhoven. The Campus is also the base for Philips Research.

One of the staff departments based at Semiconductors' headquarters is Quality Management Semiconductors (QMS), headed by the PD quality manager Sankara Narayan.

The visit address is:
High Tech Campus 60,
Eindhoven.

The postal address is P.O. Box 80021,
Building HTC60, 5600 JZ, Eindhoven.
Tel.: +31 40 2723012
Fax: +31 40 2722415

The Consumer Businesses Innovation Center Eindhoven (CBIC-E), The Re-use Technology Group (RTG), Library Technology Group (LTG), Operations and Technology & Customer engineering Groups (TCG) are all located at the Campus. (Same address as Headquarters – with different building number.)

Consumer businesses Innovation Center Eindhoven (CBIC-E) is located in building HTC41 and employs 160 personnel. Its mission is to be the leading provider of solutions to TV set makers, supporting them with system knowledge, architectures, designs and software components. The center executes development and innovation projects for the Consumer business cluster.

Quality manager of ICE is Francois Roullier.
Tel.: (31) 40 2724448.

The Re-use Technology Group (RTG), Library Technology Group (LTG), Operations and one of the Technology & Customer engineering Groups (TCG) are located in building HTC46.
These groups, are part of CTO, and employ about 150 people.

Quality Manager of CTO departments is Henk Bijl
Tel: (31) 40 27 22546

Other sites in Eindhoven

Marketing & Sales
The Marketing & Sales organization is located in building VS at the Boschdijk complex in Eindhoven. The organization of about 150 personnel leads the global market segments and the global sales operation units. The whole Marketing & Sales organization is covered by one worldwide ISO 9000 certificate.

Address: Complex Vredeoord
Boschdijk 525
5621 JG Eindhoven

Global Quality manager is Marty Michaels, located in San Jose, California.
Tel.: +1 408 474 8082

The Netherlands: Nijmegen

Philips Semiconductors, Nijmegen produces discrete semiconductors and professional, industrial and consumer ICs.

Starting from 5 employees in 1953 for the manufacture of diodes and low-frequency transistors, the Philips Nijmegen has grown to become the largest manufacturing facility in Europe solely dedicated to solid-state products. Besides the wafer fabs, the Nijmegen site also accommodates design facilities within the Business Lines.

The site is certified to ISO 9001:2000 and TS16949:2002 and ISO 14001:1996.

Industrial Center Nijmegen (ICN)
With about 2500 employees and 22,800 square meters of cleanroom area, ICN is the largest waferfab in Europe. ICN has four production facilities each with its own characteristics:

Manufacturing 4" (former RFN) may be small with its capacity of 80k wafers per year, but is specialized in handling the complexity of a wide range of processes and products. The process technologies, with a feature size down to 0.6 micron, include Bipolar, MOS, VDMOS, LDMOS, Passive Integration and Diodes. Beside consumer products, the main area of application is the communication market.

The capacity of Manufacturing 5" (former AN), is 600k wafers per year produced in Bipolar, BiMOS, BCD and SOI technologies. The feature size of these technologies, used mainly for automotive and mainstream consumer applications, is 1.0 micron and above. In Manufacturing 6" (former MOS-2) you will find CMOS, BiMOS and TrenchMOS technologies with a feature size ranging from 3.2 micron to 0.4 micron.
The capacity is 240k wafers per year. The main area of application is the commodity market.
Manufacturing 8" (former MOS-34) can produce 500k wafers per year. With CMOS, BiMOS, Non-Volatile, RF, Imaging and High Voltage

process technologies with feature sizes from 0.8 micron down to 0.14 micron, Manufacturing 8" supplies products for both the consumer and the industrial market.
With in-house process development and the extensive use of technologies - such as SOI, Non-Volatile (EE, OTP & Flash), BiMOS, Imaging, 0.18 micron High Voltage and all submicron baseline CMOS technologies. ICN fulfils an important role as 'motherfab' in both process transfers and support to other waferfabs. Its prototyping service is recognized worldwide as a benchmark and the center provides BLs with the fastest time-to-market for product introductions.

ICN is certified to TS 16949:2002 and ISO 14001.
Quality systems manager is Gerard de Groot.
E-mail: gerard.de.groot@philips.com
Quality assurance manager is Han Gerritsen.
E-mail: han.gerritsen@philips.com

Assembly & Test Organization Nijmegen (ATO)
Assembly and Test Organization Nijmegen (ATO-N) supports Philips Semiconductors Business Lines (BLs), Wafer Foundries and Philips Semiconductors offshore test and assembly sites for wafer testing, final testing, sample assembly and provides shipping/invoicing and test data feedback services.

ATO-N is part of the European Local Test Units (LTUs). The other two LTUs are based in Hamburg (Germany) and Caen (France).

Quality manager: Debby Persoon
E-mail: debby.persoon@philips.com

ATO – Innovation
ATO Innovation is part of the BU ATO. It is the department that develops IC packages and processes to order to support the Business Lines in Philips Semiconductors in their packaging needs.

ATO Innovation is a multi-site organization (with groups in Asia -assembly factories-, Europe and the US). The Nijmegen team consists of 55 people. Focus in Nijmegen is on pre-development (new package concepts, improved materials and assembly processes).

Quality manager: Ineke van Hattem
E-mail: ineke.van.hattem@philips.com

Business Line RF products (BL-RF)
BL-RF is part of the Emerging Business Unit (EBU) and is a multi-site activity having the worldwide business responsibility for:

- **RF Discretes** (Wideband transistors, PIN diodes, Varicaps etc) - serving markets as mobile communication and tuner applications (car radio, TV's, DVD-R etc)
- **Hybrid amplifiers and optical receivers** applied in cable TV systems and many ICs used in the domain of digital optical transmission systems

The Business Line is organized in two Product Lines (PL) and one group focusing on new RF Business Development. On top of its existing portfolio, the BL has new RF products such as Bulk Acoustic Wave (BAW) filters and low noise gain blocks for satellite receivers under development. The portfolio also allows us to address the trend of fiber optics in the Fiber to the Home Systems. Product Development and most wafer diffusion are handled locally, all assembly and testing is done off-shore.

The Business Line employs about 100 people in Nijmegen and is certified to ISO 9001:2000, TS 16949:2002 and ISO 14001 standards. Continuous improvement is driven by use of the Philips Business Excellence model.

Quality manager is Jos de Bruijn
E-mail: jos.de.bruijn@philips.com

Business Lines Standard TV Systems and Mainstream TV Solutions
The Business Lines Standard TV Systems (BL STS) and Mainstream TV Solutions (BL MTS) both belong to the Business Unit TV Systems. With headquarters in Shanghai, BL STS is represented in Nijmegen by its Business Creation Team (BCT) for Analog CRT TV, focusing on signal processing systems for Analog CRT TV sets and RGB amplifiers.

Also residing on the Nijmegen site is the BL MTS headquarters and its BCT for Analog Matrix (LCD) TV.

The Product Quality and Customer Liaison Manager of both Business Lines is Mario de Vaan.

Business Line Personal Entertainment Solutions
The Business Line Personal Entertainment Solutions is an organization providing multimedia solutions for the Connected Consumer while on the move. It belongs to the Business Unit Connected Multimedia Solutions.

Besides the Business Line headquarters, the Nijmegen site also accommodates the Market Sector Team (MST) Portables, with product range Radio ICs and Solid State Audio and the MST Amplifiers, with product range Amplifiers and Data Converters.

The customer liaison and quality officer is Jannes Marinus.

Business Line Car Entertainment Solutions
Also a part of the Business Unit Connected Multimedia Solutions, the Business Line Car Entertainment Solutions is an organization exploiting advanced entertainment solutions for the Connected Consumer in the car. With its headquarters in Hamburg, this Business Line is represented in Nijmegen by the System Segments Car Radio and Digital Car Radio.

The customer liaison officer is Dick Juffermans.

Quality or customer liaison managers
Mario de Vaan, BL STS / MTS
Tel: (31) 24 353 2533 Fax: (31) 24 353 2299
E-mail: Mario.de.vaan@philips.com

Jannes Marinus, BL PES
Tel.: (31) 24 353 4378 Fax: (31) 24 353 4637
E-mail: jannes.marinus@philips.com

Dick Juffermans, BL CES
Tel.: (31) 24 353 4283 Fax: (31) 24 353 3509
E-mail: dick.juffermans@philips.com

Business Line Cellular Systems
BL Cellular Systems is part of the BU Mobile Communications (BU-MC) and aims to be the leading supplier of system solutions and building blocks for high-volume mobile communications, consumer and computing products. The BL has about 200 employees in Nijmegen in three Market Sector Teams, and is certified to ISO 9001.

Business Excellence Manager is Kees de Vaal.
E-mail: kees.de.vaal@philips.com
The BL Quality Manager is Thierry Kieffer (Zurich).
E-mail: thierry.kieffer@philips.com
Each MST has a local Product Quality Manager and a Quality System Manager

BL Cordless & Multimedia
BL Cordless & Multimedia is part of the BU Mobile Communications (BU-MC) and provides various products.

In Nijmegen a part of MST Nexperia Mobile Multimedia is located.

BL quality manager: Jean-Emmanuel Gillet (Caen)
E-mail: jean-emmanuel.gillet@philips.com

Business Line Standard IC's, PL Logic
BL Standard ICs is part of the BU MultiMarket Semiconductors. The Product Line Logic is a major entity within the BL., being responsible for its worldwide business in standard logic ICs. Its product portfolio is one of the biggest in the industry and covers 5V and low voltage CMOS, BiCMOS and Bipolar families. The BL headquarters are located in San Jose and the Nijmegen site houses Logic Development, Logic Quality and most of its manufacturing activities.

Peter Janssen is Quality manager for Logic,with Gerrit Lodder in charge of Logic Quality Assurance and Bjorn Derix in charge of Logic Business Excellence.
E-mail: peter.gh.janssen@philips.com
E-mail: gerrit.lodder@philips.com
E-mail: bjorn.derix@philips.com

Business Line Standard IC's MCO (Microcontrollers)
This BL is part of BU MultiMarket Semiconductors Leveraging the leadership position in 8 bit 80C51 through continuous innovation, cost improvement and complete product portfolio in flash and OTP. BL Microcontrollers is well positioned to serve a broad and diverse standard product market.

Quality assurance manager: Gerrit Lodder
E-mail: gerrit.lodder@philips.com

Automotive Business Line
This BL, part of BU MultiMarket Semiconductors (BU-MMS), develops solutions for In-Vehicle Networking (IVN), and is recognized as a leading innovator and true volume supplier to the automotive industry.

Our CAN/LIN-bus and advanced SOI silicon process developments have ensured that Philips is leading automotive IVN progress.

We have or are developing developing a suite of products for:
CAN, the standard for powertrain and body electronics LIN, the Local Interconnect Network for localized area like a door Flexray, a high speed bus for reliability, safety and comfort systems.
Safe by Wire, next generation occupant protection systems. Presently the Automotive Business Line is developing an ARM based digital IVN portfolio.

Quality manager is Fred Kuper.

Fred Kuper, MMS/BL-Automotive
Tel.: (31) 24 353 2296 Fax: (31) 24 353 4100.
E-mail: fred.kuper@philips.com

Industrial Strategy and Operations Nijmegen
S&O-N is part of the industrial activity of the BU MultiMarket Semiconductors (MMS). The organization, which employs about 90 people, has two main activities: the Innovation department delivers breakthrough solutions for new and existing packages, processes and the line architecture for the assembly lines of the BU MMS and the ITEC department develops, delivers and services equipment for state of the art high volume-low cost assembly solutions.

IS&O-Nijmegen is certified to ISO9000/2000 and ISO14001. It also holds the PQA90 award.

Quality officer is Lies Braafhart
E-mail: lies.braafhart@philips.com

Quality & Analytical Services (QAS)
QAS is a shared service organization consisting of experienced specialists in three major quality related areas of expertise and competence: Failure Analysis (FA), Process & Material Analysis (PMA) and Reliability & Package Competence (RPC). Natural synergy between these three disciplines provide better value added service to the PD-wide customer base on Philips' processes and products

Quality manager: Ellen Greijmans
E-mail: ellen.greijmans@philips.com

Site Quality/Shared Quality System Services
The Site Quality department enables continuous improvement for products, processes and organizations through implementing quality and business management systems and exploiting synergy over the Site. For efficiency reasons shared quality managers' functions are offered.

Shared Quality managers are: Ellen Greijmans and Greg Wilson
E-mail: ellen.greijmans@philips.com
E-mail: greg.wilson@philips.com

Site Quality Manager: Erika Rosendahl Huber-Groiss
E-mail: erika.rosendahl.huber-groiss@philips.com

Adress Site Nijmegen:
Philips Semiconductors
Gerstweg 2,
6534 AE Nijmegen
The Netherlands.

Switzerland: Zürich

Philips Semiconductors Zürich is the headquarters of Business Unit Mobile Communications.
The site hosts the following Business Lines:

- Business Line Display Drivers – development and supporting functions for managing the production of ICs for driving small and large displays.
- Business Line Cellular Systems – marketing and development of system solutions, ICs and software for cellular telephony and supporting functions for management of production
- Business Line Cordless & MultiMedia – management, marketing, development and all supporting functions for management of system solutions and ICs for consumer communication terminals used in the home

The site holds Ford Q1, ISO 9001:2000 and ISO 14001 certifications.

Site Quality Manager is Daniel Gloor

Quality Managers
Thierry Kieffer, MC/Cellular Systems
Tel.: (41) 44 465 1460 Fax: (41) 44 465 1806

Daniel Gloor, DS/Display Drivers
Tel.: (41) 44 465 1314 Fax: (41) 44 465 1800

Philips Semiconductors,
Binzstrasse 44,
CH-8045 ZURICH,
SWITZERLAND.
Tel.: (41) 44 465 1314 Fax: (41) 44 465 1800

United Kingdom: Hazel Grove

Philips Hazel Grove occupies 15,000 square meters on the edge of the Cheshire country side, and is the headquarters of Business Line Power Management, responsible for the marketing, development and manufacturing activities for power management products.

The site has a PowerMOS wafer fabrication facility supplying products for applications in computing (motherboards, notebooks), mobile (phones, PDA, digital camera), and automotive (power train, chassis systems, body control). Products from the PowerMOS facility include a full range of standard and logic-level TrenchFETS for low voltage applications, together with protected and smart technologies, such as TOPFETs.

The plant holds TS16949:2002 and ISO 14001 registrations and has an effective TQM process firmly established. The Hazel Grove site is proud of the extensive involvement in quality improvement activities.

Quality Manager is Tim Crispin

Philips Semiconductors,
Bramhall Moor Lane,
Hazel Grove,
STOCKPORT,
CHESHIRE SK7 5BJ,
United Kingdom.

Tel.: (44) 161 957 5517
Fax: (44) 161 957 5089

United Kingdom: Southampton

The Philips Semiconductors Southampton (PSS) site has a long association with IC design and manufacture. The site started operations in 1956 as Mullard. Over the years PSS has become a world leader in teletext and CD applications, supplying products to over 40 countries. Deliveries currently stand at over 100 million pieces per year.

In 2004, PSS became a Consumer Business Innovation Center (CBIC). CBIC Southampton is one of 7 such centers established within BU Connected Multimedia Systems Cluster.

The CBIC Southampton site supports the following business activities:

Business Line Home (BL-H): headquartered in Southampton, BL-H is responsible for marketing, management, quality and logistics support of two market sectors: - audio/video: design of ICs for CD audio, CD recordable, DVD video and DVD recordable and - PC applications: design of ICs for CD ROM, CD rw and DVD rw drives.

Business Line Digital TV Systems (BL- DTVS): headquartered in Sunnyvale, California, BL-DTVS has its DTV market sector based at Southampton, responsible for design of ICs for digital television.

Advanced Systems Laboratory (ASL): a leading center of competence for the development of CD, DVD, DTV and navigation systems.

Design Technology Center (DTC): a leading Center of competence for the development of IC design tools for all PS design activities worldwide. The DTC is certified to CMM level 2.

The businesses in Southampton are located in purpose-built accommodation and represent one of the single largest concentrations of electronics engineering and software expertise in the UK. The organization currently comprises more than 500 personnel, over 50% of whom are graduates or postgraduates, predominantly in electronics engineering and software disciplines. Construction of a new building was completed in the spring of 2000 to provide accommodation for the extra staff needed to support the continuing growth in the site's activities.

Total Quality Management is practiced throughout the site, which is certified to: ISO 9001:2000, ISO 14001, PQA-90 and Investors in People, a UK Government initiative in connection with staff development and care. Additionally the site is adopting the Philips-wide BEST approach to Business Improvement.

Quality Representation (main contacts):
CBIC-S: Steve Delaney, Site Services and Quality Manager
BL-Home: Tim Johnson

Philips Semiconductors Limited,
Millbrook Industrial Estate, Southampton,
Hampshire SO15 0DJ, United Kingdom.
Tel.: (44) 2380 316565 Fax: (44) 2380 316305

USA: Fishkill, New York

The Philips Semiconductors Fishkill plant (PSF) is an 8-inch wafer fabrication and test facility in New York State, USA. The plant manufactures CMOS and QUBIC technologies with feature sizes down to 0.18 micron.
The plant occupies approximately 21,000 square meters at the Hudson Valley Research Park in Hopewell Junction, New York, and employs 875 personnel.

The facility, formerly known as MiCRUS, was purchased from IBM in July 2000. MiCRUS was originally formed as a joint venture between IBM and Cirrus Logic in 1995. In addition to the 0.35 micron and 0.25 micron CMOS technologies inherited from Cirrus Logic and IBM, PSF has received RFP (Release for Production) on Qubic 3, Qubic 4, CMOS50 and C075 (EE, OTP, FM) technologies. PSF is developing CMOS50PMU and Qubic4G, QUBiC4plus, and QUBiC4X technologies. PSF is also transferring C075SHVN and HS5 from other sites.

In July 2003 PSF achieved ISO 9001:2000 registration as recognition for its quality system meeting international standards. In June 2004 PSF achieved Semiconductor Assembly Council certification.

The Customer Advocacy Manager is Andy Hunt and the Site Quality Manager is John Hart.

Philips Semiconductors Fishkill
P.O.Box 1279
Hopewell Jct. N.Y. 12533, USA
Tel.: 845 902 1900
Fax: 845 902 1835

USA: San Jose, California

Founded in 1979 Philips Semiconductors San Jose employs approximately 1000 personnel and occupies 40,000 square meters.

San Jose is the headquarters for BU Emerging Business, BL Standard IC, BL Specialty Logic and houses the Silicon Valley activities of Consumer Business. Specific emphasis is placed on custom and semi-custom products for the target market segments Wireless Communication, Networking and Advanced Computing. The site also houses the central staff of Global Sales Organization (GSO) Americas, supports technology development (CTO - process & library), product design, and Package Development (ATO-I).

Total Quality Management (TQM) is practiced, led by the San Jose Quality and Technical Services (QTS) organization.

The main buildings within the San Jose site house the following groups:

- McKay 1 - 1101 McKay Dr:
  CFT, IT, EBU Test
- McKay 3 - 1151 McKay Dr:
  EBU, Cafeteria, Auditorium, Data Center/Servers
- McKay 4 - 1251 McKay Dr:
  EBU, Device Modeling Labs
- Ringwood 1 - 1100 Ringwood Ave.:
  PL MCO, ATO-I Lab
- Ringwood 2 - 1120 Ringwood Ct.:
  BL SIC, BL Auto, CTO, ATO-I
- Ringwood 3 - 1130 Ringwood Ct.:
  GSO, QTS, BP&A, Legal, Internal Audit
- Ringwood 4 - 1140 Ringwood Ct.:
  Consumer Business, SEHS, RCS
- Ringwood 5 - 1150 Ringwood Ct.:
  Site Services Management, Finance, HR, Purchasing, QTS Spec Services

Philips Semiconductors San Jose,
1109 McKay Drive, San Jose, California 95131,
USA.
Tel.: (408) 434-3000

China: Guangdong

Philips Semiconductors Guangdong (PSG), China, was founded in 2000 and is an International Production Center for the assembly and testing of plastic-encapsulated discrete semiconductors, including transistors, diodes and sensors.

PSG occupies over 100,000 square meters, employs over 1200 staff and has a capacity of over 20 billion devices per year, produced in leaded and SMD packages.

Quality system implementation and its improvement is always the major objective at PSG and the facility is certified to ISO/TS16949 and ISO 14001.

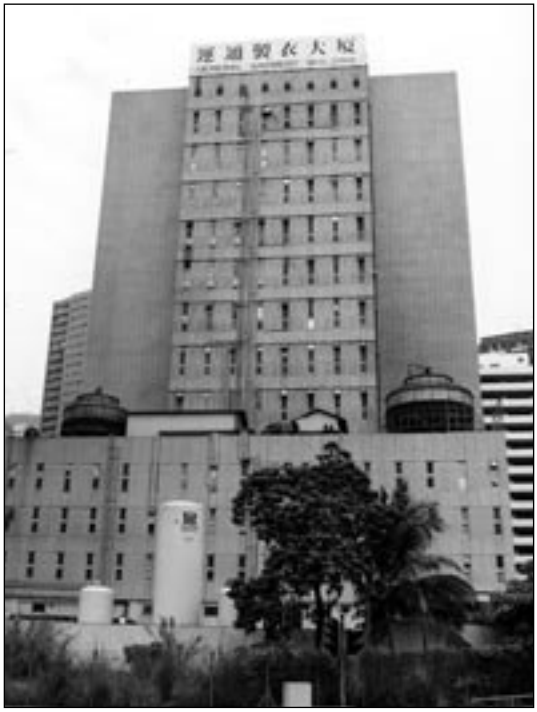
Quality Manager
Ms Mabel Lau

Senior Quality manager
KL Luk

Philips Semiconductors (Guangdong) Co. Ltd.,
Tianmei Industrial North District A Section,
Huangjiang Town DongGuan City,
Guangdong Province, 523750 P. R. China.

Tel.: (86) 769 3632838-408
Fax: (86) 769 3632818

China: Hong Kong



Philips Semiconductors Electronic Devices Limited (EDL) is an International Production Center for the assembly, testing, packaging and distribution of plastic-encapsulated discrete semiconductors including: “small-signal transistors/diodes, “junction FETs, MOSFETs, VDMOS, PowerMOS and TrenchMOS, “wide-band transistors, “thyristors and triacs.

EDL occupies 26,000 square meters and employs over 1000 staff. It has a capacity of over 10,000 million devices per year, produced on flow lines with state-of-the-art production facilities.

Quality has always been an important part of the EDL culture. EDL is certified to ISO /TS 16949, ISO 14001 and OHSAS 18001. EDL is pursuing the Philips Business Excellence Program.

Quality Manager
Mr. Morgan Tseng
tel. +86.769.3668268 ext 2308
fax. +86.769.3533699

Senior Quality manager
KL Luk

Electronic Devices Ltd. (EDL),
10th fl., General Garment Building,
100–110 Kwai Cheong Road,
Kwai Chung, New Territories,
(PO Box 122, Texaco Road Post Office),
HONG KONG.

Tel.: (852) 2424 4024 / (852) 2480 7800
Fax: (852) 2480 0602

Philippines: Cabuyao (PSPI)

Philips Semiconductors Philippines (PSPI) is an international Production Center for the assembly, testing, packaging and distribution of discrete semiconductors and hybrid modules.

Products include:

- PowerMOSFETs, high-voltage transistors, thyristors, triacs and power diodes
- RF Broadband Communication & Base station devices (CATV optical receivers, Base, RF/Microwave)
- System-in a Package solution devices (triple band, Bluetooth, Chip on Board)
- General Application devices (Sensors, Ceramic diodes/SOD110, Glass Diodes)

The plant occupies 45,300 square meters of the total 88000 square meters of land area and employs over 3300 staff. Continuous quality and productivity improvement is rigorously practiced via the Philips Business Excellence (PBE) program. Advanced quality tools and statistical techniques are widely applied. PSPI is certified to ISO 9001,QS-9000 , ISO 14001 and TS 16949.

The Plant Quality Manager is Ms. Emma R. Tomelden

The Quality Leaders for each product lines are:

- Power - Geoffrey Estalilla
- General Applications - Edd Lincuna
- Broadband communication and Base Station - Ronnie Rivera
- Systems-in-a Package Solutions – Ana Cabrera.

Mailing Address:
Philips Semiconductors Philippines Inc.,
P.O. Box 7051,
Domestic Airport Post Office,
1300 Pasay City, Manila, PHILIPPINES.

Plant Address:
Philips Semiconductors (Phils.) Inc.,
Light Industries and Science Park,
Philips Avenue, Barrio Diezmo,
Cabuyao, Laguna, Philippines.
Tel.: (63) 2-844 5139
Fax: (63) 2-844 5248

Philippines: Calamba (PSC)

Philips Semiconductors Calamba (PSC) is the third largest IC Assembly and Test Center within Philips Semiconductors' Assembly & Test Organization (ATO).

Located some 50 km south of Manila, the plant was built in two phases on 85,000 square meters of land. The first phase, with 18,000 square meters of cleanroom production area, started production in January 1999. The second phase, with an additional 25,000 square meters of cleanroom production space, was completed in 2001. The plant currently employs about 2,430 personnel.

Current assembly package capabilities include: L/QFP, SSOP, TSSOP, LFBGA, TFBGA and QFN with pin counts up to 100. Test capabilities include wafer and final testing.

Continuous Quality Improvement and Total Customer Satisfaction are key focus areas for the TQM program. Advanced quality tools and statistical techniques are part of the standard training program for all employees.

PSC successfully passed third-party certification to the ISO 9002: QS-9000 standard within its first year of operation and to ISO/TS 16949:2002 in 2003. An ISO 14001 certification was achieved in April 2000.

The Quality Manager is Ruth Montana.

Philips Semiconductors Calamba,
9 Mountain Drive, LISP-II,
Bgy. La Mesa,
Calamba, Laguna,
Philippines 4027.

Tel: (63) 49 545 7800
Fax: (63) 49 545 0681

Taiwan: Kaohsiung

Philips Semiconductors Kaohsiung (PSK) was established in 1967. Today it employs about 2,600 people. Housed in four buildings made up of approximately 66,000 square meters PSK has over 14,000 square meters of clean room facilities. Producing ICs for all IC Business Units, its annual capacity is more than 1000 million pieces. Its main packages are Shrink-DILs, SILs, QFP, L/T/H QFP,VSO, HSOP, TF/L(F)/P(H)BGA and COF. Quality is paramount in the Kaohsiung plant. Its TQM program focuses on all the employees involved QIC/QIT team improvement. Total customer satisfaction is also key and PSK has been awarded both the ISO14001, and ISO/TS16949 certification. PSK also received the prestigious Japanese Deming award, the Japanese Quality Medal (N-Prize) and PBE Silver award for continuous quality excellence.

The Quality Manager is Adam Lai.

Philips Semiconductors Kaohsiung (PSK) 10 Chin 5th Road, N.E.P.Z.
P.O. Box 35-48, KAOHSIUNG 811
TAIWAN (R.O.C.)

Tel: (886) 7-361 2511 x 8353
Fax: (886) 7-367 8084

Taiwan: Taipei

The headquarters of BU-DS (Business Unit - Display Solutions) were founded in 2002 from two Business Lines, BL Display Processing and BL Display Drivers.

The BU-DS, is based in the Nankang Software Park in the eastern part of Taipei City.
The state-of-the-art software industrial park is designed to promote the development of low-pollution, high-value-added, knowledge-intensive industries. It also houses businesses from other Philips PDs - Medical, Lighting, DAP, and the Consumer organizations.

The result of close government and private sector cooperation to create a world-class environment for companies in these industries, the Nankang Software Park aims to enhance the quality and productivity of software development and engineering design, provide a comprehensive environment for research and development, and boost the effective use of international research and development resources.

The organizations of BU-DS, BL-DP and BL-DD currently have 80+ staffs. The management team of BU-DS all reside in Taipei office.

Business Line Display Drivers:
- Management
- Finance
- Marketing
- Logistics
- CCC (Customer Competence Center)

Business Line Display Processing:
- Management
- Finance
- Marketing
- Logistics
- CCC (Customer Competence Center)

ISO 9001:2000 has been certified I by KEMA since December 2003.

BU-DS
15F-1, No.3-1, YuanQu Street, NanKang Dist.
TAIPEI 115
TAIWAN
ROC

Quality Manager
Peter Jan
Tel.: (886) 2 3789 2355
Fax: (886) 2 3789 2947

Thailand: Bangkok

Philips Semiconductors Thailand (PST), in Bangkok, assembles and tests ICs for worldwide markets. Bangkok supports Business Units headquartered in both Europe and the USA. Its major product lines include standard bipolar logic, standard CMOS logic, analog industrial, bipolar and identification devices.
Located 5 km from Bangkok's international airport, the Bangkok facility recently completed a major expansion of its site. The site now occupies 63,000 square meters, of which 45,000 square meters is allocated for manufacturing. The facility employs 3,500 personnel, and has production capabilities that exceed 3,500 million devices per year.

Its world-class manufacturing capability is driven by continuous quality improvement. The plant holds DESC, ISO 14001, ISO 9001, QS-9000, and ISO/TS 16949 certifications.

Quality department manager is Apichai Lertapiruk.

Philips Semiconductors Thailand,
303 Moo 3 Chaengwattana Road,
Laksi,
BANGKOK 10210,
THAILAND.

Tel.: (66) 2-5511052-62
Fax: (66) 2-5511063-64

Separate units and joint ventures

Austria, Gratkorn, Philips Semiconductors

Philips Semiconductors Gratkorn specializes in contactless RFID. The competence center is active in design, development and marketing of RFID IC's for: Tags & Labels, Transport & Ticketing, Near Field Communication and Car Access & Immobilization.

The Gratkorn site is part of the Business Line Identification (BL ID) in Hamburg and is ISO/TS16949 certified.

Quality Manager is Manfred Horst in Hamburg.

Manfred Horst, Business Line Identification (BL ID)
Tel.: (49) 40 5613 2625
Fax: (49) 40 5613 3554
E-mail: manfred.horst@philips.com
Address:
Philips Semiconductors Gratkorn,
Micron-Weg 1, A-8101 Gratkorn, Austria

China, Shanghai, ASMC

Advanced Semiconductor Manufacturing Corp. of Shanghai (ASMC) is a joint venture of which Philips has a 38% share. ASMC has a 125 mm wafer fab for bipolar processes and a 150 mm and 200 mm wafer fab for CMOS processes. The site employs about 930 people and is ISO 9001, TS16949 certified.

The quality contact is Hai-Zhou Pang.
Address:
385 Hong Cao Road, Shanghai, 200233 China
Tel.: (86) 21 6485 1900
Fax: (86) 21 6485 1056

France, Crolles 2

Crolles 2 is a center of excellence for CMOS innovation. A partnership with ST-Microelectronics, Freescale the facility offers a state-of-the-art 300 mm wafer pilot line for advanced research, process development and manufacturing activities.

Crolles ramps up to a capacity of 2500 wafer-starts per week with a dedicated percentage for R&D and has technology capabilities up to 45 nm. Crolles 2 is linked to Philips CTO in the Netherlands. There are 150 people directly on the payroll of the French Philips site in Crolles.

The quality activities are managed by Jean Marc Melique and Eric Bruls

Address:
860 Rue Jean Monnet,
38926 Crolles Cedex, France.
Tel.: (33) 476 925758
Fax (33)476 925757.

France, Sophia Antipolis

Sophia-Antipolis is a main center for our semiconductor mobile communications and connectivity activities, and has full business responsibility, supplying advanced ICs to most major telecommunications companies in the world.

With more than 300 employees from 19 countries, Philips Sophia Antipolis, has a real international and multi-cultural working environment. Around 70% of the employees are involved in research and development while 30% work in quality, marketing, product engineering, logistics and other supporting activities.

Today, our Sophia-Antipolis R&D center concentrates its resources on providing system solutions in the following key areas:

- Cellular baseband and infrastructure technologies (GSM, GPRS, EDGE, UMTS)
- Baseband solutions for wireless connectivity (Bluetooth™)

- Embedded Cores (DSP, ARM)
- Nexperia™ Cellular System Solutions development
- Design solutions for System On Chip
- Libraries and process technology development

The site has been certified to ISO 9001 since 1994.

The Quality System Manager is Hugues Dailliez.

Address:
Philips Semiconductors Sophia,
505, route des Lucioles, Sophia Antipolis,
06560 Valbonne, France
Tel.: (33) 4 92 96 12 34
Fax: (33) 4 92 96 11 68

India, Bangalore

Philips Semiconductors, Bangalore is based at the Philips Innovation Campus in Bangalore. It was set up in 1996, and currently has a headcount of about 400. The focus of the Bangalore team is on embedded software development and design, and development of VLSI systems.
PS Bangalore enjoys representation from CTO groups as well as Business Lines.
The CTO Groups located here are: RTG (ReUse Technology Group), DTG (Design Technology Group), LTG (Library Technology Group) and TCG (Technology Centre Group).
Business Lines that have established their respective software development groups in Bangalore, include BL Cellular and BL Connectivity.

PS Bangalore is certified to ISO 9001 and CMM level 2. Each group represented here has its own Quality Manager:
RTG – Ravishankar Savitha,
DTG - Arunava Sarker,
LTG - Binu Prakash
BL Cellular - Bappi Paul
Bl Connectivity - MRC Raju

Address
Philips Innovation Campus
1, Murphy Road, Ulsoor
Bangalore - 560008
Tel: 91-80-25579000, Fax: 91-80-25560581

Malaysia, Seremban, PSS

Philips Semiconductors Seremban Sdn. Bhd. (PSS) assembles and tests discrete products in surface mount packages like SOT23, SOT346, SOT323, SOT416, SOT457 and SOT363. Occupying an area of 29,000 square meters, it employs more than 1000 personnel. Using modern reel-to-reel BIM assembly lines, it has a capacity of more than 10 billion units per year.

The facility started as a 50/50 joint venture between Philips and Motorola in 1993. In 2001, Philips acquired the facility in full.

PSS is certified to ISO 9002:2000, ISO 14001 and TS16949.

The Quality Manager is John Kah Sik Lim.

Address:
Philips Semiconductors Seremban,
Pt. No 12687, Tuanku Jaafar Industrial Park,
71450 Seremban, Malaysia.
Tel.: (60) 6-6766 299
Fax: (60) 6-6773 099

Singapore, BU MO

BU Manufacturing Operations (BU MO) is one of the Business Units within Philips Semiconductors, handling all the manufacturing business of the ICs for all the business lines. This includes wafer fabrication, assembly and test.
BU MO has the following waferfabs (front-end operations): ICN (Nijmegen), ICFH (Hamburg), PSB (Böblingen), PSF (Fishkill), Waferfab Caen, as well as the joint ventures SSMC (Singapore) and Crolles 2. The back-end operations include five in-house plants: PSK in Kaohsiung, Taiwan; PST in Bangkok, Thailand, PSC and PSPI both near Manilla, Philippines and ATO5 in Suzhou, China. In addition, BU MO handles all subcontracting business, and also assumes responsibility for the local test sites at Nijmegen, Hamburg and Caen. BU MO is headquartered in Singapore. The Quality manager, responsible for overall product quality matters within BU MO is Enno Korma.

Address:
Philips Electronics Singapore Pte Ltd.,
620A, Lorong 1 Toa Payoh, TP2, Level 2,
Singapore 319 762.
Tel.: (65) 799 51 00
Fax: (65) 799 51 99

Singapore, SSMC

Systems on Silicon Manufacturing Co. Pte Ltd (SSMC) is a joint venture with Taiwan Semiconductor Manufacturing Company (TSMC) and the Economic Development Board of Singapore (EDBI), Philips owns 48% of the business.

SSMC has an 8 inch wafer fab with a capacity to produce 40,000 wafers a month (60% going to Philips), it has below 0.15 micron capabilities. The wafer fab has a total build up area of 92,000 square meters, of which 7,000 square meters are cleanroom manufacturing facilities. Other services offered include wafer test services, design support, low cost prototyping and test program development.

The site employs approximately 1250 personnel and is certified to ISO 9001, ISO 14001, ISO/TS 16949, BS 7799, and OHSAS 18001.

The Quality Systems Manager is Kelly Sofian.
Email: kelly.sofian@philips.com

Site Address:
70 Pasir Ris Industrial Drive 1, Singapore 519527
Tel.: (65) 6248-7000
Fax: (65) 6248-7606

Taiwan, Hsinchu, TSMC

Taiwan Semiconductors Manufacturing Company Ltd (TSMC) is a joint venture in which Philips has a 20% share. It consists of two 150 mm wafer fabs, and nine for 200 mm. TSMC is certified to ISO 9001 and TS-16949.
The Quality and Reliability Director is Dr. John Yue.
Address:
121 Park Ave 3, Science-based Industrial Park,
Hsinchu, Taiwan (ROC).
Tel.: (886) 35 780221
Fax: (886) 35 781546

USA, Tempe

Philips Semiconductors Tempe, USA, houses a broad array of functional organizations including ATO, Emerging Businesses, CTO, MMS (BLIP & BL-SIC) Field Sales, Corporate Investment Groups, Finance, TSSC and Office of Project Management.
Located in the Arizona State University Research Park, Philips Semiconductors Tempe currently has 200 employees. Made up of four buildings, the facility is 12,800 square meters.

The Tempe facility is ISO 14001 registered and many of the groups located in Tempe are ISO/TS16949 registered.

The BLIP and BL-SIC Quality Manager, Dennis Reed, is based in Tempe.
Tel.: (1) 480 752 6290

Philips Semiconductors Tempe,
8375 South River Parkway,
Tempe,
Arizona 85284,
USA.

Technology Centres Group (TCG)

TCG develops innovative System on Chip (SoC) solutions using a blend of advanced design technologies and frontline expertise, combined with professional project management, quality, and testing for both internal and external customers.

TCG is made up of several departments for design support and project management, with the Technical Centres (TCs) located close to customers. The TCG scope covers the entire project cycle from feasibility analysis, development, tape-out, validation and prototype approval. Each design is executed in partnership with a Business Line that brings the final product to the manufacturing stage.

TCG is part of the CTO organization, its Technical Centres are located in San Jose, Seoul, Eindhoven, Milton Keynes, and Sophia Antipolis. In total, it has 130 personnel.

The Quality Improvement Programs Manager for this organization is Mark Gray he is based in Sophia Antipolis.
Tel.: (33) 4 92962395
Fax: (33) 4 92961266

Part 2

References

Abbreviations

ACL	Acceptance Control Limit
AOQ	Average Outgoing Quality
AQL	Acceptable Quality Level
ASIC	Application Specific Integrated Circuit
ATD	Acceptance for Type Development
ATS	Acceptance for Type Study
BCaM	Business Creation and Management
BBS	Business Balanced Scorecard
BEST	Business Excellence through Speed and Teamwork
BGA	Ball Grid Array
BL	Business Line
BU	Business Unit
CHAMP	Complaint Handling And Management Program
CLIP	Confirmed Line Item Performance
CMM	Capability Maturity Model (for software)
CMOS	Complementary Metal Oxide Semiconductor
CPCN	Customer Product/process Change Notification
Cpk	Process Capability Index
CQB	Corporate Quality Bureau
CQS	Customer Qualification Samples
CWQI	Company-Wide Quality Improvement
DOD	Discontinuation Of Delivery
DOE	Design Of Experiments
DPMO	Defect rate Per Million Opportunities
DS	(BU) Display Solutions
EB	(BU) Emerging Businesses
EDI	Electronic Data Interchange
EDP	Electronic Data Processing
EFQM	European Foundation for Quality Management
EMC	Electromagnetic Compatibility
EMS	Environmental Management System
EMT	Executive Management Team
ESD	Electrostatic Discharge
FET	Field-Effect Transistor
FITS	Failures In Time Standard
FMEA	Failure Mode and Effects Analysis
GQS	General Quality Specification
GSO	Global Sales Operations
IC	Integrated Circuit
ICT	Information Communication Technology
IEC	International Electrotechnical Commission

IPMM	International Product Marketing Manager
IQMM	International Quality Managers Meeting
ISO	International Organization for Standardization
ISR	Initial Sample Release
JEDEC	Joint Electron Device Engineering Council
JIT	Just-In-Time
KVD	Key Value Driver
LCL	Lower Control Limit
LSL	Lower Specification Limit
MC	Management Council / (BU) Mobile Communications
MISD	Manufacturing Instructions and Standardization Department
MMS	(BU) MultiMarket Semiconductors
MOS	Metal-Oxide Semiconductor
M&S	Marketing and Sales
MSL	Moisture Sensitivity Level
MST	Marketing Segment Team (part of BL)
MTBF	Mean Time Between Failures
MTTF	Mean Time To Failure
NiPdAu	Nickel Pladium Gold
NO	National Organization
OEM	Original Equipment Manufacturer
OSRP	Overall System Realisation Process
Pb	Lead
PBE	Philips Business Excellence
PD	Product Division
PDCA	Plan-Do-Check-Action
PLCC	Plastic Leaded Chip Carrier
PPM	Parts Per Million
PQ	Packing Quantity
PQA-90	Philips Quality Award (for the nineties)
PQRA	Product Quality and Reliability Assurance (database)
PSC	Philips Semiconductors
QA	Quality Assurance
QC	Quality Control (or Quality Circle)
QBD	charge to breakdown
QDS	Quality Description Sheet
QFD	Quality Function Deployment
QFP	Quad Flat Package
QIC	Quality Improvement Competition
QIT	Quality Improvement Team
QML	Qualified Manufacturers List

QMS	Quality Management Semiconductors
QOS	Quality Operating System
QPL	Qualified Products List
QPM	Quality Policy Meeting
Q&R	Quality and Reliability
RFS	Release For Supply
RLIP	Requested Line Item Performance
RoHS	Restrictions of Hazardous Substances
ROOTS	Rapid On-line Overall Traceability System
RPN	Risk Priority Number
SAC	SnAg3.8Cu0.7
SAC	Semiconductor Assembly Council
SCM	Supply Chain Management
SEM	Scanning Electron Microscope
SER	Soft Error Rate
SMART	Specific, Measurable, Ambitious, Realistic, Time-phased
SMD	Surface-Mounted Device
Sn	Pure Tin
SOAR	Safe Operating Area
SOD	Standard Outline Diode
SOT	Standard Outline Transistor
SPaRC	Schedule, Project and Resource Core
SPC	Statistical Process Control
SPQ	Smallest Packing Quantity
TO	Transistor Outline
TOPS	Team Oriented Problem Solving
TQC	Total Quality Control
TQE	Total Quality Excellence (Ford)
TQM	Total Quality Management
TQS	Total Quality System
TTL	Transistor-Transistor Logic
UCL	Upper Control Limit
USL	Upper Specification Limit
WIT	Withdrawn
ZD	Zero Defects

Acceleration factors

A major factor in determining the reliability of semiconductors is the total stress applied by the application. The total stress will be the sum of several components, both electrical and environmental. Principal environmental stresses are vibration and humidity; electrical stresses are voltage and current. Operating temperature, resulting from ambient temperature and heat due to power dissipation, is, however, the most important applied operating stress where a semiconductor is otherwise generally operated within its ratings.

Arrhenius' equation

Swedish chemist S. Arrhenius' expression for the effect of temperature on the velocity of a chemical reaction is now widely used to predict the effect of temperature on electronic-component failure rate. It is generally used to derive an acceleration factor A, the ratio of the expected failure rate at operating temperature T_1 to the known failure rate at test temperature T_2 :

$$A = \exp\left[\frac{EA}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \qquad (1)$$

Quantity EA is the activation energy for the expected failure mechanism.
T is absolute temperature (K).
k is Boltzmann's constant (8.6 x 10-5 eV/K).

Defining E_A is obviously critical to the use of the expression. Its value depends on device construction: the materials used and the processes used to combine them. Determining the value of E_A requires a long series of life tests at different temperatures with analysis of failures to identify failure mechanisms. Weibull charts are often used to assist in the processing of the data from such tests. The whole procedure involves many thousands of hours of testing.

We make such investigations into new semiconductor structures, where entirely new processes or materials are involved; as a result activation energies for all commonly-used methods of construction are well documented, and some are given below.

Activation energies for common failure mechanisms

The activation energies for some of the major semiconductor failure mechanisms are given in the Table below. These are generalized estimates taken from published literature and internal reliability studies. In cases where a specific failure mechanism has been more thoroughly characterized for its thermal acceleration, that estimate of E_A should be used.
If no failure analysis data is available, and a reliability estimate is required, an activation energy of 0.7 eV should be used.

Activation energies for common failure mechanisms

Failure mechanism	Activation energy (eV)
Mechanical wireshorts	0.3-0.4
Diffusion and bulk defects	0.3-0.4
Oxide defects	0.3-0.4
Top-to-bottom metal short	0.5
Electromigration	0.4-1.2
Charge trapping	0.06
Electrolytic corrosion	0.8-1
Gold-aluminium intermetallics	0.8-2
Gold-aluminium bond degradation	1-2.2
Ionic contamination	1.02
Alloy pitting	1.77

Humidity

Humidity can have a significant effect on the reliability of some semiconductors. This is especially true where aluminium metallization and plastic encapsulants are used, although the silicon-nitride passivation used on the majority of Philips semiconductors greatly reduces the effect. The Peck model is used to predict the acceleration factor (A) due to the combined action of temperature (T) and humidity (H):

$$A = \left[\frac{H_2}{H_1}\right]^n \cdot \exp\left(\frac{EA}{k} \cdot \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \quad (2)$$

Here, H_1 and H_2 are the humidities associated with temperatures T_1 and T_2, respectively. The values for the other parameters are
n = 3,
Ea = 0.9 eV,
k (Boltzmann's constant) = 8.6×10^{-5} eV/K.

Examples

Figures 1 and 2 of acceleration factors calculated using Eqs (1) and (2) show the reduction in failure rate expected at various operating temperatures compared with those observed during life testing. Note that the temperatures are junction (die) temperatures in all cases.

Thermal Cycling

Thermal cycling induces stresses due to differences in expansion coefficients of the different materials in semiconductor components. The cyclic behaviour of the stresses can cause fatigue effects, leading ultimately to failure mechanisms such as cracking and shift of passivation and metal layers or wire break and bond lift. The degradation due to temperature cycling can be described by the simplified Coffin-Manson equation for low-cycle fatigue effects:

$$A = \left[\frac{\Delta T_{stress}}{\Delta T_{use}}\right]^m$$

ΔTstress and ΔTuse are the temperature excursions during the test and use conditions, respectively. A is the acceleration factor, which relates the number of cycles with ΔTstress to the number of cycles with ΔTuse. The exponent m depends on the failure mechanism (see table below).

Failure mechanism	Coffin-Manson exponent m
A1 wire bond failure	3.5
intermetallic bond fracture	4.0
PQFP delamination/bond fail	4.2
Au wire bond heel crack	5.1
interlayer dielectric cracking	5.5
chip-out bond failure	7.1
thin film cracking	8.4
die-attach Rth degradation	9.35

The model can be used to calculate life times for known failure mechanisms at use conditions, and to compare different stress conditions. The temperature ranges must be corrected for the stress-free temperature range.

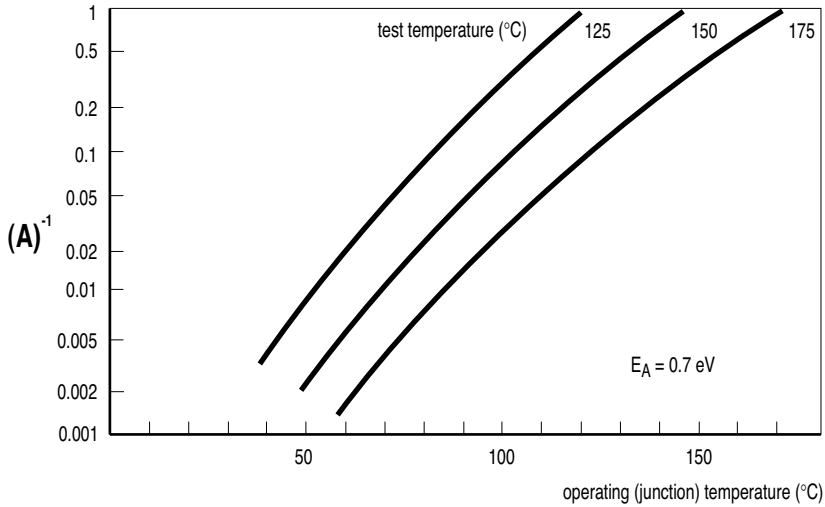


Fig. 1 The effect of reducing temperature on failure rates determined at 125 °C and 150 °C.

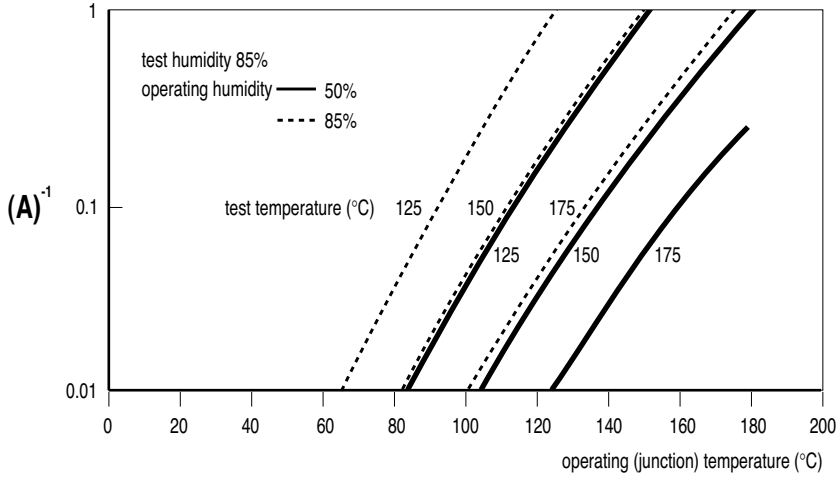


Fig. 2 The effect of two levels of operating humidity on deceleration

Acceptable Quality Level (AQL)

AQL is 'the maximum percentage defective that, for purposes of sampling inspection, can be considered satisfactory as a process average'. AQL is not a licence to ship rejects. It's the basis of sampling systems, which seek to assure a consistent level of quality to purchasers of electronic components.
However, when the quality level of a semiconductor production process is very high, a sampling system to prove this lot-by-lot becomes fairly inadequate and inefficient.

AQL values for acceptance tests

Our standard internal AQLs for Group A tests have been regularly reduced in the past, but we're reluctant to reduce them significantly from their present 0.1% level because:

- sample size increases rapidly for AQLs less than 0.1%. For quantity production, a fixed sampling plan, and level II inspection, the sample size for a 0.1% AQL is 125. However, sample size increases to 315 for a 0.04% AQL. The larger the sample the higher are the administration and handling costs. This is particularly true for visual and mechanical tests.
- our existing average process quality level for many types is already so high that lowering AQLs at acceptance testing will hardly contribute to further improvement.

For these reasons the AQL-system is only used to define the size of the sample used for final check before delivery. No lot leaves our factories if any defect is found in this final check.
Thus, AQL methods are only used to provide assurance that processing errors have not occurred (to avoid rogue lots), and to confirm that our in-process controls are effective and provide data which allows measurement of the PPM level.

Zero defects and PPM

The acceptable defect level can only be zero. Lots with defects are not accepted for delivery and will be 100% retested. The real quality level is not determined by AQL but by PPM (see section on PPM).

AQL

COMBINED SINGLE (S) AND DOUBLE (D) SAMPLING PLANS FOR NORMAL INSPECTION

(see MIL-STD-1050, IEC 410, ISO 2859)

BATCH SIZE AND INSPECTION LEVEL											CODE LETTER	AQL SAMPLE SIZE		ACCEPTANCE/REJECT NUMBER (Normal inspection)																					
26 to 50	51 to 90	91 to 150	151 to 280	281 to 500	501 to 1200	1201 to 3200	3201 to 10000	10001 to 35000	35001 to 150000	150001 to 500000	500001 to Over		SINGLE	DOUBLE	0.010		0.015		0.025		0.040		0.065		0.10		0.15		0.25		0.40		0.65		1.0	
															S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D
III	II		S4 I	S4	S3	S3			S2	S2	S2	E	13	8 16																				0/1	*
	III	II		I	S4		S3	S3				F	20	13 26																		0/1	*		
		III	II		I	S4	S4		S3	S3		G	32	20 46																0/1	*				
			III	II		I		S4			S3	H	50	32 64														0/1	*				1/2	0/2 1/2	
				III	II		I		S4	S4		J	80	50 100													0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	
					III	II		I			S4	K	125	80 160											0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	
						III	II		I			L	200	125 250									0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	5/6	2/5 6/7	
							III	II		I		M	315	200 400							0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	5/6	2/5 6/7	7/8	3/7 8/9	
								III	II		I	N	500	315 630					0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	5/6	2/5 6/7	7/8	3/7 8/9	10/11	5/9 12/13	
									III	II		P	800	500 1000			0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	5/6	2/5 6/7	7/8	3/7 8/9	10/11	5/9 12/13	14/15	7/11 18/19	
										III	II	Q	1250	800 1600	0/1	*			1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	5/6	2/5 6/7	7/8	3/7 8/9	10/11	5/9 12/13	14/15	7/11 18/19	21/22	11/16 26/27	
											III	R	2000	1250 2500					1/2	0/2 1/2	2/3	0/3 3/4	3/4	1/4 4/5	5/6	2/5 6/7	7/8	3/7 8/9	10/11	5/9 12/13	14/15	7/11 18/19	21/22	11/16 26/27		

According to MIL-STD-105D

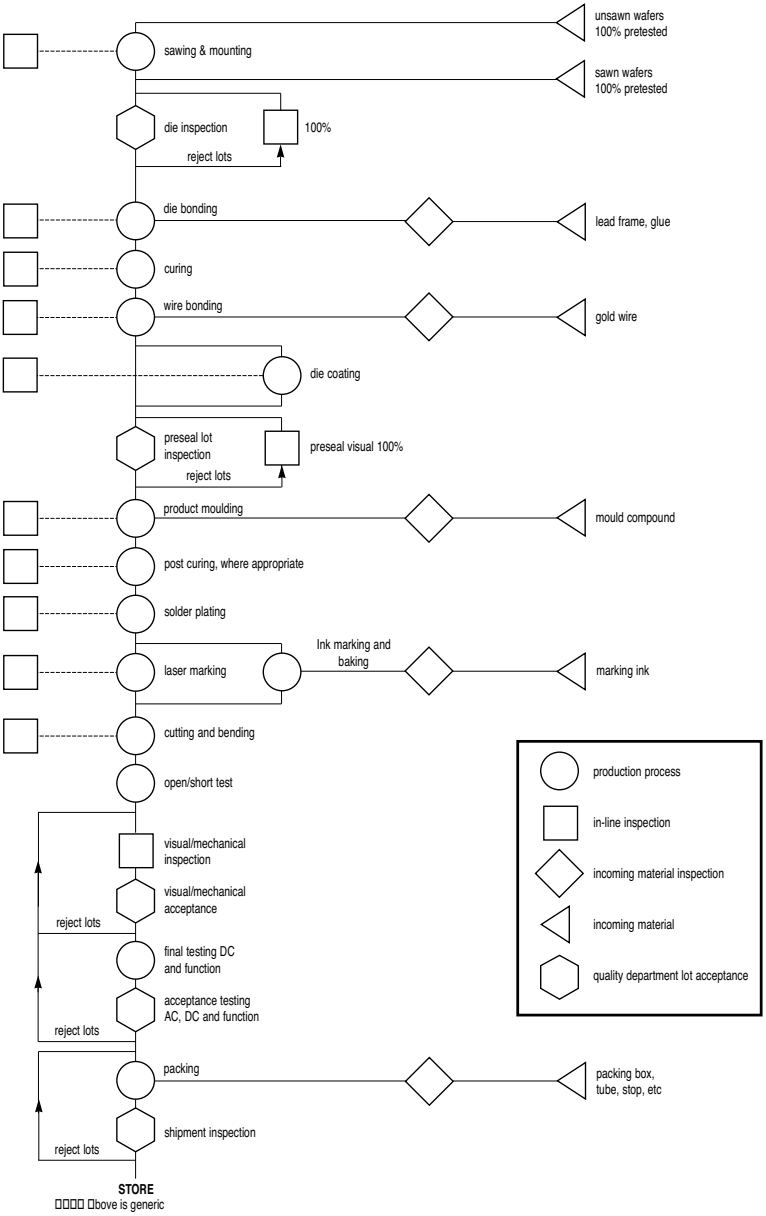
Use first sampling plan below arrow. If sample size equals or exceeds lot or batch size, do 100% inspection.

Use first sampling plan above arrow.

0/1 means 0 = acceptance number/1 = rejection number etc.

* use corresponding single sampling plan.

Assembly quality control



Automotive Quality System Standards

QS-9000
The QS-9000 Quality Systems Requirements (QSR) were developed by the Chrysler, Ford and General Motors Supplier Quality Requirements Task Force. They outline the automotive customer quality requirements for suppliers of automotive parts. Before the standard was developed, each automotive manufacturer had developed its own expectations for supplier quality systems, and the associated assessment documents.

The last issue of QS-9000 (Rev. 3) was issued in 1998. It followed requirements followed a similar structure to the ISO 9000:1994. With the QS-9000 requirements, a joint Quality System Assessment document was issued.

Fulfilling QS-9000 requirements means compliance with a number of linked documents:
- Failure Mode and Effects Analysis (FMEA)
- Statistical Process Control (SPC)
- Advanced Product Quality Planning and Control Plan (APQP)
- Production Part Approval Process (PPAP)
- Measurement System Analysis (MSA)

After December 15 – 2003, no new QS-9000 certificates were issued and no more revisions of the standard were published. Existing certificates could be valid until December 15 – 2006.

ISO/TS 16949
In the late nineties, the International Automotive Task Force (IATF) was formed with the mission to develop a global standard for automotive quality systems. The task force is a cooperation between ISO and representatives from the North American and European Automotive organizations.

Next to the "big three", the following European organizations were represented: ANFIA (Italy), VDA (Germany), CCA/FIEV (France) and SMMT (UK).

The first document was published in 1999 and was called ISO/TS 16949:1999. It used the ISO 9000:1994 structure. At that time, ISO/TS 16949 registration was optional, as an alternative to QS-9000. On March 1, 2002 the second revision was issued, based on the ISO-9000:2000 structure.

Organizations which are QS-9000 certified and want to continue their automotive registration, should have transferred to the new norm by December 15, 2003, the same deadline as for ISO 9000:2000.

In contrast to ISO, the IATF has an own accreditation body, the International Automotive Oversight Bureau (IAOB). This organization controls the Certification bodies that are authorized to do 3rd party certification audits according to ISO/TS 16949:2002.

ISO/TS 16949 requirements for the semiconductor industry
Specific semiconductor requirements are not included in the ISO/TS 16949:2002 standard and some of the requirements for mechanical parts are not applicable to the semiconductor industry.
For this reason the Automotive Electronics Council (AEC) issued a document to provide the appropriate automotive quality system requirements for the semiconductor industry.
This document is called: "Quality Management Systems, Customer Specific Requirements ISO/TS 16949:2002 Semiconductor Commodity, for use by Semiconductor Suppliers".
The document is usually called "The Semiconductor Supplement". It was issued on March 1, 2003. The numbering system follows the ISO-9000 and TS 16949 structure.
Although compliance to the requirements is requested by a number of our automotive customers, the document is (currently - Nov 2004) not yet approved by the IATF.

Automotive quality system standards in Philips Semiconductors

Our policy with respect to automotive quality system certification is that the following units should apply for 3rd party certification according to ISO/TS 16949:2002

- All shared resource manufacturing operations (Assembly & Test, wafer fabs),
- The Business Unit MultiMarket Semiconductors
- Business Lines supplying to the automotive industry: BL Car Entertainment Systems and BL Identification.

Next we ask all these units to comply with the "Quality Management Systems, Customer Specific Requirements ISO/TS 16949:2002 Semiconductor Commodity, for use by Semiconductor Suppliers". Compliance to this document will be verified through internal audits.

Preferred external wafer fabs and assembly & test subcontractors should be certified accredited to ISO/TS 16949:2002.

3rd party certifications are usually done on site level and combined with ISO-9000 audits.

The table on page 119 of the chapter "ISO-9000" shows the ISO/TS 16949 certification status of all involved units. All certificates can be downloaded from Intranet.

BEST is the Philips way to Business Excellence. The BEST program was launched on July 6, 1999 by Mr. C. Boonstra and reconfirmed by Mr. G. Kleisterlee in May 2001.
It is a management process that drives the company to world class performance levels through improvement and alignment of all business processes.

The basic Business Excellence Model

BEST presents the way we improve which starts with the way we manage. The Philips Business Excellence (PBE) Management model - an exact copy of the European Foundation for Quality Management (EFQM) Excellence Model - provides the complete integrated and common framework across Philips of how we manage our business.
It is the backbone behind improvement in Philips. PBE has a total of nine criteria, but can be summarized by the following three:

Leadership
Leaders define the goals and show direction. They set the priorities, lead by example, inspire commitment and manage the overall process. This holds for management in general but is especially true for managing improvement.

Processes
Sustainable excellent results cannot be achieved by luck. They will only be achieved consistently with world-class processes that deliver outstanding results in a predictable way. Processes must therefore be robust, simple and dynamic - they need to be adaptable to changing business requirements and improve over time.

Results
Great companies achieve great results on a sustainable basis. Measuring all the business´ results - not only financial performance - is critical in determining how far we are on the road to business excellence. These results are measured by our customers, our employees, society at large and of course, the financial community.

The BEST Management Process

Whilst PBE provides the backbone, BEST is the overall improvement framework. The acronym BEST emphasizes three main characteristics:

- **Business Excellence** (the ´BE´ in BEST) is the goal we will achieve by implementing BEST
- **Speed** (the `S´in BEST) is a key driver for performance improvement. Elimination of non value added work delivers simpler processes which can run faster. Faster processes provide quicker feedback allowing continuous improvement at a quicker pace.
- **Teamwork** (the `T´in BEST) emphasizes that improvement by individuals alone is too slow or even impossible and does not facilitate organizational learning. Teamwork is not only necessary within one´s own business but especially across organizational boundaries.

BEST is executed through a four stage management process based on the
Plan- Do- Check- Act (PDCA) cycle:

Lead and direct
Leaders set direction by determining the mission, developing the shared vision and values, and defining the ambition and business strategy, summarized in a one-page-strategy document which recaps the desired goals and can be easily understood throughout the organization.
BEST elements that fall in this category are:
- Philips excellence policy
- Philips values
- Philips Semiconductors Vision and Mission
- Philips Semiconductors Strategies
- Philips Semiconductors One Page Strategy
- Philips Semiconductors Environmental policy
- Philips Semiconductors Sustainability policy
- Philips Semiconductors Certification policy.

Prioritize and deploy
The business strategy is translated into those success factors destined to make a real performance difference which is expressed in a Business Balanced ScoreCard. Using this tool, management defines related breakthrough improvement programs, sets clear objectives and creates executable projects for which the required resources are allocated.
BEST elements that fall in this category are:
- Business processes
- Key Value Drivers (KVDs)
- Business Balanced ScoreCard (BBS)
- Breakthrough improvement program.

Organize and execute
BEST is about actions, not words. Action is taken in three main ways:
- **Breakthrough improvement projects:** Breakthrough improvement projects: Top-down defined breakthrough projects require leadership, time and expertise of dedicated trained improvement resources, such as Black Belts

- **Continuous improvement initiatives:** Bottom-up improvement as part of everyone's job and carried out by both individuals and teams. The Quality Improvement Competition (QIC) encourages the involvement of thousands of employees in improvements and recognizes their initiatives and success.

- **Problem solving projects:** rapid response teams solving immediate specific problems - part of the ongoing business improvement efforts.

A standardized methodology guides a team through each stage of process improvement. Training is provided to support the improvement program so that the necessary knowledge, skills and tools are acquired and also applied to other projects.
BEST elements that fall in this category are:
- Top Must Do actions (current year initiatives)
- Breakthrough projects
- Leadership Teams
- Quality Improvement Competition (QIC)
- Problem solving and prevention
- Knowledge management

Assess and Review
Review should be integrated in all we do to close the loop of learning and continuously do things better. It should be a regular item in project meetings and on management agenda's.

In periodical management reviews the Business Balanced ScoreCard is a key instrument to evaluate actual performance against targets and monitor action plans.

ISO-9000 audits ensure in a solid way the continuous effectiveness of the quality management system. At least once a year all business conduct an assessment based on the PBE model to benchmark their actual way of working and results achieved with world-class practices and performances.

BEST elements that fall in this category are:
- PBE assessments
- Headquarter audits
- Process Survey Tools
- Supplier audits
- Certification program
- PD/BoM Strategy and operational reviews
- PD/BU Business Review Meetings

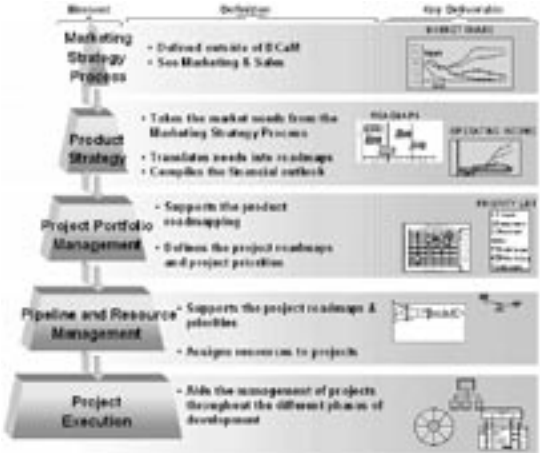
The outcome of this assessment identifies areas for improvement and allows the leaders to provide and deploy associated actions. A special case is where we apply this at the headquarters of Businesses and Divisions to review leadership in implementing BEST through Headquarter Audits.

Regular assessments of key processes through Process Survey Tools provide an additional stimulus for improvement at a more detailed level. As does benchmarking for the most critical processes.

Business Creation and Management (BCaM)

The Executive Management Team (EMT) has identified Business Creation and Management (BCaM) as one of the three key Business processes of the PD Semiconductors. For more details on Business Processes see page 68.
The BCaM program has two main components, the BCaM Processes and BCaM Tools.
Together the Processes and Tools will provide the framework to fulfill the PD's strategic priority to target R&D budget to maximum effect.
Well-defined business creation processes will enable the improved execution, and the tools will form the necessary infrastructure to support and automate the process, to make them easier to adopt and implement. The tools will also help increase visibility to portfolio and projects and will improve communication.

BCaM Process:
The overall structure of the BCaM process is shown in the following diagram:



The BCaM process breaks down into four operational processes:
- Product Strategy. This process interacts strongly with the Marketing Strategy and Marketing Planning processes (part of the Marketing Planning Process)
- Project Portfolio Management
- Pipeline and Resource Management
- Project Execution

Project Execution and a part of the Pipeline and Resource Management process replace the Overall System Realization Process (OSRP).

BCaM contains four common processes:
- Change Control
- Data Management
- Process Management
- Quality Management

BCaM Tools:

This currently covers:

- Portfolio Management
- Pipeline and Resource Management
- Project Execution

For **Portfolio Management** we will find standard solution to pull together the relevant project selection information. The information gathered will help us to make good choices when selecting the projects to support and will help us to identify the projects that will provide the best return for our investment. This will be a decision support tool that makes the process of project selection clearer and which helps to clarify the link between projects and business plans and strategies.

For **Pipeline and Resource Management** and project execution, we have chosen a resource management and project execution tool called SPaRC (Schedule Project and Resource Core) based on Niku 6. It's a standard tool for project, program and resource managers to schedule projects and resources, and track projects in line with the required project plan.

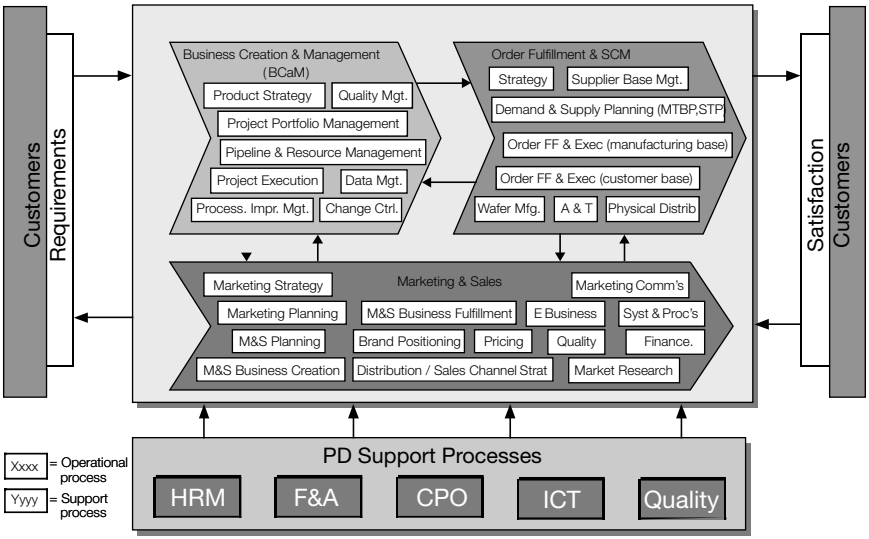
For **Project Execution** we are developing the IMPULSE BCP system to provide functionality for the development cycle and specifically covering product configuration management, product lifecycle management, change management, project deliverable management, document management.

Business Processes

The Executive Management Team has agreed on the following key business processes for our PD:

- Business Creation and Management (BCaM)
- Order Fulfillment and Supply Chain Management
- Marketing & Sales

The following picture shows the high level links between the processes.



Next to the operational processes, we distinguish five support processes:

- Human Resource Management
- Finance & Accounting
- Purchasing
- Information and Communication Technology
- Quality

Chemical content of semiconductors

Awareness in our society concerning the known effects and possible impact on human health through contact with or exposure to certain chemicals has lead to the development of regulations by the EU regarding the usage of certain chemicals in all kind of electrical and electronic application and vehicles.

Examples of these regulations are:

- The Restriction of Hazardous Waste (RoHS) directive, which restricts the use of substances like Mercury, Lead, Cadmium, Hexavalent Chromium and certain flame retardants in consumer product
- The Waste Electrical and Electronic Equipment (WEEE) Directive, which aims to reduce waste and encourage reuse, recycling and recovery
- The End-of-Live Vehicle Directive aims to reduce waste from vehicles and encourage the reuse, recycling and recovery of material from vehicles

The enactment of these directives has lead to numerous questions of our customer base regarding the chemical content of functional units, subassemblies and semiconductor products.

A limited amount of chemical content information was already available to Philips Semiconductors customers. But the company has taken the lead in catering to the new, more stringent market requirements, by rebuilding the chemical content database and publishing the industry's first catalogue on chemical content of semiconductor devices. The information is available to customers via the Internet.

The site was rebuilt using the general database platform, as already used for technical product data (Impuls), and a data collection campaign was started to store as detailed as possible the chemical constituents of the semiconductor products.

The goal of the project is to make this data available, via Internet, before end of 2004. In the meantime the existing database will be available for chemical data enquiries.

Example of output generated from the Impuls database
For 74HC126D/S15

Chemical content of 74HC126D/S15

Type number	Philips package type	Philips package type description	Moisture Sensitivity Level	Total product weight	
74HC126D/S15	SOT108		NA	63.1 mg	

Subpart	**Material group**	**Substances**	**CAS number**	**Mass (mg)**	**Mass (%)**
Mould compound	Antimony & Antimony Compounds	Sb/Sb compounds	1309-64-4	01.88	02.98
	Other	Br/Br compounds		00.94	01.49
		Epoxy resin system		15.36	24.34
		SiO2	14808-60-7	44.53	70.54
		Total		***62.71***	***99.35***
Adhesive	Silver and Silver Compounds	Ag/Ag compounds	7440-22-4	00.28	00.45
	Other	Resin system		00.13	00.20
		Total		*00.41*	*00.65*
		Total		**63.1**	**100.00**

RoHS Compliance

Disclaimer

Complaint processing / CHAMP

Communication is vital

As quality improves, and as our own testing reveals fewer defects, complaints become a very important source of data for corrective action. Moreover, data from complaints provides feedback on quality where it really matters – in the application. It is therefore essential that complaints are correctly routed and handled. Particularly, reject circumstances must be correctly documented, rejects must be analyzed in detail, and the results must be communicated to everyone involved in a short period of time.

Routing of complaints and rejects

(see Fig. 1.)

Complaints from customers are normally received by the customer–contact in the local Sales Office, who will usually send the complaint directly to the responsible Quality Centre. For ICs, this is the Business Line; for discrete semiconductors it's the regional customer support centre.

The rejects are sent from the Sales Office to the responsible Quality Centre by high-speed courier. Where a PPM cooperation exists with the customer, the rejects may be sent directly by the customer.

Information needed for complaint processing

For fast processing of the complaint, the documentation supplied with the rejects should include the following information:

– customer name
– customer-contact
– Philips part number
– lot size
– quantity tested
– quantity rejected
– quantity returned
– traceability code such as Date and Diffusion code
– inspection and test reference number
– purchase order reference
– test temperature
– test equipment
– location of failure (receiving inspection, qualification testing, assembly or field).
– accurate failure desrciption

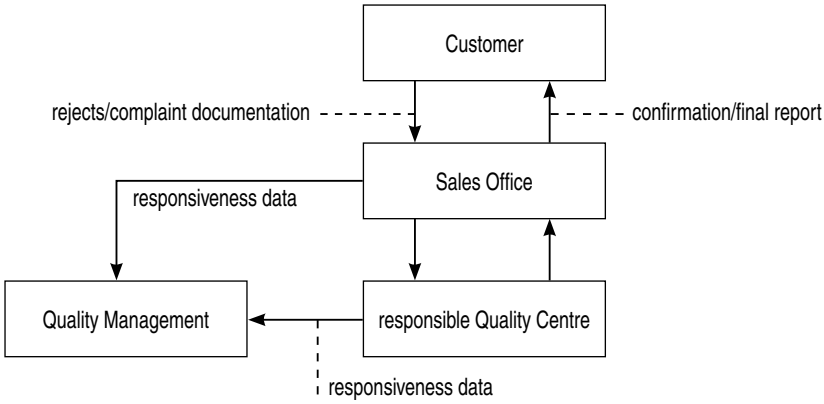


Fig. 1. Flowchart for complaint processing.

Follow-up of the complaint

After verification of the defect the products are further analyzed. It is also possible that the returned parts comply with the specification. In that case the customer is informed and the products are returned to make correlation investigation possible.

Analysis and corrective actions

After verification of the defect, the defective products are analyzed to establish the root cause. Each Quality Laboratory is equipped with sophisticated facilities for failure analysis, and staffed by specialists for identifying failures and failure mechanisms. After the root cause has been established, the 8-D method (see Quality techniques and tools) is used to solve the problem. Step 3 of this method assures containment actions to halt the delivery of further products which may have the identified failure. Steps 6 and 7 ensure that permanent corrective actions are taken to prevent repetition of the problem.

Responsiveness

The complaint procedure determines the information flow and time limits to process the complaint and communicate to the customer. Receipt of the complaint at the responsible Quality Centre is confirmed within 3 working days. The time to the final report varies between 8 and 15 calendar days, depending on complexity. The elapsed times for the various steps in processing the complaint are recorded and reported as responsiveness indicators to Quality Management.

CHAMP

Traditionally, PD Semiconductors has utilized many different complaint-handling systems, which were independent of each other. Thus one Business Line did not have access to another's system, sharing "lessons learned" was not possible and there was no "one face to the customer". Also Management Overviews (number of complaints, average throughput time etc) were difficult to obtain. To improve this situation, in March 1998 a Project Team was set up to realize CHAMP, which stands for Complaint Handling And Management Program. CHAMP was made operational at the end of 1999.

The purpose of CHAMP is to offer a worldwide accessible common system for the handling of Customer Complaints. "Worldwide" means that all Business Lines, Sales Organizations and Manufacturing Centres will use CHAMP. "Common" means that all information will be in one central database, from the smallest detail to the Final Report which is sent to the customer. With appropriate search functionality a user will be offered the possibility to search for similar root causes and corrective actions.

CHAMP offers the following complaint process flow (Fig. 2) to the users:

- Registration of a complaint
- Routeing the complaint to the responsible Business Line or Manufacturing Centre
- Verification of the Complaint
- Initiating Containment Actions
- Detailed (Electrical/Physical) Analysis
- Initiating Corrective Actions
- Writing the Final Customer Report and closing the complaint.

Around 1000 users worldwide have a direct access to CHAMP. In the longer term, it is planned that selected customers will get access to CHAMP via the Internet to register complaints, to view the progress and to retrieve the Final Customer Report (of course only for their own complaints).

Further information on the progress of CHAMP can

be obtained from the CHAMP website:
http://pww.sc.philips.com/qms/champ/index.htm

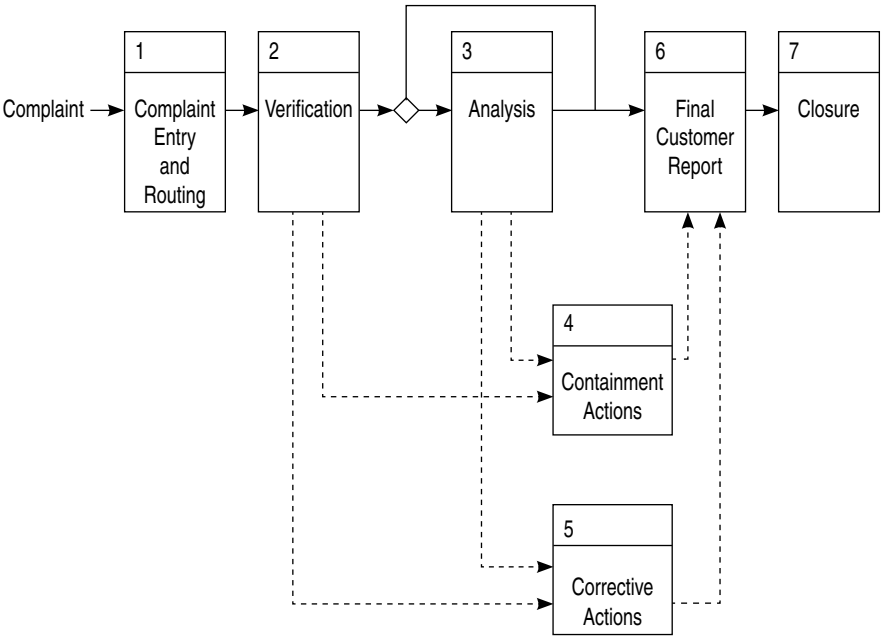


Fig. 2. CHAMP complaint process flow.

Confidence level

Conformity confidence levels

Most of the Quality Control testing of our semiconductors uses relatively small samples since such testing is expensive in time, skilled people, and elaborate equipment. However, it is obviously vital that the results should reflect those that would be obtained from testing larger samples, or whole lots. Statistical methods enable us to set probable limits to the results that would be obtained from testing a whole lot, on the basis of the results obtained from tests performed on a sample. The most common of these methods involves confidence limits.

As with most statistical predictions, it is first necessary to assume a distribution of the test results. For confidence-level calculations, however, this is not the distribution of the results of just one test, but the distribution of the results of a whole series of identical tests (a population).

Once the distribution is known, it is possible to calculate a range of values that, to a predetermined probability, contains the true value (that would be obtained from the testing of a whole lot). This range of values is termed the confidence interval, and the probability of it containing the true value is the confidence level, Fig. 1.

Reliability confidence levels

During evaluation of the results of life (endurance) tests, a correction is used that increases the actual (observed) number of failures to the value at the upper end of the confidence interval. This corrected result, known as the assessed value, is then described as being to a given upper confidence level (UCL): the actual confidence level used being the probability that the true value is not less than the assessed value. The usual confidence level applied to life test results is 60%, although 90% or even 95% confidence levels are also used. (A useful rule of thumb is: to correct a given life-test result to 60% UCL, just add one to the observed number of failures. Thus 0 failures becomes 1. Similarly, 1 failure becomes 2, etc. Actual values are 0.92 and 2.02. The method is acceptable up to 10 failures (11.52 at 60% UCL)). The statistical calculations used to determine confidence levels are similar to those used to derive process averages from Cpk values in statistical process control.

The differences between observed life test results and assessed values to upper confidence limits of 60% and 90% (UCL) are shown in Figs 2 to 4.

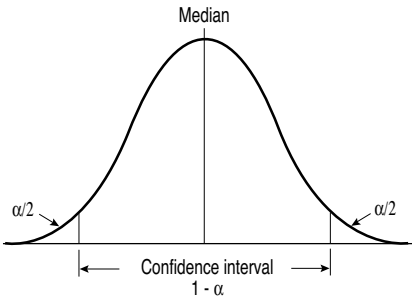


Fig. 1. A typical distribution curve (here Gaussian) with a confidence level (1 - α). Note that quantities α and (1 - α) refer to the areas under the curve. This example is a 'two-tailed' confidence interval, symmetrical about the median. Single-sided confidence levels are also used, especially with reliability data, but with asymmetrical distributions, where α is collected to one side of the confidence interval. Where α is at the high end of the distribution, the associated confidence level is termed the 'upper confidence level' (UCL).

Figure 2 shows that correcting an observed number of failures to a given confidence level shifts the derived failure rate by a constant amount irrespectiive of the number of device-hours testing. On the other hand, Fig. 3 shows that, as the observed number of failures increases in a fixed number of device-hours testing, so the calculated failure rates tend to converge to the observed value. Finally, Fig. 4 shows the calculated 60% and 90% UCL failure rates that could be obtained from tests of various durations on samples from a lot of known failure rate – in this case 10x10-6/h.

These examples show that, to obtain a failure rate close to the real value, the total device-hours testing and the test conditions must be sufficient to generate a significant number of failures. The tests that we use in Group C are carried out under Absolute Maximum Rating (accelerated stress conditions) to maximize failure rates. Even so, it is apparent that, even when no failures are observed, the accumulated results of 2 to 3 years' Group C life testing are required in order to demonstrate that we have achieved our current target failure rate (at Absolute Maximum Ratings) of 10-6/h to a UCL of 60%.

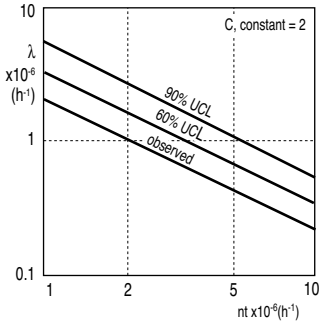


Fig. 2. Where the number of observed failures C is constant, the effect on failure rate l of correction to a given (upper) confidence level is independent of the device-hours of testing (nt).

Although 60% may seem a low value to use for semiconductors, the actual confidence level for a group of devices (in a circuit) increases rapidly with the number of devices. Even for four devices, whose failure rate was calculated individually at a UCL of 60%, the combined confidence level is about 90%, due to the sum of the applied corrections.

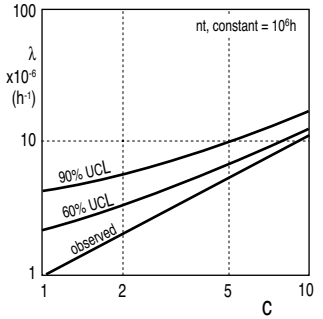


Fig. 3. As the number of observed failures increases, so failure rate λ at various confidence levels converges.

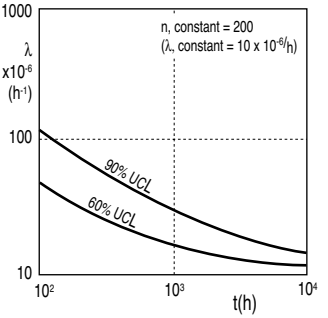


Fig. 4. Here, the true failure rate for a whole semiconductor lot is assumed to be 10^{-6}/h. Even if the sample (here, n = 200) is assumed to be representative of the lot, many device-hours of testing are required before the UCL values approach the real value. Where the correction required for a given UCL results in a large change in failure rate, the confidence band is said to be wide.

Cost of quality

The cost of quality can be a highly significant element of the profit-and-loss statement, particularly in the long term. It is the cost of achieving quality goals. Quality cost reporting provides a means for evaluating effectiveness, and establishing the basis for internal improvement programmes. It is important that quality costs are regularly reported and monitored by management. They should be related to other cost measures such as sales, turnover and added value, and should:

- evaluate the adequacy and effectiveness of the quality management system
- identify additional areas requiring attention
- establish quality and cost objectives.

How is cost of quality defined?

In real terms, the cost of quality is the summation of the cost of conformance and the cost of non-conformance, where the cost of conformance is (prevention costs + appraisal costs) and the cost of non-conformance is (internal failure costs + external failure costs).

So: cost of quality =

(prevention costs + appraisal costs)

+

(internal failure costs + external failure costs).

These costs are defined below:

Prevention costs

(the costs of trying to ensure that we do the work right first time)

These are the costs incurred in preventing the future recurrence of non-conformances. They are directed towards the satisfaction of the customer's quality, reliability and safety requirements in all operations with the first and all succeeding units of product produced.

Typical prevention costs are:

- quality planning in design, manufacturing and quality systems
- process optimization
- quality training
- developing and implementing reliability measurement and calculation methods, quality analysis methods, and quality information systems
- evaluation of vendors, and satisfying customer requirements.

Appraisal costs

(the costs of checking to make sure we did the work right first time)

These are the costs incurred in measuring, evaluating and controlling current production to assure conformance to requirements, including certain costs of related equipment and services.

Typical appraisal costs are:

- planned inspections
- laboratory testing
- process control
- quality audits
- destructive testing
- maintenance and calibration of test, measurement and inspection equipment.

Internal failure costs

(the costs we incur when we discover we didn't do the work right first time)

These are the costs generated before a product is shipped, as a result on non-conformance to requirements.

Typical internal failure costs are:

- scrap of products and materials for quality reasons
- rework or repair
- downgrading
- fault-finding of quality problems in production

- tracing and repair of non-conforming products and materials
- re-inspection and re-test on non-conforming products and materials
- losses caused by downtime
- damage caused by internal transport or storage
- costs of extra handling or storage.

External failure costs

(the costs we incur when the customer discovers we didn't do the work right first time, and demands replacement or compensation)

These are the costs generated after a product is shipped, as a result of non-conformance to requirements.

Typical external failure costs are:

- complaints investigation
- returns
- after-sales costs (free replacements, guarantees, compensation etc)
- damage due to transport (if covered by delivery terms)
- claims because of non-conforming materials or products delivered.

Balancing of quality costs

An important aspect of quality costs is the possibility of reducing internal and external failure costs by investing in prevention and appraisal. As a result, the total quality costs reduce while the quality level improves.
In the quality costs model (Fig. 1) this leads to an economic balance, where the optimum in quality cost is reached.

This optimum is not fixed in time. By continuous improvement (investment in prevention), the manufacturing process improves in time, resulting in a higher quality level at the same cost. In the quality costs model the graph for prevention and appraisal costs should thus get lower in time.

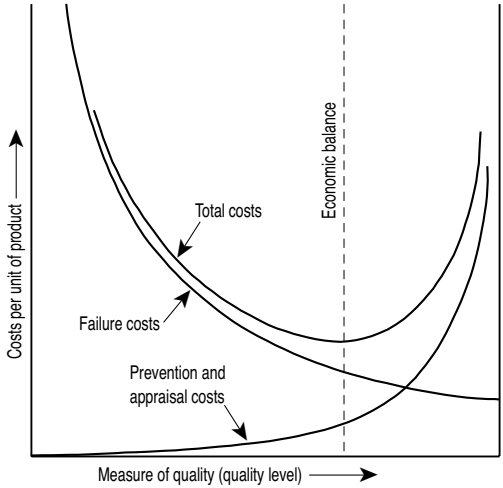


Fig. 1 Quality costs model.

Customer Notification / CPCN / DOD

When Philips Semiconductors products are to be changed or withdrawn from the market, a Customer Notification is sent in advance to the customer. This Notification is sent by the sales representative, either in the form of a Customer Product/process Change Notification or a Discontinuation Of Delivery notification.

Customer Product/process Change Notification (CPCN)

When manufacturing processes are to be changed, customers are notified 90 days before the change, by a Customer Product/Process Change Notification.
Notifiable changes are those affecting form, fit, function or reliability of the product. When customer agreement or comment is invited, there are two stages of Customer Notification: the advance notification and the final notification, respectively 90 days and 30 days before implementation of the change.
The CPCN handling process is described in quality standard SNW-SQ-650. Generation, tracking and sign-off of (advanced) CPCN messages are handled by a web-based tool: the CPCN database (only for internal use).

Discontinuation Of Delivery notification (DOD notification)

When a product is being withdrawn from the market, customers are notified in advance by a Discontinuation Of Delivery notification, which invites the customer to place “last time” orders. Where available, the DOD notification will also indicate the replacement type.
For single-source products the customer is given 9 months prior notification; for multiple-source products the time period is 6 months.
DOD notifications are only sent to customers twice a year, and contain products from all Product Groups within Philips Semiconductors.
Discontinuation of Delivery is also called pruning.
The DOD process is described in quality standard SNW-SQ-651.

Customer-specific labels

Many customers use barcode readers to check the semiconductor product-type at their receiving point and sometimes during assembly. To assist our customers we can supply products with customer-specific labels containing, for example, customer part number, supplier code and/or customer order number. Such labels are applied by regional sales operations, under the control of the regional sales label coordinator.
If a customer requests a specific label, our sales representative will discuss the possibilities with the regional sales label coordinator.
For most requests a label design will already exist, and the regional sales label coordinator will arrange a sample of a suitable label design for customer agreement.
Once the label design has been agreed by the customer, the design is implemented in the customer-specific label system. The customer part numbers and supplier codes are stored (and must be maintained) in cross-reference lists in the computer system for handling customer orders. Varying information, such as customer order number, will be supplied in the order line information. A label program in the warehouse uses this data with the label design code, to produce the label as requested by the customer.
The regional sales label coordinators are:

Europe: Ruud van Leeuwen,
E-mail: ruud.van.leeuwen@philips.com

USA: Cody Nelson,
E-mail: cody.nelson@philips.com

Asia: Jessica M.N. Chow,
E-mail: jessica.mn.chow@philips.com

The customer-specific labeling process is described in quality standard SNW-SQ-407.
The worldwide labeling coordinator is Gijs Lijbers.
E-mail: gijs.lijbers@philips.com

Drypack

If infrared or vapour-phase soldering is used to surface-mount an IC in a large plastic package (QFP or PLCC), vapourization of the small amount of moisture absorbed by the package during storage can increase the internal pressure to such an extent that the plastic cracks.
To provide an immediate solution to this problem of moisture-cracking, these ICs are packed in a resealable moisture-resistant plastic packet called a Drypack.
A Drypack is a laminated plastic packet that maintains the moisture content of the packages of the ICs it contains below 0.1% by weight for up to a year.
It must be stored at a temperature below 40 °C in an atmosphere of less than 90% relative humidity (RH).
The Drypack contains a desiccant and a humidity indicator which allows the moisture content to be checked when the bag is opened.

Using ICs from a Drypack

Before using ICs from a Drypack, it is essential to check the humidity indicator. If it shows RH of less than 10% (the colour of the 10% dot has not changed from blue to pink), the ICs it contains are ready for use. However, to prevent them absorbing moisture after the Drypack is opened, the ICs must be soldered onto a PCB within the period specified in Fig. 2. The times indicated in Fig. 2 apply to ICs awaiting soldering at a temperature of not more than 30 °C in a RH of less than 60%.
If the humidity indicator in a Drypack shows RH of more than 10% (the colour of the 10% dot has changed from blue to pink), the Drypack has been damaged, opened, or stored under too severe climatic conditions. In this case, to eliminate any possibility of moisture-cracking, the ICs contained in the Drypack must be dried (baked) before soldering.
Figure 1 shows the reduction of moisture content as a function of time for some large plastic IC packages. Figure 2 shows a typical Caution label which is on the bag. Table 1 gives the recommended drying times for reducing the moisture content of large plastic IC packages from an initial level of 0.3% by weight to less than 0.05% by weight.

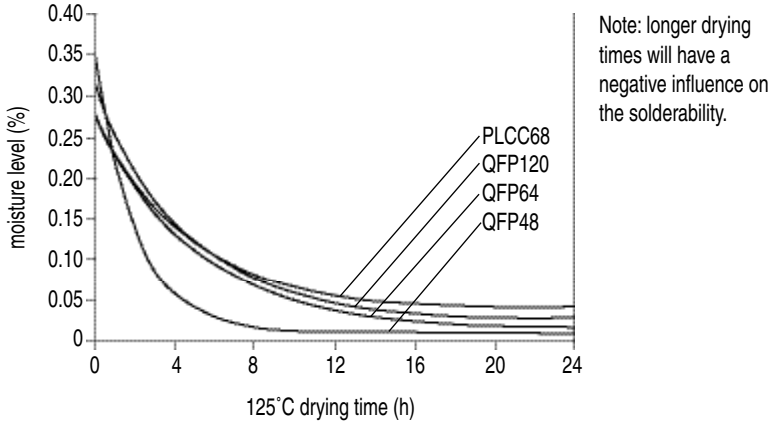


Fig. 1. Moisture content as a function of drying time for ICs in a selection of large surface-mount packages.

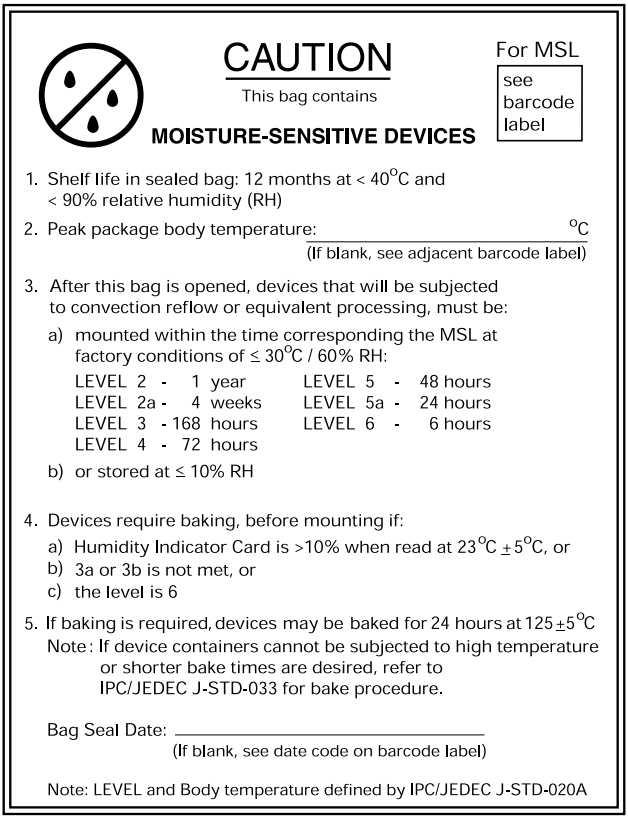
Table 1
Drying times if a Drypack indicates more than 30% RH

Package	Temp. (°C)	Drying time (h)
QFP44	125	8
QFP48	125	6
QFP64, 80, 100	125	10
QFP120, 128, 160	125	12
PLCC44, 68, 84	125	12

Resealing a Drypack

If any ICs from a Drypack are not used, the desiccant and humidity detector should be reinserted and the Drypack resealed within half an hour of opening by using commercially available heat-sealing equipment.

Fig. 2 Typical CAUTION label.



Electromagnetic Compatibility (EMC)

All electrical and electronic products, apparatus, appliances, equipment and installations marketed in European countries must comply with a strict EMC directive. The EMC directive itself does not contain any technical requirements or limits but makes reference to generic or product-specific EMC requirements which will apply for both RF emission as well as immunity.

It is particularly important that electronic products do not cause interference to sensitive receivers, for example lap-top computers in an airplane or cordless telecommunications systems in a car with ABS, air-bags and engine management systems.

The directive means that all our customers (equipment manufacturers, setmakers), independent of the product type they produce: telecom, automotive, consumer, multimedia, etc., must give a declaration of conformity based on type-testing results, either performed by themselves or carried out by a testhouse (third party). In addition, a quality assurance system (ISO 9001) is required for the production centre to guarantee reproducibility referred to the approved sample(s).

Active involvement in the EMC standardization process enables us to be aware of the EMC requirements which will apply to our customers' products within a few years time. We can't wait until one of our customers requests certain EMC specifications for our products, simply because we will be too late by the time the component is required for production.

The scope of the EMC directive is very broad and will have profound effects on the manufacturing industry, and as a result, on their suppliers.

The EMC directive itself actually excludes electronic components from the scope but for most products these will be the cause or victim of interference problems. As a major supplier of electronic components we are aware of this and we are therefore actively engaged in developing EMC-friendly components to anticipate our customers' needs for the future. These EMC-friendly components will help our customer to arrive at an economic application which will meet the European (and other international) EMC norms.

To benefit from these EMC-friendly components it will be evident that a whole system must be developed according to this philosophy. EMC guidelines will come together with these components (in application notes) which will put some constraints on our customer's application. It must be emphasised that EMC-friendly components will still require correctly designed printed circuit boards, filtering and cabling because the final product will be as weak as its weakest link.

To ensure EMC empowerment the following steps are taken:

1. EMC is generally defined in the specification of new components.
2. EMC is taken into account during the product type-approval process.
3. A network of EMC specialists is established throughout the organization.

Both in design and production centres as well as in product concept and application laboratories (PCALs) dedicated support can be given on EMC problem finding and solutions.
We have committed ourselves to help our customers in meeting the EMC requirements at minimum cost and with shortened design-in cycles.

Electrostatic Discharge (ESD)

Damage to semiconductors from electrostatic discharge (ESD) is a major cause of rejects now, and will become an even-greater hazard as device geometries shrink.

Main sources of ESD are dry, clean working conditions, coupled with the universal use of plastics for containers, clothing and work surfaces. Only rigid observance of good working practices everywhere semiconductors are handled – both individually and on boards (including rejects for analysis) – will combat it. ESD prevention is vital to the achievement of low reject levels everywhere semiconductors are used: and to the preservation of the valuable quality-improvement data in rejects.

Experiments indicate that the worst-case electrical model for a person sitting on a chair (the human-body model) is a 100 pF capacitor in series with a 1500 Ω body resistance. Human static potentials can certainly reach 10 kV; under extreme conditions they can exceed 30 kV.

The associated energy level ($^1/_2\ cV^2$) may thus be of the order of millijoules, whereas MOS devices, even with protective networks, can only dissipate 20 microjoule pulses.

Energy pulses due to excessive static charges punch fine holes in the glass layers separating metal film interconnects on semiconductor surfaces. These holes may be lined with metal or silicon vaporized during the discharge, and so provide short-circuits.

ESD IN PRACTICE

In a typical electronics-industry working environment, charges may be generated by machinery operating, plastic storage bins, job instructions stored in plastic envelopes, air blowing over machinery or table tops, and by human motion (especially in some artificial-fibre overalls), Fig. 1.

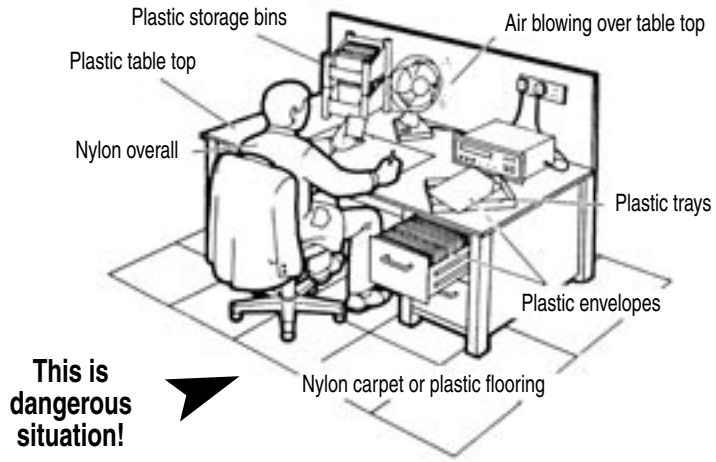


Fig. 1. ESD hazards are everywhere in a normal working environment: especially where modern synthetic materials are widely used. Static charges are invisible, ubiquitous, and destroy semiconductors without warning. Rigorous observation of a few basis precautions can have a dramatic effect on quality levels.

Tests for ESD sensitivity

All tests for ESD sensitivity are based on the discharge of a capacitor through a resistor into the device under test, Fig. 2.

Table 1 gives the circuit values for two test methods:

- machine model (low impedance) – see SNW-FQ-302B
- human-body model (high impedance) – see SNW-FQ-302A.

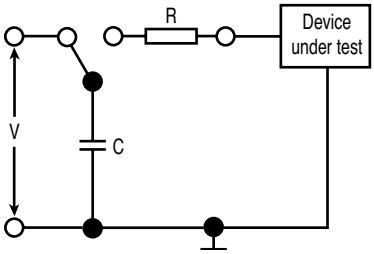


Fig. 2. Circuit for testing the sensitivity of semiconductor devices. Capacitor C is charged to the specified voltage V and then discharged into the device under test through resistor R. Values for both versions of the test are given in Table 1.

Table 1
Circuit values for ESD sensitivity tests (see Fig. 2)

component/ parameter	Philips test method: machine model	Philips test method: human-body model	units
C	200	100	pF
R	25	1500	Ω
V	>200	>2000	V

Note: for machine-model test results to be comparable, residual resistances and stray inductances must be the same.

ESD PRECAUTIONS

The ESD work station

Essential features of a work station for handling ESD devices are shown in Fig. 3. Adaptations for inspection, assembly, repair and other purposes should respect these guidelines:

- conductive work-surface sheet resistance 10 kΩ to 1 MΩ per square metre
- resistor for grounding wrist strap between 0.9 and 5 MΩ. Maximum ground current 2 mA: enough for operator to feel a fault but well below danger level
- all test equipment grounded
- switching transients suppressed
- all metal table trim, support frames and brackets grounded
- cotton working garments
- static-safe rails, bags, foam pads and shorting clips available, if needed.

ESD precautions in semiconductor design

Our semiconductors generally have either intrinsic protection networks (resulting from active junctions) or added protection networks. Protection is, inevitably, a trade-off between degraded performance (clamping diodes limit the operating voltage input range, the added parasitic capacitance reduces speed) and increased security against ESD.

Circuit layout precautions

Designing of a circuit board for ESD-sensitive devices should allow for handling by persons unaware of the ESD hazard. Observe the following precautions:

- Tracks to and from ESD-sensitive devices should not pass board edges, to minimize the risk of their being touched in handling.

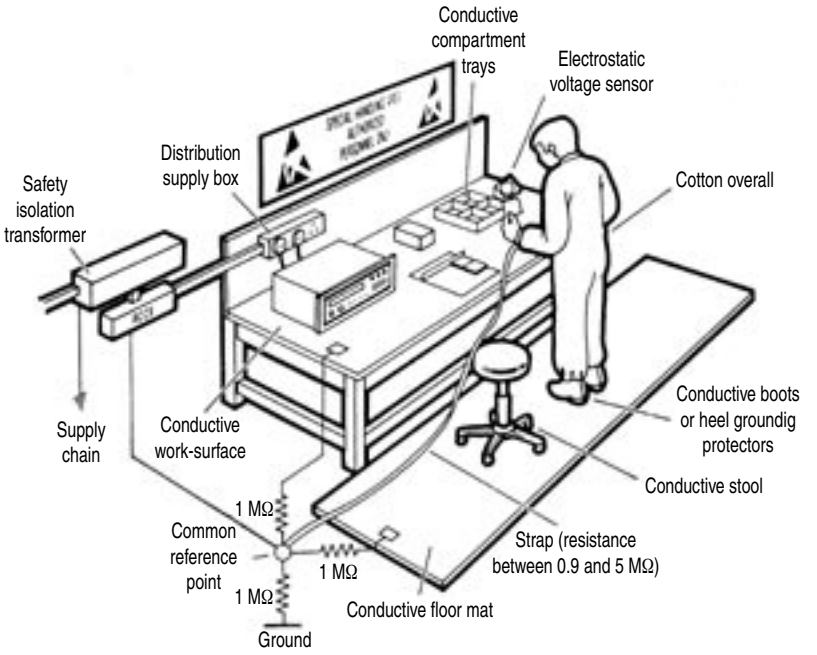


Fig. 3. Essential features of an ESD work station. Variations to suit inspection, assembly, repair and packing should follow the same principles.

- Where possible, connect a resistor of about 1 MΩ between conductors from ESD-sensitive devices and board inputs and outputs.
- Avoid long signal lines; they increase the risk of induced large-signal pick-up.
- Observe the maximum rated values for supply turn-on and turn-off transients. Suppress power supply turn-on and turn-off transients, power supply ripple or regulation and ground noise, to avoid exceeding the Absolute Maximum ratings. Fast zener protection diodes are useful here.
- Label the board with an ESD warning.
- Make sure that the service documentation calls attention to the use of ESD-sensitive devices and the precautions to be taken with them.

Marking of ESD-sensitive devices

IEC 417 and MIL-STD-1686 recommend that the symbol shown in Fig. 4(a) is used to mark ESD-sensitive devices. The symbol should be supplemented by the notice 'ATTENTION – observe precautions for handling ELECTROSTATIC SENSITIVE DEVICES'. Where space is restricted, the simplified symbol shown in Fig. 4(b) may be used. Symbol and lettering should be in black on a yellow ground.

(a)

(b)

Fig. 4(a) Warning symbol for ESD sensitivity according to IEC 417.
4(b) Simplified version for use where space is restricted.

USER PRECAUTIONS

As a general rule, ESD-sensitive devices should always be handled at an ESD station conforming to Fig. 3. Pay particular attention to stores and inspection areas where personnel may not be fully aware of ESD hazards.

Packing and storage

ESD-sensitive devices are packed in antistatic or dissipative packing material. Conductive boxes protect ESD-sensitive semiconductors from external ESD during any transport and are marked with the fig. 4 symbol. ESD-sensitive devices not supplied in antistatic packing should be returned to the supplier. ESD-sensitive devices should be stored in their original packing, preferably in a cool place set aside for the purpose. Do not unpack them until they are required for incoming inspection or use in production.

Receiving inspection

Do not put ESD-sensitive devices where static discharges can occur, even if they have protective packing. In their immediate vicinity avoid the presence of:

- materials which can develop static charges (see Table 2)
- electrical switching equipment and tools.

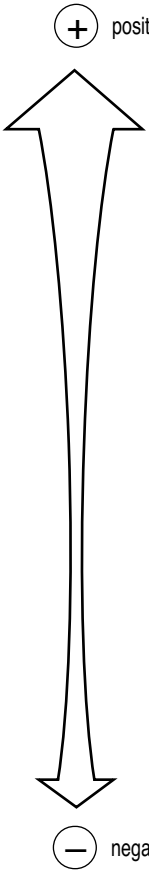
These precautions also apply to assemblies that incorporate ESD-sensitive devices.

Unpack and handle the devices at an ESD work station generally conforming to Fig. 3. Take care that the devices are not exposed to the voltage pulses that can occur when switching the power supply on and off. Increase the supply voltage slowly to its normal value before applying test signals, to avoid the latching effect that occurs when the signal voltage exceeds the supply voltage. During testing, and especially when going from one test to another, ensure that all supplied voltages are under control.

If possible, ground all unused inputs during tests. Do not allow a signal to remain on an input when the power supply is switched off. If necessary, connect a buffer stage between the signal source and the input in such a way that it automatically switches off the signal when the power supply is switched off.

After testing, repack the devices in their original anti-static packing; keeping the warning label intact. Repack at an ESD workstation.

Table 2
Triboelectric series of some common materials



air
hands
catskin
glass
mica
nylon
wool
lead
silk
aluminium
paper
cotton
steel
wood
hard rubber
nickel/copper
brass/silver
gold/platinum
sulphur
Rayon
polyester
Orlon
Saran
polyurethane
polyethylene
polypropylene
polyvinylchloride
silicon
Teflon

Assembly precautions

ESD-sensitive devices should be the last components to be inserted in a circuit board or system.

Manual insertion: Use an ESD work station.

Automatic insertion: Ground insertion equipment and machinery. Use only tools of conductive or antistatic material.
Use grounded component tongs to remove ESD-sensitive devices from their antistatic packing. Do not remove more components at a time than are immediately required.

Soldering: Attach short-circuit clips to ESD-sensitive devices before soldering them; make sure that the clip short-circuits all leads. Remove the short-circuit clips only after soldering, cleaning and drying.
Ground the soldering iron or bath. Do not solder to circuits that are connected to a switched-on power supply.
Ensure that every work surface on which a circuit board may be placed is provided with a conductive or anti-static sheet big enough to receive the whole board.

Handle boards that contain ESD-sensitive devices as single components. Pack them in antistatic or conductive packing. Label them with an ESD warning. Ground all handling personnel.

Measurement precautions

Place the board, soldered side down, on a conductive or antistatic foam pad to discharge any static electricity. Remove short-circuit clips.
Handle the board only by its edges, remove it from the foam pad for testing. After testing, replace it on the foam pad for transport.

Repair and maintenance precautions

Switch off the equipment in which the board is incorporated before removing a board containing ESD-sensitive devices.

For repair and maintenance use an ESD work station arranged as shown in Fig. 3. Place the board on an antistatic foam pad. Observing the 'Assembly precautions', remove and replace the faulty device. After testing, replace the board in the equipment.

NOTES ON STATIC ELECTRICITY

Electrostatic charge generation

In neutral material, the net charge of protons (positive charge) and electrons (negative charge) is zero. When the surface of one material is rubbed along that of another, local (frictional) heating can transfer energy to the electrons near the surface in excess of the Coulomb binding energy. Such electrons may leave their outer valence orbit and be trapped in an outer valence orbit in the other material. Thus two ions will be formed:

- positive, for electron-donor material
- negative, for electron-acceptor material.

Friction between any two surfaces involving at least one non-conductive material is a potential generator of electrostatic (triboelectric) charge; the magnitude and polarity of the charge depends on:

- the materials involved. Charge magnitude and polarity depends on the sum of the separations from the neutral boundary of the two materials in the triboelectric series (Table 2)
- frictional heat, which depends on speed and applied force
- surface conductivity. Part of the charge may be drained off during and after rubbing, inhibiting build up of maximum possible voltage, but this is true only for surface conductivities below 109 Ω per surface square.

A grounded operator cannot drain charge from a non-conductive object. Thus, an operator's clothing may be charged even though his body is grounded by a conductive wrist strap. Similarly, charged plastic boxes or trays will not be discharged by a grounded operator or bench top.

Induction

Static charges can be transferred by induction; that is, without direct contact. Objects which can transfer charges by induction include the plastic boxes, trays and covers used extensively in production lines. An ESD-sensitive device charged by induction can be damaged if touched by a grounded operator.

Removing static charges from insulating materials can only be achieved by use of ionizers.

Limitations of anti-static agents

Anti-static agents – conductive sprays – are commonly used to protect against ESD. Although they do protect against charging by friction, they do not form an effective shield and therefore give no protection against charge induction. The only sure protection against charge induction is a Faraday cage shielding the protected object from all possible sources of induced charge.

Static detection and prevention equipment

A wide range of commercial products is available to help detect static electricity, equip work stations and prevent ESD. They range from conductive bags, gloves, mats, foam, wrist straps and boxes, through to static voltmeters, ionizers and ESD simulators. Careful use of available products can help locate and prevent ESD hazards, and so improve quality wherever semiconductors are used.

Environmental care

Environmental care is an integral part of the business policy of Philips Semiconductors. It is based on four principles:

- sustainable development – development of products and processes that have minimum effect on the quality of the environment today and in the future
- prevention is better than cure
- the total effect on the environment counts – embodied in the development of products whose production (including energy use), operation and disposal at end-of-life have minimum adverse effects on the environment
- open contact with the authorities and customers.

Commitment to these four principles by Philips Semiconductors leads to a specific programme of objectives and targets and to the allocation of capacity. Programmes and progress are reviewed annually.

Environmental planning

The plants develop an annual environmental improvement plan, based on evaluation of the environmental effects of their activities and services under normal and abnormal operating conditions, and on the corporate and divisional programmes. Philips Semiconductors long-term programme is based on Philips Ecovision programme, and consists of targets for manufacturing processes and for products. From these long-term targets the annual PD goals are derived and set.

The plants report annually on the progress of their environmental improvement plan, and the PD summarizes the plant progress in a Philips Semiconductors environmental report.
The chemical content of Philips Semiconductors products is registered in a database. This data is maintained by the local MISD groups based on information supplied by the development departments at RFS (release for supply).

Legal requirements

The Corporate Environmental & Energy Office arranges the collection and recording of applicable regulatory and European legislative requirements pertaining to environmental aspects.

The local laws and regulations are recorded by each National Organization and communicated by its Environmental Coordinator to the plants within his organization.

PD Semiconductors targets 2002-2005

Process improvement

- energy saving: efficiency improvement 20%
- waste: recycled amount 70%
- water consumption: 20% reduction of intake
- emissions to air/water:
  – cat 1 eliminate
  – cat 2 ALARA as low as reasonably achievable
  – cat 3 10%.
  (reference year 2001).

Product impact

- green product marketing
- products eco-designed based on green focal areas: 100% by 2005.

Certification of the Environmental Management System

All Philips Semiconductor plants have an Environmental Management System which has been certified according to ISO 14001.

Eco-design

By adopting Eco-design principles, Philips Semiconductors constantly strives to develop products that improve functionality and minimize the environmental impact through all stages of the product lifetime, from source material, through the manufacturing process and working life to the end of its useful life. In order to facilitate the ecodesign process, five green focal areas have been identified:

- weight and material content
- presence of hazardous substances
- energy consumption in application
- recyclability
- packing materials and weight.

Each BL should set targets for these green focal areas e.g. x % reduction in energy consumption in the application compared to its predecessor and y % packing materials reduction.
A product is ecodesigned when during the design process attention is given to these green focal areas and evidence of this process can be found in the product release report, even if the targets are not achieved. This means that ecodesign indicates an effort commitment. If the targets are met, this could mean that a Green Flagship (see Green Flagship products) is created.

Lead-free products

Understanding all the potential risks of going lead-free is the key to ensuring our future success. By thoroughly addressing the following issues, we're confident that a lead-free future is just around the corner:

- forward compatibility - ensuring that new lead-free products meet customers' requirements
- backward compatibility - ensuring that current products can be used with lead-free technologies
- requalification of current products
- reliability - the ability of our devices to cope with higher temperatures.

With many years of experience in using pure tin to coat package leads/terminals, we know that tin is the logical choice for a drop-in replacement for those devices currently using lead-alloy coatings. We have studied whiskering with tin finishes, focusing on the leads of surface-mount devices and the results are encouraging. Extensive testing for all packages is now underway.

The proposed lead-free soldering process is SnAg3.8Cu0.7 (SAC) eutectic solder for general-purpose applications. In wave soldering, this would entail a bath temperature of 260 °C and a contact time of about 3 seconds. For more details see brochure 9397 750 08118.

ODC-free

In the elimination of ozone-depleting chemicals from its production processes, Philips Semiconductors can claim major successes. As early as May 1993, all plants had eliminated CFCs (chloro-fluoro-carbons) from their manufacturing processes. This led the way to a complete phasing out of all Class I and Class II ODCs (listed in the 1986 Montreal Protocol) from our products and manufacturing processes in compliance with the US Clean Air Act.

Involving partners

Suppliers and subcontractors, too, form a crucial element of our EcoDesign programme. We require them to be environmentally responsible, to have their own environmental policy and improvement plans and to record environmental information on all raw materials supplied to us. A company-wide system to communicate our environmental requirements to them is now being installed. Future preferred suppliers will also be required to have ISO 14001 certification.

Environmental policy and goals

Philips Semiconductors Sustainability Charter

Philips Semiconductors sees sustainable development as one of the most challenging issues and greatest opportunities of the 21st century. The company is committed to business practice that balances economic feasibility with social responsibility within environmental limits - demonstrating our responsibility to People, Profit and Planet (3P's).

Our Objectives and Long-term Commitments:
Philips Semiconductors' commitment to using technological expertise to improve the quality of peoples' lives shapes a variety of short-term goals. Whilst striving for continuous improvement on this basis, the business is also shaped by more long-term commitments. Philips Semiconductors is striving to become impact neutral, by exploring technologies leading to:

- Zero waste – reuse or recycle all our waste materials
- Closed loop – conserve natural resources by integrating our products and processes in the recycling loop
- Negligible global warming gas emissions
- Zero hazardous-substance emissions – eliminate emissions that adversely impact the environment
- Zero work-related injuries

Our Principles:
A key goal of the Sustainability Charter is the pursuit of sustainable development requiring us to monitor and improve our economic, social and environmental performance, then continuously reduce impacts towards zero whilst creating value. To do this, Philips Semiconductors uses the following principles:

- To interact with the environment and society with the utmost care and respect.
- Work to and where possible beyond legal and governmental standards and internal requirements, proactively striving to raise the bar within the industry.
- Recognize our responsibility to provide for future generations, balanced with the realities of competing in a global economy.
- Communicate our performance to stakeholders in an honest and transparent way.
- Co-operate across traditional product, market and sector boundaries maintaining dialogue in an open manner.
- Adopt a Life Cycle, holistic approach minimizing all environmental and social impacts from raw materials, manufacturing, use and disposal.
- Design out problems before they are created, recognizing that prevention is better than cure.
- Develop our people to utilize their creative and entrepreneurial skills and ensure both parties maximize their full potential.
- Educate stakeholders on sustainability practices and positively promote the sustainable development of our company, society and economy.
- Continuously improve across all three domains of sustainability and constantly work to minimize our impacts and maximize value.

The PD EcoVision program

Tough environmental targets have been set that take us beyond the levels we recently achieved under the previous EcoVision program. Although we are finally responsible for our performance, this can be significantly influenced by our suppliers. For example, the power requirement for the equipment we purchase and operate, accounts for a huge part of our total energy requirements. Purchasing departments have to be aware of this influence and need to incorporate environmental issues into their daily practice.
A maturity grid for "Purchasing and Supply chain management" is introduced.

- All Purchasing departments should reach level 8 by the end of 2005

For the period of the program (2002-2005), the following minimum goals have been set for our manufacturing plants:

- Reduce energy consumption by 20%
- Reduce water consumption by 20%
- Recycle 70% of our waste
- Reduce environmentally hazardous substances emission to as low as reasonably achievable (ALARA –principle)
- Reduce environmentally relevant substances emission by 10%.

The reference year is 2001. For our waferfabs specific "absolute" targets have been set.
New product development

- 100% of new products to be Eco-designed
- 1 "Green Flagship" per BU per year.
- In the ecodesign maturity matrix level 8 should be achieved

Businesses are required to ensure that all new products are created according to Eco-design principles, which are a mandatory part of the OSRP (Overall System Realisation Process) used in all development groups.

A maturity matrix for development groups has been developed. In 2005 level 8 should be reached.
At least one "Green Flagship" (best-in-class product for the industry in a particular product category) per year must be committed to per business unit.

For more information on the PD EcoVision program please visit pww.sc.philips.com/env/

Evolution of quality

The start of quality control

The concept of **Quality Control** originated in World War I. The term 'control of quality' was probably first used in a paper published in 1917, with the first book on the subject appearing in 1922. Quality developed slowly, and largely in isolation between the Wars: statistical methods were introduced to results analysis; sampling methods, already used for census applications, began to be adapted to quality control. The control chart (fundamental to Statistical Process Control) was invented by Shewart in 1924, and described in 1931, laying stress on the cost-effectiveness of the method! Thus, by the end of the 1930s, many of the fundamental tools of quality control were available, if not widely appreciated.

As with many other disciplines, quality control derived enormous impetus from World War II. By 1945, Statistical Process Control had reached an advanced state of development, and sampling methods had largely been standardized (MIL-STD-105 was published in 1950). Since its relationship to cost was, as yet, not appreciated, quality control was still largely regarded as a necessary evil; the people practising it had little status (except when things went wrong).

Quality in decline

As defence production ran down, some of the practices introduced for munitions production, especially that of the independence of the Quality Department, remained – but mainly to satisfy inspection requirements for Government contracts. (Independence soon disappeared, though, when quality practices ran contrary to short-term commercial expediency!). Had it not been for the requirements of Government agencies, quality disciplines might well have declined even further.

Fascination with statistical methods in the West largely eclipsed the original concept of quality control (as a means of defect prevention) for the next 20 years or so. In industry, perhaps the only readily-demonstrable commercial advantage of statistical quality methods lay in the AQL system which reduced inspection (the examination of 100% of items) effort. Since the statistical methods employed allowed customers to verify suppliers' claims, AQL became the basis for quality requirements in purchase contracts of all kinds, both governmental and commercial.

During the period of rapid technological development of the 1960s and early 1970s, the QA Department existed in isolation: its activities seemed to have little relevance to the exciting developments in the products themselves, and less to the process of marketing them. In other words, quality became the problem solely of the Quality Department.

The great AQL race

During the 1950s, AQLs around 1% were usual for the majority of electronic components. As equipment became more complex, with larger component counts, OEMs became more and more concerned to reduce AQLs. It's easy to see why: in TV set production using 500 components per set supplied to an AQL of 1%, there would be an average of 5 defects per set, or 99.3% of sets would be defective. With AQLs of 0.1%, however, the average number of defects would fall to 0.5 per set, and the percentage of defective sets would be down to 40%, with a consequent saving of rectification costs. (Since early failures are related to conformity, there would be fewer problems during the guarantee period, too.)

By the 1960s, with the increasing reliance on complex electronics for defence purposes, the AQL problem was becoming acute. Successful use of automatic assembly techniques also required higher component quality. Moreover, the cost consequences of on defective components being found in finished equipment tends to counter the savings due to automatic assembly.

As a result, during the early 1970s, there was pressure on component suppliers to reduce AQLs still further. However, lower AQLs mean larger samples to be tested, which increases costs for both supplier and user.
Some manufacturers even offered a choice of AQL levels. Lower values were achieved by double inspection or screening to eliminate defective products – in other words, inspecting quality in. As we can now appreciate, this did not improve the real quality of the product: weak products still crept through, to fail on the assembly line or early in the guarantee period. Moreover, the associated costs became rapidly unacceptable.

Wise men in the East...

One of the men active in quality procedure development in the USA during World War II was Dr. W. Edwards Deming. During 1942 and 1943 he published several papers supporting SPC and gave short courses on quality methods at Stanford University. About this time, Deming joined the National Bureau of Census.
In 1948, the Military Government of Japan, then headed by General Douglas MacArthur, carried out a population census, for which purpose MacArthur employed Deming. By this time, the Japanese were already looking for a means of improving their product reputation. In 1950, Deming presented courses in statistical methods of quality control. (The Deming Prize is today the most prestigious quality award in Japanese industry). The Japanese Union of Scientists and Engineers, founded in 1949, organized follow-up courses, employed other top American quality experts (who were glad of a receptive audience), including J. M. Juran in 1954, and founded a faculty of specialized teachers. By the time a licence for the production of transistors had been obtained from Bell Labs in 1955 (on which the Sony Corporation was founded), quality was an accepted management tool.
Looking back, the arrival in Japan of solid-state technology just when quality management was becoming accepted seems almost fateful. By the end of the 1960s, the quality of Japanese goods was already apparent to the consumer. By the mid 1970s, even Western industry was beginning to take notice. By 1980, when there were some 200,000 Japanese managers and engineers trained in SPC, around 40% of workers trained in quality appreciation and methods, and schools taught statistics for one or two years, the superiority of Japanese electronic products was obvious to all.

Awakening in the West

From the mid 1970s, the electronics industry in both Europe and the USA was losing market share to the Japanese so rapidly that it was evident that something had to be done. The various patent protections that had held the line for a while were due to expire, in any case, and this would make matters even worse.
It cannot be said, though, that the development of quality methods had entirely stagnated in the West. Defence requirements, again, stimulated some attack on the growing quality problems. The concept of 'Zero Defects' was introduced (Martin Company, 1961-62), and was widely publicized; and Philip Crosby originated the 'Do It Right First Time' principle while at ITT.

How bad was it?

Those outside the small circle preaching the message of quality during the 1970s probably never really knew how great the difference was between Japanese and Western quality. TV production provides a stark example: in a European TV factory in 1976, the fall-off rate averaged 200%: 2 faults per TV set produced (these were major faults: if minor faults, such as dry joints, were taken into account, the true figure

would have been nearer 1500). Japanese factories had fall-off rates around 1%. (Reliability, although perceived by the consumer as the major problem, only ever differed by a factor of four or five, except for design faults). The cost difference lay mainly in repairing all those faults. To quote the Quality Manager of one offshore Japanese TV factory (in 1979!): 'You can't sell junk, so why make junk?'.

Many of the problems stemmed from the incompatibility of the goals of production and QA. Production strove to manufacture at minimum cost and on time: quality was not part of their brief; neither was it part of the brief of the purchasing department, whose goals were minimum initial cost and prompt delivery. QA had no responsibility for cost or schedules: only for quality. Inevitably, there was always conflict, with QA blamed for holding up production, and production devising ways of deceiving QA. A favourite ploy was to mix good and reject batches after Acceptance Testing to just meet the AQL (which was a licence to ship rejects in practice).

Burying the myths

Initial reactions to Japanese success were really excuses for doing nothing about it (remember?): 'they live on a handful of rice a day'; theirs is a group culture, our workers could never perform like that'; 'wait until they expect a decent standard of living' . . . Eventually, it became obvious that the cost and quality advantage of Japanese goods was due to fundamental differences in philosophy of their design and the circumstances of their manufacture. Delegations from Western organizations started visiting Japan to see for themselves. These visits were of limited value, in practice: the gap in attitude and methodology was too great. Impressions gained could even be misleading: Western obsession with Quality Circles probably delayed real quality improvement by around two years.

Many managers were, in any case, still reluctant to believe that quality begins at the top.

Quality begins with management

Really convincing demonstrations of the importance of quality-oriented management came when Japanese companies started moving offshore; when a small team of key people moved in down the road, or took over a failing business, and, within six months, using the local labour that local management had blamed for their problems, started producing goods with a quality comparable with that of the factory back home.

Meanwhile, at Philips . . .

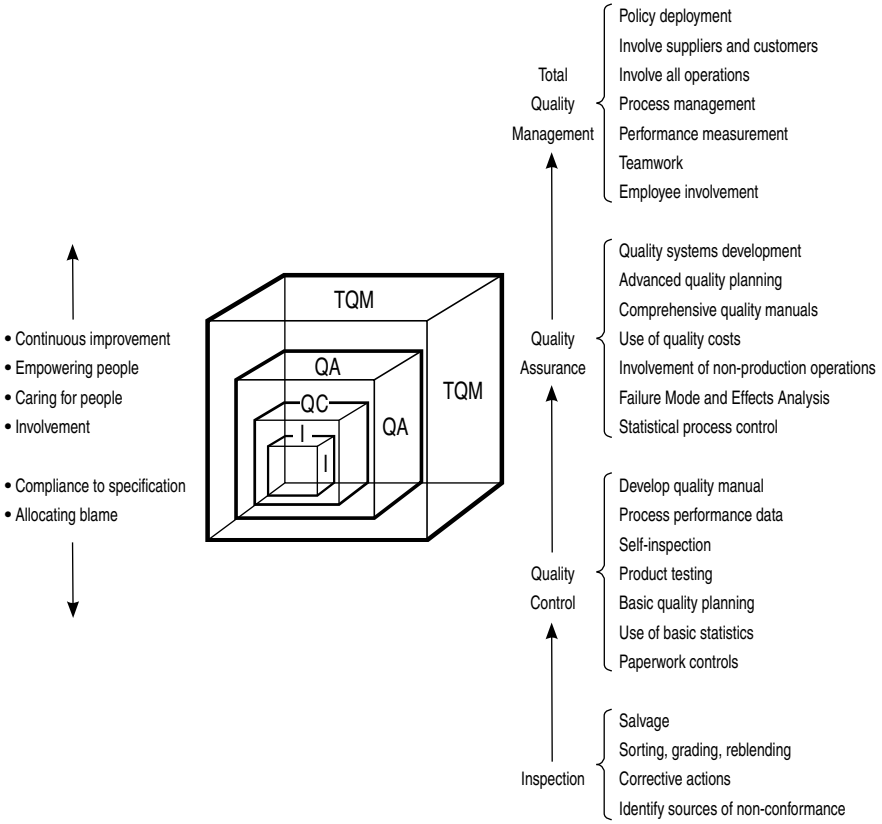
How does Philips semiconductor production fit into this picture? Well, we were ahead of our local competition in formulating, implementing and (as far as we could, honestly) publicizing our Quality Improvement. Serious attempts to improve quality started in the late 1970s, with Signetics a little ahead of the European operations. Early quality-improvement efforts were AQL-oriented, in line with those of our competition, and the requirements of customers.

Attempts to introduce PPM-based quality cooperation relationships with customers met with considerable opposition, mainly due to misunderstanding of the principles and requirements involved. We are, however, fortunate that our internal customers – such as Philips Consumer Electronics – also realized the vital importance of quality improvement, and provided valuable experience in developing in-depth customer-oriented quality-improvement procedures (as Delco did for Signetics). It was evident that education was required at all levels, an activity which has been in progress ever since. CONIM started in 1982, and the 14-step quality-improvement programme with its associated Quality College in 1984.

During this time Statistical Process Control was

introduced and the CWQI programme started.
ISO 9000 was implemented for all manufacturing centres during 1991/1992.
Total Quality Management and customer-oriented quality improvements were introduced in the early 1990s. At present BEST, directed at business excellence, is the Philips-wide improvement program.

Total Quality Management: an overview



External standardization

Standardization is aimed at achieving concensus between the parties concerned.
Internal standardization concerns the standards for parties within Philips.
With external standardization, standards are made with parties outside Philips, to be used either worldwide, for a particular region (e.g. Europe), for national use or for use between industrial organizations.
In the case of semiconductors, the external standardization covers items such as the specification of a semiconductor, test methods, mechanical outlines, symbols and definitions, data elements for quick reference data, protection against EMC and ESD, quality systems, etc.

Worldwide standardization

Worldwide standardization is carried out through the International Electrotechnical Commission (IEC) and the International Organization for Standardization (ISO). The members of these organizations are the national standards bodies.
Founded in 1906, IEC is the worldwide standardization body for electrotechnical and electronic engineering.
Founded in 1947, ISO is the worldwide standardization body for all technologies, except electrotechnical and electronic engineering.
In both organizations International Standards are prepared by technical committees. Draft International Standards, adopted by these committees, are circulated to the member bodies for approval, before acceptance by the IEC/ISO council.
The technical committee for semiconductor technology is IEC/TC47. Philips Semiconductors participates in the following committees and working groups of IEC:

- technical comittee 47:
  Semiconductor devices
- TC47/working group 1:
  Terminology
- TC47/working group 2:
  Environmental test methods
- TC47/working group 5:
  Wafer level reliability
- sub-committee 47A:
  Integrated Circuits
- SC/47A/working group 1:
  Hybrid integrated circuits
- SC/47A/working group 2:
  Logic digital integrated circuits
- SC/47A working group 3:
  Memories
- SC/47A/working group 6:
  Manufacture approval and TQM concept
- SC/47A/working group 8:
  Reliability characteristics
- SC/47A/working group 9:
  EMC measuring methods and test procedures
- sub-committee 47D:
  Mechanical standardization
- sub-committee 47E:
  Discrete semiconductor devices
- sub. committee 3D/WG3:
  Classification of components
- technical committee 91:
  Surface mounting technology

European standardization

CENELEC is a European organization for standardization and certification of electronic components. Many world standards of IEC 47 have their origin in CECC standards. CECC is now part of CENELEC.
Philips Semiconductors participates in the following sub-committees and working groups of CENELEC:

– WG Known Good Dies (KGD)
– WG QAP:
  Quality assessment procedures
– SC91:
  Surface-mounted devices
– TC110:
  EMC standards.

USA standardization

The standardization in the USA is carried out through the Electronic Industries Association (EIA). Standards for electronic devices are made by the Joint Electronic Device Engineering Council (JEDEC).
Philips Semiconductors participates in the following committees:
– IEA/JEDEC Council,
– JC-11 Mechanical (package outline) standardization,
– JC-13 Government liaison
– JC-14 Quality and reliability,
– JC-15 Electrical & Thermal characterization
– JC-16 Electrical interface & power supply standards,
– JC-40 CMOS digital logic,
– JC-42 Memories.

Availability of external standards is described in quality standard SNW-SQ-023.

Failure analysis

Since causes of failure must be defined before they can be remedied, failure analysis is a key element of any quality-improvement activity. For semiconductors particularly, it is also a delicate, complex, time-consuming and, consequently expensive operation. Careful documentation of the circumstances of failure is essential if the results of failure analysis are to be of use. Our complaints procedure is designed both to generate the appropriate documentation and to make maximum use of the results obtained.

Analysis procedures

Rejected semiconductors for analysis may come from our production, customer returns, or field service. All rejects are first given a full electrical test; those that fail (less than 50% for some customer returns) proceed for further examination.

Correlation

Where no defect according to the Final Test Specification is evident, it may be necessary to examine the coverage of the test program to detect any correlation problem; this often requires application-engineering facilities. Where there is a consistently high percentage of good devices in returns, it may be necessary to discuss test coverage and application conditions with the customer.

Examination of defects

In most cases, it is necessary to decapsulate the semiconductor to reveal the cause of the defect. However, before decapsulation, non-destructive methods can be used to gather extra information about the defect. For example, analytical electrical tests can often identify the part of the circuit responsible for the failure, and X-ray or ultrasonic inspection can reveal package defects. Decapsulation without damaging the die or the bond wires, is a delicate operation requiring special chemical etching facilities. Once the interior of the semiconductor is exposed, it can be examined with an optical microscope or a scanning electron microscope (SEM). Many of our centres have voltage-contrast SEM facilities that allow potential distributions across a die to be observed during operation. This is especially useful for examining digital ICs. Another technique uses highly temperature-sensitive liquid crystals to detect hot spots, which often pinpoint the location of a defect. Since a defect can often be hidden under several layers, the semiconductor may need to be deprocessed to allow access to the failure site. This may require a combination of wet-etching and plasma-etching. Several analytical techniques can then be used, such as Auger spectroscopy for powerful surface-analysis. Many of our centres also have EDAX SEM facilities to determine the precise nature of any foreign particles at the failure site.

Reporting results

Failure analysis results are reported fully to the departments concerned, and, where returns are involved, to the customer using the complaints procedure. Failure analysis is the major source of data for corrective action in production.

Failure Mode and Effects Analysis (FMEA)

FMEA is a structured analysis of potential failure modes and their effects, with the aim of reducing or eliminating failures of products or processes. FMEA identifies corrective actions required to prevent failures from reaching the customer, thereby assuring the highest yield, quality and reliability. As a result it reduces the cost of quality, both internally and at the customer.

FMEA has three main aspects:

1. To recognize and evaluate potential failure modes that could occur in the design or manufacture of a product.
2. To identify actions that could eliminate or reduce the chances of the potential failure occurring.
3. To document the process.

For semiconductor devices, it's normal to carry out two types of FMEA:

- Design FMEA, used by Product Design, which addresses potential product failures.
- Process FMEA, used by Process Design/ Engineering, which addresses potential process failures (which could of course cause product failures).

It's important to remember that these two FMEAs are produced independently. The Design FMEA is not a precondition for the Process FMEA; lack of a Design FMEA should never delay work on a Process FMEA.
FMEA is a multifunctional team effort. Its success requires the input of many disciplines such as Assembly, Test, Quality and Marketing.

Timing

The timing of FMEA is all-important. It's meant to be a before-the-event action, not an after-the-fact exercise. To achieve its greatest value, FMEA must be carried out before a design or process failure mode has been unknowingly designed into the product. Ideally, it should be an integral part of the product or process development, carried out between ATD (acceptance for type development) and design approval.

Benefits of FMEA

FMEA offers the following benefits:

- Assists in selecting design/development alternatives with high producibility and reliability potential, during an early phase of development.
- Ensures that all possible failure modes and their effects on the fitness-for-use of the product have been considered.
- Lists potential failures and identifies the relative severity of their effects.
- Provides an instant visual record of improvements resulting from any corrective actions taken.
- Provides a basis for an additional test programme during development and manufacturing.
- Provides historical information for future reference to aid in the analysis of possible failure modes for consideration in intended product/process changes.
- Ensures that the responsible development or process engineer organizes defect-prevention techniques for assessment at final product/ process review meetings.

Documenting the FMEA

This early warning and preventive technique provides the development or process engineer with a methodical way of studying the causes and effects of failures before the design or development is finalized. All aspects of the analysis are recorded on an FMEA form (Fig. 1).

For each identified potential failure mode an estimate is made of its cause, and the likely effect

FMEA	Type/process:	Report no.: Date: Sheet no.:

Function	Potential failure mode	Potential effect of failure	Potential cause of failure	Present				Recommended corrective actions	Resp. person	Rec. end date	Results			
				S	O	D	RPN				S	O	D	RPN

Fig. 1 Typical FMEA form.

on the fitness-for-use of the product. A risk priority number (RPN) is then calculated and assigned to each identified failure mode. RPN is calculated by multiplying together three parameters (S x O x D) where:

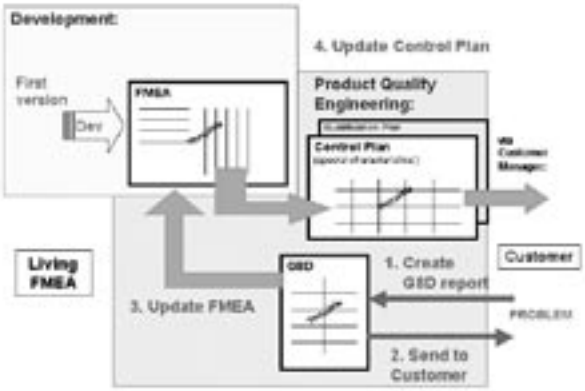
S= **severity** if the failure occurs,
O= **occurrence** of the failure,
D= **detection** likelihood before product delivery.

A value of 1 (low risk) to 10 (high risk) is assigned to S, O and D, so the RPN can be between 1 (low risk) and 1000 (high risk). The resulting RPNs are then assessed, and engineering judgement is used to decide if the risk is acceptable, whether corrective actions are necessary and, if so, what they should be and in what timescale. This information is also recorded on the FMEA form. After any necessary corrective actions have been taken, RPN is again calculated and recorded on the FMEA form, and a judgement is made to ascertain that the new result is acceptable. In this way the form can show at a glance the dramatic improvements that can result from FMEA. The FMEA form is a living document which must be regularly updated to reflect changes in design, process and use of the product.

An Excel format Design FMEA form and a Process FMEA form are available on Intranet. Short instructions for use are available as well.

Living FMEA

The link between FMEA, G8D and Control plan(s) is given in the following sheet. The Development department usually makes the initial FMEA.
In case of problems, a G8D procedure is activated. The result is an update of the corresponding FMEA that in turn, leads to an update of the respective Control Plans. The Product Quality Engineering departments usually perform updates of FMEAs and Control Plans.



Failures In Time Standard (FITS)

FITS is commonly used to express component reliability (see Reliability), and is defined as the number of failures occurring in 1 billion (10^9) hours.
Reliability calculations generally involve considerations of statistics, time and operating conditions.
Consider a group of operating semiconductors. At any elapsed time (t), the reliability R(t) of the group is given by:

$$R(t) = \frac{n_0 - n_f}{n_0}$$

where no is the initial number of semiconductors in the group and nf is the number of failures in elapsed time (t).
However, reliabilty is more commonly expressed as an exponential probability distribution:

$$R(t) = \exp(-\lambda t)$$

where λ, the failure rate, is constant with time.

From these two equations,

$$\lambda = \frac{1}{n_0 - n_f} \cdot \frac{\delta n_f}{\delta t}$$

When averaged over a long period, this approximates to:

$$\lambda = \frac{1}{n_0} \cdot \frac{n_f}{t}$$

And, over the time standard of 10^9 hours, this becomes:

$$\lambda = \frac{1}{n_0} \cdot \frac{n_f}{t} \times 10^9 \text{ FITS}$$

This simple equation is the basis of most reliability calculations. For example, consider a group of 100 semiconductors operated for 3 years under standard conditions, with only 2 failures observed:

$$\text{failure rate } \lambda = \frac{1}{100} \cdot \frac{2}{3 \times 365 \times 24} \times 10^9$$

$$= 761 \text{ FITS.}$$

In practice, we usually need to predict failure rate over a longer period, say 20 years. We can't sensibly test over such a long period, so we use a technique called Accelerated Life-Testing.

Accelerated Life-Testing

In this method of testing, components are made to perform at abnormally high levels of stress to make them fail earlier (earlier failures mean lower testing costs and quicker answers). Extrapolation is then used to convert the short life under severe conditions into the expected life under normal conditions. The same simple equation applies, except that the time t now becomes A x t, where A is the Acceleration Factor (typically between 5 and 150, see Acceleration Factors) and t is the time under stressed conditions. So, under Accelerated Life-Tests:

$$\text{failure rate } \lambda = \frac{n_f}{n_0 A t} \times 10^9 \text{ FITS.}$$

Example: a group of 100 semiconductors have been stressed for 1000 hours in a life test. The Acceleration Factor was 75, and 2 failures occurred :

$$\text{failure rate } \lambda = \frac{2 \times 10^9}{100 \times 75 \times 1000}$$

$$= 267 \text{ FITS.}$$

Confidence levels

From the failure rate determined from sample measurements an estimate of the failure rate of the whole population can be made by expressing the maximum failure rate with a certain confidence level. Poisson statistics are used to calculate conversion constants (see Table) to be used when confidence levels are taken into account:

observed failures	conversion constant at a confidence level of:		
	60%	90%	95%
0	0.92	2.3	2.99
1	2.02	3.89	4.74
2	3.1	5.32	6.29
3	4.17	6.68	7.75

Taking the previous example (2 observed failures converts to 3.1), failure rate (with a 60% confidence level) would become:

$$\text{failure rate } \lambda = \frac{3.1 \times 10^9}{100 \times 75 \times 1000}$$

$$= 413 \text{ FITS.}$$

Hence, with a 60% confidence, we can say that the actual failure rate will be less than 413 FITS. Similarly, failure rate would become:
709 FITS (with a 90% confidence level), or
839 FITS (with a 95% confidence level).

General quality specifications

Philips Semiconductors has issued a set of General Quality Specifications. The specifications will inform customers of our quality assurance system and will maximizing our product and service quality.

These specifications are for:
SNW–EQ-611
General Application Discretes
Power Management and RF Products
SNW–FQ–611
Integrated Circuits

Scope

These specifications relate to particular groups of products, and each identifies particular types of product. The specifications set out parts of the Quality Assurance Specifications that must be used by the technical organization within the Product Centers, suppliers and subcontractors. The General Quality Specifications are in accordance with ISO 9000 and represent the minimum quality requirements.

Overview
The General Quality Specifications define the general procedures that must be used for the development and manufacture of the devices and package outlines specified. They each cover the main aspects of product and process quality and reliability in:

- Development
- Production
- Management
- Defects
- Inspection and test requirements

Development
The related sections outline the general responsibilities of the Development Department and the procedures for product, process and package release.

Production
The related sections outline the quality assurance procedures that must be followed during production. It covers, among other things, incoming and in-line inspection, acceptance testing, quality assessment, special approvals and audits.

Management
The related sections outline the procedures necessary to control the process between the supplier (Development and Production) and the customer. The areas covered include quality indicators and improvement planning, traceability, failure analysis and customer complaints, product or process changes, and customer notification and quality reporting.

Inspection and test requirements
The related sections cover the in-line inspection requirements, Group A tests (acceptance tests per lot), Group B tests (conformance tests per lot), Group C tests (periodic inspection) and Group D tests (qualification approval).

Going completely Pb(lead)-free

Customers and manufacturers are keen to ensure that new regulations in Europe, the US and Far East are complied with, sooner rather than later:

- In Europe, an EU directive on Restrictions on the use of Hazardous Substances (RoHS) includes a requirement tos a.o. elimination of Pb in electronics, in all but special applications, by July 1st, 2006.
- In China, the government is working on bringing in similar legislation to the Europeans.
- In Japan, electronic waste and recycling laws oblige manufacturers to eliminate or recover their waste products containing Pb.
- In the United States, laws banning or restricting the use of Pb are coming for many products and there is an increasing demand for a total ban.

Our industry is focused on Pb-free assembly processes and the related higher temperatures needed for reflow/wave Pb-free soldering.
By investing heavily, we are developing cost-effective Pb-free manufacturing processes that guarantee component reliability. We're also being proactive in finding solutions for devices where Pb is inside the package (e.g. replacing Pb solders in some Multi-Chip Modules/SiPs with new glues).

Tackling the issues

We continue to investigate & address all of the following issues, ensuring full compatibility with new soldering processes, and to introduce Pb-free plated terminals and solder ball connections of all packages:

- Forward compatibility — ensuring "old" products containing Pb still meet customers' requirements and are compatible with both Pb-based and Pb-free solders/PCBs
- Backward compatibility — ensuring "new" Pb-free products can be used with Pb- based technologies
- Re-qualification of current products — updating the portfolio with standardized Pb-free solutions
- Device reliability — coping with higher temperatures in new Pb-free manufacturing/ assembly processes, and ensuring solder-joint reliability using new materials.

Proposed Pb-free soldering process

Based on current research, we advise using SnAg3.8Cu0.7 (SAC) eutectic solder for general-purpose applications. In wave soldering, this would entail a bath temperature of 260 ºC and a contact time of about 3 seconds. Similar alloy would also be used for reflow soldering.
Our temperature profile (see below) for testing products is based on the IPC/JEDEC joint industry standard: J-STD-020.
Our current research indicates that higher soldering temperatures affect a number of surface mount devices. It is advised to keep the package top-body temperature at 245 ºC max.
Work continues to improve the resistivity of the products to high soldering temperatures. In addition, Philips Semiconductors is assessing mechanical stress and fracturing in ceramic and glass components — SAC is stronger than Pb-based solders.

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000
>1.6 mm	260 + 0 °C *	260 + 0 °C *
1.6 mm - 2.5 mm	260 + 0 °C *	250 + 0 °C *
≥2.5 mm	260 + 0 °C *	245 + 0 °C *

Table: Pb-free Process – Package Classification Reflow Temperatures

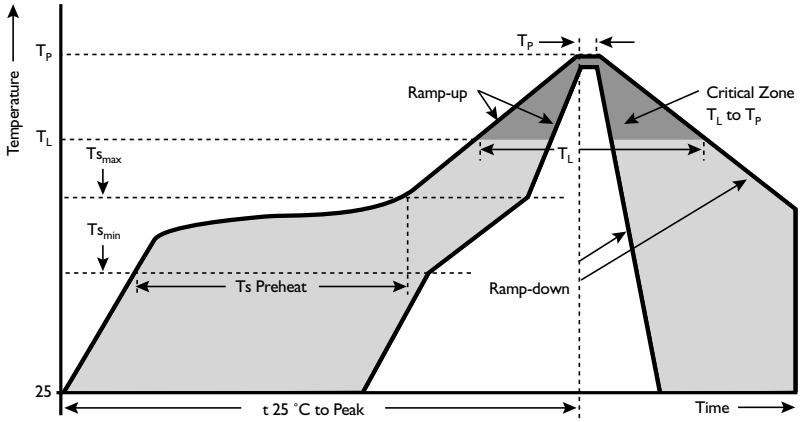


Figure: Classification Reflow Profile

Profile Feature		Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to T_P)		3°C/second max.
Preheat	Temperature Min (Ts_{min}) Temperature Miax (Ts_{max}) Temperature (Ts_{min} to Ts_{max})	150 °C 200 °C 60-180 sec
Time maintained above	Temperature (T_L) Time (T_L)	217 °C 60-150 seconds
Peak/Classification Temperature (T_P)		See Table 4.2
Time within 5° C of actual Peak Temperature (T_P)		20-40 seconds
Ramp-Down Rate		6 °C/second max.
Time 25° C to Peak Temperature		8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface

Industry cooperation

Present soldering and plating technologies using Pb are well established throughout the semiconductor industry. Likewise, the procedures and standards for evaluating quality and reliability are recognized worldwide. Philips Semiconductors is working with other leading manufacturers on a variety of new Pb-free technologies. This is to ensure that the methodologies for measuring solderability, heat resistance and whiskering are consistent, to fairly assess all competing technologies. For further details about this cooperation, please see our website at: http://www.semiconductors.philips.com/green_roadmap/documentation/index.html

Though our Pb-free technologies are based on our current research and experience, we are committed to high performance, quality and reliability, and we'll ensure that our products will continue to delight customers.

Pb-free terminals

With many years of experience in using pure tin to coat semiconductor package leads/terminals, we know that tin is the logical choice for a drop-in replacement for those devices currently using SnPb-alloy coatings. We have studied whiskering with tin finishes, focusing on the leads of surface-mount devices and the results proved successful. Extensive testing for all packages is now almost completed.

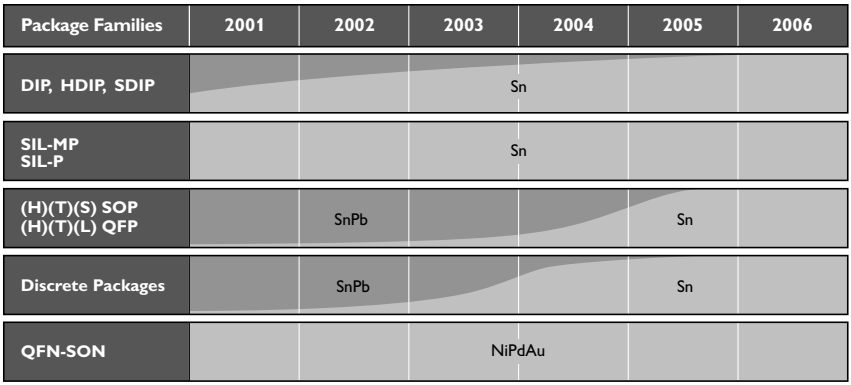
Pure Sn, NiPdAu and SAC offer a very compatible replacement for SnPb alloys and consequently they are our preferred solution. In exceptional circumstances when pure tin is not feasible, we will offer alternative alloys. For the contacts of Ball-Grid Arrays (BGAs), we selected SnAgCu alloy (SAC).

Labeling

Special product labeling will be used to identify Pb-free shipments. If space allows, individual products will be marked with a one-digit code, G, E or N. (G= Pb-free/green, E= RoHS allowable exemption and N= not-Pb-free). Part numbers will remain the same (except new BGA parts, because of their limited backward compatibility) since most customers want part numbers to be kept consistent.
Examples of label marking can be found in the section "Identification labels".

Roadmap

Philips Semiconductors will be fully compliant with new regulations by mid 2005 — well ahead of the European legislation. In fact, more than 95% of our through-hole packages (e.g. DIP, SIL) and over 50% of our surface mount packages (e.g. QFN, QFP) are already manufactured with Pb-free terminals. To check if an individual part is Pb free, go to our website:
http://www.philips.semiconductors.com/ and enter a part number. For our roadmap overview see our lead-free web pages:
http://www.semiconductors.philips.com/green_roadmap/



* Please note that the curves of the graph reflect the general transition excluding Pb allowed by exemptions (medical, telecom, etc)

Green Flagship products

When it comes to developing methods of environmental monitoring that provide a powerful tool for comparing the environmental performance of different products and processes at all stages of their lifecycles, Philips Semiconductors takes a leading role.

But commitment to the environment isn't limited to a single activity or range of devices. Every business line at Philips Semiconductors is actively working to incorporate Eco-Design principles into its products. Our Green Flagship solutions show Eco-Design at its very best, demonstrating how care for the environment combines perfectly with advanced technologies. Some of these products have obvious 'green' benefits, like the AE1000 self-powered radio, which runs off a hand-cranked rechargeable battery, while some have implications which are less immediately obvious, yet highly significant. For example, our in-car navigation systems help drivers to avoid traffic jams, resulting in fewer exhaust fumes and cleaner air for all of us –

engineering elegance from Philips Semiconductors working to protect the natural world. Here are some typical Green Flagship products from Philips Semiconductors:

Less is more

Philips Semiconductors has shrunk a complete circuit board into a single chip. The M-AFRIC (Multi-standard Alignment FRee IF IC) is the world's first IC of this type to appear on the market. M-AFRIC can be used freely without expensive external elements and supports a wide range of I2C-Bus inputs for control of tuner gain, frequency control and related features.

A substantial advantage is the saving in PCB surface, which allows a cost-effective solution for television, VCR and multimedia applications. The alignment-free concept allows the IC to be used in the many different worldwide TV standards (PAL, NTSC, SECAM) and FM radio.

M-AFRIC reduces packaging needs, power, heat and energy consumption due to the reduced size of the IC and the dispensing of the need for external components such as coils, ceramic filters and electrolytic capacitors.

Today's telematics reduce tomorrow's traffic jams

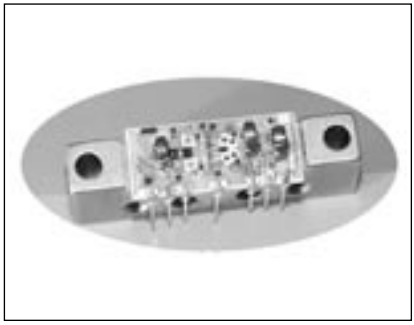
Used in automotive applications, Philips Semiconductors SAF3100 is a basic telematics processor – telematics being the integration of car navigation and infotainment systems. Philips has long been involved in the development of bus technologies, and the SAF3100 telematics processor is specially designed to interface with the in-vehicle CAN bus for communication with other electronic devices in the car.

Reducing packaging, power and cost

The OM6211 is the controlling device for an LCD screen used in cellular phones, and is mounted directly on the LCD-cell by means of flip chip technology. Its area is 35% smaller than the competition's, and 19% smaller than its predecessor (the OM4081 LCD driver IC). It also uses half the power required by its predecessor, leading to reductions in size, power and materials used. The OM6211 eliminates the need for nine external capacitors, reducing the manufacturing costs and power consumption even further. Manufacturers are able to reduce packaging size, cost and power consumption, making the cellular phone cheaper to manufacture and to run. The environment benefits as well as the consumer, with savings in material waste, production and energy.

CATV amplifier module

The CGY887A is a hybrid dynamic range amplifier for CATV systems operating in the 40 to 870 MHz frequency range. It features high gain, superior linearity and extremely low noise, and uses gold metallization to ensure excellent reliability. Operating at a supply voltage of 24 V DC, the ruggedly constructed module comes in a SOT115J package and employs both GaAs and Si dies to deliver all the required functions, minimizing the number of external components.



History of Philips Semiconductors

Philips has been a leader in the semiconductor market right from the start, 50 years ago. In 1991 its semiconductor operations became more focused by the formation of an independent product division called 'Philips Semiconductors'. Since then Philips Semiconductors has become highly successful – the world's 10th largest semiconductor supplier.
So what happened in those 50 years since the invention of the transistor? And how did Philips Semiconductors reach its top-10 position?

Those first 50 years

The invention of the transistor was announced to the press 50 years ago. It was called the 'transistor' because it was a resistor or semiconductor device that could amplify electrical signals as they passed through it ('trans' meaning 'through' in Latin). The announcement did not create much excitement at the time because the device was simply seen as a compact and rugged replacement for the vacuum tube. Even the Bell Telephone Laboratories team of inventors John Bardeen, Walter Brattain and their group leader, William Shockley, viewed it as such. Nobody had any idea what a colossal role the device would play in revolutionising electronics over the subsequent 50 years.

Before the transistor

Prior to the invention of the transistor, Philips' work on lamp technology had led to a broad understanding of materials, vacuum technology and glass processing. The birth of the radio, after the invention of the electronic valve in 1907, marked Philips' diversification into electronics. The first Philips radio valve was made in 1917 and the first complete radio in 1927. It was during the 1920s and 1930s that research took place into X-ray tubes, thermionic valves and, later on, into TV picture tubes and image intensifiers. These developments formed a platform to support the company's continued diversification, for example into the fields of medicine and dental surgery.
In 1924, this research resulted in a portable (!) X-ray system, called the 'Metalix'. Later on, image intensifiers were applied to greatly improve the quality of X-ray pictures. They also increased safety by reducing the strength of the X-ray dosages necessary for examination.
Even during this period, the Company was rapidly becoming a worldwide operation. In 1924 Philips bought a 50 percent stake in the British Company, Mullard Radio Valve Co. Ltd. In 1925 it signed a cooperation agreement with Radio Röhrenfabrik GmbH, and signed a 20-year contract for exchange of know-how, patents and manufacturing rights with RCA of America. In 1932, Philips acquired a 50 percent share of the French company, la Radio Technique. And by 1934, Philips had valve factories in nine countries. From its start in 1918, when a customer in The Hague, the Netherlands, ordered just 180 valves to start up a radio station, the total production had risen by 1933 to an amazing 100 million pieces.

Birth of the transistor

At the time of the invention of the transistor, Philips already had a contract of cooperation with Bell Telephone Laboratories' parent company, Western Electric. This opened up the way to Philips making a contribution to the further development of the transistor. Early Philips reactions were realistic rather than visionary.
A report by the Philips Electron Tubes Division in October 1948 concluded: "If it proves possible to manufacture transistors at a low cost price, with a sufficiently long life, good stability and close production tolerances, it is expected that new applications will be found for such devices where vacuum tubes have so far not proved suitable. In this way, the transistor may become a valuable addition to the electronic tube". Although it was a remarkable prediction in the context of an

apparently endless requirement for vacuum tubes, this professional assessment has since proved to have been very accurate.

Further developments

Two years after the transistor's invention, the first 'grown-junction' transistor was produced. It comprised a sandwich structure and could handle significantly more power than its predecessor. Junction transistors were also made in which small spheres of indium were placed on either side of a slice of germanium and heated until the indium alloyed into the germanium. The alloy process was subsequently replaced by diffusion.
By 1951, Philips had delivered its first germanium-crystal diodes, and in 1952 the first mass-produced transistors left the production lines of a rented building in Nijmegen, the Netherlands. In 1953 a specialized factory was built in Nijmegen to cater for this important new activity. Plants in Hamburg, Germany, and in Micham, UK, soon followed. By 1954, Philips transistors were to be found in radios, and fast-switching transistors were being supplied to manufacturers of electronic adding machines.

From transistors to circuits

Although they were initially more expensive than valves, transistors required no time to warm up and used 90 percent less energy. This made it possible to manufacture more sophisticated products. Electronic circuits could now be much more complex, using more active components, since a transistor was small, cheap, reliable and dissipated much less power than a valve. Soon many more components became available to choose from than had been available in the valve era. They satisfied demand in application domains like radio and TV, and were also used in the early computers for which much larger circuits were required.

New technology

In 1959, diode production at Philips was transferred to Stadskanaal, the Netherlands. In the same year, Philips opened their first transistor factory in Switzerland. Others followed in Brussels, Belgium (1960), and in Klagenfurt, Austria (1961).
Philips' wafer production started in 1962, with silicon slices of 19 mm diameter containing 1,000 transistors. In 1964 Philips produced its first integrated circuit (for a hearing aid) in Nijmegen. The next design was for the extraction of sound information from a TV signal. In 1965, production of ICs for colour television started in Southampton, UK. That same year, the Philips divisions, Electron Tubes, and Industrial Components and Materials, merged to form the Electronic Components and Materials (ELCOMA) division.
It is interesting to note the comparative sales of valves and semiconductors at this stage. In 1953-54, semiconductor sales had amounted to just 1.5 percent of radio and TV valve sales. But by 1958-59 the figure had increased to 23 percent. In 1963-64 it was up to 65 percent and by 1968 it stood at 95 percent.
In 1966, production of consumer ICs began in Hamburg, and Philips also cooperated with various other partners to start a joint venture company called Faselec AG in Switzerland to manufacture ICs for clocks and watches (the Philips factory was added to Faselec in 1969). Also in 1966, Philips Electronic Building Elements (PEBEI) Ltd. was established in Kaohsiung, Taiwan, for the production of ICs. In 1969, Electronic Devices Limited (EDL) was founded in Hong Kong as a joint venture between Philips and T. Zau Sr., to produce discrete semiconductors (EDL became 100 per cent Philips-owned in 1997).
Philips Research had been deeply involved in semiconductor technologies since the early years.

One of its most significant contributions came in 1966 with the LOCOS (LOCal Oxidation Of Silicon) process. It offered a means of improving the isolation between transistors on a chip, resulting in greater packing density. The process is very important for the efficient integration of millions of transistors on one chip and manufacturers all over the world are still using it.
In 1970, MOS (Metal Oxide Semiconductor) IC activities were started in Nijmegen, while further MOS facilities were also opened in Southampton in 1975 and in Hamburg in 1977. In 1974, an IC test and assembly facility was opened in Bangkok, Thailand.
In 1975, Philips acquired one of the pioneering US companies, Signetics, which had wafer fabs in Albuquerque, Orem and Sunnyvale. They produced ICs in bipolar analog, bipolar digital and MOS technologies.

Division renamed

At this point, Philips split its semiconductor activities into two parts – Discrete Semiconductors and Integrated Circuits. In 1988, the Electronic Components and Materials Division, to which both of these activities belonged, was renamed as 'Philips Components'. Philips-owned semiconductor companies in several countries were brought under the Philips banner (e.g. Valvo in Germany, RTC in France and Mullard in the UK). The rebranding was completed in 1992 with the renaming of Signetics.

Mega project

Much of the cooperation going on at this time was in conjunction with JESSI (Joint European Submicron Silicon), the coordinated effort of nine major European IC manufacturers. However, in 1990, Philips decided to withdraw from the so-called 'Mega Project', an initiative by JESSI to produce high-density memories. This decision involved stopping production of 1 Mbit SRAMs at a state-of-the-art IC fab (MOS-3) in Nijmegen. Although the plant had only been completed in 1987, the dramatic fall in memory prices proved the wisdom of that decision and the plant has since become an important production centre for consumer and telecom ICs.

New era

In that same year, Philips was in a financial crisis. Philips Components had become a very large organization. Philips President J.D. Timmer announced a major restructuring programme to bring the necessary performance improvements. As a result of the growing importance of the two semiconductor business units and the decreasing synergy with other activities of Philips Components, a new product division called Philips Semiconductors was born on January 1, 1991. Around one third of the total 75,000 employees of Philips Components transferred to the new division.
The new organization was formed under the leadership of its first CEO, Heinz Hagmeister. It comprised six core product groups: Consumer ICs, Industrial ICs, Transistors and Diodes, Power Devices, Standard Products and Application Products. Regional sales and marketing organizations (RSOs) were announced. The new organization brought many benefits: the amount of logistical and administrative interfacing between countries and worldwide staff departments was reduced; sales forces could concentrate on the business of selling, focusing on major accounts, while the distributor networks enhanced service to smaller accounts. Moreover, rapid and structured market feedback became possible and deployment of policy became quicker and more efficient.

Quality journey

Customers soon began to experience improved service levels, and Philips Semiconductors began to climb back to an increasingly competitive position. All plants were set the goal of certification to ISO 9000 standards, a target that was achieved as rapidly as November 1992. The following year, tough new goals were set and all plants were given the task of achieving the Ford TQE quality standard by the end of 1993. The PD-wide QIC (Quality Improvement Competition) was also inaugurated in that year. Teams from all over the world took part, signalling the involvement of thousands of employees. By 1997, no fewer than 667 teams comprising over 5,000 people participated in QIC. This meant that almost 20 percent of the workforce were actively engaged in the dedicated improvement process through teamwork.

Consolidation and growth

Boosted by a growing confidence, Philips Semiconductors began a period of cooperation and growth that encompassed agreements with other major manufacturers and expansion and renewal at plants around the world. Over the period 1991 to 1996 the Company implemented wafer fabrication capabilities equivalent to 1.25 million 8 inch wafers per year. These came from five new facilities: Caen and Limeil in France, Nijmegen in the Netherlands, Hazel Grove in the UK and Albuquerque in the USA, plus significant upgrades to a further five existing fabs.

In 1991, a new IC and Application Centre was opened in Southampton, UK. And in 1992, a new bipolar ICs fab, built as a joint venture with the Shanghai No.7 Radio Factory, was opened in China. In 1993, a joint venture with Motorola saw the building of a new assembly and test facility for small signal transistors and diodes in Seremban, Malaysia. 1994 saw the completion of a new assembly and test facility in Thailand. And to meet growing demand, a brand new plant was built in the Philippines to house assembly and test facilities for various discrete products.

The first systems laboratory outside Europe was opened in Sunnyvale in 1994, but the biggest announcement that year concerned the investment of 500 million Dutch Guilders in a submicron 8 inch wafer facility (MOS4YOU) in Nijmegen. The plant would feature an advanced submicron process (0.5 micron and below) developed in Crolles near Grenoble, France, in a joint project with SGS Thomson that was started in 1992.

At the end of 1994, an announcement was made that Philips and IBM would cooperate in the manufacture of wafers at IBM's Böblingen facility in Germany, initially producing 0.8 micron line-width logic products. It was a strange coincidence that the two companies should work together 25 years after they worked independently on an important early innovation in IC technology. Called Integrated Injection Logic, this process offered the potential for bipolar circuit speed with MOS circuit density. It was cross-licensed and adopted for use in microprocessors, custom gate-array chips and memories. Today, the Böblingen facility is 100% Philips owned.

In 1996, Philips Semiconductors jointly established a major new software centre in Bangalore, India, together with other Philips product divisions.

That same year, a new international production centre for discrete semiconductors was opened at Cabuyao in the Philippines. Work on building a further test and assembly facility in the Philippines, this time for ICs, was started in 1998 at Calamba, just south of Manila.

Growing customer confidence

Between 1992 and 1995, customers began to reaffirm their confidence in the new PD and scores of supplier awards were won by Philips Semiconductors around the world. In 1993, the

new CEO, Doug Dunn, was able to declare that the year had been a financial success for the PD. 1994 proved to be a recordbreaking year for Discrete Semiconductors. For the first time in its history over 10 billion parts were sold in a single year and sales exceeded 1 billion US dollars. In fact, Discrete Semiconductors made a substantial contribution to the PD's recovery and financial success. 1995 proved to be a record year for the PD. The semiconductor industry was powering its recovery from a recession and Philips Semiconductors grew an unprecedented 23 percent.

Climbing even higher

After another successful year in 1996, Philips Semiconductors returned to the world's top ten semiconductor manufacturers, based on sales. It was seen as the result of hard work.
This sentiment was clearly expressed by its newly appointed third Chairman and CEO, Arthur van der Poel: "Jumping back into the top ten is a just reward for all the hard work put into improving our performance and competitive position by employees across the PD." In 1999 Philips acquired VLSI Technology, with locations in San Jose, San Antonio, Tempe and Sophia Antipolis. In 2000 the Fishkill fab, formerly known as MiCRUS was purchased from IBM. In 2001 the SSMC fab was opened in Singapore as a joint venture with TSMC. In 2002 the discrete assembly site at Seremban, Malaysia (which was a joint venture with Motorola) became 100% Philips owned.

Philips Semiconductors today

New applications have indeed been found for the transistor and the products its invention enabled. Although very hard to detect in everyday life, these little devices play a colossal role in people's lives. And Philips Semiconductors has a solid presence in their application domains.

Now more than one in every three televisions made around the world is based on a Philips Semiconductors' one-chip tv.
One out of every two telephones in the world uses a Philips Semiconductors' line interface IC. And most of today's leading car manufacturers use Philips Semiconductors' car immobiliser technology.

Now, 50 years after the invention of the transistor, Philips Semiconductors is the tenth largest semiconductors supplier in the world. It employs approximately 30,000 people worldwide. Together, they produce around 70 million ICs and discrete semiconductors every day.

Identification labels

The identification label on our semiconductor packing box is a combination of human-readable text and machine-readable information. The label identifies the product, gives traceability and provides additional information. All the information is given in both human-readable and in 2D-coded form, some fields are also given in barcode. The 2D symbol enables all the label information to be read in one action via our traceability information system ROOTS. The 2D code is defined in Data Matrix ECC-200, the barcode is code 39.

What is CODE 39?

CODE 39 derives its name from the structure of each coded character. Each character is represented by nine bars (four white and five black) as shown in Fig. 1. Three of the nine bars are wide (binary value 1), the other six are narrow (binary value 0).
Note that every barcode pattern starts and ends with the unique (*) character. Figure 2 gives an enlarged example of the bar-code pattern representing ABC.

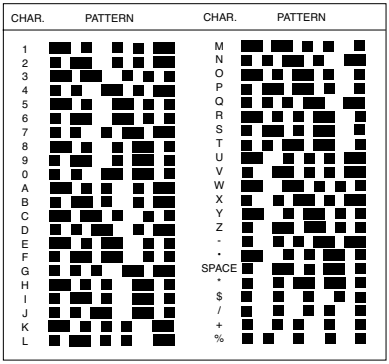


Fig. 1. Barcode patterns of the characters that can be represented by CODE 39.

The ★ symbol denotes a unique start/stop character which must be the first and last character of every barcode.

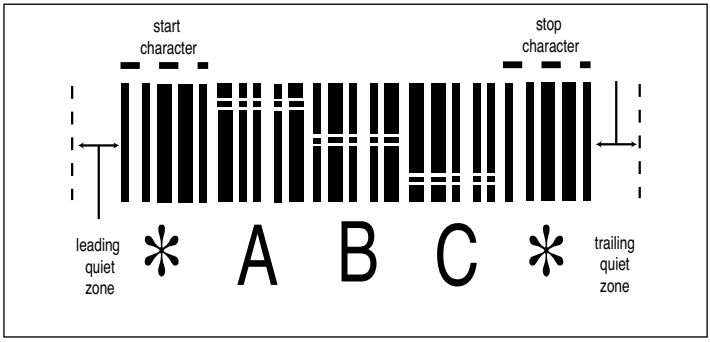


Fig. 2. Barcode representation of the characters ABC.

Philips Semiconductors identification label

One of our identification labels is shown in Fig. 3. The composition of the label is defined in the label standard SNW-SQ-404. The label contains the following data (bottom to top):

- Philips 12NC product code number (CODENO)
- Type number (TYPE)
- Packaging quantity (QTY)
- Production date (DATE)
- Traceability lot-ID (LOT)
- Product origin code (ORIG)
- Product manufacturing codes (PMC)
- Moisture sensitivity level (MSL)
- Country of origin (MADE IN), which can be shown in 2 lines (as in Fig. 3): ASSEMBLED IN / DIFFUSED IN.

It can also contain any of the following data:

- Re-approval date (REDATE)
- Second production date (DATE 2)
- Second traceability lot-ID (LOT 2)
- Customer reference (CUSTOMER)
- Customer-specific information (CUST INFO)
- Additional product information (PROD INFO).

Identification labeling is described in quality standard SNW-SQ-404.

Fig. 3. A typical identification label.

ISO 9000

ISO (the International Organization for Standardization) is a worldwide federation of national bodies. International Standards are prepared by ISO technical committees. Draft International Standards adopted by these committees are circulated to the member bodies for approval before acceptance by the ISO council. The work of ISO covers all fields of standardization with the exception of electrical and electronic engineering which, by agreement, are the responsibility of the International Electro-technical Commission (IEC). ISO 9000 guarantees conformance to specifications and procedures, but does not hamper improvement actions. As shown under Business Excellence (page 12), ISO 9000 is the stepping stone to improvements.

Evolution of the ISO standard

On December 15, 2000, the third revision of ISO 9000 was issued. Compared with the previous (1994) version, the 2000 revision implemented a number of basic changes:

- the new norm is applicable to all organizations delivering any type of product, and is independent of the size of the organization
- the new norm has a wider attention to all aspects of the business
- there is a strong relationship with the benefit, of the stakeholders
- the organization should describe 'how it works' rather than 'what it does'
- the business should be able to show continuous improvement in a closed-loop cycle
- the new norm is more user-friendly and less descriptive.

In the new ISO norm, eight quality management principles have been defined to lead the organization towards improved performance:

- customer focus
- leadership
- involvement of people
- process approach
- system approach to management
- continual improvement
- factual approach to decision making
- mutually beneficial supplier relationships.

In order to maintain certification, organizations should transfer to the new norm before December 15, 2003.

ISO 9000 in Philips Semiconductors

Philips Semiconductors follows the Philips policy that every operational unit should be ISO 9000-certified. In 1991, Philips Semiconductors started a programme for the certification of all Business Lines, Wafer Fabs, Assembly & Test operations, Sales and other operational units in Europe, the USA and the Far East. The programme was completed by the end of 1992 for all Wafer Fabs and Assembly & Test factories and for some support centres.

To obtain ISO certification, each centre is given an initial preparation period, followed by an audit on all aspects of the norm. The audit covers the centre's total organization including management, logistics, purchasing, marketing and finance.

Certification is granted by independent third-party registrars such as DNV, Lloyds, SGS Yarsley or KEMA. Philips has signed volume agreements with the three best-performing registrars. Certification can only be granted after demonstrating that the quality system is in agreement with all the ISO requirements. The registrar will make periodic surveillances to ensure that the quality system is kept up to ISO standards. In general, the following rules are applied regarding Quality systems and Certification:

- quality systems (including quality manuals) are set up according to ISO guidelines for entire organizations such as Business Lines, Wafer fabs, Assembly & Test factories and Technology groups
- certification programmes are usually carried out on site level, where several units are combined.

It is common practice to combine ISO 9000 certification with ISO/TS 16949, when applicable.

Table 1 Philips Semiconductors ISO 9000 certifications

Centre	Certified unit	Expiry date
Bangalore, India	Software dev	February 2005
Bangkok, Thailand *)	IC assembly	August 2006
Beijing, China *)	speakers for mobile	2006
Böblingen, Germany *)	fab ICs	May 2006
Cabuyao, Philippines *)	module/discretes and IC assembly	March 2006
Caen, France *)	plant ICs	April 2006
Calamba, Philippines *)	IC assembly	May 2007
Eindhoven, The Netherlands	Headquarters PD	November 2007
Eindhoven, The Netherlands	marketing and sales Europe + a/p	October 2006
Eindhoven, The Netherlands	Tech Centres Europe	April 2005
Fishkill, USA *)	fab ICs	August 2005
Guangdong, China *)	discretes assembly	July 2006
Hamburg, Germany *)	plant (ICs/discretes)/Innovation Center	May 2007
Hazel Grove, UK *)	power semiconductors	April 2007
Hong Kong, China *)	plastic-encapsulated discretes assembly	December 2006
Kaohsiung, Taiwan *)	IC assembly	June 2006
Nijmegen, The Netherlands *)	plant (IC/discretes)	June 2007
Nürnberg, Germany	Mobile comm	May 2006
PS N.A.	All design and M&S	August 2006
San José, USA	Tech Centres USA	September 2006
Seremban, Malaysia *)	discretes assembly	October 2006
Shanghai, China *)	wafer fab (ASMC)	July 2006
Shenzen, China *)	LCDs for automotive	October 2006
Singapore *)	wafer fab (SSMC)	December 2005
Sophia Antipolis, France	business lines ICs	June 2006
Southampton, UK	business lines ICs/Innovation Center	February 2006
Stadskanaal, The Netherlands	medium-power rectifier diodes	Januari 2006
Sunnyvale/San Jose, USA	ICs and sales	Januari 2006
Vienna, Austria	speakers for mobile	June 2006
Zürich, Switzerland	business lines ICs	November 2006

*) Also certified according to ISO/TS 16949:2002

Note: All centres are recertified every 3 years, prompted through a contractual agreement by the certification body. The certificates are available on Philips Intranet.

ISO 14001

ISO 14001 is an environmental standard published by the International Organization for Standardization. By achieving ISO 14001 certification, manufacturers can demonstrate a dedicated commitment to environmental care.To achieve ISO 14001 certification, a company must set up an Environmental Management System (EMS) to raise the profile of environmental issues throughout its organization and for deciding on quantifiable improvement actions. Essential elements of an EMS are:

- an organization and well-defined procedures for handling environmental issues
- clearly-defined areas of responsibility within the organization and a framework for setting up and reviewing environmental objectives
- awareness of environmental factors plus a clear improvement plan prioritizing actions on reducing environmental impact
- a published policy of continuous improvement on environmental issues.

As with Quality standards, companies must be annually or semi-annually audited by an external certifying body to verify that they are complying with the requirements. Philips Semiconductors history with ISO 14001 goes back to the roots of this highly demanding standard. In fact, our plant in Bangkok, Thailand, was the first in the world to achieve ISO 14001 certification – only three days after the standard was introduced in September 1996. Since then, the story has been one of continuous success, as shown by the Philips Semiconductors ISO 14001 certifications in the table below.

Centre	Certified unit	Certification date
Bangkok, Thailand	Assembly ICs	September 1996
Beijing, PRC	PSS	October 2001
Böblingen, Germany	Waferfab ICs	May 1998
Caen, France	ICs	December 1997
Cabuyao, Philippines	Assembly Discretes	December 1997
Calamba, Philippines	ICs	April 2000
Guangdong, China	Assembly Discretes	August 2002
Hamburg, Germany	ICs/Discretes	October 1996
Hazel Grove, UK	Discretes	June 2001
Heathrow, UK	EURSO	August 1998
Heerlen, The Netherlands	MDS	April 2004
Hong Kong, China	Assembly Discretes	December 1997
Kaohsiung, Taiwan	Assembly ICs	May 1997
Kobl, Japan	MDS	February 2004
Nijmegen, The Netherlands	ICs/Discretes	July 1998
San Jose, USA	ICs	February 2001
Seremban, Malaysia	Assembly Discretes	March 2000
Singapore	Waferfab ICs	June 2001
Singapore	SSMC	June 2004
Shanghai, PRC	MDS	January 2004
Shenzhen, PRC	MDS	March 2004
Southampton, UK	ICs	January 1998
Stadskanaal, The Netherlands	Discretes	January 1997
Sunnyvale, USA	ICs	February 1998
Tempe, USA	ICs	February 2001
Vienna, Austria	PSS	June 2003
Zürich, Switzerland	ICs	April 1998

Mean Time Between Failures (MTBF)

The period of time that a piece of electronic equipment will run without failure is a critical parameter. The MTBF (called MTTF, mean time to failure, for non-repairable equipment) is a relatively simple calculation to make, yet it causes difficulties for many electronics engineers. The purpose of this section of the handbook is to give a simple explanation of MTBF (MTTF) calculation.

Failure rate

After testing electronic components, failure rate is given by:

$$\text{failure rate} = \frac{\text{number of failures}}{\text{quantity tested x test time}}$$

Failures can be complete, partial, sudden, gradual or intermittent, and so may not show up at all during the test time. For this reason we usually quote assessed figures, based on a confidence level of 60%. The relationship between observed failures and assessed failures is:

observed failures	assessed failures
0	< 0.9
1	< 2.0
2	< 3.1
3	< 4.2
4	< 5.2 etc.

Example

500 components were tested for 10,000 hours, 1 failure was observed:

$$\text{observed failure rate} = \frac{1}{500 \times 1000} = 0.2 \times 10^{6} \text{ per hour or}$$

$$\text{assessed failure rate} < \frac{2}{500 \times 1000} = 0.4 \times 10^{6} \text{ per hour or}$$

Failure rate is usually expressed in FITS (failures in time standard, 1 FIT = 10-9 per hour). So, an assessed failure rate of 0.4 x 10-6 per hour = 400 FITS.

Calculation of MTBF

When the components are built into a piece of electronic equipment, the assessed failure rates of each individual component add up to give the assessed equipment failure rate.

Example

Consider a piece of electronic equipment containing 319 electronic components, as shown in the Table below. For each component type the assessed failure rate will be known:

component	quantity in equipment	assessed failure rate (FITS)	combined failure rate (FITS)
IC	9	500	4500
diode	20	120	2400
transistor	9	200	1800
resistor	140	20	2800
capacitor	120	20	2400
coil	21	300	6300
		Equipment failure rate = 20200 FITS	

$$\text{MTBF} = \frac{1}{\text{equipment failure rate}} \quad \frac{10^{9}}{20200} = 49505 \text{ hours}$$

So, based on continuous working for 8 hours a day, 5 days a week, the equipment should run successfully for 23 years.

Moisture Sensitivity Level (MSL)

If packed or stored incorrectly, moisture-sensitive plastic SMDs can be easily damaged by exposure to the high temperatures associated with soldering. If any moisture is present in the plastic package during soldering, it may turn into steam and expand rapidly. Under certain circumstances the force created by this expansion can cause internal delamination and, in the most severe conditions, cause internal or external package cracks (the popcorn effect). This effect can be more prominent with infra-red or vapour-phase reflow soldering methods. The effect is less in wave soldering, which only exposes the devices to high temperatures for a very short time.
To minimize this problem, Philips Semiconductors delivers moisture-sensitive ICs in a resealable moisture-resistant packing (see Drypack).

Determining moisture sensitivity level
Not all plastic packages are equally sensitive to moisture. Each has its own moisture sensitivity level (MSL) which is influenced by:

- chip size
- package body size
- package material properties
- temperatures at infra-red or vapour-phase reflow soldering. (at lead-free or SnPb soldering temperatures.) Therefore sometimes are two levels are made available each for max body temperature allowed.

Philips Semiconductors determines MSL by testing batches of each package type. After moisturizing the package to a predetermined level, it is heated to high (soldering) temperature and then cooled. The package is then checked for functionality and, if necessary, the test is repeated at a higher level of moisturization.

All Philips Semiconductors test centres perform these MSL tests and classify a MSL for each package type. Moisture sensitivity levels range from MSL = 1 (device not sensitive to moisture) to MSL = 6 (device very sensitive to moisture). Determination of MSL is covered in quality standards:

- SNW-FQ-225A
  (SMD preconditioning specification)
- SNW-FQ-225B. In accordance with Jedec J-STD-020
  (Moisture sensitivity level assessment method).

The MSL corresponds with a certain 'out of bag' time during which the product can be safely used without damage during soldering. For these 'out of bag' times see Drypack.

Philips business Excellence (PBE)

The Business Excellence Model (Fig. 1)
The Business Excellence Model recognizes that customer satisfaction, people (employees) satisfaction and impact on society are achieved through leadership-driven people management, policy and strategy, resources and processes, all of which ultimately lead to excellence in business results. It is 100% identical to the EFQM Excellence model, developed by the European Foundation for Quality Management.
Each of the nine parameters of the model can be used to assess an organization's progress towards excellence. The scoring points shown for each parameter equate to the percentages used for the European Quality Award (i.e. 100 = 10% etc.), such that the total points allocated (1000) equates to 100%. The model is split (500 scoring points each) equally between the "enabler" parameters (concerned with how an organization approaches its business in each of the areas shown) and the "results" parameters (concerned with what an organization is achieving and has already achieved).

Each of the nine criteria is described below:

- **Leadership:**
  Excellent leaders develop and facilitate the achievement of a company's mission and vision. They develop organisational values and systems required for sustainable success and implement and reinforce those values and systems through their actions and behaviors. During periods of change they retain a constancy of purpose. Where required, such leaders are able to change the direction of the organisation and inspire others to follow.
- **Excellent Organisations:**
  Excellent organisations implement their mission and vision by developing a stakeholder focused strategy. A strategy that takes into account the market and sector in which it operates. Policies, plans, objectives, and processes are developed and deployed to deliver the strategy.
- **People:**
  Excellent organisations manage, develop and release the full potential of their people at an individual, team and organizational level. They promote fairness and equality and

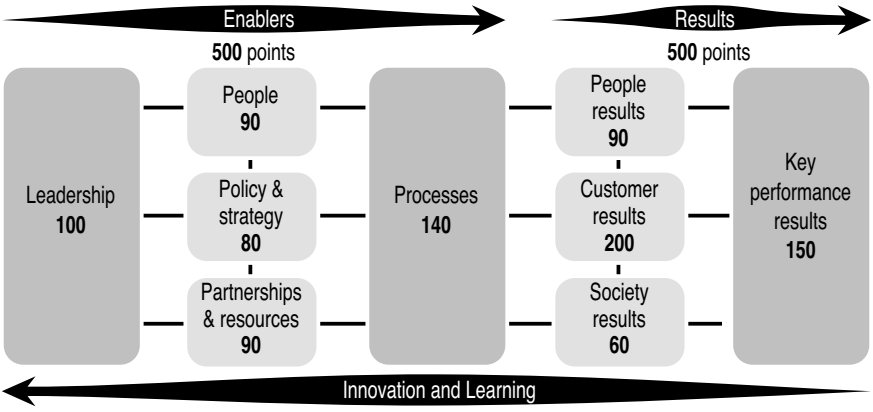


Fig. 1. The Business Excellence Model

involve and empower their people. They take care to communicate, reward and recognise in a way that motivates staff and builds commitment. Committed staff are motivated to use their skills and knowledge for the benefit of the organisation.

- **Partnerships and Resources:** Excellent organisations plan and manage external partnerships, suppliers and internal resources in order to support policy and strategy and the effective operation of processes. During planning, and whilst managing partnerships and resources, they balance the current and future needs of the organisation, the community and the environment.
- **Processes:** Excellent organisations design, manage and improve processes in order to fully satisfy, and generate increasing value for customers and other stakeholders.
- **Customer results:** Excellent organizations comprehensively measure and achieve outstanding results with respect to their customers.
- **People results:** Excellent organizations comprehensively measure and achieve outstanding results with respect to their people.
- **Society results:** Excellent organizations comprehensively measure and achieve outstanding results with respect to society.
- **Key performance results:** Excellent organizations comprehensively measure and achieve outstanding results with respect to the key elements of their policy and strategy.

Assessment and points scoring

Within the enabler parameters, assessment addresses the excellence of the approaches used and the extent of the deployment of these approaches, both vertically through all levels of the organization and horizontally across all areas and activities. Each of the enablers parameters is scored on the combination of two factors: the degree of excellence of the approach, and the extent of the deployment of the approach.
Within the results parameters, assessment addresses the organization's trends and achievements in terms of the actual performance compared to targets set and, wherever possible, compared to competitors (particularly the "best in class") for the results under review. A key distinction within the results parameters is the recognition of both direct feedback data from the relevant stakeholder, and the internal measurement of predictive performance measurements. These two areas are sometimes described as the "leading" and "lagging" indicators of performance. Each of the results parameters is scored on the combination of two factors: the degree of excellence of the results, and the scope of the results.

Implementation of PBE in Philips Semiconductors
The Philips Semiconductors Business Excellence program is aligned with the Philips Corporate policy - agreed in the June 2004 GMC meeting:

- The PD & four clusters will do annual self-assessments from 2004 onwards. Every other year, these should be validated assessments. These clusters are: Consumer, Communications, MultiMarket Semiconductors and Operations. These four units are eligible units for the presidential award. In this award there are three levels to be achieved: Bronze (500 points), Silver (600 points) and Gold (700 points).

- BUs and other units, as defined in consultation with Quality Management Semiconductors (QMS), will be encouraged to participate in the PD PBE program. These units will be requested to do regular self-assessments. The EMT determines the targets for annual assessments. Units that have achieved a level of approximately 500 points or more are requested to participate in the PD “Star Award”. For this PD Award we use the same criteria for Bronze, Silver and Gold.

Up till mid 2004 there was only one Award, the Philips PBE Award, this has now been succeeded by the Presidential Award. The following units in Philips Semiconductors have achieved PBE awards:

- MultiMarket Products, Bronze in 2000. MMP was the first unit in Philips to achieve this result.
- Assembly and Test Organization (ATO), Bronze in 2001 and Silver in 2003. ATO was the first unit in Philips to achieve the Silver Award.
- Marketng and Sales, Bronze in 2004.

Results from various assessments can be found on the QMS / BEST Intranet pages.
QMS - http://pww.sc.philips.com/qms/
BEST - http://pww.sc.philips.com/qms/best/

Philips Quality

Philips Quality defines the partners, framework and conditions for Building the Winning Company.

Philips Quality partners

It is the interaction between four partners which shapes Philips Quality:

- **Customers** who buy the company's products and services
- **People**, all of us, who are the company
- **Leaders** who merge the interests of all who have a stake in the company
- **Suppliers** who provide materials and services.

Philips Quality Framework

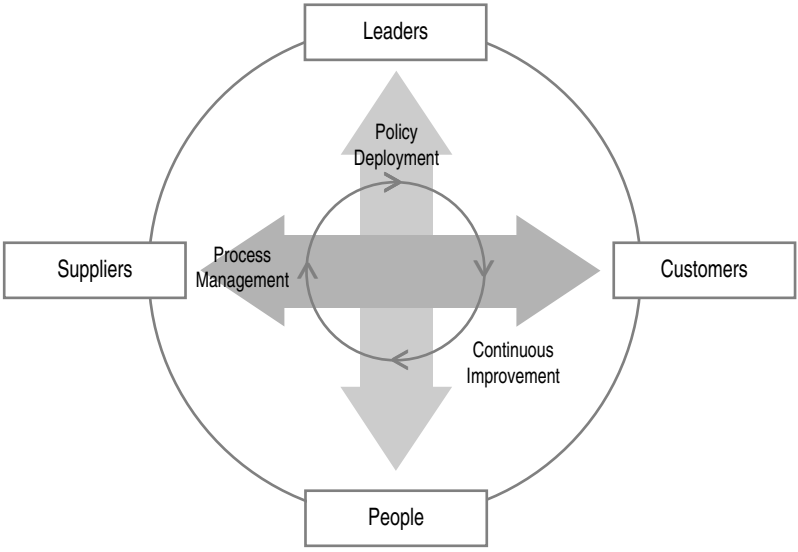
Philips Quality provides the framework for interaction between the partners.

- **Policy Deployment** communicates and translates company objectives through successive organizational layers, thereby empowering every individual to contribute to the common goal. It provides the framework for the interaction between the leaders and the people.
- **Process Management** puts all tasks in the perspective of the challenge to surpass customers' expectations. It provides the framework for the interaction between customers, the company and suppliers.
- **Continuous Improvement** means striving for perfection in a systematic and coherent way. Interaction between the four partners provides momentum to the improvement task.

Achieving Philips Quality

Achieving Philips Quality requires managing change. An important task of managers is to create the conditions leading to change in processes:

- Organize, Communicate, Learn, Recognize, Imagine
- Measure, Assure, Analyze, Audit, Benchmark.



Philips Values

The four Corporate Philips Values (the four Ds) are listed here together with some practical ideas on how we put them into everyday practice.

Delight Customers

We delight our customers by anticipating and exceeding expectations thereby creating sustainable market leadership:

- understand in detail how your work meets customers' needs
- think from the customer's point of view to improve products, services and processes
- maintain two-way communication with customers
- always seek ways to improve customer satisfaction.

Deliver on Commitments

We pursue business excellence, being rigorous in delivering on our commitments:

- work to mutually agree on commitments with clear and measurable standards
- do what you promised to do, on time
- challenge the 'way it has always been done'
- keep people informed about progress.

Develop People

We inspire and enable each other to use our creativity and entrepreneurial flair, and to maximize our potential:

- be courageous to take on new challenges or learn new skills
- openly receive feedback and constructively give candid and timely feedback
- help others to find solutions for themselves by listening, questioning and exploring options together
- be open to new ways of doing things.

Depend on Each Other

We work as 'one Philips' in an environment of transparency and trust to mobilize our collective competence and that of our business partners:

- seek to understand, acknowledge and build on others' ideas
- help others and ask for support to deliver value
- put overall business objectives ahead of your own interests
- consistently be open and respectful in all communications.

Comprehensive information about the four values can be found in:
http://www.philips.com/ourvaluesinaction

PPM

PPM – literally 'parts per million' – is the measure of quality used in conjunction with Zero Defects-oriented quality-improvement activities. PPM is a measure of actual quality, as distinct from the limiting quality set by AQL-based sampling inspection which is given as a percentage.
The use of ppm – usually numbers in the region 1 to 100 – is considered to make people more conscious of quality levels, and to distinguish ppm from AQL (given in %).

WHICH PPM?

Many ppm values are usually measured for a given product during the course of its manufacture and use, Fig. 1. Principal among these are process average reject level or estimated process quality, which may be given for inoperatives, or for mechanical/visual or electrical rejects. These levels are calculated from the manufacturers'

Acceptance Testing results:

- defect level: derived from customers' receiving inspection (where this is still carried out)
- receiving inspection level: the reject level arising from customers' receiving inspection
- line reject level: the reject level resulting from customers' assembly-line testing; generally divided into gross and net values; the net value being that agreed between customer and manufacturer after failure analysis.

Thus, ppm figures can relate to conformance to specification:

- inoperatives only (electrical and/or machanical visual)
- all electrical defects
- mechanical/visual defects
- all defects combined.

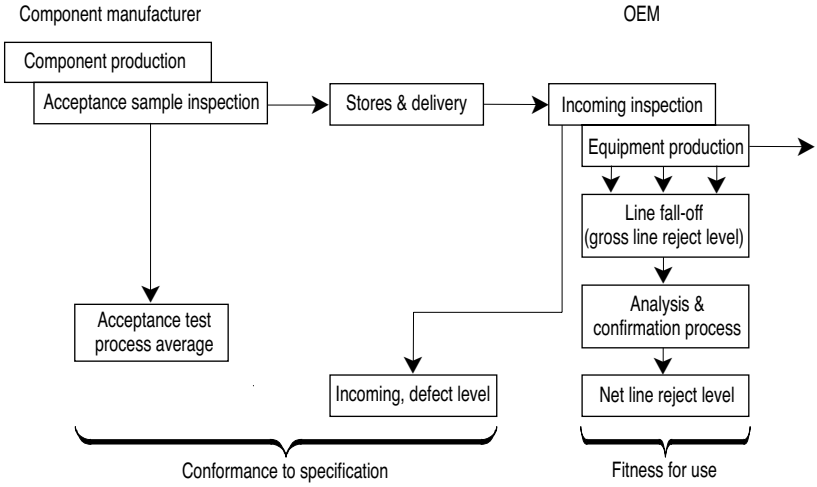


Fig. 1. Reject-level values depend on the point of measurement. Lots of most semiconductors will be inspected at a number of points between our production and our customers' assembly. The value obtained at the last point is evidently the critical one: values obtained earlier can be quality indicators only.

They can also relate to fitness for use :

- gross line rejects
- NET (OEM)
- NET confirmed
- electrical defects
- mechanical/visual defects
- all defects combined
- application
- OEM test/inspection stages.

OUR PPM VALUES

We record and publish several process average values for our semiconductors, derived from Acceptance test results. In any production period (week, month, quarter, etc.) m lots are submitted for Acceptance testing, a sample of size n is taken from each lot, and x rejects are found during testing. The number of rejects found is used to estimate the number of rejects in the whole lot:

$$X_n = N_n (x_n/n_n)$$

where Nn and Xn are the lot size and estimated rejects in the whole lot, respectively.
Then, for each test, the process average

$$P = \frac{X_1 + X_2 + ... + X_m}{N_1 + N_2 + ... + N_m} \times 10^6 \text{ (ppm).}$$

Thus, for the electrical test, n will be the sample tested and x the number of rejects found in that test; these are converted to X_n for a batch size N_n. Process average values for mechanical/visual are similarly derived.
The operation of our outgoing PPM Process Average system is such that the results of all the Q & R sample tests per type and per family are accumulated from all lots and only exclude clear rogue lots. This yields EPQ and ensures that the results represent the true process average as would be received by the customer, and eliminates problems which arise when trying to measure AOQ (Average Outgoing Quality) when an acceptance sampling scheme is based on zero acceptance number.

Verification

PPM values, especially low values, are extremely difficult to confirm. Reliable verification requires stable application conditions, fixed assembly methods and, above all, large quantities.

PQA-90

PQA-90 stands for Philips Quality Award (for Process Management) for the nineties. It set out standards for quality improvement that units throughout the concern worldwide achieved during the nineties. The award is granted by the Philips Group Management Committee.
PQA-90 provided a structure for managing improvement by systematically evaluating improvement organization and activities.

The PQA-90 Award

The PQA-90 Award provided recognition for outstanding performances in managing business processes and thereby satisfying our customers. Its purpose is to support and stimulate organizations in their efforts to achieve Philips Quality. The PQA-90 criteria (see below) served as a working tool for planning, training and assessment, and provided a framework for moving towards world-class quality. In addition, the criteria provided a common language to communicate requirements throughout the organization and with our partners.

The PQA-90 criteria

An essential step in the systematic improvement of a process is to check against criteria. The PQA-90 criteria were compatible with the standards defined in other supplier awards and with those of prestigious awards such as the Deming Prize (Japan), the Malcolm Baldrige National Quality Award (USA) and The European Quality Award (TEQA). The PQA-90 criteria are defined in six categories:

- Role of Management
  - provide leadership and set conditions
  - deploy policy
  - monitor progress and initiate actions
  - influence norms and values by personal attitude.
- Improvement Process
  - process management
  - organizing the improvement process
  - continuous learning
  - problem-solving discipline.
- Quality System
  - quality procedures
  - document control
  - internal audits
  - corrective actions.
- Relationship with Customers
  - customer-needs are guidance for action
  - customer partnerships
  - customer interface.
- Relationship with Suppliers
  - supplier assessment
  - preferred suppliers
  - supplier-partners.
- Results
  - customer satisfaction
  - performance of suppliers
  - process control.

After all Philips Semiconducters units achieved PQA-90 awards, PBE (Philips Business Excellence) was chosen as the model for all units to use for continuous improvement.

Product manufacturing codes

The product manufacturing codes marked on the packages of discrete semiconductors and ICs are listed in full in specification SNW–SZ–602. PMC's are printed on barcoded id labels.
For discrete semiconductors the code is a single upper-case or lower-case letter identifying the centre where the component is manufactured.
For ICs the code is a single letter or figure identifying where diffusion and/or assembly and/or final (QA) test is carried out.
A third character is used for RoHS classification:

G = product complying to RoHS
E = exempted from RoHS
N = all others
The following lists give the codes for the most important Manufacturing Centres.

Codes for discrete semiconductors

Code	Manufacturing Centre
D	Philips Semiconductors, Hamburg, Germany
E	Philips Semiconductors, Hazel Grove, UK
F	Philips Semiconductors, Stadskanaal, The Netherlands
H	Philips Semiconductors, Nijmegen, The Netherlands
P	Electronic Devices Ltd. (EDL), Hong Kong, China
W	Philips Semiconductors Guangdong, China
m	Philips Semiconductors Philippines Inc., Cabuyao, Philippines
t	PSS, Seremban, Malaysia.

Codes for ICs

Diffusion	Assembly	Unit
D	-	Hamburg, Germany
H/P/T/U	-	Nijmegen (AN/MOS-3/MOS-4YOU/MOS-2), The Netherlands
K	-	San Antonio, USA
M	-	Caen, France
-	P	Calamba, Philippines (PSC)
-	S	Kaohsiung, Taiwan (PSK)
V	-	Albuquerque, USA
Y	-	Shanghai, China
Z	-	Singapore
b	-	Böblingen, Germany
c	-	Fishkill, USA
k	-	Hsinchu, Taiwan
-	n	Bangkok, Thailand. (PST)

Product marking

As Fig. 1 shows, the top side of an integrated circuit from Philips Semiconductors contains identification marking. This marking normally comprises three lines (A, B, and C) of text and the Philips logo.
Line A contains the commercial type number and optional designations for crystal technology and for package type.
Line B contains the diffusion lot number and a 2-digit assembly sequence number, for traceability to the assembly batch.
Line C contains two code letters designating the diffusion centre and the assembly centre, the RoHS code letter, followed by the assembly year and week date code (YYWW), the mask layout version and the release status code (blank for released products, X for development samples or Y for qualification samples). For the code letters of the centres see “Product manufacturing codes”.
A typical example of IC marking is:
Line A: 74HL33534D
Line B: K3P08604
Line C: HnG 0422 A X

On very small packages the marking is condensed by truncating the information into two lines.

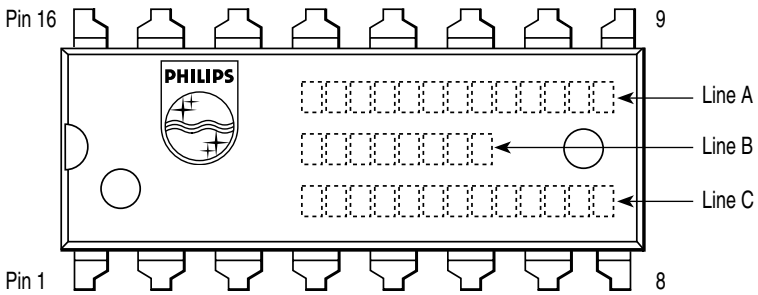


Fig. 1. The IC marking format.

Product Quality & Reliability Assurance database (PQRA)

As part of our Total Quality Management (TQM), Philips Semiconductors is committed to sharing Quality & Reliability (Q&R) data with our customers. To be helpful to the customer, the data shared must be correct, up-to-date and meaningful. To issue Q&R data in the most professional, efficient and effective way, we have developed a database (PQRA), loaded with the latest Q&R data:

- Product Quality Assurance data
- Product Reliability Assurance data.

Quality data

PQRA data provides Estimated Process Quality (EPQ) figures (in ppm, including or excluding rogue lots), either for product families or for specific products. These figures show product quality after final test, calculated from actual QA test results.

Figure 1 shows typical quality data. It contains:

- product type and family
- test type (e.g. Electrical)
- month and year when tested
- number of lots tested in the month
- Lot Acceptance Rate (LAR)
- total quantity in all lots in the month
- EPQ expressed in ppm.

Fig. 1. Typical quality data from PQRA.

Reliability data

PQRA data provides reliability data for product families or specific products. The information provided includes FITS (Failures in Time Standard), FPM (Failures Per Million) and raw batch data.

Figure 2 shows a typical FITS/FPM output.

Accessing the PQRA database

The database can be accessed through the Philips Intranet by employees of Philips Semiconductors. A password is required for access. For information to customers, the local sales office can access the PQRA database for a report, and communicate this to the customer.

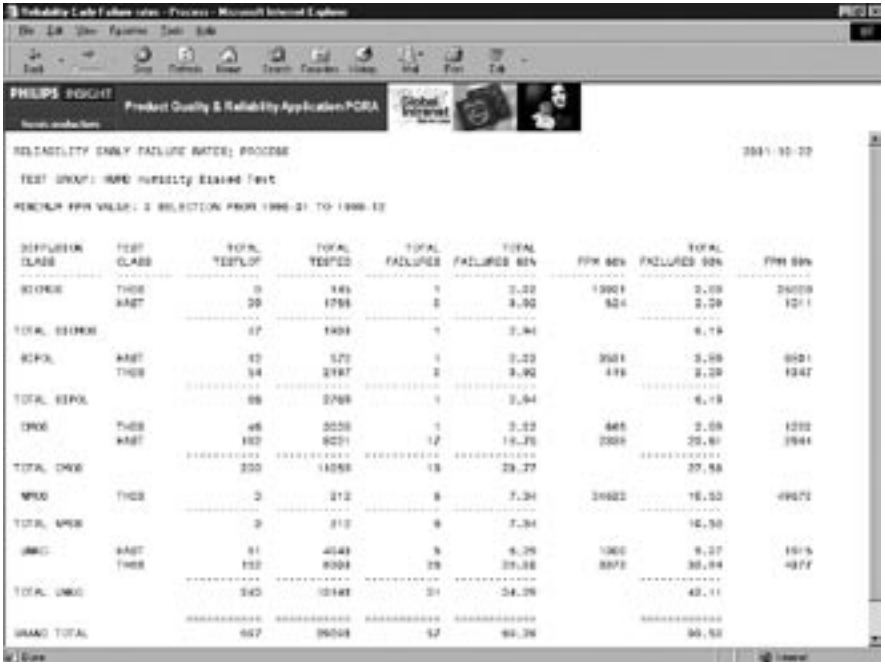


Fig. 2. Typical reliability data (FITS and FPM).

Quality Function Deployment (QFD)

With Quality Function Deployment the requirements of the customers are deployed to the development and manufacture of new products. QFD is used to translate customer requirements (expressed in customer language) into product specifications or design parameters. It also provides the opportunity to assess possible improvements and set targets.

The word 'Quality' in QFD means 'the ability to satisfy stated or implied needs', so it is used in the sense of satisfying customer needs or requirements, rather than being specific to a Quality Department or Quality System.

With QFD, customer requirements are implemented at the concept phase of development, where the product design exists only on paper, so customer needs can be implemented without expensive equipment or process changes. This is an ideal opportunity to fully implement any application aspects. The aim of QFD is to get **better products sooner**: better products because they will better fulfil the stated and implied needs of the customer: sooner because in the specification stage all parties are involved and priorities have been set for improvements towards customer requirements.

To be successful, QFD must tackle the real needs of the customer. These can only be determined by face-to-face customer visits or detailed customer research.

QFD requires multi-discipline team effort, bringing together the skills of Marketing, Development and Manufacture.

During QFD, each important specification parameter of the product is benchmarked against competitor products.

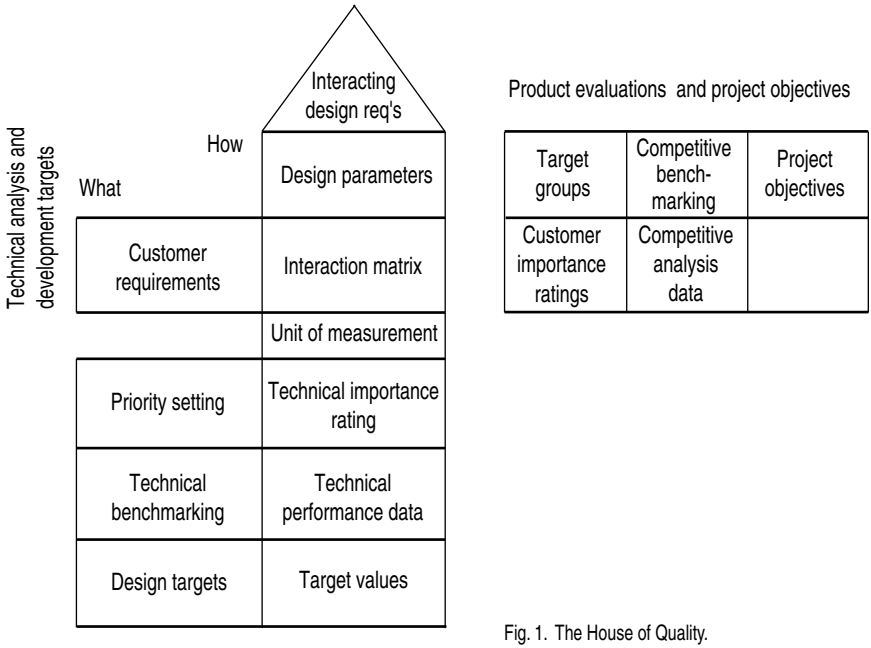


Fig. 1. The House of Quality.

The House of Quality

The main tool of QFD is the House of Quality (Fig.1). At the centre of this 'house' (under the roof) is the interaction matrix, where the customer requirements are applied to the design parameters influencing those requirements. Here, the translation is made from customer language to design language.

Figure 2 takes the House of Quality model into a working scenario. Here, the customer is categorized as a group of 'sound freaks', having a specific set of requirements imposing different 'weight' factors.

The 'What' section, at the left of the House of Quality, lists four customer needs for an audio set. Under the roof (the How section) are listed four relevant design parameters, and the interaction matrix compares What with How.

In the roof the interaction between design parameters are indicated. In the example shown, a higher number of controls has a positive (+) influence on harmonic distortion.

The relevant interaction between What and How is assessed, with interaction factors of 9 (strong), 3 (medium), 1 (weak) or none at all.

The product of demanded weight (from the customer) and interaction factor gives the weighted sum of the design parameter, which can then be ranked in accordance with the need to improve it.

For example, referring to Fig. 2, the customer has demanded a weight of 6.25 for natural sound. This has been assessed in terms of the relevant design parameters and given an interaction of 9 (strong) against frequency response and harmonic distortion. The product (9 x 6.25) gives a weighted sum of 56.25, placing these two design parameters in ranking position 1 for improvement to satisfy the customers' needs.

Below the 'House of Quality', the question of how far each design parameter must be improved is answered by benchmarking the parameter against the products of our main competitors. For example, in Fig. 2, our product has a frequency response of 0.7 dB whereas Company A's product has a better figure of 0.5 dB. A target value of 0.5 dB is therefore set for improvement.

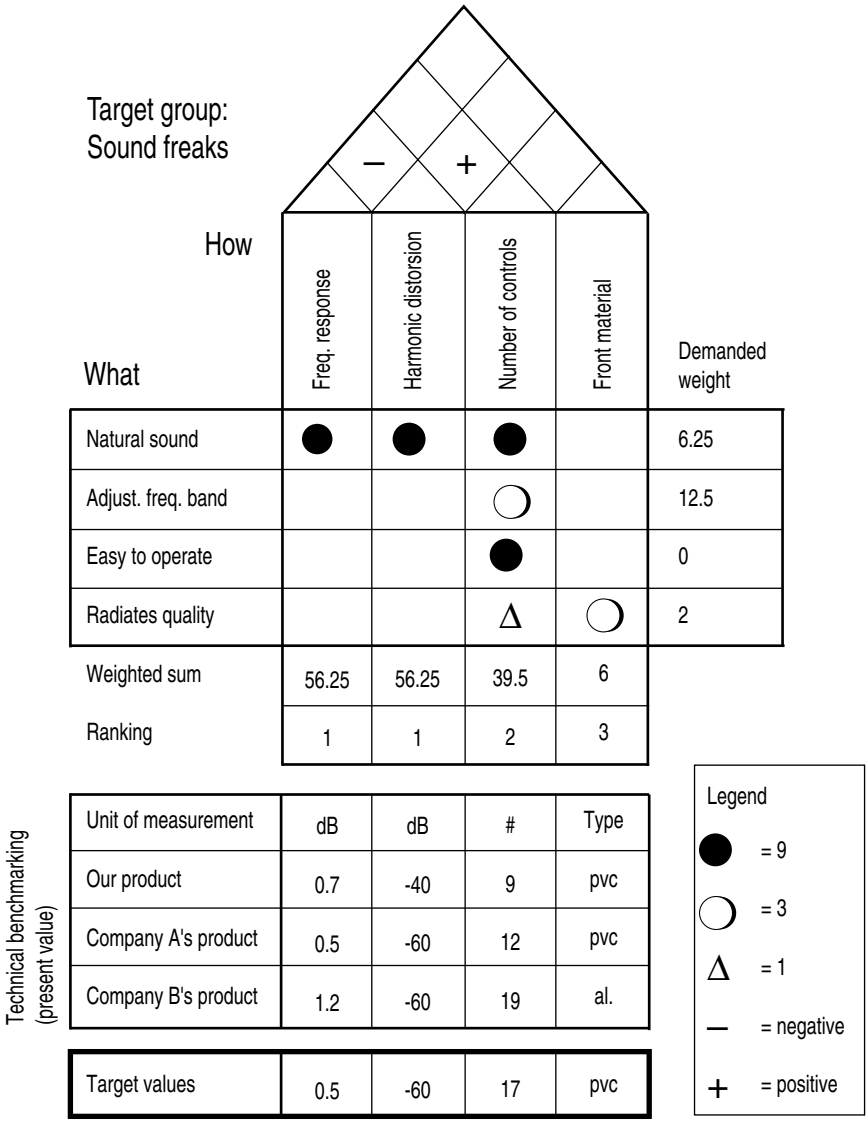


Fig. 2. House of Quality scenario 'Sound freaks'.

Quality Improvement Competition (QIC)

"Employees who work with a product or process every day are the most qualified to change or improve it". Such is the philosophy behind the Philips Semiconductors worldwide Quality Improvement Competition (QIC - pronounced "quick"). Launched in 1993, QIC encourages employees worldwide to form Quality Improvement teams with the following aims:

- To encourage improved levels of customer service and quality throughout the company
- To promote structured teamwork and the effective use of improvement tools
- To recognize and reward successful improvement projects and initiatives

Competition structure

To be eligible to QIC, project suggestions must: come from individual employees; be supported by local management; and have a direct link to quality improvement. After an initial screening process, projects are officially registered with the competition coordinators, an official registration certificate is issued, and the project team begins its work.

At the end of the calendar year, each project team must present its results at a local final, chaired by local plant management. The local winners are then entitled to compete in one of three regional finals; senior global sales operation managers chair the regional juries. Regional finalists receive special certificates and gain recognition within the company through a range of internal communications media. In regional and world finals a major customer is invited to be on the jury. From the regional finals, twelve teams are nominated for the world final. The world final is held in the first half of the following year and chaired by the CEO of Philips Semiconductors. The overall winning team receives the prestigious QIC trophy. In addition, the teams in the final get the opportunity to select a public prize, and the jury awards a special recognition prize.

Project assessment criteria

To ensure a properly structured competition, and to let participants know what is expected of them and how they will be assessed, scoring is done on six project assessment criteria based on a teamwork approach to problem solving and incremental improvement:

1. Project selection
2. Project analysis
3. Solutions
4. Results
5. Project learning
6. Working as a team

Results to date

In the 2003/04 competition the number of teams competing was 1554, the largest ever. The final took place in Athens, Greece, where the team from PSK (Kaohsiung, Taiwan) called "Cooperation" won the Gold QIC trophy.

Cost-saving benefits

Although the competition is intended to stimulate quality through employee teamwork, resulting improvements also lead to major cost-savings.
It is estimated that the annual cost-savings achieved by the finalists in the 2000/01 competition were around 30 million Euro.
And when savings by the other participating teams were also taken into account, the competition achieved an overall productivity improvement of around 20% - for the subjects under improvement.

QIC website

http://pww.sc.philips.com/qic/

Year	Location	Teams	QIC award	Vox Populi award
1993/94	Singapore	235	Heat diffusers, Manila	-
1994/95	Monte Carlo	273	Tropical Depression, Manila	Probe Fighters, Zürich
1995/96	Orlando	345	WIRA, Malaysia	Forming Busters, Malaysia
1996/97	Shanghai	527	Team 2000, Sunnyvale	RF Power Vision, Manila
1997/98	Rome	667	E.T.F.II, Hazel Grove	Pocket Team, Bangkok
1998/99	Las Vegas	714	PCF Vision 2000, Hamburg	Climber, Hong Kong
1999/2000	Bangkok	676	BonA, Nijmegen	Q Formers, Calamaba
2000/2001	Cape Town	826	LPG Leadframe Testing, Bangkok	BEST in CSS, Chengdu
2001/2002	Barcelona	926	Samahang Pilak, Cabuyao	Peso on left over, Calamba
2002/2003	Hawaii	1410	Flying Dutchman, Nijmegen	Yield of Dreams, Albuquerque
2003/2004	Athens	1554	Co-operation, Kaohsiung	Morning, Noon & Night, Tempe

Quality standards for customers

This section contains a survey of Philips Semiconductors quality standards which are made available for our customers.

Title	Related Quality Standard	12 NC number
Philips Semiconductors Quality Manual	SNM–SQ–001	9397 750 05298
Product Release Procedure	SNW–SQ–002	9397 750 08702
General Quality Spec for general apllication discrete, Power management and RF products		
Transistors in Metal-Ceramic packages	SNW–EQ–611	
General Quality specification for Integrated Circuits	SNW–FQ–611	9397 750 11357
Quality complaint procedure for Discrete Semiconductors	SNW–EQ–632	9398 510 36011
Philips Semiconductors Requirements for Packing, Labeling, Transport & Storage	SNW–SQ–401 SNW–SQ–404 SNW–SQ–405 SNW–SQ–407 SNW–SQ–623 SNW–SQ–624	9397 750 10794

Problems prevent us from performing our daily work as we want to. So to improve the performance of our daily activities, resulting in improved satisfaction of our customers, we must solve those problems. The best way to solve problems is by using the quality techniques and tools described in this section.

PDCA cycle

For problem solving and continuous improvement the Plan–Do–Check–Action (PDCA) cycle (Fig. 1) is used in its never-ending rotation. This cycle was introduced by Dr. W. Edwards Deming, and is defined as follows:

- **Plan:** With a study of the current situation, the facts are gathered to be used in formulating a plan for problem solving. Determine the goals and methods for a change or a test aimed at improvement.
- **Do:** Once a plan has been finalized, next comes the job of implementation. For solving the problems, use the problem-solving techniques mentioned later on. Carefully formulate the results and conclusions.
- **Check:** What was learned? Check the results and conclusions in comparison with the plan to see whether they have really solved the problem. Find out whether the solution brings the expected improvement.
- **Action:** Adopt the change, or abandon it, or run through the cycle again possibly under different conditions. If a result deviates from the expectation, find and correct (or remove) the cause. When problem-solving activities have been successful, a final action such as methodological standardization is taken to ensure that the new methods introduced will be practised on a continuous basis for sustained improved performance. After that, start again with the Plan stage.

Problem solving

Figure 2 shows a step-by-step summary of how a problem can be attacked. In this summary, quality tools are shown in use.

- Assessment (Identify the Problem): Use the Pareto principle (defined later in this section) to highlight major problem areas and to select the next problem to work on.
- Define the Problem: Frequently a cause or solution is stated as “the problem”. Differences between problems, causes and solutions should be understood to avoid skipping most of the problem-solving process. A problem can be described by the observed facts (is) and by the comparable facts (is not) related to What, Where, When and Magnitude. Observed facts would normally include answers to the following: On what object (product, unit, etc.) is the defect observed and what is wrong (defect)? What standard exists and what is the deviation from standard?

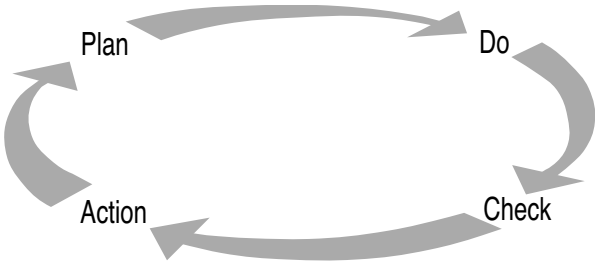


Fig. 1. The PDCA cycle.

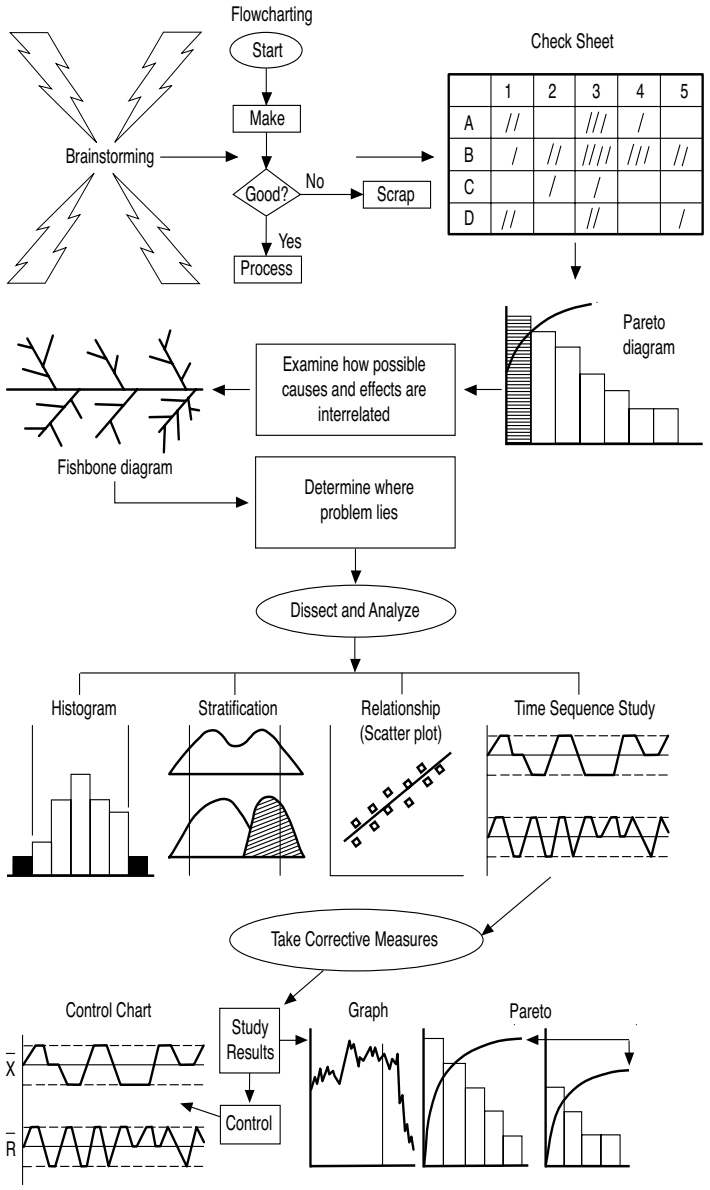


Fig. 2. Constant quality improvement using statistical quality control.

Where is the object with the defect and where on the object does the defect appear? When was the defect first observed (calendar time)?; when in the life-cycle of the object did the defect occur and in what pattern? How much of the object is defective and how many units/objects are defective? What is the trend?

- **Consideration:** Brainstorm possible causes of the problem and list ideas on a fishbone diagram (Fig. 5). Are any of the ideas related? Flowcharting (workflow, process flow, etc.) prior to brainstorming may help participant-understanding and point to contributing causes.
- **Investigation:** Determine the most likely cause. Make use of check sheets (Fig. 3) to collect data if time allows. Otherwise use other methods such as voting to decide on the most likely cause.
- **Analysis:** Decide on the most appropriate action to reduce and (if possible) eliminate the problem.
- **Initiation:** Put the action into operation. Collect data as required. Refer to higher management if necessary.
- **Verification:** Verify the result. Plot charts and graphs to highlight features.
- **Implementation:** If the solution is a success, then the appropriate action should be incorporated into the quality improvement programme.
- **Control and improvement:** Check that procedures are being adhered to and that the new level of performance is being maintained. Aim for further improvement.

8-D method for team-oriented problem solving

After a general description of problem solving, a specific method should be used for analyzing customer quality problems and reporting the results of the analysis. The 8-D method or TOPS (team-oriented problem solving) was developed by Ford Motor Company. It involved 8 steps (1 to 8), which are also used as the sequence for the 8-D report (step 0 was added later). The steps are:

- Step 0: **Prepare for the 8-D process.**
  In response to a system, evaluate the need for the 8-D process. If necessary, provide an Emergency Response Action to protect the customer and initiate the 8-D process.
  8-D application criteria are:
  – the symptoms have been defined and quantified
  – the 8-D customer(s) who experienced the symptom(s) and the affected parties (when appropriate), have been identified
  – measurements taken to quantify the symptom(s) demonstrate that a performance gap exists and/or priority (severity, urgency, growth) of the symptom warrants initiation of the process
  – the cause is unknown
  – management is committed to dedicate necessary resources to fix the problem at the root cause level and to prevent recurrence
  – symptom complexity exceeds the ability of one person to resolve.

- Step 1: **Establish team**
  Establish a small group of people with the process and/or product knowledge, allocated time, authority and skill in the required technical disciplines to solve the problem and implement corrective actions. The group must have a designated Champion and Team Leader. The group begins the team building process.

- Step 2: **Describe the problem**
  Describe the internal/external customer problem by identifying “what is wrong with what” and detail the problem in quantifiable terms.

- Step 3: **Develop Interim Containment Action (ICA)**
  Define, verify and implement the Interim Containment Action (ICA) to isolate effects of the problem from any internal/external customer until Permanent Corrective Actions (PCAs) are implemented. Validate the effectiveness of the containment actions.

- Step 4: **Define and verify Root Cause and Escape Point**
  Isolate and verify the Root Cause by testing each possible cause against the problem description and test data. Also isolate and verify the place in the process where the effect of the Root Cause should have been detected and contained (Escape Point).

- Step 5: **Choose and verify Permanent Corrective Actions (PCAs) for Root Cause and Escape Point**
  Select the best Permanent Corrective Action to remove the Root Cause. Also select the best Permanent Corrective Action to eliminate Escape. Verify that both decisions will be successful when implemented without causing undesirable effects.

- Step 6: **Implement and validate Permanent Corrective Actions (PCAs)**
  Plan and implement selected Permanent Corrective Actions. Remove the Interim Containment Action. Monitor the long-term results.

- Step 7: **Prevent recurrence**
  Modify the necessary systems including policies, practices and procedures, to prevent recurrence of this problem and similar ones. Make recommendations for systemic improvements, as necessary.

- Step 8: **Recognise team and individual contributions**
  Complete the team experience, sincerely recognise both team and individual contributions, and celebrate.

Fact gathering

All improvement starts with knowing the facts about a problem. The effects of improvement can only be demonstrated by facts. Bits of information, which together make up facts, are called data. So fact gathering can also be called data gathering. Accurate data is essential to data-based decision making. Measurability is important in collecting data. The more you use measurable data, the better your decision will be. Three types of data exist:

- Counted Data: These are noted as being present or absent and are generally answers to "how many" or "how often".
- Measured Data (often called measured variables): These are answers to questions like "how long", "what volume", "how much time". "how far", etc.
- Location Data: These answer the simple question "where?".

Before starting the data gathering, there should be a clear understanding (a plan) of which data is needed, and also the Why, When, Where, Who and How of the fact-gathering must be clear. Fact-gathering can be done by surveys, interviews, statistical tabulations and checksheets. Checksheets are the most common technique.

Checksheets (Fig. 3)

Checksheets are one of the most effective and frequently used techniques for the collection of data. They provide a systematic method for collecting data which then serves as the basis for analyzing a problem, displaying the data in graphical form, and for presentation of a solution.

From:

Type of fault	Week 1	Week 2	Week 3
A	𝍸 𝍸 𝍸 𝍸 I	𝍸 𝍸 𝍸 II	𝍸 𝍸 𝍸 𝍸 𝍸 II
B	𝍸 𝍸 𝍸	𝍸 𝍸 𝍸 I	𝍸 𝍸 𝍸
C	III	𝍸 𝍸	𝍸 I
D	𝍸 𝍸 𝍸 𝍸 𝍸 𝍸 II	𝍸 𝍸 𝍸 𝍸 𝍸 II	𝍸 𝍸 𝍸 𝍸 𝍸 II
Total no. of faults			
No. produced			
% faulty			

To:

Type of fault	Week 1	Week 2	Week 3
A	17	14	22
B	12	13	12
C	3	8	5
D	26	22	26
Total no. of faults	58	57	65
No. produced	1532	1511	1634
% faulty	3.79	3.77	3.98

Fig. 3. Typical 'counted data' checksheet.

They are also a means by which, when it is needed, more than one person can collect the same data in the same way. There are three kinds of checksheets used to record counted, measured, and location data.

A problem location or defect location checksheet is a picture, illustration or map on which data is collected. Recording data in this way often simplifies the collection process and also helps us better see the problem. An example of a defect location checksheet is a picture of a semiconductor wafer with defective die sites noted or an illustration of accident locations which can help employees to analyze accident causes to make an area safer. The simplest checksheets are for counted data. In this type of checksheet (Fig. 3) data is collected by making marks for each occurrence, usually within predefined timeperiods and then converting into a meaningful table.

Brainstorming

Using a group of people to generate as many ideas as possible is called brainstorming. This works best with a group of 6 to 12 persons. The topic for brainstorming must be clear and well understood by everybody taking part in the brainstorming session. Guidelines for brainstorming are:

- **Set an appropriate meeting place.** Selecting a venue that is comfortable, casual, and the right size will greatly enhance a brainstorming session.
- **Generate a large number of ideas.** Don't inhibit yourself or others, just let the ideas flow out. Say whatever comes into your mind and encourage others to do the same. The important thing is quantity of ideas.
- **Encourage free-wheeling.** Even though an idea may appear to be half-baked or silly, it has value. It may provoke thoughts from other members. Sometimes, making a silly suggestion can spur another idea you didn't know you had.
- **Don't criticize.** This is the most important guideline. There will be ample time later to sift through the ideas to select the good ones.

During the session, you should not criticize ideas because this may inhibit other members. When you criticize the half-baked ideas, you throw away the building blocks for the great ones.

- **Encourage everyone to participate.** Everyone thinks and has ideas, so allow everyone to speak up. Speaking in turn helps; solicit ideas clockwise around the group. Encourage everyone to share his or her ideas.
- **Record all ideas.** Appoint a recorder to note down everything suggested. The ideas should not be edited: rather, they should be jotted down just as they are mentioned. Keep a permanent record that can be read at future meetings. You may want to read through the list and take an "inventory" a few times; this process sometimes stimulates more ideas.
- **Let ideas incubate.** Once you've started brainstorming, ideas will come more easily. You are freeing your subconscious mind to be creative. Let it do its work by giving it time. Don't stop your brainstorming sessions too soon; let some time go by to allow those ideas to develop by themselves.

Pareto analysis

Having obtained the data of a problem, you can then use the Pareto principle to decide how best to use your resources, or how to concentrate on the most important facts. The Pareto principle derives its name from Vilfredo Pareto, a 19th century economist, who applied the concept to income distributions. His observations led him to state that 80% of wealth is controlled by 20% of the people (the "80–20" principle). The name "Pareto" and the universal applicability of the concept are credited to Dr. Joe M. Duran, a leading American consultant who used the philosophy "the important few and the trivial many". The Pareto principle states that only a few causes are responsible for most of the defects.

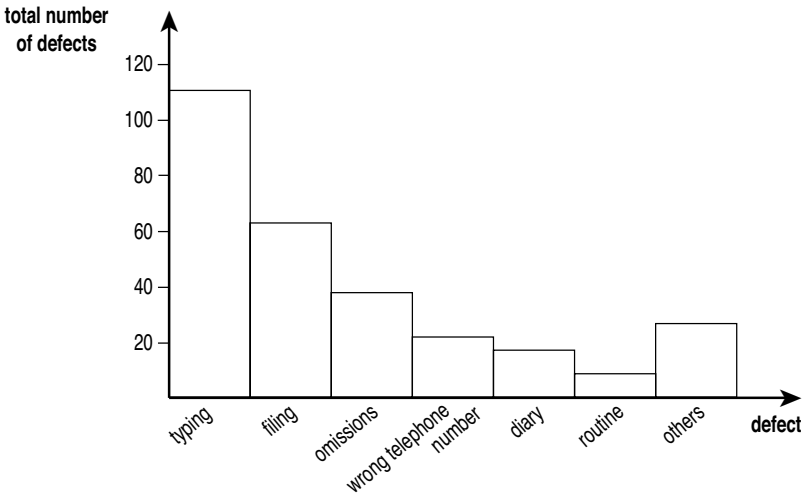


Fig. 4. Typical Pareto diagram.

In a Pareto diagram (Fig. 4) the total number of defects is entered, and the number of defects are shown for each cause.
The Pareto diagram is a specific type of column graph in which the vertical columns (the causes) are arranged in descending order from left to right to picture the frequency with which related categories occur. The one exception to the descending order is the 'others' category, a collection of very minor categories which, regardless of size, always appears on the far right of the diagram. The Pareto diagram is primarily used to distinguish the vital few categories (causes) from the trivial many to aid in setting priorities by choosing those causes for improvement which can give the highest improvement results.

Fishbone diagram (Fig. 5)

After using Pareto to select a problem to improve, the next step is to find the causes of that problem using cause-and-effect analysis, which is a structured analysis used to separate and define causes. The effects are the symptoms which let us know that we have a problem. A fishbone (also called cause-and-effect or Ishikawa: named after Professor Kaoru Ishikawa) diagram can be constructed for the analysis (Fig. 5). The construction is a four-step process:

- First, the problem or "effect" is named and placed in a box on the right, and a long process arrow is drawn pointing to the box.
- Second, the major categories of causes are decided. These major categories are placed parallel to and some distance from the main process arrow. The boxes are then connected by arrows slanting toward the main arrow. These branches (zones) represent groups of possible causes. With technical problems (shown in Fig. 5) these branches could be: Methods, Manpower, Material and Machines. For each branch, sub-branches are drawn which give possible causes of the problem. For the branch "Manpower", for example, the sub-branches could be training, motivation, workmanship, supervision, etc.

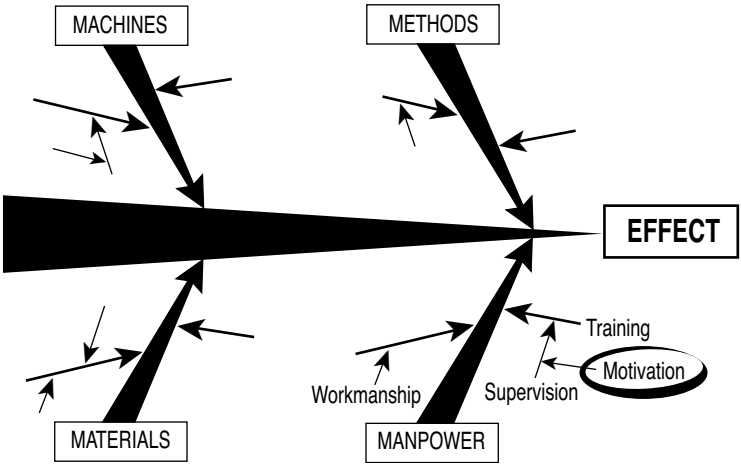


Fig. 5. Typical fishbone diagram.

- Third, the completion of the diagram is done by brainstorming for causes. The causes are written on the chart, clustered around the major category or subdivision which they influence. These minor causes are connected by arrows pointing to the main process arrow. The causes should be divided and subdivided to show, as accurately as possible, how they interact.
- Fourth, the most likely causes are circled. This is usually done after all possible ideas have been posted on the diagram. Only then is each idea critically evaluated. The most likely ones are circled for special attention (see 'Motivation' circled under 'Manpower').

Separate diagrams may be needed if the defined problem is not specific enough, so causing some major categories of the diagram to be overloaded. This indicates the need for additional diagrams. The diagramming exercise will give a better understanding of the real causes of the problem and can be a basis for further measurements or corrective action.

Histogram (Fig. 6)

If data is tabulated and arranged according to size, the result is called a frequency distribution. The frequency distribution will indicate where most of the data is grouped and will show how much variation there is. A histogram (Fig. 6) is a column graph depicting the frequency distribution of data collected on a given variable. To construct a histogram, you need data, the more data you have, the more accurate your histogram will be. 0A minimum acceptable amount of data is from 30 to 50 measurements. The different values are grouped in classes, by setting class boundaries. Often the range (largest measurement minus the smallest measurement) of data divided by 10 is used to obtain the width of the intervals (class width) to be plotted on the horizontal axis of the histogram, each interval being one column wide. The more data you have, the larger the number you should divide by to determine the interval (e.g. if over 250, divide by 20 instead of 10).

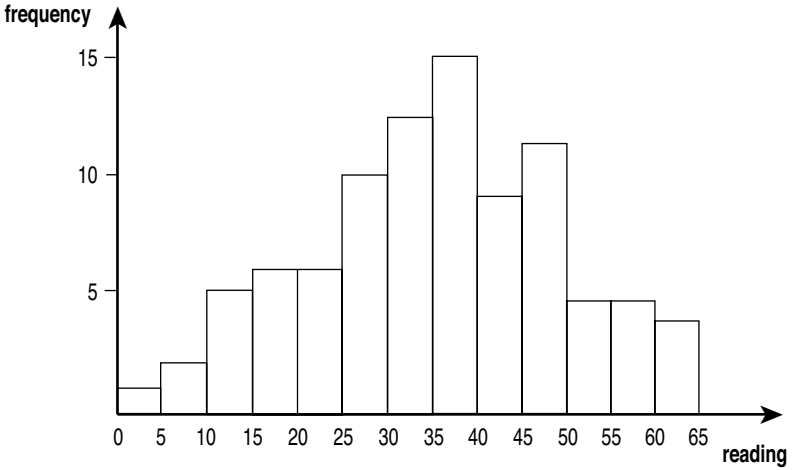


Fig. 6. Typical histogram.

The number of values in each class is shown in the histogram, where each is represented by a bar. The result shows a representation of the occurring values of the variable. The shape or curve formed by the tops of the columns has a special meaning. This curve can be associated with statistical distributions that in turn can be analyzed using mathematical tools. The various shapes which can occur are given names such as normal, bimodal (or multi-peaked) or skewed. A special significance can sometimes be attached to the causes of these shapes. A normal distribution causes the distribution to have a "bell" shape and is often referred to as a "bell-shaped curve". Histograms enable us to do three things:

- **Spot abnormalities in a product or process.** Absence of a normal distribution is an indication of some abnormality in the variable being measured.
- **Compare actual measurements with required standards.** These standards can be indicated by dotted vertical lines imposed over the histogram.
- **Identify sources of variation.** The presence of more than one source of variation in the population of the histogram may produce a multi-peaked curve.

Control chart (Fig. 7)

The control chart was invented in 1924 by Dr. Walter A. Shewart. Control charts are discussed briefly in the Statistical Process Control section of this handbook. Control charts (Fig. 7) are tools to be used to achieve stable processes by monitoring the variability of significant process parameters. At stated intervals some values of a repeated measurement are averaged. The average value is plotted on the control chart, which indicates control limits. Attribute charts (P, % defective; nP, number of defectives; U, defects per unit; C, number of defects) are used when variability data is not available or is difficult to obtain. These charts may be used for monitoring a process, however, they are more of a process/product appraisal tool than a process control tool. The purpose of control charts for variables is to compare the process behaviour against its inherent variability as determined by control limits. It is a tool for deciding when to adjust a process and when to leave it alone. Its effectiveness is enhanced by careful selection of the sampling method parameters (the following points apply mainly to Shewart Control charts):

- When the sample is chosen so that variation within the sample is significantly less than

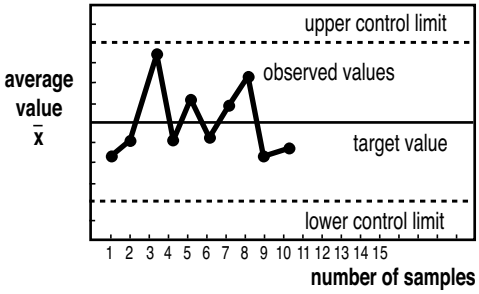


Fig. 7. The control chart, a running plot of average values from regular sample measurement, is fundamental to Statistical Process Control.

variation between samples, then the control limits for the average value (x) will be extremely narrow compared to individual sample averages, resulting in too many out-of-control conditions.

- Another problem may occur when non-homogeneous groups are included in a sample (stream effect). In this case, the control limits for the average value (x) will be too wide compared to the individual sample averages, resulting in the control chart not being sensitive to process changes.
- Sample sizes for x and R are usually between 3 and 6. A sample size of 4 or 5 is usually selected as a compromise between the amount of information gained and the cost of obtaining the information.
- Sample sizes for x and S are usually between 7 and 10. A sample size of 7 or 8 is usually selected to obtain reasonably sensitive control limits. A standard deviation chart should replace the range chart any time the sample size exceeds 10.
- For calculation of centreline and control limits for R or S and x, data is collected preferably in chronological order for 25 or more samples. For most control charts, the control limits are calculated on a basis of the average plus/minus 3 times the standard deviation of the statistic used.

It is customary to place the charts for x and R one above the other so that average and range for any one sample are in the same vertical line. Always interpret the R or S part of the chart first and when they are in control, then interpret the x part of the chart. When the R and S points are out of control, the control limits for x chart are not reliable. 'Out of Control' can be determined by observing the following rules:

- One or more plotted points outside the control limits. If a sample average falls outside the limit lines, it is evidence that a general change affecting all pieces has occurred between samples. If a sample range falls outside limits, it is evidence that the uniformity of the process has changed.
- A trend of five or more consecutive plotted points that are all increasing or all decreasing.
- A run of five or more consecutive plotted points that are all above or all below the centre line.
- Any other non-random pattern. Note that Juran/Shewart have a few other indicators of non-randomness (2 out of 3 successive points at 2 standard deviations or beyond from centre line; 4 out of 5 successive points at 1 standard deviation or beyond from centre line; not only one point out of 10 or nine out of 10 within one Sigma of the centre line) but these definitions are difficult for a typical operator to apply.

If any of these occurs, this is an indication that the process has changed and action must be taken.

Scatter diagram (Fig. 8)

A scatter diagram (Fig. 8) can be used to test the relationship between two variables (X and Y). In the case of defects and causes, the Y-axis could be the number of defects, and the X-axis the value of a variable which could cause the defects (e.g. a temperature). If the plotted measurements show a line, there is correlation. Without correlation the points will be without a pattern.

Numerous problems encountered in quality control require the estimation of relationships between two or more variables. Often interest centres on finding an equation relating one particular variable to another set of one or more variables. 'Least squares' is a statistical technique for estimating the parameters of an equation relating a particular variable to a set of variables. Some authors refer to this as least squares or curve fitting, whereas many practitioners refer to it as regression analysis and call the resulting equation a regression equation. If the scatter diagram is

plotted on linear-linear graph paper and a straight line results, the line would be represented by the equation Y = AX + C where A is the slope and C is the Y intercept. A relationship may be non-linear. If a scatter plot is done on other forms of probability graph paper (e.g. log-normal, Weibull) and the plotted measurements form a line, the equation is represented by the mathematical model upon which the probability graph paper is constructed. Experience has shown that most continuous characteristics follow one of several common probability distributions, i.e. the “normal”, the “exponential” and the “Weibull”.

X →

Y	0.5 – 0.74	0.75 – 0.99	1.00 – 1.24	1.25 – 1.49	1.50 – 1.74	1.75 – 1.99	2.00 – 2.24	2.25 – 2.49	2.50 – 2.74	2.75 – 2.99	Frequency
8.25 – 8.49								I	III	II	6
8.00 – 8.24									IIII		5
7.75 – 7.99							III	III			6
7.50 – 7.74					II	II	IIII	I			9
7.25 – 7.49					III	IIIII	III	I			13
7.00 – 7.24				III	IIIII	II	I				12
6.75 – 6.99				IIII	II	I					7
6.50 – 6.74			IIII	III							7
6.25 – 6.49		I	I								2
6.00 – 6.24	I	II									3
Frequency	1	3	5	10	13	11	11	6	8	2	70

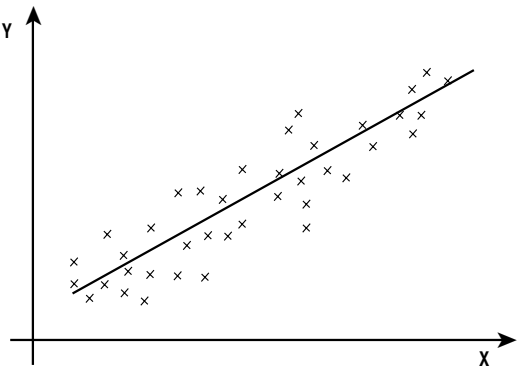


Fig. 8. Typical scatter diagram.

Paynter chart (Fig. 9)

A Paynter chart is a tool to track in time whether corrective actions have proved effective in solving a problem, usually in a manufacturing process. It is used in combination with the 8-D method to show which corrective actions have been taken and when.

Figure 9 shows a typical Paynter chart for a discrete semiconductor. Here, in August 1994, a batch of discrete semiconductors displayed 20 failures due to deformed leads. Investigations showed that the reel unit was creating lead interruption, and causing lead deformation.

A corrective action (A1) was taken to install a new reel unit, and new batches were tested monthly. In November 1994, two further failures deformed-lead failures occurred, and a further corrective action (A3) was taken to modify the tape carrier. No further failures have occurred (up to July 1995), but the monthly tests can continue until it is felt that further testing in unnecessary.

The same chart shows that a batch in September 1994 displayed 14 failures due to cracked body. A corrective action (A2) was taken to modify the handler to put less stress on the body. Subsequent monthly testing has shown no further failures.

	9408	9409	9410	9411	9412	9501	9502	9503	9504	9505	9506	9507
Deformed lead	20 A1	0	0	2	0 A3	0	0	0	0	0	0	0
Cracked body	0	14	0 A2	0	0	0	0	0	0	0	0	0

Corrective actions:
A1: Install new reel unit to prevent lead interruption
A2: Modify handler to put less stress on body
A3: Modify tape carrier to improve lead feed.

Fig. 9. Typical Paynter Chart.

Spider graph (Radar chart) (Fig. 10)

The Spider graph derives its name from its shape, which resembles a spider's web. It provides an instant visual indication of the rating by one key customer of our performance criteria, compared with the customer's "best in class" supplier.

Figure 10 shows our supplier performance rating for one key customer over a 9-month period (3 quarters) based on five performance criteria – service, product quality, cost of use, product range and overall performance.

In the first quarter the key customer rated us at 60%, 91%, 30%, 50% and 61% respectively in the five performance criteria categories compared with their "best in class" supplier ratings of 100%, 100%, 87%, 100% and 86% respectively. This was considered unacceptable and a Quality Improvement Programme was initiated.

The results of this programme are shown by the much improved customer ratings in the Spider graphs for quarters 2 and 3.

The aim of Philips Semiconductors is to obtain Spider graphs from each strategic/key customer and improve our performance to the superior level, so becoming each customer's first choice as a semiconductor supplier.

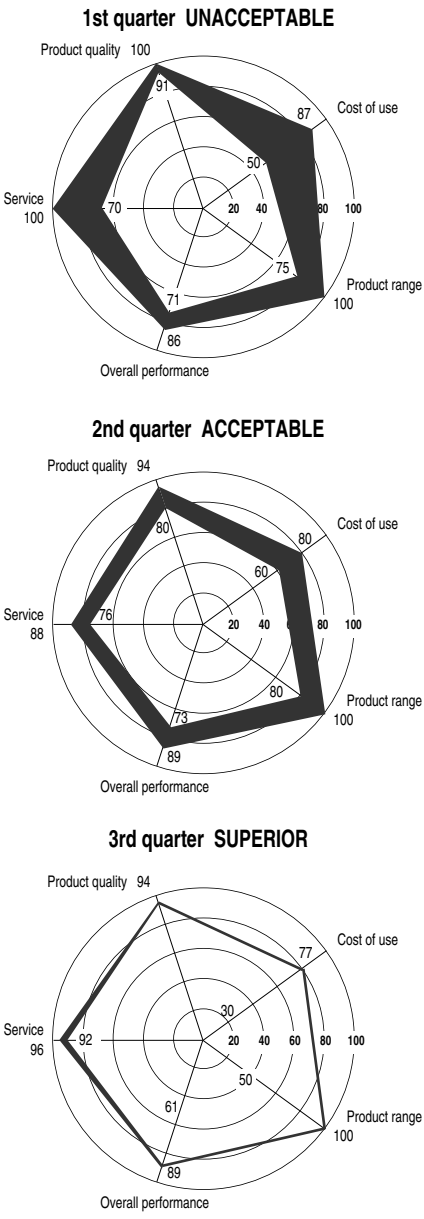


Fig. 10. Typical Spider graph showing the supplier performan rating of Philips Semiconductors for one key custom for three successive quarters.

Quality testing

Philips Semiconductors' Total Quality Management (TQM) system ensures that quality is built-in during the design, development and manufacture of our products. In the Quality Assurance part of the TQM system, quality testing continuously verifies product conformance to specifications, and product reliability.

The conformance test programs for our products are:

- **Acceptance tests**
  These acceptance tests on finished products verify conformance to the Final Device Specification. The test results are used for quality feedback and corrective actions.
  The inspection and test requirements are detailed in the General Quality Specifications.
- **Acceptance tests**
  These measure and monitor the conformance of final products to the required level of reliability. Their purpose is to identify reliability performance trends and to collect data of failure rates and failure modes.
- **Acceptance tests**
  These reliability tests assess new or modified products, or manufacturing processes.

Tables 1 to 3 give an example of the tests used for small-signal transistors and diodes. For further details, refer to the relevant quality standards: SNW–EQ-611 and SNW–FQ–611, in Quality Standards.

Table 1 Acceptance tests

Examination or test		Requirements		
Sub-group	**Description**	**Lot-size**	**Normal**	**Reduced**
A1	Visual/Mechanical Inoperative	1K –10K 10K –35K 35K–150K 150K–500K	0/200 0/315 0/500 0/800	0/80 0/125 0/200 0/315
A2a	Electrical Inoperative			
A2b	Electrical Primary DC			
A3	Electrical Other DC	1K –10K 10K –35K 35K–150K 150K–500K	0/32 0/50 0/80 0/80	0/13 0/20 0/32 0/32
A4	Electrical AC			
A5	Visual inspection	1K –10K 10K –35K 35K–150K 150K–500K	0/80 0/125 0/200 0/315	0/32 0/50 0/80 0/125

Table 2 Monitoring tests

Examination or test		Inspection requirements	
Sub-group	**Description**	**n**	**c**
C1	Dimensions	22	0
C2a	Characteristic inspection	22	0
C2b	Complementary characteristics	22	0
C2c	Verification of maximum ratings (where appropriate)	22	0
C3	Robustness of terminations (other than B3)	22	0
C4	Soldering heat & solderability with and without ageing	22	0
C5	Temperature cycling, 200 cycles	45	0
C6	Mechanical treatment (shock and/or acceleration and/or vibration)	45	0
C7	Reverse bias tropical at 85 °C/85% RH, 1000 h, with bias	45	0
C8	Endurance at maximum ratings, performed per test, 1000 h	45	0
C9	Storage at high temperature, 1000 h	45	0
C15	Autoclave, 96 h, 121 °C, 100% RH, no bias	45	0

Table 3 Qualification tests

Examination or test		Inspection requirements	
Sub-group	**Description**	**n**	**c**
D2	Electrical characteristics inspection	45	0
D5	Temperature cycling, 1000 cycles air-to-air	77	1
D8	Endurance at maximum ratings performed per test >1000 h	77	1
D9	Storage at high temperatures > 1000 h	77	1
D10	Storage at low temperatures > 1000 h	77	1
D11	HAST test (unsaturated) 133°C, 85% RH, 96 h with bias	77	1
D12	Thermal shock, liquid to liquid, 100 cycles	77	1
D13	Passive flammability	45	0
D14	ESD investigation	30	–
D15	Autoclave, 144h, 121°C, 100% RH, no bias	77	1
_	Adhesion strength test SMD	45	1

Release of new products

For product development and product release of semiconductors, all Product Groups use the same basic flow chart (Fig. 1).

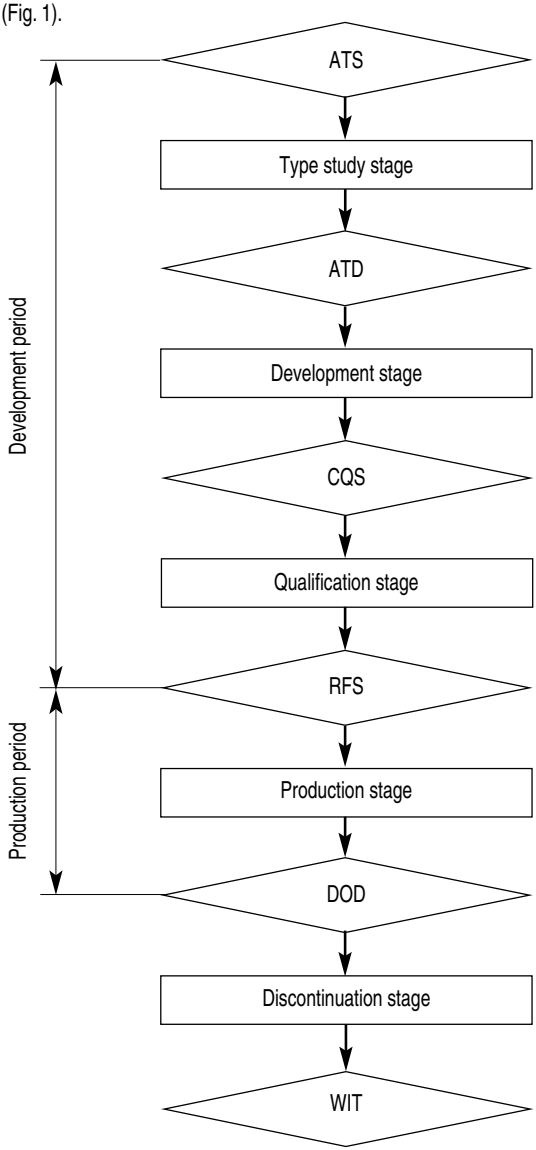


Fig. 1. Product life cycle flow chart.

The product life cycle flow chart (Fig. 1) contains five milestones which are described below.

Acceptance for Type Study (ATS)

The ATS milestone is the point where a feasibility study is started to determine whether the development of a particular product has technical and commercial feasibility.

Acceptance for Type Development (ATD)

The ATD milestone is the point where the feasibility study is concluded and assessed. If the result has been successful and provisions have been made for financial allocations, it becomes the starting point of type development. Type development can also include a Pilot Production stage.
The ATD can also be the starting point of the development period, in cases where a feasibility study is not necessary.

Availability of Customer Qualification Samples (CQS)

The objective of this milestone is to enable the supply of representative samples of a new type to customers for their qualification.
The CQS milestone is reached when the final design is achieved and there is reasonable confidence that products meet the quality and reliability requirements.
Customer Qualification Samples must be manufactured on the production lines which will be used for the full production.
Commercial delivery of products before RFS is only possible when all relevant conditions are met. These have to be further detailed and controlled by local procedures.

Release For Supply (RFS)

The RFS milestone is the official and formal release of the product as an irreversible commitment to the market. It is the point in the life cycle where the device specification is frozen and product responsibility is handed over from the development to the manufacturing department.

Discontinuation Of Delivery (DOD)

The DOD milestone is the point where the decision is taken to withdraw the type from the market. Customers receive notification.

Withdrawn (WIT)

The type is withdrawn from the market.

- During the development stage (before RFS) experiments and tests are carried out to prove:
  – conformance to specifications
  – reproducibility
  – reliability.
  During this stage samples can be delivered to customers.
- At RFS, the development is complete, and commercial and technical data is available.
- After RFS the product is commercially available and will be included in a data handbook and the catalogue. Eventual changes must follow the international change procedure, including the notification of customers.

The product release process is covered in quality standard SNW-SQ-002.

Reliability

Reliability is the ability of an item to perform a required function under stated conditions for a stated period of time (IEC 271 definition). Thus, reliability is a measure of the quality remaining after some time, exposed to particular operating stresses.

Reliability and failure rate

Like other measures of quality, reliability is a probability: the probability of a component surviving for a given time. For semiconductors, reliability is generally quoted in terms of failure rate: determined by the number of failures observed in a sample of semiconductors operated at a stated stress level for a fixed time. Reliability can be calculated from failure rate :

$$R(t) = \exp(-\lambda t)$$

where λ is the failure rate, which is assumed to be constant.

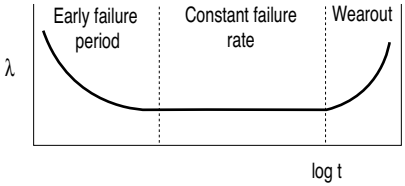


Fig. 1. The bathtub curve of failure rate with time is characterized by the initial early failure period, intervening constant-failure rate period, and a final wearout or end-of-life period.

Failure rate is not usually constant, however, but varies with time in the way typified by the familiar bathtub curve, Fig. 1. This translates into a corresponding reliability curve, Fig. 2.

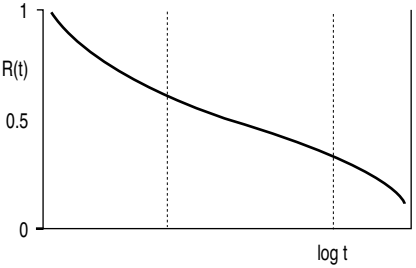


Fig. 2. The curve for reliability versus time, derived from the bathtub curve for failure rate, exhibits the same three regions.

Real improvements in the quality of our semiconductors in recent years have resulted in better reliability, especially during the early-failure period, so that their reliability bathtub curve is now less pronounced at the beginning, as shown in Fig. 3.

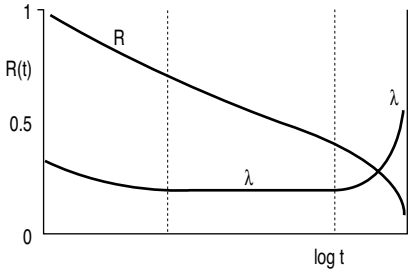


Fig. 3. Improved semiconductor conformity resulting from our quality-improvement activities has resulted in improved reliability, especially during the early-failure period, and a flatter bathtub curve. Reliability is higher until wearout sets in.

MTBF, MTTF and call rate

Reliability in finished equipment depends on the reliability of the variety of components that it comprises, under the operating conditions determined by the design of the equipment as a whole, and the environment in which it operates. Two measures of equipment reliability are common: Mean Time Between Failures, MTBF, (used where equipment is repaired as it fails) and Mean Time To Failure, MTTF, (used where repair is not carried out). Both are defined as the ratio of the cumulative observed operating time to the number of failures. Thus, MTTF is $1/\lambda$.

Call rate, a common indicator of the reliability of consumer equipment, is the number of service calls required during the guarantee period per hundred equipments sold. Since semiconductors operate mainly in the early-failure period (if there has been no burn-in) during the guarantee period, the improvements in our conformity and early-failure rate greatly reduce guarantee costs.

Observed and assessed reliability

Failure rate, reliability, MTBF and MTTF are classed as either observed or assessed. The observed value is that calculated from the recorded time and observed failures. Assessed values are those corrected to a given confidence level.

Return shipments

PD quality standard SNW–SQ–636 'Procedure for return shipments' categorizes return shipments into three groups:

- Commercial returns
- Logistic returns
- Technical returns.

Each of these groups involves different responsibilities and goods-flow procedures as shown in Figs 1, 2 and 3 below, which use the following key:

= Return Number

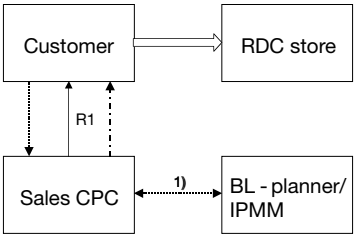
= Goods flow

= Information

RDC = Regional Distribution Centre

Commercial returns (Fig. 1)

These are goods returned from the customer because his stock level is too high.



Note 1): for commercial returns

Return Shipment Number/
Returns Material Authorization/
Goods Accompanying Document

Return request/ return approval

Returned goods flow

Credit note

Fig. 1. Commercial returns.

Logistic returns (Fig. 2)

These are goods not ordered, or with wrong 12 NC number, or of wrong quantity, or with the wrong label.

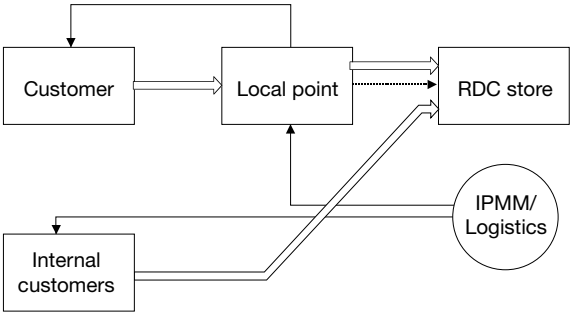


Fig. 2. Logistic returns.

Technical returns (Fig. 3)

These are goods which do not meet specification or are over the maximum agreed age. For goods which do not meet specification, the samples sent to the factory will be analyzed. If the analysis justifies the complaint, corrective action will be taken.

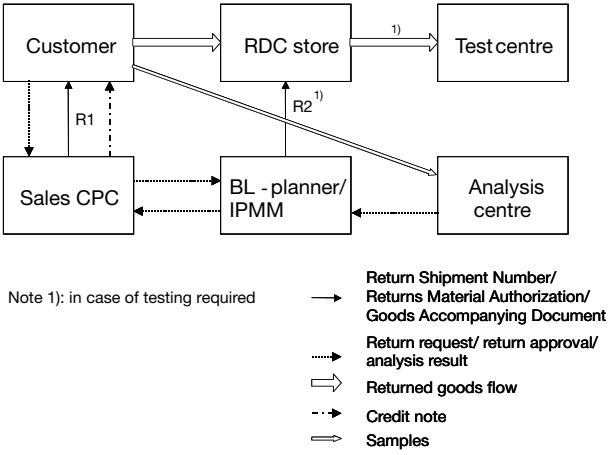


Fig. 3. Technical returns.

Sampling on the Fly

Many of the techniques and procedures used to monitor and protect product quality today have hardly changed since Quality Control was first introduced over 50 years ago. Electronic component quality levels have changed, though: by around a thousand times. Process averages of 1% or more that used to be the industry standard have been replaced by reject levels around 10 to 100 ppm. Quality procedures that were designed for the old 1% levels can present a significant hazard when applied to modern production. This is especially true for semiconductors. With Sampling on the Fly, we ensure not only that none of the valuable data needed for the initiation of corrective action is lost, but also that the very low reject levels currently achieved in production are not put at risk during inspection.

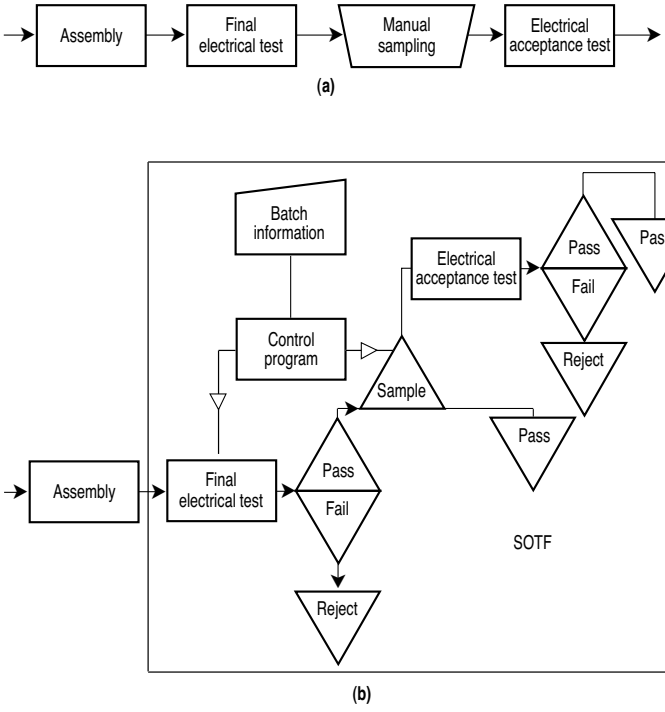


Fig. 1. Compared with the traditional system (a) where batches are sampled manually following final electrical tests, Sampling on the Fly (b) reduces manual handling with associated ESD hazard and the risk of mixing good and reject semiconductors.

Sampling on the Fly

Applying modern data processing and automatic handling techniques to Quality-Control Acceptance testing can result in both improvements in the validity of the procedure and a reduction in the hazards associated with additional handling.
This is the basis of our development of Sampling on the Fly (SOTF), a powerful extension of conventional sampling inspection.
SOTF allows the Group A electrical tests to be integrated with the 100% final electrical inspection. The procedures are compared in Fig. 1, where the reduction in quality-hazarding manual handling due to SOTF is evident. A further benefit is the rigorously-stochastic software-controlled sampling that is an integral feature of the SOTF system. Finally, data recorded from the sampling inspection is available for Statistical Process Control.

SOTF test system

To accommodate SOTF procedures, the automatic test equipment used for the 100% electrical test is augmented by an active terminal. This runs the sampling software and integrates the electrical Acceptance Test sequence with the final electrical test.

Test initiation

At the commencement of the final electrical test run on each batch the following data is entered into the terminal:

- device type
- die lot number
- assembly batch card number
- gross batch quantity
- week code number
- sampling status (normal, tightened or reduced)
- test station number
- budget yield.

From this data the SOTF program is selected automatically; it estimates the quantity of good devices after the test, and initiates the sampling routine. The yield revealed by the test at 10%, 50% and 90% of the batch is checked and the sampling interval simultaneously adjusted to ensure that the required sample is distributed over the full quantity of good devices.

Advantages

Besides the primary benefits of SOTF:

- even distribution of samples over all good devices in a batch
- reduced handling and so reduced hazard;

we have taken the opportunity to collect further data for use in our quality-improvement programme.
After each SOTF run, the terminal generates a summary sheet detailing the attributes (yields, defect rate) of both the 100% and sampling electrical test and the electrical variables in the sample. This shows the distribution of static parameters over the batch. Full device traceability enables this data to be used for the continual process improvement required for progress towards zero defects.

Self-qualification

Self-qualification is a service performed by Philips Semiconductors to provide customers with information concerning the qualification of major changes to any process, material or product.
The purpose is to provide formally-documented, detailed information in advance of the qualification of a product or process, and to conduct a thorough and well-documented programme with results that will help secure customer approval. This activity is intended to minimize the impact on customers' resources, and to expedite the change-approval process so that timely and well-coordinated implementation can be accomplished.
Customers participating in self-qualification are given an opportunity to check the proposed qualification beforehand against their own standards and application-specific conditions. Customers may audit the project, and are given the option of modifying or enhancing the qualification plan according to their needs.

Self-qualification proposal

The self-qualification proposal informs customers of major process or product changes by describing those changes in detail, and by proposing a stress plan to be used in all qualification activities. An interim report is issued when there is a need to modify or change any information prior to final report approval, or when a customer specifically requests immediate information prior to the publication of the final report. The final report describes findings relative to the proposal, and is aimed at satisfying both internal and external customers' reliability requirements. In some cases the final report may be published as a stand-alone document, having no proposal prior to its writing.

Programme review

A Quality Review Board carefully monitors the programme to ensure that all requirements are met.

Each proposal is published at least 30 calendar days prior to initiation of qualification activities.
The final report is released within 30 calendar days after completion of the qualification project (when the last test group has completed its appropriate stress duration), and at least 30 days prior to the expected date of implementation.
The Quality Review Board assesses each self-qualification activity for conformance and accuracy in the following areas:

- Qualification schedule in proposal and interim reports (optional)
- List of affected products
- Process/product attributes
- Benefits derived from the process/product change
- Other reliability considerations, adding to the report's credibility
- Product selection for stress (what and why)
- Plan modifications (if appropriate)
- Definition of stresses and stress conditions
- Qualification samples (including sample sizes)
- Sample description and history
- Burn-in schematics with drawings
- Preliminary stress results (where applicable)
- Detailed stress results (presented in final report)
- Schematics (to accompany text in "Qualification Plan" section). These may either be included in the report or offered "upon request"
- Individual qualification summary pages (Reliability Engineering Project Summary documents)
- Failure Analysis report
- Applicable Structural Similarity rules and results.

Semiconductor Assembly Council (SAC)

SAC is a worldwide organization of semiconductor assembly subcontractors, suppliers and end-users, established to certify subcontract quality systems and control practices. It represents about 95% of the non-Japanese semiconductor industry, and has some Japanese companies among its members as well.
The main function of SAC is to provide subcontractor quality system certification. It also promotes teamwork with suppliers and customers, and provides a forum for discussion of non-proprietary technology issues and best practices, giving an opportunity to benchmark in the industry.
SAC certification is carried out by an audit team of semiconductor specialists coming from within the industry. The audit team represent at least two but usually three semiconductor companies. The SAC Audit Committee continually reviews data from SAC-certified subcontractors in order to monitor their continued compliance to the certification.
SAC procedures also include a de-certification procedure in case of any serious lapse in quality standard by a certified subcontractor.

SAC in Philips Semiconductors

As a SAC member, Philips Semiconductors provides SAC qualified auditors and participates in SAC audit teams. SAC certification is a means of developing the quality system of our subcontractors. We are required to do this by the ISO/TS 16949 Quality System Requirements that we have implemented in all Philips Semiconductor facilities. The SAC standard is compatible with TS 16949.
As a SAC member, Philips Semiconductors has an influence on the audit standard, and also receives the audit reports done by SAC on each assembly subcontractor. It's therefore not necessary for Philips Semiconductors to carry out its own quality system audit on subcontractors, thereby saving time and money.

Six Sigma

The Six Sigma definition used by Philips Semiconductors originated within Motorola. In January 1987, Motorola set as one of its corporate goals to achieve Six Sigma capability within 5 years (i.e. by 1992). When Motorola Inc. won the USA Malcolm Baldrige National Quality Award in 1988, other companies began to benchmark themselves against Motorola. As a result, the Motorola concept of Six Sigma began to be adopted by others (e.g. IBM, Ford). The Motorola goal applies to all areas of the business, not just product and process quality, and is oriented toward approaching the standard of zero defects. The strategy includes the six steps to Six Sigma for manufacturing and another six steps to Six Sigma for non-manufacturing.

The 1991 Philips SPC Conference Six Sigma Definition

"A total business culture involving the dynamic process of identifying key product/service characteristics (as defined by both internal and external customers) and controlling elements followed by the determination of process capability and the continuous reduction of variability leading to the achievement of 3.4 ppm (Cp = 2.0, Cpk = 1.5)."

Refer to the Statistical Process Control section of this handbook for concepts such as Sigma, Process Capability and Capability Indices Cp and Cpk.

Philips Semiconductors quality improvement goals include "improve process capability to achieve 6 Sigma performance by the end of 1994"

Application of Six Sigma within manufacturing

Within manufacturing, variation of a process is measured in standard deviations (Sigma) from the mean. The normal variation, defined as process width, is ± 3 Sigma around the mean (Fig. 1). Approximately 2700 parts per million (ppm) will fall outside the normal variation of ± 3 Sigma. For a product to be manufactured virtually defect-free, it must be designed to accept characteristics which are significantly more than ± 3 Sigma away from the mean.

The way to achieve this is to reduce variability, resulting in a smaller value of Sigma. It can be shown that a design which can accept twice the normal variation of the process (± 6 Sigma) can be expected to have no more than 3.4 ppm for each characteristic (Fig. 2), even if the process mean were to shift ± 1.5 Sigma.

The ± 1.5 Sigma shift allowance is the Motorola contribution to the definition of Six Sigma. A design specification width of ± 6 Sigma and a process width of ± 3 Sigma produces a Cp of 12/6 = 2, as Cp is (by definition) the specification width divided by the process width. Cpk is the distance of the process mean to the nearest specification limit divided by half the process width. In the case of 1.5 Sigma shift, Cpk is (6 - 1.5)/3 = 1.5.

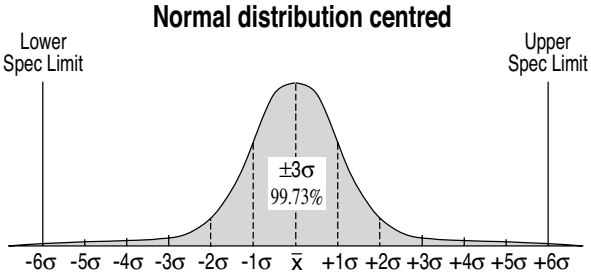
Application of Six Sigma in both non-manufacturing and manufacturing

The concept of defect rate per million opportunities for error (DPMO) can be used in both manufacturing and non-manufacturing areas. The DPMO is an attributes measurement (compared with the variables measurements used to calculate Cp and Cpk). An example of DPMO is the parts per million (ppm) measurement used for electrical and visual mechanical quality (refer to the PPM section of this handbook). A typical example of calculating DPMO in a non-manufacturing area is:

A product or service contains 80 opportunities for

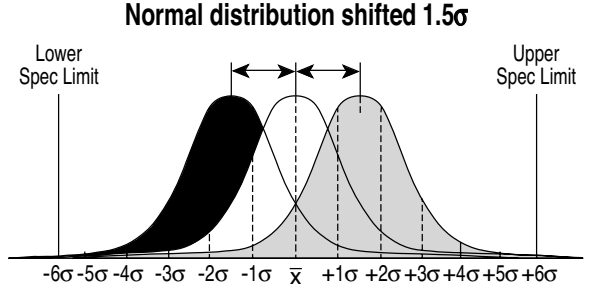
error in 2500 units processed. If 45 defects are discovered, the defect rate is:

$$DPMO = \frac{45 \times 10^6}{2500 \times 80} = 225.$$



SPEC LIMIT	PERCENT	DEFECTIVE PPM
±1 sigma	68.27	317,300
±2 sigma	95.45	45,500
±3 sigma	99.73	2,700
±4 sigma	99.9937	63
±5 sigma	99.999943	0.57
±6 sigma	99.9999998	0.002

Fig. 1. Typical process variations with a centred distribution between Six Sigma limits. Only 2 devices per billion fail to meet the specification target.



SPEC LIMIT	PERCENT	DEFECTIVE PPM
±1 sigma	30.23	697,700
±2 sigma	69.13	308,700
±3 sigma	93.32	66,810
±4 sigma	99.379	6,210
±5 sigma	99.9767	233
±6 sigma	99.99966	3.4

Fig. 2. Effects of a 1.5 Sigma shift, where only 3.4 ppm fail to meet specification.

Soft Errors

Soft errors are temporary failures in electronic circuits. No permanent damage is seen.
SER (soft error rate) is caused mainly by incident alpha-particles from product materials like molding compound, leads, and silicon wafers. Neutrons from cosmic radiation form the second important source of SER. SRAM and DRAM (embedded) memories are the most affected circuits.
The impact on logic circuitry may become critical in future CMOS technologies.

SER becomes worse for advanced technologies with smaller feature sizes, mainly due to smaller capacitances and lower voltages. Customer requirements are usually in the order of 1000 FIT (failures per billion device hours) per product. Requirements depend to a large extent on the application, for instance SER is not expected to be critical in TV and radio circuits. The most effective methods of protecting circuits are to use low-alpha materials (plastic, solder) and on-chip error correction.

SER is measured by:

- accelerated alpha soft error testing of test chips, using Am241 or Th232 alpha sources
- accelerated neutron and proton testing, using neutron or proton beams to estimate cosmic ray SER
- alpha emission tests on wafers and package materials to determine the flux of alpha particles incident on the chip surface
- System SER (SSER) testing - This is an unaccelerated test to assess the true product FIT rate.

Accelerated tests are done on test chips to determine the SER sensitivity of circuits. Based on the results of accelerated tests, emission data from product materials and known cosmic ray intensity a prediction of product SER is made. The SSER test can be done occasionally to verify the prediction models.

Software quality

At a time where applications and components GO DIGITAL the quality of software itself and the capability of software development centres get more and more important. Many organizations within Philips Semiconductors are active in software design. These organizations meet each other in the SMM (Software Managers Meeting) and the SPI (Software Process Improvement) task force.

Software release

The whole Software Development Process including software release is described in the "Overall System Realisation Process" (OSRP). under pww.osrp.sc.philips.com.
The table shows the milestones in the software release and the deliverables per milestone.

Deliverable \ Milestone	Planning	Definition	High level Design	Implementation	Integration & Test	Release	Archiving
Project management plan	S	S	C, S	C, S	I, S		
Software requirements specification	D	I, S					
Software acceptance test specification		I					
Software architectural design			I, C				
Software detailed design				C			
Source code				C			
User documentation			D	I			
Software integration test report					C		
Release note						S	
Performance indicators							C
Software project evaluation							C
Software project archive							S

Legend :
D : Draft (created but not yet cross-checked or inspected)
C : Cross-checked
I : Inspected
S : Signed (by the persons responsible)

Software capability (CMM)

The capability of software development centres is assessed against the Capability Maturity Model (CMM), as described in the publication CMU/SEI-93-TR-24 d.d. February 1993 by the Software Engineering Institute of the Carnegie Mellon University.

In this model starting organizations are at CMM level 1. The highest level is 5.
The levels are called 1: initial, 2: repeatable, 3: defined, 4: managed and 5: optimizing.
The policy of Philips Semiconductors is for all centres to reach at least level 2 in 2001.
Some software centres are certified on level 3.

The requirements for the first levels are given below :

CMM level 2	CMM level 3
Software configuration management	Peer reviews
Software quality assurance	Intergroup communication
Software subcontractor management	Software product engineering
Software project tracking and oversight	Integrated software management
Software project planning	Training program
Requirements management	Organization process definition Organization process focus

Statistical Process Control (SPC)

No machine, operator, batch of parts or raw material can ever be consistently precise: there will always be variations about any specification. Thus, the properties of a product from any production line will vary about the target (median) value; the further characteristic values are from the median value, the less often they should occur, as shown in Fig. 1.

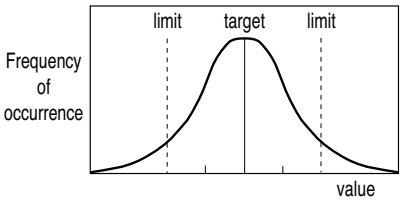


Fig. 1. A typical distribution of the values of the product characteristic. Ideally, the peak (median) value should coincide with the target value for the product, and very few products should be out of limit.

Analysis of the causes of variation (e.g. operator errors, setting errors, faulty raw material spreads) reveals two distinct categories: random (chance) causes and assignable causes (causes that can be identified and corrected). If all the assignable causes of variation can be identified and eliminated, those that remain will be random: due to the natural limitations on accuracy, such as tolerance and noise. When this condition is reached, the process is said to be under control.

Process capability

Once a process has been brought to a state of statistical control, it then becomes possible to engineer it so that its output meets the specification. In Fig. 2(a), the shaded areas represent out-of-limit products, in other words, scrap. Moreover, the most frequently-occuring

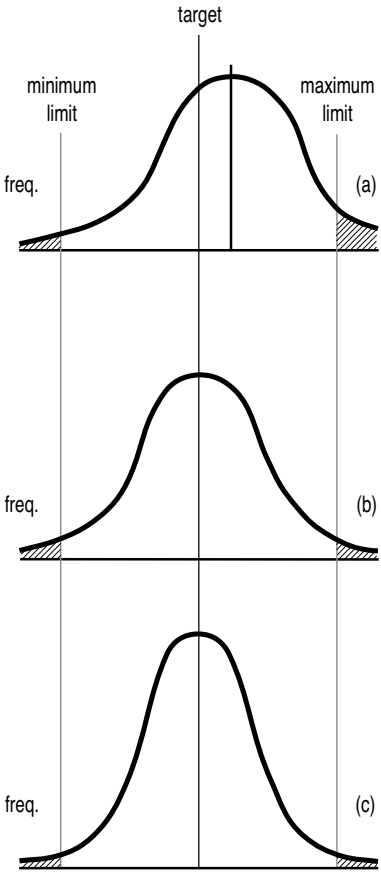


Fig. 2. Analysis of the causes of variations in product characteristics from a process (a) can be used to progressively improve the process (b) so that less scrap (shaded areas) is produced. A process producing negligible scrap for economic purposes (c) is said to be under (statistical) control.

product properties do not coincide with the target specification. By adjustment of conditions, product properties are shifted to peak on the target value; by reducing equipment tolerances and raw

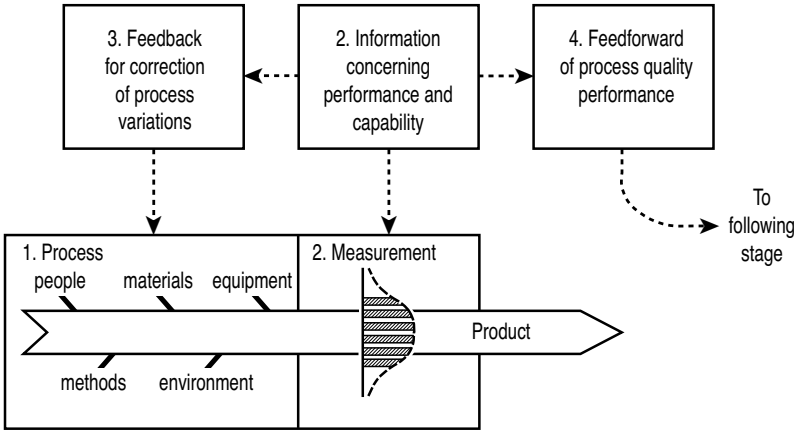


Fig. 3. Statistical Process Control applies feedback around a process to eliminate assignable causes of variation and reduce the effect of random causes. Information generated can also be used to predict product quality for use at later stages in production.

material spreads, the random variations of the product characteristics are progressively reduced, Fig. 2(b), the yield improves, and the costs decrease. When process spreads have been reduced so that virtually the whole output of a process is within specification limits, Fig. 2(c), that process is said to be capable.

Process control system

In its basic form, Statistical Process Control (SPC) works by treating a production process as a control system, and adding that essential element, the feedback loop. Analysis of product properties at each stage of the process reveals assignable variations, and records the extent of the random variations so that corrections can be applied to bring the process under control. Data generated by SPC is also fed forward to warn of extraordinary spreads or deviations, so that corrective action can be planned and any necessary screening instituted.

The principal elements of the type of process-control feedback system using SPC that we operate are shown in Fig. 3.

1. The **process** itself is an interaction of people, equipment, materials, methods and environment, each of which exerts a characteristic influence on the product.
2. **Measurement** monitors output and variation, providing performance and capability information.
3. **Feedback** translates measurement information into action to influence the process towards improved output.
4. **Feedforward** informs the following stage about the distribution of product properties so that compensating measures can be planned or screening instituted.

Control charts

Central to the operation of SPC, the control chart also known as the 'Shewart control chart', compares product characteristics graphically with calculated control limits. Its principal function is the detection of assignable causes of variation in the process.

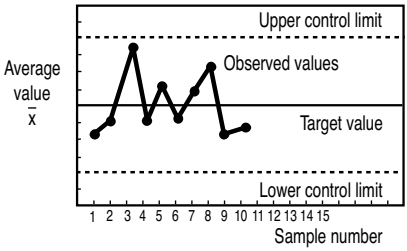


Fig. 4. The control chart, a running plot of average values from regular sample measurement, is fundamental to Statistical Process Control.

A typical SPC control chart is a running plot of the average value of measurements carried out on samples of products, as shown in Fig. 4 with control limits marked. Where control limits are chosen to be + or – 3 times the standard deviation s of the characteristic being monitored, if random causes of variation only are present (with no extraordinary trends), 99.7% of plotted values will fall within the limits. This property can be used as the criterion of process capability. The majority of variations outside 3s control limits will be due to assignable causes, which should be investigated. Besides the average values from samples, a chart of the range (maximum less minimum value) may also be kept. Variations in the average value of range R indicate changes in the uniformity of raw materials, or the state of maintenance of the process equipment or test equipment. As with changes in average values x, so variations in R should be investigated: causes of deteriorations must be corrected; improvements may indicate beneficial changes that could be applied to other processes.
Since control charts are usually available to each operator or displayed at each work station, they are an excellent means of involving everyone directly in the quality aspects of their activity.

Capability criteria

A useful way of relating the results obtained from SPC to the quality of finished products is to relate the specification limits (upper and lower) to the standard deviation s and to the deviation of the process mean M to the target value T.
The potential process capability index (Cp) defines a process in terms of its parameter spread with respect to the defined limits of a specification. It is a function of two variables: the width of the specification and the process spread, where the process spread is measured by 6 Sigma (± 3 Sigma).

$$Cp = \frac{\text{specification width}}{\text{process spread}} = \frac{USL - LSL}{6\ \text{Sigma}}$$

where USL and LSL are the upper and lower specification limits.

Note that Cp measurement does not take into consideration where the distribution is located in relation to the specification.

The process capability index (C_{pk}) measures the actual process capability by taking into consideration where the distribution is located in relation to the specification. For a process parameter distribution that is normal, stable and centred, $Cp = C_{pk}$. If the distribution is not centred, the process capability index C_{pk} = minimum value of

$$\frac{USL - M}{3\sigma} \quad \text{and} \quad \frac{M - LSL}{3\sigma}$$

or (mathematically the same)

$$C_{pk} = \frac{USL - LSL - 2|M - T|}{6\sigma}$$

(| M – T| is the absolute value of M – T).

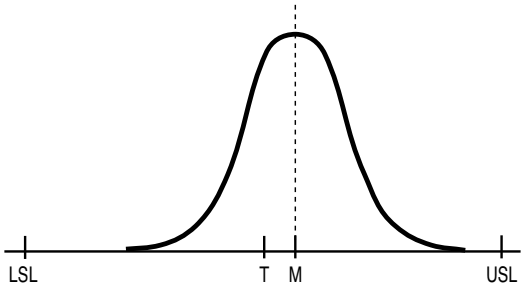


Fig. 5. Lower specification limit (LSL) and upper specification limit (USL) can be defined in terms of the standard deviation σ. M is the process mean, and T the target value (mid-way between USL and LSL).

The capability index shows whether a process is capable of producing products within specification. If the distance of the process mean M to the nearest specification limit is 3σ (USL – M = 3σ), then C_{pk} = 1.
In that case, if the distribution is assumed normal (Gaussian), the chance of products out of specification is P_z = 0.00135, or 1350 ppm. This value applies to one specification limit, so for a symmetrical situation (T=M), the process average would be 2700 ppm.

Values of Pz are tabulated in Table 1, where:

$$Z = \frac{USL - M}{\sigma} \quad \text{or} \quad \frac{M - LSL}{\sigma}$$

With this symbol Z, the capability index can be calculated as C_{pk} = Zmin/3.

Current market requirements for process average are such that most customers regard C_{pk} = 1.33 (Z = 4) as a minimum value for the capability index, the goal being C_{pk} = 1.5

General notes on C_{pk}

- The major use of C_{pk} is to monitor improvement. Consequently, the most valid comparisons that can be made with C_{pk} are those against itself over time. Supplier comparison is not a recommended use of C_{pk}. C_{pk} can be affected by the specification limits, measurement equipment and accuracy.

- C_{pk} variation may be due to insufficient sampling. A minimum sample size of 5 is recommended for calculating x and R per parameter per lot. To establish x and R control limits, a minimum of 10 lots is recommended. A C_{pk} calculation for a parameter of a single lot using a small sample size (e.g. 5) is subject to variation due to insufficient sample size. To obtain a valid C_{pk}, a minimum of 100 measurements (for example 20 samples of 5 each) is required.

- A negative C_{pk} would occur when the mean of the population is outside the specification limit. By definition in such cases Cpk = 0.

- In general, calculation of a composite C_{pk} value for a product group, product, process or

process node, is of limited value due to lack of focus on individual characteristics for future improvement. However this technique is used occasionally for reporting to management or customers. If a composite Cpk index is desired, it is usually represented by the minimum of all indices or a weighted average of the individual characteristic indices.

Benefits

Early warning of deviations provided by SPC before large quantities of defective items have been produced reduces scrap and so helps achieve delivery schedules. Finally, the availability of information in a clear and relevant form makes for more informed commercial and managerial decisions.

Although SPC has long been in use in our semiconductor factories, its application is now being extended and intensified as part of the development of our Quality Assurance system, and the broader Quality Awareness programmes pursued throughout our organization. Statistical Process Control is a powerful tool for monitoring manufacturing processes, revealing variations in product characteristics and identifying the causes. The improved control of a process that results from continued use of SPC increases yield, reduces rework, reduces inspection effort, and lowers costs. The increased volume of information that SPC generates, together with the associated interpretation and organization of data, provides early warning of impending quality problems, and makes for more accurate decisions concerning the changes required to maintain product quality.

Table 1
Values of P_Z for selected values of Z assuming a normal distribution

Z	P_Z	Z	P_Z
6.0	10^{-9}	2.4	0.0082
		2.3	0.0107
		2.2	0.0139
5.5	2×10^{-8}	2.1	0.0179
		2.0	0.0228
5.0	3×10^{-7}		
		1.9	0.0287
		1.8	0.0359
4.5	3.4×10^{-6}	1.7	0.0446
		1.6	0.0548
4.0	0.00003	1.5	0.0668
3.9	0.00005	1.4	0.0808
3.8	0.00007	1.3	0.0968
3.7	0.00011	1.2	0.1151
3.6	0.00016	1.1	0.1357
3.5	0.00023	1.0	0.1587
3.4	0.00034	0.9	0.1841
3.3	0.00048	0.8	0.2119
3.2	0.00069	0.7	0.2420
3.1	0.00097	0.6	0.2743
3.0	0.00135	0.5	0.3085
2.9	0.0019	0.4	0.3446
2.8	0.0026	0.3	0.3821
2.7	0.0035	0.2	0.4207
2.6	0.0047	0.1	0.4602
2.5	0.0062	0.0	0.5000

Use of this table for values of Z greater than 4 should be restricted to cases where the distribution has accurately been measured.

Structural similarity

When a semiconductor device design is modified, a major process step is changed, or a new type has to be qualified, structural similarity can be taken into account in deciding the amount of characterization and qualification (reliability testing) that needs to be carried out. Structural similarity determines the extent to which test results from a specific device or family can be considered representative for other similar types.

When applied to reliability aspects, structural similarity is indispensable in predicting the reliability performance of types similar to those that have been specifically subjected to reliability testing. Not only is reliability testing of every type expensive, it's also unnecessary, since device type itself is less important than the common structural aspects and generic data of the group of types. For example, humidity testing explores the package, the lead finishing, the passivation of the die, the metal deposition and the spread between diffusion batches. Humidity test results are hardly influenced by individual features of a device type (with the exception of operating voltage), so once reliability tests have been completed on one type, it's not necessary to test other structurally-similar types in that specific family.

Structural similarity is also used to determine which types are grouped for reliability monitoring as part of the periodic investigation of conformance to reliability requirements.
The worst-case device (i.e. the most-complex or the largest die size) in a structurally-similar group is usually subject to stressing. A good reliability performance means a high probability of a good performance from other types in the same group, and removes the need to test these other types. Structural similarity is test-dependent, the allowed grouping of types being unique to a specific test. For example, a solderability test may only need to be done on one sample of all the types from one assembly line having a similar pin-count, the same envelope and the same lead-finish. Here, electrical performance and the wafer-fab process are not relevant.

However, other tests may use electrical performance or the wafer-fab process as prime selection criteria for structurally-similar grouping.

There are 2 levels of Structural Similarity:
1. Low: this level is used for reliability monitoring
2. High: this level is used for reliability qualification

Generally the end product, as it is shipped to the customer, consists of three constituents:
1. Wafer Fabrication Process
2. Assembly Process and Package
3. Integrated Circuit Design

For each of these constituents, Structural Similarity is defined

Structural similarity grouping based on wafer process

For Wafer Fabrication Processes, the Structural Similarity levels are:
Level 1 (Wafer Fabrication Process Family):
- Same Wafer Fabrication Process Technology (CMOS, BICMOS, BIPOLAR, BCD, NMOS, PMOS),
- Same Foundry,
  And
- Same technology generation (A technology generation is mainly characterized by feature size, and in addition by new process steps and/or materials. A shrink version is usually not seen as a new technology generation.)

This level is used for reliability monitoring

Level 2: A Wafer Fabrication Process is considered Structurally Similar to a reference Process if it:

- Belongs to the same Wafer Fabrication Process Family (Level 1),
- Has the same layer build-up or has less layers,
- Concerns an equal shrink version,
- Has the same backend technology,
  And
- Has the same voltage range

Structural similarity grouping based on envelope family

For Assembly and Package, the Structural Similarity levels are:

Level 1 (Package Family):

- Same Package technology (e.g. QFP, BGA, SO),
  And
- Same Assembly Plant

Level 2: A Package is considered Structurally Similar to a reference Package if it:

- Belongs to the same Package Family (Level 1)
- Has the same or smaller body size,
- Has the same or lower pin/ball count,
- Has the same or larger outer lead or ball spacing,
- Has the same or larger inner lead spacing,
- Has the same or smaller die pad size,
- Has the same leadframe topology/substrate material,
- Has the same die attach material,
- Has the same wire bond technology: discriminate stitch on ball, or downbonds etc.,
- Has the same moulding compound,
  And
- Has the same construction characteristics: chip-coat, exposed die-pad, fused leads heat-spreader, heat-tape

Structural similarity grouping based on Integrated Circuit Design

Structural Similarity for Integrated Circuit Design is only defined on Level 2 (designs are not monitored). An Integrated Circuit Design is considered Structurally Similar to a reference Design if it:

- Is designed for the same Wafer Fabrication Process Family on level 2,
- Has the same die size category, defined by: $A_{die,1} \leqq 1.3 * A_{die,2} + 10\ [mm^2]$, where $A_{die,1}$: is the area of the larger, and $A_{die,2}$: is the area of the smaller die,
- Has the same cell library (e.g. RAM, ROM, Flash, MIPS-core) and the same I/O library for digital and mixed signal circuitry,
  And
- Has the same design criteria (e.g. frequency, operating temperature, supply voltage, power dissipation and current levels) for analogue, power, memory

Supplier quality system

Purpose

Philips Semiconductors purchases hardware, software, processed materials and services on a large scale, for the manufacture of its high-quality semiconductor products.
Suppliers to Philips Semiconductors must be fully responsible for the quality of their products, thereby consistently ensuring compliance with the quality standards and conditions agreed upon.
The suppliers' quality assurance system should meet at least the ISO 9001 requirements. For a number of purchased products, specific requirements for defect prevention and continuous quality improvement are applicable.
The full requirements are defined in the Philips Semiconductors Supplier Quality System. This system contains the Quality System requirements (SNW–SQ–003) and special requirements per category in series SNW-SQ-011X. It is an essential tool in the selection and qualification process of the suppliers. It also facilitates the development of long-term, mutually supportive, relationships that permit reduction of incoming inspection, inventory and lead-times. In short: increased quality at reduced cost.

Certification requirements

Philips Semiconductors certification of suppliers' quality assurance systems is an essential step towards becoming a fully certified supplier. The supplier certification requirements and procedures depend on the specific nature of the relevant production products.

Strategic and preferred suppliers must be in compliance with, and certified to, the Philips Semiconductors Supplier Quality System requirements, and in addition, to ISO 9001.
All other suppliers must still be in compliance with ISO 9001.
In both cases the certification must be granted by an accredited third-party inspectorate.

Sustainability@Philips Semiconductors

What are we talking about – the definitions

- **Sustainability** is defined as "meeting the needs of the present generation without compromising the ability of future generations to meet their own needs"
- **Sustainable** development is the path to sustainability
- **Sustainable** entrepreneurs are companies pursuing this path

Philips Semiconductors sees sustainable development as one of the most challenging issues and greatest opportunities of the 21st century. The company is committed to business practices that balance economic feasibility with social responsibility within environmental limits - demonstrating our responsibility to People, Profit and the Planet (the 3Ps).

Our Vision And Long-term Commitments:

- Philips Semiconductors' commitment, to using technological expertise to improve the quality of peoples' lives, shapes a variety of short-term goals. Whilst striving for continuous improvement on this basis, the business is shaped by more long-term vision and commitments. Philips Semiconductors is striving to become impact neutral then restorative in the long-term.

Key Goal:

- A key goal of the Sustainability Charter is the pursuit of sustainable development.
  This requires us to monitor and improve our economic, social and environmental performance, then continuously reduce impacts towards zero whilst creating value.

Thermal resistance

The thermal characteristics of semiconductors are a major consideration for both manufacturers and users because high junction temperatures can have an adverse effect on device performance and long-term stability.
When the semiconductor dissipates power it gets hot. The lower the thermal resistance, the quicker the die can dissipate this heat via the lead-frame to the heatsink.
The thermal resistance Rth of the package is measured in °C/W or K/W (K in kelvin) and is a key parameter in the calculation of junction temperature T_j, using the equation:

$$T_j = R_{th}P + T_a,$$

where P is the dissipated power in watts and T_a is the ambient temperature.
Practical measurements of T_j are made to MIL-STD 883C, method 1021.1, using the temperature-sensitive parameter (TSP) technique.

Package design

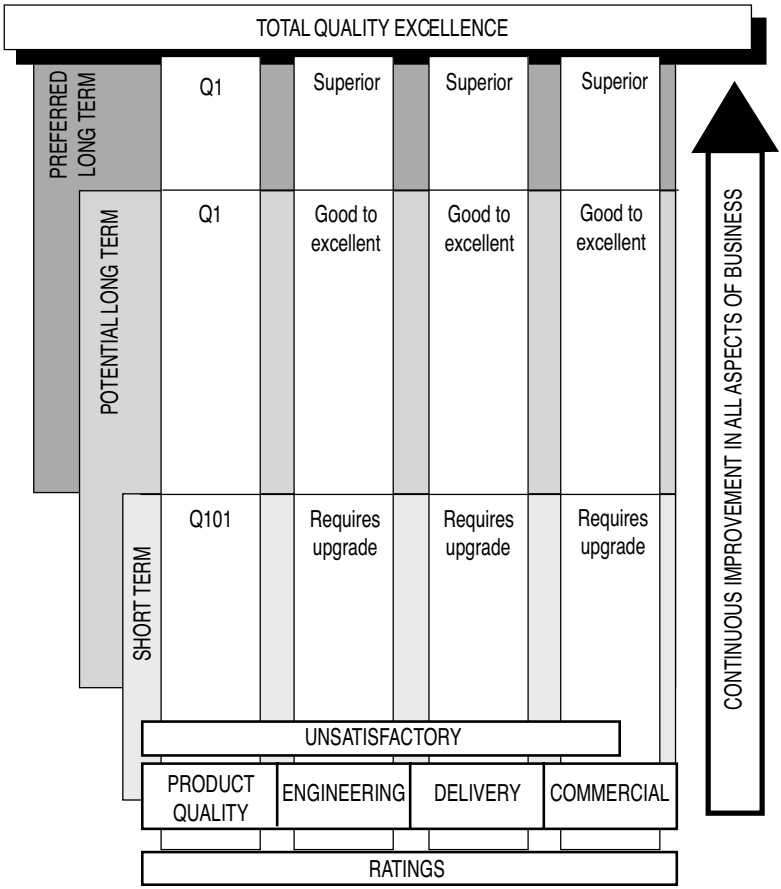
For good thermal performance, it's essential that thermal resistance is kept low by good package design. Some elements of package design affect thermal resistance more than others:

- **Die size** has a large effect on thermal resistance. In general, the smaller the die size, the higher the thermal resistance.
- **Die attach methods and materials** must be carefully selected for maximum reliability, since they can affect thermal resistance.
- **Lead-frame material**, particularly for plastic packages, has a significant effect on thermal resistance. The higher the material's thermal conductivity, the lower will be its thermal resistance, due to the heat-spreading effect of the lead-frame. An alloy 42 lead-frame has a higher thermal resistance than a copper alloy lead-frame. For hermetic packages, which do not use copper lead-frames, the lead-frame material has a less-significant effect on thermal resistance because the thermal conductivity of ceramic is much higher than that of moulded plastic.
- **Lead-frame design**, particularly for plastic packages, must maximize thermal dissipation wherever possible. The design is usually determined by die size and pad layout. However, large pads and support structures help to lower thermal resistance.
- **Bond wires**, due to their small diameter, do not provide a significant thermal path and therefore have little effect on thermal resistance.
- **Package body material** can affect thermal resistance. However, material selection is determined more by reliability and manufacturing constraints than by thermal considerations.
- **Internal heat spreaders** can help to reduce thermal resistance in plastic packages by improving the heat distribution through the package. They are mainly used in power devices for consumer applications. Typically, tests indicate that internal heat spreaders can reduce thermal resistance by:
  - 35 to 40% in PDIL 64 packages
  - 23 to 32% in PLCC 68 packages
  - 9 to12% in SOL 20, 24 and 28 packages.
- **External heatsinks** can help to reduce thermal resistance in power semiconductors. Three varieties of heatsink are in common use: flat-plate heatsinks (including chassis), diecast finned heatsinks and extruded finned heatsinks.
  Heatsink thermal resistance is a function of surface finish. A painted surface will have a greater emissivity than a bright unpainted one.

Total Quality Excellence (TQE)

TQE at the Ford motor company is the highest recognition that full-service suppliers can achieve. It represents a superior level of excellence and continuous improvement in everything suppliers do to meet Ford customers' needs and expectations.
Criteria are based on the Supply Base Management process which focuses on product quality, engineering, delivery, and commercial performance.
It requires a commitment to ensure excellence and continuous improvement in all aspects of business.
It involves executives, management, and its employees in creating a culture that emphasizes: leadership, information analysis, strategic quality planning, human resource utilization, quality assurance of products and services, quality results, and customer satisfaction.

Supply Base Management process



TQE minimum criteria

Unlike Ford Q1, which is awarded on a plant basis, TQE is awarded on a commodity basis.
All supplier plants producing the commodity must hold Q1 for at least one year, and be free of validated initial sample rejections, owner notifications, and recalls for the petitioned commodity from at least six months prior to submission of the TQE petition through the award approval.
Evidence of continuous improvement is required in all four major areas of evaluation:

- product quality
- engineering
- delivery
- commercial.

The TQE award requires also that suppliers provide evidence of how they manage continuous improvement.
Areas of consideration and examples of continuous improvement include, but are not limited to:

- leadership
- information analysis
- strategic quality planning
- human resource utilization
- quality assurance of products and services
- quality results
- customer satisfaction.

In November 1991, Philips Semiconductors as a total organization entered the TQE programme with Ford Electronic Division. All product groups and engineering, delivery and commercial functions have now reached, and are maintaining TQE level.
The TQE Award (see photo) was granted to Philips Semiconductors on November 3rd 1995.

Traceability / ROOTS

It's essential that the manufacturing history and the location of all products manufactured by Philips Semiconductors can be traced at any time. Traceability starts during diffusion, by identifying the diffusion batch. At assembly, the traceability identifiers: date code and PMC (Product Manufacturing Codes for the diffusion and assembly site) are added. The traceability data is marked on the product and printed on the identification label. Traceability is particularly important if quality problems occur. For example, if a quality problem is detected after the delivery of products to a warehouse or customer, Philips Semiconductors will take containment action to limit the damage effects of such faulty products. If the problem is detected while products are in the warehouse, the containment action taken is to block the affected products to prevent delivery to customers. If the problem occurs after delivery to the customer, the containment action taken is to advise the customer and provide specific information to trace the faulty products.

Backward traceability

In case of a customer complaint, a product can be traced back (from its lot-ID) to the production centres where diffusion and assembly took place.

Forward traceability

If a potential quality problem is detected in a certain lot, forward traceability identifies customers who have received products from that lot and/or in which warehouses these products are stored.

Traceability system (ROOTS)

ROOTS (Rapid On-line Overall Traceability System) is operational from the end of 1999. The system contains a database with manufacturing and delivery data. All manufacturing and warehouse systems are connected to this database to feed the traceability data to the system. The database also includes the manufacturing data of the subcontractors. Users can reach the database through Intranet and can define questions (reports) to the database about manufacturing history of lots and about customers to which products of a lot were shipped. The ROOTS dataflow schedule (Fig. 1) on the following page shows the data collection points (oval-shaped) for ROOTS in the life cycle of a product. The main ones are:

DIFS = diffusion start
DIFE = diffusion end
PTSO = pre-test out
ASMS = assembly start
ASMO = assembly out
FTSO = final test out
WHSE = transfer to distribution warehouse
SHIP = shipment to customer.

Further information on ROOTS can be obtained from the ROOTS website:
http://pww-roots.amec.cdc.philips.com/

The traceability process is described in quality standard SNW-SQ-405.

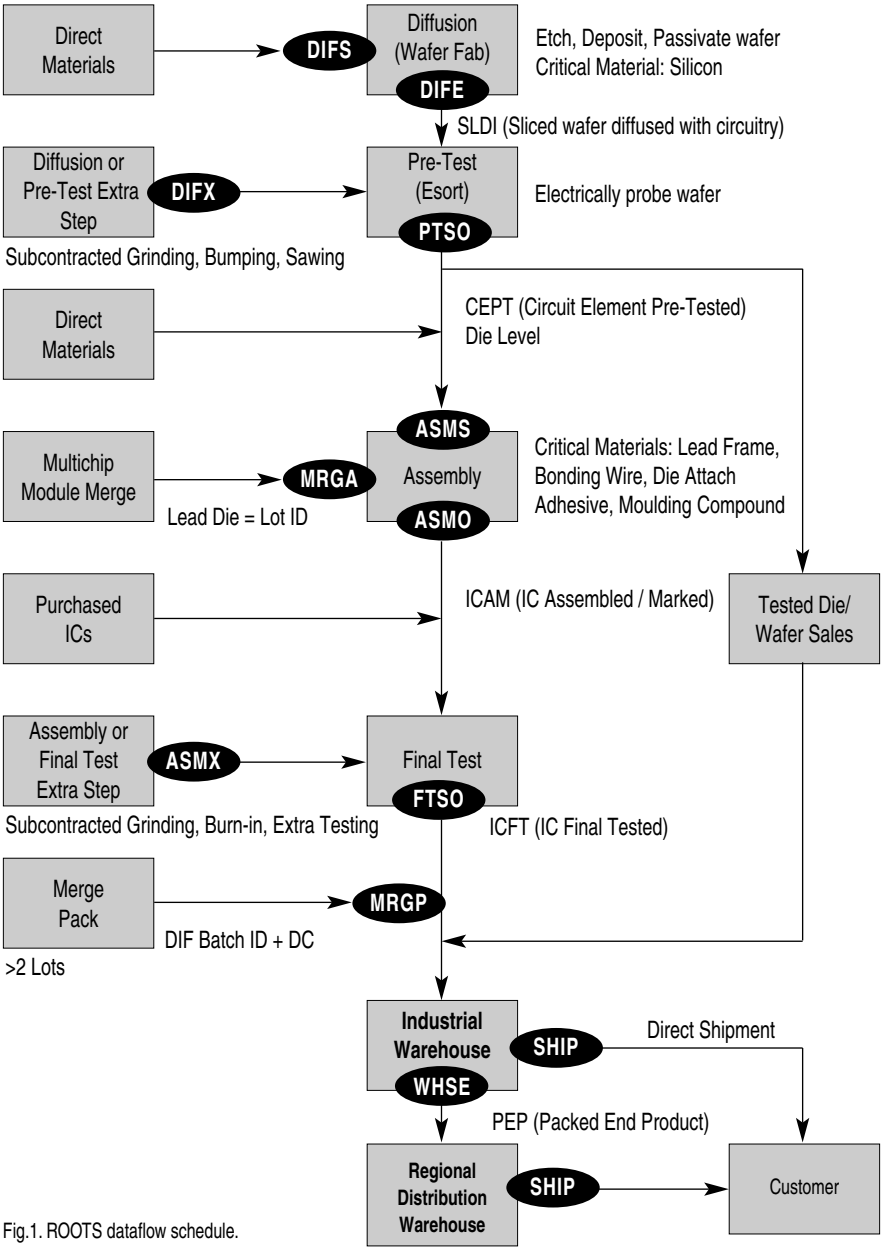


Fig.1. ROOTS dataflow schedule.

Wafer level reliability

Wafer Level Reliability constitutes a set of reliability tests which are done on wafer level, and which address mainly wear-out mechanisms. The tests are usually done on test structures that are designed to accelerate specific failure mechanisms. Some examples of mechanisms are electromigration, hot carrier degradation, gate oxide breakdown, mobile ion instability, stress migration, and junction spiking. The most important mechanisms are described briefly below.

Electromigration

The electron current in metal interconnects exerts a force on the metal atoms which acts in the direction of the electron flow. This causes displacement of the atoms, which can result in voids at places where the electron flux diverges, and in hillocks at places where the electron flux converges. Catastrophic failures occur when a metal line is completely open or when a short circuit between two metal lines develops. Electromigration is tested by forcing a stress current through metal lines at elevated temperature. The acceleration factor (A) is given by Black's equation:

$$A = \left(\frac{J_2}{J_1}\right)^n \cdot \exp\left(\frac{E_a}{k} \cdot \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

Where J1 and J 2 are the current densities at use and stress conditions respectively, T1 and T2 are the corresponding absolute temperatures and k = Boltzmann's constant (8.6 x 10-5eV/K).
The activation energy (Ea) depends on details of the backend process, and lies usually between 0.5 and 1 eV. For AC currents the degradation is reduced compared to DC, due to duty cycling and healing effects. For frequencies >1 kHz electromigration does not cause measurable degradation.

Hot carrier degradation

The electric field in the channel of a MOS transistor in saturation reaches a maximum value near the drain. In this small region of high electric field, electrons or holes are accelerated to velocities higher than the thermal velocity. Under certain bias conditions these hot carriers drift to the Si-SiO2 interface where they can generate interface traps, or pass the energy barrier at the interface and get trapped in the oxide. The result is a shift in the characteristics of the transistor. The degradation increases with decreasing channel length, and is a concern for sub-micron technologies. Hot carrier degradation is tested on MOS transistors under worst-case bias conditions. The acceleration factors (A) are given by the equations:

- for NMOST

$$A = \exp\left(B \cdot \left(\frac{1}{V_{ds1}} - \frac{1}{V_{ds2}}\right)\right) * \left(\frac{L_{eff1}}{L_{eff2}}\right)^c$$

- for PMOST

$$A = \exp\left(B \cdot \left(\frac{1}{V_{ds1}} - \frac{1}{V_{ds2}}\right)\right) * \exp\left(C \cdot \sqrt{\frac{L_{eff1}}{L_{eff2}}}\right)$$

Vds1 and Vds2 are the drain-source voltages under use and stress conditions respectively; Leff1 and Leff2 are the effective channel lengths of the transistor in the product and test structure respectively; B , c and C are process-dependent constants. Under AC bias conditions the transistor stays in the worst-case situation for only a fraction of the time. This gives a cycle time reduction factor of the degradation, which can amount to more than an order of magnitude.

Gate oxide breakdown

Thin gate oxides suffer from electrical breakdown under electrical field stress. There are several theories for the breakdown mechanism, but there is no general agreement yet. Gate oxide breakdown is tested on MOS capacitors by applying electrical stress. In the EBD test the oxide is stressed with a ramped voltage until breakdown and the breakdown field (EBD) is determined.

The QBD test applies a constant or stepped current until breakdown, and the total injected charge to breakdown (QBD) is determined.

The TDDB (time-dependent dielectric breakdown) test stresses the oxide with a constant voltage until breakdown. This test allows extrapolation of test results to use conditions. The most conservative acceleration factor is given by the E-model:

$$A = \exp\ (\gamma \cdot (E2 - E1))$$

where E1 and E2 are the oxide fields in use and in stress conditions respectively, and „ is a constant.

Bias Temperature Instability

Advanced CMOS processes (0.18 µm and below) are vulnerable to Bias Temperature Instabilities. The transistors degrade under negative or positive gate-source bias at high temperatures. The effect of degradation is a shift of the transistor parameters with time, caused by an increase of both the interface state density and fixed oxide charge. The most important parameters are the threshold voltage and the saturation current.

The effect occurs in all types of transistors, but PMOS transistors degrade more than NMOS transistors, and in dual gate oxide processes it is the thick oxide transistor that degrades most.

The degradation mechanism is still subject of study. The following model has been found to fit the measured degradation of the threshold voltage of GO2-PMOSTs:

$$|\Delta V_T| = A \times t^m \times V^n \times e^{-Ea/kT}$$

Where

- ΔV_T = the worst-case threshold voltage shift (mV)
- A = weight coefficient
- t = stress time (s)
- m = time power coefficient
- V = gate-source, drain or substrate voltage (V)
- n = voltage acceleration coefficient
- E_a = activation energy (eV)
- K = Boltzmann constant (8.617e-5 eV/K)
- T = temperature (K)

Weibull

Weibull probability paper and the associated analysis procedures are used extensively to analyse the results of reliability testing. Given sufficient results, it is possible to obtain indications of the number and characteristics of failure mechanisms quickly, and to predict useful life. During investigations into fatigue phenomena in metals, W. Weibull arrived in 1939 at the formula for a family of distributions named after him. The curve of the Weibull function varies according to the numerical values of the parameters, Fig. 1, especially shape factor ß. When ß is unity, the Weibull function reduces to the eponential distribution. When ß = 3.44, the distribution is normal (Gaussian). In its most general form, the Weibull formula is:

$$R(t) = \exp - \left\{ (t - g)/n - g) \right\}^{\beta}$$

Here, R(t) is the instantaneous reliability after time t, n is the characteristic life (the time to 63.2% failures), and g is the time during which no failures occur.

In practice, Weibull methods make it possible to determine in a straightforward way which distribution best fits a set of data. In practice, this is usually done using Weibull probability paper, as shown in Fig. 2, in which the vertical axis is proportional to InIn1/R(t). The horizontal axis is a log scale of time. Where, for a given set of test conditions, points plotted on the chart lie on a straight line, it is likely that a single failure mode is involved and a Weibull distribution applies.

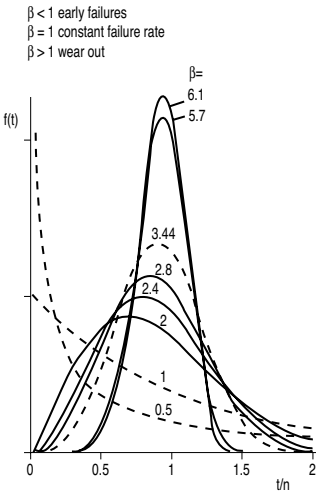


Fig. 1. The Weibull family of distributions varies with the values of the parameters used, especially shape factor ß. When ß is unity, the distribution is exponential.

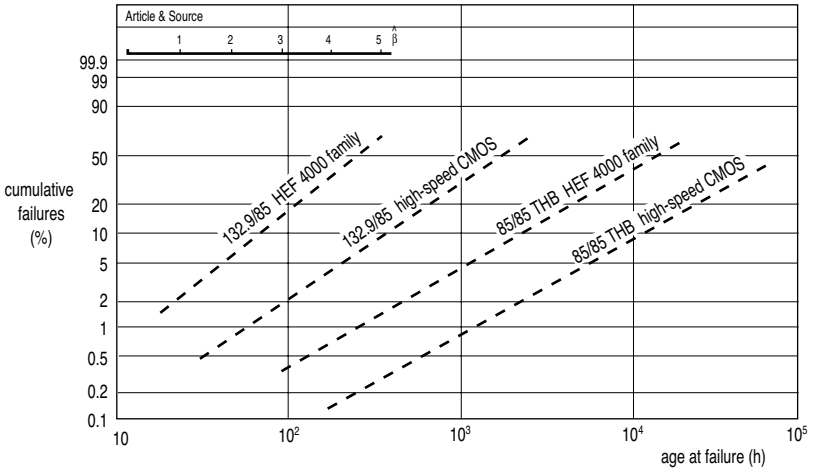


Fig. 2. Weibull plots of cumulative percentage failure against time. This example, taken from Technical Publication 249, compares the results of standard (85/85) and accelerated (132.9/85) humidity tests on CMOS ICs.

Weibull analysis of the bathtub curve – the characteristic plot of failure rate versus time, Fig. 3 – of a semiconductor might reveal an initial region where ß<1 (early failures), with a final region where ß>1 (wearout), Fig. 4. Plotted on a Weibull chart, these would resolve into two lines representing the dominant early-failure and wearout mechanisms, Fig. 5.

The Weibull shape factor ß is the directional coefficient of the line that best fits cumulative failure/life points plotted onto a Weibull chart.

With charts provided with a ß estimation point and scale, Fig. 6, ß may be found by drawing a vertical to the (straight) line of best fit of the plotted points that passes through the ß estimation point, and reading ß from the scale. Characteristic life h is, of course, the intersection between the best fit line and the 63.2% cumulative failure level. Since the origin of the chart is at a low value of cumulative failures, it is usually sufficient to take the intersection between the best fit line and the time axis as the value of g.

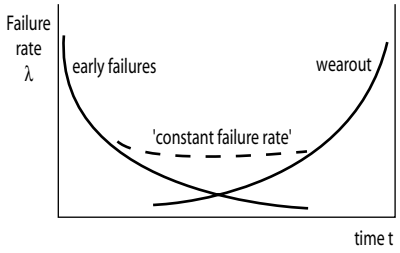


Fig. 3. The variation of failure rate with the life of a device is typified by the bathtub curve.
(Note: the constant failure rate region (dashed) is a combination of the end of the early failures period and the beginning of the wearout period.)

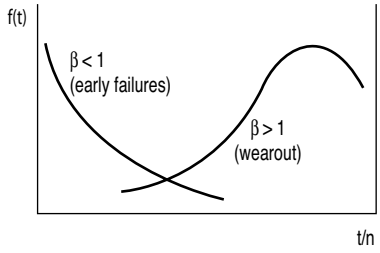


Fig. 4. The bathtub curve of a given device type might be resolved into two Weibull distributions for the early failures and for wearout.

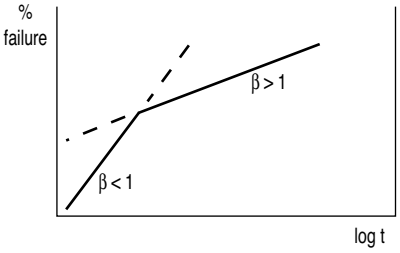


Fig. 5. A Weibull plot of the results of a life test on a sample of the devices of Fig. 4 would reveal two distinct regions corresponding to the two types of failure.

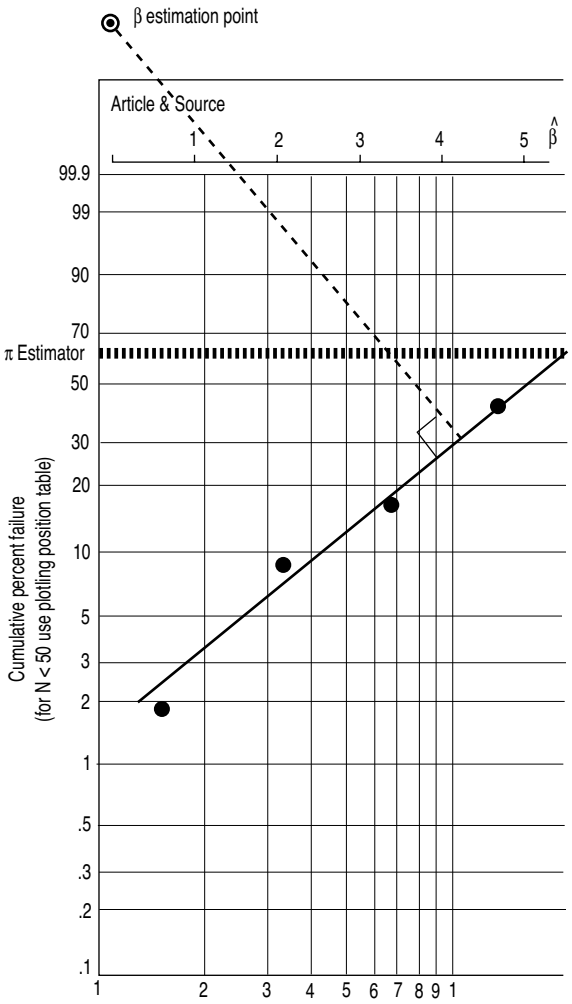


Fig. 6. Use of the ß estimation point. A vertical to the line of best fit intersects the ß scale at the value corresponding to the failure distribution of the results plotted.

Part 3

Keywords

Keywords

A

accelerated test:
A test in which the applied stress level is chosen to exceed that stated in the reference conditions in order to shorten the time required to observe the stress response of the item, or magnify the response in a given time. To be valid, an accelerated test shall not alter the basic modes and mechanisms of failure, or their relative prevalence. IEC 50 (191).

acceptance:
A conclusion that a batch, lot or quantity of product, material or service satisfies the requirement criteria based on the information obtained from the sample(s).

acceptance criteria (in statistics):
Specification criteria for acceptance of individual (quality) characteristics.

acceptance inspection:
Inspection to determine whether an item, lot or service delivered or offered for delivery is acceptable.

alert: see **customer advisory.**

approval:
Declaration by a body vested with the necessary authority that a set of published criteria has been fulfilled.

assessed reliability:
The reliability of an item determined by a limiting value or values of the confidence interval associated with a stated confidence level, based on the same data as the observed reliability of nominally identical items. IEC 50 (191).

audits:
A Quality Audit is an independent, in-depth examination of the documentation and implementation of instructions and quality methods, especially for a production line or factory, but also for stores and other activities.
Such audits often reveal deficiencies that have been ignored or missed by the people operating the department concerned, or stimulate the solution of problems that limit achievable quality levels.
Audits are usually performed by one or more small teams – two members per team is typical – who spend a few days (depending on the size of the operation) observing working practices and checking documentation. Audits may be performed either by customers, third parties, government agencies or by corporate quality management. Before the actual audit, the Quality Manual and other publications describing the activity are usually examined by the auditor.
A typical audit might start by the audit team being introduced to key people; the auditors may then decide to divide activities between teams, allocating particular departments to each team. Following their examination of the working areas and documentation, the audit teams may interview individuals to discuss specific problems that have been revealed. After a final discussion, the auditors then prepare a report for circulation to key people in the organization audited. After some time, there may be a follow-up meeting to assess the value of the audit recommendations.
Since audits are regularly performed by major customers or government agencies, it is essential that only accurate information is provided, whether directly or by publications. To organize this in a professional way, required customer-audits should be notified to the PD-auditor who will coordinate the required actions.

average outgoing quality (AOQ):
The expected average quality level of outgoing product for a given value of incoming product quality. Unless otherwise specified, the average outgoing quality (AOQ) is computed over all accepted lots plus not-accepted lots after the latter have been inspected 100% and the nonconforming items have been replaced by good items.

B

backward traceability:
Tracing back a product to the production centres and to the manufacturing dates for each process step.

batch:
A definite quantity of some commodity manufactured or produced under conditions which are presumed uniform. (ISO Guide 30)

bathtub curve:
A plot of failure rate against time that resembles a cross-section of a bath.

C

call rate:
The call rate of a set is the number of repairs per guarantee period per 100 sets sold expressed as a percentage (%).

concession:
Written authorization to use or release a quantity of material or components already produced but which do not conform to the specified requirements.

conformity:
The fulfilment of a specified requirement by a quality characteristic of an item or service, the assessment of which does not depend essentially on the passage of time.

control chart:
A chart, with upper and/or lower control limits, on which values of some statistical measure for a series of samples or sub-groups are plotted. The chart frequently shows a central line to assist detection of a trend of plotted values towards either control limit.

control limits:
The levels indicating the upper and lower boundaries within which a particular variable may fluctuate in a given period without any actions required to be taken.

corrective action:
An action required by a user from its supplier to correct quality hazards and so prevent recurrence.

critical defect:
A defect that, according to judgement and experience, is likely to result in hazardous or unsafe conditions for individuals using, maintaining, or depending upon the considered product, or that is likely to prevent performance of the function of a major end item.

customer advisory:
Notification to the customer about a quality problem occurring in one of the lots of a certain product.

D

defect:
The nonfulfilment of intended usage requirements. (ISO 3402).

defect (major):
A defect, other than critical, that is likely to result in a failure or to reduce the usability of the considered product for its intended purpose.

defect (minor):
A defect that is not likely to reduce materially the usability of the considered product for its intended purpose, or that is a departure from established specifications having little bearing on the effective use or operation of this product.

derating:
1. Reduction of the intensity of stress for the purpose of gaining an advantage at another point, e.g. improvement of reliability.
2. Translation of the test result under accelerated conditions to a result under normal operating conditions, by the use of calculation models.

design review:
A formal, documented, comprehensive and systematic examination of a design to evaluate the design requirements and the capability of the design to meet these requirements and to identify problems and propose solutions. (ISO 8402).

double sampling:
Sampling inspection in which the inspection of the first sample of the size given by the sampling plan leads to a decision to accept a lot, not to accept it, or to take a second sample of the size given by the sampling plan; the inspection of the second sample then leads to a decision of acceptance or non-acceptance.

E

early failure period:
That possible early period, beginning at a stated time and during which the failure rate decreases rapidly in comparison with that of the subsequent period. IEC 50 (191).

endurance test (in quality):
An experiment carried out over a period of time to investigate how the properties of an item are affected by application of stated stresses and their duration. IEC 50 (191).

environment (in environmental testing):
All external physical conditions that may influence the performance of an item.

estimated process quality:
The ppm level detected in sampling inspection recalculated in relation to lot size.

F

failure:
The termination of the ability of an item to perform a required function. IEC 50 (191).
(catastrophic): Failure which is both sudden and complete. IEC 50 (191).
(complete): Failure resulting from deviations in characteristic(s) beyond specified limits such as to cause complete lack of the required function. IEC 50 (191).
(critical): Failure which is likely to cause injury to persons or significant damage to material. IEC 50 (191).
(gradual): Failure that could be anticipated by prior examination or monitoring. IEC 50 (191).
(major): Failure, other than a critical failure, which is likely to reduce the ability of a more complex

item to perform its required function. IEC 50 (191).
(minor): Failure, other than a critical failure, which does not reduce the ability of a more complex item to perform its required function. IEC 50 (191).
(misuse): Failure attributable to the application of stresses beyond the stated capabilities of the item. IEC 50 (191).
(partial): Failure resulting from deviations in characteristic(s) beyond specified limits, but not such as to cause complete lack of the required function. IEC 50 (191).
(sudden): Failure that could not be anticipated by prior examination or monitoring. IEC 50 (191).

failure mechanism:
The physical, chemical or other process which results in failure. IEC 50 (191).

failure rate:
For the stated period in the life of an item, the ratio of the total number of failures in a sample to the cumulative time on that sample. The failure rate is to be associated with particular and stated time intervals (or summation of intervals) in the life of the items, and with stated conditions. IEC 50 (191).

fall-off rate:
The observed number of failures in the production line, expressed in ppm. IEC 50 (191).

field call rate:
See **call rate.**

field data:
Data from observations during field use. IEC 50 (191).

final inspection:
Lot inspection carried out at the end of a production line.

fitness for use:
The ability of a product, a process or a service to fulfil a defined purpose under specific conditions.

FITS (failures in time standard):
failures in 109 hours.

forward traceability:
Tracing a lot to the customers and/or stores which have received products from that lot, and tracing the corresponding shipment data.

G

H

I

incoming inspection:
Lot inspection by a consumer on a lot delivered or offered for delivery.

in-process (in-line) **inspection:**
Product inspection carried out at various discrete stages in manufacture.

inspection:
Activities such as measuring, examining, testing, or gauging one or more characteristics of a product or service and comparing these with specified requirements to determine conformity. (ISO 8402).

inspection (100%):
Inspection of every item of product, process or service, i.e. the whole (as contrasted with any form of sampling inspection).

inspection by attributes:
A method which consists in taking note, for every item of a population or of a sample taken from this population, of the presence or absence of a certain qualitative characteristic (attribute) and in counting how many items have or do not have this characteristic.

inspection by variables:
A method which consists of measuring a quantitative characteristic for each item of a population or of a sample taken from this population.

inspection level:
An index of the relative amount of inspection of a sampling scheme, chosen in advance and relating the size of samples to the lot size, so that a lower (higher) intensity can be selected if past experience shows that this will be satisfactory.

J

Just In Time (JIT):
JIT production is a pull-through system as opposed to producing for stock. Upstream operations build only as much product as downstream operations request. Also, purchased parts or materials are received only in the quantities that the downstream operations need. The primary advantage is low inventory costs. Stocks are a major problem: they absorb capital, are subject to handling errors and damage, and delay the discovery of production problems.
The system demands that product is produced right first time and without delay. This requires well optimized processes for manufacturing, planning and purchasing and requires a high level of workforce involvement.

K

L

liability (product or service):
A generic term used to describe the onus on a producer or others to make restitution for loss related to personal injury, property damage or other harm caused by a product or service. The limits on liability may vary from country to country according to national legislation. (ISO 8402).

lot:
See **batch.**

lot-by-lot inspection:
Inspection of products submitted in a series of lots.

lot tolerance percent defective (LTPD):
A quality level which in a sampling plan corresponds to a specified and relatively low probability of acceptance (usually 10%).

M

mark of conformity:
A mark attesting that a product or a service is in conformity with specific standards or technical specifications.

market-driven quality (MDQ):
The partnership programme of IBM with its suppliers. The programme is aimed at 'Quality, driven by market needs, that achieves total customer satisfaction through the delivery of timely, defect-free solutions that offer the best value to customers'.
IBM's market-driven principles are:

1. Make the customer the final arbiter.
2. Understand our market.
3. Commit to leadership in the markets we choose to serve.
4. Execute with excellence across our enterprise.

material specification:
The document that describes in detail the materials, components, or supplies used in manufacturing the item.

maverick lot:
A lot having an actual or potential problem that may go undetected until its use in the final application. The problem can be in the field of quality, reliability or functionality.

mean time between failures (MTBF):
For a stated period in the life of an item, the mean value of the length of time between consecutive failures, computed as the ratio of the cumulative observed time to the number of failures, under stated conditions. IEC 50 (191).

mean time to failure (MTTF):
For a stated period in the life of an item, the ratio of the cumulative time for a sample to the total number of failures in the sample during the period, under stated conditions. IEC 50 (191).

merge (traceability):
The function in which multiple lots are combined into one lot.

N

nonconformity:
The nonfulfilment of specified requirements. (ISO 3402).

normal inspection:
The inspection which is used when there is no reason to think that the quality level of the production differs from the acceptable level provided for.

O

observed reliability (of non-repaired items):
For a stated period of time, the ratio of the number of items which performed their functions satisfactorily at the end of the period to the total number of items in the sample at the beginning of the period. IEC 50 (191).

P

parameter:
A variable in a system whose magnitude is determined by influences outside that system.

performance test:
A test for assessing a performance characteristic directly or through simulation of the influencing factors occuring in use, sometimes under more severe conditions.

population:
The totality of items under consideration.

predicted failure rate:
For the stated conditions of use, and taking into account the design of an item, the failure rate computed from the observed, assessed or extrapolated failure rates of its parts.

probability:
A real number in the scale 0 to 1 attached to a random event. It can be related to a long run relative frequency or occurrence or degree of belief

that an event will occur. The scale 0 to 1 can be expressed as a percentage. 100% is certainty.

probability of acceptance:
When using a given sampling plan, the probability that a lot will be accepted when the lot or process is of a given quality.

probability of rejection:
The probability that a lot of a given quality will be rejected by a given sampling plan.

process:
The method of operation in any particular stage of any element, group of elements or total aspect of production or service.

process average:
The process level averaged over a defined time period or quantity of production.

process capability:
A measure of inherent process variability.

process inspection:
Inspection of a process by examination of the process itself or of the product characteristics at the appropriate stage(s) of the process.

process quality control:
That part of quality control that is concerned with maintaining process variability within the required limits.

process under statistical control:
A process, the mean and variability of which remain stable with no adverse trends.

product-hold:
The function to prevent delivery of products from a certain lot.

product qualification package:
At the introduction of new products, or after significant changes in products (or processes), a set of quality and reliability information must be made available. This information can be based on generic data of the product family supported by type-specific data indicating that set targets will be reached. This product qualification package must be suitable for giving to customers.

Q

qualification approval:
The status given to a manufacturer's production unit, whose product has been shown to meet all the requirements of the product specification and quality plan.

quality:
The totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs. (ISO 8402).

quality assurance:
All those planned and systematic actions necessary to provide adequate confidence that a product or service will satisfy requirements for quality. (ISO 8402).

quality audit:
A systematic and independent examination to determine whether quality activities and related results comply with planned arrangements and whether these arrangements are implemented effectively and are suitable to achieve objectives. (ISO 8402).

quality control:
The operational techniques and activities that are used to fulfil requirements for quality. (ISO 8402).

quality level:
Any relative quality measure obtained by comparing observed values with the relevant requirements.

quality management:
That aspect of the overall management function that determines and implements the quality policy. (ISO 8402).

quality manual:
A document setting out the general quality policies, procedures and practices of an organization.

quality operating system (QOS):
A Ford methodology focused on Continuous Improvement, QOS requires the gathering of recent data on business key parameters, which are relevant for the department concerned. Quality operating systems are used for each level of the business chain. The data is analyzed and presented in such a way that it can be quickly reviewed by management. In this way QOS provides a systematic method of monitoring performance improvement on key parameters, and at the same time allows for a data-driven management approach towards problem recognition.

quality plan:
A document setting out the specific quality practices, resources and sequence of activities relevant to a particular product, service, contract or project. (ISO 8402).

quality policy:
The overall quality intentions and direction of an organization as regards quality, as formally expressed by top management. (ISO 8402).

quality system:
The organizational structure, responsibilities, procedures, processes and resources for implementing quality management. (ISO 8402).

R

range:
The difference between the greatest and the smallest observed values of a quantitative characteristic.

rejection:
A conclusion that a quantity of a product, material or service has not been shown to satisfy the requirement criteria based on the information obtained from the sample(s).

reliability:
The ability of an item to perform a required function under stated conditions for a stated period of time. IEC 50 (191).

repeatability (of measurements):
The closeness of the agreement between the results of successive measurements of the same quantity carried out by the same method, by the same observer, with the same measuring instruments, in the same laboratory at quite short intervals of time. (ISO GUIDE 30).

risk:
The combined effect of the probability of occurrence of an undesirable event, and the magnitude of the event.

rogue lot (batch):
A lot rejected under circumstances indicating a fundamental processing error, such as mishandling. A rogue lot is usually defined as being a lot for which the sampling inspection result indicated a less than 5% chance of acceptance according to the relevant sampling system.

S

sample (of a reference material):
A representative quantity of material extracted from a batch of reference material. (ISO GUIDE 30).

sampling inspection:
The inspection of products, processes or services using samples (as distinct from 100% inspection).

sampling plan:
A specific plan which states sample size(s) to be used and the associated acceptance criteria.

sampling system:
A collection of sampling schemes, e.g. one indexed by lot-size ranges, inspection levels and AQLs.

screening inspection:
Complete inspection, i.e. 100% examination of a quantity of material or items of a product, with rejection of all items or portions found nonconforming.

screening test:
A test, or combination of tests, intended to remove unsatisfactory items or those likely to exhibit early failures. IEC 50 (191).

Shewart control chart:
1. A chart for controlling a process by attributes using percent nonconformity
2. A chart for controlling a process by variables using charts for controlling the central location and the dispersion.

Shewart control limits:
In a control chart, the limit below which (upper limit) or above which (lower limit) or the limits between which the statistic under consideration lies with a very high probability when the process is under control.

specification:
The document that prescribes the requirements with which the product or service has to conform. (ISO 8402).

split (traceability):
The function in which a single lot is divided into two or more separate lots.

standard deviation:
The square root of the variance (see variance).

state of statistical control:
A state in which the variations among the observed sampling results can be attributed to a system of chance causes which does not appear to change with time.

statistical process control (SPC):
The application of statistical quality control to individual process stages.

statistical quality control:
That part of quality control in which statistical techniques are used.

T

target specification:
The document that describes the primary purpose of an item and gives the essential guidance concerning such matters as its style, grade, performance, appearance, conditions of use (including health and safety considerations), characteristics, packaging, conformity, reliability, maintenance, etc.

test specification:
The document that describes in detail the methods of conducting tests including, if necessary, the criteria for assessing the result.

tightened inspection:
The inspection, more severe than the normal inspection, to be applied when the inspection results of a number of lots indicate that the quality level of the production is below specifications.

traceability:
The ability to trace the history, application or location of an item or activity, or similar items or activities, by means of recorded identification. (ISO 3402).
(backward): A product is traced back to the production centres for diffusion, assembly, testing and packout to the manufacturing processes and quality data. This is needed in the case of a customer complaint.
(forward): The customers who received products of a certain lot, are traced. This is needed for an advisory, when customers must be warned for a (potential) quality problem in a certain lot.

type approval:
Approval of a certain product or group of products considered by the approval body as representative for the continuous production.

U

useful life:
The period from a stated time, during which, under stated conditions, an item has an acceptable failure rate, or until an unrepairable failure occurs. IEC 50 (191).

V

variance:
The sum of the squares of the difference between the values of the number of observations and the arithmetic means of these observations divided by the number of observations.

verification of reject:
The process whereby, following examination by the supplier, an item rejected as unserviceable at some stage in its use is agreed to contain one or more defects according to the agreed specification.

verification sampling:
A sampling scheme to ascertain whether the producer's sampling procedures are in accordance with his declared sampling scheme.

W

waiver:
1. For material or products see concession.
2. For procedures, a written authorization to deviate from a specified requirement. This waiver must be temporary, the end date being part of the written authorization.

warning limits:
In a control chart, the limit below which (upper limit) or above which (lower limit) or the limits between the statistic under consideration lies with a high probability when the process is under control.

wear-out failure:
Failure whose probability of occurrence increases with the passage of time and which occurs as a result of processes which are characteristic of the population.

X

Y

Z

zero-defect philosophy:
The principle that no defect level is acceptable, but that all defect causes should be traced and eliminated in the quest for perfect products. Note that 'zero' can never be a target for process-average reject levels since such targets, by definition, must be both achievable and measurable.

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