

# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JUNE 1978

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**MICROPROGRAMMED  
CPU ARCHITECTURE  
OFFERS USER-ALTERABLE  
MINICOMPUTER PERFORMANCE**

**DESIGN CONSIDERATIONS FOR  
DUAL-DENSITY DISKETTE CONTROLLERS**

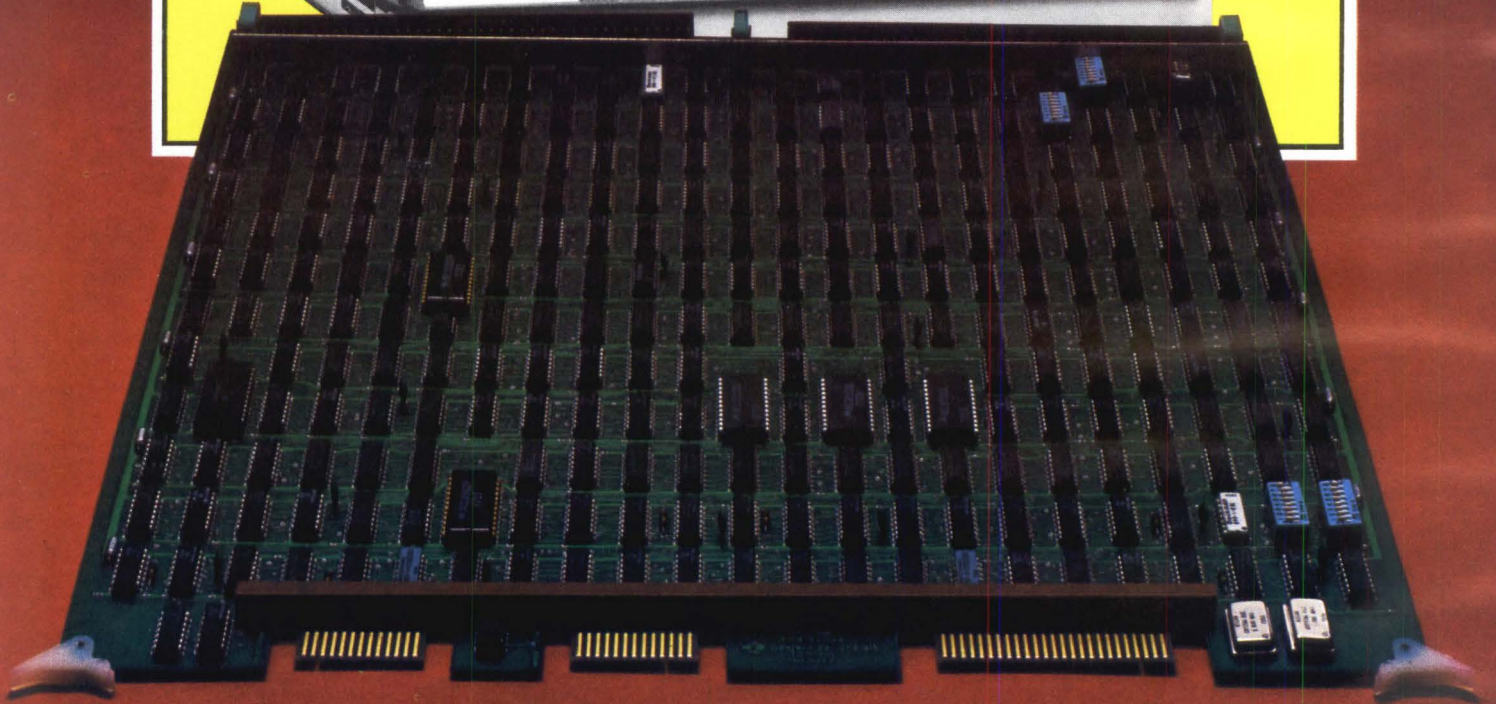
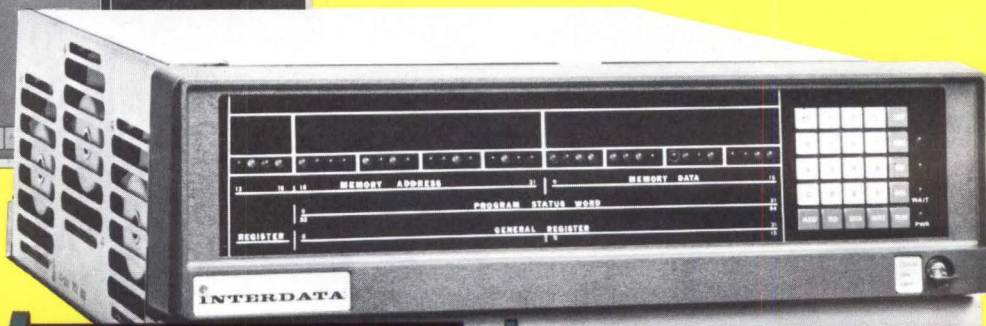
**SOFTWARE ANALYSES FOR COMBINATORIAL LOGIC**



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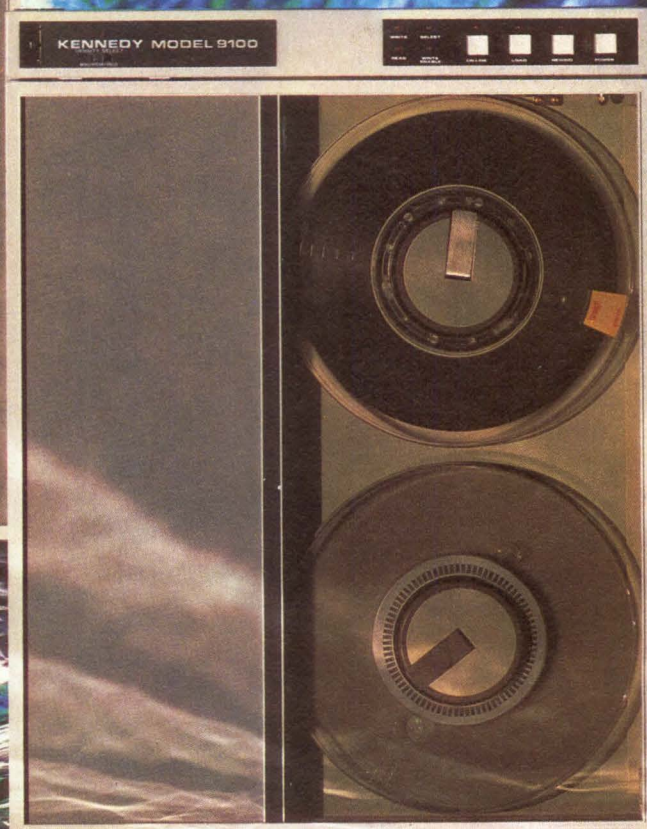
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# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

JUNE 1978

VOLUME 17, NUMBER 6

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Design constrained to emulate its family of predecessors except for the targeted microprogrammable CPU, the resultant minicomputer executes the expanded and powerful attributes of microcode to achieve comparable hardware throughput rates at reasonable cost

### DESIGN CONSIDERATIONS FOR DUAL-DENSITY DISKETTE CONTROLLERS 103

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by Paul Prazak

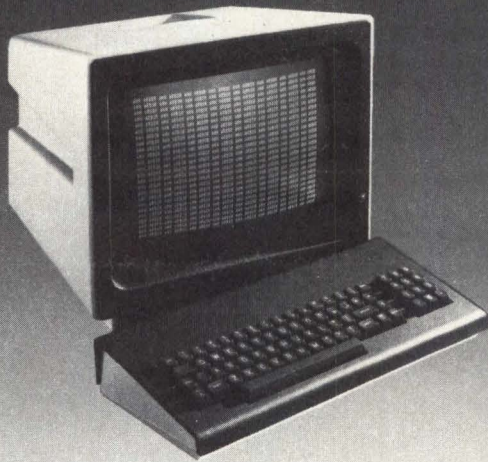
Determining static errors of a D-A converter is a time-consuming task unless an elaborate test setup is available; however, it is possible to evaluate D-A converter performance in less than a minute with only a power supply, digital voltmeter, and handheld programmable calculator



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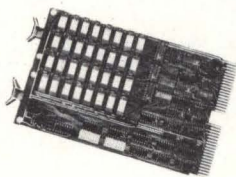
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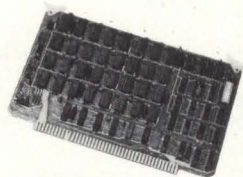
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# The Birth of a Notion.



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# CALENDAR

## CONFERENCES

**JUNE 20-22—32nd Annual Conv of the Armed Forces Communications and Electronics Assoc (AFCEA)**, Sheraton-Park Hotel, Washington, DC. INFORMATION: Judith H. Shreve, AFCEA Skyline Ctr, 5205 Leesburg Pike, Falls Church, VA 22041. Tel: (703) 820-5028

**JUNE 26-28—36th Annual Device Research Conf**, U of California, Santa Barbara, Calif. INFORMATION: James C. McGroddy, 1978 DRC Chm, IBM T. J. Watson Research Ctr, Yorktown Heights, NY 10598. Tel: (914) 945-1228

**AUG 1-4—4th Workshop on Computer Architecture for Non-Numeric Processing**, Minnowbrook Conf Ctr, New York, NY. INFORMATION: Prof P. Bruce Berra, 441 Link Hall, Syracuse U, Syracuse, NY 13210. Tel: (315) 423-2826

**AUG 6-9—3rd Jerusalem Conf on Information Technology (JCIT)**, Jerusalem, Israel. INFORMATION: Anthony Ralston, SUNY at Buffalo, 4226 Ridge Lea Rd, Amherst, NY 14226

**AUG 20-25—Sym for Innovation in Measurement Science**, Hobart/Smith College, Geneva, NY. INFORMATION: Peter Vestal, Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

**AUG 21-25—4th Internat'l Congress of Cybernetics and Systems**, Amsterdam, The Netherlands. INFORMATION: Dr J. Rose, c/o College of Technology, Feilden St, Blackburn, Lancashire BB2 1LH, England

**AUG 21-31—17th USITA Data Communications Conf**, Scheman Continuing Education Bldg, Iowa State Ctr, Iowa State U, Ames, Iowa. INFORMATION: Paul Bond, Conf Director, Engineering Ext, 110 Marston Hall, Iowa State U, Ames, IA 50011

**AUG 22-25—Internat'l Conf on Parallel Processing**, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: Dr Charles S. Elliott, College of Engineering, Wayne State U, Detroit, MI 48202. Tel: (313) 577-3812

**AUG 28-SEPT 1—8th Australian Computer Conf**, Canberra, Australia. INFORMATION: ACS-8 Programme Committee, PO Box 448, Canberra, ACT 2601, Australia

**SEPT 4-6—5th Nat'l Systems Conf**, Punjab Agricultural U, Ludhiana, India. INFORMATION: Dr R. K. Varshney, Organizing Secretary, NSC 78, Dept of Electrical Engineering, PAU Ludhiana 141004, India

**SEPT 4-8—Searcc 78, South East Asia Regional Computer Conf**, Philippine Internat'l Conv Ctr, Manila, Philippines. INFORMATION:

Searcc 78, Philippine Computer Society, MCC PO Box 950, Makati, Metro-Manila, Philippines

**SEPT 5-8—COMPCON Fall '78**, Capital Hilton, Washington, DC. INFORMATION: COMPCON Fall, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

**SEPT 6-8—FOC '78, Fiber Optic and Communications Expo**, Hyatt Regency-O'Hare, Chicago, Ill. INFORMATION: Information Gatekeepers, Inc, 167 Corey Rd, Suite 212, Brookline, MA 02146. Tel: (617) 739-2022

**SEPT 6-8—Internat'l Optical Computing Conf**, Imperial College, London, England. INFORMATION: S. Horvitz, Box 274, Waterford, CT 06385. Tel: (203) 442-0771

**SEPT 12-14—Western Electronic Show and Convention (WESCON)**, Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: W. C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

**SEPT 19-22—Conf on Microprocessors in Automation and Communications**, U of Kent at Canterbury, England. INFORMATION: Conf Secretariat, Institution of Electronic and Radio Engineers, 99 Gower St, London WC1E 6AZ, England

**SEPT 21-23—Interactive Techniques in Computer-Aided Design**, Palazzo dei Congressi, Bologna, Italy. INFORMATION: Dr Betram Herzog, Computer Ctr, U of Colorado, Boulder, CO 80303. Tel: (303) 492-6501

**SEPT 26-28—The Automatic Test Equipment Conf and Expo (ATEX)**, Hynes Auditorium, Boston, Mass. INFORMATION: Bill Hickey, Golden Gate Enterprises, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94086

**SEPT 26-29—4th Internat'l Conf on Computer Communication (ICCC-78)**, Kyoto Internat'l Conf Hall, Kyoto, Japan. INFORMATION: ICC-78 Executive Committee, c/o Internat'l Affairs Bureau NTT, 1-6, Uchisaiwai-cho, 1-chome, Chiyoda-Ku, Tokyo 100, Japan

**OCT 6-11—Japan Electronics Show '78**, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: Japan Electronics Show Assoc, No 24 Mori Bldg, 11 F, 3-23-5, Nishi-Shinbashi, Minato-ku, Tokyo 105, Japan

**OCT 10-12—2nd Conf of the European Cooperation in Informatics (ECI)**, Verice, Italy. INFORMATION: Prof Dr Peter Lockemann, Institut für Informatik II, Universität Karlsruhe, Postfach 6380, D-7500 Karlsruhe 1, Germany

**OCT 17-19—EUROMICRO 78, 4th Sym on Microprocessing and Microprogramming**, Munich, Germany. INFORMATION: Dr Helmut Berndt, Siemens AG, Div WS PZ1, Postfach 70 00 78, D-8000 Munchen 70, West Germany

**NOV 20-22—15th BIAS Internat'l Conf: Automation and Microcomputer**, Milan Fair Ground, Milan, Italy. INFORMATION: Federazione delle Associazioni Scientifiche e Tecniche, Piazzale Roldolfo Morandi, 2, 20121 Milan, Italy

## SEMINARS

**JULY 10-12—Queueing Systems; JULY 17-19—Satellite Data Communications; and JULY 24-26—Experts on Networks**; Arlington, Va; Arlington, Va; and Atlanta, Ga. INFORMATION: Technology Transfer Inc, PO Box 49765, Los Angeles, CA 90049. Tel: (213) 476-1331

**AUG 8—Industrial Robot Research Seminar**, U of Rhode Island, Kingston, RI. INFORMATION: Ada Willis, Dept of Electrical Engineering, Kelley Hall, URI, Kingston, RI 02881. Tel: (401) 792-2514

## SHORT COURSES

**JULY 10-14—Charge Transfer Devices: 1978 Theory and Applications; and July 18-20—Microcomputers: Principles and Applications**, American U, Washington, DC. INFORMATION: Jennifer Murphy, Director, Office of Summer Sessions and Special Sessions, American U, Mass and Nebraska Aves, NW, Washington, DC 20016. Tel: (202) 686-2697

**JULY 10-21—Programming Methodology; JULY 17-22—Operating Systems; and JULY 31-AUG 11—Compiler Construction; and Computer Graphics**, U of Calif, Santa Cruz, Calif. INFORMATION: Joleen Kelsey, U of Calif Ext, Carriage House, Santa Cruz, CA 95064. Tel: (408) 429-2614

**JULY 13-14—Program Testing Tutorials**, San Francisco, Calif. INFORMATION: Software Research Associates, PO Box 2432, San Francisco, CA 94126. Tel: (415) 921-1155

**JULY 19-21—Microprocessors**, George Washington U, Washington, DC. INFORMATION: Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

**AUG 28-30—Interfacing Instrumentation and Control Hardware to Minicomputers; AUG 29-SEPT 1—Understanding Microprocessors and Their Applications**, U of Wisconsin, Madison, Wis. INFORMATION: James E. Nicholls, Dept of Engineering, U of Wisconsin-Ext, 432 N Lake St, Madison, WI 53706. Tel: (608) 262-2061



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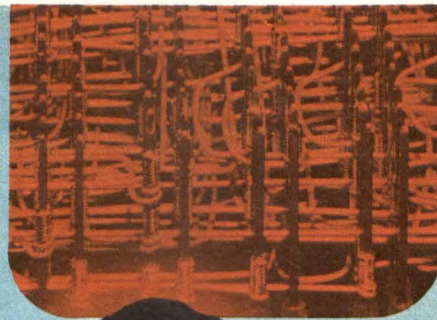
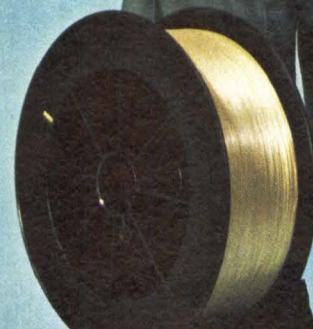
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4096 x 1 BIT HMOS STATIC RAMs

DEVICE	Max. Access Time (ns)	Max. Active Current (mA)	Max. Standby Current (mA)
2141-2	120	70	20
2141-3	150	70	20
2141-4	200	55	12
2141-5	250	55	12
2141L-3	150	40	5
2141L-4	200	40	5
2141L-5	250	40	5
2147	70	160	20
2147-3	55	180	30
2147L	70	140	10





# LETTERS TO THE EDITOR

To the Editor:

Iteration	Class	w	x	d(x)	Modify w
1	1	(0,0,0)	(3,1,1)	0	yes
2	1	(3,1,1)	(1,2,1)	6	no
3	2	(3,1,1)	(1,-2,-1)	0	yes
4	2	(4,-1,0)	(2,-1,-1)	9	no
5	1	(4,-1,0)	(3,1,1)	11	no
6	1	(4,-1,0)	(1,2,1)	2	no
7	2	(4,-1,0)	(1,-2,-1)	6	no

Since publication of the article, "Pattern Recognition: Basic Concepts and Implementations" (see *Computer Design*, Dec 1977, pp 57-68), I have discovered two notable errors. First, the derivation in the first column on p 61 involves several  $w_0$  symbols. Six are unit vectors that do not have the  $\wedge$  mark over them. This could be confusing to a reader unaware of such omissions. [These lines are reprinted in correct form below.]

$$\text{Line 11: } \hat{w}_0 = \frac{w_0}{\|w_0\|}$$

$$\text{Line 21: } D(\text{line}) = |\hat{w}_0 \cdot x| = \left| \frac{-w_{n+1}}{\|w_0\|} \right| = \left| \frac{w_{n+1}}{\|w_0\|} \right|$$

$$\text{Line 25: } \|Y - N\| = \hat{w}_0 \cdot y - \hat{w}_0 \cdot x$$

$$\text{Line 28: } \hat{w}_0 \cdot x = \frac{w_0 \cdot x}{\|w_0\|} = \frac{w \cdot x}{\|w_0\|} - \frac{w_{n+1}}{\|w_0\|}$$

$$\text{Line 30: } \hat{w}_0 \cdot x = \frac{w_{n+1}}{\|w_0\|}$$

Second, the perceptron example (Fig 10) on p 67 necessitates change. The 1s under the x values in iterations 3, 4, 7, 8, 11, and 12 should be negative. This leads to a much longer tabulation in Fig 10 before convergence, making the corrected table pedagogically unwieldy. A simpler example is given in the table above, using the same  $x_1$  and  $x_2$  but with  $-x_3 = (1, -2, -1)$  and  $-x_4 = (2, -1, -1)$ . The final weight vector (4, -1, 0) is perpendicular to a line which separates the two classes. The value of  $d(x)$  is a measure of how close a given  $x$  is to  $d(x) = 0$ . Note that  $x_1$  and  $-x_4$  have the largest values of  $d(x)$  and are farthest from  $d(x) = 0$ , while  $x_2$  is closest and has the smallest value of 2.

I hope these corrections will make the article easier to assimilate.

Dennis Feucht  
Tektronix, Inc  
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To the Editor:

First thank you for the pleasure your magazine gave my husband. All his life he worked as an engineer and designer and tech writer and was a great reader.

Unfortunately my husband dropped dead of a sudden and unexpected heart attack.

My husband saved all magazines and since his passing my son has given all my husband's books and magazines to three different schools, so all







A black and white photograph of a 5.25-inch floppy disk drive. The drive's door is open, revealing a circular disk tray. A hand, wearing a light-colored long-sleeved shirt, is holding a 5MB floppy disk by its central hub. The disk is positioned over the tray. The drive's interior has a grid-like structure. The overall scene is set against a dark background.

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## COMMUNICATIONS TRAFFIC ANALYSIS

---

**John E. Buckley**

Telecommunications Management Corporation  
Cornwells Heights, Pennsylvania

---

**C**ommon voice and data communications networks are a continuing trend in today's information systems. Therefore, it is increasingly important to statistically analyze and project the operational behavior of a known traffic pattern on a fixed communications network. Before an organization decides to implement its voice and data traffic on a common communications network for maximum cost savings, the effect of such savings must be accurately profiled. Many statistical algorithms address this requirement; however, in actual practice, the basic technique described below has been found useful in accurately projecting such communications traffic behavior.

Assume that there are both randomized voice and data communications calling patterns; the combined pattern is then segmented into a representative period, such as the average usage or the peak usage hour. Assume also that both voice and data events have equal access to the shared network. Since most calling networks are computer-controlled, they provide automatic network selection, as well as queuing if the facilities are busy at the time of selection. The major concerns of network design and management are the definition of the proper type and quantity of network facilities and relative economic advantages and disadvantages of various queue lengths.

The technique is applicable to any system where a number of random-duration, randomly generated events, together comprising a definable "demand," are to be transmitted over a limited number of available paths or routes. The paramount unknown to be determined is the probability of "blocking"—that is, an event finds all available paths or routes in use. Where such blockage occurs, the automatic building and distribution of a queue must also be determined; and, with respect to the queue, the amount of recovered traffic must be statistically definable. The difference between the queued volume and the recovered volume is the queued overflow. In operational terms, it must be decided: is this overflow volume cancelled, is it reinitiated against the communications network, or is it transmitted over the more costly toll network? These problem definitions are readily applicable to a

telephone switching system where the "events" are telephone calls, and the "paths" are transmission circuits.

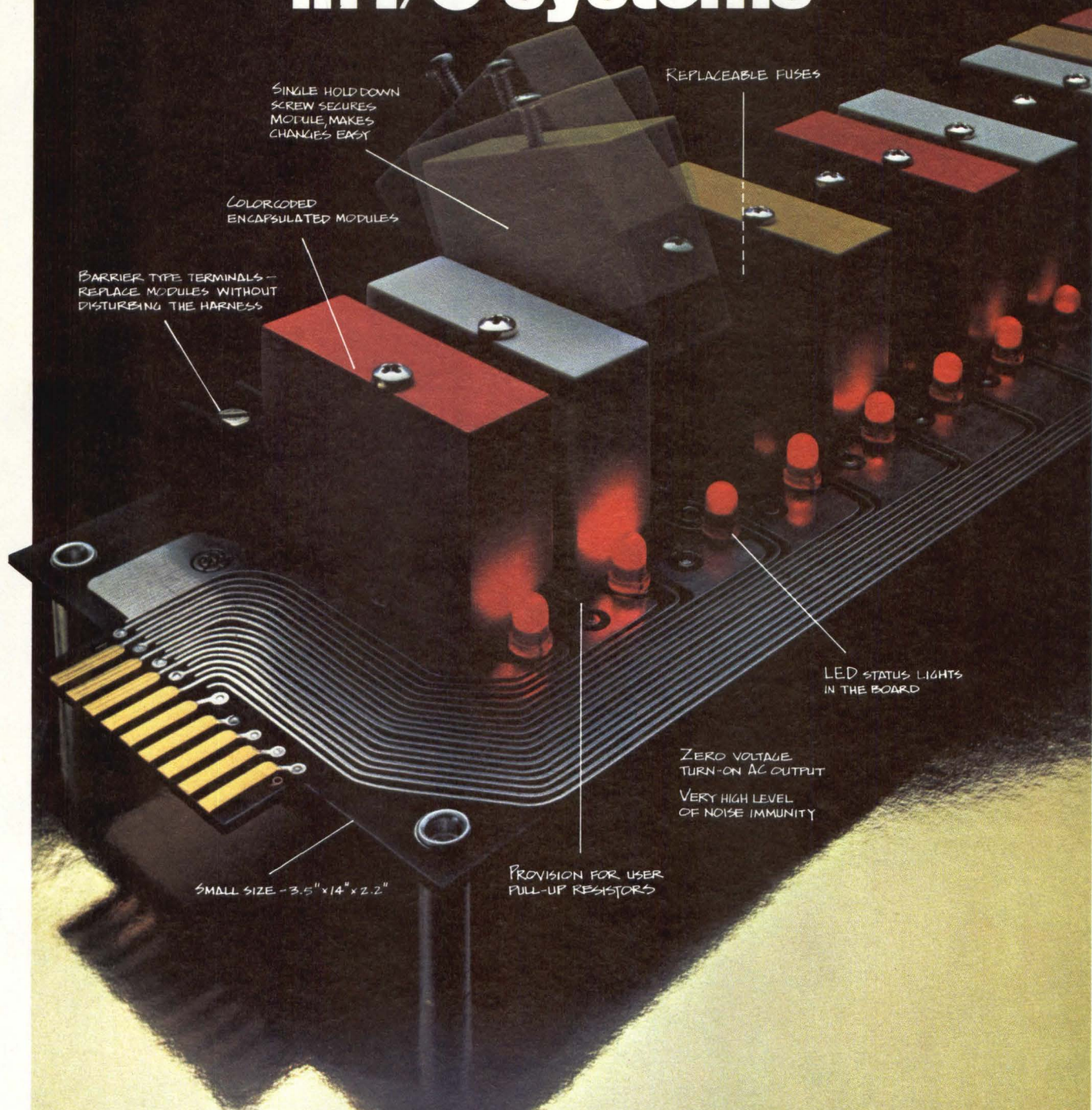
Communications engineering principles, applied to a switched telephone system, have resulted in a calculated grade of system service, based on an average or a peak period of operation. Two demand characteristics must, then, be defined: the duration spectrum of the event or events that would be expected to occur during the selected time period; and the relation of the selected period of time to total demand. In communications network system design, the first of these characteristics is usually the total amount of required time represented by the "demand" during the selected period of elapsed time. The second characteristic is, typically, the representative hour of operation, and can therefore be regarded as the application of a worst-case design philosophy.

Logically, if the system can accommodate the peak period with a satisfactory grade of service, it follows that all other periods of operation will enjoy an even better grade of service. It should be remembered, however, that this relation takes into account neither system economics nor other realities; and the term "satisfactory" is not always subject to a purely objective definition. Such a design goal should be to achieve an acceptable—vastly different from the best—grade of service. Demand in a selected hour is the sum of all call durations, or total time required to sequentially establish and complete all selected-hour calls, expressed in "hundred call seconds" (ccs). There are 3600 seconds, or 36 ccs, in one hour.

Private line and/or WATS network engineering is based on the number of calls to be handled, average call duration, and available circuits or trunks. These criteria are directly dependent on the average call duration and on the total demand for available circuits. In the event of an all-circuits-busy condition, the call must be queued until a circuit is free. Delay on queued calls is primarily determined by the average call length and by the number of possible paths that could be available to process the waiting call. Once the selected-hour demand has been established, it is assumed that this demand will be pro-



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## The Execution

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## The Product Today

Now, one year later, the 7710 is being produced in a new facility that has been specifically designed for high volume production.

The drive itself meets or exceeds all the original design requirements.

The overall dimensions of 5" x 8½" x 19", allow for direct physical replacement of a floppy disc drive.

Memory capacity is 11.12 megabytes, with a 24 megabyte version to be available in early 1979. Average access time is 50 milliseconds.



## Specifications Model 7710

### PHYSICAL CONFIGURATION

Height: 5.25 in.—13.34 cm  
Width w/o slides: 8.55 in.—21.75 cm  
Width with slides: 8.96 in.—22.75 cm  
Depth w/o Bezel: 19.0 in.—48.26 cm  
Weight: 22 lbs.— 9.98 Kg

### RECORDING CHARACTERISTICS AND DATA

Recording Capacity: 11 megabytes  
Data Tracks per Surface: 350  
Track Density: 300 T.P.I.  
Recording Density: 5868 B.P.I.  
Disc Speed: 3600 R.P.M.  
Transfer Rate: 648 K Bytes/sec.

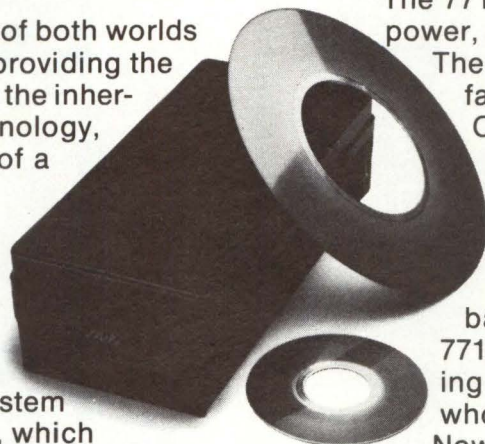
Average Access Time: 50 ms  
Servo System: Full Track Following  
Latency Time: 8.3 ms  
Track to Track: 10 ms

### POWER

The drive requires a D.C. Power Supply:  
+24 volts, ±12 volts, ±5 volts  
Power Consumption: 100 watts

### ENVIRONMENT

The drive will operate normally within the following Temperatures:  
10°C–50°C (50°F–120°F)  
Relative Humidity: 10% to 80%  
(Non-condensing)



The drive requires no scheduled maintenance, and the M.T.B.F. is 10,000 hours.

The 7710 uses only 100 watts of D.C. power, and no A.C. power is required.

The inexpensive cost is an extra facet of this diamond: \$1,500 in O.E.M. quantities, and a mere \$2,400 when the built-in controller is included.

## Applications

For most minicomputer based business systems, the 7710 has the capability of expanding system capacity to handle a whole new class of applications. Now you can eliminate the problems inherent in multiple floppy disc installations by using the 7710 to enhance the cost/performance of your business system.

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**TABLE 1**  
**Optimum Network Loading Distribution**

Total minutes	=	20,000
Total calls	=	4000
Average call length	=	5.0 min
Total CCS	=	71.4

Network	Minutes Utilized
Trunk 1	5700
Trunk 2	5020
Trunk 3	4130
Trunk 4	3061
Trunk 5	1765
Trunk 6	324
Total	20,000

based on the probability of finding all trunks busy, and this probability is the basis of the circuit capacity tables, developed from the Poisson theory. These tables identify grades of service as P01, P02, P03, . . . , which indicate the probability of a call finding a circuit busy during the selected hour. For example, P01 signifies probability of 1 in 100 calls finding a busy condition; P02, 2 in 100; etc. With P10 grade of service, 90 calls in 100 will find idle trunks on the first attempt. A representative grade of service for the public telephone network is, typically, at 2:100 or P02, using Poisson distribution.

Specifically, Poisson probability is used where the number of provided trunks or facilities assures a minimal percentage of blocked calls. The selected-hour load to a group of circuits is the amount of traffic (demand) expressed in terms of ccs which will receive the optimum grade of service. The extent to which total available circuit time in the group is actually used during the selected hour is an indication of the group's efficiency and loading.

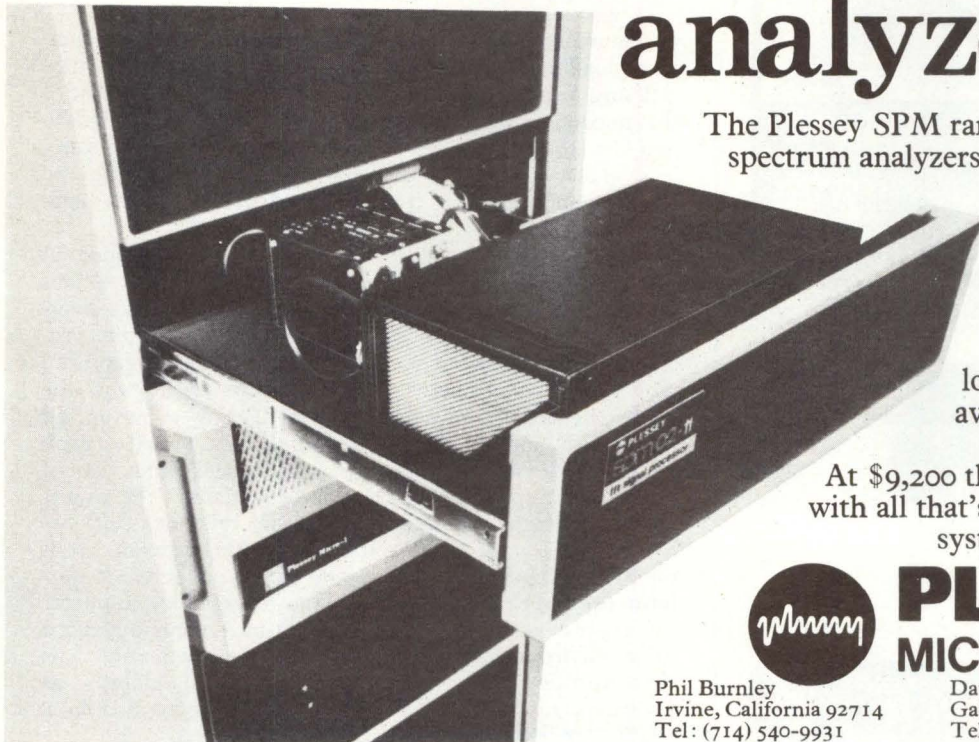
As shown in Table 1, potential fixed network loading using an optimum P02 grade of service indicates a requirement for six circuits or trunks. Total minutes to the Band 5 area are assumed to have occurred over a 21-day activity month comprised of 8-hour business days. This traffic loading represents a total of 71.4 ccs average hour calling activity. Using P02 Poisson distribution, the total of six circuits would not incur any local network blocking. The objective of a fixed network would be to install a minimum number circuits or trunks which would be shared by all of the specified calling activity.

If economic analysis indicates that it is desirable to install only three trunks, the traffic on trunks 4 through 6 in Table 1 would statistically find this network busy and would be assigned to this network's queue. In this ex-

cessed without any blockage—which could only be introduced by the public telephone network. In such an event, the call would be automatically reintroduced.

Communication common carriers define network service in the context of these terms. Grade of service is

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ample, a total of 5150 traffic minutes would experience a busy network and would comprise the accumulated queued minutes.

The next analysis objective is to determine how many of these queued minutes would actually be recovered by the network, and how many minutes would be designated as queue overflow as defined above. In this phase of the analysis the average call length and the number of potential trunks or "paths" are critical. Since the selected network has three paths, a call waiting in the queue has three opportunities to gain access to the network. Assume that all three trunks are busy with average-length calls; also assume that the three additional calls are attempted. Finding the trunks busy, these additional calls will be relegated to the queue. The first of these will have three opportunities to seize an available trunk. The second of these additional calls, however, will have only two opportunities to be connected to an available trunk while the third queued call will only be given one. As shown in Table 2, the average queue time of these three queued calls is 183.3 s. The maximum queue time in this example is twice the average, or 366.6 s.

If a 5-min maximum queue length is to be established for operational or management reasons, a total of 81.8% of the queued traffic will actually be recovered by the 3-trunk network. In this example, this recovered queue traffic would equate to 4212.7 min while 937.3 min of queued traffic would be determined to be queue overflow traffic. This overflow could be cancelled, reintroduced to the network, or be completed using an alternate route such as the toll network. The recovered queued traffic will typically distribute over the three network trunks in proportion to the sequence and loading originally calculated for

TABLE 2

Queue Length Determination

Average call length	=	5.0 min	=	300 s
Total available trunks	=	3		
First call average queue	=	100 s		
Second call average queue	=	150 s		
Third call average queue	=	300 s		
		<b>Total</b>		<b>550 s</b>
Average queue time	=	183.3 s		
Maximum queue time	=	366.6 s		

TABLE 3

Projected Network Loading Distribution

Total minutes	=	20,000
Total calls	=	4000
Average call length	=	5.0 min
Total CCS	=	71.4
Queued minutes	=	5150
Recovered queued minutes		4312
Overflow queued minutes	=	937
		<b>Minutes Utilized</b>
<u>Network</u>		<u>Utilized</u>
Trunk 1		7317
Trunk 2		6444
Trunk 3		5302
Overflow		937
		<b>Total</b>
		20,000

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optimum network loading. Table 3 shows projected network loading for these characteristics.

Using this analysis one can rapidly determine that if the maximum queue length threshold were extended to 366.6 s, the queue overflow would be reduced to zero. The value of different maximum queue lengths can be easily quantified using this suggested traffic analysis technique.

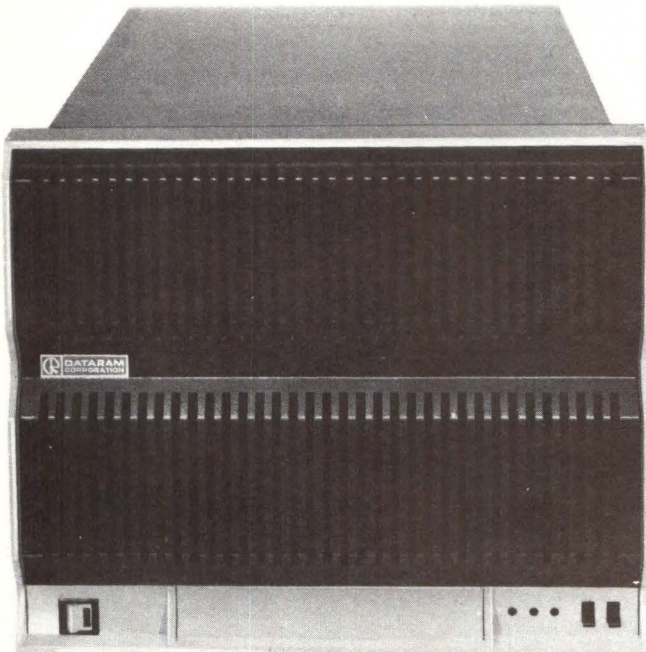
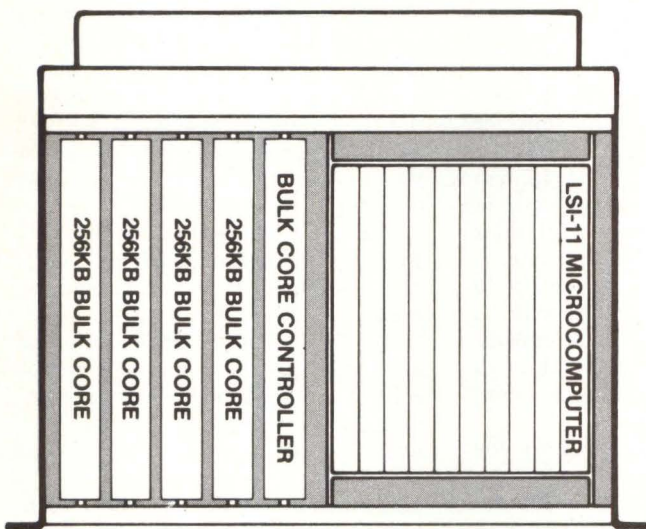
As with any statistical analysis, there are inherent assumptions which can result in unacceptable deviations from reality. In this example, the inconsistent use of average traffic distributions and average call durations provides an average network profile. To profile the expected range of possible network performance accurately, the same calculations must be performed using a maximized call length and maximized traffic distribution (ie, peak day, peak hour). Conversely, a minimized projection of the same parameters must then be calculated. The results are an envelope of expected network tolerance and behavior. By use of a reiterative computer program, it is relatively simple to develop the expected network performance envelope through a range of variable parameter values. It is important to realize that in a communications traffic environment, diversification of the communications characteristics is the norm. Such statistical analysis, as discussed, must always be interpreted and applied in a relative context.



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## Preprogrammed Analyzer Eases Troubleshooting of Data Networks



Hewlett-Packard serial data analyzer can record up to 2048 characters in any combination of transmit and receive. Data are trapped and displayed in real time, with transmit data displayed in video on a 10 x 13-cm CRT. Full-duplex data are shown as interleaved characters in proper timing relationships. Separate 1024-char buffer generates user-entered messages for the simulate modes

Active or passive troubleshooting of data communications networks is enabled by model 1640A serial data analyzer from Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 95304. In the passive mode, it can be connected to an RS-232-C (V.24) interface, to monitor and record both the transmit and receive data. When used in active mode, the analyzer can simulate a computer, modem or terminal, and can interact with the network under test. The user is relieved of the need for programming the device because it is provided with a keyboard-controlled "menu" selection of all pre-programmed RUN mode parameters, such as triggering (trap) conditions

and format specifications. Initial settings can be recalled at any time for review and modification.

On both monitor and simulation modes, the analyzer can operate in full duplex, half duplex, or simplex on 2- or 4-wire links. Transmission is up to 19.2k bits/s synchronous, or to 9600 bits/s asynchronous, with a choice of 15 internal clock speeds. Data can be made up of five through eight information bits, plus a parity bit, in ASCII, HEX, or EBCDIC.

A "copy" mode feature allows the user to monitor protocol exchanges between CPU and terminal, and automatically transfer either transmit or receive data into the unit's transmit

buffer. It is not necessary to enter complex protocol sequences via the keyboard. Copy mode allows data to be edited prior to transmission; this feature reduces need for the user to be intimately familiar with network protocol, and minimizes possibility of human error during message composition.

The analyzer can be set to trigger on five modes: on any 8-char sequence, including "don't care" states and "not" chars; on any control-lead positive state; if and only if an error occurs; on a specified time interval between any two events up to 6 s apart; and on an external event.

A patch panel matrix at the top of the front panel connects the analyzer to the interface and enables simulation of various terminal or computer configurations. It also allows the user to configure his own variation of the RS-232-C interface. A Mylar overlay can be punched for each configuration.

An HP-IB (IEEE-488) option allows user programming and remote control of the 1640A through a programmable controller. Optional p/ROMS permit up to eight different menus or test patterns to be entered automatically via a rear-panel push-button.

Circle 450 on Inquiry Card

## Distributed Data Entry Key-to-Diskette System

Used either as a standalone system or as part of a computer communications network, Universal Distributed System 2000, (UDS 2000) from Sperry Univac, PO Box 500, Blue Bell, PA 19422, can handle distributed or decentralized data processing, be used as a remote data entry system, or as a remote communications device. The freestanding, user-programmable system uses a stored program micro-processor to accept keyboard or peripheral input and store the data on the flexible diskette. In the basic system configuration, a desk-type cabinet houses a master workstation with 32k bytes memory, display screen and keyboard, and single diskette drive. Three additional workstations, which can be located as far as 2000 ft (610 m) away from the master, can be added to expand the system. Each

workstation may have up to two diskette drives. Workstation main storage is expandable to 65k bytes in 8k byte increments.

The master workstation has a 96-char keyboard. Various national fonts are available, including a 128-char Katakana set. Three keyboard styles are available: keypunch, keypunch/adding machine, or typewriter. Display is 7 x 9 dot matrix on a 9" (23-cm) CRT; capacity is 512 char, in a format of eight 64-char lines.

System is user-programmable either by check-box programming using a simple coding sheet, or through a procedural language, or COBOL subset, for tailoring the system for specific needs.

Optional peripherals to complement the system include a freestanding mag tape unit, card reader, interpreting punch or verifying punch for i/o, character printer or line printer, and data communications controller.

System transmits and receives synchronous data in half-duplex mode over a single line. Speeds of 2000, 2400, 4800, and 9600 bits/s are available. Binary Synchronous Communications (BSC), Uniscope<sup>®</sup> 100 terminal line protocol, and Univac Data Link Control (UDLC), are communications protocol options.

Circle 451 on Inquiry Card

## Virtual Network Supports Multiple Protocols

Virtual Network<sup>™</sup> is a network architecture in which the location and function of any and all elements of the network are completely transparent to the user; which will support, at the same time, SNA/SDLC, X.25, and bisynchronous protocols; and which allows the user to geo-



# electro-optical solutions

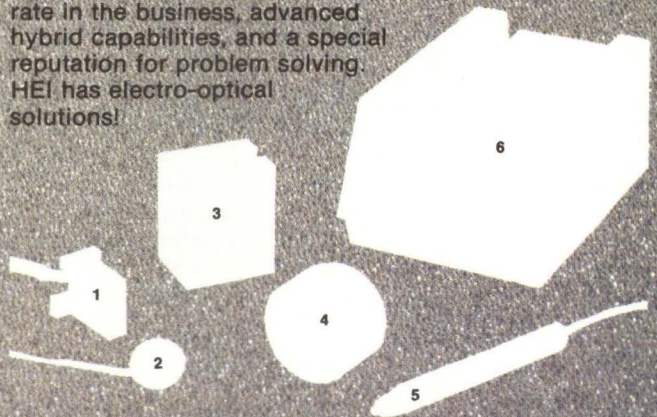


HEI offers all kinds of engineering solutions through innovative application of optical technology and hybrid electronics. The company that produced the original optical switch nearly ten years ago has developed an entire line of functional electronic blocks which may be used in a number of applications. A few examples are shown above.

1. Multi-Channel Reader - This economical 2 to 14 channel reader is widely used for line printer control. TTL outputs with up to ten fan-outs per channel.
2. Optical Thumbwheel Switch - Incremental output for up/down counting. Seventy-two square wave pulses per revolution, bounce-free. Compact and long-lived.
3. Industrial Optical Switch - Switches up to six amps AC, continuous load. Requires only 110 VAC, and replaces solid-state relay, power supply and interconnections. Complete circuit isolation. Ideal for motor control, limiting, etc.
4. Incremental Encoder - Low cost encoder includes disc and sensors. Provides square wave output, broad temperature capability.
5. Light Pen - TTL outputs for light pen "hit" and "switch". Adjustable light sensitivity to 2 footlamberts. Integral hybrid circuitry. Optional "no-touch" switch and coiled cord.

6. Card Reader - For hand-fed operations. Reads both punches and marks. Thirteen channel, square wave outputs with strobe. Can be custom configured. Lowest price on the market.

HEI also supplies various optical switches, card readers, arrays, shaft encoder sensors, subminiature photo transistors and custom hybrid services. Deal with the company that has the lowest reject rate in the business, advanced hybrid capabilities, and a special reputation for problem solving. HEI has electro-optical solutions!



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PRODUCT #2, CIRCLE 139

PRODUCT #3, CIRCLE 137

PRODUCT #4, CIRCLE 140

PRODUCT #5, CIRCLE 138

PRODUCT #6, CIRCLE 141

*The Optoelectronic Specialists*

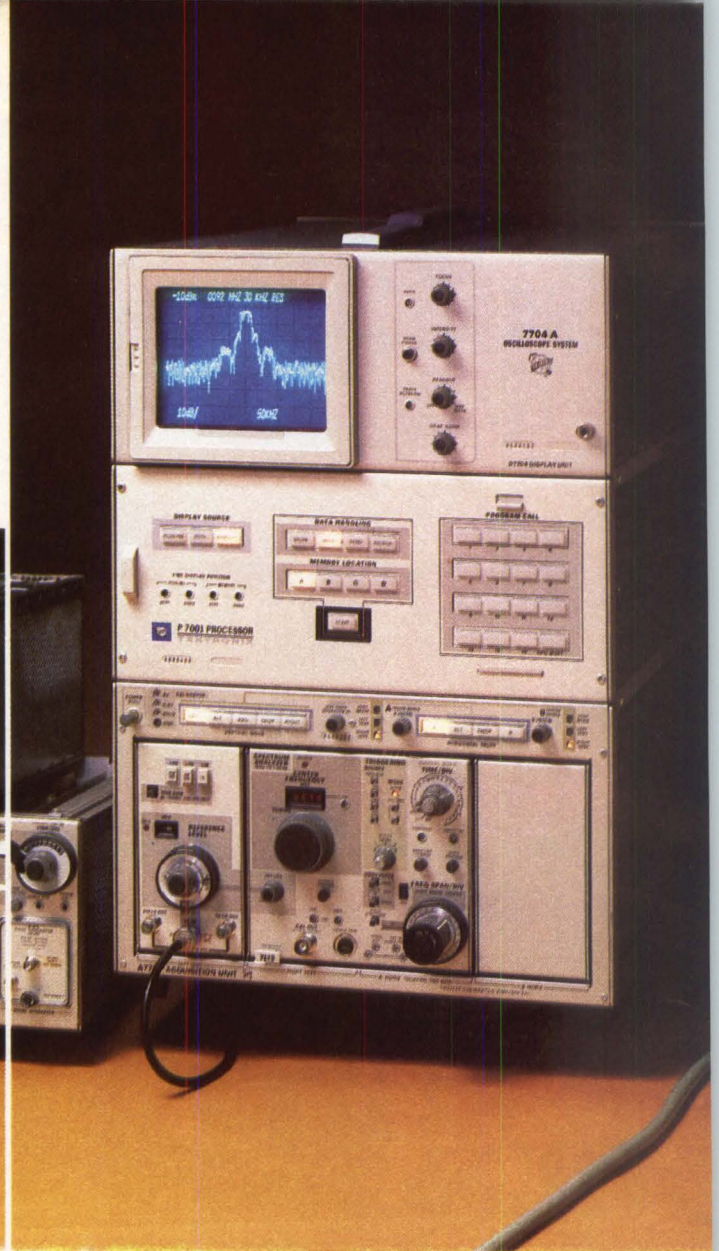
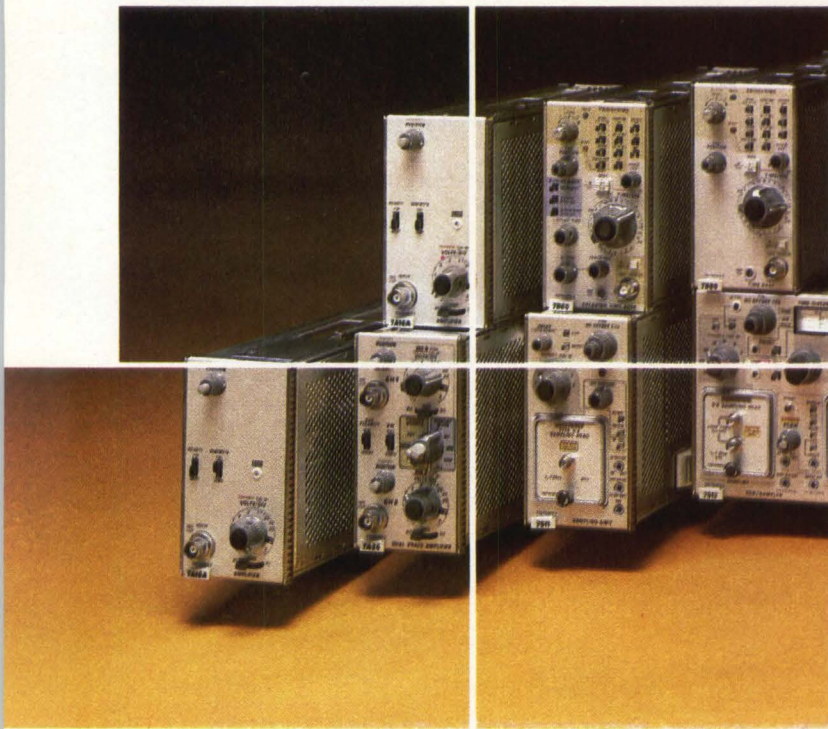
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# Put your waveform on the GPIB...

## ...with a Tektronix Digitizing Oscilloscope!



## The Digital Alternative

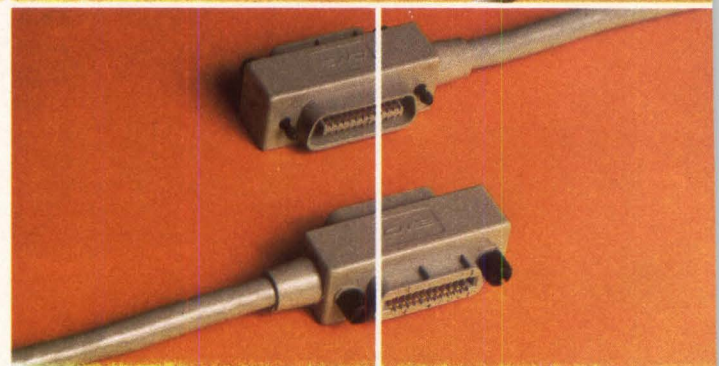
Our Digitizing Oscilloscope is a versatile data acquisition instrument based on the familiar TEKTRONIX 7704A Oscilloscope with a P7001 Processor added for interface to the digital world.

**Signal Acquisition Flexibility.** The Tektronix Digitizing Oscilloscope acquires data through a wide selection of standard 7000 Series Plug-Ins such as amplifiers, time bases, spectrum analyzers, sampling heads to 14 GHz, time domain reflectometers, curve tracers, digital counters or multimeters and more.

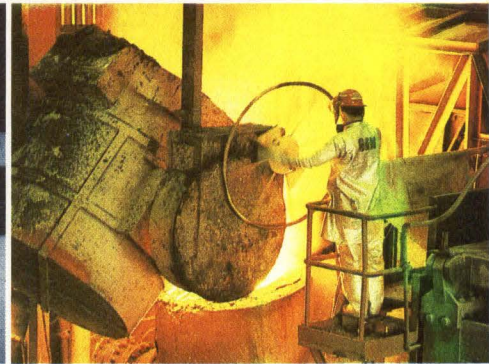
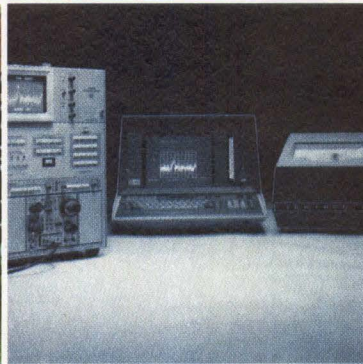
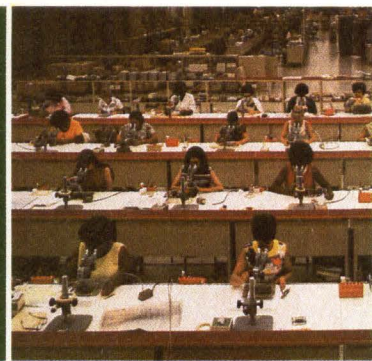
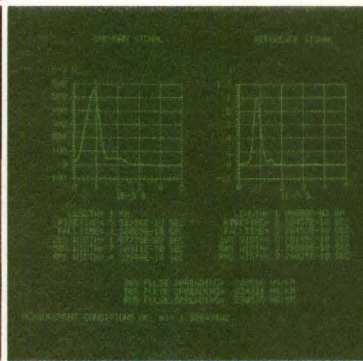
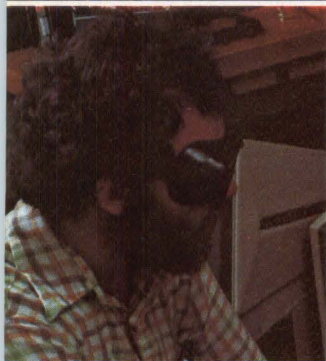
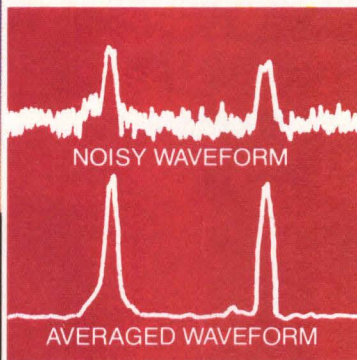
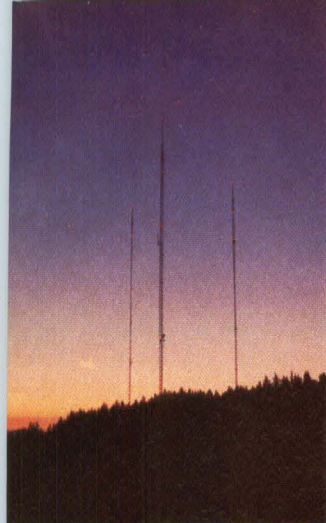
**A/D Conversion with Four Waveform Memories.** Almost any waveform that can be displayed on an oscilloscope, can be digitized to 10 bit by 512 horizontal point resolution and stored in any of four memories in the P7001 Processor. In addition to waveform data, all crt scale factor readouts are stored as well. Any of four stored waveforms may be recalled for display on the crt.

**New GPIB Interface.** A/D conversion memory selection and data transfer can now be controlled externally via the the GPIB bus. Digitized waveforms in any of the four memories may be transferred to a GPIB controller for analysis and automated processing. Complex waveform calculations are now possible with the convenience of oscilloscope acquisition.

**And a New Optional Hardware Signal Averager.** It permits rapid averaging of repetitive waveforms for dramatic signal to noise improvement.







**With that kind of flexibility, practical applications for the Digitizing Oscilloscope are numerous!**

In the field of...

**Research**—a Digitizing Oscilloscope can be used to analyze fiber optic circuits, or for their research and design. This unit is also an effective tool in chemistry and chemical research for electrochemical and perturbation kinetic studies.

**Development**—a Digitizing Oscilloscope can be used in microwave system development by extracting pertinent spectrum analysis data for study through a frequency range up to 60 GHz.

**Production ATE**—a Digitizing Oscilloscope can be used to automate ultra-sonic testing of nodular iron in foundries. This unit can even automate electronic system tests or diagnostic troubleshooting systems in the aero-space industry, and in many other types of production test environments.

**Component Testing**—a Digitizing Oscilloscope can be used to characterize coax insertion losses, or characterization of semiconductors. With appropriate programming this unit can also provide profiles and histograms of line transient absorbing materials and devices.

Interfaces available are GPIB (IEEE 488-1975), CAMAC, CP Bus (for operation with PDP 11 Series), TEK Calculator and others.

Optional controller based systems with powerful TEK SPS BASIC software and graphic terminal display offers unmatched signal processing sophistication!

Photos courtesy of:  
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STREET ADDRESS \_\_\_\_\_

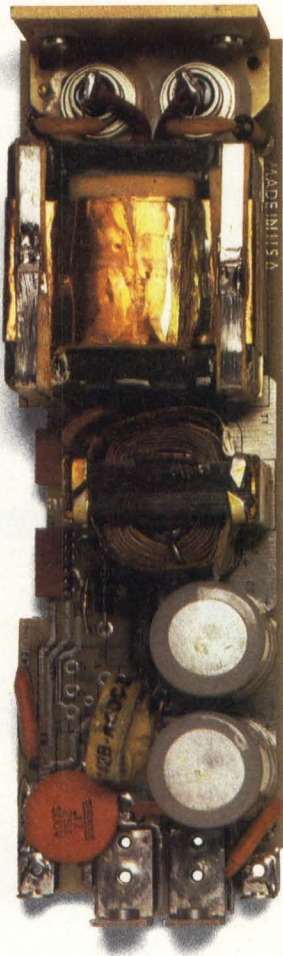
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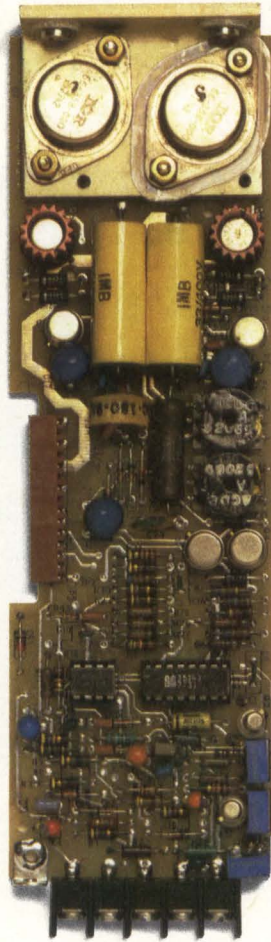
For technical data, circle 18 on Inquiry Card.  
For a demonstration, circle 19 on Inquiry Card.



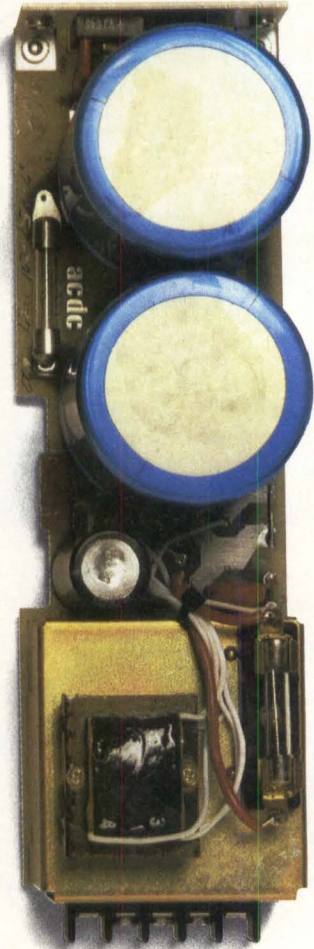
# THREE REASONS WHY OUR NEW SWITCHERS ARE MORE RELIABLE THAN THE POWER SUPPLIES YOU'RE USING NOW.



**OUTPUT BOARD**



**CONVERTER BOARD**



**INPUT BOARD**

The Sub-Modular Switcher family is a big breakthrough. Because the electronics are simple – just three boards. Input, converter, and output.

So we've significantly decreased parts and increased component reliability, thanks to LSI technology. We've used less, so to speak, to give you more.

Our internal modules don't use loose wiring or harnessing. The circuitry is integrated onto printed circuit boards, and joined by an interconnecting strip. The result is a power supply that's far less expensive – \$1/watt for certain models in OEM quantities.

The Sub-Modular Switcher family is available in 22 models. So you can choose from single or multiple output versions, with power ranges from 50 to 300 watts.

To make sure each Sub-Modular

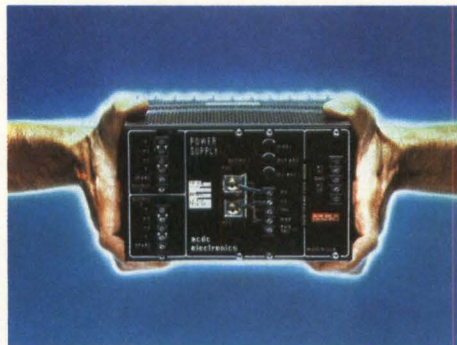
Switcher lives up to its specifications, we computer test all its operational parameters. And you get a complete EDP test report with every one you buy. The Sub-Modular Switcher's calculated MTBF exceeds its 5-year warranty. In fact, Life Test data indicate that actual MTBF should be considerably greater than the warranty period.

So, if you're tired of expensive, unreliable switchers, write for our free brochure.

It'll tell you all about our Sub-Modular Switchers.

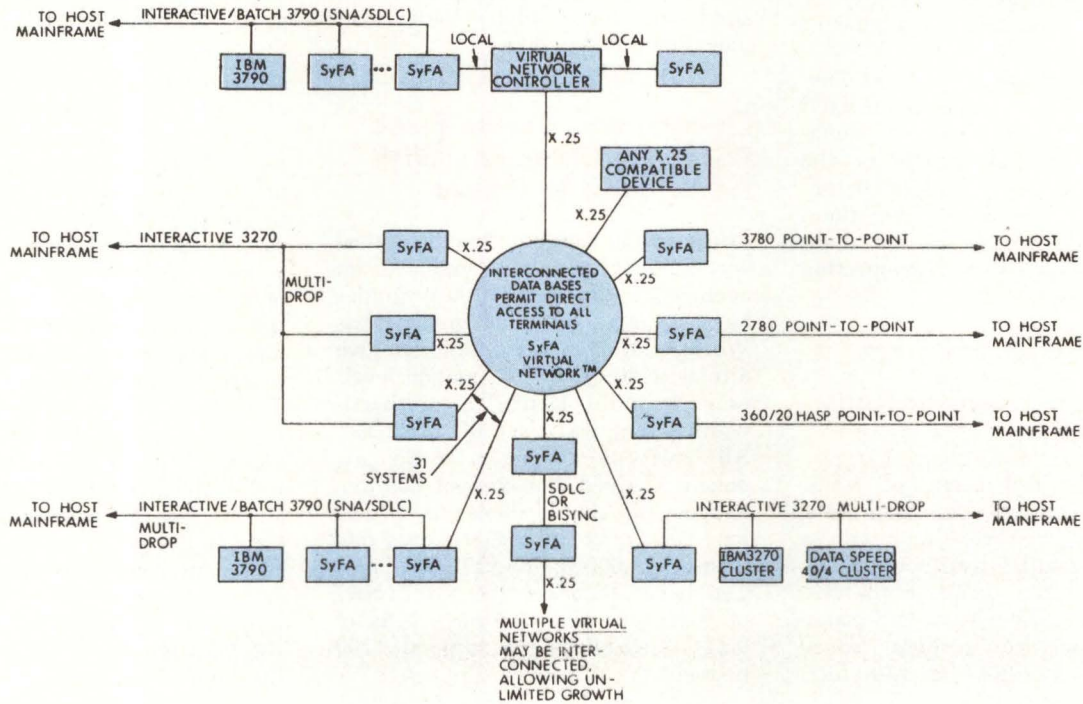
The ones built to keep you in power.

For further information, write to us on the East Coast at 211 W. Clay Ave., Roselle Park, New Jersey 07204, (201) 241-6077. On the West Coast, write to 401 Jones Road, Oceanside, California 92054, (714) 757-1880.



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KEEPING YOU IN POWER.





Various combinations possible with typical SyFA virtual network. User has available two concurrent high speed synchronous channels: one automatic channel uniting SyFA systems at file management level using X.25 protocol; plus additional synchronous communications channel which can be used in various forms to concurrently communicate, interactively or in batch mode, with mainframe system or other distributed installations. Communications protocols are supported via software emulators; complexion of network and protocols used can be changed dynamically by down-line loading software from central site

graphically distribute his data base, while retaining direct access to any data base from any terminal in the network. Virtual network interconnects multiple SyFA network processing systems (*Computer Design*, Mar 1978, p 20) and was developed by Computer Automation, Inc, 18651 Von Karman, Irvine, CA 92713. Since the system simultaneously supports all major communications protocols, the user is never forced to dedicate his system to one particular network architecture.

The architecture allows 31 network processors and 992 information station terminals to be interconnected to a common geographically distributed data base via local or remote high speed channels. Each processor supports up to eight disc drives; therefore a configuration using 300M-byte disc drives can provide a com-

mon online storage of 74.4 billion bytes, in addition to data files residing on mainframe systems.

Since any number of virtual networks may be linked together, there is no upper limit to the total number of systems or terminals which may be configured. Also, since the system supports all major communications protocols, such equipment as IBM 3270 terminal clusters, 3790 (SNA/SDLC) systems, Teletype Dataspeed 40/4 clusters, or X.25-compatible units can be interfaced to the network. Virtual network communications are handled automatically at the file management level, and are therefore transparent to the terminal user.

The entire network is controlled by the virtual network controller, (based on a version of the company's LSI 4/90 computer), which contains appropriate directory and space alloca-

tion information. Since the virtual network communications use X.25 protocol, the network can be optionally interfaced to a public packet switching network, or to other X.25-compatible units. First deliveries are scheduled for the third quarter of 1978.

Circle 452 on Inquiry Card

### High Speed Modems Are Approved by FCC For Direct Connection

Direct connection of the 9600-, 7200-, and 4800-bit/s LSI series high speed data modems to the Direct Distance Dial (DDD) network has been approved by the Federal Communications Commission. The registered model 22055 dual dial option



## COMMUNICATION CHANNEL

from Codex Corp, 15 Riverdale Ave, Newton, MA 02195 contains protective functions previously provided by the telephone company's external data access arrangement (DAA) or protective connecting arrangement (PCA).

In addition to the dedicated line, two dial-up lines can be connected directly into the modem via miniature data jacks. A switch in the modem alternately connects it between the dedicated and dial lines, facilitating the testing of the dedicated circuit without disconnecting the dialed lines.

## Racal, Vadic Negotiations Completed

The business and assets of Vadic Corp, 222 Caspian Dr, Sunnyvale, CA 94086, have been acquired by Racal Electronics Ltd, Bracknell, Berks, UK, for a figure in the \$10 million area. Vadic designs and manufactures low to medium speed modems, in the 300- to 2400-bit/s

range. This move, coupled with the purchase of ICC/Milgo last year, enables the Racal group to offer voice-band modems from the lowest speeds up to 9600 bits/s, augmented by baseband and wideband units at significantly higher data rates. The name of the new company is Racal-Vadic; it will operate independently of Miami-based Racal-Milgo. Vadic employs some 200 people.

## Optical Waveguide Price Decrease Coincides With Addition of 16 Fibers

Prices on the Corguide line of optical waveguides have been reduced an average of 25%, and 16 waveguides have been added by Corning Glass Works, Corning, NY 14830, to give a total of 20 types. Attenuation levels range from 3 to 10 dB/km, and bandwidths from 200 to 1000 MHz/km. All have core diameters of 63  $\mu\text{m}$ , outside cladded diameters of 125  $\mu\text{m}$ , and outside coated diameters of 138  $\mu\text{m}$ . Tensile strength screen tests rate them at 25,000 lb/in<sup>2</sup> (1757kg/cm<sup>2</sup>). Ten have numerical apertures (NA) of 0.24; the other 10 have NAs of 0.21. Waveguides are shipped 1100 m/reel.

## Data Communications System Software Enhancement

Users of the PIX-II Virtual Data Link may now assign priority access parameters to remote devices in mixed interactive and RJE configurations by use of a software enhancement, newly introduced by Paradyne Corp, 8550 Ulmerton Rd, Largo, FL 33541. The software allows remote console entry of simple control words which group interactive devices, such as IBM 3720-type display terminals, into a high-priority subset, and similarly to place batch-type devices, such as printers, card readers, and tape systems, into a lower priority subset group. All of the devices are supported on a single physical link for reduction of line costs. All data communications functions, including the prioritizing enhancement, are handled within the PIX-II system; there is no teleprocessing overhead on the mainframe. CRT terminals interact with the host on an attention interrupt basis, eliminating CPU device polling cycles. Device-access priorities may be established on the basis of the device mix, in terms of work patterns, or on a special-need basis.

Circle 453 on Inquiry Card

# Put a Pittman® D-C motor in your hands for consistent performance at a reasonable price



When you're designing a permanent-magnet motor into your product, it will pay you many times over to look at the Pittman line. We may not have all the answers but you'll get prompt and accurate design data plus realistic prices and deliveries. We've been helping others power their equipment for over 40 years. So, contact us regarding:

**SERVO MOTORS**—currently in three standard series, inputs from 6 to 30 V d c, load speeds up to 10,000 rpm, and stall torques from under one to more than 100 oz-in

**GEARMOTORS** — in two standard series for torque outputs to 300 oz-in, gearing for output shaft speeds from 2 to 650 rpm

Integral tachometers can also be supplied with selected motors as well as any model gearmotor.

And we welcome inquiries about modified units and special designs. Let us hear from you. The Pittman Corporation, a Subsidiary of Penn Engineering & Manufacturing Corp., Harleysville, PA 19438. Telephone 215: 256-6601



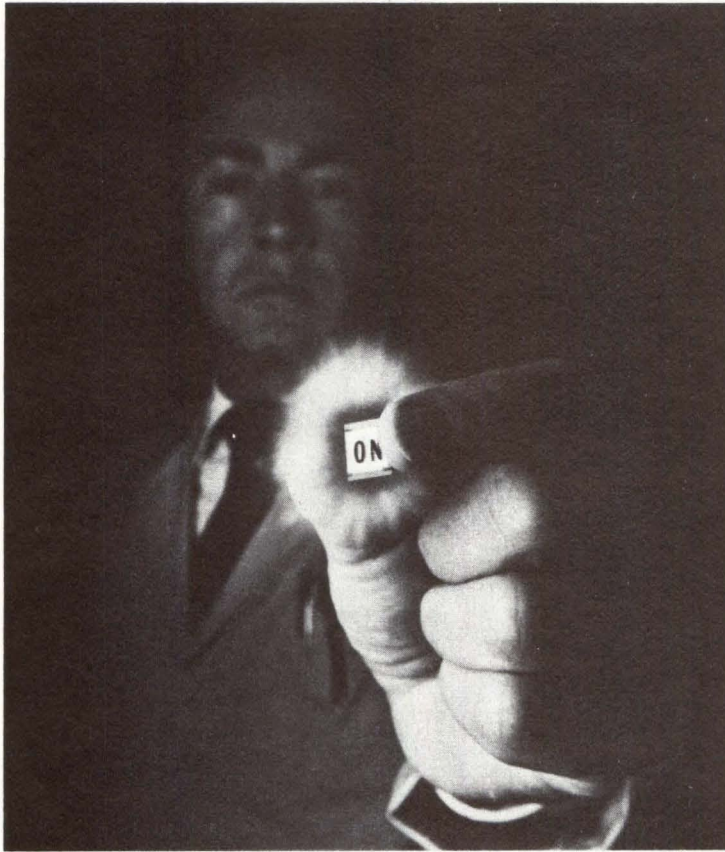
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## THE PITTMAN CORPORATION

6A/77



## Make intelligent keys brighter.



Introducing Fairchild's Datakey™ display. A state of the art LCD technology that makes intelligent keyboard keys smarter yet. It uses LCD's as keyboard keys to display messages by means of reflected-ambient light.

For example, in a computer control keyboard, Datakey can turn a blank function key into an intelligent message by illuminating the key only when it's a live option.

This simplifies operation, saves time and opens the door for less experienced (and less costly) operators.

Or in telephone keyboards, Datakey can replace incandescent bulbs and keys. And because it uses only nanoamps of power, it doesn't even require hookup to your main power source.

And that's just the beginning.

Our Datakey display is so innovative we're still discovering things it can do.

### Can we give you a light?

Maybe you have an application where our Datakey LCD technology will shine. It can be built in many sizes. And with a great complexity of characters. In fact, we can make displays using virtually any symbol or picture you come up with.

### We're lighting the way.

Of course, it's not surprising that Fairchild would develop this new LCD technology. We've been manufacturing LCD's for years. And we have a fully dedicated, high volume factory turning them out.

If you'd like to read our Datakey LCD Application Note and receive a sample key, just ask on your company letterhead. Write: Fairchild Camera and Instrument Corporation, 464 Ellis Street, Mountain View, CA 94042. Tel: (415) 493-3100. TWX: 910-373-1227.

**FAIRCHILD**

**Call us on it.  
(415) 493-3100**



## U.S.-U.K. Packet Switched Data Service

An international packet switched service to and from the United Kingdom is scheduled to start July 1, 1978, according to RCA Global Communications, Inc, 60 Broad St, New York, NY 10004. It will expand the company's overseas low speed data service offerings, and provide customers in both countries access to computer services and to a wide range of data base information. A variety of terminals operating at rates between 110 and 1200 bits/s, asynchronous, can be accommodated by the system. Customers in the U.S. will have access to the service through the conventional telephone network, by value-added carriers such as Telenet and Tymnet, and through specialized common carriers. They may also interconnect directly with the RCA international data exchange at the New York gateway.

The company says that this is the first international use of the X.25 switching protocol recommended by the CCITT, (Consultative Committee on International Telephone and Telegraph); the protocol allows users to operate terminals at 2500, 4800, and 9600 bits/s in the synchronous mode, directly into the international data network. Packet switching optimizes the switching and transmission capacity of the international network through the use of virtual circuit paths. In this way, there is no longer a requirement for terminals to be exactly matched to the characteristics of a computer host, as long as both the computer and terminal conform to the CCITT protocol.

RCA has received authority to proceed with the service to the United Kingdom, via the services of the British Post Office, and will shortly file a tariff to incorporate the new packetized charging methods.

## Uniform Tariffs Proposed for Public Data Network

Uniform nationwide pricing for use of its public data network is planned by Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036. Subject to approval by the

FCC, the new tariff structure will be implemented July 1, 1978. The company says it is the first US common carrier to offer data communication rates independent of distance and user location throughout the continental United States. Regardless of the customer's location, there will be a single rate, for each speed of service, for dedicated or leased line access to the network.

For dedicated access, the new rates range from \$300/mo for 50- to 300-bit/s transmission, to \$1100/mo for 9600-bits/s. Included in these charges are a port at a network switching center, the access line, and the required modems or digital interfaces.

Users dialing into the network for connection to a distant computer will be charged a flat rate of \$3.25/h in all cities directly served by the network. This rate applies to both 110- to 300-bit/s and 1200-bit/s access.

Also planned is In-WATS service for 1200-bit/s terminals to augment its In-WATS service for lower speed communications. Both services will be priced at \$15/h.

The company has additionally filed rates for PPX (Private Packet Exchange) service, aimed at customers who have a high concentration of usage in a particular city. PPX allows purchase of a group of ports at any network location at rates "offering an attractive alternative to a private concentrator or public dial-in service" according to Mr Ralph Johnson, vice-president, marketing. PPX features capability of automatically switching overflow calls to public dial ports.

## Software Packages Aid Network Design

Network designers having access to the Tymnet network can now avail themselves of a set of network design tools that, up to the present, were available only to larger users for implementation on in-house computers. Small- to medium-size users of leased line networks, with point-to-point or multipoint configurations may use this modular software system to determine the most cost-effective network architecture, according to the DMW Group, Inc, 2975 Hickory Lane, Ann Arbor, MI 48104.

The design packages include the Network Design and Management System, (NDMS) and Response 1 and 2. NDMS calculates optimum network layouts and produces detailed reports on such variables as line configuration, network partitioning, traffic generation, and multi-stage network design based upon throughput as well as upon response time.

Response 1 and 2 modules of the system are interactive programs that calculate maximum traffic volume a single multipoint line can handle, and the response time for a typical terminal on a specified line, respectively. Both modules also compute message length, polling wait time, and other important characteristics.

Users accessing these programs via Tymnet will be charged a monthly software subscription fee and Tymnet processing charges. Subscription agreements are on the basis of 3-mo, 6-mo, or 1-yr periods.

Circle 454 on Inquiry Card

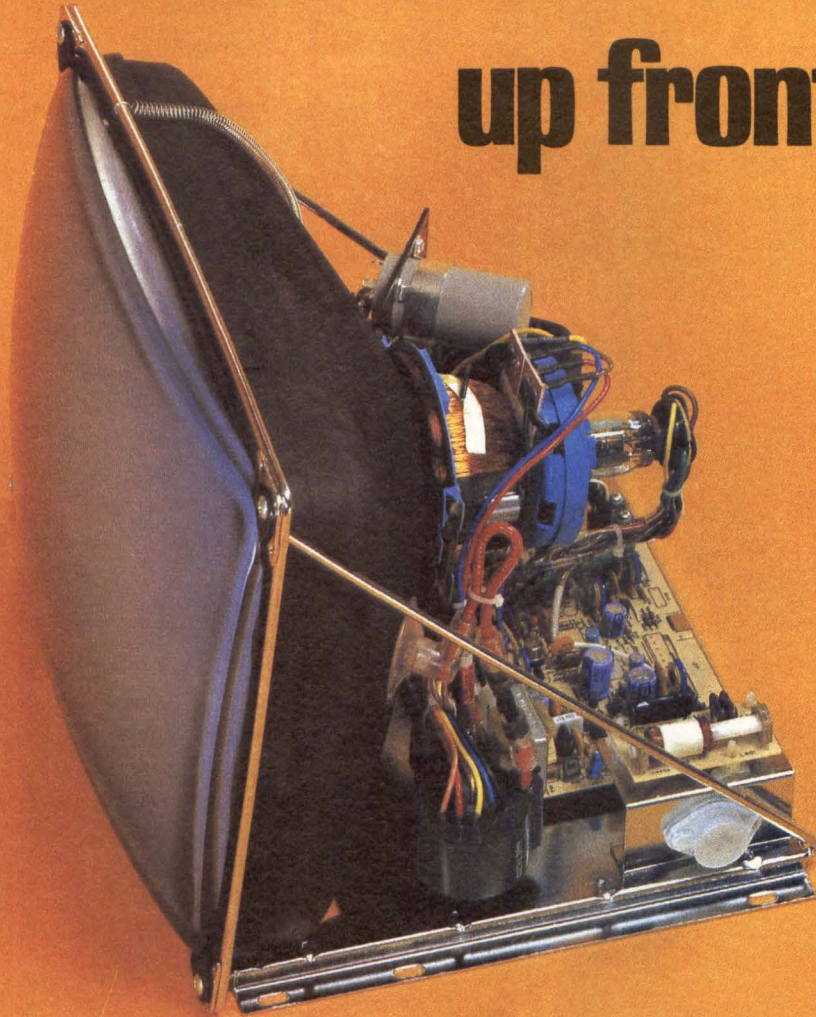
## Contracts Awarded For Dual Development of TDMA Burst Modems

Two development contracts provide for delivery of five prototype time-division multiple access burst modems and associated equipment from both the Satellite Communications Div of Harris Corp, Melbourne, Fla, and Fujitsu, Ltd, Tokyo, Japan with firm prices for optional quantities for operational use. Satellite Business Systems, 8003 Westpark Dr, PO Box 908, McLean, VA 22101 will conduct field tests with three from each manufacturer; the remaining units will continue life testing at the contractors' plants.

Providing signal processing and modulation/demodulation of burst-mode digital bit streams, the modems will be located at customer-premises earth stations, along with the radio frequency terminal and satellite communications controller. The company plans to launch its first two satellites in the second half of 1980 and begin serving large communications users through its Operational System in early 1981. □



# Don't be afraid to pay just a little more... up front!



## You'll find that life cycle costs tell the real story

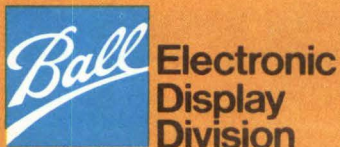
The quoted price for a CRT display is just the beginning. Cut corners here, and you pay for it later. For example:

**Alignment** — Will that low-cost monitor be completely adjusted and ready to go when you receive it? In-house adjustment hassles can wipe out that lower price in a hurry.

**Specifications** — Do those bargain displays meet performance minimums now? Will they in six months? *The display is your face to the world.* It should look good. It should be built right.

**Maintenance** — Low MTBF figures will jeopardize product performance and make you look bad. A small investment in quality parts and design at the start will cut future maintenance costs.

Remember, the best CRT display purchase is one that is a bargain year after year, every time your customer turns it on. Don't find out about life cycle costs the hard way. Your Ball representative will be happy to explain the benefits of paying just a little more initially for CRT displays. Ask him.



Ball Electronic Display Division  
P.O. Box 43376, St. Paul, Mn. 55164 (612) 786-8900. TWX: 910-563-3552

**General Sales Offices:**

Addison, Illinois (312) 279-7400      Santa Clara, California (408) 244-1474  
Ocean, New Jersey (201) 922-2800      Upland, California (714) 985-7110

CIRCLE 23 ON INQUIRY CARD



**There may be a  $\mu$ P board  
out there we can't test.**



**But we haven't found it yet.**



Chances are we won't. Dozens of different  $\mu$ P boards have run through our new 3040A Logic-tester™ in the first six months, with 100% success.

You never know what our rapidly changing technology will produce tomorrow though, and you need assurance your tester can handle it. The 3040A delivers that confidence, and more.

Like testing at full data and clock rates. Four bi-directional buses handled at one time. And four processors test your board's  $\mu$ P instructions, RAMs, ROMs, PIAs . . . all at multi-MHz rates!

All this and programs finished in *days*, not months.

To us, the most important consideration is that boards passing our tester will work in your product . . . every single IC and component. *That's* confidence, and it keeps both of us in business.

If confidence is important to you, look into the Fluke logic testers priced between \$13,000 and \$60,000. Features like dynamic LSI diagnostics and Autotrack™, the guided clip system that reduces your operator's probing time and error, and saves money.

We've got more logic test systems operating in the world than anyone. For data out today, CALL COLLECT (415) 965-0350. Or, circle the number below for general data.

For a complete technical package, drop a line on your company letterhead to Don Harter, Fluke Trendar Corporation, 630 Clyde Avenue, Mountain View, California 94043.

In Europe, write Fluke (Nederland) B.V., P.O. Box 5053, Tilburg, The Netherlands. Or, telephone: (013) 673973. Telex: 52237.





## Voice Data Entry Computer Terminal Allows User to Select 900-Word Vocabulary

The Intelligent Voice Terminal enables operators to enter data directly into a computer in familiar English language terms by speaking into a microphone or telephone handset. Operating with a vocabulary of up to 900 words, the user programmable system can significantly increase overall accuracy of data entered into computerized data bases by allowing errors to be immediately and easily corrected at the source.

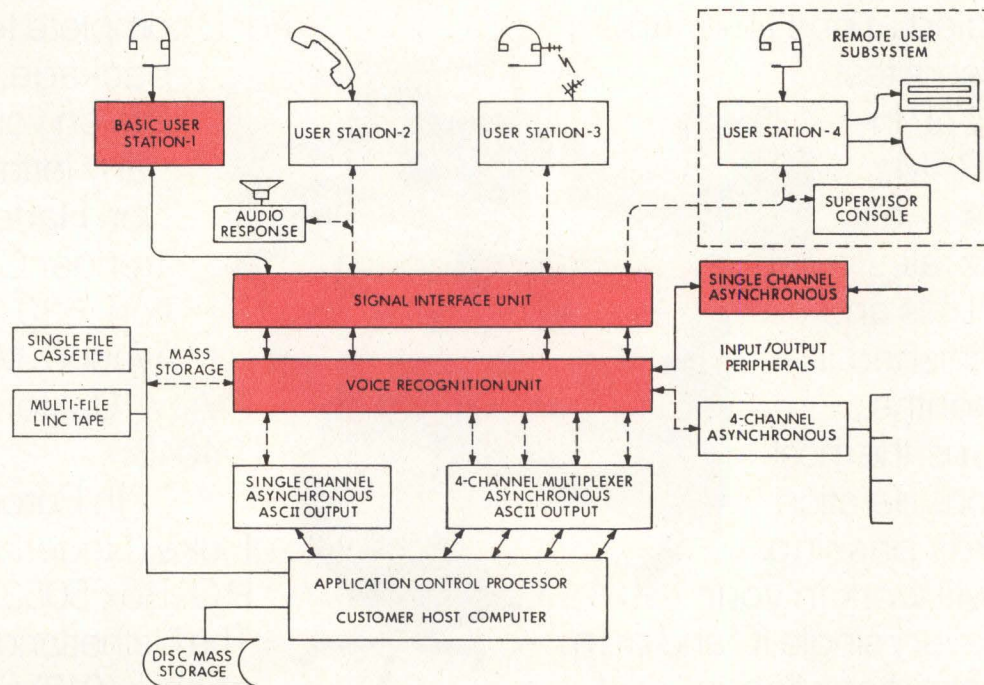
Developed by Interstate Electronics Corp, 707 E Vermont Ave, PO Box 3117, Anaheim, CA 92803, a basic system contains an input/operator feedback station, intelligent controller (user programmable processor), asynchronous output or control interface, and executive software. An ex-

panded system will handle up to four user-input stations simultaneously, provide audio response through a voice synthesizer unit, and accommodate optional features for computer interfacing, i/o peripherals, and mass storage. Single or multiplexed 4-channel ASCII interfaces allow completely interactive operation with most computers and information processing systems.

Heart of the terminal is an acoustic pattern classifier that produces a digital code in response to a received utterance. The classifier consists of spectrum analyzer, analog multiplexer and A-D converter, programmed digital processor, reference pattern memory, and output interface. The spectrum analyzer divides

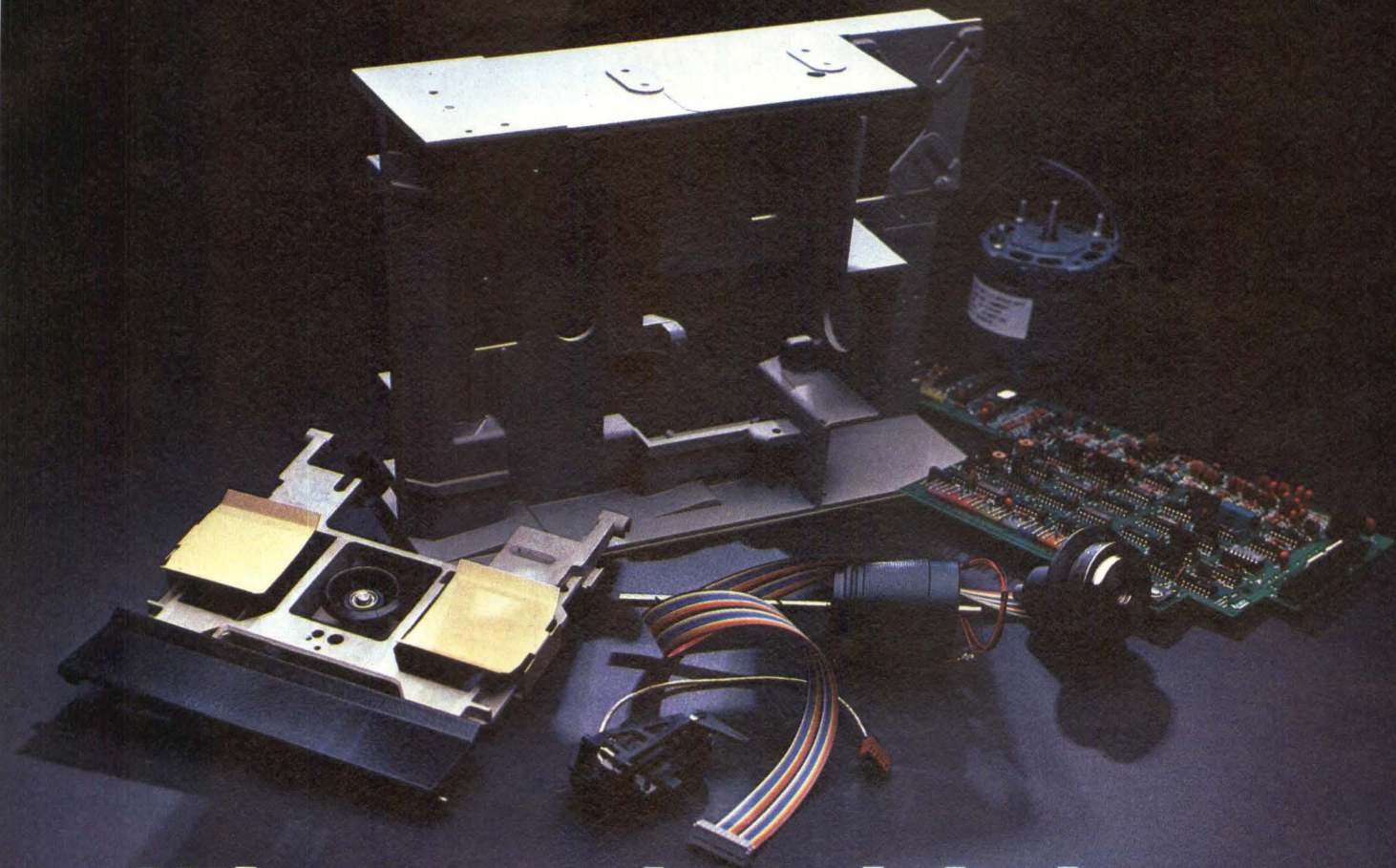
the input speech signal into 16 frequency bands that cover the useful frequency range. By means of parallel detection and lowpass filtering the resulting 16 analog signals represent a power spectrum that constitutes the feature for speech classification.

A coding compressor compensates for changes in the rate of articulation and reduces the spectral data generated by each utterance to a fixed-length code for the classifier. It reduces every word, regardless of length, to a 240-bit pattern. A word boundary detector establishes the start and end of each utterance by experimentally determined criteria. During the training period, the operator repeats each vocabulary word. The estimator compensates for variations to form a 240-bit reference pattern stored in the memory to represent a particular vocabulary word.



Basic voice terminal uses intelligent terminal controller comprising voice recognition unit and signal interface unit, single voice channel with user station, and asynchronous interface. Providing up to 900 vocabulary words, Interstate Electronic's basic system can expand to control up to three additional voice channels





# When you break it down you see why it stands up.

Something special for PDP-11<sup>®</sup> users.

When the Remex-11 disk system was announced, all the talk was about the accompanying software.

Like how we can pack more data per disk and accomplish fast block transfers. IBM and DEC media compatibility. Soft sectoring. Ease of programming and more.

But our hard-wearing hardware deserves a message all its own.

We feature high quality disk drive mechanical components, including precision heads with geometry identical to that of IBM.

Instead of the typical lead screw configuration, we incorporate a V-groove lead screw and ball bearing stylus carriage. You get faster stepping with far less friction. And no worry about frequent disk realignment maintenance to assure track-to-track seeking accuracy.

To precisely center diskettes, Remex has replaced the usual (and cheaper) media cone with a special flexible clutch mechanism.

Naturally, this kind of preventive engineering helps keep drives from wearing out. But more

importantly, from an accuracy standpoint, it helps keep them from "wearing out of tolerance," assuring excellent media interchangeability now and later on.

Other unique features further assure gentle media handling: An anti-crunch interlock door mechanism, and a larger diskette opening.

It's all part of the quality package Remex insists on. The result is a flexible disk system packed with control electronics and up to four drives capable of over 30,000 hours of normal use. With nationwide service to back it up.

For more information, contact: Ex-Cell-O Corporation, Remex Division, 1733 East Alton St., P.O. Box C19533, Irvine, CA 92713. Phone: (714) 557-6860. TWX: (910) 595-1715.

Ex-Cell-O Corporation

**REMEX** DIVISION

Paper isn't the only thing we look good on.

CIRCLE 25 ON INQUIRY CARD



# “Simplicity is the key to advanced fiber optic terminations. That’s why OPTIMATE connectors light the way.”


Meaningful progress in fiber optics technology is no longer hampered by impractical termination techniques. Today, AMP innovation is opening the way for an expanding array of applications.

We are especially proud of the unique contributions of our OPTIMATE line. These connectors have made universal termination possible for a wide variety of fiber optic cable. And they do it simply, quickly and with highly repeatable accuracy. Single optic fibers, as small as .004", can be terminated and OPTIMATE connectors incorporate a resilient material which ensures optical centering. Precise, accurate polishing is easy and fast, thanks to a simple adaptor.

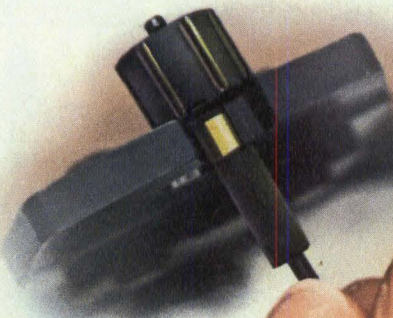
There are more OPTIMATE contributions...such as providing for the intermixing of fiber optics with conventional power or signal cable in a wide range of standard housings. And more are on the way. Because we at AMP have over 2,000 people involved in research, development and engineering

activities alone. And because we are committed to the same kind of leadership in fiber optics that we have achieved in other termination areas.

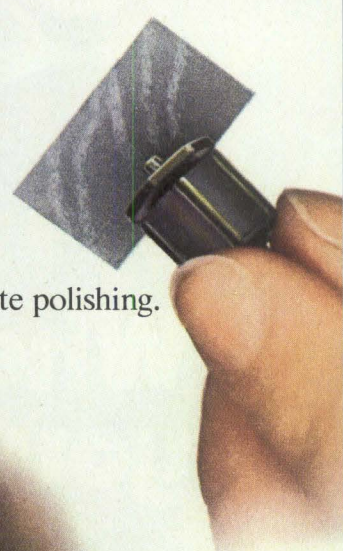
For more information on our OPTIMATE line, just call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.



1. Few parts to assemble.

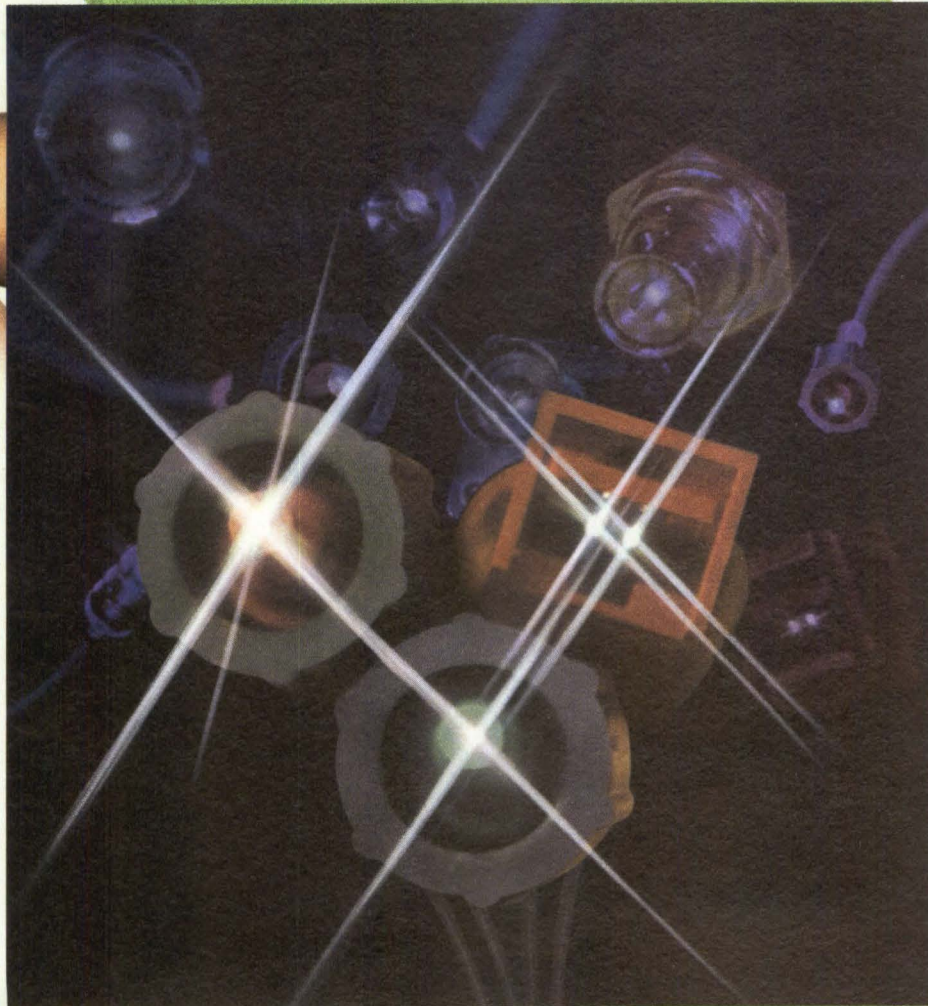


2. Simple, proven crimp.



3. Accurate polishing.






**AMP has a better way  
...Fiber Optics**



To help you innovate, two **OPTIMATE Kits** are available: just connectors, cable and tooling, or complete with active devices by Motorola Semiconductor Products Inc., and predrilled circuit boards for construction of optical links with TTL or CMOS input/output.

For more information, call Customer Service at (717) 564-0100.

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**AMP**  
INCORPORATED

CIRCLE 26 ON INQUIRY CARD



# Upgrade your system with Mostek's 64K ROM.

Mostek's newest ROM, the MK 36000 offers 24-pin compatibility with our complete family of 8K and 16K ROMs, as well as existing EPROMs. That means you can achieve higher system density at a much lower cost.

Mostek's 64K ROM can be accessed in 250ns max; it requires no more than 220 mW active power, and automatic standby power is just 25 mW typical.

Mostek's widely copied Edge-Activated™ design concept provides many other features including +5V only power with ±10% tolerance, on-chip address latches, totally

	NUMBER OF BITS	PIN-COMPATIBLE	ACCESS TIME	ACTIVE POWER (MAX)	STANDBY POWER (MAX)
MK 30000	8,192		350ns	330 mW	330 mW
MK 34000	16,384	Yes			
MK 36000	65,536		250ns	220 mW	40 mW

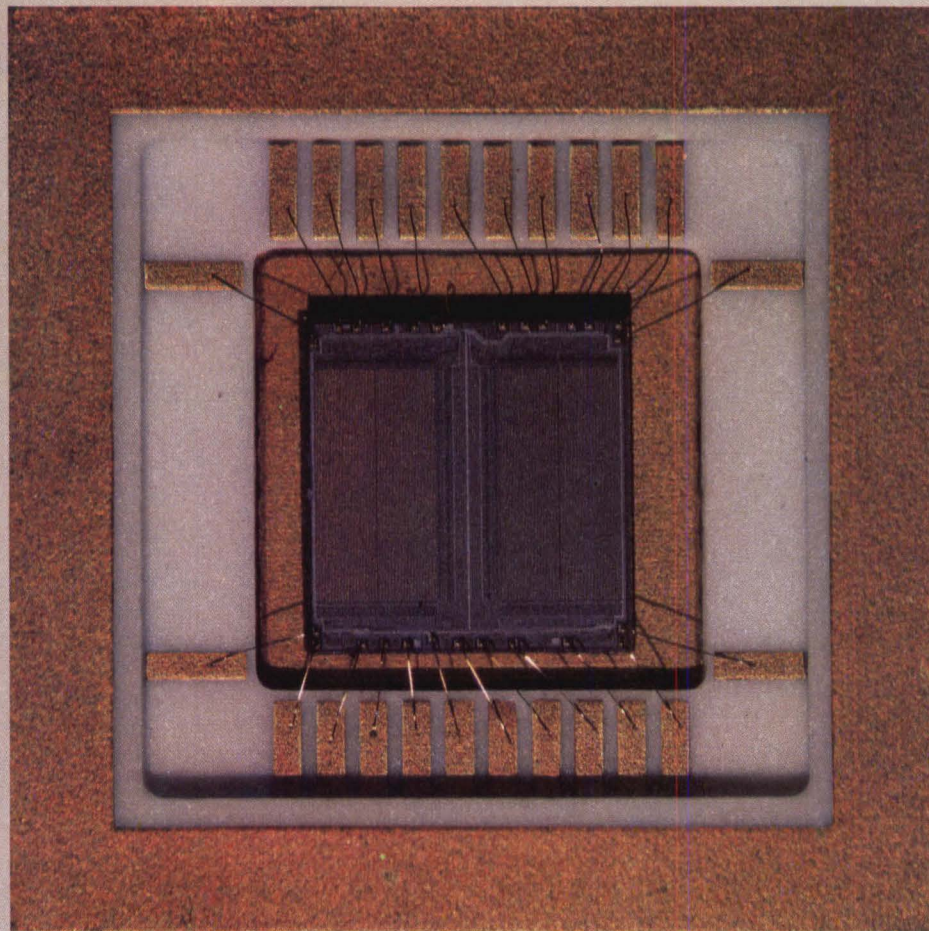
static operation, and direct TTL compatibility with common I/O.

Not only do you get all that in the standard 24-pin package, but you can get it now. There's no better way to upgrade your system than

with Mostek's 64K ROM.

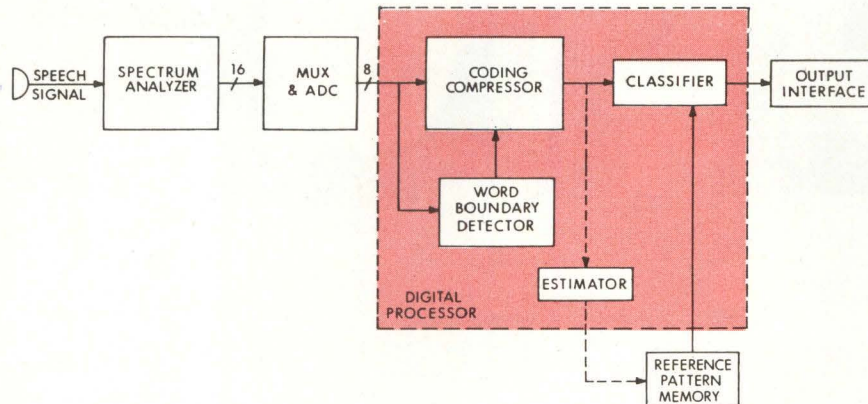
For more information on Mostek ROMs, call a Mostek distributor or sales representative now. Or contact Mostek at 1215 West Crosby Road, Carrollton, Texas 75006; telephone (214) 242-0444. In Europe, contact Mostek GmbH, West Germany; telephone (49) (0711) 701045.

## MOSTEK.



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Essential to terminal's ability to accept voice data entry is acoustic pattern classifier, which is made up of spectrum analyzer, analog multiplexer, and A-D converter, programmed digital processor, reference pattern memory, and output interface

These 240 bits represent the tendencies common to the utterance and the variations that are inevitable when a human being repeats the utterance several times under varied conditions.

After the system has been "trained" to a particular operator's voice, each new pattern from the coding compressor is compared with a syntactically determined subset of all previously learned reference patterns in memory. In sum, the system not only learns the desired vocabulary word, but learns also to distinguish it when spoken with the variations normal to the speech habits of a particular operator. Recognition accuracy is greater than 99%. In addition, its syntax processor allows organized vocabulary lists for specific interactions so that a rejection rate of 90 to 98% of invalid inputs, including extraneous noise, is achieved.

Supplied as an integral component, VOICE (voice-oriented in-core executive) operating system allows users to specify system parameters. Among these are configuration parameters, including vocabulary size, number of users, configuration of I/O devices, and number and size of internal buffers and data arrays; dictionary of vocabulary items to be used along with representations for each vocabulary item; and a dictionary of prompt and error messages. Also user-specified is an action structure associating an appropriate system action with each command that is recognized. Actions may range from simply outputting a code associated with a recognized word to executing a complex computer program that is a function

of several previously input commands. A syntax structure associates subsets of the dictionary with specific functions to be performed in the application. The syntax structure provides a context for the user, and permits the use of large vocabularies without loss of recognition accuracy.

A variety of voice input and feedback options are available to tailor the terminal to operator and environment. Operator voice characteristics (reference patterns), terminal control programs, and operator input data can be stored using a variety of mass storage devices. Numerous input/output peripheral devices are also available to enable configuration to special requirements. With the telephone compatibility option, a standard telephone handset forms a direct voice link with the host computer.

Circle 170 on Inquiry Card

### Vector Graphic System Uses 32-Bit Micro, Dual Bus Architecture

A microprocessor-based self-refreshing vector graphic system, the MEGAPHIC 7000 provides high performance interactive computer graphics. Designed by Megatek Corp, 1055 Shafter St, San Diego, CA 92106, the total refresh system uses a 32-bit microprocessor and a dual bus architecture to provide capabilities that include selective erase of points without affecting the remainder of the image, 12-bit resolution (4096 x 4096), and 16 levels of intensity.

The graphic display unit (GDU) is composed of a number of independent modules connected to one another by an asynchronous 3-state bus structure. This architecture facilitates expansion or addition of options. Four basic modules in a minimum system are vector generator (VG), graphic processor (GP), memory module (MM), and computer interface (CI). Each plugs directly into a motherboard backplane which resides in a rackmountable or tabletop chassis.

An optional peripheral control unit (PCU) plugs into the CI module and controls interrupt priority and data flow between host computer and graphic peripherals via an additional 16-bit bidirectional data bus. In addition, each system includes a 21" (53-cm) diagonal electromagnetic monitor.

Built around bipolar bit-slice architecture for speed and versatility, the 32-bit wide graphics processor controls access of the graphics display list stored in the memory module, interpreting display data, controlling graphics functions, and preparing x-y coordinate pairs for input to a FIFO memory. The vector generator incorporates a proprietary design that provides sharp, constant intensity vector. 12-bit resolution and 16 levels of intensity are standard. A FIFO buffer and high speed normalize circuits are used to supply maximum average throughput and to permit the digital portion of the system to keep up with the high speed and precise ramp-comparator vector complement to the magnetic deflection tube technology. Each vector generator can control two monitors, with either identical or dif-



# BENCHM

**Before you design-in  
a Z-80, 6800 or 8085, compare it with  
the high performance R6500.**

Rockwell's R6500 delivers boosted performance and economics through its third-generation pipelined architecture with 13 powerful addressing modes, true indexing capability, complete decimal/binary arithmetic mode selection, on-chip clock and proven 2MHz performance. Prove it to yourself — Benchmark it!

R6500





# MARK IT!

## **R6500 offers innovative architecture and technology.**

The 8-bit R6500 is produced with N-channel, silicon gate, depletion load technology and innovative architecture. The result is smaller, faster chips to keep your system costs down and performance up.

A family of ten software compatible CPUs in 28- and 40-pin DIP packages give you the most cost-effective fit for your application. Prove it to yourself — Price it!

## **R6500 is designed for greater memory and I/O efficiency.**

Of the leading NMOS microprocessors, only the R6500 has 13 addressing modes and true indexing capability. More addressing modes coupled with an advanced instruction set makes programming the R6500 easy and efficient. Fewer program steps means lower memory cost and faster program execution.

R6500 memory-managed I/O eliminates performance bottlenecks associated with the separate I/O buses, I/O commands and register overhead required by other microprocessors.

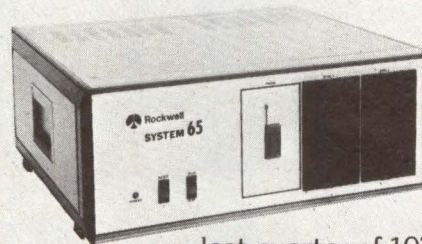
A broad selection of memory, I/O and combination memory-I/O-timer circuits are available. And Rockwell is presently delivering the industry's first fully static 32K ROM — the R2332 — and the industry's fastest 32K ROM — the R2332-3.

## **SYSTEM 65 gets you started for less.**

SYSTEM 65 Microcomputer Development System is efficient and easy-to-use and is equipped with dual mini-floppies. It's priced at only \$4800.

ROM-resident SYSTEM 65 firmware features a two-pass assembler, text editor and symbolic debug/monitor package. Current loop, RS-232C, printer and scope sync ports are also provided. The optional USER 65 (User System Evaluator) module extends the power of SYSTEM 65 for in-circuit emulation.

Other design support includes KIM-1, TIM, timesharing cross-assembler, complete documentation and extensive applications engineering.



Industry researchers say the multiple-sourced 6500 outshipped the Z-80, 6800 and 8085 during the last quarter of 1977. Benchmark it!

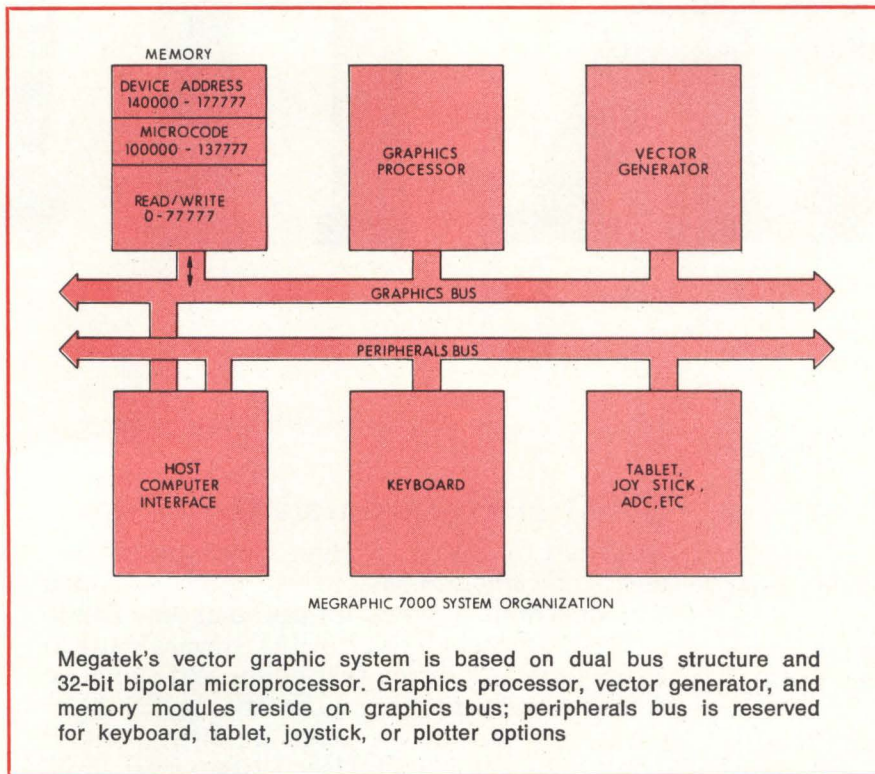
For more information, contact your local Hamilton/Avnet distributor or write: D/727-A Microelectronic Devices, Rockwell International; P.O. Box 3669; Anaheim, CA 92803 or phone (714) 632-3729.



**Rockwell International**

...where science gets down to business





ferent images. Two modules can be plugged into each system chassis, to drive four individual displays.

Memory modules use fast 4k RAMs for display refresh. Each module can accept up to 4k (32-bit) words RAM and 2k (32-bit) words p/ROM. Each system accepts up to eight memory modules.

### Intelligent Clustered Terminal System Offers 3270 Emulation

Capable of supporting eight keystations and four printers, System 4000, an intelligent clustered terminal system, can perform onsite processing independently within a cluster even if communication with the central processing unit is broken. In designing the system, Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166 built in emulators that allow operation in IBM 3270 and 2260 terminal modes, cutting line costs for users of those terminals by concentrating data.

System components include cluster controller/processor, floppy disc storage for up to 1M bytes of data, keyboard/display stations, and high

Flexibility of the equipment is not limited to standard options or configurations. Standard (DMA) interfaces and graphics software modules are available for DEC PDP-11 Uni-bus™ and Data General Nova™ and Eclipse™ minicomputers, allowing users to chose the host computer.

Circle 171 on Inquiry Card

speed line printer. Terminals are capable of buffered synchronous operation at data rates up to 9600 bits/s. Keystations can function in different modes simultaneously, with some performing online data entry over communications lines, while others edit local data on disc. Keystations and printers operate over a single coaxial cable at distances up to 2000 ft (610 m) from the main cluster.

Both application and emulation programs in the system are user programmable. Applications programs provide a uniform method of accessing data in disc storage; programming may be done in COBOL and ESAL. For emulation, high level KCL and COUPLE languages are used in programming terminal control and communications protocol.

Circle 172 on Inquiry Card

### Computer Systems Improve Operating Speed With High Performance Processors

Among the features of 1000 F-series computer systems introduced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304 are improved operating speed, a hardware processor for floating point operations, and use of 350-ns 16k RAMs. The series includes the memory-based model 25 and the disc-based model 45, which handles main memory arrays as large as 2M bytes, and F-series computers, models 2111F and 2117F.

Speed improvements in the F-series processor are attained by use of a scientific instruction set (sis) for hardware execution of transcendental and logarithmic functions, a separate hardware processor for faster execution of floating point instructions, a set of microprogrammed routines that accelerate FORTRAN performance, and 16k RAM high performance memory. The scientific instruction set is a group of hardware-executed instructions that calculate trigonometric and logarithmic functions of floating point numbers at extremely high speeds. The instructions use the hardware executed floating point instruction set as a computing resource, allowing the processor to complete a sine function in 47.6  $\mu$ s. The fast FORTRAN processor accelerates commonly used FORTRAN operations, such as parameter passing between sub-routines, GO TOs, and array address calculations.

When coupled with computation features provided by the processor, RTE-IV, the realtime executive operating system, provides the model 45 with ability to handle programs that include data arrays as large as 2M bytes. An extension of RTE-III and -M operating systems, the executive supports user program code up to 54k bytes in each of 64 memory partitions. Space available for user code is independent of operating system size or number of drivers. An extended memory area addressing capability allows 2M-byte arrays of data to be accommodated. Concurrent execution of realtime, interactive, and batch programs is possible.

Graphics capabilities for 1000 series systems are provided by GRAPHICS/1000 software. A graphics plotting package allows plots to be described in any coordinate system and then converts automatically to whatever



# Take a chance on a power supply and win an airline trip.



## Red Eye Flights to Customer Sites

A chancy power supply's bottom-line cost doesn't show up on a price list. It shows up in increased emergency service calls, total aggravation, and catastrophic downtime costs to the customer. Our Switching Regulated Power Supplies - the Dependables - can minimize such worries.

## Time Proven Winners: the Dependables

For over 19 years, the Dependables have proved their reliability in OEM digital applications where superior line and dynamic load regulation are needed. And their low RFI/EMI and low output ripple (less than 3 mV peak-to-peak at line frequencies) make them ideal for sensitive analog applications.

## Brownoutproof: These Days a Must

The Dependables can supply their specified regulated outputs **at full load** over input variations from 92 to 138 or 184 to 250 VAC. And they'll keep it up for several minutes even if the input drops to 70 or 140 VAC. If AC fails completely, the supplies will hold up for at least 30 mSec., allowing orderly shutdown or shift to optional DC backup. **Catalog DP-27** gives details on our single output supplies and brownoutproof features.

The tables at the right list our standard single and multiple output supplies. Other configurations can be provided. Standard DC input voltages are 48, 120 or 220 VDC.

## Multiple Output Supplies

AC Input - Model Number	PM2675	PM2676	PM2677	PM2678
DC Input - Model Number	PM2775	PM2776	PM2777	PM2778
Total Power	375W	600W	750W	850W
Main Channel Max Power	250W	500W	600W	750W
Second Channel Output	10 amperes or 150 watts			
Third Channel Output	10 amperes or 150 watts			
Fourth Channel Output	4 amperes or 75 watts			
Standard Output Voltages	2, 3, 5, 12, 15, 18, 21, 24, 28			

## Single Output Supplies

AC Input - Model Number	PM2496	PM2497	PM2498
DC Input - Model Number	PM2721	PM2722	-
Outputs:	Volts	Amps	Amps
	2	100	200
	3	60	100
	5	50	100
	5	-	150
	12	25	60
	15	25	50
	18	22	45
	21	18	38
	24	16	33
	28	13	27
			400
			200
			200
			300
			120
			100
			90
			76
			66
			54

To find out how the Dependables can keep your system on the air and your maintenance people out of it, call or write Pioneer Magnetics, Department B, today.



**Pioneer  
Magnetics**

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Telephone (213) 829-6751 • TWX 910-343-6249



## Whose whose in LSI-11 memories?

### Strand Century, Inc.

Los Angeles, California

The company:  
The leading manufacturer of memory light control systems for theatrical productions and TV shows.

Notable application:  
Lighting controls for the Broadway hit "Annie."  
(Photo 1, courtesy Martha Swope.)

Whose CPU:  
Digital Equipment Corporation LSI-11

Whose memory:  
Monolithic Systems Corporation MSC 4601 Dual Height

Whose decision:  
David Cunningham,  
Director Research and Development

Comment:  
"We've been buying both quad and dual height memories from Monolithic Systems for several years. The outstanding cooperation of their people and their on-time deliveries were major factors in selecting them."

### American Sign & Indicator Corporation

Spokane, Washington

The company:  
The world's largest supplier of computer directed lighted signs, scoreboards and color displays.

Notable application:  
Mark 400 Spectacolor Display on Times Square  
(Photo 2, courtesy American Sign & Indicator Corporation.)

Whose CPU:  
Digital Equipment Corporation LSI-11



2.



3.

Whose memory:  
Monolithic Systems Corporation MSC 4601 Dual Height

Whose decision:  
David Cole, Director of Materials

Comment:  
"Our displays have used Monolithic Systems' LSI-11 memories exclusively since 1976. Cost and delivery were the primary reasons for changing vendors and Monolithic's new dual height version has kept us convinced we made the right choice."

### EG & G Princeton Applied Research Corporation

Princeton, New Jersey

The company:  
The leading manufacturer of signal recovery

instrumentation and pioneer in multichannel electro-optical detection techniques.

Notable application:  
The OMA-2 Optical Multichannel Analyzer (Photo 3) permits real-time spectral analysis from below 200 nanometers to nearly 2.0 micrometers. RAM memory is used for storage of the scan format.

Whose CPU:  
Digital Equipment Corporation LSI-11

Whose memory:  
Monolithic Systems Corporation MSC 4501 Quad Board

Whose decision:  
John Zipper, Project Manager

Comment:  
"We've standardized on Monolithic Systems' LSI-11 quad memories for two reasons...price and they work."

### Your company

Whether your LSI-11 based system is a leader in the industry or heading in that direction, head in our direction for LSI-11 compatible memories. For price, delivery and reliability.

**DEC compatible memories... from the first.**



Monolithic Systems corp

14 Inverness Drive East  
Englewood, Colorado 80110  
303/770-7400

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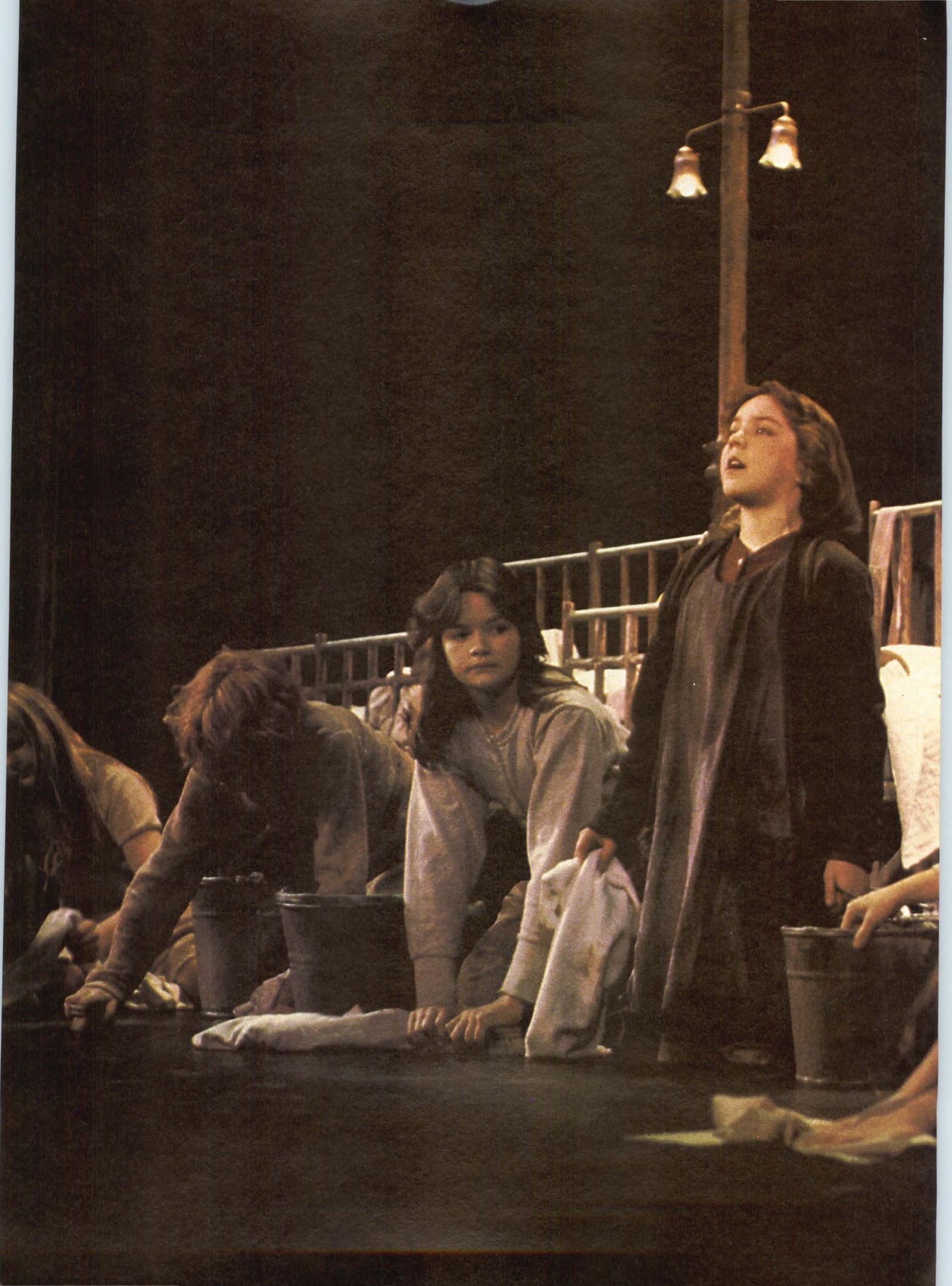
CIRCLE 30 ON INQUIRY CARD

1. (Right) A scene from "Annie." Presented by Mike Nichols. Winner of 7 Tony Awards -1977 -including Best Musical, Best Musical Award 1976-77, N.Y. Drama Critics' Circle. Produced by Irwin Meyer, Stephen R. Friedman and Lewis Allen.

2. (Left top) World's largest computer controlled Spectacolor display at the nation's number one sign location, Times Square in New York City. Eighty-two hundred lamps enable the extraordinary system to perform cartoon like animation in up to 17 different colors.

3. (Left bottom) Just as the human eye detects the variations in the visible light spectrum, the OMA-2 provides a real-time readout of wavelengths and intensities of this spectrum. Suitable detectors allow OMA-2 to "see" into the ultraviolet and infrared regions as well.









F-series processors in HP 1000 series, model 45 add hardware floating point processor, scientific instruction set, and fast FORTRAN processor in form of micro-coded routines to provide performance needed in computation intensive applications

coordinates are appropriate to the display peripheral being used. The package accommodates a choice of 2648A raster-scan terminal, 7245A thermal plotter-printer, or 9872A 4-color graphics plotters.

Representative prices for units in the series include model 25 with F-series processor, 64k-byte memory, and 2645 console terminal at \$27,500; model 40, using the E-series processor

with 128k-byte memory, 2645 terminal, and 7906 20M-byte disc drive, supported by RTE-IV begins at \$40,000. Combining all the enhancements with 128k-byte memory, 2648 graphics terminal, RTE-IV operating system, 20M-byte disc, and graphics plotting software, the F-series model 45 is priced at \$46,500 in a desk-styled system.

Circle 173 on Inquiry Card

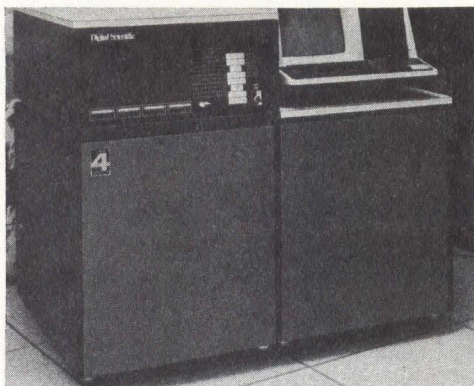
## Midrange Computer Handles Batch and Interactive Applications

META 4<sup>R</sup>/5000 series computers range from low end processors to systems offering performance comparable to that of midrange System/370 CPUs. Digital Scientific Corp, 11425 Sorrento Valley Rd, San Diego, CA 92121 designed the systems to handle high throughput, timesharing applications. System overhead and peripheral idle time are reduced by giving individual users access to all system functions while concurrent jobs are running. Processing results are spooled to any disc subsystem, with-

out programmer intervention, cutting the time required to do the job.

All processing is carried out under control of a timesharing operating system (TFS), which supervises a batch operating system, optional interactive data entry and retrieval system, and a conversational terminal operating system. The operating system also supports APL and BASIC language processors, plus FORTRAN IV, COBOL, and RPG II compilers.

First of the series, model 5020 provides multiprogramming control for up to 32 job streams, including two concurrent card reader/punch jobs, and up to 30 terminals, in interactive, batch, or remote batch appli-



Digital Scientific's META 4<sup>R</sup>/5000 series small computer systems handle high throughput timesharing applications with power of mainframe processors at lower prices than comparable large scale minicomputers

cations. The 16-bit computer is equipped with 500-ns semiconductor memory with capacity for 128k bytes. A microprogrammed control panel permits ready control of program execution, determination of system status, and passage of information to and from programs.

The system accommodates a range of peripheral hardware including standard IBM devices, such as the 1403-N1 line printer, via channel simulation. It interfaces to magnetic tape drivers and to 2310, 2311, and 2314 type disc storage systems, and is capable of handling eight 164M-byte discs for a random-access disc subsystem with 1320M-byte storage capacity. Available communications adapters handle IBM BiSync protocol and 4-, 8-, 12-, and 16-line asynchronous adapters operating at speeds as high as 19.2k bytes/s on each line.

To assure troublefree operation, an extended power sequencing and system parameter monitoring (SENTRY) feature keeps track of various dc power levels, cooling air flow, and temperature throughout the system, and controls sequencing of operations. In automatic diagnostic mode it can isolate suspected power or line problems as well as equipment problems.

Circle 174 on Inquiry Card

## Terminal Processing System Expands Through Modular Plug-ins

A complete terminal processing system in a desktop package, MDT-400 incorporates an 8-bit microprocessor, up to 32k bytes of memory, mini-diskette, keyboard, CRT display, and communications interface. In the systems, Compugraphic Corp, 80 Industrial Way, Wilmington, MA 01887 has provided an extended bus architecture that allows additional memory modules, communications interface, and hardcopy printer options to be added by simply plugging them in. Device handlers are built-in, allowing configuration expansion in the field.

Hardware/software flexibility permits the unit to be used for text or word processing, source data acquisition, distributed processing, and network communications. Each of the 122 keys on the keyboard can be programmed and complete keyboard configurations can be loaded from



# Quick Change Artist.

**Our OEM 600 lpm printer  
has a replaceable character cartridge  
as fast and easy to change as a typewriter ribbon.**

How fast?

Less than a minute.

How easy?

Easy enough for anyone with the strength to pick up 10 lbs. and the skill to change a typewriter ribbon.

Data 100 knows what an OEM wants in a line printer.

Like fast and easy

character set interchangeability. A capability that's standard on our 600 lpm printer.

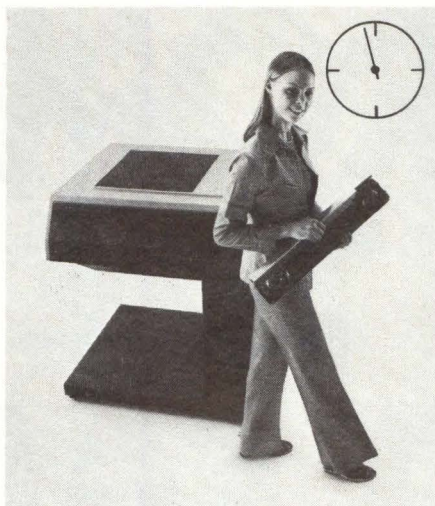
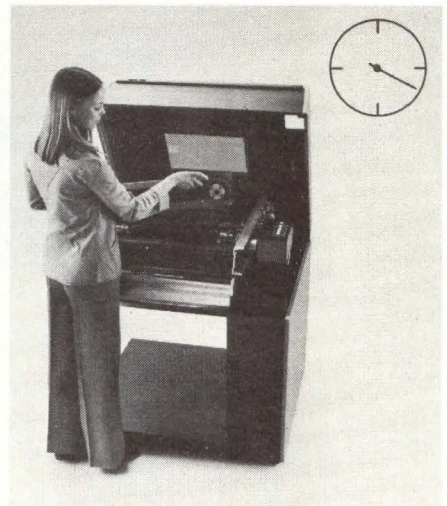
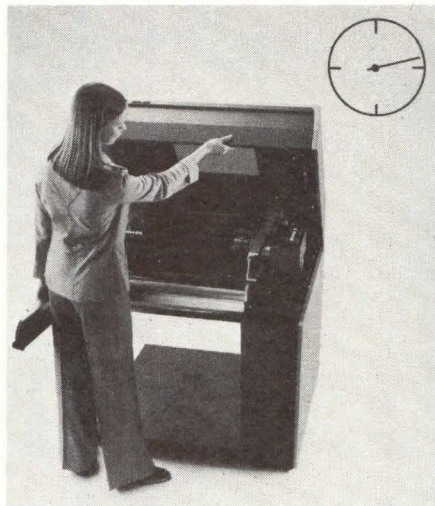
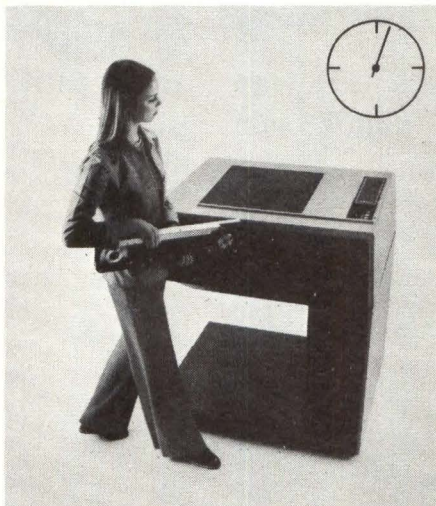
It not only gives the user greater flexibility, but also eliminates the need to buy two line printers just to satisfy that requirement.

Make good sense to you?  
It should. We're adding

this Quick Change Printer to our Data 100 systems, too.

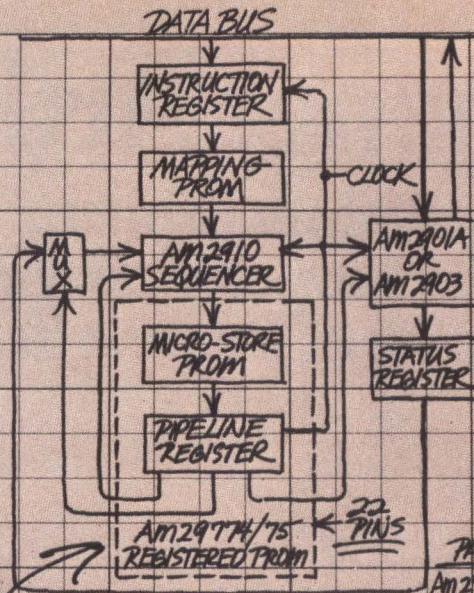
**DATA 100**  
CORPORATION

**Data 100 knows  
what an OEM wants  
in a line printer.**



NEWPORT BEACH CA (714) 549-0982 • SANTA CLARA CA (408) 732-1530 •  
BRAintree MA (617) 848-6100 • SOUTHFIELD MI (313) 358-3984 • EDINA MN (612) 941-6500 •  
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HEMEL HEMPSTEAD ENGLAND (0442) 66511 • BRUSSELS BELGIUM 251-69-72 •  
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INCORPORATING THE PIPELINE REGISTER ONTO THE SAME CHIP AS THE PROM REDUCES INSTRUCTION SET-UP TIME, ALLOWING THE AM2910 TO OPERATE AT ITS MAXIMUM CAPABILITY, ALSO SAVING BOARD SPACE, DESIGN TIME AND POWER!

PARTS	SIZE	ORGANIZATION	OUTPUTS	MAX ACCESS TIME	
				COM2	MIL
Am 2715N/19	256	32x8	00/35	40ns	50ns
Am 271520/21	1024	256x4	00/35	45ns	60ns
Am 271512/13	2048	512x4	00/35	50ns	60ns
Am 271515	4096	512x8	35 only output latches	60ns	90ns
Am 2974/75	4096	512x8	00/35 registered	N/A	clocked through registers

Advanced Micro Devices is in the PROM business. And what an opening!

# PROM'S: THE FIRST FAMILY.



## THE FAMILY.

There's a 256-bit, a 1K, a 2K and a 4K with output latches. Choose open-collector or three-state outputs. All have the same electrical characteristics. All are programmable from the same card set.

Are they fast? Are they fast! Just take a look at the chart.

Performance and reliability? MIL-STD-883 for free. Designed for military performance. Enough said.

And with every AMD PROM, you get one small miracle: After almost two billion fuse hours of testing, the fuse failure rate is zero. Zip. None.

The magic ingredient is platinum-silicide. The programming is fast. The yields high. And the long term reliability is excellent.

## ANOTHER FIRST.

In the family you'll find an Am29774/75, the world's first 512 x 8 registered PROM.

Make room for it. 35% less room. It's a 22-pin part. It's 35% smaller than 24-pin counterparts.

Here's yet a third first: easy pipelined microprogramming. The Am29774/75 has edge-triggered full master/slave registers built right into each output, eliminating an external 20-pin octal register and saving another 20% in board area.

All this means is that the next time you need high performance PROMs, call The First Family.

Call Advanced Micro Devices.

# Advanced Micro Devices



Multiple technologies. One product: excellence.  
901 Thompson Place, Sunnyvale, California 94086  
Telephone (408) 732-2400

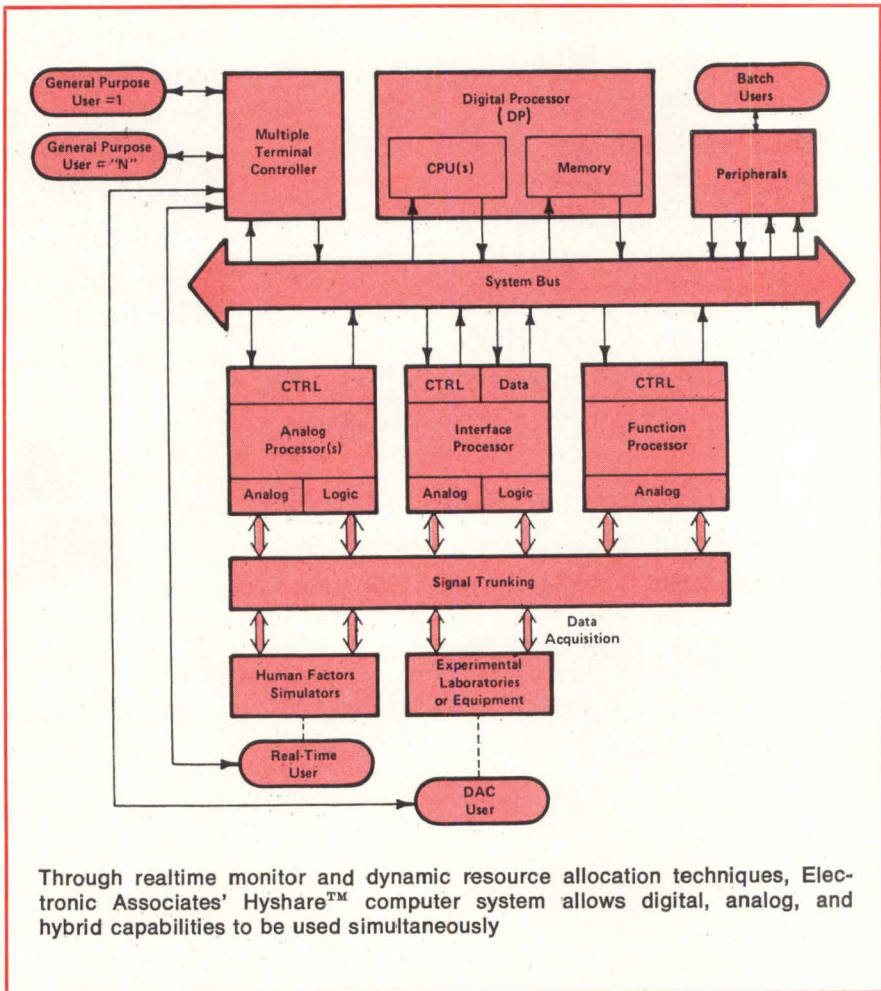


diskette. Eighteen user-defined keys can be changed by an operator with a few keystrokes; the data key allows variable as well as fixed data to be associated with each of these keys. Full cursor controls, scrolling, a 128-char set, and a special key for fast cursor and data positioning provide flexible screen management. Communications include asynchronous or binary synchronous interfaces with software implemented protocols that allow communication with most host processors.

Users can write their own application programs using the program development facility which supports assembler and high level language. Complete file management is provided for transferring data to and from the disc and setting up disc files. Two communications emulators—Teletype 33/35 and IBM 2780—are available.

Representative prices are \$4275 for a model 401 with 8k-bytes RAM, integral minifloppy, CRT, and keyboard; and \$4500 for the 402 with an additional 8k bytes of memory. Substantial discounts are available on quantity purchases.

Circle 175 on Inquiry Card



Through realtime monitor and dynamic resource allocation techniques, Electronic Associates' Hyshare™ computer system allows digital, analog, and hybrid capabilities to be used simultaneously

### Hybrid Computer Meets Demands of Large Scale Multitasking Applications

HYSHARE™, a hybrid computer developed by Electronic Associates, Inc, West Long Branch, NJ 07764, meets multiuser, multitask demands of large simulation and scientific computation laboratories. Consisting of a model 3200 digital computer and up to six high speed analog processors, the A-D and D-A communications interface uses online dynamic resource allocation techniques which allow analog processors to be assigned to specific tasks or linked together.

Capable of functioning as a digital, analog, and hybrid system at the same time, the computer incorporates a realtime monitor and priority structure that permit several tasks to proceed simultaneously. These tasks are interrupt driven hybrid simulation at speeds of 150M, 250M, or more operations/second; time-shared scientific digital computation; analog-only simulations on selected analog processors; setup and check-

out of analog/hybrid programs via the digital computer; and compilation of new simulation programs.

The digital processor is a 32-bit word machine with up to 1M bytes of 600- or 900-ns cycle time core memory. Up to 16 terminals are accommodated through the system bus interface to which all peripherals and analog interfaces are addressed. 600 systems use the 681 10-V analog computer, while 700 systems use the 781, a large scale 100-V analog computer. Both the 681 and 781 are controlled entirely through the digital processor. Systems incorporating the multivariable function generation system, in addition to the analog processors, can operate at digital-equivalent speeds of up to 500M operations/s.

System bus interface, an extension of the system interface bus (SIB) for the digital processor, is data communications/transfer medium for the entire system. All functional elements of the computer—CPU, I/O controllers, and memory—communicate over

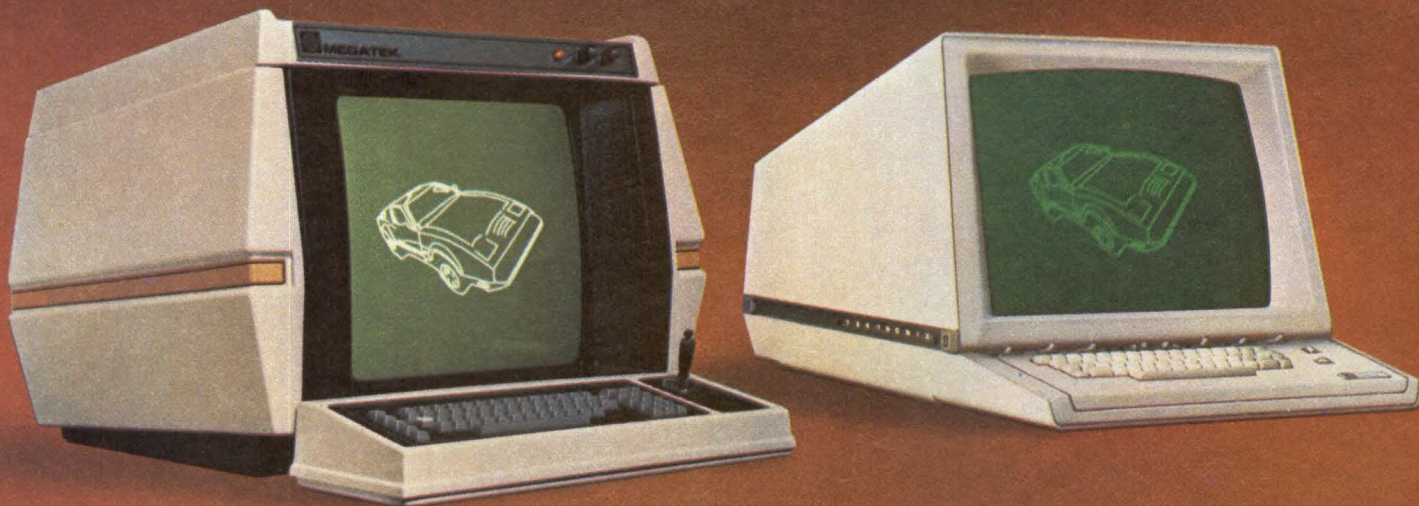
this high speed, synchronous time divided, multiplexed bus, as do the communications interface and optional function generator/processor. Aggregate data rate for the bus is 26.67M bytes/s. The bus is bidirectional, with 32 data lines and 24 address lines, with transfers requiring 150 ns. Direct memory data transfer allows direct device communication to memory without CPU intervention.

The communications interface is fully integrated into the digital processor by direct connection to the bus. Its time-critical design provides fast (<75 μs) interrupt response, multiplexed ADC and DAM conversion direct to and from core, floating point conversion, and variable interval realtime hybrid operations clock.

Up to six parallel analog processors may be included in a given system. Through the interface, and given the appropriate instructions, each analog unit may be assigned to a separate, single task; or they may be trunked together in any



# Twins.



## Your computer can't tell them apart.

Good product, the 4014™. So good, in fact, that we designed our MEGRAPHIC 5014 Refresh Graphics System to do everything the 4014™ does, and more.

The secret? A high performance graphic processor coupled with a high resolution electromagnetic CRT. A built-in minicomputer. And EMUTEK™, our proprietary \*TEKTRONIX® emulator that makes your computer think it's talking to a 4014™.

But, right away, you'll see that one system delivers more graphics for the money.

Zoom, scale, clip, rotate, and "rubber band" images to your heart's content. The 5014 is a refresh graphics system and that means there is no need to erase the whole screen to make changes. The 5014 does it in real time. Plus a full FORTRAN OS.

And, unlike storage tubes, the 5014 has variable brightness levels. So you can see clearly even under the strongest office lighting.

But, best of all, the MEGRAPHIC 5014 costs substantially less than comparable systems. For the OEM, that means better margins. And, for the sophisticated end

user, it simply means more interactive graphics for the money.

So before you buy any graphics system, call MEGATEK at (714) 455-5590.

Don't wait. And don't pay more for less. If your 4014™ just isn't enough system, call Peter Shaw today and ask for a demonstration of the MEGRAPHIC 5014 System.

Thirty days later, you could have twins.

\*\*\*TEKTRONIX® and 4014™ are registered trademarks of Tektronix, Inc., use of which in no way constitutes endorsement.

*The refreshing alternative.*



**MEGATEK  
CORPORATION**

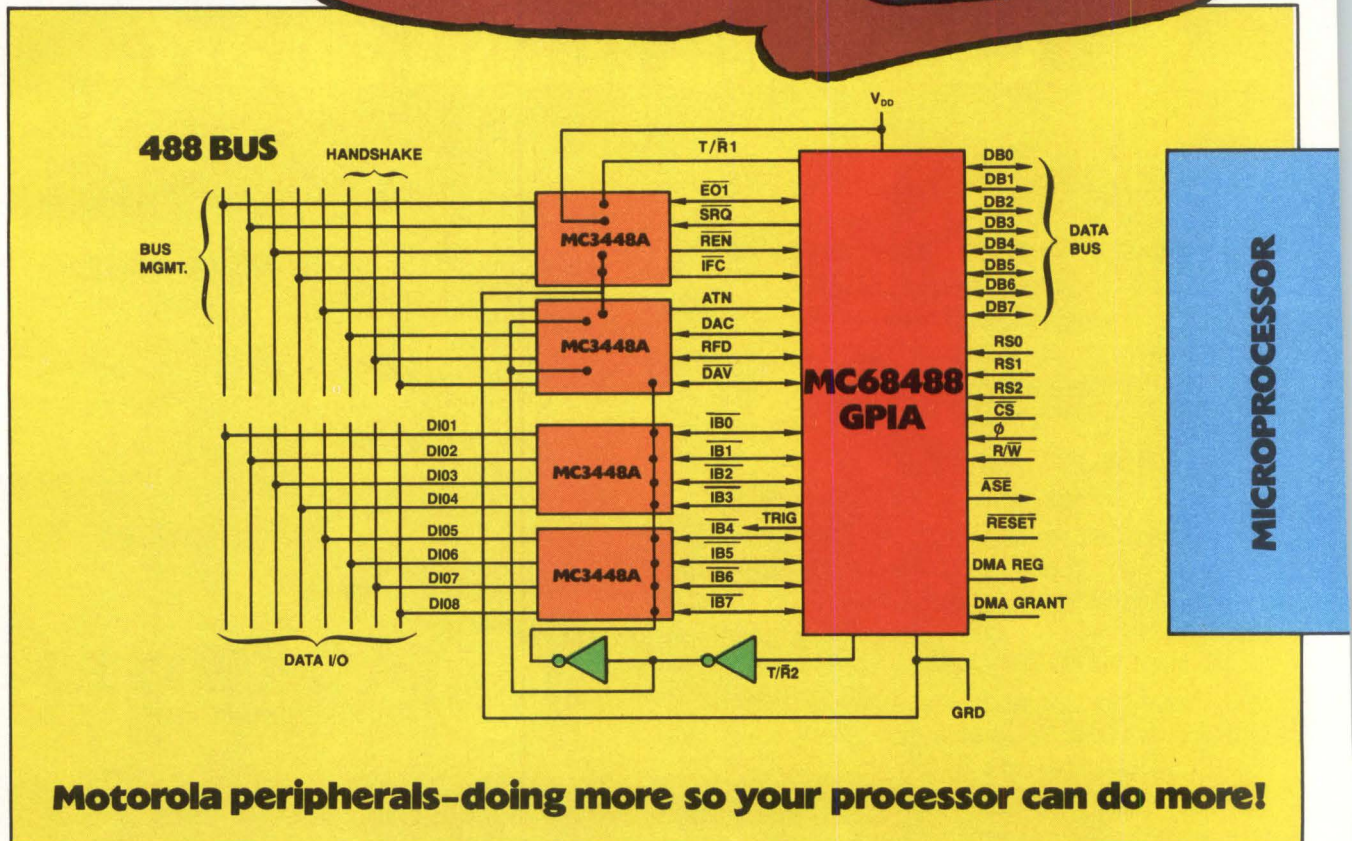
3931 Sorrento Valley Blvd.  
San Diego, California 92121  
Telephone: (714) 455-5590  
TWX: 910-335-2056

14, rue de l'Ancien Port  
1201 Geneva, Switzerland  
Telephone: (022) 32.97.20  
Telex: 23343

CIRCLE 32 ON INQUIRY CARD



# Implement your 488 bus with the MC68488,



**Motorola peripherals—doing more so your processor can do more!**



# the easy, low-cost way Motorola's unique GPIA.

Motorola's MC68488 General-Purpose Interface Adapter, GPIA, makes microprocessors-microcomputers IEEE 488-bus compatible.

Development of the IEEE Standard 488 instrument bus enabled practical interconnection and remote programming or controlling of multiple programmable instruments. However, interface between the microprocessor or microcomputer and the 488 bus remained a costly and cumbersome task.

The GPIA provides that interface simply and inexpensively, and automatically handles handshake protocol needed on the instrument bus. As part of our fully compatible M6800 Family, it's designed to operate with all the M6800 microprocessors and single-chip microcomputers, but it serves other microprocessors, too. It's absolutely unique.



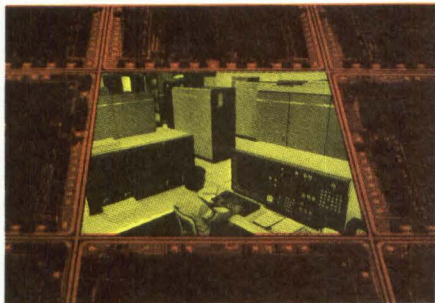
Probably most useful among the GPIA benefits are features like its serial polling capability, single or dual primary address recognition, and secondary address capability. There's so much more: complete source and acceptor handshakes, talk-only or listen-only capability,

synchronization trigger output, and selectable automatic features that minimize software. There's plenty of software to implement your own features, though, never fear.

Many designers will appreciate the GPIA's operation with a DMA controller, the programmable interrupts, and RFD holdoff for prevention of data overrun. As indicated, although the MC68488 is a member of the M6800 Family, with some additional logic it also can serve non-'6800 processors as the easiest, least expensive 488 bus interface. In 25-99 quantities, the plastic MC68488P is \$19.00, and the MC68488L ceramic device is \$21.50.

The GPIA is designed to team up with our MC3448A standard 488 bus drivers, to meet the complete electrical specifications of the IEEE 488 bus. Use it, and we believe you'll agree, it's *the* way to get your instruments on the bus.

## Your microprocessors can do more, because Motorola LSI puts systems on silicon.



Our various LSI and VLSI technologies range across CMOS, NMOS, LSTTL, and ECL, from single-bit to 16-bit capability, and provide a choice among multi-chip, two-chip, single-chip, and the bit-slice approach. There's a full complement of hardware and software support to make it all go.

The M6800 Family is the epitome of our concept for putting your systems on our silicon. With existing and soon-to-be available components, it offers an amazing variety of complexity and performance in applications from controls, to instrumentation, to data handling and communications.

- Multi-chip microprocessor-based systems from the MC6800 to the MC6809
- two-chip MC6802 systems
- single-chip microcomputers and microcontrollers like the MC6801 and the MC6805.

Everything, including development and support hardware and software is fully compatible.

Family memories, RAMs, ROMs, and EPROMs, a variety of peripheral control and I/O chips, and special purpose components like the GPIA generate an unmatched synergism. To ensure that your microprocessors can do more, we don't just build components, we put systems on silicon.

A new brochure covering Motorola's total systems-on-silicon capability is now available. For a copy, and copies of both the MC68488 data sheet and our 32-page IEEE 488 Bus Implementation brochure, circle the reader service number or send your written request to Motorola Semiconductor Group, P.O. Box 20912, Phoenix, AZ 85036.



**MOTOROLA INC.**



# Ramtek makes Colorgraphics easy.

**Ramtek's  
6200A MICROGRAPHIC™**  
computer terminal not only  
gives you affordable color,  
intelligence and graphics,  
it's simple to program as well.



You could be creating your own Colorgraphics within half-an-hour of first sitting down at Ramtek's Micrographic terminal. You won't need a background in programming either. The Micrographic's program language is simple and intuitive.

Your Micrographic images will be exceptionally bright and flicker free as well. The high resolution 512 element by 256 line matrix makes it convenient to put the information you want to see on the screen the way you want to see it.

Since the Micrographic offers full, true Colorgraphics, you can display and use vectors, conics, plots and bar charts. Combine them with independently refreshed high speed alphanumerics, addressable anywhere within a 25 row by 80 character matrix. Characters can be individually erased, modified or updated at will.

And, both graphics and alphanumerics can be displayed in up to eight colors each — out of a possible 64. These are powerful capabilities that have never before been available in one package. And now, you can get them all for a new low price — under \$10,000.

The Micrographic terminal is controlled by a powerful Z-80 microprocessor with up to 28K bytes of PROM and 16K bytes of RAM.

Ramtek control software permits TTY compatibility and high-level graphic functions commanded by ASCII text strings.

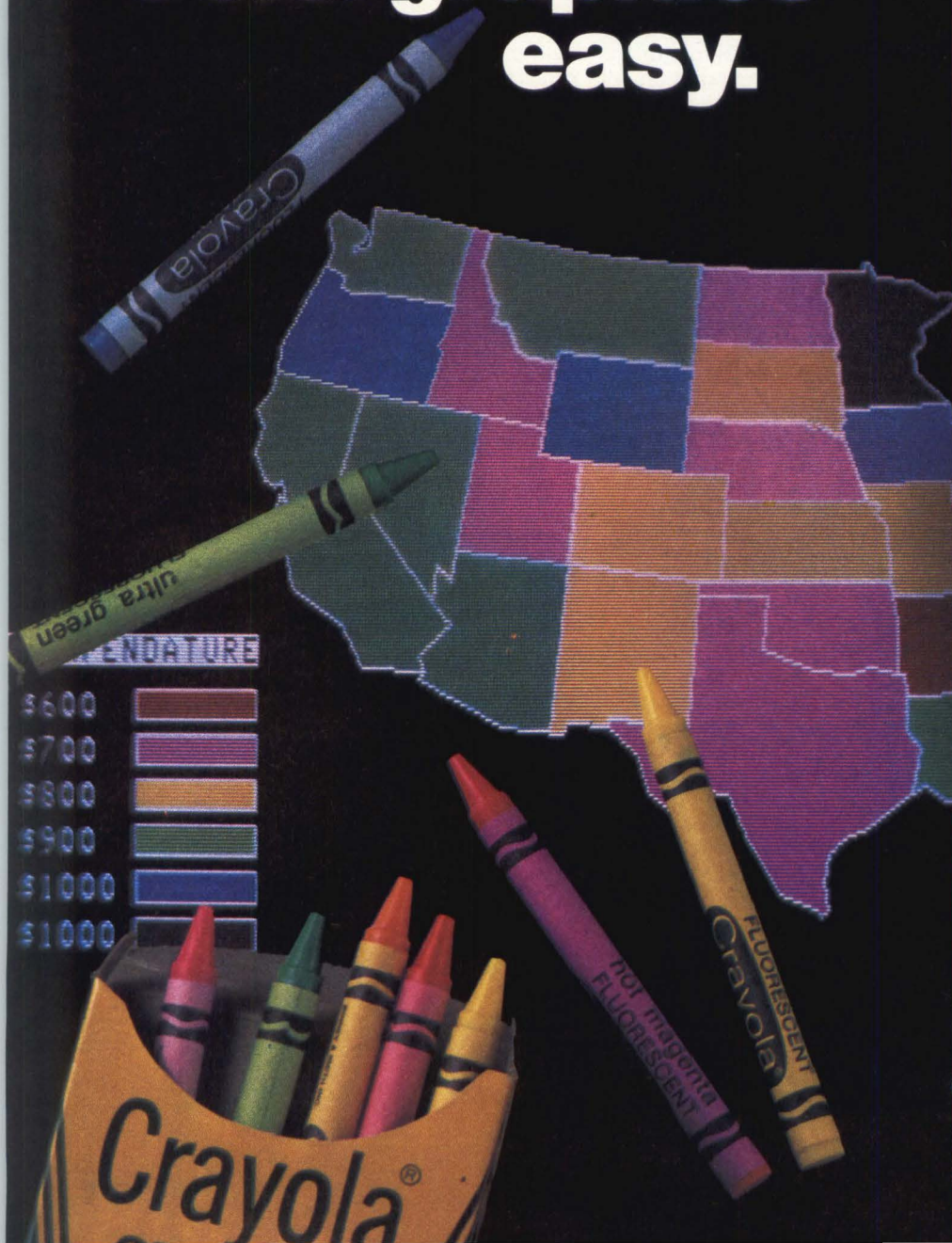
As you need them, there are several options to choose from, including: extended RAM memory, interactive joystick and packaged software.

For more information, write: Ramtek, 585 N. Mary Avenue, Sunnyvale, CA 94086. We'll be pleased to show you how simple Colorgraphics can be with the Ramtek Micrographic terminal.

**ramtek**  
Our Experience Shows

REGIONAL OFFICES: Sunnyvale, CA (408) 735-8400  
Newport Beach, CA (714) 979-5351 — Dallas, TX (214) 422-2200  
Huntsville, AL (205) 837-7000 — Cleveland, OH (216) 464-4053  
Washington, D.C. (703) 960-3550 — W. Germany (0611) 595980

CIRCLE 34 ON INQUIRY CARD





desired combination to obtain the desired analog computation power for problem solution.

Software, in addition to the real-time monitor and the embedded priority structure, includes the ECSL Program Generation-Compilation System and an advanced HYTRAN interactive operations interpreter/executive program. FORTRAN IV compiler, BASIC interpreter, symbolic assembler, hybrid operating systems, and extensive scientific and mathematical runtime libraries are included.

Circle 176 on Inquiry Card

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### **Bus-Oriented Systems Speed Throughput With Dedicated Processors**

Expandable EX3000 computer systems are built around architectural and software concepts of much larger machines. Developed by Extensys Corp, 380 Bernardo Ave, Mountain View, CA 94040 using cost-effective microprocessor circuits for computational and control functions, the system provides distributed processing capability for hardware and multitasking for system software.

Its modular, flexible structure is made up of a series of boards and subsystems, allowing users to put together configurations for a variety of specific applications while offering expansion capability as usage demand increases. Subsystems include FOS 1000, a diskette subsystem with 1M to 4M bytes of online storage; HDS 1500, a hard disc subsystem offering 96M bytes of storage; MTS 400, a multiple terminal subsystem with eight or more independent RS-232-C serial interfaces; and EIT 2000, a terminal/operator processor subsystem with keyboard, CRT, RS-232-C serial interface, and expanded video features. The RM 650 board provides 16k to 64k bytes of RAM storage. MM16, the memory management board, allows bank switching of up to 1M bytes of RAM and has a priority DMA mechanism for high speed transfers. The 8085 CPU board, MPU 805, provides space for 16k of p/ROM, an 8-level prioritized vectorized interrupt, and interval timers/event counters.

The bus-oriented system contains several processors, some of which are dedicated to particular functions. The system's host processor assigns tasks to subsidiary processors which execute them on demand to increase system throughput. Configurations may contain up to 16 subsidiary processors which control any combination of one or more floppy disc, hard disc, or remote terminal RS-232-C subsystems. Up to eight 9600-baud serial lines can be multiplexed into each terminal subsystem; remote terminals can also be plugged into the bus as local operator's terminals.

System software includes a multitasking, multiuser operating system (EMOS), which provides high level interface between application programs and system hardware components. In addition to file handling capabilities and program development tools, system software provides user memory protection and intersystem communication to allow multiple systems to operate with a common data bank.

In a typical configuration the system consists of combination system console/terminal, three remote terminals, 24M-byte hard disc, 200-char/s matrix printer, 192k RAM with DMA, and eight independent microprocessor controlled RS-232 channels. Processing is distributed throughout 19 microprocessors to maintain performance and to support multiuser capability.

Circle 177 on Inquiry Card

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### **Vector Function Chainer for Array Processors Reduces Host Overhead**

Vector Function Chainer automatically ties together array processor assembly-language routines so that a long series of array processor computations can be initiated by a single FORTRAN call from the host computer rather than separate calls for each routine. Announced by Floating Point Systems, Inc, PO Box 23489, Portland, OR 97223, the software is intended for use on the company's AP-120B and -190L processors.

Vector function chainer (VFC) software allows a user to chain together standard math library routines and

user-created routines. While its principle benefit is reduced host overhead, an additional benefit is that programmers can use familiar FORTRAN syntax to create new array processor routines.

Parallel, pipelined computers with optimized architecture for scientific computations, the array processors offer up to 200X increase in computing power for minicomputers, and a 10X increase for large computers. Architecture is optimized for vector data processing with seven independent data paths, floating point adder and multiplier, integer arithmetic unit, memory, and interface. Adequate precision is made available by a 38-bit floating point format.

Circle 178 on Inquiry Card

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### **Networking Systems Offer Distributed Processing At Low Cost**

Distributed processing series 220 DPS networking systems from General Automation Inc, 1055 S East St, Anaheim, CA 92803 are claimed to provide mainframe computing power at terminal prices in source data processing applications. The family offers batch processing capability in COBOL or FORTRAN, a comprehensive ISAM/PSAM file management package, and remote batch communications.

Systems are based on the 16-bit GA-16/220 LSI computer with 128k bytes of 400-ns semiconductor memory, and 10M bytes of online disc storage. Each CPU/cluster processor can support up to four online video display terminals operating in a multitasking environment up to 2000 ft (610 m) away. Systems provide 2780 communications capability for access to most remote host systems and support peripherals including line printers for hardcopy output.

Software includes comprehensive data entry software that provides supervisory functions necessary to use system resources efficiently. Easyform, a forms generation package, allows screen formats to be created online without compilation.

Circle 179 on Inquiry Card



# Bye, Bye D

**\$1795\***

**A Perkin-Elmer CRT  
and a 100 cps thermal printer.**

**If you buy a DECwriter after reading this ad, you deserve it.**

Our popular Pussycat Printer and Model 1100 Interactive CRT Terminal. Together, they do a lot more than a DECwriter III and cost less.

In fact, at \$1795, it's like buying a top-quality printer and getting a terrific little CRT free.

And what a CRT! The Model 1100 displays 80 characters per line in an easy-to-read, 9 x 12 matrix and communicates at up to 9600 baud. Compare that to DECwriter III's puny 1200 baud.

Then when your results are ready, touch the PRINT key and the Pussycat printer lays down a whole screenful of characters in only 20 seconds. But, best of all, the CRT is ready for use again in 2 seconds or less. So the operator can go right back to work.

The Pussycat Printer is silent, too. And, because you print only what you want, there are no mounds of unsightly printout around the machine.

Clean. Quiet. Inexpensive. The Pussycat Printer and the Model 1100 CRT from Perkin-Elmer. Compared to a DECwriter III, they do more and cost less.



\*US domestic price, quantity 75.  
Model 1100 and Pussycat Printer: \$2795, quantity 1.  
Owl-1200 and Pussycat Printer: \$3695, quantity 1.

DECwriter® is a registered trademark of Digital Equipment Corp.



# ECwriter!®

**\$2395\***

**A Perkin-Elmer editing CRT with  
line drawing and a 100 cps thermal page printer.**

You can also plug the Pussycat Printer into our Owl-1200 Terminal and have a powerful editing terminal with forms drawing capabilities and hard copy, too.

Draw forms or bar charts on the Owl, then print them on the Pussycat. The Pussycat even prints inverse video fields for highlighting charts.

The Owl and The Pussycat. Another great CRT thermal printer combo from Perkin-Elmer.

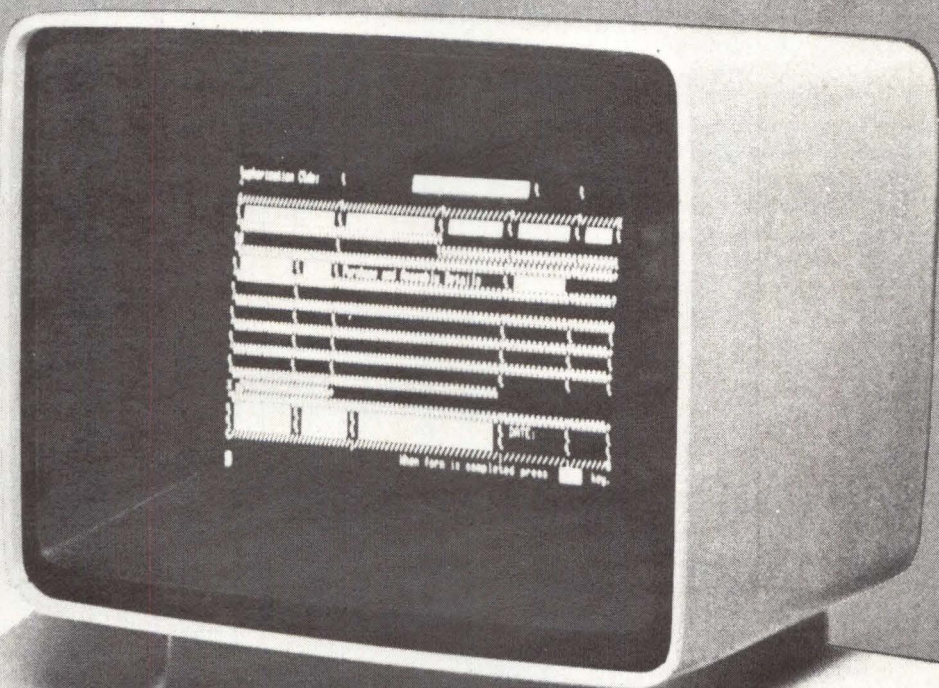
**Call (800) 631-2154, toll free, to order your Pussycat and CRT.**

For more information, write Terminals Division, Route 10 and Emery Avenue, Randolph, New Jersey 07734, or **telephone toll-free (800) 631-2154.**

**PERKIN-ELMER**  
Data Systems

Helping people succeed with computers.

**CIRCLE 28 ON INQUIRY CARD**





## Hardware/Software Combination Increases FORTRAN Performance

A combination of hardware and software, the FORTRAN Enhancement Package substantially improves performance of FORTRAN VI programs on the model 8/32 Megamini<sup>®</sup> computer. Available from the Interdata Div of Perkin-Elmer Corp, 2 Crescent Pl, Oceanport, NJ 07757, the package implements FORTRAN RTL routines in the 2k writable control store, increasing their speed of execution two to three times over assembly level implementation.

Single and double precision routines include trigonometric functions such as SQRT, EXP, COS, SIN, ALOG, DSQRT, DEXP, DLOG, and real and double exponentiation. These occupy approximately 1.5k of the writable control store, leaving 0.5k available for system customization. A software development package includes a microassembler that allows users to create microprograms as simply as assembly level programs, and a support program with debugging facilities.

Circle 180 on Inquiry Card

## Enhancement Memory Expands 360/65 Capacity To 9M Bytes

A plug compatible mainframe memory for IBM 360/65 computers, the ARM-2365G offers memory expansion up to 9M bytes. Produced by Ampex Corp, 200 N Nash St, El Segundo, CA 90245, the enhancement memory provides expansion capability for all versions of the IBM 2065 processor without adding IBM upgrades, and with minimal modifications to the processor.

From one to four memories can be attached to the processor through the 2065 storage discriminator, which creates one to four independent memory ports. This capability permits expansion of systems already fully populated with IBM memory to the desired memory capacity.

The memory is software transparent to the system in operation. Two-way interleaving is performed in the same manner as with IBM

2365-2 memory and each installation includes a convenient reconfiguration capability.

In addition, a software patch is provided for the machine-check handler to implement correct error recovery management with expanded memory. Effective cycle time is 750 ns, with an access time of 400 ns.

The cabinet provides space for 512k to 2048k bytes of memory and requires 8 ft<sup>2</sup> (0.74 m<sup>2</sup>) of floor space. Each cabinet houses a completely independent memory system including interface logic, 2-way internal interleaving, fetch protect, customer engineering panel, and an internal test unit allowing memory testing and corrective maintenance to be performed offline. Since it is non-volatile, no elaborate power backup is required to protect against data loss in the event of a power interruption.

Circle 181 on Inquiry Card

## Operating System Provides Large Machine Capability on Minicomputer

Developed for commercial data processing applications, FAST<sup>™</sup> is an advanced multitasking operating system for Interdata 16- and 32-bit computers. Concepts used by Cybertek Computer Products, Inc, 3255 Wilshire Blvd, Los Angeles, CA 90010 in designing the system are similar to those found in large machine operating systems, such as IBM's 360/370 OS/MVT.

The system minimizes time required to run a program and maximizes CPU utilization. FAST features dynamic memory allocation without fixed partitions, which allows programs to load immediately where there is space in memory. A powerful link-editor minimizes object module load time.

Appropriately, the system handles multiterminal, interactive applications quickly; up to 100 terminals are accommodated simultaneously. Programs can be executed rapidly because of five disc access methods; overlapped I/O, so the processor can execute other tasks while I/O takes place on a previous one; and spooling,

which allows writing printer output files to disc rapidly.

FAST provides a powerful facility for program development. With its IBM-like concepts, storage-to-storage instruction set, and 360/370 BAL-like assembler, it enables easy transition from large machines to minicomputers. The entire system requires as little as 20k of memory for system residence. Two versions—FAST/16 and FAST/32—run on Interdata 16-bit processors and 32-bit machines, respectively. Both versions provide complete task management; memory management services; file management; system control facilities, including a powerful command language; multi-terminal capability; and compatibility with Interdata and IBM software.

Circle 182 on Inquiry Card

## COBOL Software Package Optimizes Programs, Speeds Development Cycle

OPTIMIZER III is intended to both improve COBOL program quality and reduce development costs, by working directly with programmers, providing the information needed to produce more reliable programs with less effort. Developed by Capex Corp, 2613 N 3rd St, Phoenix, AZ 85004, the software presents information to the program listing, showing what the program does and does not do, what was tested, and where performance can be improved.

By providing the programmer with easy-to-use COBOL-oriented information, the need for cryptic hexadecimal dumps is virtually eliminated. Since automatic object program optimization techniques are used, all programs produced are smaller and faster. The result is a reduction in the number of program compiles and test shots required to develop the program, a reduction in printing load, and overall improvement in program performance and reliability.

The package supports all aspects of COBOL programming and operates in conjunction with any IBM ANS COBOL compiler on any of the IBM OS, OS/VS, or MVS operating systems. No system or compiler changes are required.

Circle 183 on Inquiry Card



# Identical twins...almost.



**This one prints.  
\$655.**



**This one prints & plots.  
\$795.**

In 1977, AXIOM pioneered low-cost electrosensitive line printing, setting an example which others have been quick to follow.

However, we believe that once you are the market leader, you should stay out in front. So we're proud to announce the birth of two exceptional new products, the EX-801 MicroPrinter and the EX-820 MicroPlotter which set new standards for versatile low-cost hardcopy.

These babies are beautiful, housed in sleek molded cases designed by the award-winning Inova design group. But beauty is more than skin deep. Each unit is packed with unique features. Like serial RS232C/20mA and parallel ASCII inputs as standard. Reverse printing. Oversized input buffers. Expandable character sets. User program memory for real "intelligence."

Twins, yes, identical, not quite....

## Meet the MicroPrinter

Here's the answer to a micro (or mini) computer's fondest dreams. Designed around the Intel 8048 microprocessor, the EX-801 MicroPrinter operates to 160 cps (that's 14 times faster than a TTY), and gives you the choice of 3

intermixable character sizes to provide 80, 40 or 20 columns on 5-inch wide electrosensitive paper, making this printer ideal for CRT hardcopy, data logging, remote message printing, program listing, record keeping... In fact, any application needing fast, low-cost copy.

## Introducing the MicroPlotter

Our EX-820 MicroPlotter does everything the EX-801 does — plus it plots. Under software control, you have unlimited flexibility to mix alphanumeric ASCII and graphics on any line. Just define the size of each graphic field, and choose from 3 pre-programmed dot resolutions up to 128 dots per inch. Once the fields have been defined, the EX-820 automatically formats graphic and alphanumeric printouts to your specs.

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The EX-801 and EX-820 are both complete stand-alone units, including molded case, power supply, parallel ASCII and Serial RS232C/20mA interfaces, character generator, low paper detector, bell, built-in self tester and paper roll holder. Not to mention a whole range of fantastic low-cost

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state flow and

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for detailed analysis.**

Now, it's easy to get a clear picture of system activity in your minicomputer or microprocessor with HP's 1610A Logic State Analyzer and one of HP's interface boards. Just plug into the system . . . use a simplified menu concept for quick set-ups . . . and with a few simple keyboard entries, you'll have an easy-to-interpret display of your state flow including address, data and control line activity, or the time interval between specific bus-arbitration steps.

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Simple keystrokes let you define sequence requirements for a specific bus-arbitration process. And by selecting the count time, you can measure the elapsed time intervals between all of the specified sequences. Now you can accurately troubleshoot timeout problems or optimize time-dependent code.

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Trace-list menu lets you observe the results of the specified handshake. The time interval adjacent to each event can be either relative (between each event) or absolute (referenced to the trace start). And by defining another trace specification, you can easily monitor program flow in the numerical bases of your choice.

TRACE LIST						TRACE-COMPLETE	
LABEL BASE	A OCT	B BIN	C BIN	D BIN	E BIN	TIME DEC	
SEQUENCE	173062	0	1	0	0	8	US
SEQUENCE	173070	0	0	0	1	6	US
SEQUENCE	173074	0	0	0	0	1	US
SEQUENCE	173075	0	0	0	1	4	US
SEQUENCE	173075	0	0	0	0	17	MS
START	173532	1	1	1	1	1	US
+01	173532	0	0	0	0	1	US
+02	000000	0	0	0	0	1	US
+03	000000	0	0	0	0	1	US
+04	000000	0	0	0	0	1	US
+05	000000	0	0	0	0	1	US
+06	000000	0	0	0	0	1	US
+07	000000	0	0	0	0	1	US
+08	177544	0	0	0	0	1	US
+09	177564	0	0	0	0	1	US
+10	177564	0	0	0	0	1	US
+11	177564	0	0	0	0	1	US
+12	177564	0	0	0	0	1	US
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+14	177564	0	0	0	0	1	US

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088/5

**CIRCLE 36 ON INQUIRY CARD**





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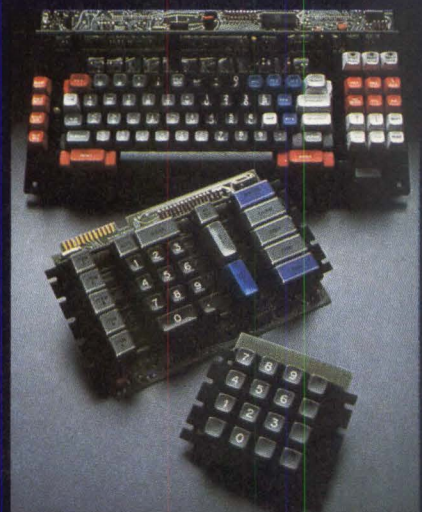
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CIRCLE 37 FOR DATA



## Pascal Software For Disc-Based Minicomputer Systems

A general-purpose, block-structured language noted for ease and speed of use and for its excellent maintainability, 990 Pascal is closely compatible with the standard Pascal as defined by Jensen and Wirth in their "Pascal Users Manual and Report." Introduced by Texas Instruments Inc, Digital Systems Div, PO Box 1444, Houston, TX 77001, the software executes in the multiuser environment of the DX10 disc-based operating system to add over 170 interactive user-oriented commands plus 240 utilities. Additionally, the DX10 operating system supports COBOL, RPG II, Business BASIC, BASIC, and FORTRAN IV programming languages.

Included in the software object license are a Pascal compiler and runtime library, a nester utility for standardized source indentation, a configuration processor to support separate compilation of nested program modules, and a reverse assembler that outputs Pascal object modules in 990 assembly language source format. Minimum hardware requirement is the TI DS990 model 4 packaged disc system, which contains a 990/10 minicomputer with 128k-byte memory, a 10M-byte disc drive, a 911 video display terminal, a single-bay desk enclosure, and a DX10 disc operating system software license.

Circle 184 on Inquiry Card

## Magnetic Card Composer Aids in Preparing Copy for Offset Printing

An electronic direct impression composition unit that can use magnetic cards, the Mag Card Composer, adds flexibility to preparation of copy for publication. Its primary use is preparation of copy to be photographed and converted to offset printing plates; however, a direct image master can be made. Applications in commercial printing, and inhouse printing departments of large and small companies are within the range of this equipment.

The composer is attached to a low profile console which contains the unit's electronics as well as a pack-feed unit for reading and recording

up to 50 magnetic cards with a total capacity of 250k characters. The equipment, introduced by International Business Machines Corp, Office Products Div, Parson's Pond Dr, Franklin Lakes, NJ 07417, offers a built-in memory that automatically retains and replays up to 8k characters of keyboarded copy.

Material entered into the unit is easily reformatted; thus a page of single-column copy can be played out in any configuration the copysetting specs require. Changes in text are done quickly and simply. Once all the information is recorded correctly in memory, the operator gives the unit a few simple instructions, and it automatically prints out the text.

Over 125 fonts are available in 13 languages and 11 different type styles with basic type sizes ranging from 6 to 12 points. All are interchangeable with IBM's other direct-impression composition equipment.

Circle 185 on Inquiry Card

## Large-Scale Computer Exhibits 1.8 Times Speed of Predecessor

FACOM M-200, developed by Fujitsu Limited, 6-1 Marunouchi 2-chome, chiyoda-ku, Tokyo 100, Japan, is 1.5 to 1.8 times faster than the M-190. Connected with up to four CPUs, this large-scale computer exhibits about five times as much performance as an M-190. When connected with as many as four channel processing units (CHP), it can have a maximum of 64 channels. An improved multiple virtual storage (MVS) function is suitable for high speed processing such as timesharing systems.

Use of LSI technology allows reduction in electric power requirements, and results in greater system reliability and economy. Logical elements adopt 100-gate/chip ECL LSI, and the main logical circuit is all LSI. Main storage element uses NMOS LSI with 16k bits/chip to provide capacity for up to 16M bytes, and buffer storage employs bipolar LSI of 1k bits/chip with capacity for 64k bytes. OSIV/F4 and OSIV/X8 operating systems are available.

OSIV/F4 and /X8, provide a range of functions which can meet needs for local batch processing, remote batch processing, online real-time processing, conversational mode

processing, timesharing system (TSS), and Advanced Information Manager (AIM). OSIV/X8 uses "VS Overlay System" technology, and a "Temporary Fix" concept for its multi-virtual storage control.

Circle 186 on Inquiry Card

## Enhancements Add Power to Structural Analysis Programs

Structural analysis programs that are available through CYBERNET Services have been enhanced to provide more flexibility, higher accuracy, and greater capability. CDC/NASTRAN now offers new elements, multilevel substructuring methods, and a labor-saving dynamic analysis feature. EAC/EASE2 has added a plotting postprocessor and a beam special output postprocessor. Internal heat transfer analysis, and element, materials, and structural procedures library additions are among enhancements provided by MARC-CDC. All are available from Control Data Corp, Box O, Minneapolis, MN 55440.

The QUAD4 quadrilateral and TRIAC3 triangular plate elements in CDC/NASTRAN analyze combinations of membrane action, bending, sandwich plate properties, or heterogenous materials. Improvements in theoretical accuracy are particularly noticeable in membrane actions, which provide for linearly varying thickness along the edges.

E2SPEC, the plotting post-processor for the EAC/EASE2 structural analysis program, uses either card input or EASE2 results to create time-history plots or response-spectrum curves, and automatically produces a printer plot of each curve, making it possible to preview printer plots before selecting more expensive pen plots. E2BSO provides greater capabilities in analyzing beams. It will combine load cases, produce tabulation of quantities along any beam and supply a minimum-maximum summary for any number of load cases.

Major enhancement in the MARC-CDC linear and nonlinear structural analysis program is internal incorporation of heat transfer analysis, previously a standalone program, MARCHEAT. □

Circle 187 on Inquiry Card



## Control and Instrumentation Conference Emphasizes Industrial Applications of Microprocessors

As it has done at each of its past three annual conferences, the IEEE's Professional Group on Industrial Electronics and Control Instrumentation once again concentrated its technical presentations on "Industrial Applications of Microprocessors." General topics at the March 20 to 22 conference, held in Philadelphia, Pa, included data acquisition, testing, signal processing, monitoring, motor control, energy systems, and consumer systems as well as varied industrial control applications. In addition, evening panel sessions with extensive audience participation periods were held on I/O analog interfaces and new control devices. The following summaries cover a sampling of papers presented that are particularly relevant to digital control and automation.

### Intelligent Automobile With Artificial Eyes

Engineers at the Mechanical Engineering Laboratory in Tokyo, Japan have developed an "intelligent" vehicle<sup>1</sup> that uses two television cameras mounted above one another on the vehicle's front bumper and hood as "eyes." Road obstacle data "seen" by these "eyes" are converted by a microprocessor into steering, accelerating, and braking commands to the vehicle. On a test track this automobile has been driven successfully at 19 mi (30 km)/h.

Artificial vision and its application to automated devices—robots, for example—are currently subjects of research studies in many countries.<sup>2</sup> In addition, there have been a number of studies on automatically driven vehicles. (Some such vehicles have been driven at 62 mi (100 km)/h by sensing a magnetic field produced by a wire-reference system.) However, Mechanical Engineering Laboratory engineers have added the

ability to "see" the road and have developed a vehicle with functions to control speed and to enable it to turn at a corner. "Problem solving" is accomplished by a microprocessor, 8k bytes RAM, 3k bytes ROM, I/O interface, and D-A and A-D converters.

The two TV cameras function as part of a pattern recognition device to note the presence of obstacles or to indicate a clear path in front of the vehicle. Because the cameras are physically offset, the images seen are shifted from one another vertically. By scanning the images, the spatial shift is converted into a time difference between the two video signals. In order to provide brightness/darkness changing points, the video signals are fed into differential circuits and then to waveshaping circuits (Fig 1).

Both resulting pulse trains are input to an AND gate and then to a flip-flop. By changing the delay time, an obstacle can be detected at any distance between 5.5 and 22 yd (5 and 20 m) and in any direction within the 41-deg viewing area.

The pattern recognition device digitizes the field of view according to the delay time between signals and establishes a mesh of zones (Fig 2). All zones are strobed continuously by the device to detect obstacles or to note clear paths. Output data indicate distance from vehicle to zone, left and right edges of clear paths, and locations of obstacles. Single image scan time is 33.3 ms; processing time is less than 2 ms. Road condition data from the pattern recognition device and speed signals from the vehicle are sent to the problem solving device, which then resolves the condition in front of the vehicle, generates proper maneuvering command signals, and sends those signals to the respective manipulating devices.

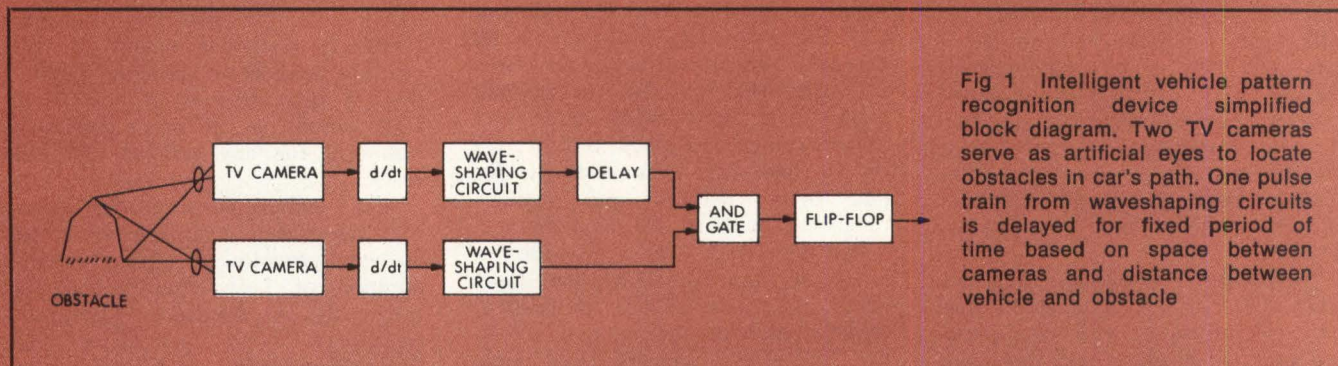
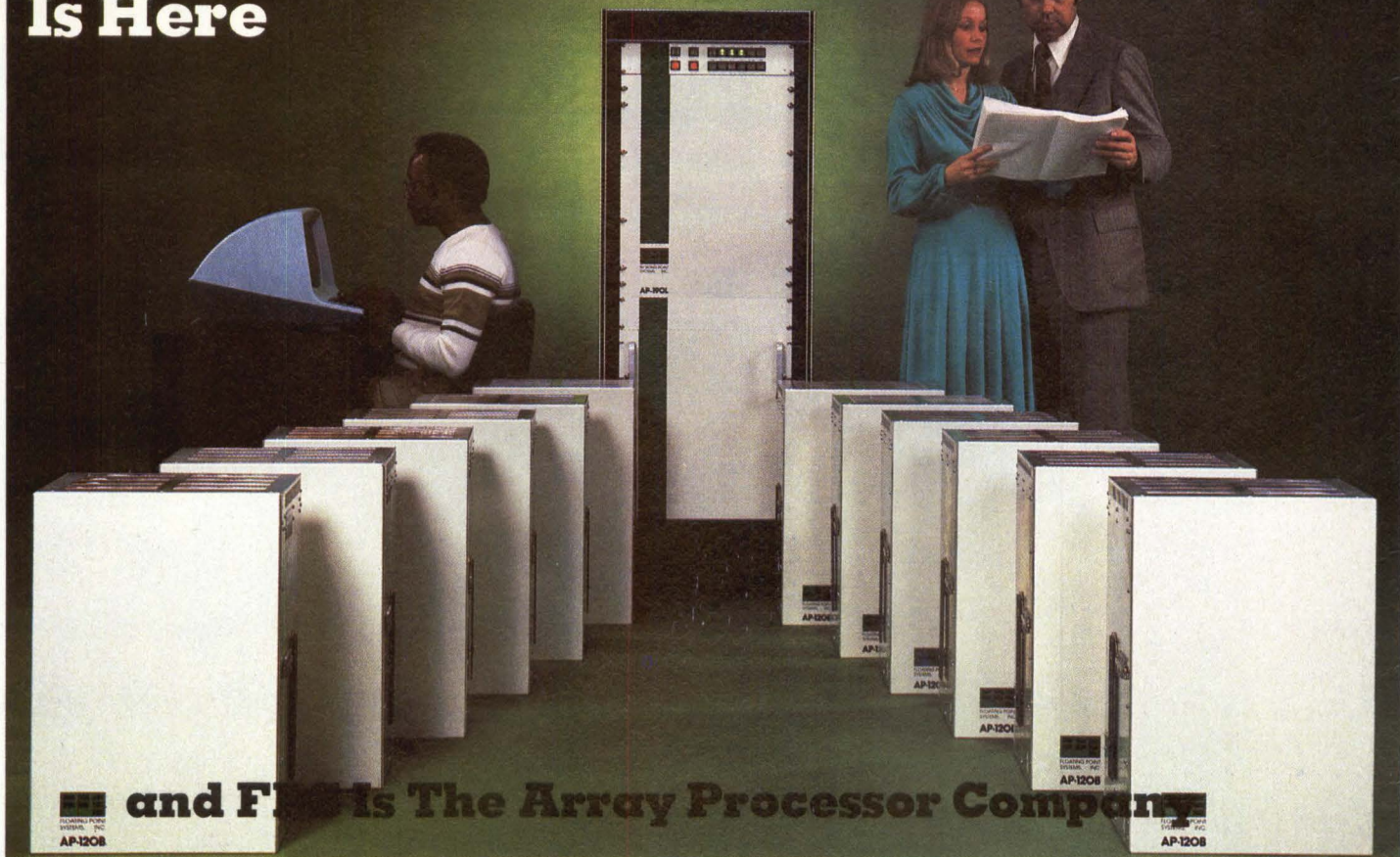


Fig 1 Intelligent vehicle pattern recognition device simplified block diagram. Two TV cameras serve as artificial eyes to locate obstacles in car's path. One pulse train from waveshaping circuits is delayed for fixed period of time based on space between cameras and distance between vehicle and obstacle



# The Age of Array Processing Is Here



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COMPUTER DESIGN 6/78

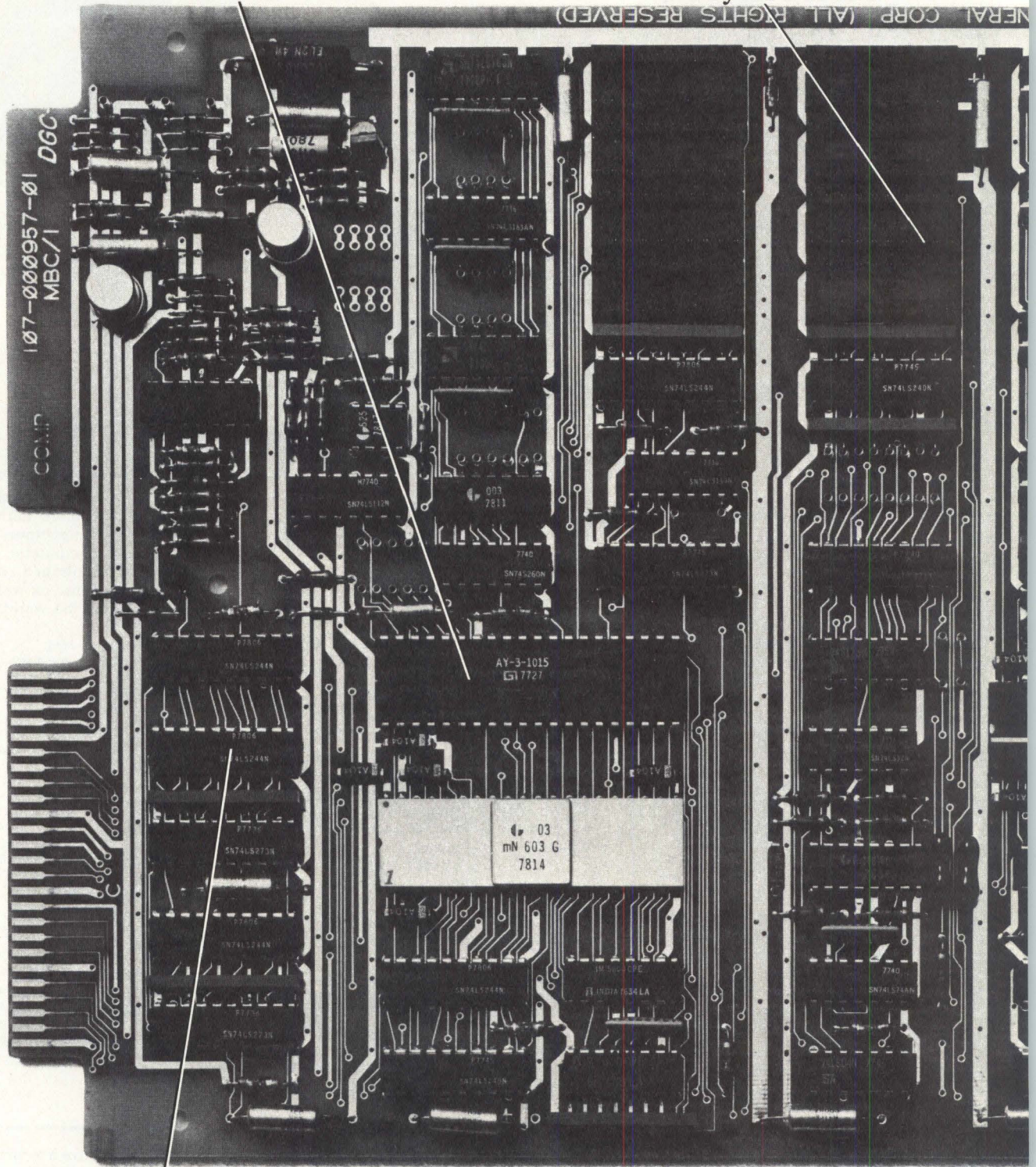
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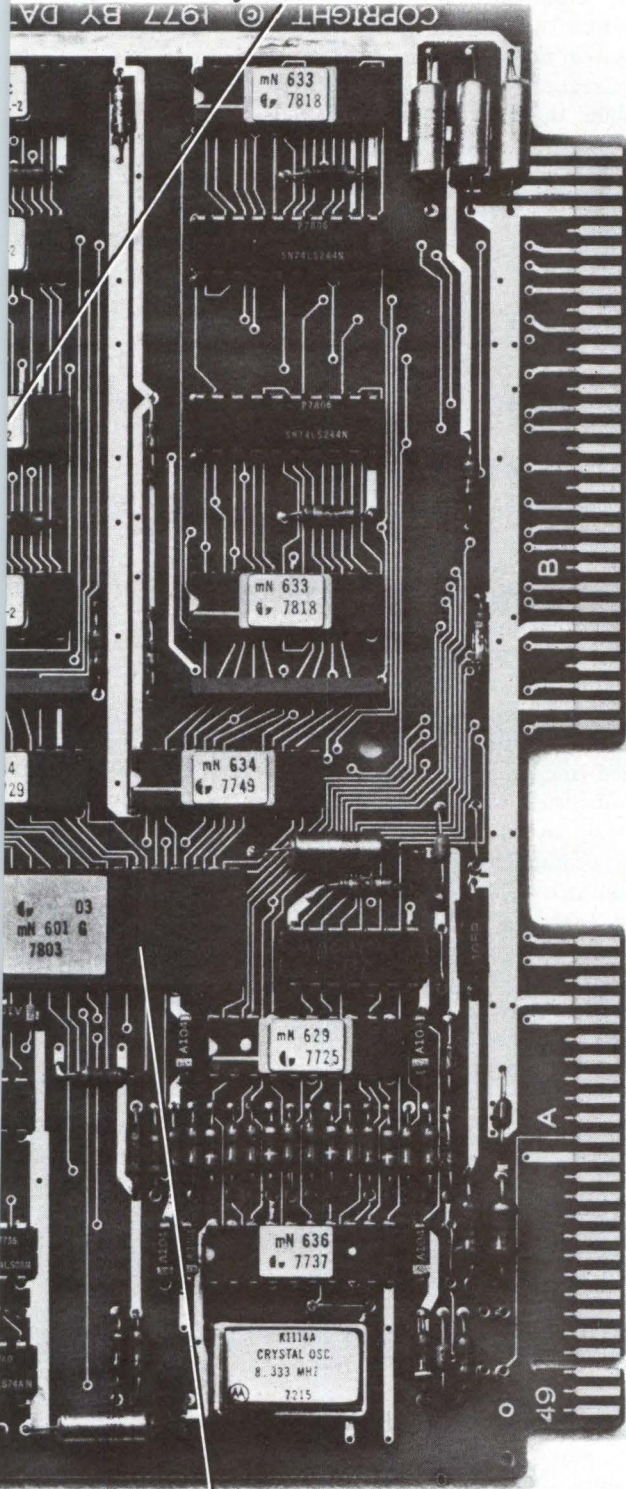
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CD-6

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**Automatic Tester for  
Electronic Engine Control Systems**

Because automobile mechanics may have difficulty following deductive processes in diagnosing malfunctions in the electronic engine control systems incorporated on some 1978 model cars, an automatic tester has been designed as an aid.<sup>3</sup> This diagnostic device leads the mechanic step by step through collection of data and the analysis of results.

An engine control system influences spark plug timing, fuel mixture, recirculation of exhaust gas, and air input to the manifold for operation of catalysts. Several engine condition inputs are measured by the system to determine engine revolutions per minute and load conditions.

Simulation signals for the system under test can be generated by the tester on up to 16 input lines (Fig 3). A 48-channel multiplexer in the system includes

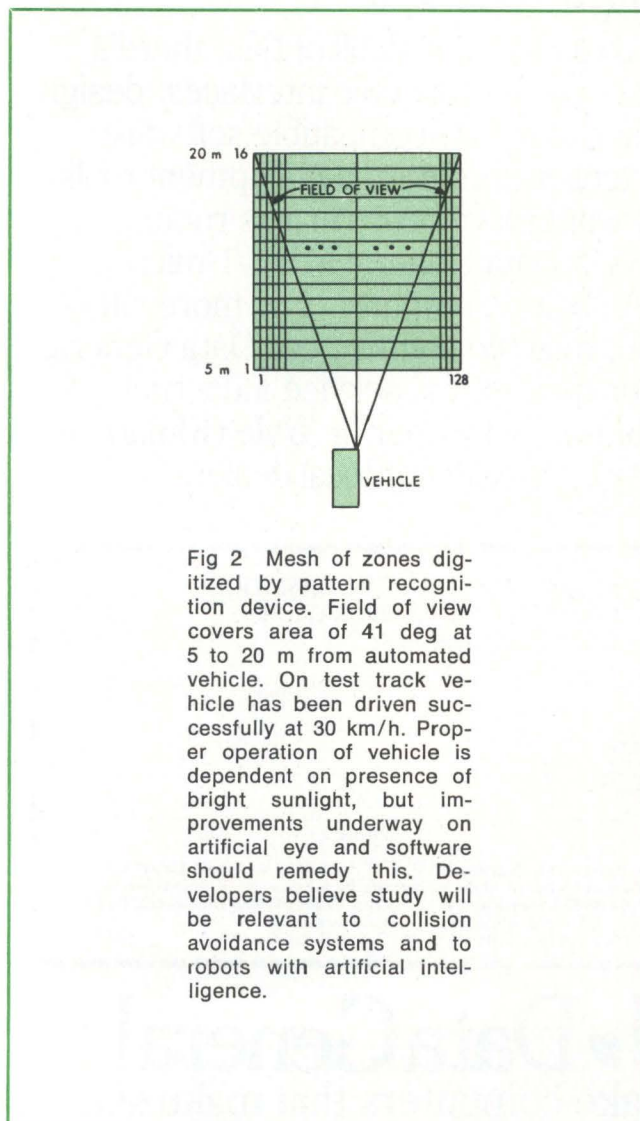


Fig 2 Mesh of zones digitized by pattern recognition device. Field of view covers area of 41 deg at 5 to 20 m from automated vehicle. On test track vehicle has been driven successfully at 30 km/h. Proper operation of vehicle is dependent on presence of bright sunlight, but improvements underway on artificial eye and software should remedy this. Developers believe study will be relevant to collision avoidance systems and to robots with artificial intelligence.

a 10-bit D-A converter in which only the eight high order bits are used. Eight multiplexer channels are utilized internally for self test or measurement; although the other 40 channels are available for external test functions, that number is far in excess of any present system requirements.

CRT messages are condensed into a message dictionary that enables the computer programmer to call out a message either by the address of a complete message or the address of words from the dictionary. This reduces the amount of material which the computer has to generate for each message, but requires storage of an indexed dictionary.

A Z80 microprocessor was chosen for the test system. The CRT screen display is loaded into a 256-character static RAM by the computer in one pass, and contents of the RAM are then read in synchronism with the display by special display control circuitry.

**Energy Demand Limit Control**

By contract, large power users are charged at a per kilowatt-hour rate based on the highest demand recorded during a given interval that can range from a month to a year. Therefore, such users attempt to regulate power consumption rate to within predetermined limits for any period.

A number of demand limit control systems have been designed,<sup>4</sup> but performance characteristics make most of them useful only for specific applications. The specialized requirements inherent to foundries having electric furnaces whose power levels can be adjusted continuously or in small steps resulted in development of a microcomputer-based device. A 1-chip Intel 8748 microcomputer continuously calculates margin between predicted energy usage accumulated at the end of the demand interval and the demand limit set by the contract with the utility.<sup>5</sup> Based on these predictions, the controller provides power limit commands for up to four electric furnaces.

Memory on the microcomputer chip consists of only 1k bytes of EPROM and 64 bytes of RAM but that is adequate for this application. An 8243 port expander accommodates excess I/O channels.

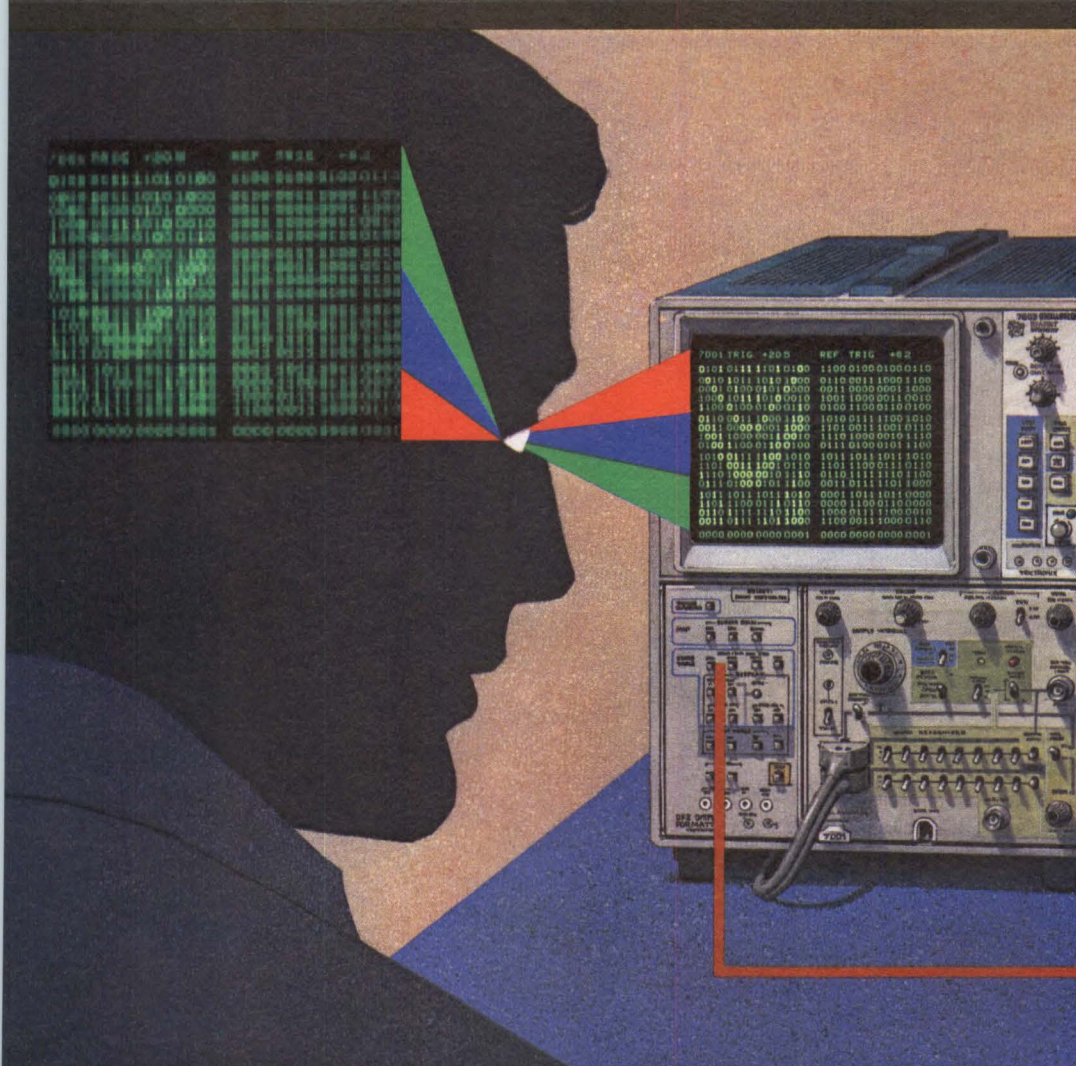
As indicated in Fig 4, closures of count and sync contacts within the demand meter cause current flow in optoisolators to set respective flip-flops that interrupt the main program sequence and identify the closure during the interrupt polling routine. The principal output appears on an 8-bit bus. Six bits are bused directly to output interface modules; two remaining bits are decoded to four priority selection lines that are also bused to the modules.

Power level data for the selected priority are clocked into the 6-bit latch by the priority line pulse. This sets up a corresponding pattern of relay contact closures that establishes a specific value of resistance in series with the power level control potentiometer at the furnace control console. As the 6-bit power level data increases, it establishes a corresponding



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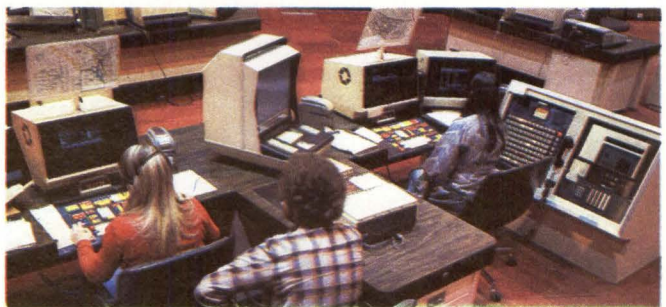
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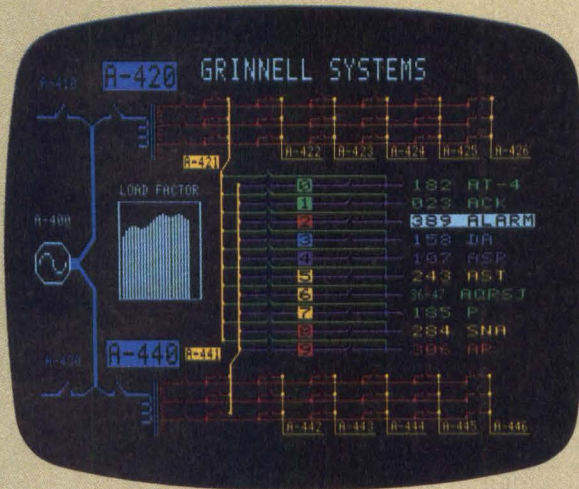
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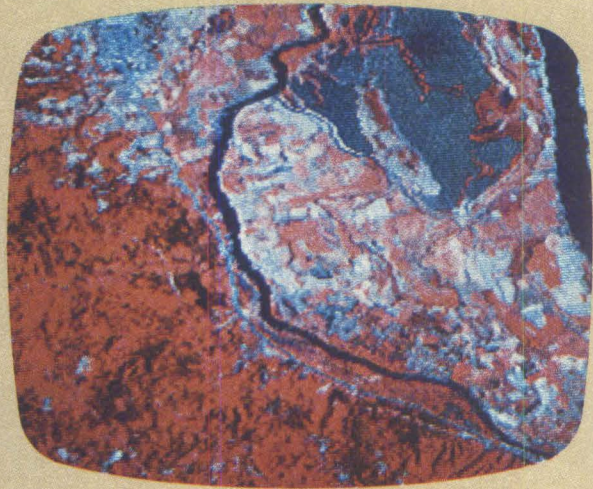


# Introducing GMR-37

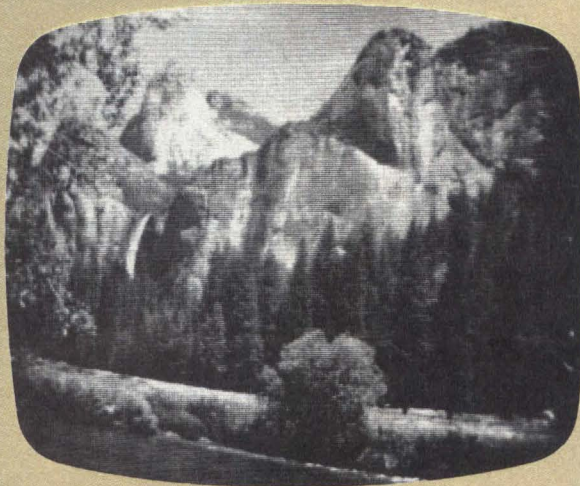
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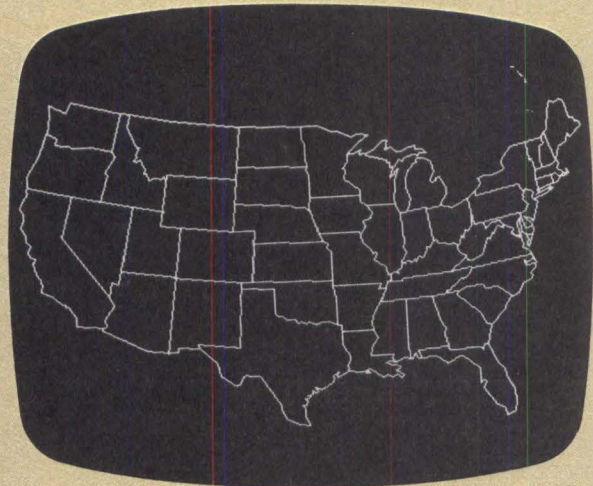
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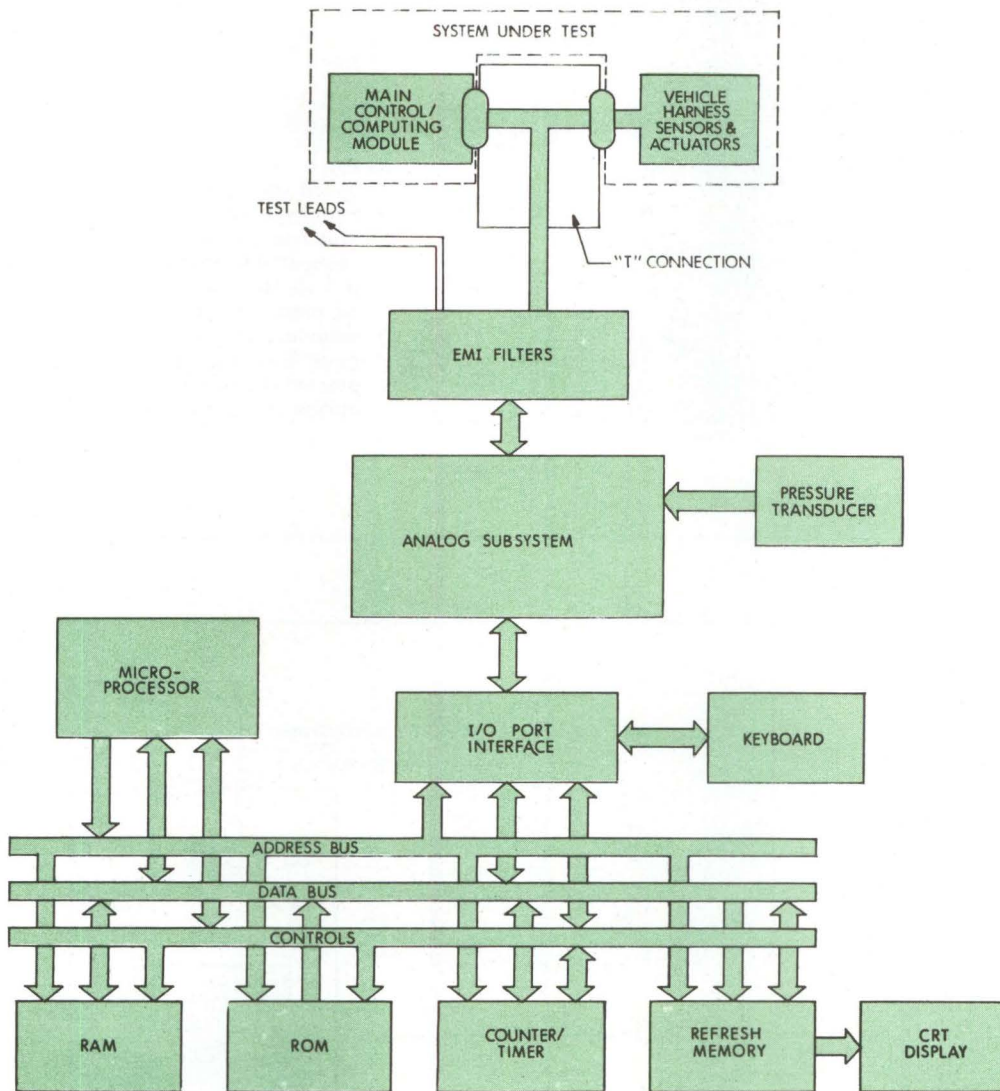


Fig 3 Block diagram of test system for electronic automotive engine control system. Automatic test system leads mechanic through all procedures in specified sequence by instructions and comments displayed on CRT in up to eight lines of ASCII characters. Mechanic's responses input through 20-char keyboard are repeated on display

current value to the potentiometer. The control furnace power therefore is a function of the data output issued by the microcomputer.

Count signals are accumulated and compared at frequent intervals to an advancing limit which progresses linearly from an adjustable preset value at the beginning of the interval to an adjustable limiting value at the end. At each instant, the rate at which the count approaches the limit is calculated in addition to the

difference between them, and these values are used to compute the allowable power level for each furnace.

#### Control of Wind Turbine Generator

A prototype wind turbine generator located at the NASA station in Sandusky, Ohio<sup>6</sup> operates unattended under control of a microprocessor-based system (Fig 5). Its 120-ft (36.6-m) diameter blades turn at 40 r/min



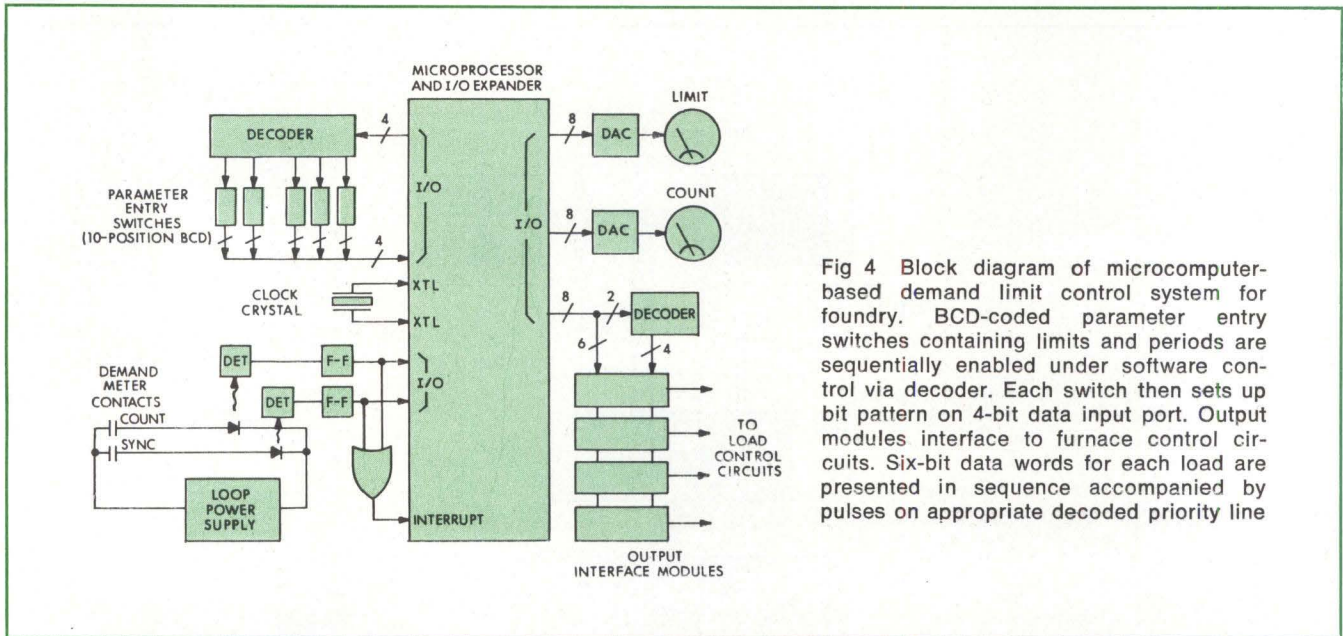


Fig 4 Block diagram of microcomputer-based demand limit control system for foundry. BCD-coded parameter entry switches containing limits and periods are sequentially enabled under software control via decoder. Each switch then sets up bit pattern on 4-bit data input port. Output modules interface to furnace control circuits. Six-bit data words for each load are presented in sequence accompanied by pulses on appropriate decoded priority line

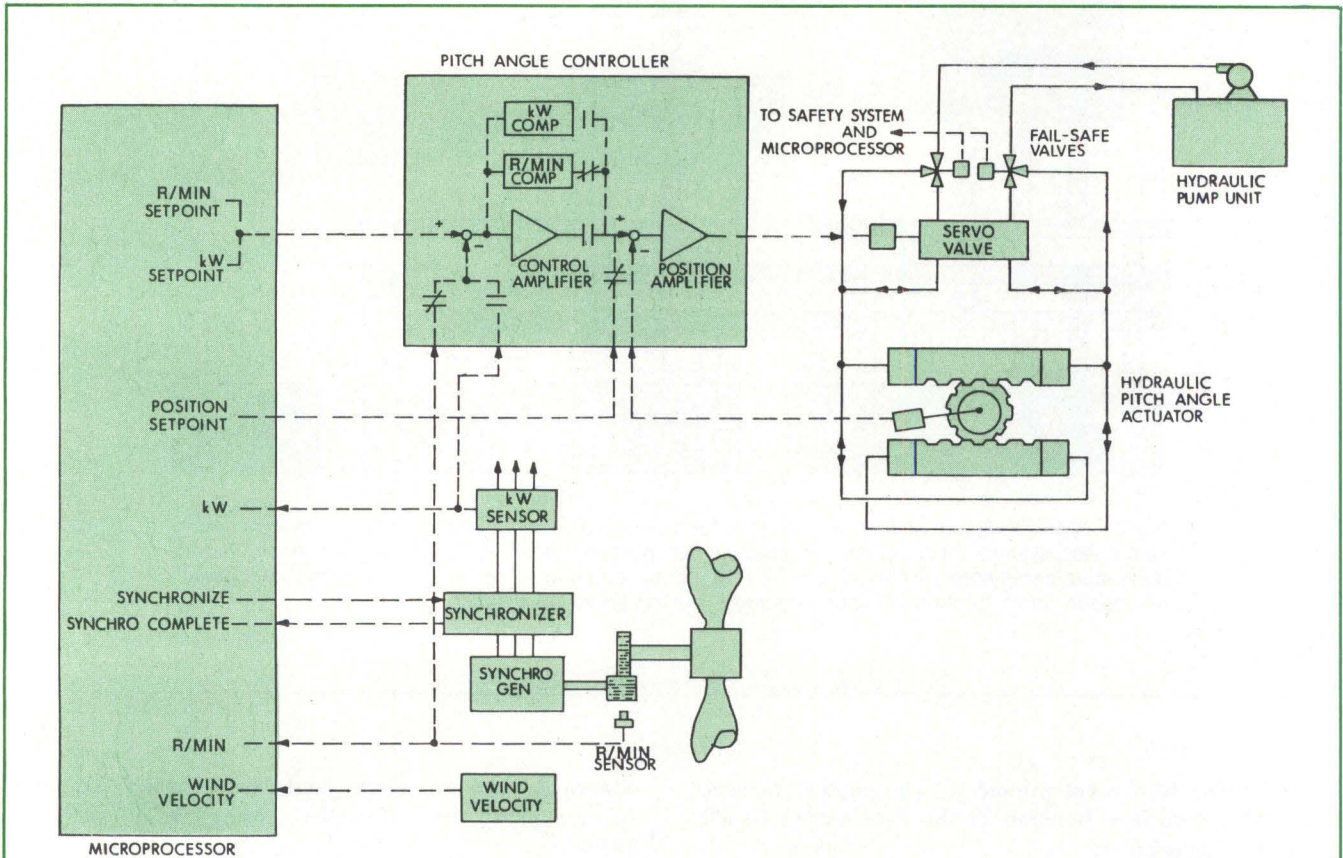
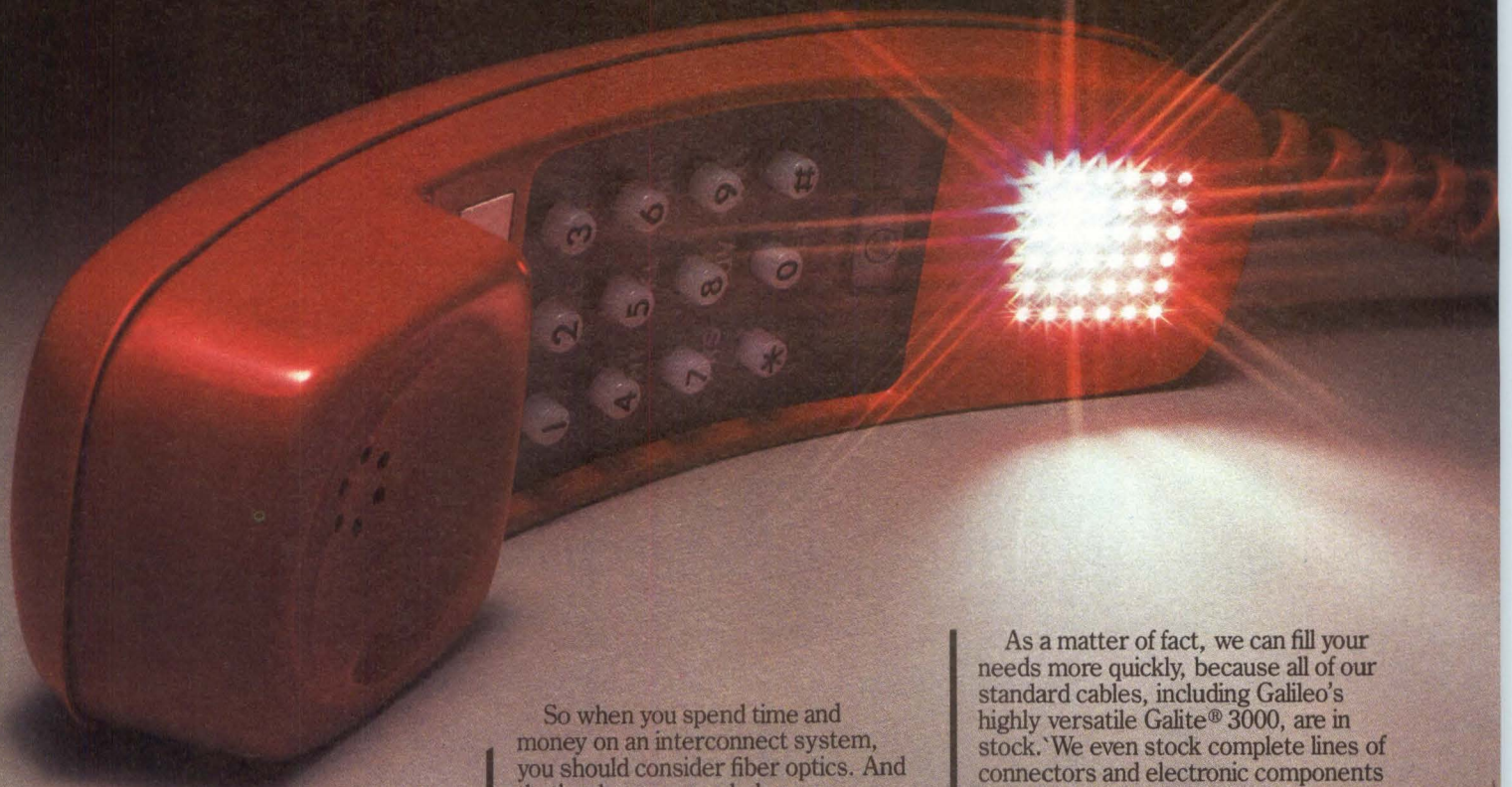


Fig 5 Block diagram of control system for NASA-designed 110-kW wind turbine generator. Microprocessor selects one of three closed loop modes of operation. Signals from sensors are compared to setpoints for blade rotation speed (r/min), kilowatt (kW) output, and blade position. 45:1 gear train increases rotor speed to match 1800-r/min speed of synchronous generator



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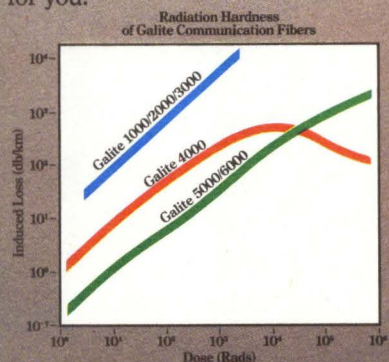
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You will find we offer more than fiber optics. We also offer know-how.



# Intel announces 32K and 64K for EPROM and micro



**Check Pin 18 on our new 2332. It's the key to compatibility with high performance microcomputers and EPROMs.**

Now's the time to get samples or place your order for the 2332 or 2364. They're our new 32K and 64K ROMs that will change the way you design your system. Here's how.

Microcomputer system components—EPROMs, ROMs and microprocessors—need to be designed as an integral unit, not piecemeal. That's the only way to provide maximum design flexibility and ensure a longer life cycle for your system. We've looked ahead at your future design requirements to provide you with components today that will enable you to take advantage of tomorrow's advances. The result is a family of compatible 5V EPROMs and ROMs for microcomputer systems.

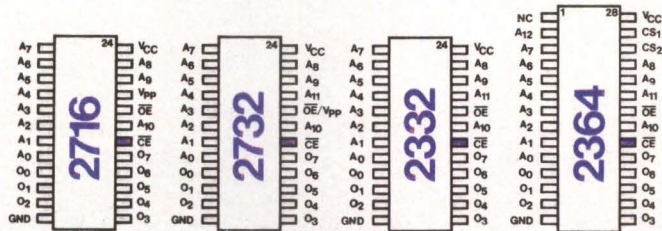
Intel's new 2332 and 2364 are the latest members of that family. They provide system compatibility in three important ways.

First, these new ROMs have a guaranteed access time of 300 ns—fast enough to take full advantage of new, advanced microprocessors. To achieve 300 ns speed with low power dissipation, our parts are Edge-Enabled. That's where Pin 18 comes in. It provides the Chip Enable function necessary for the internal clock circuitry.



# 64K ROMs designed computer compatibility.

Second, the 2332 and 2364 are compatible with our 2716 industry-standard 16K EPROM and will be compatible with our 32K EPROM when it is introduced. Again, Pin 18 is the key. Note that Pin 18 performs the same power control function on all devices. So you can prototype with EPROMs and go directly to high density ROMs for production.



	16K EPROM	32K ROM/EPROM	64K ROM
Organization	2K x 8	4K x 8	8K x 8
Active Icc (max)	100 mA	40 mA	40 mA
Standby Icc (max)	25 mA	15 mA	15 mA
Access Time (max)	350-450 ns	300 ns	300 ns

Engineering the 2332 and 2364 for microcomputer system compatibility led us to the third important advance—the end of bus contention problems. In new multiplexed microprocessor systems, such as the MCS-85 and MCS-86, the Output Enable (Pin 20) needs to be independent of the Chip Enable (Pin 18) which is the power control and selection function. So the 2332 and 2364 have an Output Enable ( $\overline{OE}$ ) for independent control of the data bus, with no possibility of multiple device selection. And input latches on all Edge-Enabled devices allow direct interface with new multiplexed microprocessors.

Low power is essential to meet today's design requirements. We've achieved low power in our 32K and 64K ROMs that can't be matched by fully static parts. Active current of the 2332 and 2364 is 40 mA (maximum). And Intel's Edge-Enabled devices have the added benefit of using Pin 18 for the power control function. So standby current is automatically reduced to 15 mA (maximum).

To get complete details on this important and complex subject, send for our 2332/2364 applications note AP-30, "Applications of Intel's 5V EPROM and

ROM family for microcomputer systems." It provides board layout recommendations, system design applications, timing diagrams, function explanations and discusses PL/M modular software compatibility. Write: Intel Corporation, Literature Dept., 3065 Bowers Avenue, Santa Clara, CA 95051.

Or for samples of these new parts, contact your local Intel representative.



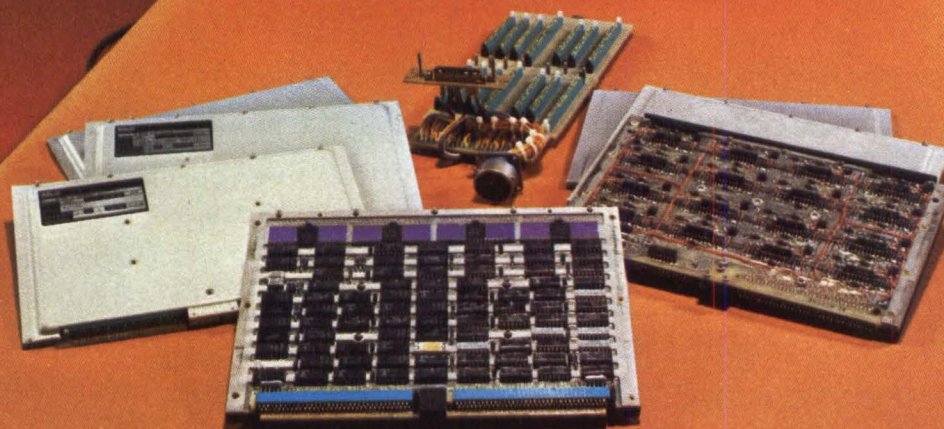
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CIRCLE 46 ON INQUIRY CARD



## DIGITAL CONTROL AND AUTOMATION SYSTEMS

to produce 100 kW of electrical power in an 18-mi (29-km)/h wind.

Controller operation can be in any one of three modes as selected by the microprocessor. In "position" mode, the pitch controller functions as a closed loop position control system driving the pitch angle until it corresponds to the position command setpoint generated in the microprocessor. In "automatic-r/min" mode, the pitch controller acts as a closed loop *speed* control system, adjusting the pitch angle until the rotational speed of the blade corresponds to the speed command setpoint generated in the microprocessor. In "automatic-kW" mode, the pitch controller acts as a closed loop *power* control system that positions the blade pitch angle until the power output of the wind

turbine matches the kilowatt setpoint generated in the microprocessor.

Blade pitch angle is controlled by driving an electrohydraulic servovalve that controls the flow of hydraulic fluid to the pitch angle actuator. A signal from a rotary differential transformer, representing the actual pitch angle, is fed back to the input of the position amplifier where it is compared with the position command signal. The position command signal comes from the microprocessor when the controller is in "position" mode or from the control amplifier when the controller is in either of the "automatic" control modes.

For "automatic-r/min" control, a revolution-per-minute sensor detects the actual rotary speed of the

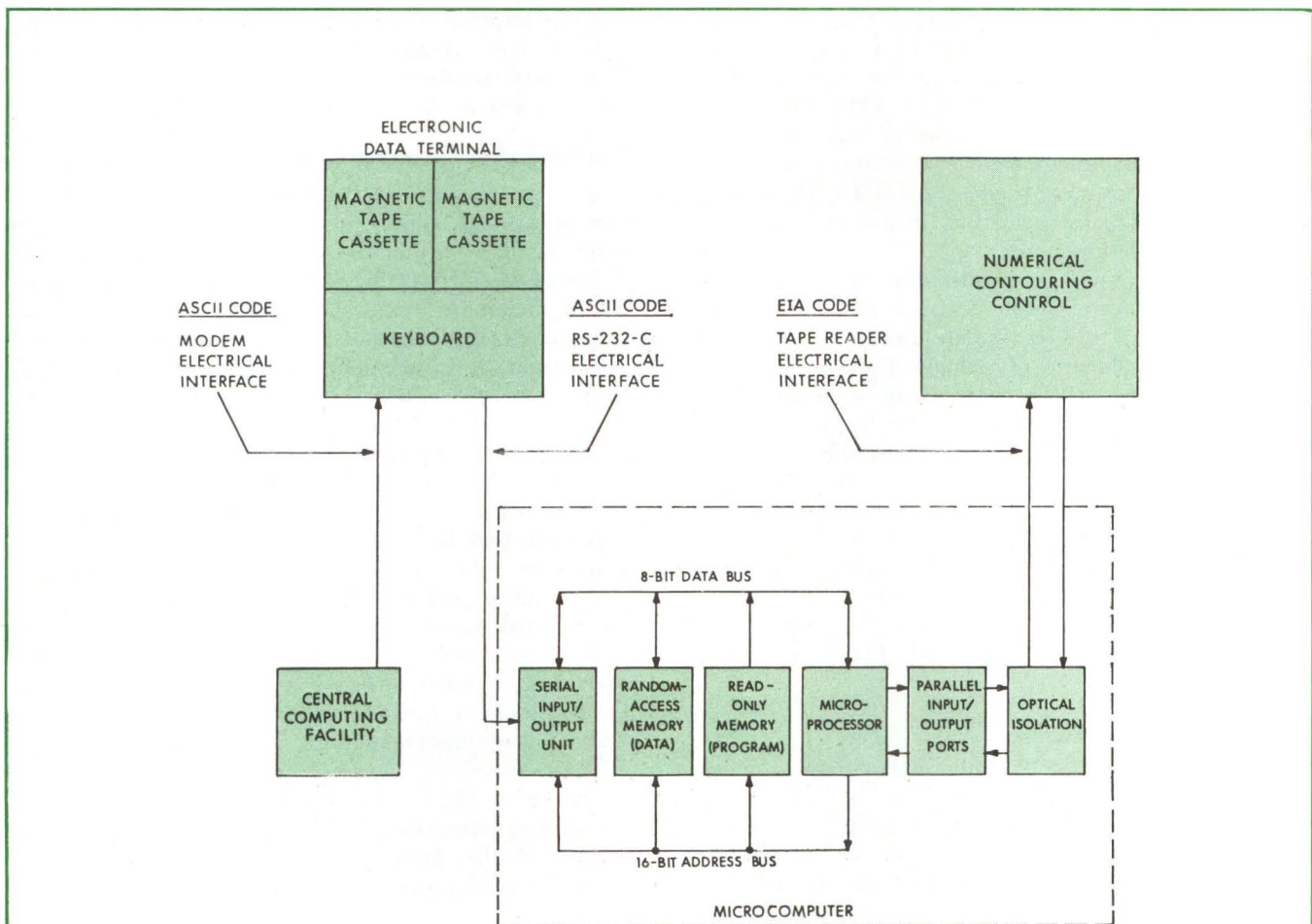


Fig 6 Block diagram of microprocessor-based NC unit for 3-axis milling machine. Original paper tape unit is used for standard runs but dual magnetic tape cassettes input control data for jobs requiring large amounts of data. Because microprocessor has to communicate via existing signal and control lines, system contains high speed optically coupled isolator as interface to numerical contouring control



blades and feeds a signal back to the input of the control amplifier. This feedback signal is compared against the speed command setpoint generated by the microprocessor and an error signal is calculated. The controller amplifier uses the error signal to compute the position command signal that goes to the position amplifier.

For "automatic-kW" control, a power sensor feeds a signal back to the input of the control amplifier where it is summed with the kilowatt setpoint signal from the microprocessor. An error signal is derived and used to compute the position command signal for the closed loop position control system.

### Shipboard Weapons Power Drive Controller

When developers of a solid-state shipboard device for directing various weapons hardware incorporated a microprocessor in the power drive control system,<sup>7</sup> they used a Texas Instruments 990/4 microprocessor development system during feasibility testing. However, that system, based on the 16-bit TMS 9900 microprocessor, was used only because no militarized development system then matched capabilities of the 9900. Later, when the Hughes AN/UYK-30 military microcomputer became available, it was substituted in the engineering design model.

The need to minimize quantization noise in analog power drives governed the decision to use a 16-bit processor, and a 128-Hz sample rate was chosen to minimize the influence of sample harmonics in the analog hardware—in effect providing a "continuous" signal to the power drive analog hardware.

Analog inputs to the microcomputer are channeled through an analog multiplexer to a 12-bit converter, and digital inputs derived from s-D converters are channeled through a digital multiplexer. Analog inputs are angle error voltages and velocity commands. Digital inputs are mode request bits from various switches, outputs of the 16-bit s-D converter, 14-bit target designation commands, and 14-bit handwheel input commands.

### Numerical Control Data Input Unit

At the Los Alamos Scientific Laboratory Shops, a microprocessor system has been added to numerical contouring control of a 3-axis milling machine as an enhancement to the original paper tape input device. Existing jobs will continue to be run from paper tape but new jobs that require large amounts of input data will receive NC instructions from dual tape cassettes. No modifications to the controller were necessary.<sup>8</sup>

System CPU is an Intel 8080A microprocessor, backed up by 256 words of RAM and 1k words of EPROM. The CPU card also contains three output and three input 8-bit ports as well as an 8-level priority interrupt manager (Fig 6). Input data terminal is a Texas Instruments model 733 ASR with dual magnetic tape cassettes, full ASCII keyboard, hardcopy printer remote

device control, automatic search control, and modem for telephone line interface.

RAM is provided by two Signetics 2606-1 type 1k-bit (256-word x 4-bit) static MOS devices, while EPROM is provided by four Intel 1702A type 2k-bit (256-word x 8-bit) UV erasable devices. An additional 1.8k words of EPROM are provided for the operational program. I/O ports are made up of six Intel 8212 type 8-bit LSI devices, and 8-level interrupt capability is provided by an Intel 8214 priority interrupt control unit. Incoming cassette data are stored on a 16k-word RAM card made up of Intel 2107 type (4k-word x 1-bit) dynamic devices.

Program software was written in the procedure-oriented Intel PL/M high level language. Approximately 400 lines of PL/M source language needed for system requirements produced 2800 lines of assembly language instruction words.

The software program organizes the 16k words of RAM as a circular buffer. Two pointers control the end and the beginning of data entered into the circular buffer. When the circular buffer is nearly full, the cassette terminal is turned off. A check of the circular buffer space availability is made continually and the cassette terminal is turned on again after the milling machine has commanded data from the microprocessor. This check produces a value for a variable that provides hysteresis for control of the data cassettes.

### Electric Railway Car Onboard Supervisory Control

Trains on two lines of the Japanese National Railways run at average speeds of 99 mi (160 km)/h. Each train is made up of 16 electric railcars for a total length of 438 yd (400 m). Yet an automatic train control system maintains train speed within set speed limits, keeps a specified distance between any two trains, and slows trains from maximum speed—up to 130 mi (210 km)/h—to under 19 mi (30 km)/h before stopping at a station.

Therefore, information concerning conditions onboard each car is an absolute requirement in order to prevent troubles with onboard apparatus, detect any apparatus that is malfunctioning, and make emergency repairs or take corrective actions quickly. Such data are compiled and supplied to the control system by an onboard supervisory control system. Originally this system was based on a minicomputer controller. However, a microprocessor-based system has been developed to maintain all functions except automatic inspection and automatic train operation.<sup>9</sup>

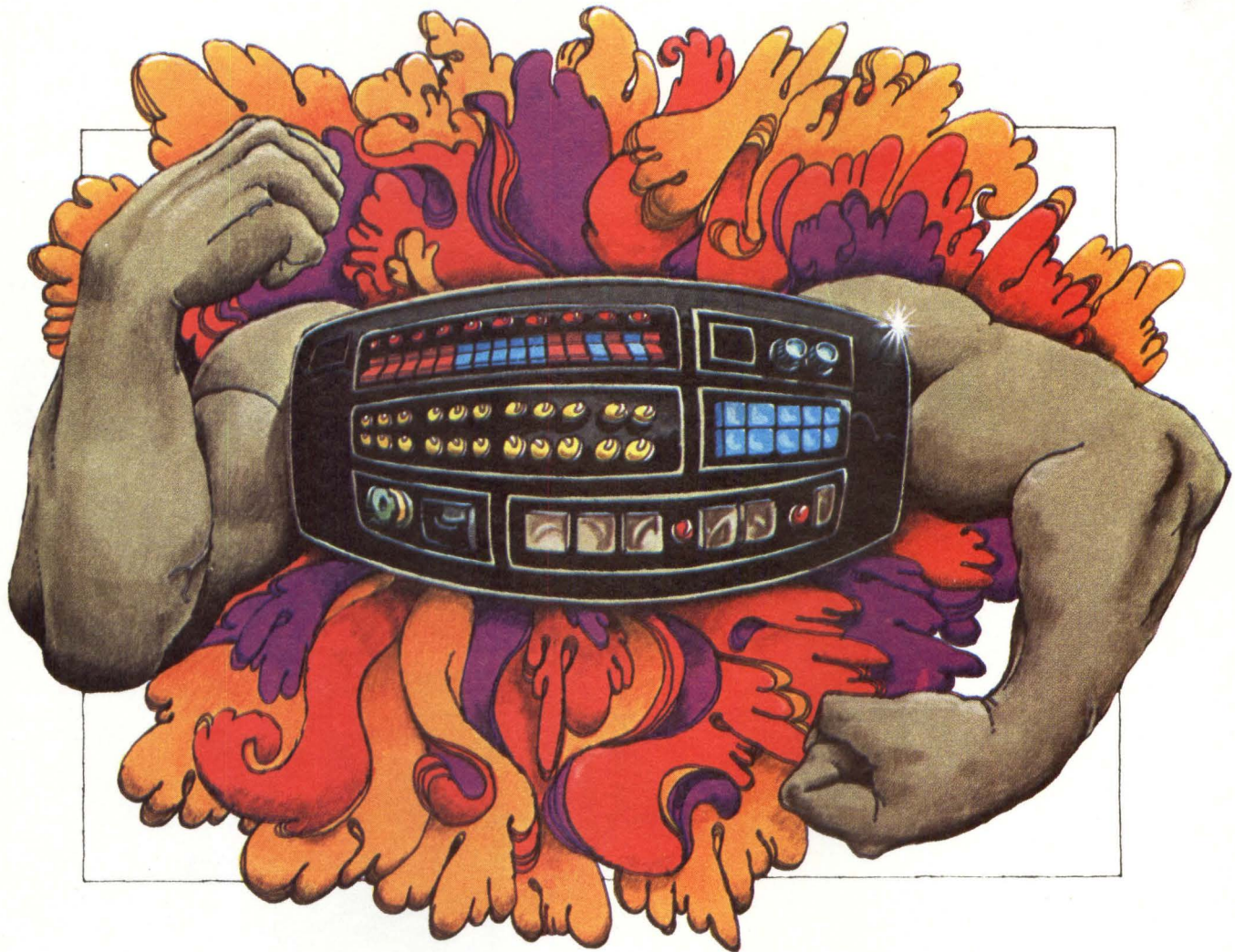
Two supervisory systems, each configured basically as shown in Fig 7, are installed in every railcar—one for routine operation, the other for backup in case of failure of the first. A 12-bit, single-chip microprogrammed microprocessor handles eight levels of interrupt.

A 1k-word RAM stores data and temporary values used in calculations and provides a work area for multiple processing of application programs by the operating system. Programs and constants are stored in a 5.5k-word p/ROM (3.2k are presently unused but are available for system expansion.)

Software for the supervising system is divided into operating system and application programs. In order to monitor and control application programs that



# Our I/O muscle-builder for plant minicomputers.



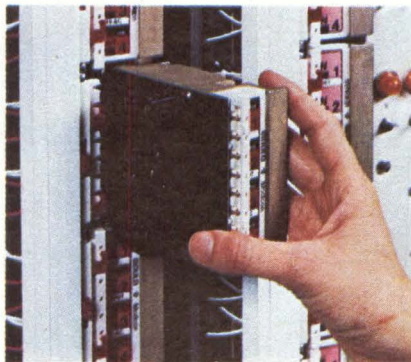
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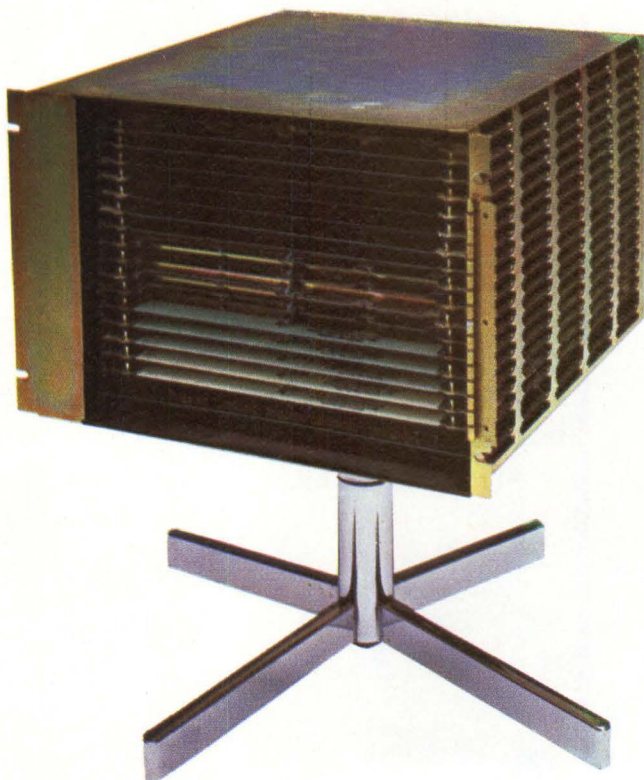
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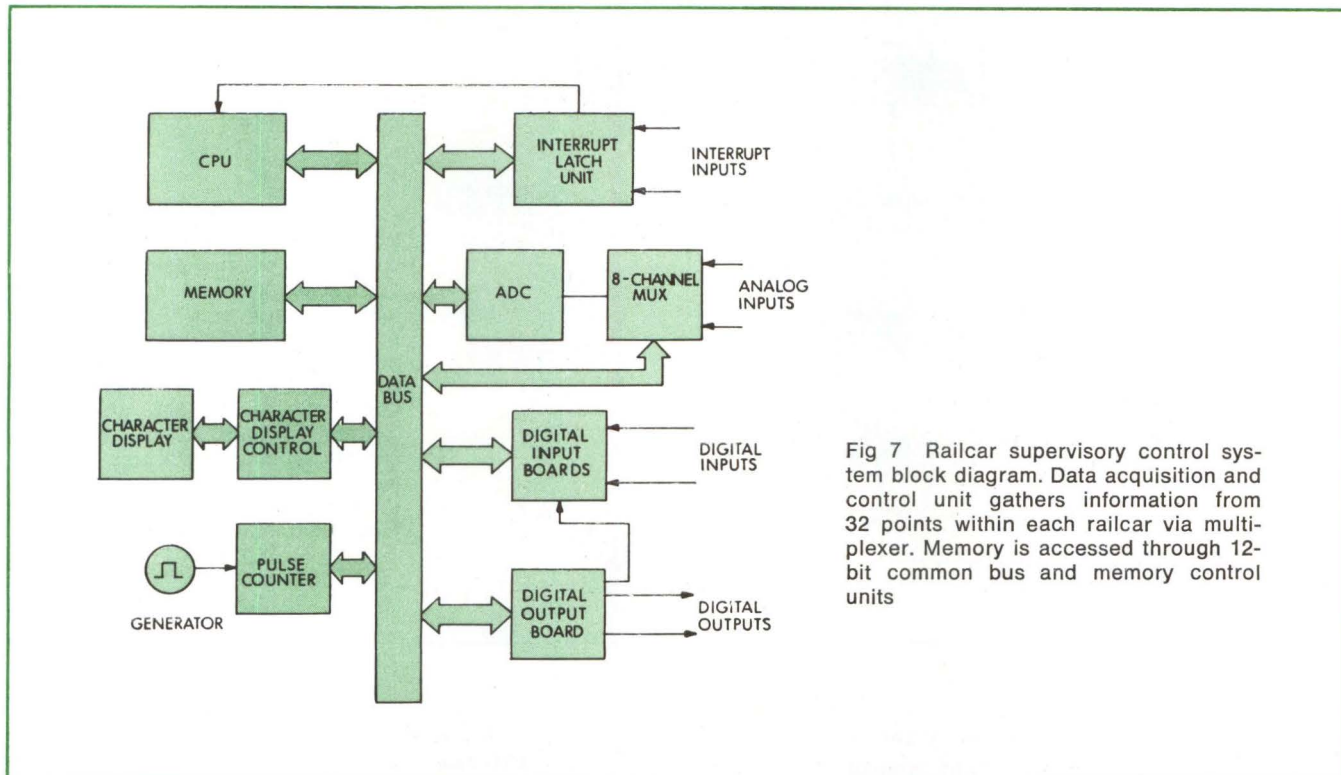


Fig 7 Railcar supervisory control system block diagram. Data acquisition and control unit gathers information from 32 points within each railcar via multiplexer. Memory is accessed through 12-bit common bus and memory control units

realize various functions, an operating system was developed that was similar to the one used in the mini-computer. This system is capable of multiple processing of 20 application tasks on the basis of the task priority. It can handle eight levels of interrupt signals at the most and can analyze 12 interrupt inputs introduced in the microprocessor through an interrupt input board. In addition, it controls and selects the overlaid memory chips for memory extension. About 210 words of RAM and 400 words of p/ROM are used for the operating system.

### Chlorine Plant Supervisory System

An 8080A microprocessor with 12k of p/ROM and 17k of RAM are key elements of a microcomputer-based supervisory system (Fig 8) for a memory-anode chlorine plant.<sup>10</sup> The system monitors 52 (expandable to 60) chlorine cells and stores data for each of 16 buses of every cell.

Data consist of both current and voltage values which are provided by a cell scanner that monitors the bus currents and voltages and performs an A-D conversion upon request. Storage is provided for present, 24-h, and month-to-date data. Data are retrieved from the computer memory using selected keyboard commands.

In normal mode of operation, the computer begins a cell scan by sending the address of cell 1, bus 1 to the cell scanner. When data are ready, the status signal from the scanner is used to interrupt the

computer and the data are input into memory. Alarm conditions for both the voltage and current are tested and logged if an alarm condition exists. The operator is notified of an alarm condition via a CRT and a serial printer.

Alarms in the system are generated from both cell scanner and computer. Those generated by cell scanner are tested as a result of an interrupt produced every 2 s by a hardware clock. Alarms are of three types: primary and secondary bus current, and low voltage.

### Control of Microwave Oven

Availability of inexpensive single-chip microcomputers has made microprocessor control practical for home appliance applications. One is for a microwave oven that combines a microcomputer with a high voltage reed relay to form a power control system.<sup>11</sup>

Principal factors that must be controlled are variable power, defrost, temperature, and memory cooking as well as clock functions. Use of a microcomputer with the high voltage relay reduced component count and simplified operation. Plans for a future oven control system include adapting a sensor device with greater capability and a different microcomputer that contains an A-D converter and more interface circuits.

### Filmstrip Projector Control

A very inexpensive one-chip microcomputer containing 640 words (8-bit) of ROM, 48 words (4-bit) of RAM, and 22 I/O ports, has been included in the design



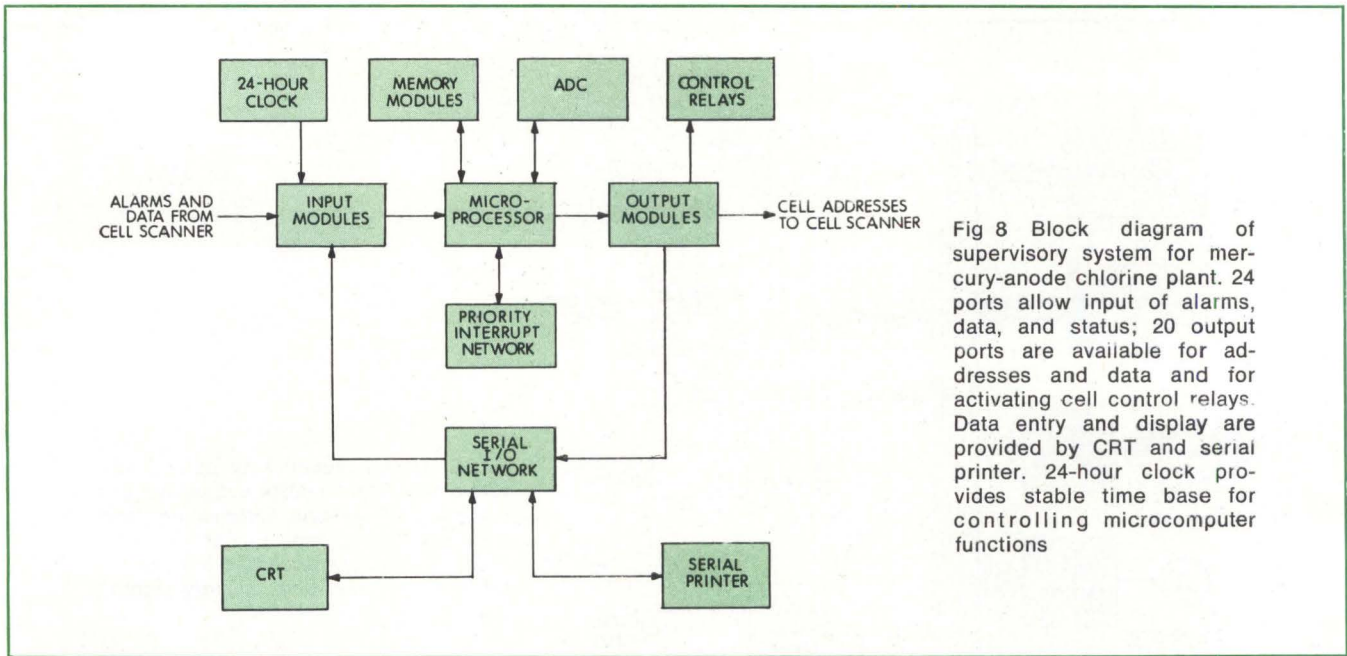


Fig 8 Block diagram of supervisory system for mercury-anode chlorine plant. 24 ports allow input of alarms, data, and status; 20 output ports are available for addresses and data and for activating cell control relays. Data entry and display are provided by CRT and serial printer. 24-hour clock provides stable time base for controlling microcomputer functions

of a controller for a filmstrip projector with synchronized audio accompaniment.<sup>12</sup> The system includes a built-in audio cassette player for narratives that relate to the filmstrip. The tape normally runs continuously and inaudible cuing tones recorded on the tape track enable synchronization by causing the film to advance frame by frame.

A Rockwell PPS-4/1 microcomputer used as control element has neither interrupt capability nor other direct means of keeping track of time. In addition there is no means for precise frequency control of the processor's clock. Therefore, the program is written as a large loop which considers in turn each input that requires action to be taken and checks internal software timers that control output signal times. Because period of the most rapidly occurring input signal is 6 ms, the main loop was carefully adjusted so that its maximum execution time was less.

All available ROM, most of the RAM, and all I/O ports of the microcomputer were utilized for the program. The program was assembled on an IBM 370/168 computer using Rockwell's cross assembler written in FORTRAN IV. Monitor and prototyping facilities of the Rockwell PPS-4 Assembler were used for program debugging.

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3. E. R. Pelta and K. S. Gold, "A Microprocessor Control Automatic Test & Diagnostic System for Use on Electronic Automotive Engine Control Systems," pp 106-112

4. *Computer Design*, May 1978, pp 50-56
5. R. F. Herrman, "A Microprocessor-Based Demand Limit Control," pp 50-54
6. A. J. Gnecco and G. T. Whitehead, "Microprocessor Control of a Wind Turbine Generator," pp 143-149
7. D. L. Chenoweth *et al*, "Development of a Power Drive Controller Using the TMS 9900 Microprocessor and the AN/UYK-30 Military Microcomputer," pp 168-173
8. C. D. Ethridge and W. M. Seifert, "Microprocessor Data-Input-Control Unit for Mark Century Numerical Contouring Control," pp 77-82
9. S. Yasukawa *et al*, "Microprocessor-Based Supervising System of High-Speed Electric Railcars," pp 227-232
10. J. L. Hilburn *et al*, "A Microcomputer-Based Supervisory System for a Mercury-Anode Chlorine Plant," pp 46-49
11. T. Yashioka *et al*, "A Microprocessor Control for Microwave Oven," pp 159-163
12. J. D. Garland and J. V. Landau, "A Microcomputer-Controlled Filmstrip Projector," pp 164-167

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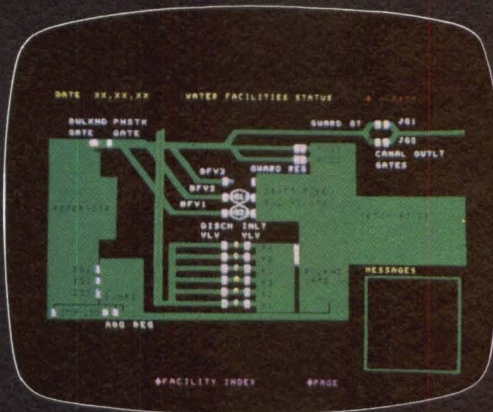
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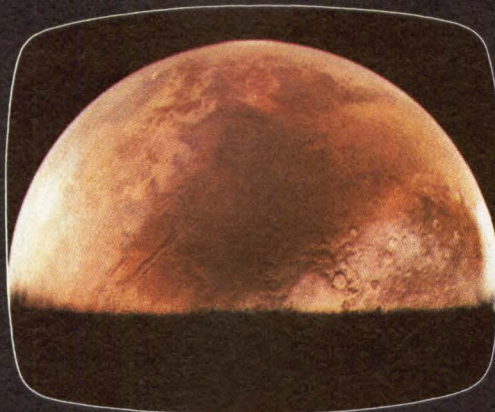


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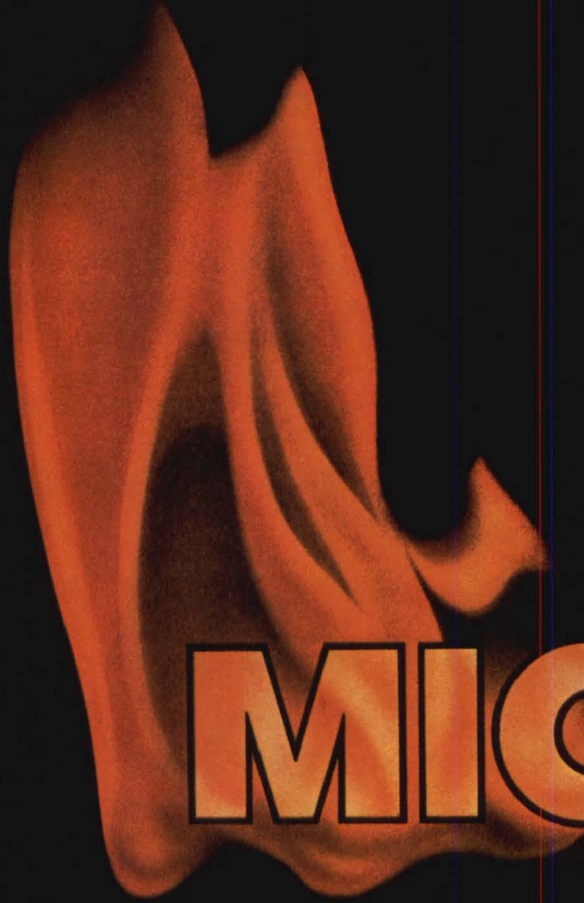
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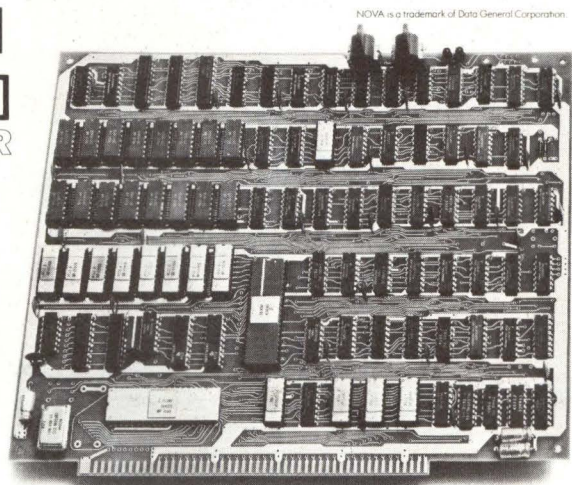
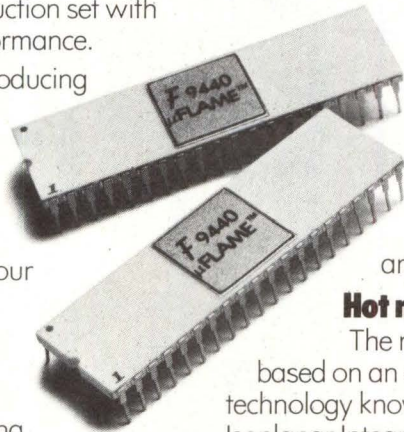
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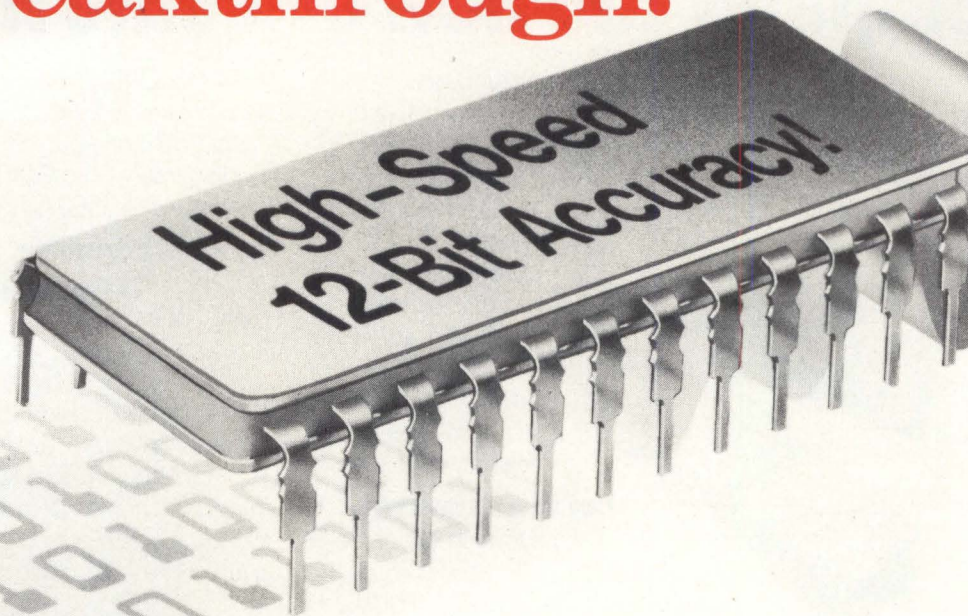
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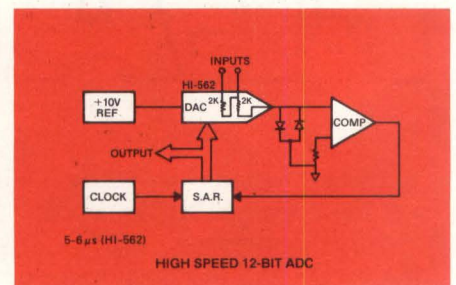
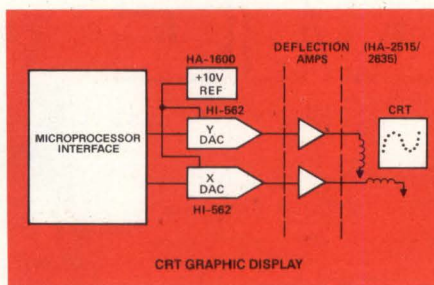
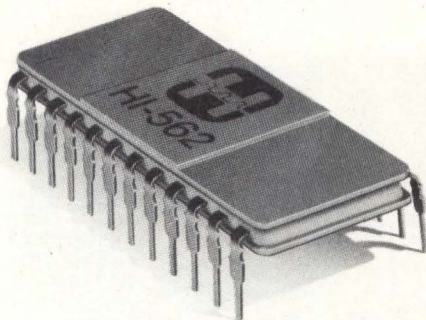
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# MICROPROGRAMMED CPU ARCHITECTURE OFFERS USER-ALTERABLE MINICOMPUTER PERFORMANCE

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Microprogramming is designed directly into central processor organization, while preserving existing support hardware and software, resulting in a versatile minicomputer that offers increased performance capabilities of extremely fast computation, self-testing, remote program loading, customized I/O interfacing, and very high data transfer rates

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**Philip Gordon and Scott Stallard**      Hewlett-Packard Company, Cupertino, California

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**M**ost minicomputers are developed in a family concept, sharing instruction set definitions, principles of operation, and/or logical structures. Traditionally this compatibility-retaining foundation has been extended through designs which either encompassed a broader range of applications or replaced outdated, less competitive models, usually at lower cost and greater performance.

Initially designed with relatively simple instruction sets and hardwired control logic, minicomputers later appeared with microprogrammed control sections that not only supported more complex instructions in firmware, but also minimized cost as read-only memory (ROM) technology became less expensive than hardwired logic. Currently minicomputers feature complex instructions for floating-point and decimal arithmetic, fast Fourier transform, and data array operations. Support documentation, training programs, and hardware and software packages enable these minicomputers to be customized to the application through microprogramming—the technique by which programs are writ-

ten for execution on the internal control processor. Although typically reserved to accomplish emulation of the machine instruction set, microprogrammable minicomputers provide this access and allow control over the entire control processor. Analysis of the Hewlett Packard 21MX E-Series minicomputer shows how general microprogramming techniques provide an opportunity to design improved minicomputers while working within a framework of family compatibility.

## **Design Constraints**

The goal in designing the E-Series minicomputer was to improve on the performance of its predecessor without significantly increasing cost. Because the computer was to be based upon the previous architecture, it was constrained as to peripheral interfacing, operating systems, compilers, application programs, and other software. These constraints, coupled with price and performance requirements, dictated that the design be based physically on existing hardware assemblies, such



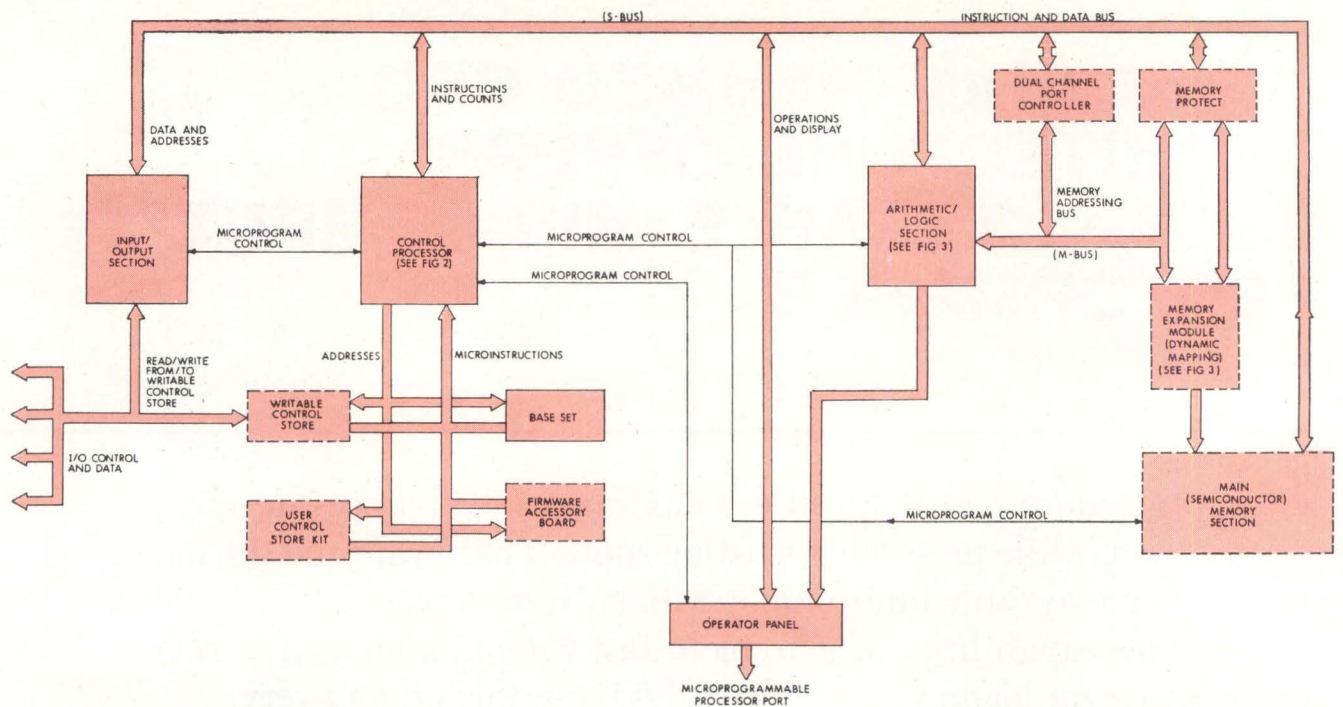


Fig 1 Block diagram of minicomputer processors, including accessories. I/O system communicates across single data bus and address (select code) bus. I/O control signals are generated by microprogrammed control processor or dual-channel port controller (DMA-like). Memory system consists of protection interface, controller, and dynamic mapping system, which provides for maximum physical address space of 2M bytes

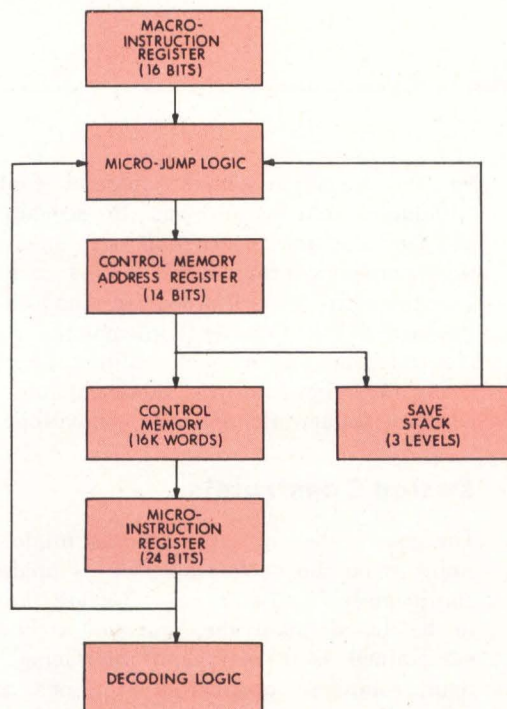


Fig 2 Control processor operation. While microinstruction residing in microinstruction register is being executed, control memory address register is incremented to present new address to control memory to access next microinstruction. At end of microcycle, microinstruction register is clocked with new microinstruction and procedure is repeated. Sequential microinstruction processing is interrupted by micro-jump logic, wherein control memory address register is parallel-loaded with target branch address



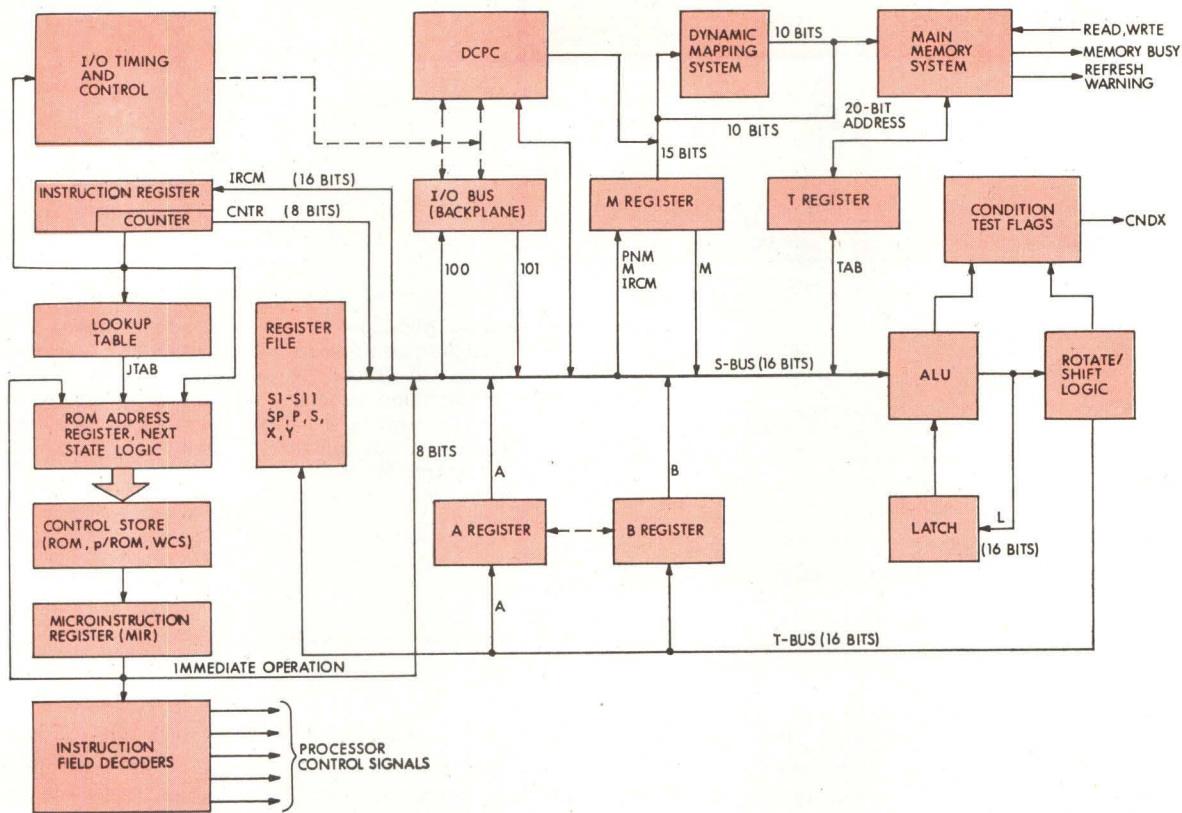


Fig 3 Arithmetic section operation. Minicomputer is based on microprogrammed, bus-oriented control processor. Typical data manipulative microinstruction calls for contents of register to be enabled onto S-bus, while certain arithmetic and/or shift operations are further specified for duration of microcycle. At end of cycle, specified destination register is clocked to load resultant data from its input lines

as memory, system options, power modules, and packaging. Therefore attention focused on one design opportunity—the central processing unit (CPU).

## CPU Architecture

Ten minicomputer variations or revisions made up the existing family. All shared the same basic architecture and kernel instruction set. The architecture evolved around two accumulators, and 70 instructions that operated on 16-bit data. As the family expanded the instruction set grew to include 128 standard instructions, to perform indexed references, and to operate on multiple word floating-point data, but implementation techniques remained similar.

The E-Series CPU is designed as two functional sections: control processor and arithmetic section (Fig 1). The control processor (Fig 2) is the core of the minicomputer and guides it sequentially through various basic processing and decision-making steps required to execute higher order software instructions (referred to as macroinstructions). This control processor executes microinstructions in a time interval called a microcycle.

A microinstruction is a coded word that defines a single data manipulative operation to be carried out by the arithmetic section (Fig 3). Divided into fields

that contain micro-operand primitives (mnemonics that specifically control a small portion of the arithmetic section of the CPU), microinstructions physically reside in a special control memory and are stored in a microinstruction register (MIR), where they are executed. This register provides simultaneous access of the next sequential microinstruction from control memory during execution of the current one. Micro operands (ops) are the basic building blocks for constructing microinstructions, which, in turn, are combined for creating microprograms. Two microprograms (a fetch routine and an execute routine) are required to completely execute a macroinstruction. Depending upon the minicomputer and the macroinstruction under execution, other microprograms, such as an indirect operand routine or an indexing routine, may be required.

A 24-bit wide microinstruction word is used—identical to that of earlier microprogrammable minicomputers. Length, format, and structure of the microinstruction qualify the control processor design as a “diagonal” structure, rather than a purely horizontal structure or a vertical structure. This compromise design accommodates a high degree of functional parallelism (characteristic of the horizontal structure), while keeping firmware costs low and microprogramming techniques relatively simple (indicative of a vertical structure).



23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPERATION					ALU					S-BUS					STORE					SPECIAL			
READ WRTE					PASS INC ADD AND					A (REG) B (REG) P (REG) X (REG) IOI					A (REG) B (REG) P (REG) X (REG) IOO					R1 L1 STFL SOV			

(a)

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPERATION					COND					S	ADDRESS										SPECIAL		
JMP JSB RTN					OVFL COUT ALZ					RJS	JUMP TARGET										CNDX		

(b)

MNEMONIC	FUNCTION
JMP	JUMP TO SPECIFIED CONTROL MEMORY ADDRESS
JSB	JUMP TO SUBROUTINE AS SPECIFIED BY ADDRESS FIELD
RTN	RETURN FROM SUBROUTINE
R1	LOGICAL RIGHT-SHIFT 1 BIT
L1	LOGICAL LEFT-SHIFT 1 BIT
STFL	SET CPU TEST FLAG
SOV	SET CPU OVERFLOW BIT
RJS	REVERSE JUMP SENSE
OVFL	OVERFLOW BIT BRANCH CONDITION
COUT	ALU CARRY OUT BRANCH CONDITION
ALZ	ALU OUTPUT ALL ZEROS BRANCH CONDITION

Fig 4 Microinstruction field definitions. Two most frequently used microinstructions are fairly typical in format to encoded vertical microprogramming structures, but are wide enough to perform multiple operations simultaneously. Mnemonic assignments listed under various fields are not all-inclusive

Of the provided microinstructions, the two most commonly used are the data manipulative microinstruction and the conditional branch microinstruction. Data manipulative microinstructions are divided into five fields [Fig 4(a)]. The S-bus (system data bus) field specifies one of 32 registers to be enabled onto the S-bus for the duration of the microcycle; the ALU field specifies one of 32 arithmetic or logical operations to be performed on S-bus data; and the store field selects one of 32 target registers to be updated with new data at the end of the microcycle. The operation and special fields specify two of 16 or 32 auxiliary functions, which may or may not be incidental to the data operations. For example, a main memory read or write cycle may be initiated concurrently with data manipulation by appropriate mnemonics in the operation field. In the special field, the data shifter could be programmed to shift the resultant ALU data left or right one bit, set the flag register, or set the overflow register.

The second most frequently used type of microinstruction is the conditional branch, similarly divided into five fields [Fig 4(b)]. Here the operation field specifies the type of branch to occur (such as a jump, jump to subroutine, or return from subroutine). The special field affirms the conditional branch, and the conditional (COND) field selects one of 32 testable CPU conditions. These may include the overflow register, ALU carry out, or the data output of the ALU all zeros. In the S field, the reverse jump sense (RJS) bit may be set to test the opposite condition specified. The address field is the branch target reached if the condition tested is successfully met.

Commands initiated by the control processor section (Fig 3) are actually carried out in the arithmetic section of the CPU. While the macroprogrammer uses only two accumulators and two index registers, a supplement of internal hardware registers is required

to properly carry out macroinstruction execution. The arithmetic section is a straightforward logical structure based upon the macroinstruction set and rules of operation. Nearly all registers, whether directly available to the macroprogrammer or not, can be enabled onto the S-bus. The ALU and shifter operate on this data, subsequently placing resultant data onto the T-bus (transfer bus). Registers are appropriately loaded from either the S-bus or T-bus.

## Fast Executing Macroinstructions

In a microprogrammable minicomputer, macroinstruction execution time is the product of the number of microinstructions in all microprograms required to complete it and the microcycle time, plus any extra penalties, such as waiting for main memory cycles to complete. Decreasing the execution time of a macroinstruction usually requires that either fewer microinstructions be used to complete it, faster microcycles be provided, or faster memories be used. In the present design, all three capabilities were improved.

Although exact microprogram compatibility with existing processors was not required, preservation of the microword's structure and format as well as mnemonics and definitions of most micro ops simplifies the task of transferring existing programs. A tradeoff was encountered between the general-purpose control processor (easy to microprogram) and a complex and powerful (but difficult to understand) set of micro ops that would, if used properly, reduce the overall number of microinstructions required to perform the same task. The design solution offers a general-purpose control processor to the microprogrammer, but retains the capability to rapidly execute the most frequently used standard macroinstructions.



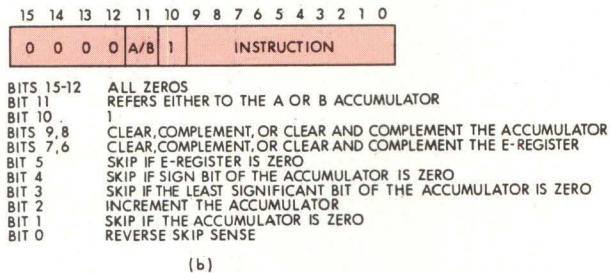
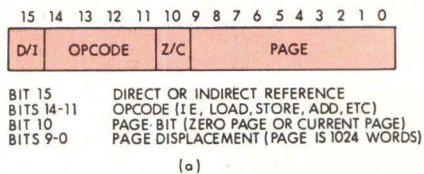


Fig 5 Group instructions. Formats of memory reference group and alter-skip group instructions do not lend themselves to execution by general-purpose emulators

From a frequency analysis of instruction execution, the class of macroinstructions called the memory reference group is encountered approximately two-thirds of the time. Memory reference group instructions share a common format [Fig 5(a)] with a 4-bit opcode and a 10-bit page displacement. Page displacement must be concatenated with either five zero bits or the upper five bits of the internal program counter, depending upon whether the macroinstruction references the base (zero) memory page or the current memory page. In an efficient, but pure, general-purpose microprogrammable CPU, from three to six microinstructions may be required to mask and merge the contents of instruction register and program counter, depending upon the results of a test of the page bit, to create the target operand address. The 1  $\mu$ s necessary would be a prohibitive time penalty in a minicomputer that was to completely fetch and execute such a macroinstruction in that time. Therefore, a concession to the general-purpose microprogrammable minicomputer was made, and supplemental hardware was included in the arithmetic section to create the effective operand address by factoring all inputs simultaneously with the loading of the instruction register; thus, no time penalty was encountered in the process of creating the operand address.

In the process of executing a class of macroinstructions called the alter-skip group, a dramatic example occurs. The format [Fig 5(b)] includes a common opcode. Bit 11 designates which accumulator the macroinstruction references, bits 9 and 8 specify an arithmetic operation, bits 7 and 6 specify a logic operation on the extend register, and additional operations can be specified by setting any of the lower six bits. Complicating the execution are rules determining in which order tests and data operations are to occur. In a general-purpose microprogrammable CPU, it may take 25 or more microinstructions, too great a penalty to

be considered in the updated design. The concession was to add hardware to fully execute this type of macroinstruction, adhering to all testing sequences in two to four microinstructions depending upon the tests and operations desired. The dedicated, finely tuned hardware, which handles the complexities of the instruction set, is in fact simply an optimization of hardware techniques used in earlier hardwired machines that is appended to the current microprogrammable machine to execute the base set faster. A certain set of micro ops became the firmware link from the control processor to enable this complex hardware. These micro ops are used exclusively for high speed execution of the base set macroinstructions; they are not useful to the microprogrammer in general-purpose computations because of their machine-oriented definitions.

Although supplemental hardware is necessary to emulate the macroinstruction set of the previous hardwired machine with reasonable performance, this hardware need not impact the general microprogrammable machine.

In most microprogrammable minicomputers processing of a typical macroinstruction is divided into two distinct phases: fetch and execute. Responsibility for reading main memory at the location pointed to by the program counter, possibly incrementing the program counter, waiting for main memory to complete the access, and loading the returned data into an instruction register, usually belongs to the fetch phase. These functions are usually incorporated into a single, common, fetch microprogram. The link to the execute phase is the subsequent enabling of decoding logic (usually a ROM or a programmed logic array that looks at various instruction bits and maps them into an appropriate execute phase (ie, one of many execute microprograms that is specifically dedicated to execution of a particular macroinstruction)).



Because access time of most minicomputer main memories is much longer than the microcycle, the fetch microprogram can require up to one-half of the total time dedicated to processing even a simple macroinstruction [Fig 6(a)], due to the often inefficient wait for main memory. One solution to this problem is to reduce effective main memory access time through use of superfast memory systems, interleaved modules, and/or cache frontend memories. This minimizes effective fetch time, but results in increased cost.

In the processor under consideration the problem was attacked using an approach that requires no additional hardware costs beyond the basic memory system, yet attaches virtually no main memory wait penalty to fetching the macroinstruction. The concept involves pipelining macroinstruction fetches so that they appear as transparent to the overall macroinstruction processing time as possible. The next fetch (read of main memory) begins when the execution microprogram of the previous macroinstruction nears completion. The corresponding main memory read time, typically much greater than the execution time of a single microinstruction, thus overlaps as much as possible the execution microprogram of the earlier macroinstruction; therefore, by the time the first macroinstruction is completely executed, the next macroinstruction is available for use at the main memory. Consequently, a shorter fetch microprogram is required [Fig 6(b)] to load data into the instruction register and to perform a direct program branch to its execution microprogram. Implementing an overlapped fetch can be straightforward in a microprogrammable minicomputer. Near the end of all executed microprograms, one microinstruction is inserted to update the program counter and memory address register, and to begin the actual memory access for the next macroinstruction. This extra microinstruction is not an absolute time penalty, but rather a relocation of a microinstruction that eventually would have been encountered in the fetch microprogram. By initiating the next macroinstruction access early, what is traditionally the fetch microprogram is distributed among all execute microprograms (Fig 7).

The possibility of using interleaved main memory with a high speed cache front-end was analyzed, but was determined to offer no significant performance increase beyond that achieved with the overlapped fetch concept [Fig 6(c)]. One factor in this decision was that high speed random-access memories (RAMs) provided a main memory that cycled in less time than the access time of many cache-based memory systems that were commercially available. Therefore, enhancement of the control processor through microprogramming methods was the most cost-effective approach to augmented performance.

Memory system in the minicomputer is implemented in an asynchronous method: ie, any speed memory system can be accommodated automatically. Since memory activity can occur in parallel with execution of the requesting microprogram, memory access time is generally masked by other computational tasks.

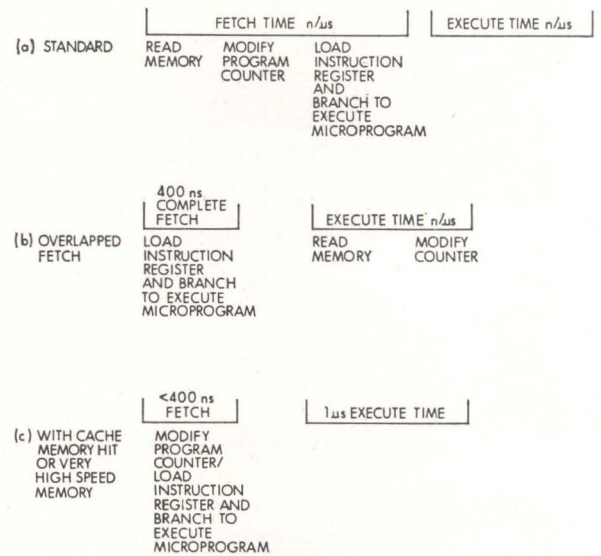


Fig 6 Fetch and execute times. Overhead to fetch macroinstruction can be significant for low cost microprogrammable minicomputers. Pipelining, or overlapping, fetch operation or adding cache are two ways to overcome this penalty

When, in a main memory read access, memory data are required by the microinstruction sequence, the control processor will "pause," if required, until the memory system access time has been realized. This pause time is a function of memory system speed and the amount of other computations (microinstructions) that can be performed between memory start command and the data retrieval command (or next memory start command).

Dynamic modulation of microinstruction execution times is implemented in a further effort to fine tune the control processor for fast performance. As previously indicated, data manipulative microinstructions represent a high frequency and, therefore, a performance-dictating event. Data paths within the processor are limited by device delays and bus loading to an approximately 175-ns read-modify-write cycle. The basic control processor is designed, then, to extract maximum performance by defining the clock system such that those instructions execute in 175 ns.

Branching instructions, however, impose a sequence of events that cannot be accommodated in 175 ns. The microaddress register (MAR) is incremented typically at the end of each microinstruction. Since a branch is detected and its condition is evaluated in the micro-



A. TRADITIONAL FETCH		B. OVERLAPPED FETCH	
MICROINSTRUCTION	DESCRIPTION	MICROINSTRUCTION	DESCRIPTION
1	UPDATE PROGRAM COUNTER AND MEMORY ADDRESS REGISTER, AND BEGIN READ	1	LOAD INSTRUCTION REGISTER FROM MAIN MEMORY
2	WAIT FOR MEMORY	2	BRANCH TO EXECUTE ROUTINE
3	WAIT FOR MEMORY	3	•
4	LOAD INSTRUCTION REGISTER FROM MAIN MEMORY	4	•
5	BRANCH TO EXECUTE ROUTINE	5	•
6	•	6	UPDATE PROGRAM COUNTER AND MEMORY ADDRESS REGISTER, AND BEGIN READ
7	•	7	•
8	•	8	RETURN TO FETCH MICROPROGRAM
9	•		
10	RETURN TO FETCH MICROPROGRAM		

Fig 7 Traditional vs overlapped fetch. Processor (b) saves time because it has initiated its memory fetch near completion of previous execute microprogram. Processor (a) may lose valuable time waiting for relatively slow main memory to complete access cycle, as in traditional fetch sequence. Using high speed cache memory in (a) would reduce wait time as illustrated in Fig 6(c). Concepts of processor in Fig 7(b) can be economically applied to any microprogrammable minicomputer where microcycle interval is faster than main memory access time

instruction immediately preceding the target microinstruction, the MAR must be reloaded during execution of the branch instruction. To allow for subsequent delays through control store of this new address, the microinstruction must be stretched (to 280 ns, in this design) to guarantee that access time. While other schemes avoid this problem, such as a "prepare to branch" instruction in a previous program step, they were found to be conceptually more difficult to code, and were therefore deemed unacceptable in a user microprogrammable environment.

### Self-Test Microprogramming

Microprogramming allows for inexpensive self-test capabilities in a minicomputer. Performed automatically on power-on or boot-up, or invoked manually, these self-tests ensure a properly configured and cabled processor, and provide a degree of confidence in memory system and internal data paths. Extending through standalone memory-resident diagnostics to online system fault detection programs, they require access to internal control points not accessible to the macro-machine, but made available through the microprogrammable processor. These control points are tested

first in the self-test sequence, as they are required for the manipulation of the data paths and the control processor state sequence. Upon successful completion, data paths, shifter, ALU, and register file are checked for any "stuck-at" faults or addressing errors. If at any point an error is detected, the failure is reported through a previously verified link, which might be a light-emitting diode (LED) display, or as in this design, a hardware front panel. Reported information should be sufficiently explicit to direct the operator to the failing assembly.

On system boot-up, a read-write complement-restore test is performed on the memory system to assure that it is nondestructive. On cold power-up and manual self-test, a more thorough test on the memory is performed. Here, microprogramming provides the capability to test processor-installed memory with a diagnostic that is not resident in the same memory. Test patterns and addressing sequences are chosen as worst-case tests for dynamic RAMs, error-correction syndrome in the memory controller, and processor-to-memory handshake logic. This capability is invaluable in quick diagnosis of "soft" or "hard" memory failures. Any failure detected is reported to the front panel along with the address and failing data patterns, allowing



for quick board exchange and fast interpretation of failure information.

## Remote Program Load

A common problem is how to gain the attention of a minicomputer system regardless of its present state without extensively manipulating an operator panel or system console. Applications may include systems where a minicomputer is an inaccessible element in the configuration, "turnkey" systems that power-up intelligently without operator assistance, or remote unattended satellite systems. Solutions have been obtained through such schemes as specific power bootstrap sequences or terminal drivers in either ROM, main memory, or default firmware in microprogrammed machines. Downline loading capability has been more difficult to ensure, however. An unattended, remote, minicomputer installation that has improperly executed its program is difficult to analyze from a master system if, for example, interrupts to the remote system are not subsequently recognizable. Microprogrammable capability called remote program load (RPL) has been incorporated in the present design to solve this.

An external input/output (I/O) device requests RPL by asserting a request line in the I/O backplane that is sampled by the emulation microprogram during fetch and indirect routines. This triggers a sequence of events and invokes a microprogram that halts the computer, presets the I/O system, loads one of four selectable ROM-resident bootstrap programs into main memory for disc or other I/O systems, and initiates its execution. RPL provides two convenient modes of operation. First, a properly configured system will automatically boot after power is applied, and no intervention is required. Second, RPL provides the same auto-boot capabilities in a remote computer site or satellite system. Any backplane I/O device may invoke RPL, or it may be triggered from a user-written assembly program (privileged) that is executed.

## Improved Microprograms

Microprogrammable minicomputers offer increased computing power. The application price/performance ratio can be improved by developing microprograms to alleviate computational bottlenecks in the system. Microcoding is generally effective when used to complement programs or portions of programs that are executed frequently. Examination of a program's locality with an activity profile generation program or other monitoring technique will show that certain (and usually small) segments of code are being executed most of the time. By microcoding those segments of code, performance can be increased six to ten times or more by the total program.

Microcoding in this manner serves to tune a processor system to a specific task. Since macro-machine

(assembly) instructions are usually general in their capabilities, defined instructions improve the efficiency of control over the memory-data path system. In addition, main memory is freed from maintaining state sequence control (program flow) for those segments that are microprogrammed. Since the control processor in this design can cycle two to three times faster than the memory system, and since approximately 40% of all memory accesses by assembly language programs are to facilitate program sequence control, resulting performance is significantly improved.

Microprograms are invoked by 176 user instruction group (UIG) machine-language opcodes that map to specific locations in control store. The UIG opcode may be followed by a parameter list of arbitrary length. Control store address space is 16k words, which provides a large capacity for potential code development.

Microprograms are developed by the use of a debug-aid, microassembler/cross-reference generator, text editor, programmable ROM (p/ROM) tape generator,

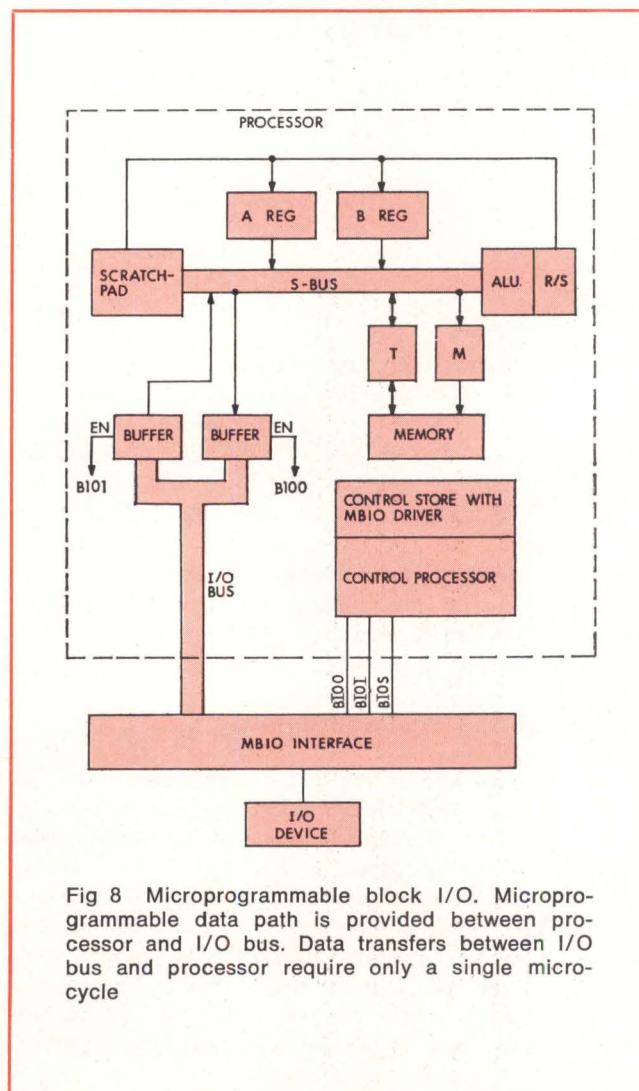


Fig 8 Microprogrammable block I/O. Microprogrammable data path is provided between processor and I/O bus. Data transfers between I/O bus and processor require only a single micro-cycle







to activate signals BIOI and BIOS. Conversely, to output data to the external device, the microword is

OP	SPECIAL	ALU	STORE	ENABLE	COMMENT
		PASS	I/O	A	Pass Reg A Data Into I/O Device

to activate signals BIOO and BIOS. Several devices can be addressed using the select code scheme used in the traditional interface. Several other control and test signals in the I/O system can be re-interpreted and defined according to requirements. Since the external device controller card resides in the I/O backplane of the processor, it can use the interrupt system of the minicomputer family.

Custom interfaces that do not reside in the I/O backplane may use the microprogrammable processor port (MPP). Interface between the minicomputer and an external device using the MPP link is shown in Fig 9. Once again, under microprogram control, data are passed to and from the external device using the proper mnemonic in the source and destination registers, as follows

MPP Control Signal					COMMENT
OP	SPECIAL	ALU	STORE	ENABLE	
	MPP1	PASS	MPPB	A (output)	Pass Reg A Data Into Microport B
	MPP2	PASS	A	MPPB (input)	Pass Microport B Data to Reg A

MPP1 and MPP2 are optional control lines, which are user-defined if desired. By using the MPP, and under microprogram control, high data transfer rates can be attained as follows

Transfer Type	Data Rate
Burst Mode (<16 words to register file)	5.7M words/s (max, port to scratchpad transfer)
Synchronous (no flag test for handshake, "assumed data-ready")	1.58M words/s (max, port to main memory transfer)
Asynchronous (complete handshake, interruptible, halttable)	0.75M words/s (For applications where transfer can be suspended)

The MPP is generally most effective at transferring buffered data in a block fashion. Possible applications for the MPP are connection to a high speed array processor or a hardware floating-point processor, allowing parallel processing between external processor and associated microprogram.

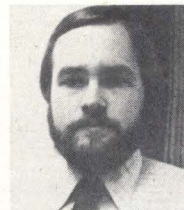
## Summary

Microprogrammed architecture allows fine tuning of a processor to a specific application in a cost-effective

manner. The designer can provide speed gains and emulate sophisticated macroinstructions with great ease, as well as provide a more structured debug environment in which to develop them. Similarly, powerful features may be inexpensively added with the aid of microprogramming to produce a more useful and adaptable minicomputer. Similarly judicious use of microprogramming allows the minicomputer to be custom-tailored to a particular task in a cost-effective and performance-oriented fashion. Microprogramming offers several valuable benefits that include: (a) higher execution speed at low cost, (b) better main memory utilization, (c) increased security for code segments, (d) additional functionality through full control of the control processor, (e) a high speed communication link to a variety of custom I/O interfaces, (f) nonvolatile self-test capability, and (g) an inexpensive method of implementing new capabilities.

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Philip Gordon, currently a development engineer at Hewlett-Packard, was involved in development of the 21MX M-Series and subsequent E-series minicomputers. He holds a BSEE degree from the University of California at Berkeley.

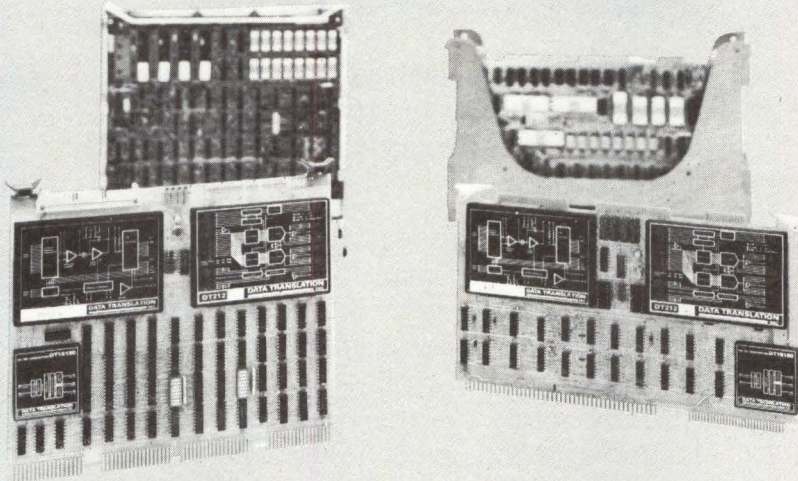


Scott Stallard holds a BSEE from the University of California at Berkeley and is working on his MSEE degree from Stanford University. He is currently a development engineer for Hewlett-Packard, where he participated in design and integration of the E-series minicomputer.



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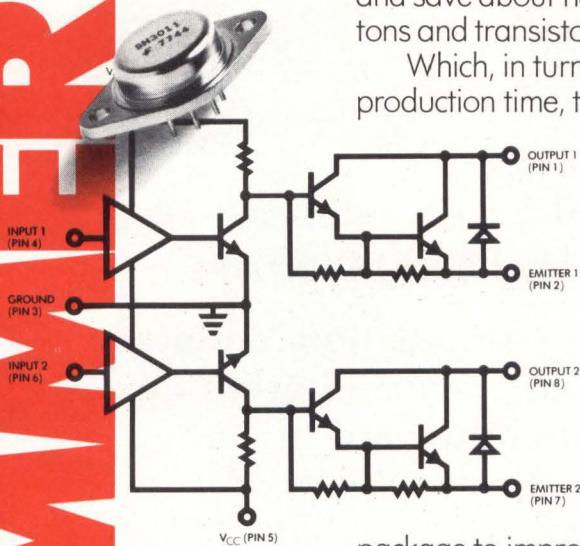
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# DESIGN CONSIDERATIONS FOR DUAL-DENSITY DISKETTE CONTROLLERS

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An expanded outlook of design factors for a dual-density diskette controller involves system integration of the diskette drive and covers bit packing densities, data recovery methods, input and output interfaces, and available methods of accessing data

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**John Worden**     Magnetic Peripherals, Incorporated, Oklahoma City, Oklahoma

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Implementation of flexible diskette drives as low cost data processing peripheral memory devices is increasing rapidly in terminals and standalone systems, where storage capacity, performance, and capability to random-access data make them suitable for on- and offline information and software applications. Previously limited by the ability to operate using single-density, single-sided media, the storage capacity of flexible diskette drives quadrupled during the past year when units capable of both double-density and 2-sided media read/write operation were introduced. However, since existing single-sided, single-density-encoded diskette drive controllers were incapable of operating 2-sided, double-density-encoded devices, a major effort was needed to develop controllers that were capable of handling the double-density drives.

The most useful diskette controller will operate with either single-sided, single-density-encoded diskettes or 2-sided, single- or double-density-encoded diskettes, ie, a dual-density diskette controller. A controller that would provide IBM compatible format for data interchange using single-density-encoding, and would operate with double-density capability under program control for file use, would furnish maximum diskette flexibility and storage capability and would maintain current media interchange standards.

Implementation of these criteria and considerations for the dual-density controller demands particular

attention to the hardware/software interfaces of both the diskette drive and the host computer. Specifically, the controller interface must consider diskette format, read/write-erase head design, data encoding and recovery means, and diskette drive requirements. The host computer interface must be concerned with software command-level interface, logical interface between the two devices, and the timing relationships necessary for contiguous-sector data transfers—the optimum condition for diskette data transfer.

## Soft- and Hard-Sector Formats

The most commonly used diskette format is the single-density, soft-sectored (or IBM 3740 compatible) type, wherein a diskette is preformatted with individual record identification fields followed by the data field (Fig 1). A 2-sided diskette doubles the data capacity of a single-sided diskette; similarly, double-density devices double both capacity and data transfer rate of the single-density devices. Storage capacities for soft-sectored diskettes are specified in the Table. Increasing the number of bytes per sector and decreasing the number of sectors per track actually increases the total storage capacity of the diskette because track capacity is more efficiently utilized. For single-density IBM format of 77 tracks, 74 are used for data storage,



### Soft-Sector Diskette Capacities

	Single-Sided Single Density	2-Sided Single Density	Single-Sided Double Density	2-Sided Double Density
Diameter	7.88" (200.2 mm)			
Package size	8 x 8" (203.2 x 203.2 mm)			
Coating	Magnetic Oxide			
Total tracks/diskette	77	154	77	154
Data tracks/diskette (includes index)	74	148	74	148
Data transfer rate	31.2k bytes/s	31.2k bytes/s	62.5k bytes/s	62.5k bytes/s
Spindle speed	360 rev/min			
Average latency	83.3 ms			
Unformatted capacity				
bytes/track	5208	10,416	10,416	20,832
bytes/disc (74 tracks)	385,392	770,784	770,784	1,541,568
Formatted capacity (bytes/sector for)				
26 sectors/track	128	128	256	256
15 sectors/track	256	256	512	512
8 sectors/track	512	512	1024	1024
4 sectors/track	1024	1024	2048	2048
2 sectors/track	2048	2048	4096	4096
1 sector/track	4096	4096	—	—
Bytes/diskette (74 tracks for)				
26 sectors/track	246,272	492,544	492,544	985,088
15 sectors/track	284,160	568,320	568,320	1,136,640
8 sectors/track	303,104	606,208	606,208	1,212,416
4 sectors/track	303,104	606,208	606,208	1,212,416
2 sectors/track	303,104	606,208	606,208	1,212,416
1 sector/track	303,104	606,208	—	—
Data reliability				
Recoverable errors	1 in 10 <sup>9</sup> bits			
Unrecoverable errors	1 in 10 <sup>13</sup> bits			

two as alternates for bad tracks, and one for maintenance purposes. Track 00 is the index track and certain sectors within it are defined for specific data. The controller design must consider bad tracks, variable sector sizes, and single and double densities.

Hard-sectored techniques use equally spaced holes around an inner circumference of the diskette. These holes are sensed by a photocell to define the beginning of each sector location (Fig 1). A hard-sectored diskette with 32 sector holes, 128 data bytes/sector, and 4096

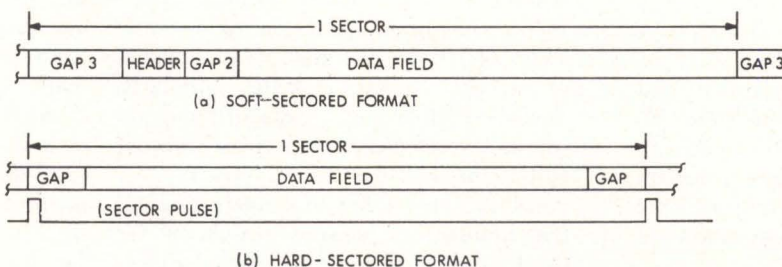


Fig 1 Sectored diskette formats. Soft-sectored diskette consists of two fields (header and data) per sector; hard-sectored diskette may contain only one field (data) per sector. Hard-sectored diskettes allow greater data storage per track because header fields are eliminated



bytes/track, represents 23% more storage capacity than a similarly encoded soft-sectored diskette.

For a soft-sectored diskette, the controller locates a sector by searching for and interpreting the contents of the header field. In 3740 compatible format the header contains track number, sector number of the following data field, diskette side (0 or 1), and length of the following data field. Once the desired header field is located, data contents of this sector may be read or written by enabling the read or write gate at a fixed time interval from the header field.

To read or write a hard-sectored diskette, the controller uses a sector counter register, which is initialized to zero by the singular index pulse from the diskette drive. The sector counter is then updated with each sector pulse, and the controller locates the desired sector by comparing contents of the sector counter with the desired sector value. Data contents of this sector are then read or written by enabling the read or write gate at a fixed time interval from the diskette drive sector pulse.

A hard-sectored data field may contain an imbedded header for read verification, whereas a soft-sectored format usually contains only system data. Start of data field bytes may also be different. Media interchangeability and incompatibility of separate hard- and soft-sectored diskette controllers are key design considerations. Since current IBM devices do not use hard-sectored, compatible designs do not require additional logic to handle hard-sectored operation.

## Read/Write-Erase Head Design Impact

Presently, two types of read/write and erase head constructions are prevalent—tunnel erase and straddle erase (Fig 2). Both types consist of a single read/write magnetic transducer and two erase magnetic transducers. The read/write transducer senses or

creates magnetic field flux reversals on the diskette media in line with disc rotation. These flux transitions are interpreted as digital data bits by the controller according to the data encoding scheme used. Erase transducers create a separation band between adjacent tracks on the diskette: a magnetic field in line with disc rotation for tunnel erase and at right angles to it for straddle erase. The tunnel-erase design has the advantage of minimizing the noise influence of data stored in adjacent tracks; the tunnel erase geometric construction produces a more clearly defined erase band, thus improving signal to noise ratios.

An advantage of straddle erase heads results from the shorter distance from the read/write head to the end of the erase head. This allows erase current to be turned on and off earlier, while still ensuring erased bands the entire length of the written data fields. (Note that this timing is affected by different head velocities and packing densities at the inner and outer tracks.) Shorter erase times allow shorter gaps between data or data header fields on the diskette, which permits more recoverable data to be written on the diskette. From a cost viewpoint, analysis shows insignificant manufacturing advantages of one head type over the other when yield, material, and labor factors are considered. However, from a business standpoint, the tunnel-erase head has a definite advantage due to its wide acceptance in the industry and its multiple sources.

What type of erase head to use in conjunction with a diskette controller design is mainly a system consideration. Most drives incorporate a fixed delay interval to control erase current turn-on and turn-off; ie, erase-coil control is not accessible by the controller. If IBM format is used, either head type should allow data to be read or written, since IBM equipment uses a tunnel-erase head. However, if nonstandard IBM format is used, with gap times between data and/or data and header fields determined by the controller for the optimum performance characteristics of a

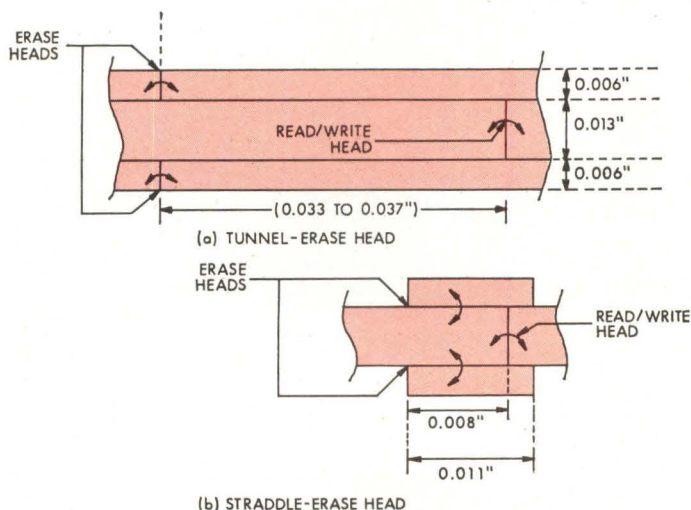


Fig 2 Read/write and erase head types. Tunnel-erase and straddle-erase heads are independent conventional magnetic transducers that create magnetic field at diskette surface proportional to current applied through individual read/write or erase coils. Principle is common for both erase head configurations. Major differences are constructional and geometric, which create head views shown looking from diskette surface



straddle erase head, this format can not be read or written if the drive uses a tunnel-erase head.

## Dual-Density Format Considerations

Modified frequency modulation (MFM), double-density-encoded, soft-sectored diskette format utilized by the CDC 9474 controller (see Fig 3) is generally the same as the IBM 3740 single-density, soft-sectored case except for different gap lengths, preambles, data contents, data transfer rates, and address marks. Each data sector is defined with a header or identification (ID) field and a data field. ID field consists of a preamble (PRE) that allows the controller to differentiate between MFM encoded clock and data bits, lock in a phase-locked loop data detector or synchronize the data recovery detector, and enable an address-mark decode. The unique address ID mark (AMH) allows controller electronics to group each succeeding 8-data-bit group into data bytes that define meaningful binary data, thereby establishing byte synchronization. ID field also contains track (T) and head (H) number for position verification of the head, sector (S) value in the ID field that identifies the data field sector location, and data record length field (LL) that informs the controller how many bytes of data are to be transferred to or from the data field. The 2-byte cyclic redundancy check (CRC) characters are compared to regenerated CRC bytes during reading to verify data.

Header gap 2 (GAP2) field allows the controller designer to establish the timing relationship relative to the location of the data field. It also permits a tolerance gap that enables drive electronics to switch between header read mode and data field write or read mode. Generally header fields are not rewritten after a format operation. Data fields are written, including preamble, address mark, data, and CRC at a location on the diskette determined by a fixed time interval from the header field. Data field will shift slightly between gaps 2 and 3 due to controller and device tolerances, creating "write splices" of unknown data and clock content. Care must be taken in the design to prevent false address mark detection due to these write splices.

Data fields are read by enabling read electronics a fixed time interval after the desired header (ie, past possible write splices). Purpose of the data field preamble is identical to that of the ID field preamble. Data field address mark (AMD) establishes byte synchronization and identifies the data field as valid data or as a control field. For data integrity, regenerated CRC bytes are compared to recorded CRC bytes.

Logic implementation of a hard-sectored diskette controller differs from that of soft-sectored controllers; however, data rate logic is the same. Read/write timing is controlled by occurrence of the sector pulse, and sector location is determined by counting sector pulses relative to the index pulse, or possibly by reading the imbedded header of the previous sector. In practice, the entire sector is written, including preamble char-

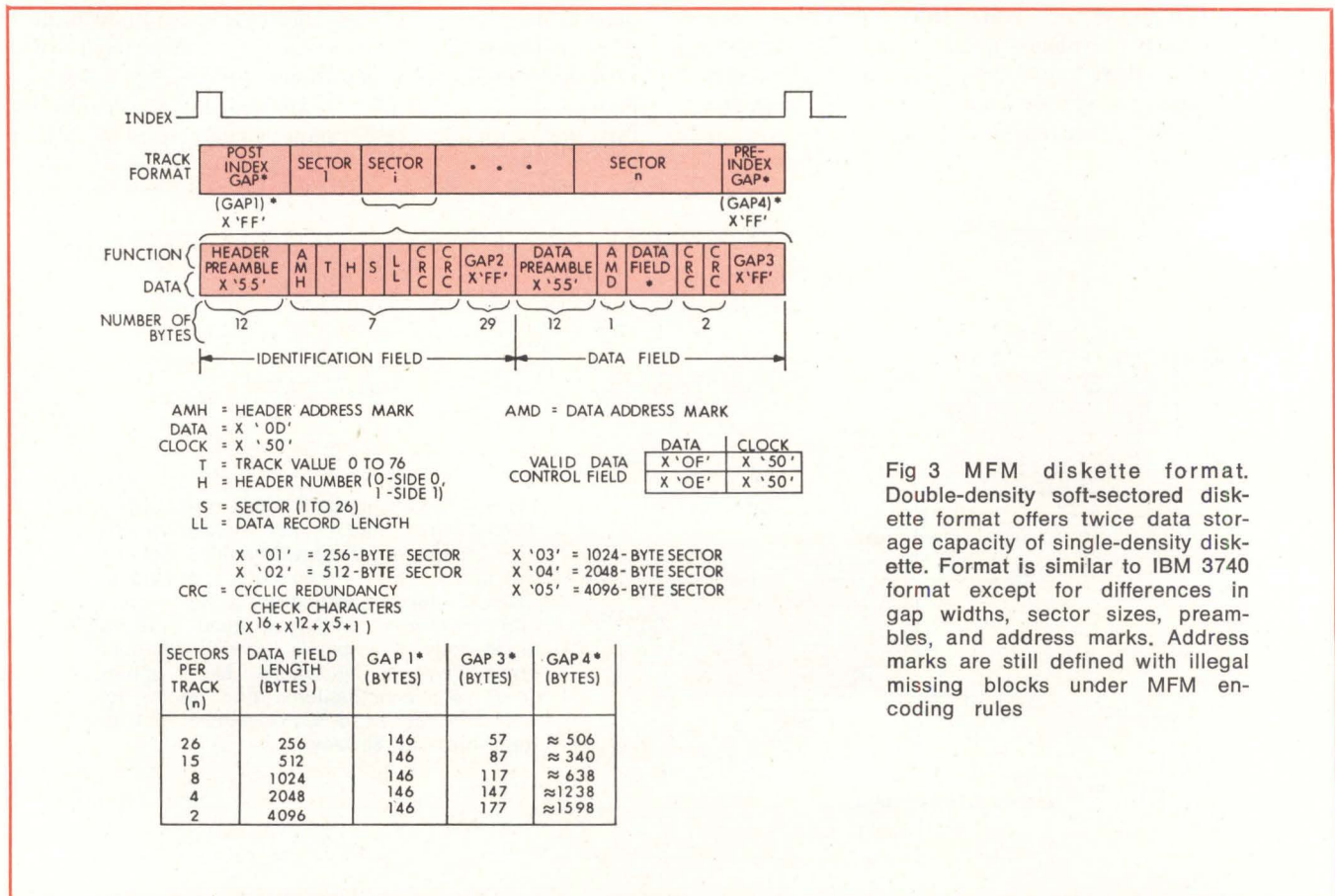


Fig 3 MFM diskette format. Double-density soft-sectored diskette format offers twice data storage capacity of single-density diskette. Format is similar to IBM 3740 format except for differences in gap widths, sector sizes, preambles, and address marks. Address marks are still defined with illegal missing blocks under MFM encoding rules



acters, address mark, imbedded header in the data field for possible read verification, data field, and CRC. For sector reads, preamble and address mark are functionally equivalent to their soft-sectored counterparts; however, hard-sectored address marks usually do not contain illegal missing clocks. Imbedded header of the sector being read can be used only for sector verification as it is really part of the data field.

## Encoding Schemes and Data Recovery Methods

Four encoding schemes in current use with flexible diskette drive devices are frequency modulation (FM), also referred to as double-frequency (DF) coding; modified frequency modulation (MFM); modified-modified frequency modulation ( $M^2FM$ ); and group code recording (GCR). (See Refs 1-5). Single-density IBM 3740 compatible diskette units use FM encoding.<sup>6</sup> Double-density diskette drives and their associated controllers use either MFM,  $M^2FM$ , or GCR encoding. Hardware complexity generally increases in the following order: FM, MFM,  $M^2FM$ , and GCR. Implementation cost and/or IBM interchange compatibility will greatly affect the double-density encoding scheme chosen. Key factors to be considered for all schemes and methods are data recovery method, peak-shifting for double-density encoding, and coding/decoding.

Data recovery for FM encoding can be accomplished by either a one-shot pulse or a phase-locked oscillator (PLO). Since the latter is mandatory for all double-density encoding schemes, it should be used with both single- and double-density encoded diskettes. For FM encoding, the read head signal frequency components<sup>1</sup> are 125 and 250 kHz—a subset of the 125-, 166.7-, and 250-kHz frequency components of MFM encoding.<sup>1</sup> For  $M^2FM$  encoding, frequency components<sup>1</sup> are 100-, 125-, 166.7-, and 250-kHz, which require a wider bandwidth but still have FM frequencies as a subset. However, GCR frequencies<sup>1</sup> are 104.17-, 156.25-, and 312.5-kHz, without any FM encoding frequencies as a subset.

The PLO data recovery method has several advantages over the one-shot method even in single-density controller operation. As a result of its inherent locking onto the data stream frequencies, the PLO averages and negates the effects of phase shift due to different motor speeds, drive bit shifting, and circuit delays. In contrast, a one-shot pulse interval is fixed and is not modifiable to the incoming data stream frequencies. Additionally, a PLO automatically accounts for speed variations in defining window times for data or clock bits, whereas speed variations must be subtracted from one-shot window times.

Peak shifting<sup>1,2</sup> is a characteristic of magnetic discs that results from interference of adjacent bit flux reversals, which cause a flux reversal to be read slightly before or after its nominal time. Although not critical in single-density encoded diskettes, due to wider data window times, peak shifting becomes critical in the inner tracks of double-density encoded media. Critical bit patterns are 011, 1000, 110, and 0001, with pulses occurring according to MFM encoding criteria. In the innermost tracks (43 to 77) peak shifting may be accounted for through "write precompensation<sup>1,2</sup>" where

the appropriate bit either delays or precedes the theoretical bit times by 250 ns. This holds true for MFM and  $M^2FM$  encoding but is of questionable value for GCR.

In addition, the controller should be able to accommodate two different write currents—a high value for the outermost tracks (00 to 42) and a low value for the innermost tracks (43 to 77)—for better data recovery reliability and compatibility with single-density IBM formats. Controller requirements involving both single- and double-density coding can use MFM advantageously for double-density encoding, with the resultant simpler design also furnishing the FM frequency component subset required for single-density encoding.

## Diskette Drive Control Lines

The write data line to the disc drive electronics (Fig 4) is a single serial line at the hardware level with write data being composed of 250-ns pulses for data or clock bits. Associated with it are a write enable line that brackets the write data and a low write current line that is turned on if tracks 43 to 77 are being written. Composite data and clock signals are transmitted over the single read data line. Two other read-lines—read data separated and clock separated—are available, but are not generally used for formats having missing clock patterns in address marks.

A head load signal line loads the read/write head against the medium; a head select line is used to select the appropriate head for double-sided operation. Head movement is usually controlled by a 10- $\mu$ s pulse (3- to 10-ms step rate) that steps the head one track at a time, acting in conjunction with a direction signal that moves it toward innermost or outermost tracks, one track at a time. Some drive units use separated pulsed step-in and step-out signals instead. Generally, the desired track is specified to the controller, which should be able to calculate the direction and number of tracks to be crossed to reach the specified track from the current one, and to handle interim assigned replacement tracks (two maximum) while performing this seek.

Initial radial reference point for soft-sectored diskettes is established at power turn-on by stepping the head out one track at a time until the track 00 positioning signal is detected. Rotational timing is available in the index/sector pulse to give a rotational reference point on the diskette; normally, this signal is used only during formatting and for diskette speed checks. For hard-sectored diskettes, a sector pulse is generated for each sector that is photoelectrically sensed on the diskette; this pulse is generally encoded into and with the index hardware lead, but may be obtained via a separate lead.

Drive status includes a ready line indicating that medium is in place and that the drive is ready for operation; a write fault line monitoring the interactive control of the write data, write enable, and head load signals; and a write protect line indicating when the write protect slot in the diskette is uncovered. Unit select and write fault reset input leads provide signals to select a particular drive and to reset a drive after a detected write fault, respectively.



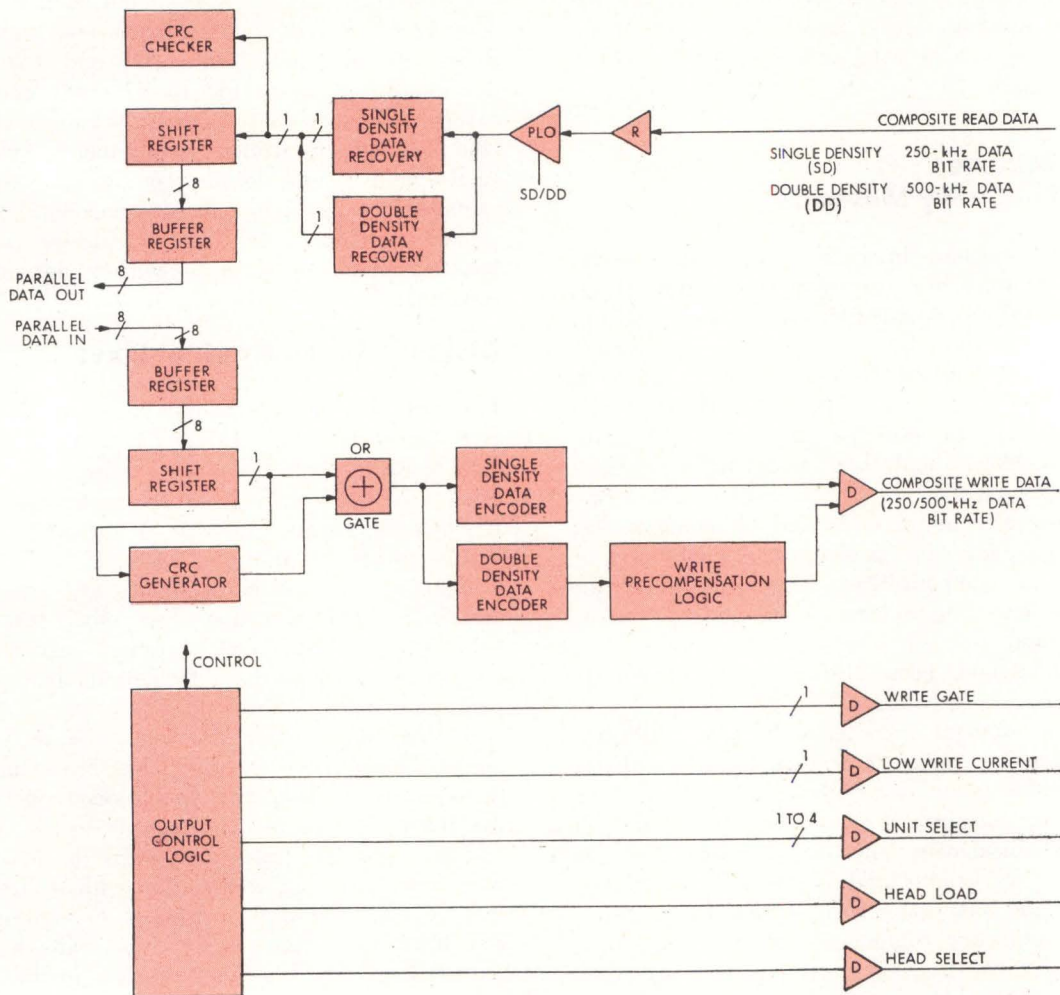


Fig 4 Diskette drive serial data interface. Data are available if unit is selected, head is selected and loaded, and write gate is not enabled. Write data frequencies, data encoding, and data recovery are different for single- and double-density encoded diskettes. Data are written on diskette by serial write data line if enveloping write-gate signal is true, unit is selected, and head is selected and loaded. Double-density diskettes may also require write precompensation. Low write current line is available to reduce write current for innermost tracks to minimize peak shifting. This functional system contains some logic that may be shared

Typical power requirements of diskette drives are 120 or 240 Vac, 24 Vdc, or  $\pm 5$  Vdc. The designer should evaluate the feasibility of either the controller or an alternate source providing the power.

### Subsystem Logical Interfaces

Subsystem interfaces for diskette controllers (Fig 5) usually involve either parallel data and control signal lines connected to an associated host processor or serial transfer of both data and control information between drive/controller and a remote processing system over a hardwired or communication type circuit.

The obvious advantage of parallel over serial data transfer is speed—more than 35 times faster in most applications—but this is often offset by the simpler hardware (and software) requirements of the RS-232-C serial interface and baud rates transmitted over data set telephones. However, a standardized software level interface is not implied, and various communication protocols are not covered. Note that for either interface the controller must contain logic to handle a high level software interface, which specifies desired unit, track, sector, direction of data transfer, status exchange, and the ability to obtain desired single or double density format.



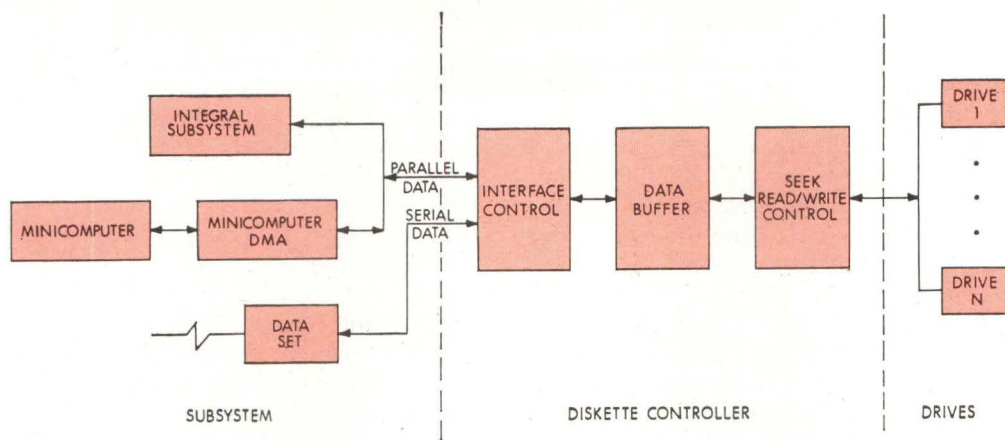


Fig 5 Diskette controller subsystem interface. Subsystem interfaces usually involve either parallel data and control line interface or serial transfer of both control and data over hard-wired or communications interface. Advantage of speed via parallel interface must be traded off against low cost standard RS-232-C communications interface

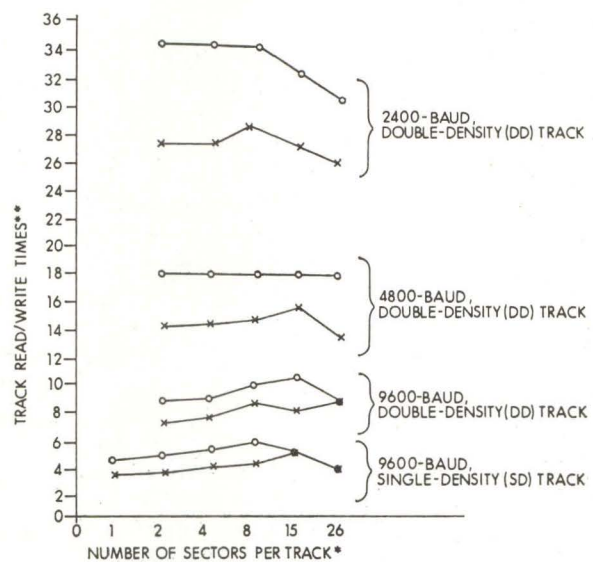
For maximum flexibility, drive controllers use generalized parallel interfaces with character present and character accept handshake logic, since fast processor interfaces vary between manufacturers. Normally these controllers contain data buffers to account for the mismatch between data rates of the drive and parallel interface. A 2-byte buffer is adequate to handle data transfers on-the-fly if data transfer rate and byte response time of the host processor are less than 16  $\mu$ s. However, if the interface has a fast data transfer capability but requires a relatively long time to get control of the data transfer channel, sufficient buffering must be provided to cover this extended access time.

Serial (RS-232-C) data transfer is generally effected at a maximum rate of 9.6k baud. Since the serial interface can not handle straight-through diskette data transfer rates in real time, data must be buffered at least on a sector basis.

## Contiguous-Sector Transfers and Interface Timing

Seek time for a data file is a function of file placement on the diskette, and is defined in terms of both track-to-track traverse and read/write head settling times. Typical times vary from 3- to 10-ms track-to-track and 10- to 20-ms settling time; thus a 77-track seek could require from 248 to 770 ms. Careful organization of data files on the diskette plus the final position of the read/write head after a file access operation can minimize seek times.

Contiguous sector reading or writing using a parallel interface results in the most efficient transfer of data between the drive/controller subsystem and its host processor. For example, an entire track of data may be transferred in one diskette revolution (0.167 s) plus the diskette latency (time to find the first sector), if contiguous sectors on the diskette can be read or



NOTES: ● = ASYNCHRONOUS  
× = SYNCHRONOUS

\* SECTOR SIZE FOR DOUBLE-DENSITY IS TWICE DOUBLE FREQUENCY. THE NUMBER OF BYTES PER SECTOR IS PER TABLE 1

\*\* INCLUDES SECTOR LATENCY AND ASSUMES A SINGLE SECTOR BUFFER. DOES NOT INCLUDE COMMUNICATION-LINE-TURNAROUND TIME

Fig 6 Read/write times for sectors per track. Track read/write times for RS-232-C interface are dependent on number of sectors per track, number of data bytes per sector, baud rate, and communications interface character structure (asynchronous vs synchronous). Double-density track takes longer than single-density track due to double number of bytes per sector. Impact of two extra bits (start and stop) for asynchronous character structure is most noticeable at lower baud rates. Impact of diskette rotational latency has visual impact on slope and parallelism of curves at all baud rates and number of sectors per track. Effectors of all communications protocols are not included



written. The first sector accessed must always allow for rotational latency, ie, 0 to 167 ms (83 ms avg). However, where the next sector of data to be transferred is just missed, necessitating another complete rotation of the disc before writing or reading can occur, a delay of up to 26 revolutions (or 4.342 s) will result if 26 sectors/track are to be transferred. To read or write contiguous sectors with minimal data buffering, data transfer rate to the host processor must be equal to or greater than that of the diskette drive (62,500 bytes/s for a double-density drive, or 31,250 bytes/s for a single-density drive).

Another critical design parameter for consecutive sector transfers is the amount of information that must be transferred between host and controller. This information—transferred between the last data field byte and the preamble of the next data field—verifies a successful transfer of the previous sector and specifies the next sector transfer. Information interchange may vary from a complete drive status transfer; host specification of the next sector, head, and track; to a single good/bad status lead with an automatic controller sector, head, and track update; or to a simple read/write command. If system constraints disallow consecutive sector transfers, sector interleaving—separation of sequential logical sectors by one or more physical sectors—should be evaluated for enhancing system performance.

Contiguous sector read or write operations are not possible using a single sector buffer with the serial RS-232-C interface. Achievable track read/write times are shown in Fig 6. A timing analysis should be performed to assure that, after line turnaround times and line protocol times have been executed, the diskette did not just miss a multiple of its revolution time. If baud rate and timing just miss a multiple of revolution time, 4.3 s are added to the time for a 26-sector read and/or write. Parallel interface controller design techniques, as well as multiple sector buffers, can be used to eliminate wasted revolutions encountered with the serial interface. Nonparallelism of asynchronous and synchronous transmission modes (Fig 6) indicates this wasted revolution time. Effects of the two extra bits required for asynchronous transmission (start and stop), plus the effect of rotational latency due to the different time intervals employed, can be seen. Note the greater effect of the two extra bits at lower transmission rates. Slopes of the curves are affected primarily by the greater number of information bytes required for the lesser number of sectors per track and by the relationship of the diskette rotational position after data transfer to the next sector.

It is evident that software-interface timing considerations are concerned mainly with data transfer, while the controller handles head positioning and timing for diskette read and write operations with respect to the physical location of the sector on the diskette.

## Summary

A dual density controller doubles data storage capacity of a diskette. Cost impact is in the controller design and not in the drive or medium. Industry standardization and media interchangeability are

achieved if the IBM 3740 single-density soft sectored format is used. This format also permits utilization of either multiple-sourced tunnel erase head diskette drives or single-sourced straddle-erase head drives. System data storage capacities are increased either by utilizing a hard-sectored format or by redefining the format for straddle erase head performance parameters; however, media interchangeability and multiple source diskette drive problems are created.

Higher cost for a dual density controller results from use of a PLO to recover both single and double density encoded data, different or more complex data recovery and encoding circuitry (FM versus MFM, M<sup>2</sup>FM, or GCR), different decoders for preambles and address marks, different gap sizes in terms of byte counts, doubled data transfer rates, and write precompensation for double density data encoding.

Diskette controller to processor interface design is determined mainly by performance tradeoffs. While a high speed parallel interface for both data and control yields greater performance, no standardized parallel interface exists and this interface differs for each processor. In addition, controller implementation, software/hardware interface, and diskette format impact realizable system performance due to the timing relationships required to achieve optimum performance levels with consecutive sector data transfers. Although yielding a lower system performance, the RS-232-C communications interface for both data and control implements an industry-standardized electrical interface. Since many communications protocols exist, final diskette controller design will depend upon the selected method. The determining performance factor is the communications baud rate, which requires at least a sector-length buffer in the controller, but timing considerations are more critical for the parallel interface.

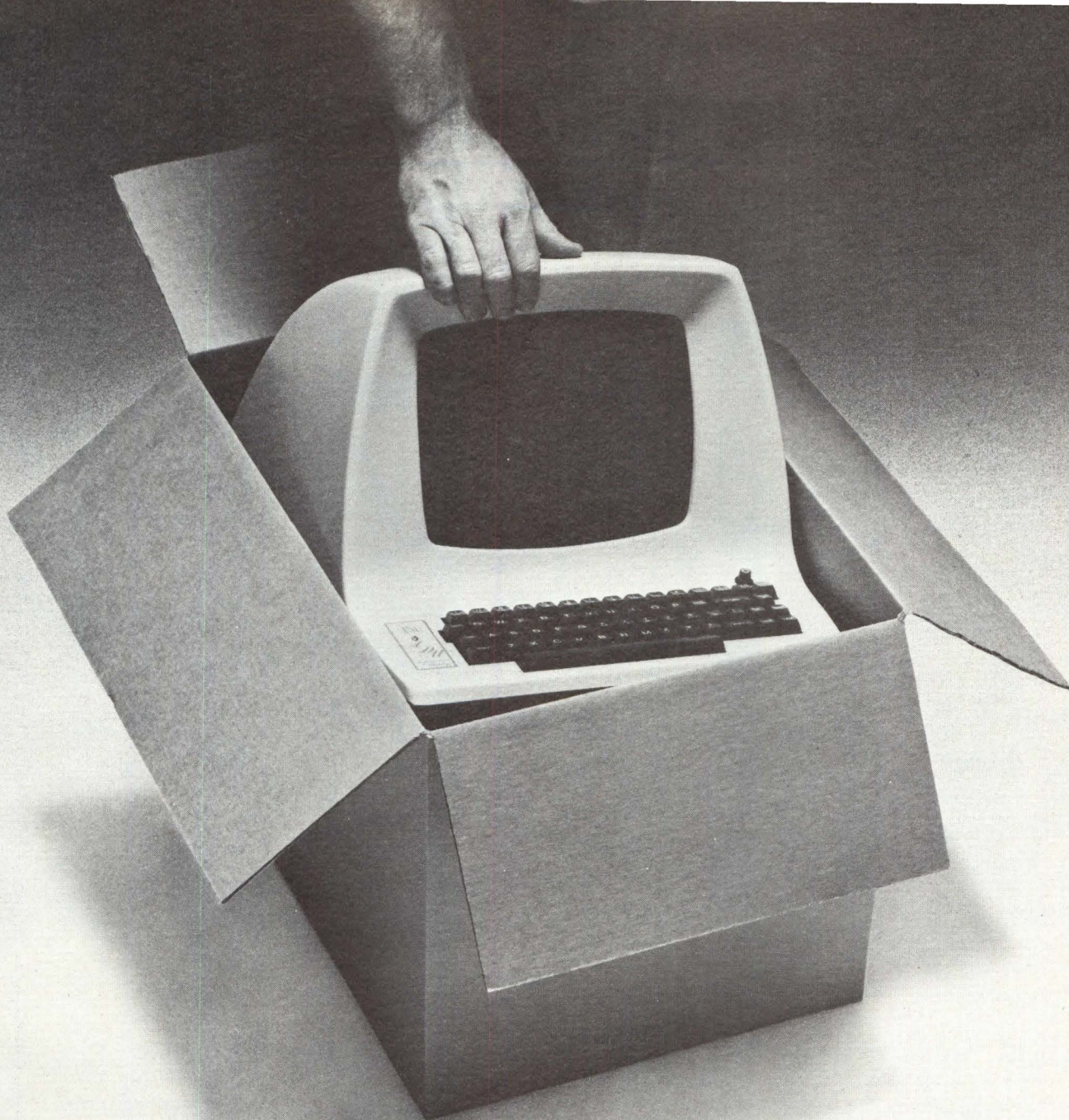
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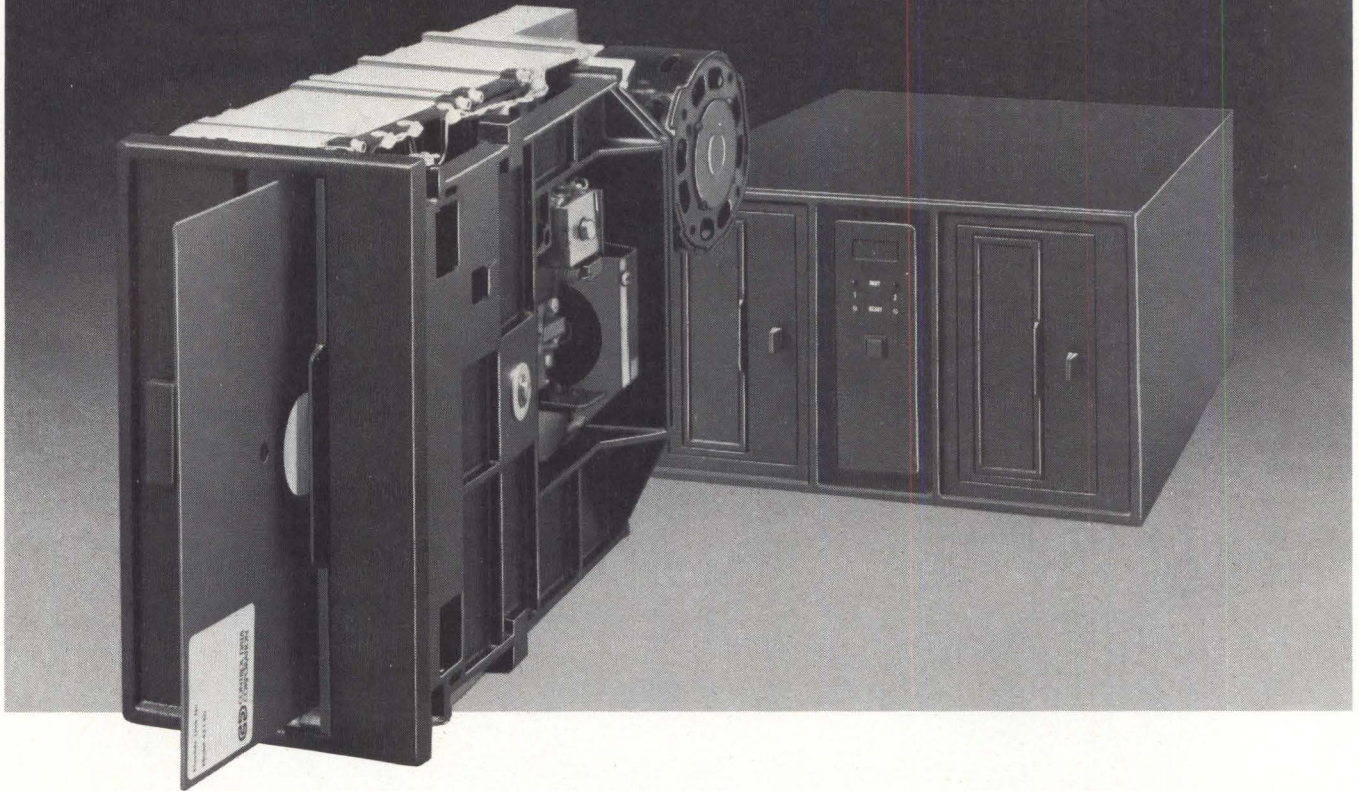
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# SOFTWARE ANALYSES FOR COMBINATORIAL LOGIC

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To produce output logic functions from variable inputs in microprocessor-based monitor and control systems, the traditional hard-wired approach is replaced by ad hoc, match, and lookup software methods, whose operational speed, memory size, and costs are compared to provide improved price/performance

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**B**asic focus of most instrumentation and control systems involves monitoring a number of input variables and generating output functions that are logical combinations of these variables. In many cases, the output function involves simple combinatorial logic. Numerous textbooks and papers have been written regarding efficient hard-wired implementation of such functions, but little has been written regarding their implementation in software. Consequently, with the increasing number of microprocessor-based systems, it is important that simple and efficient software methods be available so that costs of program development and computer hardware can be minimized.

Any combinatorial logic function can be written as a sum of products (eg,  $F = \overline{W} \cdot X \cdot \overline{Y} + Z$ ). This is probably the most commonly used form. Such simple expressions can be easily programmed for a computer, since most computers possess AND, OR, and COMPLEMENT instructions. However, for a more complex expression, the required program is not so straightforward.

## Ad Hoc Method

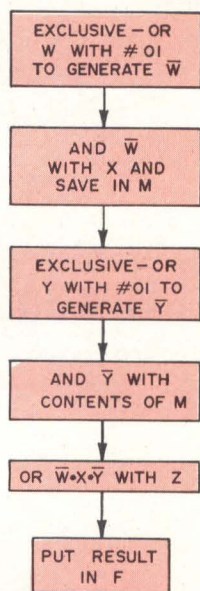
The "ad hoc" method involves writing a separate program to generate each unique switching function desired. The term "ad hoc" emphasizes that the pro-

gram corresponds to a single specific function. Each product term is generated by applying the AND instruction to the corresponding input variables (or their complements) sequentially until all literals (ie, variables or their complements) have been ANDed. Then, the product terms are sequentially ORED together.

This method is best explained by the following example. The function to be generated is  $F(W, X, Y, Z) = \overline{W} \cdot X \cdot \overline{Y} + Z$ . Assume that variables W, X, Y, and Z have already been entered into the computer and that each is stored in a separate memory location as a 1 or a 0. Thus, if the computer words are eight bits wide, a "true" variable would be 00000001, while its complement would be 00000000. Similarly, depending on whether the resulting  $F(W, X, Y, Z)$  is 1 or 0, a 1 or 0 will be stored in a prespecified memory location. Assume that the corresponding memory locations are W, X, Y, Z, and F for the remainder of this example.

Since most computers have instructions that can operate on only one, or at most two arguments (independent variables), F will be generated sequentially as indicated in the flowchart in Fig 1(a). A variety of similar ad hoc approaches could produce the same result. For example, Z could be tested first. If it is 1, a 1 output would be generated for F. If Z is 0, then  $\overline{W} \cdot X \cdot \overline{Y}$  could be generated and tested. A 1 output would be generated if  $\overline{W} \cdot X \cdot \overline{Y}$  is 1;





(a)

START	MOV A, M	;PUT W IN REGISTER A.
	XRI 01H	;NEGATE W BY IMMEDIATE EXCLUSIVE OR WITH 01 (HEXADECIMAL).
	INX H	;INCREMENT H AND L REGISTER PAIR.
	ANA M	;AND W̄ (REGISTER A) WITH X.
	MOV B, A	;SAVE WX IN REGISTER B.
	INX H	;INCREMENT H AND L REGISTER PAIR.
	MOV A, M	;PUT Y IN REGISTER A.
	XRI 01H	;NEGATE Y BY IMMEDIATE EXCLUSIVE OR WITH 01 (HEXADECIMAL).
	ANA B	;AND Ȳ (REGISTER A) WITH W̄X (REGISTER B).
	INX H	;INCREMENT H AND L REGISTER PAIR.
	ORA M	;OR W̄ * X * Ȳ (REGISTER A) WITH Z.
	INX H	;INCREMENT H AND L REGISTER PAIR.
END	MOV M, A	;PUT FUNCTION IN MEMORY LOCATION F.

(b)

Fig 1 Ad hoc method. For computer generation of function  $F = \bar{W} \cdot X \cdot \bar{Y} + Z$ , each block of flowchart (a) may require several instructions, depending on particular instruction set involved. Exclusive-ORing a bit with 1 results in negation of that bit, while Exclusive-ORing with 0 results in no change. Corresponding 8080 assembly language listing (b) shows variables W, X, Y, Z, and F stored in consecutive memory locations, with H and L address registers initially set to address where W is located. If used as subroutine, additional instructions would be required for "bookkeeping" operations, such as saving and restoring A, B, H, and L registers

otherwise, the output would remain 0. Fig 1(b) shows an assembly language listing for an 8080 program which could result from the flowchart. Each mnemonic instruction listed in the program must now be assembled into its corresponding 8080 machine language instruction. In the 8080, the H and L registers (all registers are eight bits wide) serve as address registers for memory, and the results of all logical operations are deposited in register A.

One advantage of the ad hoc method is that it is straightforward in the sense that program flow is directly related to the form of the switching function. In addition, for functions with very few variables and product terms, the resulting program may be faster and use less memory than the more general methods to be described.

Several disadvantages are associated with the ad hoc method. Each new logic function requires that another program be written, which, of course, results in high development costs due to initial program writing and subsequent error debugging. This lack of standardization also is detrimental to software maintenance. In addition, programs become quite lengthy and complex as the function to be implemented becomes more complex; multiple output functions of the same input variables require that separate programs be written

for each function; and the approach wastes memory space, since an 8-bit byte (in the 8080) is used to represent a single logic variable. Using this approach, it is not practical to store all variables in one word, because most computers do not possess instructions to perform logical operations between word bits.

## Match Method

This method involves matching input variables against a set of words corresponding to the switching function. The variables are packed into a single word in a predefined order, with a 1 representing a true variable and a 0 representing a negated variable. The variable word is compared sequentially with a prestored table of product terms which, when ored together, represent the switching function. If the variable word exactly matches any product word, a 1 output is generated.

If the switching expression is a sum of "minterms" (ie, each product term includes all variables or their negations), the table will simply consist of these minterms. For functions involving a large number of variables, the minterm table could be lengthy. An alternative approach would be to first apply standard minimization techniques to the function, thus reducing



the number of product terms required in the table. In this case, however, some of the product terms will not contain all literals, and the matching operation must be preceded by a masking operation that will exclude the "don't-care" variables. Masking means changing specific bits of a word to 0 by ANDing those bit positions with 0 and all other bit positions with 1.

Again, the approach is best illustrated by an example using the function  $F(W, X, Y, Z) = \overline{W} \cdot X \cdot \overline{Y} + Z$ . The variables have already been entered into the computer and are stored as one word. Each product term is stored in a stack, alternating with the corresponding mask term. A pushdown stack is a memory storage array that is filled by pushing new information sequentially onto its top, and emptied by sequentially popping information off the top in a last-in, first-out (LIFO) format. In the 8080, the stack is stored in read/write memory and is accessed through a stack pointer register that always holds the address of the top of the stack. Data can be popped from the stack into a working register, and the stack pointer will automatically point to the new top-of-stack location. The end of the array is indicated by an all zero mask. Thus, in this instance, the stack is initially set as follows.

		Variables							
		S	T	U	V	W	X	Y	Z
Top of stack =		0	0	0	0	1	1	1	0
		X	X	X	X	0	1	0	X
		0	0	0	0	0	0	0	1
		X	X	X	X	X	X	X	1
End of array =		0	0	0	0	0	0	0	0
		X	X	X	X	X	X	X	X

The mask precedes the corresponding minterm. An X means that it does not matter whether the bit is a 0 or a 1 since it will be masked out of the comparison anyway. Fig 2(a) presents a flowchart for this program. The Exclusive-OR operation results in a 0 in each bit position where a match (both 0s or both 1s) occurs, and the AND operation sets the "don't-care" positions to 0. Thus, a perfect match of a product term with the critical positions of the variable word results in F being set equal to a logical 1. The 8080 assembly listing is shown in Fig 2(b).

While fairly compact and logical, the method more importantly allows one program to handle any single output logic function (eight variables maximum in the example shown). In fact, the same program can be used for a variety of functions by simply setting the stack pointer to the top of the appropriate product term table.

Multiple output functions of the same variables require multiple tables and multiple calls of the same program. Also, the size of the table and the amount of time required depend upon the function being implemented. The number of necessary terms may be reduced beforehand by standard minimization schemes, either manually or computer generated. However, for very complex functions, both could become excessive, particularly time. A final disadvantage is due to the use of the stack pointer. Normally the stack pointer is used to facilitate the transfer of parameters and saving of registers during subroutine calls and execution of interrupt service routines. Since the match method uses the stack pointer, each subroutine or interrupt

TABLE 1

Output Listing for Function  $F = \overline{W} \cdot X \cdot \overline{Y} + Z$

Location	Contents	Location	Contents
0000	00000000	1000	00000000
0001	00000001	1001	00000001
0010	00000000	1010	00000000
0011	00000001	1011	00000001
0100	00000001	1100	00000001
0101	00000001	1101	00000001
0110	00000000	1110	00000000
0111	00000001	1111	00000001
1000	00000000	1100	00000000
1001	00000001	1101	00000001
1010	00000000	1110	00000000
1011	00000001	1111	00000001
1100	00000000		
1101	00000001		
1110	00000000		
1111	00000001		

routine must ensure that the stack pointer is properly saved at the beginning and restored at the end of the routine.

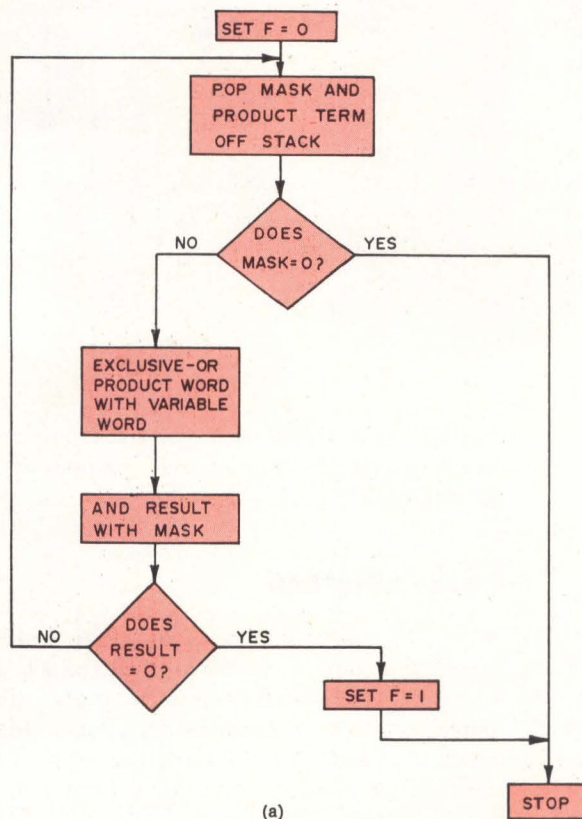
### Lookup Method

With this method, the appropriate output value is "looked up" in a prestored table, which is analogous to using a read-only memory (ROM) for hardware implementation of combinational logic. Incoming variables are packed into a word that is used as a pointer address for some location in a prestored output table corresponding to the desired function. Thus, for eight input variables, there are 256 possible address locations, each of which can represent eight output values for an 8-bit computer. If only a single output is desired, 32 8-bit words are necessary. In this case, five input variable bits select the output word, and the three remaining variable bits select the proper output bit in that word.

For instance, with the generated function  $F = \overline{W} \cdot X \cdot \overline{Y} + Z$ , the variables have been read into the computer and are stored as one 8-bit word. The output table for the function consists of 32 8-bit words as shown in Table 1. The variable word represents S T U V W X Y Z. The four unused variables (S, T, U, V) are always 0, and the output bit is always found in the least significant bit (LSB) position. Thus, the same program can be used for any single output function of eight (or less) variables by addressing another output table. The five LSBs of the variable word are used to select the output word, while the three most significant bits select the proper bit from that word. The flowchart and assembly language listing of Fig 3(a) and (b) demonstrate this method.

A slight modification of the same program can be used in a system for any function of up to eight





(a)

Fig 2 Match method. Flowchart (a) demonstrates function  $F = W \cdot X \cdot Y + Z$ ; however, any logic function can be generated by appropriately setting stack contents. 8080 assembly language listing (b) assumes that stack and stack pointer have already been set up, variable word has been loaded into register B, and A and C registers have been initialized to 0. C register will be set to 1 if value of function is 1

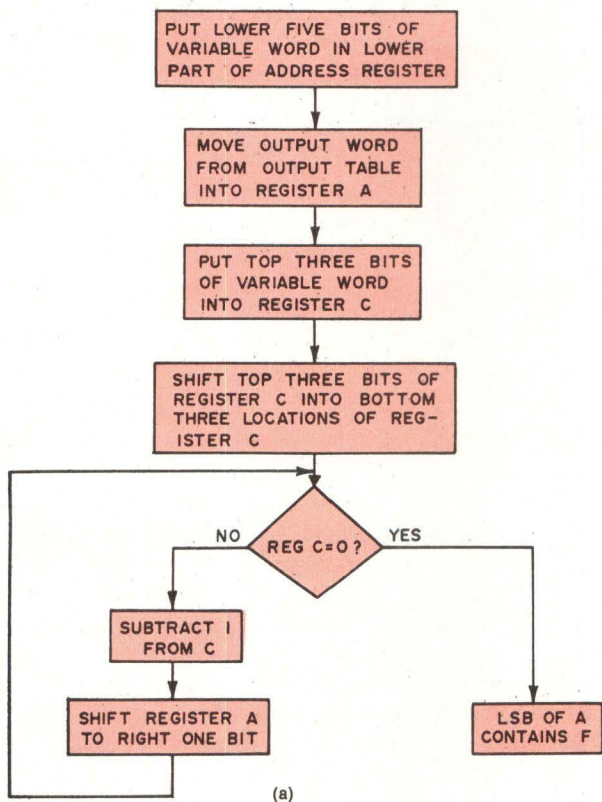
START	POP DE	;PUT PRODUCT TERM AND MASK IN D,E REGISTERS.
	ADD E	;TEST MASK FOR ZERO AND
	JZ DONE	;STOP IF ZERO.
	MOV A,B	;PUT VARIABLE WORD IN REGISTER A.
	XRA D	;ZEROS WHERE MATCHES OCCUR.
	ANA E	;ZEROS WHERE DON'T-CARES OCCUR.
	JZ ONE	;ZERO RESULT MEANS F = 1,
	JMP START	;OTHERWISE TEST NEXT PRODUCT TERM.
ONE	INR C	;SET F = 1.
DONE		

(b)

variables by storing the appropriate output table for each function. In addition, multiple output functions can be handled easily by restructuring the output array so that all outputs are in the same output word

and by appropriately modifying the addressing approach used in the program. Finally, the amount of memory required is constant for the same number of input variables and output functions of those variables.





(a)

1	START	MVI A,1FH	;FORM MASK FOR ROM BYTE LOCATION.
2		ANA B	;PUT LOWER FIVE VARIABLE BITS IN A.
3		MOV L,A	;PUT ARRAY LOCATION OF OUTPUT BYTE IN L.
4		MVI H,00H	;SET H = 0.
5		DAD D	;GENERATE ADDRESS OF OUTPUT BYTE BY ADDING D,E (START OF ARRAY) TO H, L.
6		MVI A,E0H	;FORM MASK FOR OUTPUT BIT LOCATION.
7		ANA B	;PUT UPPER THREE VARIABLE BITS IN A.
8		RLC	;ROTATE BIT LOCATION
9		RLC	;FROM A <sub>7</sub> A <sub>6</sub> A <sub>5</sub>
10		RLC	;TO A <sub>2</sub> A <sub>1</sub> A <sub>0</sub> .
11		ADI 00H	;SET CONDITION FLAGS PROPERLY.
12		MOV D,A	;PUT BIT LOCATION IN D.
13		MOV A,M	;PUT OUTPUT BYTE IN A.
14	TEST	JZ DONE	;TEST FOR ZERO BIT COUNT.
15		DCR D	;DECREMENT BIT COUNT.
16		RRC	;ROTATE OUTPUT BYTE RIGHT.
17		JMP TEST	;GO TO TEST.
18	DONE		

(b)

Fig 3 Lookup method. Flowchart (a) and 8080 program listing (b) for computer generation of logic function correspond to one another. Output function is stored in 32 x 8-bit table that is addressed by variable word. Program assumes that initial address of output table has been loaded into registers D and E and that variable word has been loaded into register B. Upon completion of operation, value of function will be stored as LSB of register A

The amount of memory and time required with the lookup method is relatively large for simple functions. However, the program could be slightly modified to save memory or time for simple functions at the

expense of some loss of standardization. The amount of time required varies as a function of the number of shifts required in the output word, while the amount of memory required depends upon the number of input



**TABLE 2**  
**Comparison of Memory and Time Required by Logic Methods**

Logic Method	F <sub>0</sub>		F <sub>1</sub>		F <sub>2</sub>	
	Memory (Bytes)	Time (μs)	Memory (Bytes)	Time (μs)	Memory (Bytes)	Time (μs)
Ad Hoc	20	40	—	—	—	—
Match	20	70	40	320	190	2600
Lookup	60	90	60	90	260	10

variables and on the number of output functions to be generated. For example, a 4-variable, single-output function need use only two 8-bit bytes in its output table. This requires that the program of Fig 3 be modified so that only the lower bit of the variable word is used to define the ROM byte location. This can be done by changing the mask in line 1 of Fig 3(b) to 01, and defining the variable word as W X Y \_ \_ \_ \_ Z. Alternatively, time can be saved at the expense of memory by using a 16-byte table with only one bit of each byte being used to designate the output value. To do this, the mask in line 1 of Fig 3(b) would be changed to 0F and the variable word defined as \_ \_ \_ \_ W X Y Z. Lines 6 through 12 and 14 through 17 can be eliminated, since they concern rotation of the output word. Other variations to the basic approach can be generated similarly.

## Summary

The approximate amount of memory and time required on a 0.5-μs 8080A are compared in Table 2. The ad hoc approach is not compared for the more complex functions, since it would not be practical in terms of programming, memory, and time costs in these cases. The times for F<sub>0</sub> ( $\overline{W} \cdot X \cdot \overline{Y} + Z$ ) and F<sub>1</sub> (any 8-variable, single-output expression with ten product terms) using the lookup method are average values, based on four shifts of the output byte required to produce the correct output. The minimum time (no shifts) would be about 40 μs, while the maximum time (seven shifts) would be about 140 μs. Note that for F<sub>2</sub> (any 8-variable, 8-output expression with ten product terms per output), the output table contains 256 bytes, without shifting. This reduces the complexity of the program and the time required, at the expense of output table memory.

The comparisons indicate that there is little to be gained from the ad hoc approach, particularly when programming costs and loss of standardization are con-

sidered. In general, the match approach uses less memory than the lookup approach at the expense of time used. For the control of slow processes, the timing factor may be unimportant. It should be reemphasized, however, that if the number of variables is reduced, the output table required for the lookup method can be greatly reduced by modifying the program slightly. Therefore, the designer should weigh the application speed requirements and tradeoffs between hardware and software development costs (for the total number of units to be constructed) before choosing the particular programming method of implementation.

## Acknowledgement

The author wishes to acknowledge the generation of the match method by Michael O'Shaughnessy.

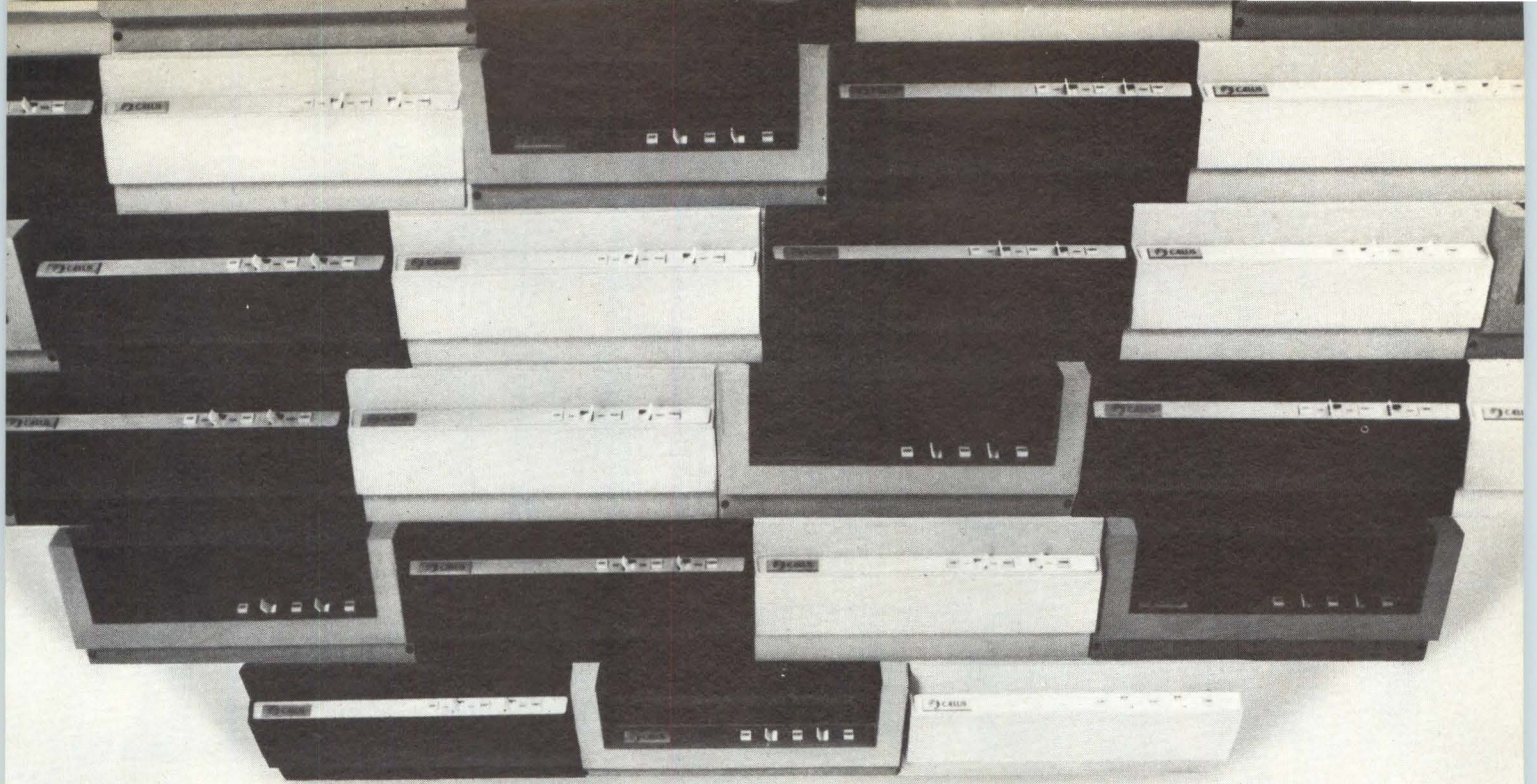
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# Programmable Handheld Calculator Computes Digital-to-Analog Converter Errors

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**Paul Prazak** Burr-Brown Research Corporation, Tucson, Arizona

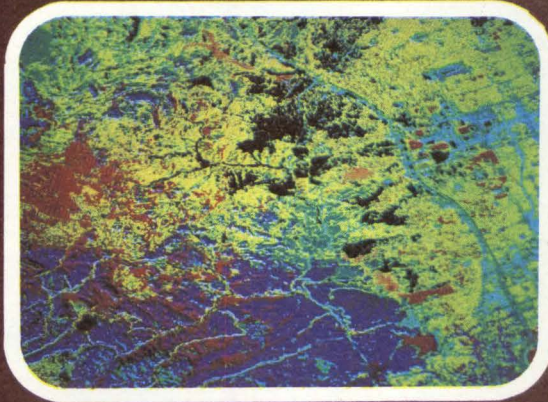
**T**he total error of a digital-to-analog converter is most meaningfully expressed as the sum of three error components: offset or minus full scale error, gain error, and linearity error. Offset error is the deviation of the actual converter's all bits off output value ( $V_{-FS}$ ) from the all bits on output value of an ideal converter. Gain error is the difference between the actual output span [all bits on output value ( $V_{FS}$ ) minus the all bits off output value] and the ideal output span; initial gain and offset errors can easily be eliminated in many applications with external potentiometers. Linearity error is the deviation of the analog output value relative to the straight line drawn between the all bits off and the

all bits on output values. Sometimes called relative accuracy, linearity error is the true measure of digital-to-analog converter performance because it cannot be adjusted externally; this error is usually specified in terms of least significant bits (LSBs), where one LSB is equal to  $(V_{FS} - V_{-FS}) / (2^n - 1)$ , and  $n$  equals the number of digital input lines or bits. Most digital-to-analog converter applications require a linearity error of less than  $\pm 1/2$  LSB for any digital input code to ensure that the output will be monotonic (ie, the analog output will increase or remain the same for an increasing digital input code).

A program has been developed for an SR-52\* programmable calculator and PC-100A printer to allow

a designer to rapidly evaluate and record the error performance of a binary-coded digital-to-analog converter (DAC) with a minimum amount of input data. The user enters into the calculator the output voltage or current value obtained by turning each bit on by itself, beginning with the most significant bit (MSB). The SR-52 automatically calculates and prints the offset error [% of full scale range (FSR)], gain error (%), and linearity error (in both LSBs and volts), as well as the worst-case linearity error (in LSBs) and associated digital input code. It requires less than one minute to execute the calculator program for a 12-bit DAC. The program can be modified easily for use without the printer.





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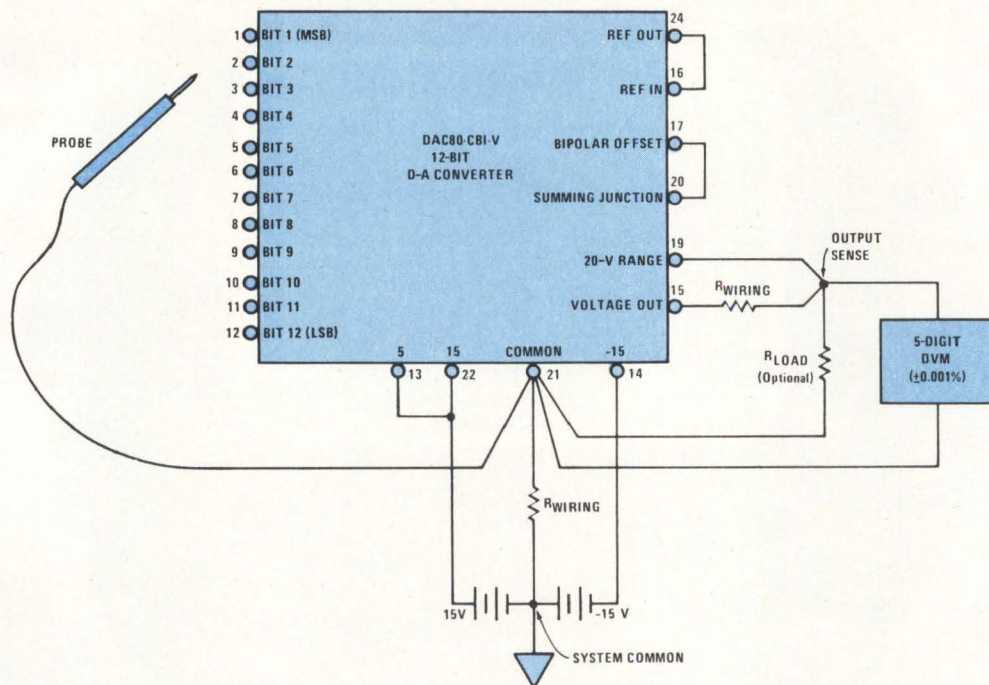
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DAC test setup. Each bit line is connected to ground one at a time beginning with MSB. Output voltage noted on voltmeter is entered into SR-52 calculator to provide complete dc error analysis of 12-bit DAC in less than 1 min. Only minimum input data are needed; results are given in units common to most major converter types

## Test Setup

The test setup in the Figure is applied to the DAC80-CB1-V 12-bit DAC; however, the program will operate for any binary-coded DAC with a resolution of 12 bits or less. Necessary test equipment includes a regulated ( $\pm 0.1\%$ ) power supply of  $\pm 15$  V (other DACs may require different voltages), and a digital voltmeter (DVM) whose accuracy is at least 10 times better than the linearity of the converter being tested;  $\frac{1}{2}$  LSB is about 0.012% of the FSR for a 12-bit DAC. Therefore, a 5-digit DVM (accuracy =  $\pm 0.001\%$ ) is required.

Since the digital input code of the DAC80 is complementary binary (a 0 on a digital input line turns that bit on), all that is necessary is to simply connect each bit to ground one at a time beginning with the MSB; the voltmeter reading is noted, and the output voltage is entered into the calculator. The only other information required is the FSR

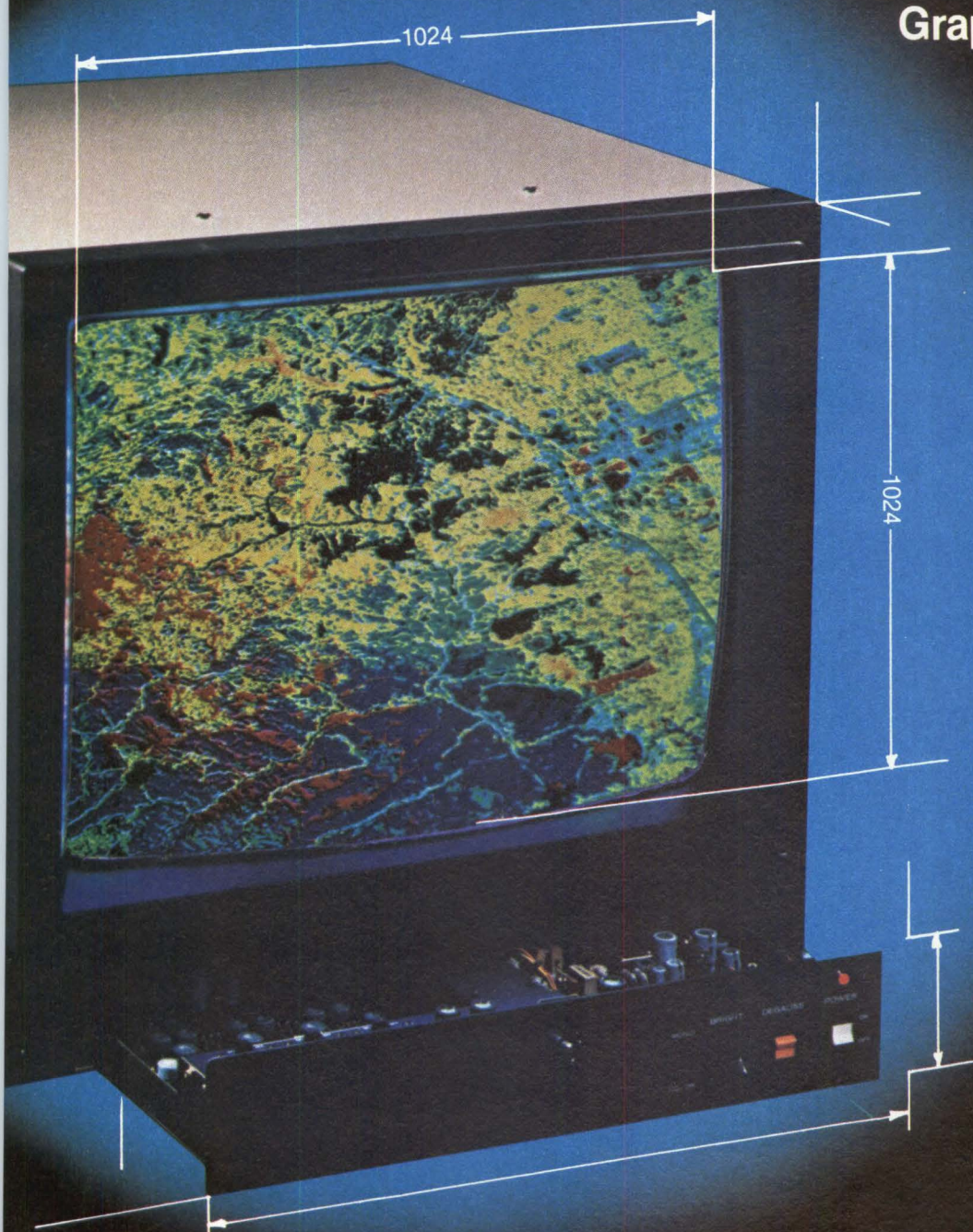
TABLE 1  
SR-52 User Instructions for  
12-Bit DAC Error Analysis Program

Step	Procedure	Enter	Press	Display
1.0	Load program card (sides A and B)			
2.0	Initialize		E	1.0000
3.0	Input data			
3.1	Enter full scale range	$V_{FSR}$	B	$V_{FSR}$
3.2	Enter minus full scale (ideal)	$V_{-FS \text{ ideal}}$	C	$V_{-FS \text{ ideal}}$
3.3	Enter minus full scale (actual)	$V_{-FS \text{ actual}}$	D	$V_{-FS \text{ actual}}$
3.4	Enter output value obtained with each bit turned on by itself (begin with MSB)	$V_{ob_i}$	A	1.0000
3.5	Repeat 3.4 for each bit (12 bits max)			
4.0	Calculate D-A errors		Run	Worst-case binary code.



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### Error Analysis Printout for 12-Bit DAC

	FULL SCALE RANGE	20.0000
	IDEAL (ALL BITS OFF)	10.0000
	ACTUAL (ALL BITS OFF)	-9.9973
INPUT	BIT 1 VOLTAGE (MSB)	0.0004
	BIT 2	-4.9985
	BIT 3	-7.4980
	BIT 4	-8.7478
	BIT 5	-9.3718
	BIT 6	-9.6848
	BIT 7	-9.8410
	BIT 8	-9.9193
	BIT 9	-9.9585
	BIT 10	-9.9790
	BIT 11	-9.9878
		BIT 12 (LSB)
	OFFSET ERROR (% OF FSR)	0.0135
	GAIN ERROR (%)	-0.0261
	LINEARITY ERROR (GAIN AND OFFSET ERROR ELIMINATED)	
	BIT 1 (VOLTS)	0.0003
	(LSB S)	0.0633
	BIT 2 (VOLTS)	0.0001
	(LSB S)	0.0214
	BIT 3 (VOLTS)	0.0000
	(LSB S)	-0.0098
	BIT 4 (VOLTS)	-0.0002
	(LSB S)	-0.0356
	BIT 5 (VOLTS)	0.0007
	(LSB S)	0.1358
	BIT 6 (VOLTS)	0.0001
	(LSB S)	0.0167
OUTPUT	BIT 7 (VOLTS)	0.0001
	(LSB S)	0.0186
	BIT 8 (VOLTS)	-0.0001
	(LSB S)	-0.0214
	BIT 9 (VOLTS)	-0.0003
	(LSB S)	-0.0517
	BIT 10 (VOLTS)	-0.0002
	(LSB S)	-0.0463
	BIT 11 (VOLTS)	-0.0003
	(LSB S)	-0.0539
	BIT 12 (VOLTS)	-0.0002
	(LSB S)	-0.0372
	W.C. LINEARITY ER. (LSB)	0.2559
	WORST CASE CODE	3296.0000

TABLE 2

### SR-52 Coding Form for 12-Bit DAC Error Analysis Program

Loc	Code	Key	Loc	Code	Key	Loc	Code	Key
000	43	RCL		65	X		98	prt
	01	1		43	RCL	075	99	pap
	06	6		01	1		99	pap
	75	—	040	06	6		43	RCL
	43	RCL		94	+/-		01	1
005	01	1		85	+		07	7
	05	5		43	RCL	080	85	+
	95	=		01	1		01	1
	42	STO	045	07	7		95	=
	01	1		75	—		20	1/x
010	08	8		43	RCL		65	X
	55	÷		01	1	085	53	C
	43	RCL		04	4		36	IND
	01	1	050	85	+		43	RCL
	04	4		43	RCL		06	6
015	65	X		01	1		09	9
	01	1		04	4	090	75	—
	00	0		55	÷		43	RCL
	00	0	055	02	2		01	1
	95	=		45	Y <sup>x</sup>		06	6
020	99	pap		43	RCL		54	)
	98	prt		09	9	095	95	=
	43	RCL		08	8		75	—
	09	9	060	95	=		43	RCL
	09	9		55	÷		01	1
025	75	—		43	RCL		04	4
	01	1		01	1	100	55	÷
	42	STO		04	4		02	2
	06	6	065	95	=		45	Y <sup>x</sup>
	09	9		42	STO		43	RCL
030	95	=		01	1		06	6
	42	STO		07	7	105	09	9
	09	9		65	X		95	=
	08	8	070	01	1		98	prt
	42	STO		00	0		65	X
035	00	0		00	0		02	2
	00	0		95	=	110	45	Y <sup>x</sup>

(10 V for a 0- to 10-V output or 20 V for a ±10-V output, for example), the ideal minus full scale or all bits off voltage (0 V for a 0- to 10-V output or -10 V for a ±10-V output, for instance), and the actual all bits off value. No adjustments of gain or offset errors are required for computing linearity error since the calculator automatically computes a "best-fit" straight line between the all bits on and all bits off output values of the DAC. Actual input and output data obtained with this test method and the printer are shown in the Error Analysis Printout for 12-Bit DAC.

#### Error Analysis Program Equations

$$\text{Offset Voltage (V}_{OS}) = V_{-FS \text{ actual}} - V_{-FS \text{ ideal}}$$

$$\text{Offset Error (\% of FSR)} = \frac{V_{OS}}{V_{FSR \text{ ideal}}} \times 100$$

$$\text{Gain Error} = \Delta K = \frac{V_{FSR \text{ actual}} - V_{FSR \text{ ideal}}}{V_{FSR \text{ ideal}}}$$

$$= \frac{\left[ \sum_{i=1}^n V_{ob_i} - nV_{-FS \text{ actual}} \right] - \left[ V_{FSR \text{ ideal}} - \frac{V_{FSR \text{ ideal}}}{2^n} \right]}{V_{FSR \text{ ideal}}}$$

where:  $V_{FSR}$  = full scale range

$n$  = number of bits



Loc	Code	Key	Loc	Code	Key	Loc	Code	Key
	43	RCL		06	6	177	01	1
112	09	9		09	9	06	06	6
	08	8		58	dsz	98	98	prt
	55	÷	147	00	0	99	99	pap
	43	RCL		07	7	81	81	HLT
	01	1		07	7	182	46	LBL
117	04	4		99	pap	11	11	A
	95	=		43	RCL	98	98	prt
	98	prt	152	01	1	36	36	IND
	99	pap		03	3	42	42	STO
	22	INV		98	prt	187	09	9
122	80	if pos		43	RCL	09	09	9
	01	1		01	1	44	44	SUM
	04	4	157	09	9	01	01	1
	02	2		98	prt	07	07	7
	44	SUM		81	HLT	192	01	1
127	01	1		46	LBL	44	44	SUM
	03	3		12	B	09	09	9
	02	2	162	42	STO	09	09	9
	45	Y <sup>x</sup>		01	1	81	81	HLT
	53	(		04	4	197	86	rset
132	43	RCL		98	prt	46	46	LBL
	00	0		81	HLT	15	15	E
	00	0	167	46	LBL	25	25	CLR
	75	-		13	C	47	47	CMS
	01	1		42	STO	202	57	fix
137	54	)		01	1	04	04	4
	95	=		05	5	01	01	1
	44	SUM	172	98	prt	42	42	STO
	01	1		81	HLT	09	09	9
	09	9		46	LBL	207	09	9
142	01	1		14	D	81	81	HLT
	44	SUM		42	STO			

Labels: A = bit values, B = FSR, C = -FS ideal, D = -FS actual, E = initialize  
Registers: 00 = bit counter, 01 = bit 1 value, 02 = bit 2 value, 03 = bit 3 value,  
04 = bit 4 value, 05 = bit 5 value, 06 = bit 6 value, 07 = bit 7 value, 08 = bit 8 value,  
09 = bit 9 value, 10 = bit 10 value, 11 = bit 11 value, 12 = bit 12 value, 13 = worst-case  
linearity error, 14 = FSR, 15 = -FS ideal, 16 = -FS actual, 17 = gain error, 18 = V<sub>os</sub>,  
19 = worst-case code, 69 = counter, 98 = n (# of bits), 99 = counter

## User Instructions

Concise user instructions<sup>1</sup> for the programmable calculator are listed in Table 1; the SR-52 coding form for the DAC error analysis program is shown in Table 2. The computations performed by the program are listed under the Error Analysis Program Equations.

An implicit assumption in the calculation of total linearity error and worst-case code is that the individual bit errors are not interdependent; that is, the contribution to the output value of each individual bit should not change when the other bits are turned on or off.<sup>2</sup> If the contribution to the output value of each bit is dependent upon whether the other bits are turned on or off, the converter is said to exhibit superposition error. Almost all DACs exhibit a slight superposition error due to thermal gradients or critical currents sharing a common ground path; but as long as it is less than 1/10 LSB, it can be neglected. This error is almost always negligible for well-designed discrete, hybrid, or monolithic DACs that have a resolution of 12 bits or less.

The PC-100A printer provides a convenient hard copy of all input and output data. To use the program without the printer, replace the print statements (prt) at calculator memory locations 021, 074, 107, 119, and 154 with halt statements (HLT). The results will be displayed in the same order as shown in the Error Analysis Printout. Simply press run after recording each result.

This program can check the accuracy of DACs used in automatic or manual test equipment, process control, or data processing to determine quickly whether calibration is required. Another application is to check DACs on an incoming inspection basis to ensure that critical parameters are being met.

## References

1. "SR-52 Owner's Manual," Texas Instruments, Inc, Dallas, Texas, 1975
2. T. Cate, "Tom Cate of Burr-Brown speaks out on D/A converter specs," *EDN*, June 1, 1971, pp 34-40

\*Interested readers may obtain a copy of Mr Prazak's program for the TI-59 calculator by requesting it in writing from the Editor, *Computer Design* magazine.

$V_{ob_i}$  = individual bit output voltage or current

Gain error (%) =  $\Delta K \times 100$

Bit error (volts) =  $E_i = \frac{1}{1 + \Delta K} (V_{ob_i} - V_{-FS \text{ actual}}) - \frac{V_{FSR \text{ ideal}}}{2^i}$

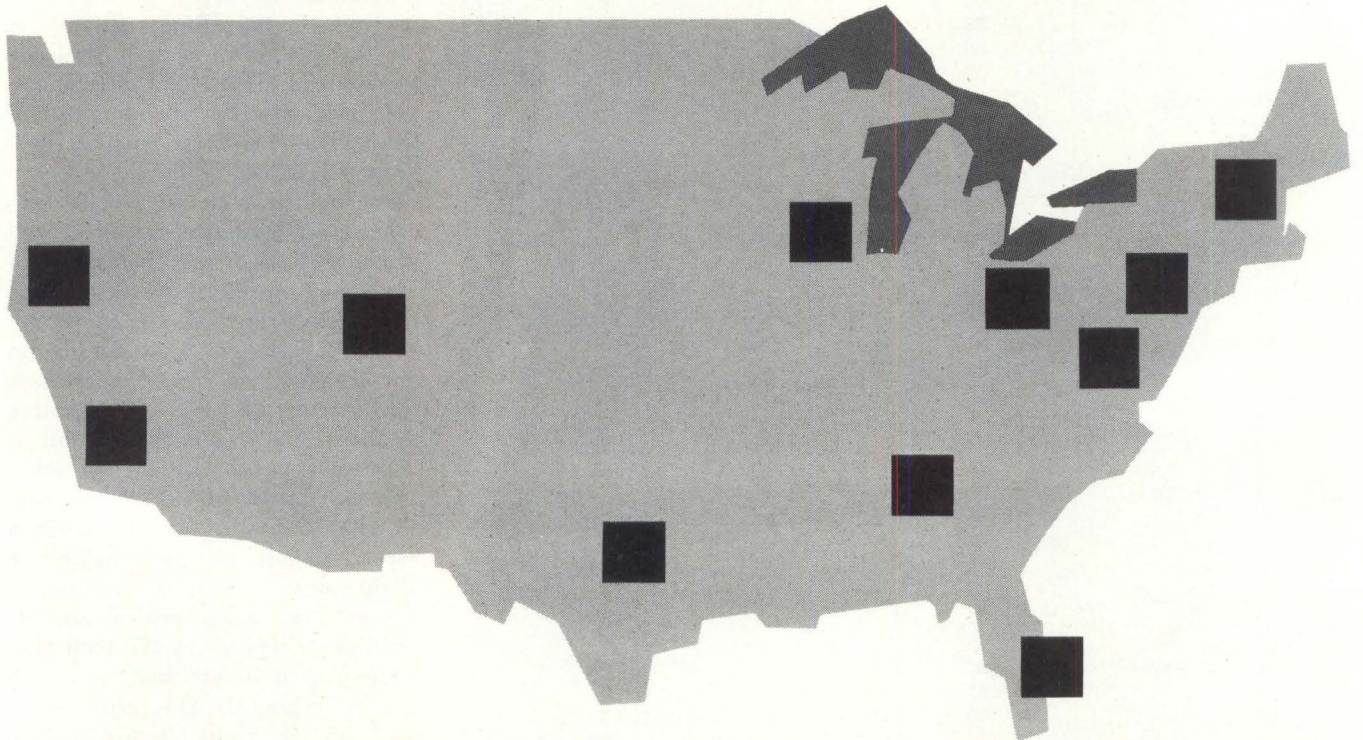
Bit error (LSB) =  $\epsilon_i = \frac{E_i \times 2^n}{V_{FSR \text{ ideal}}}$

Total linearity error (LSB) =  $\sum_{i=1}^n \epsilon_i, (\epsilon_i > 0)$

Worst-case code (decimal) =  $\sum_{i=1}^n 2^i, (\epsilon_i > 0)$



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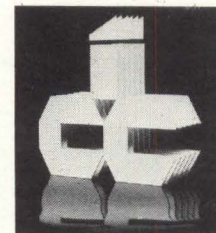
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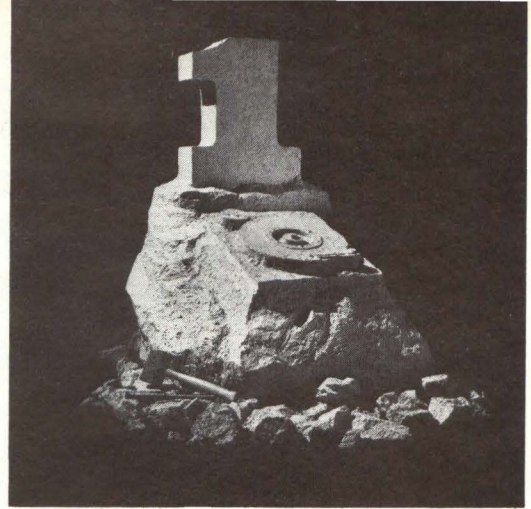


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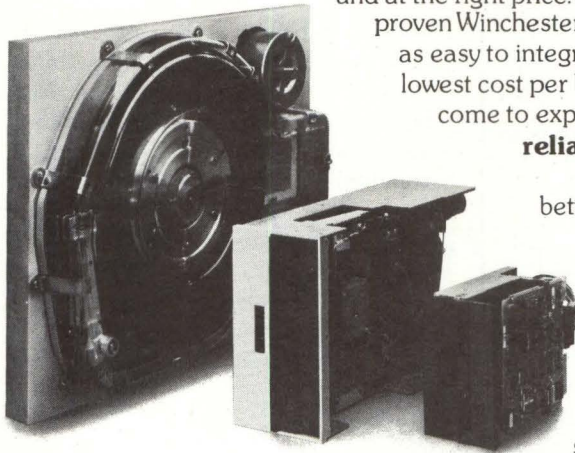
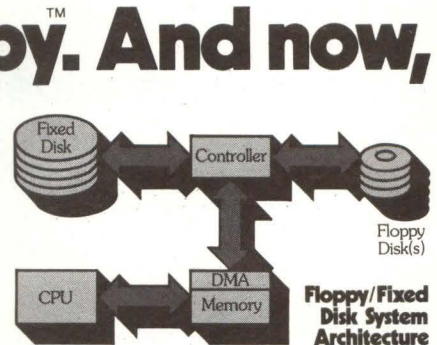


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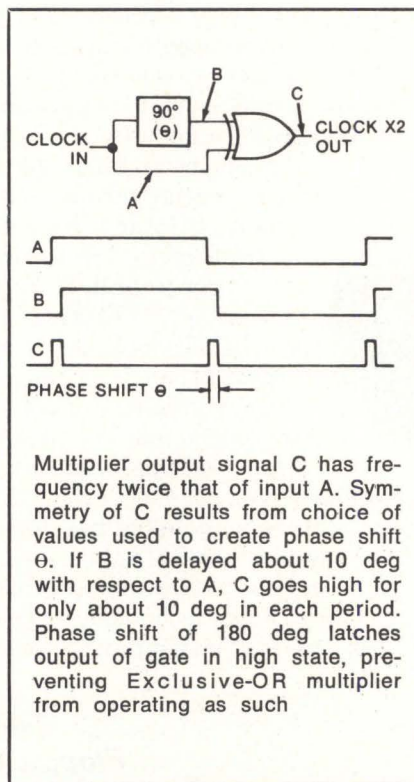
## Exclusive-OR Frequency Multiplier

*Degree of signal phase shift determines desired multiplication factor*

An exclusive-OR logic element and phase-shift network combine to perform frequency multiplication in a digital logic circuit. The exclusive-OR gate structure uses both input terminals connected in parallel to receive signals from the same source. Prior to injection into the gates, the input signal is split: half passes through the phase shifter and into one gate, while the remainder is directly introduced to the other gate input. Assuming a phase shift of 90 deg, the output frequency of the exclusive-OR is twice the frequency of the source.

The degree of output signal symmetry (and therefore the multiplication factor) depends on the amount of phase shift employed. For multiplication factors other than 2, a series of gate circuits and phase-shift elements are cascade-connected. The degree of phase shift is selected for each element to yield a cumulative multiplication factor.

Owing to the operation of an exclusive-OR gate (the output goes high when one of the inputs does), the gate output varies between a logic-low state and a logic-high condition at twice the frequency of the source signal. As shown in the Figure, logic variable A is the signal that appears at one input of the gate and at the phase-shift network input. Logic vari-



able B represents the network output signal, and variable C is the gate output. The degree of phase shift of logic variable C relative to A is a function of  $\theta$ , about 10 deg in the example.

Although a single exclusive-OR function is limited to frequency

doubling when its common-source inputs are phase-shifted, an infinite variety of multiplying factors can be achieved by cascading functions and choosing values of  $\theta$  that, when cumulatively added, represent the total phase shift required. When N exclusive-OR gates are cascaded, the total phase shift needed at the input to the Nth exclusive-OR gate is  $N / (180/n)$  degrees, where n is the desired multiplication factor.

### Note

This work was done by Kenneth G. Harf of The Singer Co for Johnson Space Center. For further information, write to: John T. Wheeler, Johnson Space Center, Code AT3, Houston, TX 77058. Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 USC 2457 (f)] to The Singer Co, Binghamton, NY 13902. (MSC-16677).

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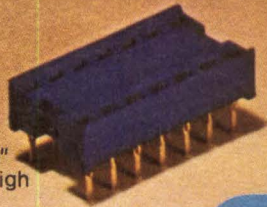
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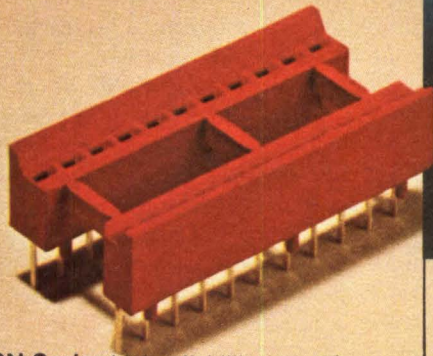
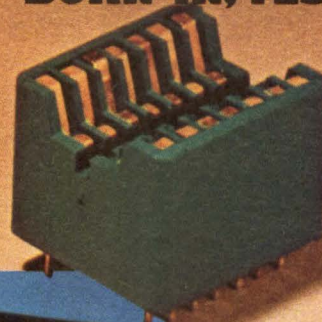
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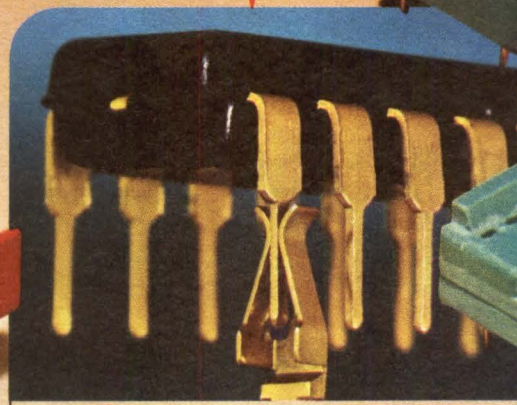
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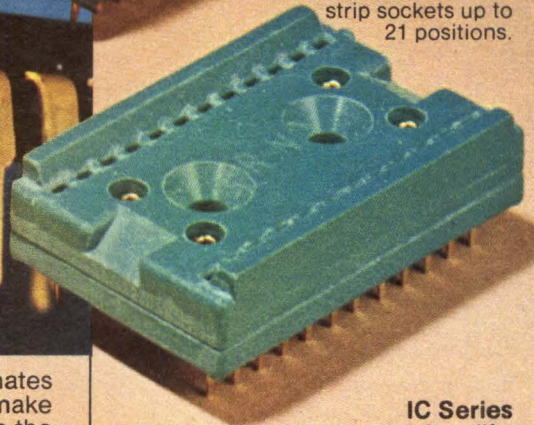


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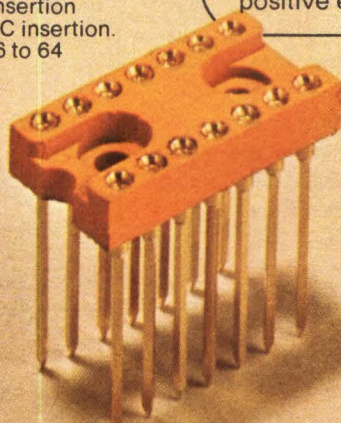
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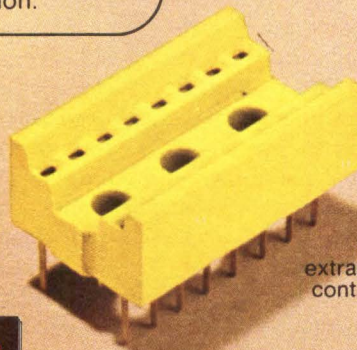


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## Concatenated Algebraic Decoder

*A coding/decoding technique for manipulating information in digital data streams*

For manipulating digital data, this technique mates two separate coding/decoding methods to produce a hybrid inner-code/outer-code system. Hardware to implement the technique has been developed using interactive digital circuitry to manipulate casually related digital data.

The inner code is an (8,4) orthogonal code which may be regarded as a (7,4) Hamming code augmented by an overall parity check bit (the last bit in each word). To correct one error, the decoder determines the 3-bit Hamming Code syndrome ( $p_1p_2p_3$ ) from the first seven code-word bits. If the syndrome is all 0s, no errors have occurred; if the code word contains an odd number of 1s, overall parity bit is in error (excluding, of course, the possibility of three or more errors). In either event, information bits 1, 2, 3, and 5 can be assumed to be correct.

If the syndrome is other than all 0s, it will uniquely identify the location of the error (again provided only one error has occurred). A logical combination of the syndrome bits can then be used as the error corrector. (If the error is not in an information bit, no correction is required.)

Thus, if the word contains no errors, no correction is made. If it contains either one or two errors, they are corrected. If the word contains three or more errors it is rejected. A total of 0.017 ms is avail-

able for carrying out the two steps needed to decode each inner code word. These decoded words then constitute the 4-bit symbols of the outer code. Symbols are shifted serially in groups of 15 to the outer-code decoder shift register.

Only erasures are to be corrected in the outer-code decoder. When the code word contains at most two erasures, it is always possible to shift the code word cyclically until one erasure appears at either the 4th or 9th symbol position and the other appears at the 10th, 11th, 12th, 13th, or 14th position. In the absence of either erasures or errors, any nine consecutive symbols of a (15,9) Reed-Solomon Code define the next succeeding symbol. If one of these nine symbols is an erasure, the 10th symbol then uniquely determines what these symbols must be. But this is precisely the situation when the code word is cyclically shifted as described above.

If the code word contains errors as well as erasures, the corrected erasures may be in error. If the number of erasures plus errors is six or less, however, distance properties of the code guarantee that the resulting corrected word will not be a code word and, hence, that some of the parity checks must fail. This event can therefore be detected by shifting the code cyclically 15 times (ie, 15 1-symbol shifts), and checking each time to see whether or not all the

parity check relationships are satisfied. While only six shifts are required, it is convenient to return the code to its original position.

Both erased symbols will be replaced by the time two full cycles (30 shifts) have been completed. Then the corrected word is shifted 15 more times. If any parity checks fail during this last step, or if more than two erasures are observed, the reject flip-flop is set and the decoded word is rejected. Otherwise it is accepted as a valid word. This completes the decoding operation. The decoded pair of command words can then be read out serially (or on a 4-bit byte basis) from the 9th column of a shift register. This can be done while the first nine symbols of the next code word are being read in.

### Note

This work was done by Raytheon Co for Johnson Space Center. For further information, write to: John T. Wheeler, Johnson Space Center, Code AT3, Houston, TX 77058. (MSC-14058).

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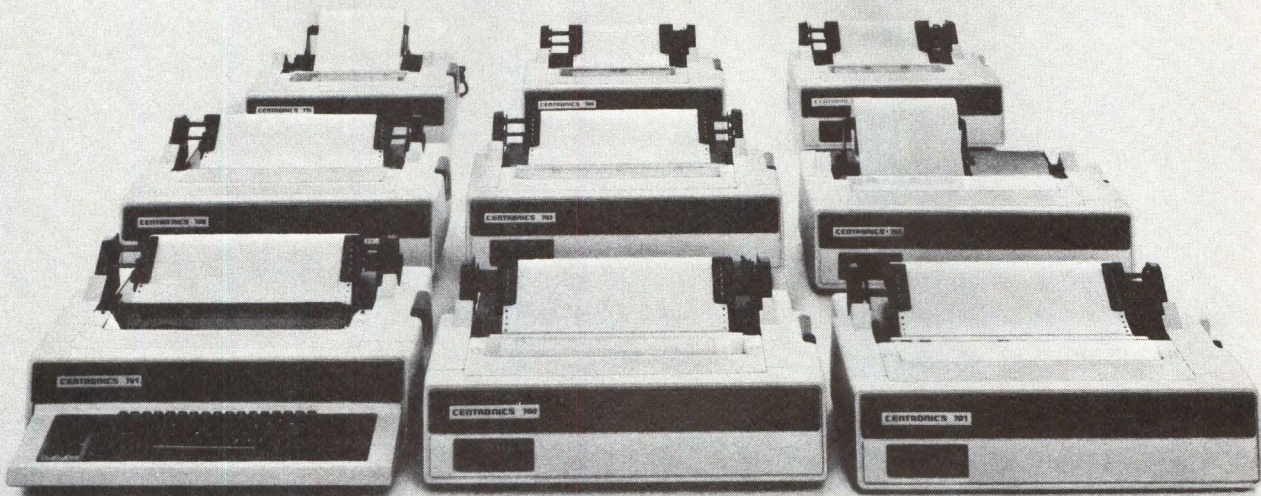


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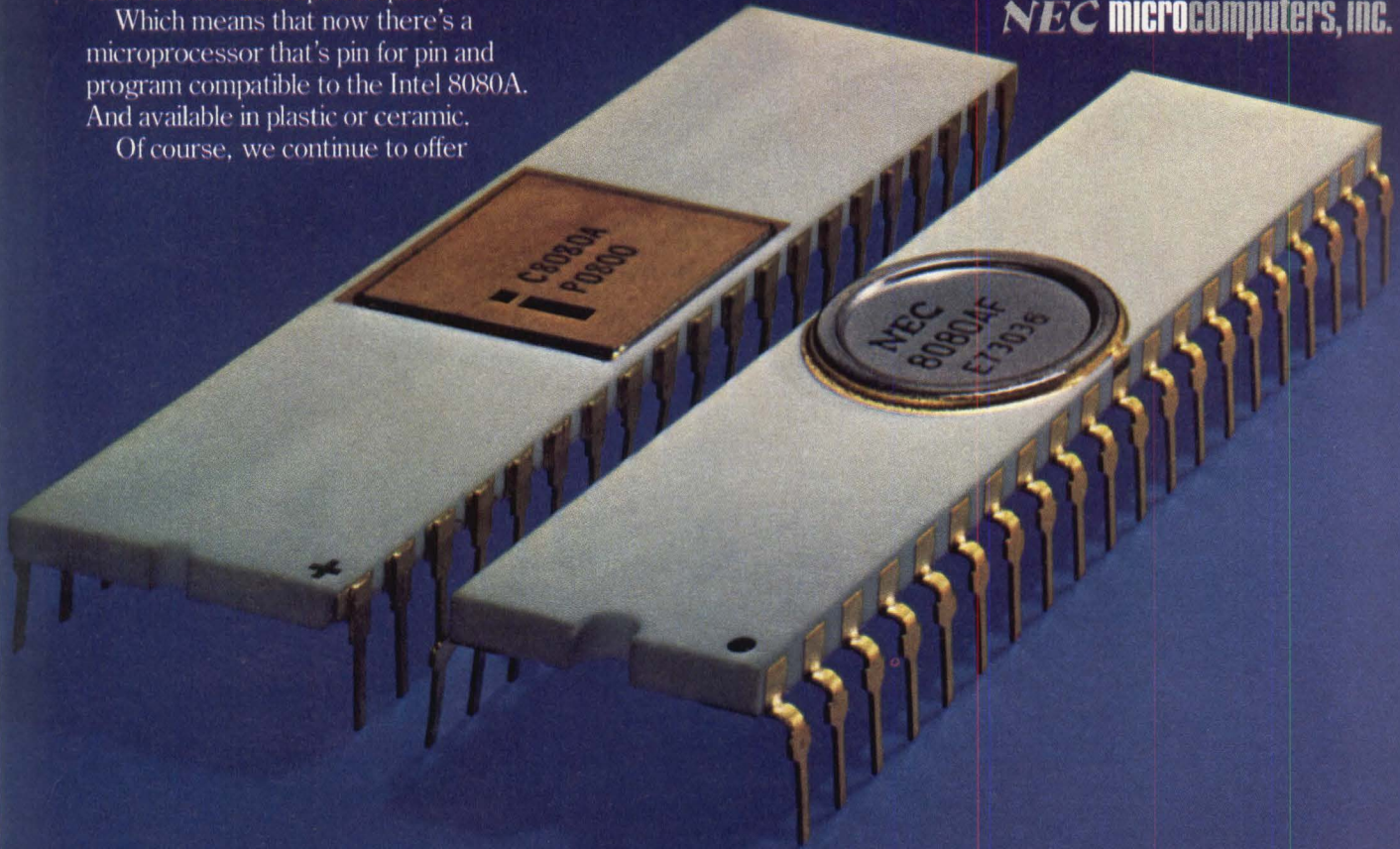
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## MICROCOMPUTER INTERFACING: COMMAND DECODERS

**Jonathan A. Titus and Christopher Titus**  
Tychon, Inc

**Peter R. Rony and David G. Larsen**  
Virginia Polytechnic Institute and State University

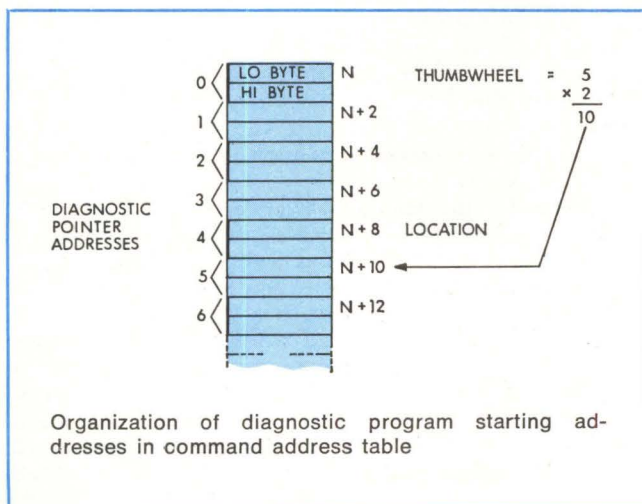
As microcomputer programs become larger and larger, it becomes apparent that the user may wish to execute only certain sections, or all of the program sections, perhaps in different orders. One way of executing only certain sections would be to enter into the microcomputer the starting address of each section, or the address where the first instruction of each section is stored in memory. After entering the starting address, the user would have to instruct the microcomputer to begin execution of the program at that address. If the program contains ten sections, ten starting addresses and the function of each program section would have to be remembered.

An easier method would be to enter a single letter or number into the microcomputer using a teletypewriter,

terminal, thumbwheel switch, or small keyboard. Once the character is entered from one of these input/output devices, the microcomputer has to determine the proper address to jump to, based on the entered character. Command decoder software permits commands to be entered into the microcomputer and decoded. Once the actions are performed, the microcomputer can return to the command decoder software so that another command can be entered, decoded, and acted upon.

A simple 8080 system monitor program can be written to enter information into the microcomputer's read/write memory, to list the content of memory, and to move the content of one memory location to another. A teletypewriter can enter these commands into the microcomputer. The letters X, Y, and Z could be used in the command decoder software so that the microcomputer executes the enter, move, and list commands; however, it is difficult to remember that the X key corresponds to enter instructions and the Z key corresponds to list instructions. It would be easier to use the first letter of each command in the software: the E key causes the microcomputer to execute enter instructions—input some data; M executes move instructions, which move the content of memory; and L implements list instructions, which list the content of memory.

Software required to decode the command entered on the teletypewriter is listed in Example 1; the software required to perform the enter, list, and move functions is not listed. At address CMDDEC, the teletypewriter input subroutine is called. The 8080 microprocessor only returns from the TTYIN subroutine when a key has been pressed. The 7-bit ASCII character will be in register A when the microprocessor does return. The content of register A (the ASCII value for the key that was pressed) is then compared to the ASCII values for the valid single-letter commands (105 for E, 114 for L, and 115 for M).





EXAMPLE 1

Single-Letter Command Decoder for the 8080

CMDDEC,	CALL	/Get a character from the teletypewriter	ANI	/Save only the receiver's status flag.
	TTYIN	/or CRT.	001	
	0		JZ	/The flag is 0, so no keys
	CPI	/Was an E entered?	TTYIN	/have been pressed. Wait for a key.
	105		0	
	JZ	/Yes, then jump to the instructions	IN	/A key was pressed, so input the
	ENTER	/stored at the symbolic address	000	/ASCII character.
	0	/"enter."	ANI	/Set the parity bit to a logic 0.
	CPI	/Was an L entered?	177	
	114		RET	/And return with the character in the
	JZ	/Yes, then jump to the instructions		/A register.
	LIST	/stored at the symbolic address	MOVE,	• /Execute these instructions to perform
	0	/"list."	•	• /the "move" function.
	CPI	/Was an M entered?	•	
	115		JMP	/When complete, jump back to the
	JZ	/Yes, then jump to the instructions	CMDDEC	/command decoder so that another
	MOVE	/stored at the symbolic address	0	/command can be entered and decoded.
	0	/"move."		
	JMP	/The character was not an E, L, or M.	LIST,	• /Execute these instructions to perform
	CMDDEC	/So ignore the character by jumping back	•	• /the "list" function.
	0	/to the beginning of the program.	•	
			JMP	/When complete, jump back to the
TTYIN,	IN	/Input the status word of the UART	CMDDEC	/command decoder so that another
	001		0	/command can be entered and decoded.

If the ASCII value for the pressed key is equal to any one of these values (the immediate data bytes for the CPI instructions), the microprocessor jumps to the section of the program that corresponds to that command.

No instructions are included in Example 1 to actually cause the move, list, or enter function to be performed. However, at the end of each section, the microprocessor should be programmed to jump back to CMDDEC. This means that after the microprocessor completes a task, it jumps back to the command decoder software so that another command can be entered, decoded, and the appropriate actions taken.

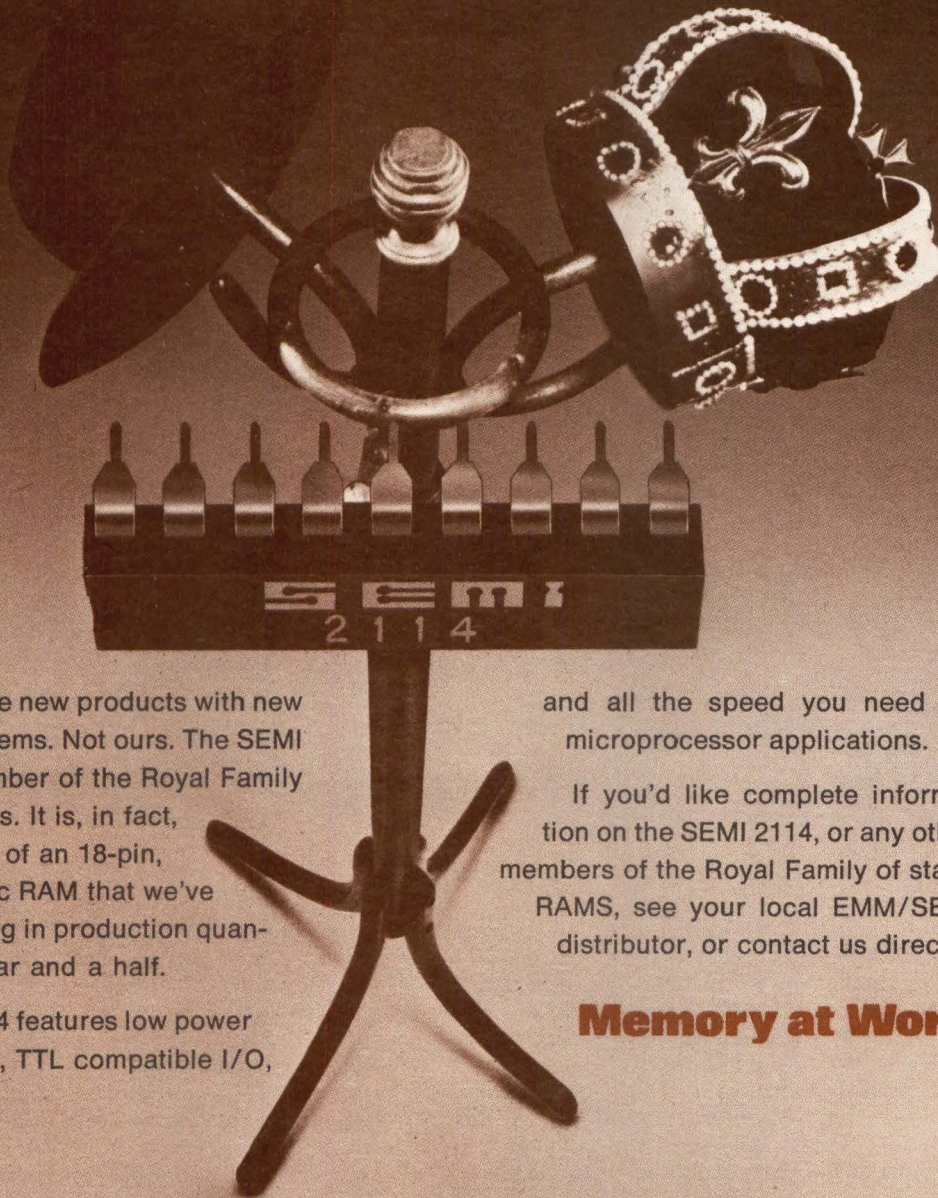
Suppose that in another program, a command decoder is needed for enter, exit, extract, and equalize commands. Because these commands all begin with the letter E, the single letters N, E, X, and Q could be used respectively for a single-letter command decoder. It might be difficult to remember whether E represents exit and X is extract, or that X is exit and E is extract. To solve this problem, the microprocessor can be programmed to recognize the first four letters of each command. Command EXTR would have to be entered for the extract sequence of instructions to be executed, and EQUA would have to be entered to execute the equalize sequence of instructions. Of course, a command decoder could be written so that the entire command is entered (exit, extract, enter, and equalize). Only if every character in the entered command matches the characters stored in memory are the desired actions performed by the microcomputer. Such a program requires about 60 memory locations for the command decoder program and additional memory to store the ASCII characters for each command.

In some small systems it may be difficult to justify the cost of a teletypewriter or terminal. Instead, a thumbwheel switch, which is a very inexpensive peripheral device, might be used to enter different commands. The thumbwheel switch is used in this case (see Figure) to specify a diagnostic program that the microcomputer must execute to test digital-to-analog or analog-to-digital converters, memories, or peripheral devices. The switch has ten positions and produces binary-coded decimal (BCD) codes 0 through 9 (0000 through 1001). However, a particular diagnostic program must relate to a number on the switch. A pushbutton can be interfaced to the microcomputer; when it is pressed, producing a logic 0, the number on the thumbwheel switch should be interpreted as the number of a diagnostic program. The program listed in Example 2 must be called periodically to check the state of the pushbutton, and if it is pressed, to interpret the data from the thumbwheel switch as a diagnostic program number. If the pushbutton is not pressed, the microprocessor returns to the program that called CHECK.

Periodically, the microprocessor must call the CHECK subroutine. The first instruction in the subroutine inputs the data from the thumbwheel switch and the state of the pushbutton. The ANI instruction saves only the state of the pushbutton in the A register. If the pushbutton is not pressed, the microprocessor will return from the subroutine. If the pushbutton is pressed, indicating that a diagnostic program must be executed, the microprocessor will not return from the subroutine; instead, the stack pointer is incremented by two. This has the function of cleaning the return address for the subroutine off of the stack.



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## EXAMPLE 2

### Command Decoder Using a Thumbwheel Switch

CHECK,	IN	/Input the status of the pushbutton
	340	/and the thumbwheel switch data.
	ANI	/Save only the pushbutton's
	020	/state in the A register.
	RNZ	/Return if the pushbutton is a logic 1.
	INXSP	/Increment the stack pointer to "clean"
	INXSP	/the return address off of the stack.
	IN	/Input the data from the thumbwheel
	340	/switch again.
	ANI	/Save only the thumbwheel switch data.
	017	
	ADDA	/Double the data from the switch.
	LXIH	/Load register pair H with the "base
	TABLE	/address" of the address table.
	0	
	MOVEA	/Save the doubled number in the E register.
	MVID	/Set the D register to 000.
	000	
	DADD	/Add the switch data to the table address.
	MOVEM	/Load a value from the table in memory, into E.
	INXH	/Increment the memory address.
	MOVDM	/Load a value from the table in memory, into D.
	XCHG	/Move the two address bytes into H and L.
	PCHL	/Jump to the address pointed to by H and L.
TABLE,	•	/Address to jump to if a 0 is on
	•	/the thumbwheel switch.
	•	/Address to jump to if a 1 is on
	•	/the thumbwheel switch.
	•	
	•	
	•	
	•	/Address to jump to if a 9 is on
	•	/the thumbwheel switch. This is the
		/end of the table.

The microprocessor then inputs the BCD data from the thumbwheel switch and sets all other bits in register A to 0 by executing the ANI instruction. The BCD data in register A are doubled when the ADDA instruction is executed. This result is saved in the E register, and the D register is set to 0. The address for the table that contains the starting addresses for the ten diagnostic programs is loaded into register pair H. The doubled BCD value is added to the address of the table. Register pair H now points to the starting address of the diagnostic program, the number for which was dialed in on the thumbwheel switch. This address has to be moved from memory into register pair D (the D and E registers) by two MOV-type instructions.

Once the starting address is in register pair D, it is moved into register pair H and then loaded into the microprocessor's program counter. The microprocessor then begins to execute the diagnostic program specified by the thumbwheel switch. With this type of command decoder, ten addresses must be stored in the command address table, even if only three diagnostic programs are stored in memory. Otherwise, a number could be dialed in that does not represent a valid diagnostic pro-

gram number. The seven "dummy" addresses could be used to jump the microprocessor back to the beginning of the program, causing no net effect.

Command decoders in one form or another are used in most microcomputer programs. BASIC interpreters use these decoders to perform different tasks for LET, SIN, LN, DIM, READ, and PRINT commands; editors, assemblers, debuggers, system monitors, and operating systems use them to allow users to direct the flow of information. Microcomputer-controlled peripherals such as p/ROM and EPROM programmers and floppy discs also use command decoders, as do many end-user products. The microcomputer-controlled microwave oven has a command decoder to defrost, broil, or simmer food, and an atomic absorption spectrophotometer has to know whether it is running blanks, unknowns, or standards. Without command decoders, which are an important building block in microcomputer software, the application of microcomputers to many problems would be severely limited.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.





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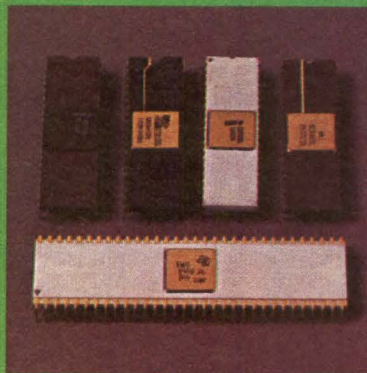
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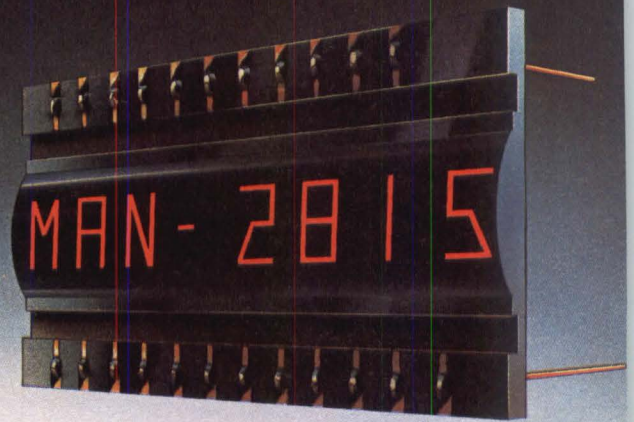
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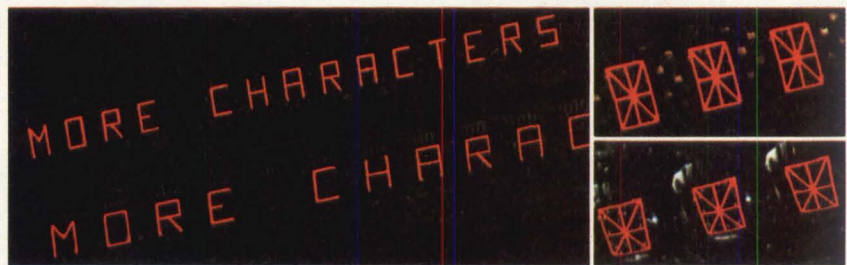
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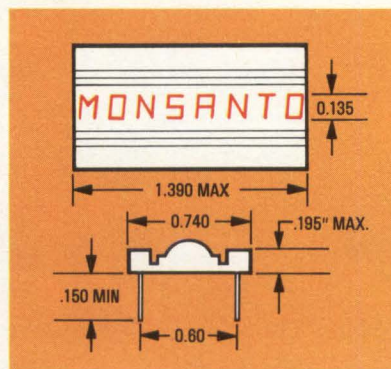
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**Left:** More characters—MAN2815 (top) and competitive unit character density in same panel space. **Right:** Less distortion—MAN2815 (top) and competitive unit when viewed 25° off of normal.

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## A-D/D-A Data Acquisition Package for microNOVA Saves On Both Software and Interface Design

Hardware interface circuit design, fabrication, and software program development problems that are involved in preparing to operate a computer system are alleviated for Data General's microNOVA series of microcomputers with the introduction of an analog A-D/D-A data acquisition system by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021. This SineTrac ST-MNOVA series includes a hardware interface and development software program on paper tape. The circuit board slides directly into the microNOVA's card guides, and

is mechanically and electrically compatible with the computer bus.

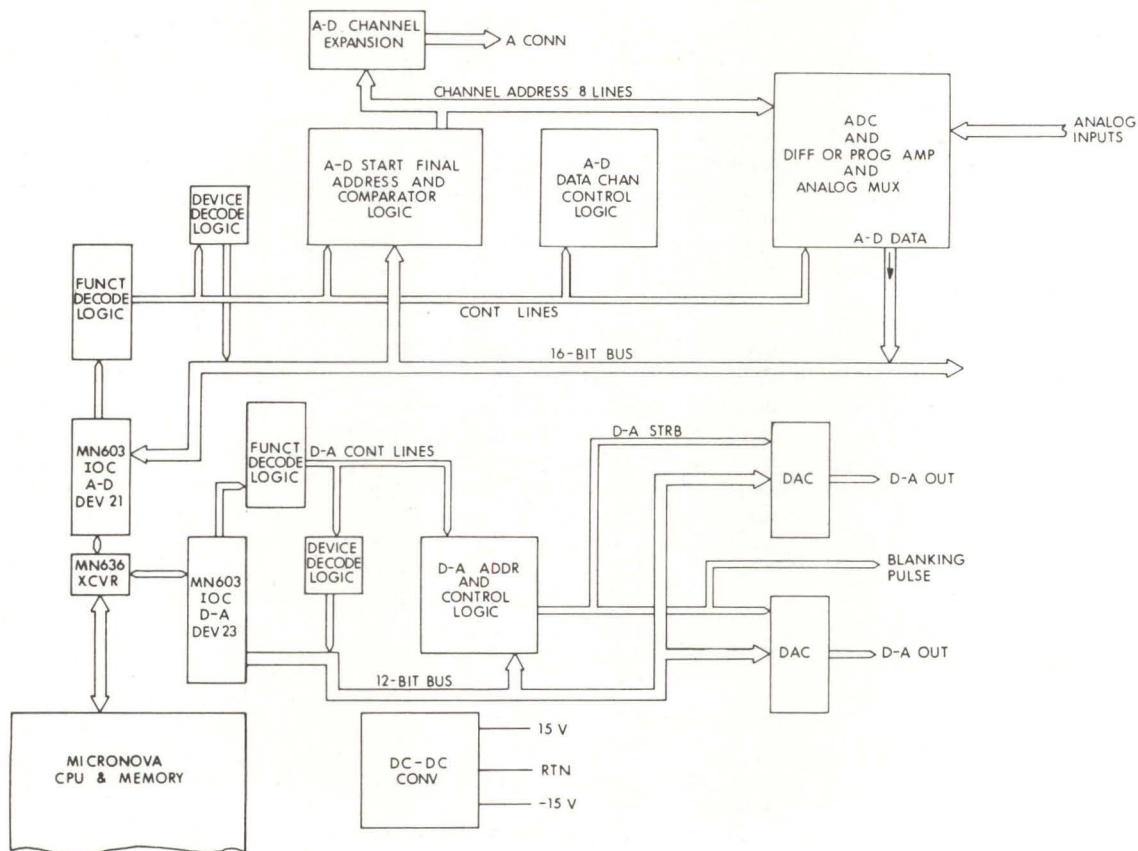
Three PC board layouts comprise the family, and may be varied to match a user's configuration and cost requirements. All measure 7.5 x 9.5" (19.1 x 24.1 cm). The high density microcircuit A-D and D-A components are manufactured inhouse.

The A-D/D-A master board accommodates up to 32 single-ended or 16 differential A-D channels with two optional D-A channels and a  $\pm 15$ -V dc-de power converter. The A-D is a successive approximation 12-bit converter.

Prices start at \$630 (single units) for 16 A-D channels. Add-on items such as additional A-D channels, ADC, amplifiers, and converter are priced separately.

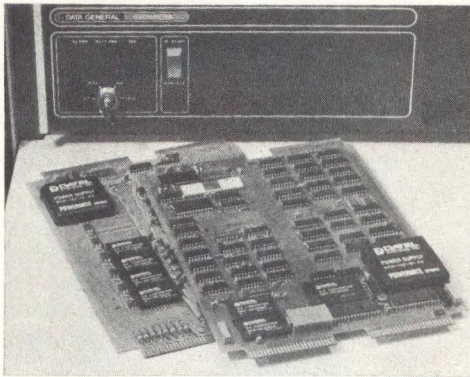
The A-D slave channel expander board, priced at \$345, acts as a slave under control of the A-D/D-A master board while adding 64 single-ended or 32 differential channels. Further expansion to 256 channels is available by cascading several of the boards inside the computer or by using the company's System 256 remote A-D/D-A housing and a controller-only version of the master board.

In addition to the master board's two D-A channels, a standalone peripheral offers four or eight 12-bit D-A



Sine-Trac A-D/D-A board is directly compatible with bus characteristics of microNOVA; it may be interfaced to all other Data General peripherals and software support offered for the microcomputer. Various component configurations are available, allowing 32 A-D channels, two D-A channels, dc/dc power converter, differential or programmable amplifier, and analog multiplexer. Datel supplies diagnostic paper tape program with board for teletypewriter printouts once analog signal connections are made





Datel's data acquisition package contains 32 A-D and two D-A channels on single board (right) that slides into Data General's microNOVA microcomputer, relieving user of the problem of designing and building hardware interface circuit and developing software programs. Optional peripheral is 4-channel, 12-bit D-A board with 15-V power converter (left), or 8-channel board requiring external  $\pm 15$ -V power. Optional A-D channel expander board, adding 64 channels, acts as a slave under control of master board

channels/board. The 4-channel board may include the optional  $\pm 15$ -V power converter, while the 8-channel version requires external  $\pm 15$ -V power; both have a 12-bit TTL port. Prices start at \$550 and \$785, respectively. The master board and D-A peripheral exclude certain Data General controller circuits which are available separately from Datel or Data General.

The master board aids signal conditioning with its offering of an optional differential instrumentation amplifier for fixed gains to 1000, and gain-programmable amplifiers. It operates with the company's software, as well as Data General's NOVA assembly language, BASIC, FORTRAN, DOS, RDOS, and programs for peripheral devices.

Interfacing is by register transfer, interrupt, or DMA to all microNOVA compatible peripherals. An included diagnostic program tape allows immediate teletypewriter printouts of analog input signals as soon as signal connections are made, applying it to all situations that require analog voltage I/O to the computer.

Designed to place A-D/D-A components and interface controller inside the computer, the board holds D-A sections with two extra latched digi-

tal bits per DAC. The bits may be used under program control. To achieve process system compatibility, an A-D channel used with a D-A channel permits the user to insert the computer in the control loop; in addition, 4- to 20-mA current inputs (common to process transmitters) are included. Optional onboard DACs can serve to calibrate the A-D section.

Hardware functions such as current and final channel address registers for the A-D section and a selectable clock for DMA mode relieve software requirements and increase throughput. Each A-D and D-A section appears as a separate I/O address in the microNOVA 6-bit peripheral address bus, and is referenced as such by the assembler mnemonics.

The A-D section features a 20- $\mu$ s throughput period, 12-bit binary resolution, 2's complement coding,  $\pm 10$ -V input range, and overall system accuracy of  $\pm 0.025\%$  of full-scale input range. Sample-and-hold aperture time is 50 ns with 12- $\mu$ s acquisition time and 8  $\mu$ s of A-D conversion. I/O transfer rates of 45k samples/s in DMA mode can be achieved. The D-A section has 12-bit accuracy with  $\pm 5$ - or  $\pm 10$ -V output ranges, 50-m $\Omega$  impedance, and drive of  $\pm 5$  mA.

Circle 400 on Inquiry Card

### Microcomputers for Data Communications Contain CCD Memory

Up to 256k bytes of low cost CCD memory are available in the 20 series communications processor, a Z80-based communications-oriented microcomputer system from Micom Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311. The memory interface implementation permits the CCD

to be accessed in the same manner as a floppy disc.

The processor is suited to the implementation of concentrators or contention units with four or eight channels, and single-channel converter systems between different communications protocols. The memory configuration enhances applications in large data environments, as well as CRT terminal controller uses requiring a large paging memory.

In a 2.5" (6.35-cm) high package, the unit can be equipped with up to nine synchronous and asynchronous communications interfaces, 6k bytes of p/ROM control firmware, 7k bytes of RAM buffer storage, and an operator's console consisting of LED status display and 10-position thumbwheel switch. This module permits diagnostic test and system monitoring. Additional RAM and p/ROM can be provided in custom configurations. Other features include an auto-restart timer, programmable realtime clock, and rear-mounted 25-pin connectors.

The processor normally is supplied in turnkey systems with firmware to perform communications network functions. Alternatively, it is available to OEMs with a program development system to facilitate firmware development.

Circle 401 on Inquiry Card

### Improved Language Augments $\mu$ Computer System Development

FORTAN, an applications language rather than a system-type language, allows a system designer to create software modules to solve problems that other microprocessor development languages cannot adequately handle. Applications requiring large amounts of detailed arithmetic computations are easily processed by FORTRAN-80, which meets and exceeds the ANS FORTRAN 77 language subset specification ANSI X3J3/90.


Intel Corp's Microcomputer Systems Div, 3065 Bowers Ave, Santa Clara, CA 95051 has developed the language to operate on Intellec<sup>®</sup> Series II models 220 and 230, and the MDS-800 and -888 development systems as well. Equipped with this problem-solving tool, the system can perform standalone FORTRAN processing, in addition to developing applications software for microprocessor-based systems. It is available in single- and double-density floppy diskettes at a price of \$1750 for single units.

Supporting the company's floating-point standard, the language has a complement of intrinsic functions including all trigonometric functions and absolute value. Formatted I/O is produced with FORTRAN and the ISIS-II run-time library to ease the problem of I/O handling.

The language produces relocatable and linkable object code that is compatible with both PL/M and 8080/8085 macro assembler. In addition, it supports full symbolic debugging with ICE-80<sup>™</sup> and -85<sup>™</sup>, and contains



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CIRCLE 89 ON INQUIRY CARD



sophisticated code optimization to ensure efficient compiled programs that use the least amount of memory.

Such benefits as reduced, concise codes; reduced program size; more power; greater reliability; and improved I/O handling are obtained from FORTRAN-80. A structured programming approach is supported by an if . . . then . . . else . . . if . . . else . . . end if construct. String variables also are permitted.

The language handles sequential and direct access files. It also implements internal file units for formatting and reformatting of data in internal memory buffers. Added error handling facilities permit a branch to a specified location if an error occurs.

List directed formatting enables a read or write without a format statement; data representation may be formatted, free formatted, or unformatted. Finally, this version supports logical or nonequivalence operators and permits arrays of up to seven dimensions.

Further extensions that have been added are logical operators, binary and hexadecimal integer constants; and ability to specify an integer or logical storage length of one, two, or four bytes. Besides these language features, the compiler facilitates program development. Multiple compilations of a main program and subroutines, similar to those of large-scale data processing systems, are performed together. Assembly language listings, as well as cross-reference, symbol attribute, and error listings, of any compiled program are produced to aid in debugging.

Circle 402 on Inquiry Card

### Microcomputers Solve Professional and Small Business Problems

System 88 is a line of personal computing microcomputers. Hardware, contained in three separate units, consists of a main unit using an 8080-processor and accommodating from one to three mini-floppy drives, an upper/lower case keyboard with control keys, and a quick updating video monitor. PolyMorphic Systems, 460 Ward Dr, Santa Barbara, CA 93111 is offering the system (excluding printer) for a starting price of \$2795.

With a flexible file system and built-in application aids, system software includes complete operating



Line of PolyMorphic Systems 88 microcomputers includes System 8813 consisting of processor, mini-floppy drives, keyboard, video monitor, and system software

software plus word processor, BASIC, and complete macro assembler on disc. BASIC has multidimensioned strings and numeric arrays, a plot statement to support graphics, variable cross-reference listing by line number, and inverse trig and hyperbolic functions. The text editor allows

the operator to move, copy, and delete blocks of text, search for specific strings, and exercise 2-dimensional cursor control. In addition, an integral RS-232 printer utility is already configured for several printers and can be adapted to others.

Circle 403 on Inquiry Card

### Single-Board Analog Output Systems Mate With LSI-11/ $\mu$ Computers

Two single-board analog output systems, designed to plug into the backplane of Digital Equipment Corp's LSI-11/2 microcomputer series, are available from Data Translation Inc, 4 Strathmore Rd, Natick, MA 01760. Both models, the 12-bit DT2766 and 8-bit DT2767, have four D-A output channels on a dual height card. Each DAC is fully buffered to avoid intermediate outputs. Four digital outputs are available for TTL control signals. All channels are powered directly off the computer's 5-V power through a highly regulated, low noise dc-dc converter.

Each board is shipped with test and calibration software for verified operation with the computer at the field site. The LSI-11/2, in combination with either model, forms a 4-channel analog output system. Applications include industrial and laboratory uses for computerized control and readout.

The 2766 offers 12-bit resolution and accuracy of  $\pm 0.012\%$  FSR, while the 2767 has 8-bit resolution and accuracy of  $\pm 0.2\%$  FSR. Differential linearity is  $\pm \frac{1}{2}$  LSB, gain and offset are adjustable to 0 for each channel, and settling time is 3  $\mu$ s to 0.01% FSR.

Circle 404 on Inquiry Card

### Disc Controller Formatter Interfaces Easily to Microcomputers

Designed to provide a cost-effective interface for microprocessor-based computer systems, the DCF10 hard disc controller formatter conforms to industry standard 2.5M, 5M, 10M, and 20M-byte disc drives. These drives may use an IBM 2315 or 5440 removable cartridge and up to three fixed platters.

Physically, the device is a 3.5" (8.9-cm) rackmount chassis package for low power dissipation, with no fan cooling required. Functionally, the controller can be divided into three parts: the computer interface, including address decoding; the drive controls, concerned with drive status and head position; and the data transfer portion for writing and reading.

The disc drive contains one or more platters with data recorded on both surfaces. The cartridge is organized into 200 or 400 cylinders, with each one containing two or more tracks with the same track number. Each track's data are subdivided into 24 equal sectors, and each sector has four main fields.

Sync field is the first. A 2-byte header field follows, which contains the cylinder, sector, and head address as well as a defective track flag re-



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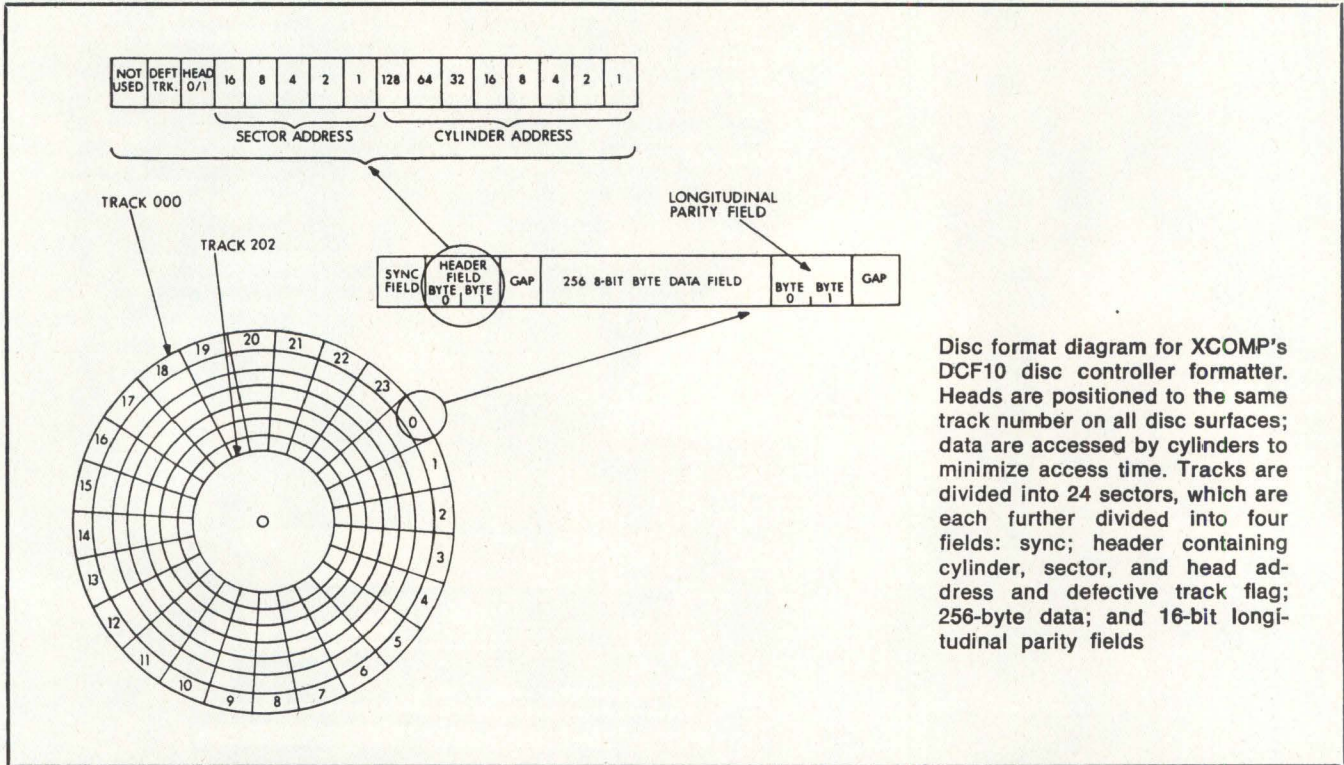


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CIRCLE 69 ON INQUIRY CARD





Disc format diagram for XCOMP's DCF10 disc controller formatter. Heads are positioned to the same track number on all disc surfaces; data are accessed by cylinders to minimize access time. Tracks are divided into 24 sectors, which are each further divided into four fields: sync; header containing cylinder, sector, and head address and defective track flag; 256-byte data; and 16-bit longitudinal parity fields

corded on the disc when a surface analysis program was run. This field is tested by hardware before a data transfer is started; a defective track or address mismatch aborts the transfer. Next is a 256-byte data field, and finally a 16-bit longitudinal parity field that the controller adds during a write operation; it is read at the end of a read operation to guarantee data reliability.

Controller and disc communicate through use of various processor instructions. Either a CPU memory DMA chip or buffer (with 256 bytes minimum) controls data transfers. The DMA must be assigned a high priority on the memory bus to meet the 310k-byte transfer rate.

The disc controller from XCOMP Inc, 7571 Convoy Ct, San Diego, CA 92111 utilizes random access, rotating memory disc drives to provide up to 40M bytes of storage on micro-computer systems. It operates up to four disc drives with simultaneous seek and overlapping seek/data transfer in multiple disc drive systems.

The controller bus, a byte-oriented i/o system used to communicate with the CPU, comprises eight bidirectional data lines, seven control lines, three test lines, and one initialize line. Data lines transfer an 8-bit byte of data between the processor and controller.

Communication over the bus is performed on a request/response basis where each sequence is processor-controlled. The design of the controller, which incorporates a universal 8-bit CPU interface, facilitates adaptation to any 8-bit computer. Circle 405 on Inquiry Card

### System Monitor for 8085 Microprocessors Is Hardware Connected

Examination and modification of memory locations and microprocessor registers at any point in an operating program through the implementation of addressable traps can be handled by the MICRO MATE-85 system monitor operating with a keyboard terminal. The operating program may be started or stopped at any location, or may be stepped one location at a time. With this tool from Spectrogram Corp, 385 State St, North Haven, CT 06473, both the microprocessor system development engineer and programmer may load or punch a paper tape of memory data for 8085 micro-processor systems that do not contain conventional peripheral i/o. Circle 406 on Inquiry Card

### S-100 Compatible Single-Board μComputer Holds 8k p/ROM, 8k RAM

Geared toward OEM users, the Little Brain I is a 6802-based single-board microcomputer that is S-100 compatible. Components include an 8-bit bidirectional data bus, 16-bit address bus, onchip 128 x 8-bit RAM, clock oscillator and driver, expandable interrupt system, and DMA capability. The board has onboard voltage regulators; fully buffered, TTL compatible data, address, and control buses; and a 128-word scratchpad memory. The 1.8-MHz crystal controlled timing assures accurate program execution and i/o operation.

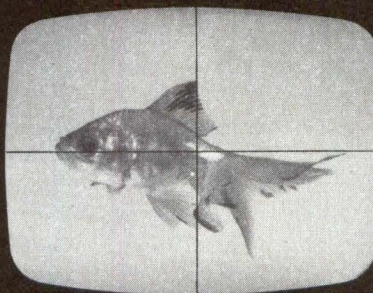
Program memory permits from 1k x 8 to 16k x 8 words of p/ROM to be installed on the processor board. UV erasable 2708, nonerasable 2708P, or 2716 type p/ROMs may be used; 7643 type fusible-link p/ROMs may be used in place of up to 8k of RAM. The 2114 type fully static RAM may be installed in 1k x 8-bit increments for an onboard capacity of 8k x 8 words.

Seven baud rates from 110 to 19.2k are switch selectable; 16 rates are available onboard through jumpers. The RS-232-C i/o features full- or half-duplex asynchronous operation



While the fish in the bowl darts about in front of a TV camera, cross-hairs on a video monitor track its constantly shifting centroid. The MAP-300 array processor — with 15 million floating point operations per second — follows the fish, continually processing digitized video data in real time. An I/O Scroll™ interfacing the TV camera inputs digitized video directly into the MAP at a rate of 4 million pixels per second. This goldfish and its TV-twin are the proof that even the most demanding real time array processing tasks are now possible . . . but ONLY with MAP.

Fast I/O Scrolls — input/output address processors — provide MAP's real time capability. They pull data directly into MAP and rush it to one of three independent memory



busses at transfer rates up to 40 megabytes per second. CSPI is delivering a full line of economical I/O Scrolls that interface a wide variety of peripheral devices to MAP. A torrent of data that would swamp any computer or other array processor can move directly through MAP like a fish through water.

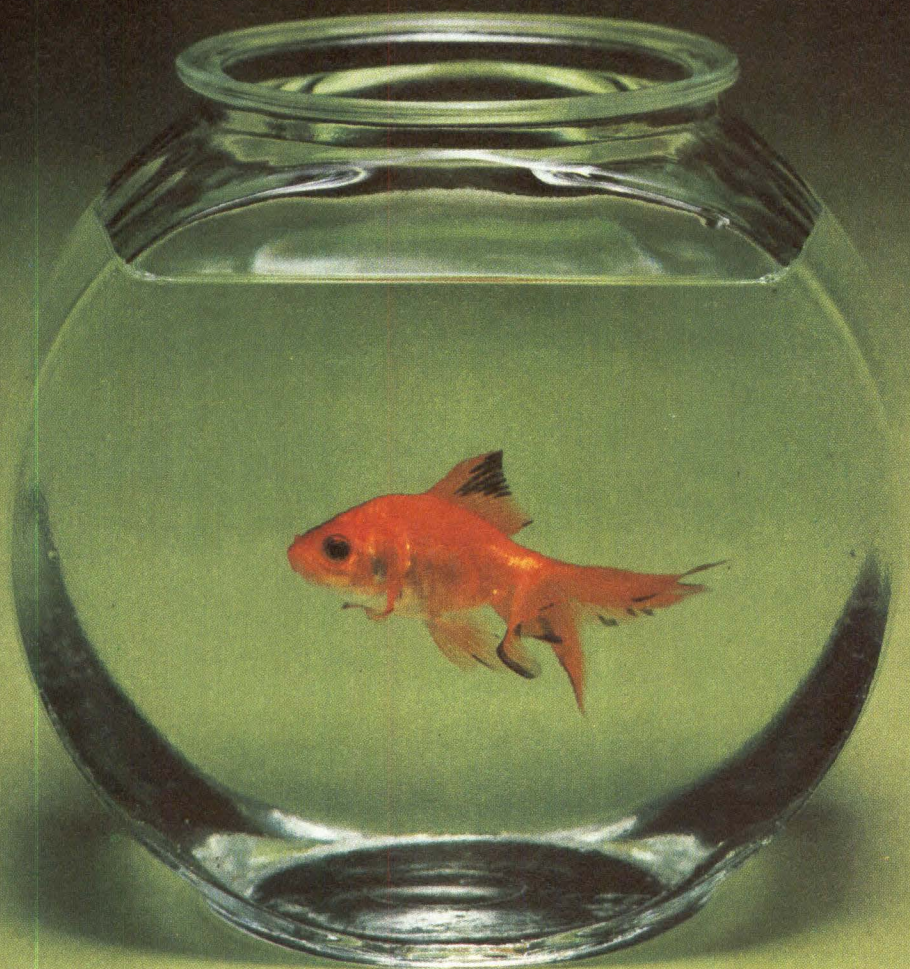
If you didn't catch our fish act at the IEEE Conference in Tulsa, talk to someone who did or ask for a demonstration yourself. Write to CSPI for references, technical specifications, pricing, and application notes on real time array processing.

**CSPI** CSP Inc.

209 Middlesex Turnpike  
Burlington, MA. 01803  
(617) 272-6020

# What can a goldfish tell you about Array Processing?

**MAP™ is the only Array Processor that functions in real time...all the time.**



CIRCLE 70 ON INQUIRY CARD



**MODCOMP Classic. A lot of computer. But not a lot of money.**

Our new MODCOMP Classic costs less than any other super mini. Yet, in benchmark tests, it's outperformed the best of them. The reasons?

- A super fast floating point processor.
- 7 MAP files and 240 registers for lightning fast context switching.
- Unique multi-word architecture.
- MOS or core memory with effective cycle times as low as 125 nanoseconds.
- An enhanced Fortran oriented instruction set.
- I/O processors that can handle up to eight million bytes per second.
- An optional communications processor

which provides a multiplexed direct memory path for up to 256 full duplex lines.

- And a CPU that can execute many instructions in 200 nanoseconds.

**Built to save you the biggest expense of all — downtime.**

The Classic features our exclusive wire-wrapped PC boards that are more reliable and easier to service than soldered boards. Hardware diagnostics and test connectors that allow you to test all components quickly. And PC boards that plug in and out for fast replacement.

You also get our product development tools to help you get your system up and running fast. And our service and support to keep your system running, successfully.

**A complete family of computers. Plus field-proven software.**

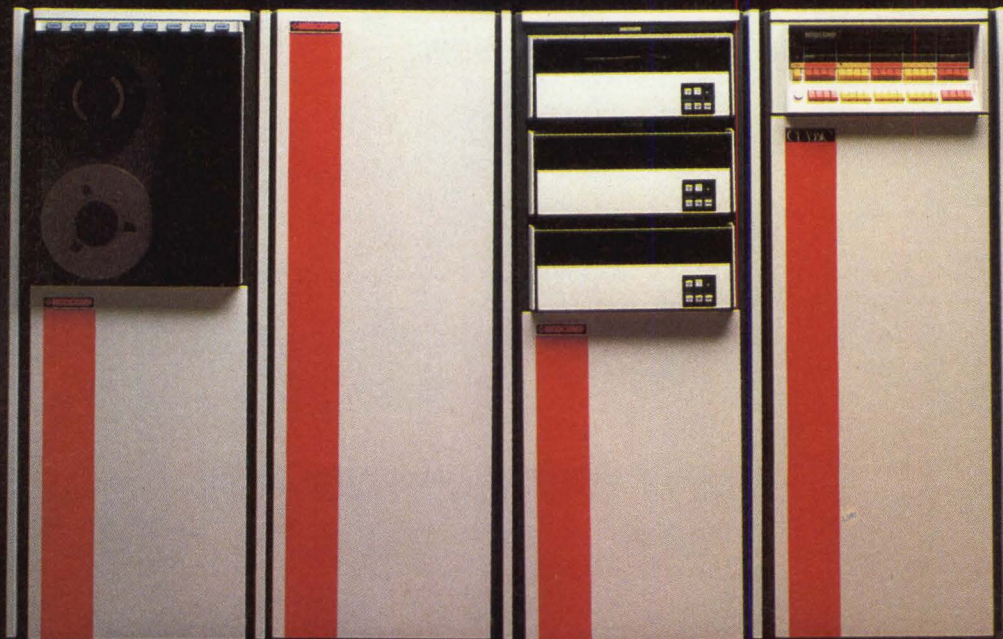
Classic is a complete family of computers. Supported by a full complement of peripherals, process I/O interfaces and software operating systems. And it's upward compatible with all MODCOMP computers.

Whether you're a computer user or an OEM, if you're thinking about buying or expanding a computer system, consider cost/performance, reliability and ease of implementation.

And consider Classic. Because it will probably be your first choice on all three counts.

Send for our MODCOMP Classic brochure.

**When you put a name like  
Classic on a new computer, you've either  
got a lot of nerve. Or a lot of computer.**



**CLASSIC / MODCOMP**  
Dedicated to your success

Modular Computer Systems, Inc., 1650 W. McNab Road, Ft. Lauderdale, FL 33309 • Phone (305) 974-1380  
See the MODCOMP Classic at booth # 1507 during the 1978 National Computer Conference.

CIRCLE 71 ON INQUIRY CARD



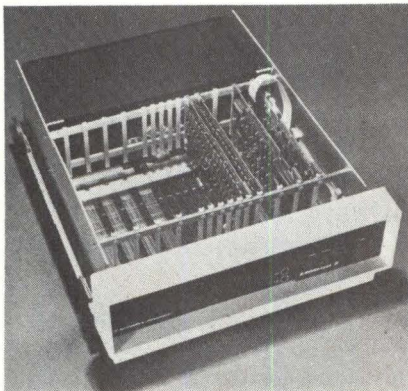
and automatic parity generation and checking. Other specs include power requirements of 8 Vdc at 1.6 A (max) and 16 Vdc at 100 mA, operating temperature of 1 to 70 °C, and 98% relative humidity.

BPI Electronics, Inc, 4470 SW 74th Ave, Miami, FL 33155 has added a monitor that operates through the RS-232-C I/O channel permitting operation with most CRTs, hardcopy terminals, and computers. Multidrop operation permits up to 1000 boards to operate on the same I/O line. Each board receives and retransmits characters to the next terminal; the selected station then interprets incoming characters as commands. Command mode is terminated by an escape sequence. Error messages are transmitted for parity and framing errors, as well as receiver overrun.

Custom programming services are available. A fully socketed version with 2k monitor/debug program and 1k words of RAM sells for \$395. Circle 407 on Inquiry Card

### µComputer Development Tool Operates in Dual Memory Map Mode

EXORciser II, an extended version of the EXORciser Development System, offers capabilities needed to design and develop high performance microcomputer systems based on the M68BXX series of 2-MHz chips from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. The system directly supports designs



Motorola's EXORciser II consists of two modules, power supply, and 14-slot chassis which holds PC board modules necessary to user to emulate microcomputer system hardware. Development system contains motherboard, data and address buses, and RS-232-C port

of 1.5-MHz M68AXX and 1.0-MHz M6800 series.

With this tool, the user is able to communicate with systems, load programs, monitor the execution of programs in real time, and isolate and analyze hardware and software problems. Optional modules allow configuration of the company's other microprocessor and microprogrammable families.

Dual memory map mode of operation allows full use of the complete microprocessor addressing map. With this feature, emulation and debugging of the user's system can be achieved more completely since memory in the 65k-byte map does not need to be allocated to the EXbug 2 program, which resides in its own 65k-byte map. It may also reside in the user's memory map.

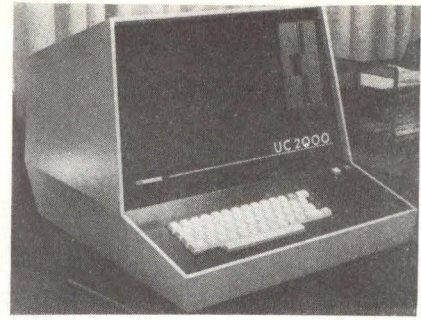
Optional modules are provided with a jumper arrangement for assigning memory and peripherals to either map in the dual map mode, or to any page in extended memory systems. A 20-pin connector on certain modules offers additional flexibility for implementing priority interrupts, multipaged memory and I/O systems, parity error detection, and power down restart.

The basic unit consists of MEX6800-2 MPU II with timer and priority interrupt controller, and MEX 68DB2 Debug II modules, power supply, and 14-slot chassis with cover to accommodate emulation PC board modules. A motherboard provides power and signal connections to the microprocessor control, data, and address buses, and an RS-232-C port facilitates communications with peripherals. The module supplies eight selectable baud rates, from 110 to 9600 bits/s, and serves as the communications link between EXbug 2 firmware and the user's terminal.

Circle 408 on Inquiry Card

### Microcomputer Uses Plug-in Cards to Achieve Application Flexibility

The S-100, 8080-based UC2000 microcomputer system is available in five configurations (A to E) which range from a mainframe card rack to a complete system with CPU, memory, multiple floppy disc, and printer. Although systems B through E are supplied with an 8080-based computer, any S-100 compatible computer



can be used in the A system version, thus suiting it for industry, business, and hobby applications. Prices start at \$995.

The 54 x 48 x 39-cm console is provided with a 12-MHz, 30.5-cm CRT which has a 7 x 9 matrix upper/lower case alphanumeric font, 96 ASCII character set, and 64-char x 16-line display. The 8-card slot mainframe can hold up to 64k bytes of RAM. The standard system is supplied with 8k bytes. Also included are an 18-A power supply, axial blower, and 56-key ASCII unit with various keyboard options.

Plug connections on all subsystem modules facilitate maintenance. An IEC approved emi filtered power connector is standard; DB25 type connector slots are provided on the rear panel for peripheral interfacing. A 230-V, 50-Hz power option also is available.

Infinite, Inc, 1924 Waverly Pl, Melbourne, FL 32901 has developed a special built-in program that electronically replaces the function of many mechanical switches, thereby reducing the operating controls required. Extensive software is available for the system.

Circle 409 on Inquiry Card

### µProcessor Development System Communicates With Host Mainframe

Microprocessor design teams that use development software stored in a large mainframe computer can now use the 8001 or 8002 microprocessor development systems from Tektronix, Inc, PO Box 500, Beaverton, OR 97077 as work stations communicating with the central mainframe over standard RS-232 lines. The added software feature allows downloading of source data from the host computer operating system and uploading of data from the development units to the host.

Users will be able to implement the 8001 as a work station; software development capabilities that it lacks may be supplied through the user's



own program. Another alternative is to link 8001 stations to an 8002 to access the capabilities of the 8002.

A central design data base also may be shared among several units operating as design work stations. Programs designed for one micro-processor system can be borrowed for another system under development; they can be tested, debugged, modified, or expanded using the 8002 to operate on the new system. Separate hardware/software teams working on the design of a common system can interact through the central computer, thus saving time and increasing the chance of an optimum design solution.

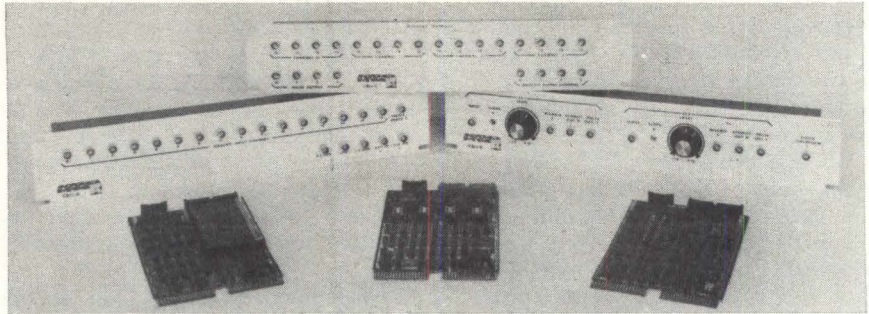
This program is a standard feature of the 8002. To operate it, the user must enter a simple program in the mainframe computer. The necessary program listings and operating instructions for several computer operating systems will be supplied.

An updated processor emulator module that supports the Intel 8085A microprocessor also has been announced for both development systems. When inserted into the system, the card may be used to develop, edit, and test software for the 8085A. Using the prototype control probe, the finished breadboarded system may be connected to the development system for in-circuit emulation, in real time, of the complete hardware/software prototype. The systems now support the Intel 8080A and 8085A, Motorola 6800, Texas Instruments TMS 9900, and Zilog Z80 microprocessors and their appropriate second sources.

Circle 410 on Inquiry Card

### Realtime Clock, A-D and D-A Converters Are LSI-11 Compatible

Three types of data acquisition cards, compatible with the LSI-11/2 and LSI-11, are the ADC11, a 16-channel, 12-bit ADC; the DAC11, a 4-channel, 12-bit DAC; and the DRTC11, a programmable realtime clock. All are functional supersets of similar Digital Equipment products, but are in the dual width format; they plug into the LSI-11 backplane. Andromeda Systems, Inc, 14701 Arminta St #J, Panorama City, CA 91402 has introduced compatible connector boxes (CB11 series) which facilitate external connection to these cards.



The ADC card has 16 multiplexed inputs (eight differential inputs may be special ordered). Its conversion rate is 20  $\mu$ s/channel (50 kHz). Operational modes are auto-sequence, burst, and truncation. Full rate conversions independent of the CPU program speed are due to the 16-word FIFO data buffer.

Providing remote ground sensing, each of the four analog output channels of the DAC card has a 12-bit DAC that settles to  $\pm 1/2$  LSB in less than 3  $\mu$ s. There also are 16 digital control outputs (4/channel) and four pulse outputs (1/channel).

Methods for generating and measuring time intervals, counting events, and determining the frequency of a signal are provided by the counter/timer. It interrupts the LSI-11 at programmed intervals or on detection of an external signal via its two Schmitt trigger inputs that may be set to trigger on a positive or negative transition between  $\pm 12$  V. There are 13 internally generated rates ranging from 1  $\mu$ s to 1 h, and five operational modes: single interval, repeated interval, event time from trigger, event interval time, and frequency count.

Circle 411 on Inquiry Card

### Minicomputer-Based Software Improves Microprocessor Design

By using computers more powerful than the microprocessor that is incorporated in a system design, OEMS can experience higher speed, larger memory, more powerful editing capability, and higher speed peripherals of a host computer during the design phase. OEMS using S2000, S6800, and S9900 microprocessors of American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 can obtain minicomputer-based software from The Boston Systems Office, Inc, 400-1 Totten Pond Rd, Waltham, MA 02154.

The software includes cross assemblers, relocating cross assemblers, cross linkage editors, and simulator-debuggers. It is written in host CPU assembly language for the DECsystem10, DECsystem20, PDP-11, and Data General Nova, SuperNova, and Eclipse.

The exact instruction set of the microprocessor is used on the minicomputer. An unlimited-size block of instructions can be written as a single macro-instruction. Conditional assem-

bly instructions permit several versions of the program to be generated using a single source file.

Error messages are displayed on the terminal and are placed in the listing file. The assemblers generate dummy object code for correction when errors occur. The ASCII object file can be in AMI standard hexadecimal, relocatable, or other formats permitting the files to be downline loaded directly into RAM or p/ROM.

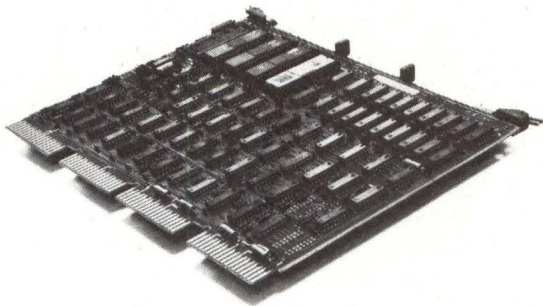
Circle 412 on Inquiry Card

### Linearizing ADC Interfaces With 8-Bit Microprocessors

Handshaking between 8-bit microprocessors and the company's series 100 analog scanner line, the SL110 linearizing A-D converter employs a byte serial architecture to enable a processor to command and interrogate up to 160 channels of data along a single, bidirectional, 8-bit data bus. The converter is designed by the San Diego Instrument Laboratory, 7969 Engineer Rd, San Diego, CA 92111



# Nice going, DEC<sup>®</sup>

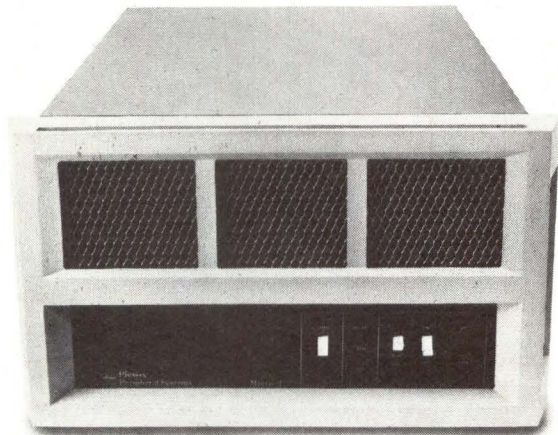


## DEC's microcomputer

DEC's LSI-11<sup>®</sup> has been called the world's most powerful 16-bit microcomputer, and we wouldn't argue with that at all.

Good show, DEC.

®Registered trademark of Digital Equipment Corporation



## Plessey's Micro-1

In fact, we like DEC's micro so much that we turned it into a mini and named it the Plessey Micro-1.

The Micro-1 consists of a DEC LSI-11 combined with a Plessey Unibus<sup>®</sup> converter and Plessey backplanes, memory controller and interfaces, packaged in either a 5¼" or 10½" rack-mount chassis.

The Plessey Micro-1 has the full instruction repertoire of the PDP-11/34<sup>®</sup> (more than 400 instructions), supported by DEC's RT11 operating systems and diagnostic software. You can mix Q bus<sup>®</sup> and Unibus interfaces and peripherals; use DMA from your floppies and discs; and think what you can do with the multi-level priority interrupt structure.

All this minicomputer performance is available at microcomputer prices. And we're shipping now.

Values like these have made us the largest independent supplier of DEC-compatible peripherals. Our product line presently includes add-in/add-on core and semiconductor memories, cartridge disc systems, floppy disc systems, mag tape systems, complete computer-based systems, and a wide variety of backplanes, expansion chassis, and other accessories.

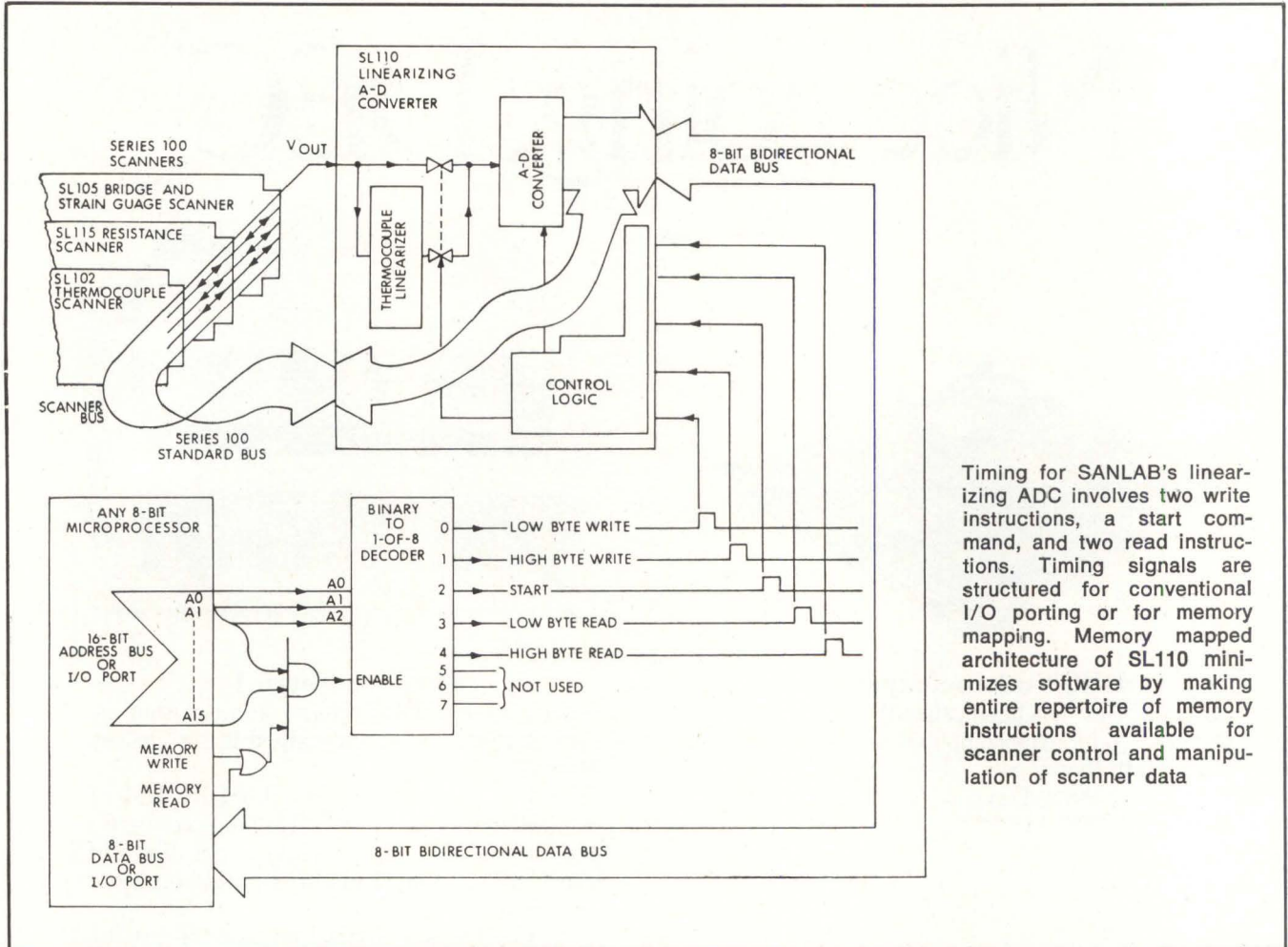
We're the only real alternative to DEC, a complete single source. For all the details, please contact the nearest Plessey sales office today.



## Plessey Peripheral Systems

17466 Daimler, Irvine, California 92714, (714) 540-9945





Timing for SANLAB's linearizing ADC involves two write instructions, a start command, and two read instructions. Timing signals are structured for conventional I/O porting or for memory mapping. Memory mapped architecture of SL110 minimizes software by making entire repertoire of memory instructions available for scanner control and manipulation of scanner data

to store and load processor commands into the scanners, initiate scanner sampling, linearize and digitize the resulting outputs, and store the results in onboard memory for processor retrieval.

Linear and nonlinear modes are bit selectable. When activated, an on-

board thermocouple linearizer provides special functions accurate to within 0.1% of full scale for scanner signals. Sample rates up to 40 channels/s are available.

Features include a 3-state I/O structure, TTL/CMOS compatibility, choice of direct bus connection or porting

through peripheral interface devices, and memory mapping. Output data are provided in binary engineering units and bit selectable temperature scales in Celsius or Fahrenheit. The \$445 unit plugs into a standard 6.25" (16-cm) card slot on 1" (2.5-cm) centers. Circle 413 on Inquiry Card

### Multiple Port Computer Functions Alone or as Frontend Processor

Asynchronous communications at selectable rates from 110 to 9600 baud, and synchronous communications at rates in excess of 50k baud are enabled by the MM1-MSK single-board computer with four serial I/O ports. Said by Control Logic, Inc, 9 Tech Circle, Natick, MA 01760 to be the first such computer to provide multiple serial communications ports, it is

supplied with a Z80 CPU that has 1k bytes of 2708 EPROM, or 2k bytes of 2716 EPROM and 1280 bytes of RAM.

Interrupt capability is provided upon receipt of data from all four ports, as well as three external interrupt states. Compatible with the company's MM1 microcomputer line, the board can be used as a frontend communications processor for a general-purpose microcomputer system as well as a standalone single-board computer.

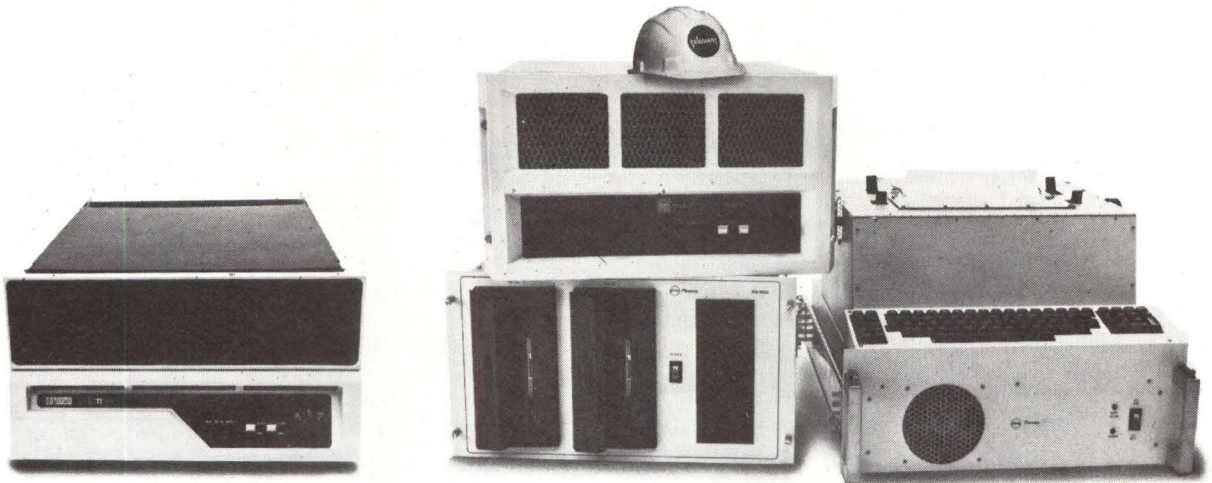
Circle 414 on Inquiry Card

### Development System Supports Z80 $\mu$ Processor Design

A 2-chip method is incorporated by Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 in the ZDS-1/40 development system to reduce problems inherent with connecting the user's system to a development system, and to allow precise emulation to clock frequencies of 4 MHz. Realtime emulation is achieved by using two microprocessor circuits—a Z80-A CPU in-



# We're getting tough with DEC<sup>®</sup>



## The PDP-11/34<sup>®</sup> by DEC

The DEC PDP-11/34 is fast and powerful. Standard features include stack architecture, multi-level vectored interrupts, hardware multiply/divide and memory management, DMA and a powerful set of over 400 instructions.

And a broad range of hardware and software options make it an even better value for today's systems.

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## The PM 1150/RP Ruggedized Processor

We've ruggedized the computer power on the left to make it adaptable to a wide range of environmental conditions. These include ships, vans and rigorous test and industrial control applications.

The PM 1150/RP withstands vibrations up to 1.7 G from 5 to 150 Hz and shocks up to 8 G. Optional ruggedized peripherals include a dual floppy disc system and an 80 column daisy-wheel printer. And the 1150/RP is priced much lower than you would expect.

Adding value to minicomputers has made us the largest independent supplier of DEC-compatible peripherals. Our product line presently includes add-in/add-on core and semiconductor memories, cartridge disc systems, floppy disc systems, mag tape systems, complete computer-based systems, and a wide variety of backplanes, expansion chassis, and other accessories.

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served into the prototype system and a second Z80 CPU inside the development system. The standalone hardware and software design tool supports development of Z80- and Z80A-based microprocessor systems, and will be able to support upcoming Z8 and Z8000 products.

The 4-MHz emulator is offered together with the development system for \$11,690 or as a factory-installed option ZRTE for \$2750 to upgrade users' existing ZDS/U development systems to accommodate 4-MHz components. Emulator hardware features include a thick-film hybrid version of the Z80A CPU with the same timing and ac characteristics. The emulator inserts directly into the user's system via a 6-ft (1.8-m) flat cable.

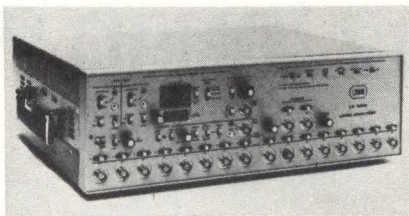
Features include memory mapping and protection in 1k-byte segments, user memory refresh, verification of user clock integrity, and detection of memory access to nonexistent or write protected blocks. A disc-based software package provides user debug and initialization commands, which set the mode of emulation, and display and edit the memory map.

The standard development system includes 32k bytes of main memory with capacity of up to 65k bytes on a single board. In addition, it offers an RIO operating system with relocating assembler, linker, text editor, and logical file structure; floppy disc drives that each hold up to 300k bytes of storage; and programmable breakpoint module that enables monitoring and testing of specific address, data, and control bus states to stop program execution or create a scope sync. A programmable realtime storage module enables recording of address, data, and control bus lines for selected operations; and I/O ports may be accessed when user mode or user clock is selected.

Circle 415 on Inquiry Card

### 50-MHz Analyzer Displays Multiple Channel Data for 16-Bit Systems

The model LA1850 logic analyzer provides 18 channels of 150-word deep unlatched or latched data storage, plus three additional qualifiers, suiting it to 16-bit computer systems that require display of several channels of information besides the data/



address lines. Operating at speeds up to 50 MHz, the unit features an integral display formatter that allows a user to study timing or mapping displays, or binary, hexadecimal, or octal data on any oscilloscope or monitor.

Features include a separate 510-word reference memory for comparisons, positive or negative logic formatting, cursor and trigger markers, synchronous and asynchronous capturing of signals, and dual thresholds with ECL, TTL, and variable settings. Trigger capability overcomes false triggering on 3-state logic buses and lengthy software loops.

The 5.25 x 16.65 x 13.95" (13.3 x 42.3 x 35.4-cm) unit is supplied by EH International, Inc, 515 Eleventh St, PO Box 1289, Oakland, CA 94604 with 18 miniature clip-on probes. Price is \$6100. Optional trigger pods can provide up to 40 additional qualifier inputs.

Circle 416 on Inquiry Card

### Expandable $\mu$ Computer System Contains Variable Format Display

The SEVEN-X microcomputer system, which gives flexibility to the OEM, includes a display processor that easily handles formats of up to 132 columns, and permits direct display of line printer-oriented data. Display parameters can be modified in real time by software. Dense text, bold messages, and bit-map graphics are exhibited in different windows of the same display. ECD Corp, 196 Broadway, Cambridge, MA 02139 provides extensive software utilities for development support and incorporation into the end product.

Standard keyboard comes with relegendable keycaps. OEMs can modify software tables in the keyboard handler utility to alter key functions. Codes generated by different shift states can be altered independently by software.

Each system is equipped with an external I/O bus driver, which can be

daisy-chained to up to 10 peripheral devices. The system is easily interfaced and expandable. A central system bus can support up to 12 displays and 16 fully independent processors. A single stack can hold up to 1M bytes of RAM.

The basic system consists of a 16k central processor, a display processor, and a general I/O and system support board. It is supplied in an enclosure with a power supply and one expansion slot.

Circle 417 on Inquiry Card

### Committee Scrutinizes Necessity for Microprocessor Standards

Possible standards on microprocessors will be studied and identified by a group (X3/SPARC/MICRO) being organized within American National Standards Committee X3, which is responsible for developing standards on computers and information processing. Administrative secretariat is the Computer and Business Equipment Manufacturers Association (CBEMA), 1828 L St, NW, Suite 1200, Washington, DC 20036.

A number of general-purpose X3 standards already published or under development may be applicable to microprocessors, such as those on Minimal BASIC, magnetic tape cassettes, and flexible discs, or they may require adaptations to be useful for microprocessor applications. A proposed scope, work program, and completion timetable will be drafted for each standard that the group finds needed and feasible.

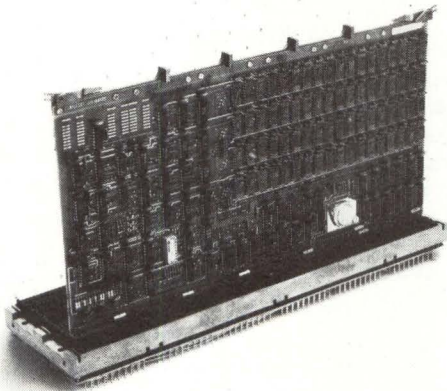
Both users and producers of microprocessors are being sought. Interested persons may contact group chairman Donald Feinberg, principal software engineer with Digital Equipment Corp, 146 Main St, Maynard, MA 01754, for further information.

### Online Program Debugger Enhances Multiuser Development System

Users can increase efficiency for writing and debugging programs with DEBUG which operates in conjunction



# DEC<sup>®</sup> never had it so good



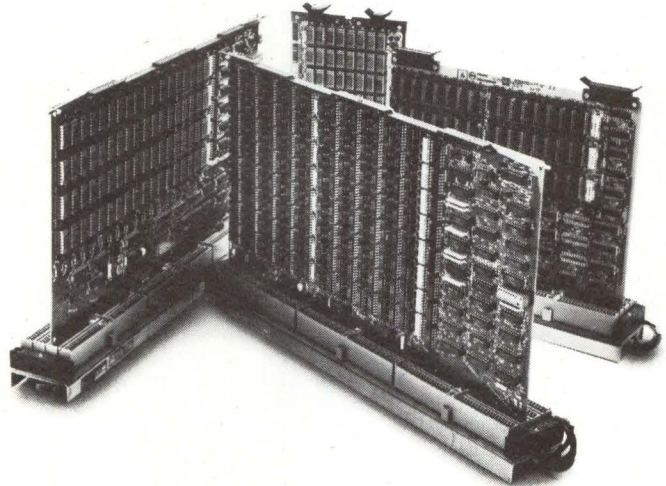
## **DEC's semiconductor memories:**

If you want to, you can always buy semiconductor memories for your DEC mini's from DEC.

But they tend to be bulky (16K bytes to a board for some mini's and *five* boards for their ECC unit).

And you probably already know about DEC's pricing structure on additional memory.

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## **Plessey's:**

We offer a complete family of DEC-compatible semiconductor memories.

64K, 128K and 256K bytes (with ECC) for the DEC PDP-11<sup>®</sup> series. 128K words for the PDP-8A<sup>®</sup>. And 64K bytes for the LSI-11<sup>®</sup>, PDP-11/03<sup>®</sup> and our own Micro-1.

Our plug-compatible memories cost less and run faster than DEC's. Reliability is ensured through 100% component burn-in and 100% board testing. Each and every memory is then run in the minicomputer it was designed for before we ship it out the door.

This kind of care has made us the largest independent supplier of DEC-compatible peripherals. Our product line presently includes add-in/add-on core and semiconductor memories, cartridge disc systems, floppy disc systems, mag tape systems, complete computer-based systems, and a wide variety of backplanes, expansion chassis, and other accessories.

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CIRCLE 74 ON INQUIRY CARD

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**MULTIPLE  
OUTPUT**

**OPEN  
FRAMES**

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IS NO.1 FOR...**



**Reliability:** Every unit — 2 hour burn-in plus 2 full functional tests.

**Quality:** Two-year warranty. U.L. Recognized, CSA Certified.

**Delivery:** "Off-the-shelf" — Nationwide.

**Variety:** 25 multiple output models in 9 different case sizes in 4 basic series...

**Dual Output:**  $\pm 5V$  to  $\pm 24V$ , 0.4A to 6A; tracking outputs,  $\pm 0.02\%$  regulation.

**Triple Output:** 5V and  $\pm 9V$  to  $\pm 15V$ , 0.2A to 12A, OVP on 5V outputs, 115/230 VAC input.

**Floppy Disk:** Four new triple output models for floppy disk memory applications.

**Microprocessor:** Dual, triple, and quad output models for microprocessor based systems.

And still at the same 1973 prices

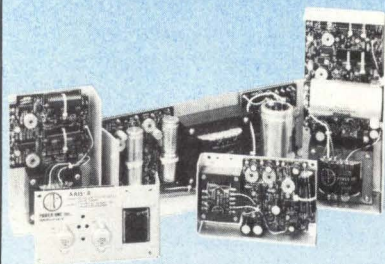
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Power One Drive • Camarillo, CA 93010  
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**MICRO PROCESSOR DATA STACK**

with MUTE release 2.1 of MuPro Systems Div, 424 Oakmead Pkwy, Sunnyvale, CA 94086. For use with the 80DOS microprocessor development system, the debugger offers breakpoints, display, modify, control, trace, and address calculation capabilities. Interuser protection is provided by allowing each user to prohibit program access to areas outside its memory boundaries.

Up to 10 fast and emulation breakpoints may each be set. Fast mode allows the program to be run at full speed, software emulation mode allows use of emulation breakpoints and trace of the last 128 instructions executed, and step mode allows the user to specify a number of instructions that are to be executed in emulation mode.

Display may be in hexadecimal, decimal, octal, binary, or disassembled source code. The debugger is supplied in functional modules with both the source code and relocatable object code included.

Circle 418 on Inquiry Card

**Self-Contained System  
Offers Powerful  
Microcomputing Ability**

The General microcomputer system from Technical Design Labs, Research Pk, Bldg H, 1101 State Rd, Princeton, NJ 08540 is based on the 4-MHz Z80-A processor. It contains a 32k x 8 dynamic RAM (128k capacity), a micro floppy disc drive with 350k-byte capacity, and 80 x 25 lines of video with upper/lower case, blink, reverse video, half and zero intensity, protected field, and graphics with special characters. Also built in are a 22-MHz, 800-line monitor and standard 77-key keyboard with numeric entry pad and special function keys.

Among the features are an interrupt controller, 4-channel DMA control, four memory mapping registers, and dedicated i/o ports with separate connectors. Up to 64k of ROM may be placed in the system; both video and graphics RAMs are separate. Software definable character sets are optional. An operating system in ROM, the company's DISK BASIC, and word processing software come with the computer.

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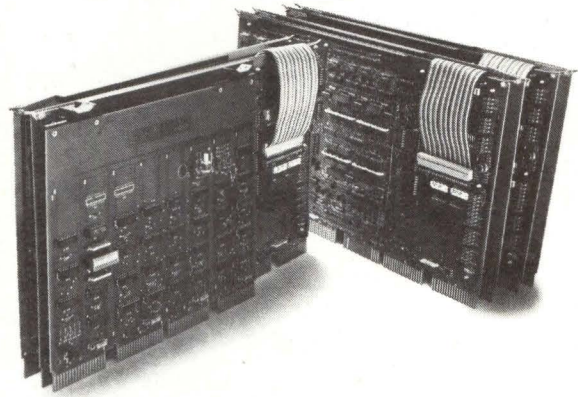


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## Semiconductor Memory for 6800 System Is Easily Expandable

CI6800, a 16k x 8 semiconductor memory system, is designed for operation with Motorola's EXORciser<sup>®</sup> and MC6800 evaluation module. By interchanging the 4027 4k x 1 dynamic memory chip with a 16k equivalent, the memory is expandable to 32k, 48k, or 64k with no further modifications. The board from Chrislin Industries, Inc, Computer Products Div, 31312 Via Colinas, #102, Westlake Village, CA 91361 plugs directly into existing EXORciser connectors. Data access time is 300 ns and cycle time is 750 ns.

Circle 420 on Inquiry Card

## μProcessor Power Supply Features Floating Multiple Outputs

A line of high performance power supplies, announced by Acopian Corp, 131 Loomis St, Easton, PA 18042, includes dual and triple output models which provide 5-, 9-, 12-, and 15-V outputs, with output current ratings to 6 A. All outputs are floating, and may be connected in either polarity.

Line and load regulations are ±0.15% for most models; ripple, 1 mV rms. Standard input is 105 to 125 Vac, 50 to 400 Hz. Two types of case construction are available.

Circle 421 on Inquiry Card

## 6800 BASIC Interpreter Is Optimized for Industrial Applications

The 6800 4k BASIC interpreter from Wintek Corp, 902 N 9th St, Lafayette, IN 47904, having such features as rapid coding and debugging, easy maintenance, and advanced control structures, is oriented toward process control and monitoring. It features control of interrupts, direct memory R/W, assembly language subroutine, and flexible I/O.

The interpreter may reside in RAM or in p/ROM for instant power-on operation. If the BASIC program also is stored in p/ROM, the interpreter immediately enters run mode, allowing unattended operation. Cassette and p/ROM versions are available.

Circle 422 on Inquiry Card

## CPU Board and Microcomputer Are F8-Based Components

Two F8 products targeted for the serious hobbyist and design engineer have been introduced by Comptronics, 19824 Ventura Blvd, Woodland Hills, CA 91364. The first is an S-100 bus compatible, F8 CPU board, model F8S100, complete with 3850 CPU and 3853 static memory interface. The unit provides sockets for 2k of EPROM monitor, two processor I/O sockets, and connections for six I/O ports. The board has 64 bytes of scratchpad RAM, and a fully buffered data bus.

The second product, model KD80, is an F8 microcomputer with keyboard and 6-digit display. It provides an audio interface and speaker compatible with the onboard KD-BUG (3856) music routine, 2k of RAM expandable through an S-100 connector, and 1k of EPROM with four additional 2708 sockets.

Circle 423 on Inquiry Card

## Z80 CPU Board Operates With 8080 Software Without Modification

Offering the Z80 CPU board either assembled or in kit form, Vector Graphic, Inc, 790 Hampshire Rd, Westlake Village, CA 91361 has incorporated a blocked design with on-board state select. The board is jumper-selectable for operation at 2 or 4 MHz and has fully buffered Z80 lines. Operation with standard 8080 software occurs without modification.

Circle 424 on Inquiry Card

## High Density, Wirewrap Boards Serve Separate μProcessors

Designed to provide design flexibility in circuit layout and interfacing, two high density, prepinned microprocessor Wire-Wrap<sup>™</sup> panels have been announced by Hybricon Corp, 410 Great Rd, Littleton, MA 01460 for the Intel SBC-80/10 and Zilog Z80. For the SBC-80/10, the 2-8010A has 62 rows of 52 contacts, each on a 0.100 x 0.100" (0.254 x 0.254-cm) grid pattern with plated through holes. I/O holes for up to three 50-pin flat cable connectors are contained at the

top of the board. The 6.75 x 12" (17 x 30.5-cm) panel has two ground planes and 10 independent power buses.

The 2-Z80 board features 36 columns of 59 plated through holes on a 0.100 x 0.100" (0.254 x 0.254-cm) pattern; both boards can hold any combination of IC DIPS from 8 to 40 pins. The Z80 panel has a double row of 47 contact holes on 0.100" (0.254-cm) spacing at the top for mounting flat cable connectors. Measuring 7.70 x 7.50" (19.6 x 19.1 cm), it combines six power and ground planes. Documentation kits are optional for both boards.

Circle 425 on Inquiry Card

## 8-Channel Serial I/O Module Is EXORciser Compatible

The 9650 asynchronous serial interface module is pin and outline compatible with the Motorola EXORciser<sup>™</sup>, Micromodules<sup>™</sup>, and MEK-6800D2 evaluation kit. It features full address decoding and fully buffered data, address, and control lines, occupying 16 consecutive memory addresses. Creative Micro Systems, 6773 Westminster Ave, Westminster, CA 92683 includes eight MC6850 asynchronous communications interface adapters with full RS-232-C signal conditioning. An onboard bit rate generator simultaneously provides 14 standard rates that can be strapped individually to each ACIA.

Circle 426 on Inquiry Card

## Microprocessor Handles Communication Protocols In Optical Readers

An Intel 8085 has been added to the series 4000 readers by Chatsworth Data Corp, 20710 Lassen St, Chatsworth, CA 91311 to handle different communications protocols. A minor change of program EPROM can upgrade a user's system. The three models are the 4200 1-sided timing mark reader, the 4300 reader for timing mark and standard tab cards, and the 4800 2-sided card reader. One of the available programs is said to emulate the Hewlett-Packard 7260A optical reader at one-third the cost of that machine.

Circle 427 on Inquiry Card



## Timing Control Board for LSI-11, -11/2 Keeps Track of Time and Date

Dual-size peripheral board TCU-50D from Digital Pathways, Inc, 4151 Middlefield Rd, Palo Alto, CA 94306 provides calendar and realtime functions for Digital Equipment Corp's LSI-11 and LSI-11/2. On receipt of a read instruction, unit will present date and time. Units are preset to correct date and local time, and are reset by a simple software routine. Rechargeable battery backup keeps timing unit functioning for up to three months.

Circle 428 on Inquiry Card

## Compact Board for 6800 Parts Is Offered With a Single-Board Computer

A single-sided PC board for Motorola 6800 components has circuits etched for 6802 MPU, 6846 ROM, 6810 RAM, and 6850 ACIA I/O port. To enable other addresses, the back of the card may be coated with photoresistant paint, and the unused metal cladding etched away.

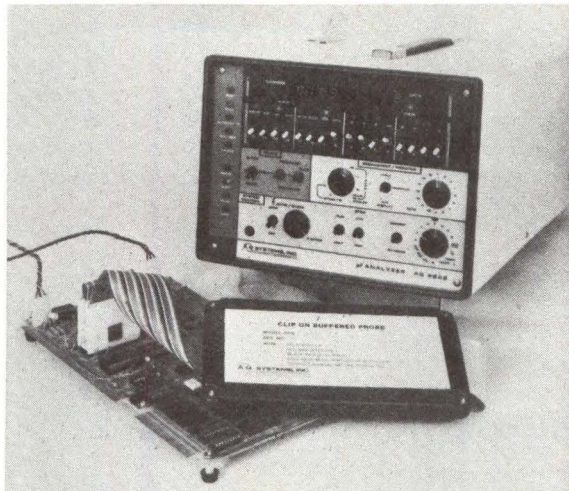
Another product from Lumbert Computer Co, 1200 W Alameda #104, Tempe, AZ 85282 is the Ace, a miniature, fully operational single-board computer with 1-MHz clock, programmable timer, and 2k ROM monitor. A full-scale 6802 system, it provides for parallel output up to 50k bytes/s interleaved with serial output up to 500k bytes/s.

Circle 429 on Inquiry Card

## 8080 Analyzer Is Useful In Development Testing, Service, and Training

Interactive control of the microprocessor and full monitoring of the address bus, data bus, and status lines are major features of the AQ8080 microprocessor system analyzer that is compatible with and satisfies diagnostic needs of all 8080 system configurations. A fully buffered 40-pin clip-on probe connects the analyzer directly to the microprocessor chip under test.

AQ Systems, Inc, 1736 Front St, Yorktown Heights, NY, 10598 has



Independent hardware design of AQ System's 8080 microprocessor system analyzer offers compatibility with all system configurations; memory allocation, address or port assignment, special clock, or separate terminal is not required. 8080 chip to be tested is not removed from socket, eliminating possibility of damage, and system is tested in normal configuration

built in controls and displays to permit the user to examine or modify all memory locations, I/O ports, and internal microprocessor registers. LED displays are provided for analyzer and microprocessor system status, microprocessor cycle status, and binary data. Two hexadecimal displays show data, address, and switch register.

Powerful debugging capabilities are provided by conditional breakpoint, data breakpoint, and monitor functions. Address qualifier and loop count

features isolate most hardware and software problems; an external breakpoint qualification input is provided for user defined test conditions.

Programs may be single stepped by a machine cycle or instruction step, or run at an adjustable speed of 1 to 4000 steps/s while examining memory or registers. The program trace recorder, which provides a block mode of instruction stepping, can also store 128 instructions.

Circle 430 on Inquiry Card

## LSI-11 Systems Gain I/O Efficiency From Communications Software

An RT-11 compatible software driver for the Mighty-Mux™ 11L, DMA, serial line multiplexer has been announced by Educational Data Systems, Inc, 1682 Langley Ave, Irvine, CA 92714. It provides efficient I/O for any RT-11 based LSI-11 system, and supports simultaneous full-duplex asynchronous I/O to as many as 128 ports on the multiplexer. Control requests determine port status, set port characteristics, assign logical/physical port mapping, and abort I/O requests.

For standalone multiplexer operations, modules are provided which may be linked directly to an applications package, avoiding the intervention and overhead of the RT-11 I/O subsystem. A second configuration loads the package as a standard RT-11 driver. The driver will function with any V02 system and is provided at no charge to users of the Mighty-Mux.

Circle 431 on Inquiry Card

## Building Blocks Configure LSI-11s to Customize Needs

Components needed to assemble a reliable DEC LSI-11 microcomputing system or system substation to fit a user's requirements are available from D/L Logic, Inc, 141-A Central Ave, Farmingdale, NY 11735. Relay rack mountable and frontloading bin or chassis accommodates low profile PC boards and/or wirewrapped boards. Fans and baffles are chassis mountable in various configurations, permitting bins to be stacked. Several DEC LSI-11 blocks are mountable in one chassis.

LSI-11 microprocessor cards are offered, as are wirewrappable cards with shut down overload protection, accommodating 162 sockets for standard ICs; Q-Bus extender cards, mountable on an LSI-11 block; and Q-Bus terminator cards. Wirewrap card backplanes accommodate up to 11 connectors. A power supply assembly also is available. □

Circle 432 on Inquiry Card



## INTEGRATED INJECTION LOGIC— A TECHNOLOGY STATUS REPORT

**Eric R. Garen**

Integrated Computer Systems, Inc, Santa Monica, California

Integrated injection logic (IIL) has been hailed in recent years as one of the most significant developments in the area of LSI technology. Its inherent advantages include high packing density (thereby allowing high integration levels and many gates per chip) and a low speed-power product allowing device speed to be traded off with power consumption over a range of nearly four orders of magnitude. Other benefits are compatibility of linear and digital functions on the same chip; higher operating temperature ranges than available with MOS ( $-55$  to  $125$  °C is standard); and higher radiation resistance than MOS. In addition, IIL devices are potentially capable of very low power and low voltage operation.

Within the last 2 years many companies have developed IIL products that are now realizing some of these inherent advantages. However, the limited experience with this

technology to date poses difficulties in design and processing.

### IIL Fundamentals

Basic building block of IIL is the single-input, multiple-output inverter stage, shown in Fig 1(a). It consists of a multiple collector npn transistor whose base is driven by a current-source, the "injector". In the circuit implementation of the IIL gate, Fig 1(b), the injector is a lateral pnp transistor.

IIL gate configuration lends itself to logic connections with a single input and multiple outputs. This is somewhat different from other conventional logic configurations, which are typically multiple-input, single-output connections. IIL gates can be directly cascaded together by

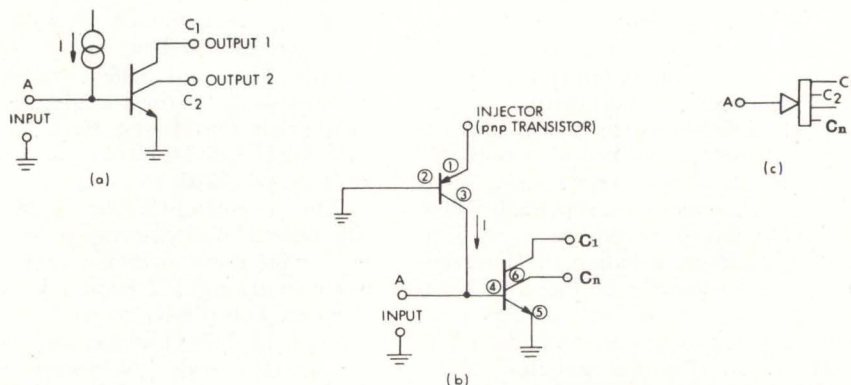


Fig 1 Basic IIL inverter configuration. (a) Electrical diagram, (b) IIL implementation with numerals indicating correspondence to numbered elements of Fig 7 (c) IIL gate symbol (Courtesy Exar Integrated Systems, Inc)



**C-R-T, C-R-T, alpha-numericity,  
ASCII-key, multi-key, programmability,  
Blinkity, blankety video-bility,  
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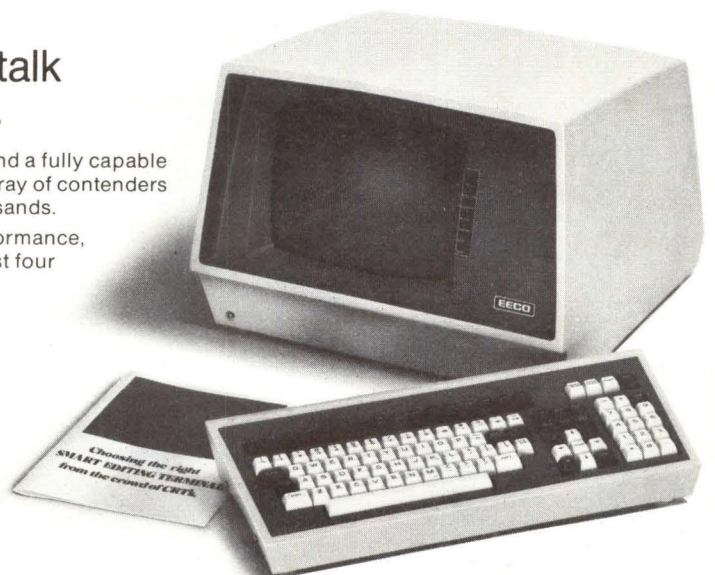
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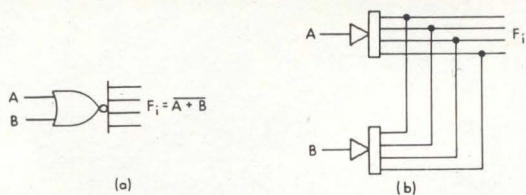


Fig 2 IIL NOR gate. (a) Logic symbol, (b) circuit implementation using inverters (Courtesy Exar Integrated Systems, Inc)

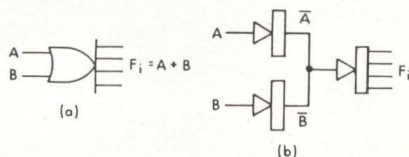


Fig 3 OR-gate implementation. (a) Logic diagram, (b) IIL gate diagram (Courtesy Exar Integrated Systems, Inc)

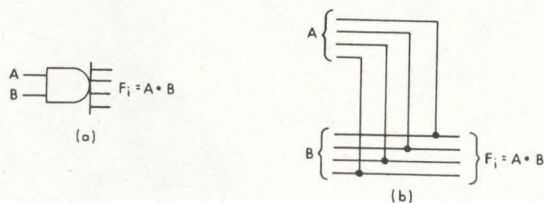


Fig 4 AND gate implementation using wired-AND connection. (a) Logic symbol, (b) circuit implementation using direct wired-AND connection, (c) AND gate symbol (Courtesy Exar Integrated Systems, Inc)

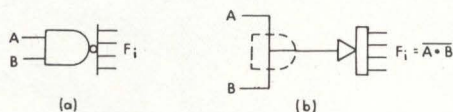


Fig 5 NAND gate implementation using wired-AND connection. (a) Logic symbol, (b) IIL gate diagram (Courtesy Exar Integrated Systems, Inc)

simply connecting the output of one gate to the input of the next. The only requirement is that the output of the previous gate should be able to "sink" an amount of current equal to the injector current of the next one.

At the present time, no "official" gate symbol exists for IIL gates. For the purpose of this discussion the symbol shown in Fig 1(c) is used.

Since the IIL gate outputs are "open-collector" type stages, multiple outputs can be directly connected together to form a "wired-AND" function (Fig 2). The connection shown corresponds to a NOR gate. By directly coupling inputs or outputs of various gates, OR, AND, and NAND functions can also be easily obtained, as shown in Figs 3 through 6.

Fundamentals of logic system design using IIL technology are basically no different than in designing with other logic families. One initially starts with a complex system, then subdivides it into simpler sub-blocks, finally reducing it to the level of simple gates. There remains, however, the one significant difference, which deserves repeating: while most other logic families are built around multiple-input, single-output gates, IIL is designed around single-input, multiple-output gates. Thus, one of the important steps in designing IIL systems is to convert the conventional logic diagram into an interconnection of IIL inverter stages.

After a little practice, drawing an IIL schematic or gate diagram from a conventional logic diagram is easy.

The following steps are typical of those used by a designer in making this conversion.<sup>1</sup>

*Step 1:* Redraw the logic diagram using multi-output IIL, so that each output feeds into only one other input.

*Step 2:* Buffer the interface signals feeding AND and NAND gates with two series inverters. This allows IIL inputs to be fed from separate IIL outputs when making a wired-AND connection (Fig 4).

*Step 3:* Replace each AND gate with a wired-AND connection and each NAND gate with a wired-AND followed by an inverter.

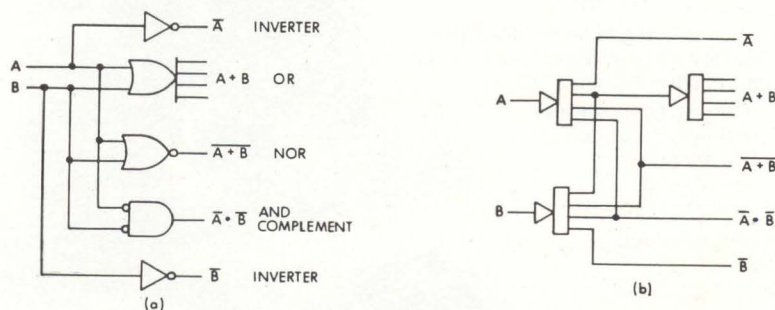


Fig 6 Possible logic combinations using three IIL gates. (a) Logic diagram, (b) IIL gate connection diagram (Courtesy Exar Integrated Systems, Inc)



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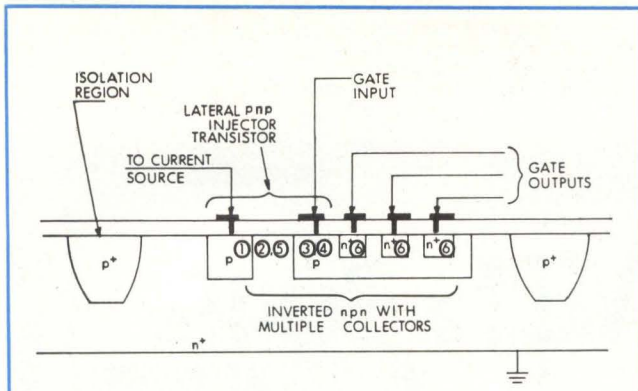


Fig 7 IIL gate structure for all-digital LSI circuits. Numerals indicate correspondence to numbered elements of Fig 1(b)

Step 4: Replace NOR and OR gates with their IIL equivalents (Figs 2 and 3), and redraw the diagram using only IIL inverters.

Step 5: Simplify the IIL gate interconnection by eliminating redundant logic gates.

As mentioned previously, a key advantage of IIL is its high packing density. This is a direct result of the layout of the fundamental gate on the wafer. In the cross-sectional view of Fig 7, the basic structure of an IIL inverter is a "merged" structure consisting of a pnp injector transistor together with a multiple collector "inverted" npn transistor.

The current source is the lateral pnp, with the n-type background serving as its base. Note that this n-type region, which is grounded, also serves as the emitter of the npn transistor. Collectors of the npn are formed by diffusing n-type regions into the p-type base region of the npn transistor. This p-type base region of the npn also serves as the collector region of the lateral pnp transistor. In this manner, various electrodes or terminals of the IIL gate are merged to give a very compact device layout.

Compared to conventional bipolar npn transistor structure, the npn transistor of Fig 7 operates in an upside-down, or "inverted" mode. In conventional npn transistors the background n region serves as the collector, and the n+ topside diffusion forms the emitter. In the case of the IIL gate, the roles of these "emitter" and "collector" regions are reversed.

Further compacting of an array of IIL gates is possible, since many gates in an array structure can share a single p-type injector rail as shown in Fig 8. This fundamental structure is employed by Texas Instruments in the "4-

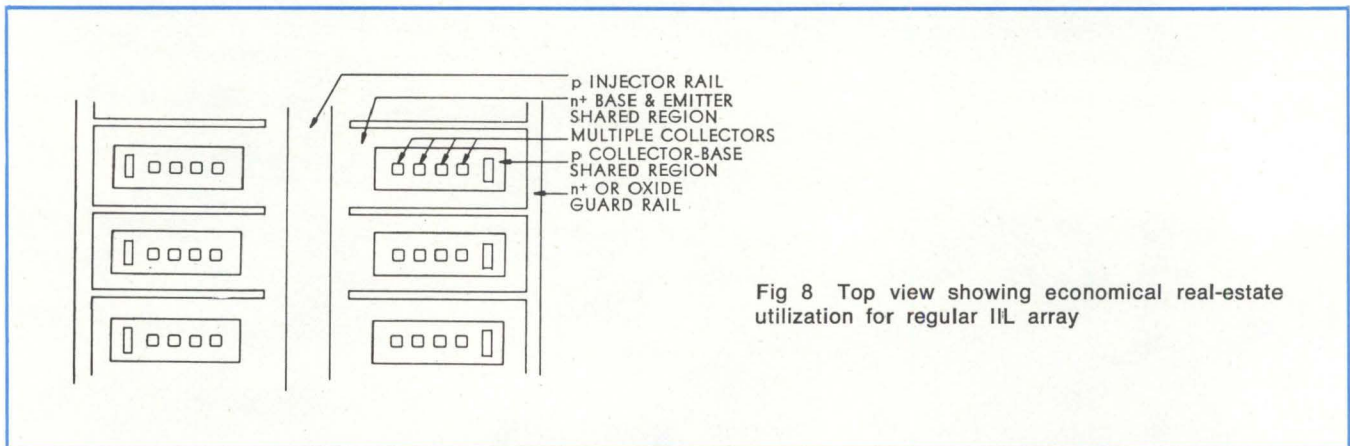


Fig 8 Top view showing economical real-estate utilization for regular IIL array

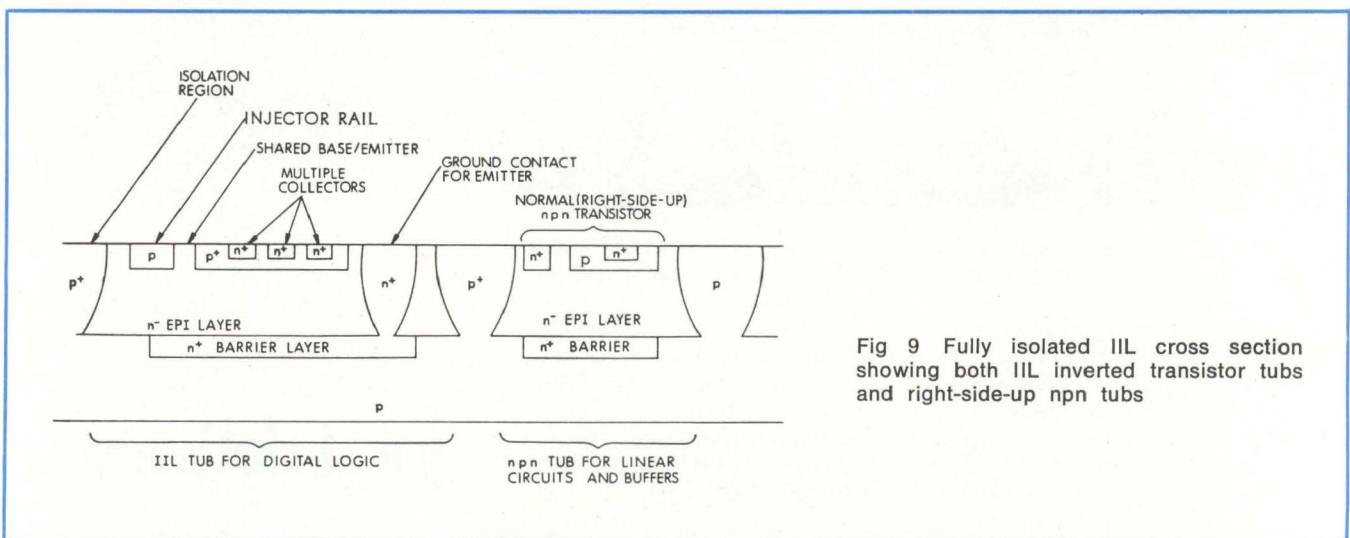
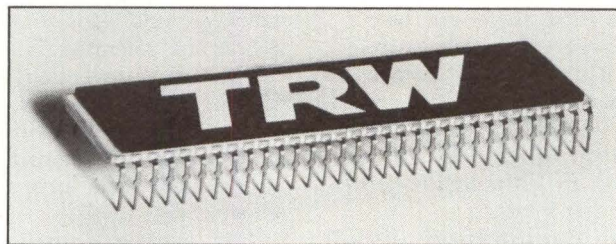


Fig 9 Fully isolated IIL cross section showing both IIL inverted transistor tubs and right-side-up npn tubs



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mask"  $\text{IIL}$  process used to implement the SBP 9900 microprocessor product line.

That approach, however, is not particularly well-suited to implementing analog circuits. If both linear and digital circuits are required, the "fully isolated"  $\text{IIL}$  process shown in Fig 9 is utilized. In this process some "tubs" contain  $\text{IIL}$  inverted mode transistors used for digital logic, while other tubs contain right-side-up npn devices for linear circuit capability. This structure is employed by TI in watch circuits and other  $\text{IIL}$  devices, by Analog Devices in the AD571 monolithic analog-to-digital converter, and by Exar Integrated Systems in semicustom master chips with both linear and digital capabilities.

### Obstacles to Design and Processing

For all the potential advantages of  $\text{IIL}$ , it confronts the chip designer with many unique problems in implementation. First is the requirement for a constant current supply to the injectors. This can either be developed on the chip itself with a constant current source or, more typically, implemented offchip by inserting a series resistor between the voltage supply and each  $\text{IIL}$  chip.

Once the current is available on the chip, however, the difficulty has only begun. Because the speed of an  $\text{IIL}$  gate is directly related to the injector current, it is crucial that all  $\text{IIL}$  gates on a chip receive a uniform current. This poses serious design problems. First, the on-die power buses must be substantial to prevent voltage drop from one end of the bus to the other. Even a 10-mV drop has significant implications. Typically such drops are corrected by inserting a low series resistance between the metal power bus and each p-injector rail. These "ballast" resistors must be custom-designed to differing sizes to compensate for voltage drop along the bus.

Similarly the p-injector rail itself can experience drops and therefore must periodically be broken up into smaller rails separately supplied from the metal buses. The current distribution problem is compounded by the potential for mismatched diodes in the junctions between each p-type injector rail and the surrounding n-material. To summarize this first problem, the success of the  $\text{IIL}$  circuit requires considerable effort by the designer to assure a uniform power supply distribution.

Next, there is the problem of packing density. The primary limitation today in  $\text{IIL}$  packing density is imposed by the area required for metal interconnections. First, as described previously, power buses must be substantial. Second, in the fully-isolated  $\text{IIL}$  technology extensive ground buses are required. Furthermore, interconnecting  $\text{IIL}$  gates appears to be a more complex problem than interconnecting conventional logic, due to the multiple-output single-input structure of  $\text{IIL}$ . The result typically requires a 2-level metallization process and utilizes significant chip area simply for interconnection. In some cases a third level of interconnection may be necessary for efficient chip layout and can only be accomplished by the use of diffused resistive tunnels within the crystal itself.

The multiple-output single-input structure also presents the designer with the problem of how to distribute high fanout nodes such as clocks and other control circuitry—and this is the third major problem area. A designer has two choices. Either he must use an internal buffer created with a normal npn transistor to drive one high current line, or he can use many individual lines fanning out from a single  $\text{IIL}$  gate. However, achieving a high fanout is difficult with the normal inline structure of the  $\text{IIL}$  gate

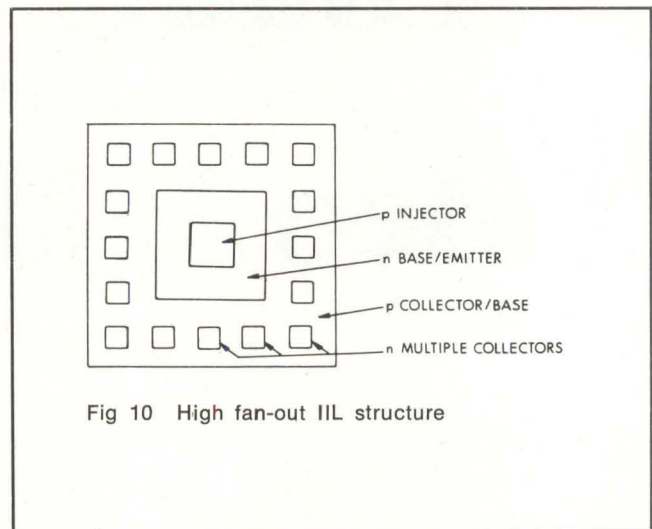


Fig 10 High fan-out  $\text{IIL}$  structure

shown in Fig 8. If more than four collectors are required, arranging them linearly results in an uneven current distribution between them. Obviously, one could develop a tree-like structure of gates to achieve a higher fanout; however, this leads to significant delays, which generally cannot be tolerated in clocks and other control signals. To avoid this, various other geometries such as that shown in Fig 10 have been suggested. This approach does not avoid the difficulty of routing these multiple individual output lines around the chip nor the resulting requirement for a large interconnection area, as explained above.

Still another design challenge is the implementation of output buffers, especially in the 4-mask process, which does not have right-side-up transistors. Texas Instruments has overcome this problem by perfecting the implementation of inverted transistors with  $\beta = 100$ . An output buffer built from two of these in parallel can sink 20 mA with an injector current of only 100  $\mu\text{A}$ . Achieving  $\beta = 100$  for inverted transistors is not simple, and other manufacturers have had difficulty with this process.

The designer's problem is further compounded by the lack of a generally available accurate model for the fully isolated  $\text{IIL}$  inverted transistor. Models must often be artificially manipulated to match the measured characteristic curves of these inverted transistors by using unrealistic  $\beta$  values (ie, different from the actual measured  $\beta$ ). This implies that existing models do not account for various phenomena in the inverted transistors and that more sophisticated models must be defined. Present chip design is often an empirical procedure, in which each modification of the gate layout must be checked to determine its effects.

Finally, fabricating the  $\text{IIL}$  circuits, especially those employing the fully isolated  $\text{IIL}$  linear-digital structure, requires specialized processing capability. First, the base region of the inverted transistors must be extremely narrow to achieve a high  $\beta$ . However, without very tight process control the base of some inverted transistors may disappear entirely, a phenomenon known as "punch through," which poses obvious yield problems. The second difficult process requirement is the maintenance of a very thin epilayer (the  $n^-$  region in Fig 9). Growth of this epitaxial layer must be fully controlled. On the one hand it should be extremely thin to minimize the stored



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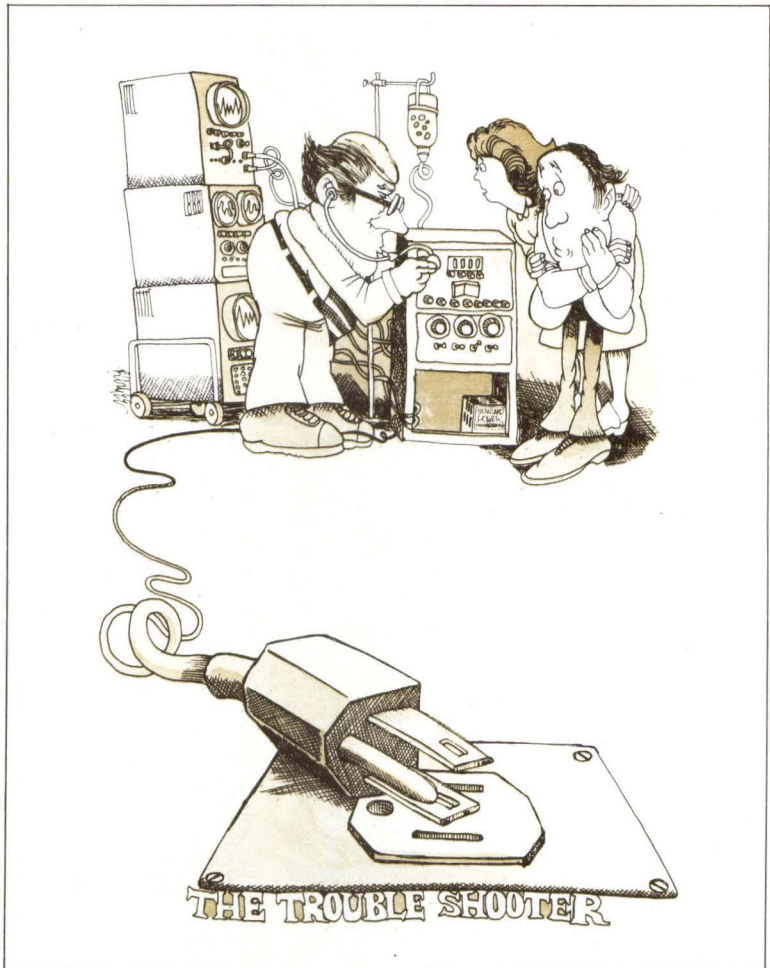
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charge which must be removed to turn on the  $\text{IIL}$  gate. On the other hand it must be thick enough not to break down when maximum voltage is applied across the right-side-up npn transistors. Despite these processing constraints, several manufacturers are now successfully producing  $\text{IIL}$  digital as well as digital/linear LSI circuits.

### Current Approaches

An evident exception to the empirical tendency in chip design is Texas Instruments' model for the TI 4-mask gate structure. This model was used by an automatic chip layout program in the design of the SBP 9900 microprocessor. The program, known as "Boolean Source Description Language," uses as its input the designer's NAND-gate logic diagram, and outputs the composite layout required for chip implementation. Furthermore, this source description language can generate its own test patterns for the chip. TI has used this program to design each of the three versions of the SBP 9900 and reports that each time it produced a fully functional circuit on the first try, indicating that the model is accurate within the range of layout variations.

The initial SBP 9900 was a 2-MHz chip. Guard rings between gates were implemented with  $n^+$  silicon, and resistive tunnels were used to achieve a third level of interconnection. The second version implemented several logic changes and removed the interconnecting tunnels.

In the third version, the 3-MHz SBP 9900A, several changes were incorporated to improve speed. The  $n^+$

guard rings were replaced with oxide separators, to prevent crosstalk between adjacent  $\text{IIL}$  gates. Lookahead logic was also added to increase speed. Segmented injectors interconnected by aluminum replaced the previous long injector rails. Furthermore, bonding pads were made 20% larger so the chip could subsequently be shrunk. The final product contains 6182 gates on a 76,000  $\text{mil}^2$  die. Although the chip layout software does an extremely accurate job, it is relatively inefficient in its use of real estate. A chip size comparable to the 57,000  $\text{mils}^2$  of the smaller  $\text{NMOS}$  9900A could probably be attained if the layout were done by conventional chip design techniques.

In addition to the microprocessor itself, development is continuing on seven peripheral chips. These utilize both 4-mask (oxide separated) and fully-isolated  $\text{IIL}$  processes.

TI indicates that present yield is adequate to serve the expanding marketplace. No major hurdles in improving yields are foreseen, the present limiting factor being the process's recent start down the experience curve.

An exciting linear/digital  $\text{IIL}$  product was recently announced by Analog Devices. The AD-751 is a monolithic 10-bit successive approximation mode A-D converter with onchip temperature-compensated voltage reference and also 3-state buffer outputs which enable it to attach directly to a microprocessor bus. To achieve high density coupled with good speed, the heart of the circuit is implemented with  $\text{IIL}$  technology. A fixed current source necessary for other circuitry on the chip also supplies the injector current necessary for the  $\text{IIL}$  gates, thus doing double duty. The power distribution problem initially posed design challenges, but once solved this has presented no problem in manufacturing. Chips utilize single metal interconnection with some deep side diffusion underpass structures for interconnection. The  $\text{IIL}$  gates are not being pushed to their speed limits, and therefore a normal 10- $\mu\text{m}$  epitaxial layer is used. To prevent breakdown in the normal linear transistors, circuit design provides that these transistors are never exposed to the full voltage swing of even one power supply.

Another  $\text{IIL}$  chip now in production is available from Exar Integrated Systems. A master chip approach allows a designer to customize his own  $\text{IIL}$  linear/digital circuit. A family of chips, each with both standard  $\text{IIL}$  digital gates and also linear driver circuits is available in various sizes. These semicustom chips were described in this column in Sept 1977 in the article entitled "Semicustom Integrated Circuits—The Do-It-Yourself LSI Chip."

### Summary

$\text{IIL}$  technology has made significant progress in becoming commercially viable in recent years. As the manufacturers gain more experience with both design and processing of this technology, it is expected that the problems and limitations listed above will be satisfactorily solved and the process will yield more circuits that achieve the advantages first promised by  $\text{IIL}$ .

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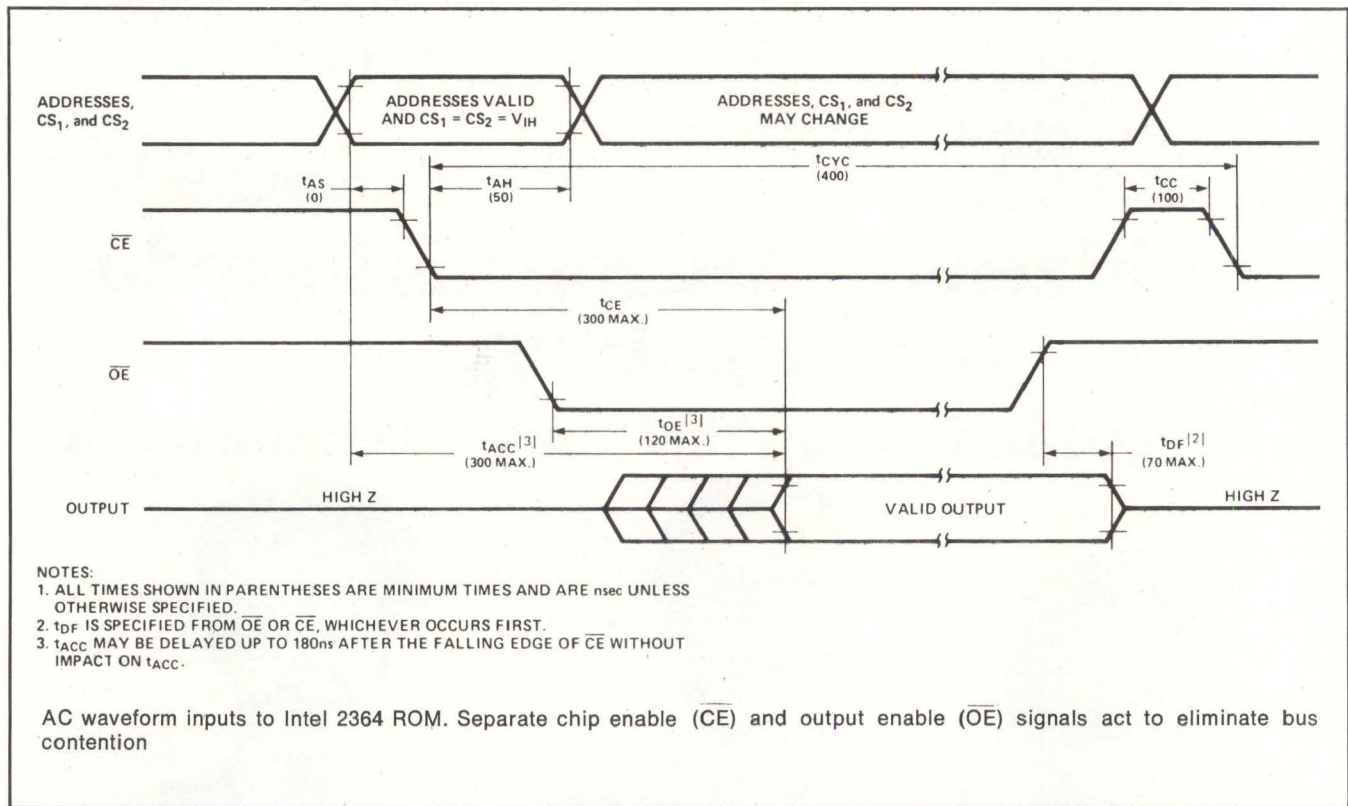
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## High Density ROMs Meet Needs of Advanced Microprocessor Systems



A 32k and a 64k ROM offering 300-ns maximum access time and low power dissipation are configured as edge-enabled devices—a property that allows a ROM to meet speed requirements of state-of-the-art microprocessors while dissipating 25% of the power of a static ROM. The 32k device (2332) is organized as 4k x 8 bits while the 64k (2364) version is organized as 8k x 8 bits.

Both devices are interchangeable with new generation 5-V EPROMs and upward compatible with future very high density devices storing more than 64k bits. A 32k-bit edge-enabled EPROM, the 7232, with matching specifications and features, is to be added to the family. The ROMs are also interchangeable with last generation 8k-bit EPROMs by the same manufacturer—Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. They eliminate bus contention, a persistent problem for high performance systems, through the use of a separate output enable function.

As indicated in the waveform diagram, a clock issues a chip enable signal ( $\overline{CE}$ ) which powers up input circuitry for access; other operations

are timed by internal circuitry and by the output enable command signal ( $\overline{OE}$ ), which activates data output buffers.

The  $\overline{CE}$  input is decoded from the high order system address bits and the  $\overline{OE}$  input is separately controlled by the microprocessor. For example, the "read" bus control command generated by 8080A and 8085 microprocessors can be connected directly to the  $\overline{OE}$  input of all edge-enabled EPROM/ROM devices in the system. Most microprocessors provide such commands.

Other features of the two ROM devices include 400-ns cycle time, 5-V  $\pm 10\%$  power supply, direct TTL compatibility on all inputs and outputs, and a 3-state output for direct bus interface. Typical supply currents are 20 mA in active operation and 8 to 10 mA during standby. Maximum supply currents are specified as 40-mA average maximum in active operation and 15-mA standby current.

The chips go into active operation when selected via  $\overline{CE}$  decoding, and go on low power standby when deselected. Devices have onchip address latches. Addresses are latched

within 50 ns after the  $\overline{CE}$  input becomes true. Thereafter, addresses can vary without affecting the data cycle in progress.

The manufacturer suggests that a bipolar p/ROM be used for  $\overline{CE}$  decoding. Conventional TTL decoders and jumper packs may be used, but use of a p/ROM as a programmable decoding logic array offers several additional advantages. It facilitates storage density upgrades by allowing programmers to reassign device addresses without requiring wiring changes; and, since no wiring changes are needed, it reduces costs and problems of manufacturing and inventory control.

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### Low Cost, 30-MHz Video ADC Performs Typical Conversions in 33 ns

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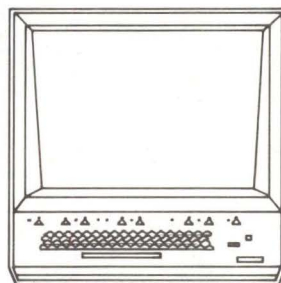
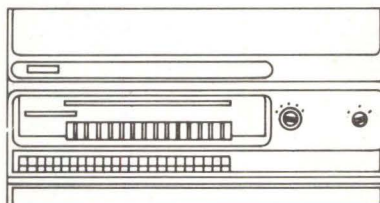
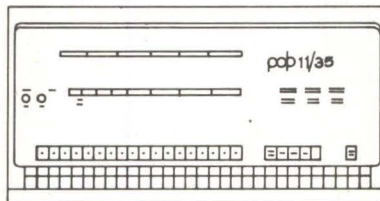
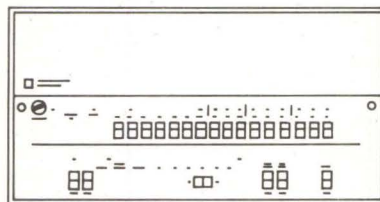
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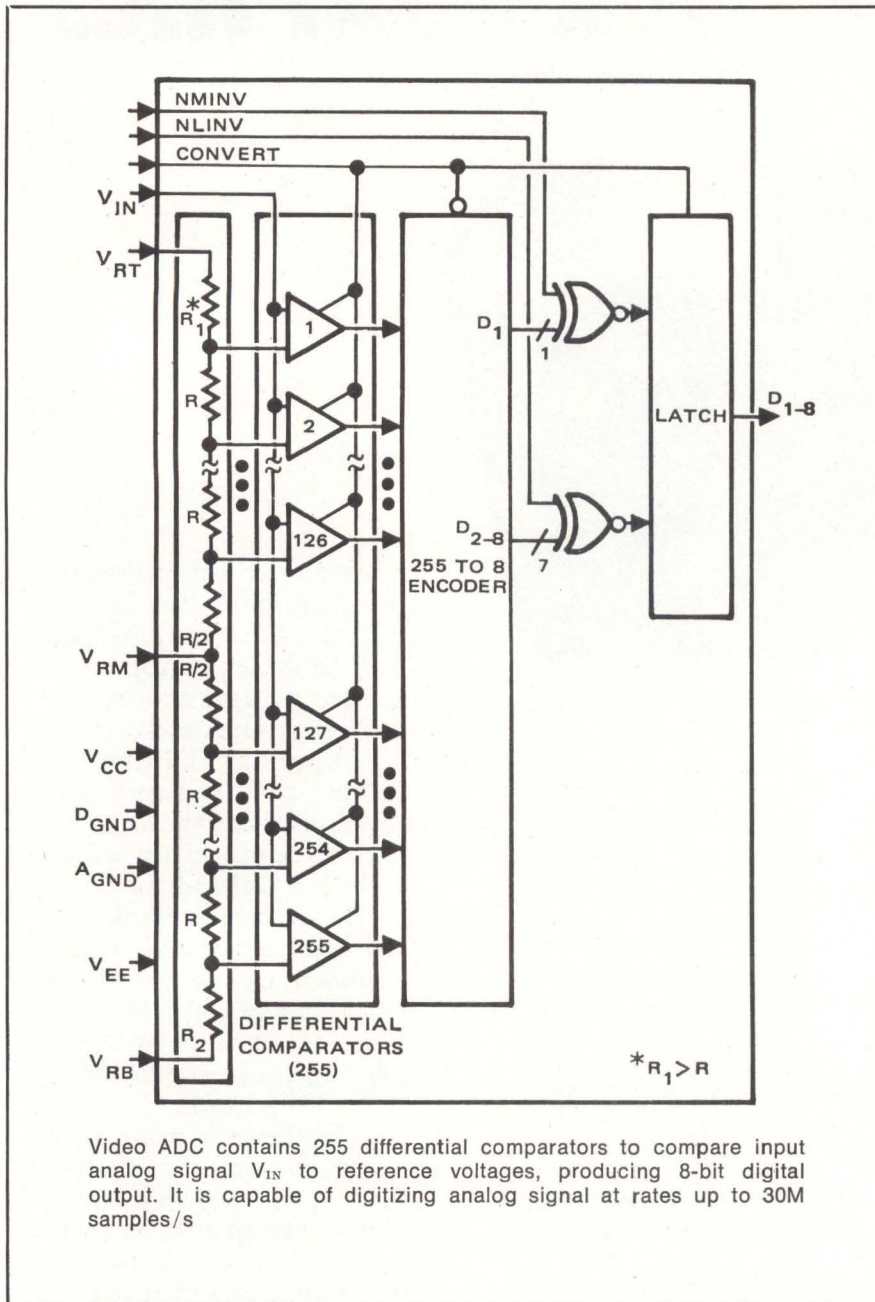
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A controller consisting of a pair of complementary mos integrated circuits has been designed to serve as the interface element between a processor and an LED or gas discharge alphanumeric display. There is sufficient digit dead time to multiplex gas discharge displays, although this depends on the model of the display.

This intelligent display controller is available as a 130 x 130 mil, 28-pin package in two versions: MM74C911, which will multiplex four digits, using eight bits of input information; and MM74C912, which will multiplex six digits, using a 16 x 7-bit onchip ROM addressed by four data bits. The -11 version has both digit and segment expansion capability; the -12 has digit expansion capability, with the decimal point input going directly to the output.

Both display controllers are produced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. They are designed for easy interfacing to microprocessor and bus-oriented systems. Each of the devices has a write enable and a chip enable pin, and can be randomly accessed on input. They are designed to replace as many as five to ten discrete transistors and medium scale integrated circuits.

As shown in the diagram (input waveform to display controller), data are written into the internal registers by first bringing chip enable ( $\overline{CE}$ ) low. Address information is not latched by  $\overline{CE}$ , and therefore can change before or after  $\overline{CE}$  is low. Address information must be stable  $t_{sa}$  ns before write enable,  $\overline{WE}$ , goes low, where  $t_{sa}$  is address setup time. Data are written into the addressed register when both  $\overline{CE}$  and  $\overline{WE}$  are low. Data should be stable  $t_{sd}$  ns before the rising edge of  $\overline{WE}$ , where  $t_{sd}$  is data setup time. Chip enable and  $\overline{WE}$  may simultaneously return high.

In order to drive display segments, display controllers were designed to drive 40 mA minimum. This was achieved using a buffered guard band CMOS process in which the segment outputs make use of a parasitic npn emitter follower bipolar transistor structure inherent in the CMOS process and an n-channel sink transistor. Segment outputs can be tri-stated by the use of an output enable pin. In

less than half the cost of existing modular converters.

TDC1007J is a single chip containing 20,000 closely matched bipolar components and providing 255 comparators with combining logic. It features a 1-deg differential phase, 1% differential gain, binary or 2's complement output, and 2-W power dissipation, and is available as a 64-pin DIP.

Absolute maximum ratings include: supply voltage of 0 to  $\pm 7.0$  V; input voltages of  $-0.5$  to 5.5 V (digital), 0.5 to  $-2.5$  V (analog); and output

voltage of  $-0.5$  to 7.0 V. Nominal recommended operating conditions are: 5 V for supply voltage  $V_{cc}$  and  $-6$  V for supply voltage  $V_{ee}$ ; 0 V for reference input  $V_{rt}$  and  $-2$  V for reference  $V_{rb}$ ; and a 25 °C operating temperature.

The device is available from TRW LSI Products, PO Box 1125, Redondo Beach, CA 90278. A fully tested, printed circuit board to enable potential users to evaluate the converter also is available.

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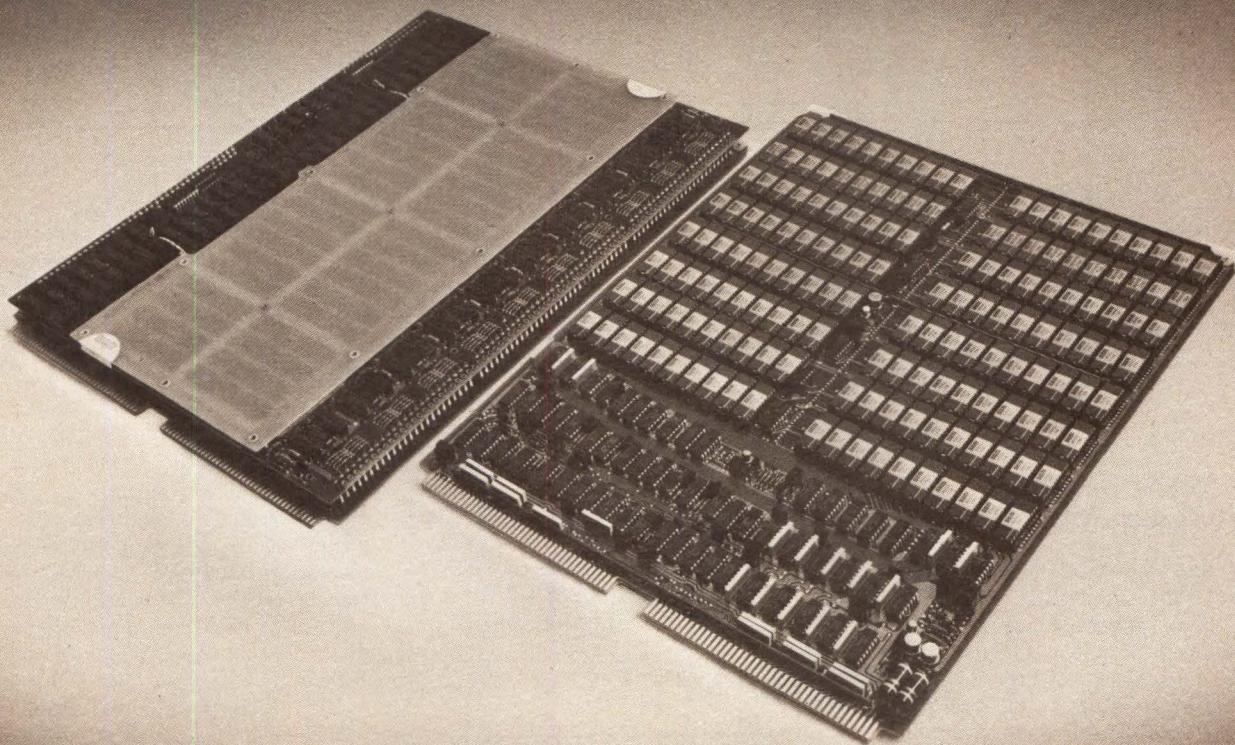


**Memory problems? EMM can help.**

**Semiconductor or core**

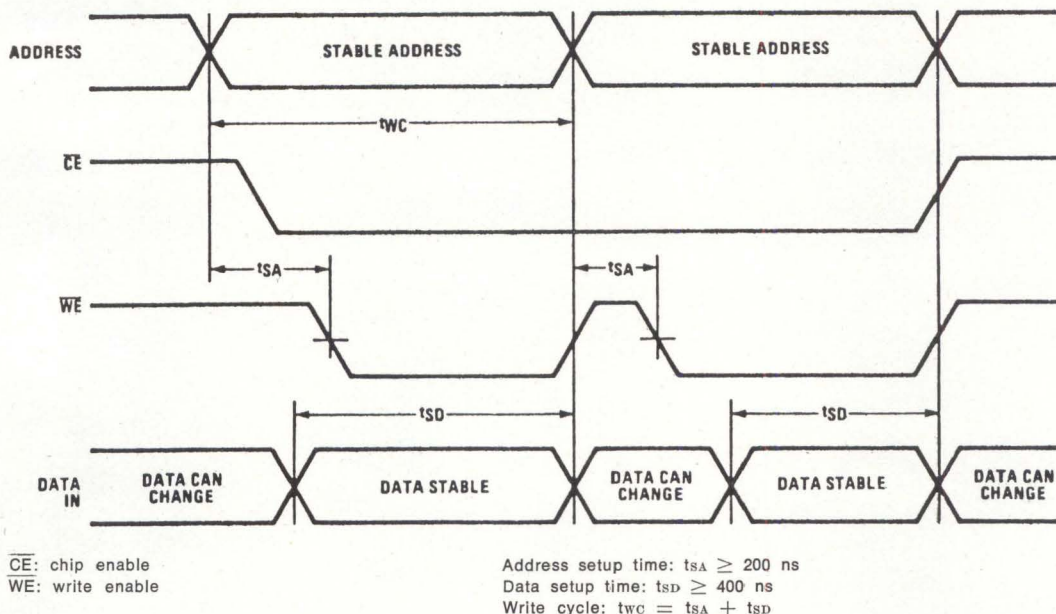
**Just the right size**

**Any speed you need**



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Input waveforms to National Semiconductor display controller. Chip enable ( $\overline{CE}$ ) low writes data into internal registers. Since address information is not latched by  $\overline{CE}$ , it can change before or after  $\overline{CE}$  is low. Data are written into addressed register when both  $\overline{CE}$  and  $\overline{WE}$  are low

situations where power has failed, this can be used to turn off the segments of the display being driven, to save power.

Display controllers provide a random access to the master portion of an onchip register selected by an ad-

dress operation. Normally, an onchip oscillator will sequentially address the slave portion of the internal registers. However, it is also possible to randomly access the slave portion of the registers via the digit lines by the use of a digit I/O control pin.

A third version of the controller, not yet available, is designated MM74C913. It will be identical to the MM74C912 except that the decimal point input and output and the digit and segment Tri-State controller will be omitted.

### Fully Static 32k ROM Is TTL Compatible

A 32k MOS mask ROM, the 2632 is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives. Maximum supply current is 80 mA and, while 450-ns access time is guaranteed, typical access time is 375 ns. The unit features two programmable chip select inputs as well as OR-tie compatibility on the outputs to facilitate memory expansion.

Produced by Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, the fully static device is in an industry-standard 24-pin package. It is

completely TTL compatible and operates from a single 5-V supply. Organized as 4096 x 8 bits, the device is pin compatible with the 2607 1k x 8 static ROM, the 2616 2R 6 x 8 static ROM, and both 2708 and 2716 EPROMS.

Circle 352 on Inquiry Card

### USART Chip Programmable For Maximum Flexibility

A programmable universal synchronous/asynchronous receiver/transmitter (USART) chip, the TR 1953, is

contained in a standard 28-pin DIP. Its functional configuration is programmed by system software for maximum flexibility, allowing the system to receive and transmit virtually any serial data communication signal presently in use (including IBM BiSync).

This device is available from Western Digital Corp, 3128 Red Hill Ave, PO Box 2180, Newport Beach, CA 92663. Its synchronous mode features internal or external character synchronization, automatic sync insertion, and baud rates from dc to 65k. Its asynchronous mode features line break detection and generation (1, 1½, or 2 stop), false start bit detection, baud



# DESIGN a voice command system with the Siliconix CODEC

Enter the **Siliconix CODEC Design Contest** and win an Apple II — the world's best-selling personal computer — or another great prize. All you have to do is use Siliconix' CODEC to design a microprocessor-based system which responds to your spoken words (or talks back to you). Our CODEC is a two-chip set: the DF331 coder is a high-speed serial output A/D converter — a complete subsystem-on-a-chip; the DF332 decoder converts high-speed digital bit streams into analog signals. The system you design must be capable of understanding or speaking at least 16 words.

Here's what you can win:

**1st prize:** Apple II personal computer (retail value \$1,445). A completely self-contained computer system with high resolution color graphics in 15 colors (with color TV); BASIC in ROM, 16K bytes of RAM, built-in video interface, cassette I/O, four A/D inputs with two game paddles supplied, eight peripheral slots, three TTL inputs and four TTL outputs. Apple II plugs into any standard TV using a modulator.

**2nd prize:** Siliconix LCD Stopwatch-In-A-Wristwatch. Features time, day, date, plus split timing stopwatch functions.

**3rd prize:** Siliconix LED Stopwatch. Includes split timing function.

**4th prize:** Siliconix Telephone Timer. Includes start/stop and timeout.

**5th prize:** Siliconix LED Stopwatch. Features a digital start/stop timer.

All entries must be accompanied by our official entry blank. Get yours, along with complete contest rules, data sheets and other information, by filling out the coupon below.



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CD 6/78

**Siliconix CODEC Design Contest**  
2201 Laurelwood Road  
Santa Clara, CA 95054

Yes, I want to know more about the Siliconix CODEC Design Contest. Please send me details and the official entry blank.

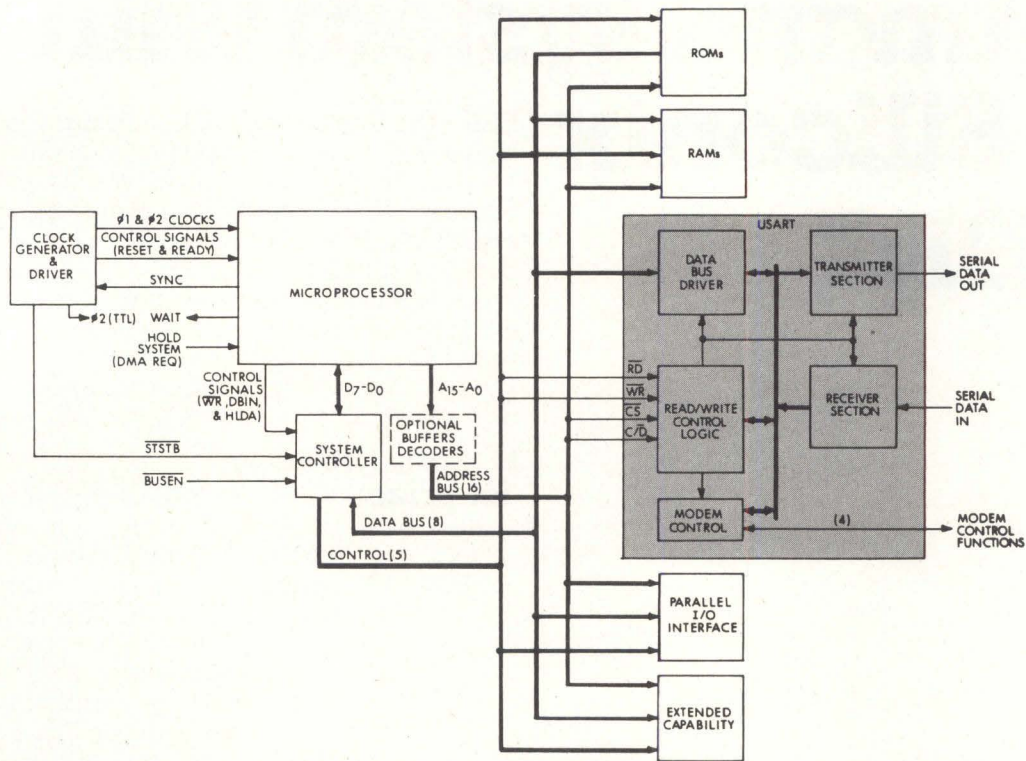
Name: \_\_\_\_\_ Title: \_\_\_\_\_

Company: \_\_\_\_\_ (Optional)

Address: \_\_\_\_\_ Mail Station: \_\_\_\_\_

City: \_\_\_\_\_ State: \_\_\_\_\_ Zip: \_\_\_\_\_





Western Digital USART as interface to microcomputer. When input signals to chip go low, chip select (CS) enables communication between USART and microprocessor, read (RD) allows microprocessor to read data or status information, and write (WR) allows microprocessor to write data or control words into USART. Control/data input signal (C/D) is used to determine overall device operation

rates from dc to 9.6k, and three selectable clock rates (1, 16, or 64 times the baud rate).

Both modes provide transmission error detection (using parity, overrun, or framing) and double buffering of data. The device is TTL compatible, using a single TTL clock for either synchronous or asynchronous operation. Characters are specified by a 5- to 8-bit code.

Absolute maximum ratings include ambient temperature under bias of 0 to 70 °C, storage temperature of -65 to 150 °C, voltage on any pin with respect to ground of -0.5 to 7 V, and 1-W power dissipation. Dc electrical characteristics include maximums of 0.8 V for input low voltage and 0.45 V for output low voltage, and minimums of 2.0 V for output high voltage and 2.4 V for output high voltage. Maximum input leakage is 10 μA. Typical power supply

current is 45 μA with a maximum of 80 μA.

Circle 353 on Inquiry Card

### Single Chip Display/Keyboard Controller Has All Drive Functions

A general purpose, programmable alphanumeric display/keyboard controller that interfaces directly with most 8-bit microprocessors contains virtually all display control functions on a single chip. The device has a built-in 32 x 8 RAM, as well as ASCII character generators for 7-, 14-, and 16-segment displays. It internally generates all timing and refresh signals for both display and keyboard functions and, in addition, includes an intelligent controller and bus interface.

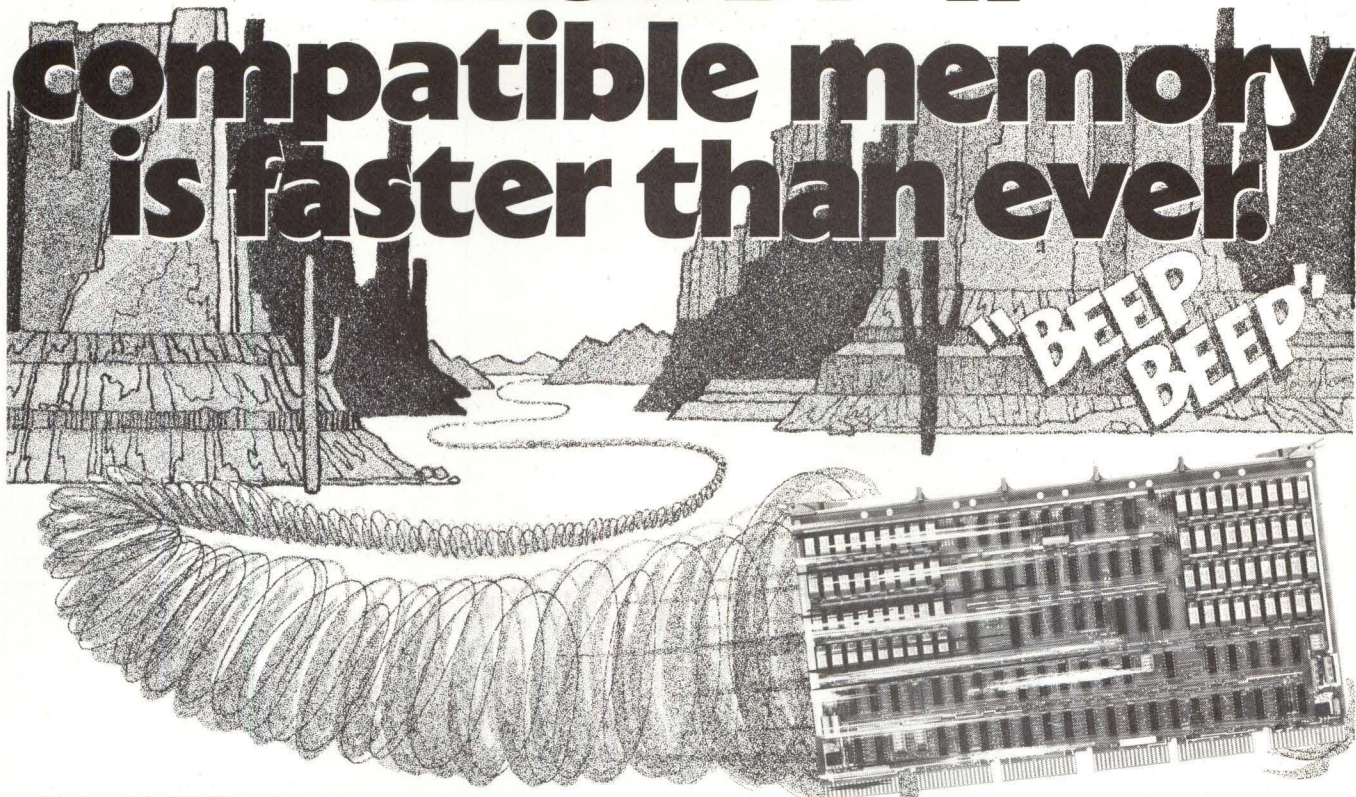
All timing and refresh signals to drive between 1 and 32 characters are on the display portion. The chip will refresh LED, gas discharge, incandescent, and other displays. A dual scan mode permits driving long displays at half the refresh rate and half the peak current of the conventional single scan mode, while maintaining flicker-free condition.

A 22-word instruction set includes such commands as clear display, shift display left/right, blank cursor, read/write display, and self/test. Display and keyboard parameters (the number of characters in the display, refresh frequency, and the number of keys, are fully programmable.

MTX-B1, produced by Matrox Electronic Systems, PO Box 56, Ahuntsic Sta, Montreal, Quebec H3L 3N5, Canada, requires a single 5-V ±10% power supply (60 mA). All display and keyboard i/o pins are TTL com-



# This PDP-11\* compatible memory is faster than ever!



Motorola's MMS1117 is an easy, inexpensive way to add-in high-density, high-speed storage with parity option features for your PDP-11 system. Now it's more than 20% faster than ever before. Speeds for all three MMS1117 speed options are significantly faster, with typical system Read Access Time of the fastest version reduced from 370 ns to 290 ns.

The MMS1117 provides total electrical and mechanical compatibility with 10 different UNIBUS\* PDP-11 processors: not only the 11/04 and 11/34, but the new 11/60 plus the 11/05, 11/10, 11/35, 11/40, 11/45, 11/50 and 11/55. It just plugs into any new Hex SPC slot (DD11B, DD11C, DD11D, DD11P).

Each speed option of the MMS1117 is available in your choice of 32, 64, 96, or 128 kilobytes. Each offers parity plus on-board parity generation and checking logic. There's no need for an external parity control module. The system imposes one UNIBUS load regardless of memory size and parity.

MMS1117 power requirements are low despite its speed and density. A fully populated 128 kilobyte system with parity and controller operates at the following rates: 5 V  $\pm$ 5% @ 3.0 A (typ), +15 V @ 0.2 A standby or 0.7 A continuous maximum access, and -15 V @ 0.03 A.

## 128 Kilobyte MMS 1117

Speed Option	Read Access Time (typical)	Price 1-5
Fastest	290 ns	\$4,305
Faster	360 ns	\$3,920
Fast	390 ns	\$3,530

## More Motorola Memory Systems

System	Organization	Description
MMS1110	16K x 16	
MMS1110-1	12K x 16	Add-in for LSI-11 systems
MMS1110-2	8K x 16	
MMS1110-3	4K x 16	
MMS1118L	16K x 18	Add-in for PDP-11/05, 11/10, 11/35 and 11/40 systems with the MF11-L backplane
MMS1118	16K x 18	Add-in for PDP-11/04, 11/34 systems
MMS1118-1	12K x 18	
MMS1118-2	8K x 18	
MMS3400	32K x 18 or 64K x 9	For 3400N systems
MMS68102	16K x 8	Battery backup for M6800 and other synchronous systems; pin-compatible with EXORciser† micromodule
MMS68102-1	8K x 8	
MMS68102A	16K x 9	
MMS68102A-1	8K x 9	
MMS68103	16K x 8	Hidden refresh for M6800-based systems
MMS68103-1	8K x 8	
MMS68103A	16K x 9	
MMS68103A-1	8K x 9	
MMS68104	16K x 8	For MEK6800D2 Kit
MMS80810	32K x 8	For 8080A-based systems; pin-compatible with SBC 80/10/20
MMS80810-1	16K x 8	

†Trademark of Motorola Inc.

## Get fast delivery, proven reliability.

Our standard memory line also includes systems for the SBC 80/10 and 80/20, LSI-11, 3400N, and a variety of M6800-based systems. Motorola also has excellent custom capability for the design and manufacturing of memory systems to your exact specifications.

Regardless of your requirements, you can expect fast delivery, leadership pricing, and the high level of reliability for which Motorola products are known.

Assistance is available from your Motorola sales office. Request a copy of the MMS1117 data sheet by writing Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

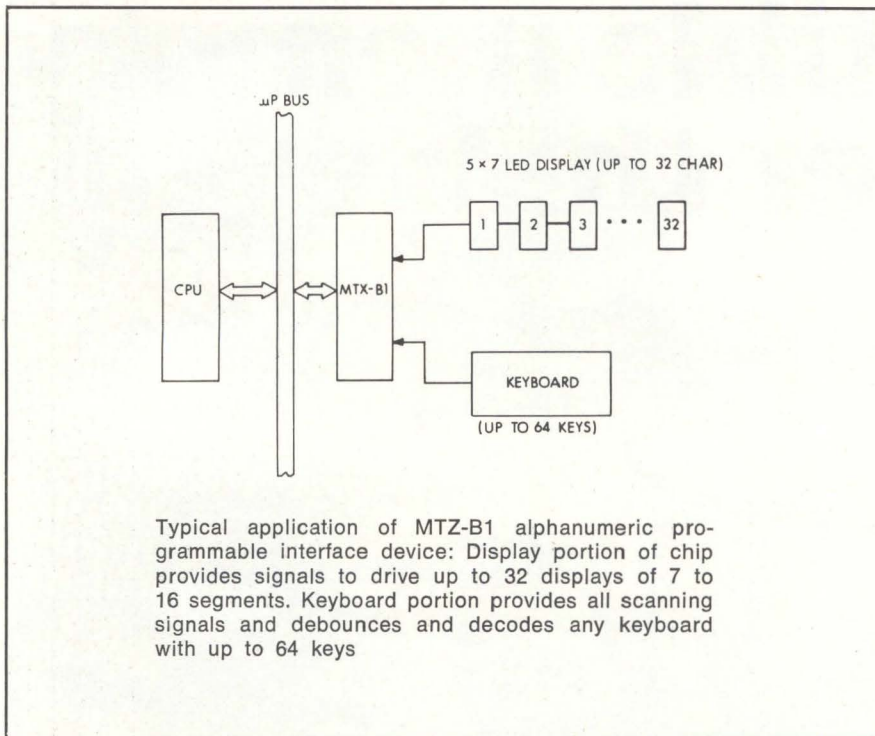
\*Trademark of Digital Equipment Corporation.

## Beep Beep!



**MOTOROLA**  
Semiconductor Group





patible, and the chip can be interfaced to any TTL, CMOS, or NMOS microprocessor through an I/O port or bus. It is available in a 40-pin standard plastic DIP.

Absolute maximum ratings include: 0 to 70 °C ambient temperature under bias; -65 to 150 °C storage temperature; 0.5 to 7 V on any pin with respect to ground; and

5-W power dissipation. Dc operating characteristics call for maximum voltages of 0.8 V (input low voltage) and 0.45 V (output low voltage), and minimum voltages of 2.0 V (input high voltage) and 2.4 V (output high voltage); maximum leakage current is  $\pm 10 \mu\text{A}$  for input and  $-10 \mu\text{A}$  for output.

Circle 354 on Inquiry Card

### LSI Circuits Allow User To Program Chip Logic

A family of bipolar circuits called PAL (programmable array logic) promise to replace up to 90% of standard TTL and to reduce random logic chip count by a 4-to-1 factor. Unit cost is said to be lower than that of microprocessors, custom logic, or FPLAS. Typical propagation/delay is 25 ns.

Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086 is currently sampling the devices and plans to start high volume production by mid-year. Full production of 15 models is expected by year-end.

With these LSI circuits, users can program their own logic on a chip—from random gates to arithmetic functions—by inserting appropriate personality cards into a standard p/ROM programmer. In this way, fusible-link

programming eliminates hardwired breadboarding required by conventional logic. A "last link" fuse, when blown, prevents verification, thus providing security for a user's proprietary algorithm.

To facilitate programming the company has developed a software program called PALASM (Pal Assembler), written in FORTRAN IV. When the user inputs his design specifications, he gets a fuse pattern and p/ROM programmer format output.

Among typical applications are programming to decode hexadecimal input signals and directly drive LED displays, with only one device per 7-segment display stage; using one device plus six octal interface devices to interconnect any S-100 bus computer and external peripheral equipment; programming to interface between any microprocessor and exter-

nal controllers; and monitoring the address bus for security checking in a data processing system. Other applications include a binary-to-BCD coder/decoder, hex keyboard scanner, 8080 or Z80 control logic, 6-bit shift register, and accumulator ALU.

Circle 355 on Inquiry Card

### Voltage-To-Frequency Converter Guarantees Temperature Drift

A second generation voltage-to-frequency converter, offering a linearity capability of  $\pm 0.05\%$  maximum, high noise rejection, and compatibility with all logic forms (DTL, TTL, CMOS), features a bandwidth of greater than 100 kHz. The RC4152, developed by Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040, is pin-for-pin compatible with the RC4151, and is available from stock in ceramic or plastic DIL or metal can packages.

This converter offers guaranteed temperature drift. Both current source and voltage reference have guaranteed maximum temperature coefficients of  $\pm 100 \text{ ppm}/^\circ\text{C}$ ; one-shot stability is rated at  $\pm 50 \text{ ppm}/^\circ\text{C}$  maximum.

The device consists of comparator, one-shot, precise gated current source output, internal voltage reference, and open-collector output. The elements, when combined with external pin connections, perform a variety of circuit functions. A few of the applications include precision V-F and F-V converters, isolation amplifiers, pulse-width modulators, programmable pulse generators, frequency scaling, and motor speed control.

Circle 356 on Inquiry Card

### Analog Input Module Compatible With Most Microprocessors

A self-contained analog input device consisting of 12-bit CMOS A-D converter, instrumentation amplifier, input multiplexer, address decoder, and control logic is available in an 80-pin quad-in-line package. The MP22, produced by Burr-Brown, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734, interfaces to most microprocessors without requiring ad-



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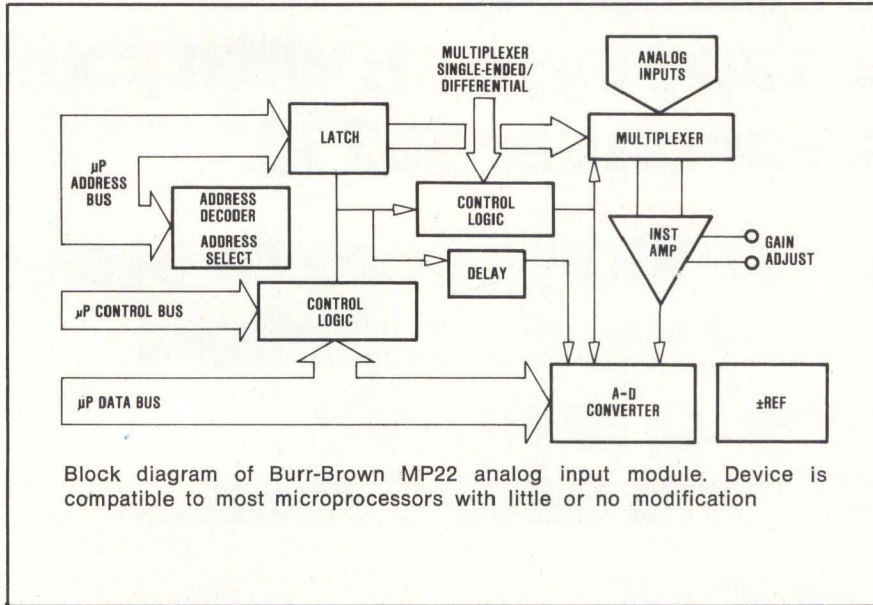
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**CIRCLE 87 ON INQUIRY CARD**



## AROUND THE IC LOOP



ditional external components. It interfaces directly with 8080A, 8048, Z80, and SC/MP microprocessors, and with

minimal external logic is compatible with 6800, 650X, F8, and 8085 microprocessors as well as PDP-8, PDP-

## MOSFET and Bipolar Combine in Dual Supply Voltage Comparators

BIMOS voltage comparators with a MOSFET input and a bipolar output on a single chip are available in either single or dual versions. Use of mos transistors in the input stage provides the user with very high impedance

( $\approx 1.7 T\Omega$ ), common mode rejection for input signals at potentials below that of the negative supply rail, and retention of the in-phase relationship of the input and output for input signals below the negative rail.

Output of the device is the open collector of an npn transistor, a feature providing flexibility in a broad range of comparator applications.

11, Nova, and Eclipse minicomputers.

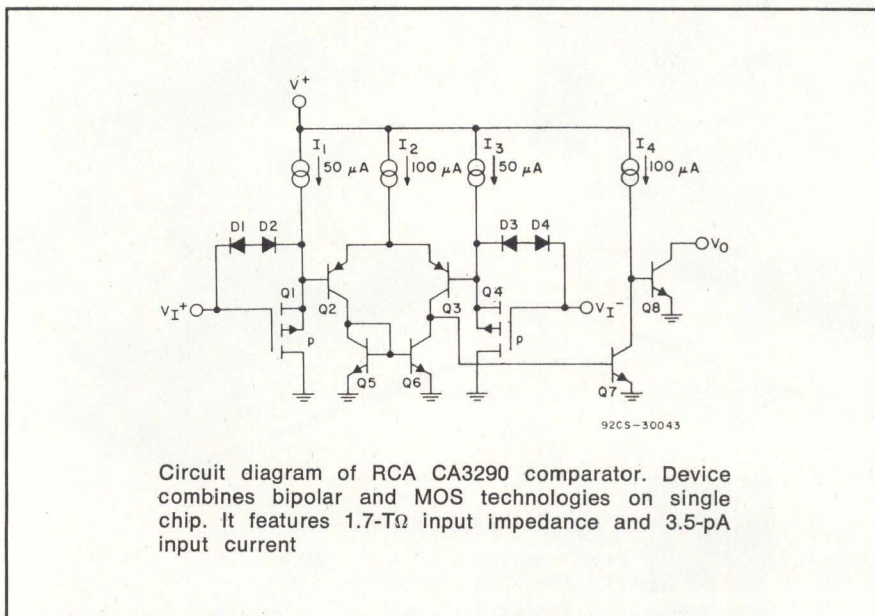
Interrupt, halt, and DMA request signals are generated by internal logic. The device accepts 16 single-ended or 8 differential analog signals and can digitize low or high level inputs.

The A-D converter is a successive approximation device offering 35- $\mu$ s conversion time and 3-state outputs. Laser-trimmed, thin-film networks are used to maintain linearity and stability over wide temperature ranges. Twelve address lines can select up to 4096 memory locations. A time delay between channel selection and start of conversion allows the analog multiplexer and amplifier to settle before conversion starts. This delay, 15  $\mu$ s, is sufficient for gains from unity to 50.

Characteristics of the low drift instrumentation amplifier include high speed at gains above unity and gain programming with an external resistor allowing input ranges as low as  $\pm 5$  mV. Gain may be selected from unity to 54 dB.

The module's control logic generates signals to halt or interrupt the CPU while conversion takes place. It also signals the CPU to indicate when data can be read.

Circle 357 on Inquiry Card



Output-oring function can be implemented by parallel connection of open collectors. Output pullup resistor can be connected to a power supply having a voltage range within the rating of the device in use; the magnitude of this voltage may be set at a value independent of that applied to the V+ terminal.

CA3290 series devices include the 3290, 3290A, and 3290B. Their manufacturer (RCA/Solid State Div, Rt 202, Somerville, NJ 08876) notes that these are the first multiple technology dual voltage comparators available from the semiconductor industry.

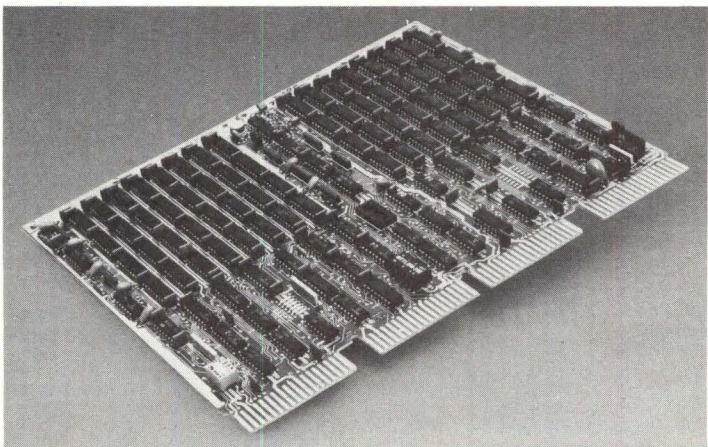
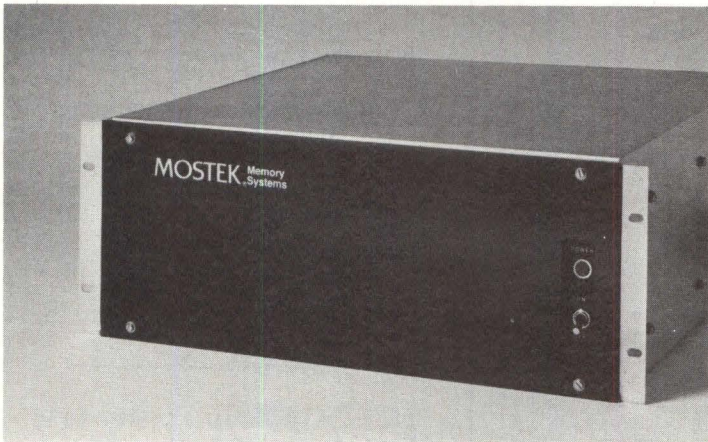
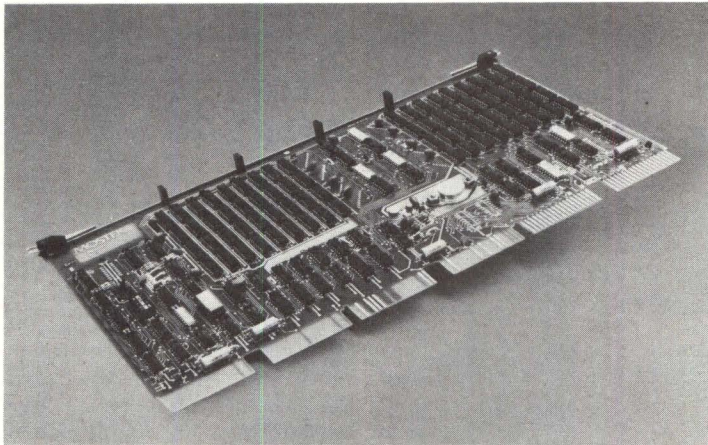
The input circuit permits a wide excursion of input voltages without need for level-shifting components. These devices are well suited for applications in long time delay circuits, square-wave generators, A-D converters, and high source impedance voltage comparators.

Other specifications include low input current (3.5 pA typ at 5 V), high speed performance (a response time of 1.2  $\mu$ s on the rising edge and 200 ns on the falling edge), and a dc supply voltage ranging from 4 to 36 V (4 to 44 V for the CA3290B). Devices are available in 8-lead DIP, 14-lead DIP, 8-lead TO-5, and 8-lead TO-5 with DILCAN.

Circle 358 on Inquiry Card



# Look to Mostek Memory Systems for density, price and delivery.



Mostek Memory Systems provides a complete line of super-dense memory boards with performance and reliability to match our industry-standard dynamic RAMs. Each board undergoes extensive burn-in and testing prior to shipment and comes with a full one-year warranty. In addition, you get highly competitive prices, OEM discounts, and immediate availability.

**PDP-11**\* The Mostek 8001 has a number of capacity options that include 16K, 32K, or 64K words by 18 bits on a single hex board. And it's fully hardware and software compatible with Digital Equipment Corporation memory modules.

**PDP-11/70**\* The Mostek 8601 memory system in a 7-inch chassis provides up to 1 megabyte of storage with ECC and logging. It's the most compact 11/70 add-on memory available, making possible upgrades from 128K bytes to 4 megabytes of total storage.

**LSI-11**\* The Mostek 8002 is a totally hardware and software compatible card for LSI-11/PDP-11/03. This add-in memory system ranges in capacity from 8K to 32K words x 16 bits on a quad card allowing you to place the maximum capacity on a single card.

Call now for the complete story. Either the Eastern office 201/842-5100, Western office 408/287-5081, or Memory Systems Marketing at 214/242-0444, extension 2552. Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006. In Europe, contact Mostek GmbH, West Germany; telephone (0711) 701096.

**MOSTEK** Memory Systems

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\* 1978 Mostek Corporation



**PLL Offers Improved Temperature Stability**

A precision phase-locked loop circuit (PLL) with ultra stable characteristics and designed for a wide range of inputs is well suited for frequency synthesis, detection, and tracking filter application. The XR-2212 PLL is directly compatible with MOS, DTL, and

TTL families and microprocessor peripheral systems.

This circuit features the following broad input capabilities: frequency range from 0.01 Hz to 300 kHz; voltage range from 4.5 to 20 V (Fig 1); and dynamic range from 2 mV to 3 V rms. It is stable over a wide temperature range, with a stability of 20 ppm/°C (Fig 2), and features quad-

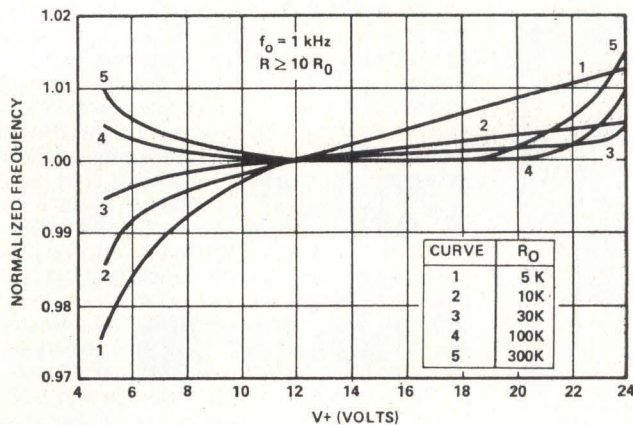


Fig 1 Typical  $f_0$  vs power supply characteristics, as function of timing resistance,  $R_0$ , for PLL. Frequency varies by only few percent over 20-V input range, and is flat over wide range for higher values of R

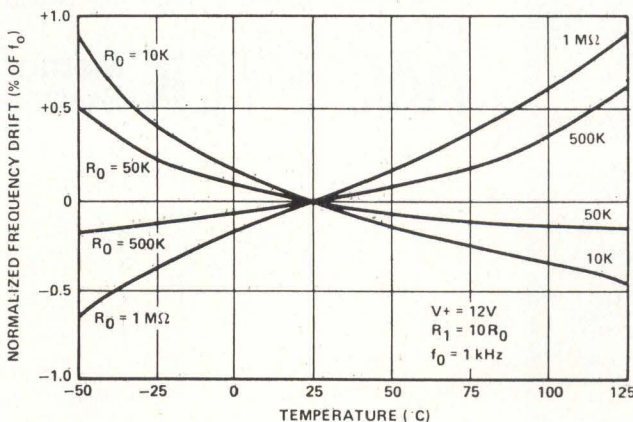


Fig 2 Typical center frequency drift vs temperature as function of timing resistance  $R_0$ . Frequency varies by less than 1% over wide temperature range

rate vco outputs and an adjustable tracking range ( $\pm 1$  to  $\pm 80\%$ ). Introduced by Exar Integrated Systems, Inc, 750 Palomar Ave, Sunnyvale, CA 94086, the 16-pin device has absolute maximum ratings of 18-V power supply and a 3-V rms input signal level.

The circuit consists of an input preamplifier, a phase detector, a stable voltage-controlled oscillator, and a high gain differential amplifier. vco is brought out externally so that the circuit can operate as a frequency synthesizer. A differential amplifier section can be used as a high speed comparator for FSK demodulation. Center frequency, bandwidth, and tracking range of the PLL are controlled independently by the choice of external components.

Circle 359 on Inquiry Card

**CMOS Latch Meets JEDEC B Specs**

An 8-bit addressable latch with parallel output storage register, the SCL 4099B is usable as a 1-of-8 demultiplexer, multiline decoder, or A-D converter. Addressing a particular bit with write disable low stores data in that bit. When write disable goes high, data entry is inhibited. Whatever the state of write disable, latching of previous data is not affected, and all eight outputs are continuously available. A master reset input resets all latches to a low level.

Supplied in a 16-lead package by Solid State Scientific Inc, Montgomeryville, PA 18936, this CMOS device is available with standard or MIL-STD-883B processing. It is a direct replacement for the CD4099B and fully complies with the JEDEC B specification.

Circle 360 on Inquiry Card

**BIFET Op Amp Features Low Input Offset Voltage**

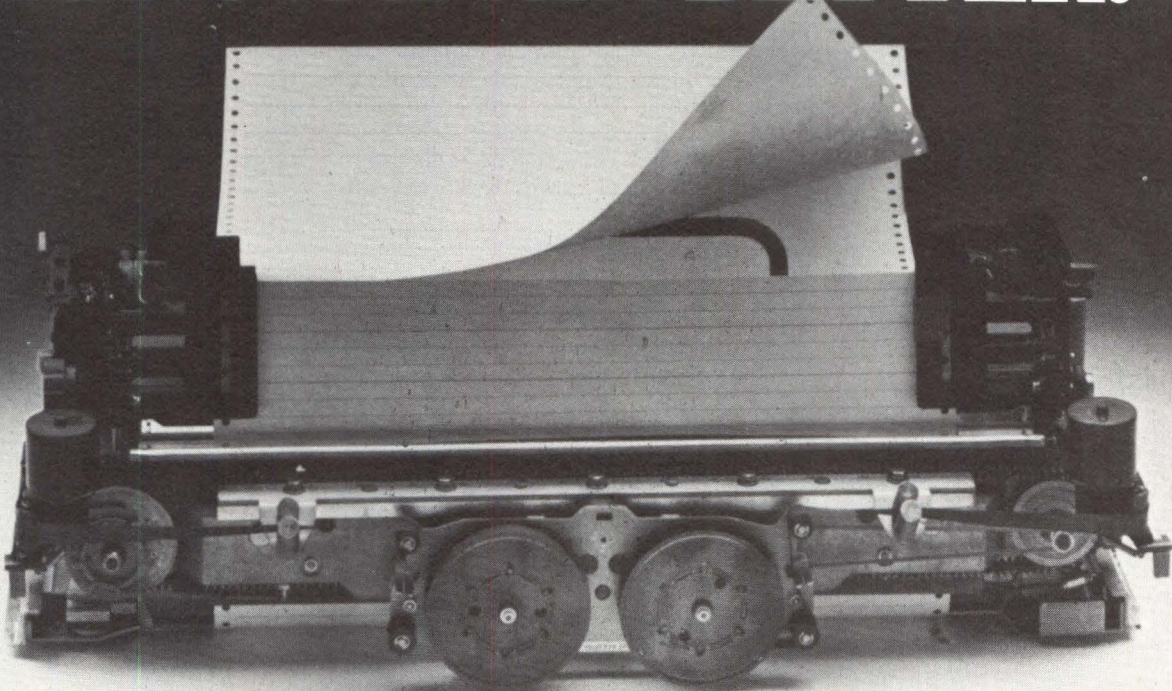
Low input offset voltage (0.5 mV max) is featured in a BIFET op amp that also features internal frequency compensation and high slew rate of 13 V/ $\mu$ s. The device has an input bias current of 0.2 nA, input offset current of 3 nA, and offset voltage temperature coefficient of 10  $\mu$ V/°C.

The TL087C is produced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222. It is available in either an 8-pin plastic (P suffix) or ceramic (JG) dual-in-line package and operates over a 0 to 70 °C temperature range.

Circle 361 on Inquiry Card



# THE BEST 300 LPM PRINTER ON THE MARKET IS NOW EVEN BETTER.



In order to build up a customer base of more than 40,000 units in three years, you have to have a superior printer. And no matter how you look at it, the Teletype\* model 40 printer has a lot going for it.

Look at cost. Nowhere does anyone offer as much in a 300 LPM printer for as little as the model 40 costs. At the OEM price of under \$2000, it even compares favorably against low-speed printer costs.

Look at reliability. The model 40's unique design utilizes a minimum of moving parts for a maximum of on-line time. Plus proven LSI (Large Scale Integration) circuitry handles many functions formerly performed mechanically. This reduces hardware requirements and increases printer life.

Look at features. The unit is completely operational to give you everything necessary to go on-line. You also get 32 switch-selectable no-cost options to choose from, easily changeable character sets, and self-diagnostics.

Finally, look at product support. Not only do we offer nationwide service, we'll maintain your printer for as little as \$23 per month—and that includes labor and material.

With all that going for the model 40, how could we make it even better? Two ways.

First, we gave it a new, simplified OEM interface. Simply command the motor on, watch for the next character command, and send data.

Next, ribbon life has been significantly extended with our new re-inker mechanism that's available as a low-cost option.

No wonder we're getting a reputation as the OEM printer people.



**THE OEM PRINTER PEOPLE**

\*Teletype is a trademark and service mark of the Teletype Corporation.

CIRCLE 68 ON INQUIRY CARD



**ICs Provide Tones for DTMF Telephone Dialing**

Integrated tone dialers provide eight different audio sinusoidal frequencies that are mixed to provide tones usable for dual tone multifrequency (DTMF) telephone dialing. Both MK 5087 and MK 5089, available from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, use an inexpensive 3.579545-MHz television color burst

crystal as a frequency reference. The user can build tone dialing circuits without trimming or expensive frequency adjustment.

The MK 5087 was designed for integrated tone-dialer applications that require wide supply operation with regulated output, opposite-polarity logic outputs (one with push-pull output and one with open emitter output), single contact static keyboard inputs, single tone inhibit option, operation down to 3.5 V, and

the U.S. standard 2500-type hybrid network. The MK 5089 was designed for integrated tone-dialer applications that require wide supply operation, negative-true keyboard input, chip disable input, stable-output tone level, an "any key down" output that is open circuit when no keyboard buttons are pushed and pulls to the V- supply when a button is pushed, and operation down to 3 V, with low distortion.

Circle 362 on Inquiry Card

**ADC Available for High Speed Industrial Data Acquisition Applications**

Features of a 12-bit A-D converter include 8- $\mu$ s conversion time, optional input buffer amplifier, and five user-selectable input ranges. Both internal and external clock options are available to the user. MNADC85 is guaranteed to have no missing codes over an operating range from -25 to 85 °C. Its manufacturer, Micro Networks

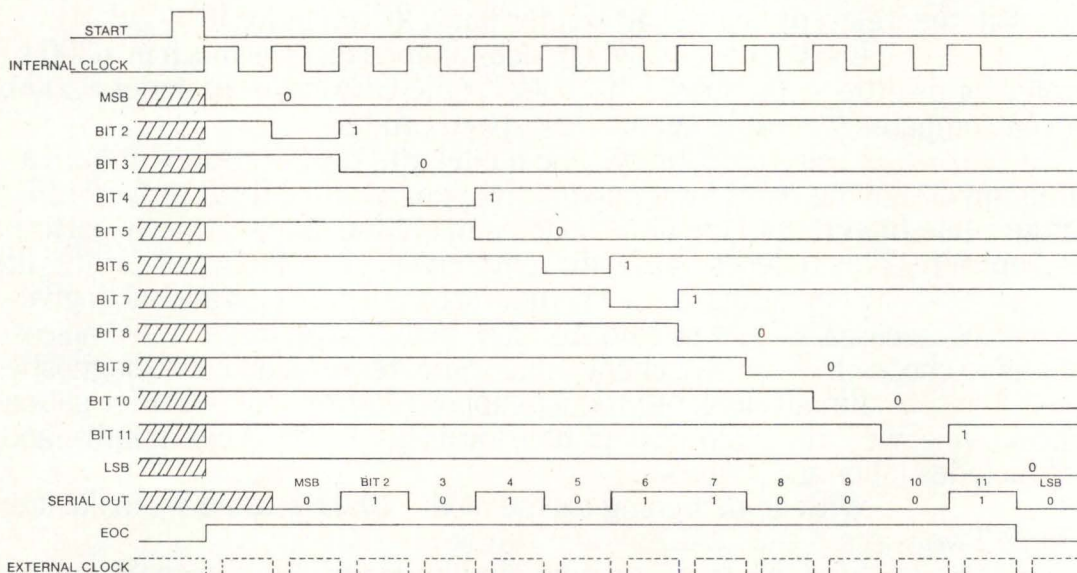
Corp, 324 Clark St, Worcester, MA 01606, states that it meets or exceeds published specifications of Burr-Brown's ADC85, offering a 2  $\mu$ s faster conversion time and a significantly lower power consumption.

Both serial and parallel data outputs are included. The device provides a status output for interfacing in microprocessor-based applications.

Applications include biomedical equipment, industrial controls, and

data acquisition systems. For data acquisition, the ADC can be used with the MN7130 multiplexed sample/hold amplifier to configure a complete 16-channel data acquisition system in two dual-in-line packages.

Specifications call for analog input ranges of  $\pm 2.5$ ,  $\pm 5$ , or  $\pm 10$  V (bipolar) and 0 to 5 or 0 to 10 V (unipolar). Maximum digital input pulse width is 50 ns. The device is packaged in a small, hermetic, 32-pin DIP.



Timing diagram for Micro Networks high speed ADC. Output code shown is for digital word 0101 0110 0010, corresponding to analog input of 6.633 V on 0- to 10-V input range. Start command must be at least 50 ns wide and must remain low during conversion. Data will be valid 30 ns after end-of-conversion signal (EOC) goes low and will remain valid until start of next conversion cycle. For external clock, serial and parallel outputs will be synchronous with falling edge of clock

Circle 363 on Inquiry Card







## PRODUCT FEATURE

# Office Environment, 300-Line/Min Printer Maintains Self Diagnosis



Dual microprocessors that communicate through interrupts and command words share control of the T-3300, a 300-line/min printer based on a patented comb matrix mechanism. One 8085 microprocessor controls print functions via a print bus; another controls I/O, status, and diagnostic functions along an I/O bus. Interconnection between buses is by data and status lines.

Offered in both freestanding and desktop versions, this first of an expected series of printers from Tally Corp is designed for the office environment, with emphasis on human engineering requisites. Yet it mixes service related diagnostic aids with operator convenience features.

### Functional Description

Main memory associated with the print control microprocessor (CPU) is preprogrammed to perform all basic printing functions. However, flexibility is achieved through programmable read-only memory (p/ROM) associated with the I/O control microprocessor. The print control CPU handles paper advance and ribbon motors as well as dot row and column, character generator, and counter/timer functions. Variations in character generation, vertical for-

mat unit (VFU) control, interface control, control of options, and diagnostic functions are handled by the I/O CPU, chiefly through use of "snap-in" modules or p/ROMs that enable the printer to be tailored to any application.

The character control p/ROM can be programmed to allow any ASCII character to be interpreted as any other; eg, an "A" input could be interpreted under p/ROM instructions to be an order to perform a line feed. More normal variables, such as print on paper motion, are defined by an option p/ROM. Unique applications

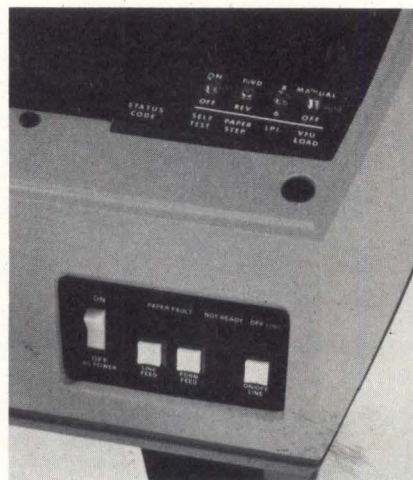
when required can be handled by adding two patch program p/ROMs.

Special driver circuits, terminations, and similar provisions can be added through a custom printed circuit board. One such board, for example, contains long line driver circuits for use with parallel interfaces.

Diagnostic procedures handled by the I/O CPU begin with a self-test to verify hardware, RAM, and software for both CPUs. If each CPU proves to be performing properly, the I/O CPU is used to troubleshoot the remainder of the printer. However, if a CPU is found to be defective, the relevant CPU board is replaced or repaired before further tests are performed.

A 2-digit status display on the printer front panel (see closeup photograph) distinguishes between operator correctable faults and those that require service. It also displays the response to many maintenance routines for quick fault isolation. Six operator-correctable and 23 service-correctable indications are programmed.

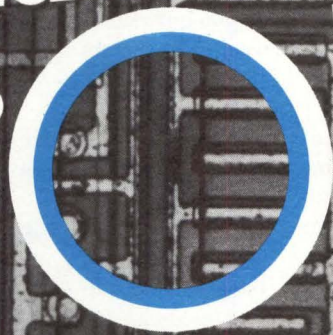
In addition, the self-test procedure checks operation of indicators, switches, and motors. It will also access all I/O lines and print out the contents of the option p/ROM. Seven separate patterns can be printed, allowing precise examination



Close-up view of T-3300 controls



# Effective Shielding Could Have Prevented This IC Burn Out



Micro-min electronics in low power, complex digital circuitry is increasing rapidly in EDP mainframes and peripherals.

But, acrylics, wools, silks and moving nylons in a computer room can yield a good combination for serious problems...increased susceptibility to static charges. A few steps and a spark from body to computer cabinet is all it takes to produce a charge as high as 30,000 volts. And, if the cabinet and/or components are poorly grounded, the charge can be transmitted to components causing overloading and circuit malfunction.

## **Metex Shielding Provides Ideal Protection from Low Signal IC Overload**

Metex shielding products such as Combo Strip® Gasketing, Xecote™ Conductive Coating and Xecon® Conductive Elastomer protect your

equipment by shielding it from this predatory energy...keeping it away from digital IC's and other vulnerable components.

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Viewing screens, air vents, cabinet slots and any other enclosure openings are access points for EMI/RFI energy. Easily picked up by sensitive components by induction, EMI/RFI radiation can cause distortion of low power signals and overloading of subsequent circuits. This may lead to IC degradation, or catastrophic failure.

Metex provides Shield-Vu® Shielded Windows of any size or shape, constructed of finely knitted wire fused between panes of acrylic or glass, that offer effective attenuation with over 90% visibility. We also make air intake and exhaust vents

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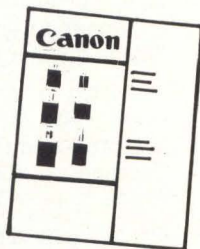
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of print registration, character quality, and overall system operation.

Ribbon system power supply, CPU board, and print mechanism are individual modules that can be easily removed and replaced. Quick-disconnect cables also permit various VFU modules to be readily interchanged.

The print mechanism has only two moving parts: a paper advance assembly that controls paper motion, and a single-piece oscillating comb, with a hammer for each of 132 print positions, that prints one horizontal row of dots at a time. Characters are formed with an overlapping dot pattern.

There are no lubrication points, electronic timing, or hammer flight time adjustments and, therefore, no preventive maintenance. High failure rate parts such as clutches, belts, brakes, and chains have been eliminated.

The matrix scanning technique uses a flexure conversion in which rotary stepping motor motion is transformed into a linear horizontal scan motion. A flexible steel band clamped to the motor shaft oscillates over a 15-deg arc, causing the attached print comb to mogate (oscillate) horizontally. Total horizontal travel is limited to the width of a single character.

### Specifications

Standard ASCII characters (96-char set) are formed over 132 columns by a 7 x 7 dot matrix at 10-char/in (4/cm) horizontal spacing with selectable 6- or 8-line/in (2.4 or 3.4/cm) spacing. Character size is 0.062 x 0.096" (1.6 x 2.4 mm) with a nonaccumulative vertical and horizontal print registration of  $\pm 0.005$ " (0.127 mm). A 7 x 9 matrix (for descenders), underlines, and custom character sets and sizes are available options. Single line advances (no print cycle) require a maximum of 35 ms; slew speed is 10 in (4 cm)/s.

Forms from 4 to 15.8" (10.2 to 40.1 cm) wide having standard business machine pinfeed are handled by adjustable pinfeed tractors with a minimum of five feedholes engaged at all times. As many as five copies plus original can be made on forms up to 0.024" (0.61 mm) thick. Paper advance speed is 12 in (30.5 cm)/s minimum (60 lines/s).

Vertical format is controlled by a forms length selector switch, 8- or

12-channel VFU loop, or direct access electronic VFU loaded through the I/O. Fine adjustment to the paper position is made electronically, one dot row at a time, using a control panel switch. Although an audio alarm sounds when the printer reaches 3" (7.6 cm) from the bottom of the form, printing can continue to the last line position on the forms, at which point printing is inhibited.

A reel-to-reel ribbon system is used, with a self-threading leader. The reusable fabric ribbon has a minimum life expectancy of  $20 \times 10^6$  characters.

Centronics, Dataproducts, Data Printer, and serial interfaces are available in addition to a standard Tally parallel interface. Interface electrical levels are: logic 0 (low), 0 to 0.8 Vdc at 1.6-mA sink; logic 1 (high), 3.0 to 5.0 Vdc at 400- $\mu$ A source.

Field-selectable input voltages are 100 V  $\pm 10\%$ , 117 V  $\pm 10\%$ , and 220 V  $\pm 10\%$  -15%, all at factory-set optional 50 or 60 Hz  $\pm 2\%$ ; and 240 V  $\pm 10\%$  at 50 Hz  $\pm 2\%$ . Power requirements are 800 W nominal, 1450 W maximum.

Operating temperature range is 40 to 100 °F (5 to 37 °C), 10 to 95% relative humidity, noncondensing. Storage range is 0 to 145 °F (-17 to 62 °C). The unit can be operated at altitudes up to 10,000 ft (3 km). Acoustic noise generated by the printer does not exceed 65 dB(A), and is below the NC 55 curve, while printing a 64-char ASCII pattern on single-part paper [measurements taken at 5 ft (1.5 m) above the floor and 3.3 ft (1 m) from the equipment].

Unit dimensions are 32 x 20 x 43" (81 x 51 x 109 cm) for the freestanding unit and 32 x 26 x 13" (81 x 66 x 33 cm) for the desktop version. Weight is approximately 170 lb (77 kg).

### Price and Delivery

T-3300 printers with Dataproducts or Centronics interface, complete self-diagnostics, 96-char ASCII set, and 12-channel direct access vertical format unit are priced at \$6100 for the end user. OEM discounts are available. Delivery is 90 days ARO. Tally Corp, 8301 S 180th St, Kent, WA 98031. Tel: 206/251-5500.

**For additional information circle 199 on inquiry card.**



# You won't believe our Ballistic™ Printer until you see one in print. And in person.



Unless you've been in hiding, you've probably heard about LSI's family of Ballistic Printers. Built with the same proven dependability of the Dumb Terminal and his Smarter Brothers.

Our latest matrix printer, the 200A, comes with standard features like a Space and Blank Character Compression Buffer. Tabbing over Blank Spaces ability. Half Duplex or Full Duplex Operation. And a fully buffered input, optionally expandable to 1024 characters. Not to mention its microprocessor versatility, and firmware flexibility.

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The Ballistic Printer uses a five-start lead screw and servo to print bi-directionally at 180 cps. Direct, simple, positive. And very accurate.

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CIRCLE 93 ON INQUIRY CARD

191



## PRODUCTS

### Computer Controls Digitizer Functions to Receive Continuous Tone Image of Real World Events

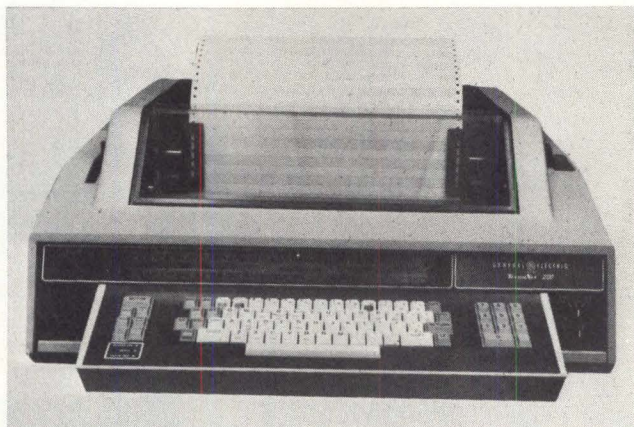
Creating a 32 x 32 element picture that is accepted by most computer systems, the type 511 optical image digitizer permits the computer to perceive events and artifacts in the real world. The host computer controls all functions of the digitizer. Integration time variations permit electronic adjustment of sensitivity by the host. Repetitive scans of the scene at different exposures generate a series of images that produce continuous tone images when combined. Housed in an aluminum case, the 8.2- x 4.0- x 2.5-cm unit (excluding lens and connector) has an integral 1/4-20 thread for mounting. The fast (f1.9/13-mm) lens focuses from 0.2 m to infinity for use in robotics and process control. Sensitivity is equivalent to ASA 200 emulsion. **Periphicon**, PO Box 324, Beaverton, OR 97005.

Circle 200 on Inquiry Card



### Matrix Impact Printers in Interactive and Line Printer Versions Operate at up to 1200 Baud

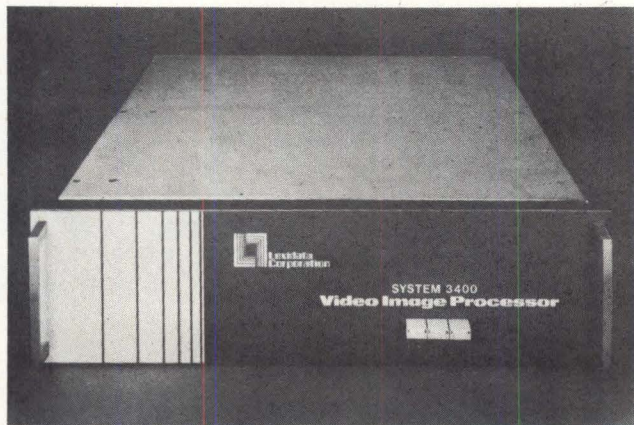
The self-contained TerminiNet™ 200 teleprinter series consists of an interactive KSR unit mated with an RO configuration that can be modified into a line printer. Serial asynchronous transmission is at 110, 200, 300, and 1200 baud, full or half duplex. The unit prints a line of up to 136 char, 10 char/in (4/cm), with 3 other print compressions as well. The 6-pin tractor impact print mechanism with straight wires, ballistic firing, and laminated core has a 7 x 9 matrix for single and multiform usage. Features include servo control of carriage and paper advance, 20-in (51-cm)/s slew rate, 1k buffer, selectable vertical spacing, bidirectional printing (line printer only), vernier tractor adjustment, handling of 2 to 16.5" (5 to 42 cm) paper widths, and the company's Mobius loop ribbon cartridge. **General Electric Co, Data Communication Products Business Dept**, Waynesboro, VA 22980.



Circle 201 on Inquiry Card

### Raster Scan Graphics and Imaging System Doubles Speed of Random Image Updating

System 3400 video image processor features 750-ns/pixel random updating that is twice as fast as other raster scan systems. Suited to dynamic imaging and graphics applications, the tool has such functions as high speed blinking between 2 or more images, side-by-side display of up to 20 64 x 64 images, zoom, 4-directional scrolling, or inverting the displayed intensity. Single-chassis unit with self-contained power supply and cooling can be configured as a 320 x 256 pixel display by up to 16 bits of memory/pixel. A company-designed 80-ns cycle time 12-bit microprocessor works with a memory controller. Up to 8 CRT outputs are generated by 1 system. B/W, gray scale, or color output is available, with 3 lookup table options. It interfaces to any 8-, 16-, or 32-bit host computer over DMA, command I/O, or RS-232 links. **Lexidata Corp**, 215 Middlesex Tpk, Burlington, MA 01803.



Circle 202 on Inquiry Card



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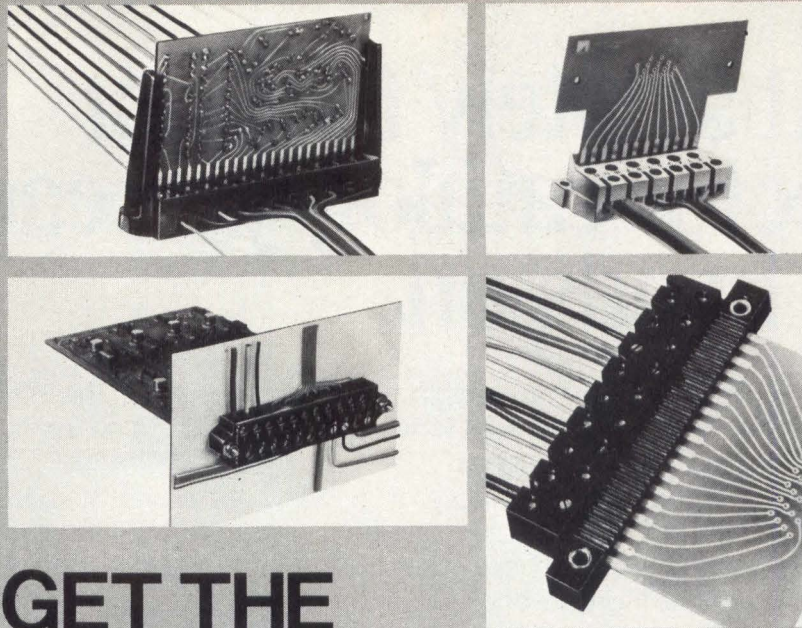
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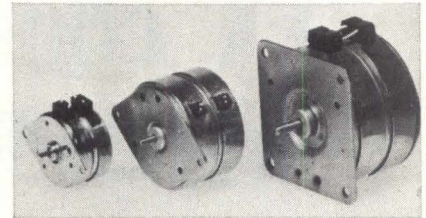
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\*U.S. Patent No. 3,930,706.  
Other patents pending.



## PRODUCTS

### PERMANENT MAGNET STEPPING MOTORS

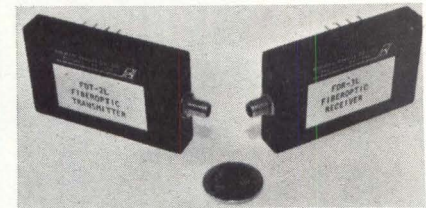


High quality permanent magnet motors are available in stepping angles of 7.5, 9, 11.25, and 15°. Design features include choice of std dual self-aligning sleeve bearings or optional dual ball bearings. Construction assures performance in applications where extremes in duty cycles, temp ranges, or mechanical shock loads must be met. Torque ratings range from 0.6 to 21 oz-in based on motor size and step angle desired. Stepping rates up to 2000 steps/s are possible. **Berger-Lahr Corp**, Peterborough Rd, Jaffrey, NH 03452. Circle 203 on Inquiry Card

### DMA LINE PRINTER CONTROLLER

1200 series controller interfaces Data General Nova and Eclipse CPUs to Dataproducts 2200 series printers and Data Printer Chaintrain printers. Transparent to existing software, controller is contained on a single 15 x 15" (38.1 x 38.1-cm) PC board, and occupies 1 I/O slot in computer. It incorporates all circuitry needed to effect full-word data transfers via high speed data channel on a cycle stealing basis. **Digital Associates Corp**, 1039 E Main St, Stamford, CT 06902. Circle 204 on Inquiry Card

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FIBERCOM<sup>™</sup> FDT and FDR series feature immunity to electrical interference, broad bandwidth over great distances, and elimination of ground loops. RS-232, 422, and 423, and MIL-STD-188 line receivers and drivers are built-in options. With an IR LED wavelength of 880 nm std (820 nm optional), 4 receivers and 1 transmitter cover in 4 bandwidths from dc to 10M bits/s RZ or dc to 20M bits/s NRZ over distances to several kilometers with bit error rates <math>10^{-12}</math>. **Radiation Devices Co, Inc**, PO Box 8450, Baltimore, MD 21234. Circle 205 on Inquiry Card



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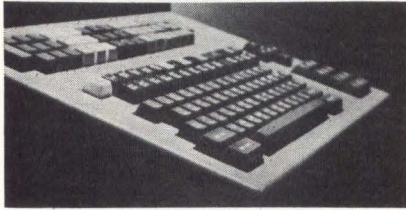
SBS:crs

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## PRODUCTS

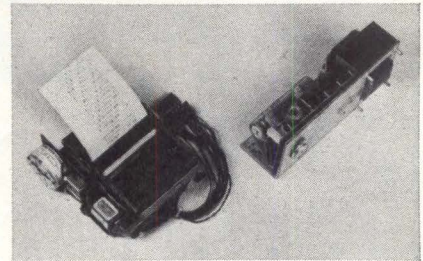
### COLOR GRAPHICS DISPLAY SYSTEM



Model 5217 single-channel display generator, including dual RS-232 interfaces, p/ROM programmed microprocessor, and power supply, is contained within the operator's keyboard. Any RS-170 compatible monochrome or color CRT monitor may be used with this unit. It features 8 colors; 256 char and symbols; individual char control of color, blink, intensity, size, normal or reverse video, and protect; and full edit capability. Display format is 80 char/line x 48 lines/page. **Aydin Controls**, 414 Commerce Dr, Fort Washington, PA 19034.

Circle 206 on Inquiry Card

### MECHANISMS/CONTROLS FOR IMPACT COLUMN PRINTERS



A family of elements to provide inexpensive column printing includes series PR15 and PR21 impact printing mechanisms for 15 and 21 col, respectively; a Mostek 3870-based interface/controller model 4-621-9210; F8-based interface/controller model 4-621-9205; system power supply model CP242; and separate programmed 3870 chips. The resultant system accepts ASCII, RS-232-C, or BCD data formats, and prints at 1.5 (alphanumeric) or 3 lines/s (numeric). **Sodeco, div of Landis & Gyr, Inc.**, Elmsford, NY 10523.

Circle 207 on Inquiry Card

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±12V ADC80: 10 and 12 bits, 25  $\mu$ sec max conversion time, ±1/2 LSB non-linearity, internal reference, clock and comparator. Price: (100's) \$49.50.

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**BURR-BROWN**



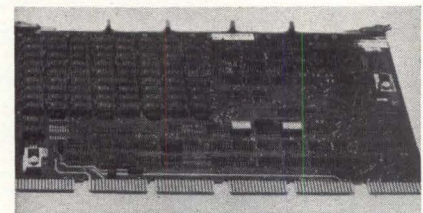
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### SINGLE-AXIS POSITION SENSOR

PIN-LSC/30D is a Schottky barrier diode with an active area of 1.22 cm<sup>2</sup>. As a light spot moves across this area, electrical currents are generated which are proportional to distance from contact point to light spot, providing linear real-time analog information on both location and movement in a single axis. Sensor provides continuous position signal with accuracy independent of light spot size. Spectral range is 350 to 1100 nm. Responsivity is 0.55 A/W at 850 nm (pk). **United Detector Technology, Inc.**, 2644 30th St, Santa Monica, CA 90405.

Circle 208 on Inquiry Card

### 32k SEMICONDUCTOR MEMORY FOR PDP-11



Single-card Add-In-11 memory system that plugs directly into a single card slot of DEC PDP-11/04 and 11/34 minicomputers provides 32k x 18 bits of dynamic MOS memory. It allows memory expansion in 32k-word increments to the computer's limits. Fully hardware and software compatible with the 11/04 and /34 modified Unibus, the unit has onboard parity generation and checking circuits, and control status register, which holds any detected parity error. **Fabri-Tek, Inc.**, 5901 S County Rd 18, Minneapolis, MN 55436.

Circle 209 on Inquiry Card



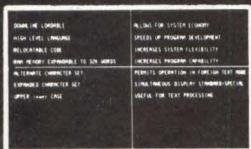
# DELTA DATA introduces a new era in video display terminals

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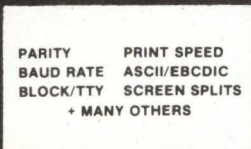
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processing and office environments  
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*A powerful, high performance  
terminal that offers an intelligent  
choice for your special terminal  
requirements.*

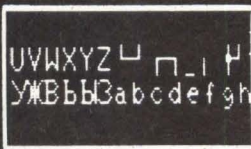
Introducing the new DELTA 7000 Series. A family of intelligent terminals which combines the latest 16-bit micro-processor technology with our own proven video display technology. We designed the DELTA 7000 with your interests in mind—from data communications (TTY/IBM 3270 emulation) to specific applications (Text Processing). Then we built in many special features, and loaded the DELTA 7000 with memory to handle your unique applications programs—at a most attractive price.



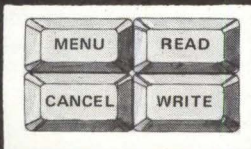
**MULTIPLE SPLIT SCREEN**  
allows you to divide the  
screen into independent  
display areas



**ELECTRONICALLY  
ALTERABLE ROM**  
allows status to be set from  
keyboard or remotely, and  
retained during power off



**EXTENDED  
CHARACTER SET**  
generates special fonts  
and displays up to 672  
different characters



**MULTI-CHARACTER  
FUNCTION KEYS**  
permit one key to display  
or send a string of multiple  
characters or codes

Enter your new era in video displays  
with the new DELTA 7000. Write or  
call for more information today.



Woodhaven Industrial Park  
Cornwells Heights, PA 19020  
(215) 639-9400

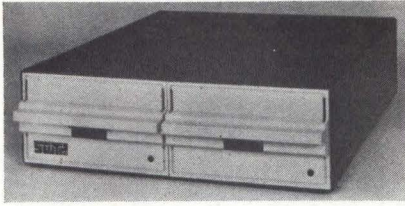
U.K. Subsidiary:  
DELTA DATA SYSTEMS LTD.  
Welwyn Garden 33833

Service in over 150 locations in the U.S. and  
14 European countries and Canada.



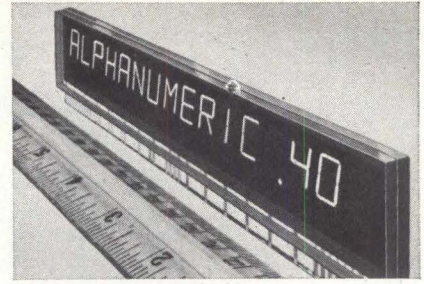
## PRODUCTS

### DUAL DRIVE FLOPPY DISC SYSTEM



Hardware for DMAF1, a single-density, double-sided 8" (20.3-cm) disc system, consists of SS-50 bus compatible DMA controller capable of handling up to 4 drives and 2 143M double-density rated disc drives. System is housed in a 5.375 x 17.125 x 20.5" (13.653 x 43.498 x 52.1-cm) aluminum chassis with regulated power supply, drive motor control board, cooling fan, diskette, and interfacing cables. Software includes micro-computer disc operating system, and an 8k BASIC interpreter. **Southwest Technical Products Corp.**, 219 W Rhapsody, San Antonio, TX 78216. Circle 210 on Inquiry Card

### PLASMA PANEL DISPLAYS

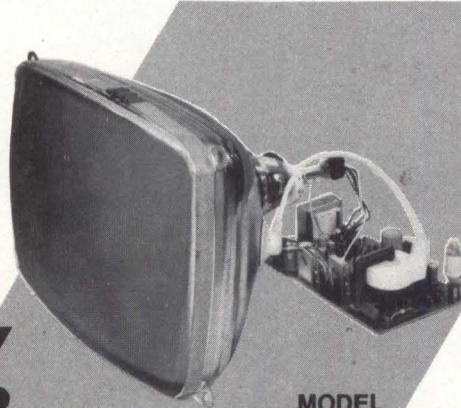


Two series of 16- and 14-char alphanumeric plasma displays with 0.400" (1-cm) and 0.500" (1.3-cm) char heights, respectively, operate at a typ peak current of 630  $\mu$ A/segment and at a temp range of 0 to 55 °C. Typ light output is 50 ft-L and viewing angle is 130 deg. Type PD-14A050 and -16A040 utilize a long-life cold cathode, neon gas discharge display panel design. Char segments are bused together internally for multiplexed operations. **Dale Electronics, Inc., Display Dept.**, Box 609, Columbus, NE 68601. Circle 211 on Inquiry Card

Direct from Tokyo

## 12" CRT DISPLAY MONITOR

Compatible with  
TV12 or TV120  
Priced Below the  
Competition  
Built-in Quality,  
Performance,  
Dependability



MODEL  
CIQDM-12 (Kit)

The low-cost CIQDM-12 CRT Display Monitor provides data equipment manufacturers with sharp, highly reliable image presentation.

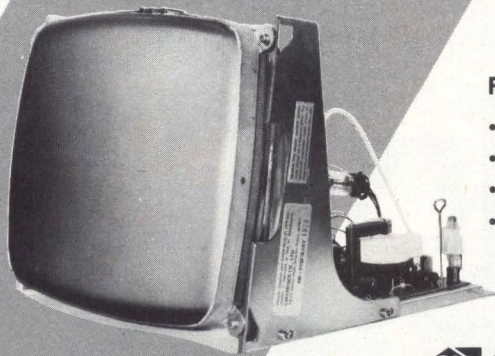
Separate horizontal drive, vertical drive, and video signal inputs mean elimination of composite sync and video signal processing and simple output circuitry.

The completely new design of the compact integrated PCB utilizes the latest semiconductor and other components, providing a dependable performance level never before possible.

Delivered with P4 phosphor as standard. Available options are P31 and P39 phosphors, sturdy zinc chromate plated chassis and a power supply module which is compatible with practically any power supply standard in the world.

### FEATURES

- Uniform High Resolution
- Integrated PC Board
- Dependable Construction
- Squareness of Picture



MODEL CIQDM-12C  
(with optional chassis)

### C. ITOH ELECTRONICS, INC.

5301 Beethoven Street Los Angeles, Calif. 90066  
Telephone: (213) 390-7778 Telex: (WU) 65-2451

280 Park Avenue, New York, NY 10017  
Telephone: (212) 682-0420 Telex (WU) 12-5059

### INTERACTIVE DATA BASE MANAGEMENT SYSTEM

Infotrieve™ and Informat™ facilitate maintenance and management of large or small Nova-based data bases. When used in conjunction with Iris™ operating system, Infotrieve, a CRT-oriented query system, operates on formatted, contiguous, and indexed random files. It requires no memorization of grammatical formats or protocols. Informat is a general-purpose report writer which utilizes selection facilities of Infotrieve and extends its report writing facilities. **Educational Data Systems, Inc.**, 1682 Langley Ave, Irvine, CA 92714. Circle 212 on Inquiry Card

### DATA TRANSMISSION TERMINAL



Error-protected BiSync or SDLC formats incorporated in the digital mag tape system enable increased throughput efficiencies at rates to 56.2k bits/s. Standalone model 7300 transmits IBM format data via DDD, WATS, leased, or private line links. Database protection ranges from simple char parity to selected repeat ARQ. Error checking is provided on char or block basis. Unit also contains a single-chip LSI micro-processor and self-test capability. **Quad Systems, Inc.**, 11900 Parklawn Dr, Rockville, MD 20852. Circle 213 on Inquiry Card



# For Intelligent Family Planning

# Think Ontel

Buying intelligent terminals . . . think Ontel! We've planned and engineered our family of intelligent terminal systems to meet maximum OEM user needs. With the recent introduction of the Ontel OP-1/R, the first truly user-programmable intelligent terminal in its price range, we've broadened our product family. We now offer powerful cluster systems. Master terminals coupled with intelligent slaves provide unique distributive processing capabilities.

Ontel terminals are more than just well-designed, flexible and reliable . . . they're low-cost total systems all engineered to complete *your* systems family.

#### **Buying Intelligent Terminals? Think Ontel!**

Supplying the software you need is a must. We offer 3 high level languages, forms generation, word processing, text editing, extensive utilities and diagnostics . . . all running under Ontel's Disk or Diskette Operating System. Ontel software enables our users to reduce their development costs for a multitude of different applications.

A few more facts. Ontel terminals have a modular structure with up to 64K of memory and are designed for field upgrade. They're easily programmed and have a full range of controllers including communications, mass storage and printer interfaces.

**Contact Us Today For the Intelligent Answer**

Edward J. Heinze  
National Sales  
Manager

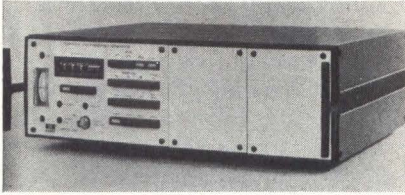
**Ontel Corporation**  
250 Crossways Park Dr.  
Woodbury, NY 11797  
(516) 364-2121





## PRODUCTS

### DIGITAL SYNTHESIS WAVEFORM GENERATOR

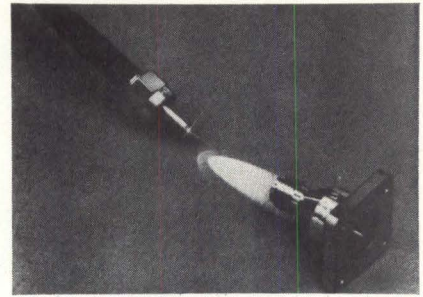


Model 350 precision low frequency generator uses a crystal-controlled clock and digital synthesis techniques to generate sine, square, triangle, ramp, haversine, haversquare, havertriangle, and inverted waveforms. 9 frequency ranges with 3-digit resolution provide an overall frequency range of 10 nHz to 999 Hz. When operating in ramp or triangle mode, min step amplitude is 50  $\mu$ V/step at max signal amplitude of 20 V pk-pk. In sine mode, min step phase angle resolution is 0.00045° (1.62" of arc).

**Exact Electronics, Inc.**, 455 SE 2nd Ave, Hillsboro, OR 97123.

Circle 214 on Inquiry Card

### FIBER-OPTIC COMMUNICATION DATA CABLE



With 0.204-mm fiber core and 0.48-mm numerical aperture, 3000-LC cable yields superior coupling efficiency to commercially available std connectors, and is suited for optical data links operational to 330 m. Single fiber, step index optical communication cables are available in 4 std jacket configurations. High temp strengthened cables and hybrid configurations combining electrical wire and fiber optics are also available. **Galileo Electro-Optics Corp.**, Galileo Pk, Sturbridge, MA 01518.

Circle 215 on Inquiry Card

# NOVA & ROLM users ...here's plug compatible cartridge storage



### CARTRIDGE TAPE DRIVE THE MODEL 650 PROVIDES:

- 30 IPS Read/Write, 90 IPS Rewind/Search
- 48,000 Bits/Sec Transfer Rate
- 2.5+ Megabytes per cartridge
- Small Size—Rugged Design

### TAPE STORAGE SYSTEMS

- Model 2200—1 or 2 Tape Drives in 5" package
- Model 2400—Up to 8 Tape Drives in 9" package
- Model 2710—Portable Recording System with up to 2 Drives
- Model 86008 Formatter—Used in all Tape Storage Systems. Complete ANSI compatibility with powerful data handling features.

### INTERFACES

All tape systems are available with the following controllers: PDP-11/LSI-11/NOVA, ROLM/INTERDATA/ALTAIR/8080/RS232/NTDS.

For more information, call us today.

**Qantex** DIVISION  
NORTH ATLANTIC INDUSTRIES, INC.

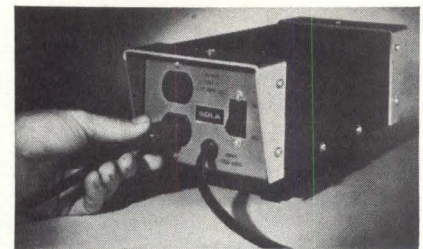
200 TERMINAL DR., PLAINVIEW, NEW YORK 11803 • 516-681-8350 • TWX: 510-221-1879  
See us at NCC—Booth 1213-1215

### 300-BAUD PAPER TAPE TERMINAL

DLC 3000 can be connected to 300-baud printers, visual display units, and other equipment via an RS-232-C interface to provide ASR capability; it can also stand alone to send and receive data, and to punch and duplicate tape. Punch/reader mechanism is available separately to OEMs. Terminal's floor-standing pedestal package utilizes <1 ft<sup>2</sup> (0.09 m<sup>2</sup>) of floor space. Std switch settings include half or full duplex, and 110 or 300 baud. **Drillick LaManna Corp.**, 280 Midland Ave, Saddle Brook, NJ 07662.

Circle 216 on Inquiry Card

### POWER REGULATORS



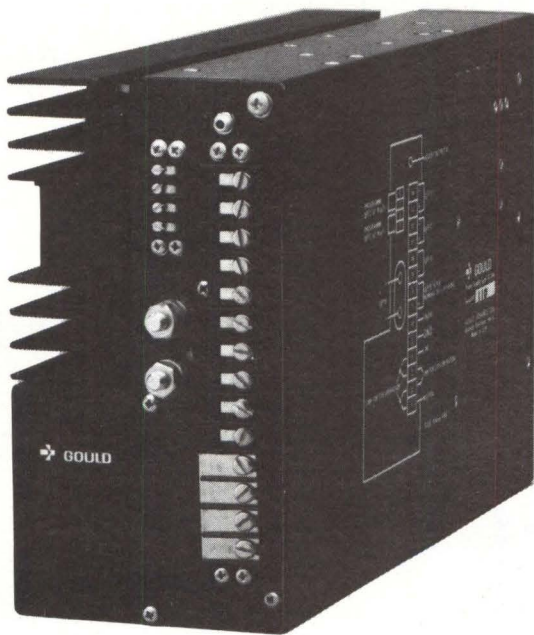
Portable, plug-in micro/minicomputer regulators exceed performance ratings of ultra-isolation transformers and add voltage regulation, overvoltage protection, and short-circuit current limiting. Units guard against most ac power problems except total blackout. Transverse-mode noise attenuation is 60 dB; common-mode noise attenuation is 120 dB. Expanded line features 2 60-Hz models with 140- and 250-VA load ratings. **Sola Electric Co.**, 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 217 on Inquiry Card



# The big switch

**...is to energy saving switchers.**



300 watt, quad output MGQ 300: 75% energy efficient.

Switching power supplies are more efficient than linears.

To produce a 200 watt output, a linear supply needs 400 watts coming in. A Gould switcher needs only 270. The switcher saves the 130 watts that the linear throws off in the form of heat.

Since the switcher dissipates less heat, your system operates at a lower temperature. This improves overall reliability and can reduce the need for external cooling.

But energy efficiency isn't the only advantage switchers offer. They're 1/3 the size and 1/4 the weight of linears. And they offer far better holdup and brownout protection.

Gould offers single and multiple output switchers with power levels from 8 to 2,250 watts. And custom designs can be provided to meet your exact specifications. You'll be backed by a high volume production capability and worldwide service network that only a \$1.5 billion company like Gould could offer.

For more information contact Gould Inc., Electronic Components Division, 4601 North Arden Dr., El Monte, CA 91731. Phone (213) 442-7755.

**Gould.**  
**The power in switching power supplies.**





## PRODUCTS

### FRONTEND PROCESSOR INTERFACE



LSI-X.25 microprocessor-based units interface computers and their peripherals to packet switching networks supporting CCITT approved X.25 protocol. Frontend processor implements packet switching support for DEC's PDP-11 systems. Microprocessor contains X.25 network software as well as interactive terminal interface for RSTS and RSX operating systems. Unit connects to communications network through synchronous channel at speeds up to 9600 bits/s. DMA performs transfer to PDP-11. **Cableshare Ltd**, 393 Rectory St, London, Ontario N5W 3W2, Canada. Circle 218 on Inquiry Card

### DATA LINK ANALYZER WITH CASSETTE UNIT OPTION



The 803A uFox™ is a diagnostic tool for data communications facilities. For online testing, it monitors the data stream in various codes, checking text, control, and protocol characters. Offline, it simulates a CPU, terminal, or modem to isolate problems. Microprocessor control and a conversational language make operation easy for non-programming personnel. An optional cassette unit supplements internal program memory and allows events of interest to be recorded. **Halcyon, Inc**, 1 Halcyon Plaza, 2121 Zanker Rd, San Jose, CA 95131. Circle 219 on Inquiry Card

# A new T-bar® miniature 6PDT Toggle Switch

Full Size.



**2 million cycles**  
for computers, minicomputer and main frame forming, data communications equipment, medical, industrial instrumentation, and stop-start test switching

T-BAR Series 202 6PDT Mini-Paddle Lever Switches are designed for "must operate" applications. T-BAR Edge-to-Dome™ bifurcated contacts provide the SitStill™ reliability that protects the integrity and stability of millions of circuits during continuous use or even long periods of inoperation. The 202 retains its initial characteristics through 2-million operations. Call for application help.

**T-bar** INCORPORATED

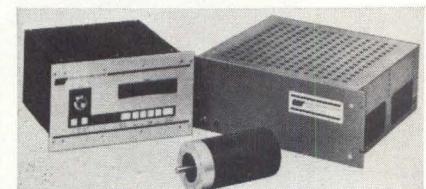
SWITCHING COMPONENTS DIVISION

141 Danbury Road Wilton, CT 06897 Telephone: 203/762-8351 TWX: 710/479-3215

### COMMUNICATIONS CONTROLLER WITH DOUBLE DISC UNIT

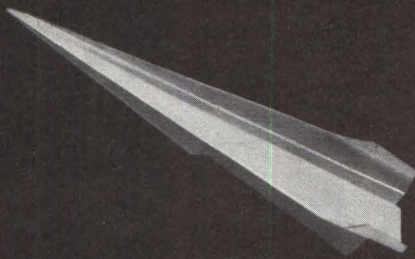
A disc unit added to the Smarts controller provides expanded storage and file capacity, and additional work space for editing large files. Operating as a single, integrated system, the disc can store over 540k char on 2 diskettes in up to 120 operator-named files. Disc space is dynamically allocated. Upon operator command, the controller's file directory lists all files on both diskettes. Operators can randomly access any message by file name. **Western Union Data Services**, 70 McKee Dr, Mahwah, NJ 07430. Circle 220 on Inquiry Card

### DIGITAL POSITIONING SYSTEMS



The DPS high speed, high accuracy shaft positioning system allows the user to select any of 1500 variations and options from a small number of stock modules. Fitting the needs of small and large quantity users, the plug-in systems are preadjusted, assembled, and tested. The company designs and manufactures all of the basic system—motor, position feedback transducer, and control electronics. Features include speeds of 5 to 5000 r/min and power up to 1.8 hp. **Electro-Craft Corp**, 1600 Second St S, Hopkins, MN 55343. Circle 221 on Inquiry Card





**TRANSMISSION:**  
Page; Field; Modified  
Field; Prompted  
Transmission; Device  
Status; Function Keys.

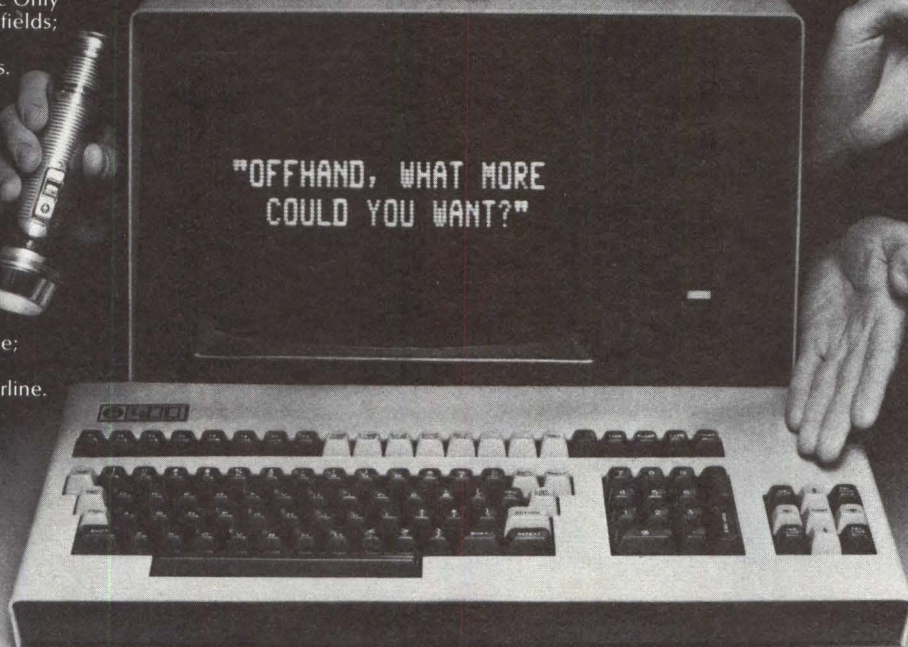
**INTERFACE:**  
EIA RS-232; Current  
Loop; 17 data rates  
(switch selectable)  
including 19, 200  
chars/sec; Half duplex  
support; Line  
turnaround characters;  
Reverse channel.

**EDITING  
FUNCTIONS:**  
Insert/Delete line and  
character; Columnar  
Tabbing; Cursor  
Addressability; Cursor  
Sense; Numeric Only  
fields; Security fields;  
Erase Variable/  
Protected fields.

**OPTIONS:**  
Buffered Printer  
Interface (RS-232 and  
parallel), separately  
addressable from the  
CPU; Standard Polling;  
Paging.

**VIDEO:**  
Normal; Reverse;  
Blink; Low/half  
intensity; Underline.

**KEYBOARD:**  
Removable, solid  
state with international  
character layouts.



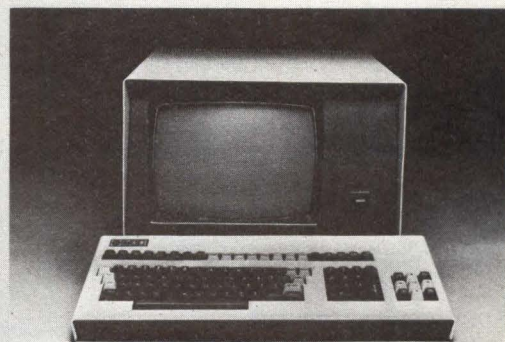
When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is its cost; at \$1,095 in quantities of 100 or more, it's the most versatile terminal for the price you can get your hands on.

More information on the I-400 is quickly within your grasp. Call Infoton toll-free at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth at Infoton, Second Avenue, Burlington, MA 01803.

Prepared by Chickering/Howell, Los Angeles.

**CIRCLE 103 ON INQUIRY CARD**



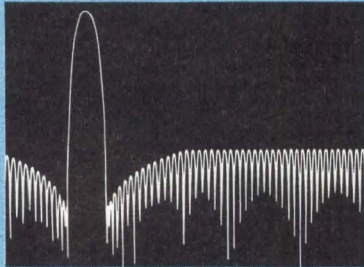
**Infoton 400**



# ADVANCED TECHNICAL

Course 412 — Four days

## Digital Signal Processing



**HOUSTON**  
July 18-21  
**NEW YORK**  
Aug. 1-4  
**CHICAGO**  
Aug. 15-18  
**SAN DIEGO**  
Sept. 26-29  
**WASHINGTON D.C.**  
Oct. 10-13

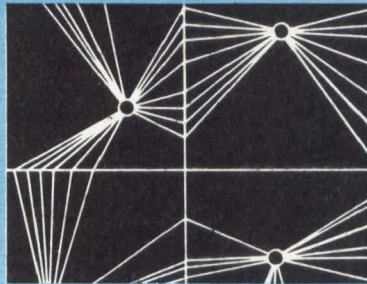
The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensible manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

- An Overview of Applications
- Digital vs. Analog Signals
- Operations on Digital Signals
- Recursive Filters
- Nonrecursive Filters
- Design Techniques
- Computer Aided Design
- Statistical Approaches
- Spectral Estimation
- Application Case Study

Course 350 — Four days

## Distributed Processing and Computer Networks

**HOUSTON**  
July 25-28  
**CHICAGO**  
Aug. 8-11  
**NEW YORK**  
Aug. 22-25  
**WASHINGTON D.C.**  
Sept. 26-29  
**SAN DIEGO**  
Oct. 17-20



This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of the concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

- What is to be Distributed?
- Data Communication Concepts
- The Computation Continuum
- Computer Networks
- Network Protocols
- Database Structures
- Database Requirements
- Security Considerations
- Evaluation and Selection
- Management and Control



## MICROPROCESSORS & MICROCOMPUTERS FIVE-DAY COURSE SERIES

Course 111: One day — Monday

**MICROPROCESSOR PROJECT MANAGEMENT**  
From design through manufacture, QA and field service

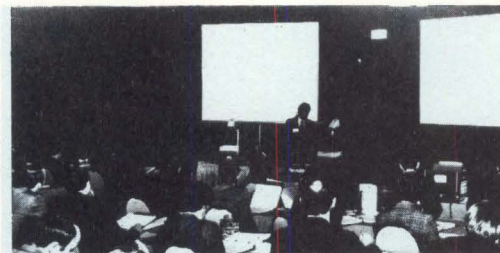
Course 102s: One day — Tuesday

**MICROPROCESSORS AND MICROCOMPUTERS:**  
A Comprehensive Technical Introduction and Survey

Course 130: Three days — Wed., Thurs., Fri.

**HANDS-ON MICROCOMPUTER PROGRAMMING  
AND INTERFACING WORKSHOP**

EACH student receives a complete 8080 micro-computer and interfacing system for his personal use throughout the course.



**SEATTLE**  
July 10-14

**DALLAS**  
July 24-28

**WASHINGTON D.C.**  
Aug. 14-18

**MINNEAPOLIS**  
Aug. 21-25

**LOS ANGELES**  
Sept. 18-22

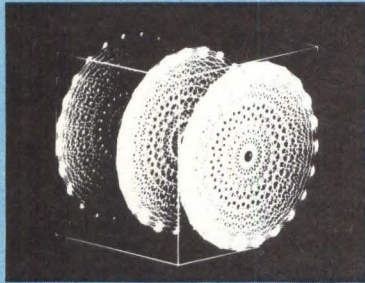
**NEW YORK**  
Sept. 25-29



Course 365 — Four days

## Computer Graphics

State of the Art Techniques and Applications



**BOSTON**  
July 18-21  
**SAN FRANCISCO**  
July 25-28  
**NEW YORK**  
Aug. 8-11  
**HOUSTON**  
Sept. 12-15  
**WASHINGTON D.C.**  
Oct. 10-13

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

- Display Hardware
- Color Display Techniques
- Two Dimensional Graphics
- Three Dimensional Graphics
- Transformations
- Software Structures
- The Hidden Line Problem
- The Hidden Surface Problem
- Software 'Build or Buy'
- Selection Methodology

Course 440 — Four days

## Fiber Optic Communication Systems

**WASHINGTON D.C.**

July 25-28

**CHICAGO**

Aug. 22-25

**HOUSTON**

Sept. 19-22

**SAN DIEGO**

Oct. 3-6



This course is designed for engineers, scientists and managers involved in the planning, design and implementation of all types of communication systems. The course covers the fundamental principles of fiber optic based systems, and the state of the art in system components including light sources, optical fibers, single and multifiber cabling, fiber coupling, photodetectors, receiver and repeater technology, and fiber optic networks. Commercially available components will be surveyed to illustrate design techniques for the cost effective, practical application of this important new technology.

- Advantages of Fiber Optics
- Optical Fiber Transmission
- Cabling Technology
- Light Sources
- Detection Technology
- Receiver/Transmitter Technology
- Modulation Techniques
- Digital Communications
- Data Bus Design
- System Design and Analysis

## FREE BROCHURES

For additional course details, information about group discounts and course series discounts for 111, 102s and 130, and information about special hardware options for course 130, please fill out and return this coupon or call the ICS ENROLLMENT SECRETARY, (213) 450-2060

### COURSE FEES:

Course 111 or 102s: \$195 (U.S.)  
Course 130: \$495 (U.S.)  
Course 350, 365, 412 or 440: \$595 (U.S.)

### Please Enroll Me in Course Number:

350    365    412    440  
 111    102s    130

City & Date \_\_\_\_\_



## TO ENROLL

Please fill out, detach and return this coupon. A Confirmation Letter with complete details will be forwarded to you. Mail to:

**Enrollment Secretary**  
**Integrated Computer Systems, Inc.**  
3304 Pico Blvd., P.O. Box 5339  
Santa Monica, CA 90405

For Immediate Confirmation, Call: **(213) 450-2060**

Name \_\_\_\_\_ Job Title \_\_\_\_\_

Company \_\_\_\_\_ Mail Stop \_\_\_\_\_

Address \_\_\_\_\_

City \_\_\_\_\_

State \_\_\_\_\_ Zip \_\_\_\_\_ Telephone \_\_\_\_\_

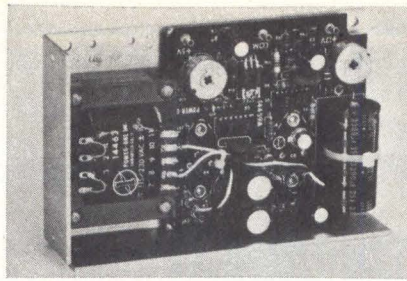
Please send additional information



## PRODUCTS

### FLOPPY DISC DRIVE POWER SUPPLIES

Model CP-249, originally designed for Shugart SA400 Minifloppy™ system, is dedicated to 5.25" (13.34-cm) format. Supply provides dual outputs of 5 V at 0.7 A, and 12 V at 1.1 A steady state with 1.7 A pk. Std features include 115/230-Vac ±10% input capabilities, ±0.05% line and load regulation, and full protection against short-circuit and

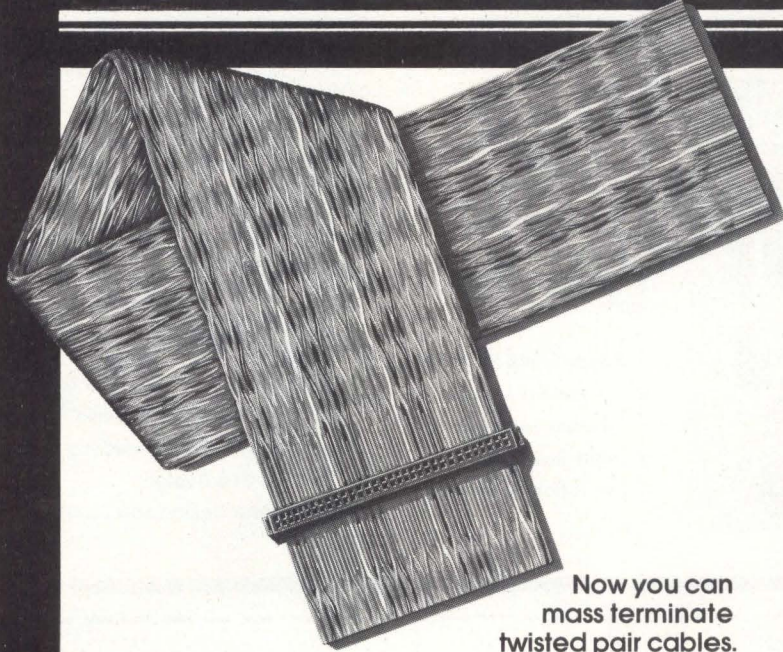


overload. Max ripple is 3.0 mV pk-pk while transient response is 30 μs for a 50% load change. **Power-One Inc.**, Power One Dr, Camarillo, CA 93010. Circle 222 on Inquiry Card

### 128k x 22 SEMICONDUCTOR MEMORY CARD

Oncard options offered by the MICRO-RAM 3500 single-card memory system include ECC (single-bit error correction and multiple-bit error detection) and word or byte parity generation and checking. Card also has page mode, byte mode, error stop, and a fault location LED display which operates in conjunction with the ECC option. Provisions have been made for battery backup. System can be plugged into Micromemory 3000 chassis or used independently. **EMM Commercial Memory Products, a div of Electronic Memories & Magnetics Corp.**, 12621 Chadron Ave, Hawthorne, CA 91250. Circle 223 on Inquiry Card

## CABLEGRAMS FROM SPECTRA-STRIP.™



Now you can  
mass terminate  
twisted pair cables.

Spectra-Strip's Twist 'N' Flat Cable is great when you need reduced crosstalk and fast, low-cost, mass termination. In applications like high speed computer and communication equipment using digital techniques.

Our standard Twist 'N' Flat comes with 26 solid or 28 stranded AWG wire. The twisted section is 18" and parallel section is 2" with conductors on .050" centers. Custom configurations are available that vary the wire gauge, pitch and length of the twisted and parallel sections. You also get the same crosstalk characteristics of our Twisted Pair Cable.

Twist 'N' Flat. Another unique idea patented by Spectra-Strip.

**SPECTRA-STRIP**™  
ALL WE DO IS KEEP EVERYTHING TOGETHER.

an Eltra company

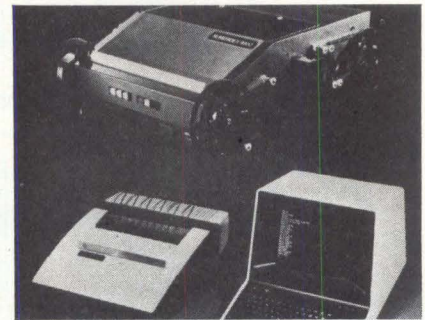
P.O. BOX 415  
GARDEN GROVE, CA 92642  
(714) 892-3361

### 1250-MHz FREQUENCY COUNTER

Designed for IEEE-488 bus applications, model 6043A is a thin line shape, measuring 1.75" (4.44 cm) in panel height. It automatically measures frequencies from 20 Hz to 1250 MHz, displaying them on an 8-digit LED readout. Interface to IEEE-488 bus is available at a rear panel connector. LED indicators on the front panel display programmable mode of the counter. Front panel pushbuttons offer selection of resolution from 0.1 to 1000 Hz in decade steps; X1, X10, and X100 input attenuation for inputs to 100 MHz; and reset and hold controls. **Systron-Donner Corp., Instrument Div.**, 10 Systron Dr, Concord, CA 94518.

Circle 224 on Inquiry Card

### NC MACHINE TOOL PROGRAMMING SYSTEM



Model 9800 combines buffer memory and video display, allowing all program preparation and editing to be done at the console without the need to manually write the program, generate a tape, or initiate a program printout. The program is held in memory and displayed on the monitor where it can be verified or changed; a char, word, or line can be typed on the keyboard and automatically inserted. Features include a 24-line capacity, impact printer, and programming terminal unit. **Numeridex, Inc.**, 241 Holbrook Dr, Wheeling, IL 60090.

Circle 225 on Inquiry Card



# C-1000



## THE FIRST TV CAMERA DESIGNED FOR COMPUTER INTERFACE

### **SUPERB RESOLUTION—**

Observe minute detail with resolution over 1000 TV lines.

### **VIRTUALLY DISTORTION-FREE—**

Image is accurate, linear from center of screen to outer edge with less than 0.2% distortion.

### **STABLE—**

Less than 0.05% drift per 24 hours, less than 0.2% from 10° C to 40° C.

### **PLUS ALL LINES NEEDED FOR DIGITAL AND ANALOG COMPUTER INTERFACE**

**THIS UNIT IS "INSTRUMENT QUALITY"  
—NOT A VIDEO SYSTEM FOR  
ENTERTAINMENT VIEWING**

### **APPLICATIONS:**

#### **MEDICAL**

Tissue analysis  
Blood analysis  
Neurological—X-Y movement analysis  
Optical Instrument data analysis  
Other analysis of visual data

#### **INDUSTRIAL**

Aerial photography analysis—crop areas,  
insect infestation  
IR Analysis—detect forest fires, direct robot  
fire fighters  
Bottle inspection—using polarized light  
Dimension analysis and control, area  
measurement, displacement measurement  
Printed pattern analysis and control  
Missile tracking

#### **UNIVERSITY**

Analysis of any visual information that can be  
measured through variation in light intensity  
Medical research  
Physics research  
Laser technology

# HAMAMATSU

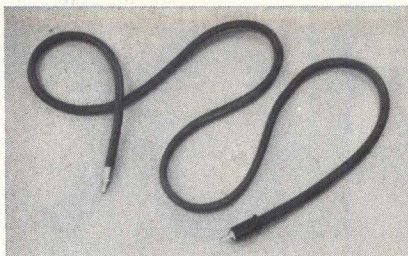
HAMAMATSU CORP. • 120 WOOD AVENUE • MIDDLESEX, NEW JERSEY 08846 • (201) 469-6640



## PRODUCTS

### FIBER-OPTIC FLEXIBLE LIGHT GUIDES

Designed for data processing, scanning, programming, mark sensing, and medical instrumentation and recording, PVC-sheathed light guides operate in temps from -40 to 220 °F. Easily installed guides use 0.002" (0.0051-cm) glass fibers and transmit a beam of intense bright cold light. Std designs include single, bifurcated, and trifur-



cated branch tips to match link-up needs, with 600- to 700-dB/km attenuation, and 68° acceptance angles. **Valtec Corp, Fiberoptics Div**, West Boylston, MA 01583.

Circle 226 on Inquiry Card

### DIAGNOSTIC CONTROLLED MODEM

The 2400-bit/s synchronous modem's diagnostic features, contained in the master and remote site modems, function as the controller for the entire communications network. They provide a secondary channel with command mode procedures. Test and control of remote site modems are performed over this secondary channel. Test pattern generator and detector, EIA std RS-232 interface, and online compatibility with Bell System 201B and 201C data sets are std. **Penril Corp**, 5520 Randolph Rd, Rockville, MD 20852.

Circle 227 on Inquiry Card

## The world's cheapest 8-Bit, 16-MHz VIDEO A/D

- It's complete...
- It's self-contained...
- It's proven...
- 1000's are in operation

and now  
it's only  
**\$479!\***

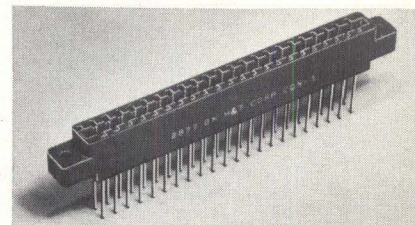


## COMPUTER LABS

COMPUTER LABS, INCORPORATED  
505 EDWARDIA DR. ● GREENSBORO, N. C. 27409  
919/292-6427 ● TWX 510-922-7954

\*In quantity of 100.

### EDGE CONNECTORS



A 22/22-contact connector for single- or double-sided PC boards, model CON-1 features 0.025" (0.63-mm) square 3-level wirewrapping contacts on 0.156" (4.0-mm) centers. Contacts are nickel-silver over beryllium-copper, and feature reliable bifurcated/bellows design. Connector body is molded of UL and MIL approved VALOX™, an insulating material of superior dielectric, thermal, and chemical characteristics. **OK Machine and Tool Corp**, 3455 Conner St, Bronx, NY 10475.

Circle 228 on Inquiry Card

### PORTABLE DUAL-TRACE 15-MHz OSCILLOSCOPE



Bandwidth of model 1432 triggered sweep scope covering 0.5  $\mu$ s to 1.5 s is rated at 15 MHz with a vertical sensitivity rating of 2 mV/div; usable response extends beyond 30 MHz. Optional battery pack mounts and is recharged inside the case. A built-in universal power supply provides operation on 117 Vac, 234 Vac, or 12 Vdc. Display modes are chopped or alternate. Algebraic addition and subtraction of channel B and A input signals as well as automatic stability control, are included. **B&K-Precision, Dynascan Corp**, 6460 W Cortland Ave, Chicago, IL 60635.

Circle 229 on Inquiry Card



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PRINTRONIX...**

**THE FIRST**

**600 LPM**

**RASTER MATRIX  
IMPACT LINE  
PRINTER/PLOTTERS!**

The same unique concept that offers you higher standards of performance in 150 and 300 lpm multi-copy line printing has been applied to produce the Printronix 600, the industry's first 600 lpm raster matrix impact line printer!

The elegantly simple print mechanism assures you of three cost/performance advantages no other impact, chain, drum or belt printer can equal. Unsurpassed print quality. Incomparable reliability, proven by more than 5000 units in the field. And, the capability to plot graphs, charts, bar codes, large character labels or what have you. Alphanumeric printing plus plotting capability for the same price, or less, than an alphanumeric printer alone.

Now Printronix spans the complete medium speed range with 150, 300 and 600 lpm models. At any speed . . . they're your best buy! Get all of the facts. Contact: Printronix, Inc., 17421 Derian, Irvine, CA 92714. (714) 549-8272

**PRINTRONIX**

**The leader in  
raster matrix technology**

**CIRCLE 108 ON INQUIRY CARD**





## PRODUCTS

### INTELLIGENT TERMINAL SYSTEM



OP-1/R is user-programmable and will run std OP-1 programs (including those written in high level languages), utilities, and communications packages. Terminal is configured to be used in clustered or online systems. Features include multiple microprocessors sharing 4k, 8k, 16k, or 32k RAM, plus up to 8k of ROM or p/ROM. Set of 128 char, 7 x 9 dot matrix, and line drawing capabilities are characteristic of its display. Communications capabilities are asynchronous from 110 to 19.2k baud. **Ontel Corp**, 250 Crossways Park Dr, Woodbury, NY 11797. Circle 230 on Inquiry Card

### LETTER QUALITY IMPACT PRINTER

For use with PTS-100™ programmable terminal systems, 45-char/s model 3408 printer is microprocessor-controlled and provides typewriter-like output quality. Featuring a servo-controlled daisy wheel with Courier or pica font, the unit produces sharp fully formed char on from 1- to 6-part forms. Features include switch-selectable form feed in increments from 1 line to 14" (35.6 cm), full ASCII char set, and a 132-char/line x 6-line/in (2/cm) format. **Raytheon Data Systems Co, Communications Dept**, 1415 Boston-Providence Tpk, Norwood, MA 02062. Circle 231 on Inquiry Card

### DUAL KEYBOARD TERMINAL SYSTEM

TC 800 terminal system combines reliability of individual intelligent terminals with economy of a controller-based system. Online terminal system can be configured as a 2-workstation standalone unit or satellite system in a clustered master/satellite terminal environment. 3 self-contained and free-moving video display units are available, with screen capacities of 260, 480, and 1920 char. Each terminal has 16 I/O channels. **Olivetti Corp of America**, 500 Park Ave, New York, NY 10022. Circle 232 on Inquiry Card

### DATA ACQUISITION MODULE

ADAM 100, a 12-bit A-D with 100-kHz throughput and full scale accuracy of  $\pm 0.025\%$ , is contained in a 3 x 4.6 x 0.375" (7.6 x 11.7 x 0.953-cm) metal can that provides 6-sided electrostatic and electromagnetic shielding. Unit contains a high speed sample and hold, and 16 channels of single-ended pseudodifferential or 8 fully differential multiplexer inputs, all jumper selectable at pinouts. Module also includes 3-state outputs for data transfer to bus oriented systems. **Adac Corp**, 15 Cummings Pk, Woburn, MA 01801. Circle 233 on Inquiry Card

### LOG/ANTILOG AMPLIFIERS

Featuring 200-kHz bandwidth at signal current of 1  $\mu$ A, log/antilog amps provide 1% conformance accuracy to ideal log operation over 4 decades of current logging (20 nA to 200  $\mu$ A). 2% accuracy is also guaranteed over 5 decades of operation, 10 nA to 1 mA. Models 759N/P are housed in 1.125 x 1.125 x 0.4" (2.858 x 2.858 x 1.02-cm) package that features a complete dc logarithmic amp. No external components are required to select scale factor or reference current; they may be externally adjusted by the user. **Analog Devices, Inc**, PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062. Circle 234 on Inquiry Card

# Two lightweight contenders for your triple power needs



In this corner, the AED101, a highly efficient power supply designed specifically to provide the DC power range required by floppy disk subsystems operating one to four drives. Extremely lightweight and compact, the 101 provides triple-output power (+5V @ 12 amps; -12V @ .7 amps; +24V @ 3.5 amps) for up to 4 drives plus drive electronics, formatter and interface circuitry.

It also offers OVP, foldback current limiting, 5V switching regulator, and is UL recognized.

In the other corner, the AED201, 4 1/2 lbs. lighter and designed to meet the special DC power requirements for one to two floppy disk drives (+5V @ 5 amps; -5V @ .7 amps; +24V @ 2.8 amps). The 201 provides foldback limiting on +5V, superior power efficiency, and is designed to meet UL478 Standards. Both models are field proven, and they are available right now. \*Prices shown are for 100-249 per year.

**IDEAL POWER FOR SHUGART  
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OTHER FLOPPY DRIVES**

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DESIGN, INC.**

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Sunnyvale, California 94086. Phone 408-733-3555



Thanks to the N123's interactive programming, non-technical people can do what programmers do. And non-technical people are a lot easier to find these days.

The fact is, the N123 programs itself automatically from any verified backplane. Your "programmer" merely sets up the pin-naming scheme, enabling the system to print error messages in your own language.

And all this involves is using a keyboard to answer a series of questions asked by the system through its CRT display.

### **SMALL SYSTEM, BIG ADVANTAGE.**

Although designed for smaller backplanes (8000 points or less), the N123 has many advantages in common with our larger, computer-controlled N151.

Easily understood error messages are one advantage. Daisy-chained fixture cards are a second. A ten-year warranty is a third.

Best of all, users of the N123 report exceptionally fast payback.

For an information package that includes both details of the system and a payback analysis, write Teradyne, 183 Essex Street, Boston, Massachusetts 02111.

# **SO SIMPLE TO PROGRAM YOU DON'T NEED PROGRAMMERS.**



The N123 backplane test system.

# **TERADYNE**

CIRCLE 110 ON INQUIRY CARD



## PRODUCTS

### 600-LINE/MIN RASTER MATRIX IMPACT PRINTER



Printer offers advantages of raster matrix impact printing, and enables full spectrum of medium speed printer requirements to be met at low cost. Advantages include multicopy print quality; high reliability, made possible by simple printing mechanism with up to 50% fewer parts than drum, chain, belt, or band printers; full 96-char ASCII set expandable to 160 chars without speed degradation; and an inherent computer graphics/plotting capability. **Printronic Inc.**, 17421 Derian Ave, Irvine, CA 92714. Circle 235 on Inquiry Card

### PRECISION FIBER-OPTIC CABLES

In lengths to 1 km, optical cables are available in 1-, 2-, 4-, 6-, 8-, and 10-fiber versions. Designed-in strength features help alleviate problems of fiber elongation, microbends, and changes in attenuation. Testing method gives users precise information about optical cables, particularly rating their stress limits. Cables are appropriate for duct and interior installations. Attenuation levels are 6 dB in premium and 10 dB in std grade. **Siecor Optical Cables, Inc.**, 631 Miracle Mile, Horseheads, NY 14845.

Circle 236 on Inquiry Card

### PROGRAMMABLE ASYNCHRONOUS ADAPTER

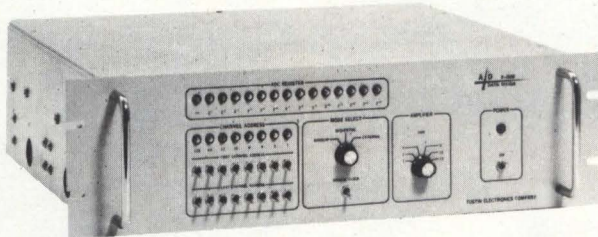
Dual line adapter, geared for Interdata minicomputer users, provides 2 PASLA compatible RS-232-C channels on a half board, maintaining software and hardware compatibility with host products. Flexibility is increased through use of independent 10-bit addresses, data set status disable, duplex mode, and a 50 to 19.2k baud rate. Low power Schottky construction reduces power consumption of 2 channels from 3.2 to 0.75 A at 5 V. Adapter is used for data set and local terminal communication. **RDV Engineering**, 319 Dolores Cir, Placentia, CA 92670. Circle 237 on Inquiry Card

### CORE MEMORY REPLACEMENT FOR FIXED DISC SYSTEM

Buscomm DS-11 replaces DEC's RF-11/RS-11 fixed disc system. Having no rotational latency, memory system contains a memory controller and modules, display card, power supply, and chassis. Chassis holds 8 memory modules providing max storage capacity of 1M words or 2M bytes. Unit is software transparent to all operating systems and diagnostics that support RF-11/RS-11 disc systems, and features on/offline switch, built-in self-test, selectable transfer rates to 1M words/s, and selectable block transfer mode. **Standard Memories/Trendata**, 3400 W Segerstrom Ave, Santa Ana, CA 92704. Circle 238 on Inquiry Card

### 8-BIT VIDEO A-D CONVERTER

VADC-820 samples at a 20-MHz rate and is compatible with NTSC and PAL stds. Module is designed for digitizing TV and radar signals for storage, measurement, and transmission. Flexibility is provided by 4 pin-programmable input voltage ranges whose end points can be screwdriver adjusted up to  $\pm 10\%$  by internal gain trim. Binary coded ranges are 0 to 1 V and 0 to 2 V; offset binary ranges are  $\pm 0.5$  and  $\pm 1.0$  V. **ILC Data Device Corp.**, Airport International Plaza, Bohemia, NY 11716. Circle 239 on Inquiry Card



Tustin manufactures a wide variety of off-the-shelf Data Acquisition Systems utilizing a building block approach. Possibly one of our standard systems will fulfill your requirements. If not, because of the flexibility of our systems, we should be able to provide you with a non-standard unit with minimal engineering costs. We have provided systems with a combination of the following features:

- $\pm 10.0$  MV to  $\pm 10.0$  Volts Full Scale
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- $\pm 0.01\%$  Full Scale Accuracy
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- Instrumentation Amplifier per Channel — 100 KHz Bandwidth @ 140 DB CMRR
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- Digital-to-Analog Converters
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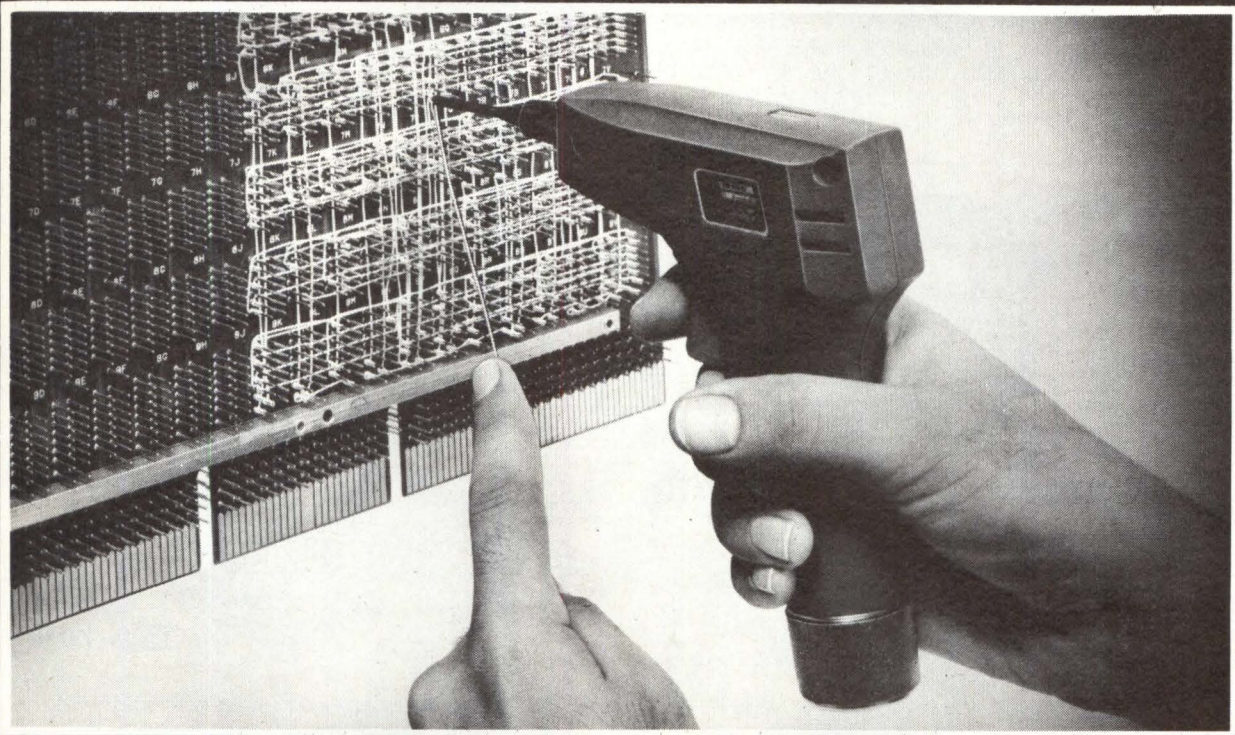
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## "INDUSTRIAL" WIRE-WRAPPING TOOL

MODEL BW928

**\$49<sup>95</sup>**

BATTERIES NOT INCLUDED  
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Model BW928-BF \$52.95
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- LEIGHT WEIGHT  
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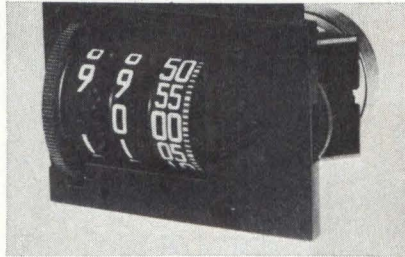


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## PRODUCTS

### PRECISION TIMER FOR AUTOMATIC CONTROL



Used where automatic and precise time control is required, series 7667 is highly readable and accurate, and replaces analog/dial timers that cannot control long time intervals. Setting of timer is bidirectional, with an accuracy of  $-2$  to  $4$  s from any setting. Timer displays and controls up to 99 min and 55 s. Left wheels display minutes, while right wheel displays seconds by increments of 5 with 1-s graduations between figures. Timer counts down to 0:00 as soon as interval is set and 115-Vac, 60-Hz power is applied. **Veeder-Root**, 70 Sargeant St, Hartford, CT 06102.

Circle 240 on Inquiry Card

### MILITARY COMPLIANT SWITCHING POWER SUPPLY

800 series power supplies, available for 1- and 3-phase operation, function without degrading environmentally from  $-55$  to  $71$  °C. Using JAN TX material, MTBF ratings surpass MIL-E-5400 and MIL-T-21200 requirements. Available for cold plate, forced air, or convection cooling, supplies eliminate risk factor associated with custom designs. Also available for commercial applications, units operate at 5 V, 60 or 120 A, and 28 V, 25 A. **Trio Laboratories, Inc**, 80 Dupont St, Plainview, NY 11803. Circle 241 on Inquiry Card

### SWITCHING POWER SUPPLIES

Featuring ac and dc inputs, brownout protection, tight regulation, and a MTBF of 100k hours, 20 SA series models operate over an input range of 115 Vac 10%,  $-20\%$  or 92 V to 127 Vac, or from a 120- to 165-Vdc input. Input frequency can be 47 to 440 Hz. Line regulation is  $<0.1\%$  for input range, 0.3% for 25-W model; load regulation is  $<0.1\%$  for no load to full load, 0.2% for 25-W model. Noise and ripple are 50 mV pk-pk for 5-V unit, and 100 mV pk-pk for 9- to 24-V units. **KEC Electronics Inc**, 21535 Hawthorne Blvd, Torrance, CA 90503. Circle 242 on Inquiry Card

### CIRCUIT VERIFIERS

High speed electrical inspection tools for bare boards, backplanes, flex circuits, and harness or cable assemblies, series 50 verifiers can check 4095 test points for opens and shorts in 1.6 s. Test time is  $400 \mu\text{s}$ /point regardless of network pattern or number of points. System allows rapid go/no-go inspection. With optional cassette recorder and printer, it can provide permanent program storage and complete error record. Programming is done from known-good board in 2 min typ at max capacity. **Everett/Charles, Inc**, 2806 Metropolitan Pl, Pomona, CA 91767. Circle 243 on Inquiry Card

### LINE PRINTER MICROPROCESSOR CONTROLLER

Primary function of the Motorola 68B00L-based MAGNUM-300 controller for the Printronix model 300 line printer is to allow a host computer or terminal to create varying size block letters from 0.1 to  $>12$ " (0.25 to 30.5 cm) in height. Transparent mode permits operation as a std line printer or block char printer. Added features include intermixed char sizes, over printing, horizontal and vertical tabbing, and automatic paper slewing. **Quality Micro Systems, Inc**, PO Box 1644, Mobile, AL 36601. Circle 244 on Inquiry Card



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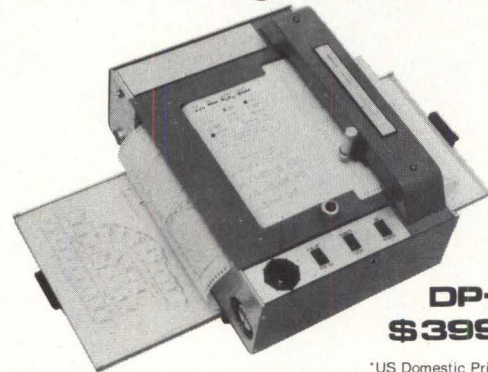
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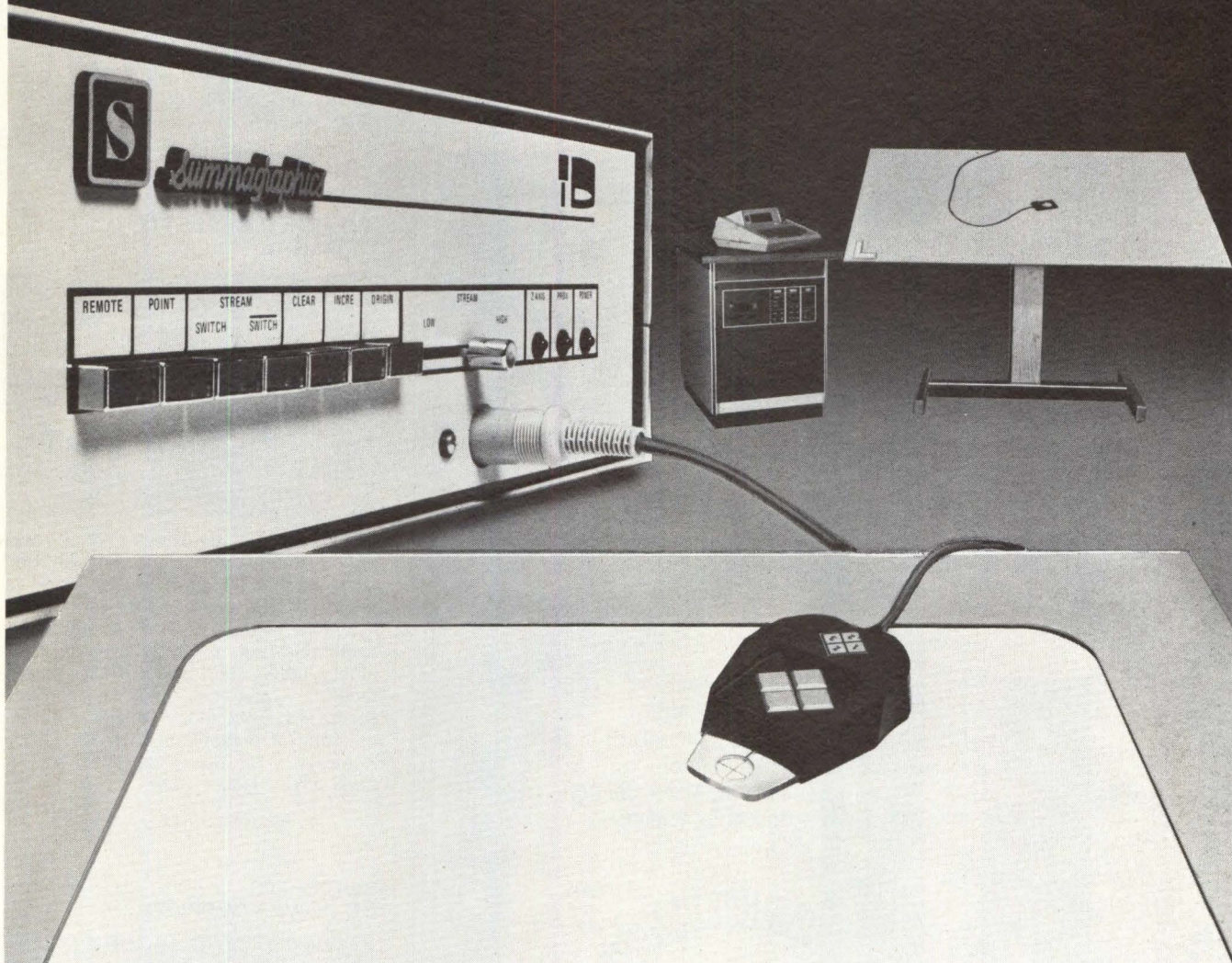
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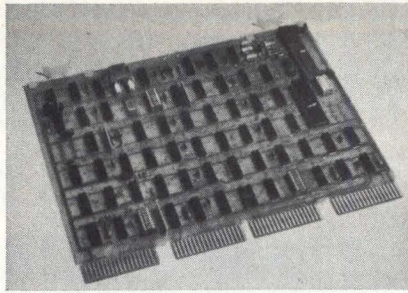
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## PRODUCTS

### ASYNCHRONOUS SERIAL CHANNEL INTERFACE

A DL-11 A, B, C, D, E compatible interface for PDP-11, CDL-11 is a universal link between Unibus and any asynchronous serial interface. Only 1 jumper is used for selecting required DL-11 compatible version. Register addresses, vectored interrupts, and 16 available baud rates are selected via DIP switches. The link is fully compatible



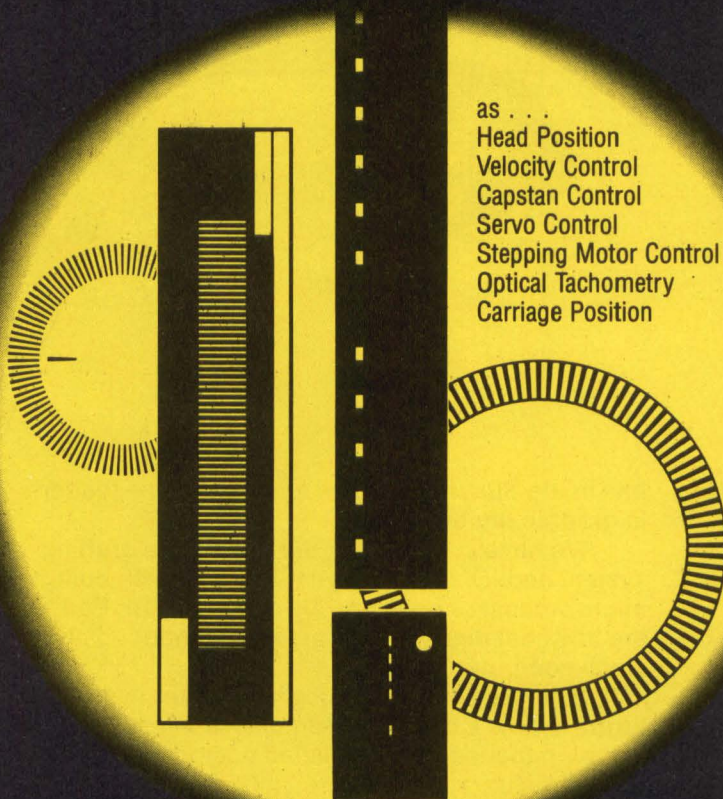
with DEC software. **Computer Interface Technology**, 2080 S Grand Ave, Santa Ana, CA 92705.  
Circle 245 on Inquiry Card

### MICROPROCESSOR-CONTROLLED DIGITIZER SYSTEMS

Second generation DATATAB II digitizing systems contain user-oriented functions that are controlled from the 16-button cursor. Dual function keys permit presetting, scaling, rotation, orientation, and area and line length calculations; 9 buttons initiate data recording and have operator assignable flags up to 20 char each. Other functions include point or rate recording, event count, and output device control. A 20-char alphanumeric display provides X,Y coordinate location and prompting. **Altek Corp**, 2150 Industrial Pkwy, Silver Spring, MD 20904.  
Circle 246 on Inquiry Card

## POSITION SCALES CODE DISCS APERTURE PLATES in glass, plastics & metals

for use in DISK DRIVES, TAPE TRANSPORTS, PRINTERS,  
PLOTTERS, CARD READERS, TAPE READERS  
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Ask about our New .006" thick METRIFILM GLASS DISCS . . . combine the low cost and weight of plastic, film or thin metals with the high performance of glass.

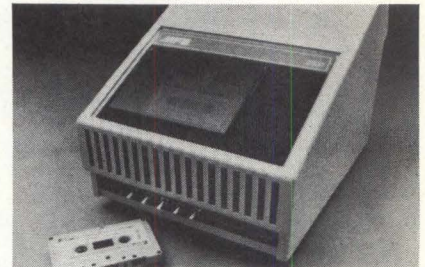


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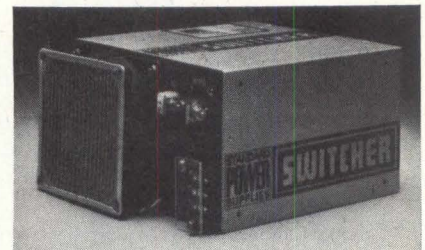
control thru measurement

### BUFFERED CASSETTE TERMINAL



Model 2500 incorporates 450B tape drive, which allows recording on both sides of tape, to provide 350k-char capacity. ANSI compatible, terminal is available with TI or NCR compatibility, selectable rates up to 2400 baud, and a binary mode. TTY and RS-232-C interfaces are also std. This microprocessor-based system increases storage capacity of present models. **MFE Corp**, Keewaydin Dr, Salem, NH 03079.  
Circle 247 on Inquiry Card

### SWITCHING DC POWER SUPPLIES



Rated at 750 W, SWS 750 units provide 5, 12, 15, 24, or 28 Vdc, from 28 to 150 A. Design features include over temp protection, low input shutdown protection, and full load burn-in. Units have 80% efficiency rating, low emi-rfi (suppressed at source with line filters), paralleling capability, and brownout capability (to -15% of input line). Full load operation is maintained for 30 ms after loss of input line. All models meet UL 478. **Standard Power, Inc**, 1400 S Village Way, Santa Ana, CA 92705.  
Circle 248 on Inquiry Card

← CIRCLE 116 ON INQUIRY CARD



## CRT TEST SET POWER SUPPLY



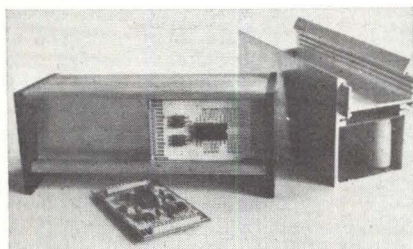
Including 3 regulated power supplies assembled in 1 unit, model CRT-30 supplies high voltages for CRT test set. Anode output adjustment from 0 to 30 kV at 2 mA, focus output from 0 to 8 kV at 1 mA, and grid output of 0 to 1 kV at 1 mA are provided by 3 10-turn dials. Ripple and regulation specs of 0.01% max allow precision testing of CRTs. High speed dynamic focus control and remote digital or analog programming and monitoring are added features. **Bertan Associates, Inc.**, 3 Aerial Way, Syosset, NY 11791. Circle 249 on Inquiry Card

## TELEPRINTER TERMINALS

Models 1001, 1002, 1003, and 1005 make up family of 30- and 120-char/s teleprinters for use with series 60 computers. Terminals are available as send/receive devices or receive-only printers, and incorporate dot matrix impact printing and microprocessor-based electronics. 1001 and 1002 models are basic asynchronous terminals operating in full-duplex mode at 300 and 1200 bits/s, respectively. 1003 operates at selectable rates of 110, 200, or 300 bits/s; while 1005 communicates at 1200 bits/s. **Honeywell Information Systems**, 200 Smith St, Waltham, MA 02154. Circle 250 on Inquiry Card

## MODULE HOLDER AND CASE

Module PC or user created breadboards can be located in several positions in the holder and case of ruggedly constructed aluminum extrusion with a 0.06" (0.16-cm) wall. Logic modules can be interchanged in the low profile holder, which contains slots to mount on equipment walls for test or prototype use without repackaging. Combined with case and end plates, it can be used to package test circuits, demo units, or small quantity production. **Ecsand Labs**, 39165 Johnnycake Ridge, Willoughby, OH 44094.



Circle 251 on Inquiry Card

## PROCESS CONTROL INTERFACE MODULES

PCM1 can be connected to most dc motor speed controls, allowing motor speed to be increased or decreased with an increase in signal current. Connection allows speed control to retain its normal operating characteristics. Module accepts std inputs of 1 to 4 mA, 5 to 10 mA, and 10 to 50 mA by selection of proper shunting resistors. Master power supply, which enables multiple control of 2 to 10 modules, is adjustable between approx 1 to 4 mA. **Minarik Electric Co.**, 232 E Fourth St, Los Angeles, CA 90013. Circle 252 on Inquiry Card

## SLANTED CHARACTER DIGITAL DISPLAY

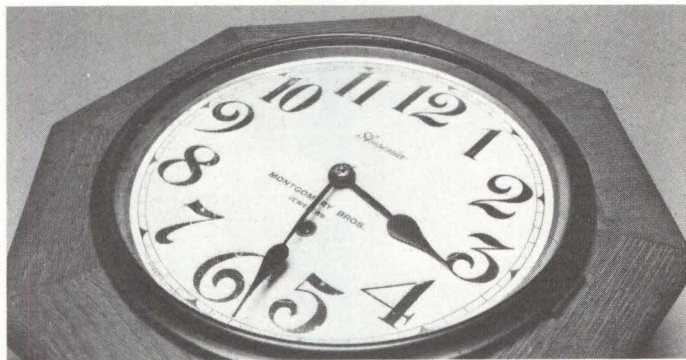
Incandescent digital displays with 0.625" (1.588-cm) slanted char and 120° viewing angle provide 9000-ftL brightness for readability in direct sunlight. Model GL 1050S is available with built-in, directly viewed decimal point. Displays can be filtered to any color, and may be dimmed for night viewing. Ceramic case, DIP terminals, and low profile design allow space saving in panel installations. Displays are TTL-compatible. **Refac Electronics Corp.**, PO Box 809, Winsted, CT 06098. Circle 253 on Inquiry Card

## 1.5- $\mu$ s ACCESS TIME STORAGE SYSTEM

Solid-state MaxiRAM system provides access time of 1.5  $\mu$ s with a transfer rate of 625k words/s, assures 0 latency, and offers total transparency to the host computer with a built-in controller. Modular capacity ranges from 0.524M to 8.388M bytes. Each 19" (48-cm) chassis accepts up to 8 pluggable modules of 524k bytes each; a second chassis may be interconnected, providing up to 8.388M bytes through 1 controller. **Imperial Technology, Inc.**, 821 S Douglas St, Suite 102, El Segundo, CA 90245. Circle 254 on Inquiry Card

## OPTICAL ABSOLUTE SHAFT ENCODER

Available in negative or positive logic, GC 30 series encoders have output format of continuous parallel gray code. "Whole word" output assures an exact reading when absolute position must be known after power has been interrupted and then reinstated. All electronics are integral and output is directly compatible with most ICs. Resolutions of up to 10 bits (2°) are available with accuracy of  $\pm 3.0'$  of arc. Std input power is 5 Vdc  $\pm 5\%$  at 300 mA max. **Disc Instruments, Inc.**, 102 E Baker St, Costa Mesa, CA 92626. Circle 255 on Inquiry Card



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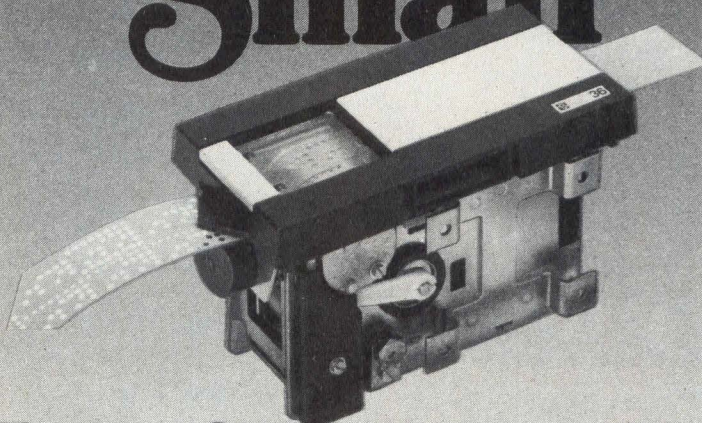
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CIRCLE 119 ON INQUIRY CARD

## PRODUCTS

### SWITCHING POWER SUPPLIES

S-line supplies deliver 30 W of dc power at 50 °C with available voltages of 5, 9, 12, 15, and 24 Vdc, all adjustable at 10 and -30%. Unit measures 5.125 x 1.125 x 5.75" (13.018 x 2.858 x 14.61 cm) and weighs 1.4 lbs (0.63 kg). It features remote error sensing, adjustable overcurrent, remote on/off control, built-in overvoltage protection, and a surge limiting input circuit. Built-in emi filtering and fully enclosed 1-piece aluminum case minimize radiated interference. **Kepeco, Inc.**, 131-38 Sanford Ave, Flushing, NY 11352.  
Circle 256 on Inquiry Card

### 16k-CHARACTER DATA BUFFER

With std features including search and edit routines, auto answer, transparency mode, and self-contained diagnostics, microprocessor-controlled solid-state data buffer stores up to 16k char. Unit interconnects between asynchronous RS-232 or TTY compatible terminals and a modem/CPU for store and forward applications. Dual UARTs provide for online baud rate conversion with speeds selectable from 110 to 19.2k baud. **Columbia Data Products, Inc.**, 6655 Amberton Dr, Baltimore, MD 21227.

Circle 257 on Inquiry Card

### INTELLIGENT PRINTING SYSTEM



IPS-7300 handles data logging, factory data collection, and label printing. Consisting of 120-char/s keyboard send-receive printer with moveable keyboard/display station, and 8-bit programmable microcomputer, system operates in a standalone environment, or in a local or remote mode within an online system. Data input station consists of a gas discharge display and 64-char, ASCII compatible keyboard. Basic configuration includes microcomputer with 8 I/O registers and 10k bytes of semiconductor memory; 32-char display and keyboard, and RS-232-C asynchronous communications interface. **Dataroyal, Inc.**, 235 Main Dunstable Rd, Nashua, NH 03060.

Circle 258 on Inquiry Card



### LIMITED DISTANCE MODEM

Model 7300 provides data communications over unloaded private cable systems or telephone company supplied local exchange loops. Analog and digital loopback, command loopback, and test pattern generator diagnostic capabilities support system and self tests. Full- or half-duplex operation over 4-wire lines or simplex operation over 2-wire lines occurs at 8 data rates from 19.2k to 1800 bits/s. The modem meets power vs frequency specs of Bell Systems PUB 43401. **Tele-Dynamics Div of Ambac Industries, Inc.**, Fort Washington, PA 19034.

Circle 259 on Inquiry Card

### DIGITAL TIME DELAY RELAY WITH THUMBWHEEL SWITCHES

A compact, low power, solid-state relay set by direct reading thumbwheel switches, series 280 Digilay operates from an input voltage of 12 Vdc  $\pm 10\%$ , and is capable of timing from 1 ms to 9999 s in on or off delay modes. Accuracy and repeatability is  $\pm 0.5\%$ . Max power turn-on time is 30 ms and min power recycle time is 10 ms. Spdt relay and spdt reed relay switch options provide switching times ranging from 1 ms to 10  $\mu$ s. **International Microtronics Corp.**, 4016 E Tennessee St, Tucson, AZ 85714.

Circle 260 on Inquiry Card

### WIREWRAP BOARDS FOR SERIES/1

Up to 72 20-pin or 64 16-pin IC positions are available on MB1-49-WW72 and WW64 wirewrap boards. Series/1 boards accommodate any 0.300, 0.400, or 0.600" (0.76, 1.02, or 1.52-cm) center DIPs. 2 40-pin ribbon-cable edge connectors are provided. This board occupies a single chassis slot in IBM computer. All general-purpose interface boards are doubled-sided with plated through holes and are constructed of UL-approved FR-4 material. Power and ground are wired to each std socket position. **MDB Systems Inc.**, 1995 N Batavia St, Orange, CA 92665.

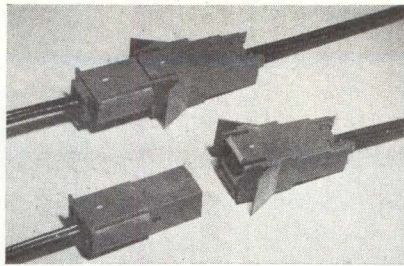
Circle 261 on Inquiry Card

### CABLE SOCKETS

Flat ribbon cable or twisted pair cable assembled to DIP IC sockets are used for display mounting, IC extenders, test probes, or board-to-board cable sockets. Std sizes are 8 through 40 contacts/conductor in single or double-end styles, or with a male plug on one end. Cable may exit from top or side of most socket sizes. Contacts are beryllium-copper, gold-plated. Connections are soldered and epoxy encapsulated; assemblies are tested for continuity and shorts. **Samtec, Inc.**, 810 Progress Blvd, New Albany, IN 47150.

Circle 262 on Inquiry Card

### SELF-ALIGNING FIBER-OPTIC CONNECTOR



Accommodating duplex fiber-optic cables with 0.013 to 0.017" (0.33 to 0.43 mm) dia fibers, overlapping style connector aligns mating fibers along their center axis. Elastomeric support members surrounding both fiber pairs conform under pressure to the exact fiber diameters, centering each on the axis of its mating fiber. Fiber-bearing inserts are hermaphroditic. When mating matched diameters, insertion losses are  $< 1$  dB; with 0.004" (0.1-mm) dia mismatch, max insertion loss is  $< 3$  dB. **AMP Inc.**, Harrisburg, PA 17105.

Circle 263 on Inquiry Card

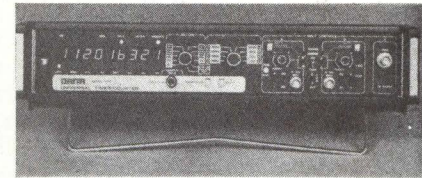
### DISC CONTROLLER FOR NOVA/ECLIPSE MINICOMPUTERS

Single-board, CPU resident disc controller allows minicomputers to access up to 1.2G bytes of online storage.

MSC-1300, a bipolar microprocessor-based controller, implements burst error detection and correction, IBM-like I/O channel communication techniques, data transfer rate throttling, overlap seek, and built-in microdiagnostics which automatically isolate faults within disc subsystem. **Microcomputer Systems Corp.**, 440 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 264 on Inquiry Card

### UNIVERSAL TIMER/COUNTER



9500 series 100-MHz universal timer/counters with frequency period, period average, time interval and average, totalize, and ratio measurement feature patented auto trigger, which aids in measuring signal parameters. Synchronous window permits operator to isolate a pulse or section of time. Selective gate control allows user to measure period of single or train of pulses or events. Model 9514 is microprocessor controlled unit; 9510 is without control. **Racal-Dana Instruments Inc.**, 18912 Von Karman Ave, Irvine, CA 92715.

Circle 265 on Inquiry Card



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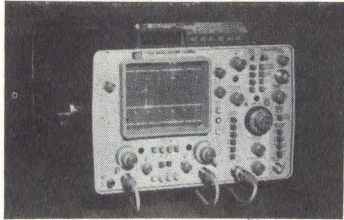
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## PRODUCTS

### 100-MHZ OSCILLOSCOPE

Model 1742A delta time oscilloscope allows measurements of time between 2 observed events to be made with 1% accuracy; dual channel delta time (time interval) is built in. An optional 3½-digit autoranging digital multimeter displays

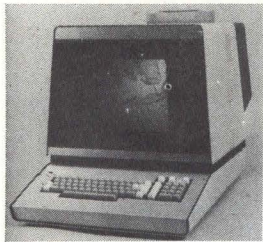


time in seconds, milliseconds, or microseconds, and can be used to measure ac and dc voltage and current as well as resistance. In delta time mode, the unit measures time between 2 events on either channel A or B, or

between an event on 1 channel and an event on the other. Continuous trigger view capability permits either external or internal trigger source to be simultaneously displayed with the 2 vertical channels. Vertical deflection factors range from 5 mV to 20 V/div over the full 100-MHz range. **Hewlett-Packard Co**, 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 266 on Inquiry Card

### PLASMA DISPLAY GRAPHICS TERMINALS



A desktop configuration stand-alone graphics terminal incorporating a disc operating system with full size floppy disc drives, ORION-60 DOS includes an editor, 8080 assembler, dynamic debugger, and file handler. In addition, DOS will support both a FORTRAN IV compiler and a BASIC interpreter containing

graphics subroutines and extensions as well as other high level languages. An optional random access 35-mm rear projection unit, which may be contained within the system enclosure, allows optical information to be projected onto the rear of the screen and combined with computer generated graphic displays. A touch panel option provides data entry from the screen by sensing the operator's finger. **Magnavox Display Systems**, 2131 S Coliseum Blvd, Fort Wayne, IN 46803.

Circle 267 on Inquiry Card

### INDUSTRIAL AUTOMATION COMPUTER

Features of the MiniMizer 10 series control computers, aimed specifically at the industrial automation user, include analog and digital I/O subsystems with multiple differential outputs, self-scanning ADCs, programmable gains and ranges, current and voltage outputs, optically isolated digital I/O, and power switching ac or dc outputs. Series comes in 7- or 14-card heights, for rackmounting or in a cabinet for tabletop use. 16-bit multiple general register architecture is implemented on a single n-MOS chip. Add-on memory modules include RAMs, p/ROMs, and CMOS. Various serial communications options and other peripherals are supported. Powerful Executive program is resident in an over 8k-bit p/ROM. Programs are written in BTRAN<sup>®</sup>, a high level language combining best features of BASIC and FORTRAN. **Stynetic Systems Inc**, Flowerfield Ind Pk, St James, NY 11780.

Circle 268 on Inquiry Card

### SELF-PROGRAMMABLE LOGIC STATE ANALYZER



The 32-channel model 532 intelligent logic state analyzer is capable of programming itself for automatic operation. Using auxiliary memory board which plugs directly into internal bus, analyzer can store 8 individual tests: 1 in RAM and 7 in UV p/ROMs. Analyzer is connected to a known good system and conditions for triggering are programmed in through the keyboard. With known good system operating and triggering conditions satisfied, a 32-bit x 250-word set of data is collected by main memory. A data compression algorithm operates on the data to compute a representative hexadecimal signature. This signature, the data set, and front panel settings may be transferred from main memory to an auxiliary memory element. **Paratronics, Inc**, 800 Charcot Ave, San Jose, CA 95131.

Circle 269 on Inquiry Card

### PROGRAMMABLE DISPLAY TERMINALS

7000 series terminals incorporate 16-bit microcomputers, and are offered in three versions depending upon programming configurations, memory size, and other considerations. All have 14" (35.6-cm) diag screens, 128-char set, expandable to 912, and split screen option that allows the screen to be divided into 8 independent display areas. Memory and programming features combined with operating features enable users to custom tailor a program from the keyboard. Operating features of models 7000, 7500, and 7300 include 7 x 9 dot matrix, character generation in a 10 x 12 field, extended character sets (up to three 224-char sets can be resident), 6 separate video attributes such as blink, underscore, and reverse, and special keyboards with up to 20 program function keys. **Delta Data Systems Corp**, Woodhaven Industrial Pk, Cornwells Heights, PA 19020.

Circle 270 on Inquiry Card

### MOVING FONT LINE PRINTERS



Series 3000 models 3600, 3300, 3150, and 3075 provide 600, 300, 150, and 75 lines/min respectively and feature a single line advance time of 25 ms and a slew speed of 15 in/s (38.1 cm/s). Inking is via operator-replaceable cassette using a Mobius endless loop, 0.56" wide x 66 yd long (1.42 cm x 60 m), inked nylon ribbon. Units offer a std 64-char ASCII set, with 48-, alternate 64-, 96-, and 128-char repertoires available as options.

Character element is a lightweight single piece, operator interchangeable, type band. Microprocessor driven printer is full-line buffered with selftest capability. **Data Printer Corp**, 99 Middlesex Ave, Malden, MA 02148.

Circle 271 on Inquiry Card



### AC-DC AND DC-DC SWITCHING POWER SUPPLIES

Black Demon series PWM inverter type supplies employ 1-switch transistor circuit, and achieve control by a single dc voltage, to offer a significant increase in power density. Single-ended transistor circuit, which is pulse width modulated but feeds power forward by normal transformer action method, eliminates core saturation problems to provide 70,000-h MTBF. Ratings of 5 Vdc at 10 A through 48 Vdc at 1.5 A in 115- or 220-V nom ac input are available with dc inputs of 12, 28, or 48 V nom. **Adtech Power, Inc.**, 1621 S Sinclair St, Anaheim, CA 92806. Circle 272 on Inquiry Card

### EXTRA LENGTH DATA CARTRIDGE

Providing 50% more data capacity and 450' (137 m) of tape interchangeable with Scotch brand DC 300A data cartridge, DC 300XL is suitable for back-up of disc data systems and in applications where extensive logging is involved. The tape was developed for the cartridge; an improved heat-stable hub provides additional reliability. The device operates with data processing and data handling systems; 2 sizes are DC 300 for std systems and DC 100 for minicomputers and terminal systems. **3M Co.**, PO Box 33600, St Paul, MN 55133. Circle 273 on Inquiry Card

### HIGH VOLTAGE CABLE BREAKDOWN TEST SET

Shorts, opens, and miswires in connectorized cables can be identified quickly using front panel selectable test voltages of 28, 100, 250, and 500 Vdc on the hi pot test set. Models have 50 or 100 points. Test dwell time is programmable from 10 ms to 9.99 s. LED displays and indicators show type and location of faults. Insulation resistance threshold is adjustable from 5.3 k $\Omega$  at 28 V to 1000 M $\Omega$  at 500 V; max test current is limited to 6 mA. **Addison, Inc., div of Muirhead**, 1101 Bristol Rd, Mountainside, NJ 07092. Circle 274 on Inquiry Card

### IMAGE DIGITIZERS

IEEE-488 compatible interface and choice of a digital field or frame grabber can be coupled directly to computer. DS-12F with 256 x 256 pixel resolution and DS-20F with 512 x 512 pixel resolution allow modular memory expansion. Model DS-12F digitizes a field in 0.0167 s, while model DS-20F digitizes an entire frame in 0.033 s. Both units store information in RAM or pass it on to a CPU via IEEE-488 compatible interface bus. **Quantex Corp.**, 252 N Wolfe Rd, Sunnyvale, CA 94086. Circle 275 on Inquiry Card

### CRT TERMINAL SWITCHING POWER SUPPLY



Low field leakage and optional synchronized input for minimal video disturbance are features of the SPU series switch regulated power supplies designed to match critical needs of CRT terminals. Multiple output voltage ranges are available. Model SPU-5-15/15 delivers 5, 15, and -15 Vdc at 200 W continuous duty. Short, overload, and overvoltage protection is provided. Series has  $\pm 5\%$  voltage adjustments on all outputs, switch selected 110- or 220-Vac inputs. **Dynetic Systems Corp.**, 19128 Industrial Blvd, Elk River, MN 55330. Circle 276 on Inquiry Card

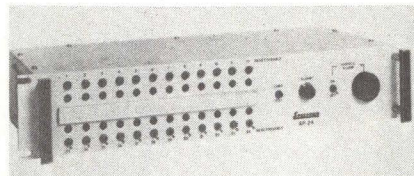
### MULTITASKING EXECUTIVE FOR PDP-11

MTX-11, a multitasking executive for PDP-11 and LSI-11 computers, maximizes computer's throughput and efficiency using intertasking communications techniques. Software executes

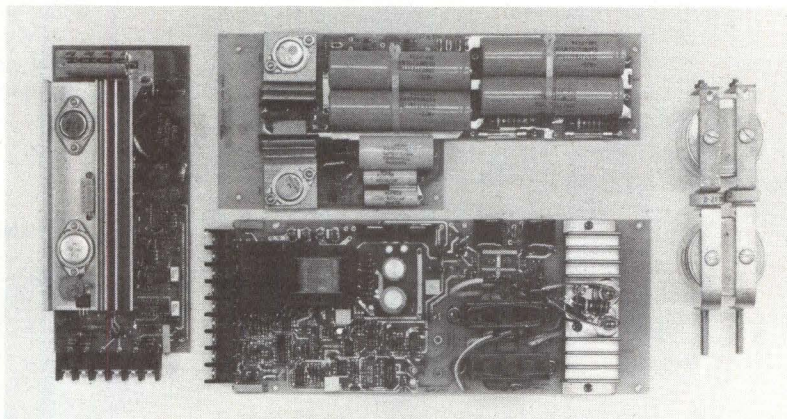
multiple tasks on an interleaved basis with software priorities determining which task to execute if competition exists for CPU and system resources, providing rapid response times and high data throughput. **Virtual Systems, Inc.**, 1500 Newell Ave, Suite 406, Walnut Creek, CA 94596. Circle 277 on Inquiry Card

### INTERFACE SIGNAL ALARM PANEL

Faulty or marginal circuits are identified by the AP-24, a data communications diagnostic tool that provides an alarm when an RS-232 signal from up to 24 EIA interfaces is absent or lost for a specified time period. It may supplement the computer console printer, or provide an alert panel in the communications control center. Features include individual channel monitoring, with reset and disable switch, and adjustable time interval from 0.001 to 20 s. **Spectron Corp.**, PO Box 620, Moorestown, NJ 08057.



Circle 278 on Inquiry Card



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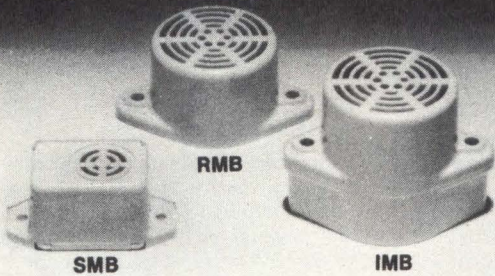
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## PRODUCTS

### MICROPROCESSOR CONTROLLED LINE PRINTERS



Graphics capability, program controlled font selection, and a choice of plug compatible interfaces are offered by 300-, 250-, 160-, and 125-line/min printers. The 132-col 300- and 160-line/min models print 7 x 7 char; 250- and 125-line/min units form 5 x 7 or 9 x 7 char. Users may change fonts on command, selecting from 12 different styles including true lower case, double height, and double width. Graphics capability

is also offered. Microprocessor-based RS-232 and plug compatible interfaces are available for popular CRTs, minicomputers, and microprocessors. All include built-in diagnostics.

**Okidata Corp.**, 111 Gaither Dr, Mt Laurel, NJ 08054.

Circle 279 on Inquiry Card

### IEEE-488 BUS INTERFACE FOR UNIBUS PDP-11

IB-11, a bus interface conforming to the IEEE Std 488-1975 instrumentation bus, permits as many as 15 instruments to be connected to PDP-11s with Unibus architecture. Field-installable, the interface can be integrated into standard laboratory systems, such as DECLAB 11/34 and 11/60. It is complemented with a set of FORTRAN-compatible subroutines, incorporating commands such as "call IBSEND" and "call IBGET" to allow full access to the bus functionality while reducing need for the user to manage protocol details. Mnemonic calls are designed for easy recognition, minimizing program development time. **Digital Equipment Corp.**, Maynard, MA 01754.

Circle 280 on Inquiry Card

### MULTICHANNEL WORD GENERATOR

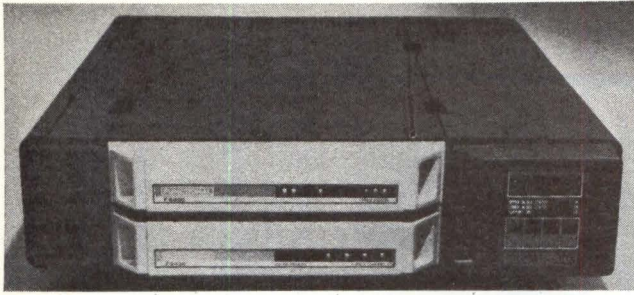


Offering from 1- to 8-channel operation with 10-MHz data rates up to 512 total bits, the model RS-600 word generator features separate external clock and trigger inputs, separate sync and data clock output, and TTL compatible inputs and outputs, and offers easy front panel programming. Switch-selectable output modes range from 1 channel x 512 bits to 2 channels x 256 bits/channel, 4 channels x 128 bits/channel, or 8 channels x 64 bits/channel. Users define total number of bits to be output by setting the last address thumbwheel switch. Output word/bit period is set by internal period thumbwheel switches and ranges from 1 to 999 with 100 ns, 1  $\mu$ s, or 1 ms resolution. **Interface Technology**, 852 N Cummings Rd, Covina, CA 91724.

Circle 281 on Inquiry Card



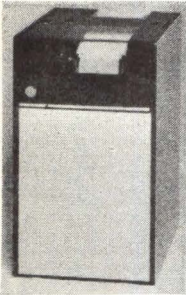
## 7.5M-BYTE, 64-BIT SCIENTIFIC COMPUTER



F6400, a 64-bit computer designed specifically for manipulation, storage, and retrieval of large volumes of data, allows users to place all working data and program information in memory rather than segmenting it onto discs. Architecture of the system enables each CPU to simultaneously read or write on up to 28 separate disc drives. Each computer can have up to 2G bytes of disc storage and multiple CPUs can be interconnected in a network. I/O throughput rate of up to 40M bytes/s allows each CPU to have up to 60 micro-processor controlled terminal ports in operation simultaneously. The system is designed to compile and execute PL/I and FORTRAN IV+. **Functional Automation**, 118 North-eastern Blvd, Nashua, NH 03060.

Circle 282 on Inquiry Card

## 300-LINE/MIN PRINTER FAMILY



Offering both parallel and serial interfaces, 80-col (154), 132-col (202), and 72-col forms access (250) printers are included in the Innovator line of 300-line/min printers. Forms access printer provides for immediate access to a printed form, utilizing a tear bar to avoid waste when printing forms such as airline tickets. All models operate at 300 lines/min and use tractor feed mechanism. Each fully formed character is printed on paper by a hammer for each column within a rotating carrier belt. Up to 6

copies can be achieved. Type carriers are available with OCR, gothic, and Katakana fonts. Print speeds up to 500 lines/min can be obtained using the optional IBM 1403 equivalent 48-char set. **Innovative Electronics, Inc.**, 15200 NW 60th Ave, Miami Lakes, FL 33014.

Circle 283 on Inquiry Card

## SYNCHRONOUS/ASYNCHRONOUS PORT SELECTORS

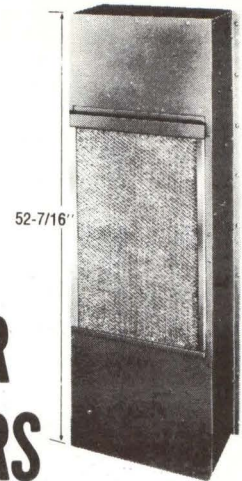
Timeline 450 computer port selector accommodates synchronous and asynchronous inputs at mixed speeds to 9600 bits/s and allows up to 254 lines to contend for up to 32 ports. As many as 32 of the 254 lines may be synchronous and contend for up to 16 of the 32 ports. Port selectors handling all asynchronous traffic to 1200 bits/s will allow the 254 lines to contend for as many as 124 ports. An optional automatic computer select (ACS) feature allows 1 port selector to serve multiple CPUs. The user makes choice via terminal keyboard and the 450 makes connection to proper computer. Users with front ends having automatic speed recognition may also specify automatic baud recognition on port selector asynchronous inputs. **Infotron Systems Corp.**, Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.

Circle 284 on Inquiry Card

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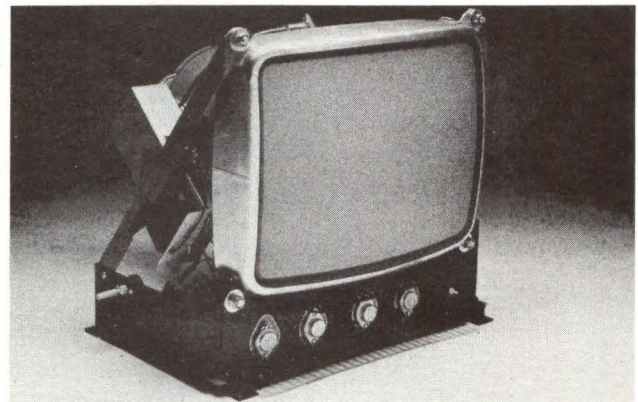
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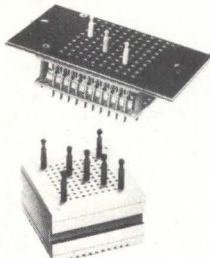
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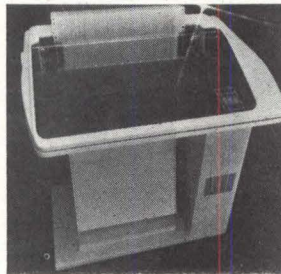
Analytical Systems Corporation

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**CIRCLE 135 ON INQUIRY CARD**

## PRODUCTS

### 180-CHAR/s BIDIRECTIONAL PRINTER



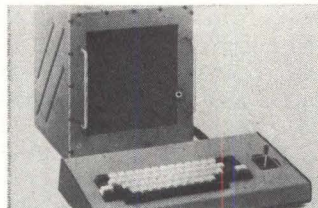
Models 6073 and 6074 Dasher™ LP2 printers offer high performance and functionality by incorporating mechanical assemblies with minimum parts count, 16-bit microNova™ microprocessor, and firmware driven operation. Logic seeking bidirectional printing results from use of the microprocessor. Efficient use of central processor

time is improved by use of RAM which is available to the microprocessor for buffering incoming data. Printhead uses a free-flight design in which small armatures propel printwires, substantially reducing tip wear and extending head life. Devices are RO with parallel interfacing for high speed output. Speeds range from 80 lines/min for 132-char lines to 300-lines/min for lines of 20 char. **Data General Corp**, Rte 9, Westboro, MA 01581.

Circle 285 on Inquiry Card

### MIL-SPEC PLASMA DISPLAY TERMINAL

Model PD 3000 offers a 20,000' (6.1-km) operating, 70,000' (21-km) nonoperating, high altitude capability and high resolution graphics with more than 4000 characters displayed. Op temp range is -32 to 55 °C. Weighing 53 lb (24 kg) and measuring 13 x 14 x 12"



(33 x 35 x 30 cm), compact unit has a flicker- and distortion-free flat panel display area of 8.5 x 8.5" (21.6 x 21.6 cm). An rfi-emi enclosure to meet MIL-E-5400R, MIL-STD 901C, and MIL-STD-461 is std. Software includes a realtime macroinstruction set that provides sub-routines for display control, alphanumeric display, and incremental and vector graphics. An internal 16-bit parallel microprocessor with 330-ns execution time enables a worst case vector line to be written in 10 ms. **Interstate Electronics Corp**, 707 E Vermont Ave, Anaheim, CA 92803.

Circle 286 on Inquiry Card

### LED PCB PANEL LIGHT WITH VARIABLE HEIGHT MOUNTING

Allowing the viewing plane to be changed without repositioning PC board or panel, PC201 series LEDs incorporate from 1 to 3 0.125" (3.175-mm) extenders which fit directly on the basic LED and are constructed of black nylon. Each extender has 0.020" (0.508-mm) standoffs on the bottom for flow soldering. At a drive current of 20 mA, the devices output 50 mcd (red), 32 mcd (amber), and 24 mcd (green) typ with clear tinted encapsulation. Available with built-in resistors for various voltages ranging from 2.4 to 28 Vdc, units are also available for ac operation. BPS-1 sockets, available for mounting the devices in sockets instead of soldering, provide a tight secure mount. **Data Display Products**, 303 N Oak St, Inglewood, CA 90301.

Circle 287 on Inquiry Card



# LITERATURE

## Data Couplers

Data sheet, which covers data coupler option, describes interfacing digital clocks directly to communications port of a computer, CRT terminal, teleprinter, or other recording device. **Chrono-Log Corp.**, Havertown, Pa.

Circle 300 on Inquiry Card

## Keyboards

Model R53/LTT keyboard that incorporates a microprocessor and low profile, reed keyswitches is explained in brochure including electrical and mechanical data. **C. P. Clare & Co.**, Chicago, Ill.

Circle 301 on Inquiry Card

## Wires/Cables

Catalog includes cable selector guide, cross-reference tables, and glossary, thus serving as a comprehensive manual to those who specify electronic and electrical wire and cable. **Manhattan Electric Cable Corp.**, C-I-C Electronic Div, Rye, NY.

Circle 302 on Inquiry Card

## Color Graphics Computers

CG series of graphic and alphanumeric readout computers, consisting of 13, 15, and 19" (33, 38, and 48-cm) models, are covered in technical bulletin which states video display specs and options. **Chromatics, Inc.**, Atlanta, Ga.

Circle 303 on Inquiry Card

## Switching Power Supplies

Brochures outline specs of 500-W MG5-100 and 25-W MMG series miniature power supplies, including data voltages, frequency range, and brownout margins, and present attributes, packaging techniques, and dimensional diagrams. **Gould Inc., Electronic Components Div.**, El Monte, Calif.

Circle 304 on Inquiry Card

## Computer Performance Techniques

Proven techniques for use with available hardware and software to detect and prevent errors in automated data systems are detailed in a report entitled *Performance Assurance and Data Integrity Practices*. Price is \$2.20, stock #003-003-01879. **Superintendent of Documents, U.S. Government Printing Office**, Washington, DC 20402.

## $\mu$ Processor Compatible DACs

Bulletin presents specific features, block diagrams, tabulated performance specs, and logic diagrams illustrating 12-bit series 7545 and 7546 CMOS converters. **Beckman Instruments, Inc.**, Fullerton, Calif.

Circle 305 on Inquiry Card

## Multirate Wire Line Modem

Bulletin cites physical and electrical characteristics of a militarized wire line modem offering data rates in increments of 150, 300, 600, and 1200 bits/s in binary mode and 2400 bits/s in duobinary mode. **GTE Sylvania, Inc.**, Needham, Mass.

Circle 306 on Inquiry Card

## Permanent Magnet Motors

Ceramic, alnico, or rare earth permanent magnet motors, tachometer assemblies, and cube torque and stepper motors are featured in catalog containing schematics, performance curves, and drawings. **Clifton Precision, Litton Systems, Inc.**, Clifton Heights, Pa.

Circle 307 on Inquiry Card

## Communication Equipment

Technical summaries, application information, and block diagrams are furnished in booklet encompassing line of am, FSK, and analog telemetering transmitters and receivers, as well as encoders and decoders. **RFL Industries, Inc.**, Boonton, NJ.

Circle 308 on Inquiry Card

## Test and Measuring Instruments

Catalog provides information, technical specs, and illustrations of test and measuring instruments such as oscilloscopes, recorders, multimeters, voltmeters, signal generators, and audio and video service equipment. **Philips Test & Measuring Instruments, Inc.**, Mahwah, NJ.

Circle 309 on Inquiry Card

## Solid-State Uninterruptible Power Systems

Illustrated brochure lists components, std features, special options, and specs; and describes design and engineering direction of Accupower<sup>®</sup> line of solid-state ups. **Emerson Electric Co., Industrial Controls Div.**, Santa Ana, Calif.

Circle 310 on Inquiry Card

## Matrix Printhead

Ballistic<sup>™</sup> printhead for matrix printers is described in 2-pg technical bulletin which discusses operating principles, full electrical and print specs, pc board connections, and physical dimensions. **Lear Siegler, Inc./Electronic Instrumentation Div., Data Products**, Anaheim, Calif.

Circle 311 on Inquiry Card

## Plug and Socket Connectors

Blade-type plug and socket connectors for panel and cable mounting are exhibited in catalog which includes specs, connector and panel mounting dimensions, and photos of all connector types. **Vernitron Corp., Beau Products Div.**, Laconia, NH.

Circle 312 on Inquiry Card

## PDP-11 Enhancements

Literature packet includes data sheets, page of programming specs, and deck of pocket-sized cards with a photo and technical summary of PDP-11 enhancement models. **Able Computer Technology, Inc.**, Irvine, Calif.

Circle 313 on Inquiry Card

## Single-Chip $\mu$ Computer

Catalog gives overview of S2000 computer-on-a-chip by pointing out architecture, special operating modes, specs, instruction set, and design support tools available. **American Microsystems, Inc.**, Santa Clara, Calif.

Circle 314 on Inquiry Card

## Networking Distributed Computers

Brochure summarizes Phase II DECnet software products, charts product functionality on communication and user/program levels, and describes RAMP features. **Digital Equipment Corp.**, Northboro, Mass.

Circle 315 on Inquiry Card

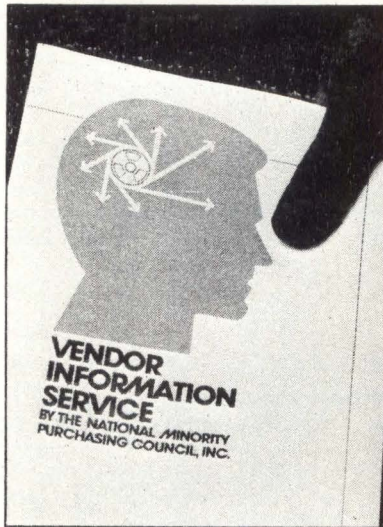
## 2400-Bit/s Modems

Illustrated sections in booklet elaborate on design and operation, indicators and controls, test features and options, and specs of the 24 LSI Mark II and CS 24 LSI series modems. **Racal-Milgo, Inc.**, Miami, Fla.

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## LITERATURE

### Pushbuttons/Selectors/Lights

Over 20 basic models are listed in 12-pg catalog with details on control function options and color choices for line of miniature oil-tight pushbuttons, selectors, and pilot lights. **Alco Electronic Products, Inc.**, North Andover, Mass. Circle 317 on Inquiry Card

### Programming Language

Bulletin L-2589 comprises process flow diagrams, control tasks, and I/O specs for SPEAK EASY language which programs the company's UDAC™ process controllers. **Reliance Electric**, Cleveland, Ohio. Circle 318 on Inquiry Card

### μP and Logic Analyzers

Booklet introduces concepts of microprocessor and logic analyzers with photos, timing diagrams, data domains, and map modes for both. **Biomation**, Santa Clara, Calif. Circle 319 on Inquiry Card

### Electronic Hardware

Catalog contains detailed drawings, material and performance specs, photos, and application data for line of hardware including socket and terminal strips, IC sockets, adapters, plugs, and jacks. **Samtec, Inc.**, New Albany, Ind. Circle 320 on Inquiry Card

### Computer-Aided System

Brochure describes capabilities of computer-aided design, drafting, and manufacturing (DDM) to be used during entire design cycle to develop ideas and mechanical designs. **Calma**, Sunnyvale, Calif. Circle 321 on Inquiry Card

### Miniaturized Power Supplies

Catalog outlines parameters and key operating specs of std submodule line of power supplies which feature from 1 to 10 outputs ranging from 0 to 300 Vdc. **Arnold Magnetics Corp.**, Culver City, Calif. Circle 322 on Inquiry Card

### Test Systems

Brochure provides information and specs on 203 semiconductor memory test system with full description of three subsystems and a review of system software. **Siemens Corp., Measurement Systems Div.**, Cherry Hill, NJ. Circle 323 on Inquiry Card

### Word Processing Keyboard

Brochure describes assignment coding matrix, 3-mode operational system, and key arrangement for ASR 33 keyboard, and also contains electrical data specs and mechanical descriptions. **Datanetics Corp.**, Fountain Valley, Calif. Circle 324 on Inquiry Card

### CMOS Chips

Catalog describes variety of CMOS ICs including the 4000 series of std and time-keeping circuits, 1802 microprocessor and associated I/O circuits, and both ROM and RAM products. **Solid State Scientific, Inc.**, Montgomeryville, Pa. Circle 325 on Inquiry Card

### A-D/D-A Peripheral Systems

Brochure on SineTrac PDP series slide-in cards for DEC PDP-11 minicomputers is composed of block diagrams and details on mounting, channel expansion, and programming methods. **Datel Systems, Inc.**, Canton, Mass. Circle 326 on Inquiry Card

### Multiplier Applications

Examples of applications, theory, and a bibliography are included in guide which shows ideas on using multipliers, dividers, squarers, and square rooters to solve analog problems. **Analog Devices, Inc.**, Norwood, Mass. Circle 327 on Inquiry Card

### Microcomputer Systems

52-pg, 4-color catalog details line of kit and fully assembled microcomputers, accessories, software packages, parts, and literature. **Tandy Computers, a div of Tandy Corp.**, Fort Worth, Tex. Circle 328 on Inquiry Card

### Reed Relays

Guide for electronic specifiers and buyers of reed relays contains mechanical and electrical characteristics, dimensional drawings, and device schematics. **Hamlin, Inc.**, Lake Mills, Wis. Circle 329 on Inquiry Card

### DC-DC Power Supplies

"Design-A-Kit" form that simplifies special dc-dc supply specs and requirements serves as fundamental user's guide for requesting quotation from manufacturer. **Stevens-Arnold, Inc.**, South Boston, Mass. Circle 330 on Inquiry Card



# GUIDE TO PRODUCT INFORMATION

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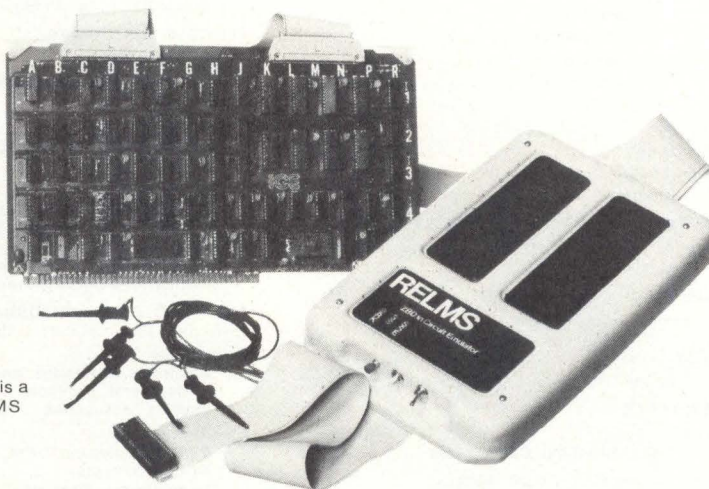
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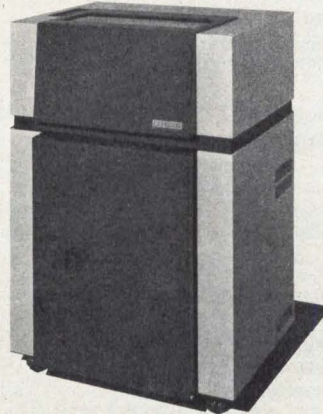
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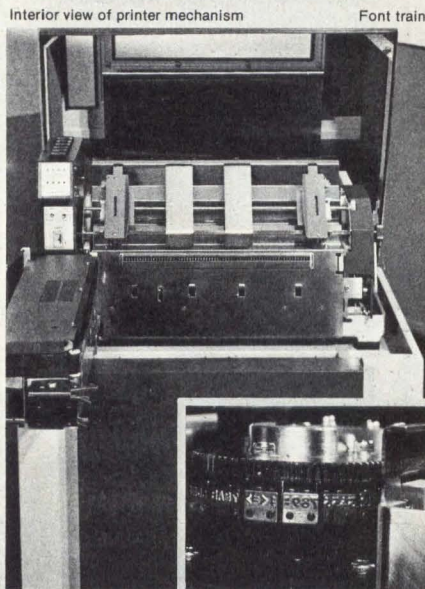
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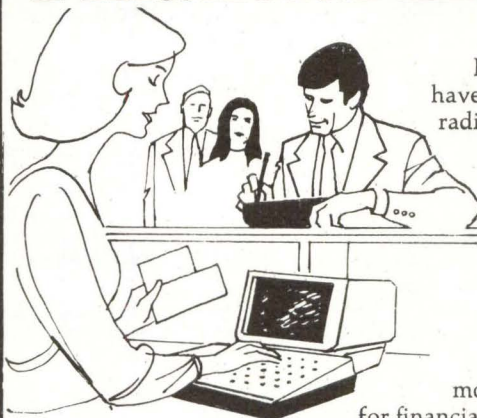
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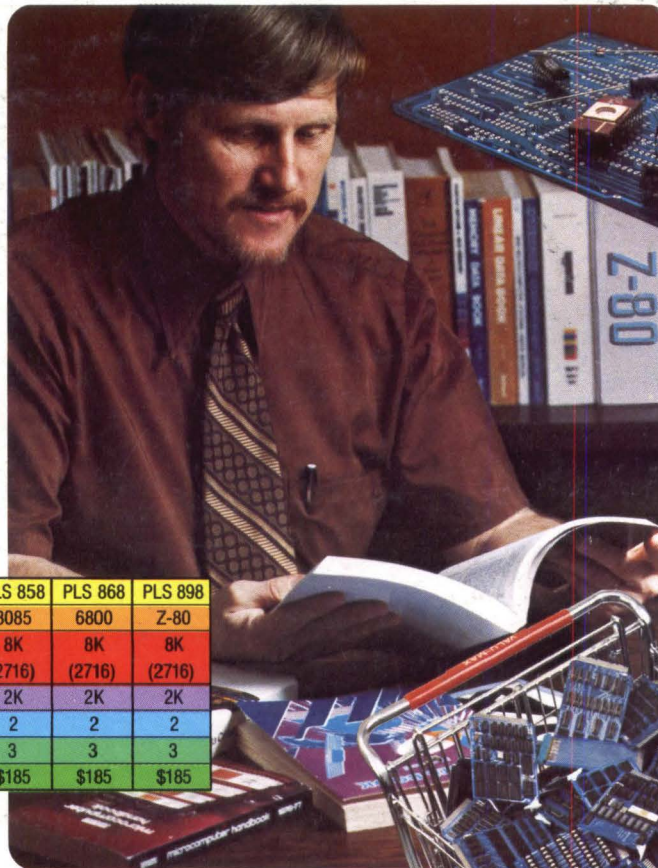
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