NXP Semiconductors
Application Note

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S32V234 Hardware Design Guide

1. Introduction

S32V234 is a high-performance automotive processor designed to support computationally intensive sensor fusion and vision applications that require automotive safety levels, consisting of up to four ARM® Cortex-A53®, one Cortex-M4®, dedicated modules and processors for acceleration of image vision processing tasks. The device architecture is developed with scalability in mind.

It enables users to leverage leading edge Camera Vision modules like APEX2, ISP, GPU and others.

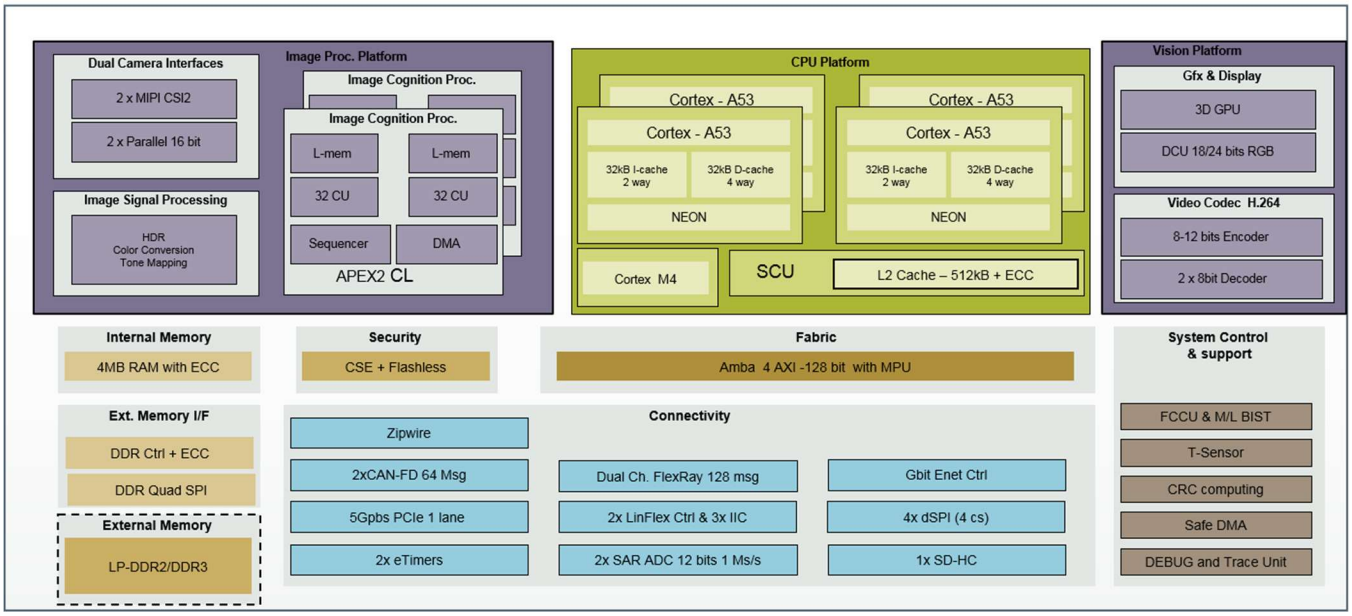
This application note illustrates the S32V234 power supply options and details the external circuitry required for power supplies, oscillator connections, and supply decoupling pins. It also discusses configuration options for clock, reset, ADC modules, MIPI-CSI2 and Display interfaces, as well as recommended debug and peripheral communication connections and other major external hardware required for the device.

Please note that information from the S32V234 Reference Manual, Data Sheet, and/or Errata report may be repeated in this application note for the convenience of the reader. The Reference Manual, Data Sheet and Errata report are the official specifications for S32V234 and should be reviewed

Contents

for the most up-to-date information available for this device.

Figure 1. S32V234 block diagram



1.1.1. S32V234-EVB2 Evaluation Board

The S32V234 EVB2 is the evaluation board created by NXP for this device. We recommend using it as example when creating a new board. This board was not designed for a real automotive production environment but can be helpful to answer many doubts about connecting interfaces and HW configurations for someone creating a new design. See www.nxp.com/s32v234evb for more details about this evaluation board. Note however that the DDR3/L byte lane prime connection on the EVB2 is known to be incorrect.

1.1.2. Recommended Reference Manual Sections

The following sections are recommended reads for Hardware Engineers designing a PCB with S32V234 device:

- Chapter 2: Introduction. It will give a general overview of what is available on the device.
- Chapter 5: Signal Description. In addition to this chapter, the RM has some files attachments. Refer to the IO Signal table for details about each pin in the device.
- Chapter 20: System Integration Unit Lite2: This system provides control over all the electrical pin controls and GPIO.
- Chapter 22: Clocking. Provides a global understanding of the clock architecture
- Chapter 28: Reset Overview: Provides a general understanding of Reset architecture and modules.

- Chapter 67: Power Management
- Chapter 70: Functional Safety Overview: provides a quick reference regarding Functional Safety documentation available

2. S32V234 Design Checklist

This document provides a design checklist for the S32V234 processor. The design checklist tables recommend optimal design and provide explanations to help users understand better. All supplemental tables referenced by the checklist appear in sections following the design checklist tables.

2.1. Design Checklist Tables

2.1.1. Reset, TEST Pin and Boot Mode Checklist

Check box	Recommendations	Explanation/Supplemental Recommendations
	1. The EXT_POR should be asserted until all the SOC Voltage supplies have stabilized after power supply ramp.	While the PMC module within the device will not de-assert the internal POR until supply voltages are stable. It is advisable to wait for supply stability to avoid unnecessary device resets caused by LVD/HVD triggered resets.
	2. A 10KΩ pull-up is recommended on RESET. If a decoupling capacitor is used on the RESET or EXT_POR signals, the RC time constant must not exceed 1ms.	If the time constant is such that the RESET signal rises too slowly, this may result in the input circuit oscillating.
	3. Check that TEST pin is connected to GND	This is for factory test only.
	4. BOOTMOD[0] (AC20) and BOOTMOD[1] (AC21) pins must not be left floating. Make sure these signals have been pulled up/down as required with a 10kΩ resistor.	Use pull-up or pull-down resistors to select the desired boot mode. See RM for details.
	5. Make sure all signals that require to be pulled to a defined input state are pulled with an external resistor up to 10kΩ instead of the internal pulls.	Internal default weak pulls are not always strong enough, external pulls are always required for defined signal states. Use of 100k pad pull settings by software is not recommended.

2.1.2. Oscillator/ Crystal Checklist

Check box	Recommendations	Explanation/Supplemental Recommendations
	1. Choose 1 of the 2 clocking options; • Connect a 40MHz crystal between EXTAL and XTAL. • Connect a suitable 40MHz single end clock input to EXTAL.	Clock input may only be 40MHz
	2. If using an external oscillator instead of a crystal check erratum e11133	The erratum describes the conditions that must be met to properly boot with an external oscillator

2.1.3. DDR3/L Checklist

Check box	Recommendations	Explanation/ Supplemental Recommendations
	1. Connect the DDR0_ZN and DDR1_ZN balls on the processor to a 240Ω, 1% resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. If swapping of byte lanes has been used to ease layout routing. The S32V2 DM and DQS signals must match that of the connected byte lane (DM0, DQS0, nDQS0 must follow the Least significant byte).	Control signals must match the Byte Lane Data signals.
	3. If swapping bits within the byte lane, the prime bit of each byte (D0, D8, D16 etc) must not be swapped.	During write leveling, the CLK sampling feedback Is driven onto the prime bit of each byte and sampled by S32V2 controller on the prime bit only.
	4. Only one ODT signal is required per CS signal.	
	5. The architecture for each chip inside the DRAM must be x16 or x32.	This processor does not support byte mode
	6. DDRx_CLK0 should have more propagation delay to a memory chip on the PCB layout than the corresponding DQS for that	This allows write leveling calibration perform correctly.

	memory chip. The extra propagation delay should not exceed ½ clock.	
	7. 16 bit mode is not recommended due to reduced throughput	S32V234 uses cases normally require high throughput and a 16bit bus will be limiting. In addition, erratum e11136 is applicable and calibrations routines need to be software based.

2.1.4. LPDDR2 Checklist

Check box	Recommendations	Explanation/ Supplemental Recommendations
	1. Only 32bit configuration mode is supported	For LPDDR2 the controller only supports 32bit mode, check erratum e11136 for more details
	2. Make sure your design does not use LPDDR2 memories that are dual die and have a single CS.	Review erratum e11155, we don't recommend dual die memories for new designs.
	3. Connect the DDR0_ZN and DDR1_ZN balls on the processor to a 240Ω, 1% resistor to GND.	This is a reference used during DRAM output buffer driver calibration.
	4. CKE0 and CKE1 require external pull-down resistors to GND for JEDEC compliance when using LPDDR2.	CKE[1:0] must be pulled down to meet the JEDEC sequence until the controller is configured and starts driving. NXP designs use 10kΩ

2.1.5. Power Supplies

Check box	Recommendations	Explanation/ Supplemental Recommendations
	1. For part numbers that GPU is not available VDD_LV_CORE_GPU power supply must be connected to ground.	Connecting the GPU Supply to ground will ensure no additional leakage current is consumed by the device.
	2. For part numbers with 2 cores VDD_LV_CORE_ARM must be connected to ground.	Connecting the CPU supply to ground will ensure no additional leakage current is consumed by the device.
	3. Apart from the special cases of the VDD_LV_CORE_GPU and VDD_LV_CORE_ARM all remaining	The device can malfunction if any of the supplies is not powered apart from the special cases mentioned on 1 and 2.

	power supplies must be always powered	
	4. Make sure the supply voltage level properly matches the devices connected to the I/O being fed by that voltage rail	The device allows some supplies to work at 3.3V or 1.8V, double check that you don't have incompatible voltage connected to those rails or proper voltage level translators are used.

2.1.6. PCIe Checklist

Check box	Recommendations	Explanation/Supplemental Recommendations
	1. Use an appropriate reference clock generator.	The PCIe standard specifies a 100 MHz clock (Refclk) with greater than ±300 ppm frequency stability at both the transmitting and receiving devices.
	2. The differential transmitter must be AC coupled. Use a 0.1 µF-series capacitor on PCIE_TX_P and a second 0.1 µF on PCIE_TX_N.	To ensure PCIe specification compliance, AC coupling is required at each transmitter. The receiver must be DC coupled.
	3. Each PCIE_REXT ball should be connected to the ground through a 200Ω, 1% resistor.	The PHY uses an external resistor to calibrate the termination impedances of the high-speed inputs and outputs of the PHY.

2.1.7. MIPI CSI Checklist

Check box	Recommendations	Explanation/Supplemental Recommendations
	1. An accurate 15K ohm resistor with 1% variation or lower is required for CSIn_ZQ	Pin to connect an external reference resistor to for autocalibration.

2.1.8. QSPI/NOR-Flash Checklist

Check box	Recommendations	Explanation/Supplemental Recommendations
	1. For HyperFlash (from Cypress), the interface supports the NXP specific Central Read Strobe (CRS) functionality and is only supported on Flash A interface.	Make sure you order the NXP specific HyperFlash (Cypress) part number from your vendor.

2.1.9. I2C Checklist

Check box	Recommendations	Explanation/Supplemental Recommendations
	1. Verify the target I^2C interface clock rates.	The I^2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I^2C port.
	2. Verify that there are no I^2C address conflicts on any of the I^2C buses utilised.	There are multiple I^2C ports available on the chip, so if a conflict exists, move one of the conflicting devices to a different I^2C bus. If this is not possible, use an I^2C bus switch (**NXP part number** PCA9646**).**
	3. Do not place more than one set of pull-up resistors on the I^2C lines.	This could result in excessive loading and potential incorrect operation. Choose the pull-up value commensurate with the bus speed being utilized.
	4. Ensure that the VCC rail powering the I^2C interface balls match the supply voltage used for the pull-up resistors and slave I^2C devices.	Prevent device damage or incorrect operation due to voltage mismatch.

2.1.10. JTAG Standard Debug Connector Checklist

Check box	JTAG Signal	I/O Type	Recommendation	Supplemental / Comments
	TMS	I	10kΩ pull-up	

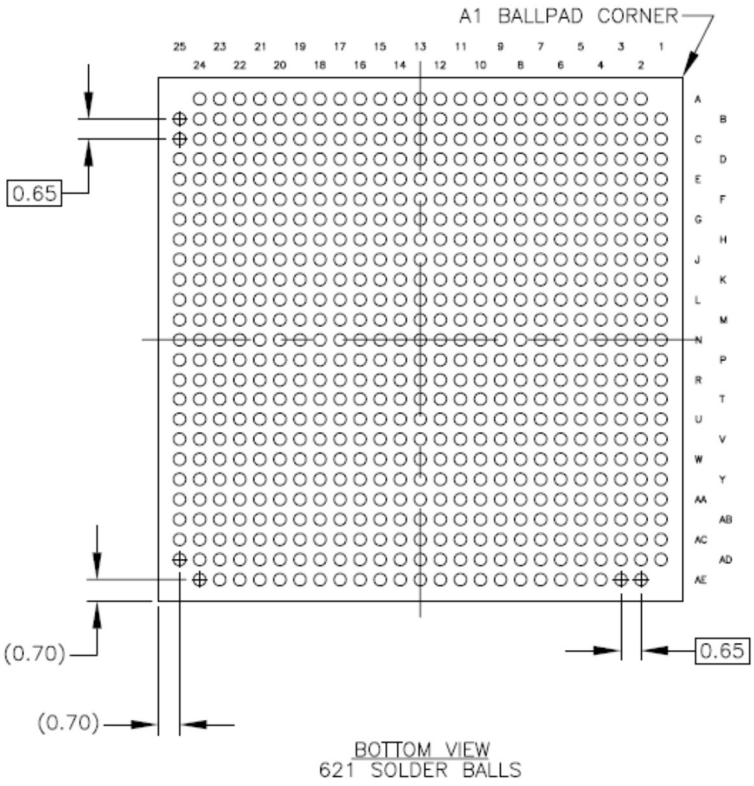
Check box	JTAG Signal	I/O Type	Recommendation	Supplemental / Comments
	TCK	I	10kΩ pull-down*	Is mandatory to place this pull-down otherwise LBIST can present failures.
	TDO	O	10kΩ pull-up	This is a three-state output signal
	TDI	I	10kΩ pull-up	
	JCOMP	I/O	Pull it down (10kΩ) if the debugger has access to the signal to overdrive it, otherwise pull it up	When this signal is pulled down it disables JTAG and boundary scan modes.

* Mandatory

3. S32V234 package overview

The S32V324 is available in a single package type: 621 FC-BGA package that is suitable for development, debug and commercial production.

Package dimensions are given below. For complete details please review the package datasheet which is available on nxp.com with the following package number: 98ASA00819D



Package

−17x17mm FCPBGA 0.65mm pitch

−Die thickness: 30mil (780µm)

−Die size: 7.62mm x 7.51mm

−SRO: 0.35mm SMD

−Solder Ball: 96.5Sn3.5Ag 0.40mm

4. Power supply

The S32V234 processor includes a robust power management infrastructure. It provides power monitoring for all internal voltages and clock gating capabilities for peripheral and core modules. The

monitoring capability is used to ensure supply voltages and internal voltages are within the required operating ranges before the processor can exit from the reset state and enter operation.

The S32V234 processor does not have an on-chip regulator. An external switching regulator should be used to derive core supply. The analog voltage supplies needs to be protected from noise on digital supply, at least by means of decoupling capacitors. Better filters can be used if they do not affect regulator stability. A separate regulator for analog supply is preferred.

The S32V234 processor has only one operating mode, with no specific standby or stop modes. However, by taking advantage of the devices clock gating capabilities current consumption can be greatly reduced.

Run Mode: Entire SoC is powered and clock gated.

- Run Mode with clock/power gating: the power consumption of the SoC can be managed by clock gating of the unused processing blocks and peripherals in the SoC and power gating blocks which supports it.

The main power supplies required are:

- 1.0 V external supply for the core voltage
- 1.8 V external supply for digital logic and interfaces, analog circuits and GPIO
- 3.3 V external supply for GPIO
- 1.2 V, 1.35 V or 1.5 V external supply for the DRAM I/O depending on the selected DRAM

4.1. Power Supply Proposal

The S32V234 is an SOC composed of a variety of high-performance computing cores, high speed memory interfaces, peripherals and analog subsystem modules. The supply current drawn on the 1V voltage rails dominates the overall power consumption of the device, with considerable static power consumption (leakage) at Tj=125°C for the worst silicon (please refer to the device datasheet, section Power consumption for the current information). Dynamic power consumption can be managed with clock gating or with frequency adjustment. For applications which do not require the GPU or Second A53 core per cluster, a static power gating options is available which should drastically reduce the maximum static power consumption.

NXP recommends using a primary FS85/FS84 regulator Vbat (12V/24V) and the secondary PF8200 PMIC for S32V234. This validated system solution meets the load requirements of the S32V234 SoC for all use-cases and provides the necessary safety mechanisms to comply with ASIL B functional safety ratings (scalable to ASIL C with proper supply monitoring).

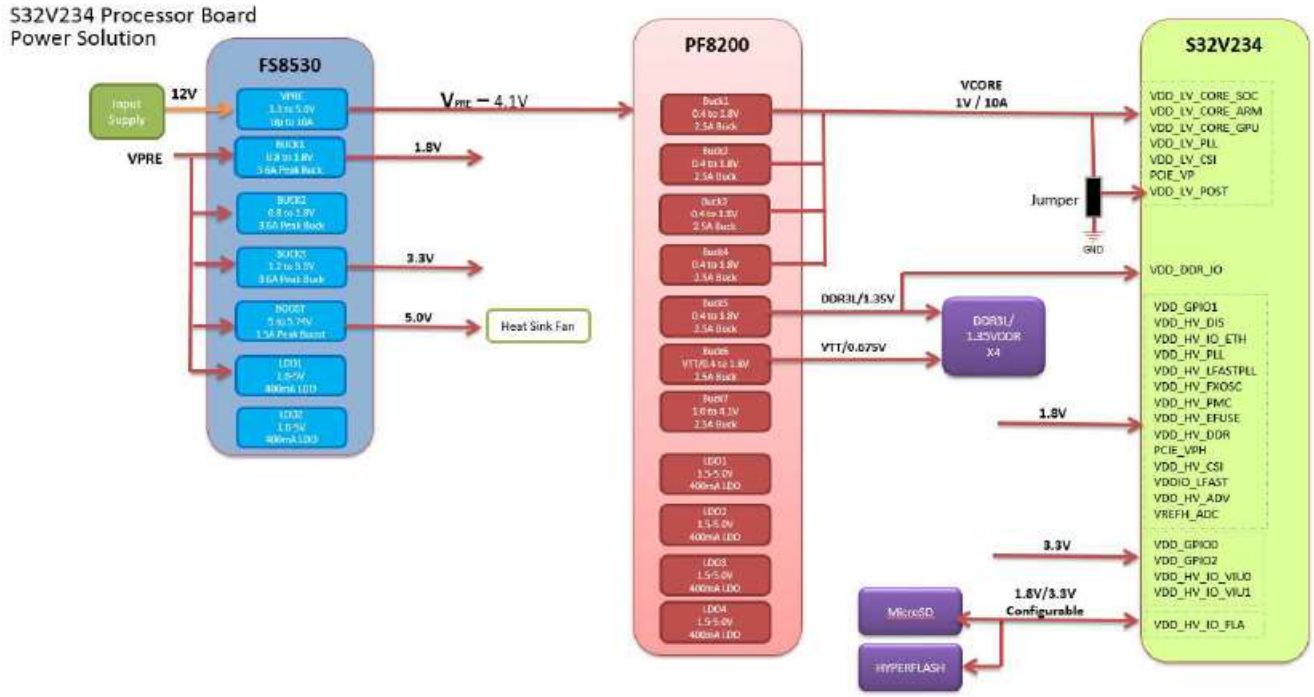
The recommended configuration is shown in the diagram below with the PF8200 rails connected as follows:

- Buck1 through 4 are configured in a Quad-phase architecture for best thermal distribution, ripple, noise and transient response. The Quad-phase DC-DC converter provides output current as high as 10A
- Buck 5 provides power to the DDR I/O rail
- Buck 6-7 supply the 1.8V/3.3V IO rails
- Buck 6 can optionally be used to provide VTT (by tracking Buck5/2)
- Four LDOs are also available to provide a low noise supply for the 1.5V-5V 400mA analog voltage supplies

The FS85/FS84 is an automotive grade, functionally safe multi-output power supply integrated circuit, with focus on Radar, Vision, ADAS, Radio and Infotainment applications. It includes multiple switch mode and linear voltage regulators. It offers external frequency synchronization input and output, for an optimized system EMC performance. In addition to this, FS85 provides Wake signals to achieve low power modes in the system.

The FS85/FS84 includes enhanced safety features, such as a fail-safe output, making it an integral part of a safety-oriented system partitioning, thereby covering different safety integrity levels (FS85 ASIL-D/ FS84 ASIL-B/ PF82 ASIL-B). It is developed in compliance with ISO26262 standard.

For more details about the FS8x and PF8x power regulators, please contact local NXP Sales Representative.



4.2. Power supply signals and decoupling

Supply ramp rate on all rails must be below 25 V/mS. Refer to the datasheet for further operating conditions of the power supplies.
The Power supplies are divided into three groups. **CORE, IO & Analog.** The rails are further subdivided by their voltage and again by their function.
Table 4 lists all the SOC power domains with the corresponding pin names.

SOC supply pins

Function	Supply Voltage	Description
VDD_GPIO0	3.3 V	Isolated I/O Voltage Supply for pad segment GPIO0 and PMC
VDD_GPIO<n=1,2> VDD_HV_IO_VIU0 VDD_HV_IO_VIU1 VDD_HV_IO_DIS VDD_HV_IO_FLA	1.8 V or 3.3 V	Isolated I/O 1.8V/3.3 V supply for multi voltage I/O segments
VDD_HV_IO_ETH	1.5 V / 1.8 V / 2.5 V / 3.3 V	Isolated I/O supply for multi voltage Ethernet IO segment
VDD_DDR_IO	1.2 V / 1.35 V / 1.5 V	LPDDR2/DDR3L/DDR3 IO Supply
VDDIO_LFAST	1.8V	LFAST IO Bank Supply
VDD_LV_CORE_SOC, VDD_LV_CORE_ARM, VDD_LV_CORE_GPU	1.0 V	Core Logic Low Voltage Supply
VDD_HV_CSI VDD_HV_PLL, VDD_HV_LFASTPLL, VDD_HV_FXOSC, VDD_HV_PMC, VDD_HV_EFUSE, VDD_HV_DDR VDD_HV_ADV PCIE_VPH	1.8 V	Internal Analog and PLL subsystem supplies 1.8V
VREFH_ADC		ADC Voltage Reference
VDD_LV_CSI VDD_LV_PLL PCIE_VP	1.0 V	Internal Analog and PLL subsystem supplies 1.0V

*VDD_LV_POST is for NXP internal test purposes only and must be connected to Ground in production board design.

4.2.1. Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the S32V234-EVB layout for an example of the desired decoupling capacitor placement.

The following list introduces how to choose correct decoupling scheme:

- Place the largest capacitance in the smallest package that budget and manufacturing can support.
- Minimize trace length (inductance) to small caps
- Series inductance cancels out capacitance
- Tie caps to GND plane directly with a via
- Place capacitors close to the power ball of the associated package from the schematic
- The smaller the capacitor value, the closer to the SoC pins it should be placed

Recommended decoupling per power supply

Supply	Decoupling Capacitors	Additional Notes
VDD_GPIO<n=0,1,2> VDD_HV_IO_VIU0 VDD_HV_IO_VIU1 VDD_HV_IO_DIS VDD_HV_IO_FLA VDD_HV_IO_ETH VDDIO_LFAST	1x 10 µF 1x 1 µF 1x 0.1 µF 2x 0.01 µF 1x 1000 pF	• Number of decoupling capacitors are per power rail. • Place one 0201 cap per power pin where possible.
VDD_DDR_IO	8x 1 µF 3x 0.1 µF 6x 0.01 µF 4x 1000 pF 3x 10 µF 3x 22 µF	• Place one 0201 cap per power/ground pin pair • Use 22µf and 10µf bulk caps to supply sufficient current at point of load
VDD_LV_CORE_SOC VDD_LV_CORE_ARM VDD_LV_CORE_GPU	4 x 22 µF 4 x 10 µF 14 x 1 µF 8 x 1000 pF	• Place one 0201 cap per power/ground pin pair • Place 10uF caps near to the device • Place 22uF caps near to power supply circuit
VDD_HV_CSI VDD_HV_PLL VDD_HV_LFASTPLL VDD_HV_XOSC VDD_HV_PMC VDD_HV_EFUSE VDD_HV_DDR VDD_HV_ADV PCIE_VPH	1x 10 µF 2x 1 µF 2x 0.01 µF 1x 1000 pF	• Number of decoupling capacitors are per power rail. • Place one 0201 cap per power pin where possible. • Ferrite recommended for analog supplies to isolate noise
VREFH_ADC	1x 1000 pF 1x 1 µF	• Place one 0201 cap per power pin where possible. • Ferrite recommended for analog supplies to isolate noise
VDD_LV_CSI VDD_LV_PLL PCIE_VP	1x 1 µF 1x 0.01 µF 1x 10 µF	• Number of decoupling capacitors are per power rail. • Place one 0201 cap per power pin where possible. • Ferrite recommended for analog supplies to isolate noise

4.3. Power Management Controller

The S32V234 has a dedicated module for configuration and monitoring of power supplies, enable signals, internal component trimming, and power-on reset generation. The Power Management Controller (PMC) consists of an analog block and a supporting digital interface that provides control over the analog components. The Power Management Controller chapter in the device reference manual explores the digital block in some depth.

NOTE: Please read the PMC chapter of the latest S32V234 reference manual. It describes the detailed sequences that must be followed during Reset and Power up which must be thoroughly understood when designing S32V234 hardware. This document gives an overview of the PMC and is not intended to replicate the full information.

5. Device Reset configuration

The S32V234 MCU requires only simple external reset circuitry. External circuitry for device configuration is not required. The device is configured during reset based on Fuse configuration/boot switch configuration.

5.1. External Reset signals

S32V234 device features two active-low external reset signals:

Functional reset (/RESET)
Power-on reset (/EXT_POR)

/RESET is a bidirectional reset input/output that indicates if the device is active (high signal) or in reset. It needs an external pull-up to ensure a high signal after the reset sequence has completed. A falling edge on this pin will trigger a functional reset to the Reset Generation Module(RGM). Forcing this pin low will keep the device in the last phase of the reset sequence (Phase3[Functional]).

/EXT_POR allows external supply circuits to signal to the MCU when power is available, so the power-up sequence can begin. It should be forced high when the critical power supplies cross the LVD threshold.

Both pins operate on the 3.3 V power domain.

NOTE: Input pins do not support hysteresis, therefore very slow ramps (like the ones generated by an RC circuit with a large RC value) can induce bounces in the input read state during the transition from logic low to logic high or vice versa. This applies to the /RESET and /EXT_POR and therefore it is recommended to use an 10kΩ pull up with a 0.1µF decoupling cap. Alternative RC values may be used, but the values must not result in an RC time constant greater than 1mS.

5.2. BOOTMOD and RCON pins

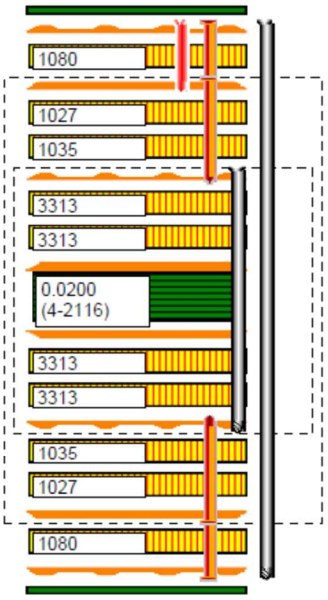
Typically, in development/pre-production systems, the RCON switches will be used to determine the device booting configuration. The RCON pins together with the BOOTMOD pins control the booting behavior of the devices. The BOOTMOD pins are configured with a very weak internal pulldown resistor during powerup and reset stages. These internal pull resistors should not be depended on to achieve the desired state during lathing. Designers must use external pull resistors with a value no greater than 10kΩ to set the desired state.

6. PCB stack up recommendation

High-speed design requires a good stack up in order have the right impedance for the critical traces. The constraints for the trace width may depend on a number of factors, such as the board stack up and associated dielectric and copper thickness, required impedance, and required current (for power traces). The NXP S32V234-EVB2 reference design uses a minimum trace width of 3 mils for the DDR routing. The stack up also determines the constraints for routing and spacing.
Consider the following when designing the stack up and selecting the material for your board.

- Board stack-up is critical for high-speed signal quality.
- You must pre-plan impedance of critical traces.
- High-speed signals must have reference planes on adjacent layers to minimize cross-talk.
- NXP reference design uses Megtron 6.

The recommended stack up is 8-layers, with the layer stack as shown in the following figure.

Layer	Calc Thickness	Primary Stack	Description
	0.0005		Taiyo 4000-BN
Layer - 1	0.0019		**3/8oz Sig (Std Plt)**
	0.0027		R-5670K
Layer - 2	0.0012		**1/2oz P/G (0.0006 Plt)**
	0.0037		R-5670K
Layer - 3	0.0019		**3/8oz Sig (Std Plt)**
	0.0075		R-5670K
Layer - 4	0.0012		**1oz P/G**
	0.0200		R-5775K
Layer - 5	0.0012		**1oz P/G**
	0.0075		R-5670K
Layer - 6	0.0019		**3/8oz Sig (Std Plt)**
	0.0037		R-5670K
Layer - 7	0.0012		**1/2oz P/G (0.0006 Plt)**
	0.0027		R-5670K
Layer - 8	0.0019		**3/8oz Sig (Std Plt)**
	0.0005		Taiyo 4000-BN

Materials: Panasonic R-5670K Megtron 6 prepreg
Panasonic R-5775K Megtron 6

EVB stack-up implementation

Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1 Surface MS	L1	0.00470	0.0045	-	-	50	5.0	49.21
	-	-	-	-	L2			
2 EC Microstrip	L1	-	0.0040	0.0140	-	100	10.0	97.73
	-	-	0.0040	-	L2			
3 Stripline	L3	0.0040	0.0040	-	L2	50	5.0	49.43
	-	-	-	-	L4			
4 EC Stripline	L3	0.00350	0.0037	0.0140	L2	100	10.0	98.05
	-	0.00350	0.0037	-	L4			
5 Stripline	L6	0.0040	0.0040	-	L5	50	5.0	49.43
	-	-	-	-	L7			
6 EC Stripline	L6	0.00350	0.0037	0.0140	L5	100	10.0	98.05
	-	0.00350	0.0037	-	L7			
7 Surface MS	L8	0.00470	0.0045	-	L7	50	5.0	49.21
	-	-	-	-	-			
8 EC Microstrip	L8	-	0.0040	0.0140	L7	100	10.0	97.74
	-	-	0.0040	-	-			

6.1. High-speed signal routing recommendations

The following list provides recommendations for routing traces for high speed signals. Note that the propagation delay and the impedance control should match in order to have the correct communication with the devices.

Apply the below good-practice rules to all high-speed signals:

- Route them with higher priority than low-speed signals.
- Control impedance of the traces.
- Do not cross-split reference planes during the routing.
- Avoid creating slots, voids, and splits in reference planes; verify that via voids do not create such splits (space-out vias).
- Avoid having layer transitions.
- If layer transition is inevitable:
    - Try staying within the same reference plane (just referenced to the opposite side thereof).
    - Make sure the trace impedance does not change after the layer transition.
    - Differential signals must transition in the same locations and the same way
- High-speed signals (DDR, RGMII, display) must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in reference planes. Review via voids to ensure they do not create splits (space out vias).
- A solid GND plane must be directly under crystal, associated components, and traces.
- Clocks or strobes that are on the same layer need at least 2.5× spacing from an adjacent trace (2.5× height from reference plane) to reduce cross-talk.
- All synchronous modules should have bus length matching and relative clock length control.
    - For SD module interfaces:
        - Match data and CMD trace lengths (length delta depends on bus rates)
        - CLK should be longer than the longest signal in the Data/CMD group (+5 mils)
    - Similar DDR rules must be followed for data, address and control as for SD module interfaces

7. DDR connection information

7.1. Resources for DDR signal routing recommendations

Use the following references for information about DDR signal routing recommendations:

- S32V234 Datasheet PCB routing Guidelines Section
- S32V234 Reference Manual Multi Mode DDR Controller (MMDC) Chapter
- S32V234-EVB Design Files
- Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces AN3940 (non S32V234 specific)

8. PCI Express interface recommendations

The S32V234 provides a ×1 PCIe lane. The PCIe module supports PCI Express Gen 2.0 interfaces at 5 Gb/s.
The S32V234 does not support extracting reference clock from RX data, the reference clock must be provided to the S32V234's PCIe physical interface either externally or internally.
As far as use cases, if S32V234 is configured as a PCIe Endpoint, in a common reference clock architecture, the external reference clock port is to be used. If S32V234 is to be used in a separate reference clock architecture, the internal clock source may be used. Using a separate reference clock architecture however is not recommended as it can make more difficult to comply with PCIe clocking specifications.

8.1. PCI Express general routing guidelines

Use the following recommendations for PCI Express general routing:

- The trace width and spacing of the lanes ×1 signals should be such that the differential impedance is 85 Ω ± 10%.
- The PCIE_REXT contacts should be connected to a 200 Ω 1% resistor to ground. The trace length between the pin and the resistor should be minimized. The resistor value is defined within the data sheet and should determine the exact resistor value.
- Route traces over continuous planes (power and ground). Avoid split planes, plane slots, or anti-etch.
- Maintain the parallelism (skew matched) between differential signals. These traces should be the same overall length.
- Keep signals with traces as short as possible.
- Route signals with a minimum number of corners. Use curved traces if it all possible.
- Maintain symmetry of differential pair routing.

8.2. PCI Express coupling lane

Based on our development design, we have the following coupling signal schema. Consult the PCI-SIG documentation for detailed information.

- DC-coupled Rx signals with 0 Ω resistors
- AC-coupled Tx signals with 0.1µF capacitors

8.3. Additional resources for PCI Express signal routing recommendations

For more information about, PCI Express signal routing recommendations, see the following.
NXP Hardware Design Considerations for PCI Express® and SGMII

- PCI-SIG, PCI Express Base Specification.
- PCI-SIG, PCI Express Card Electromechanical Specification.
- PCI-SIG, PCSIG Board Design Guidelines for PCI Express™ Architecture.
- PCI Express Basics: Developing Physical Design Rules for PCIe

9. MIPI-CSI2 PCB considerations

9.1. PCB considerations:

- High speed traces should not be routed across pinfield of connectors.
- Vias on the PCB should be engineered for proper impedance as required by the application.
- Avoid Via stubs by using back drill methods or proper layout planning.
- Blind/buried vias can also be used as appropriate, provided that the via is engineered to appear as a matched Zo in series with the trace.
- Vias should have a 50 Ohm controlled impedance
- Ensure the vias are symmetrical between the differential signals
- Ensure multiple return path ground vias (preferably 4 vias) next to the signal path vias
- The reference planes on the board should be designed to have as low impedance as possible.
- The board designer should give due consideration to the electrical performance issues such as dI/dt and IR drops.
- Cross talk has to be minimized across all tracks.
- Ensure that no tracks run parallel to the differential pairs to minimize crosstalk.
- Minimize skew between the complimentary traces of the differential pair and equalize wire length and transmission line properties. If via's and other discontinuities are un-avoidable, ensure that they are symmetrical.
- Differential pairs may be routed on the same plane provided that crosstalk is minimized among neighboring pairs as shown in Figure 5.
- Differential pairs should always be routed together and kept as close as possible to each other. Additionally, the length of the differential traces should be kept equal
- Avoid tracks jumping reference planes.
- Minimize parasitic cap on REXT pad as much as possible (only with optional calibrator).
- It is important to deliver an analog-grade power supply to the IP. Typically, an L-C filter is used, with the "C" being composed of multiple devices to achieve a wide spectrum of noise absorption. Although the circuit is simple, there are specific board layout requirements. To achieve good low-frequency cut off there should be a large capacitor (>5uF) in the filter design. As the filter also needs to sustain its attenuation into moderately high frequencies, so there will additionally be at least one capacitor in parallel. The routes from the high frequency capacitor(s) to the chip must be kept short and the capacitor must preferably be placed right underneath the chip on the reverse side of the board. Cursory analysis suggests that a third, very high frequency, capacitor should help reduce noise.

- Board layout around the high-frequency capacitor and the path from there to the pads is critical. It is vital that the quiet ground and power are treated like analog signals.
- The power (VDDx) path must be a single wire from the IC package pin to the high frequency cap, then to the low frequency cap, and then through the series element (e.g. ferrite bead) then to board power (VDD board). The distance from the IC pin to the high frequency cap should be as short as possible.
- The ground path should be treated similar to the power path. The power and ground traces should be short, and run close and parallel as far as is possible, with large spacing's to adjacent traces.

10. Unused peripherals

Always appropriately connected to the power rails and decoupling networks as recommended.
The following table provides recommendation for unused peripherals.

IP name	Connection of the input/output pads when IP is not used.
PCIe	The REXT should be connected to GND via a 200 Ω resistor and the HS pins allowed to float.
MIPI	ZQ and High Speed serial signals can be left floating.
LFAST	Leave pads as NC (with output buffer disabled, input buffer disabled, internal termination disabled).
GPIO	Leave pads as NC (weak pull down enabled with output buffer disabled, input buffer disabled).
DDR	Leave pads as NC (with output buffer disabled, input buffer disabled). Properly connect ZQ and VREF per specification.

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