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Revision History

PROTO REV1	30.05.06
PROTO REV2 Flash address correction	14.09.06

MWI: 081-8360EPSYS-5
PCB: 084-00XXX-1

LEGEND :

On-page signal connection
 Off-page signal connections
 Signal has pull-up
 Signal has pull-down
 FPGA pins termination

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Title

MPC8360EA_MDS_PB

Size
A

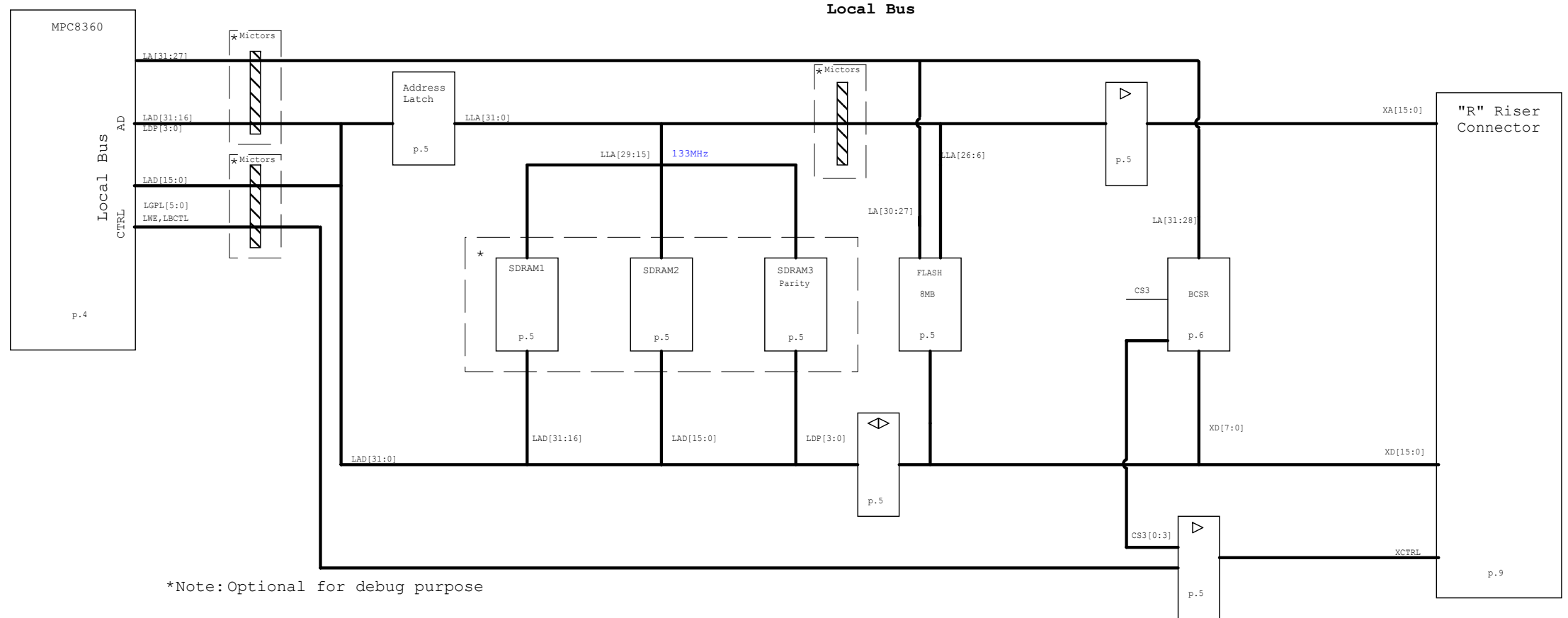
Document Number

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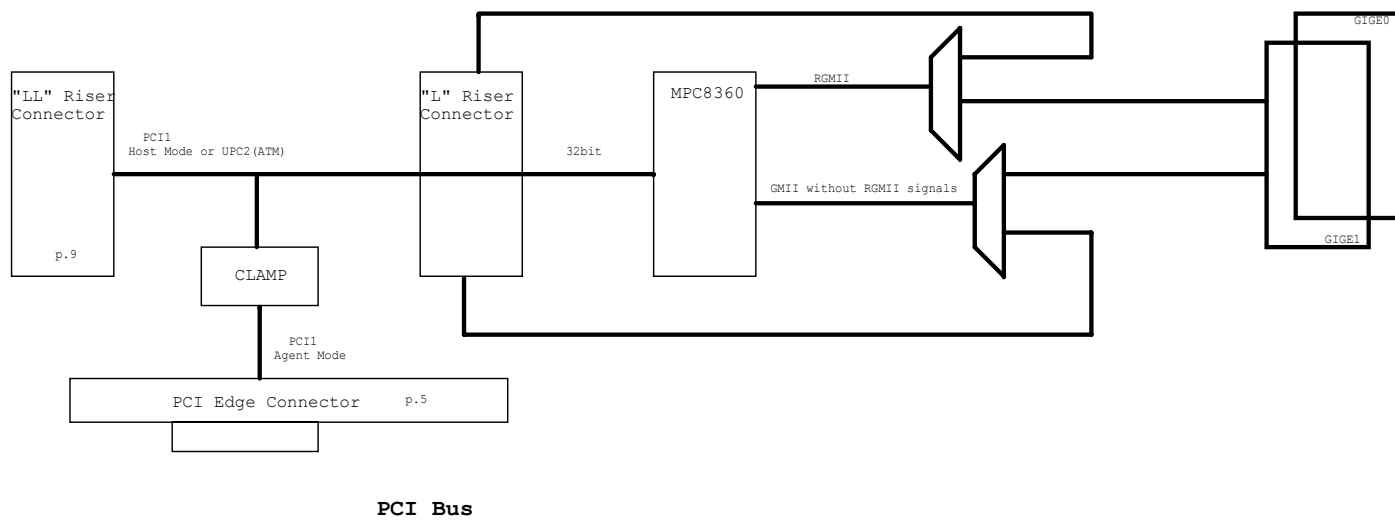
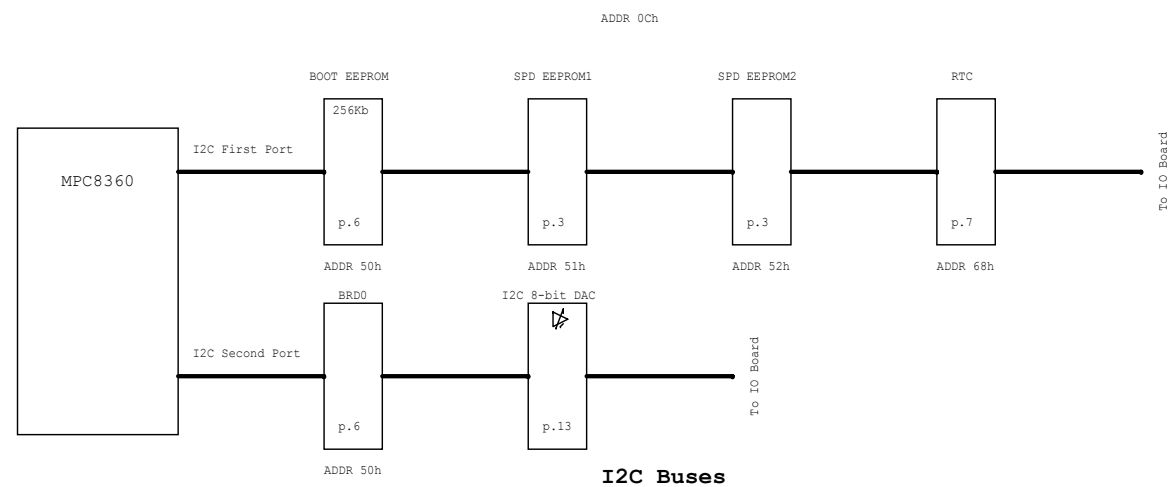
Rev
PROTO2

Date: Thursday, September 14, 2006

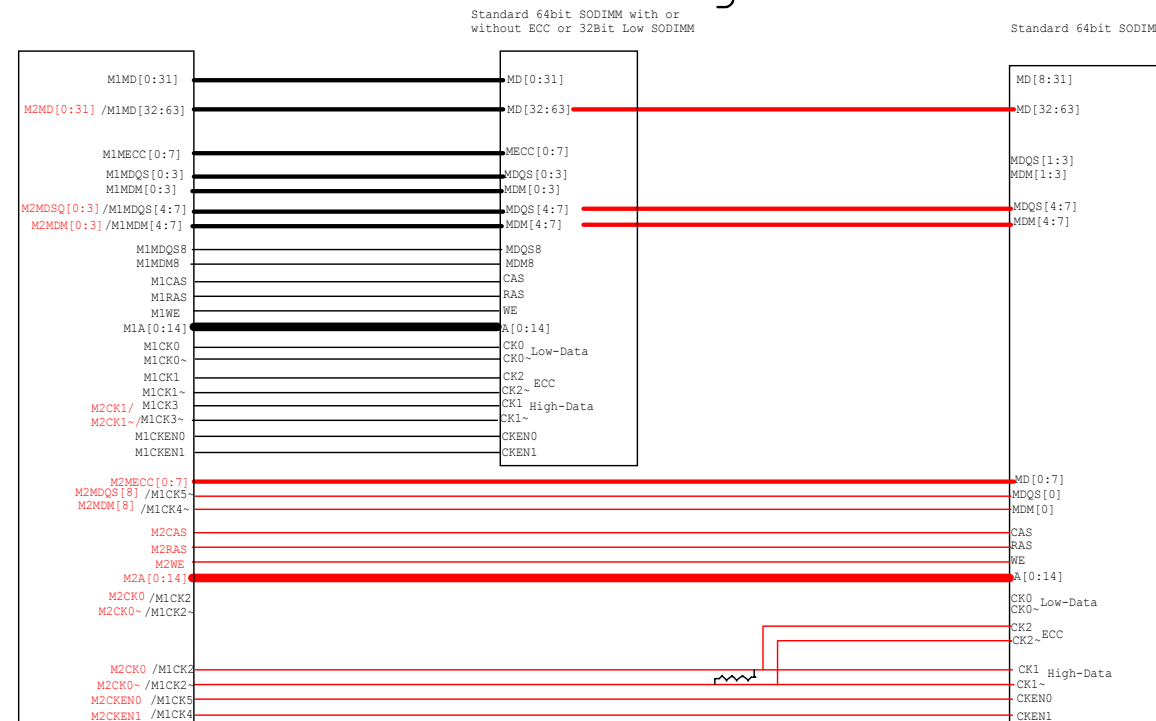
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*Note: Optional for debug purpose



DDR Block Diagram





5

4

3

2

1

D

D

C

C

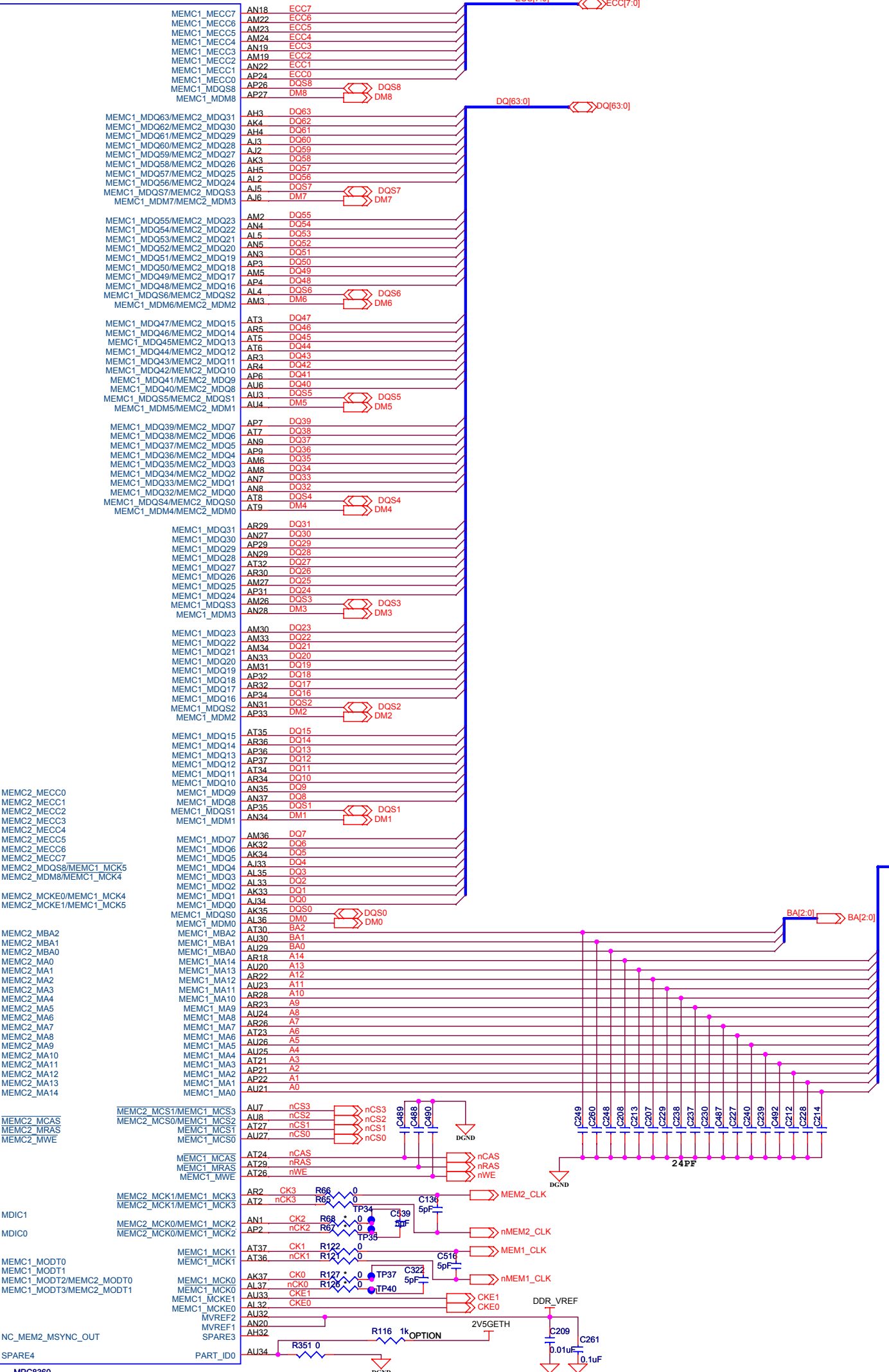
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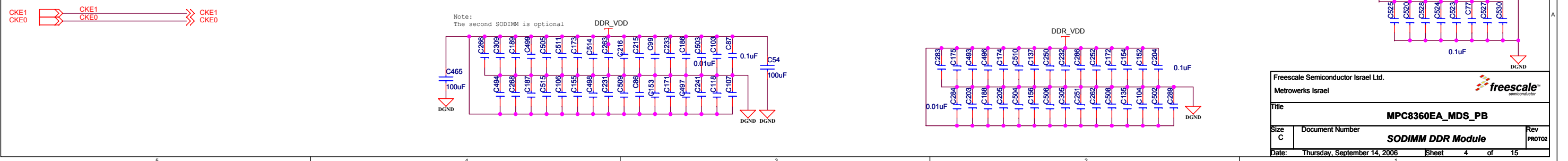
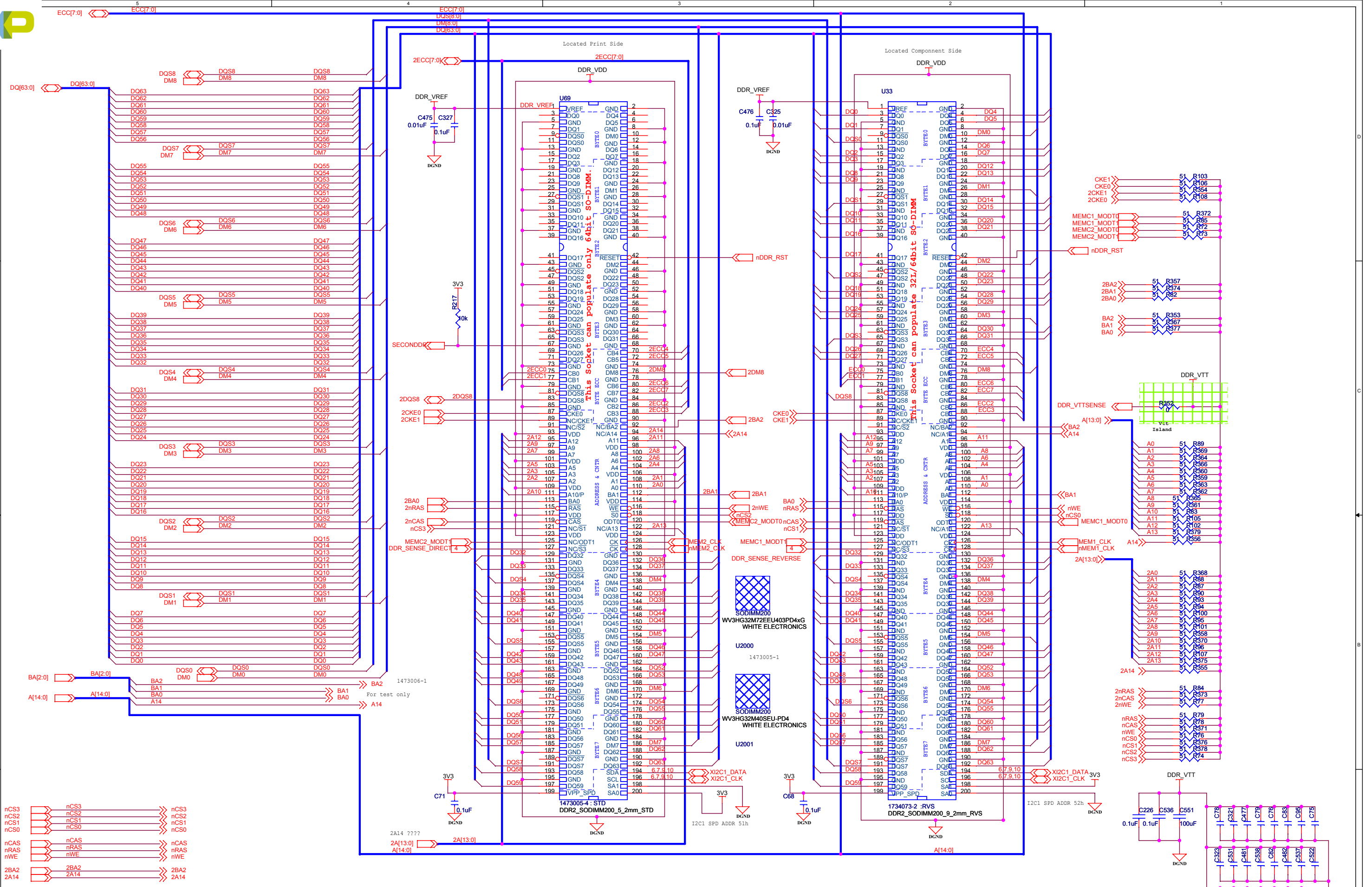
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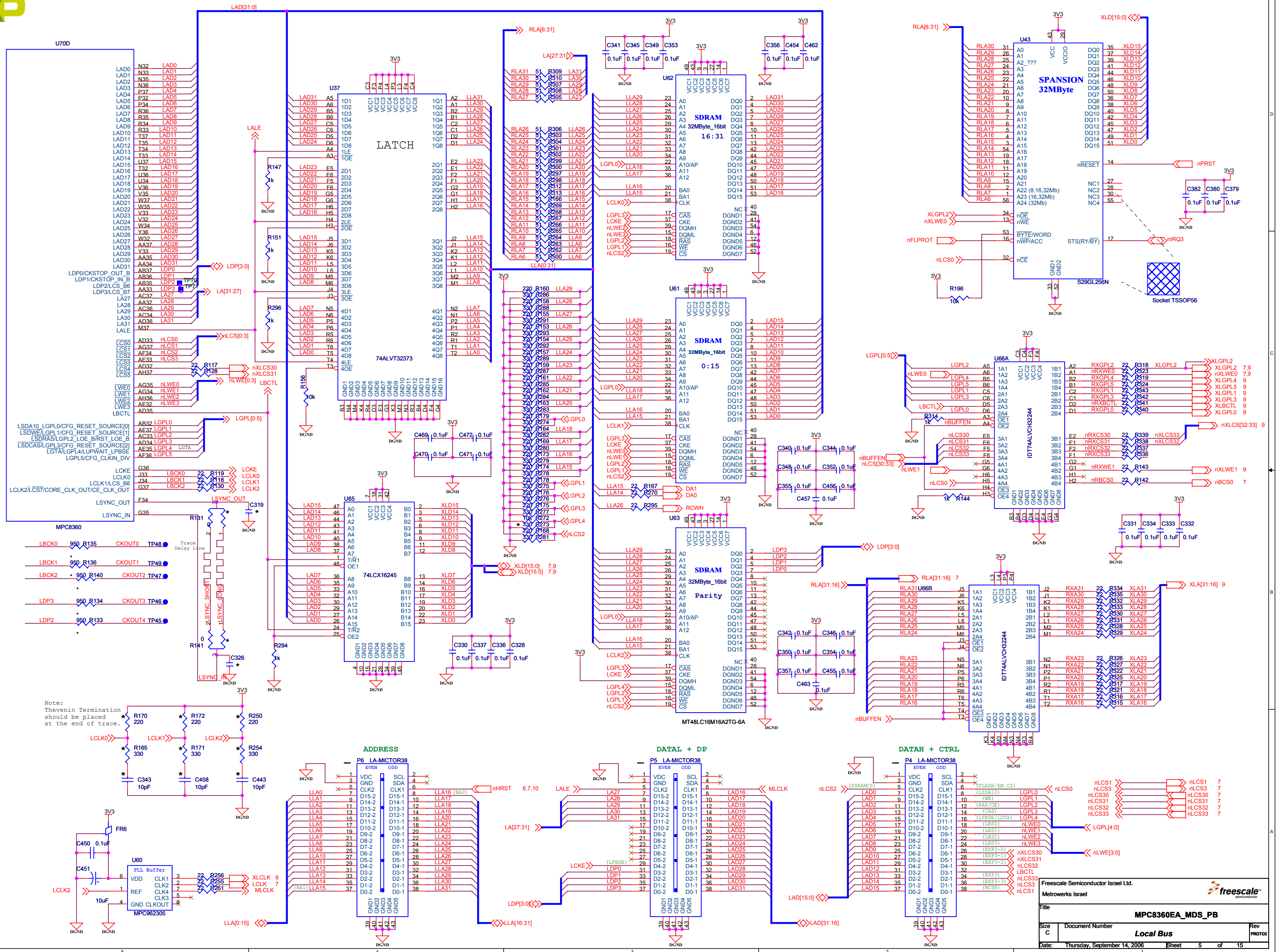
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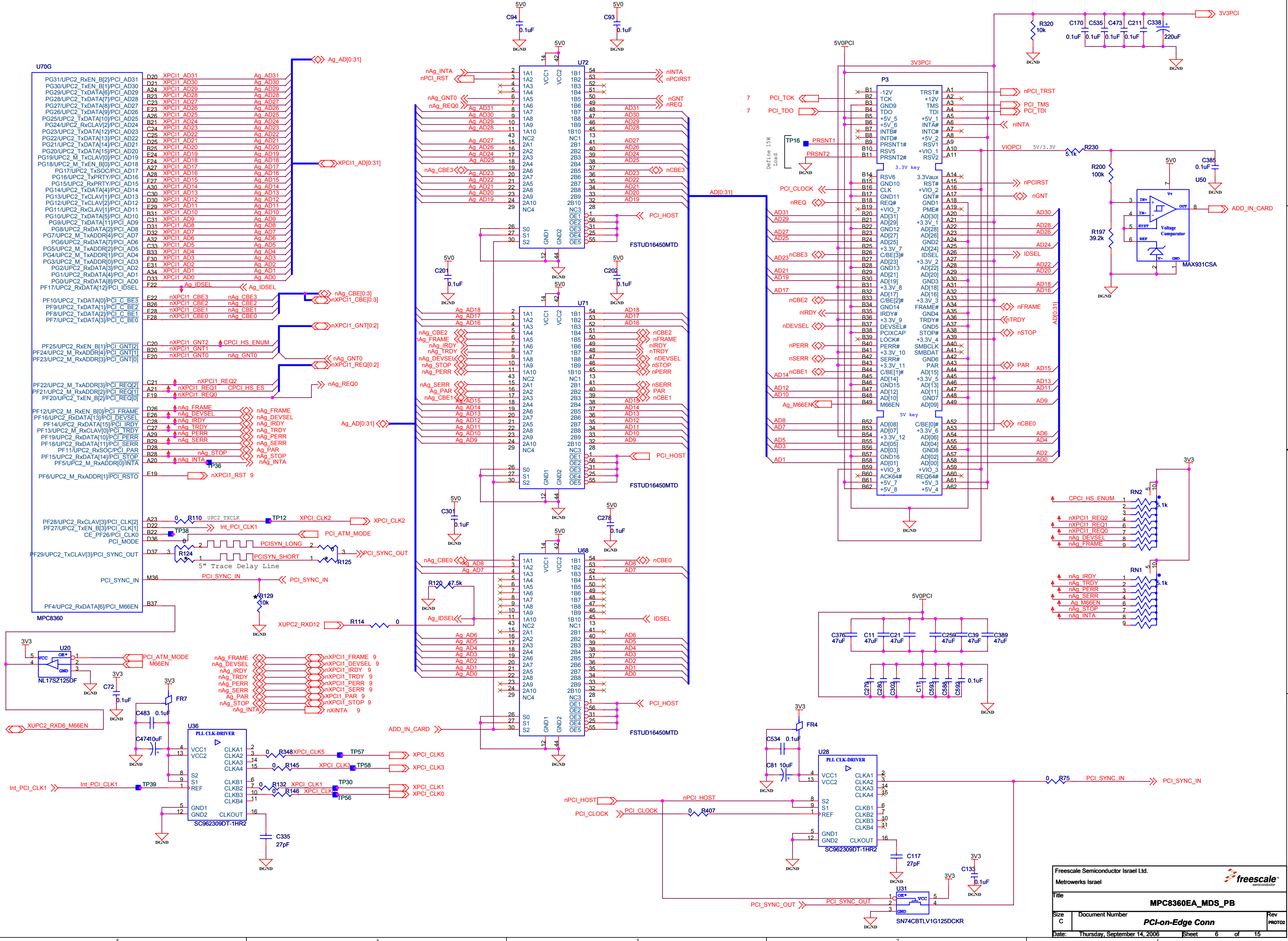
Note:
Thevenin Termination
should be placed
at the end of trace.

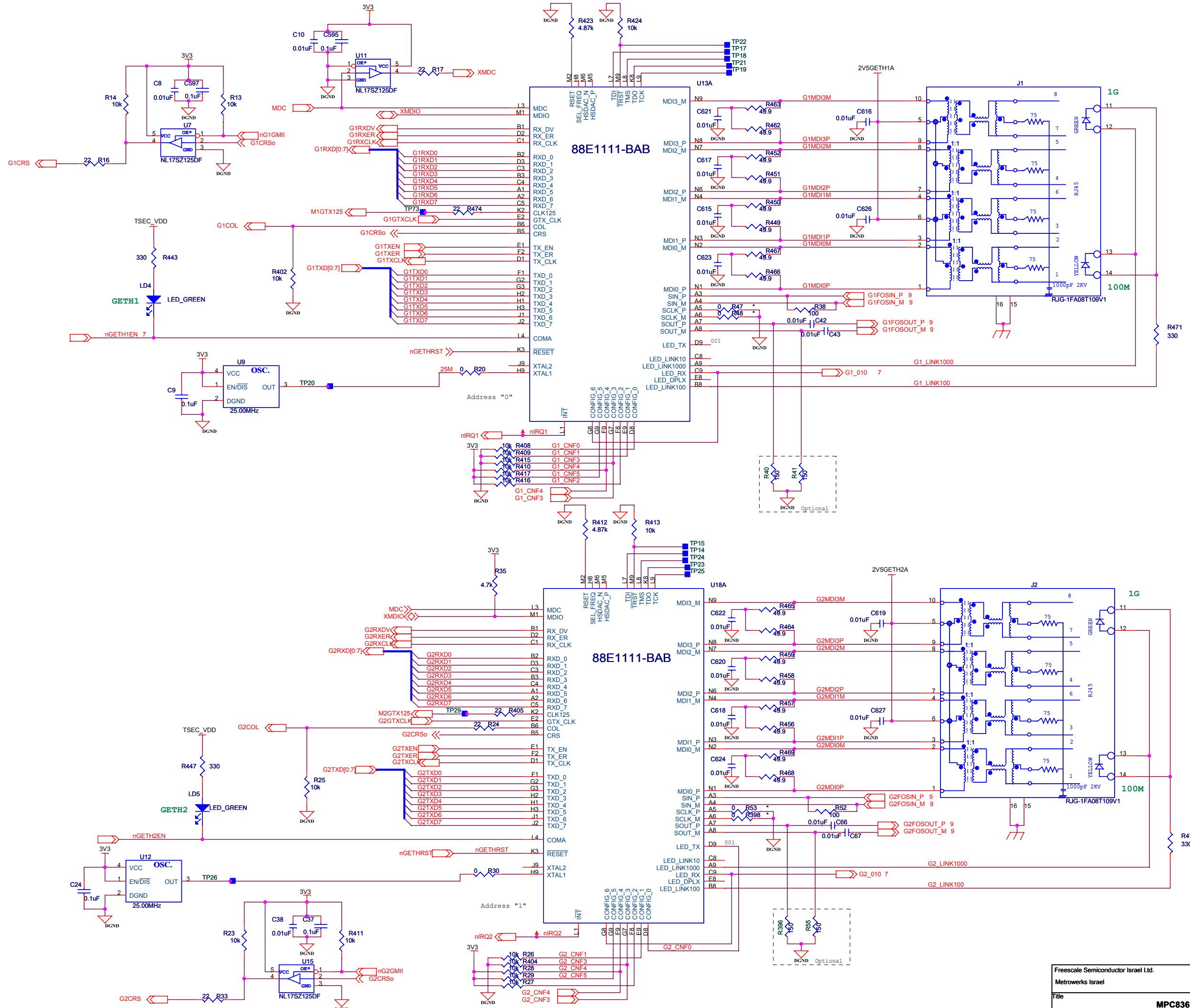
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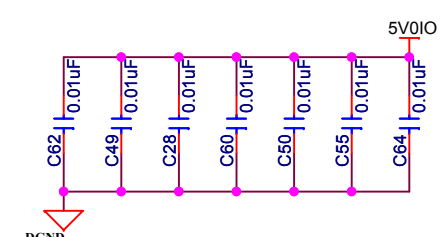
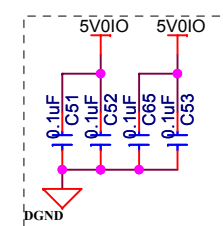
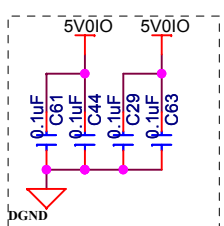
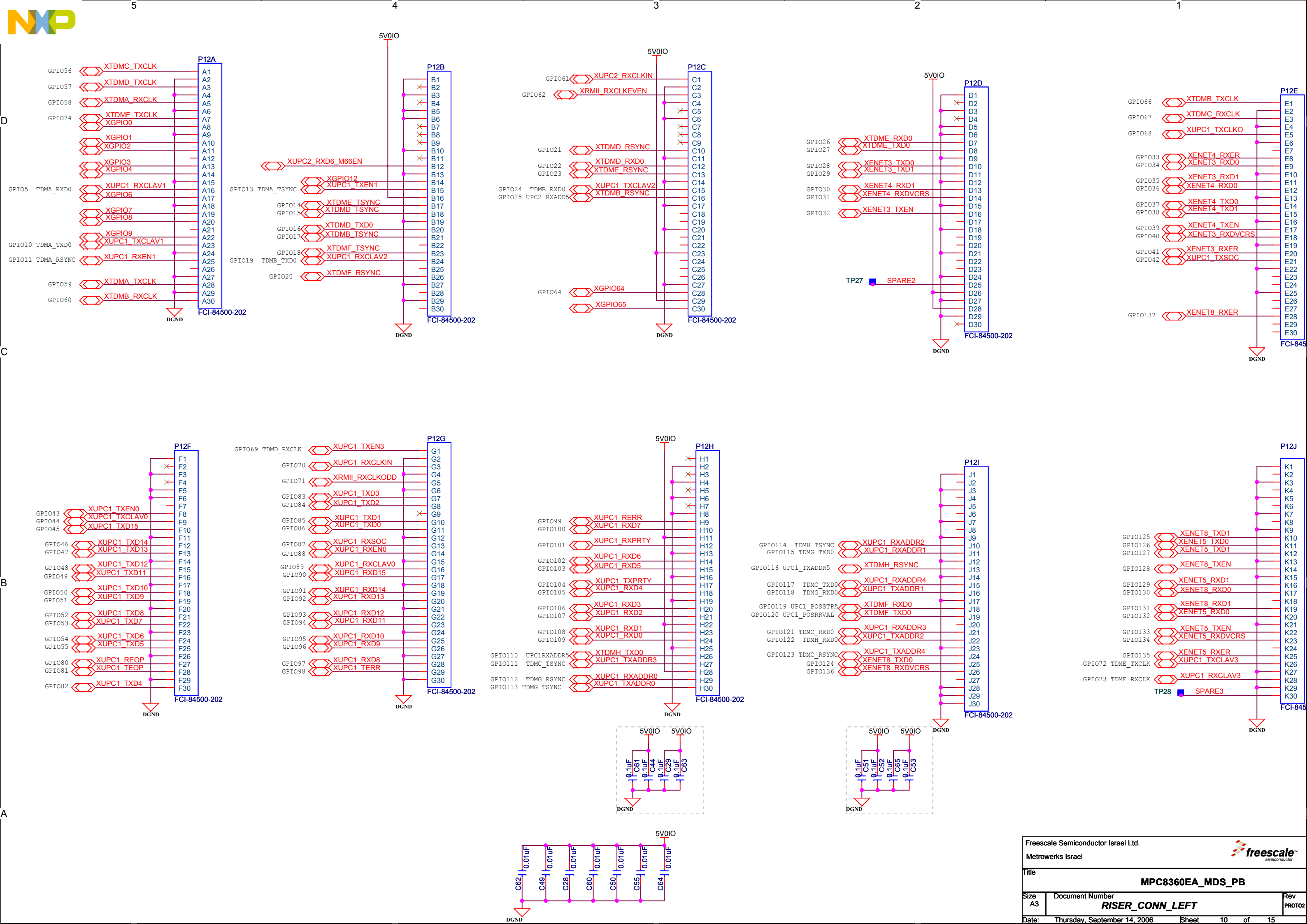
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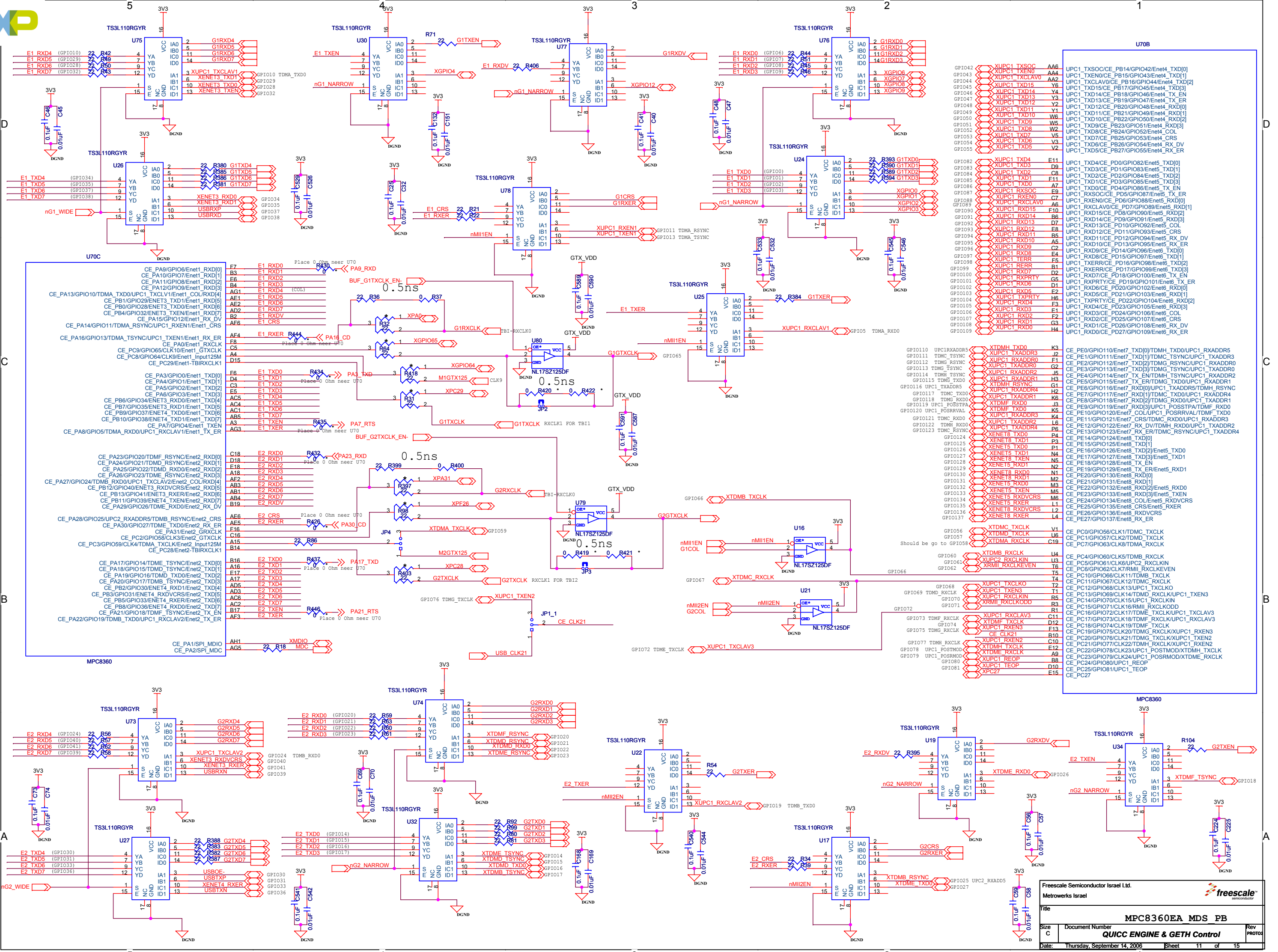
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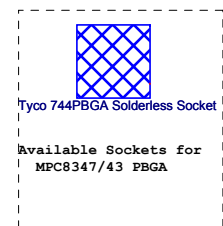
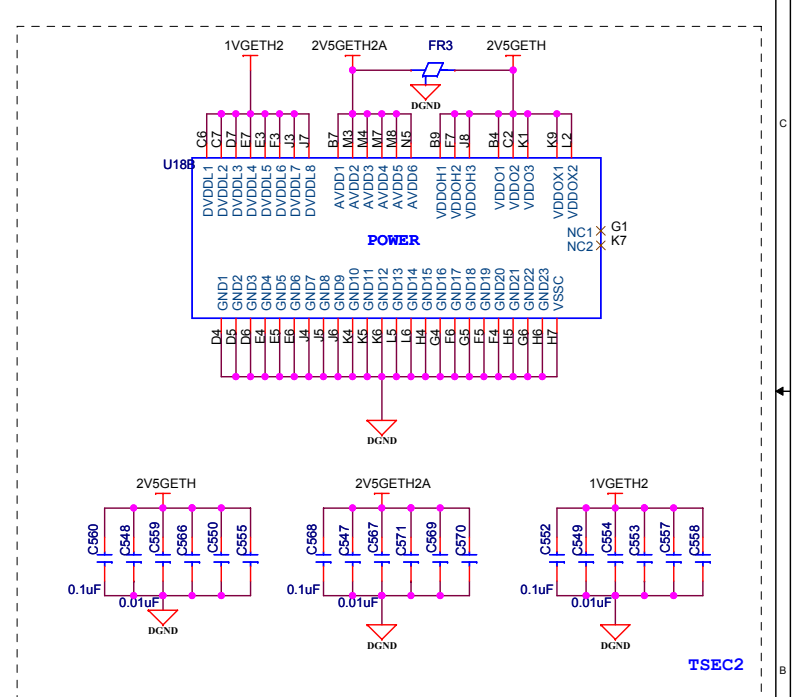
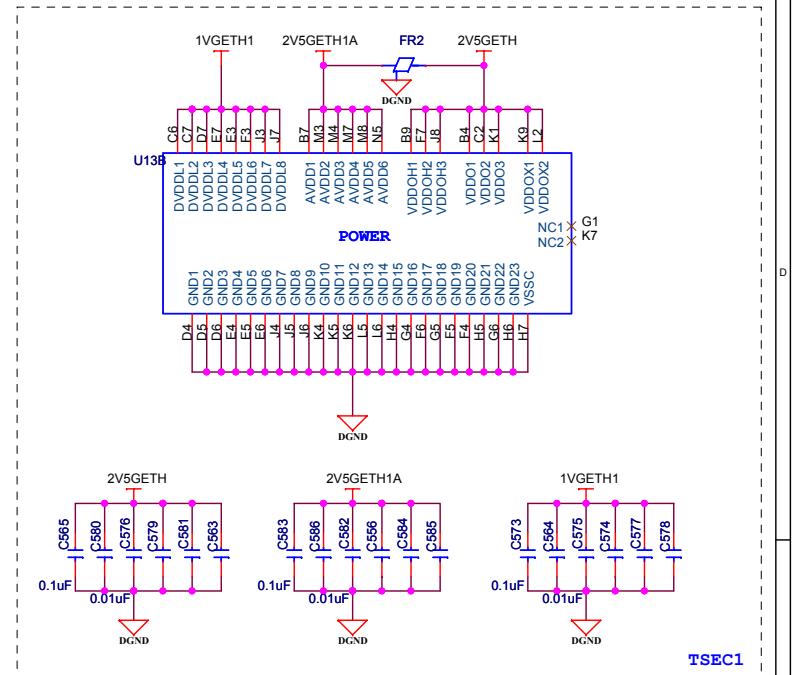
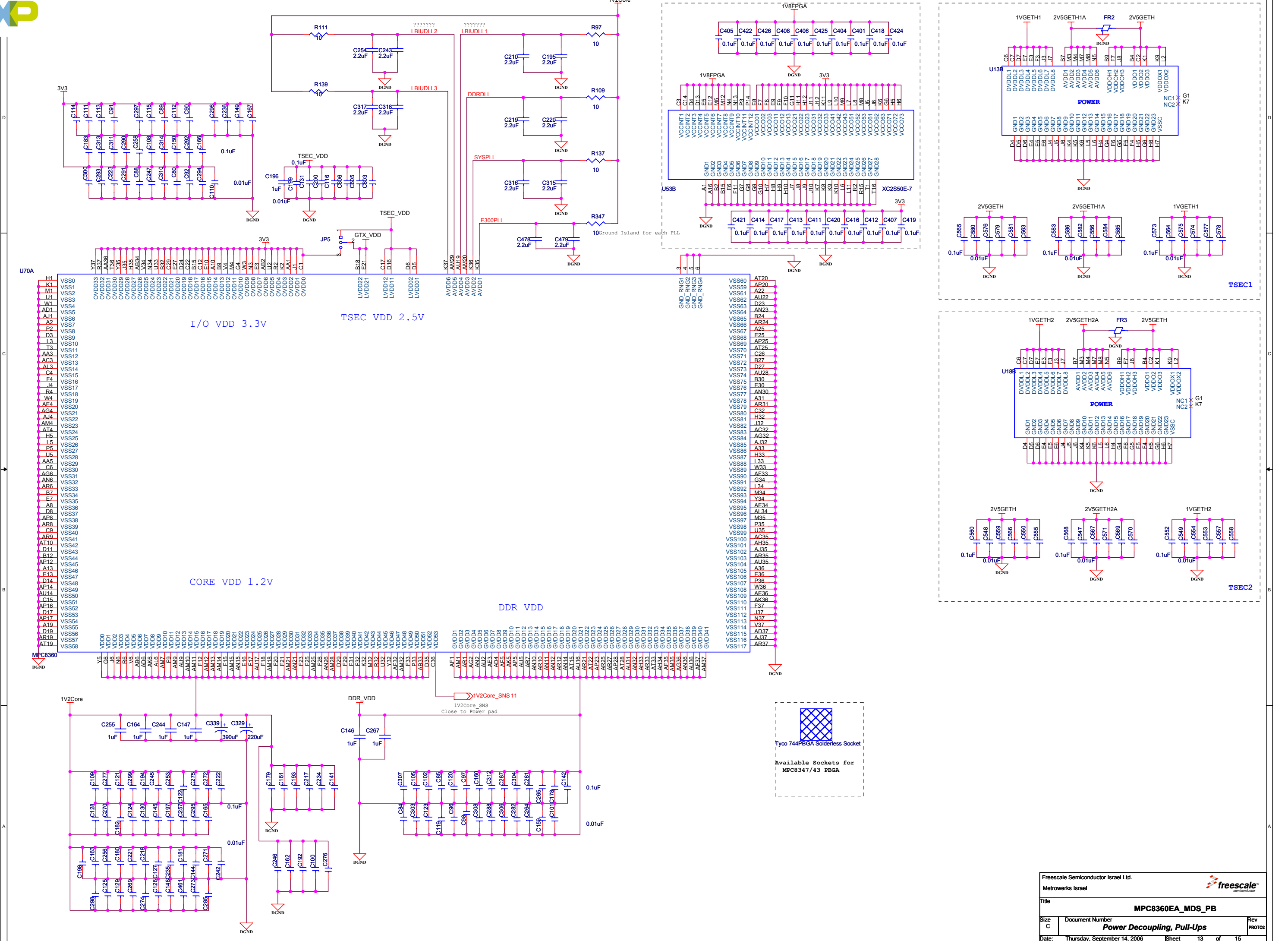
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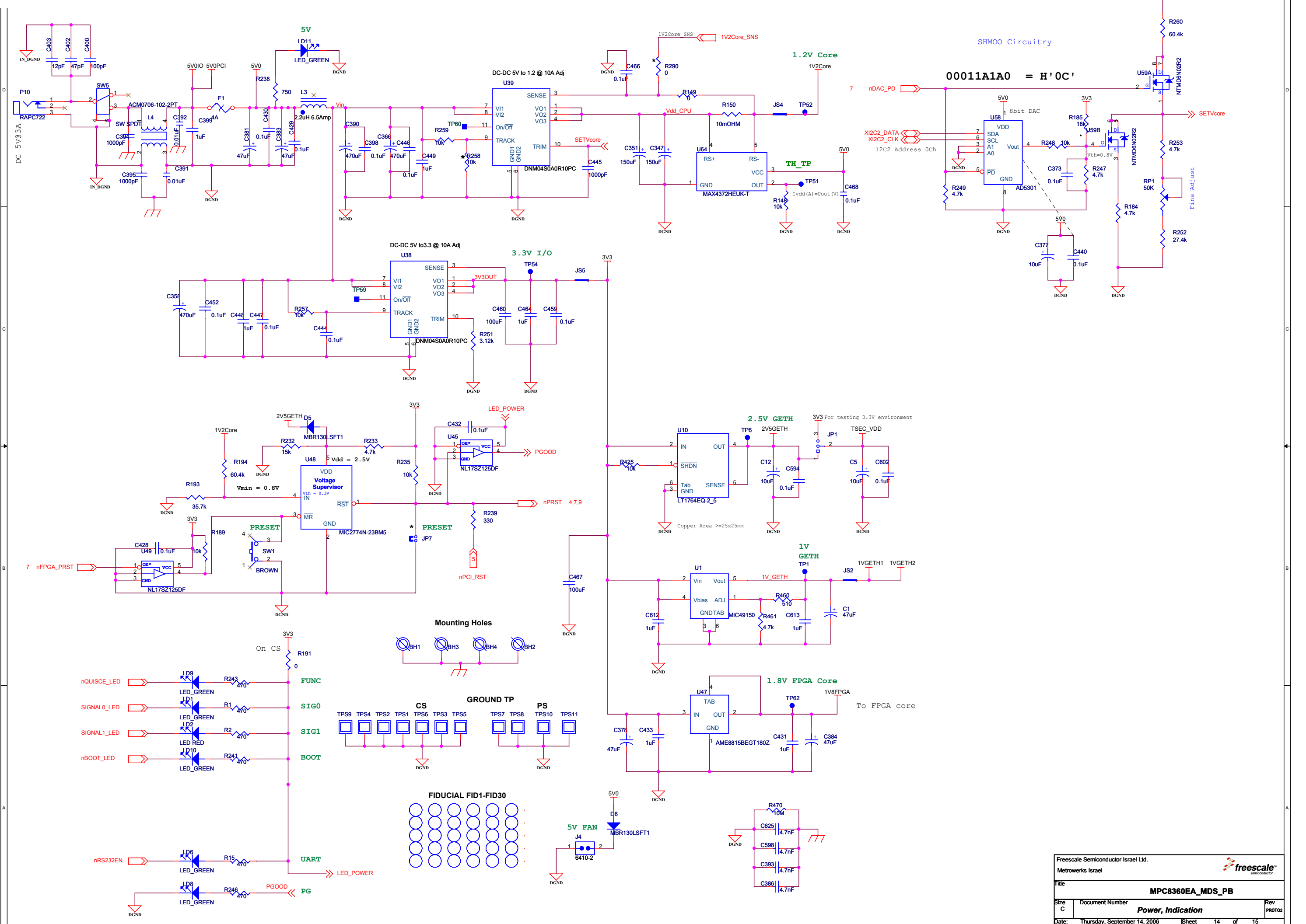












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