High Voltage Solar Inverter DC-AC Kit

User's Guide

Literature Number: TIDU402
September 2014

High Voltage Solar Inverter DC-AC Kit

1 Introduction

Inverters, especially solar inverters, have gained more attention in recent years. Solar inverters produce solar energy input, then feed that solar energy to the grid. So the grid-tie technology and some of the protection are key points when designing a solar inverter system.

This document describes the implementation of the inverter kit that used as a DC-AC part of the High Voltage Solar Inverter DC-AC Kit. The kit has a nominal input of 400-V DC, and its output is 600 W, which can be fed to the grid.

Many fields use this inverter, such as motor control, UPS, and solar inverter systems. The main function of the inverter is to convert the DC power to AC power by using the power electronics like the IGBT and MOSFET. Traditionally, many inverter systems will be implemented by the analog components. As the development of the digital processors, more and more low cost and high performance micro-controllers had got into the market. At the same time, more and more inverter systems trends to use the micro-controllers to implement the digital controller which can not only simplify the system structure but also improve the output performance of the inverters.

Among the various inverter systems, there are two different types. The first type is the voltage output type, which outputs AC voltage as a voltage source. For example, the inverter in the UPS system is a typical voltage-type inverter. The other type is the current type, which outputs AC current in a specified power factor. The motor control inverter and the solar inverter are the current type inverters for this design. This document will mainly discuss the current type inverters for the solar system.

Many different topologies for inverters have come out recently. This design uses a full-bridge topology including four IGBTs as a reference design, which is easy to get started and transplant to the real product.

1.1 Basic Principles

The topology for a full-bridge current-type inverter is shown in Figure 1.

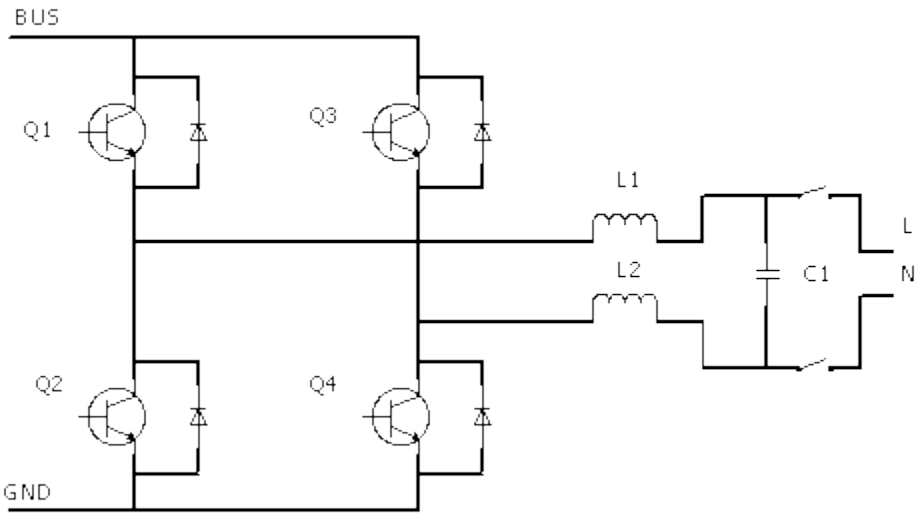

Figure 1. Topology of Full-Bridge Current-Type Inverter

To have an AC ouput, the full-bridge topology uses a sinusoid pulse width modulation (SPWM) control strategy. These strategies can be divided to the following two categories:

- Single polar modulation
- Dual polar modulation

1.1.1 Single Polar Modulation Theory

Single polar means the voltage in the AC side of the inverter has only positive or only negative voltage. An example of the single polar modulation is shown in Figure 2.

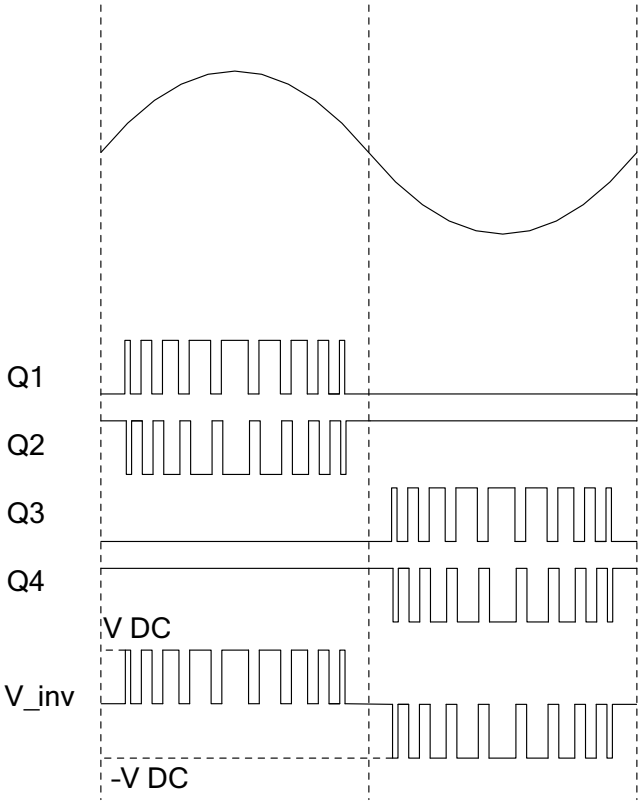

Figure 2. Single Polar Modulation Theory

In Figure 2, when in the positive cycle of the sine wave, the output voltage of the inverter is changing from the Vdc to 0, while the negative cycle is the –Vdc to 0. In the positive cycle, if the duty of Q1 is d, then the cycles relate between the output voltage V_o and the DC BUS voltage V_{bus}:

$$V_o = dV_{bus} \quad (1)$$

1.1.2 Dual Polar Modulation

1.1.3 Controller Loop

For the current type inverter, the output current will be controlled. A majority of solar inverter systems have a DC-DC part in front of the DC-AC part, which is used to boost up the panel voltage and execute the MPPT. The DC-DC will not control the DC BUS voltage but will control the input panel voltage and work in the power output mode. So, the DC-AC part (inverter) is responsible for controlling the DC BUS voltage.

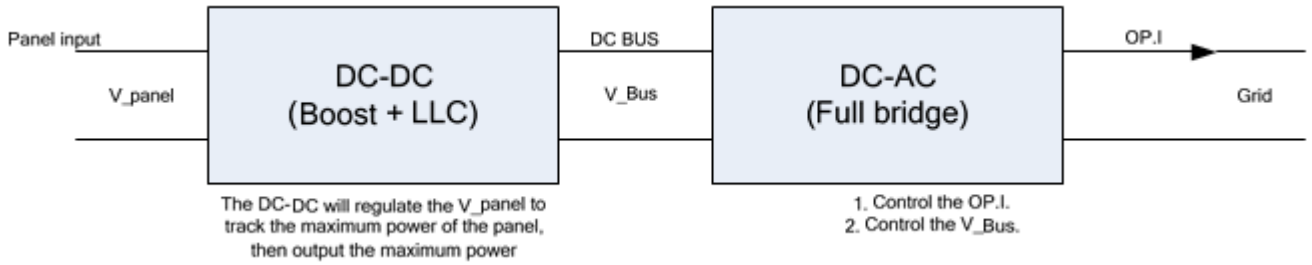

Figure 3. Typical Solar Inverter Structure

The DC BUS works as a link between the DC-DC and DC-AC part. When the DC BUS voltage rises, the DC-AC increases its output current to keep the DC BUS in a specified value, which increases the output power of the system. When the DC BUS voltage starts to fall, the DC-AC decreases its output current to prevent the DC BUS from falling down, which decreases the output power.

The typical controller structure for the inverter part is shown in Figure 4:

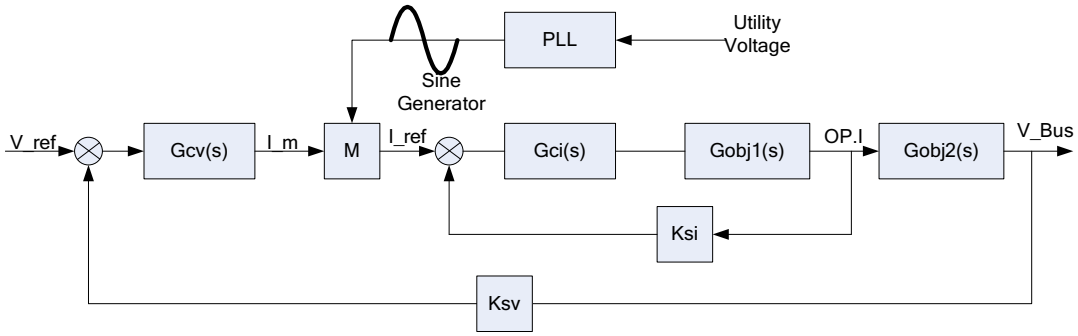

Figure 4. Controller Loop of the Inverter Part in Solar System

The double-loop control system is used in Figure 4. The internal loop is the output current loop; it will trace the I_ref, which is the product of the I_m and Sine. The external loop is the DC BUS voltage loop; it will keep the BUS voltage to V_ref. The PLL ensures the grid voltage and the output current synchronize.

NOTE: When the DC-DC part and DC-source in CV mode do not connect, disable the external loop.

2 Design Introduction

2.1 Hardware

2.1.1 Key Components

The kit uses the following key components, as shown in Figure 5: four pieces of 600-V IGBT drivers, designed to the module type; two pieces of 2.5-mH inductors; two pieces of relay to control the grid-tie connection; and the Hall current sensor to sense the inductor current.

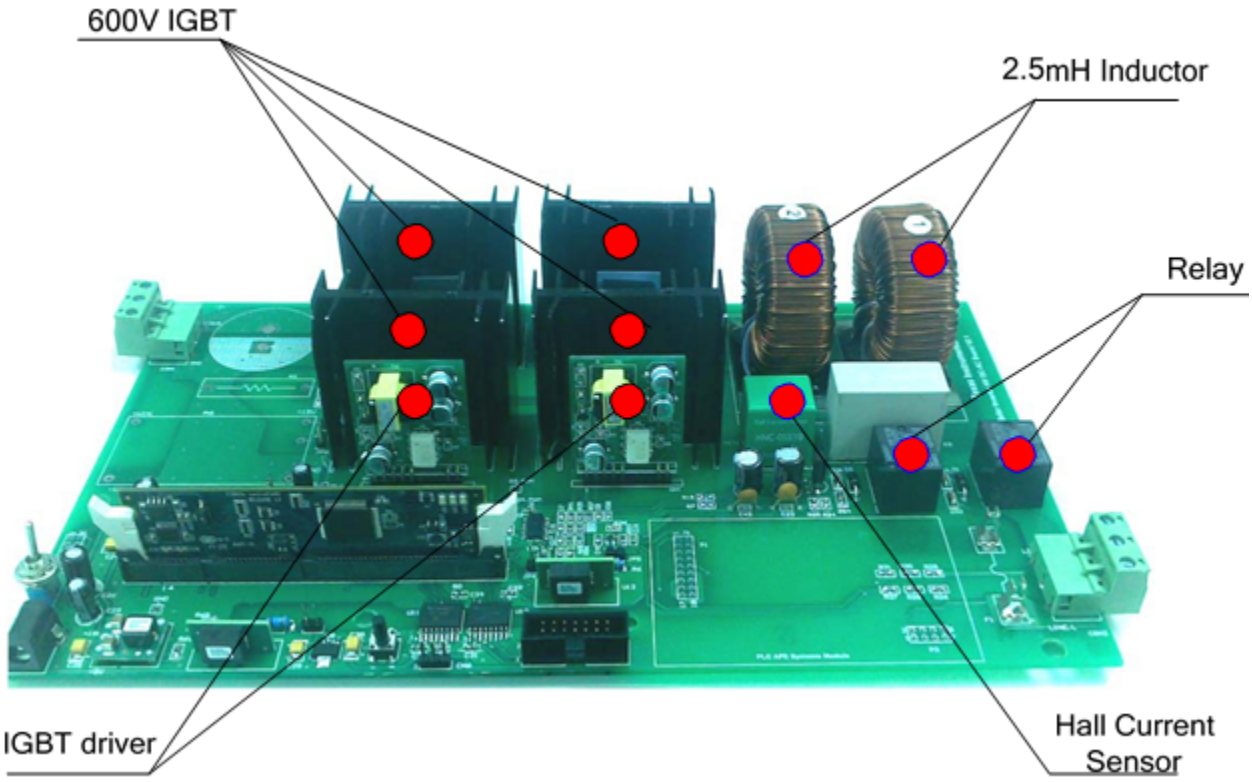

Figure 5. Key Components on the Board

Figure 6 and Table 1 explain the PCB placements:

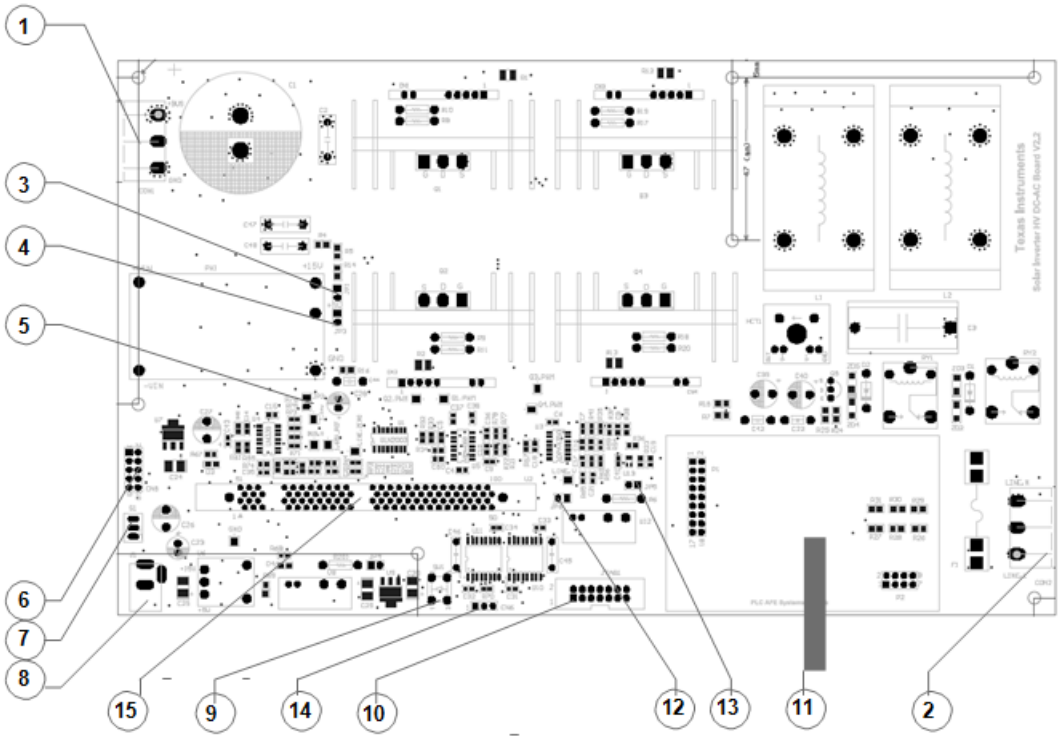

Figure 6. PCB Placement

Table 1. Key Points

ITEM NUMBER	POINTS NAME	COMMENT
1	CON1	The DC bus connector for the DC-DC input.
2	CON2	The Utility connector L and N.
3	JP1	Onboard 15-V jumper
4	JP3	Onboard 5-V jumper
5	JP2	IGBT driver 15-V jumper
6	CN5	DC-DC board signal interface
7	S1	External 15-V adapter switch
8	J1	External 15-V input jack
9	SW1	Operation button
10	JTAG1	JTAG interface for external emulator
11	PLC AFE Systems Module	Not used in this version
12	JP6	TRST jumper
13	JP5	–15-V power jumper
14	CN6	RS-232 port
15	U2	DIM100 28035 control card port

2.1.2 Auxiliary Power Supply

The auxiliary power of the kit can be available in two ways. One way is using the external 15-V adapter. Insert the adapter to J1, then switch S1 to power on. The other way is using the power module on board. See the preliminary jump configuration in Table 2:

Table 2. The Jumper Setting for the board

JUMPER	EXTERNAL 15-V ADAPTER	ONBOARD 15-V
JP1	×	√
JP2	√	√
JP3	×	×
JP6	Unaffected	×

2.1.3 Signal Sensing

Three key signals are used in the controller loop:

- The DC BUS voltage
- The inductor current
- The grid voltage

The DC BUS voltage sensing is very simple. From the circuit, the sample ratio of the signal can be calculated as the following:

$$K_{ratio\_DCBUS} = \frac{R_6}{R_4 + R_5 + R_{14} + R_6} = \frac{10}{3010} = 0.003322 \quad (2)$$

For the inductor current sensing, there is a hall sensor whose sample ratio is 4/5. The differential circuit is used to get a appropriate ratio. The current sample ratio of the current is calculated here:

$$K_{ratio\_current} = K_{hall} \frac{R41}{R35 + R15} = 0.15974 \quad (3)$$

For the utility voltage, only the differential circuit is used. The current is calculated here:

$$K_{ratio\_grid\_voltage} = \frac{R_{59}}{R_{26} + R_{27} + R_{28} + R_{54}} = 0.003311 \quad (4)$$

NOTE: The sample circuit has a 1.65-V offset for the inductor current and grid voltage. Subtract this offset in the firmware.

2.1.4 Zero Crossing Detection

The zero crossing detection is used to detect the frequency and is very convenient to detect the islanding conditions. The kit uses a comparator to get a falling edge in every positive zero crossing. Besides, a positive feedback from the comparator is used to get a sharp edge. **See the schematic for the detail information.**

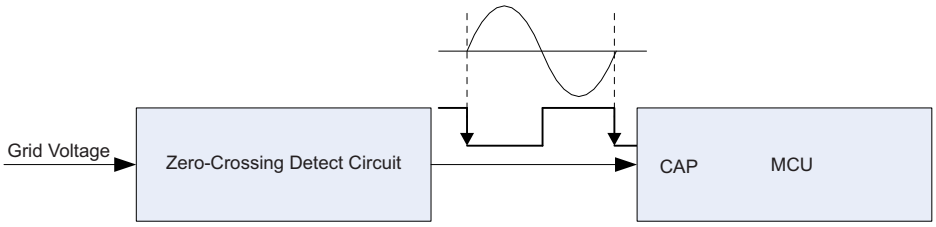

Figure 7. Zero Crossing

The CAP of the MCU captures the falling edge of the input signal and saves the capture value, which represents the positive zero crossing time of the grid voltage. The firmware design has an interrupt for the capture event. The frequency can be calculated by the following method:

$$f_{grid\_freq} = \frac{f_{cpu\_clk}}{(CAP_0 - CAP_1)} \quad (5)$$

where

- f_{grid_freq} is the grid frequency
- f_{cpu_clk} is the MCU CPU clock
- CAP_0 is the capture value this time
- CAP_1 is the capture value saved last time

2.1.5 IGBT Driver

The kit has four IGBT driver modules, which isolate and amplify the driving capacity. Figure 8 shows the functional diagram for the driver:

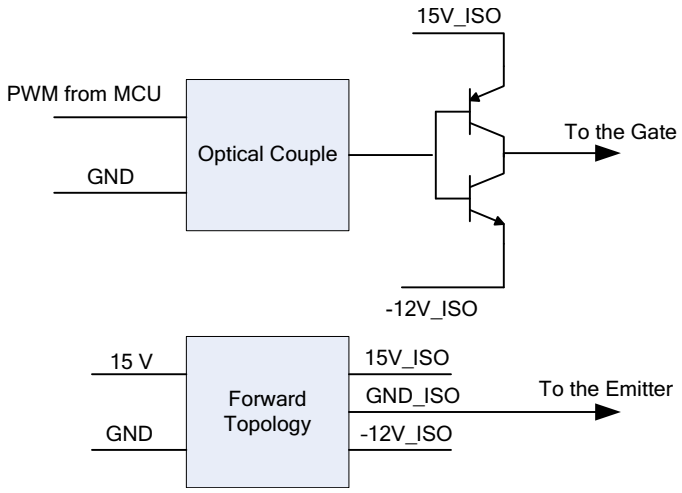

Figure 8. IGBT Driver Diagram

The driver can output 15 V for the turning on status and –12 V for the turning off status.

2.1.6 Inductance

An inductor in the main circuit smooths the current ripple. The inductance is determined by the switching frequency f_s, the DC BUS voltage V_{bus}, and the requirement of current ripple ΔI. In a certain switching period, the inductor current can be described as:

$$L\frac{\Delta I}{\Delta T} = V_L \quad (6)$$

where

- L is the inductance

If, in the single switching period, the rise of the current ΔI_r is equal to the fall of the current ΔI_f, then calculate:

$$L\frac{\Delta I_r}{\Delta T} = L\frac{\Delta I}{dT_s} = V_{bus} - V_o \quad (7)$$

$$L\frac{\Delta I_f}{\Delta T_f} = L\frac{\Delta I}{(1-d)T_s} = -V_o \quad (8)$$

Link Equation 7, Equation 8, and **[missing equation?]** to get:

$$\Delta I = \frac{V_{bus}}{Lf_s}\left[-(d-0.5)^2 + 0.25\right] \quad (9)$$

From Equation 8, the maximum ΔI occurs at d = 0.5 , and the maximum value is:

$$\Delta I_{max} = \frac{V_{bus}}{4Lf_s} \quad (10)$$

Equation 10 can help calculate the inductance requirement of full bridge inverter with the single polar modulation.

2.2 Firmware

2.2.1 Firmware Structure

The Firmware design uses the typical front and background system. For the background, three different timer-based tasks are scheduled to deal with the non-urgent tasks. Three interrupt service routines are used as the front to deal with the urgent things, such as close loop controllers, capture events, and SCI receiving.

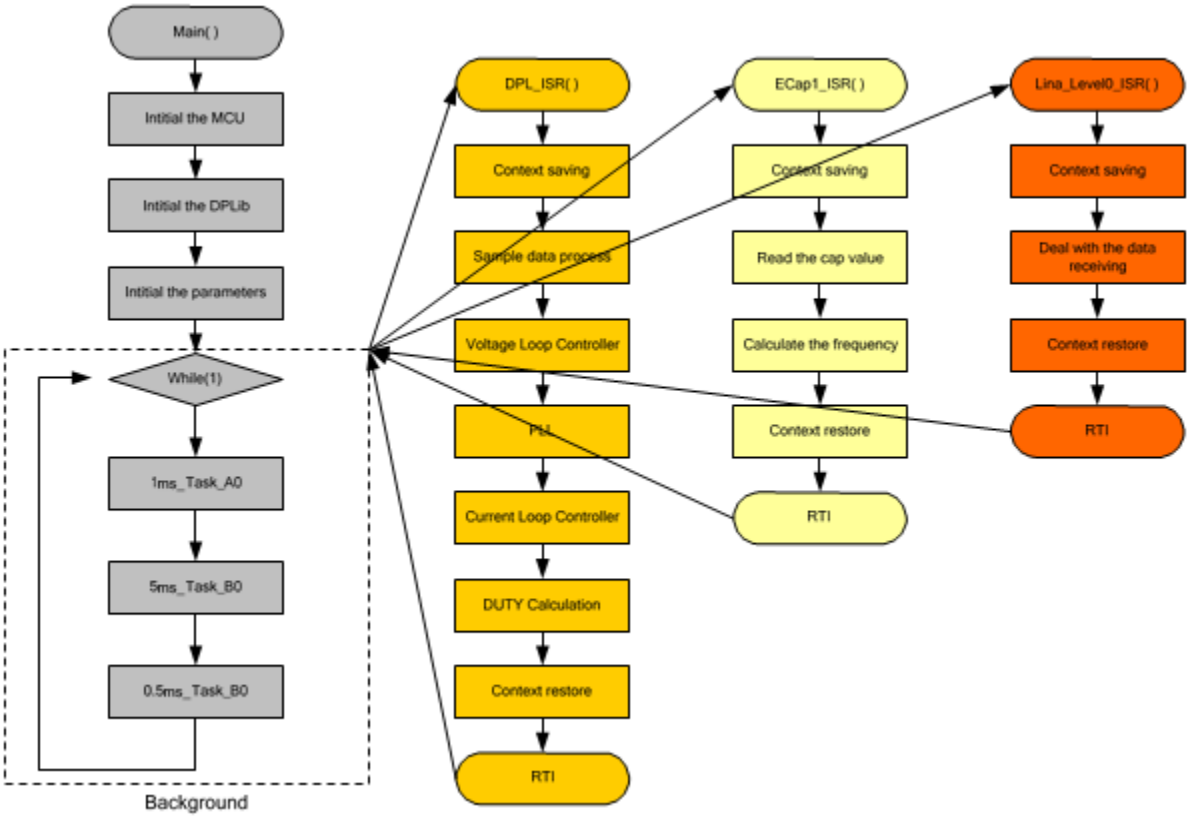

Figure 9. Firmware Structure

2.2.2 Status Machine

The status machine distinguishes the different statuses of the system. A different status represents a different running mode. According to the mode, the other tasks can take the appropriate action.

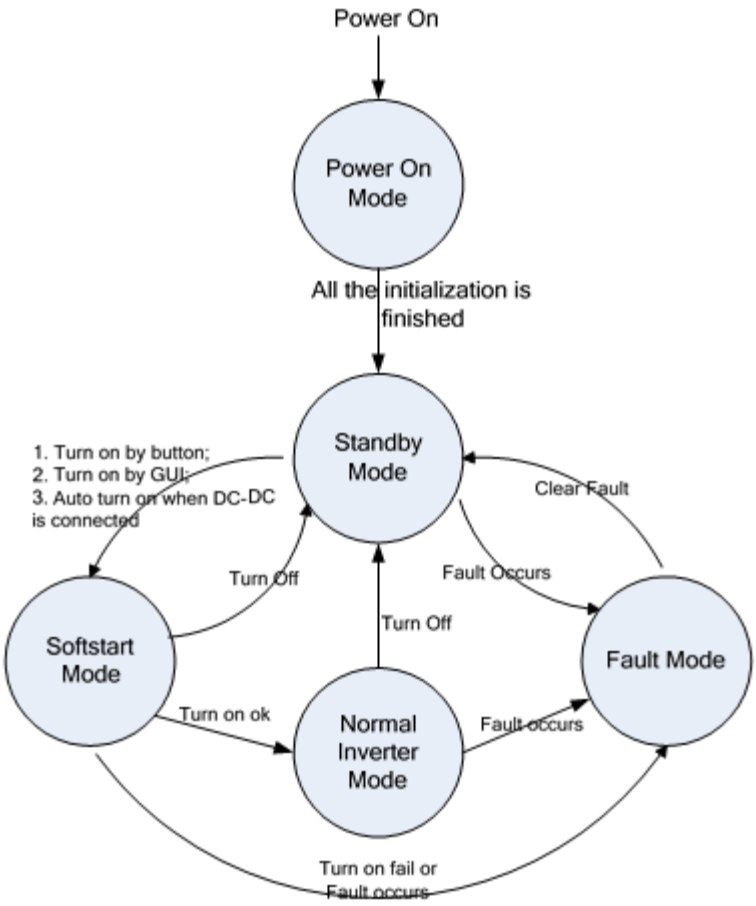

Figure 10. Status Machine

There are five different running modes in the firmware:

- *Power-on mode*: When the board powers up, the MCU will initialize itself in power-on mode first. When the MCU finishes, the system will transfer to standby mode automatically.
- *Standby mode*: When the system is in standby mode, all pulse width modulations (PWMs) and relays are off. The system is waiting for the command to turn on and will detect if any fault occurs.
- *Soft-start mode*: When there is a turning on command, the system will go to the soft-start mode first, which turns on the PWM and relay. If no fault occur, the system will transfer to normal inverter mode automatically.
- *Normal inverter mode*: When the system is in normal inverter mode, the system feeds the energy out. If no faults or turning off command occurs, the system will stay in this mode.
- *Fault mode*: When there is a fault, for example a BUS overvoltage, the system will transfer to fault mode immediately. All PWMs are off and the output relay is cut off from the output. The fault can be cleared by the button or the GUI. When the fault is cleared, the system will return to standby mode.

2.2.3 LED Flashing Design

The LED on the control card will flash in different ways according to the running modes defined in Section 2.2.2 (see Table 3). The LD2 is defined as the mode LED, and the LD3 is defined as the fault LED.

Table 3. LED Flashing Definition

SYSTEM MODE	LD2	LD3
Power-on mode	Always on	Always on
Standby mode	Flashing every 0.5 seconds	Always off
Standby mode (with warning[1])	Flashing every 0.5 seconds	Flashing every 0.5 seconds
Soft-start mode	Flashing fast	Always off
Normal inverter mode	Always on	Always off
Fault mode	Always off	Always on[2]

(1) **When the LD3 is flashing, press the button on the board or click the turn on button in the GUI to clear the warning.** The system can be turned on only if there is no fault or warning. The warning can be generated by the following conditions: turning off, grid voltage out of range or the DC bus voltage abnormal. Please check the firmware for the warning generation details. The flag named FSuperFlag.BIT.FwWarning represent the warning status.

(2) **If the LD3 is flashing or always on, power off and check the hardware.**

2.2.4 Tasks

The system uses three main tasks in the background:

- *Task_A0*: This one-millisecond task has four subtasks, but only tasks A1 and A3 are used in the system. The subtask A1 deals with the status machine transition. A1 checks the status every 20 ms. When the running mode is changed, the new running mode will take effect after 20 ms. The subtask A3 detects onboard buttons and controls LED flashing.
- *Task_B0*: This four-millisecond task has four subtasks. The subtask B1 detects faults, including the short circuit check, overcurrent check, grid voltage and frequency check, and the DC BUS voltage check. The subtask B2 calculates the measurements for the grid voltage RMS and output current RMS, active power, DC BUS voltage, and zero crossing check. The subtask B3 checks activation. The subtask B4 deals with the GUI command processing and board-to-board communication.
- *Task_C0*: This 0.5 millisecond task only uses C0 to check the SCI communication.

2.2.5 Interrupts

Three interrupts are used to deal with real-time events:

- *ADCINT1*: The interrupt is generated by the ADC EOC. When the ADC sampling finishes, the interrupt will trigger. The ISR will execute the controller algorithm.
- *ECAP1_INT*: The interrupt is generated by the capture event. When the zero crossing occurs, the falling edge will trigger the capture event.
- *LIN0INTA*: The interrupt is generated by the RXD event of the LINA. The LIN is used as the SCI port to communicate with the DC-DC board.

3 How to Build the Firmware

3.1 File Structure of the Project

The software project has many files, including the c files, the assembly (asm) files, and the head and command (cmd) files. Table 4, Table 5, and Table 6 describe the files in detail, respectively.

Table 4. C Files

C FILES NAME	DESCRIPTION
ADC_SOC_Cnf.c	Initializes the ADC
SciCommsGui.c	Communicates with the GUI
SolarHv_DCAC-DevInit_F2803x.c	Initializes the MCU device
SolarHv_DCAC-CAP_Cnf.c	Initializes the cap
SolarHv_DCAC-Lin.c	Communicates with the DC-DC board
SolarHv_DCAC-main.c	**The background**
SolarHv_DCAC-PWM_Cnf.c	Initializes the ePWM

Table 5. Assembly Files

ASM FILES NAME	DESCRIPTION
SolarHv_DCAC-CNTL_2P2Z.asm	**The 2P2Z controller for the current**
SolarHv_DCAC-ADCDRV_5CH.asm	ADC sample
SolarHv_DCAC-DLOG_4CH.asm	Get the real time data
SolarHv_DCAC-GEN_SIN_COS.asm	Generate the sine and cosine wave
SolarHv_DCAC-INV_ICMD.asm	Calculate the current loop reference
SolarHv_DCAC-ISR.asm	The ADC interrupt ISR for the controller
SolarHv_DCAC-PWMDRV.asm	Calculate the CMPR and update the duty

Table 6. Head and Command Files

OTHER FILES NAME	DESCRIPTION
SolarHv_DCAC-Settings.h	The project build setting
SolarHv_DCAC-f28035_**FLASH.CMD**	Command file for code running in Flash
SolarHv_DCAC--f28035_RAM.CMD	Command file for code running in RAM

3.2 Blocks Introduction

The following blocks are used to realize a specified function. Users can use these blocks in their own projects.

3.2.1 ADCDRV_5CH: m n p q s

The block ADCDRV_5CH is an ADC sampling driver module, which can be used to get five sample channels.

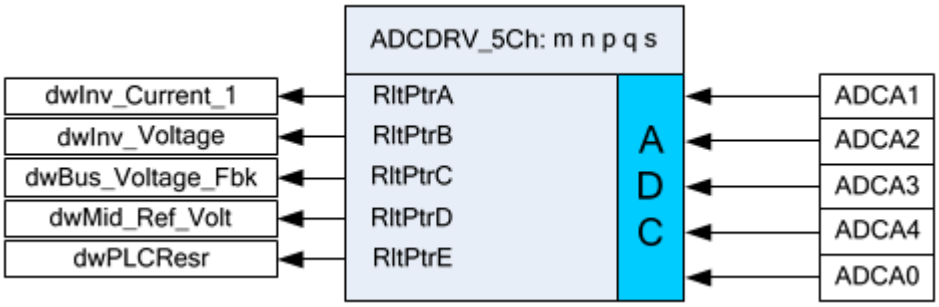

Figure 11. ADCDRV_5CH Block

This ADC uses five channels:

- *ADCA1* is assigned to sense the inductor current. dwInv_Current_1 is named for this channel in the software, and the format of dwInv_Current_1 is Q24.
- *ADCA2* is assigned to sense the grid voltage. dwInv_Voltage is named for this channel in the software, and the format of dwInv_Voltage is Q24.
- *ADCA3* is assigned to sense the DC BUS voltage. dwBus_Voltage_Fbk is named for this channel in the software, and the format of dwBus_Voltage_Fbk is Q24.
- *ADCA4* is assigned to sense the 1.65-V reference. dwMid_Ref_Volt is named for this channel in the software, and the format of dwMid_Ref_Volt is Q24.
- *ADCA0* is reserved for future PLC applications.

3.2.2 GEN_SIN_COS: n

GEN_SIN_COS: n is used to generate the sine wave and cosine wave.

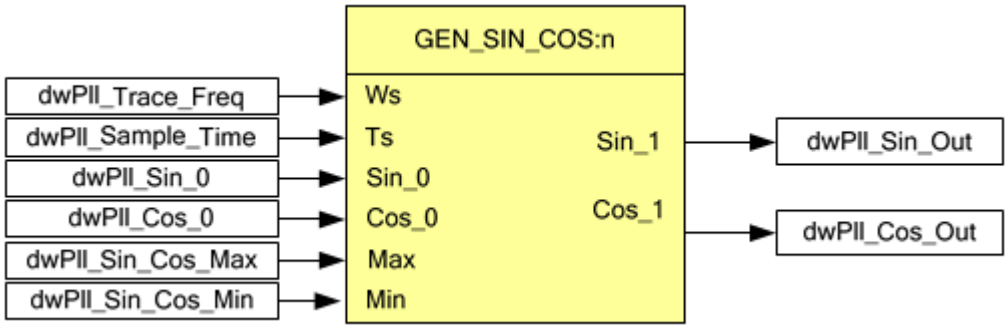

Figure 12. GEN_SIN_COS: n

Ws is the frequency input of the generator. dwPll_Trace_Freq is assigned for this input, and the format is Q20. For example, dwPll_Trace_Freq = _IQ20(376.9911) represents 60 Hz.

Ts is the sample frequency of the generator. dwPll_Sample_Time is assigned for this input, and the format is Q24. For example, dwPll_Sample_Time = _IQ(0.000052) represents **52e-6** seconds.

Sin_0 is the initial value of the sine value. dwPll_Sin_0 is assigned for this input, and the format is Q22. The default value of the dwPll_Sin_0 is 0.

Cos_0 is the initial value of the sine value. dwPll_Cos_0 is assigned for this input, and the format is Q22. The default value of the dwPll_Cos_0 is _IQ22(0.99).

Max is the maximum value of the output value. dwPll_Sin_Cos_Max is assigned for this input, and the format is Q22. The default value of the dwPll_Sin_0 is _IQ22(0.99)

Min is the minimum value of the output value. dwPll_Sin_Cos_Min is assigned for this input, and the format is Q22. The default value of the dwPll_Sin_Cos_Min is 0.

3.2.3 INV_ICMD:n

INV_ICMD:n is used to calculate the current reference.

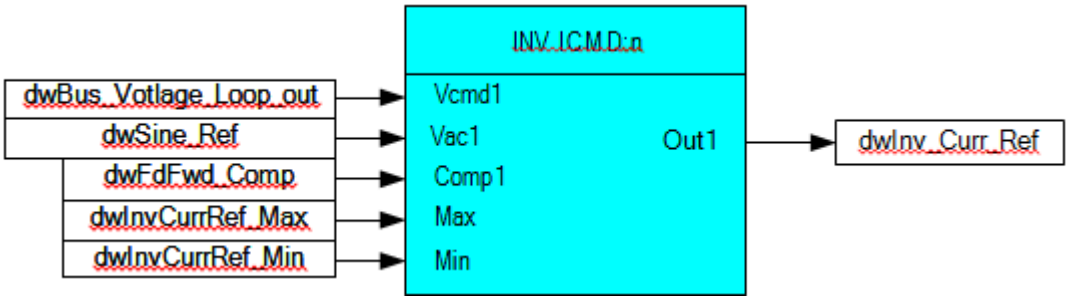

Figure 13. INV_ICMD:n

Vcmd1 is the amplitude of the reference current, which is usually the voltage loop controller output. The dwBus_Voltage_Loop_Out is assigned as the interface. The format is Q24.

Vac1 is the unit sine wave, which represents the reference angle of the current, usually the sine generator's output. The dwSine_Ref is assigned as the interface. The format is Q24.

Comp1 is the compensation for the change of the grid voltage. The default value is 1.

Max and *Min* are the output's limitations.

Out1 is the output of the block. dwInv_Curr_Ref is assigned as the interface, and the format is Q24.

3.2.4 PWMDRV:n

PWMDRV: n is used to calculate the CMPR according to the controller's output and update the CMPR register when it finishes the calculation.

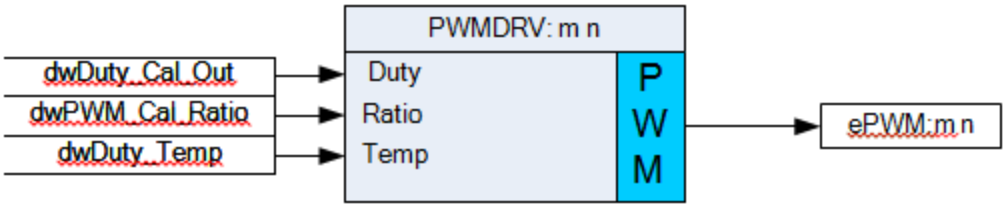

Figure 14. PWMDRV:n

Duty is the output of the controller, which is usually the current loop controller output. dwDuty_Cal_out is assigned for this input, the format is Q24.

Ratio is the conversion ratio between Duty and the CMPR value. The format is Q8. The ratio can be calculated by the following method. Ratio = Period * 1000 / Vdc.

Temp is reserved for debug.

3.2.5 CNTL_2P2Z:n

This is same to the blocks defined in **Digital Power Library**.

3.2.6 DLOG_4CH:n

This is similar to the blocks defined in the Digital Power Library, but the start of the log is different. In this project, when the variable wDataEnable is 1, the block starts the data log.

3.3 Build Step

The following subsection discusses the incremental build and realizes the functions step by step. The build step can be set by the pre-defined macro INCR_BUILD in the head file named SolarHv_DCAC-Settings.h. See the setting in Table 7:

Table 7. Incremental Build Option

INCR_BUILD = 1	Open loop build
INCR_BUILD = 2	Close loop without PLL
INCR_BUILD = 3	Close loop with PLL

3.3.1 Start the CCS Project

1. Connect the USB cable to the ISO PiccoloB control card. Short jumpers JP2, JP4, JP5, and JP6, and open jumpers JP3 and JP1.
2. Insert the 15-V adapter to J1, then switch the S1 to power on the auxiliary power.
3. Start CCS v4 and create a new workspace. When the IDE is opened, click the menu: Project \Import Existing CCS \CCE Eclipse Project and under Select Root Directory navigate to and select ..\controlSUITE\development_kits\Solar HV Kit\DC-AC board.
4. When the project opens successfully, see the following workspace:

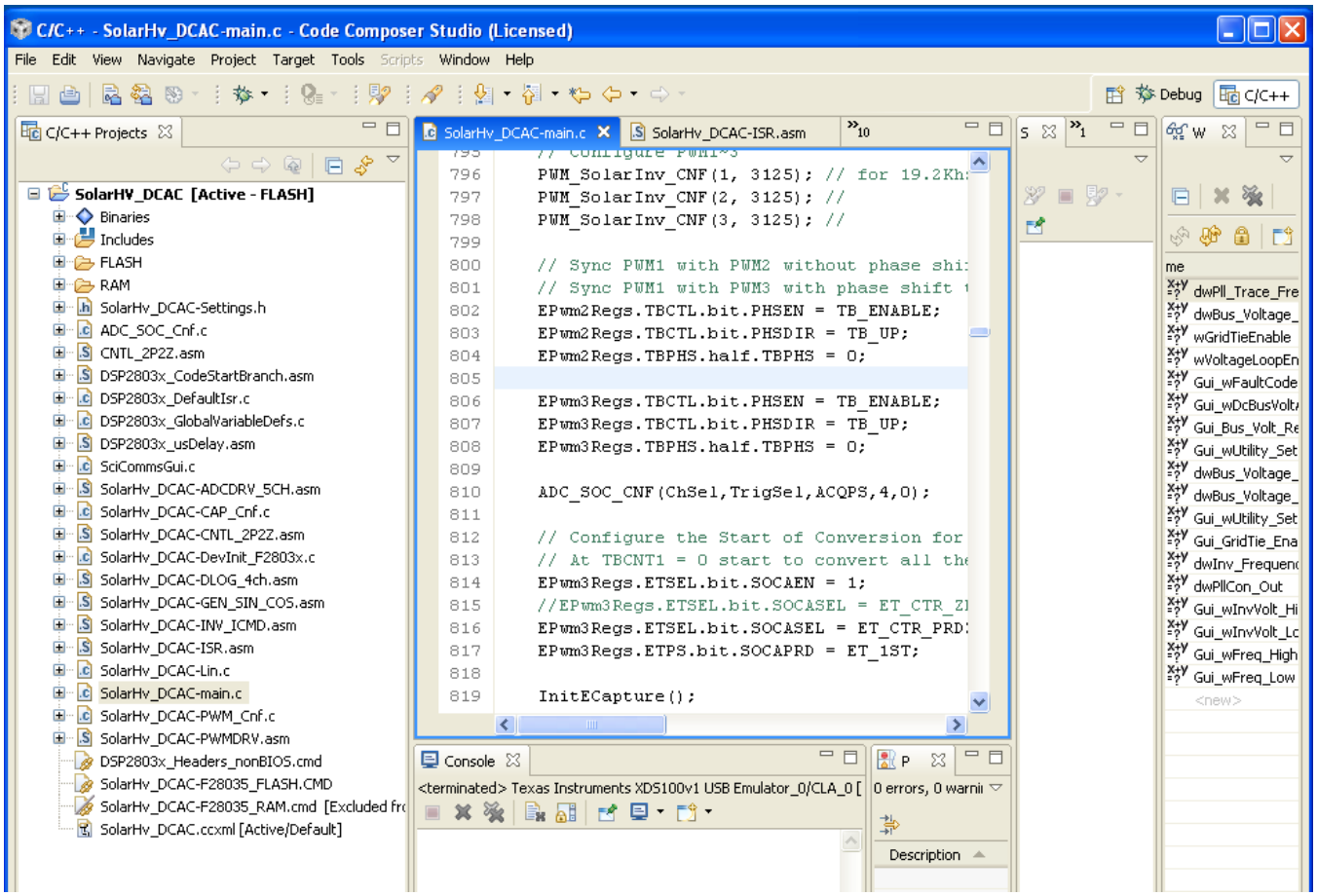

Figure 15. Something

5. Change the incremental build option by setting a value to INCR_BUILD.

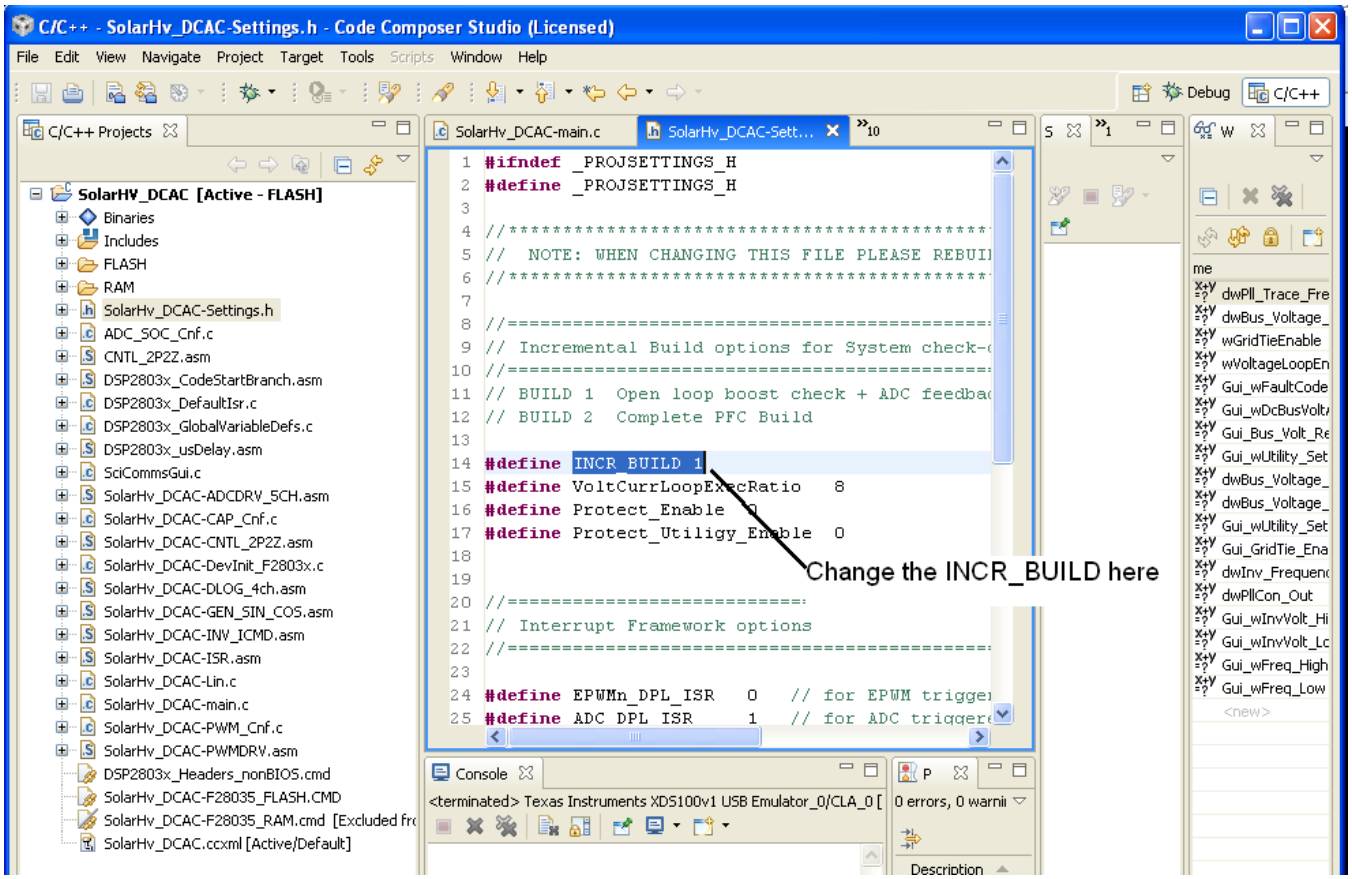

Figure 16. Something Else

6. Set the build configuration by clicking the menu: Project\Active Build Configuration. If the user wants to run the code in RAM, choose the RAM or the FLASH option.
7. Rebuild the project by clicking the menu: Project\Rebuild All. If there is no error, the new .out file will be created.
8. In the .ccxml file that opens, select *Connection* as *Texas Instruments XDS100v2 USB Emulator*, and under the device, scroll down and select *TMS320F28035*. Click *Save*.
9. Start the TI debugger by clicking the *Target\Debug Active Project*.
10. When the code is loaded successfully, see the following debug window:

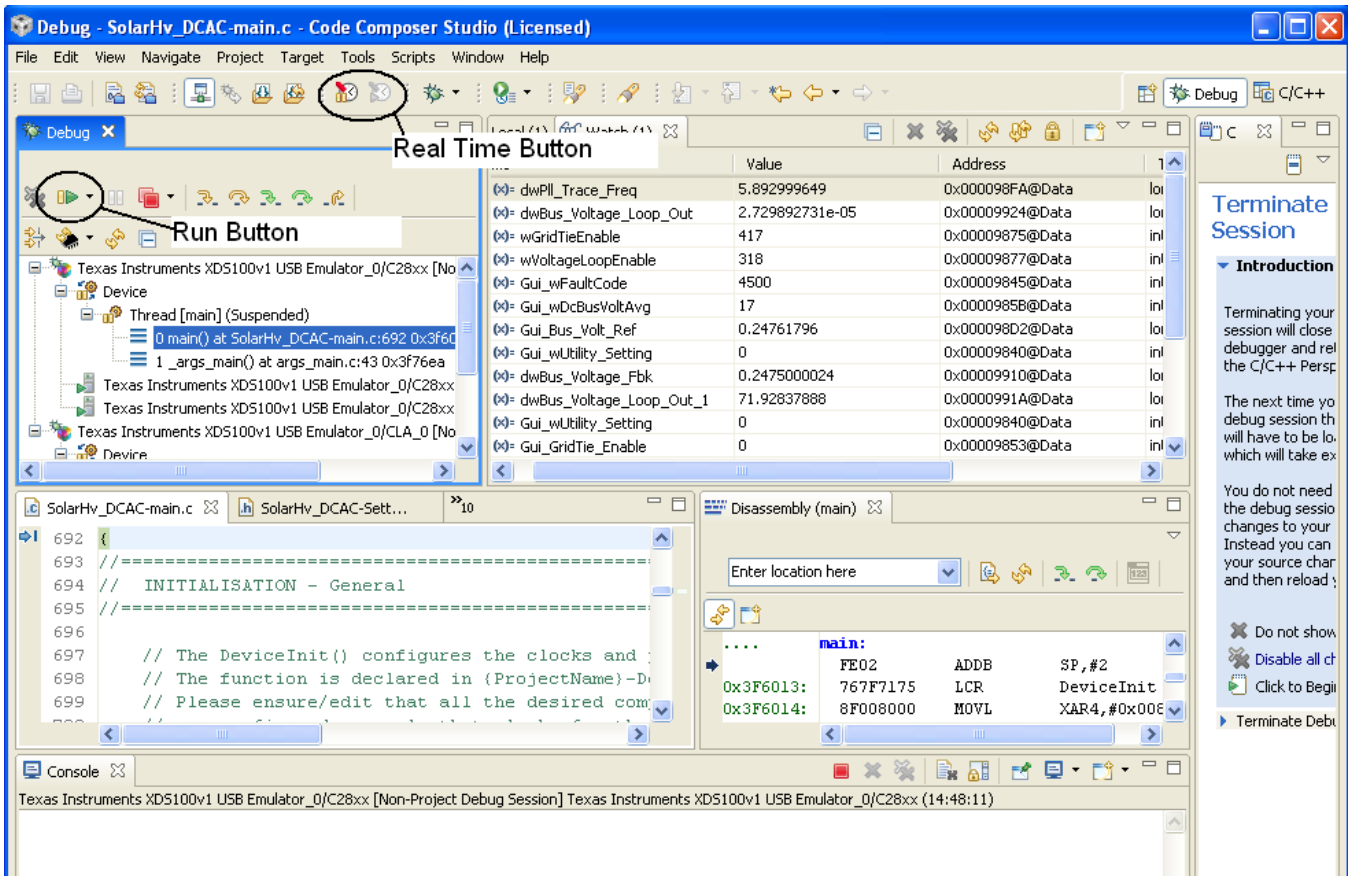

Figure 17. Something Also

11. Use the *Real-Time Debug* option by clicking the button in the tool bar.
12. Run the code by clicking the *Run* button in the toolbar.

3.3.2 Open Loop Build

The first step is the open loop build, let the board output a sine wave. In this step, the GEN_SIN_COS and the PWMDRV block are used to generate the SPWM. Because DLOG_4CH and ADCDRV_5CH are also used, the user can check the sample data by real time or the GUI (If the GUI is used, the user must run the code in the flash).

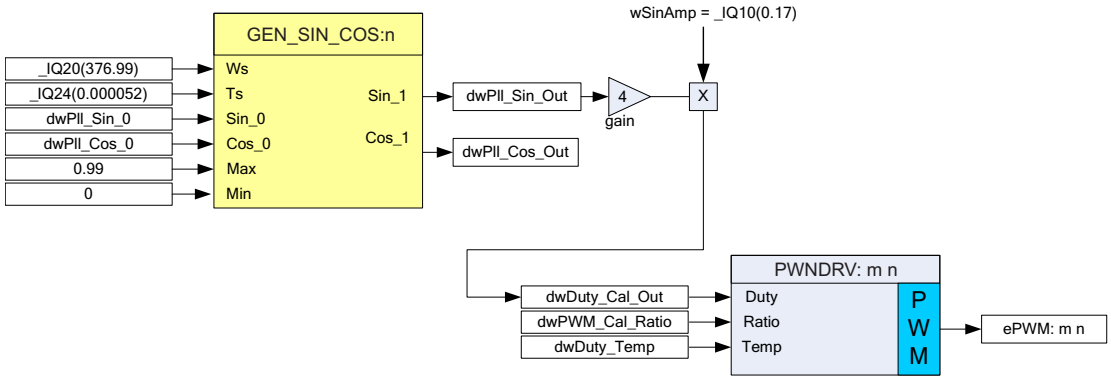

Figure 18. Open Loop Build

The open loop build can be available when set the INCR_BUILD = 1 in the SolarHv_DCAC-Settings.h file. When the code is running, set the DC source input to about 400 V, then press the SW1 to turn on the board.

3.3.3 Close Loop Build without PLL

When the grid is not connected to the board, the board can run the close loop without the PLL. The build will output a constant current to the load. Before this step, complete the open loop test successfully; the loop must connect a resistor load to the output. The suggested resistor load is 25 ohm/1000 W.

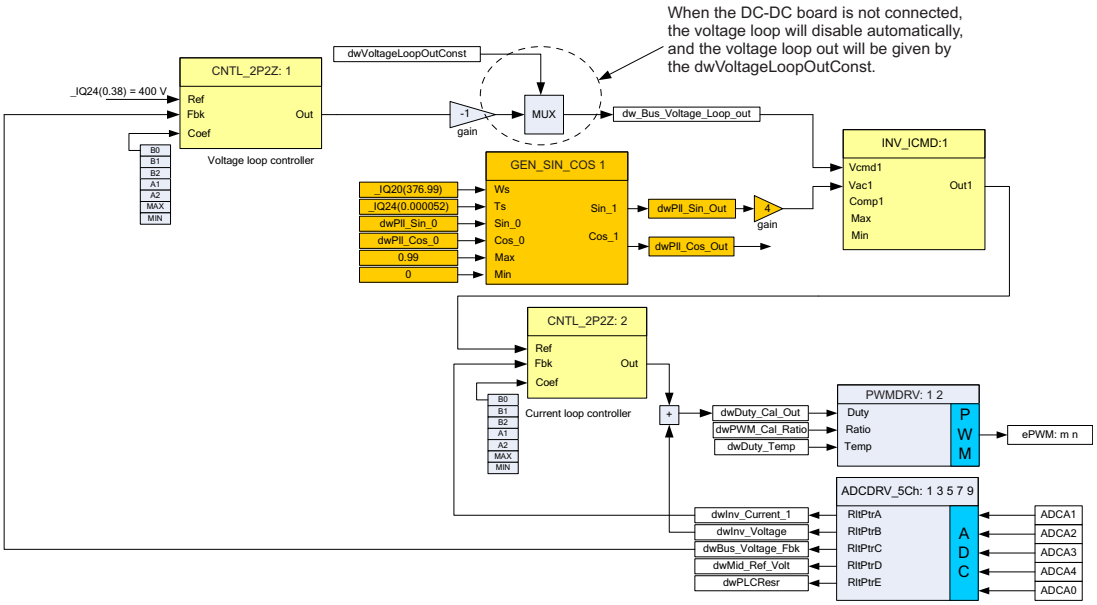

Figure 19. Close Loop Build without PLL

The close loop without PLL build can be available when set the INCR_BUILD = 2 in the SolarHv_DCAC-Settings.h file. When the DC-DC board is not connected, the voltage loop will be disabled automatically. The dw_Bus_Voltage_Loop_Out will be given by the dwVoltageLoopOutConst directly. The user can modify the dwVoltageLoopOutConst in real time to get a different output current value.

3.3.4 Close Loop Build with PLL

If all the above build is finished, user can do the final build step for the grid tie test. The user must connect the test tool to the board like the following diagram.

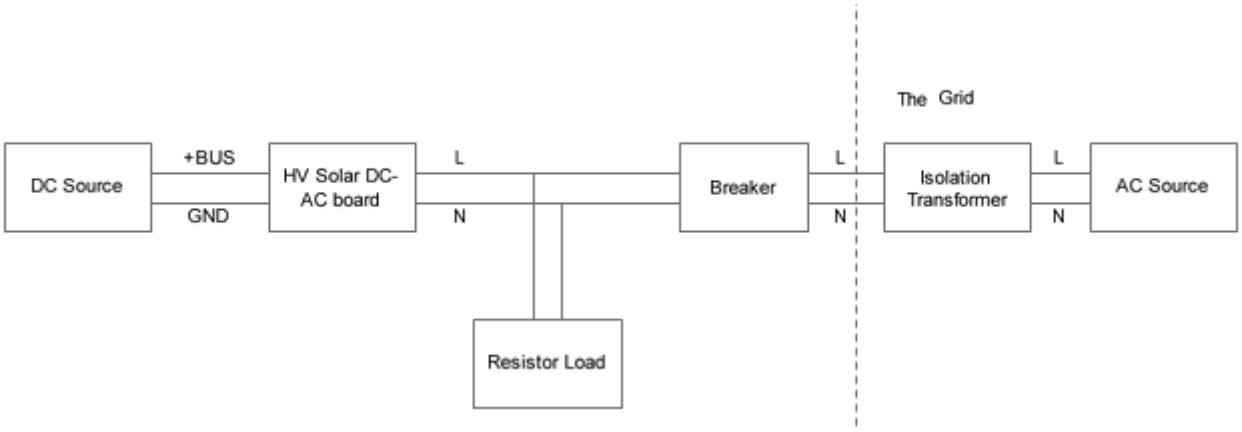

Figure 20. Test Connection

For safety, use a breaker between the grid and inverter output.

NOTE: All tests should be done in a lab, and the user must use the AC source to emulate the grid. There is no security when the user uses this board to connect to the grid.

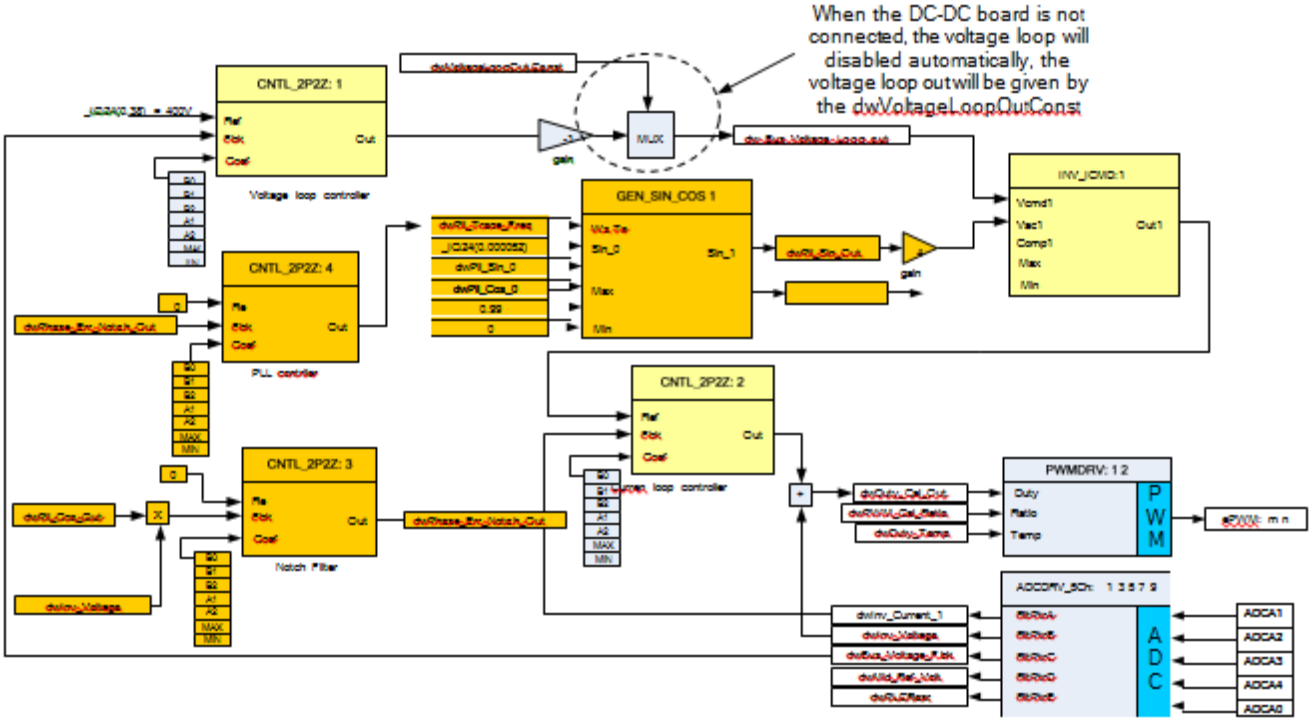

Figure 21. Close Loop With PLL Build

The close loop with PLL build can be available when set the INCR_BUILD = 3 in the SolarHv_DCAC-Settings.h file. Please note that when the DC-DC board is not connected, the voltage loop will be disabled automatically. The dw_Bus_Voltage_Loop_Out will be given by the dwVoltageLoopOutConst directly. User can modify the dwVoltageLoopOutConst in the real time to get the different output current value.

4 Test Results

4.1 Specification

The system main spec is below:

Power Rating: 600 W.
Norminal Grid Voltage: 120 V/60 Hz (RMS), 220 V/50 Hz.
Output Power Factor: 1.
THDi: <5%
Panel Input Voltage Range: 400 V.
Grid Tie. Anti-islanding Protection.
Test Condition: AC source connected, with 120-V AC/60 Hz;
DC bus voltage: 400 V
Power range: 100 to 600-W output;
Grid-Tie.
Room Temperature

4.2 DC-AC Board Current Loop Grid-Tie Test Results

CH2: Output Current (Blue)
CH3: Grid Voltage (Red)
CH4: BUS voltage

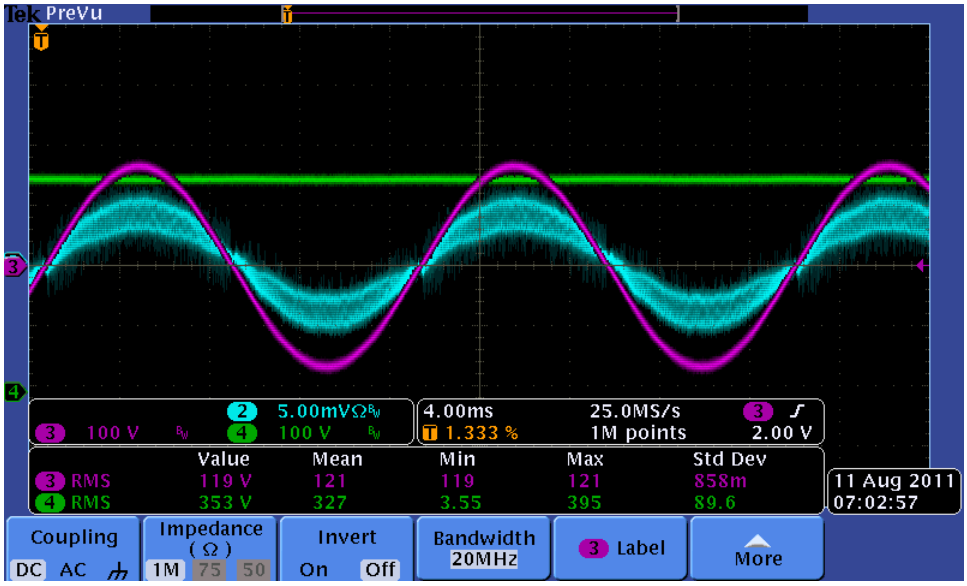

Figure 22. Light Load Current and Grid Voltage Waveform

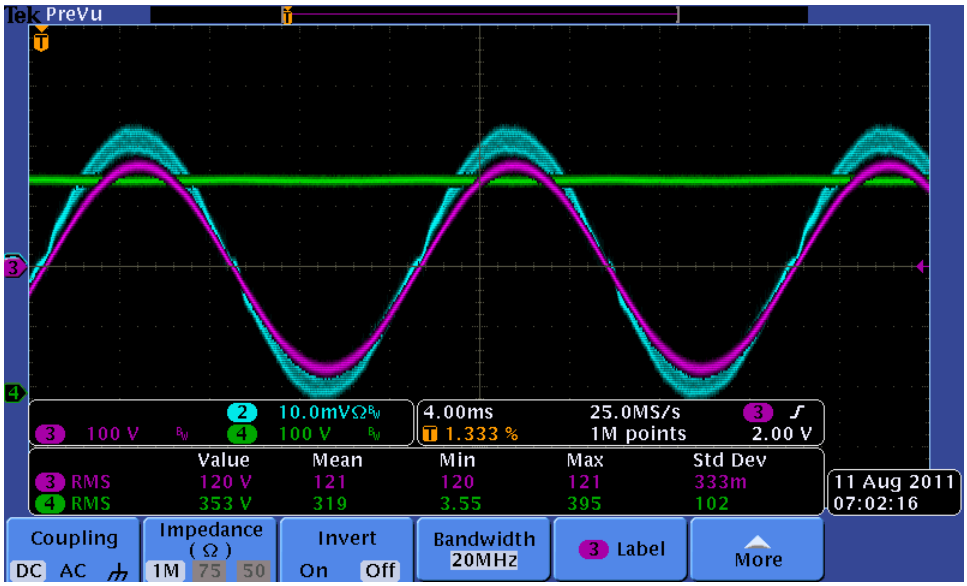

Figure 23. Middle Load Current and Grid Voltage Waveform

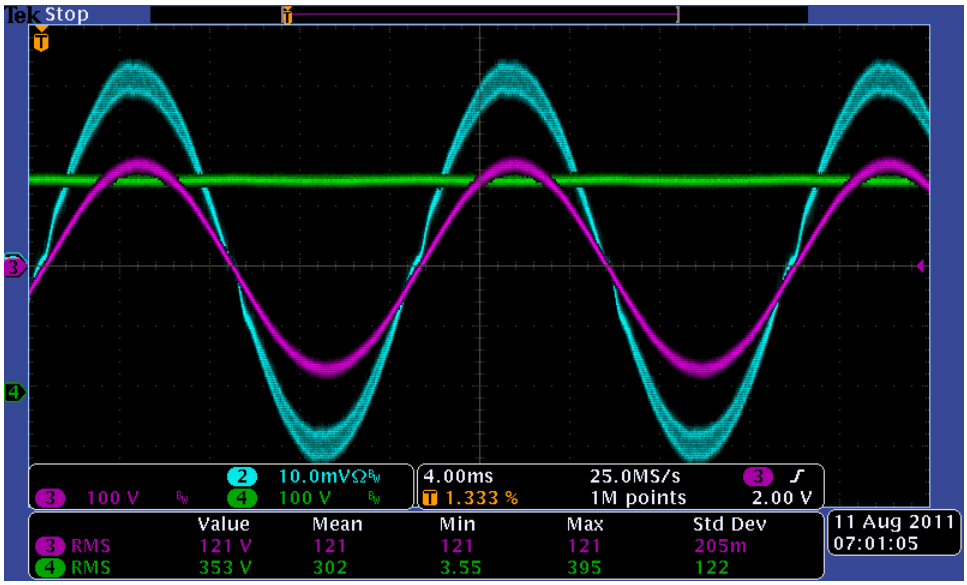

Figure 24. Full Load Current and Grid Voltage Waveform

4.3 Output Power Factor and THDi

Table 8. PF and THDi

INV V_OUT	INV P_OUT	OUTPUT PF	THDI
119.5	100.3	0.983	12.60%
119.8	151.6	0.992	8.70%
119.2	198.4	0.995	6.80%
119.5	248.1	0.996	5.80%
119.8	297.7	0.997	5%
120.1	344.1	0.997	4.30%
119.6	391.7	0.997	3.90%
119.9	439.2	0.997	3.60%
120	464.2	0.997	3.40%

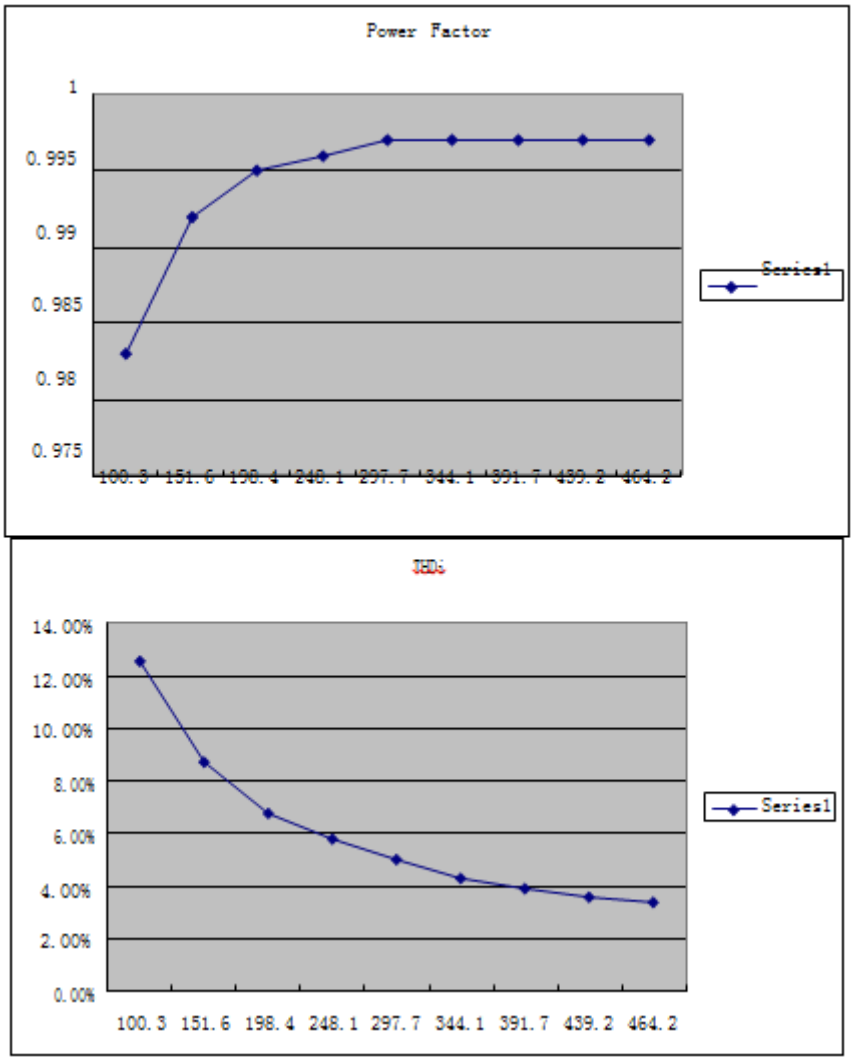

Figure 25. PF and THDi

4.4 Efficiency

Table 9. Efficiency

ITEM	DC_IN (V)	AC_OUT (V)	OUTPUT (W1)	INPUT (W)	EFFICIENCY (%)
1	400	120	609	632	96.3
2	400	120	536	557	96.2
3	400	120	500	521	95.9
4	400	120	446	467	95.5
5	400	120	356	376	94.5
6	400	120	302	321	94.1

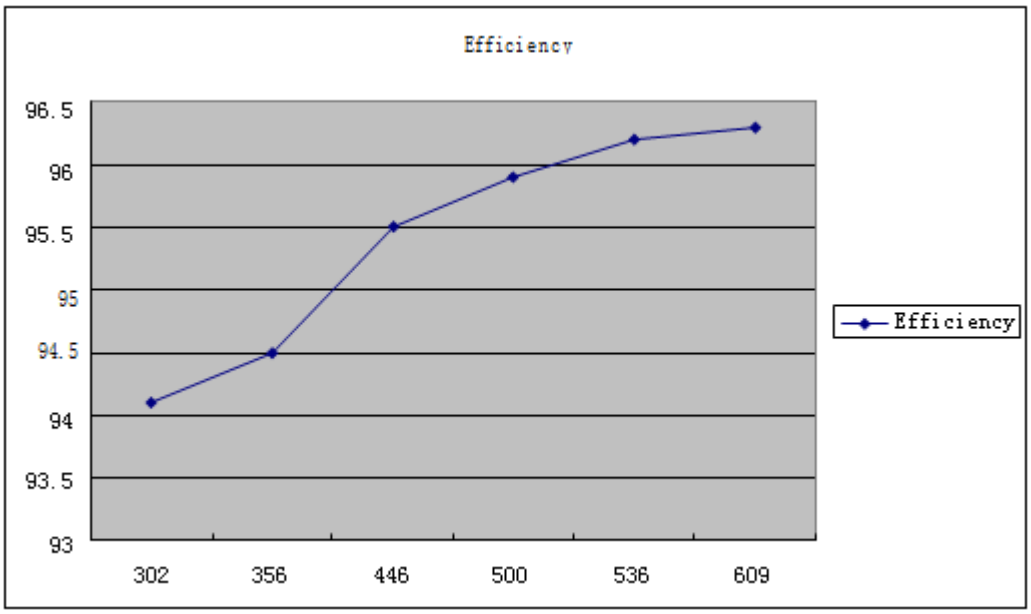

Figure 26. Efficiency

4.5 HV Solar System Test

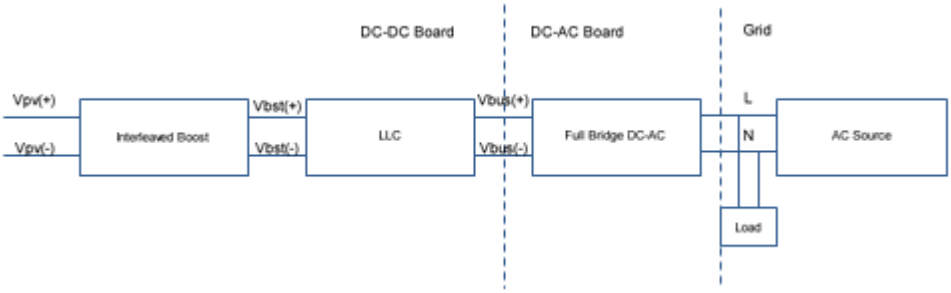

Figure 27. System Structure and the Connection

CH2: Output Current (Blue)
CH3: Grid Voltage (Red)
CH4: BUS voltage

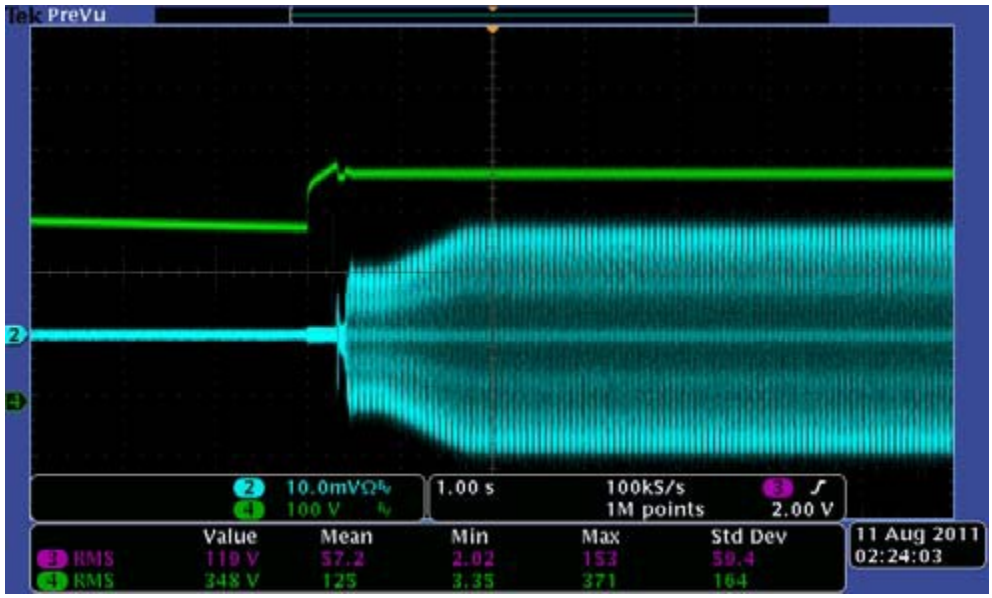

Figure 28. 120-V AC/60 Hz, Turning on

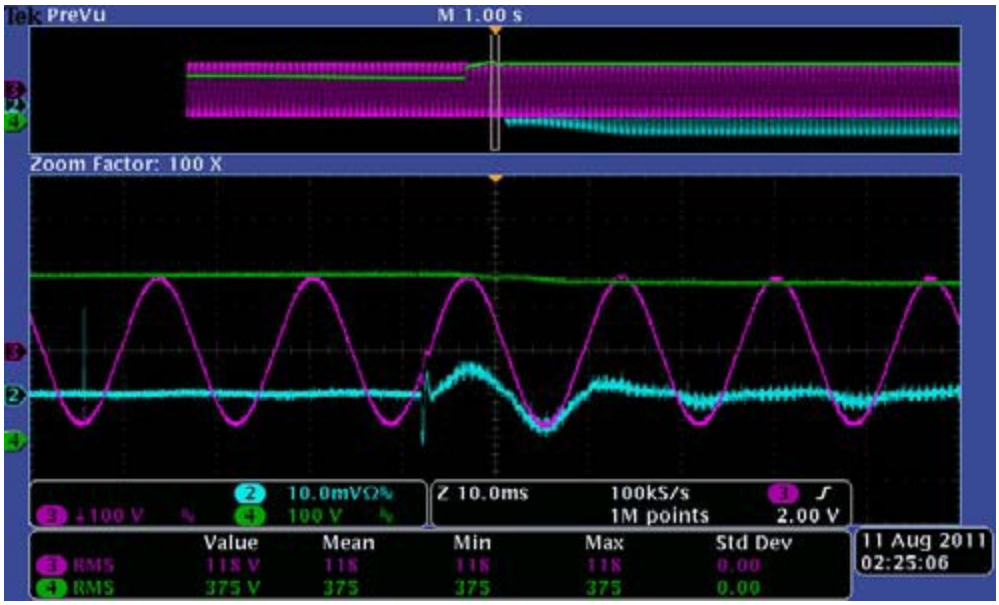

Figure 29. Turning on Overview

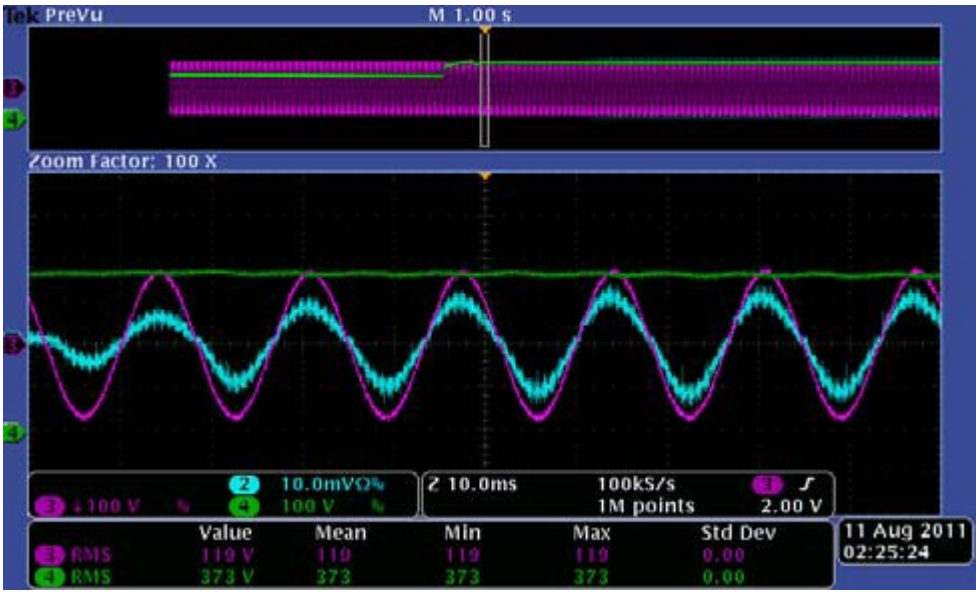

Figure 30. DC-AC Turning on the PWM

CH2: Output Current (Blue)
CH3: Grid Voltage (Red)
CH4: BUS voltage

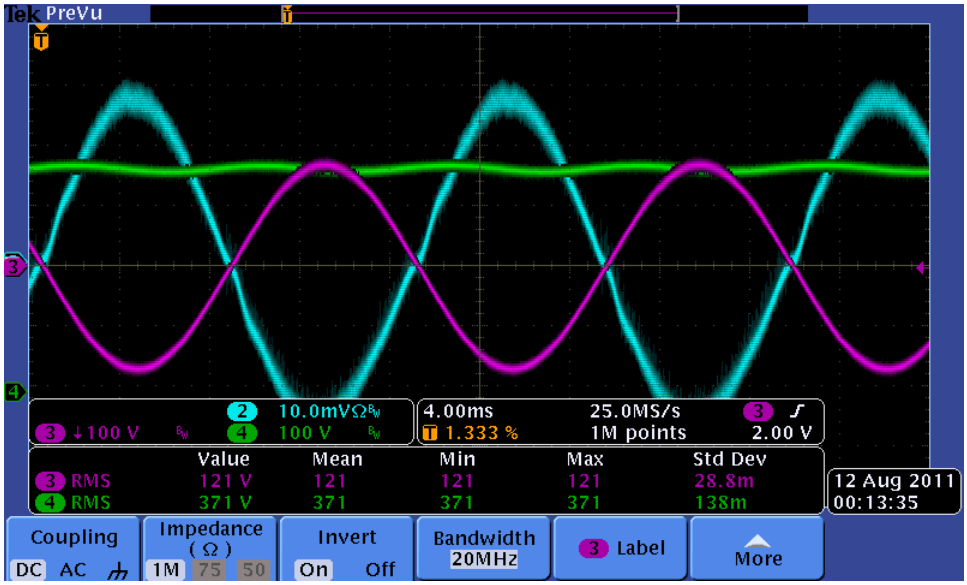

Figure 31. Something

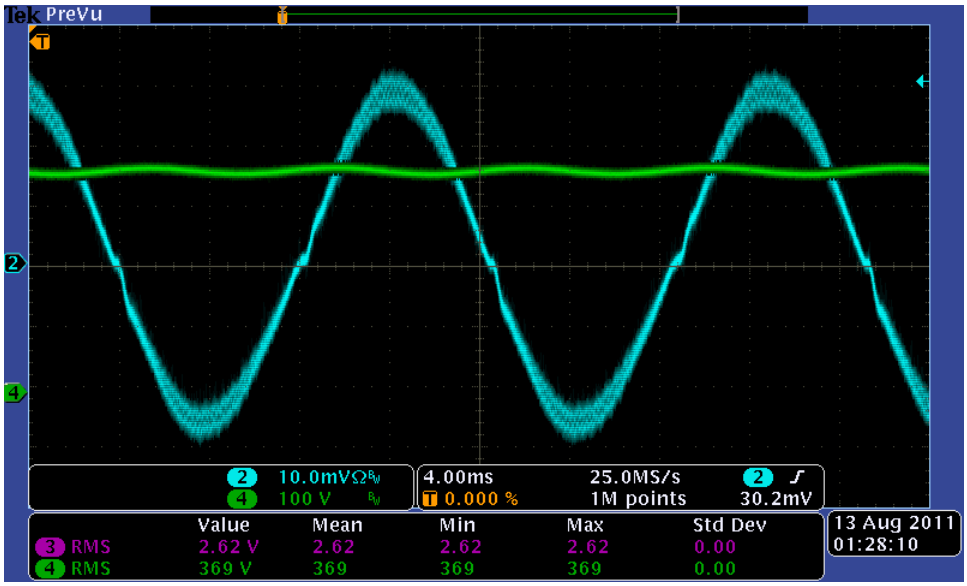

Figure 32. Something Else

5 Design Files

5.1 BOM

Table 10. BOM: Main Board v2.7

DESIGNATOR	FOOTPRINT	QTY	VALUE	DIGIKEY PART NO	MANEX PART NO	MFGR PART NO	VENDOR PART NO
C1	CE1035P2	0	470 u/450 V	Not connected			
C2, C47, C48	CAP-P10-13X4.5	3	0.02 2u/630 V	P12125-ND			
C3	C27515P2	1	1 u/275 V	"DigiKey Part No:399-5467-ND Manufacturer Part No:R46KR410000M1K"			
C4, C6, C9, C15, C37, C38	C0603	6	100 nF/16 V	478-1259-2-ND			
C5, C10, C11, C12, C13, C14, C18, C20, C21, C36, C50	C0603	11	1 nF/16 V	0603YC102MAT4A-ND			
C7, C8, C16, C17	C0603	4	220 pF/16 V	0603YC221MAT2A-ND			
C19	C0603	1	0.47 uF/25 V	445-5145-2-ND			
C22, C42	C07521A	2	1000 pF/50 V	P4036A-ND			
C23, C28	E/2.5/6.5/E1@	2	22 uF/25 V	493-1058-ND			
C24, C29	CAP-3528	2	10 uF/16 V	478-1675-2-ND			
C25	CAP-3528	1	22 uF/10 V	478-3040-2-ND			
C26	Radial Can(2563)	1	100 uF/25 V	P10413TB-ND			
C27	Radial Can(2550)	1	100 uF/16 V	P10408TB-ND			
C30	CAP-3528	1	22 uF/10 V	478-3040-2-ND			
C31, C32, C33, C34	C0603	4	100 nF/10 V	478-1259-2-ND			
C35	C0603	1	220 pF/10 V	0603YC221MAT2A-ND			
C39, C40	Radial Can(5080)	2	220 uF/25 V	P10377TB-ND			
C41	C0603	1	0.1 uF/25 V	478-1244-2-ND			
C43	C0603	1	0.47 uF/25 V	445-5145-2-ND			
C44	Radial	1	10 nF/50 V	478-4271-2-ND			
C45,C46	Axial	2	0.1 uF/100 V	478-3154-1-ND			
CN1, CN2, CN3, CN4	HDR1X10	4	The Driver Module	Driver board			
CN5	HDR2X5	1	The DC-DC signal interface. Standard 0.1" SIL headers, cut to fit, total needed 2x5	Refer to the V1 board	260-0009772		
CN6	HDR1X3	1	The External SCI port	Not connected			

Table 10. BOM: Main Board v2.7 (continued)

DESIGNATOR	FOOTPRINT	QTY	VALUE	DIGIKEY PART NO	MANEX PART NO	MFGR PART NO	VENDOR PART NO
CON1, CON2	CN3P/7.62	2	The Power Line Connector, including the Header and Plug	ED1734-ND(Plug) ED2851-ND(Header)			
D1, D2	D10626A	2	1N4937	1N4937FSTR-ND			
D3, D4	LED0805	2	LED	404-1021-1-ND			
F1	F275P2	1	10 A/250-V AC	F2519-ND			
The Ears for F1	Through hole	2		F3784-ND			
HCT1	HCT-HNC-05SYB	1	HNC-05SYB	Bought from China			
J1	DCJACK	1	15-V Power DC Jack connector	CP-002AH-ND	260-0005141	PJ-002AH	
JP1, JP2, JP3, JP4, JP5	HDR1X2	5	Standard 0.1" SIL headers, cut to fit, total needed 1x2	260-0008027			
JP6	HDR1X2	1	Standard 0.1" SIL headers, cut to fit, total needed 1x2	260-0008027			
JTAG1	JTAG	1	JTAG port. Standard 0.1" SIL headers, cut to fit, total needed 2x7	Refer to the V1 board	260-0009772		
L1, L2	Inductor-57x30	2	3.5 mH/T184-8/90	Bought from China			
P1	HDR2X9	1	PLC Interface/Not Connected	Not connected			
P2	HDR2X4	1	PLC Interface/Not Connected	Not connected			
PW1	PR902A	1	PR902/Texas Instruments	The TI module			
Q1, Q2, Q3, Q4	TO247-HS	4	First Choice: IRG4PC30FDPBf	First Choice: IRG4PC30FDPBF-ND			
HS1,HS2,HS3,HS4	TO247 Heat-sink	4	Heat-sink	Bought from China			
Q5	FET350R	1	2SK2962	2SK2962(F)-ND			
R1, R2, R12, R13	R1210	4	1.33 KSM/0.5 W	541-1.33KAATR-ND			
R4, R5, R14, R26, R27, R28, R29, R30, R31	R0805	9	1 M /1%	P1.00MHDKR-ND			
R6, R201	R10623	2	10/0.5 W	P10BBCT-ND			
R7, R15	R0805	2	20 K/1%	P20.0KCTR-ND			
R8, R9, R17, R18	R10623	4	47 K/0.5 W	P47KBBTB-ND			
R10, R11, R19, R20	R10623	4	10/0.5 W	P10BBCT-ND			
R16	R0805	1	10 K/1%	P10.0KCTR-ND			
R21, R32, R33, R59, R61, R62, R78	R0603	7	10 K/1%	P10.0KHTR-ND			
R22, R34, R43, R48, R49, R65, R66, R77	R0603	8	1 K/1%	P1.00KHTR-ND			
R23	R0603	1	270 K	P270KGTR-ND			

Table 10. BOM: Main Board v2.7 (continued)

DESIGNATOR	FOOTPRINT	QTY	VALUE	DIGIKEY PART NO	MANEX PART NO	MFGR PART NO	VENDOR PART NO
R24	R0805	1	150	P150ATR-ND			
R25	R0805	1	3 K	P3.0KATR-ND			
R35, R37, R38, R41, R71, R73, R74, R75, R76	R0603	9	4.99 K/1%(0603)	P4.99KHTR-ND			
R36	R0603	1	30 K/1%(0603)	P30.0KHTR-ND			
R44, R64, R72	R0603	3	100/1%(0603)	P100HTR-ND			
R54, R56	R0603	2	20 K/1%(0603)	P20.0KHTR-ND			
R55	R0603	1	510 K/1%(0603)	P510KHTR-ND			
R57	R0603	1	100/1%(0603)	P100HTR-ND			
R67	R0603	1	1.2 K(0603)	P1.2KGTR-ND			
R68	R0603	1	1.5 K	P1.5KGTR-ND			
R69	R0805	1	330 (0805)	P330CTR-ND			
R70	R0603	1	10 K (0603)	P10.0KHTR-ND			
RY1, RY2	RELAY-G5LA-1	2	G5LA-14-DC12	Z2561-ND			
S1	SW-3P8X5	1	The 15-V power switch	Refer to the V1 board	249-0000911	108-2AS1T1203-EVX	108-2AS1T1203-EVX
SW1	KRS640	1	The Turn on Key	TL1105TF100Q-ND			
TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP10, TP11	PIN1	10	The test points	Not connected			
U1	2003SM	1	ULN2003ADR	296-1368-1-ND			
U2	DIMM100-1D27	1		Refer to the V1 board	160-0000913	87630-1001	538-87630-1001
U3, U5	TL074SM	2	OPA4350	OPA4350UA-ND			
U4	339SM	1	LM339	296-1013-2-ND			
U6	PTH08080	1	PTH08080	296-20432-ND			
U7, U9	SOT-223-3P	2	TLV1117-33	296-21112-2-ND			
U8	DCH010505	1	DCH010505	296-20638-ND			
U10	IC-SOIC16P-1.27DW	1	ISO7240C	296-22617-2-ND			
U11	IC-SOIC16P-1.27DW	1	ISO7242C	ISO7272CDWR-ND			
U12	DCH010515	1	DCH010515	296-20642-ND			
U13	DCK	1	TPS71501DCKR	296-12957-2-ND			
ZD2, ZD3, ZD4, ZD5	ZD123BSM	4	15 V-CSM/22131	BZV55C15-TPMSTR-ND			

Table 11. BOM: Driver Board v2.5

DESIGNATOR	VALUE	DESCRIPTION	FOOTPRINT	QUANTITY	DIGIKEY NO	WHERE TO BUY
C1, C2, C4	10 u/35 V	CE6666SM	CE6666	3	493-2282-2-ND	USA
C3, C5	104/50 V	C0603SM	C0603	2	478-5052-2-ND	USA
C6	103/50 V	C0603SM	C0603	1	478-1227-2-ND	USA
C8	103/50 V	C0603SM	C0603	1	478-1227-2-ND	USA
C9	104/50 V	C0603SM	C0805	1	478-1395-2-ND	USA
C10	102/50 V	C0603SM	C0603	1	478-1215-2-ND	USA
CN1	DB0HP07L	DB0HP07L	DB0HP07L	1	SAM1051-10-ND	USA
D2, D3, D4	ES2D	1 Amp Fast Recovery Rectifier		3	ES2DFSTR-ND	USA
Q1, Q2	RK7002	7002TSM	7002TSM	2	RK7002BT116TR-ND	USA
Q3	2SC2873	TR62NTSM	TR62NTSM	1	568-6805-2-ND	USA
Q4	2SA1213	TR62PTSM	TR62PTSM	1	2DA1213YDITR-ND	USA
R1	15 K	R0603SM	R0603	1	541-15KGCT-ND	USA
R2, R4	300	R0603SM	R0603	2	541-300GCT-ND	USA
R3	150 ohm/0.5 W	R1206NSM	R1206	1	541-150UCT-ND	USA
R5	2.2 KSM (0603)	R0603SM	R0603	1	541-2.2KGCT-ND	USA
R6, R7	10 K	R0805BSM	R0603	2	P10KCBCT-ND	USA
R8	1.5 KSM (0805)	R0805BSM	R0805	1	P1.5KCBCT-ND	USA
R9	10 ohm	R0805BSM	R0603	1	P10CBCT-ND	USA
R10	10 ohm	R1206NSM	R1206	1	541-10ECT-ND	USA
TX1	TXEE10		Trans-12x12-8pin	1		China
U1	UC3845	38458BSM	8-SIOC	1	296-27153-2-ND	USA
U2	TLP350SM	PH350SM	TLP627-2	1	TLP350F-ND	USA
ZD1	16 V	ZD123TSM	ZD123TSM	1	FLZ16VBTR-ND	USA

5.2 PCB Layouts

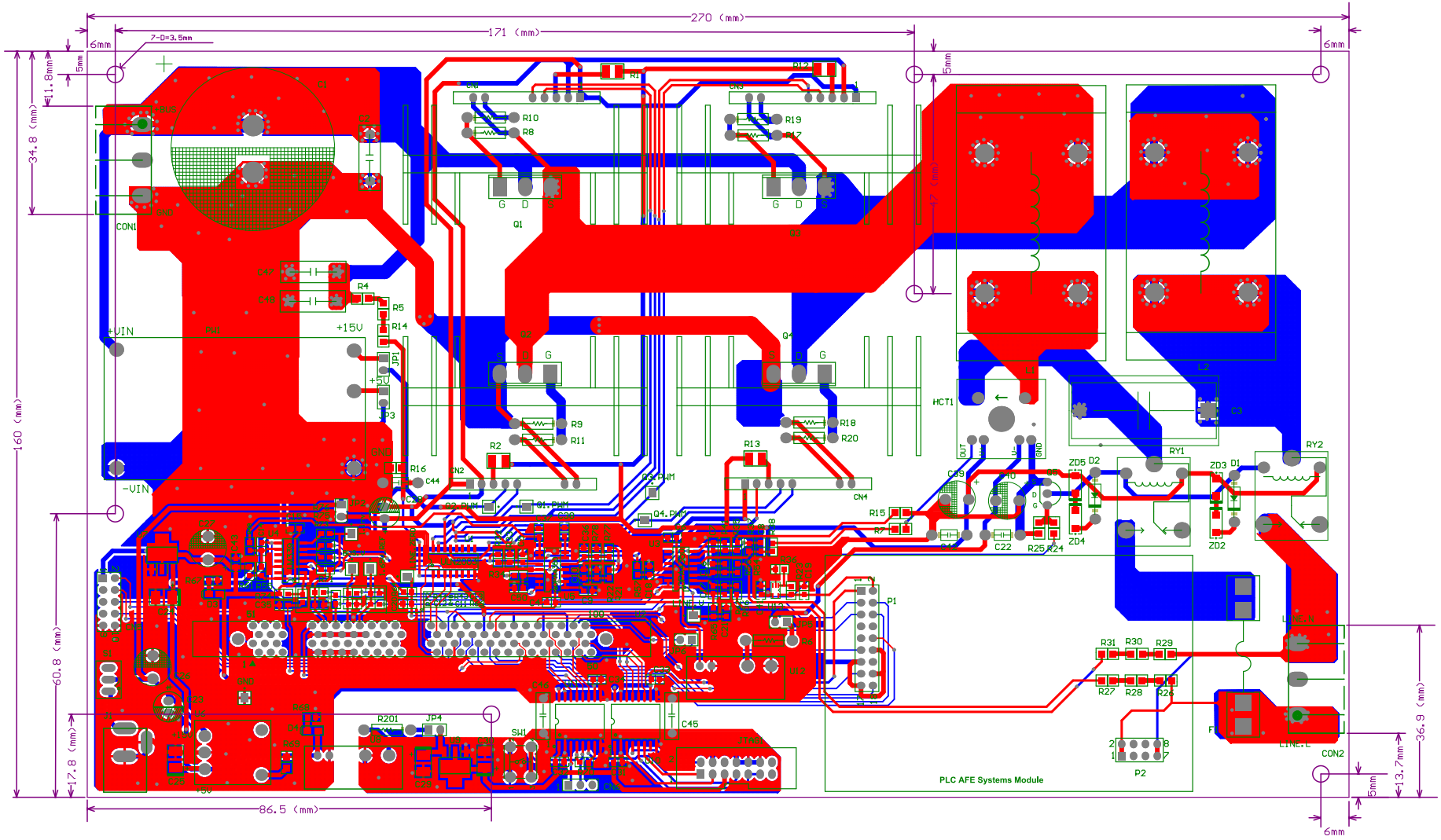

Figure 33. PCB Layout

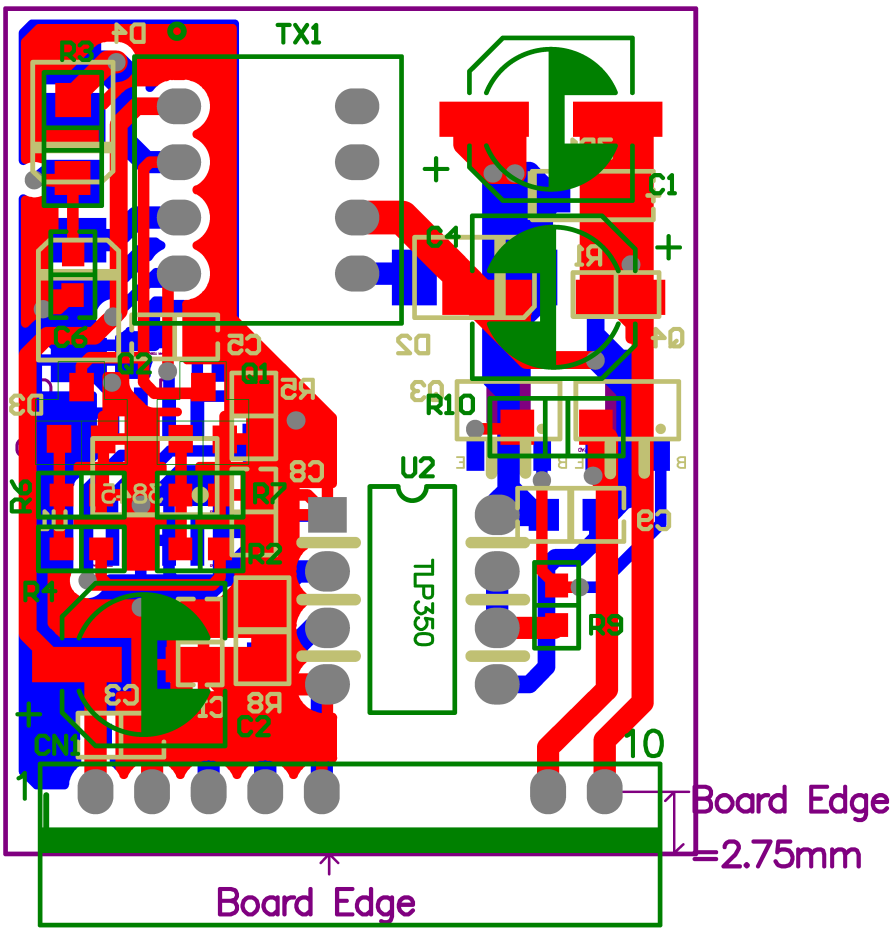

Figure 34. Dimensions

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265