Application Report

nFBGA Packaging

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ABSTRACT

This application report provides technical background on nFBGA packages and explains how to use them to build advanced board layouts.

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1 Introduction

The parallel pursuit of cost reduction and miniaturization in recent years has increased emphasis on very small integrated circuit (IC) package solutions. This is particularly evident in consumer-based end equipment using digital signal processor (DSP) solutions such as wireless telephones, laptop computers, and hard-disk drives. Despite the formal definition, packages with an area similar in size to the IC they encapsulate are loosely referred to as chip scale packages (CSPs). Figure 1-1 illustrates this trend.

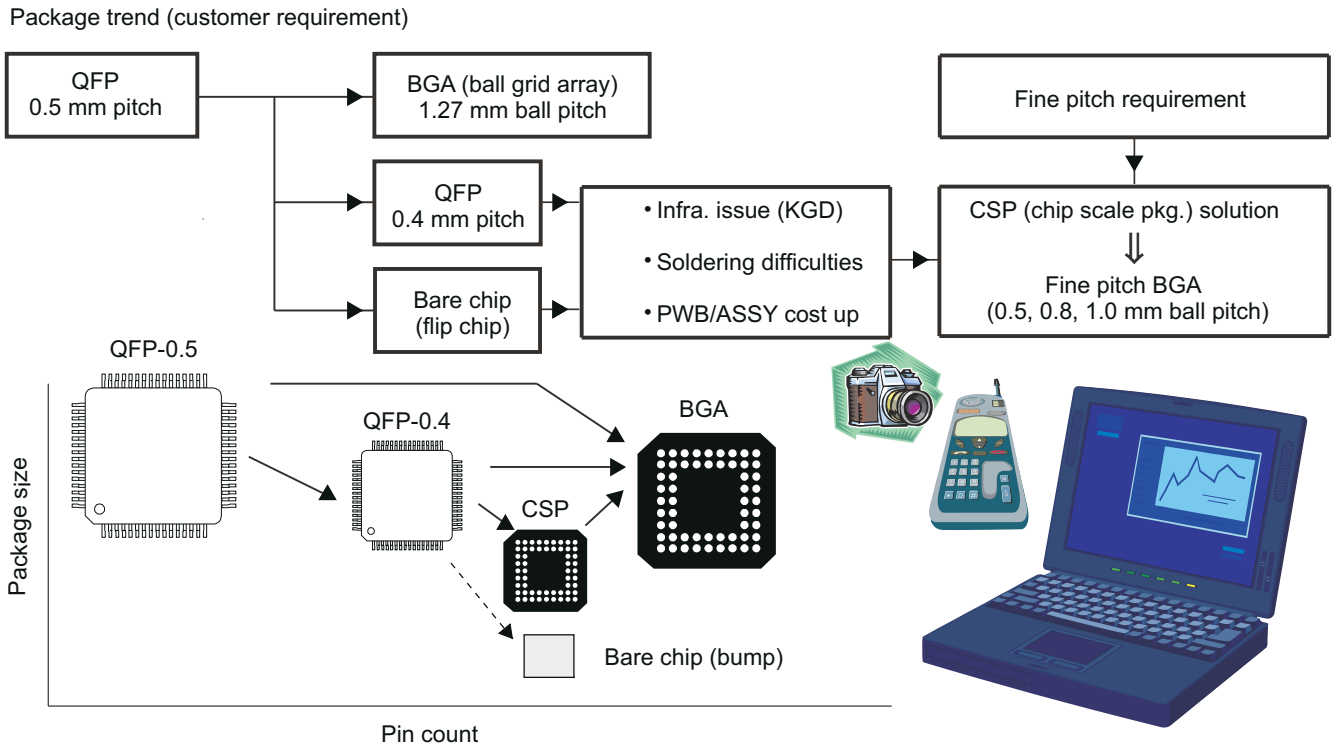

Figure 1-1. Packaging Trends

CSPs are in many ways an ideal solution to the cost reduction and miniaturization requirements. They offer enormous area reductions compared to quad flat packages (QFPs) and have increasing potential to do so without adding to system-level cost. In the best case, CSPs compete today on a cost-per-terminal basis with QFPs. Various CSPs from Texas Instruments (TI) are now available at cost parity with thin QFPs.

Texas Instruments produces a laminate-based family of CSPs known as New Fine Pitch Ball Grid Array packages (also referred to as nFBGA packages). Like most other CSPs, nFBGA packages use solder alloy balls as the interconnect between the package substrate and the board on which the package is soldered. The nFBGA family comes in a range of solder ball pitch, and can accommodate various stacked die configurations, with as many as three die housed in each package. Figure 1-2 shows the structure of TI's nFBGA package.

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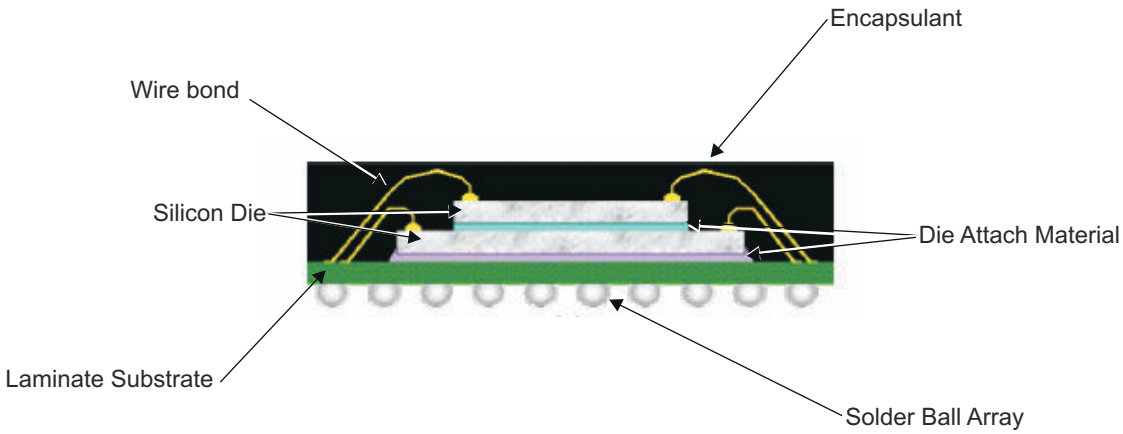

Figure 1-2. Structure of TI's nFBGA Package

TI also offers small body nFBGAs for customers looking to reduce the PCB footprint even further. Structure is nearly identical to that of the standard nFBGA shown in Figure 1-2. The major difference is the package thickness. Standard nFBGAs have a thickness of ~1 mm while the small body variants can range from 0.45-1 mm. This is achieved by using a thinner substrate material and die attach film instead of epoxy.

Package stack up can be minimized even further by using solder bumps rather than the standard BGA solder balls. The reduced height of the bumps allows the smallest possible package height while offering exceptional board level reliability performance. Figure 1-3 shows the structure of TI's small body nFBGAs.

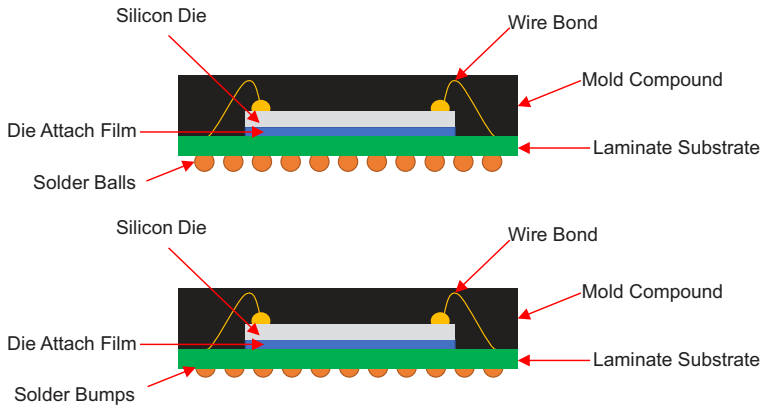

Figure 1-3. Structure of TI's Small Body nFBGA Packages

Texas Instruments addressed several key issues in package assembly to produce a CSP that is not only physically and mechanically stable but cost-effective for a wide variety of applications.

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Figure 1-4 shows a general flow used to produce TI nFBGA packages.

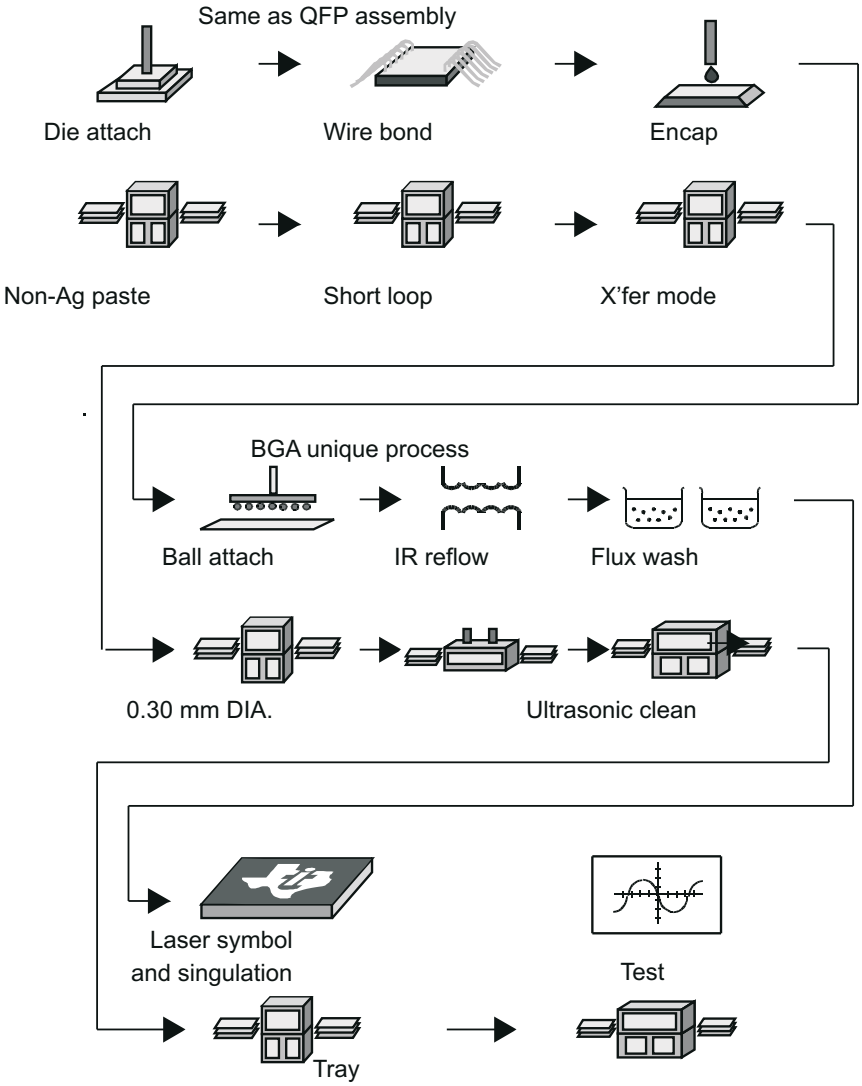

Figure 1-4. nFBGA Package Assembly Flow

The nFBGA package has been fully qualified in numerous applications and is being used extensively in mobile phones, laptops, modems, handheld devices, and office environment equipment. For more information on using reliable and cost-effective nFBGA packaging in your application, contact your local TI field sales office.

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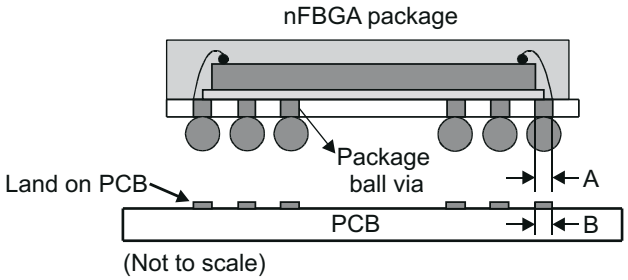
2 PCB Design Considerations

2.1 Solder Land Areas

Designs of both the nFBGA package itself and the printed circuit board (PCB) are important in achieving good manufacturability and optimum reliability. In particular, the diameters of the package vias and the board lands are critical. While the actual sizes of these dimensions are important, their ratio is more critical. Figure 2-1 illustrates the package via-to-PCB configuration and Figure 2-2 illustrates why this ratio is critical.



A = Via diameter on package
B = Land diameter on PCB
Ratio A/B should equal 1.0 for optimum reliability.

Figure 2-1. Package Via to Board Land Area Configuration

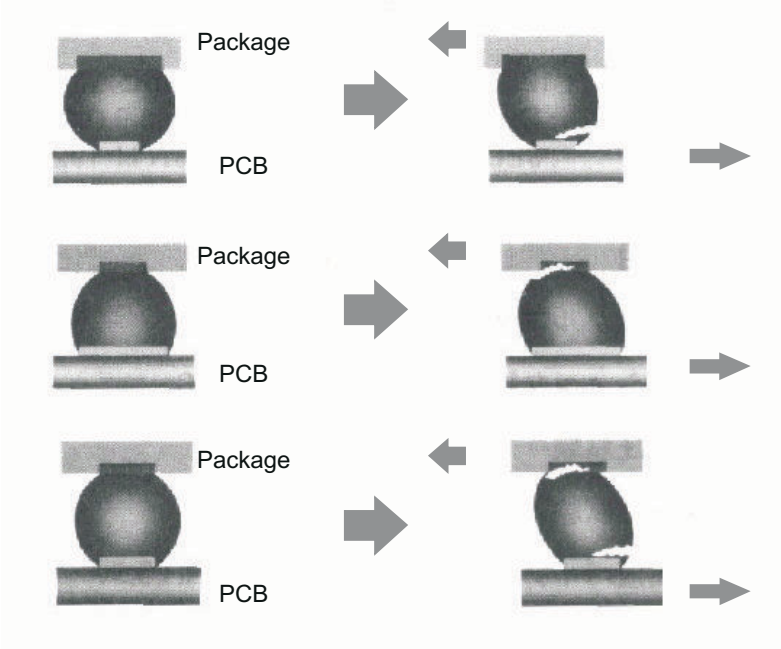


Figure 2-2. Effects of Via-to-Land Ratios

In the top view of Figure 2-2, the package via is larger than the PCB via, and the solder ball is prone to crack prematurely at the PCB interface. In the middle view, the PCB via is larger than the package via, which leads to cracks at the package surface. In the bottom view, where the ratio is almost 1:1, the stresses are equalized and neither site is more susceptible to cracking than the other.

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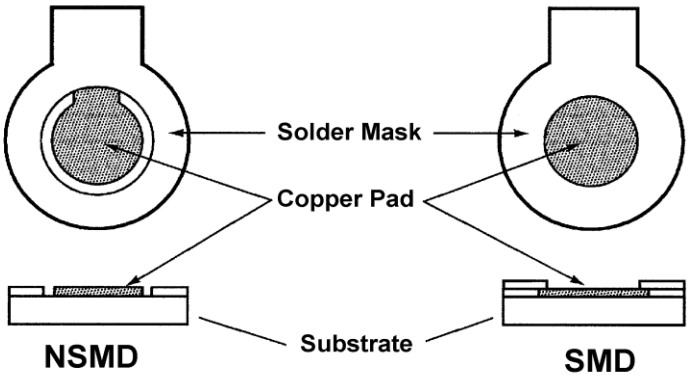
Solder lands on the PCB are generally simple round pads. Solder lands are either solder-mask-defined or non-solder-mask-defined.

- *Solder-mask-defined (SMD) land.* With this method, the copper pad is made larger than the desired land area, and the opening size is defined by the opening in the solder mask material. The advantages normally associated with this technique include more closely controlled size and better copper adhesion to the laminate. Better size control is the result of photo imaging the stencils for masks. The chief disadvantage of this method is that the larger copper spot can make routing more difficult.
- *Non-solder-mask-defined (NSMD) land.* Here, the land area is etched inside the solder mask area. While the size control is dependent on copper etching and is not as accurate as the solder mask method, the overall pattern registration is dependent on copper artwork, which is quite accurate. The tradeoff is between accurate dot placement and accurate dot size.

For an example of optimum land diameters and configurations for a common nFBGA pitch, see Table 2-1.



A. It is not recommended to use "U" shape PCB land because of trapping void during reflow.

Figure 2-3. Optimum Land Configurations

Table 2-1. Optimum Land Configurations

All Measurements in mm		Ball Size, SMO, Pad Size and Apertures are Shown in Diameters				
		PCB Design		Stencil Design		
Ball Pitch	Solder Mask Type	SMO	Pad Size	Thickness	Aperture	Area Aspect Ratio
0.4	SMD	0.225	0.300	0.076	0.250	0.82
	NSMD	0.300	0.225			
0.5	SMD	0.300	0.400	0.100	0.300	0.75
	NSMD	0.400	0.300			
0.65	SMD	0.350	0.450	0.127	0.350	0.69
	NSMD	0.450	0.350			
0.8	SMD	0.400	0.500	0.152	0.400	0.66
	NSMD	0.500	0.400			
1	SMD	0.450	0.550	0.152	0.450	0.74
	NSMD	0.550	0.450			

- Area Ratio = Area of Aperture / Area of Aperture Wall
- For optimal release of solder paste, Area Ratio ≥ 0.66 is recommended.

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2.2 Conductor Width/Spacing

Figure 2-4 presents some design considerations based on commonly used PCB design rules. Conventionally, the pads are connected by wide copper traces to other devices or to plated through holes (PTH). As a rule, the mounting pads must be isolated from the PTH. Placing the PTH interstitially to the land pads often achieves this.

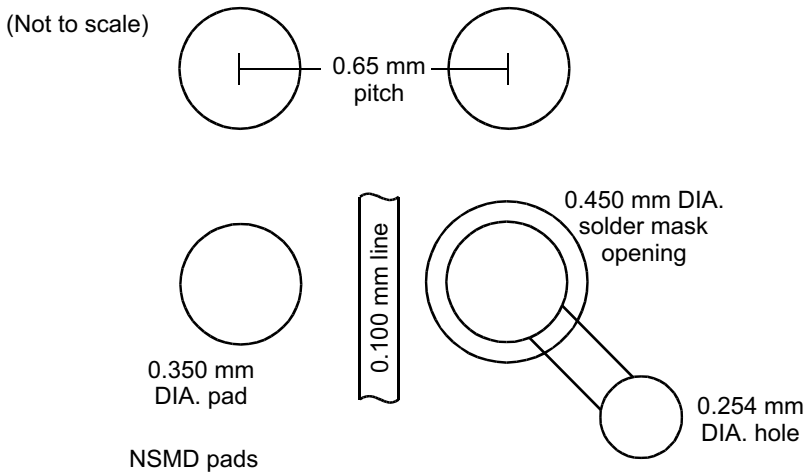

Figure 2-4. PCB Design Considerations (Conventional)

2.3 High-Density Routing Techniques

A challenge when designing with CSP packages is that as available space contracts, the space available for signal fanout also decreases. Routing of nFBGA packages can be especially challenging because of the tight ball pitch and a full array of solder balls that most packages have. By using a few high-density routing techniques, the PCB designer can minimize many of these design and manufacturing challenges.

2.4 Via Density

Via density, as mentioned earlier, can be a limiting factor when designing high-density boards. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the routability of the board by requiring less board space and increasing via density. The invention of the microvia, shown in Figure 2-5, has solved many of the problems associated with via density.

Figure 2-5. Microvia Structure

Microvias are often created using a laser to penetrate the first few layers of dielectric. The laser can penetrate a 4-mil-thick dielectric layer, creating the 4 µm microvia shown in Figure 2-5. The layout designer can now route to the first internal board layer. Two layers (each 4 mils thick) can be laser-drilled, creating a 200 µm microvia diameter. In this case, routing to the first two internal layers is possible.

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2.5 Conventional PCB Design

The relatively large via density on the package periphery, mentioned earlier, is caused by limited options when routing the signal from the ball. To reduce or eliminate the via density problem on the periphery of the package, designers can build the PCB vertically from the BGA pad through the internal layers of the board, as shown in Figure 2-6. By working vertically and mechanically drilling 250 µm vias between the pads on the board and the internal layers, designers can create a “pick-and-choose” method. They can pick the layer and choose the route. A “dog bone” method is used to connect the through-hole via and the pad. This reduces the risk of trapped voids that can reduce the board mount process margin.

This method requires a very small mechanical drill to create the necessary number of vias for one package. Although this method is the least expensive, a disadvantage is that the vias go through the board, creating a matrix of vias on the bottom side of the board, which may limit the use of using the back side for routing.

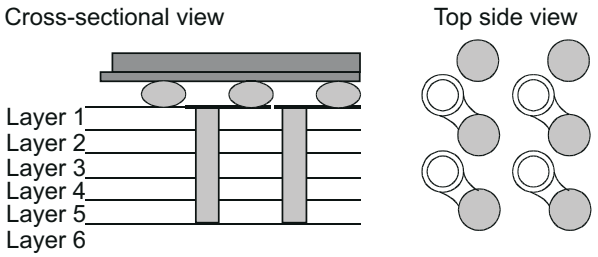

Figure 2-6. "Dog Bone" Via Structure

2.6 Advanced Design Methods

Another option is to use a combination of blind and buried vias. Blind vias connect either the top or bottom side of the board to inner layers. Buried vias usually connect only the inner layers. Figure 2-7 illustrates this method using 4-mil laser-drilled microvias in the center of the pads and burying the dog bone on layer 2.

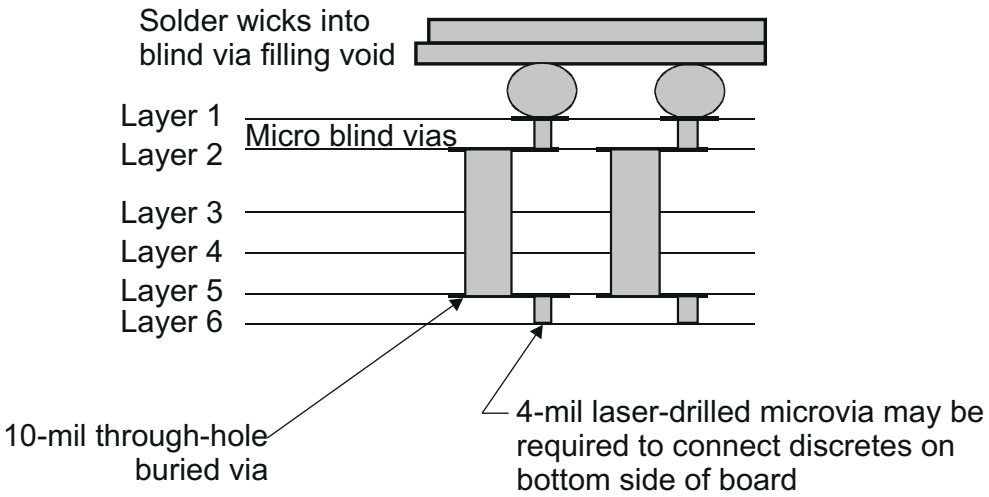

Figure 2-7. Buried Vias

Since the buried via does not extend through the underside of the board, the designer can use another set of laser-drilled blind microvias, if needed, to connect the bypass capacitors and other discrete components to the bottom side.

More information on these advanced techniques is available by contacting your local TI field sales office.

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3 Reliability

Reliability is one of the first questions designers ask about any new packaging technology. They want to know how well the package will survive handling and assembly operation, and how long it will last on the board. The elements of package reliability and system reliability, while related, focus on different material properties and characteristics and are tested by different methods.

Package reliability focuses on materials of construction, thermal flows, material adherence/delamination issues, resistance to high temperatures, moisture resistance and ball/stitch bond reliability. Thorough engineering of the package is performed to prevent delamination caused by the interaction of the substrate material and the mold compound.

TI subjects each nFBGA to rigorous qualification testing before the package is released to production. These tests are summarized in Table 3-1. All samples used in these tests are preconditioned according to guidelines of the Joint Electronic Device Committee (JEDEC) A113 at various levels. Typical data is presented in Table 3-2. The nFBGA packages have proven robust and reliable.

Table 3-1. Package-Level Reliability Tests

Test Environments	Conditions	Read Points
HAST	85RH/85°C	600 hrs., 1000 hrs.
Temp. Cycle	-55/125°C	500 cycles, 750 cycles, 1000 cycles
Thermal Shock	-55/125°C	200 cycles, 500 cycles, 750 cycles, 1000 cycles
HTOL	125°C, Op. voltage	500 hrs., 600 hrs., 1000 hrs.
HTOL(1)	140°C, Op. voltage	500 hrs.
HTOL(1)	140°C, Op. voltage	500 hrs.
Bake(1)	150°C, 170°C	600 hrs., 1000 hrs., 420 hrs.
HAST(1)	170°C	96 hrs.

(1) Optional tests. One or more of them may be added to meet customer requirements.

Table 3-2. Package-Level Reliability Test Results

		Package Types		
	Leads	113ZVD	289ZVL	289ZWE
	Body (mm)	8x8	12x12	13x13
	Die (mm)	4.2 × 4.2	5.8 × 5.7	10.6 × 8.2 (Die 1) 8.1 × 7.7 (Die 2)
	Level	3	3	3
Test Environment				
T/C, -55/125°C	(500 cycles) (1000 cycles)	0/78 0/78	0/83 0/83	0/246 0/245
T/S, -55/125°C	(500 cycles) (1000 cycles)		0/77 0/77	0/77 0/77
HAST, 85°C/85%RH	(600 cycles) (1000 cycles)	0/78 0/78	0/78 0/78	0/77 0/77
150°C Storage	(600 cycles) (1000 cycles)	0/45 0/45	0/77 0/77	0/77 0/77
HTOL	(1000 hrs.)	0/120		

Board-level reliability (BLR) issues generally focus on the complex interaction of various materials under the influence of heat generated by the operation of electronic devices. Not only is there a complex thermal situation caused by multiple heat sources, but there are cyclical strains due to expansion mismatches, warping and transient conditions, non-linear material properties, and solder fatigue behavior influenced by geometry, metallurgy, stress relaxation phenomenon, and cycle conditions. In addition to material issues, board and package design can influence reliability. Thermal management from a system level is critical for optimum reliability, and thermal cycling tests are generally used to predict behavior and reliability. Many of these are used in conjunction with solder fatigue life models using a modified Coffin-Manson strain range-fatigue life plots (number of cycles to failure has an inverse exponential relationship with the thermal cycle temperature range).

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In addition to device/package testing, board-level reliability testing has been extensively performed on the nFBGA packages. Various types of daisy-chained packages were assembled to special boards, with electrical measurements made in the initial state and then at intervals after temperature cycles were run. Table 3-3 shows a summary of a wide range of board-level reliability.

Table 3-3. Board-Level Reliability Summary

Conditions (With Solder Paste)						Failures/Sample Size						
						Requirements			Extended Range			
Package	TI Mfg Site	Body	Pitch	Die	Temp.	500	800	1000	1500	2000	2500	3000
	Test Site	(mm)	(mm)	(mm)	Cycle (°C)	(Cycles)			(Cycles)			
ZVD 113 balls	TI Hiji	8×8	0.65	5x5	-40/125	0/36	0/36	0/36	0/36	0/36	0/36	0/36
ZVD 113 balls	TI Hiji	8×8	0.65	4.2x4.2	-40/125	0/48	0/48	0/48	0/48	0/48	0/48	4/43
ZVD 289 balls	TI Hiji	12×12	0.50	9x9	-40/125	0/95	0/95	0/95	0/95	0/95	0/94	0/94
ZVD 289 balls	TI Hiji	12×12	0.50	6.5x6.5	-40/125	0/36	0/36	0/36	0/36	0/36	0/36	1/36
ZWA 11 Balls	TI Phi	2x 1.4	0.4	1x0.6	-40/85	0/33	0/33	0/33	0/33	0/33	0/33	0/33

Table 3-4 summarizes conclusions from the testing. Two important conclusions are that the PCB pad size needs to match the via size, and that solder paste is needed for attachment to give optimal reliability.

Table 3-4. Summary of Significant BLR Improvements

Condition	Improved BLR →		
Die size	Larger	→	Smaller
Die edge	Over balls	→	Within ball matrix
Ball count	Smaller	→	Larger
Ball size	Smaller	→	Larger
PCB pad size	Over/undersized	→	Matches package via (for NSMD ~90% of via)
Solder paste	None or insufficient	→	Thickness 0.10 nom. (type matches reflow)

3.1 Reliability Calculations

Another important aspect of predicting how a package will perform in any given application is reliability modeling. Thermal, electrical, and thermomechanical modeling, verified by experimental results, provide insight into system behavior, shorten package development time, predict system lifetimes, and provide an important analytical tool. In applications such as BGAs, where the interconnections are made through solder balls, the useful life of the package is, in most cases, dependent on the useful life of the solder itself. This is an area that has been studied extensively, and very accurate models for predicting both solder behavior and interpreting accelerated life testing exist.

The current methodology employed at Texas Instruments includes both extensive model refinement and constant experimental verification. For a given package, a detailed 2D finite element model (FEM) is constructed. This model is used to carry out 2D plain strain elastoplastic analysis to predict areas of high stress. These models also account for the thermal variation of material properties, such as modulus of elasticity, coefficient of thermal expansion, and Poisson's Ratio as a function of temperature. These allow the FEM to calculate the thermomechanical plastic strains in the solder joints for a given thermal loading.

The combination of finite element analysis (FEA), accurate thermal property information, and advanced statistical methods allows prediction of the number of cycles to failure for various probability levels. Using the assumption that cyclic fatigue lifetime follows a Weibull distribution, various probability levels can be calculated. For these calculations, the Weibull shape parameter used is $\beta = 4$, which is based on experimental data calibration. It is also consistent with available experimental data found in the literature for leadless packages. This then results in Equation 1.

$$Nf(\times\%) = Nf(50\%)[\ln(1-0.01\times)/\ln(0.5)]1/\beta \quad (1)$$

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Using Equation 1, and using the plastic strain ξp in combination with the S–N curves, the data below is an example of the accuracy possible with this method:

Sample Finite Element Simulation and Life Prediction:

144 GGU @ T/C: -40/125°C

{Model}→ ξp = 0.353% on the outmost joint → Nf(50%)= 4434 cycles

→ Nf(1%) = 1539 cycles

{BLR Testing}→ -40/125°C (10 min/10 min)

→ Nf(1%) = 1657 cycles

Modeling is most useful in exploring changes in materials, designs, and process parameters without the need to build experimental units. For example, modeling was used to study the effects of changes in board thickness and pad size. Table 3-5 shows the simulated effects of pad size and board thickness on the fatigue life of a 144-GGU package.

Table 3-5. Effects of Pad Size and Board Thickness on Fatigue Life

Example1: Effects of pad size on fatigue life • **Package: 144 GGU** • **Die: 8.8 x 8.8 x 0.279 mm** • **Board: FR-4 board 52 mils thick**	**Pad Dia. (mils)**	**Pad Standoff (mm)**	**Solder Center Dia. (mm)**	**Plastic Strain (%)**	**Nf (1%) (cycles to failure)**	**Difference**
	12	0.3847	0.4908	0.4400	998	0.88x
	13	0.3689	0.4951	0.4127	1134	1
	14	0.3523	0.5005	0.3908	1263	1.11x
	15	0.3350	0.5060	0.3741	1377	1.21x
Example 2: Effects of board thickness on fatigue life • Package: 144 GGU • Die: 8.8 x 8.8 x 0.279 mm • Board: FR-4 • Pad Size: 13 mils	**Board Thickness (mils)**	**Plastic Strain (%)**	**Nf (1%) (cycles to failure)**	**Difference**		
	50	0.4095	1152	1		
	31	0.4095	1249	1.08x		

3.2 Package Characteristics

Texas Instruments has extensive package characterization capabilities, including an electrical measurements lab with TDR/LRC (Time Domain Reflectometer/inductance resistance capacitance) and network analysis capabilities, a thermal measurements lab with JEDEC standard test conditions up to 1000 watts, and extensive electrical, thermal, and mechanical modeling capability. Modeling was implemented at TI starting in 1984. Stress analysis is done with the Ansys Analysis tool, which provides full linear, nonlinear, 2D and 3D capabilities for solder reliability, package warpage, and stress analysis studies. An internally developed tool (PACED™) is used for electrical modeling that gives 2.5D and full 3D capability for LRC models, transmission lines, lossy dielectrics, and SPICE deck outputs. The thermal modeling tool was also internally developed (ThermCAL™) and it provides full 3D automatic mesh generation for most packages.

Complex geometries, transient analysis, and anisotropic materials can be modeled with it. With these capabilities, a full range of modeling from device level through system level can be provided. Package modeling is used to predict package performance at the design stage, to provide a package development tool, to aid qualification by similarity, and as a failure analysis tool.

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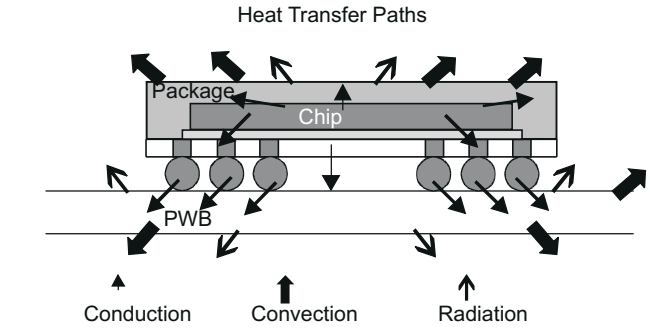
3.3 Thermal Modeling

Figure 3-1 outlines the thermal modeling process. Thermal modeling data for sample nFBGA packages can be found in Appendix C.



(TQFP shown for illustration purposes)

Model's three heat-transfer mechanisms:
- Conduction
- Convection
- Radiation

Method:
- Define solid
- Mesh solid
- Solve large number of simultaneous equations relating each defined mesh point to each other

Sources of error:
- Convection coefficients
- Material properties
- Solid definition inaccuracies

Figure 3-1. Thermal Modeling Process

4 Surface-Mounting nFBGA Packages

Surface-mount technology (SMT) has evolved over the past decade from an art into a science with the development of design guidelines and rules. While these guidelines are specific enough to incorporate many shared conclusions, they are general enough to allow flexibility in board layouts, solder pastes, stencils, fixturing, and reflow profiles. From experience, most assembly operations have found nFBGA packages to be robust, manufacturing-friendly packages that fit easily within existing processes and profiles. In addition, they do not require special handling. However, as ball pitch becomes smaller, layout methodology and placement accuracy become more critical. Below is a review of the more important aspects of surface-mounted CSPs. The suggestions provided may aid in efficient, cost-effective production.

4.1 Design for Manufacturability (DFM)

A well-designed board that follows the basic surface-mount technology considerations greatly improves the cost, cycle time, and quality of the end product. Board designers should comprehend the SMT-automated equipment used for assembly, including minimum and maximum dimensional limits and placement accuracy. Many board shapes can be accommodated, but the front of the board should have a straight and square edge to help machine sensors detect it. While odd-shaped or small boards can be assembled, they require panelization or special tooling to process in-line. The more irregular the board — non-rectangular with no cutouts — the more expensive the assembly cost.

Fiducials (the optical alignment targets that align the module to the automated equipment) should allow vision-assisted equipment to accommodate the shrink and stretch of the raw board during processing. They also define the coordinate system for all automated equipment, such as printing and pick-and-place.

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The following guidelines may be helpful:

- Automated equipment requires a minimum of two and preferably three fiducials.
- A wide range of fiducial shapes and sizes can be used. Among the most useful is a circle 1.6 mm in diameter with an annulus of 3.175/3.71 mm. The outer ring is optional, but no other feature may be within 0.76 mm of the fiducial.
- The most useful placement for the fiducials is an L configuration, which is orthogonal to optimize the stretch/shrink algorithms. When possible, the lower left fiducial should be the design origin (coordinate 0,0).
- All components should be within 101.6 mm of a fiducial to assure placement accuracy. For large boards or panels, a fourth fiducial should be added.

If the edges of the boards are to be used for conveyer transfer, a cleared zone of at least 3.17 mm should be allowed. Normally, the longest edges of the board are used for this purpose, and the actual width is dependent on equipment capability. While no component lands or fiducials can be in this area, breakaway tabs may be.

Interpackage spacing is a key aspect of DFM, and the question of how close you can safely put components to each other is a critical one. The following component layout considerations are recommendations based on TI experience:

- There should be a minimum of 0.508 mm between land areas of adjacent components to reduce the risk of shorting.
- The recommended minimum spacing between SMD discrete component bodies is equal to the height of the tallest component. This allows for a 45° soldering angle in case manual work is needed.
- Polarization symbols need to be provided for discrete SMDs (diodes, capacitors, and so forth.) next to the positive pin.
- Pin-1 indicators or features are necessary to determine the keying of SMD components.
- Space between lands (under components) on the backside discrete components should be a minimum of 0.33 mm. No open vias may be in this space.
- The direction of backside discretes for wave solder should be perpendicular to the direction through the wave.
- Do not put SMT components on the bottom side that exceed 200 grams per square inch of contact area with the board.
- If space permits, symbolize all reference designators within the land pattern of the respective components.
- It is preferable to have all components oriented in well-ordered columns and rows.
- Group similar components together whenever possible.
- Room for testing must be allowed.

4.2 Solder Paste

TI recommends the use of paste when mounting nFBGAs. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- It helps compensate for minor variations in the planarity of the solder balls.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.

Paste selection is normally driven by overall system assembly requirements. In general, the “no clean” compositions are preferred due to the difficulty in cleaning under the mounted component. Most assembly operations have found that no changes in existing pastes are required by the addition of nFBGA, but due to the large variety of board designs and tolerances, it is not possible to say this will be true for any specific application.

Nearly as critical as paste selection is stencil design. A proactive approach to stencil design can pay large dividends in assembly yields and lower costs. In general, nFBGA packages are special cases of BGA packages, and the general design guidelines for BGA package assembly applies to them as well. There are some excellent papers on BGA assembly, so only a brief overview of issues especially important to nFBGA packages is presented here.

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The typical stencil hole diameter should be the same size as the land area, and 100-120-µm-thick stencils have been found to give the best results. Good release and a consistent amount of solder paste and shapes are critical, especially as ball pitches decrease. The use of metal squeegee blades, or at the very least, high durometer polyblades, is important in achieving this. Paste viscosity and consistency during screening are some variables that require close control.

4.3 Solder Ball Collapse

To produce the optimum solder joint, it is important to understand the amount of collapse of the solder balls, and the overall shape of the joint. These are a function of:

- The diameter of the package solder ball via.
- The volume and type of paste screened onto the PCB.
- The diameter of the PCB land.
- The board assembly reflow conditions.
- The weight of the package.

The original ball height on the package for a typical 0.5-mm-pitch package is 0.20 mm. After the package is mounted, this typically drops to 0.15 mm, as illustrated in Figure 4-1.

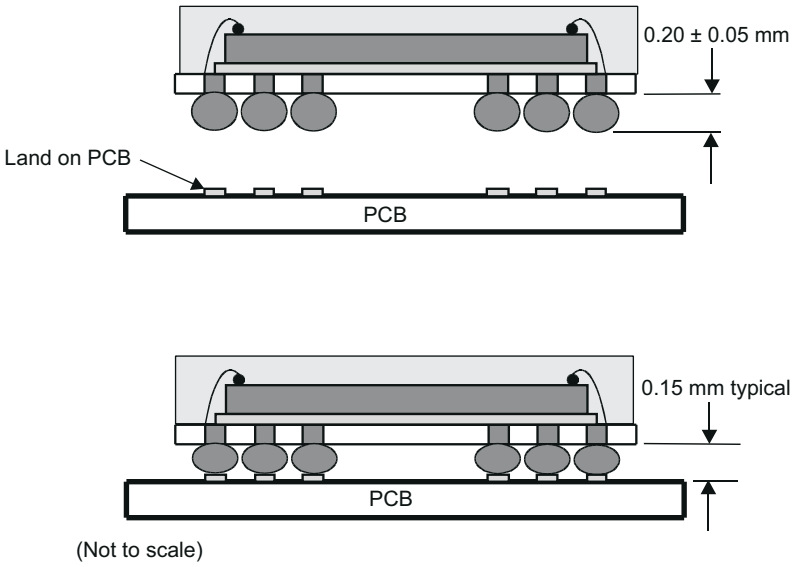

Figure 4-1. Solder Ball Collapse

Controlling the collapse, and thus defining the package standoff, is critical to obtaining the optimum joint reliability. Generally, a larger standoff gives better solder joint fatigue strength, but this should not be achieved by reducing the board land diameter. Reducing the land diameter will increase the standoff, but will also reduce the minimum cross-section area of the joint. This, in turn, will increase the maximum shear force at the PCB side of the solder joint. Therefore, a reduction of land diameter will normally result in a worse fatigue life, and should be avoided unless all the consequences are well understood.

4.4 Reflow

Solder reflow conditions are the next critical step in the mounting process. During reflow, the solvent in the solder paste evaporates, the flux cleans the metal surfaces, the solder particles melt, wetting of the surfaces takes place by wicking of molten solder, the solder balls collapse, and finally solidification of the solder into a strong metallurgical bond completes the process. The desired end result is a uniform solder structure strongly bonded to both the PCB and the package with small or no voids and a smooth, even fillet at both ends. Conversely, when all the steps do not carefully fit together, voids, gaps, uneven joint thickness, discontinuities, and insufficient fillet can occur. While the exact cycle used depends on the reflow system and paste composition, there are several key points all successful cycles have in common.

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The first of these is a warm-up period sufficient to safely evaporate the solvent. This can be done with a pre-heat or a bake, or, more commonly, a hold in the cycle at evaporation temperatures. If there is less solvent in the paste (such as in a high-viscosity, high-metal-content paste), then the hold can be shorter. However, when the hold is not long enough to get all of the solvent out or too fast to allow it to evaporate, many negative things happen. These range from solder-particle splatter to trapped gases, which can cause voids and embrittlement. A significant number of reliability problems with solder joints can be solved with the warm-up step, so it needs careful attention.

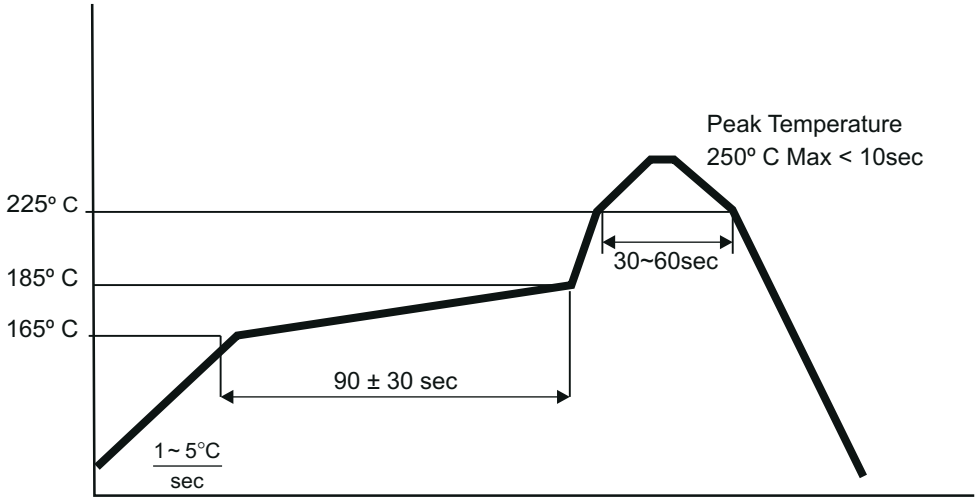
The second key point that successful reflow cycles have in common is uniform heating across the package and the board. Uneven solder thickness and non-uniform solder joints may be an indicator that the profile needs adjustment. There can also be a problem when different sized components are reflowed at the same time. Care needs to be taken when profiling an oven to be sure that the indicated temperatures are representative of what the most difficult to reflow parts are seeing. These problems are more pronounced with some reflow methods, such as infrared (IR) reflow, than with others, such as forced hot-air convection.

Finally, successful reflow cycles strike a balance among temperature, timing, and length of cycle. Mistiming may lead to excessive fluxing activation, oxidation, excessive voiding, or even damage to the package. Heating the paste too hot, too quickly before it melts can also dry the paste, which leads to poor wetting. Process development is needed to optimize reflow profiles for each solder paste/flux combination.

The profile shown in Figure 4-2 is an ideal one for use on a Pb-Free nFBGA package in a forced-air-convection furnace, which is the most highly recommended type. The best results have been found in a nitrogen atmosphere. The corresponding optimal reflow profile for an nFBGA package exhibiting eutectic SnPb solder balls is shown in Figure 4-3.

The guidelines upon which these profiles are based are general. Modification to the ideal reflow profile will be driven by the interplay of solder-paste particle size and flux percentage with process variables such as heating rates, peak temperatures, board construction factors, and atmosphere. These modifications are dependent on specific applications.

It should be noted that while they are more rugged than most CSP-type packages, many nFBGA packages are still slightly moisture-sensitive at the time of publishing this application report. The time out of a dry environment should be controlled according to the label on the packing material. This will prevent moisture absorption problems with the package such as “popcorning,” or delamination.



RT to 150 ± 10C	$\frac{1\sim 5°C}{sec}$
175 ± 10C	90 ± 30 sec
225°C	30 ~ 60 sec
245 ~ 250°C peek	10 sec

Figure 4-2. Recommended Reflow Profile of Pb-Free nFBGA Package

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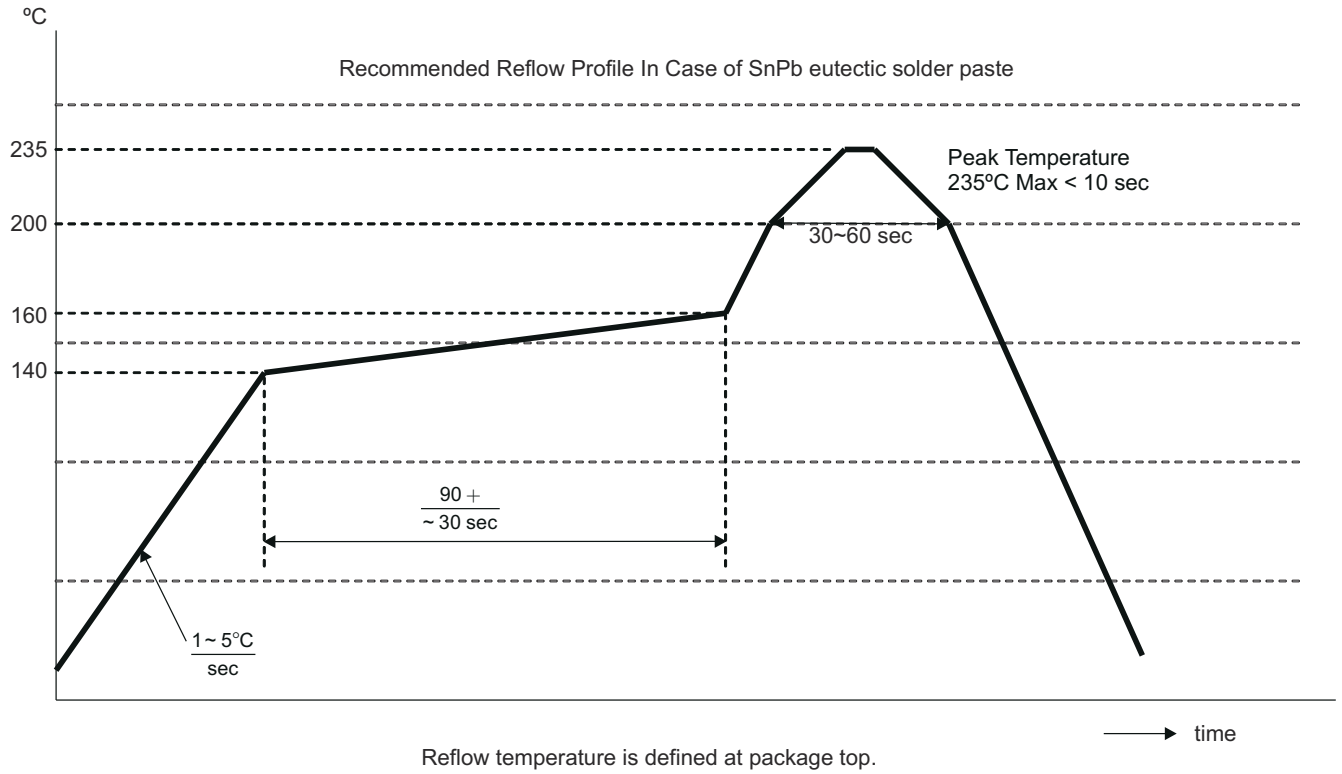

Figure 4-3. Recommended Reflow Profile of Eutectic SnPb nFBGA Package

Other concerns with BGA packages are those caused by a PCB bowing or twisting during reflow. As PCBs get thinner, these problems will become more significant. Potential problems from these effects will show up as open pins, hourglass solder joints, or solder discontinuities. Proper support of the PCB through the furnace, balancing the tab attachments to a panel, and, in worst cases, using a weight to stiffen the PCB can help prevent this. In general, the small size of CSPs create fewer problems than standard BGAs. It is also true that BGAs generally have fewer problems than leaded components.

4.5 Inspection

The nFBGA packages have been designed to be consistent with very high-yield assembly processes. Because of their relatively light weight, nFBGA packages tend to self-align during reflow. Since the pitch of the ball pattern is large compared to that of fine-pitch leaded packages, solder bridging is rarely encountered. It is recommended that a high-quality solder joint assembly process be developed using the various inspection and analytical techniques, such as cross-sectioning. Once a quality process has been developed, detailed inspection should not be necessary. Visual methods, while obviously limited, can offer valuable clues to the general stability of the process. Electrical checks can confirm interconnection. Both transmission X-rays and laminographic X-rays have proven to be useful nondestructive tools, if desired.

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5 Packing and Shipping

The nFBGA packages are shipped in either of two packing methods:

- Trays
- Tape and Reel

5.1 Tray Packing Method

Thermally resistant plastic trays are one of the two methods currently used to ship these packages. Each family of parts with the same package outline has its own individually designed tray. The trays are designed to be used with pick-and-place machines. Figure 5-1 gives typical tray details. Tray packaging is used in compliance with JDEC standards.

The steps in Figure 5-2 illustrate the packing method used to ship trays. Before the trays are sealed in the aluminum lined plastic bag, they are baked in accordance with the requirements for dry-packing at the appropriate level.

Figure 5-1. Shipping Tray Detail

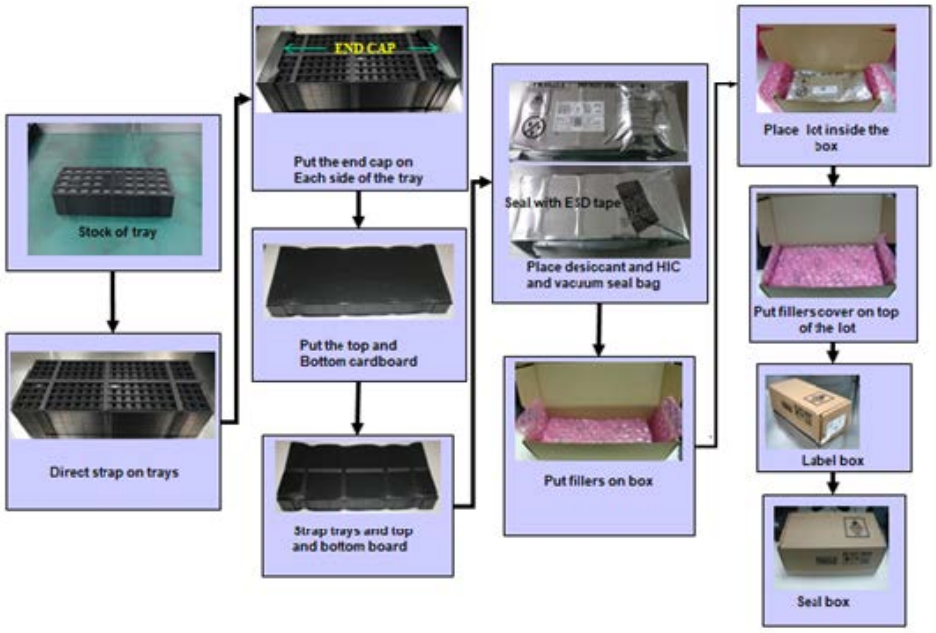

Figure 5-2. Steps of Packing Method for Ship in Trays

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5.2 Tape-and-Reel Packing Method

The embossed tape-and-reel method is generally preferred by automatic pick-and-place machines, although trays remain an option for those customers who prefer them for nFBGA packages. The tape is made from an antistatic/conductive material. The cover tape, which peels back during use, is heat-sealed to the carrier tape to keep the devices in their cavities during shipping and handling. The tape-and-reel packaging used by Texas Instruments is in full compliance with EIA Standard 481-A, "*Taping of Surface-Mount Components for Automatic Placement*." The static-inhibiting materials used in the carrier-tape manufacturing provide device protection from static damage, while the rigid, dust-free polystyrene reels provide mechanical protection and clean-room compatibility with dereeling equipment currently available on most high-speed automated placement systems.

5.3 Tape Format

Typical tape format is shown in Figure 5-5. The variables used in Figure 5-3 and Table 5-1 are defined as follows: W is the tape width; P is the pocket pitch; and F is the distance between the drive hole and the centerline of the pocket.

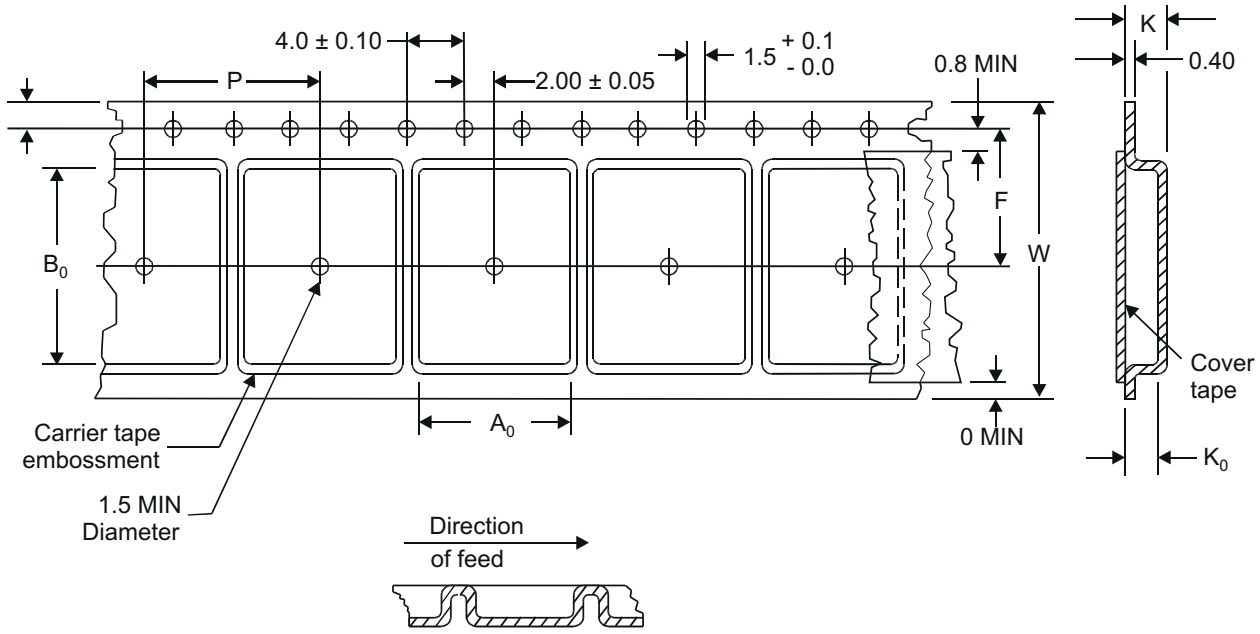

Figure 5-3. Single Sprocket Tape Dimension

Table 5-1. Tape Dimensions

Tape Width (W)	Pocket Pitch (P)	Centerline to Drive Hole (F)	Package Size(1)
16	8	7.5	6 × 6
16	12	7.5	8 × 8
24	16	11.5	10 × 10
24	16	11.5	12 × 12
24	16	11.50	13 × 13
24	24	11.50	14 × 14
8	4	3.5	2 × 1.4
8	4	3.5	2 × 2.5
12	4	5.5	2.45 × 2.45
12	4	5.5	2.5 × 3

(1) All dimensions are in millimeters.

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The reels are shown in Figure 5-4. In this figure, G is the width of the tape, N is the diameter of the hub, and T is the total reel thickness.

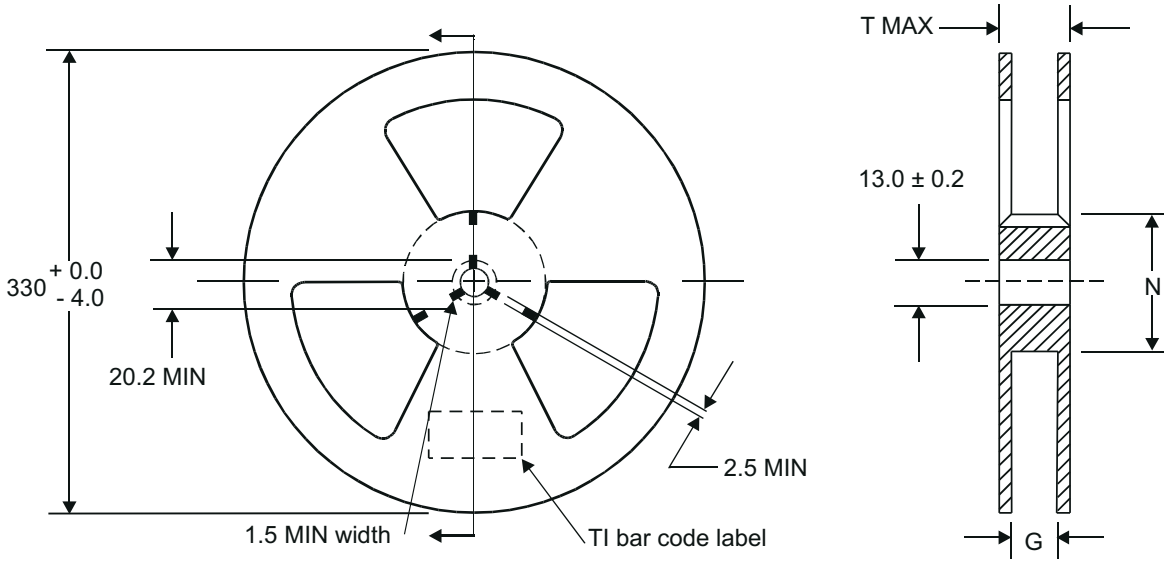

Figure 5-4. Reel Dimensions

Table 5-2. Reel Dimensions(1)

Tape Width (G)	Parts per Reel
16	2500
24	1000

(1) After the parts are loaded into the reel, each individual reel is packed in its own “pizza” box for shipping, as shown in Figure 5-5.

After the parts are loaded into the reel, each individual reel is packed in its own “pizza” box for shipping, as shown in Figure 5-5.

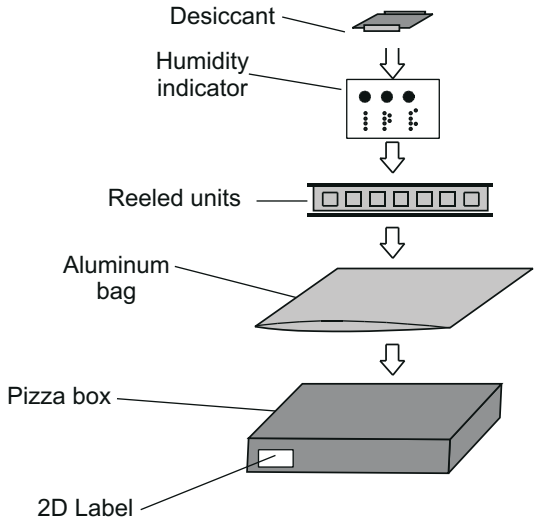

Figure 5-5. Tape-and-Reel Packing

5.4 Device Insertion

Devices are inserted toward the outer periphery of the tape by placing the side with the device name face up and the side with the balls attached face down. The pin-1 indicator is placed in the top left-hand corner of the pocket, next to the sprocket holes.

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5.5 Packaging Method

For reels, once the taping has been completed, the end of the leader is fixed onto the reel with tape. The product name, lot number, quantity, and date code are recorded on the reel and the cardboard box used for tape delivery. Each reel is separately packed in a cardboard box for delivery.

Trays are packed with five loaded trays and one empty tray on top for support and to keep packages secure. The stack is secured with stable plastic straps and sealed in a moisture-proof bag.

Customer-specific bar code labels can be added under request or general purchasing specification.

Moisture-sensitive packages are baked before packing and are packed within 8 hours of coming out of the oven. Both the tape-and-reel and the tray moisture-proof bags are sealed and marked with appropriate labeling warning that the packages inside the bags are dry-packed and giving the level of moisture sensitivity.

6 Sockets

6.1 The Design Challenge

The fine pitch of nFBGA packages makes socketing a special challenge. Mechanical, thermal, and electrical issues must be accommodated by the socket designer. The size of a specific package within the TI nFBGA family is based on the package construction, and is independent of die size. Therefore, a range of die sizes and I/Os within a family will have the same package dimensions. Each different family has a specific I/O pitch and array. For maximum socket versatility, an adapter or “personalizer” can be customized for each application, allowing a single-socket body to be used with many packages. This feature is especially useful in the early days as the technology is being developed and adopted as well as during volume production phase to minimize socket costs.

6.2 Contacting the Ball

A number of different approaches for contacting the solder ball are shown schematically in Figure 6-1. The pinch style contact has been used extensively for contacting solder balls in conventional BGAs and is starting to be proposed also for the most advanced fine pitch CSP packages.

The most common methods used for contacting as small as 0.4 mm pitch CSP packages are either metal pinch (a) or metal (f). Both methods provide the most reliable solutions with less ball deformation and small socket form factor at an affordable cost. Texas Instruments Interconnect Business Unit (TI IBU) has designed both pinch and micro tuning fork (metal type) contacts that satisfy all of these requirements. Further information on the availability of these sockets can be obtained from your local TI Field Sales representative.

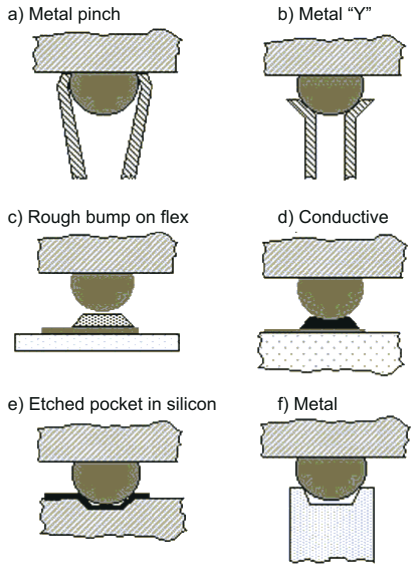

Figure 6-1. Approaches for Contacting the Solder Ball

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6.3 Pinch Contact

The contact is designed to grip the solder ball with a pinching action. This not only provides electrical contact to the solder ball but also helps retain the package in the socket. The contact is shown in Figure 6-2. It was made using a beryllium copper alloy. This alloy is used for spring applications that are exposed to high stresses and temperatures because of its excellent stress relaxation performance and formability.

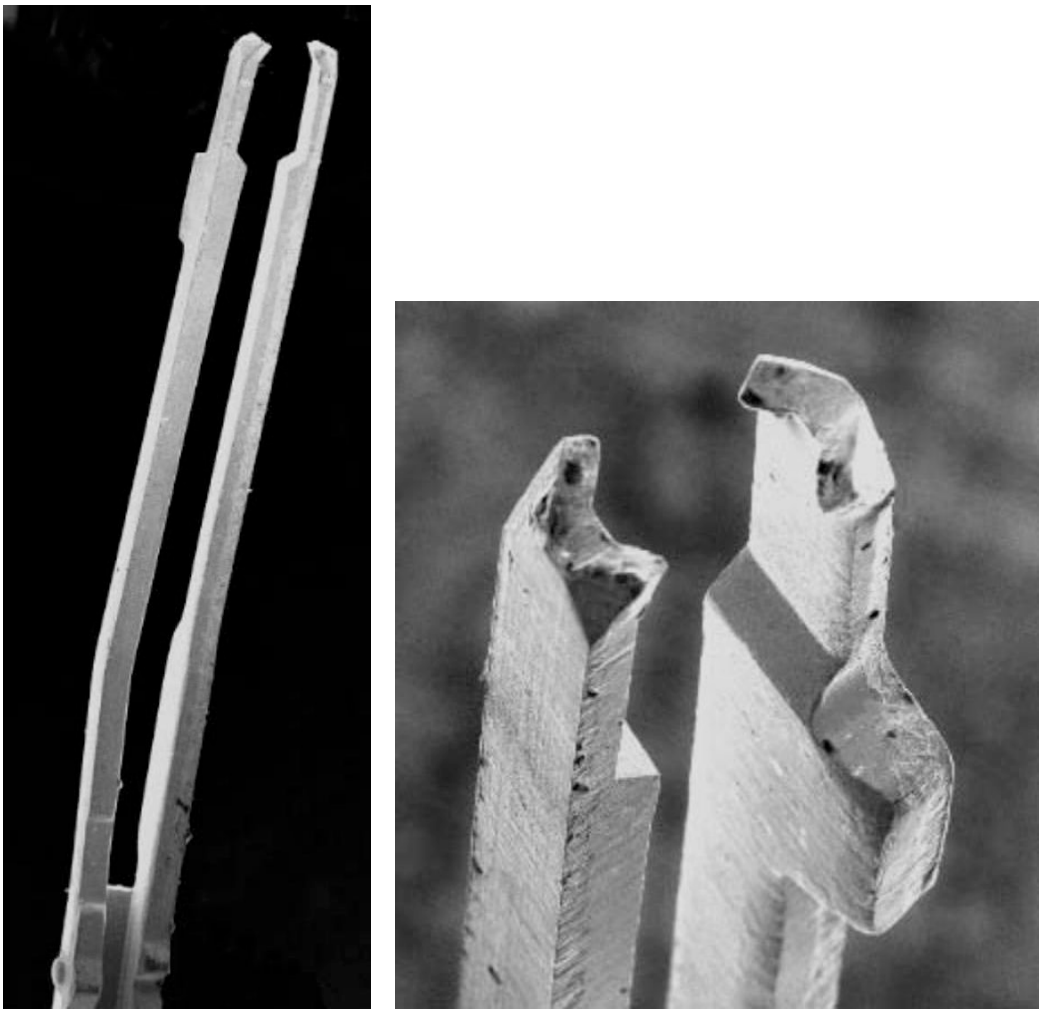

Figure 6-2. Pinch Contact for Solder Ball

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Each contact incorporates two beams that provide an oxide-piercing interface with the sides of the balls above the central area—the equator. No contact is made on the bottom of the solder ball so the original package planarity specifications are unchanged. A photo-micrograph of the contact touching the solder balls is shown in Figure 6-3.

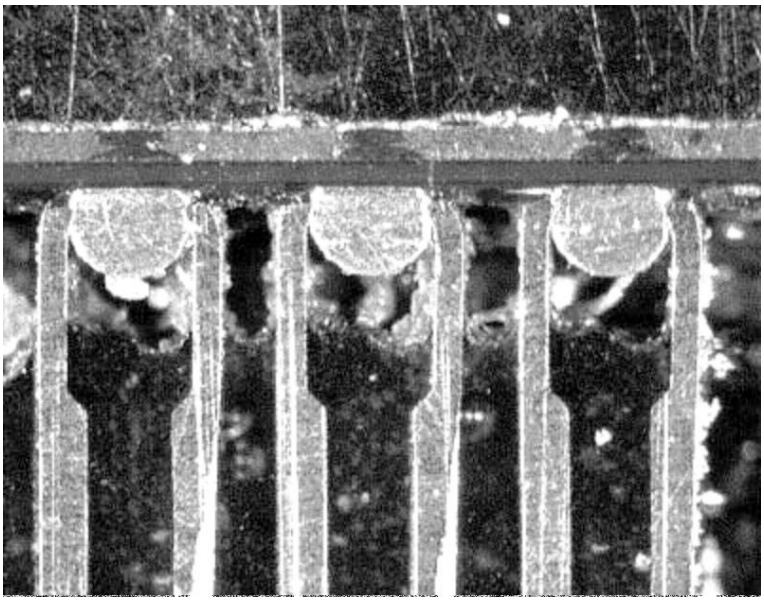

Figure 6-3. Contact Area on Solder Ball

The witness marks left on the solder ball from the contact are shown in Figure 6-4. This ball was contacted at room temperature and it is clear that there was no damage to the bottom of the ball or any witness marks from the contact above the equator.

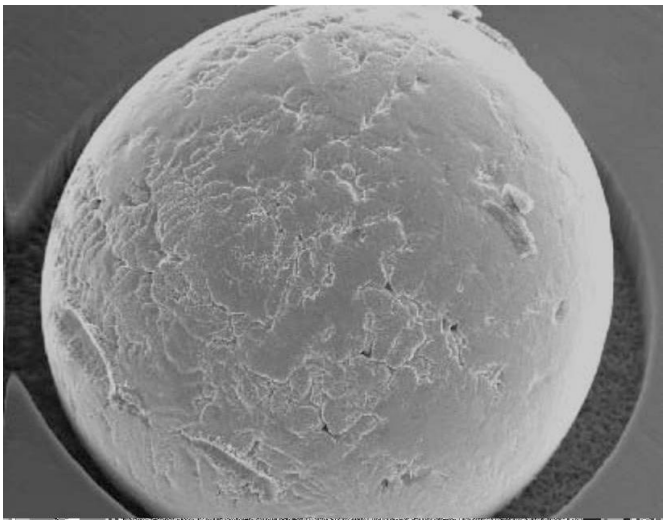

Figure 6-4. Witness Marks on Solder Ball

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The effect of burn-in on the probe marks was examined by simulating a cycle and placing a loaded socket into an oven at 125°C for nine hours. The result is shown in Figure 6-5. The penetration of the contact into the solder ball due to the higher temperature is greater but is well within the acceptable range. There was no visible pickup of solder on the contact tips. The location of the contact pinch is clearly seen in this photograph.

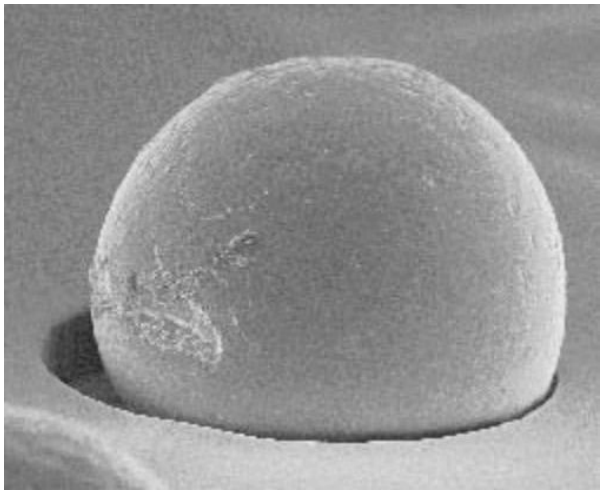

Figure 6-5. Effect of Bur-In on Probe Mark

6.4 Micro Tuning Fork Contact

Micro tuning fork contact system with vertical launch secures the solder balls to provide stable electrical continuity. Figure 6-6 shows how the micro fork contacts solder ball as well as solder witness marks after 24 hours at 150°C. There is also no contact made on the bottom of the solder ball preventing ball damage that could affect solder ball planarity specification, as illustrated in Figure 6-7.

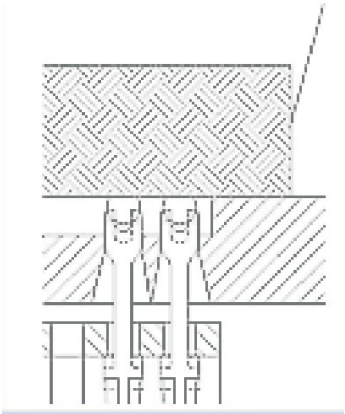

Figure 6-6. Micro Tuning Fork Contact for 0.5mm Pitch

Figure 6-7. Micro Tuning Fork Contact and Contact Marks on Solder Balls

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6.5 Texas Instruments Sockets

Figure 6-8 shows Texas Instrument's most advanced 0.8 mm and 0.5 mm pitch showing :

- Very small form factor
- Open top solution for easy automatic loading/unloading operations.

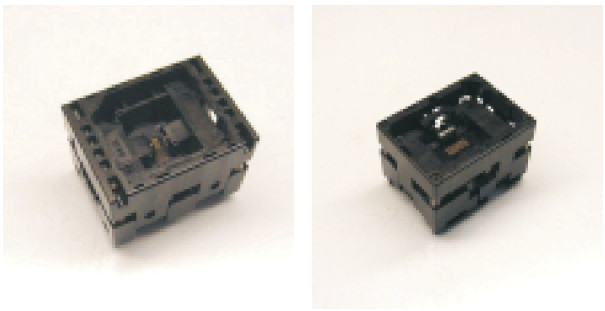

Figure 6-8. Socket Examples: Tuning Fork (Left) and Pinch Style (Right)

7 Summary

Some very good progress has been made during the past few years in developing fine pitch CSP packages sockets for CSP ball pitch. Sockets are now very common and proposed by most sockets manufacturers with open top or clam shell options.

Texas Instruments Interconnect Business Unit will provide you with a complete range of sockets technology for CSP package. For further information your local TI Field Sales representative can give you up-to-date information or please visit web site http://www.ti.com/snc/products/controls/burnin.htm

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A Frequently Asked Questions

A.1 Package Questions

Q **Do the solder balls come off during shipping?**

A No, this has never been observed. The balls are inspected for coplanarity, diameter, and other physical properties prior to packing for shipment. Because solder is used during the ball-attachment process, uniformly high ball-attachment strengths are developed. Also, the ball-attachment strength is monitored frequently in the assembly process to prevent ball loss from vibration and other shipping forces.

Q **Is package repair possible? Are tools available?**

A Yes, some limited package repair is possible, and there are some semiautomatic M/C tools available. However, TI does not specify the reliability of repaired packages.

Q **What are the leads that appear on the package edge for? Are they connected to the inner pattern?**

A Those leads are used for plating connections during the plating of Ni/Au on the copper trace during the fabrication of the substrate. Since they do have electrical connection with the inner pattern, they can be used for test probing and signal analysis. There is no reliability risk with them.

Q **Is burn-in testing possible? How about ball damage?**

A There are commercial sockets available for fine pitch package burn-in. For further information your local TI Field Sales representative can give you up-to-date information. The ball damage observed falls within specified tolerances, so the testing does not affect board mount.

Q **Is tape-and-reel shipping available?**

A Yes, tape-and-reel is an available method for shipping nFBGA packages.

Q **How does the packaging cost compare to QFPs?**

A CSPs are in many ways an ideal solution to cost reduction and miniaturization requirements. They offer enormous area reductions in comparison to QFPs and have increasing potential to do so without adding to system-level costs. In the best case, CSPs compete today on a cost-per-terminal basis with QFPs. For example, various CSPs from Texas Instruments are now available at cost parity within QFPs.

A.2 Assembly Questions

Q **What alignment accuracy is possible?**

A Alignment accuracy for the nFBGA package is dependent upon board-level pad tolerance, placement accuracy, and solder ball position tolerance. Nominal ball position tolerances are specified at ±50 µm. These packages are self-aligning during solder reflow, so final alignment accuracy may be better than placement accuracy.

Q **Can the solder joints be inspected after reflow?**

A Process yields of 5-ppm (parts per million) rejects are typically seen, so no final in-line inspection is required. Some customers are achieving satisfactory results during process set-up with lamographic X-ray techniques.

Q **How do the board assembly yields of nFBGAs compare to QFPs?**

A Many customers are initially concerned about assembly yields. However, once they had nFBGA packages in production, most of them report improved process yields compared to QFPs. This is due to the elimination of bent and misoriented leads, and the ability of these packages to self-align during reflow. The collapsing solder balls also mean that the coplanarity is improved over leaded components.

Q **Are there specific recommendations for SMT processing?**

A Texas Instruments recommends alignment with the solder balls for the CSP package, although it is possible to use the package outline for alignment. Most customers have found they do not need to change their reflow profile.

Q **Can the boards be repaired?**

A Yes, there are rework and repair tools and profiles available. TI strongly recommends that removed packages be discarded.

Q **What size land diameter for these packages should I design on my board?**

A Land size is the key to board-level reliability, and Texas Instruments strongly recommends following the design rules included in this document.

Q **The solder ball tolerance of the small body nFBGA is wider than that of other similar WCSP packages. What is driving this wider tolerance?**

A The WCSP has the solder ball mounted directly on the die. The nFBGA balls are mounted on the solder pad of the substrates. This pad size is driven by the solder mask opening so there is slight variation. In addition, the nominal solder ball size for the WCSP is smaller than the NFBGA. This larger ball size and variation in solder pad size are what causes there to be a wider tolerance for the nFBGA solder ball dimension.

Q **Will design changes need to be made on the PCB if the package is switched from a WCSP to an nFBGA of the same size?**

A No, in most cases, the recommended PCB pad size is the same for both packages so the so the same PCB can be used.

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Q **The small body nFBGA is slightly higher than the current package solution. Will this be an issue?**

A Unless the final product has a strict height restriction, minor differences in package height (± 0.05 mm) are not significant. The only impact would be to the pick and place process. The customer would simply need to measure the actual component thickness and adjust the process accordingly. This is standard procedure for component placement setup.

Q **Will any changes need to be made to the SMT process to support small body nFBGAs?**

A nFBGAs can support both flux dip and paste printing SMT processes. In addition, solder balls used for nFBGAs may be larger than that of other packages so, the stencil aperture will need to be reduced.

Q **Are smaller pitch sizes available?**

A Currently, 0.4 mm is the smallest ball pitch that TI offers for nFBGA packages. Pitch sizes smaller than 0.4 mm are not widely used in the industry for BGA packages and would require customization of the customer PCB.

A.3 Small Body nFBGA Package Questions

Q The solder ball tolerance of the small body nFBGA is wider than that of other similar WCSP packages. What is driving this wider tolerance?

A The WCSP has the solder ball mounted directly on the die. The nFBGA balls are mounted on the solder pad of the substrates. This pad size is driven by the solder mask opening so there is slight variation. In addition, the nominal solder ball size for the WCSP is smaller than the NFBGA. This larger ball size and variation in solder pad size are what causes there to be a wider tolerance for the nFBGA solder ball dimension.

Q Will design changes need to be made on the PCB if the package is switched from a WCSP to an nFBGA of the same size?

A No, in most cases, the recommended PCB pad size is the same for both packages so the so the same PCB can be used.

Q The small body nFBGA is slightly higher than the current package solution. Will this be an issue?

A Unless the final product has a strict height restriction, minor differences in package height (± 0.05mm) are not significant. The only impact would be to the pick and place process. The customer would simply need to measure the actual component thickness and adjust the process accordingly. This is standard procedure for component placement setup.

Q Will any changes need to be made to the SMT process to support small body nFBGAs?

A nFBGAs can support both flux dip and paste printing SMT processes. In addition, solder balls used for nFBGAs may be larger than that of other packages so, the stencil aperture will need to be reduced.

Q Are smaller pitch sizes available?

A Currently, 0.4mm is the smallest ball pitch that TI offers for nFBGA packages. Pitch sizes smaller than 0.4mm are not widely used in the industry for BGA packages and would require customization of the customer PCB.

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B Package Data Sheets

Table B-1 shows TI's strategic package lineup, followed by package data sheets for many of the package families offered as standard products by Texas Instruments. As new packages are added, they will be placed on the strategic package lineup. Contact your TI field sales office for information on the most current offerings. Samples are available for all packages shown in Table B-1.

Table B-1. TI's Strategic Package Line-Up

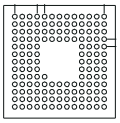
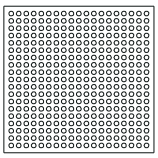
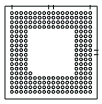
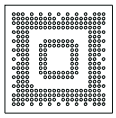
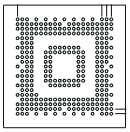
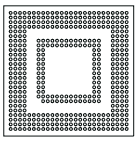
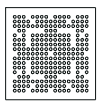
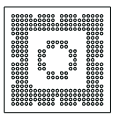
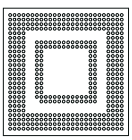
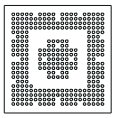
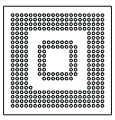
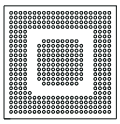
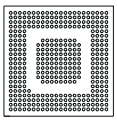
nFBGA Package Product Guide								
Pitch (mm)	Package Size (mm)							
	6×6	7×7	8×8	10×10	12×12	13×13	14×14	16×16
0.8					145ZWS 			361ZWT 
0.65			113ZVD					
0.5	87ZVW	72ZST	195ZWV	225ZWF 	289ZVL 	289ZWE 	447ZAC 	
		143ZWU		241ZWG 	293ZVL 		447ZAF 	
		143ZZC			318ZVL 			
		152ZZB			325ZVL 			
					385ZWK 			
					385ZWM 			

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Table B-1. TI's Strategic Package Line-Up (continued)

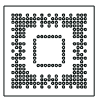
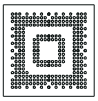
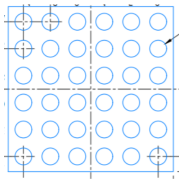
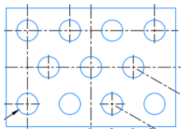
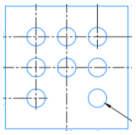
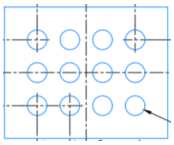
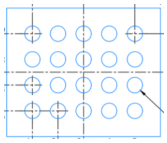
nFBGA Package Product Guide								
Pitch (mm)	Package Size (mm)							
	6×6	7×7	8×8	10×10	12×12	13×13	14×14	16×16
0.4		209ZXN		241ZWJ 				
				289ZWJ 				
				360ZWJ				

Table B-2. TI's Strategic Small Body Package Line-Up

nFBGA Package Product Guide					
Pitch (mm)	Package Size (mm)				
	2 x 1.4	2 x 2	2 x 2.5	2.45 x 2.45	2.5 x 3
0.4					
0.5					

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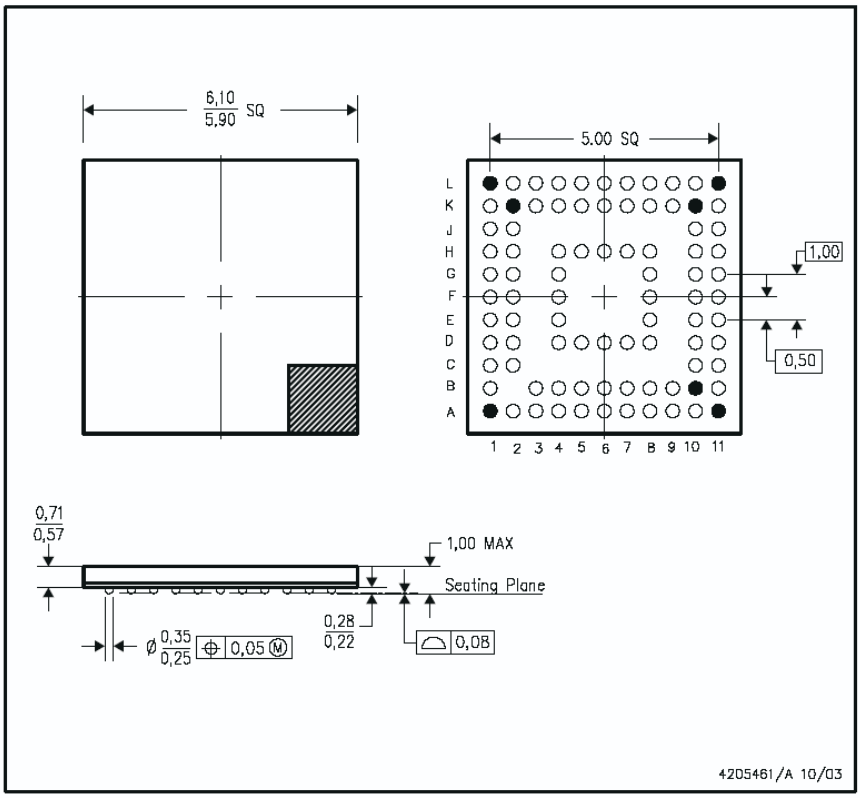

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration.
D. A1, A11, L1, L11, B10, K2, K10 to be dummy balls.
E. This package is lead-free.

Figure B-1. 87ZVW Package Outline (6 x 6mm, 0.5mm pitch)

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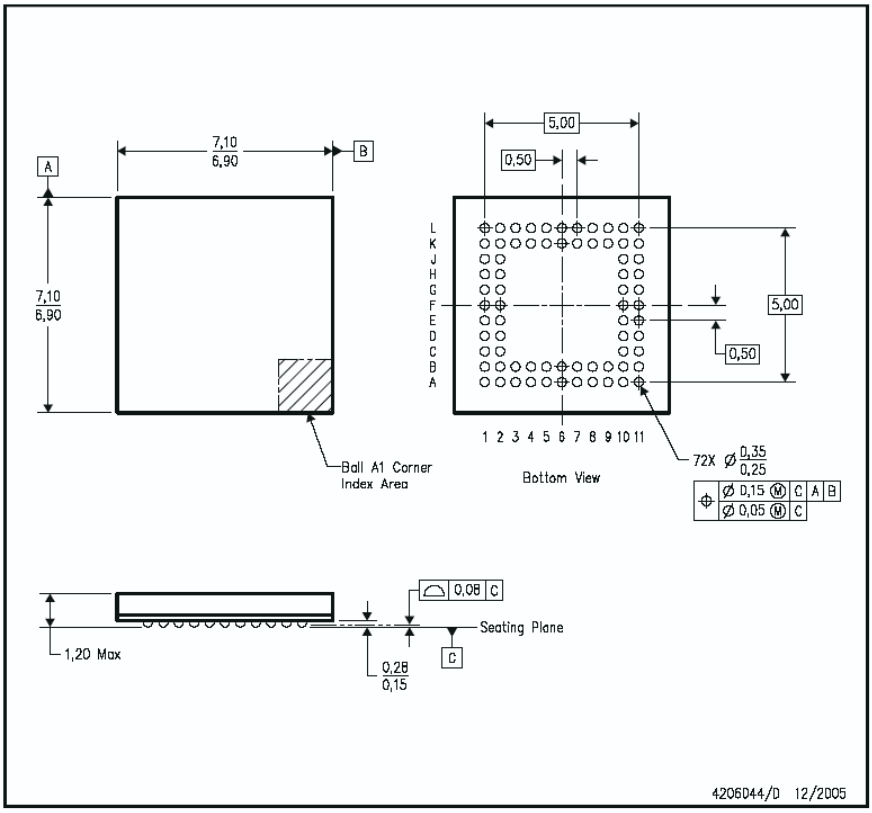

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Complies to JEDEC MO–195 variation AD (depopulated).
D. This package is lead–free. Refer to the 72 GST package (drawing 4206043) for tin–lead (SnPb).

Figure B-2. 72ZST Package Outline (7 x 7mm, 0.5mm pitch)

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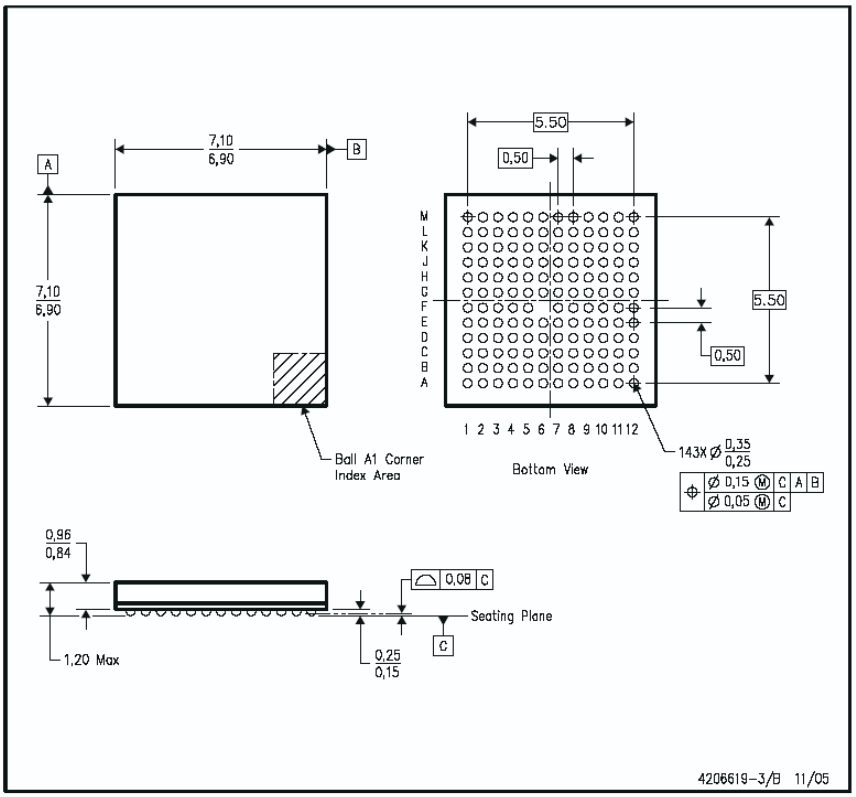

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO-225 registration is pending.
D. This is a lead-free solder ball design.

Figure B-3. 143ZZC Package Outline (7 x 7mm, 0.5mm pitch)

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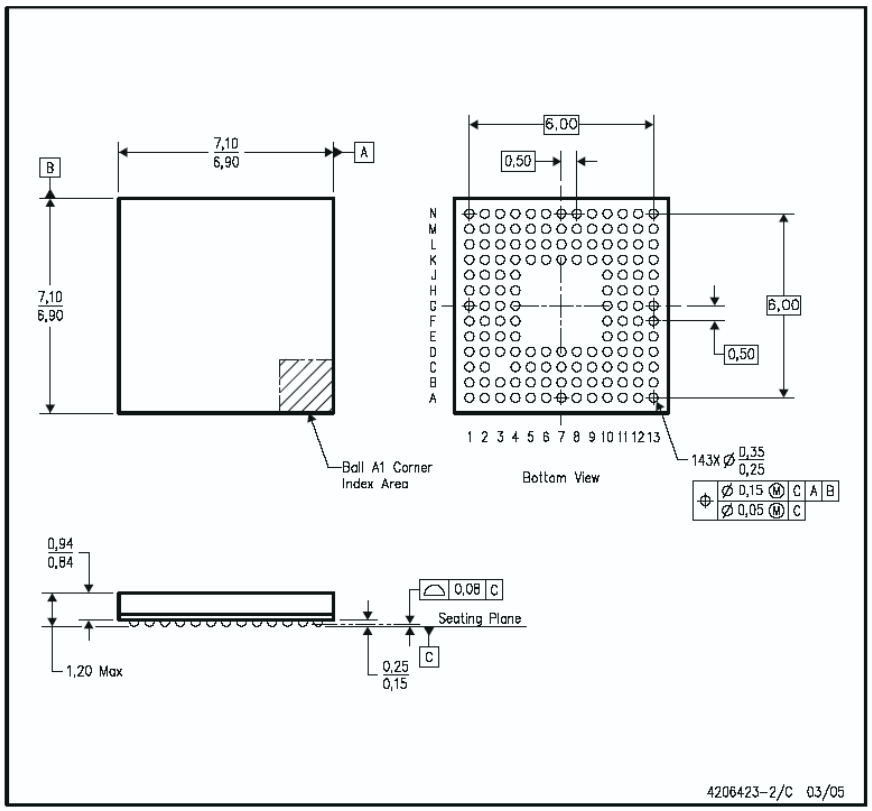

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO-225 registration is pending.
D. This package is lead-free.

Figure B-4. 143ZWU Package Outline (7 x 7mm, 0.5mm pitch)

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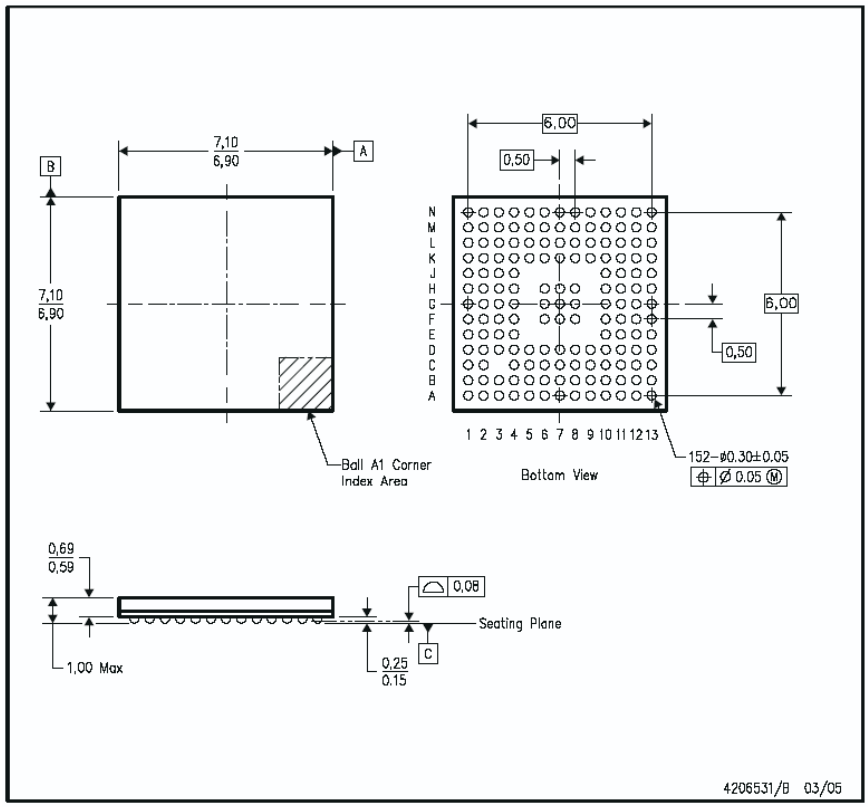

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. JEDEC MO–225 registration is pending.
D. This package is lead–free.

Figure B-5. 152ZZB Package Outline (7 x 7mm, 0.5mm pitch)

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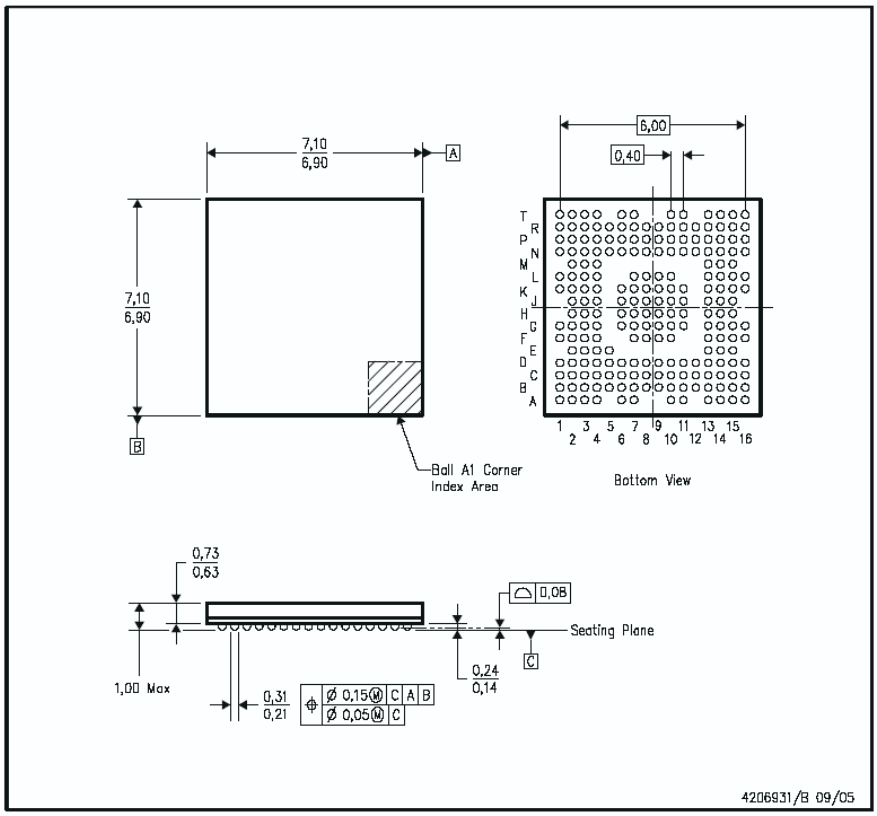

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–195.
D. This package is lead–free.

Figure B-6. 209ZXN Package Outline (7 x 7mm, 0.4mm pitch)

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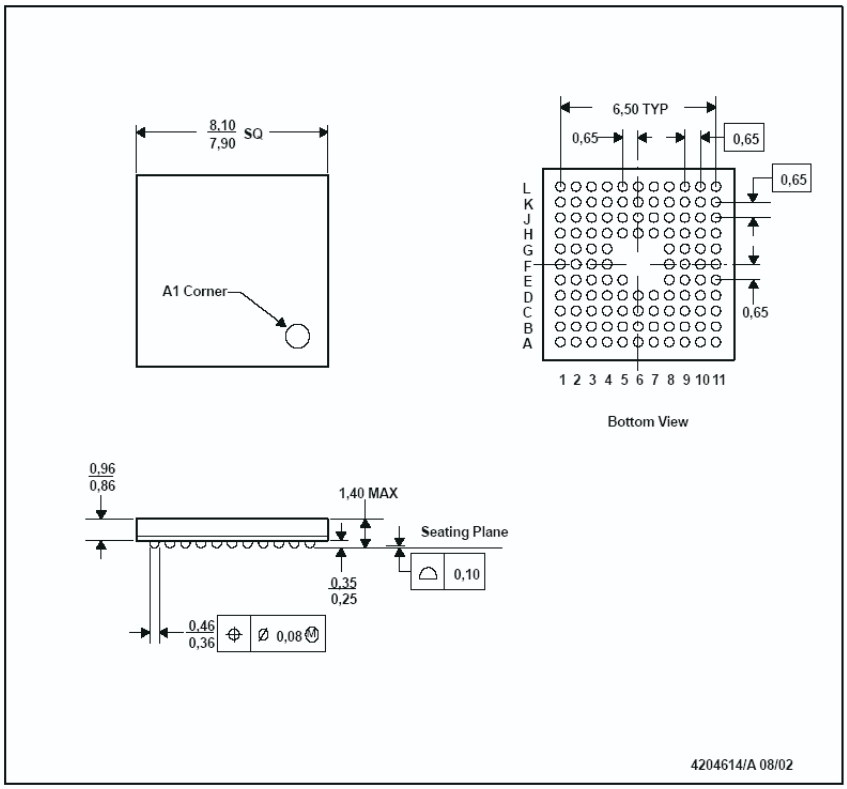

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. LFBGA configuration
D. This package id lead-free.

Figure B-7. 113ZVD Package Outline (8 x 8mm, 0.65mm pitch)

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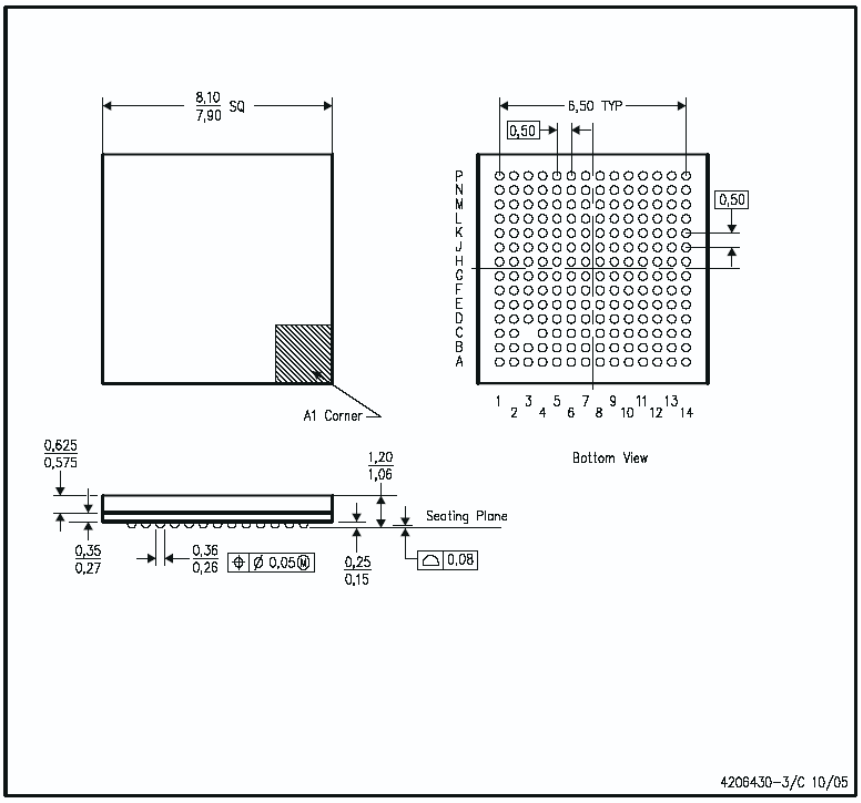

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead-free solder ball design.

Figure B-8. 195ZWV Package Outline (8 x 8mm, 0.5mm pitch)

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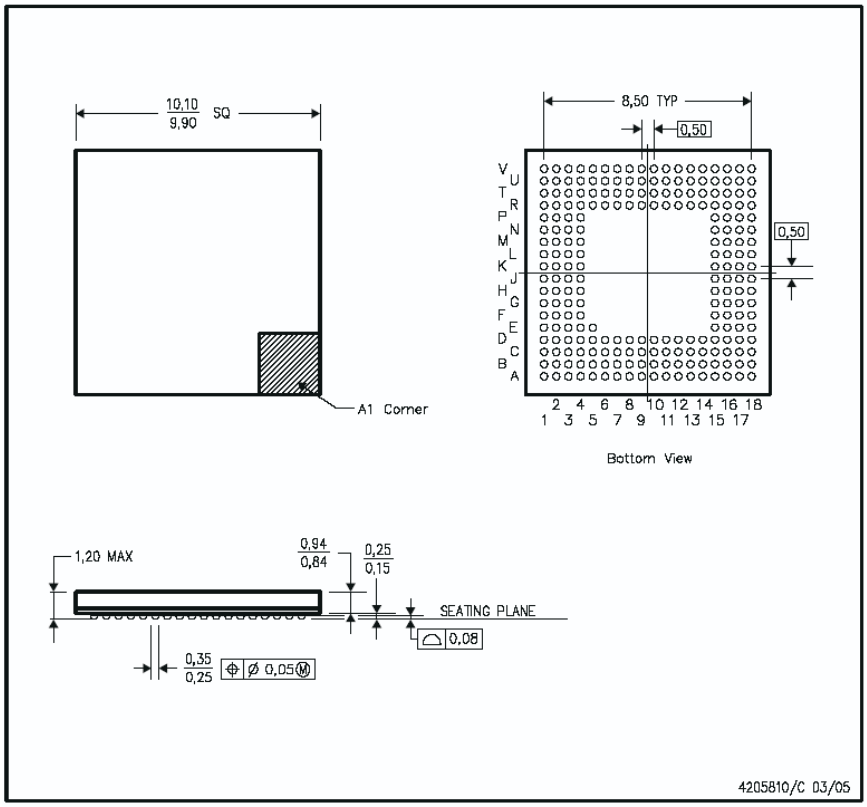

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration
D. This package is lead-free.

Figure B-9. 225ZWF Package Outline (10 x 10mm, 0.5mm pitch)

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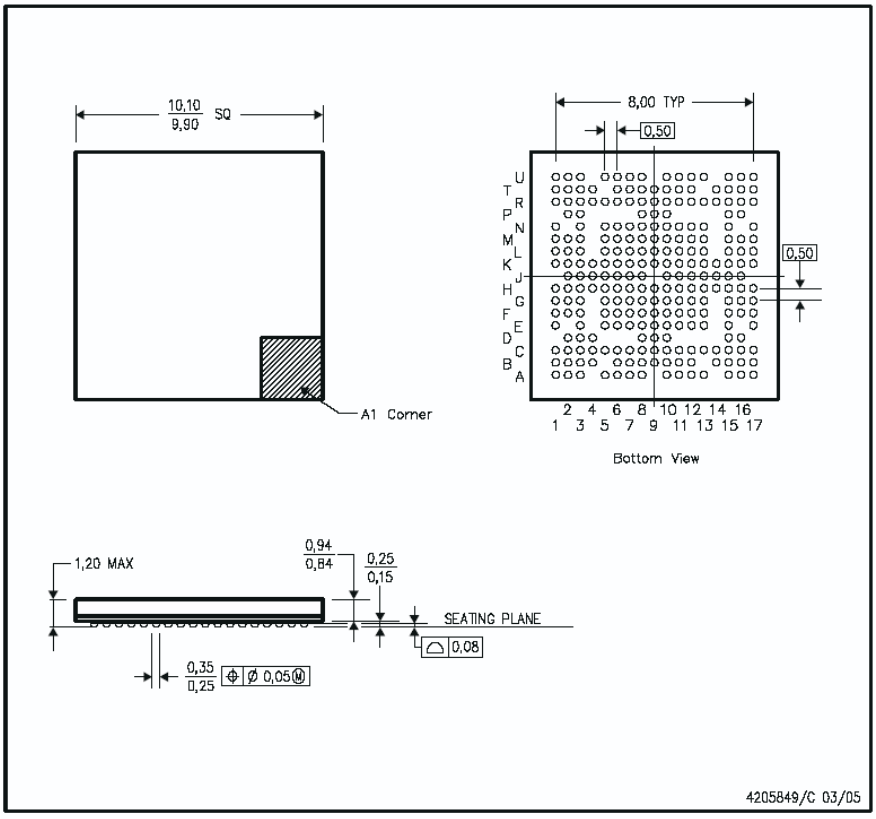

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. nFBGA configuration
D. This package is lead-free.

Figure B-10. 241ZWG Package Outline (10 x 10mm, 0.5mm pitch)

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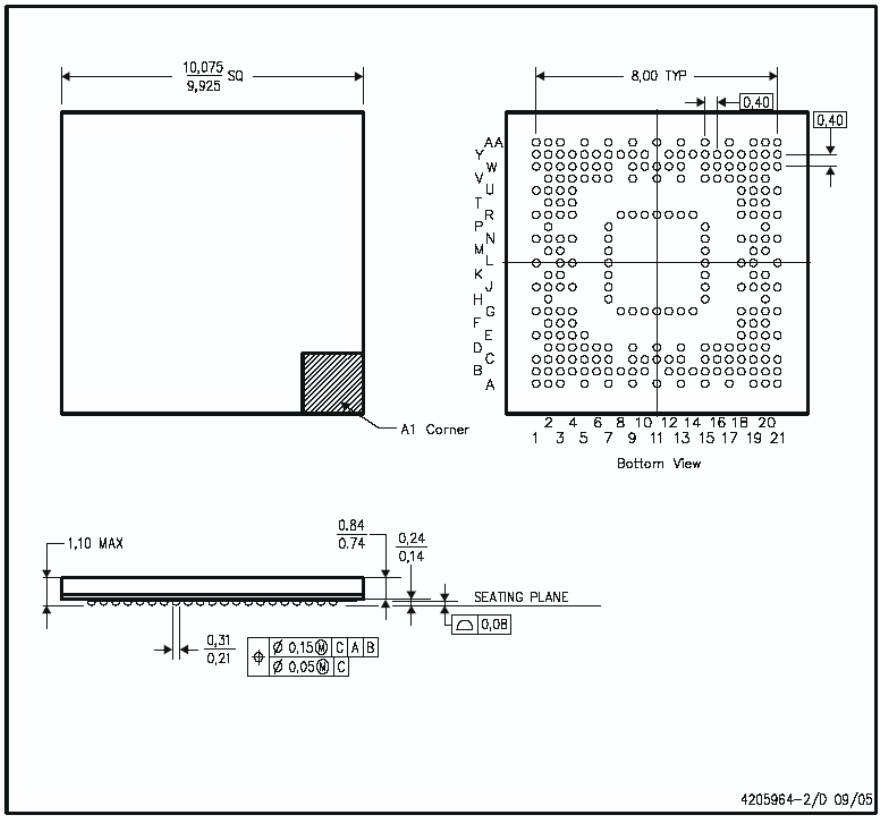

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-11. 241ZWJ Package Outline (10x10mm, 0.4mm pitch)

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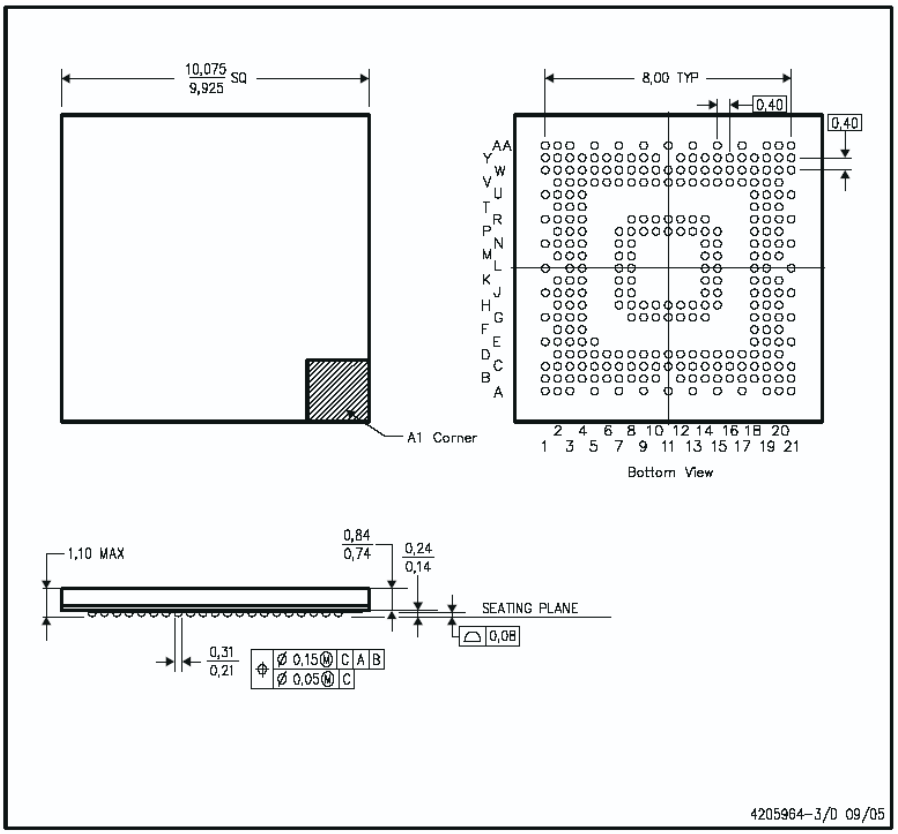

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-12. 289ZWJ Package Outline (10 x 10mm, 0.4mm pitch)

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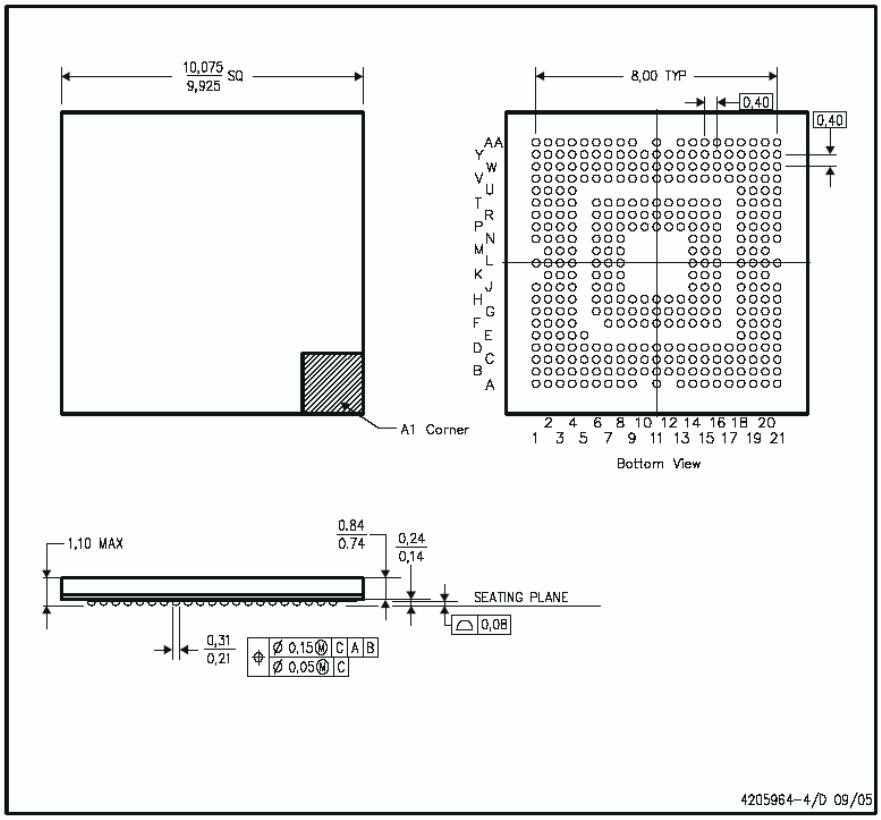

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-13. 360ZWJ Package Outline (10 x 10mm, 0.4mm pitch)

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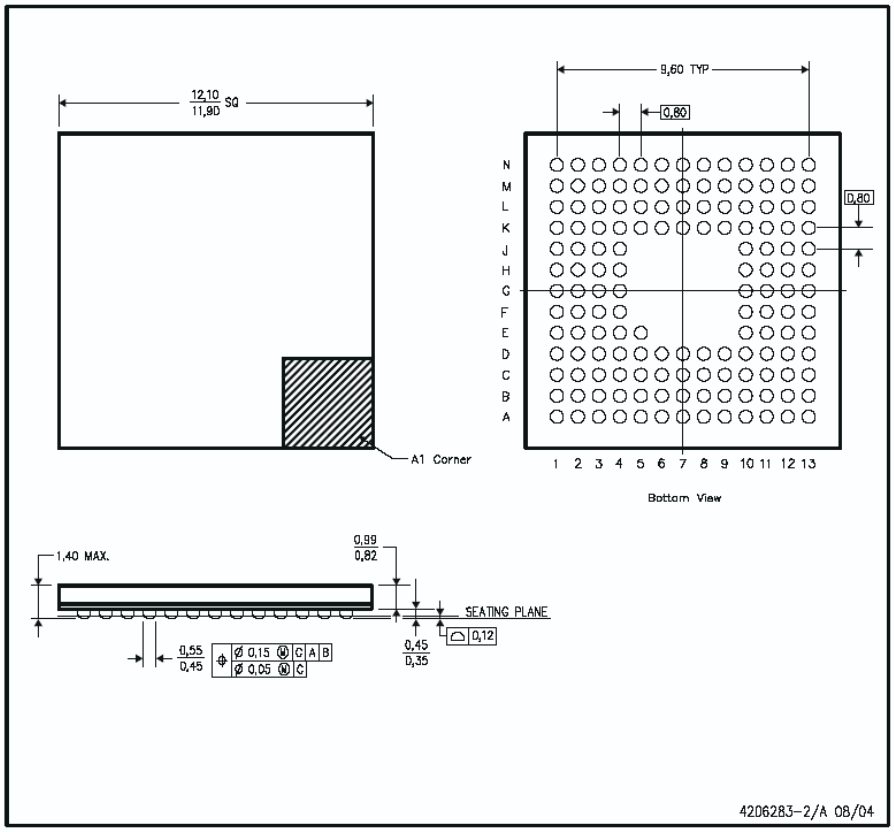

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-14. 145ZWS Package Outline (12 x 12mm, 0.8mm pitch)

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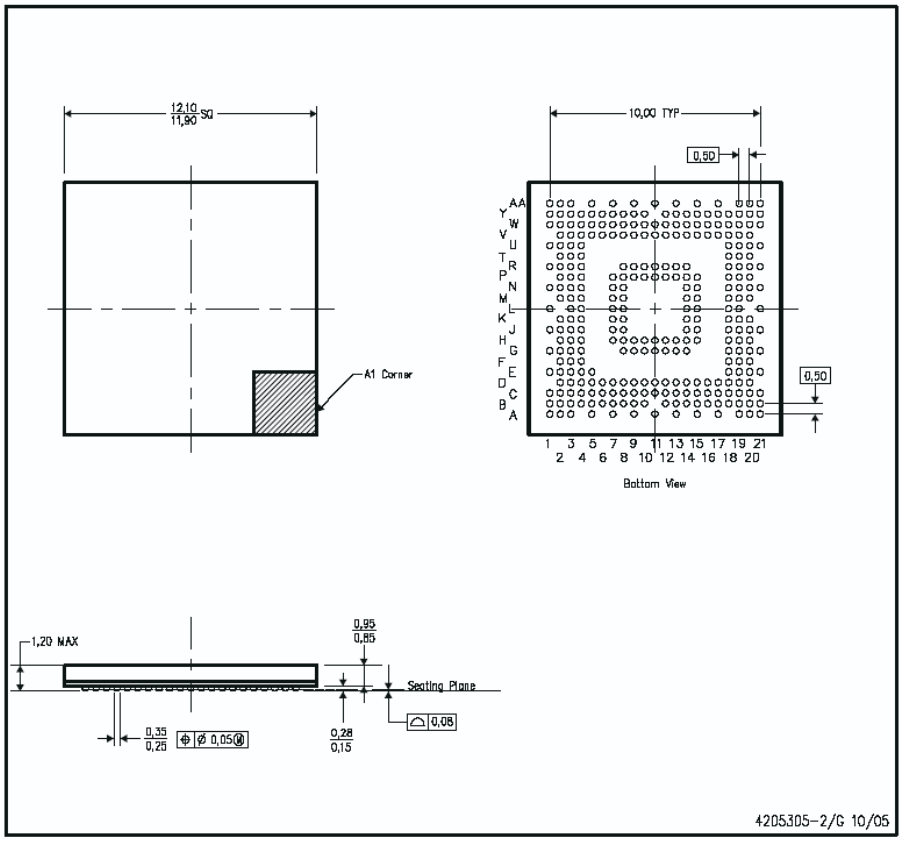

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-15. 289ZVL Package Outline (12 x 12mm, 0.5mm pitch)

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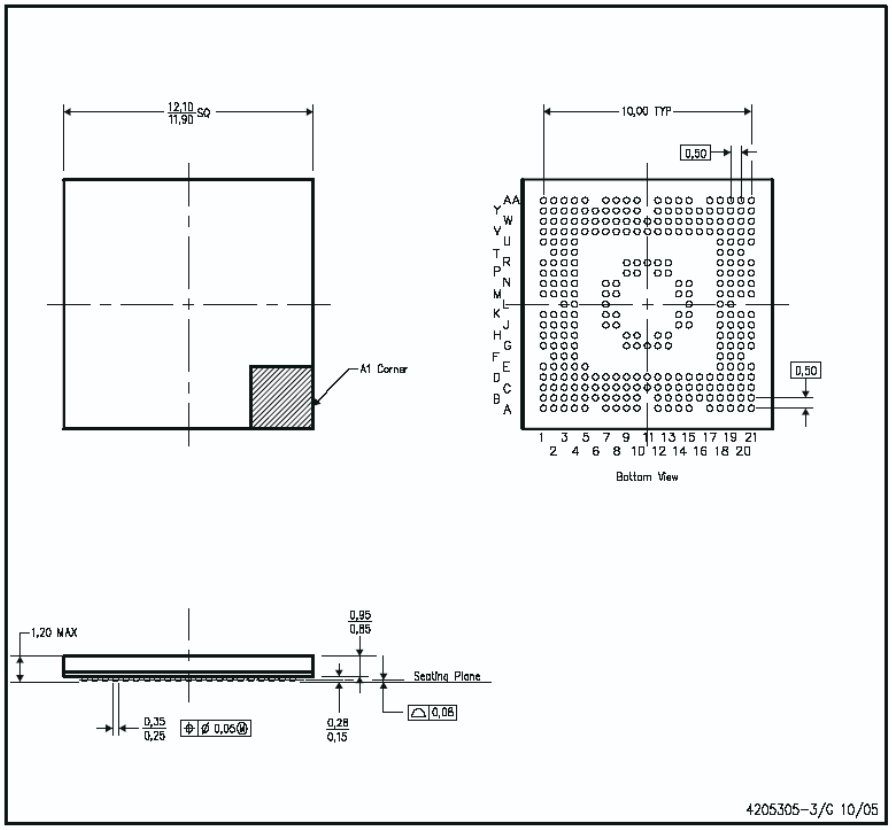

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-16. 293ZVL Package Outline (12 x 12mm, 0.5mm pitch)

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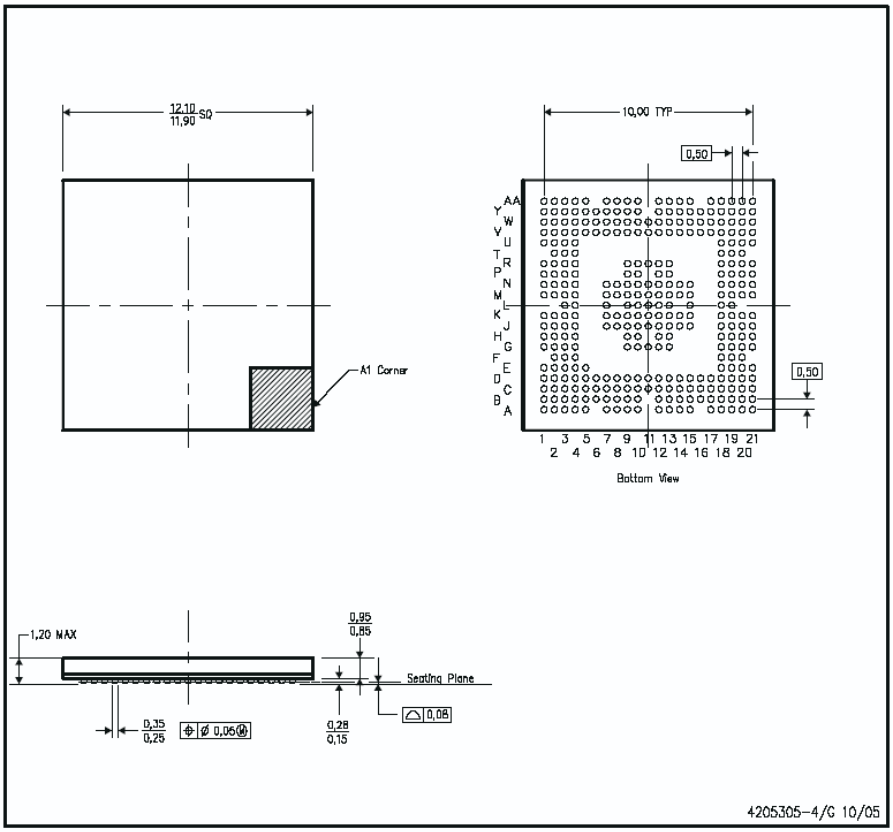

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-17. 318ZVL Package Outline (12 x 12mm, 0.5mm pitch)

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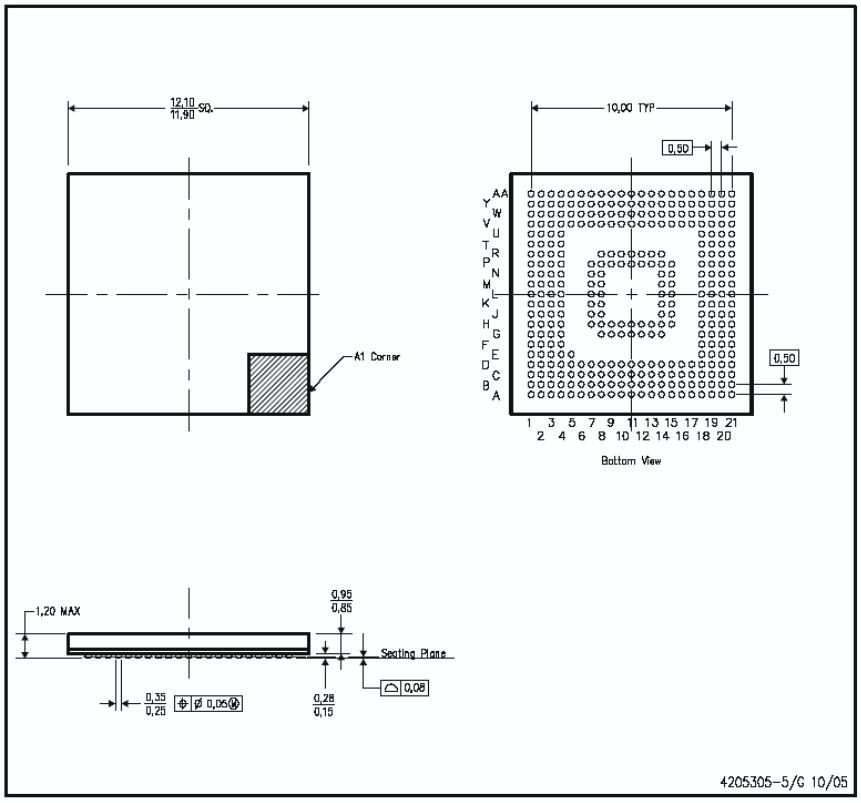

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-18. 325ZVL Package Outline (12 x 12mm, 0.5mm pitch)

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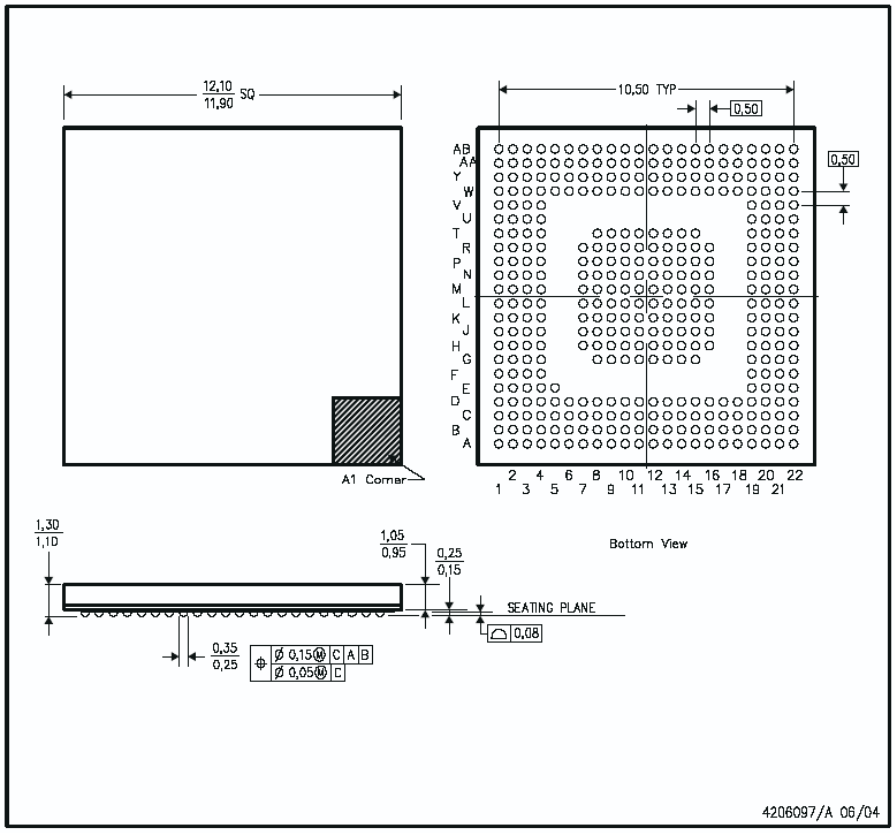

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
B. This package is lead–free.

Figure B-19. 385ZWM Package Outline (12 x 12mm, 0.5mm pitch)

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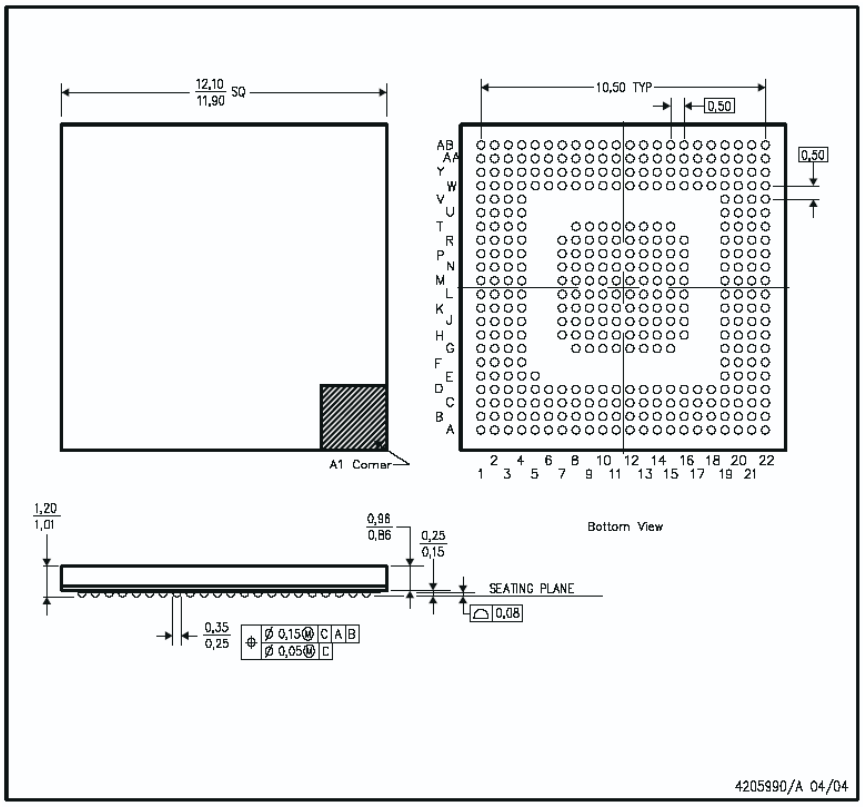

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
B. This package is lead-free.

Figure B-20. 385ZWK Package Outline (12 x 12mm, 0.5mm pitch)

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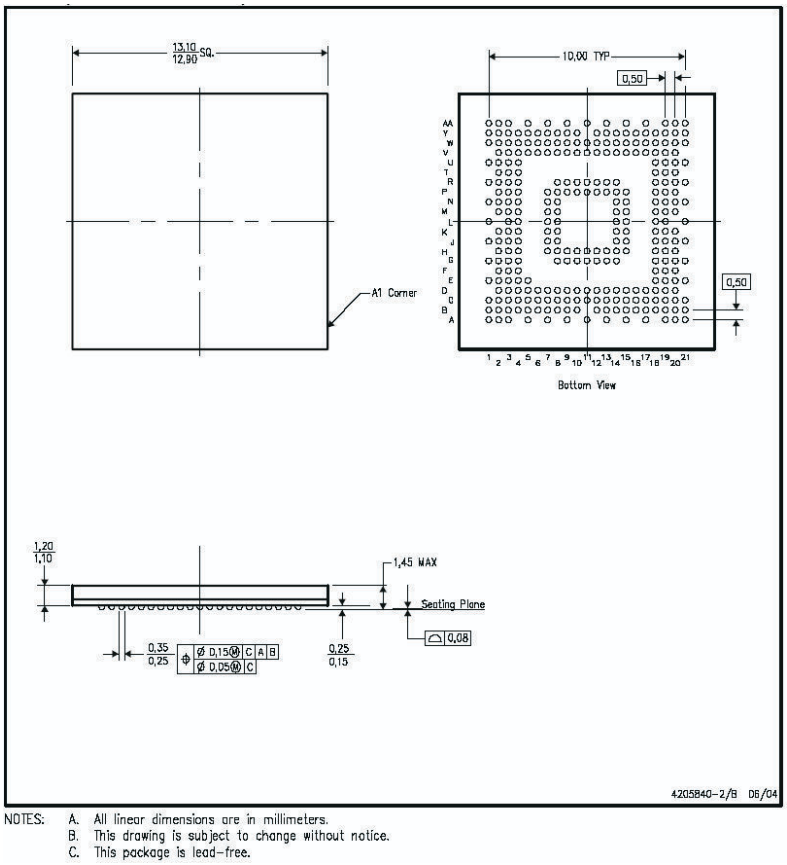

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-21. 289ZWE Package Outline (13 x 13mm, 0.5mm pitch)

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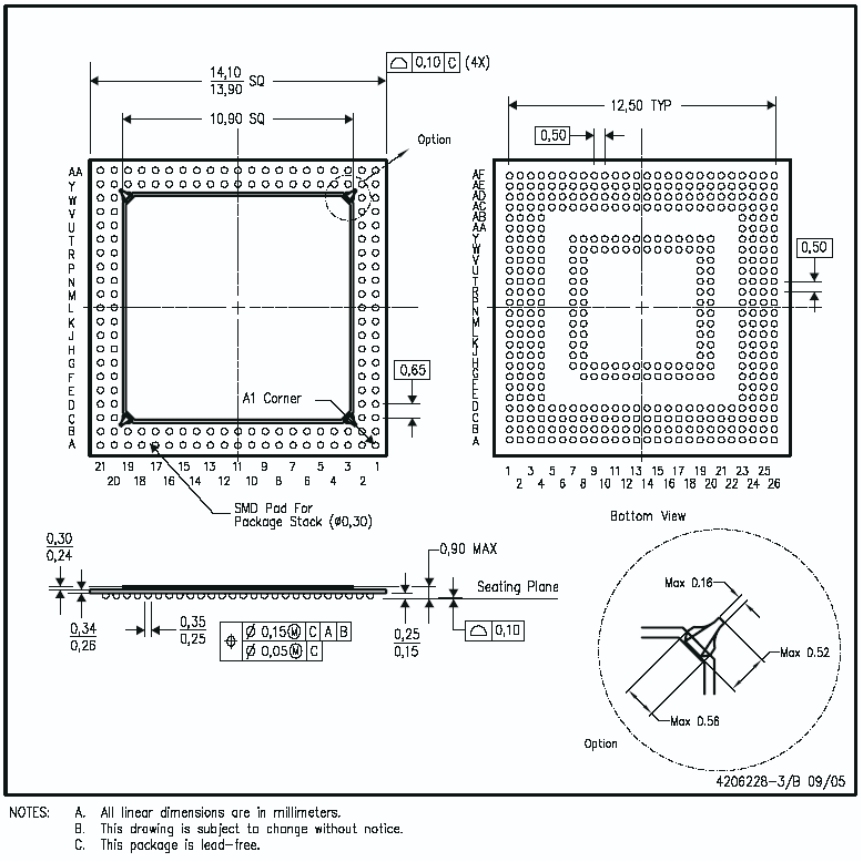

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-22. 447ZAC Package Outline (14 x 14mm, 0.5mm pitch)

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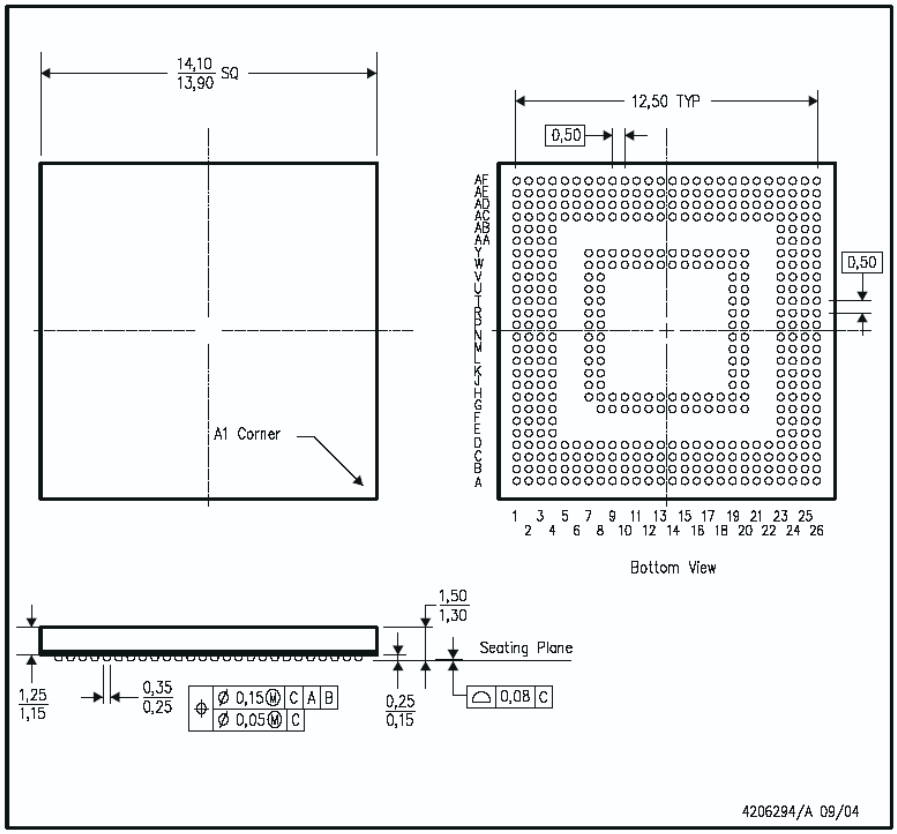

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead–free.

Figure B-23. 447ZAF Package Outline (14 x 14mm, 0.5mm pitch)

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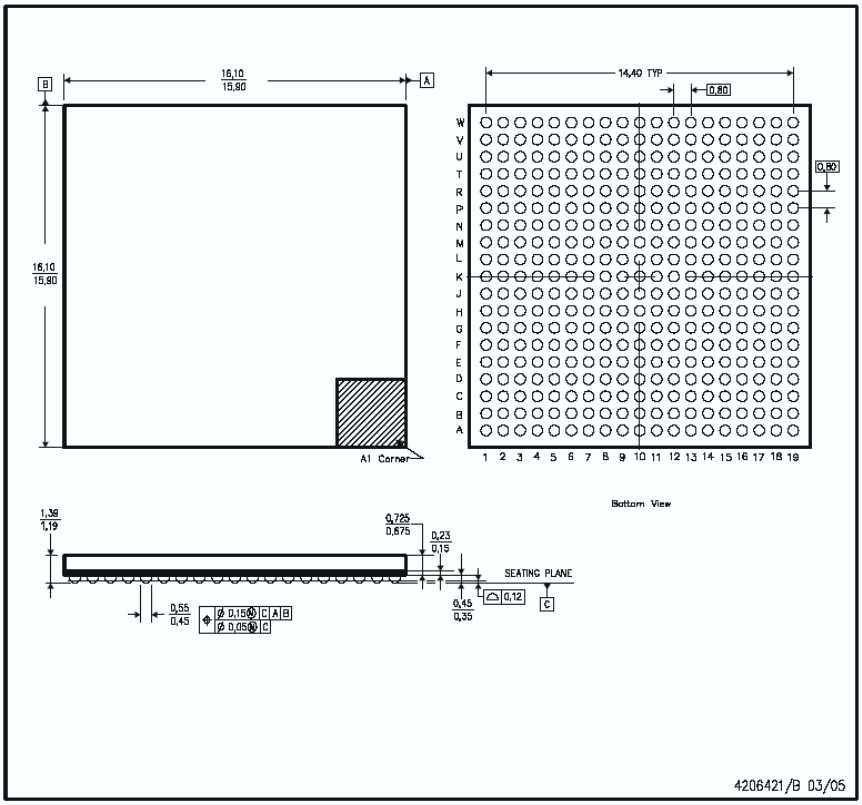

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is lead-free.

Figure B-24. 361ZWT Package Outline (16 x 16mm, 0.8mm pitch)

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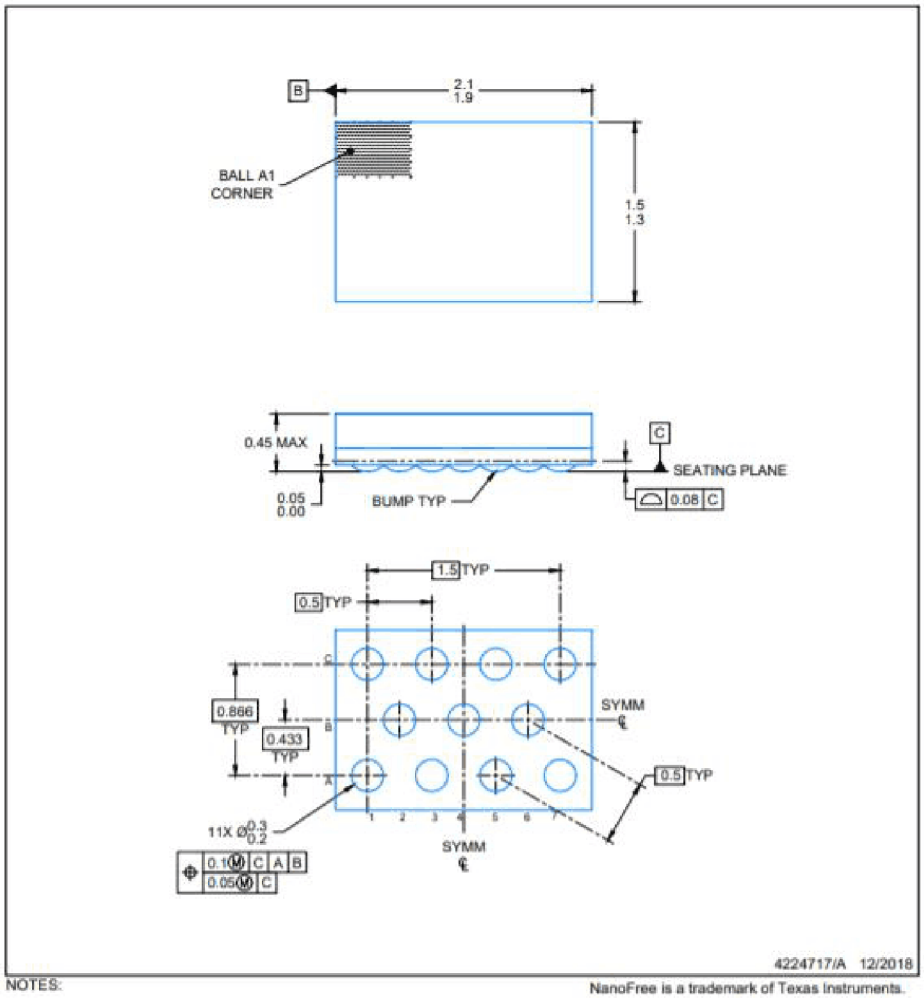

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Figure B-25. 11ZWA Package Outline (2 x 1.4mm, 0.5mm pitch)

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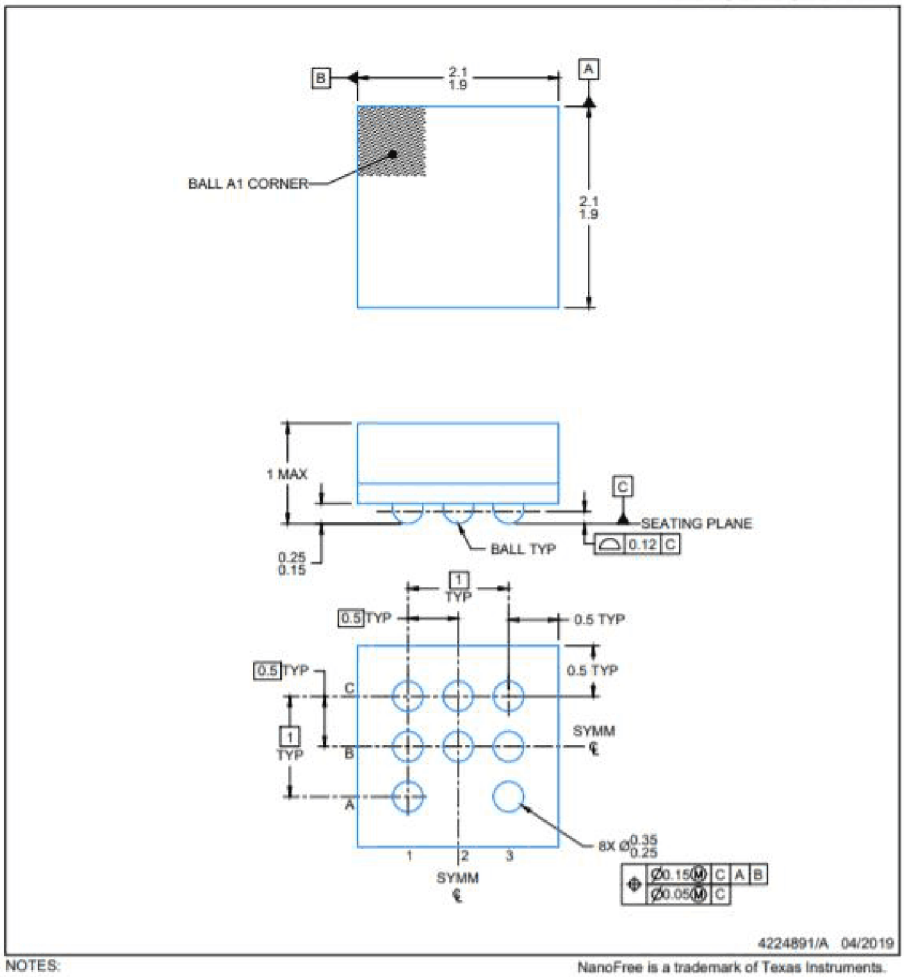

Figure B-26. 8 NMB Package Outline (2 x 2mm, 0.5mm pitch)

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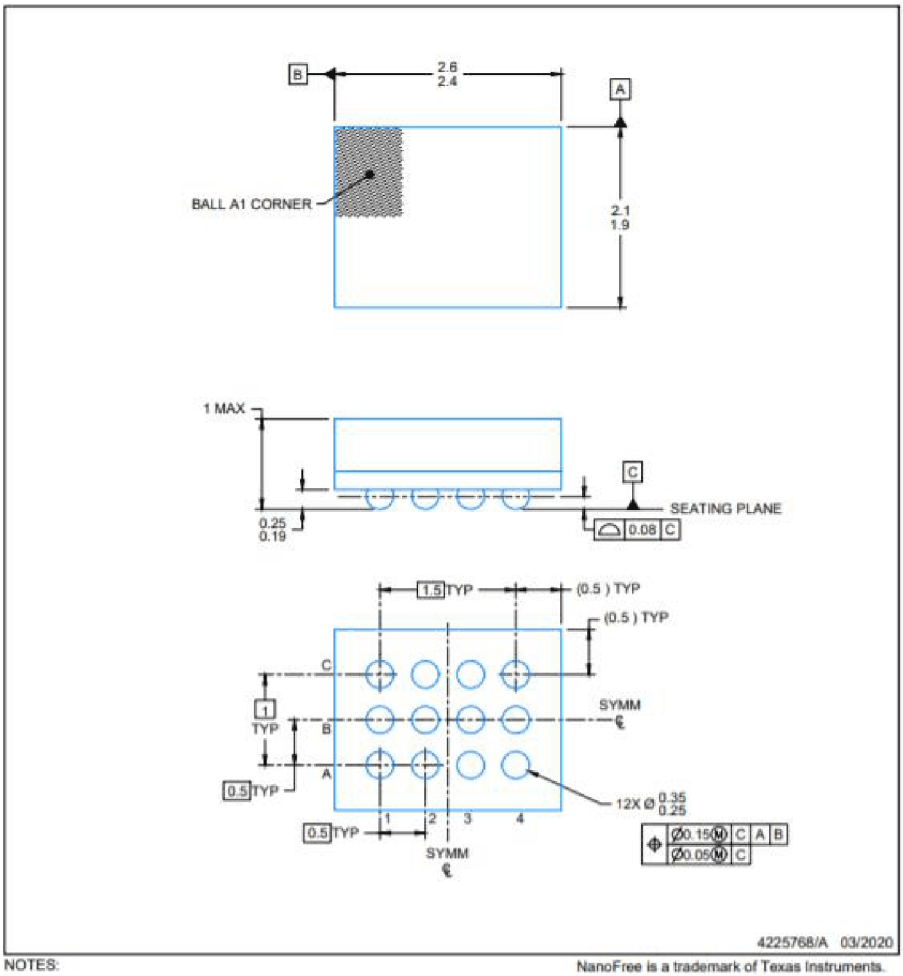

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Figure B-27. 12NMN Package Outline (2 x 2.5mm, 0.5mm pitch)

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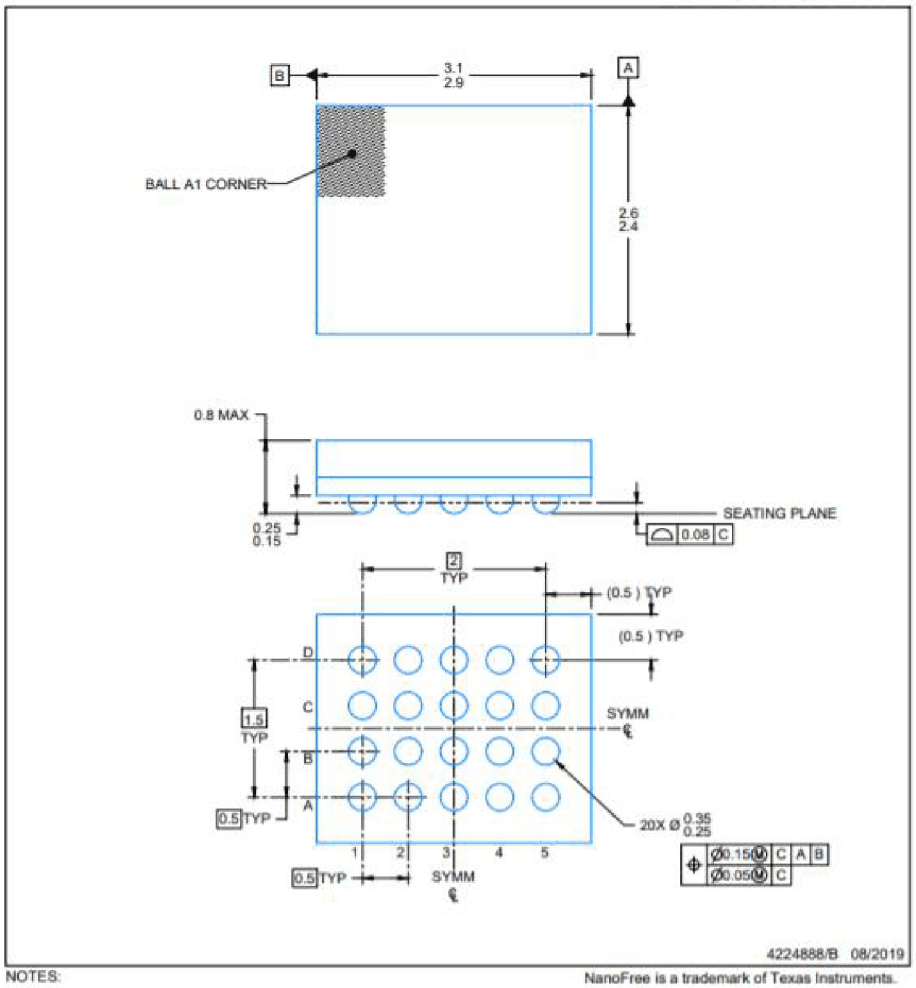

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Figure B-28. 20NME Package Outline (2.5 x 3 mm, 0.5mm pitch)

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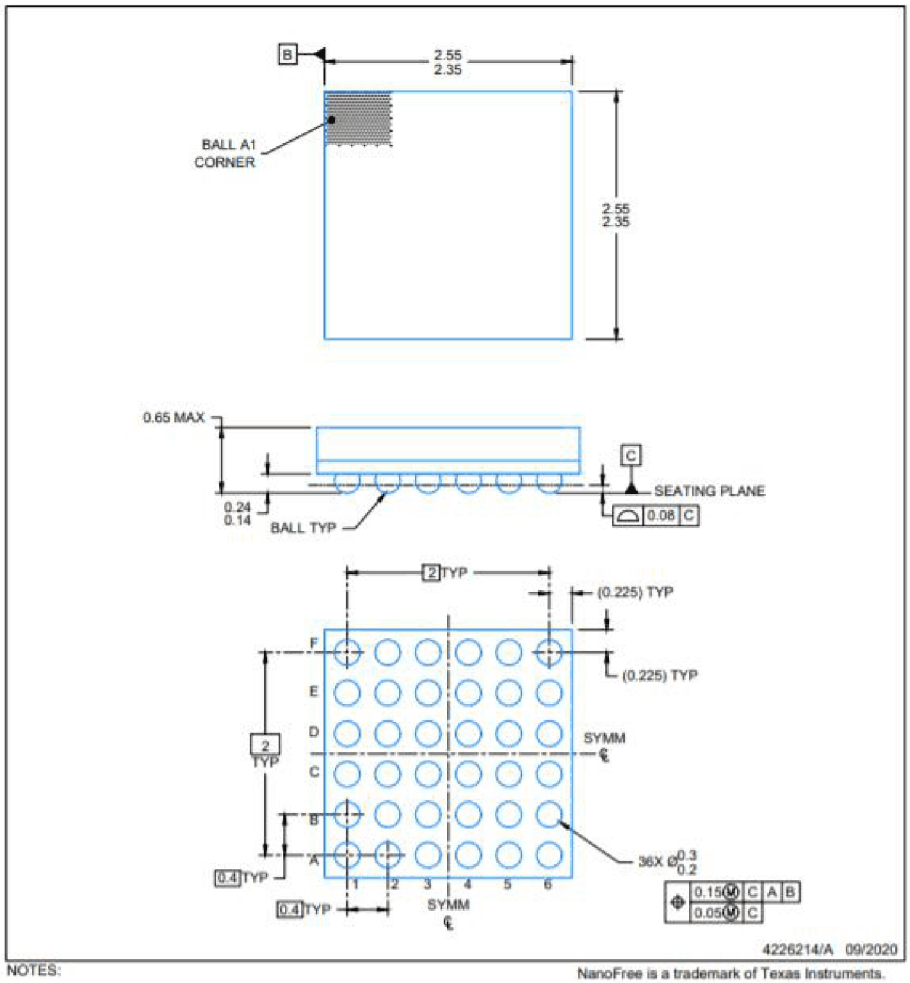

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Figure B-29. 36ZEC Package Outline (2.45 x 2.45 mm, 0.4mm pitch)

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C Thermal Modeling Results

Table C-1, Table C-2, and Table C-3 detail thermal modeling results from 8x8mm, 12x12mm, and 16x16mm nFBGA packages, respectively.

Table C-1. 8×8 mm nFBGA Thermal Simulation Result

	Die Size (mm)	2.0 × 2.0 mm		4.0 × 4.0 mm		6.0 × 6.0 mm	
Power = 1w	**Velocity (m/s)**	**1S0P**	**2S2P**	**1S0P**	**2S2P**	**1S0P**	**2S2P**
θJA (°C/W)	0	140.148	101.061	100.476	61.161	89.286	50.352
	1	129.084	97.211	89.269	57.353	78.173	46.554
	2	124.432	96.281	84.656	56.439	73.714	45.622
	3	121.435	95.611	81.895	55.675	70.399	44.774
Pusai JT (°C/W)	0	2.244	2.076	0.625	0.462	0.509	0.342
	1	2.238	2.066	0.582	0.429	0.480	0.308
	2	2.215	2.062	0.559	0.403	0.441	0.290
	3	2.196	2.059	0.545	0.399	0.429	0.278
Pusai JB (°C/W)	0	78.144	80.346	32.656	33.063	20.345	21.658
	1	75.007	77.987	30.032	32.785	18.921	21.539
	2	74.760	77.876	29.997	32.687	18.710	21.437
	3	74.616	77.742	29.733	32.200	18.306	21.380
θJC (°C/W)		29.984	—	12.050	—	7.347	—
θJB (°C/W)		77.056	78.643	31.636	33.043	19.899	21.226

Table C-2. 12×12 mm nFBGA Thermal Simulation Result

	Die Size (mm)	3.0 × 3.0 mm		6.5 × 6.5mm		10.0 × 10.0 mm	
Power = 1w	**Velocity (m/s)**	**1S0P**	**2S2P**	**1S0P**	**2S2P**	**1S0P**	**2S2P**
θJA (°C/W)	0	89.520	62.812	61.940	35.763	53.538	28.380
	1	80.639	59.169	52.553	32.150	44.582	24.786
	2	77.284	58.444	49.596	31.427	41.273	24.032
	3	75.257	57.923	47.675	30.897	39.314	23.518
Pusai JT (°C/W)	0	0.855	0.623	0.373	0.274	0.306	0.216
	1	0.791	0.589	0.356	0.239	0.246	0.183
	2	0.782	0.588	0.321	0.209	0.236	0.176
	3	0.732	0.585	0.300	0.207	0.227	0.156
Pusai JB (°C/W)	0	46352	49.411	15.822	18.310	8.886	10.687
	1	45.699	49.091	15.689	17.954	8.650	10.422
	2	45.553	48.646	15.499	17.922	8.472	10.405
	3	45.483	48.208	15.424	17.903	8.287	10.380
θJC (°C/W)		16.586	—	5.742	—	4.428	—
θJB (°C/W)		46.695	47.787	15.894	16.429	8.180	8.604

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Table C-3. 16×16 mm nFBGA Thermal Simulation Result

Power = 1w	Die Size (mm)	3.0 × 3.0 mm		8.5 × 8.5mm		14.0 × 14.0 mm	
	Velocity (m/s)	1S0P	2S2P	1S0P	2S2P	1S0P	2S2P
θJA (°C/W)	0	88.870	69.542	48.861	27.847	39.056	21.145
	1	81.509	66.538	69.164	24.125	31.690	17.579
	2	79.283	65.851	36.777	23.404	28.913	16.870
	3	77.860	65.395	35.387	22.974	27.514	16.410
Pusai JT (°C/W)	0	0.888	0.820	0.290	0.355	0.237	0.181
	1	0.828	0.755	0.226	0.280	0.177	0.103
	2	0.808	0.740	0.225	0.155	0.164	0.099
	3	0.801	0.737	0.218	0.153	0.159	0.098
Pusai JB (°C/W)	0	59.993	61.429	11.901	12.620	5.252	5.523
	1	59.895	61.026	11.667	11.925	5.231	5.470
	2	59.349	59.877	11.270	11.591	4.806	5.267
	3	59.284	59.842	11.176	11.584	4.776	5.104
θJC (°C/W)		20.002	—	3.797	—	1.853	—
θJB (°C/W)		57.658	58.886	10.183	10.717	4.898	5.158

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2015) to Revision C (May 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3
• Update was made in Section 1	3
• Updates were made in Section 3	10
• Update was made in Section 5.1	18
• Updates were made in Section 5.3	19
• Update was made in Appendix A	26
• Update was mad in Appendix A.2	26
• Updates were made in Appendix B	28

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