

LPC55S2x/LPC552x

Errata sheet LPC55S2x/LPC552x

Rev. 1.7 — February 25, 2021

Errata sheet

Document information

| Info | Content |
|-----------------|--|
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| Abstract | LPC55S2x/LPC552x errata |



Revision history

| Rev | Date | Description |
|-----|----------|--|
| 1.7 | 20210225 | Added USB.4 errata, Section 3.7 “USB.4: In USB high-speed device mode, device writes extra byte(s) to the buffer” . |
| 1.6 | 20201214 | Includes Section 3.5 “USB.3: For the USB high-speed device controller, the detection handshaking fails when certain full-speed hubs are connected” . |
| 1.5 | 20200826 | Adds Section 3.6 “WAKEIO.1: Wake-up I/O register reports incorrect wake-up source” . |
| 1.4 | 20200826 | Adds Section 5.1 “ROM bootloader updated to provide API functionality for entry to ISP mode” . |
| 1.3 | 20191204 | Updated ROM.1 workaround. |
| 1.2 | 20191021 | Enhances product identification and adds USB.1 and USB.2 errata. |
| 1.1 | 20190923 | Describes ROM failure to enter ISP mode when an image is corrupted with flash pages in an erased or unprogrammed state. |
| 1.0 | 20190719 | Initial version. |

Contact information

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1. Product identification

The LPC55S2x/LPC552x VFBGA98 package has the following top-side marking:

- First line: LPC55S2x/LPC552x
- Second line: JEV98
- Third line: xxxxxxxx
- Fourth line: zzzyywwxR
 - yyww: Date code with yy = year and ww = week.
 - xR: Device revision 1B

The LPC55S2x/LPC552x HLQFP100 package has the following top-side marking:

- First line: LPC55S2x/LPC552x
- Second line: xxxxxxxx
- Third line: zzzyywwxR
 - yyww: Date code with yy = year and ww = week.
 - xR: Device revision 1B

The LPC55S2x/LPC552x HTQFP64 package has the following top-side marking:

- First line: LPC55S2x/LPC552x
- Second line: JBD64
- Third line: xxxx
- Fourth line: xxxx
- Fifth line: zzzyywwxR
 - yyww: Date code with yy = year and ww = week.
 - xR: Device revision 1B

2. Errata overview

Table 1. Functional problems table

| Functional problems | Short description | Revision identifier | Detailed description |
|---------------------|--|---------------------|-----------------------------|
| ADC.1 | Async interrupts with resume not supported. | 1B | Section 3.1 |
| ROM.1 | ROM fails to enter ISP mode when image is corrupted with flash pages in an erased or unprogrammed state. | 1B | Section 3.2 |
| USB.1 | USB HS host fails when connecting to an LS device (mouse). | 1B | Section 3.3 |
| USB.2 | Automatic USB rate adjustment not functional when using multiple hubs. | 1B | Section 3.4 |

Table 1. Functional problems table ...continued

| Functional problems | Short description | Revision identifier | Detailed description |
|---------------------|--|---------------------|-----------------------------|
| USB.3 | For the USB high-speed device controller, the detection handshaking fails when certain full-speed hubs are connected. | 1B | Section 3.5 |
| WAKEIO.1 | Wake-up I/O cause register identifies the wake-up I/O (WAKEUP pins) source from deep power-down mode. | 1B | Section 3.6 |
| USB.4 | In USB high-speed device mode, device writes extra byte(s) to the buffer if the NBytes is not multiple of 8 for OUT transfer | 1B | Section 3.7 |

Table 2. AC/DC deviations table

| AC/DC deviations | Short description | Product version(s) | Detailed description |
|------------------|-------------------|--------------------|----------------------|
| n/a | n/a | n/a | n/a |

Table 3. Errata notes

| Errata notes | Short description | Revision identifier | Detailed description |
|--------------|---|---------------------|---|
| ISP.1 | Devices with date code 2101 (yyww) and ROM patch version (T1.1.5) will have runBootloader API function. | 1B | Section 5.1 "ROM bootloader updated to provide API functionality for entry to ISP mode" |

3. Functional problems detail

3.1 ADC.1: Async interrupts with resume not supported

Introduction

The ADC controller is available on all LPC55S2x/LPC552x devices. Trigger detect with up to 16 trigger sources is supported with priority level configuration. A software or hardware trigger option is provided for each.

Problem

The following problems are all related to the restart after interrupt feature:

- Low priority trigger executes twice when resumed.
- Trigger can't restart when it is configured to do so.
- Incorrect trigger resumed after exception.

Work-around

There is no work-around.

The async interrupts with resume is not supported on device revisions 0A and 1B.

3.2 ROM.1: ROM fails to enter ISP mode when image is corrupted with flash pages in an erased or unprogrammed state

Introduction

On the LPC55S2x/LPC552x, if the image is corrupted with flash pages in an erased or unprogrammed state, the ROM may fail to automatically enter ISP mode.

Problem

When secure boot is enabled in CMPA, and the flash memory contains an erased or unprogrammed memory page inside the memory region specified by the image size field in the image header, the device does not automatically enter into ISP mode using the fallback mechanism, as in the case of a failed boot for an invalid image. This problem occurs when the application image is only partially written or erased but a valid image header is still present in memory.

Work-around

Perform a mass-erase to remove the incomplete and corrupted image using one of the following methods:

- Execute the erase command using Debug Mailbox. The device will enter directly into ISP mode after exiting the mailbox.
- Enter into ISP mode using the Debug Mailbox command and use the flash-erase command.
- Reset the device and enter into ISP mode using the ISP pin. Use the flash-erase command to erase the corrupted (incomplete) image.

3.3 USB.1: HS host fails when connecting with the LS device (mouse)

Introduction

The USB1 high-speed controller is available on select LPC55S2x/LPC552x devices and provides a plug-and-play connection of peripheral devices to a host with three different data speeds:

- high-speed with a data rate of 480Mbps.
- full-speed with a data rate of 12 Mbps.
- low-speed with a data rate of 1.5 Mbps.

Many portable devices can benefit from the ability to communicate with each other over the USB interface without intervention of a host PC.

Problem

USB HS host fails when connecting with an LS device (mouse).

Work-around

To support Full-Speed and Low-Speed applications, it is recommended to use the USB0 Full-Speed port and the USB1 High-speed port for Device or Host. In addition, should an application require support of Low-Speed USB devices with a USB High-Speed Host, this can be accomplished by inserting a USB Hub between the USB1 High-speed port and external USB devices.

3.4 USB.2: Automatic USB rate adjustment is not functional when using multiple hubs

Introduction:

Full-speed and low-speed signaling uses bit stuffing throughout the packet without exception. If the receiver sees seven consecutive ones anywhere in the packet, then a bit stuffing error has occurred, and the packet should be ignored.

The time interval just before an End of Packet (EOP) is a special case. The last data bit before the EOP can become stretched by hub switching skews. This is known as dribble and can lead to a situation where dribble introduces a sixth bit that does not require a bit stuff. Therefore, the receiver must accept a packet where there are up to six full bit times at the port with no transitions prior to the EOP.

Problem:

The LPC55S2x/LPC552x devices use the start of an EOP for frequency measurements. This is not functional when going through multiple hubs that introduce a dribble bit because of hub switching skews. For this reason, the start of the EOP cannot be used for frequency measurements for automatic USB rate adjustment (by setting USBCLKADJ in the FRO192M_CTRL register). The problem does not occur when a single hub is used.

Work-around:

Use the FRO calibration library provided in technical note TN00063. This library allows the application to have a crystal-less USB device operation in full-speed mode.

3.5 USB.3: For the USB high-speed device controller, the detection handshaking fails when certain full-speed hubs are connected

Introduction

See the USB2.0 specification for details regarding the USB High-speed Detection Handshake protocol.

Problem

As a high-speed device, when certain full-speed hubs are connected, the USB device does not detect the HOST KJ sequence correctly and, as a result, does not recognize the speed of the connected host. In this case, the USB device can act erratically due to the wrong speed detection.

Work-around

There are two workarounds:

1. The software work-around below can be implemented in `usb_dev_hid_mouse` where API is called `"USB_DeviceHsPhyChirpIssueWorkaround()"`. In event handler in `USB_DeviceCallback()`,
 - On `"kUSB_DeviceEventBusReset"` event, `USB_DeviceHsPhyChirpIssueWorkaround()` should be called to identify the speed of the host connected to. If full-speed host is connected or `"isConnectedToFshostFlag"` is set, `FORCE_FS` (bit 21) of `DEVCMSTAT` register should be set to force the device operating in full-speed mode.
 - On `"kUSB_DeviceEventDetach"` event, `FORCE_FS` (bit 21) of `DEVCMSTAT` register should be cleared.
2. The software work-around below is available in tech note (TN00071) In event handler in `USB_DeviceCallback()`,
 - On `"kUSB_DeviceEventAttach"` event, set `PHY_RX` register trip-level voltage to the highest. `USBPHY->RX &= ~(USBPHY_RX_ENVADJ_MASK); USBPHY->RX |= 2;`
 - On `"kUSB_DeviceEventBusReset"` event, check the `DEVCMSTAT[SPEED]` to determine the connected bus speed. (`SPEED` are bits 22 and 23). If `DEVCMSTAT[SPEED]=FS`, `FORCE_FS` (bit 21) of `DEVCMSTAT` should be set to force the device operating in full-speed mode.
 - On `"kUSB_DeviceEventGetDeviceDescriptor"` event, or first `SETUP` packet has arrived, Set the `USBPHY_RX[ENVADJ]` field back to default 0. Otherwise, `USBPHY_RX[ENVADJ]` field will remain as 2 unless a disconnect event occurs.
 - On `"kUSB_DeviceEventDetach"` event, Clear `FORCE_FS` (bit 21) of `DEVCMSTAT` register to zero. Reset `USBPHY_RX[ENVADJ]` field back to default 0.

3.6 WAKEIO.1: Wake-up I/O register reports incorrect wake-up source

Introduction

On the LPC55S2x/LPC552x, a wake-up I/O cause register is available to identify the wake-up I/O (WAKEUP pins) source from deep power-down mode.

Problem

Before entering DEEP-POWER-DOWN, the following configuration is set for the wake-up sources:

- Wake-up I/O 0 as falling edge.
- Wake up I/O 1 as rising edge.
- Wake up I/O 2 is disabled.
- Wake up I/O 3 as falling edge.

1st case: The first wake up event is a rising edge on wake up I/O 1. PMC->WAKEIOCAUSE will indicate Wake-up I/O 0 trigger (wrong), Wake up I/O 1 trigger (correct) and Wake up I/O 3 trigger (wrong) as wake up I/O cause.

2nd case: The first wake up event is a falling edge on wake up I/O 3. PMC->WAKEIOCAUSE will indicate Wake-up I/O 0 trigger (wrong) and Wake up I/O 3 trigger (correct) as wake up I/O cause.

3rd case: The first wake up event is an RTC. PMC->WAKEIOCAUSE will indicate Wake-up I/O 0 trigger (wrong) and Wake up I/O 3 trigger (wrong) as wake up I/O cause.

Work-around

None. This issue does not occur when the wake I/O is not configured as falling edge.

3.7 USB.4: In USB high-speed device mode, device writes extra byte(s) to the buffer

Introduction

The LPC55S2x/LPC552x device family include a USB high-speed interface (USB1) that can operate in device mode at high-speed. The NBytes value represents the number of bytes that can be received in the buffer.

Problem

The LPC55S2x/LPC552x USB device controller writes extra bytes to the receive data buffer if the size of the transfer is not a multiple of 8 bytes since the USB device controller always writes 8 bytes. For example, if the transfer length is 1 bytes, 7 extra bytes will be written to the receive data buffer. If the transfer length is 7 bytes, 1 extra bytes will be written to the receive data buffer.

Work-around

Reserve an additional, intermediary buffer along with the buffer used by the application for USB data. After the USB data transfer into the intermediary buffer has been completed, use memcopy to move the data from the intermediary buffer into the application buffer, skipping the extraneous extra byte. This software work-around is implemented on the SDK software platform.

4. AC/DC deviations detail

No known errata.

5. Errata notes detail

5.1 ROM bootloader updated to provide API functionality for entry to ISP mode

ISP.1: Devices with date code 2101 (yyww) and ROM patch version (T1.1.5), the ROM bootloader will be updated to provide an API (runBootloader API) for the user application to enter the ISP mode based on the designated ISP interface mode.

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