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April 1st, 2010
Renesas Electronics Corporation

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R8C/38C Group

Timer RG PWM Mode (Buffer Operation)

1. Abstract

This document describes the setting method and an application example of PWM waveform output and duty change using R8C/38C Group timer RG PWM mode (buffer operation).

2. Introduction

The application example described in this document applies to the following MCU:

- MCU : R8C/38C Group

The sample program in this application note can be used with other R8C/38C Group MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using this application note.

3. Application Example

3.1 Program Outline

A PWM waveform of 100 μs period/variable duty is output from the TRGIOA pin in timer RG PWM mode. High duty of PWM output is output from 10% to 100% every 10% in 10 ms intervals using timer RB. Buffer operation of the general register is used to change duty cycles. The PWM output duty changes 10% → 20% → ... → 90% → 100% → 90% → ... → 10% → 20% → 30% → ... repeatedly.

Main settings

- The high-speed on-chip oscillator (fOCO40M) is used for the count source.
- The timer RG counter (TRG) is cleared at the compare match with the general register (TRGGRA).
- The general register (TRGGRD) is used as the buffer register of the TRGGRB register.
- High-level output is set for a PWM waveform at the compare match of registers TRG and TRGGRA. Low-level output is set for a PWM waveform at the compare match of registers TRG and TRGGRB (PWM mode).

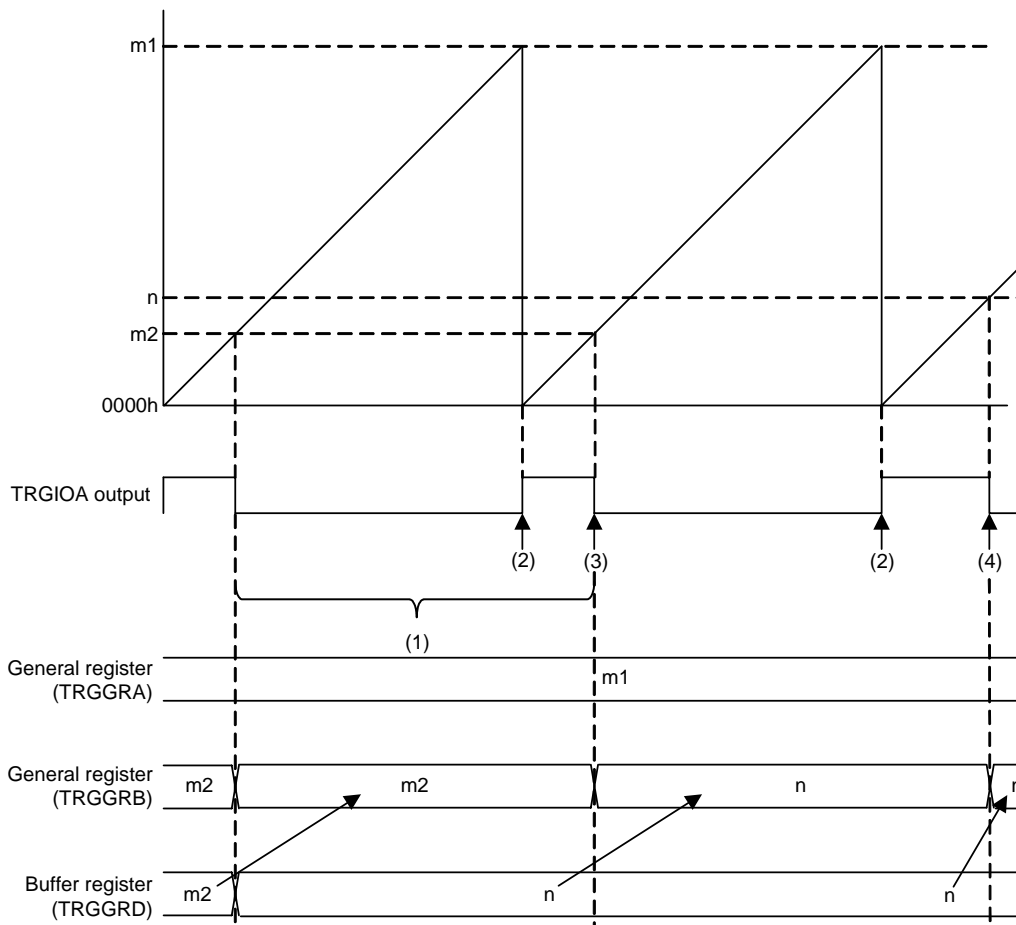
Formula for PWM period

$$\begin{aligned}
 100 \mu\text{s} &= 1 \div \text{fOCO40M} \times (\text{TRGGRA} + 1) \\
 &= 1 \div 40 \text{ MHz} \times (39999 + 1) \\
 &= 25 \text{ ns} \times 4000
 \end{aligned}$$

Table 3.1 lists the pin used and its function. Figure 3.1 shows the buffer operating example in PWM mode and Figures 3.2 to 3.6 show output timing charts when changing duty cycles.

Table 3.1 Pin and Function

Pin Name	I/O	Function
P5_6/TRGIOA	Output	PWM output



	Hardware Handling	Software Handling
(1)	–	(a) Set TRGGRD (n).
(2)	(a) Values of TRG and TRGGRA (m1) match. (b) Clear TRG to 0000h. (c) High-level output from the TRGIOA pin	–
(3)	(a) Values of TRG and TRGGRB (m2) match. (b) Transfer the value of TRGGRD (n) which is used as the buffer register to TRGGRB. (c) Low-level output from the TRGIOA pin	–
(4)	(a) Value of TRG and TRGGRB (n) match. (b) Transfer the value of TRGGRD (n) which is used as the buffer register to TRGGRB. (c) Low-level output from the TRGIOA pin	–

m1: TRGGRA value (4000-1)

m2: TRGGRB value for duty XX%

n: TRGGRD value for duty YY% and TRGGRB value after duty cycle changes

TRG: Timer RG counter

TRGGRA: Timer RG general register A

TRGGRB: Timer RG general register B

TRGGRD: Timer RG general register D

Figure 3.1 Buffer Operating Example in PWM Mode

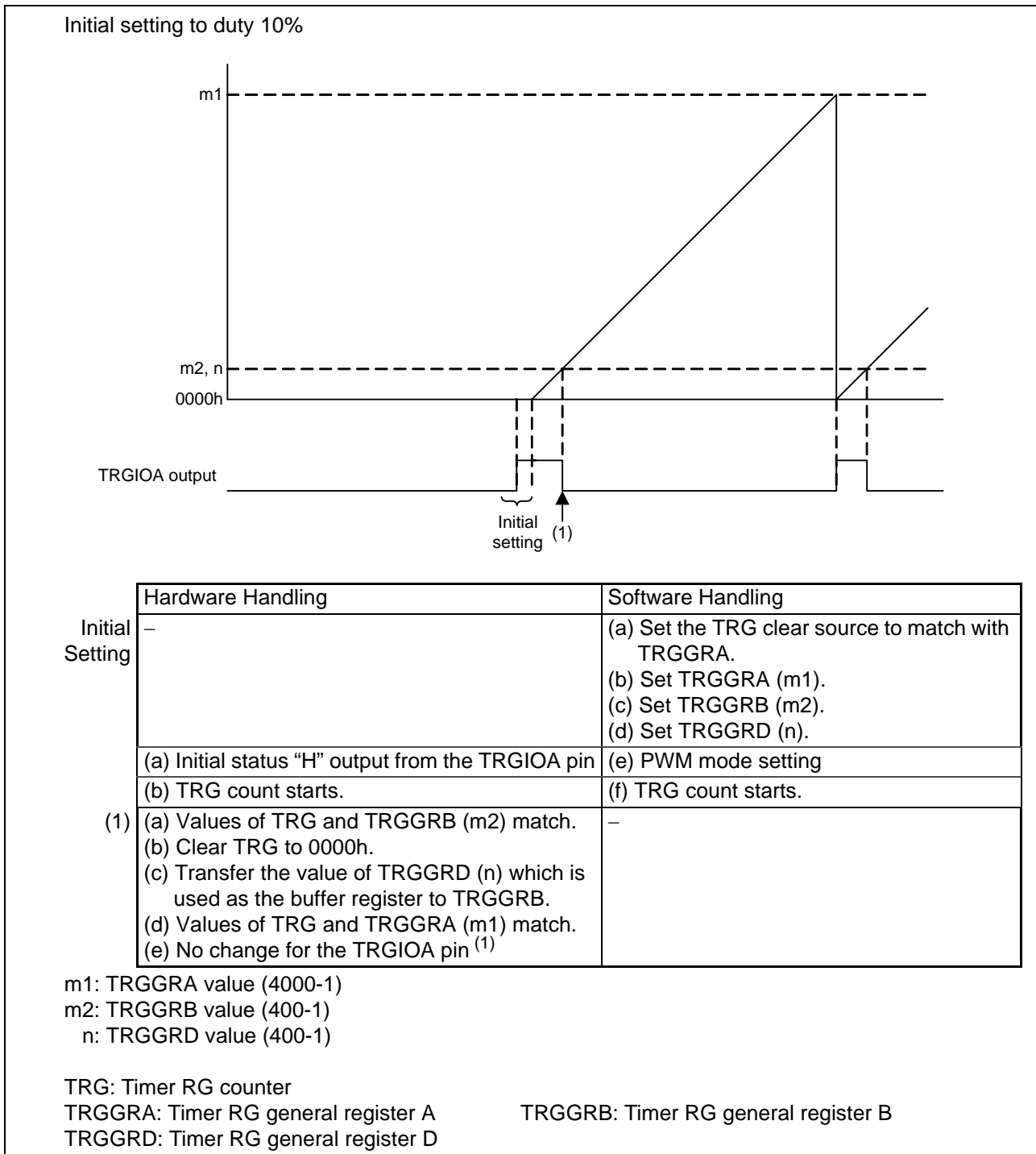


Figure 3.2 Output Timing Chart When Changing Duty Cycles (1)

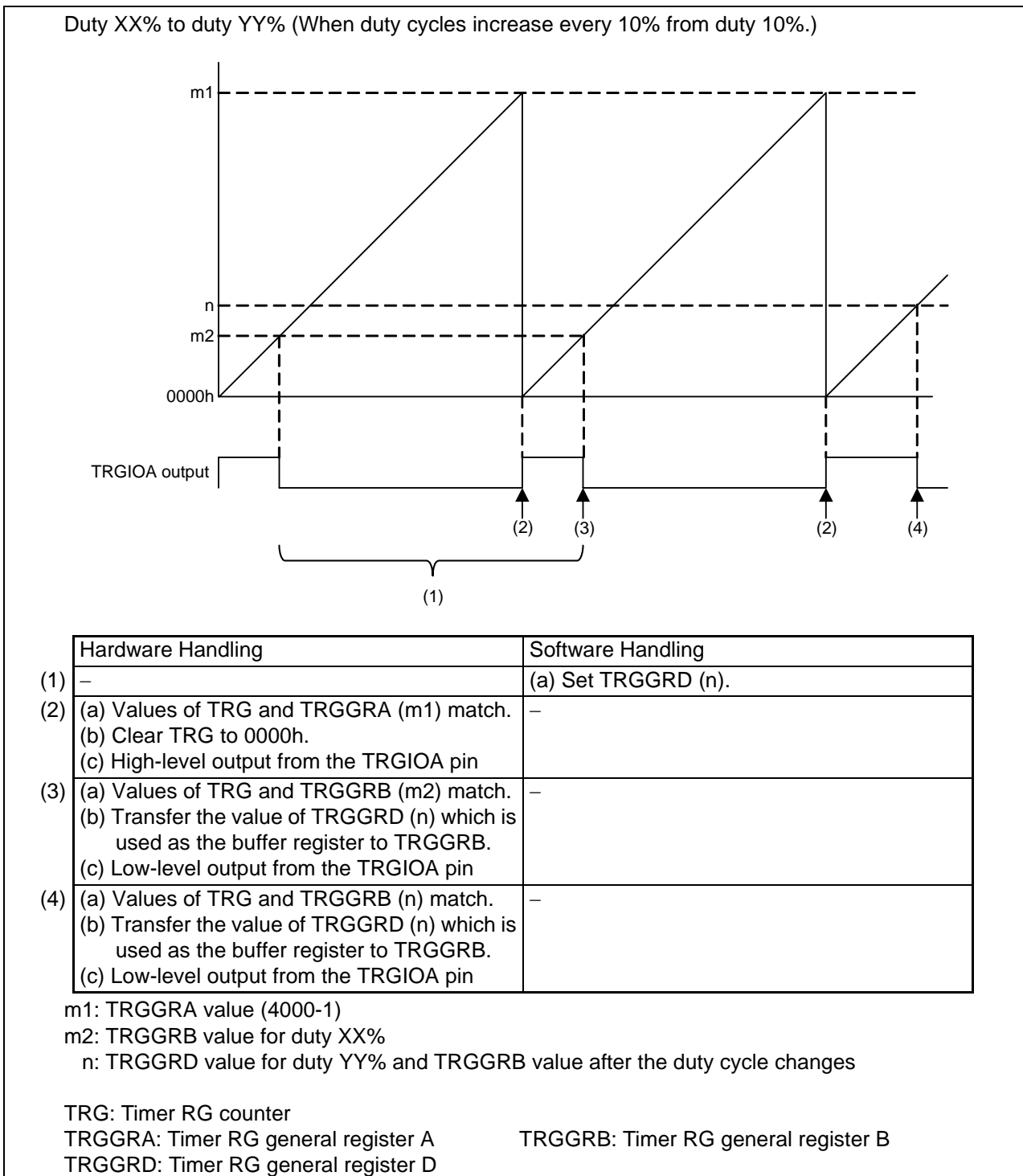


Figure 3.3 Output Timing Chart When Changing Duty Cycles (2)

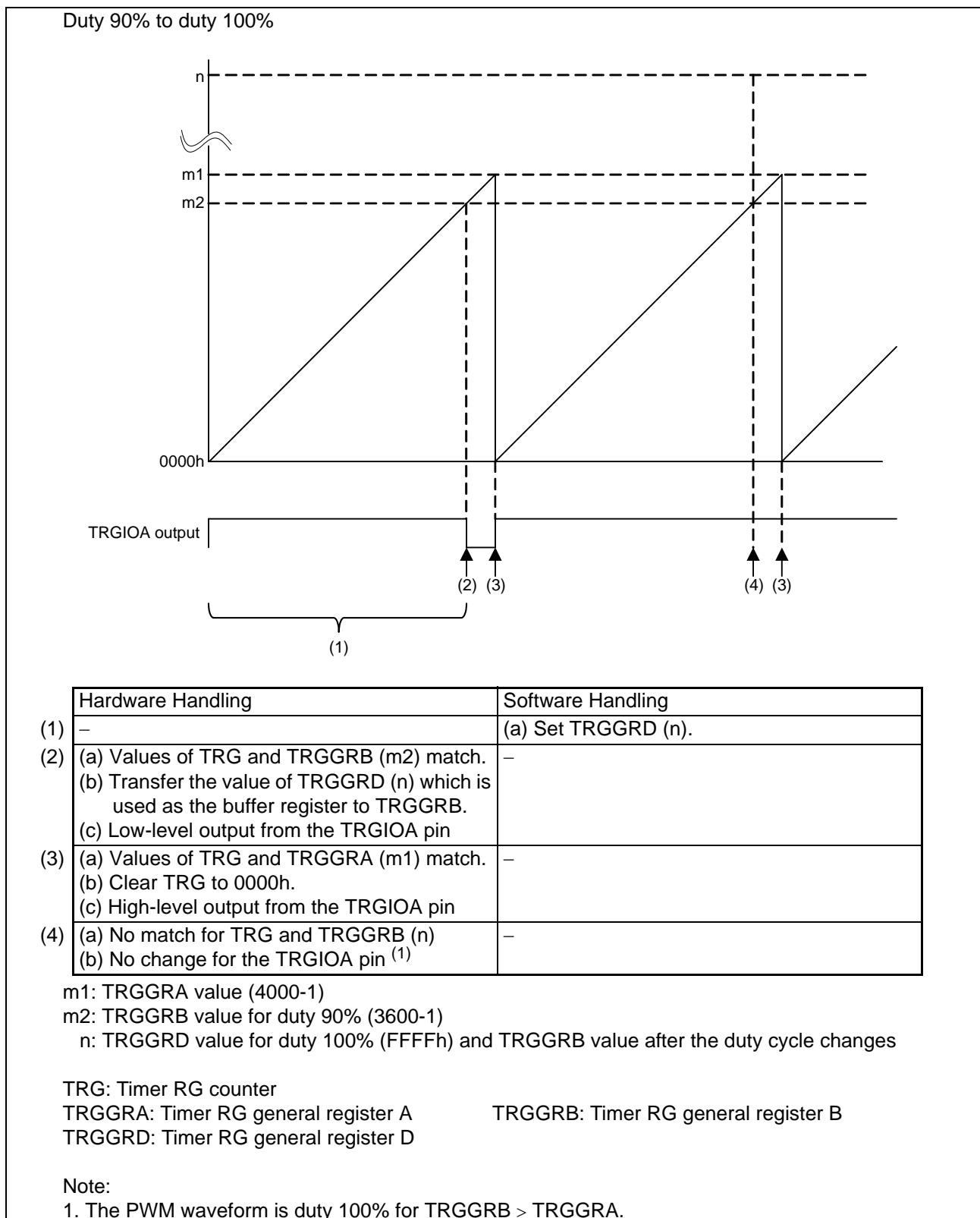


Figure 3.4 Output Timing Chart When Changing Duty Cycles (3)

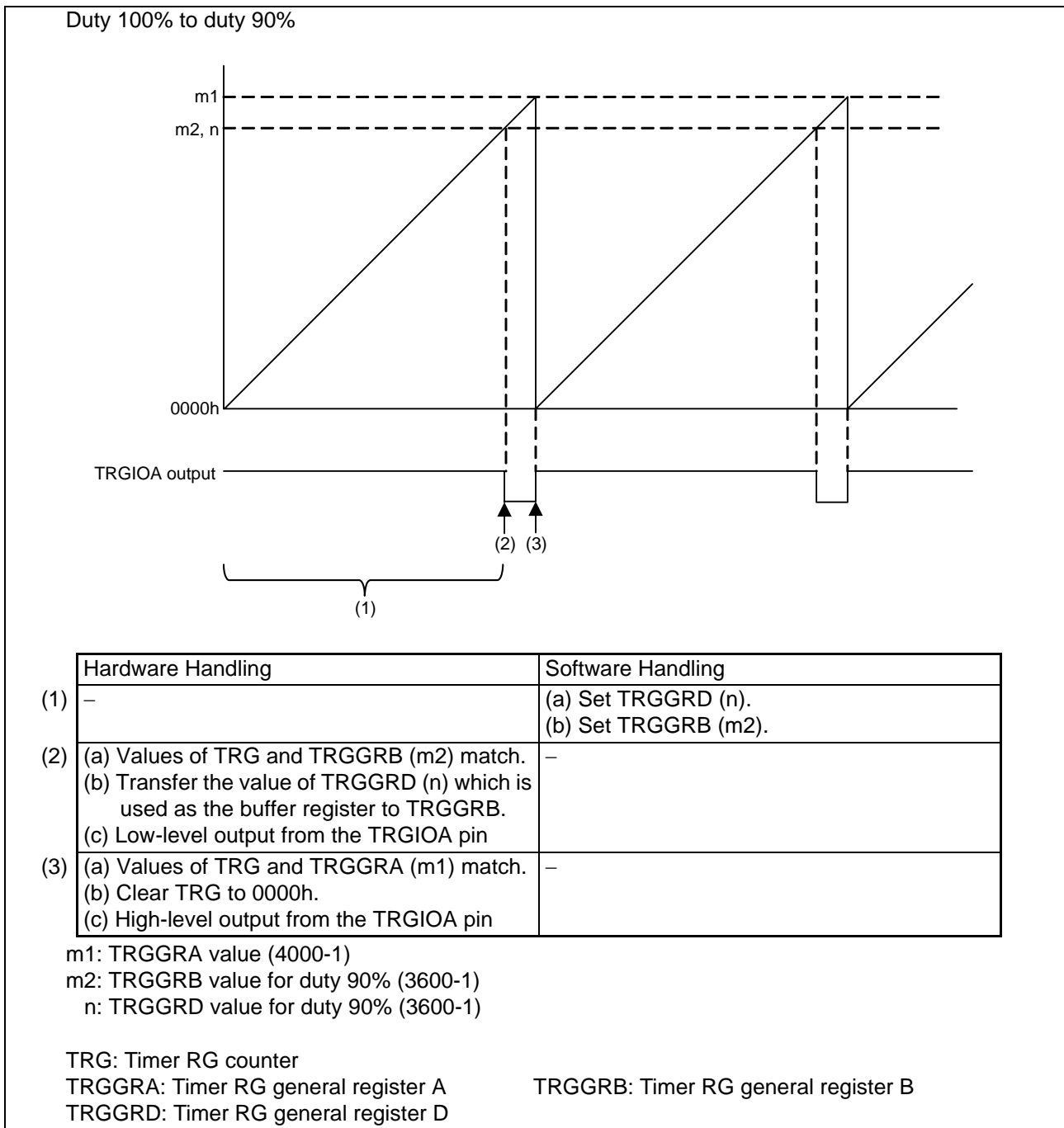


Figure 3.5 Output Timing Chart When Changing Duty Cycles (4)

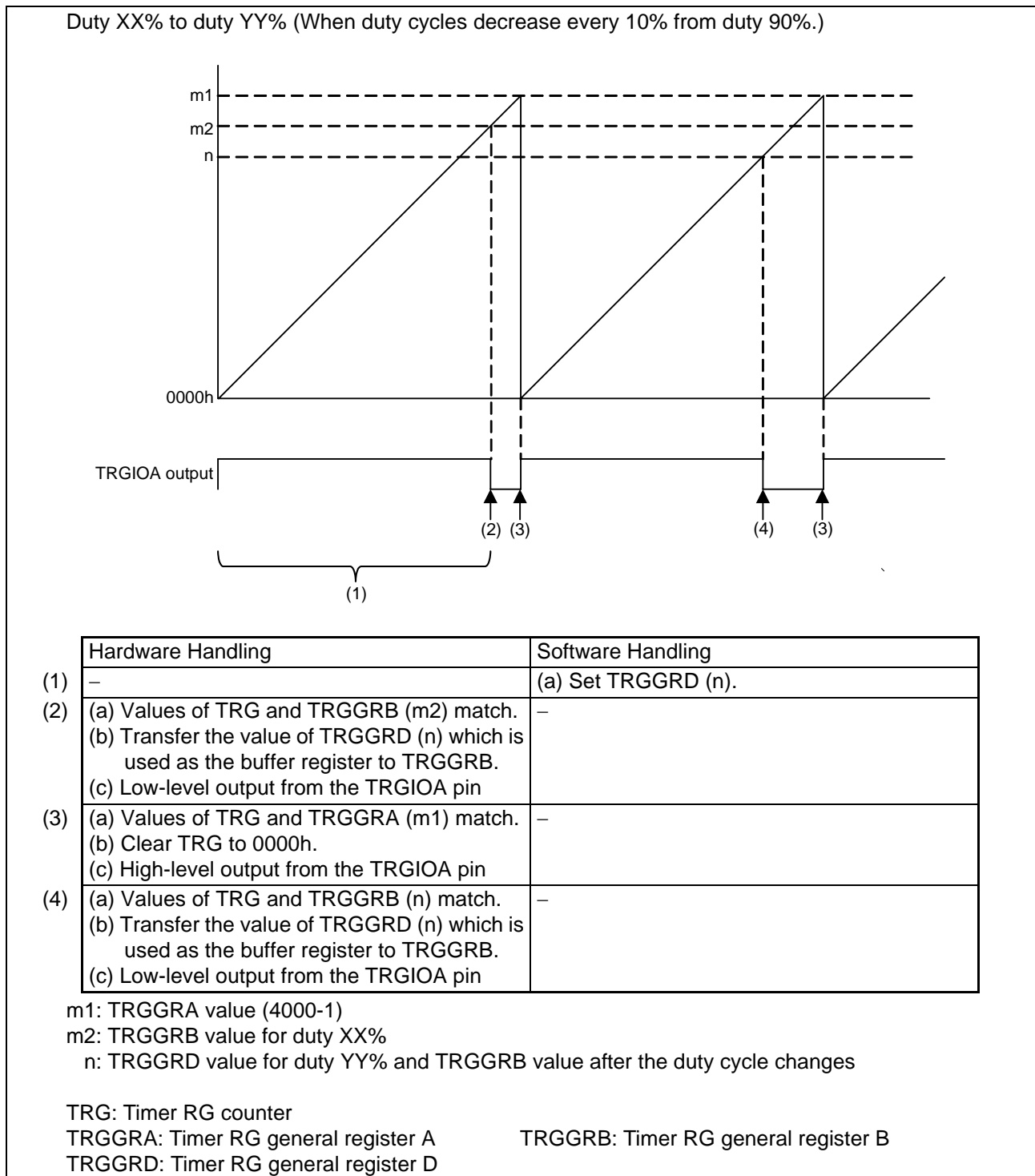


Figure 3.6 Output Timing Chart When Changing Duty Cycles (5)

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	319 bytes	In the rej05b1163_src.c module
RAM	1 byte	In the rej05b1163_src.c module
Maximum user stack	9 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.

The above applies to the following conditions:

- C compiler: M16C/60, 30, 20, 10, and Tiny, and R8C/Tiny Series Compiler V.5.45 Release 00
- Compile option: -c -finfo -dir "\$(CONFIGDIR)" -R8C

4. Software Outline

This section shows the initial setting procedures and values to set the example described in section 3. **Application Example.** Refer to the latest **R8C/38C Group Hardware Manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The system clock (high-speed on-chip oscillator) is set.		

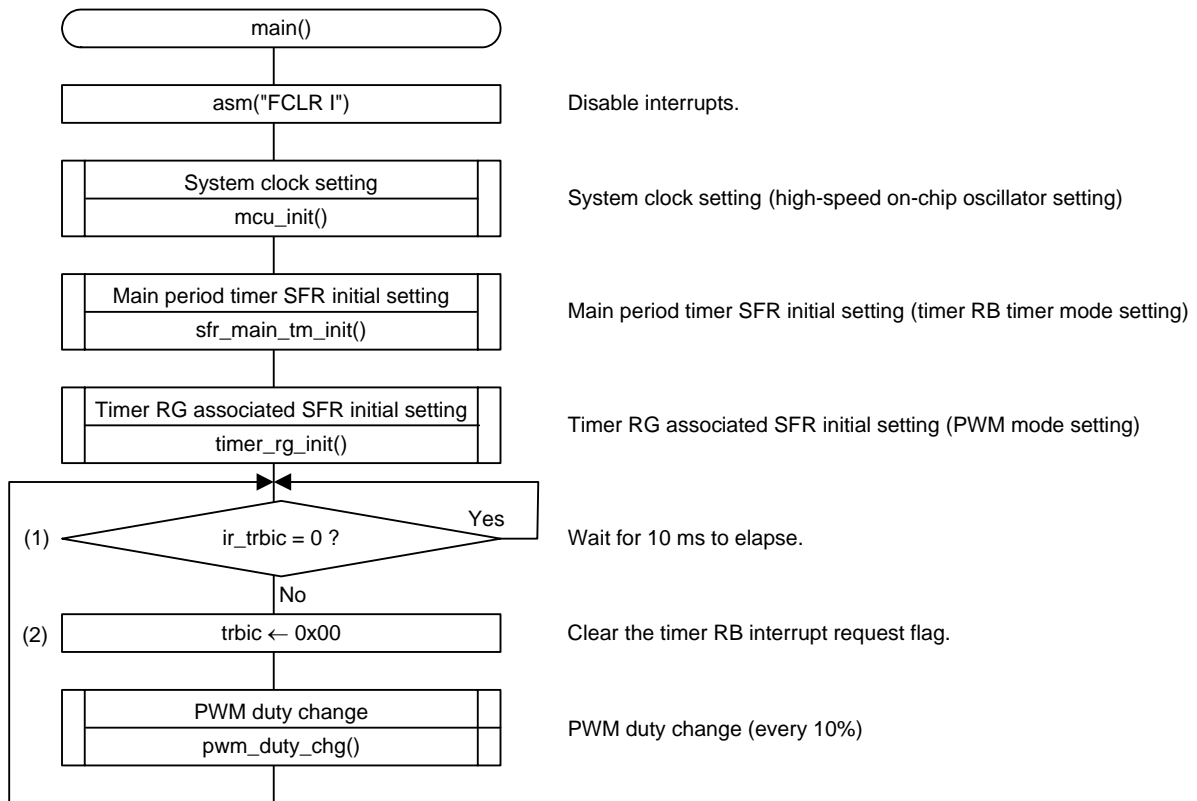
Declaration	void sfr_main_tm_init(void)		
Outline	Main period timer SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The SFR register is initialized to use timer RB in timer mode.		

Declaration	void timer_rg_init(void)		
Outline	Timer RG associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	The SFR register is initialized to use timer RG in PWM mode (buffer operation).		

Declaration	void pwm_duty_chg(void)		
Outline	PWM duty change		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char duty_mode		RAM for duty mode control
Returned value	Type	Value	Meaning
	None	—	—
Function	Change the PWM duty cycle from 10% to 100% and from 100% to 10%.		

4.2 Main Function

• Flowchart



• Register Settings

(1) Wait until the timer RB interrupt request is generated.

Interrupt Control Register (TRBIC)

Bit	Symbol	Bit Name	Function	R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W

(2) Clear the timer RB interrupt request flag.

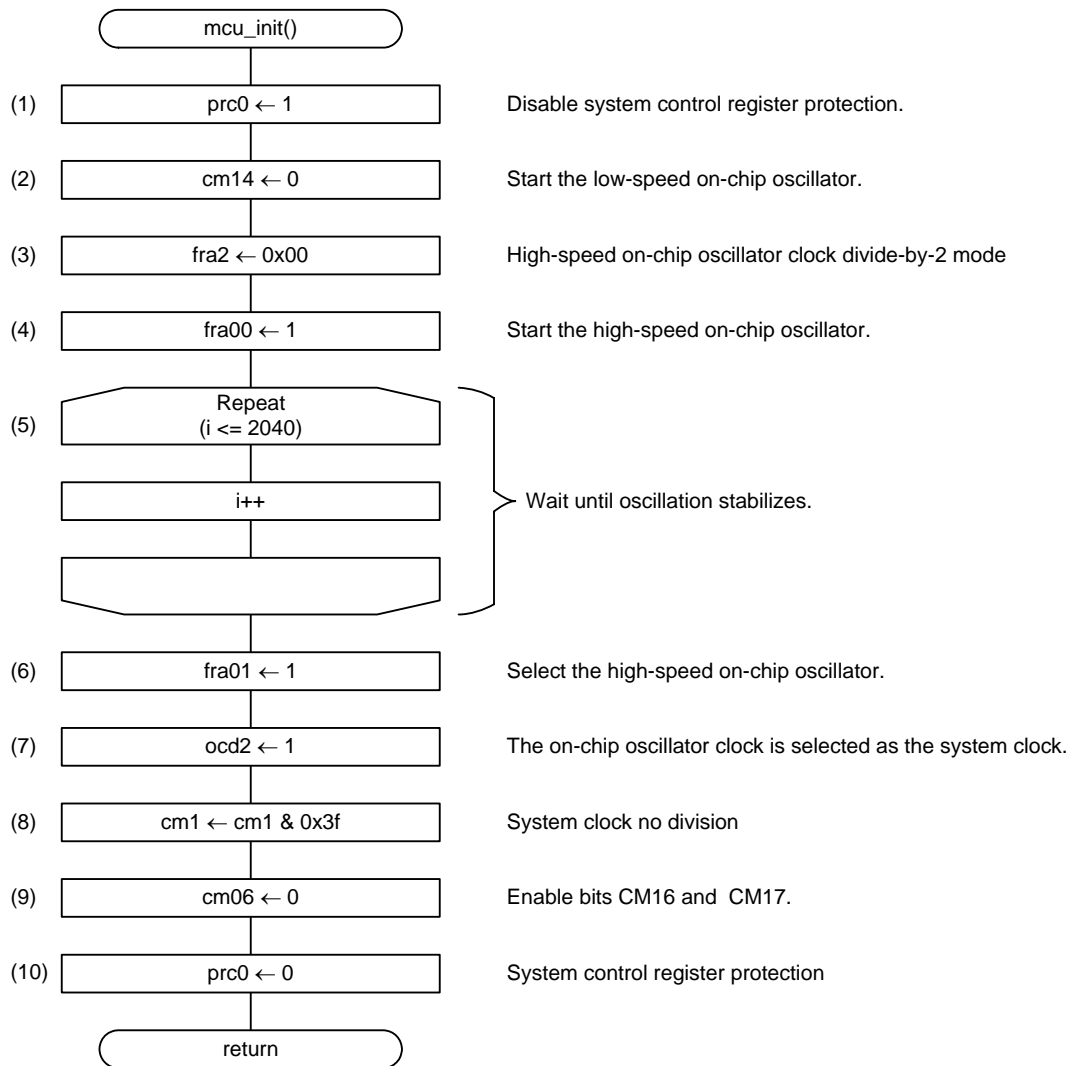
Interrupt Control Register (TRBIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR			Interrupt request bit

4.3 System Clock Setting

• Flowchart



• Register Settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the divide ratio of the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division clock for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock division select bit 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock division select bit 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

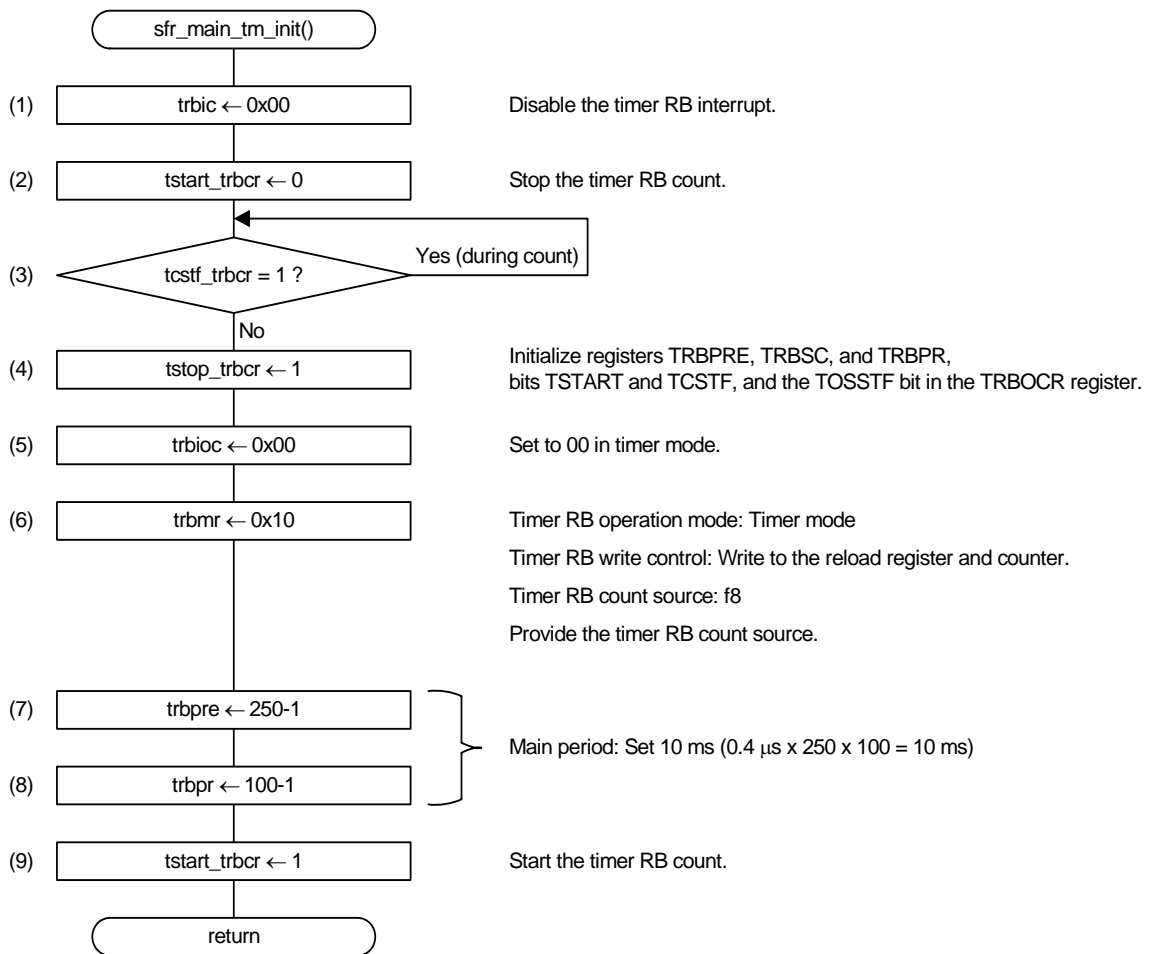
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Main Period Timer SFR Initial Setting

• Flowchart



• Register Settings

(1) Disable the timer RB interrupt.

Interrupt Control Register (TRBIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(2) Stop the timer RB count.

Timer RB Control Register (TRBCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit	0: Count stops	R/W

(3) Wait until the timer RB count stops.

Timer RB Control Register (TRBCR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RB count status flag	0: Count stops 1: During count	R

(4) Initialize registers TRBPRE, TRBSC, and TRBPR, bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register.

Timer RB Control Register (TRBCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	1		

Bit	Symbol	Bit Name	Function	R/W
b2	TSTOP	Timer RB count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W

(5) Set the timer RB I/O control register.

Timer RB I/O Control Register (TRBIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W

(6) Set the timer RB mode register.

Timer RB Mode Register (TRBMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	0	1	0	—	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bit	b1 b0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b3	TWRC	Timer RB write control bit	0: Write to reload register and counter	R/W
b4	TCK0	Timer RB count source select bit	b5 b4 0 1: f8	R/W
b5	TCK1			R/W
b7	TCKCUT	Timer RB count source cutoff bit	0: Provides count source	R/W

(7) Set 250-1 (F9h) to the timer RB prescaler register.

Timer RB Prescaler Register (TRBPRES)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	0	0	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(8) Set 100-1 (63h) to the timer RB primary register.

Timer RB Primary Register (TRBPR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	1	1	0	0	0	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RB prescaler underflows	00h to FFh	R/W

(9) Start the timer RB count.

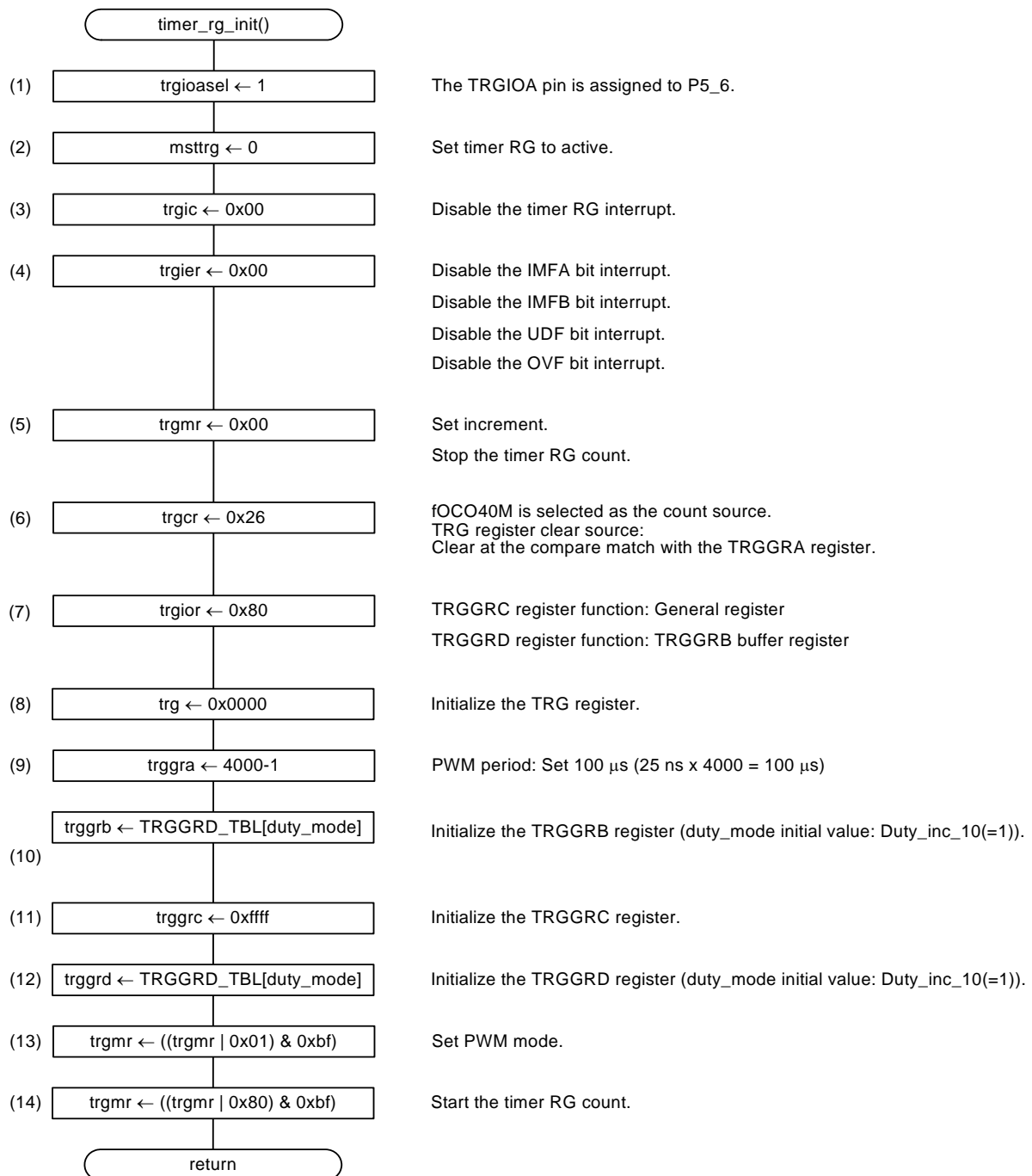
Timer RB Control Register (TRBCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit	1: Count starts	R/W

4.5 Timer RG Associated SFR Initial Setting

• Flowchart



• Register Settings

(1) The TRGIOA pin is assigned to P5_6.

Timer Pin Select Register (TIMSR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	1	—	x	—	x

Bit	Symbol	Bit Name	Function	R/W
b4	TRGIOASEL	TRGIOA pin select bit	1: P5_6 pin assigned	R/W

(2) Set timer RG to active.

Module Standby Control Register (MSTCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	x	x	x	—	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	MSTTRG	Timer RG standby bit	0: Active	R/W

(3) Disable the timer RG interrupt.

Interrupt Control Register (TRGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—		0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R

(4) Set the timer RG interrupt enable register.

Timer RG Interrupt Enable Register (TRGIER)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input-capture/compare-match interrupt enable bit A	0: Interrupt by IMFA flag disabled	R/W
b1	IMIEB	Input-capture/compare-match interrupt enable bit B	0: Interrupt by IMFB flag disabled	R/W
b2	UDIE	Underflow interrupt enable bit	0: Interrupt by UDF flag disabled	R/W
b3	OVIE	Overflow interrupt enable bit	0: Interrupt by OVF flag disabled	R/W

(5) Set the timer RG mode register.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	—	x	x	x	x	0	

Bit	Symbol	Bit Name	Function	R/W
b1	MDF	Phase counting mode select bit	0: Increment	R/W
b7	TSTART	TRG count start bit	0: Count stops	R/W

(6) Set the timer RG control register.

Timer RG Control Register (TRGCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	0	1	x	x	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TCK0	Count source select bit	b2 b1 b0 1 1 0: fOCO40M	R/W
b1	TCK1			R/W
b2	TCK2			R/W
b5	CCLR0	TRG register clear source select bit	b6 b5 0 1: TRG register cleared by input capture or compare match with TRGGRA register	R/W
b6	CCLR1			R/W

(7) Set the timer RG I/O control register.

Timer RG I/O Control Register (TRGIOR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	x	x	x	0	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b3	BUFA	TRGGRC register function select bit	0: Not used as the buffer register of the TRGGRA register	R/W
b7	BUFB	TRGGRD register function select bit	1: Used as the buffer register of the TRGGRB register	R/W

(8) Initialize the timer RG counter to 0000h.

Timer RG Counter (TRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	In PWM mode, count operation is increment.	0000h to FFFFh	R/W

(9) Set the compare value 4000-1 (0F9Fh) with the timer RG counter to the timer RG general register A.

Timer RG General Register A (TRGGRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	1	1	1	1	1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	1	1	1	1

Bit	Function	R/W
b15 to b0	Compare value with TRG register	R/W

(10) Initialize the timer RG general register B to 400-1 (018Fh).

Timer RG General Register B (TRGGRB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	0	1	1	1	1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	R/W
b15 to b0	Compare value with TRG register	R/W

(11) Initialize the timer RG general register C to 0FFFFh.

Timer RG General Register C (TRGGRC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	1	1	1	1	1	1	1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Compare value with TRG register	R/W

(12) Initialize the timer RG general register D to 400-1 (018Fh).

Timer RG General Register D (TRGGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	0	0	0	1	1	1	1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0	0	0	0	0	0	0	1

Bit	Function	R/W
b15 to b0	Compare value with TRG register	R/W

(13) Set PWM mode.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value		—	x	x	x	x		1

Bit	Symbol	Bit Name	Function	R/W
b0	PWM	PWM mode select bit	1: PWM mode	R/W

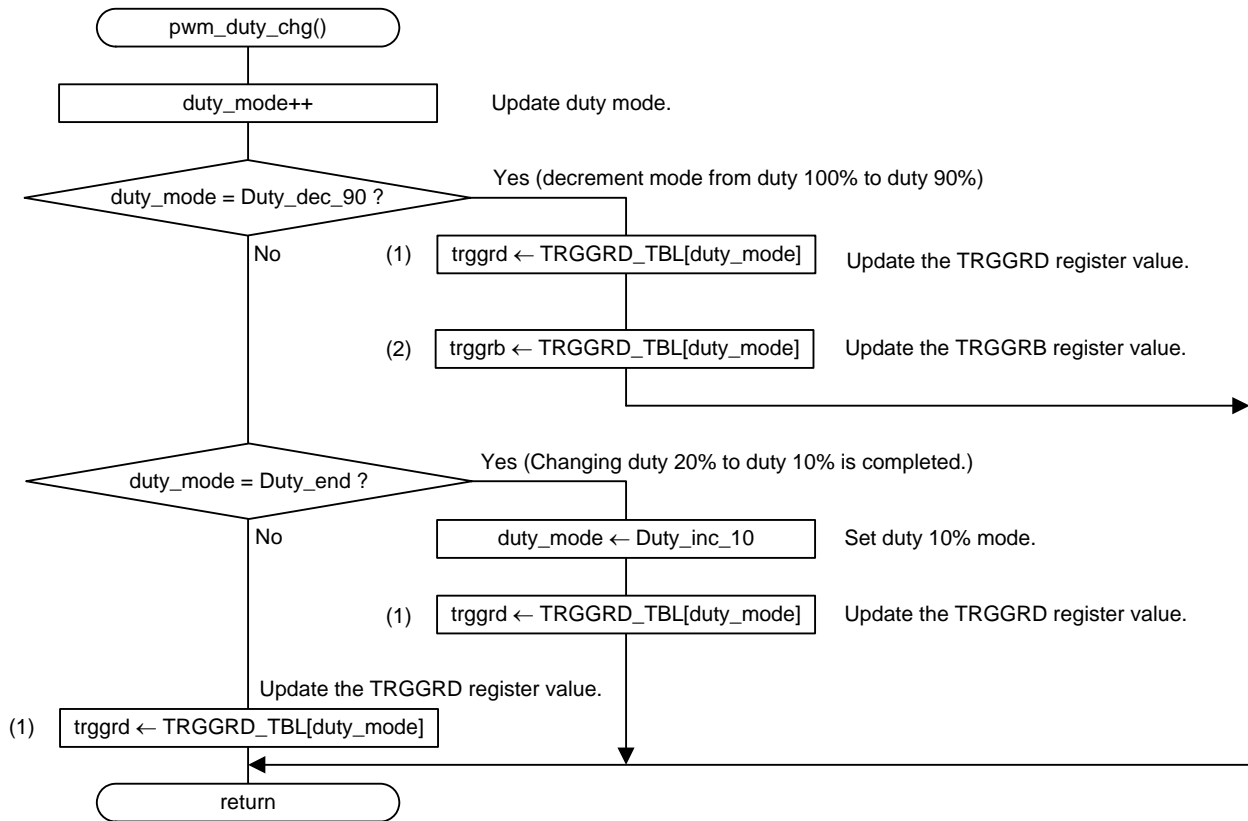
(14) Start the count for the timer RG counter.

Timer RG Mode Register (TRGMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	1	—	x	x	x	x		

Bit	Symbol	Bit Name	Function	R/W
b7	TSTART	TRG count start bit	1: Count starts	R/W

4.6 PWM Duty Change



• Register Settings

(1) Update the timer RG general register D value.

Timer RG General Register D (TRGGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	R/W
b15 to b0	Compare value with TRG register	R/W

(2) Update the timer RG general register B value. Since the compare match of registers TRG and TRGGRB does not occur and buffer transfer from the TRGGRD register is not performed when the TRGGRB register setting is duty 100%, setting the TRGGRB register by a program is necessary.

Timer RG General Register B (TRGGRB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Bit	b15	b14	b13	b12	b11	b10	b9	b8
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	Function	R/W
b15 to b0	Compare value with TRG register	R/W

5. Sample Program

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu of the R8C/Tiny Family page.

6. Reference Documents

Hardware Manual
R8C/38C Group Hardware Manual Rev.0.10
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
<http://www.renesas.com/>

Inquiries
<http://www.renesas.com/inquiry>
csc@renesas.com

REVISION HISTORY	R8C/38C Group Timer RG PWM Mode (Buffer Operation)
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 29, 2009	-	First Edition issued

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