ADSP-BF533 EZ-KIT Lite®
Evaluation System Manual

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Analog Devices, Inc.
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ANALOG DEVICES

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Regulatory Compliance

The ADSP-BF533 EZ-KIT Lite is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF533 EZ-KIT Lite has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC amended by 93/68/EEC and therefore carries the "**CE**" mark.

The ADSP-BF533 EZ-KIT Lite has been appended to Analog Devices, Inc. Technical Construction File (TCF) referenced '**DSPTOOLS1**' dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body as listed below.

Technical Certificate No: Z600ANA1.011

Issued by:

Technology International (Europe) Limited
60 Shrivenham Hundred Business Park
Shrivenham, Swindon, SN6 8TY, UK

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

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PREFACE

USING THE ADSP-BF533 EZ-KIT LITE

PREFACE

Thank you for purchasing the ADSP-BF533 EZ-KIT Lite®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test the capabilities of the ADSP-BF533 Blackfin processors. The development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-BF533 assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-BF533 processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-BF533 processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to http://www.analog.com/dsp/tools.

The ADSP-BF533 EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

Product Overview

The board features:

- Analog Devices ADSP-BF533 Blackfin processor
  - Performance up to 600 MHz
  - 160-pin mini-BGA package
  - 27 MHz `CLKIN` oscillator
- Synchronous dynamic random access memory (SDRAM)
  - MT48LC32M16 - 64 MB (32M x 16 bits)
- Flash memories
  - 2 MB (512K x 16 x 2chips)
- Analog audio interface
  - AD1836 – Analog Devices 96 kHz audio codec
  - 4 input RCA phono jacks (2 channels)
  - 6 output RCA phono jacks (3 channels)
- Analog video interface
  - ADV7183 video decoder w/ 3 input RCA phono jacks
  - ADV7171 video encoder w/ 3 output RCA phono jacks
- Universal asynchronous receiver/transmitter (UART)
  - ADM3202 RS-232 line driver/receiver
  - DB9 male connector

- LEDs
    - 10 LEDs: 1 power (green), 1 board reset (red), 1 USB (red), 6 general-purpose (amber), and 1 USB monitor (amber)
- Push buttons
    - 5 push buttons with debounce logic: 1 reset, 4 programmable flags
- Expansion interface
    - PPI, SPI, EBIU, Timers2-0, UART, programmable flags, SPORT0, SPORT1
- Other features
    - JTAG ICE 14-pin header

The EZ-KIT Lite board has two flash memories with a total of 2 MB of memory. The flash memories can be used to store user-specific boot code, allowing the board to run as a stand-alone unit. For more information, see "Flash Memory" on page 1-15. The board also has 64 MB of SDRAM, which can be used by the user at runtime.

SPORTs interface with the AD1836 audio codec to aid development of audio signal processing applications. SPORT0 also attaches to an off-board connector for communication with other serial devices. For information about SPORT0, see "SPORT Audio Interface" on page 2-3.

The parallel peripheral interface (PPI) of the processor connects to both a video encoder and video decoder, facilitating development of video signal processing applications.

The UART of the processor connects to an RS-232 line driver and a DB9 male connector, providing an interface to a PC or other serial device.

Additionally, the EZ-KIT Lite board provides access to most of the processor's peripheral ports. Access is provided in the form of a

three-connector expansion interface. For information about the expansion interface, see “Expansion Interface” on page 2-8.

Purpose of This Manual

The *ADSP-BF533 EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes the operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF533 EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts that describe your target architecture. For the locations of these documents, see “Related Documents”.

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user’s manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-BF533 EZ-KIT Lite" on page 1-1
  Describes the EZ-KIT Lite functionality from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-BF533 EZ-KIT Lite Hardware Reference" on page 2-1
  Provides information on the EZ-KIT Lite hardware components.
- Appendix A, "ADSP-BF533 EZ-KIT Lite Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1
  Provides the resources to allow board-level debugging or to use as a reference design. Appendix B is part of the online help.

What's New in This Manual

This is revision 3.2 of the *ADSP-BF533 EZ-KIT Lite Evaluation System Manual*. The manual has been updated to include CCES information. Additional changes include the following.

- The "Configuring Flash Memory" section has been updated to reflect obsoleted flash memory devices.
- Modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  http://ez.analog.com/community/dsp
- Submit your questions to technical support directly at:
  http://www.analog.com/support
- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to processor.tools.support@analog.com and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.
- E-mail your questions about processors and processor applications to:
  processor.support@analog.com or
  processor.china@analog.com (Greater China support)
- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)
- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  www.analog.com/adi-sales

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF533 Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information

about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

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EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin Embedded Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF533 Blackfin Processor Hardware Reference	Description of the internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.

Example	Description
filename	Non-keyword placeholders appear in text with italic style format.
	**Note:** For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	**Caution:** Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	**Warning:** Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING THE ADSP-BF533 EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-BF533 EZ-KIT Lite evaluation system.

The information appears in the following sections.

- "SDRAM Interface" on page 1-13·
  Defines the register values to configure the on-board SDRAM.
- "Flash Memory" on page 1-15
  Describes the on-board flash memory.
- "LEDs and Push Buttons" on page 1-19
  Describes the board's general-purpose IO pins and buttons.
- "Audio Interface" on page 1-20
  Describes the board's audio interface.
- "Video Interface" on page 1-21
  Describes the board's video interface.
- "Board Design Database" on page 1-22
  Provides information about board design.
- "Example Programs" on page 1-22
  Provides information about the example programs included in the ADSP-BF533 EZ-KIT Lite evaluation system.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online help.

For more detailed information about programming the ADSP-BF533 Blackfin processor, see the documents referred to at "Related Documents".

Package Contents

Your ADSP-BF533 EZ-KIT Lite evaluation system package contains the following items.

- ADSP-BF533 EZ-KIT Lite board
- Universal 7.5V DC power supply
- USB 2.0 type cable

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.

The ADSP-BF533 EZ-KIT Lite board is designed to run outside your personal computer as a standalone unit.

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. Figure 1-1 shows the default jumper settings, DIP switch, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

To connect the EZ-KIT Lite board:

1. Plug the provided power supply into J9 on the EZ-KIT Lite board. Visually verify that the green power LED (LED1) is on. Also verify that the red reset LED (LED2) goes on for a moment and then goes off.
2. Connect one end of the USB cable to an available full speed USB port on your PC and the other end to ZJ1 on the ADSP-BF533 EZ-KIT Lite board.

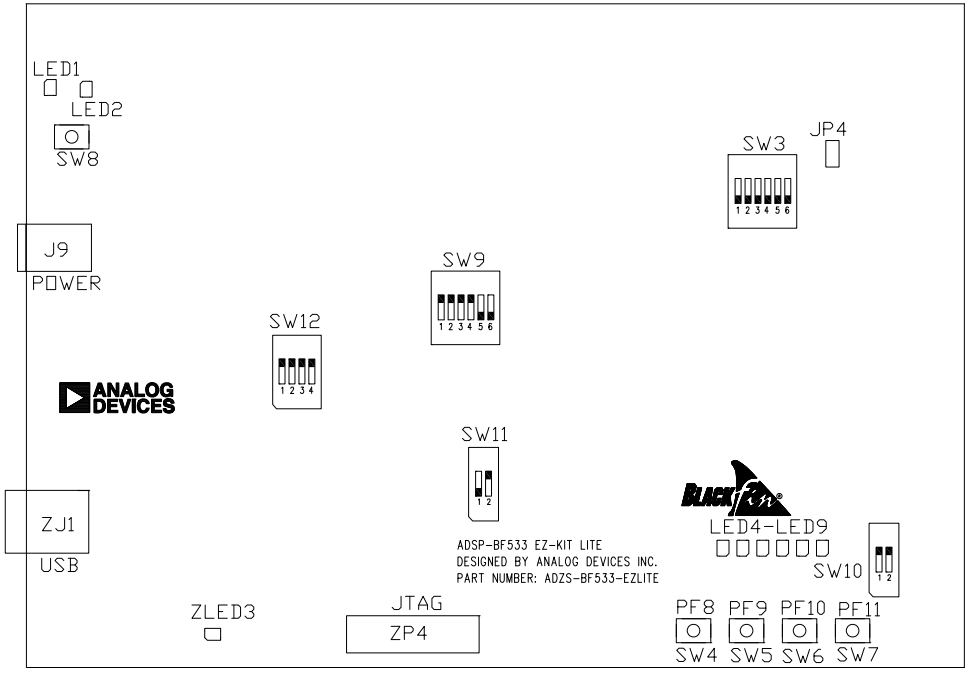

Figure 1-1. EZ-KIT Lite Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF533 EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector ZP4 (labeled JTAG) on the EZ-KIT Lite board.

Using the on-board Debug Agent:

1. Plug one side of the USB cable into the USB connector ZJ1 (labeled USB) on the EZ-KIT Lite board.
2. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the 7.5V power adaptor.

1. Plug the jack-end of the power adaptor into the power connector J9 (labeled POWER) on the EZ-KIT Lite board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled LED1) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power indicator is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled ZLED3) on the debug agent is on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-KIT Lite board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run > Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click  (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF533**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-KIT Lite** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:
    - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF533 EZ-KIT** Lite via Debug Agent.
    - For emulator connections, choose the type of emulator that is connected to the board.
7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.
8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click  and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run** > **Terminate**.

To delete a session, choose **Target** > **Session** > **Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.
3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.

- From the **Session** menu, **New Session**.
- From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
- From the **Session** menu, **Connect to Target**.

4. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF533**. Click **Next**.
5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.

6. The **Select Platform** page of the wizard appears on the screen. Ensure that the selected platform is **ADSP-BF533 EZ-KIT Lite via Debug Agent**. Specify your own **Session name** for your session or accept the default name.

   The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session.

   Click **Next**.

7. The **Finish** page of the wizard appears on the screen. The page displays your selections.Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-KIT Lite. Once connected, the main window's title is changed to include the session name set in step 6.

To disconnect from a session, click the disconnect button  or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-BF533 EZ-KIT Lite software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF53x family. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license

becomes permanently disabled. If the evaluation license is installed but not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  http://www.analog.com/salesdir/continent.asp.

The EZ-KIT Lite hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-BF533 EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-BF533 EZ-KIT Lite via the USB debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user's program to 20 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-KIT Lite hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Memory Map

The ADSP-BF533 processor has internal SRAM that can be used for instruction or data storage. The configuration of internal SRAM is detailed in the *ADSP-BF533 Processor Hardware Reference*.

The ADSP-BF533 EZ-KIT Lite board includes two types of external memory, SDRAM and flash memory.

The size of the SDRAM is 64 Mbytes (32M x 16-bits). The processor's memory select pin $\overline{\texttt{SMS0}}$ is configured for the SDRAM.

The flash memory is implemented with two dual-bank flash memory devices. These devices include primary and secondary flash memory as well as internal SRAM and registers. Primary flash memory totals 2 Mbytes mapped into two separate asynchronous memory banks, 1 Mbyte each. Secondary flash memory, along with SRAM and registers, occupies the third bank of asynchronous memory space. The processor's $\overline{\texttt{AMS0}}$, $\overline{\texttt{AMS1}}$, and $\overline{\texttt{AMS2}}$ memory select pins are used for that purpose.

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map

Start Address		End Address	Content
External Memory	0x0000 0000	0x07FF FFFF	SDRAM bank 0 (SDRAM). See "SDRAM Interface" on page 1-13.
	0x2000 0000	0x200F FFFF	ASYNC memory bank 0 (primary flash A). See "Flash Memory" on page 1-15.
	0x2010 0000	0x201F FFFF	ASYNC memory bank 1 (primary flash B). See "Flash Memory" on page 1-15.
	0x2020 0000	0x202F FFFF	ASYNC memory bank 2 (flash A and B secondary memory, SRAM and internal registers). See "Flash Memory" on page 1-15.
	All other locations		Not used

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map (Cont'd)

Start Address		End Address	Content
Internal Memory	0xFF80 0000	0xFF80 3FFF	Data bank A SRAM 16 KB
	0xFF80 4000	0xFF80 7FFF	Data bank A SRAM/CACHE 16 KB
	0xFF90 0000	0xFF90 3FFF	Data bank B SRAM 16 KB
	0xFF90 4000	0xFF90 7FFF	Data bank B SRAM/CACHE 16 KB
	0xFFA0 0000	0xFFA0 FFFF	Instruction SRAM 64 KB
	0xFFA1 0000	0xFFA1 3FFF	Instruction SRAM /CACHE 16 KB
	0xFFB0 0000	0xFFB0 0FFF	Scratch pad SRAM 4 KB
	0xFFC0 0000	0xFFDF FFFF	System MMRs 2 MB
	0xFFE0 0000	0xFFFF FFFF	Core MMRs 2 MB
	All other locations		Reserved

SDRAM Interface

The three SDRAM control registers must be initialized in order to use the MT48LC32M16 – 64 MB (32M x 16 bits) SDRAM memory.

If you are in an EZ-KIT Lite or emulator session and a reset operation is performed, the SDRAM registers are set automatically to the values listed in Table 1-2. The values are derived for maximum flexibility and work for a system clock frequency between 54 MHz and 133 MHz. For more information about the **Target Options** dialog box, see the online help.

To disable the automatic setting of the SDRAM registers, do one of the following:

- CCES users, choose **Target > Settings > Target Options** and clear the **Use XML reset values** check box.
- VisualDSP++ users, choose **Settings > Target Options** and clear the **Use XML reset values** check box.

Automatic configuration of SDRAM is not optimized for any SCLK frequency. Table 1-2 shows the optimized configuration for the SDRAM registers using a 118.8 MHz, 126 MHz, and 133 MHz SCLK. The frequency of 118.8 MHz is the maximum SCLK frequency when using a 594 MHz core frequency, the maximum frequency for the EZ-KIT Lite when using the internal voltage regulator. Only the EBIU_SDRRC register needs to be modified in the user code to achieve maximum performance.

Table 1-2. SDRAM Optimum Settings

Register	SCLK = 133 MHz (Processor MAX)	SCLK = 126 MHz (CCLK = 756 MHz)	SCLK = 118.8 MHz (CCLK = 594 MHz)
EBIU_SDGCTL	0x0091 998D	0x0091 998D	0x0091 998D
EBIU_SDBCTL			
ADSP-BF533 EZ-KIT Lite revision 1.6 and below	0x0000 0013	0x0000 0013	0x0000 0013
ADSP-BF533 EZ-KIT Lite revision 1.7 and above	0x0000 0025	0x0000 0025	0x0000 0025
EBIU_SDRRC	0x0000 0406	0x0000 03CF	0x0000 0397

An example program is included in the EZ-KIT Lite installation directory to demonstrate how to set up the SDRAM interface.

Flash Memory

The following sections describe how to use the memory and general-purpose IO pins, as well as how to configure the flash memory devices.

The ADSP-BF533 EZ-KIT Lite board employs two PSD4256G6V flash general-purpose IO devices from STMicroelectronics. These devices not only have flash memory but also extra IO pins, which are memory mapped.

Example code is provided in the EZ-KIT Lite installation directory to demonstrate how to program the flash memory as well as to demonstrate the functionality of the general-purpose IO pins.

Flash Memory Map

Each device includes the following memory segments:

- 1M byte of primary flash memory
- 64K bytes of secondary flash memory
- 32 Kbytes of internal SRAM
- 256 Bytes of configuration registers (IO control)

Access to each segment can be 8-bit or 16-bit. The processor's $\overline{\texttt{AMS0}}$, $\overline{\texttt{AMS1}}$, and $\overline{\texttt{AMS2}}$ memory select pin are used for that purpose. Asynchronous memory bank 0 is always enabled after a hard reset, while banks 1 and 2 need to be enabled by software. Table 1-3 provides an example on asynchronous memory configuration registers.

Table 1-3. Asynchronous Memory Control Registers Settings Example

Register	Value	Function
EBIU_AMBCTL0	0x7BB07BB0	Timing control for banks 1 and 0
EBIU_AMBCTL1 bits 15-0	0x7BB0	Timing control for bank 2 (bank 3 is not used)
EBIU_AMGCTL bits 3-0	0xF	Enable all banks

Each flash chip is initially configured with the memory sectors mapped into the processor's address space shown in Table 1-4.

Table 1-4. Flash Memory Map

Start Address	End Address	Content
0x2000 0000	0x200F FFFF	Flash A primary (1MB)
0x2010 0000	0x201F FFFF	Flash B primary (1MB)
0x2020 0000	0x2020 FFFF	Flash A secondary (64KB)
0x2024 0000	0x2024 7FFF	Flash A SRAM (32KB)
0x2027 0000	0x2027 00FF	Flash A registers (256 Bytes)
0x2028 0000	0x2028 FFFF	Flash B secondary (64KB)
0x202C 0000	0x202C 7FFF	Flash B SRAM (32KB)
0x202E 0000	0x202E 00FF	Flash B registers (256 Bytes)
All other locations		Reserved

Flash General-Purpose IO

This section describes general-purpose IO signals that are controlled by means of setting appropriate registers of the flash A or flash B. These registers are mapped into the processor's address space, as shown in Table 1-4.

Flash device IO pins are arranged as 8-bit ports labeled A through G. There is a set of 8-bit registers associated with each port. These registers are Direction, Data In, and Data Out. Note that the Direction and Data Out registers are cleared to all zeros at power-up or hardware reset.

The Direction register controls IO pins direction. When a bit is 0, a corresponding pin functions as an input. When the bit is 1, a corresponding pin is an output. This is a 8-bit read-write register.

The Data In register allows reading the status of port's pins. This is a 8-bit read-only register.

The Data Out register allows clearing an output pin to 0 or setting it to 1. This is a 8-bit read-write register.

The ADSP-BF533 EZ-KIT Lite board employs only flash A and flash B ports A and B. Table 1-5 and Table 1-6 provide configuration register addresses for flash A and flash B, respectively (only ports A and B are listed). The following bits connect to the expansion board connector.

- Flash A: port A bits 7 and 6, as well as port B bits 7 and 6
- Flash B: port A bits 7-0

Table 1-5. Flash A Configuration Registers for Ports A and B

Register Name	Port A Address	Port B Address
Data In (read-only)	0x2027 0000	0x2027 0001
Data Out (read-write)	0x2027 0004	0x2027 0005
Direction (read-write)	0x2027 0006	0x2027 0007

Table 1-6. Flash B Configuration Registers for Ports A and B

Register Name	Port A Address	Port B Address
Data In (read-only)	0x202E 0000	0x202E 0001
Data Out (read-write)	0x202E 0004	0x202E 0005
Direction (read-write)	0x202E 0006	0x202E 0007

Table 1-7 and Table 1-8 depict the IO assignments.

Table 1-7. Flash A Port A Controls

Bit Number	User IO	Bit Value
7	Not defined	Any
6	Not defined	Any
5	PPI clock select bit 1	00 = local OSC (27 MHz)
4	PPI clock select bit 0	01= video decoder pixel clock 1X = expansion board PPI clock
3	Video decoder reset	0= reset ON; 1= reset OFF
2	Video encoder reset	0= reset ON; 1= reset OFF
1	Reserved	Any
0	Codec reset	0= reset ON; 1= reset OFF

Table 1-8. Flash A Port B Controls

Bit Number	User IO	Bit Value
7	Not used	Any
6	Not used	Any
5	LED9	0= LED OFF; 1= LED ON
4	LED8	0= LED OFF; 1= LED ON
3	LED7	0= LED OFF; 1= LED ON
2	LED6	0= LED OFF; 1= LED ON

Table 1-8. Flash A Port B Controls (Cont'd)

Bit Number	User IO	Bit Value
1	LED5	0= LED OFF; 1= LED ON
0	LED4	0= LED OFF; 1= LED ON

Configuring Flash Memory

The PSD4256G6V flash memory devices used on the ADSP-BF533 EZ-KIT Lite have been obsoleted by ST Microelectronics and are no longer available for purchase. The software and programming adapter to reconfigure these devices has also been obsoleted and is no longer available.

LEDs and Push Buttons

The EZ-KIT Lite provides four push buttons and six LEDs for general-purpose IO.

The six LEDs, labeled LED4 through LED9, are accessed via some of the general-purpose IO pins of the flash memory interface. For information on how to program the pins, see "Flash General-Purpose IO" on page 1-16.

The four general-purpose push button are labeled SW4 through SW7. A status of each individual button can be read through programmable flag (PF) inputs, PF8 through PF11. A PF reads 1 when a corresponding switch is being pressed-on. When the switch is released, the PF reads 0. A connection between the push button and PF input is established through the SW9 DIP switch. See "Push Button Enable Switch (SW9)" on page 2-11 for details.

An example program is included in the EZ-KIT Lite installation directory to demonstrate the functionality of the LEDs and push buttons.

Audio Interface

The AD1836 audio codec provides three channels of stereo audio output and two channels of multichannel 96 kHz input. The SPORT0 interface of the processor links with the stereo audio data input and output pins of the AD1836 codec. The processor is capable of transferring data to the audio codec in time-division multiplexed (TDM) or two-wire interface (TWI) mode.

The TWI mode allows the codec to operate at a 96 kHz sample rate but limits the output channels to two. The TDM mode can operate at a maximum of 48 kHz sample rate but allows simultaneous use of all input and output channels. When using TWI mode, the TSCLK0 and RSCLK0 pins, as well as the TFS0 and RFS0 pins of the processor, must be tied together external to the processor. This is accomplished with the SW9 DIP switch (see "Push Button Enable Switch (SW9)" on page 2-11 for more information).

The AD1836 audio codec's internal configuration registers are configured using the SPI port of the processor. The processor's PF4 programmable flag pin is used as the select for this device. For information on how to configure the multichannel codec, go to AD1836A.

The general-purpose IO pin PA0 of flash A is a source for the AD1836 codec reset. See "Flash General-Purpose IO" on page 1-16 for more information about the pin.

Example programs are included in the EZ-KIT Lite installation directory to demonstrate AD1836 codec capabilities.

Video Interface

The board supports video input and output applications. The ADV7171 video encoder provides up to three output channels of analog video, while the ADV7183 video decoder provides up to three input channels of analog video. Both the encoder and the decoder connect to the parallel peripheral interface (PPI) of the processor. For additional information on the video interface hardware, refer to "PPI Interface" on page 2-5.

For the video interface to be operational, the following basic steps must be performed.

1. Configure the SW3 DIP switch as required by the application. Refer to "Video Configuration Switch (SW3)" on page 2-10 for details.
2. Remove reset to the video device. Refer to "Flash General-Purpose IO" on page 1-16 for details.
3. If using the decoder:
    - Enable device by driving programmable flag output PF2 to 0.
    - Select PPI clock (see Table 1-7 on page 1-18).
4. Program internal registers of the video device in use. Both video encoder and decoder use a two-wire serial interface to access internal registers. A programmable flag PF0 functions as a serial clock (SCL), and PF1 functions as a serial data (SDAT).
5. Program the processor's PPI interface (configuration registers, DMA, etc.).

Example programs are included in the EZ-KIT Lite installation directory to demonstrate the capabilities of the video interface.

Board Design Database

A `.zip` file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: `http://www.analog.com/board-design-database`.

Example Programs

Example programs are provided with the ADSP-BF533 EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

2 ADSP-BF533 EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF533 EZ-KIT Lite board. The following topics are covered.

- "System Architecture" on page 2-2
  Describes the configuration of the ADSP-BF533 EZ-KIT Lite board and explains how the board components interface with the processor.
- "Jumper and Switch Settings" on page 2-9
  Shows the location and describes the function of the configuration jumpers and switches.
- "LEDs and Push Buttons" on page 2-12
  Shows the location and describes the function of the LEDs and push buttons.
- "Connectors" on page 2-16
  Shows the location and gives the part number for all of the connectors on the board. Also, the manufacturer and part number information is given for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

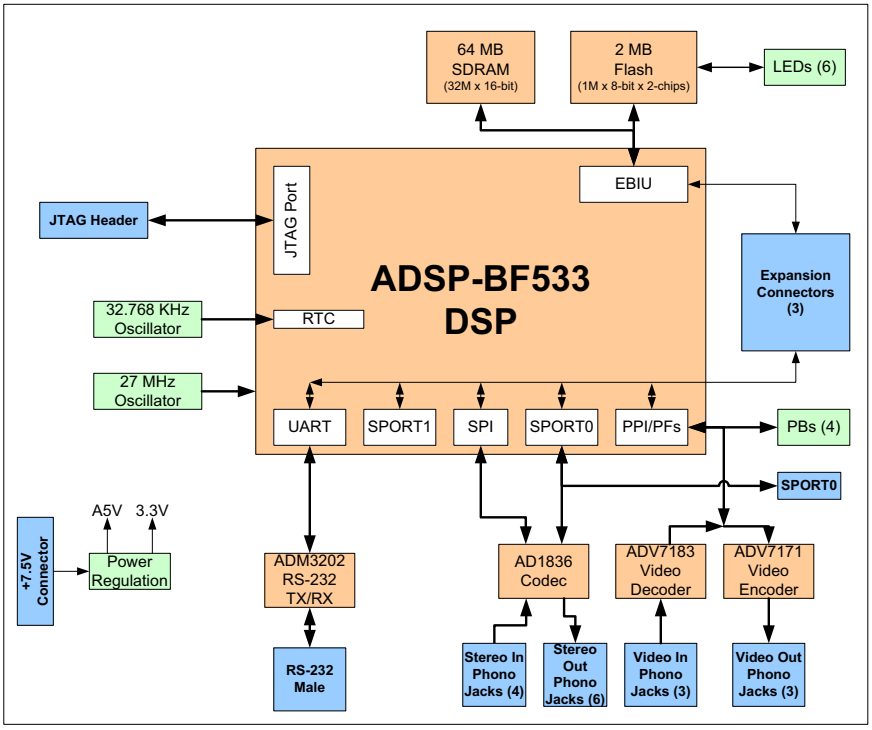

Figure 2-1. System Architecture

This EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-BF533 Blackfin processor. The processor has an IO voltage of 3.3V. The core voltage is derived from this 3.3V supply and uses the internal regulator of the processor. The core voltage and the core clock rate can be set up on the fly by the processor. Refer to the *ADSP-BF533 Blackfin Processor Hardware Reference* for more information.

The default boot mode for the processor is flash boot. See "Boot Mode Switch (SW11)" on page 2-10 for information about changing the default.

External Bus Interface Unit

The external bus interface unit (EBIU) connects an external memory to the ADSP-BF533 processor. The EBIU includes a 16-bit wide data bus, an address bus, and a control bus. Both 16-bit and 8-bit access are supported. On the EZ-KIT Lite, the EBI unit connects to SDRAM and flash memory.

64 MB (32M x 16 bits) of SDRAM connect to the synchronous memory select 0 (SMS0) pin. Refer to "SDRAM Interface" on page 1-13 for information about SDRAM configuration. Note that SDRAM's clock is the processor's clock out (CLK OUT), which frequency should not exceed 133 MHz.

Two flash memory devices connect to the asynchronous memory select signals, AMS2 through AMS0. The devices provide a total of 2 Mbytes of primary flash memory, 128 Kbytes of secondary flash memory, and 64 Kbytes of SRAM. The processor can use this memory for both booting and storing information during normal operation. Refer to "Flash Memory" on page 1-15 for details.

All of the address, data, and control signals are available externally via the extender connectors (J1-3). The pinout of the connectors can be found in "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1.

SPORT Audio Interface

The SPORT0 connects to the AD1836 audio codec and the expansion interface. The AD1836 codec uses both the primary and secondary data transmit and receive pins to input and output data from the audio inputs and outputs.

The SPORT1 connects to the SPORT connector (P3) and the expansion interface.

The pinout of the SPORT connector and the expansion interface connectors can be found in "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1.

SPI Interface

The serial peripheral interface (SPI) of the ADSP-BF533 processor connects to the AD1836 audio codec and the expansion interface. The SPI connection to the AD1836 is used to access the control registers of the device. The PF4 flag of the processor is used as the devices select for the SPI port.

The SPI signals are available on the expansion interface and on the SPI connector (P6). The interface pinout can be found in "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1.

Programmable Flags

The processor has 15 programmable flag pins (PFs). The pins are multi-functional and depend on the processor setup. Table 2-1 is a summary of the programmable flag pins used on the EZ-KIT Lite.

Table 2-1. Programmable Flag Connections

Processor PF Pin	Other Processor Function	EZ-KIT Lite Function
PF0	SPI Slave Select	Serial clock for programming ADV7171 and ADV7183
PF1	SPI Select 1, Timer CLK	Serial data for programming ADV7171 and ADV7183
PF2	SPI Select 2	ADV7183 $\overline{\text{OE}}$ signal
PF3	SPI Select 3, FS3	ADV7183 FIELD pin. See "Video Configuration Switch (SW3)" on page 2-10.
PF4	SPI Select 4, PPI15	AD1836 SPI select

Table 2-1. Programmable Flag Connections (Cont'd)

Processor PF Pin	Other Processor Function	EZ-KIT Lite Function
PF5	SPI Select 5, PPI14	
PF6	SPI Select 6, PPI13	
PF7	SPI Select 7, PPI12	
PF8	PPI11	Push button (SW4). See "LEDs and Push Buttons" on page 1-19 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF9	PPI10	Push button (SW5). See "LEDs and Push Buttons" on page 1-19 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF10	PPI9	Push button (SW6). See "LEDs and Push Buttons" on page 1-19 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF11	PPI8	Push button (SW7). See "LEDs and Push Buttons" on page 1-19 and "Push Button Enable Switch (SW9)" on page 2-11 for information on how to disable the push button.
PF12	PPI7	ADV7171 and ADV7183 data (MSB)
PF13	PPI6	ADV7171 and ADV7183 data
PF14	PPI5	ADV7171 and ADV7183 data
PF15	PPI4	ADV7171 and ADV7183 data

PPI Interface

The parallel peripheral interface (PPI) of the ADSP-BF533 processor is a half-duplex, bi-directional port that can accommodate up to 16 bits of data. The interface has a dedicated input clock (27 MHz), three multiplexed frame sync signals, and four bits of dedicated data. The remaining data bits come from the re-configured programmable flag pins. For information about the PFs multiplexed with the PPI pins, see "Programmable

Flags" on page 2-4. For information about the processor's PPI interface, refer to the *ADSP-BF533 Blackfin Processor Hardware Reference*.

Table 2-2 is a summary of the PPI pins used on the EZ-KIT Lite.

Table 2-2. PPI Connections

Processor PPI Pin	Other Processor Function	EZ-KIT Lite Function
PPI7	PF12	ADV7171 and ADV7183 data (MSB)
PPI6	PF13	ADV7171 and ADV7183 data
PPI5	PF14	ADV7171 and ADV7183 data
PPI4	PF15	ADV7171 and ADV7183 data
PPI3		ADV7171 and ADV7183 data
PPI2		ADV7171 and ADV7183 data
PPI1		ADV7171 and ADV7183 data
PPI0		ADV7171 and ADV7183 data
PF3	FS3	ADV7183 FIELD pin. For more information, see "Video Configuration Switch (SW3)" on page 2-10.
TMR1	PPI_HSYNC	ADV7171 and ADV7183 HSYNC. For more information, see "Video Configuration Switch (SW3)" on page 2-10.
TMR2	PPI_FSYNC	ADV7171 and ADV7183 VSYNC. For more information, see "Video Configuration Switch (SW3)" on page 2-10.
PPI_CLK		Input from either the ADV7183 output clock or the same 27 MHz oscillator driving the processor. For more information, see "Video Interface" on page 1-21.

The ADSP-BF533 EZ-KIT Lite board employs 8-bit PPI interface for video output and video input.

Video Output Mode

In the video output mode, the PPI interface is configured as output and connects to the on-board video encoder device, ADV7171. The ADV7171 encoder generates three analog video channels on DAC B, DAC C, and DAC D outputs. The PPI data connects to P7-0 of the encoder's pixel inputs. The encoder's PPI input clock runs at 27 MHz, in phase with CLK IN of the processor.

The encoder's synchronization signals, HSYNC and VSYNC, can be configured as inputs or outputs. Video blanking control signal is at level 1. The HSYNC and VSYNC signals can connect the multiplexed sync pins of the processor and the on-board ADV7183 video decoder via the SW3 switch, as described in "Video Configuration Switch (SW3)" on page 2-10.

Video Input Mode

In the video input mode, the PPI interface is configured as input and connects to the on-board video decoder device, ADV7183. The ADV7183 decoder receives three analog video channels on AIN1, AIN4, and AIN5 input. The decoder's pixel data outputs P15-8 drive the PPI data (PPI3-0 and PF15-12). The decoder's 27 MHz pixel clock output can be selected to drive PPI clock, as shown in Table 1-7 on page 1-18.

Synchronization outputs of the decoder, HS/HACTIVE, VS/VACTIVE, and FIELD, can connect the multiplexed sync pins of the ADSP-BF533 processor and the ADV7171 on-board video encoder via the SW3 DIP switch, as described in "Video Configuration Switch (SW3)" on page 2-10.

UART Port

The universal asynchronous receiver/transmitter (UART) port of the processor connects to the ADM3202 RS-232 line driver, as well as to the expansion interface. The RS-232 line driver connects to the DB9 male connector, providing an interface to a personal computer and other serial devices.

Expansion Interface

The expansion interface consists of three 90-pin connectors. Table 2-3 shows the interfaces each connector provides. For the exact pinout of the connectors, refer to "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1. The mechanical dimensions of the connectors can be found on page 2-17.

Table 2-3. Expansion Connector Interfaces

Connector	Interfaces
J1	5V, GND, address, data, PPI
J2	3.3V, GND, SPI, NMI, TMR2-0, SPORT0, SPORT1, PF15-0, EBIU control signals
J3	5V, 3.3V, GND, UART, flash IO, reset, video control signals

Limits to the current and to the interface speed must be taken into consideration when using the expansion interface. The maximum current limit is dependent on the capabilities of the used regulator. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory through a 6-pin interface. The JTAG emulation port of the processor also connects to the USB debugging interface. When an emulator connects to the board at ZP4, the USB debugging interface is disabled. See "JTAG (ZP4)" on page 2-20 for more information about the JTAG connector.

To learn more about available emulators, go to:
http://www.analog.com/processors/tools/blackfin.

Jumper and Switch Settings

This section describes the operation of the jumpers and switches. The jumper and switch locations are shown in Figure 2-2.

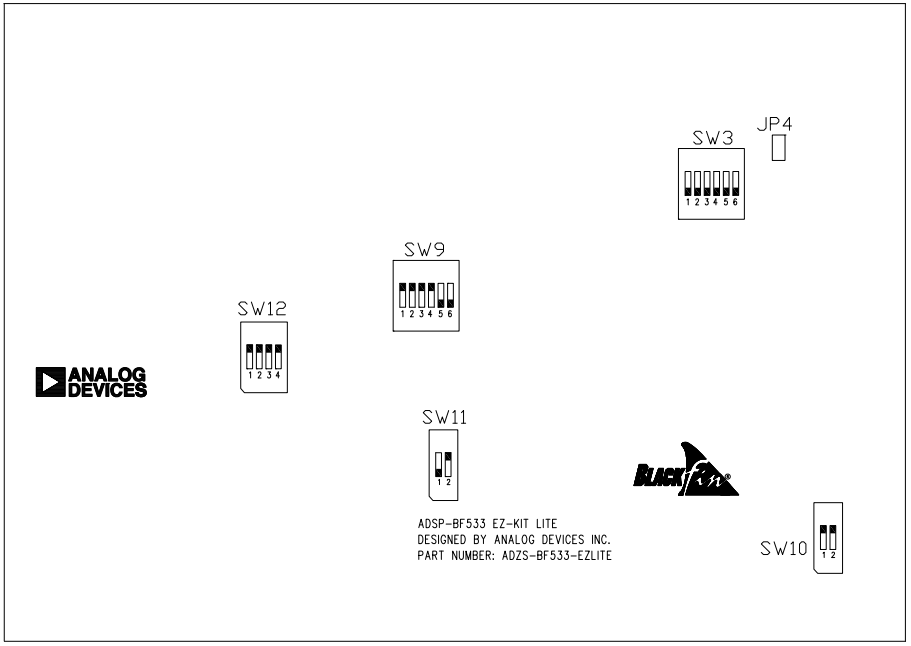

Figure 2-2. Jumper and Switch Locations

UART Loop Jumper (JP4)

The UART loop jumper (JP4) allows the loop back connection of transmit and receive signals. The default is the OFF position.

Boot Mode Switch (SW11)

Positions 1 and 2 of SW11 set the boot mode of the processor as described in Table 2-4.

Table 2-4. Boot Mode Switch (SW11)

Position 1 BMODE0	Position 2 BMODE1	Boot Mode
ON	ON	16-bit external memory
OFF [1]	**ON**	**Flash memory**
ON	OFF	SPI host slave
OFF	OFF	SPI EEPROM

1 Default settings

Test DIP Switches (SW1 and SW2)

Two DIP switches (SW1 and SW2) are located on the bottom of the board. The switches are used only for testing and should be in the OFF position.

Video Configuration Switch (SW3)

The video configuration switch (SW3) controls how some video signals from the ADV7183 video decoder and ADV7171 video encoder are routed to the processor's PPI. The switch also determines if the PF2 pin controls the $\overline{\text{OE}}$ signal of the ADV7183 video decoder outputs. Table 2-5 shows which processor's signals connect to the encoder and decoder in the default (ON) position.

Table 2-5. Video Configuration Switch (SW3)

Switch Position (Default)	Processor Signal	Video Signal
1 (OFF)	TMR1 (HSYNC)	HSYNC (ADV7171)
2 (OFF)	TMR1 (HSYNC)	HS (ADV7183)

Table 2-5. Video Configuration Switch (SW3) (Cont'd)

Switch Position (Default)	Processor Signal	Video Signal
3 (OFF)	TMR2 (VSYNC)	VS (ADV7183)
4 (OFF)	TMR2 (VSYNC)	VSYNC (ADV7171)
5 (OFF)	PF3 (FIELD)	FIELD (ADV7183)
6 (ON)	PF2	$\overline{OE}$ (ADV7183)

Positions 1 thorough 5 of SW3 determine how and if the VSYNC, HSYNC, and FIELD control signals are routed to the processor's PPI. In standard configuration of the encoder and decoder, this is not necessary because the processor is capable of reading the control information embedded in the data stream.

Position 6 of SW3 determines whether PF2 connects to the $\overline{OE}$ signal of the ADV7183. When the switch is OFF, PF2 can be used for other operations, and the decoder output enable is held high with a pull-up resistor.

Push Button Enable Switch (SW9)

The push button enable (SW9) switch positions 1 through 4 disconnect the drivers associated with the push buttons from the PF pins of the processor. Positions 5 and 6 are used to connect the transmit and receive frame syncs and clocks of SPORT0. This is important when the AD1836 audio codec and the processor are communicating in I^2S mode. Table 2-6 shows which PF is driven when the switch is in the default (ON) position.

Table 2-6. Push Button Enable Switch (SW9)

Switch Position	Default Setting	Pin #	Signal (Side 1)	Pin #	Signal (Side 2)
1	ON	1	SW4	12	PF8
2	ON	2	SW5	11	PF9
3	ON	3	SW6	10	PF10

Table 2-6. Push Button Enable Switch (SW9) (Cont'd)

Switch Position	Default Setting	Pin #	Signal (Side 1)	Pin #	Signal (Side 2)
4	ON	4	SW7	9	PF11
5	OFF	5	TFS0	8	RFS0
6	OFF	6	RSCLK0	7	TSCLK0

SPIS1/SPISS Select Switch (SW10)

The SPIS1/SPISS select switch (SW10) disconnects the SPIS1 and SPISS signals from the board, making them available on the SPI connector (P6). The default is the ON position.

SPORT0 Switch (SW12)

When is set to OFF, SW12 disconnects SPORT0 from the audio codec. The switch is used when SPORT0 signals are desired at the expansion interface. The default is the ON position.

LEDs and Push Buttons

This section describes the functionality of the LEDs and push buttons. Figure 2-3 shows the locations of the LEDs and push buttons.

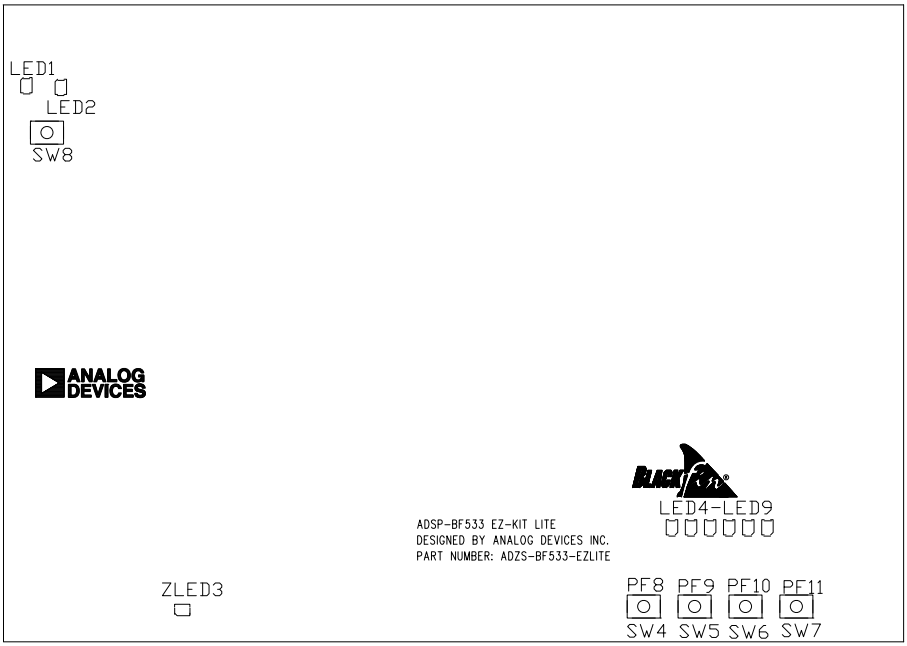

Figure 2-3. LED and Push Button Locations

Programmable Flag Push Buttons (SW4–7)

Four push buttons, SW4-7, are provided for general-purpose user input. The buttons connect to the processor's programmable flag pins PF8-11. The push buttons are active high and, when pressed, send a high (1) to the processor. Refer to "LEDs and Push Buttons" on page 1-19 for information on PFs programming. The push button enable switch (SW9) is capable of disconnecting the push buttons from the PFs (refer to "Push Button Enable Switch (SW9)" on page 2-11 for more information). The programmable flag pins and their corresponding push buttons are shown in Table 2-7.

Table 2-7. Programmable Flag Switches

Processor Programmable Flag Pin	Push Button Reference Designator
PF8	SW4
PF9	SW5
PF10	SW6
PF11	SW7

Reset Push Button (SW8)

The RESET push button resets all of the ICs on the board. One exception is the USB interface chip (U34). The chip is not being reset when the push button is pressed after the USB cable has been plugged in, and communication has been correctly initialized with the PC. After USB communication has been initialized, the only way to reset the USB is by powering down the board.

Power LED (LED1)

When LED1 is lit (green), it indicates that power is being supplied to the board properly.

Reset LED (LED2)

When LED2 is lit, it indicates that a master reset of all the major ICs is active.

User LEDs (LED4–9)

Six LEDs connect to six general-purpose IO pins of the flash memory (U5). The LEDs are active high and are lit by writing a 1 to the correct memory address in the flash memory. Refer to "LEDs and Push Buttons" on page 1-19 for information on how to use the flash when programming the LEDs.

Table 2-8. User LEDs

LED Reference Designator	Flash Port Name
LED4	PB0
LED5	PB1
LED6	PB2
LED7	PB3
LED8	PB4
LED9	PB5

USB Monitor LED (ZLED3)

The USB monitor LED (ZLED3) indicates that USB communication has been initialized successfully and you can connect to the processor using a CCES or VisualDSP++ EZ-KIT Lite session. This should take approximately 15 seconds. If the LED does not light, try cycling power on the board and/or reinstalling the USB driver.

When CCES or VisualDSP++ is actively communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Connectors

This section describes the connector functionality and provides information about mating connectors. The connector locations are shown in Figure 2-4.

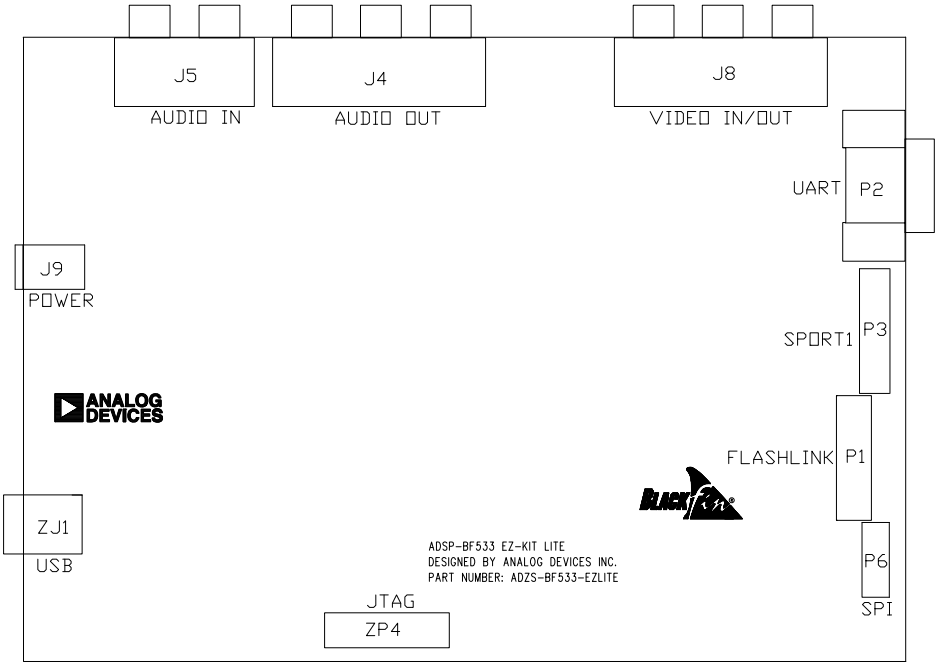

Figure 2-4. Connector Locations

Expansion Interface (J1–3)

Three board-to-board connector footprints provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see "Expansion Interface" on page 2-8. For availability and pricing of the J1, J2, and J3 connectors, contact Samtec.

Part Description	Manufacturer	Part Number
90-position 0.05" spacing, SMT (J1, J2, J3)	SAMTEC	SFC-145-T2-F-D-A
Mating Connectors		
90-position 0.05" spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05" spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05" spacing (low cost)	SAMTEC	TFC-145 series

Audio (J4 and J5)

Part Description	Manufacturer	Part Number
2x2 RCA jacks (J5)	SWITCHCRAFT	PJRAS2X2S01
3x2 RCA jacks (J4)	SWITCHCRAFT	PJRAS3X2S01
Mating Connector		
Two channel RCA interconnect cable	MONSTER CABLE	BI100-1M

Video (J8)

Part Description	Manufacturer	Part Number
3x2 RCA jacks (J8)	SWITCHCRAFT	PJRAS3X2S01

Power (J9)

The power connector provides all of the power necessary to operate the EZ-KIT Lite board. The following table shows the power connector pinout.

Part Description	Manufacturer	Part Number
2.5 mm power jack (J9)	SWITCHCRAFT	RAPC712
	DIGI-KEY	RAPC712X-ND
Mating Power Supply (shipped with EZ-KIT Lite)		
7.5V power supply	GLOBTEK	TR9CC2000LCP-Y

The power connector supplies DC power to the EZ-KIT Lite board. Table 2-9 shows the power supply specifications.

Table 2-9. Power Supply Specifications

Terminal	Connection
Center pin	+7.5 VDC@2amps
Outer ring	GND

FlashLINK (P1)

The FlashLINK connector allows you to configure and program the STMicroelectronics DSM2150 flash/PLD chip. See "Configuring Flash Memory" on page 1-19 for more information about the FlashLINK connector. The software and programming adapter to reconfigure these devices has been obsoleted and is no longer available.

Part Description	Manufacturer	Part Number
Right-angle 7X2 shrouded 0.1" spacing (P1)	FCI	68737-414HLF
Mating Assembly		
FlashLINK JTAG programmer	ST MICRO	FL-101B

RS-232 (P2)

The RS-232 compatible connector is described in Table 2-10.

Table 2-10. RS-232 Connector

Part Description	Manufacturer	Part Number
DB9, male, right angle (P2)	TYCO	5747250-4
Mating Assembly		
2m female-to-female cable	DIGI-KEY	AE1016-ND

SPORT1 (P3)

The SPORT1 connector is linked to a 20-pin connector. The connector's pinout can be found in "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1. For the flash (U5) connector pricing and availability, contact AMP.

Part Description	Manufacturer	Part Number
20-pin IDC header	FCI	68737-420HLF
Mating Connector		
IDC socket	DIGI-KEY	S4210-ND

JTAG (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. When an emulator connects to the JTAG header, the USB debug interface is disabled.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

Part Description	Manufacturer	Part Number
14-pin IDC header	FCI	68737-414HLF

SPI (P6)

The SPI connector is linked to a 12-pin connector. The connector's pin-out can be found in "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1.

Part Description	Manufacturer	Part Number
IDC header	FCI	68737-412HLF
Mating Assembly		
IDC socket	DIGI-KEY	S4207-ND

A ADSP-BF533 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF533 EZ-KIT Lite Schematic" on page B-1.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	2	74LVC14A SOIC14	U10,U33	TI	74LVC14AD
2	1	IDT74FCT3244APY SSOP20	U31	IDT	IDT74FCT3244APYG
3	1	IDT74FCT3807AQ QSOP20	U4	IDT	IDT74FCT3807AQG
4	1	SN74AHC1G00 SOT23-5	U9	TI	SN74AHC1G00DBVR
5	1	12.288MHZ OSC003	U11	DIGI-KEY	SG-8002CA-PCC-ND (12.288M)
6	1	SN74LVC1G125 SOT23-5	U7	TI	74LVC1G125DBVRE4
7	1	MT48LC32M16A2TG-75 TSOP54	U8	MICRON	MT48LC32M16A2P-75
8	2	27MHZ OSC003	U3,U36	DIGI-KEY	SG-8002CA-PCC-ND (27.00M)
9	1	32.768KHZ OSC008	U2	EPSON	MC-156-32.7680KA-A0: ROHS

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
10	1	IDT2305-1DC SOIC8	U46	IDT	IDT2305-1DCG
11	1	SN74LVC1G32 SOT23-5	U21	TI	SN74LVC1G32DBVRE4
12	1	BF533 PSD4256G6V "U5"	U5	ST MICRO	PSD4256G6V-10UI
13	1	BF533 PSD4256G6V "U6"	U6	ST MICRO	BF533 PSD4256G6V "U5"
14	1	FDS9431A SOIC8	U32	FAIRCHILD	FDS9431A
15	1	FDC658P SOT23-6	U34	FAIRCHILD	FDC658P
16	1	ADM708SARZ SOIC8	U29	ANALOG DEVICES	ADM708SARZ
17	1	ADP3338AKCZ-33 SOT-223	VR1	ANALOG DEVICES	ADP3338AKCZ-3.3-RL
18	1	ADP3339AKCZ-5 SOT-223	VR5	ANALOG DEVICES	ADP3339AKCZ-5-R7
19	1	ADP3339AKCZ-33 SOT-223	VR3	ANALOG DEVICES	ADP3339AKCZ-3.3-R7
20	2	ADP3336ARMZ MSOP8	VR2,VR6	ANALOG DEVICES	ADP3336ARMZ-REEL
21	1	ADV7171KSUZ TQFP44	U27	ANALOG DEVICES	ADV7171KSUZ
22	1	10MA AD1580BRTZ SOT23D	D1	ANALOG DEVICES	AD1580BRTZ-REEL7

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
23	2	ADG752BRTZ SOT23-6	U25-26	ANALOG DEVICES	ADG752BRTZ-REEL
24	3	AD8061ARTZ SOT23-5	U22-24	ANALOG DEVICES	AD8061ARTZ-R2
25	1	ADM3202ARNZ SOIC16	U30	ANALOG DEVICES	ADM3202ARNZ
26	8	AD8606ARZ SOIC8	U12-13,U15-20	ANALOG DEVICES	AD8606ARZ
27	1	AD1836AASZ MQFP52	U14	ANALOG DEVICES	AD1836AASZ
28	1	ADV7183BKSTZ LQFP80	U28	ANALOG DEVICES	ADV7183BKSTZ
29	1	ADSP-BF533-600 MINIBGA160	U1	ANALOG DEVICES	ADSP-BF533SKBCZ600
30	1	ADP1864 SOT23-6	VR4	ANALOG DEVICES	ADP1864AUJZ-R7
31	5	RUBBER FOOT	M1-5	MOUSER	517-SJ-5018BK
32	1	PWR 2.5MM_JACK CON005	J9	SWITCH-CRAFT	RAPC712X
33	1	RCA 2X2 CON013	J5	SWITCH-CRAFT	PJRAS2X2S01X
34	5	MOMENTARY SWT013	SW4-8	PANASONIC	EVQ-PAD04M
35	3	.05 45X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
36	4	DIP6 SWT017	SW1-3,SW9	CTS	218-6LPST

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
37	2	RCA 3X2 CON024	J4,J8	SWITCH-CRAFT	PJRAS3X2S01X
38	1	DIP4 SWT018	SW12	ITT	TDA04HOSB1
39	2	DIP2 SWT020	SW10-11	C&K	TDA02H0SB1
40	1	IDC 2X1 IDC2X1	JP4	FCI	90726-402HLF
41	2	IDC 7X2 IDC7X2	P1,ZP4	FCI	68737-414HLF
42	1	IDC 10X2 IDC10X2	P3	FCI	68737-420HLF
43	1	2.5A RESE-TABLE FUS001	F1	RAYCHEM	SMD250F-2
44	1	IDC 2PIN_JUMPER_SHORT	SJ1	DIGI-KEY	S9001-ND
45	1	DB9 9PIN DB9M	P2	TYCO	5747250-4
46	1	IDC 6X2 IDC6X2	P6	FCI	68737-412HLF
47	14	0 1/4W 5% 1206	R27-30,R148,R157-158,R167,R174-175,R177-178, R182,R193	KOA	0.0ECTRk7372BTTED
48	6	YELLOW LED001	LED4-9	PANASONIC	LN1461C
49	12	330PF 50V 5% 0805	C13,C18,C23,C28, C33,C38,C67-70, C73-74	AVX	08055A331JAT

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
50	42	0.01UF 100V 10% 0805	C82,C85,C87, C108,C112-113, C123-124,C126-128,C136,C146-147,C149-155, C159,C161,C163, C165-169,C171-174,C181,C183, C188,C190,C194, C196,C201,C204, C208	AVX	08051C103KAT2A
51	8	0.22UF 25V 10% 0805	C129-130, C137-142	AVX	08053C224FAT
52	58	0.1UF 50V 10% 0805	C2,C6,C8,C71-72, C75-81,C84,C86, C88-95,C98-100, C105,C109-111, C119,C125,C132, C143-145,C148, C156-158,C175-180,C182,C184-187,C189,C191-193,C195,C197, C209-210	AVX	08055C104KAT
53	8	1000PF 50V 5% 0805	C7,C9-11,C49-50, C52-53	AVX	08055A102JAT2A
54	6	10UF 16V 10% C	CT13,CT21-25	AVX	TAJC106K016R

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
55	32	10K 1/10W 5% 0805	R1-2,R4,R10,R12-13,R15-16,R18, R26,R32-33, R106-108,R128, R138-139, R142-143,R145, R150-151,R153, R156,R166,R172-173,R192,R214, R225,R232	VISHAY	CRCW080510K0JNEA
56	10	33 1/10W 5% 0805	R5-9,R31,R144, R179,R183,R224	VISHAY	CRCW080533R0JNEA
57	1	4.7K 1/10W 5% 0805	R17	VISHAY	CRCW08054K70JNEA
58	1	1.5K 1/10W 5% 0805	R140	VISHAY	CRCW08051K50FKEA
59	1	1.2K 1/8W 5% 1206	R129	VISHAY	CRCW12061K20JNEA
60	6	49.9K 1/8W 1% 1206	R38,R45,R54,R62, R70,R78	VISHAY	CRCW120649K9FKEA
61	12	100PF 100V 5% 1206	C15,C20,C25,C30, C35,C40,C46-48, C51,C54,C56	AVX	12061A101JAT2A
62	1	2.2UF 35V 10% B	CT27	AVX	TAJB225K035R
63	5	10UF 16V 10% B	CT1-2,CT14-16	AVX	TAJB106K016R
64	4	100 1/10W 5% 0805	R149,R152, R154-155	VISHAY	CRCW0805100RJNEA
65	6	220PF 50V 10% 1206	C16,C21,C26,C31, C36,C41	AVX	12061A221JAT2A
66	4	600 100MHZ 200MA 0603	FER14-17	DIGI-KEY	490-1014-2-ND

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
67	3	2A S2A DO-214AA	D2-4	VISHAY	S2A-E3
68	15	600 100MHZ 500MA 1206	FER1-4,FER8-13, FER18-22	STEWARD	HZ1206B601R-10
69	4	237.0 1/8W 1% 1206	R93,R95,R97,R99	VISHAY	CRCW1206237RFKEA
70	4	750.0K 1/8W 1% 1206	R86,R90,R94,R96	VISHAY	CRCW1206750KFKEA
71	16	5.76K 1/8W 1% 1206	R82-85,R87-89, R91-92,R98, R100-105	VISHAY	CRCW12065K76FKEA
72	6	11.0K 1/8W 1% 1206	R34,R48,R50,R58, R66,R74	VISHAY	CRCW120611K0FKEA
73	8	120PF 50V 5% 1206	C42-45,C55,C57-59	AVX	12065A121JAT2A
74	1	1UF 16V 10% 0805	C5	PANASONIC	ECJ2FB1E105K
75	12	75 1/8W 5% 1206	R113-114,R116-117,R120-121, R123-124,R127, R133-134,R137	VISHAY	CRCW120675R0JNEA
76	1	68UF 6.3V 20% D	CT28	AVX	TAJD686K016R
77	1	340.0K 1/8W 1% 0805	R185	VISHAY	CRCW0805-3403FRT1E3
78	6	680PF 50V 1% 0805	C14,C19,C24,C29, C34,C39	AVX	08055A681FAT2A
79	3	10UF 25V +80-20% 1210	C198-200	PANASONIC	ECJ4YF1E106Z
80	6	2.74K 1/8W 1% 1206	R41,R47,R57,R65, R73,R81	VISHAY	CRCW12062K74FKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
81	12	5.49K 1/8W 1% 1206	R35,R40,R42,R49, R51,R56,R59,R64, R67,R72,R75,R80	VISHAY	CRCW12065K49FKEA
82	6	3.32K 1/8W 1% 1206	R36,R43,R52,R60, R68,R76	VISHAY	CRCW12063K32FKEA
83	6	1.65K 1/8W 1% 1206	R37,R44,R53,R61, R69,R77	VISHAY	CRCW12061K65FKEA
84	10	10UF 16V 20%CAP002	CT3-12	PANASONIC	EEE1CA100SR
85	1	4A SSB43L DO-214AA	D6	VISHAY	SSB43L
86	1	10UH 20%IND001	L12	TDK	445-2014-1-ND
87	2	10K 50MW 5% BGA36	RN1-2	CTS	RT230B7TR7
88	25	0 1/10W 5% 0805	R3,R19,R21-25, R110-111,R132, R135-136,R141, R169,R186-188, R194,R210-211, R222,R226-228, R231	VISHAY	CRCW08050000Z0EA
89	1	190 100MHZ 5A FER002	FER23	MURATA	DLW5BSN191SQ2
90	1	3.32K 1/10W 1% 0805	R223	PANASONIC	ERJ-6ENF3321V
91	4	22 1/10W 5% 0805	R14,R109,R180-181	VISHAY	CRCW080522R0JNEA
92	6	0.68UH 10% 0805	L4-9	MURATA	LQM21NNR68K10D
93	1	.082UF 50V 5% 0805	C83	AVX	08055C823JAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
94	1	1A ZHCS1000 SOT23-312	D5	ZETEX	ZHCS1000TA pb-free
95	3	2.2UH 10% 0805	L1-3	DIGI-KEY	490-1119-2-ND
96	6	1UF 10V 10% 0805	C4,C60-61, C102-104	AVX	0805ZC105KAT2A
97	2	18PF 50V 5% 0805	C1,C3	AVX	08055A180JAT2A
98	1	10M 1/8W 5% 0805	R20	VISHAY	CRCW080510M0JMEA
99	1	64.9K 1/10W 1% 0805	R184	VISHAY	CRCW080564K9FKEA
100	1	76.8K 1/10W 1% 1206	R190	VISHAY	CRCW120676K8FKEA
101	1	147.0K 1/10W 1% 1206	R191	VISHAY	CRCW1206147KFKEA
102	1	68PF 50V 5% 0603	C64	AVX	06035A680JAT2A
103	1	470PF 50V 5% 0603	C63	AVX	06033A471JAT2A
104	1	0 1/10W 5% 0603	R159	PHYCOMP	232270296001L
105	1	24.9K 1/10W 1% 0603	R11	DIGI-KEY	311-24.9KHTR-ND
106	1	47UF 6.3V 10% B	CT26	PANASONIC	EEE0JA470WR
107	1	0.05 1/2W 1% 1206	R165	SUSUMU	PRL1632-R051-F-T1
108	1	10UF 16V 10% 1210	C65	AVX	1210YD106KAT2A

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
109	1	680 1/8W 5% 1206	R163	VISHAY	CRCW1206680RFNEA
110	1	150.0 1/8W 1% 1206	R122	VISHAY	CRCW1206150RFKEA
111	1	GREEN LED001	LED1	PANASONIC	LN1361CTR
112	1	REDLED001	LED2	PANASONIC	LN1261CTR
113	2	1000PF 50V 5% 1206	C96-97	AVX	12065A102JAT2A
114	6	2200PF 50V 5% 1206	C12,C17,C22,C27, C32,C37	AVX	12065A222JAT050
115	6	1K 1/8W 5% 1206	R115,R118-119, R125-126,R131	VISHAY	CRCW12061K00FNEA
116	3	100K 1/8W 5% 1206	R112,R130,R176	VISHAY	CRCW1206100KFKEA
117	7	270 1/8W 5% 1206	R146-147,R160-162,R164,R168	VISHAY	CRCW1206270RJNEA
118	6	604.0 1/8W 1% 1206	R39,R46,R55,R63, R71,R79	PANASONIC	ERJ-8ENF6040V
119	4	1UF 25V 20% A	CT17-20	AVX	TAJA105K020R
120	1	255.0K 1/10W 1% 0603	R171	VISHAY	CRCW06032553FK
121	1	80.6K 1/10W 1% 0603	R170	DIGI-KEY	311-80.6KHRCT-ND
122	1	6.8UH 25% IND009	L10	DIGI-KEY	308-1328-1-ND

ADSP-BF533 EZ-KIT Lite

ANALOG DEVICES
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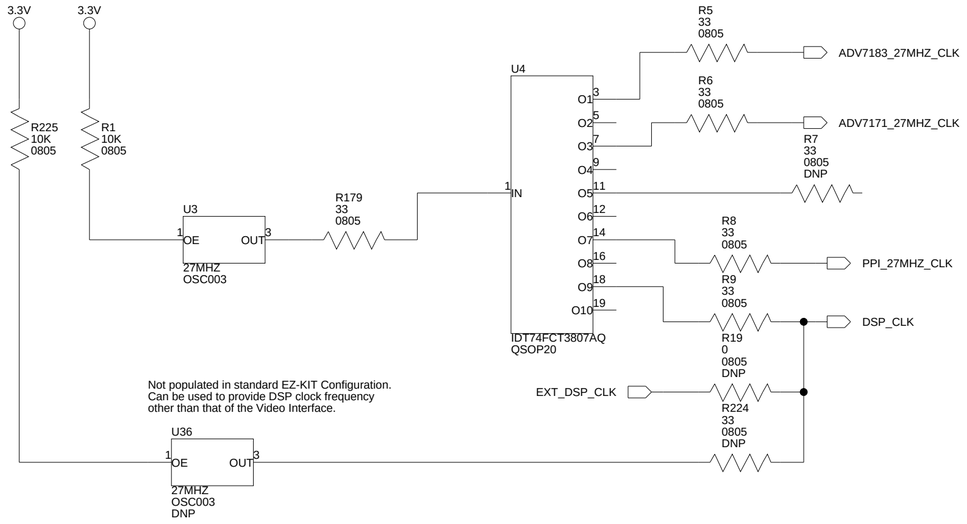
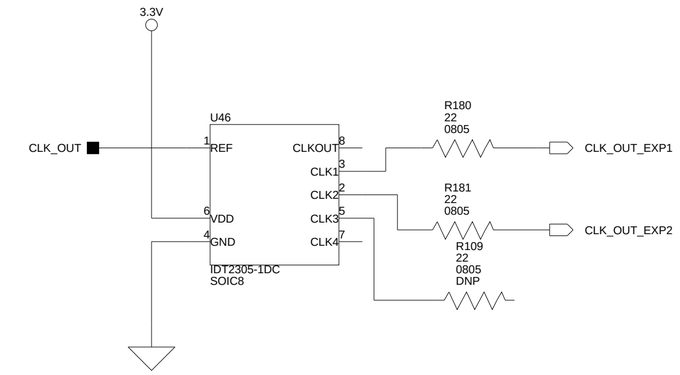
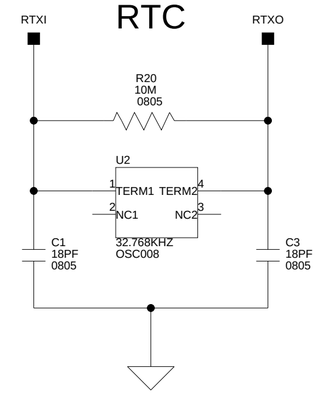
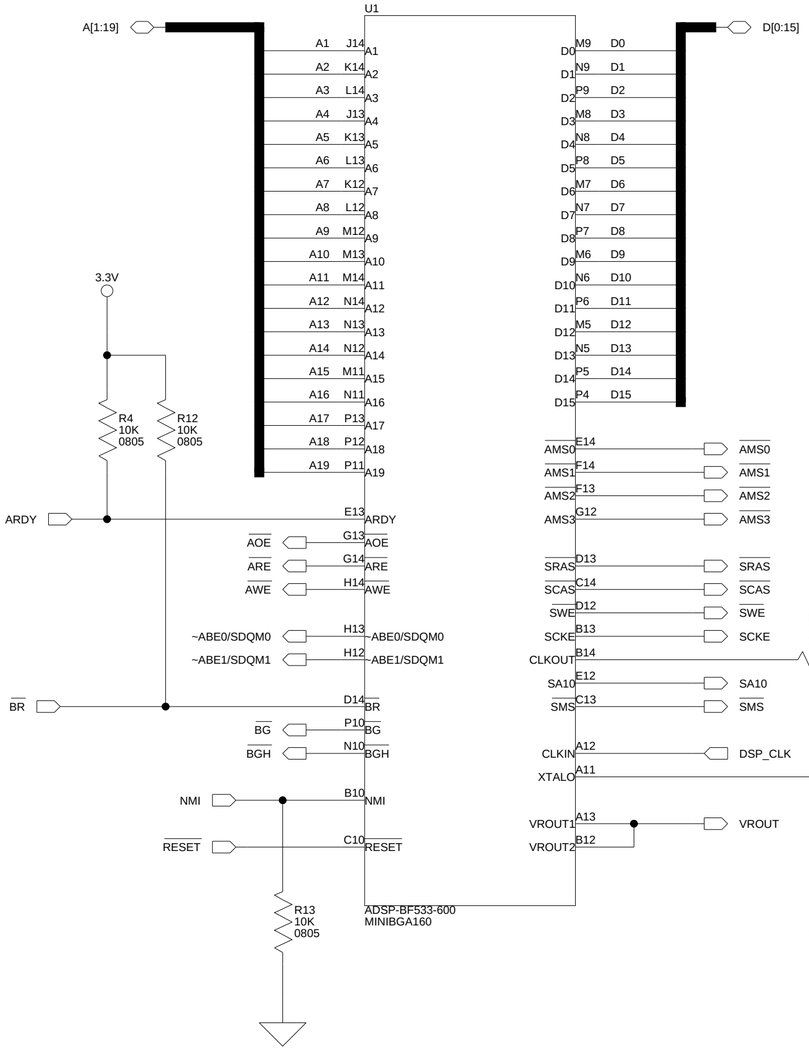
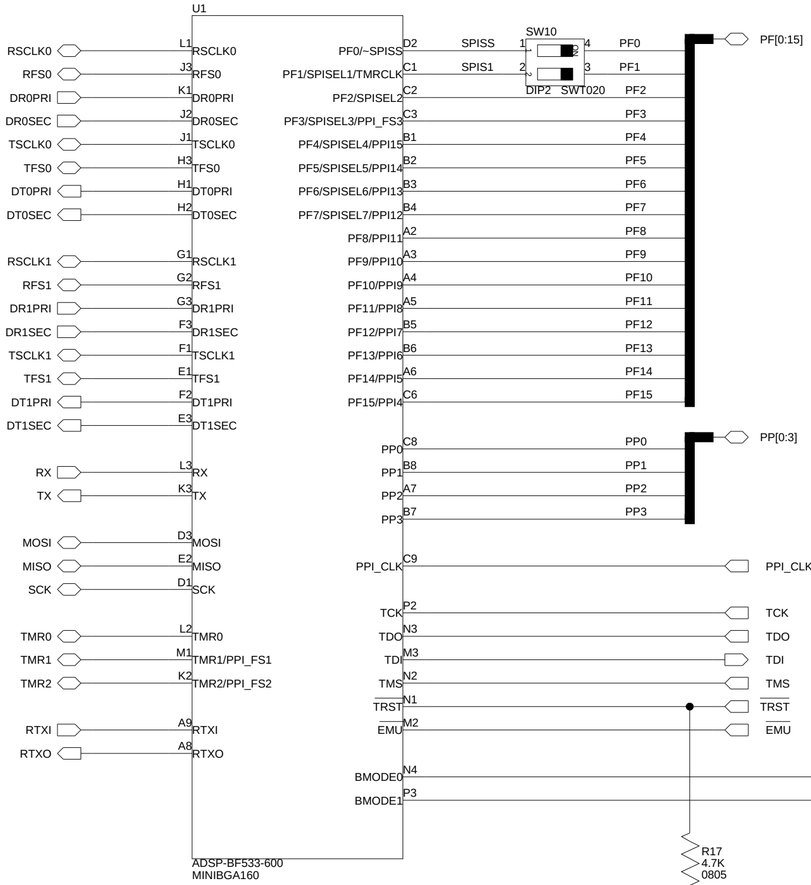
Title	ADSP-BF533 EZ-KIT LITE TITLE	
Size C	**Board No.** A0167-2001	**Rev** 2.2
Date 5-24-2007_14:20	**Sheet** 1 **of** 12	











SW2: BOOT MODE SELECT
(Default : 1 = OFF, 2 = ON)

BOOT MODE	1	2	
Execute from 16-bit external memory (bypass boot ROM)	ON	ON	
Boot from 8-bit or 16-bit flash	OFF	ON	DEFAULT
Boot from SPI host slave mode	ON	OFF	
Boot from SPI serial EEPROM (8, 16 or 24-bit address range)	OFF	OFF	

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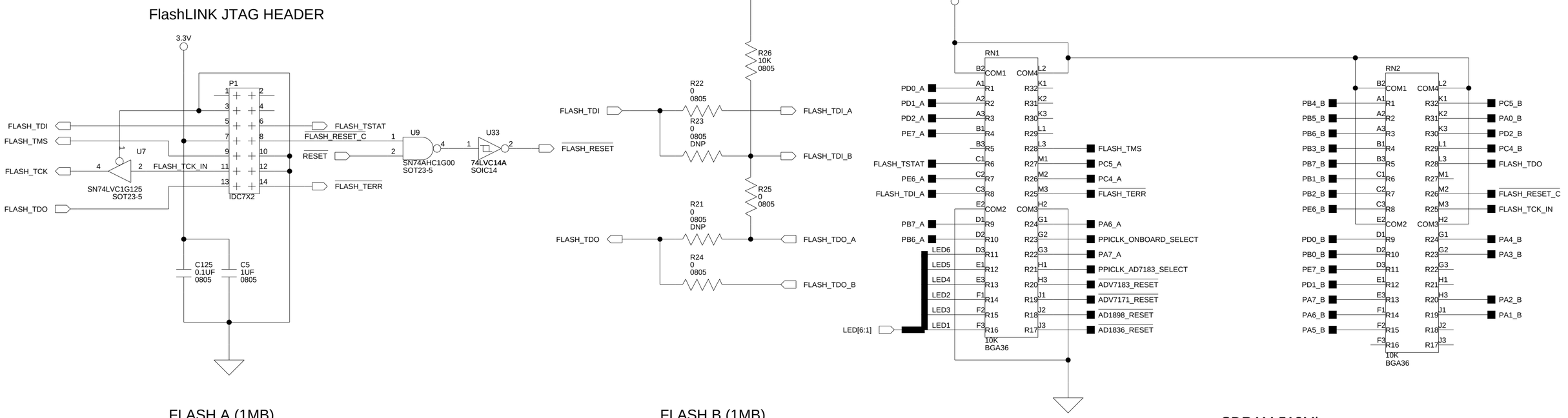
Title	ADSP-BF533 EZ-KIT LITE DSP		
Size C	Board No. A0167-2001		Rev 2.2
Date 5-24-2007_14:20		Sheet 2 of 12	



External Memory Map

Start Adress	End Address	Content
0x0000 0000	0x07FF FFFF	SDRAM Bank 0 (SDRAM)
0x2000 0000	0x200F FFFF	ASYNC Memory Bank 0 (Primary Flash A)
0x2010 0000	0x201F FFFF	ASYNC Memory Bank 1 (Primary Flash B)
0x2020 0000	0x202F FFFF	ASYNC Memory Bank 2 (Flash A and B Secondary Memory, SRAM and Internal Registers)

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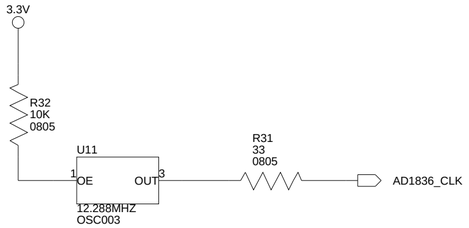
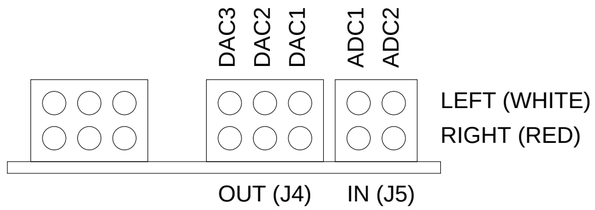
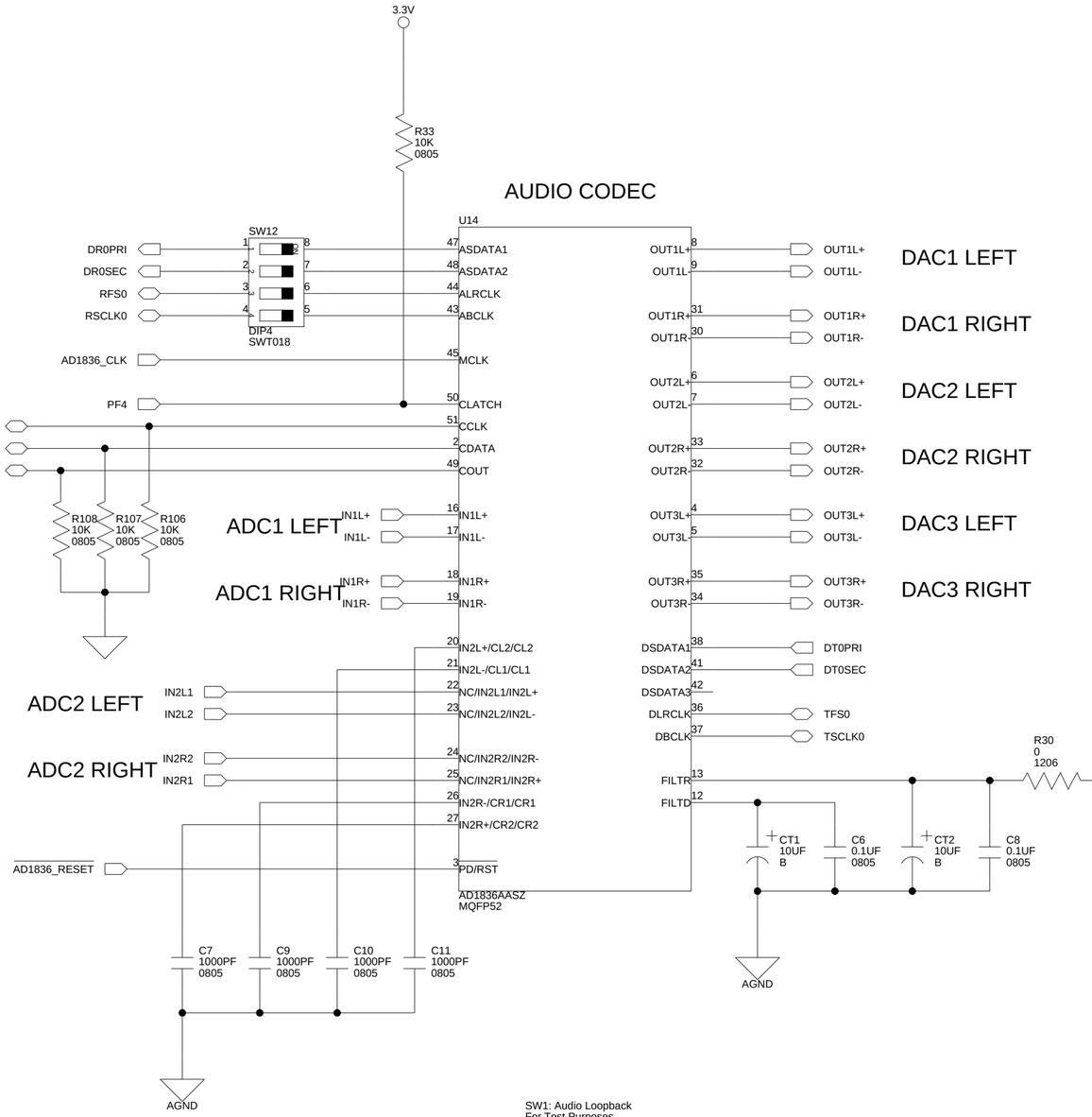
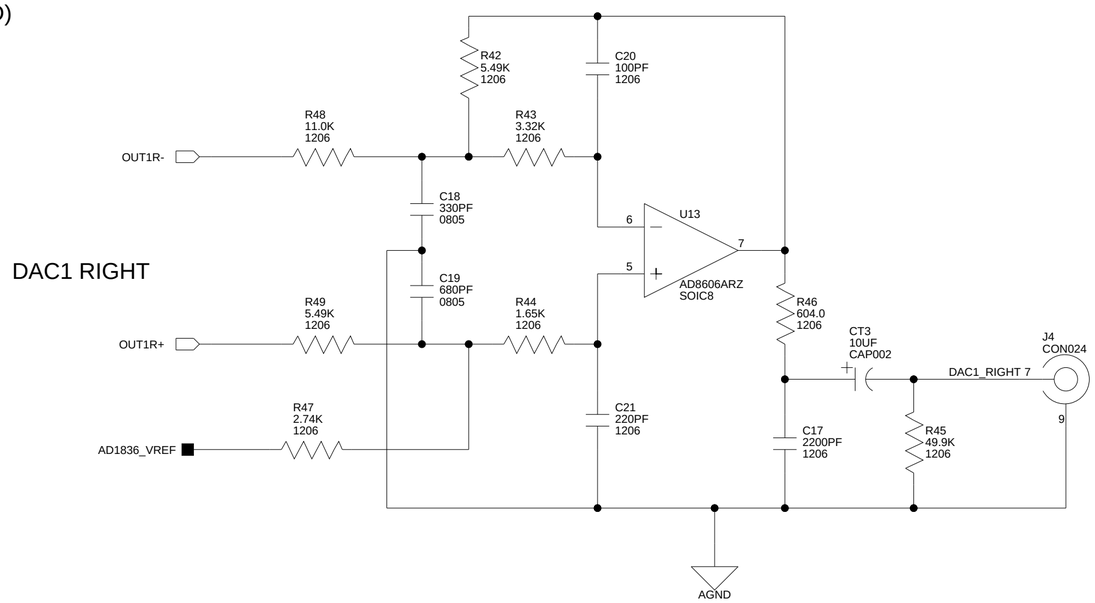
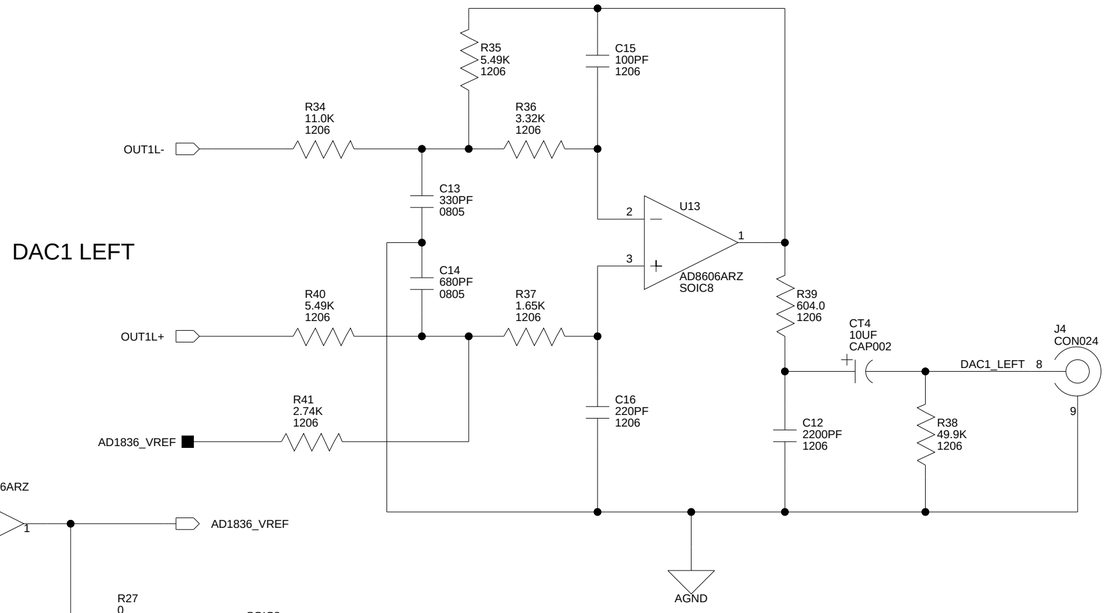
Title	ADSP-BF533 EZ-KIT LITE MEMORY		
Size C	**Board No.** A0167-2001		**Rev** 2.2
Date 5-24-2007_14:20		**Sheet** 3 **of** 12	





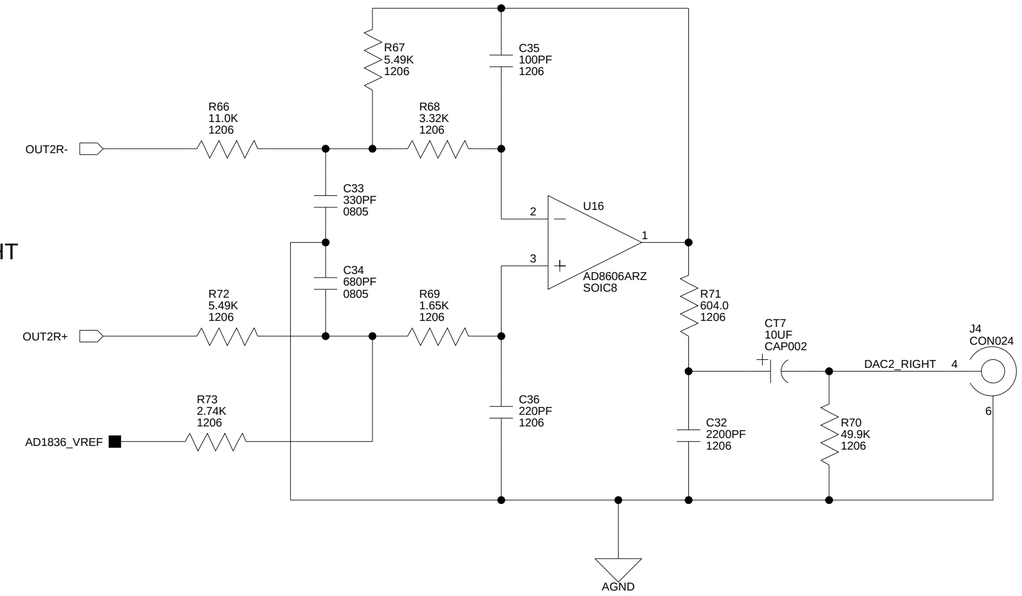




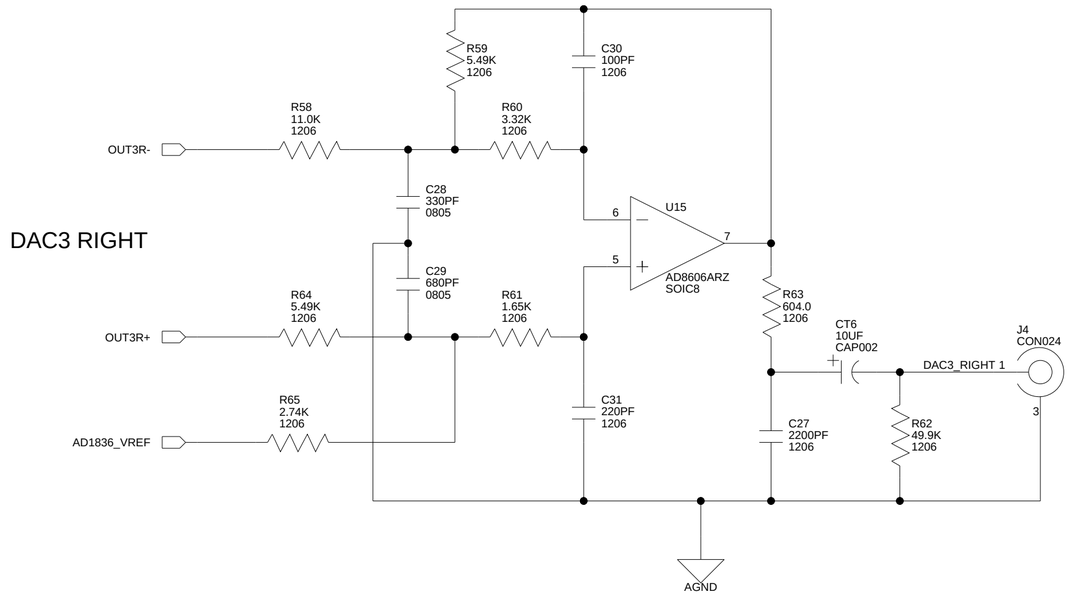


ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF533 EZ-KIT LITE AUDIO CODEC		
Size C	**Board No.** A0167-2001		**Rev** 2.2
Date 5-24-2007_14:20		**Sheet** 4 **of** 12	

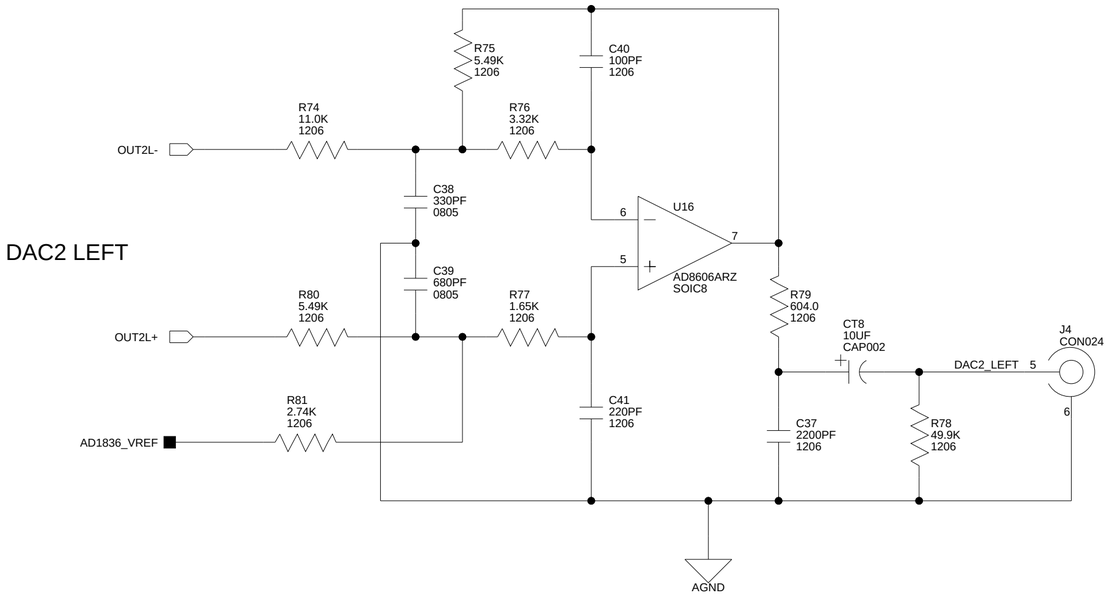
DAC2 RIGHT



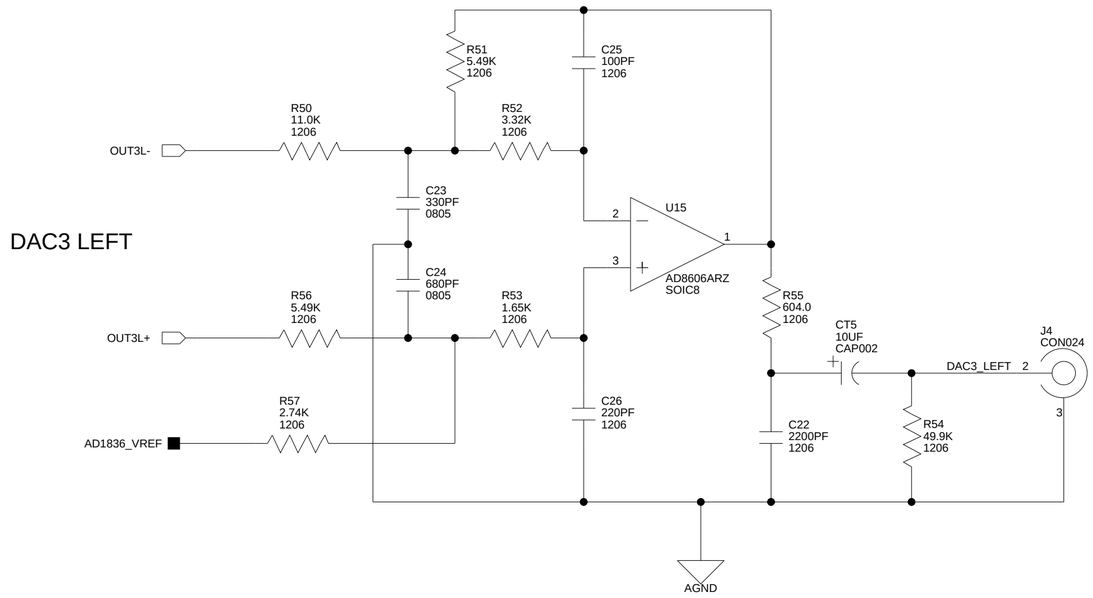
DAC3 RIGHT



DAC2 LEFT



DAC3 LEFT



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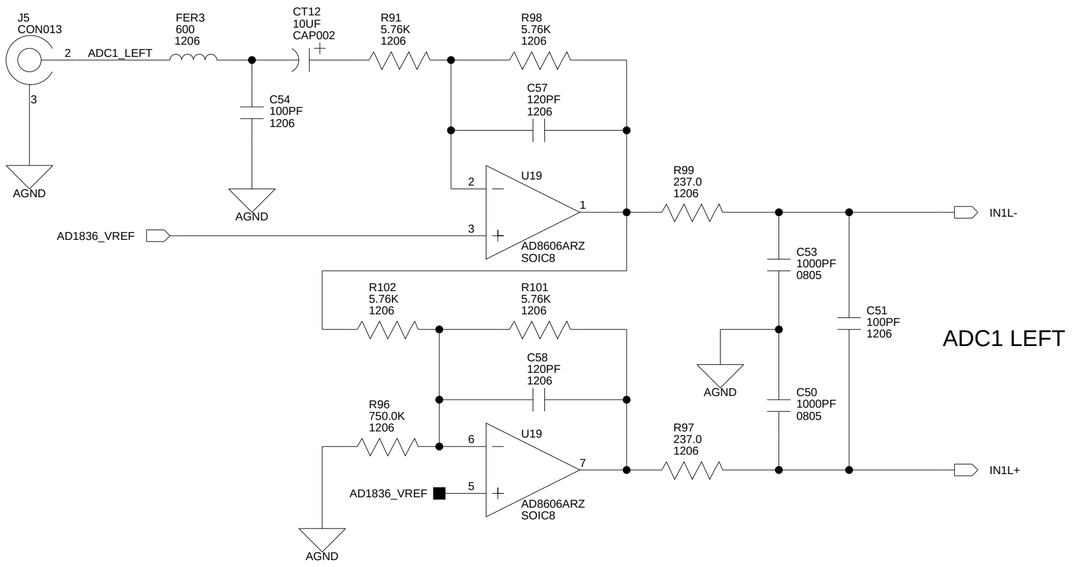
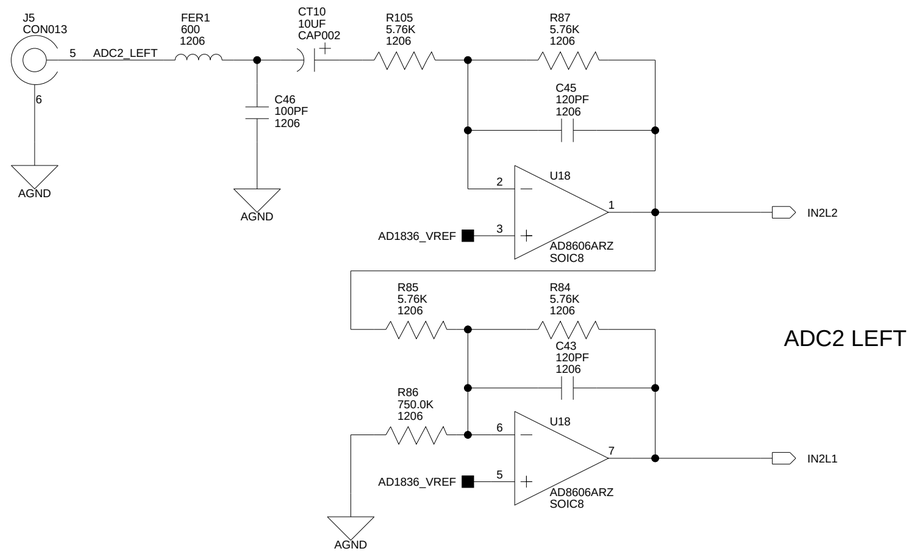
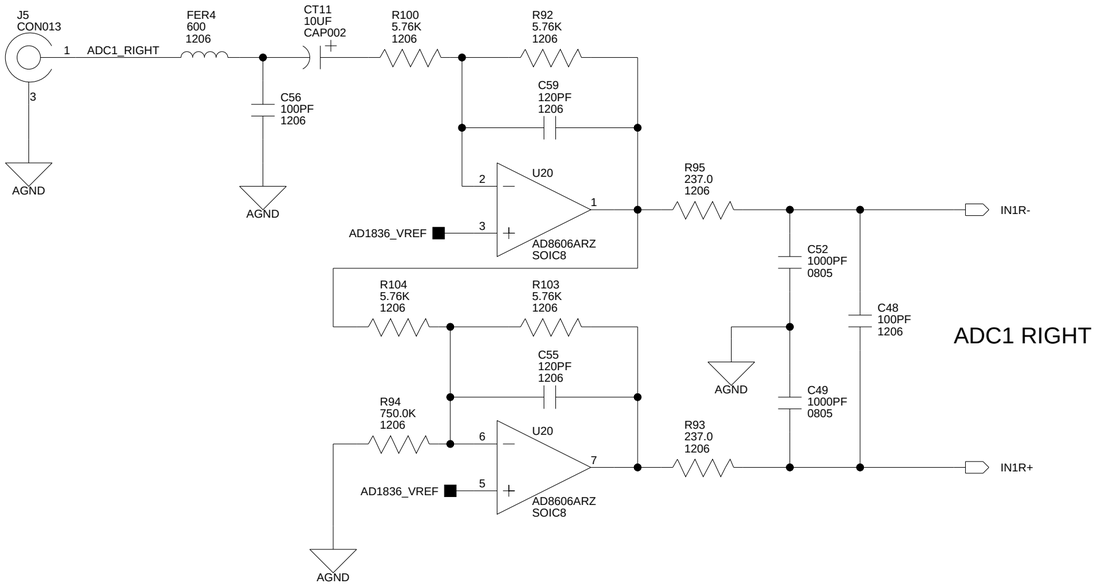
Title	ADSP-BF533 EZ-KIT LITE AUDIO OUT	
Size C	**Board No.** A0167-2001	**Rev** 2.2
Date 5-24-2007_14:20	**Sheet** 5 **of** 12	



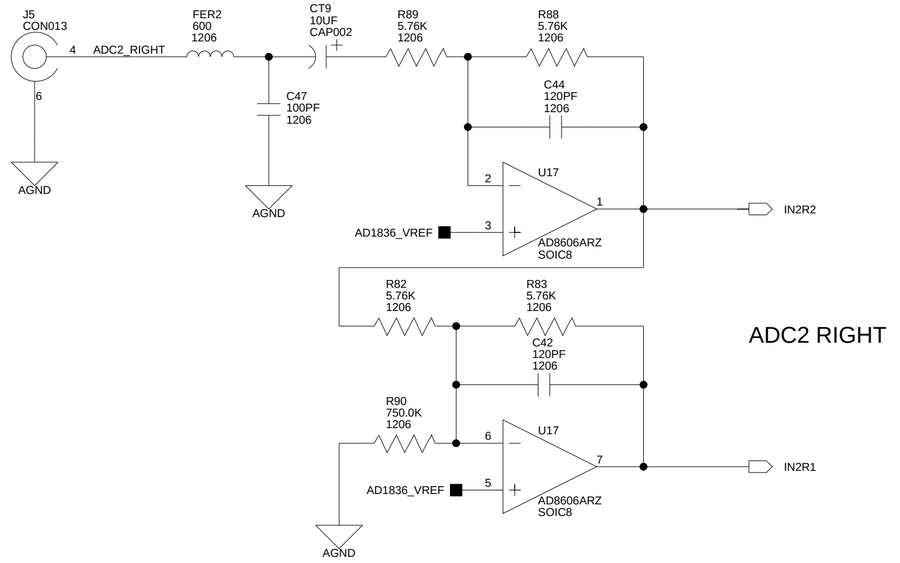
ADC1 LEFT



ADC2 LEFT



ADC1 RIGHT



ADC2 RIGHT

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
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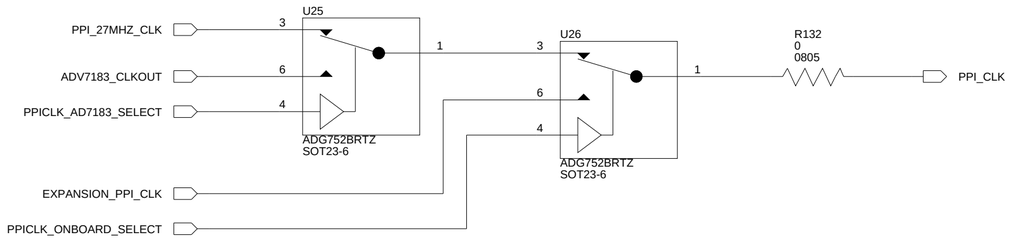
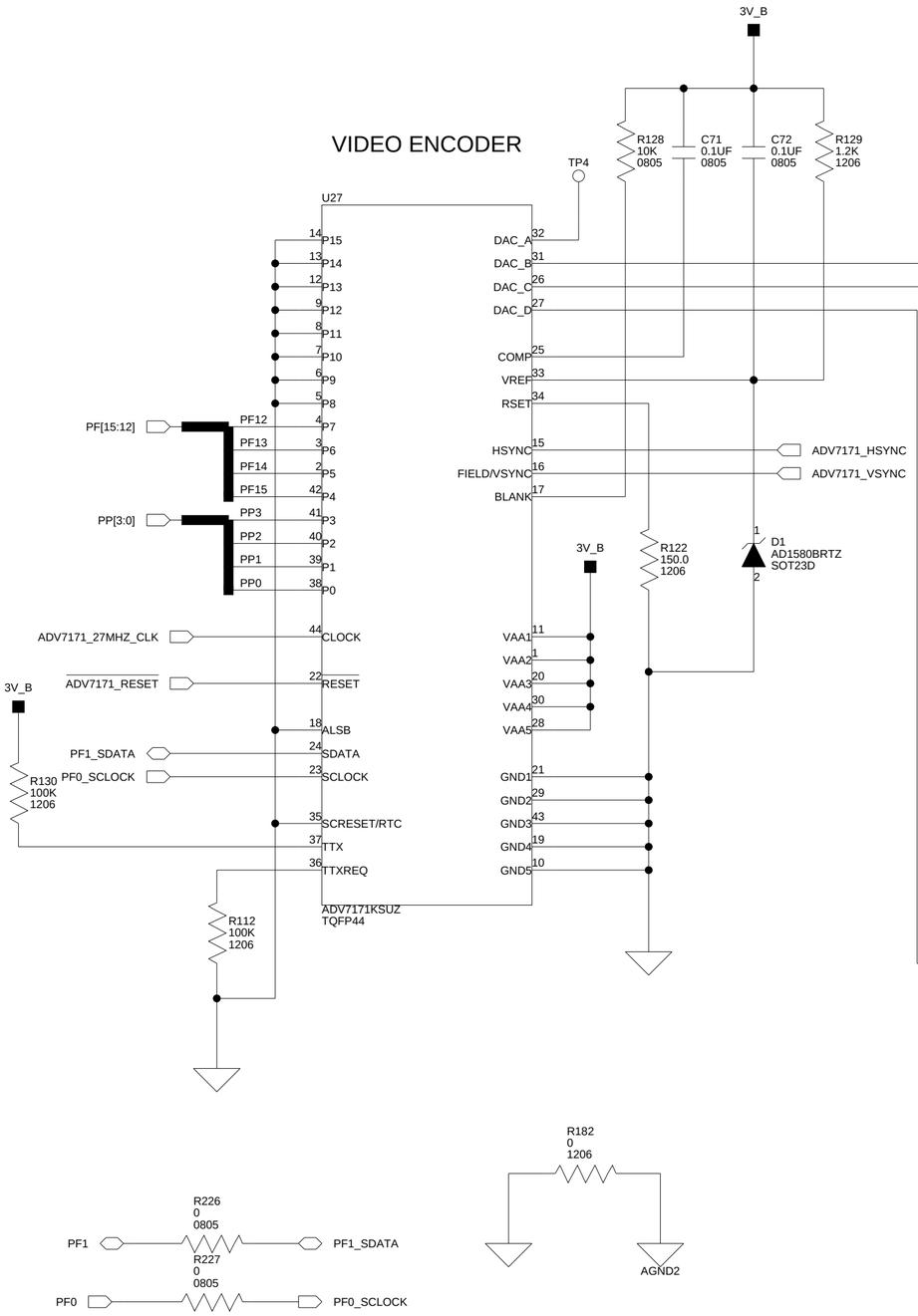
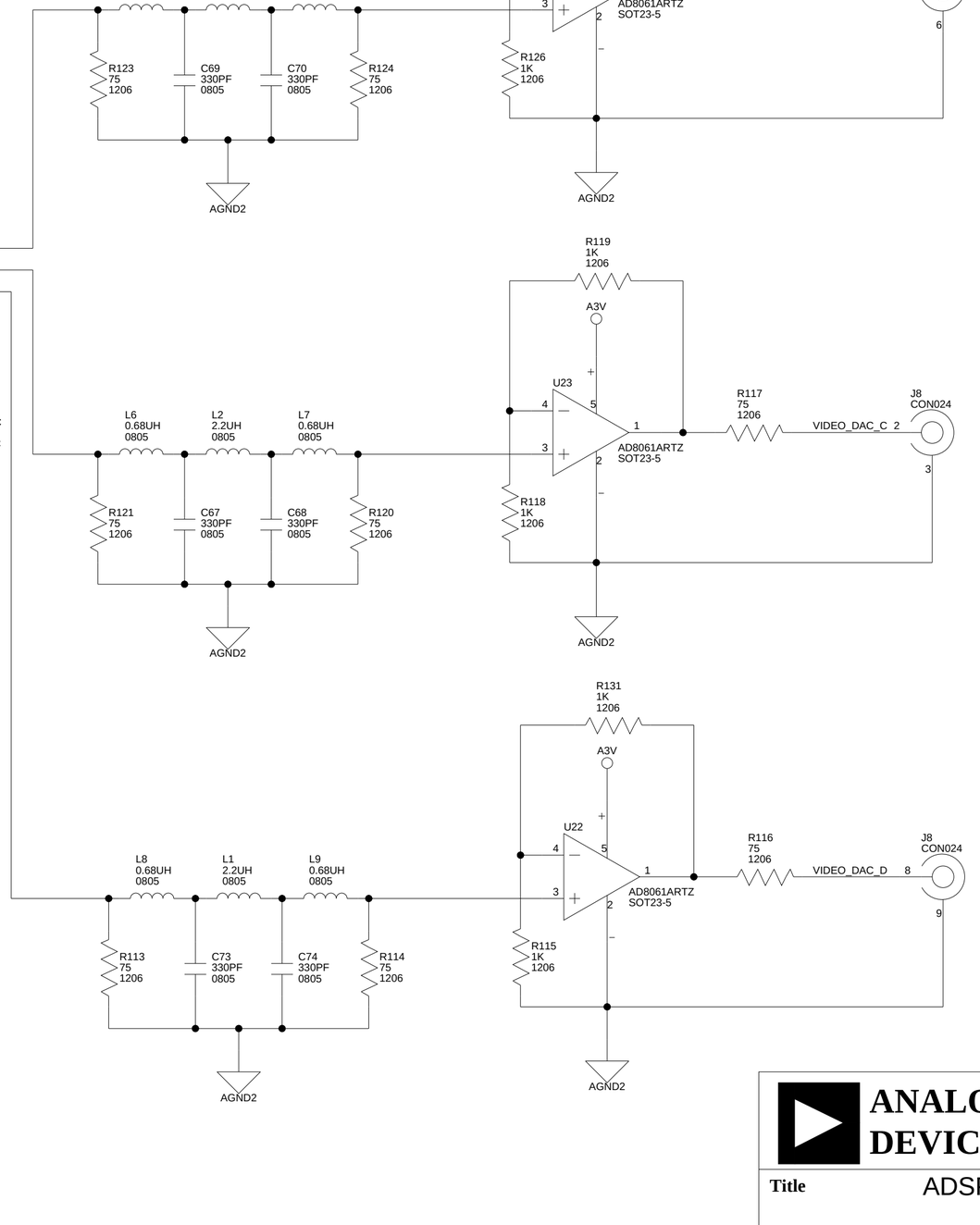
PPICLK_ONBOARD_SELECT	PPICLK_AD7183_SELECT	PPCLK
0	0	PPI_27MHZ_CLK (DEFAULT)
0	1	ADV7183_CLKOUT
1	X	EXPANSION_CLK

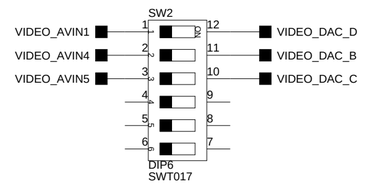
	DAC B	DAC C	DAC D
Composite Video	CVSB		CVSB
Component Video	B	R	G
Differential Component Video	U	V	Y
S Video		C	Y







SW2: Video Loopback
For Test Purposes
Default = All Off



ANALOG DEVICES
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Title	ADSP-BF533 EZ-KIT LITE VIDEO OUT		
Size C	**Board No.** A0167-2001		**Rev** 2.2
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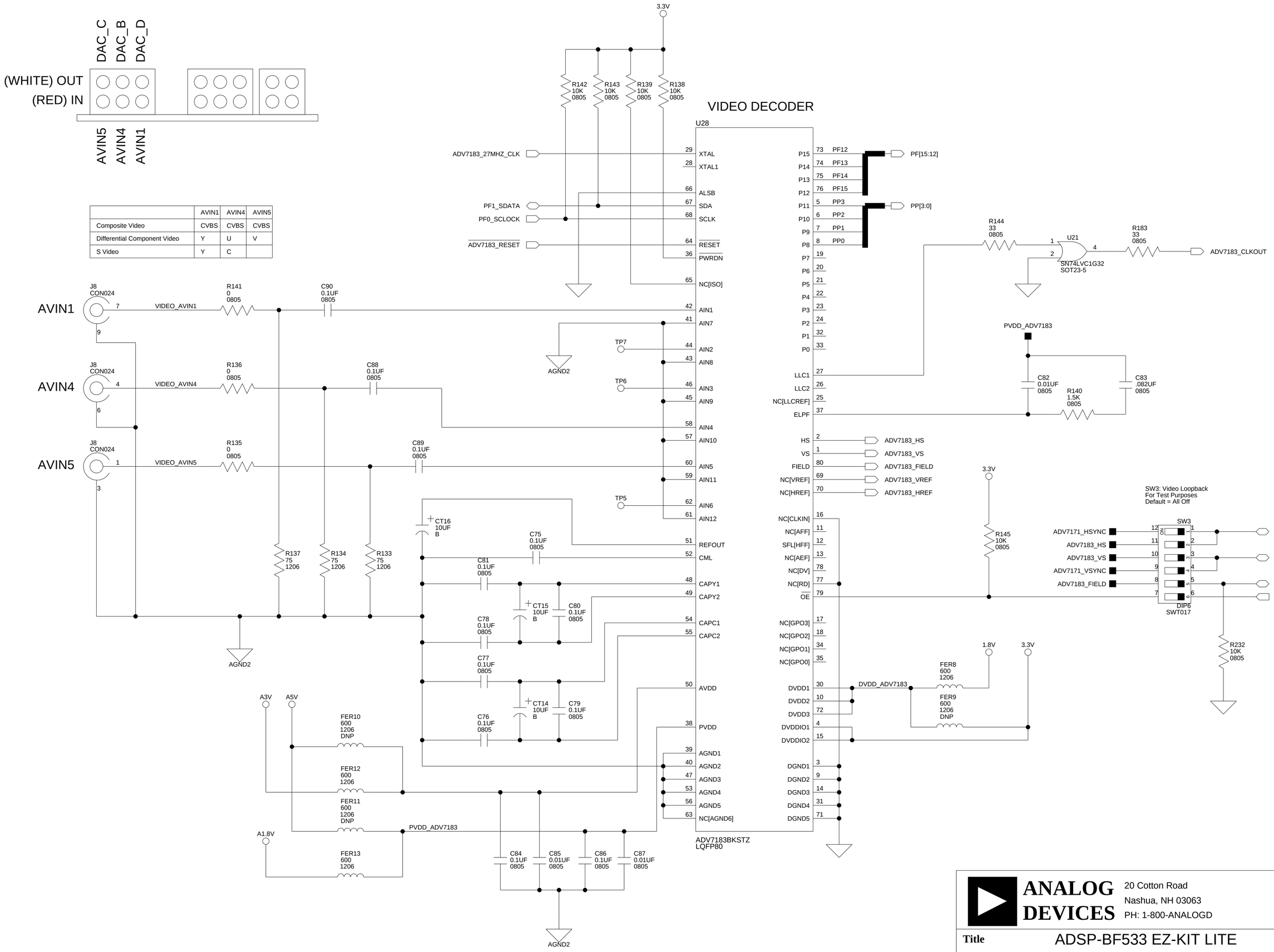

	AVIN1	AVIN4	AVIN5
Composite Video	CVBS	CVBS	CVBS
Differential Component Video	Y	U	V
S Video	Y	C	

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
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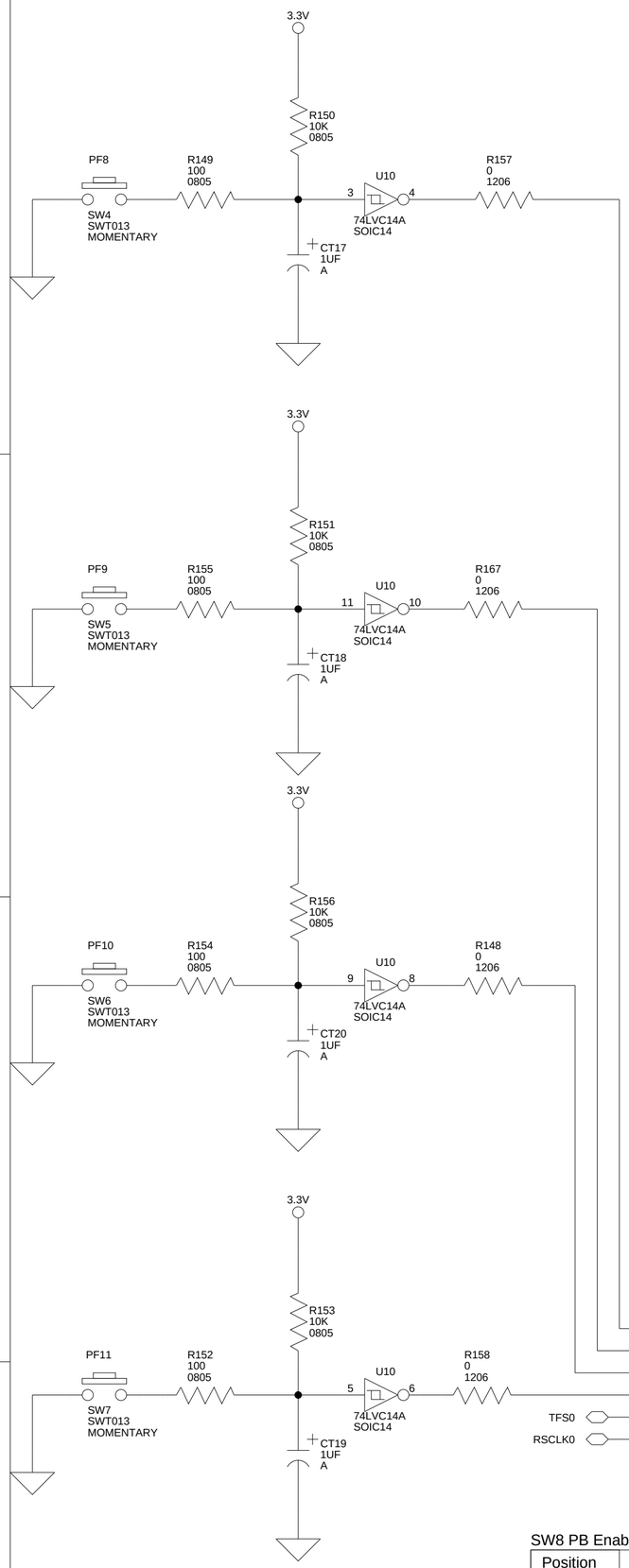

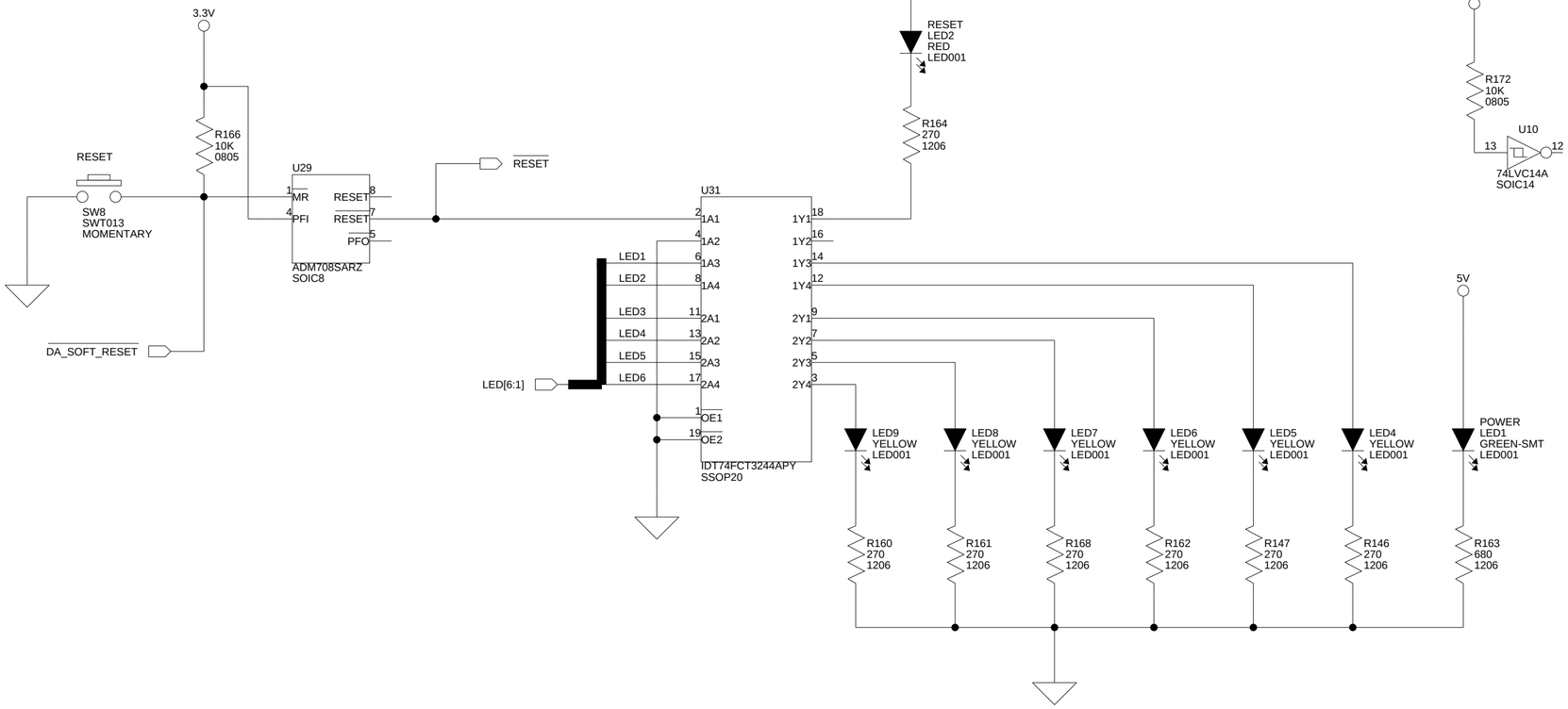

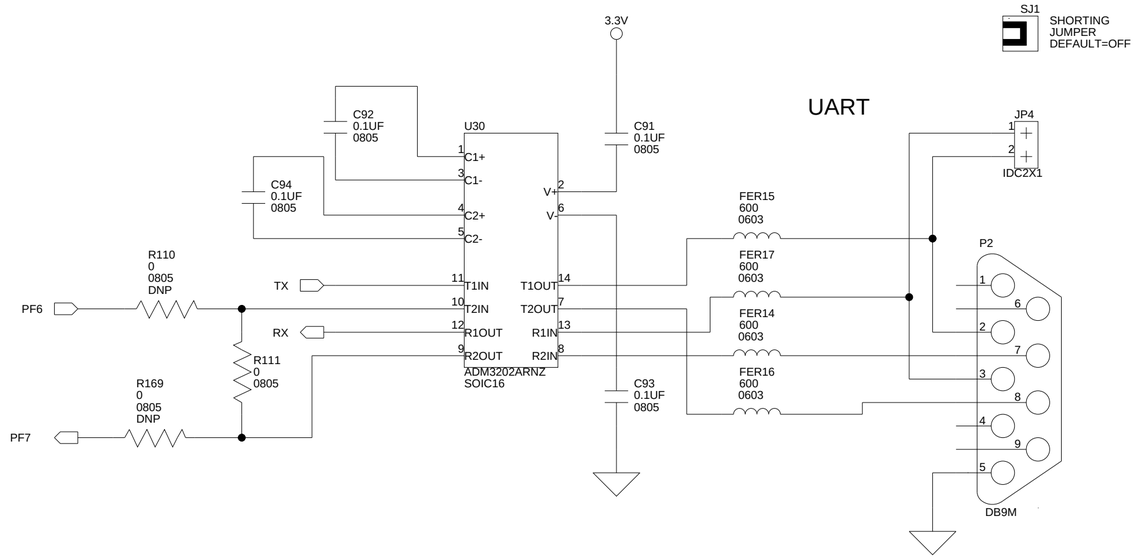

SW8 PB Enable Switch

Position	Function
1-4	Connects the push buttons to the Programmable Flags of the DSP Useful if using the PFs for another purpose.
5,6	Connects SPORT0 frame sync and clock together external to the DSP Required when AD1836 is in I2S mode

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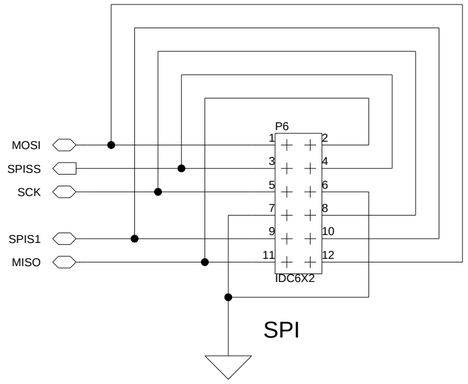
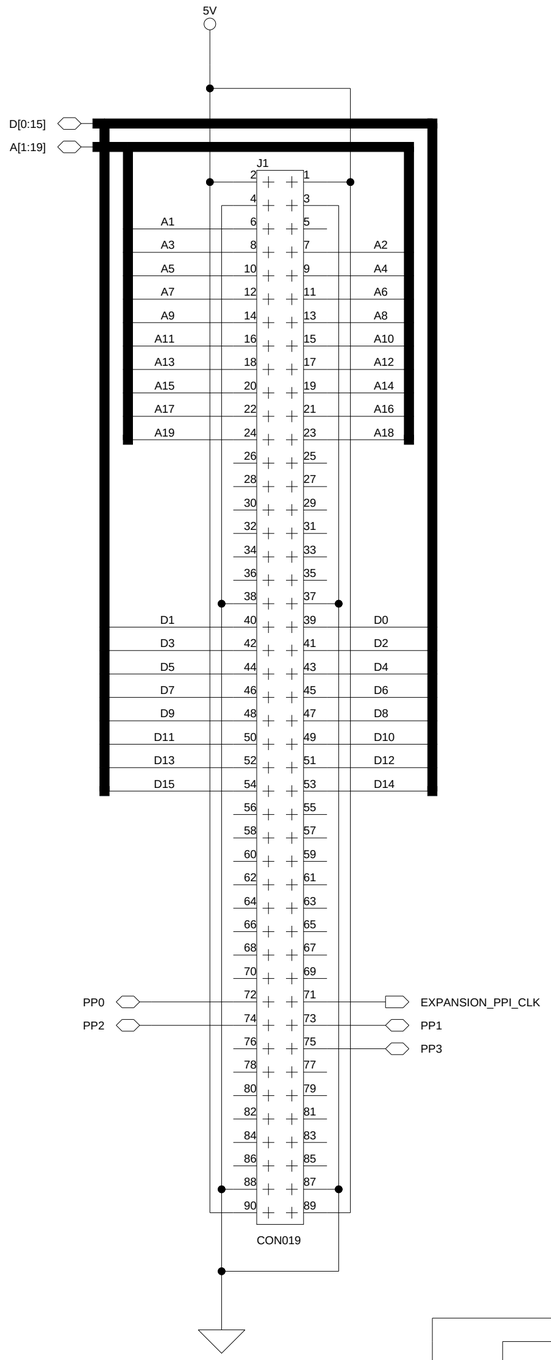
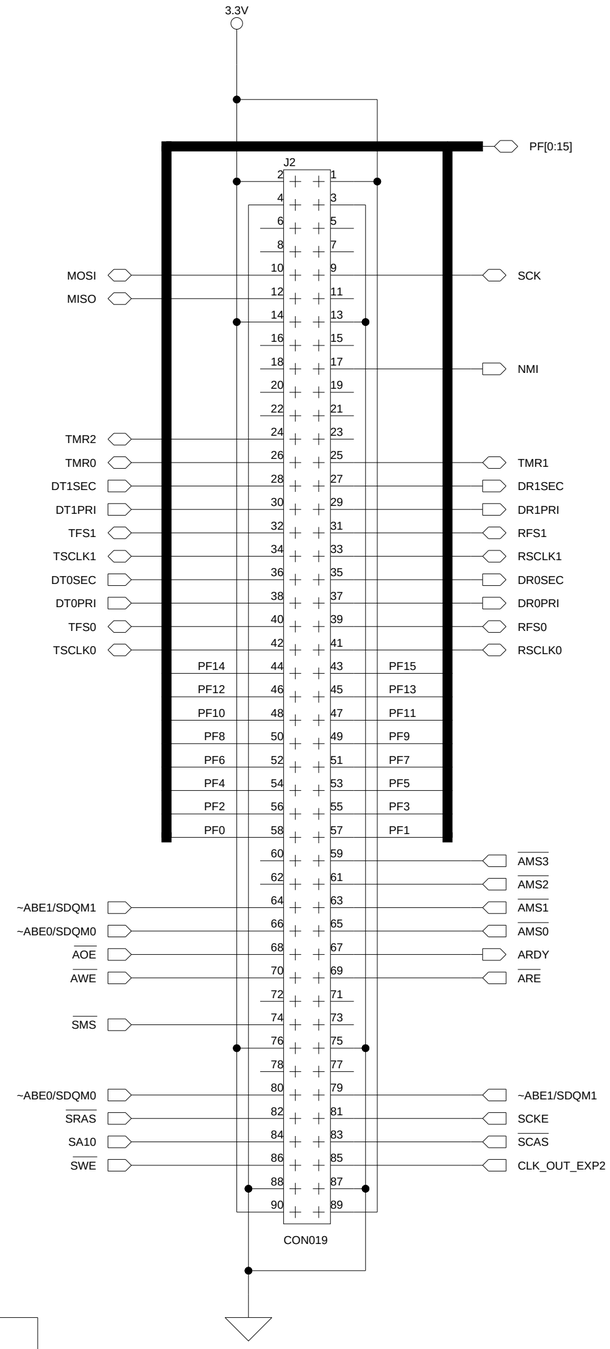
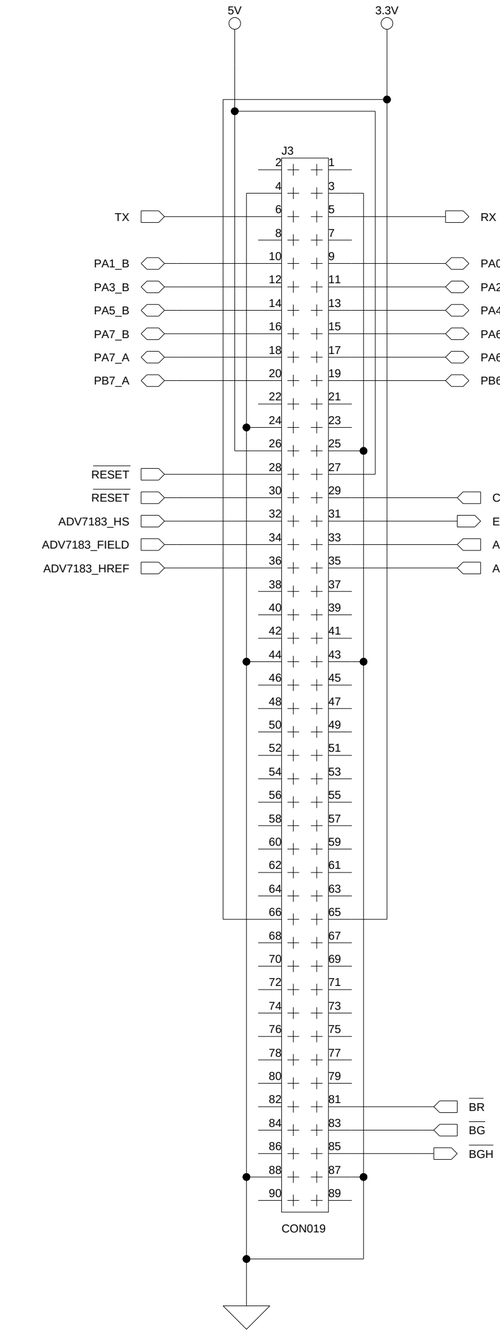
EXPANSION INTERFACE (TYPE B)





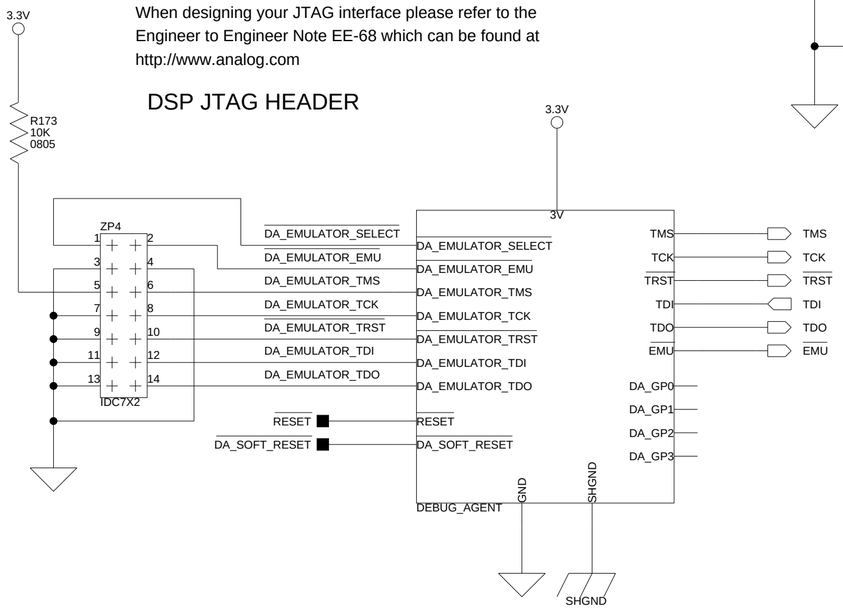




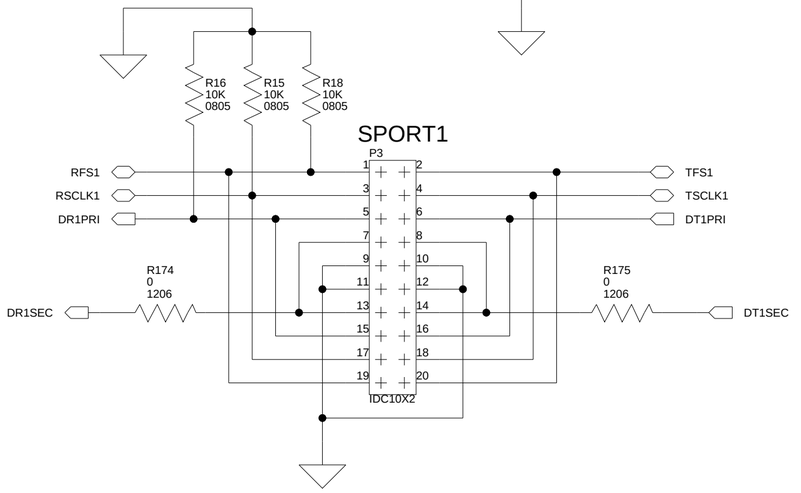
All USB interface circuitry is considered proprietary and has been omitted from this schematic.

When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com

DSP JTAG HEADER



SPORT1



ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF533 EZ-KIT LITE CONNECTORS		
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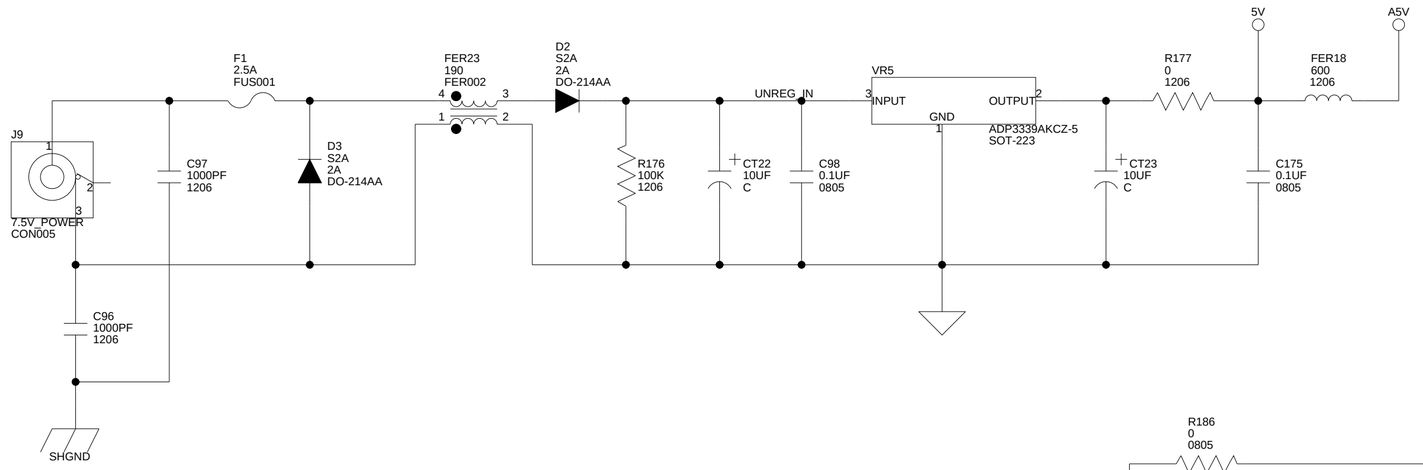
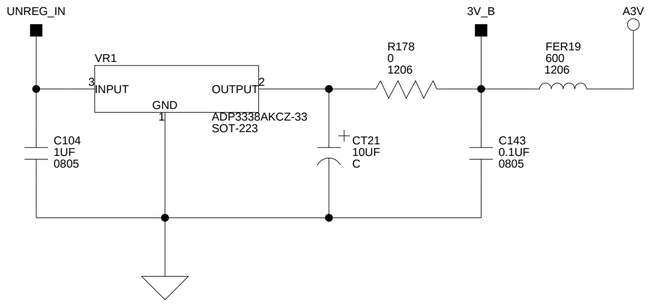
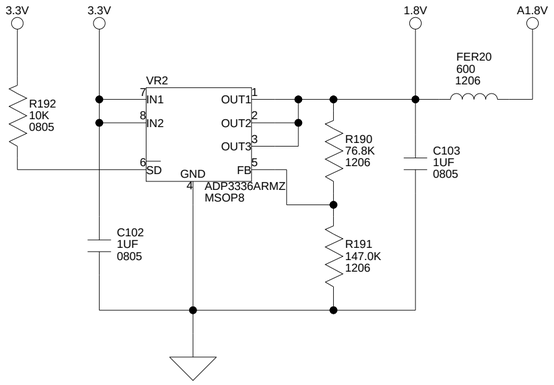
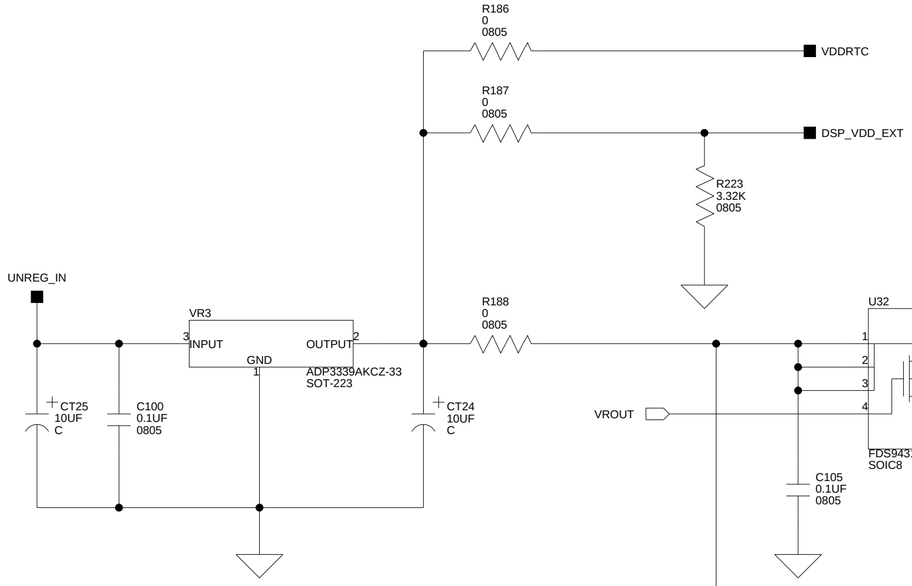




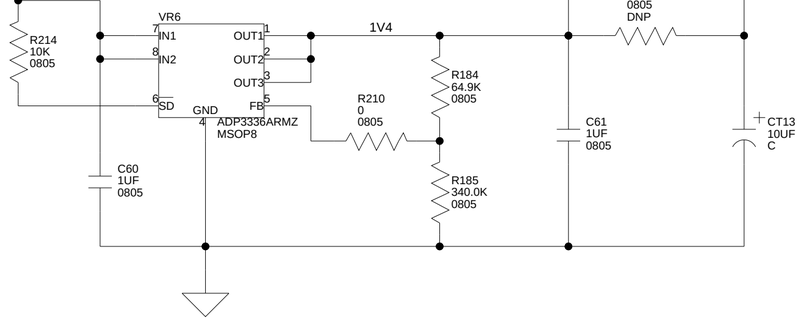


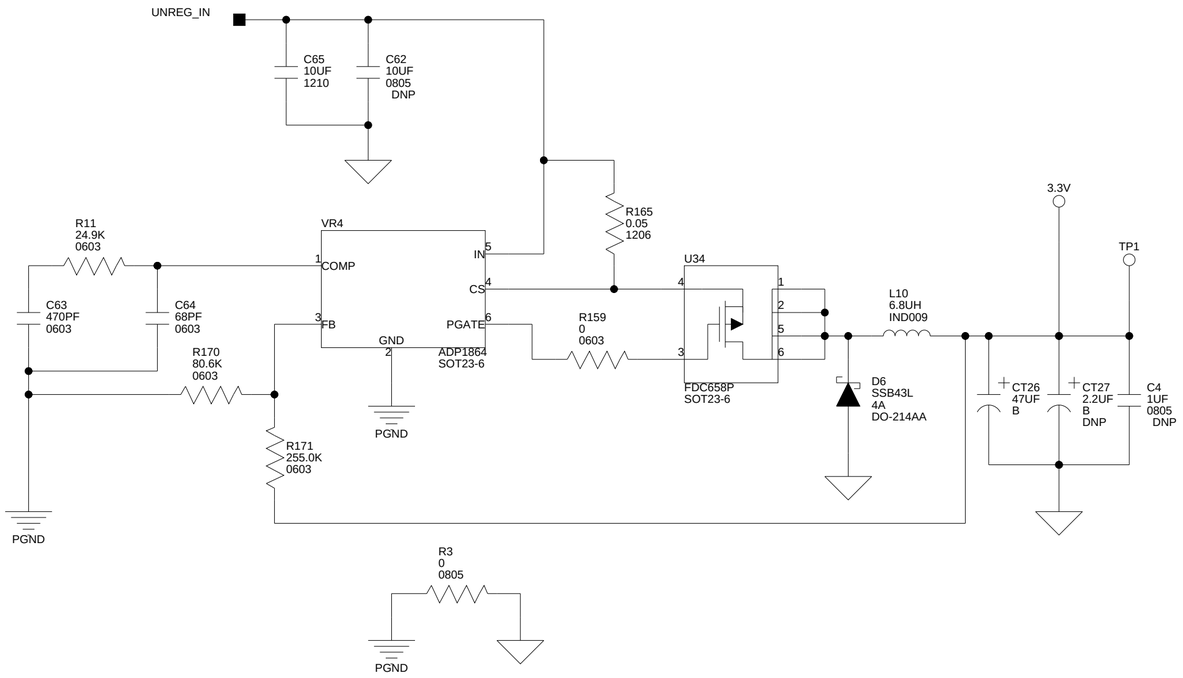


SW10: Core Voltage Source Select
DEFAULT: Not Populated

Position	Function
1 and 2	DSP_VDD_INT = DSP Internal Voltage Regulation
2 and 3	DSP_VDD_INT = 1.4V Fixed

Note: For boards without a 750MHz processor this jumper will not be populated and the DSP_VDD_INT will be hard-wired with R222 to use the processor internal regulator.





ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
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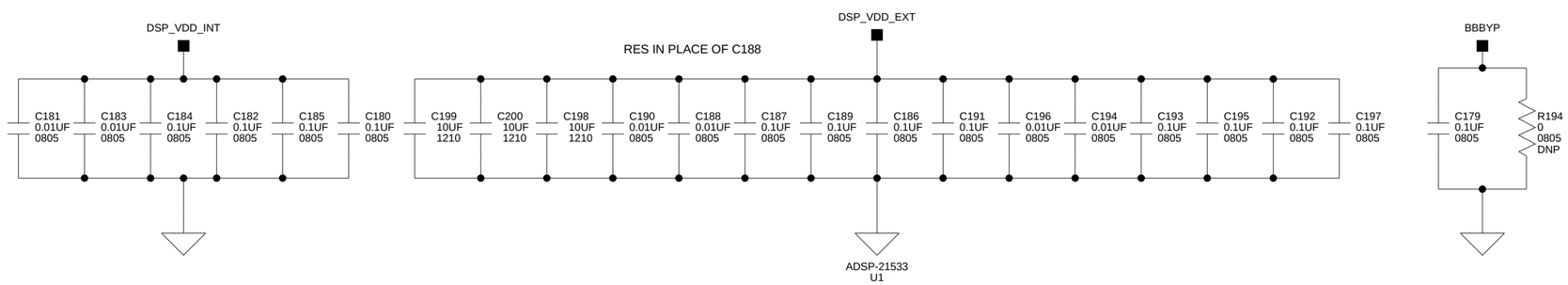

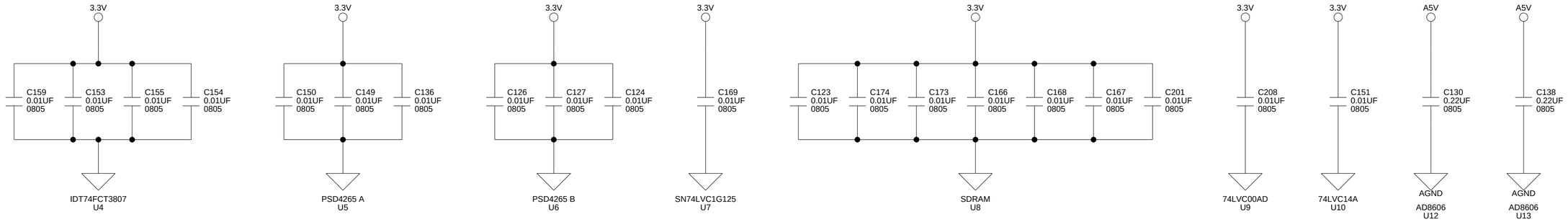

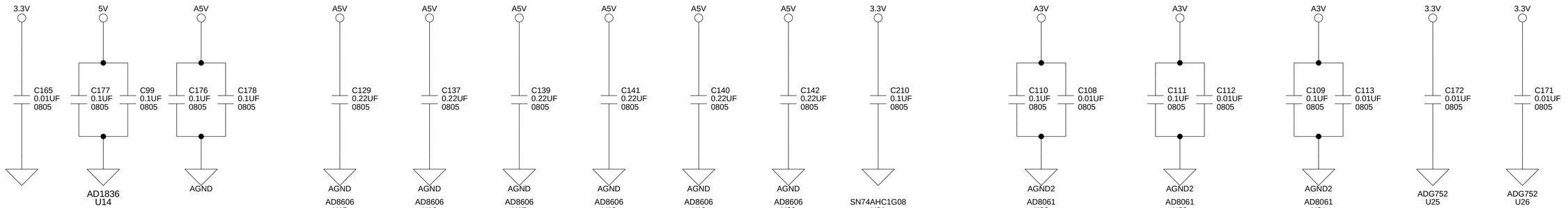

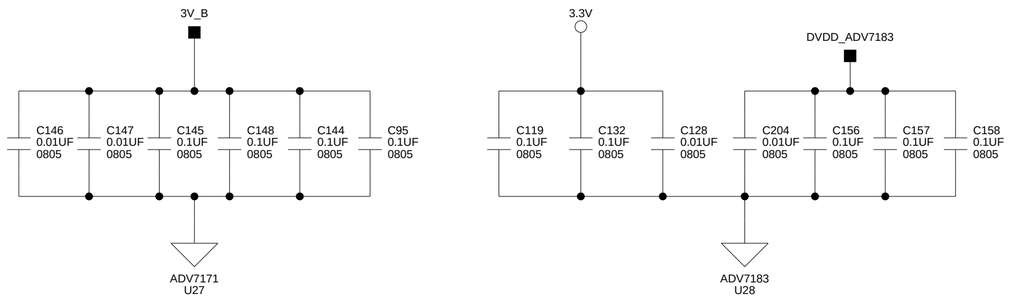

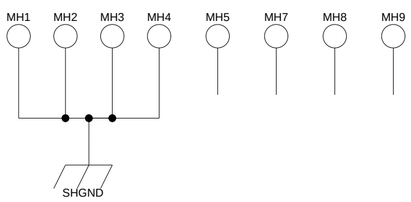

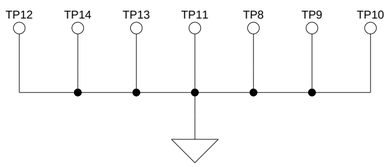

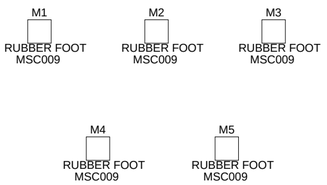

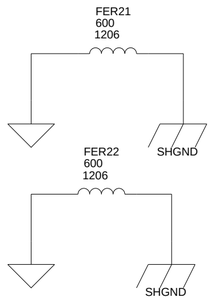

ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
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V