RS9116 n-Link™ and WiSeConnect™ Wi-Fi® and Dual-mode Bluetooth® 5 Wireless Connectivity AA0 Module Solutions Overview

LGA Module (AA0)
14 mm x 15 mm

1.1 Features

Wi-Fi

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +18 dBm with integrated PA
- Receive sensitivity as low as -96 dBm
- Data Rates:- 802.11b: Upto11 Mbps ; 802.11g: Upto54 Mbps ; 802.11n: MCS0 to MCS7
- Operating Frequency Range:- 2412 MHz – 2484 MHz

Bluetooth

- Transmit power up to +16 dBm with integrated PA
- Receive sensitivity:- LE: -92 dBm, LR 125 Kbps: -102 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2Mbps, 3 Mbps
- Operating Frequency Range:- 2.402 GHz - 2.480 GHz
- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently.
- Bluetooth auto rate and auto TX power adaptation
- Scatternet* with two slave roles while still being visible.

RF Features

- Integrated baseband processor with calibration memory, RF transceiver, high-power amplifier, balun and T/R switch
- Dual external antenna (diversity supported)

Power Consumption

- Wi-Fi Standby Associated mode current: 50uA @ 1 second beacon listen interval
- Wi-Fi 1 Mbps Listen current: 14mA
- Wi-Fi LP chain Rx current: 19mA
- Deep sleep current <1uA, Standby current (RAM retention) < 10uA

Operating Conditions

- Wide operating supply range: 1.75 V to 3.63 V
- Operating temperature: -40ºC to +85ºC (Industrial grade)

Size

- Small Form Factor: 14 x 15 x 2.1 mm

Evaluation Kit

- Single Band EVK: RS9116X-SB-EVK1

Software Operating Modes

- Hosted mode (n-Link™): Wi-Fi stack, Bluetooth stack and profiles and all network stacks reside on the host processor
- Embedded mode (WiSeConnect™): Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in RS9116; Some of the Bluetooth profiles reside in the host processor

Hosted Mode (n-Link™)

- Available host interfaces: SDIO 2.0 and USB HS
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Upto 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Embedded Mode (WiSeConnect™)

- Available host interface: UART, SPI, SDIO*, and USB CDC
- TCP throughput > 20Mbps over SDIO host interface with 20 MHz bandwidth

- Support for Embedded Client mode, Access Point mode (Upto 8 clients), Concurrent Client and Access Point mode, and Enterprise Security
- Supports advanced security features: WPA/WPA2-Personal and Enterprise*
- Integrated TCP/IP stack (IPV4/IPV6), HTTP/HTTPS, DHCP, ICMP, SSL 3.0/TLS1.2, WebSockets, IGMP, DNS, DNS-SD, SNMP, FTP Client, MQTT*
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support* for GAP, SDP, L2CAP, RFCOMM, SPP, GATT, PBAP
- Wireless firmware upgrade and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

Wireless Co-Existence Modes

- Wi-Fi Access Point, Wi-Fi Client
- Wi-Fi Access Point + Wi-Fi Client
- Wi-Fi (Client / AP) + Bluetooth 5
- Wi-Fi (Client / AP) + Bluetooth Low Energy
- Wi-Fi (Client) + Bluetooth 5 + Bluetooth Low Energy

Security

- Accelerators: AES128/256 in Embeded Mode
- WPA/WPA2-Personal, WPA/WPA2 Enterprise for Client*
- Secure Firmware upgrade* with backup

Software and Regulatory Certification

- Wi-Fi Alliance*
- Bluetooth Qualification*
- Regulatory certifications (FCC, IC, CE/ETSI, TELEC)*

* For detailed list of Software features, and available profiles, please refer the Software Reference Manuals, or, Contact Silicon Labs for availability.

All power and performance numbers are under ideal conditions.

1.2 Applications

Wearables:

SmartWatches, Wristbands, Fitness Monitors, Smart Glasses, etc.

SmartHome:

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs /switches, LED lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other consumer applications:

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart-City, etc.):

Healthcare Tags, Medical patches/pills, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, etc.

1.3 Description

Silicon Labs' RS9116 single band AA0 module provides a comprehensive multi-protocol wireless connectivity solution including 802.11 b/g/n (2.4GHz), and dual-mode Bluetooth 5. The modules offers high throughput, extended range with power-optimized performance. The modules are FCC, IC, and ETSI/CE certified.

1.4 Block Diagrams

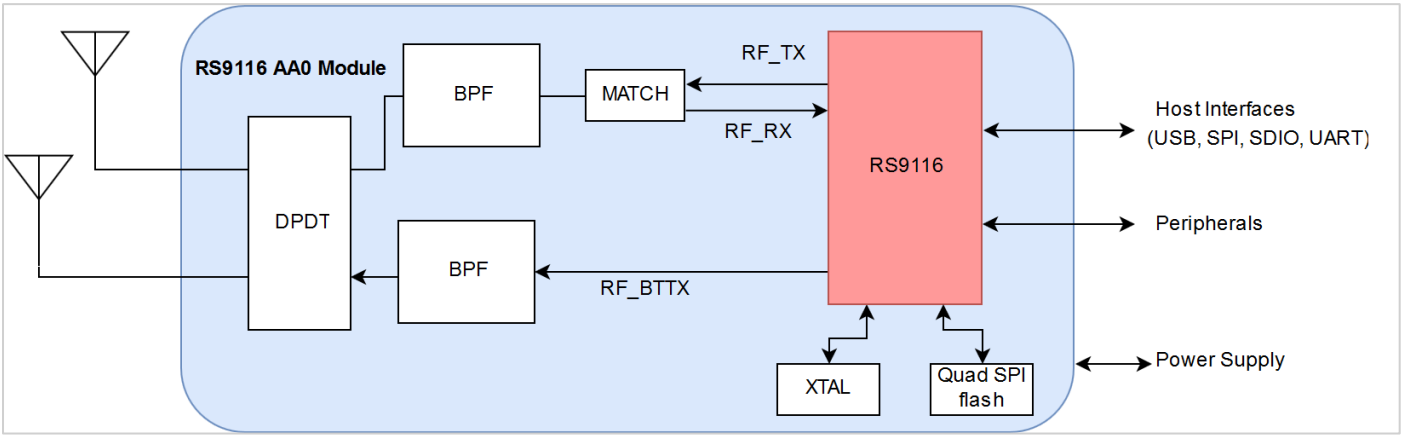

Figure 1 AA0 Module Block Diagram

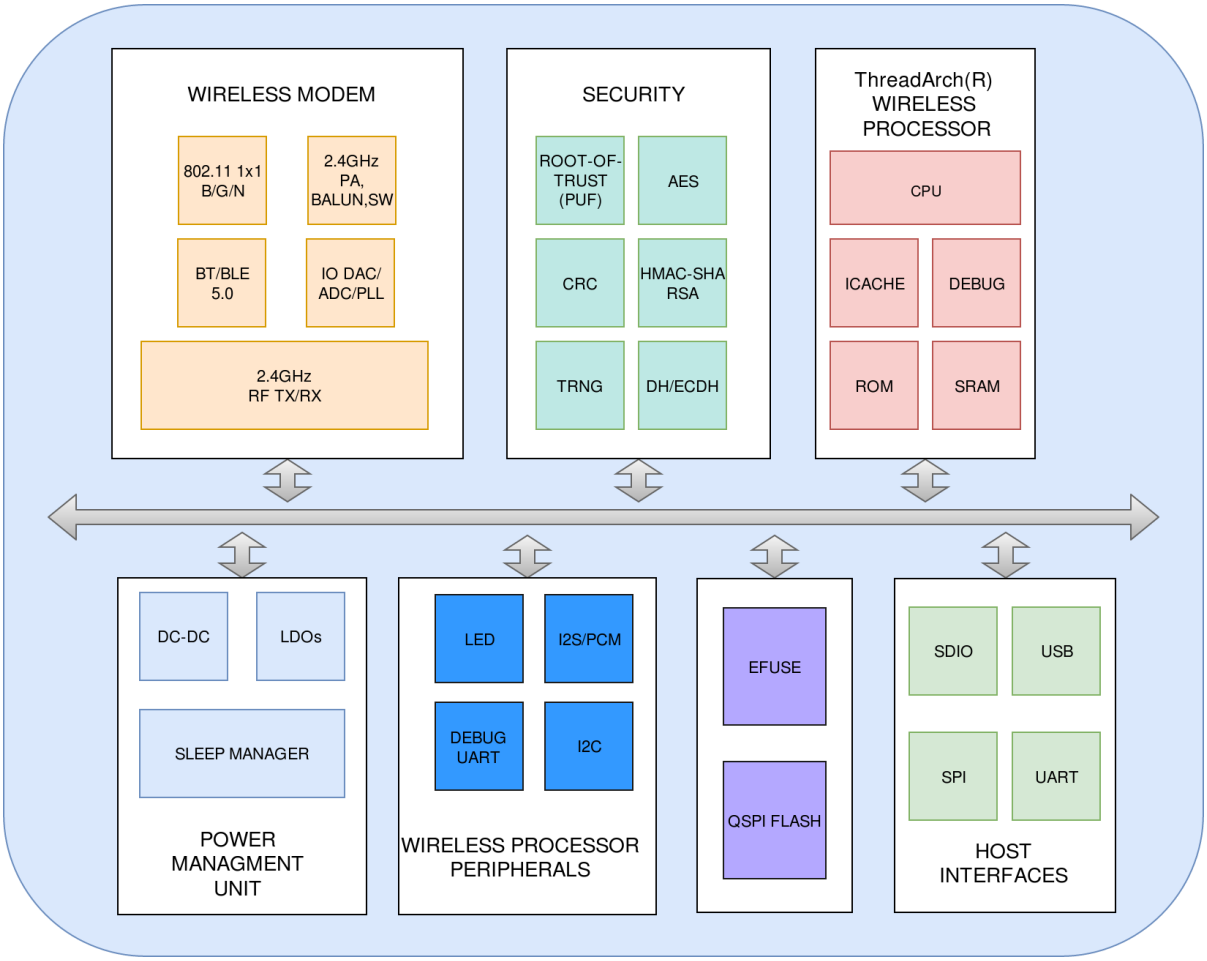

Figure 2 RS9116 Connectivity Hardware Block Diagram

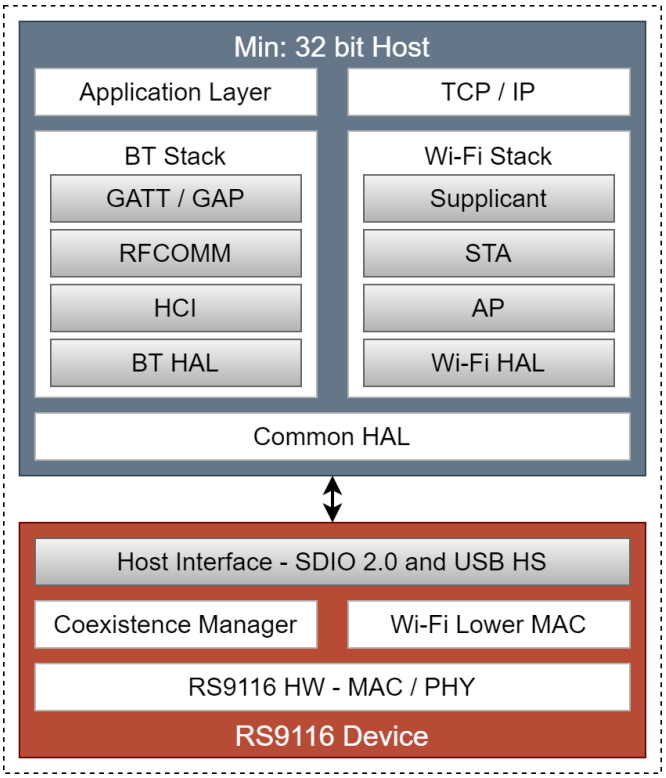

Figure 3 Hosted Software Architecture

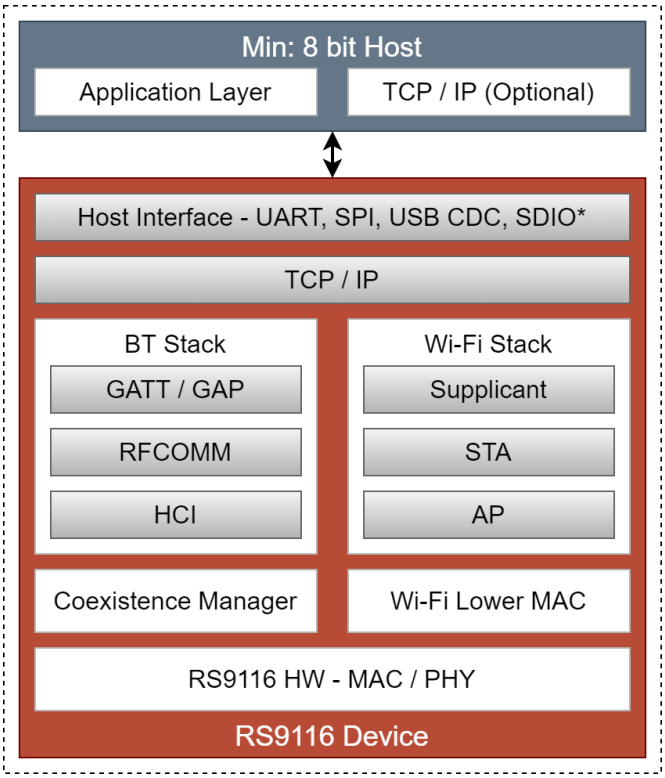

Figure 4 Embedded Software Architecture

1.5 Device Information

Part Number	Flash Type	Package Type	Package Size	Silicon Rev	Firmware Version
RS9116W-SB00-AA0-X24	Internal	LGA(101)	14 mm x 15 mm x 2.1 mm	1.3	1.2.24
RS9116N-SB00-AA0-X00	Internal	LGA(101)	14 mm x 15 mm x 2.1 mm	1.3	Not Applicable

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2 RS9116 AA0 module Pinout and Pin Description

2.1 Pin Diagram

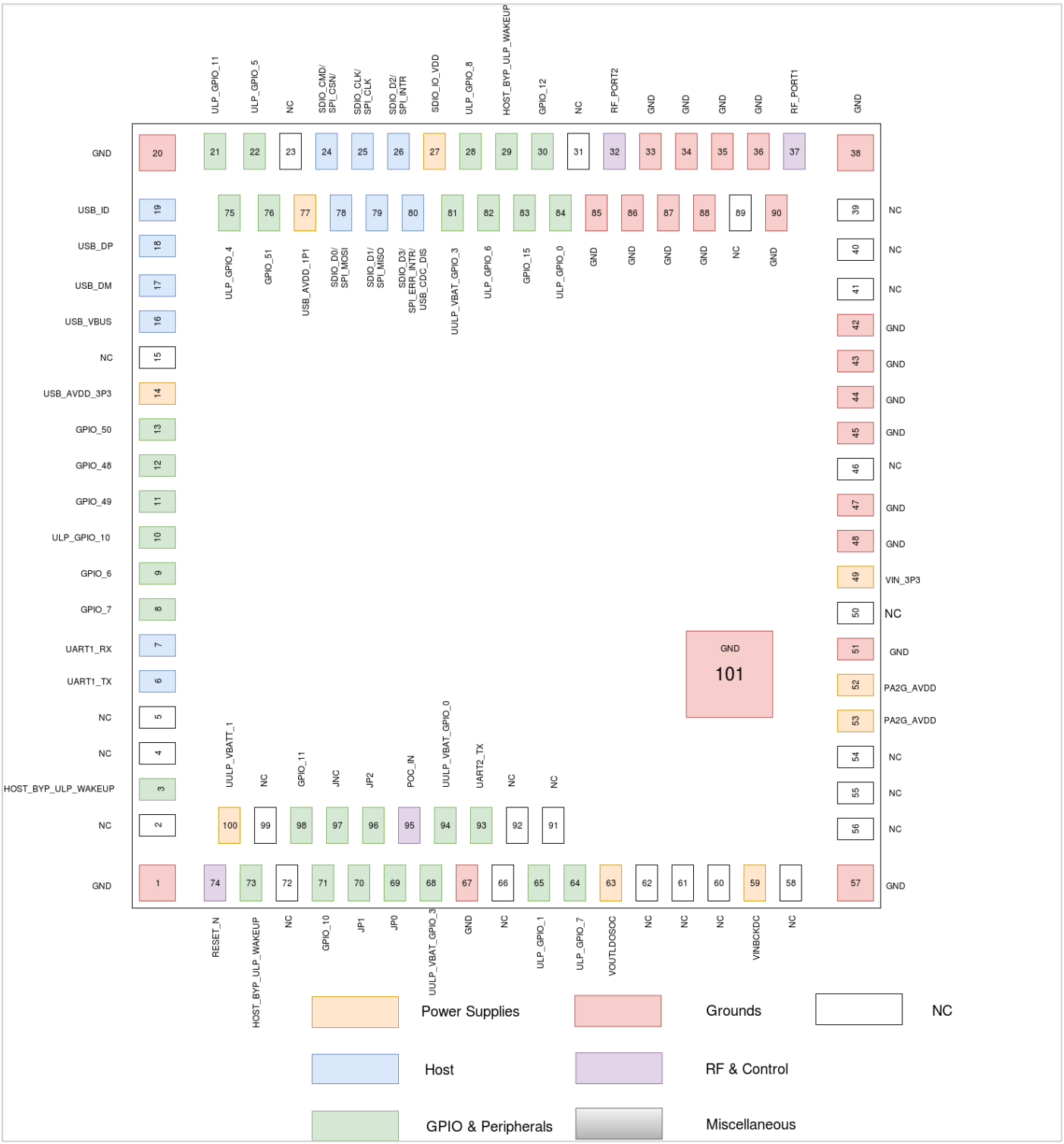

Figure 5 RS9116 AA0 pin diagram

2.2 Pin Description

2.2.1 RF & Control Interfaces

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_PORT1	37	NA	Inout	NA	Secondary antenna port, used for Antenna diversity. If used, connect to Antenna with a 50 Ω impedance as per the Reference Schematics. If unused, leave unconnected.
RF_PORT2	32	NA	Inout	NA	Default Antenna port. Connect to Antenna with a 50 Ω impedance as per the Reference Schematics.
RESET_N	74	UULP_VBATT_1	Input	NA	Active-low reset asynchronous reset signal.
POC_IN	95	UULP_VBATT_1	Input	NA	Power On Control Input.

Table 1 RF & Control Interfaces

2.2.2 Power & Ground Pins

Pin Name	Type	Pin Number	Direction	Description
UULP_VBATT_1	Power	100	Input	Always-on VBATT Power supply to the UULP domains
VIN_3P3	Power	49	Input	Digital Power Supply
VINBCKDC	Power	59	Input	Power supply for the on-chip Buck
VOUTLDOSOC	Power	63	Output	The output of SoC LDO
SDIO_IO_VDD	Power	27	Input	I/O Supply for SDIO I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
PA2G_AVDD	Power	52,53	Input	Power supply for the 2.4 GHz RF Power Amplifier
USB_AVDD_3P3	Power	14	Input	Power Supply for the USB interface

Pin Name	Type	Pin Number	Direction	Description
USB_AVDD_1P1	Power	77	Input	Power supply for the USB core
GND	Ground	1, 20, 33, 34, 35, 36, 38, 42, 43, 44, 45, 47, 48, 51, 57, 67, 85, 86, 87, 88, 90, 101	GND	Common ground pins

Table 2 Power and Ground Pins

2.2.3 Host & Peripheral Interfaces

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_6	9	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2S_DOUT - I2S interface output data. • PCM_DOUT - PCM interface output data.
GPIO_7	8	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2S_CLK - I2S interface clock. • PCM_CLK - PCM interface clock.
UART1_RX	7	VIN_3P3	Inout	HighZ	**Host** / **Default** / **Sleep** UART / UART1_RX - UART Host interfaces serial input. / HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					Non UART: HighZ / HighZ The UART interface is supported only in WiSeConnect™.
UART1_TX	6	VIN_3P3	Inout	HighZ	Host: UART — Default: UART1_TX - UART Host interfaces serial output. — Sleep: HighZ Non UART: HighZ / HighZ The UART interface is supported only in WiSeConnect™.
GPIO_10	71	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2S_DIN: I2S interface input data. • PCM_DIN - PCM interface input data.
GPIO_11	98	VIN_3P3	Inout	HighZ	**Default :** HighZ. **Sleep**: HighZ This pin can be configured by software to be any of the following • I2S_WS: I2S interface Word Select. • PCM_FSYNC: PCM interface Frame Synchronization signal.
GPIO_12	30	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					This pin can be configured by software to be any of the following • UART1_RTS - UART interface Request to Send, if UART Host Interface flow control is enabled. The UART interface is supported only in WiSeConnect™.
GPIO_15	83	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • UART1_CTS - UART interface Clear to Send, if UART Host Interface flow control is enabled. • UART1_TRANSPARENT_MODE - UART Host interface Transparent Mode, Indication that module has entered into TRANSPERENT_MODE • TSF_SYNC - Transmit Synchronization Function signal to indicate to the Host when a packet is transmitted. The signal is toggled once at the end of every transmitted packet. The UART interface is supported only in WiSeConnect™.
SDIO_CLK/SPI_CLK	25	SDIO_IO_VDD	Inout	HighZ	**Host**: SDIO **Default**: SDIO_CLK - SDIO interface clock **Sleep**: HighZ

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					SPI: SPI_CLK - SPI Slave interface clock — HighZ Non SDIO,SPI: HighZ — HighZ The SPI interface is supported only in WiSeConnect™.
SDIO_CMD/SPI_CSN	24	SDIO_IO_VDD	Inout	HighZ	**Host / Default / Sleep** SDIO: SDIO_CMD - SDIO interface CMD signal — HighZ SPI: SPI_CSN - Active-low Chip Select signal of SPI Slave interface — HighZ Non SDIO,SPI: HighZ — HighZ The SPI interface is supported only in WiSeConnect™.
SDIO_D0/SPI_MOSI	78	SDIO_IO_VDD	Inout	HighZ	**Host / Default / Sleep** SDIO: SDIO_D0 - SDIO interface Data0 signal — HighZ SPI: SPI_MOSI - SPI Slave interface Master-Out-

<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>
<table>
<tr><td></td><td>Slave-In signal</td><td></td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
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The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_D1/SPI_MISO</td><td>79</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D1 - SDIO interface Data1 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_MISO - SPI Slave interface Master-In-Slave-Out signal</td><td>HighZ</td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_D2/SPI_INTR</td><td>26</td><td>SDIO_IO_VDD</td><td>Inout</td><td>HighZ</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D2 - SDIO interface Data2 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_INTR - SPI Slave interface Interrupt</td><td>HighZ</td></tr>
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<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>I/O Supply Domain</th><th>Direction</th><th>Initial State (Power up, Active Reset)</th><th>Description [1,2,3,4]</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>
<table>
<tr><td></td><td>Signal to the Host</td><td></td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>SDIO_D3/SPI_ERR_INTR/USB_CDC_DIS</td><td>80</td><td>SDIO_IO_VDD</td><td>Inout</td><td>Pullup</td><td>
<table>
<tr><th>Host</th><th>Default</th><th>Sleep</th></tr>
<tr><td>SDIO</td><td>SDIO_D3 - SDIO interface Data3 signal</td><td>HighZ</td></tr>
<tr><td>SPI</td><td>SPI_ERR_INTR - SPI Bus Error Interrupt Signals</td><td>HighZ</td></tr>
<tr><td>USB</td><td>USB_CDC_DIS - USB-CDC Active-High Disable Signal</td><td>HighZ</td></tr>
<tr><td>Non SDIO,SPI</td><td>HighZ</td><td>HighZ</td></tr>
</table>
The SPI interface is supported only in WiSeConnect™.
</td></tr>
<tr><td>GPIO_48</td><td>12</td><td>VIN_3P3</td><td>Inout</td><td>HighZ</td><td>Default : HighZ
Sleep: HighZ</td></tr>
<tr><td>GPIO_49</td><td>11</td><td>VIN_3P3</td><td>Inout</td><td>HighZ</td><td>Default : HighZ
Sleep: HighZ</td></tr>
</table>

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
GPIO_50	13	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ
GPIO_51	76	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ
ULP_GPIO_0	84	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • WLAN_ACTIVE* : Active-High signal to indicate to an external Bluetooth IC that WLAN transmission is active. Part of the 3-wire coexistence interface. *This pin is intended to act as WLAN_ACTIVE for wireless coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions.
ULP_GPIO_1	65	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • BT_ACTIVE* : Active-High signal from an external Bluetooth IC that it is transmitting. Part of the 3-wire coexistence interface. *This pin is intended to act as BT_ACTIVE for Bluetooth coexistence. It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
ULP_GPIO_4	75	VIN_3P3	Inout	HighZ	**Default :** HighZ
ULP_GPIO_5	22	VIN_3P3	Inout	HighZ	**Default :** LP_WAKEUP_IN This is LP Powersave Wakeup indication from Device **Sleep**: HighZ This pin can be configured by software to be any of the following • LP_WAKEUP_IN : This is LP Powersave Wakeup indication to Device from HOST • HOST_WAKEUP_INDICATION : This is used as an indication from Host to the dev that host is ready to take the packet and Device can transfer the packet to host. This is supported only in UART host mode. The UART interface is supported only in WiSeConnect™.
ULP_GPIO_6	82	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • WAKEUP_FROM_Dev* - Used as a wakeup indication to host from device • BT_PRIORITY** : Active-high signal from an external Bluetooth IC that indicates that the Bluetooth transmissions are a higher priority. *For Wake-on-Wireless feature this pin needs to have a weak pull up resistor externally. **This pin is intended to act as BT_PRIORITY for Bluetooth coexistence.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					It is however not available in the current firmware. Please contact Silicon Labs to learn about availability in the future versions.
ULP_GPIO_7	64	VIN_3P3	Inout	HighZ	**Default :** HighZ
ULP_GPIO_8	28	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • LED0: Control signal to an external LED. • (* LED0 functionality currently not available in WiSeConnect™ modules)
UART2_TX	93	VIN_3P3	Inout	HighZ	**Default :** UART2_TX- Debug UART Interface serial output **Sleep**: HighZ UART2_TX : Debug UART interface serial output.
ULP_GPIO_10	10	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2C_SCL: I2C interface clock.
ULP_GPIO_11	21	VIN_3P3	Inout	HighZ	**Default :** HighZ **Sleep**: HighZ This pin can be configured by software to be any of the following • I2C_SDA: I2C interface data.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
UULP_VBAT_GPIO_0	94	UULP_VBATT_1	Output	High	**Default :** EXT_PG_EN **Sleep**: SLEEP_IND_FROM_DEV / EXT_PG_EN This pin can be configured by software to be any of the following • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode. • EXT_PG_EN: Active-high enable signal to an external power gate which can be used to control the power supplies other than Always-ON VBATT Power Supplies in ULP Sleep mode.
HOST_BYP_ULP_WAKEUP	3, 29, 73	UULP_VBATT_1	Input	HighZ	**Default :** HOST_BYP **Sleep**: ULP_WAKEUP This signal has two functionalities – one during the bootloading process and one after the bootloading. During bootloading, this signal is an active-high input to indicate that the bootloader should bypass any inputs from the Host processor and continue to load the default firmware from Flash. After bootloading, this signal is an active-high input to indicate that the module should wakeup from it's Ultra Low Power (ULP) sleep mode. The bootloader bypass functionality is supported only in WiSeConnect™.
UULP_VBAT_GPIO_3	68, 81	UULP_VBATT_1	Inout	HighZ	**Default :** HighZ **Sleep**: XTAL_32KHZ_IN / SLEEP_IND_FROM_DEV

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
					This pin can be configured by software to be any of the following • XTAL_32KHZ_IN: This pin can be used to feed external clock from a host processor or from external crystal oscillator. • SLEEP_IND_FROM_DEV: This signal is used to send an indication to the Host processor. An indication is sent when the chip enters (logic low) and exits (logic high) the ULP Sleep mode.
JP0	69	VIN_3P3	Input	Pullup	**Default :** JP0 **Sleep**: HighZ JP0 - Reserved. Connect to a test point for debugging purposes.
JP1	70	VIN_3P3	Input	Pullup	**Default :** JP1 **Sleep**: HighZ JP1 - Reserved. Connect to a test point for debugging purposes.
JP2	96	VIN_3P3	Input	Pullup	**Default :** JP2 **Sleep**: HighZ JP2 - Reserved. Connect to a test point for debugging purposes.
JNC	97	VIN_3P3	NC	Pullup	**Default :** JNC **Sleep**: HighZ JNC - Reserved. Connect to a test point for debugging purposes.
USB_DP	18	USB_AVDD_3P3	Inout	NA	Positive data channel from the USB connector.

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description [1,2,3,4]
USB_DM	17	USB_AVDD_3P3	Inout	NA	Negative data channel from the USB connector.
USB_ID	19	USB_AVDD_3P3	Input	NA	ID signal from the USB connector.
USB_VBUS	16	USB_AVDD_3P3	Input	NA	5V USB VBUS signal from the USB connector

Table 3 Host and Peripheral Interfaces

1. **"Default"** state refers to the state of the device after initial boot loading and firmware loading is complete.
2. **"Sleep"** state refers to the state of the device after entering Sleep state which is indicated by Active-High "SLEEP_IND_FROM_DEV" signal.
3. Please refer to **"RS9116 nLink Technical Reference Manual"** for software programming information in hosted mode.
4. Please refer to **"RS9116 Wireless SAPI Manual"** for software programming information in embedded mode.
5. There are some functionalities, such as SLEEP_IND_FROM_DEV, that are available on multiple pins. However, these pins have other multiplexed functionalities. Any pin can be used based on the required functionality. Customer has to note the default states before using appropriate pin.

2.2.4 Miscellaneous Pins

Pin Name	Pin Number	I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
NC	2, 4, 5, 15, 23, 31, 39, 40, 41, 46, 50, 54, 55, 56, 58, 60, 61, 62, 66, 72, 89, 91, 92, 99	NA	NA	NA	No connect.

Table 4 Miscellaneous Pins

3 RS9116 AA0 module Specifications

3.1 Absolute Maximum Ratings

Functional operation above maximum ratings is not guaranteed and may damage the device.

Symbol	Parameter	Min	Max	Units
T_{store}	Storage temperature	-40	+125	°C
$T_{j(max)}$	Maximum junction temperature	-	+125	°C
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	-0.5	3.63	V
VIN_3P3	3.3V Digital Power Supply.	-0.6	3.63	V
VINBCKDC	Power supply for the on-chip Buck	-0.6	3.63	V
SDIO_IO_VDD	I/O supplies for SDIO I/Os	-0.5	3.63	V
PA2G_AVDD	Power supply for the 2.4 GHz RF Power Amplifier	-0.5	3.63	V
AVDD_1P9_3P3	Power supply for the 5 GHz RF	-0.5	3.63	V
USB_AVDD_3P3	Power supply for the USB interface	-0.5	3.63	V
USB_AVDD_1P1	Power supply for the USB core	-0.5	1.26	V
ESD_{HBM}	Electrostatic discharge tolerance (HBM) - all I/Os except RF pins Electrostatic discharge tolerance (HBM) - RF pins Compliant with JEDEC specification JS-001-2017	-	2000 100	V V
ESD_{CDM}	Electrostatic discharge tolerance (CDM) - all I/Os except RF pins Compliant with JEDEC specification JS-002-2014	-	500	V
LU	Latchup Immunity ICE criteria at ambient temp of 25°C Compliant with JESD78D	-50	100	mA
I_{max}	Maximum Current consumption in TX mode	-	400	mA
P_{max}	RF Power Level Input to the chip on pins RF pins	-	10	dBm
I_{Pmax}	Peak current rating for power supply	-	500	mA

Table 5 Absolute Maximum Ratings

3.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Max Current (A)
$T_{ambient}$	Ambient temperature	-40	25	85	°C	NA
UULP_VBATT_1	Always-on VBATT supply to the UULP Domains	1.8	3.3	3.63	V	
VIN_3P3	Always-on VBATT Power supply to the RF	1.8	3.3	3.63	V	
VINBCKDC	Always-on VBATT Power supply to the RF	1.8	3.3	3.63	V	
SDIO_IO_VDD	I/O supply for GPIOs	1.8	3.3	3.63	V	
PA2G_AVDD	I/O supply for GPIOs	1.8	3.3	3.63	V	
AVDD_1P9_3P3	Power supply for the 5 GHz RF	1.8	3.3	3.6	V	
USB_AVDD_3P3	Power supply for the USB interface	3.0	3.3	3.63	V	
USB_AVDD_1P1	Power supply for the USB core	0.99	1.1	1.21	V	

Table 6 Recommended Operating Conditions

3.3 DC Characteristics

3.3.1 Reset Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @3.3V	0.8 * VDD	-	3.63	V
	High level input voltage @1.8V	1.17	-	2.1	V
V_{IL}	Low level input voltage @3.3V	-0.5	-	0.3 * VDD	V
	Low level input voltage @1.8V	-0.3	-	0.63	V
V_{hys}	Hysteresis voltage	0.05 * VDD	-	-	V

Table 7 Reset Pin

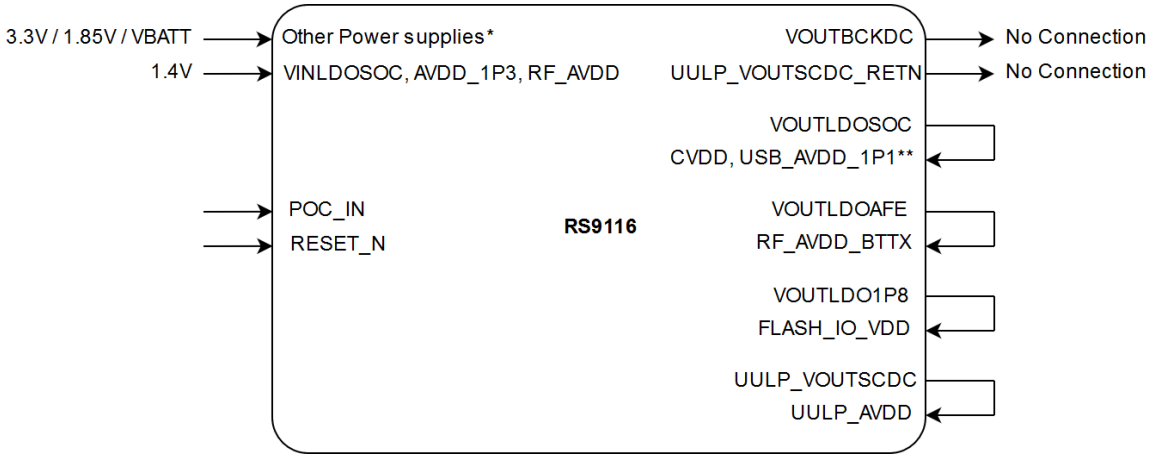
3.3.2 Power Sequence

The POC_IN and RESET_N signals should be controlled from external sources such as R/C circuits, and/or other MCU's GPIOs. However POC_OUT can be connected to POC_IN, if the supply voltage is 3.3V. Below waveforms show power sequence (Up & Down) requirements under various application needs. Note that below waveforms are not to scale.

3.3.2.1 Power-Up and Down Sequence with External 1.4V supply and POC_IN

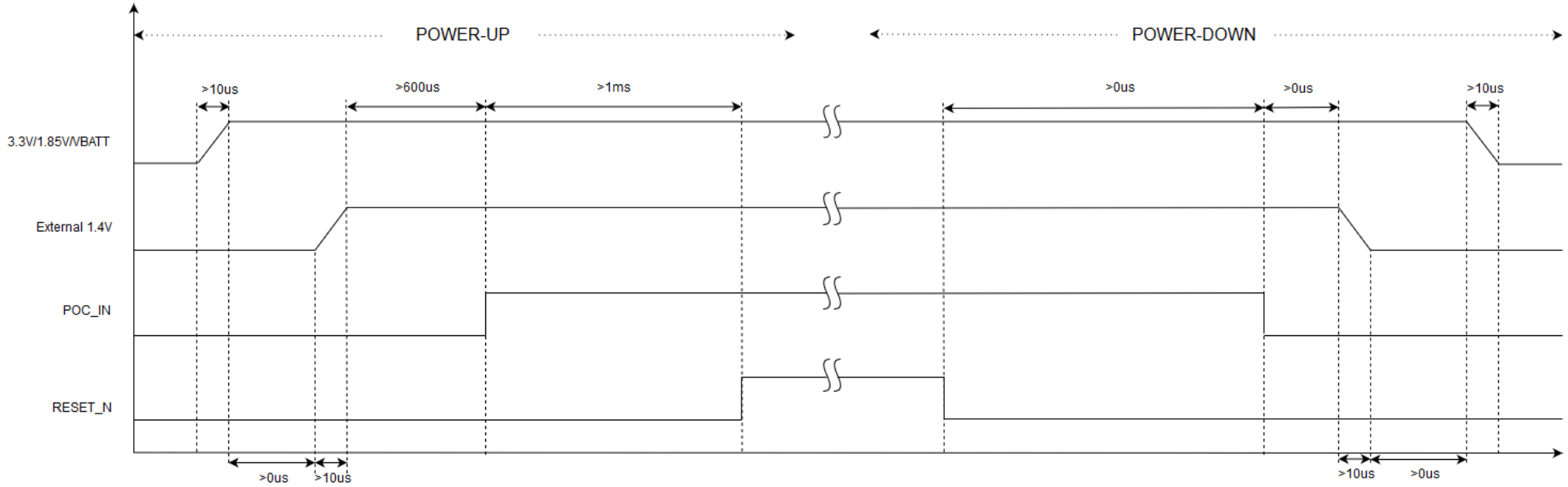
Below diagram shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when:

- System PMU (outside RS9116) can provide 1.4V supply, and hence the internal Buck regulator in RS9116 can be disabled.
- The 1.1V supply is still derived from LDO SoC (internal to RS9116).
- POC_IN is controlled externally.



NOTE:

1. Above shown is a typical connection diagram. Some of the supply pins shown above may or may not be present in the IC/Module. Check the Pinout table in this datasheet and connect accordingly.
2. * = Provide the supply voltages as per the specifications mentioned in this datasheet.
3. ** = USB power supply input connection is required if USB interface is present and used. Else, follow the connection as shown in Reference Schematics.



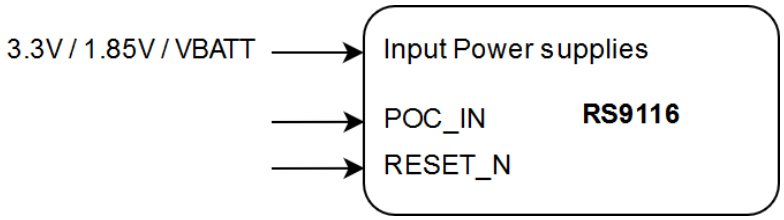
NOTE:

1. 3.3V/1.85V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.
2. Above POC_IN waveform is applicable if it is externally driven. Else, that particular waveform can be ignored, and the RESET_N timing can be considered after/before external power supplies ramp-up/down.

3.3.2.2 Power-Up and Down Sequence with External POC_IN

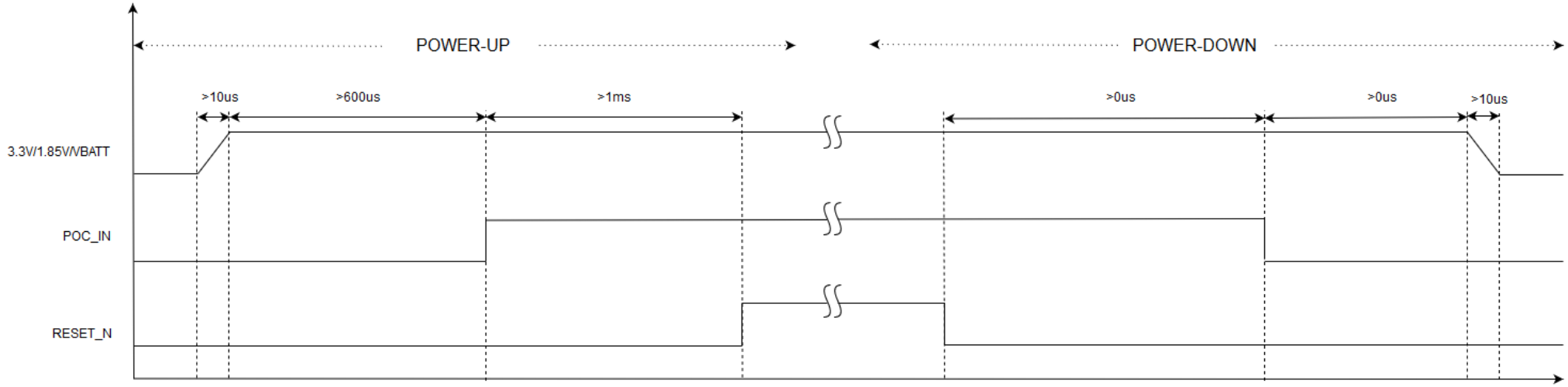
Below diagram shows connections of various power supply voltages, POC_IN and RESET_N. These connections can be used when:

- System PMU cannot provide 1.4V or 1.1V supplies and the internal buck and LDO of RS9116 are used.
- POC_IN is controlled externally.



NOTE:

1. Above shown is a typical connection diagram. Check the Reference Schematics for connections of other power supplies.



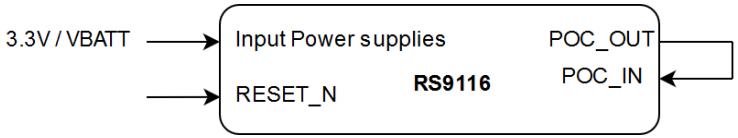
NOTE:

1. 3.3V/1.85V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.

3.3.2.3 Power-Up and Down Sequence with POC_IN connected internally

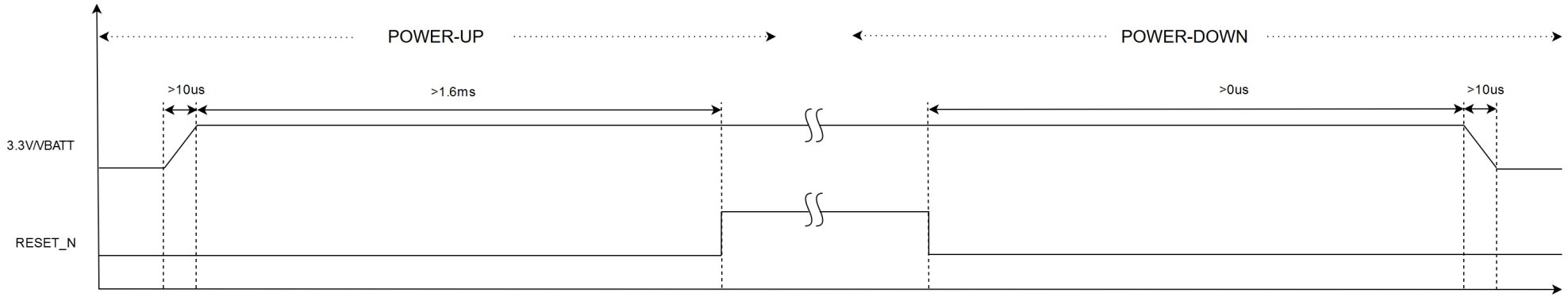
Below diagram shows connections of various power supply voltages, POC_IN and RESET_N. The typical applications of this connection can be as followws.

- System cannot provide external 1.4V & 1.1V supplies and the internal buck and LDO of RS9116 are used.
- POC_IN is looped back from POC_OUT.



NOTE:

1. Above shown is a typical connection diagram. Check the Reference Schematics for connections of other power supplies.
2. POC_OUT can be connected to POC_IN if the supply voltage is 3.3V only. Else, POC_IN has to be driven externally.



NOTE:

1. 3.3V/VBATT supply shown above must be connected to the power supply pins of IC/Module. For example, SDIO_IO_VDD, ULP_IO_VDD, UULP_VBATT_1, etc.

3.3.3 Digital Input Output Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage @3.3V	2.0	-	3.63	V
	High level input voltage @1.8V	1.17	-	2.1	V
V_{IL}	Low level input voltage @3.3V	-0.3	-	0.8	V
	Low level input voltage @1.8V	-0.3	-	0.63	V
V_{hys}	Hysteresis voltage	0.1 VDD	-	-	V
V_{OL}	Low level output voltage	-	-	0.4	V
V_{OH}	High level output voltage	VDD-0.4	-	-	V
I_{OL}	Low level output current (programmable)	2.0	4.0	12.0	mA
I_{OH}	High level output current (programmable)	2.0	4.0	12.0	mA

Table 8 Digital I/O Signals

3.3.4 USB

Parameter	Conditions	Min.	Typ.	Max.	Units
Vcm DC (DC level measured at receiver connector)	HS Mode LS/FS Mode	-0.05 0.8	-	0.5 2.5	V
Crossover Voltages	LS Mode FS Mode	1.3 1.3	-	2 2	V
Power supply ripple noise (Analog 3.3V)	< 160 MHz	-50	-	50	mV

Table 9 USB

3.3.5 Pin Capacitances

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_{io}	Input/output capacitance, digital pins only	-	-	2.0	pF

Table 10 Pin Capacitances

3.4 AC Characteristics

3.4.1 Clock Specifications

RS9116 chipsets require two primary clocks:

- Low frequency 32 KHz clock for sleep manager and RTC
    - Internal 32 KHz RC clock is used for applications with low timing accuracy requirements
    - 32 KHz crystal clock is used for applications with low timing accuracy requirements
- High frequency 40 MHz clock for the threadArch® processor, baseband subsystem and the radio

The chipsets have integrated internal oscillators including crystal oscillators to generate the required clocks. Integrated crystal oscillators enable the use of low-cost passive crystal components. Additionally, in a system where an external clock source is already present, the clock can be reused. The following are the recommended options for the clocks for different functionalities:

Functionality	Default Clock option	Other Clock option	Comments
Wi-Fi or Wi-Fi + BLE Connectivity	Internal 32KHz RC oscillator calibrated to <200ppm	32KHz XTAL oscillator input on UULPGPIO.	32KHz XTAL Oscillator clock is optional. No significant power consumption impact on connected power numbers (<10uA).
Wi-Fi + BT or Wi-Fi + BT + BLE Connectivity with low power Audio Streaming operation (A2DP Source)	32KHz XTAL oscillator input on UULPGPIO	Internal 32KHz RC oscillator calibrated to <200ppm	32KHz XTAL Oscillator clock is important for Low-power Audio Streaming operation (A2DP Source).

There is no impact on sleep/deep-sleep power consumption with/without 32KHz XTAL oscillator clock

32KHz XTAL sources:

Option 1: From Host MCU/MPU LVCMOS rail to rail clock input on UULPGPIO

Option 2: External Xtal oscillator providing LVCMOS rail to rail clock input on UULPGPIO (Nano-drive clock should not be supplied).

3.4.1.1 32 KHz Clock

The 32 KHz clock selection can be done through software. RC oscillator clock is not suited for high timing accuracy applications and can increase system current consumption in duty-cycled power modes.

3.4.1.1.1 RC Oscillator

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.0		KHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage		1.2		%
Jitter	RMS value of Edge jitter (TIE)		91		ns
Peak Period Jitter	Peak value of Cycle Jitter with 6σ variation		789		ns

Table 11 32 KHz RC oscillator

3.4.1.1.2 32 KHz External Oscillator

An external 32 KHz low-frequency clock can be fed through the XTAL_32KHZ_IN functionality.

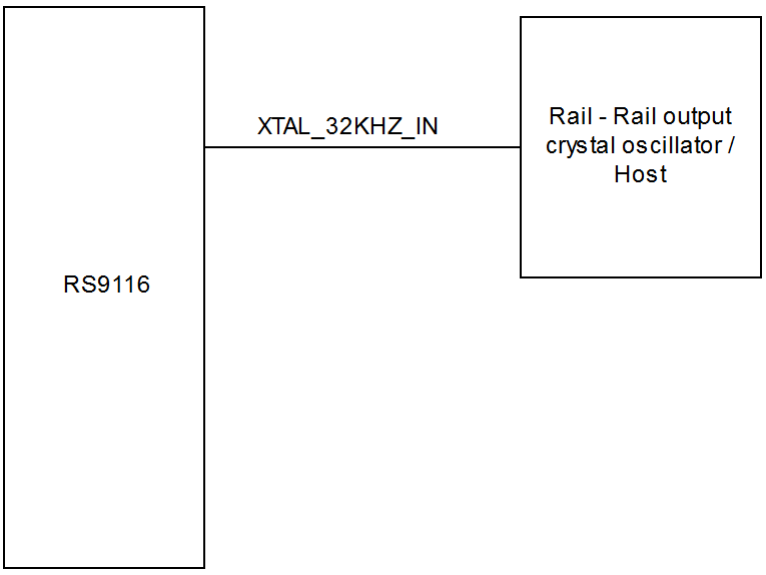


Figure 6 External 32 KHz oscillator - Rail to Rail

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		32.768		KHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-100		100	ppm
Duty cycle	Input duty cycle	30	50	70	%
V_{AC}	Input AC peak-peak voltage swing at input pin.	0.3	-	VBATT-0.3	Vpp

Table 12 32 KHz external oscillator specifications

3.4.1.2 40 MHz Clock

Load capacitance with 40 MHz internal oscillator is integrated inside the chipset and calibrated. The calibrated value can be stored in eFuse using calibration software. The module provides the below characteristics.

Parameter	Parameter Description	Min	Typ	Max	Units
F_{osc}	Oscillator Frequency		40		MHz
F_{osc_Acc}	Frequency Variation with Temp and Voltage	-20		20	ppm
ESR	Equivalent series resistance			60	Ω
Load cap	Load capacitance range	5		10	pF

Table 13 40 MHz crystal specifications

3.4.2 SDIO 2.0 Slave

3.4.2.1 Full Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sdio}	SDIO_CLK	-	-	25	MHz
T_s	SDIO_DATA, input setup time	4	-	-	ns
T_h	SDIO_DATA, input hold time	1	-	-	ns
T_{od}	SDIO_DATA, clock to output delay	-	-	13	ns
C_L	Output Load	5	-	10	pF

Table 14 AC Characteristics - SDIO 2.0 Slave Full Speed Mode

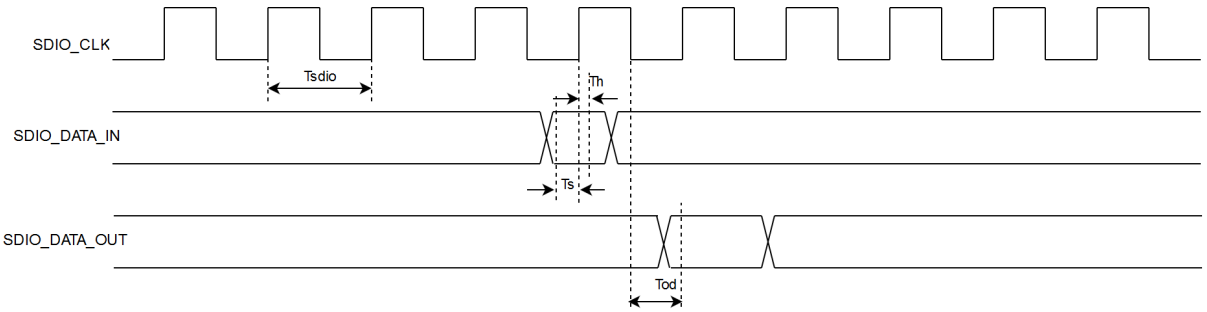


Figure 7 Interface Timing Diagram for SDIO 2.0 Slave Full Speed Mode

3.4.2.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{sdio}	SDIO_CLK	25	-	50	MHz
T_s	SDIO_DATA, input setup time	4	-	-	ns
T_h	SDIO_DATA, input hold time	1	-	-	ns
T_{od}	SDIO_DATA, clock to output delay	2.5	-	13	ns
C_L	Output Load	5	-	10	pF

Table 15 AC Characteristics - SDIO 2.0 Slave High Speed Mode

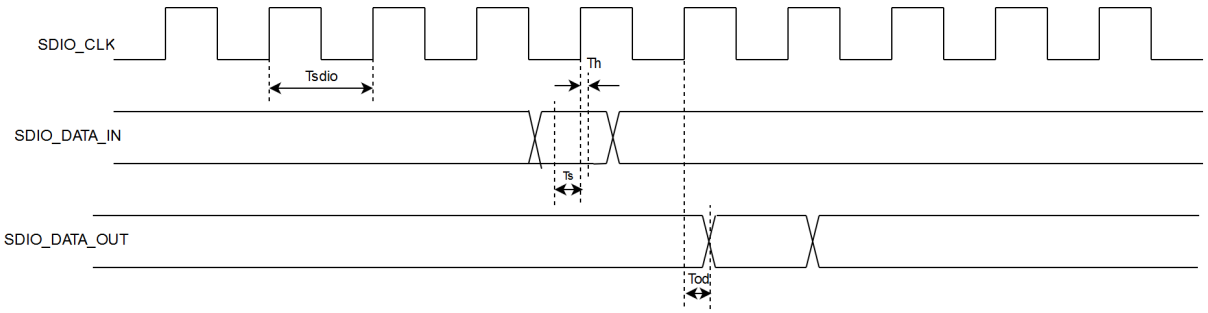


Figure 8 Interface Timing Diagram for SDIO 2.0 Slave High Speed Mode

3.4.3 SPI Slave

3.4.3.1 Low Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	0	-	25	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	-	-	8.75	ns
C_L	Output Load	5	-	10	pF

Table 16 AC Characteristics - SPI Slave Low Speed Mode

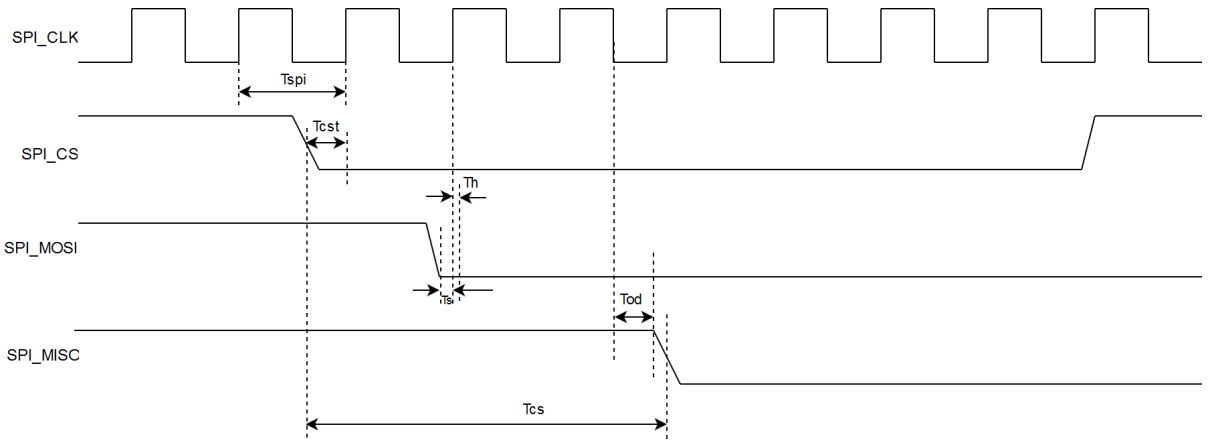


Figure 9 Interface Timing Diagram for SPI Slave Low Speed Mode

3.4.3.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	25	-	80	MHz
T_{cs}	SPI_CS to output delay	-	-	7.5	ns
T_{cst}	SPI CS to input setup time	4.5	-	-	-
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	2.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

Table 17 AC Characteristics - SPI Slave High Speed Mode

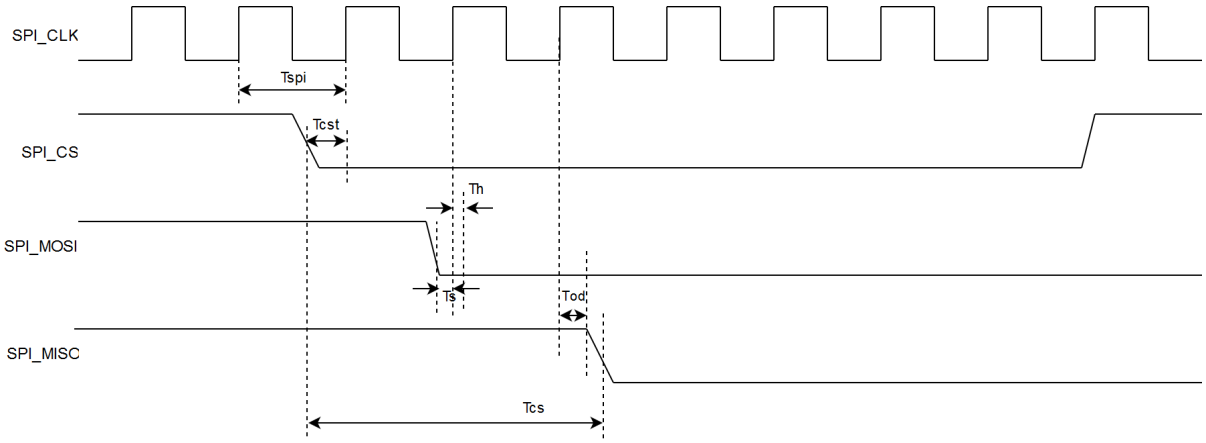


Figure 10 Interface Timing Diagram for SPI Slave High Speed Mode

3.4.3.3 Ultra High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{spi}	SPI_CLK	-	-	100	MHz
T_s	SPI_MOSI, input setup time	1.33	-	-	ns
T_h	SPI_MOSI, input hold time	1.2	-	-	ns
T_{od}	SPI_MISO, clock to output delay	1.5	-	8.75	ns
C_L	Output Load	5	-	10	pF

Table 18 AC Characteristics - SPI Slave Ultra High Speed Mode

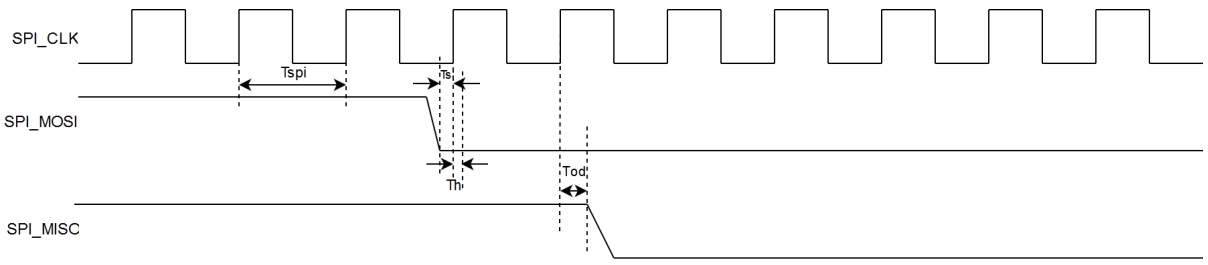


Figure 11 Interface Timing Diagram for SPI Slave Ultra High Speed Mode

3.4.4 USB

3.4.4.1 Low Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_r	Rise Time	75	-	300	ns
T_f	Fall Time	75	-	300	ns
Jitter	Jitter	-	-	10	ns

Table 19 AC Characteristics - USB Low Speed Mode

3.4.4.2 Full Speed Mode

Parameter	Parameter	Min.	Typ.	Max.	Unit
T_r	Rise Time	4	-	20	ns
T_f	Fall Time	4	-	20	ns
Jitter	Jitter	-	-	1	ns

Table 20 AC Characteristics - USB Full Speed Mode

3.4.4.3 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_r	Rise Time	0.5	-	-	ns
T_f	Fall Time	0.5	-	-	ns
Jitter	Jitter	-	-	0.1	ns

Table 21 AC Characteristics - USB High Speed Mode

3.4.5 UART

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{uart}	CLK	0	-	20	MHz
T_{od}	Output delay	0	-	10	ns
T_s	Input setup time	0	-	5	ns
C_L	Output load	5	-	25	pF

Table 22 AC Characteristics - UART

3.4.6 I2C Master and Slave

3.4.6.1 Fast Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	100	-	400	KHz
T_{low}	clock low period	1.3	-	-	us
T_{high}	clock high period	0.6	-	-	us
T_{sstart}	start condition, setup time	0.6	-	-	us
T_{hstart}	start condition, hold time	0.6	-	-	us

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_s	data, setup time	100	-	-	ns
T_{sstop}	stop condition, setup time	0.6	-	-	us
C_L	Output Load	5	-	10	pF

Table 23 AC Characteristics - I2C Fast Speed Mode

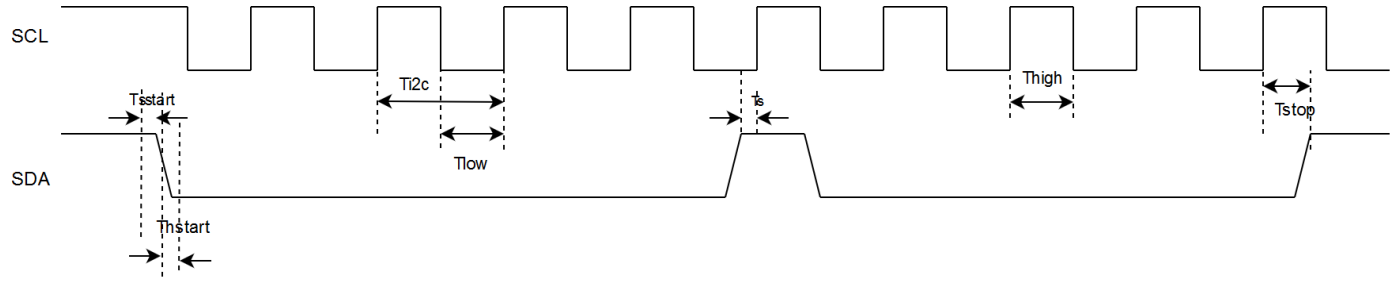


Figure 12 Interface Timing Diagram for I2C Fast Speed Mode

3.4.6.2 High Speed Mode

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2c}	SCL	0.4	-	3.4	MHz
T_{low}	clock low period	160	-	-	ns
T_{high}	clock high period	60	-	-	ns
T_{sstart}	start condition, setup time	160	-	-	ns
T_{hstart}	start condition, hold time	160	-	-	ns
T_s	data, setup time	10	-	-	ns
T_h	data, hold time	0	-	70	ns
T_{sstop}	stop condition, setup time	160	-	-	ns
C_L	Output Load	5	-	10	pF

Table 24 AC Characteristics - I2C High Speed Mode

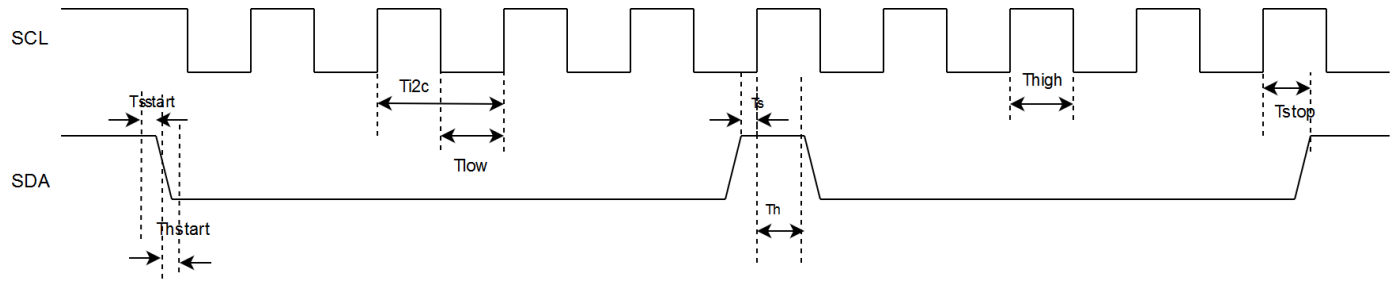


Figure 13 Interface Timing Diagram for I2C High Speed Mode

3.4.7 I2S/PCM Master and Slave

3.4.7.1 Master Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	10	-	-	ns
T_h	i2s_din,i2s_ws hold time	0	-	-	ns
T_{od}	i2s_dout output delay	0	-	12	ns
C_L	i2s_dout output load	5	-	10	pF

Table 25 AC Characteristics – I2S/PCM Master Mode

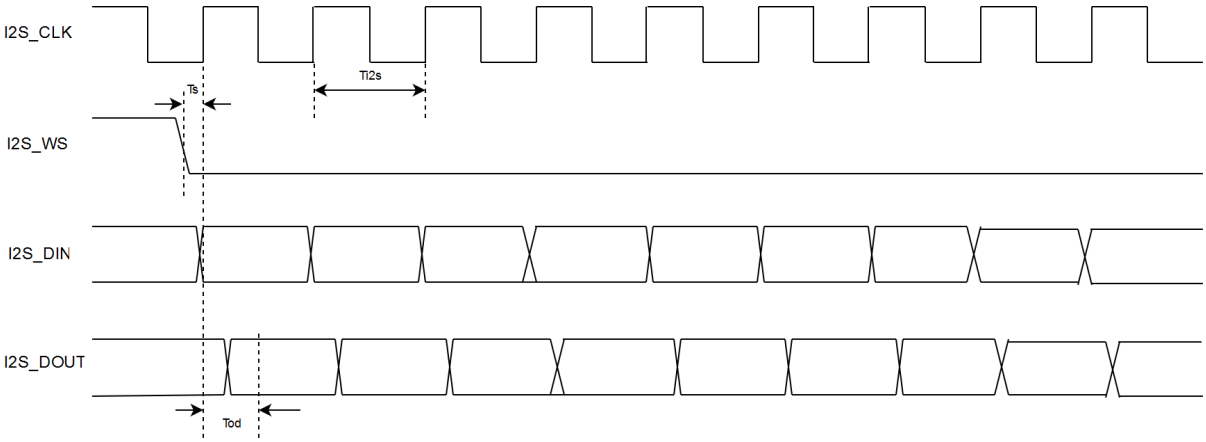


Figure 14 Interface Timing Diagram for I2S Master Mode

3.4.7.2 Slave Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Parameter	Parameter Description	Min.	Typ.	Max.	Unit
T_{i2s}	i2s_clk	0	-	25	MHz
T_s	i2s_din,i2s_ws setup time	8	-	-	ns
T_h	i2s_din,i2s_ws hold time	0	-	-	ns
T_{od}	i2s_dout output delay	0	-	17	ns
C_L	i2s_dout output load	5	-	10	pF

Table 26 AC Characteristics - I2S/PCM Slave Mode

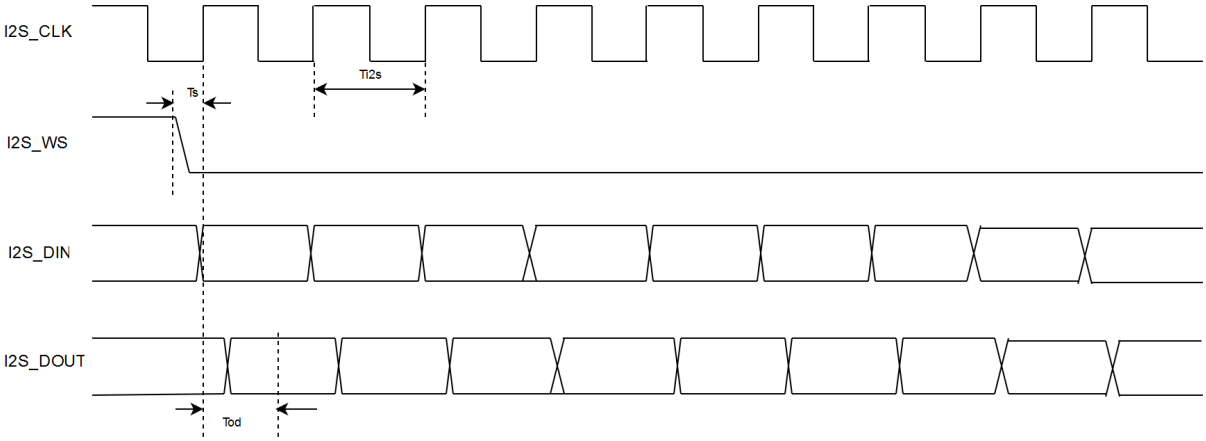


Figure 15 Interface Timing Diagram for I2S Slave Mode

3.4.8 GPIO pins

Parameter	Parameter Description	Conditions	Min.	Typ.	Max.	Unit
T_{rf}	Rise time	Pin configured as output; SLEW = 1(fast mode)	1.0	-	2.5	ns
T_{ff}	Fall time	Pin configured as output; SLEW = 1(fast mode)	0.9	-	2.5	ns
T_{rs}	Rise time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.3	ns
T_{fs}	Fall time	Pin configured as output; SLEW = 0(standard mode)	1.9	-	4.0	ns
T_r	Rise time	Pin configured as input	0.3	-	1.3	ns
T_f	Fall time	Pin configured as input	0.2	-	1.2	ns

Table 27 AC Characteristics - GPIO Pins

3.5 RF Characteristics

In the sub-sections below,

- All WLAN Sensitivity numbers and Adjacent channel numbers are at < 10% PER limit. Packet sizes are 1024 bytes for 802.11 b/g data rates and 4096 bytes for 802.11n data rates.
- For WLAN ACI cases, the desired signal power is 3dB above standard defined sensitivity level.
- For Bluetooth C/I cases, the desired signal power is 3dB above standard defined sensitivity level.
- For support of 1.85 V on RF/PA, please contact Silicon Labs.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in the Recommended Operating Conditions

3.5.1 WLAN 2.4 GHz Transmitter Characteristics

3.5.1.1 Transmitter characteristics with 3.3V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port on channel 6 (2437 MHz)(1)

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	DSSS - 1 Mbps	EVM< -9 dB	-	17.5	-	dBm
	DSSS - 2 Mbps	EVM< -9 dB	-	17.5	-	dBm
	CCK- 5.5 Mbps	EVM< -9 dB	-	17.5	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	17.5	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	17	-	dBm
	OFDM - 9 Mbps	EVM< -8 dB	-	17	-	dBm
	OFDM - 12 Mbps	EVM< -10 dB	-	17	-	dBm
	OFDM - 18 Mbps	EVM< -13 dB	-	17	-	dBm
	OFDM - 24 Mbps	EVM< -16 dB	-	17	-	dBm
	OFDM - 36 Mbps	EVM< -19 dB	-	16.5	-	dBm
	OFDM - 48 Mbps	EVM< -22 dB	-	16	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB	-	14.5	-	dBm
	MCS0 Mixed Mode	EVM< -5 dB	-	17	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	17	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	17	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	16	-	dBm
	MCS4 Mixed Mode	EVM< -19 dB	-	15	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	15	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB	-	14	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
	MCS7 Mixed Mode	EVM< -27 dB	-	9.5	-	dBm
Transmitter Emissions (6 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-148	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-158	-	dBm/Hz
	1450–1495 MHz	DAB	-	-158	-	dBm/Hz
	1570–1580 MHz	GPS	-	-148	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-122	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-130	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-110	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-123	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-134	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-132	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-127	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-120	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-116	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-95	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-103	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-114	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-130	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-148	-	dBm/Hz
Harmonic Emissions (1 Mbps @ Maximum Power)	4.8-5.0 GHz	2nd Harmonic	-	-51	-	dBm/MHz
	7.2-7.5 GHz	3rd Harmonic	-	-42	-	dBm/MHz

Table 28 WLAN 2.4 GHz Transmitter Characteristics (3.3V)

1. Up to 2dB variation in power from channel-to-channel. To meet FCC emission limits, edge channels (1 and 11) have reduced TX power.

3.5.1.2 Transmitter characteristics with 1.85V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 1.85 V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port on channel 6 (2437 MHz)(1)

Parameter	Condition	Notes	Min	Typ	Max	Units
	DSSS - 1 Mbps	EVM< -9 dB	-	14	-	dBm
	DSSS - 2 Mbps	EVM< -9 dB	-	14	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power for 20MHz Bandwidth, compliant with IEEE mask and EVM	CCK- 5.5 Mbps	EVM< -9 dB	-	14	-	dBm
	CCK - 11 Mbps	EVM< -9 dB	-	14	-	dBm
	OFDM - 6 Mbps	EVM< -5 dB	-	14	-	dBm
	OFDM - 9 Mbps	EVM< -8 dB	-	14	-	dBm
	OFDM - 12 Mbps	EVM< -10 dB	-	14	-	dBm
	OFDM - 18 Mbps	EVM< -13 dB	-	14	-	dBm
	OFDM - 24 Mbps	EVM< -16 dB	-	14	-	dBm
	OFDM - 36 Mbps	EVM< -19 dB	-	13	-	dBm
	OFDM - 48 Mbps	EVM< -22 dB	-	12	-	dBm
	OFDM - 54 Mbps	EVM< -25 dB	-	11	-	dBm
	MCS0 Mixed Mode	EVM< -5 dB	-	13	-	dBm
	MCS1 Mixed Mode	EVM< -10 dB	-	13	-	dBm
	MCS2 Mixed Mode	EVM< -13 dB	-	13	-	dBm
	MCS3 Mixed Mode	EVM< -16 dB	-	12.5	-	dBm
	MCS4 Mixed Mode	EVM< -19 dB	-	11.5	-	dBm
	MCS5 Mixed Mode	EVM< -22 dB	-	11.5	-	dBm
	MCS6 Mixed Mode	EVM< -25 dB	-	11	-	dBm
	MCS7 Mixed Mode	EVM< -27 dB	-	9	-	dBm
Transmitter Emissions (1 Mbps @ Maximum Power)	776-794 MHz	CDMA2000	-	-158	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-158	-	dBm/Hz
	1450–1495 MHz	DAB	-	-158	-	dBm/Hz
	1570–1580 MHz	GPS	-	-158	-	dBm/Hz
	1592--1610 MHz	GLONASS	-	-136	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-136	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-133	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-133	-	dBm/Hz

Parameter	Condition	Notes	Min	Typ	Max	Units
	1910–1930 MHz	TDSCDMA,LTE	-	-138	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-132	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-141	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-141	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-112	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-98	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-116	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-121	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-133	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-148	-	dBm/Hz
Harmonic Emissions (1 Mbps @ Maximum Power)	4.8-5.0 GHz	2nd Harmonic	-	-51	-	dBm/MHz
	7.2-7.5 GHz	3rd Harmonic	-	-42	-	dBm/MHz

Table 29 WLAN 2.4 GHz Transmitter Characteristics (1.85V)

1. Up to 2dB variation in power from channel-to-channel. To meet FCC emission limits, edge channels (1 and 11) have reduced TX power.

3.5.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C. Parameters are measured at antenna port on channel 1(2412 MHz)

Parameter	Condition	Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth(1)	1 Mbps DSSS		-	-96.5	-	dBm
	2 Mbps DSSS		-	-90	-	dBm
	5.5 Mbps CCK		-	-88	-	dBm
	11 Mbps CCK		-	-85	-	dBm
	6 Mbps OFDM		-	-90	-	dBm
	9 Mbps OFDM		-	-89.5	-	dBm
	12 Mbps OFDM		-	-89	-	dBm
	18 Mbps OFDM		-	-86.5	-	dBm
	24 Mbps OFDM		-	-83.5	-	dBm
	36 Mbps OFDM		-	-80	-	dBm
	48 Mbps OFDM		-	-75.5	-	dBm
	54 Mbps OFDM		-	-74	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
	MCS0 Mixed Mode		-	-89	-	dBm
	MCS1 Mixed Mode		-	-86.5	-	dBm
	MCS2 Mixed Mode		-	-85	-	dBm
	MCS3 Mixed Mode		-	-81.5	-	dBm
	MCS4 Mixed Mode		-	-77.5	-	dBm
	MCS5 Mixed Mode		-	-73	-	dBm
	MCS6 Mixed Mode		-	-71	-	dBm
	MCS7 Mixed Mode		-	-70	-	dBm
Maximum Input Level for PER below 10%	802.11 b		-	5	-	dBm
	802.11g		-	-9	-	dBm
	802.11n		-	-11	-	dBm
RSSI Accuracy Range			-3	-	3	dB
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz		-	-3	-	dBm
	824–849 MHz		-	-3	-	dBm
	880–915 MHz		-	-3	-	dBm
	1710–1785 MHz		-	-17	-	dBm
	1850–1910 MHz		-	-18	-	dBm
	1920–1980 MHz		-	-18	-	dBm
	2300–2400 MHz		-	-58	-	dBm
	2570–2620 MHz		-	-21	-	dBm
	2545–2575 MHz		-	-20	-	dBm
Return Loss			-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS		-	36	-	dB
	11 Mbps DSSS		-	37	-	dB
	6 Mbps OFDM		-	38	-	dB
	54 Mbps OFDM		-	22	-	dB
	MCS0 Mixed Mode		-	38	-	dB
	MCS7 Mixed Mode		-	20	-	dB
	1 Mbps DSSS		-	44	-	dB

Parameter	Condition	Notes	Min	Typ	Max	Units
Alternate Adjacent Channel Interference	11 Mbps DSSS		-	35	-	dB
	6 Mbps OFDM		-	46	-	dB
	54 Mbps OFDM		-	30	-	dB
	MCS0 Mixed Mode		-	46	-	dB
	MCS7 Mixed Mode		-	28	-	dB

Table 30 WLAN 2.4 GHz Receiver Characteristics on HP RF Chain

1. Sensitivities for channels 6,7,8 & 11 are up to 2dB worse

3.5.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C. Parameters are measured at antenna port on channel 1(2412 MHz)

Parameter	Condition	Notes	Min	Typ	Max	Units
Sensitivity for 20MHz Bandwidth(1)	1 Mbps DSSS		-	-94.5	-	dBm
	2 Mbps DSSS		-	-89	-	dBm
	5.5 Mbps CCK		-	-87	-	dBm
	11 Mbps CCK		-	-84	-	dBm
	6 Mbps OFDM		-	-88	-	dBm
	9 Mbps OFDM		-	-87.5	-	dBm
	12 Mbps OFDM		-	-87	-	dBm
	18 Mbps OFDM		-	-84.5	-	dBm
	24 Mbps OFDM		-	-81.5	-	dBm
	36 Mbps OFDM		-	-77.5	-	dBm
	MCS0 Mixed Mode		-	-87	-	dBm
	MCS1 Mixed Mode		-	-84.5	-	dBm
	MCS2 Mixed Mode		-	-82	-	dBm
	MCS3 Mixed Mode		-	-79.5	-	dBm
	MCS4 Mixed Mode		-	-75	-	dBm
Maximum Input Level for PER below 10%	802.11 b		-	-12	-	dBm
	802.11g		-	-15	-	dBm

Parameter	Condition	Notes	Min	Typ	Max	Units
	802.11n		-	-15	-	dBm
RSSI Accuracy Range			-3	-	3	dB
Blocking level for 3 dB RX Sensitivity Degradation(Data rate 6Mbps OFDM, Desired signal at -79dBm)	776–794 MHz		-	-3.5	-	dBm
	824–849 MHz		-	-3.5	-	dBm
	880–915 MHz		-	-3.5	-	dBm
	1710–1785 MHz		-	-19	-	dBm
	1850–1910 MHz		-	-18	-	dBm
	1920–1980 MHz		-	-23	-	dBm
	2300–2400 MHz		-	-60	-	dBm
	2570–2620 MHz		-	-22	-	dBm
	2545–2575 MHz		-	-21	-	dBm
Return Loss			-10	-	-	dB
Adjacent Channel Interference	1 Mbps DSSS		-	40	-	dB
	11 Mbps DSSS		-	36	-	dB
	6 Mbps OFDM		-	42	-	dB
	36 Mbps OFDM		-	30	-	dB
	MCS0 Mixed Mode		-	40	-	dB
	MCS4 Mixed Mode		-	30	-	dB
Alternate Adjacent Channel Interference	1 Mbps DSSS		-	50	-	dB
	11 Mbps DSSS		-	38	-	dB
	6 Mbps OFDM		-	48	-	dB
	36 Mbps OFDM		-	38	-	dB
	MCS0 Mixed Mode		-	48	-	dB
	MCS4 Mixed Mode		-	36	-	dB

Table 31 WLAN 2.4 GHz Receiver Characteristics on LP RF Chain

1. Sensitivities for channels 6,7,8 & 11 are up to 2dB worse.

3.5.4 Bluetooth Transmitter Characteristics on High-Performance (HP) RF Chain

3.5.4.1 Transmitter characteristics with 3.3 V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are measured at antenna port.(1)

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power	BR		-	12	-	dBm
	EDR 2Mbps		-	12	-	dBm
	EDR 3Mbps		-	10.5	-	dBm
	LE 1Mbps		-	16.5	-	dBm
	LE 2Mbps		-	16	-	dBm
	LR 500 Kbps		-	16	-	dBm
	LR 125 Kbps		-	16	-	dBm
Power Control Step	BR, EDR		-	3	-	dB
Adjacent Channel Power |M-N| = 2	BR		-	-	-20	dBm
	EDR		-	-	-20	dBm
	LE		-	-	-20	dBm
	LR		-	-	-20	dBm
Adjacent Channel Power |M-N| > 2	BR		-	-	-40	dBm
	EDR		-	-	-40	dBm
	LE		-	-	-30	dBm
	LR		-	-	-30	dBm
BR Modulation Characteristics	DH1		-25	-	25	kHz
	DH3		-40	-	40	kHz
	DH5		-40	-	40	kHz
	Drift Rate		-20	-	20	kHz/50 us
	Δf1 Avg		140	-	175	kHz
	Δf2 Max		115	-	-	kHz
EDR Modulation Characteristics	RMS DEVM, EDR2		-	15	-	%
	RMS DEVM, EDR3		-	5.5	-	%
	99% DEVM, EDR2		-	23	-	%
	99% DEVM, EDR3		-	9.5	-	%
	peak DEVM,EDR2		-	28	-	%

Parameter	Condition	Notes	Min	Typ	Max	Units
	peak DEVM,EDR3		-	13.5	-	%
BLE Modulation Characteristics	Δf1 Avg		225	-	275	kHz
	Δf2 Max		185	-	-	kHz
	Δf2 Avg/Δf1 Avg		0.8	-	-	-
Transmitter Emissions (BR @Maximum output power)	776-794 MHz	CDMA2000	-	-160	-	dBm/Hz
	869–960 MHz	CDMAOne, GSM850	-	-160	-	dBm/Hz
	1450–1495 MHz	DAB	-	-160	-	dBm/Hz
	1570–1580 MHz	GPS	-	-160	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-160(2)	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-115	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-148	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-148	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-136	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-148	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-148	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-116	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-142	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-134	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-128	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-139	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-139	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-148	-	dBm/Hz

Table 32 Bluetooth Transmitter Characteristics on HP RF Chain 3.3V

1. Up to 2dB variation in power from channel-to-channel.
2. Noise-floor is -160dBm/Hz with spurious tone power of -68dBm at 1601.33 MHz when transmitted signal is at 2402 MHz

3.5.4.2 Transmitter characteristics with 1.85 V Supply

TA = 25°C, PA2G_AVDD/VINBCKDC = 1.85 V. Remaining supplies are at typical operating conditions.Parameters are measured at antenna port.(1)

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmit Power	BR		-	11	-	dBm
	EDR 2Mbps		-	11	-	dBm
	EDR 3Mbps		-	11	-	dBm
	LE 1Mbps		-	13	-	dBm
	LE 2Mbps		-	13	-	dBm
	LR 500 Kbps		-	13	-	dBm
	LR 125 Kbps		-	13	-	dBm
Power Control Step	BR, EDR		-	3	-	dB
Adjacent Channel Power |M-N| = 2	BR		-	-	-20	dBm
	EDR		-	-	-20	dBm
	LE		-	-	-20	dBm
	LR		-	-	-20	dBm
Adjacent Channel Power |M-N| > 2	BR		-	-	-40	dBm
	EDR		-	-	-40	dBm
	LE		-	-	-30	dBm
	LR		-	-	-30	dBm
BR Modulation Characteristics	DH1		-25	-	25	kHz
	DH3		-40	-	40	kHz
	DH5		-40	-	40	kHz
	Drift Rate		-20	-	20	kHz/50 us
	Δf1 Avg		140	-	175	kHz
	Δf2 Max		115	-		kHz
EDR Modulation Characteristics	RMS DEVM, EDR2		-	6.5	-	%
	RMS DEVM, EDR3		-	5.5	-	%
	99% DEVM, EDR2		-	11.5	-	%
	99% DEVM, EDR3		-	10.5	-	%
	peak DEVM,EDR2		-	20	-	%
	peak DEVM,EDR3		-	14.5	-	%
BLE Modulation Characteristics	Δf1 Avg		225	-	275	kHz
	Δf2 Max		185	-	-	kHz
	Δf2 Avg/Δf1 Avg		0.8	-	-	-
	776-794 MHz	CDMA2000	-	-160	-	dBm/Hz

Parameter	Condition	Notes	Min	Typ	Max	Units
Transmitter Emissions (BR @Maximum output power)	869–960 MHz	CDMAOne, GSM850	-	-160	-	dBm/Hz
	1450–1495 MHz	DAB	-	-160	-	dBm/Hz
	1570–1580 MHz	GPS	-	-160	-	dBm/Hz
	1592–1610 MHz	GLONASS	-	-160(2)	-	dBm/Hz
	1710–1800 MHz	DSC-1800-Uplink	-	-115	-	dBm/Hz
	1805–1880 MHz	GSM 1800	-	-148	-	dBm/Hz
	1850–1910 MHz	GSM 1900	-	-148	-	dBm/Hz
	1910–1930 MHz	TDSCDMA,LTE	-	-135	-	dBm/Hz
	1930–1990 MHz	GSM1900, CDMAOne,WCDMA	-	-101	-	dBm/Hz
	2010–2075 MHz	TDSCDMA	-	-148	-	dBm/Hz
	2110–2170 MHz	WCDMA	-	-115	-	dBm/Hz
	2305–2370 MHz	LTE Band 40	-	-140	-	dBm/Hz
	2370–2400 MHz	LTE Band 40	-	-134	-	dBm/Hz
	2496–2530 MHz	LTE Band 41	-	-125	-	dBm/Hz
	2530–2560 MHz	LTE Band 41	-	-138	-	dBm/Hz
	2570–2690 MHz	LTE Band 41	-	-138	-	dBm/Hz
	5000–5900 MHz	WLAN 5G	-	-148	-	dBm/Hz

Table 33 Bluetooth Transmitter Characteristics on HP RF Chain 1.85V

1. Up to 2dB variation in power from channel-to-channel.
2. Noise-floor is -160dBm/Hz with spurious tone power of -70dBm at 1601.33 MHz when transmitted signal is at 2402 MHz

3.5.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Chain

TA = 25°C. Parameters are measured at antenna port and applicable to both PA2G_AVDD/VINBCKDC=1.85V and PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Transmit Power	BR	-	-	-4.5	dBm
	LE 1Mbps	-	-	-4.5	dBm
	LE 2Mbps	-	-	-4.5	dBm
	LR 500 Kbps	-	-	-4.5	dBm
	LR 125 kbps	-	-	-4.5	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
Adjacent Channel Power |M-N| = 2	BR	-	-	-20	dBm
	LE	-	-	-20	dBm
	LR	-	-	-20	dBm
Adjacent Channel Power |M-N| > 2	BR	-	-	-40	dBm
	LE	-	-	-30	dBm
	LR	-	-	-30	dBm
BR Modulation Characteristics	DH1	-25	-	25	kHz
	DH3	-40	-	40	kHz
	DH5	-40	-	40	kHz
	Drift Rate	-20	-	20	kHz
	Δf1 Avg	140	-	175	kHz
	Δf2 Max	115	-	-	kHz
BLE Modulation Characteristics	Δf1 Avg	225	-	275	kHz
	Δf2 Max	185	-	-	kHz
	Δf2 Avg/Δf1 Avg	0.8	-	-	-

Table 34 Bluetooth Transmitter Characteristics on LP 0 dBm RF Chain

3.5.6 Bluetooth Receiver Characteristics on High-Performance (HP) RF Chain

TA = 25°C. Parameters are measured at antenna port and applicable to both PA2G_AVDD/VINBCKDC=1.85V and PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1],[2]	BR (1 Mbps), 339 bytes, DH5 Packet, BER= 0.1%	-	-91	-	dBm
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-92.5	-	dBm
	EDR3 (3 Mbps), 1020 bytes, 3-DH5 Packet, BER= 0.01%	-	-85.5	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-91.5	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-90	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-99	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-103.5	-	dBm
Maximum Input Level	BR, EDR2, EDR3,BER= 0.1%	-	-13	-	dBm
	LE 1Mbps, 2Mbps,PER=30.8%	-	10	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
	LR 500kps, 125kbps,PER=30.8%	-	10	-	dBm
C/I Performance	BR, co-channel, BER=0.1%	9	-	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-2	-	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-19	-	-	dB
	BR, adjacent >=|±3| MHz BER=0.1%	-19	-	-	dB
	BR, Image channel BER=0.1%	-11	-	-	dB
	BR, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR2, co-channel BER=0.1%	11	-	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-2	-	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-17	-	-	dB
	EDR2, adjacent >=|±3| MHz BER=0.1%	-17	-	-	dB
	EDR2, Image channel BER=0.1%	-9	-	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR3, co-channel BER=0.1%	19	-	-	dB
	EDR3, adjacent +1/- MHz BER=0.1%	3	-	-	dB
	EDR3, adjacent +2/-2 MHz BER=0.1%	-12	-	-	dB
	EDR3, adjacent >=|±3| MHz BER=0.1%	-12	-	-	dB
	EDR3, Image channel BER=0.1%	-2	-	-	dB
	EDR3, adjacent to Image channel BER=0.1%	-15	-	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	11	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	4	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-5	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	-21	-	dB
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	-28	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	-21	-	dB

Parameter	Condition/Notes	Min	Typ	Max	Units
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	-31	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	-36	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-26	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	-36	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	-21	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	10	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-3	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-5	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	-14	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	-20	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	-34	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	-14	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	-26	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-3	-	dB

Table 35 Bluetooth Receiver Characteristics on HP RF Chain

1. **BR,EDR:** Sensitivities for channels 38,78 are up to 4dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)
2. **BLE,LR:** Sensitivities for channels 19,39 are up to 3dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)

3.5.7 Bluetooth Receiver Characteristics on Low-Power (LP) RF Chain

TA = 25°C. Parameters are measured at antenna port and applicable to both PA2G_AVDD/VINBCKDC=1.85V and PA2G_AVDD/VINBCKDC=3.3V

Parameter	Condition/Notes	Min	Typ	Max	Units
Sensitivity,Dirty TX off[1],[2]	BR (1 Mbps), 339 bytes, DH5 Packet BER= 0.1%	-	-87.5	-	dBm

Parameter	Condition/Notes	Min	Typ	Max	Units
	EDR2 (2 Mbps), 679 bytes, 2-DH5 Packet, BER= 0.01%	-	-90.5	-	dBm
	LE (1 Mbps), 37 bytes, PER=30.8%	-	-90	-	dBm
	LE (2 Mbps), 37 bytes, PER=30.8%	-	-88.5	-	dBm
	LR (500 Kbps), 37 bytes, PER=30.8%	-	-97	-	dBm
	LR (125 Kbps), 37 bytes, PER=30.8%	-	-102.5	-	dBm
Maximum Input Level	BR, EDR2 BER= 0.1%	-	-16	-	dBm
	LE 1Mbps, 2Mbps PER=30.8%	-	3	-	dBm
	LR 500kps, 125kbps PER=30.8%	-	10	-	dBm
BER Floor		-	1e-4	-	%
C/I Performance	BR, co-channel BER= 0.1%	9	-	-	dB
	BR, adjacent +1/-1 MHz, BER=0.1%	-2	-	-	dB
	BR, adjacent +2/-2 MHz BER=0.1%	-19	-	-	dB
	BR, adjacent >=|±3| MHz BER=0.1%	-19	-	-	dB
	BR, Image channel BER=0.1%	-11	-	-	dB
	BR, adjacent to Image channel BER=0.1%	-22	-	-	dB
	EDR2, co-channel BER=0.1%	11	-	-	dB
	EDR2, adjacent +1/-1 MHz BER=0.1%	-2	-	-	dB
	EDR2, adjacent +2/-2 MHz BER=0.1%	-17	-	-	dB
	EDR2, adjacent >=|±3| MHz BER=0.1%	-17	-	-	dB
	EDR2, Image channel BER=0.1%	-9	-	-	dB
	EDR2, adjacent to Image channel BER=0.1%	-22	-	-	dB
	LE 1Mbps, co-channel PER=30.8%	-	11	-	dB
	LE 1Mbps, adjacent +1 MHz PER=30.8%	-	5	-	dB
	LE 1Mbps, adjacent -1 MHz PER=30.8%	-	-4	-	dB
	LE 1Mbps, adjacent +2 MHz PER=30.8%	-	-21	-	dB

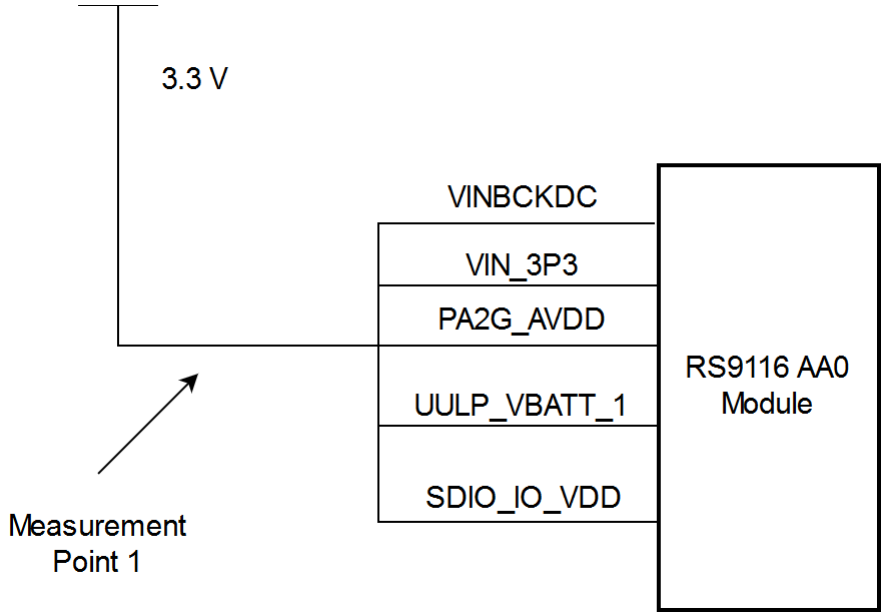
Parameter	Condition/Notes	Min	Typ	Max	Units
	LE 1Mbps, adjacent -2 MHz PER=30.8%	-	-28	-	dB
	LE 1Mbps, adjacent +3 MHz PER=30.8%	-	-22	-	dB
	LE 1Mbps, adjacent -3 MHz PER=30.8%	-	-29	-	dB
	LE 1Mbps, adjacent >= |±4| MHz PER=30.8%	-	-36	-	dB
	LE 1Mbps, Image channel PER=30.8%	-	-29	-	dB
	LE 1Mbps, +1MHz adjacent to Image channel PER=30.8%	-	-35	-	dB
	LE 1Mbps, -1MHz adjacent to Image channel PER=30.8%	-	-22	-	dB
	LE 2Mbps, co-channel PER=30.8%	-	9	-	dB
	LE 2Mbps, adjacent +2 MHz PER=30.8%	-	-4	-	dB
	LE 2Mbps, adjacent -2 MHz PER=30.8%	-	-4	-	dB
	LE 2Mbps, adjacent +4 MHz PER=30.8%	-	-13	-	dB
	LE 2Mbps, adjacent -4 MHz PER=30.8%	-	-20	-	dB
	LE 2Mbps, adjacent >= |±6| MHz PER=30.8%	-	-35	-	dB
	LE 2Mbps, Image channel PER=30.8%	-	-13	-	dB
	LE 2Mbps, +2MHz adjacent to Image channel PER=30.8%	-	-25	-	dB
	LE 2Mbps, -2MHz adjacent to Image channel PER=30.8%	-	-4	-	dB

Table 36 Bluetooth Receiver Characteristics on LP RF Chain

1. **BR,EDR:** Sensitivities for channels 38,78 are up to 4dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)
2. **BLE,LR:** Sensitivities for channels 19,39 are up to 3dB worse, due to the desensitization of the receiver from harmonics of the system clock (40MHz)

3.6 Typical Current Consumption

3.6.1 3.3 V



3.6.1.1 WLAN

Parameter	Description	Value	Units
1 Mbps Listen	LP Chain	13.82	mA
1 Mbps RX Active	LP Chain	19.67	mA
6 Mbps RX Active	HP Chain	48.2	mA
72 Mbps RX Active	HP Chain	48.2	mA
11 Mbps TX Active	Tx Power = Maximum (18dBm) Tx Power = 8dBm	270 130	mA mA
6 Mbps TX Active	Tx Power = Maximum (18dBm) Tx Power = 8dBm	285 130	mA mA
54 Mbps TX Active	Tx Power = Maximum (15dBm) Tx Power = 8dBm	200 130	mA mA
72 Mbps TX Active	Tx Power = Maximum (12dBm) Tx Power = 8dBm	180 130	mA mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Standby Associated, DTIM = 1		293	uA
Standby Associated, DTIM = 3		119	uA
Standby Associated, DTIM = 10		51	uA

3.6.1.2 Bluetooth BR and EDR

Parameter	Description	Value	Units
TX Active Current, 1 Mbps BR	LP chain, Tx Power = -2 dBm HP chain, Tx Power = Maximum (12 dBm)	9.9 130	mA mA
RX Active Current, 1 Mbps BR	LP chain HP chain	10.2 26.7	mA mA
TX Active Current, 2 Mbps EDR	HP chain, Tx Power = Maximum (12 dBm)	130	mA
RX Active Current, 2 Mbps EDR	LP chain HP chain	10.2 26.7	mA mA
TX Active Current, 3 Mbps EDR	HP chain, Tx Power = Maximum (12 dBm)	140	mA
RX Active Current, 3 Mbps EDR	HP chain	26.7	mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA

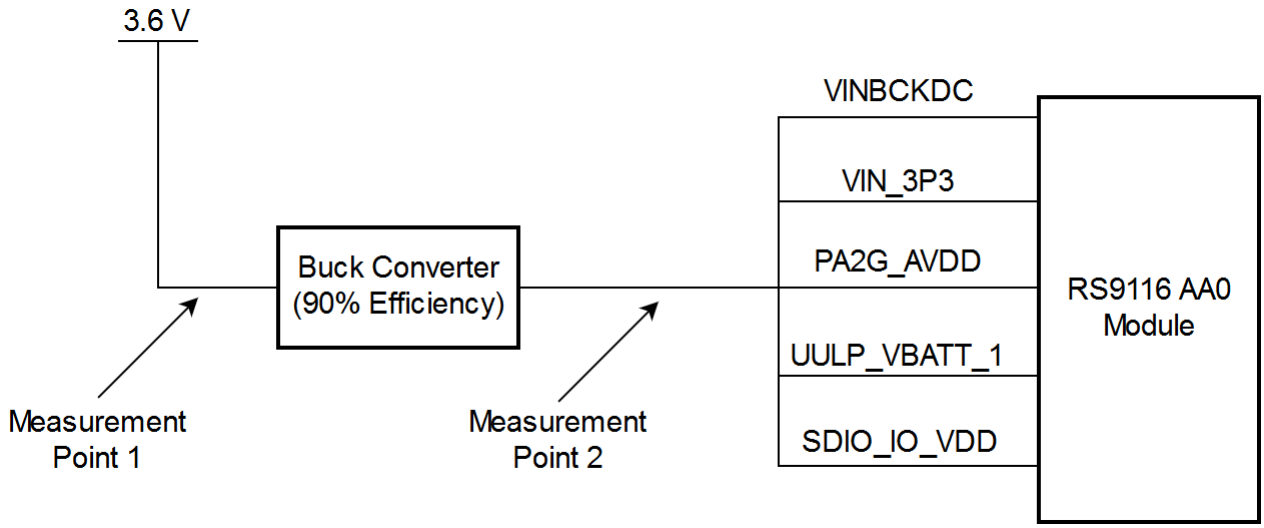
3.6.1.3 Bluetooth LE

Parameter	Description	Value	Units
TX Active Current	LP chain, Tx Power = -2 dBm LP Chain, Tx Power = 2 dBm HP Chain, Tx Power = Maximum (18 dBm)	8.9 - 190	mA mA mA
RX Active Current	LP chain HP chain	10.9 26.7	mA mA
Deep Sleep	GPIO Wake up	0.9	uA
Standby	State retained	13.1	uA
Advertising, Unconnectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = -2 dBm, LP chain	22.4	uA
Advertising, Connectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = -2 dBm, LP chain	30.1	uA
Connected	Connection Interval = 1.28s No Data Tx Power = -2 dBm, LP chain	21.8	uA
Connected	Connection Interval = 200ms No Data	72	uA

Parameter	Description	Value	Units
	Tx Power = -2 dBm, LP chain		
Scanning	Scan Interval = 1.28s Scan Window = 11.25ms LP Chain	-	uA

3.6.2 1.85 V

**Please Note that the below efficiency values are at 3.6V applied on the Buck Converter. If a better voltage is applied, then customer can expect better efficiencies.



3.6.2.1 WLAN

Parameter	Description	Value @ 3.6V	Value @ 1.85V	Units
1 Mbps Listen	LP Chain	13.4	23.5	mA
1 Mbps RX Active	LP Chain	19	33.3	mA
6 Mbps RX Active	HP Chain	37	65	mA
72 Mbps RX Active	HP Chain	39	68.3	mA
11 Mbps TX Active	Tx Power = Maximum (15dBm) Tx Power = 8dBm	133 69	233 121	mA mA
6 Mbps TX Active	Tx Power = Maximum (15dBm) Tx Power = 8dBm	136 67	238.2 117.3	mA mA
54 Mbps TX Active	Tx Power = Maximum (12dBm) Tx Power = 8dBm	106 67	185.6 117.3	mA mA
72 Mbps TX Active	Tx Power = Maximum (10dBm) Tx Power = 8dBm	97 87	170 152.4	mA mA

Parameter	Description	Value @ 3.6V	Value @ 1.85V	Units
Deep Sleep	GPIO Wake up	0.9	1.6	uA
Standby	State retained	12.3	21.5	uA
Standby Associated, DTIM = 1		250	438	uA
Standby Associated, DTIM = 3		92	161.2	uA
Standby Associated, DTIM = 10		41	72	uA

3.6.2.2 Bluetooth BR and EDR

Parameter	Description	Value @ 3.6V	Value @ 1.85V	Units
TX Active Current, 1 Mbps BR	LP chain, Tx Power = -2 dBm HP chain, Tx Power = Maximum (12 dBm)	8.6 -	15 -	mA mA
RX Active Current, 1 Mbps BR	LP chain HP chain	9.3 23	16.3 40.3	mA mA
TX Active Current, 2 Mbps EDR	HP chain, Tx Power = Maximum (12 dBm)	-	-	mA
RX Active Current, 2 Mbps EDR	LP chain HP chain	10.2 24	18 42	mA mA
TX Active Current, 3 Mbps EDR	HP chain, Tx Power = Maximum (12 dBm)	-	-	mA
RX Active Current, 3 Mbps EDR	HP chain	24	42	mA
Deep Sleep	GPIO Wake up	0.9	1.6	uA
Standby	State retained	12.3	21.5	uA
Inquiry Scan	Scan Interval = 1.28s Scan Window = 128ms	2.7	4.73	mA
Page Scan	Scan Interval = 1.28s Scan Window = 128ms	2.7	4.73	mA
Inquiry and Page Scan	Inquiry/Page Scan Interval = 1.28s Scan Window = 128ms	5.5	9.6	mA
SNIFF Mode	Sniff Interval = 500ms Attempts = 2 Tx Power = 2 dBm, HP chain	263	461	uA

3.6.2.3 Bluetooth LE

Parameter	Description	Value @ 3.6V	Value @ 1.85V	Units
TX Active Current	LP chain, Tx Power = -2 dBm LP Chain, Tx Power = 2 dBm HP Chain, Tx Power = Maximum (14 dBm)	8.6 13.6 -	15.2 23.8 -	mA mA mA
RX Active Current	LP chain HP chain	9.6 -	17 -	mA mA
Deep Sleep	GPIO Wake up	0.9	1.6	uA
Standby	State retained	12.3	21.5	uA
Advertising, Unconnectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = -2 dBm, LP chain	-	-	uA
Advertising, Connectable	Advertising on all 3 channels Advertising Interval = 1.28s Tx Power = -2 dBm, LP chain	31	54.3	uA
Connected	Connection Interval = 1.28s No Data Tx Power = -2 dBm, LP chain	25	44	uA
Connected	Connection Interval = 200ms No Data Tx Power = -2 dBm, LP chain	69	121	uA
Scanning	Scan Interval = 1.28s Scan Window = 11.25ms LP Chain	-	-	uA

4 RS9116 AA0 module Detailed Description

4.1 Overview

RS9116 AA0 module is based on Silicon Labs' RS9116 ultra-low-power, single spatial stream, 802.11n + BT/BLE5.0 Convergence SoC. The RS9116 AA0 module provides low-cost CMOS integration of a multi-threaded MAC processor (threadArch®), baseband digital signal processing, analog front-end, crystal oscillator, calibration eFuse, 2.4GHz RF transceiver, integrated power amplifier, match, bandpass filters(BPF), antenna diversity switch (DPDT) and Quad-SPI Flash thus providing a fully-integrated solution for a range of hosted and embedded wireless applications. With Silicon Labs' embedded four-threaded processor and on-chip ROM and RAM, these modules enable integration into low-cost and zero host load applications. With an integrated PMU and support for a variety of digital peripherals, RS9116 enables very low-cost implementations for wireless hosted and embedded applications. It can be connected to a host processor through SDIO, USB, SPI or UART interfaces. Wireless firmware upgrades and provisioning are supported.

4.2 Module Features

4.2.1 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n with single band support
- Support for 20 MHz channel bandwidth
- Transmit power up to +18 dBm with integrated PA
- Receive sensitivity as low as -96 dBm
- Data Rates:- 802.11b: Upto11 Mbps ; 802.11g: Upto54 Mbps ; 802.11n: MCS0 to MCS7
- Operating Frequency Range:- 2412 MHz – 2484 MHz

4.2.1.1 MAC

- Conforms to IEEE 802.11b/g/n/j standards for MAC
- Dynamic selection of fragment threshold, data rate, and antenna depending on the channel statistics
- Hardware accelerators for WEP 64/128-bit and AES
- WPA, WPA2, and WMM support
- AMPDU and AMSDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS)

4.2.1.2 Baseband Processing

- Supports DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates (6, 9, 12, 18, 24, 36, 48, 54 Mbps, MCS0 to MCS7), and Short GI in Hosted mode
- Supports IEEE 802.11n single-stream modes with data rates up to 150 Mbps
- Supports long, short, and HT preamble modes
- High-performance multipath compensation in OFDM, DSSS, and CCK modes

4.2.2 Bluetooth

- Transmit power up to +16 dBm with integrated PA
- Receive sensitivity:- LE: -92 dBm, LR 125 Kbps: -102 dBm
- Compliant to dual-mode Bluetooth 5
- <8 mA transmit current in Bluetooth 5 mode, 2 Mbps data rate
- Data rates: 125 Kbps, 500 Kbps, 1 Mbps, 2Mbps, 3 Mbps
- Operating Frequency Range:- 2.402 GHz - 2.480 GHz

- Bluetooth 2.1 + EDR, Bluetooth Low Energy 4.0 / 4.1 / 4.2 / 5.0
- Bluetooth Low Energy 1 Mbps, 2 Mbps and Long Range modes
- Bluetooth Low Energy Secure connections
- Bluetooth Low Energy supports central role and peripheral role concurrently.
- Bluetooth auto rate and auto TX power adaptation
- Scatternet* with two slave roles while still being visible.

* For detailed list of Software features, and available profiles, please refer the Software Reference Manuals, or, Contact Silicon Labs for availability.

4.2.2.1 MAC

4.2.2.1.1 Link Manager

- Creation, modification & release of logical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- Services the data transport requests from L2CAP and provides required QOS
- Support for security using ECDH hardware accelerator

4.2.2.1.2 Link Controller

- Encodes and decodes header of BT packets
- Manages flow control, acknowledgment, retransmission requests, etc.
- Stores the last packet status for all logical transports
- Chooses between SCO & ACL buffers depending on the control information coming from BBP resource manager
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

4.2.2.1.3 Host Controller

- Receives & decodes commands received from the Bluetooth Host.
- Propagates the decoded commands to respective modules
- Responsible for transmitting and receiving packets from and to Host
- Formats the responses coming from other modules of Bluetooth Controller as events and sends them to the Host.

4.2.2.1.4 Device Manager

- Controls Scan & Connection processes
- Controls all BT Device operations except data transport operations
- Storing link keys
- BT Controller state transition management
- Slot synchronization & management
- Access contract management
- Scheduler

4.2.2.2 Baseband Processing

- Supports GFSK (1 Mbps), EDR-DQPSK, EDR-D8PSK

- Supports BLE and Bluetooth long range
- Supports Data rates up to 3 Mbps

4.2.3 RF Transceiver

- Integrated 2.4 GHz transceiver with highly programmable operating modes
- Internal oscillator with 40 MHz crystal
- Inbuilt automatic boot up and periodic calibration enables ease of integration

4.2.4 Host Interfaces

- SDIO
    - Version 2.0-compatible
    - Supports SD-SPI, 1-bit, and 4-bit SDIO modes
    - Operation up to a maximum clock speed of 50 MHz
- SPI Interface
    - Operation up to a maximum clock speed of 100 MHz
- USB 2.0
    - Supports 480Mbps “High Speed” (HS), 12Mbps “Full Speed” (FS) and 1.5Mbps “Low Speed” (LS) serial data transmission
    - Support USB CDC and device mode
- UART
    - Supports variable baud rates between 9600 and 3686400 bps
    - AT command interface for configuration and data transmission/reception

NOTE: Hosted mode (n-Link) supports USB 2.0 and SDIO. Embedded Mode (WiSeConnect) supports SPI, USB CDC, and UART.

4.2.4.1 Auto Host detection

RS9116 detects the host interface automatically after connecting to respective host controllers like SDIO, SPI, UART, USB and USB-CDC. SDIO/SPI host interface is detected through the hardware packet exchanges. UART host interface is detected through the software based-on the received packets on the UART interface. USB-Device mode interface is detected through the hardware based-on VBUS signal level. The host interface detection between USB & USB-CDC will be taken care by the firmware based on the USB CDC SEL GPIO. This Host configuration is stored in always-on domain registers after detection (on power up) and reused this information at each wakeup.

4.2.5 Wireless Coexistence Manager

- Arbitration between Wi-Fi, Bluetooth, and Bluetooth Low Energy
- Application aware arbitration
- Adaptive frequency hopping (AFH) in Bluetooth is based on WLAN channel usage
- Pre inter thread interrupts generation for radio switching
- QoS assurance across different traffics

4.2.6 Software

The RS9116 software package supports 802.11 b/g/n Client, Access Point (Up to 16 clients), Concurrent Client and Access Point mode, Enterprise Security dual-mode BT 5.0 functionality on a variety of host platforms and operating systems. The software package includes complete firmware, reference drivers, application profiles and configuration graphical user interface (GUI) for Linux operating systems. The Wi-Fi driver has support for a simultaneous access point, and client mode. Bluetooth host driver utilizes Opensource host stacks like BlueZ for Linux. The application layer supports all profiles supported by BlueZ on Linux. It has a wireless coexistence manager to arbitrate between protocols.

The RS9116 software package is available in two flavors

- **Hosted mode (n-Link™):** Wi-Fi stack, Bluetooth stack and profiles, and all network stacks reside on the host processor. Support for multiple Virtual Access Points available.
- **Embedded mode (WiSeConnect™):** Wi-Fi stack, TCP/IP stack, IP modules, Bluetooth stack and some profiles reside in RS9116; Some of the Bluetooth profiles reside in the host processor

NOTE: Please refer the Software Manuals (TRM and PRM) for more details.

4.2.6.1 Hosted Mode (n-Link™)

- Available host interfaces: SDIO 2.0 and USB HS
- Application data throughput up to 50 Mbps (Hosted Mode) in 802.11n with 20MHz bandwidth.
- Host drivers for Linux
- Support for Client mode, Access point mode (Upto 16 clients), Concurrent Client and Access Point mode, Enterprise Security
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

4.2.6.2 Embedded Mode (WiSeConnect™)

- Available host interface: UART, SPI, SDIO*, and USB CDC
- TCP throughput > 20Mbps over SDIO host interface with 20 MHz bandwidth
- Support for Embedded Client mode, Access Point mode (Upto 8 clients), Concurrent Client and Access Point mode, and Enterprise Security
- Supports advanced security features: WPA/WPA2-Personal and Enterprise*
- Integrated TCP/IP stack (IPV4/IPV6), HTTP/HTTPS, DHCP, ICMP, SSL 3.0/TLS1.2, WebSockets, IGMP, DNS, DNS-SD, SNMP, FTP Client, MQTT*
- Bluetooth inbuilt stack support for L2CAP, RFCOMM, SDP, SPP, GAP
- Bluetooth profile support* for GAP, SDP, L2CAP, RFCOMM, SPP, GATT, PBAP
- Wireless firmware upgrade and provisioning
- Support for concurrent Wi-Fi, dual-mode Bluetooth 5

> * For detailed list of Software features, and available profiles, please refer the Software Reference Manuals, or, Contact Silicon Labs for availability.

4.2.7 Security

RS9116 supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256 in Embeded Mode
- WPA/WPA2-Personal, WPA/WPA2 Enterprise for Client*
- Secure Firmware upgrade* with backup

> * For detailed list of Software features, and available profiles, please refer the Software Reference Manuals, or, Contact Silicon Labs for availability.

4.2.8 Power Management

The RS9116 chipsets have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the chipset to operate from a wide variety of input sources.

- LC DC-DC switching converter for RF and Digital blocks

- Wide input voltage range (1.85 to 3.6V) on pin VINBCKDC
- Output - 1.4V and 300mA maximum load on pin VOUTBCKDC

- SC DC-DC - Switching converter for Always-ON core logic domain
  - Wide input voltage range (1.85 to 3.6V) on pin UULP_VBATT_1 and UULP_VBATT_2
  - Output - 1.05V
- LDO SOC - Linear regulator for digital blocks
  - Input - 1.4V from LC DC-DC or external regulated supply on pin VINLDOSOC
  - Output - 1.15V and 300mA maximum load on pin VOUTLDOSOC
- LDO RF and AFE - Linear regulator for RF and AFE
  - Input - 1.4V from LC DC-DC or external regulated supply on pin RF_AVDD
  - Output - 1.1V and 20mA maximum load on pin VOUTLDOAFE
- LDO FLASH - Linear regulator for internal and external Flash
  - Input - Wide input voltage range (1.85 to 3.6V) on pin VINLDO1P8
  - Output - 1.8V and 20mA maximum load on pin VOUTLDO1P8

4.2.9 Low power modes

It supports Ultra-low power consumption with multiple power modes to reduce the system energy consumption.

- Dynamic Voltage and Frequency Scaling
- Low Power (LP) mode with only the host interface active
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to LP or ULP modes

4.2.9.1 ULP mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a 32 KHz low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

ULP mode is not supported in the USB interface mode

4.2.9.2 LP mode

In Low Power mode, Network processor maintains system state and gate all internal high frequency clocks. But host interface is ready to accept any command from host controller.

The LP mode supports the following wake-up options:

- Host Request - Exit sleep state on a command from HOST controller. whenever a command from the host is received, the processor serves the request with minimum latency and the clock is gated immediately after the completion of the operation to reduce power consumption
- GPIO based wakeup - Wakeup can be initiated through a GPIO pin
- Timeout wakeup - Exit sleep state after the programmed timeout value

4.2.10 Memory

4.2.10.1 On-chip memory

The threadArch® processor has the following memory:

- On-chip SRAM for the wireless stack.
- 512Kbytes of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions.
- 16Kbytes of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 512 bytes (used to store primary boot configuration, security and calibration parameters)

4.2.10.2 Serial Flash

The RS9116 utilizes a serial Flash to store processor instructions and other data. The SPI Flash Controller is a 1/2/4-wired interface for serial access of data from Flash. It can be used in either Single, Dual or Quad modes. Instructions are read using the Direct Fetch mode while data transfers use the Indirect Access mode. The SPI Flash Controller in RS9116 has been designed with programmable options for most of the single and multi-bit operations. RS9116 AA0 module has 4 Mbytes internal flash memory.

5 RS9116 AA0 module Reference Schematics, BOM and Layout Guidelines

5.1 SDIO/SPI/UART

5.1.1 Schematics

The below diagram shows the typical schematic with SDIO/SPI/UART Host Interface.

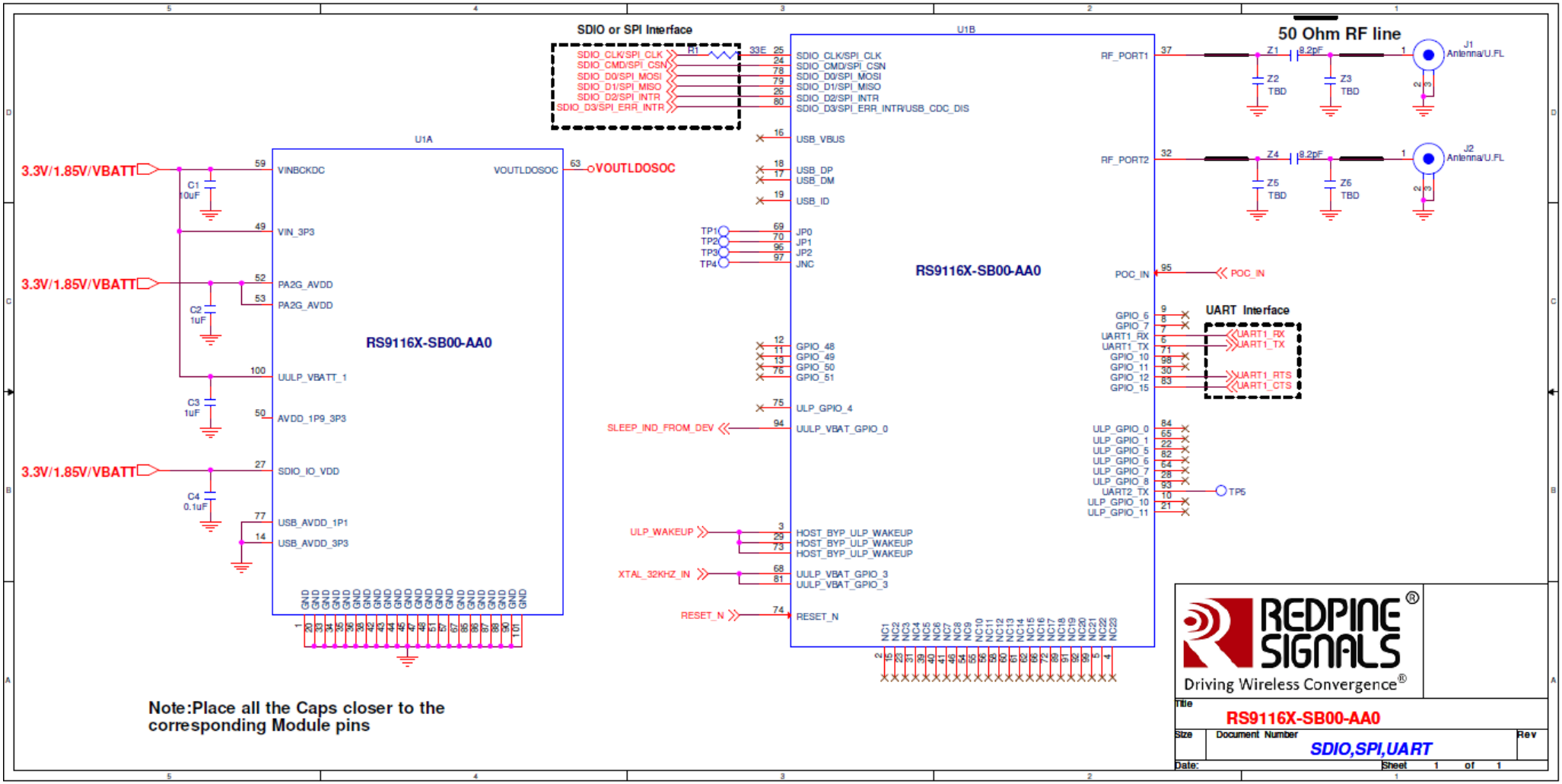

SDIO or SPI Interface
50 Ohm RF line
U1A
U1B
RS9116X-SB00-AA0
UART Interface
3.3V/1.85V/VBATT
VINBCKDC
VOUTLDOSOC
VIN_3P3
PA2G_AVDD
ULP_VBATT_1
AVDD_1P9_3P3
SDIO_IO_VDD
USB_AVDD_1P1
USB_AVDD_3P3
SDIO_CLK/SPI_CLK
SDIO_CMD/SPI_CSN
SDIO_D0/SPI_MOSI
SDIO_D1/SPI_MISO
SDIO_D2/SPI_INTR
SDIO_D3/SPI_ERR_INTR/USB_CDC_DIS
USB_VBUS
USB_DP
USB_DM
USB_ID
JP0
JP1
JP2
JNC
GPIO_48
GPIO_49
GPIO_50
GPIO_51
ULP_GPIO_4
ULP_VBAT_GPIO_0
HOST_BYP_ULP_WAKEUP
ULP_VBAT_GPIO_3
RESET_N
RF_PORT1
RF_PORT2
POC_IN
UART1_RX
UART1_TX
UART1_RTS
UART1_CTS
TP5
J1 Antenna/U.FL
J2 Antenna/U.FL
Note:Place all the Caps closer to the corresponding Module pins
REDPINE SIGNALS
Driving Wireless Convergence®
RS9116X-SB00-AA0
SDIO,SPI,UART

Figure 16 Schematics with SDIO/SPI/UART Host Interface

1. PA2G_AVDD can be driven by 3.3V source irrespective of other sources for Maximum Transmit Output power.
2. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
3. SDIO_IO_VDD can be driven by a different source irrespective of other sources to support different interfaces.
4. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification, version 2.0.
5. In SPI mode, ensure that the input signals, SPI_CS and SPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset. SPI_INTR is the interrupt signal driven by the slave device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor may be required. If it is active-low, an external pull-up resistor may be required. This resistor can be avoided if the following action needs to be carried out in the host processor
    a. To use the signal in the Active-high or Active-low mode, ensure that, during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the SPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
    b. The Host processor needs to be disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
6. In UART mode, ensure that the input signals, UART_RX and UART_CTS are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.
7. Resistor "**R1**" should not be populated if UART is used as Host Interface.

5.1.2 Bill of Materials

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	1	C1	10uF	CAP CER 10UF 10V X5R 0805	0805	Murata	GRM21BR61A106KE19L
2	2	C2,C3	1uF	CAP CER 1UF 10V 10% X5R 0402	0402	Murata	GRM155R61A105KE15D
3	1	C4	0.1uF	CAP CER 0.1UF 10V X5R 0402	0402	Murata	GRM155R61A104KA01D
4	2	J1,J2		Antenna/U.FL			
5	1	R1	33E	RES SMD 33 OHM 5% 1/10W	0402	Panasonic	ERJ-2GEJ330X
6	1	U1		Wireless Single Band Module		Redpine	RS9116N-SB00-AA0 / RS9116W-SB00-AA0

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
7	2	Z1,Z4	8.2pF	CER CHP 8.2P +/-0.25P C0G 0201 25V	0201	Murata	GRM0335C1E8R2CD01D
8	4	Z2,Z3,Z5,Z6		Optional Capacitors for Antenna Matching	0201		

Table 37 Bill of Materials with SDIO/SPI/UART Host Interface

5.2 USB/USB-CDC

5.2.1 Schematics

The below diagram shows the typical schematic with USB/USB-CDC Host Interface.

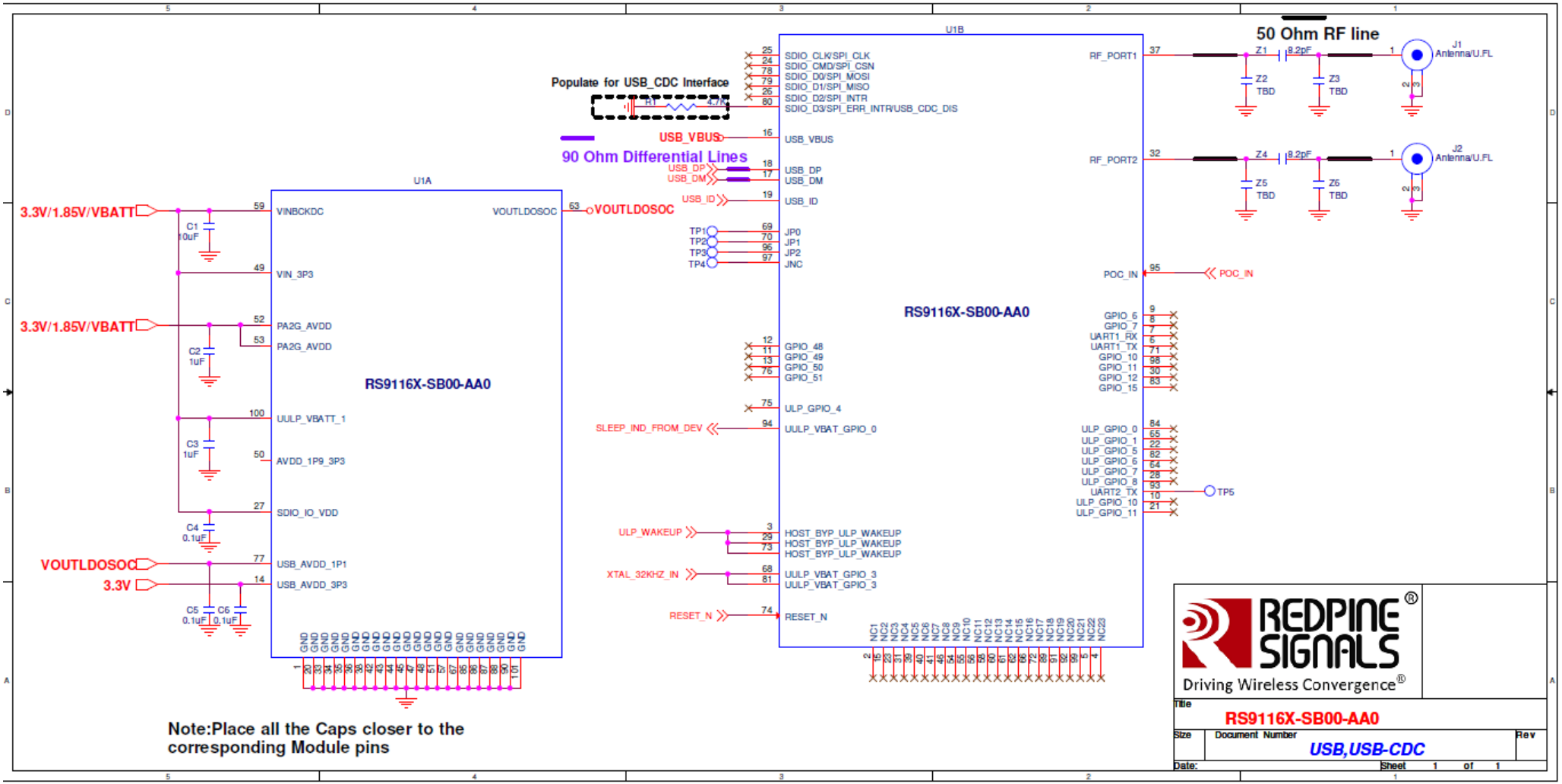

U1A
U1B
RS9116X-SB00-AA0
3.3V/1.85V/VBATT
VOUTLDOSOC
3.3V
Populate for USB_CDC Interface
90 Ohm Differential Lines
USB_VBUS
50 Ohm RF line
RF_PORT1
RF_PORT2
POC_IN
SLEEP_IND_FROM_DEV
ULP_WAKEUP
XTAL_32KHZ_IN
RESET_N
Note:Place all the Caps closer to the corresponding Module pins
REDPINE SIGNALS
Driving Wireless Convergence
Title
RS9116X-SB00-AA0
Document Number
USB,USB-CDC
Size
Rev
Date:
Sheet 1 of 1

Figure 17 USB Schematics

1. PA2G_AVDD can be driven by 3.3V source irrespective of other sources for Maximum Transmit Output power.
2. The supplies can be driven by different voltage sources within the recommended operating conditions specified in Specifications section.
3. Ensure that the pin USB_CDC_DIS is left unconnected to ensure normal USB functionality.
4. Resistor "**R1**" should not be populated if normal USB is used as Host Interface

5.2.2 Bill of Materials

S.No.	Quantity	Reference	Value	Description	JEDEC	Manufacturer	Part Number
1	1	C1	10uF	CAP CER 10UF 10V X5R 0805	0805	Murata	GRM21BR61A106KE19L
2	2	C2,C3	1uF	CAP CER 1UF 10V 10% X5R 0402	0402	Murata	GRM155R61A105KE15D
3	3	C4,C5,C6	0.1uF	CAP CER 0.1UF 10V X5R 0402	0402	Murata	GRM155R61A104KA01D
4	2	J1,J2		Antenna/U.FL			
5	1	R1	4.7K	RES SMD 4.7K OHM 5% 1/10W 0402	0402	Panasonic	ERJ-2GEJ472X
6	1	U1		Wireless Single Band Module		Redpine	RS9116N-SB00-AA0 / RS9116W-SB00-AA0
7	2	Z1,Z4	8.2pF	CER CHP 8.2P +/-0.25P C0G 0201 25V	0201	Murata	GRM0335C1E8R2CD01D
8	4	Z2,Z3,Z5,Z6		Optional Capacitors for Antenna Matching	0201		

Table 38 Bill of Materials with USB/USB-CDC Host Interface

5.3 Layout Guidelines

The following guidelines outline the integration of the module :-

1. The following Supply Pins needs to be STAR routed from the Supply Source
    a. VINBCKDC
    b. VIN_3P3
    c. PA2G_AVDD
    d. UULP_VBATT_1
    e. SDIO_IO_VDD
2. The RF_OUT2 (Module Pin No. 32) signal may be directly connected to an on-board chip antenna or terminated in an RF connector of any form factor for enabling the use of external antennas.
3. There need to be DC blocking capacitors (8.2pF) on RF_OUT_1 & RF_OUT_2 if they are connected to antennas.
4. The module has one ground pad of size 3.20mm x 3.20mm. The PCB layout must have a provision for the following:
    a. Provide a 3.20mm x 3.20mm ground copper pad on the top side of the PCB. Make sure to open the solder mask in this area so that the Cu is exposed.
    b. Provide a 3.20mm x 3.20mm ground copper pad on the bottom side of the PCB and keep open the solder mask in this area so that the Cu is exposed.
    c. The RF ground pad (pin number 101) should have 16 Vias, Each via should have a pad size of 24mil diameter and a 16mil drill.
5. The RF trace on RF_OUT should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 ohms line depends on the PCB stack, e.g., the dielectric of the PCB,dielectric constant of the material, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
6. To evaluate transmit and receive performance like Tx Power and EVM, Rx sensitivity and the like, an RF connector would be required. Since Antenna is connected to RF_PORT2, connect U.FI to RF_PORT1 for RF related Test & Evaluation.
7. For USB, it is recommended that the components and their values in the BoM be adhered to.
8. It is highly recommended that the two USB differential signals (USB_DP and USB_DN) be routed in parallel with a spacing (say, a) which achieves 90 Ω of differential impedances, 45 Ω for each trace.

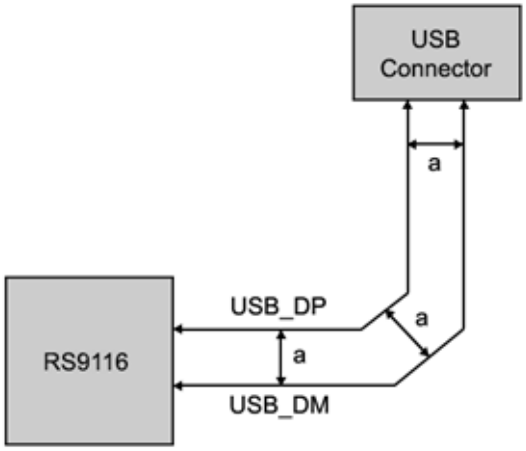


Figure 18 Spacing between USB_DP and USB_DN

9. In order to minimize crosstalk between the two USB differential signals (USB_DP and USB_DN) and other signal traces routed close to them, it is recommended that a minimum spacing of 3 x a be maintained for low-speed non-periodic signals and a minimum spacing of 7 x a be maintained for high-speed periodic signals.

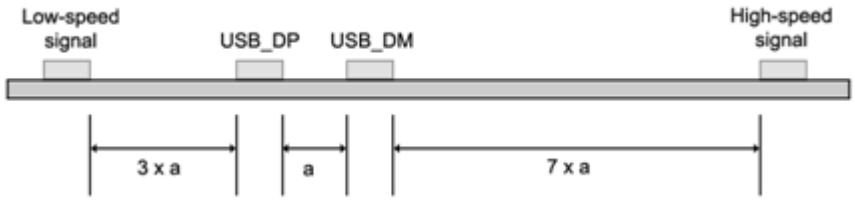


Figure 19 Spacing for Low-speed and High-speed signals around USB_DP/USB_DN

10. It is recommended that the total trace length of the signals between the RS9116 module and the USB connector be less than 450mm.
11. If the USB high-speed signals are routed on the Top layer, best results will be achieved if Layer2 is a Ground plane. Furthermore, there must be only one ground plane under high-speed signals in order to avoid the high-speed signals crossing to another ground plane.

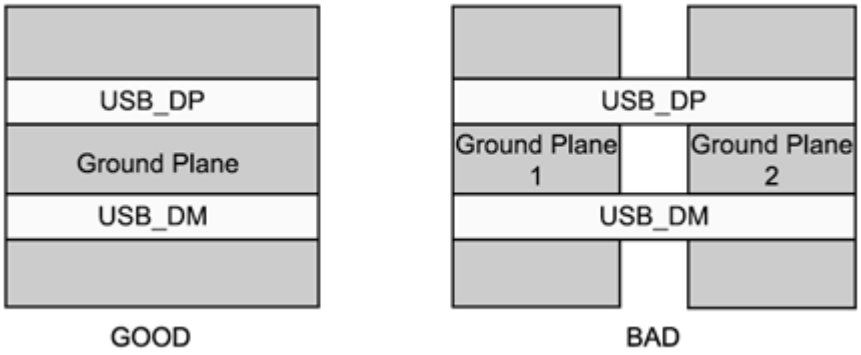


Figure 20 USB Signals and the Ground Plane

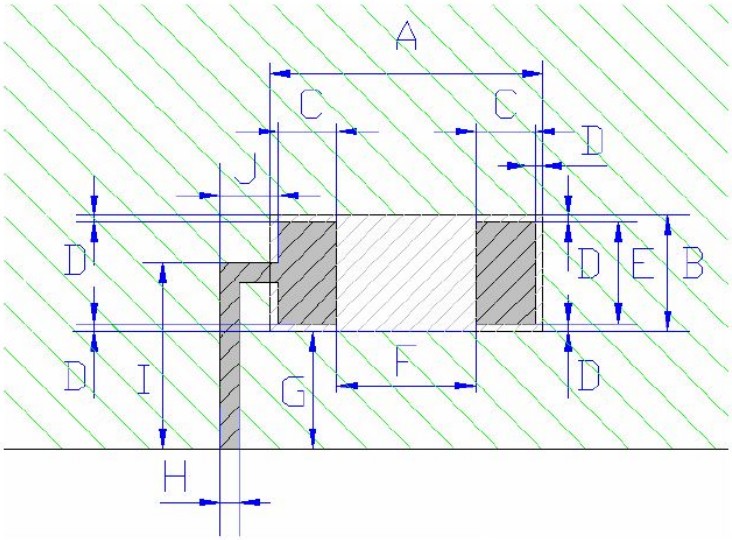
12. Each GND pin must have a separate GND via.
13. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
14. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
15. Add GND copper pour underneath IC/Module in all layers, for better thermal dissipation.

The antenna layout guidelines for single band modules without antenna are below: -

The choice of antenna depends on the application. However, if an on-chip antenna is to be used, we recommend the Fractus FR05-S1-N-0-102.

There should be no metal planes or traces in the region under the PCB antenna. The Ground plane should be removed from under and both sides of the antenna. Follow the rules listed in the figure below while doing the layout for the chip antenna.

This antenna footprint applies for the reference evaluation board described in page 4 of this User Manual.
Feeding line dimensions over the clearance zone described in figure 6 applies for a 1 mm thickness FR4 PCB.



Letter	Meas.
A	7.00
B	3.00
C	1.50
D	0.20
E	2.60
F	3.60
G	3.00
H	0.50
I	4.75
J	1.50

All dimensions are in millimetres.

Zone occupied by the antenna
Soldering pads and feed point
Clearance (PCB area without ground-plane)

Figure 21 Antenna Layout Recommendations

NOTE: The above figure shows the antenna footprint details for 0.8mm thickness FR4 PCB.

The recommended Chip Antennas are λ/4 antennas. They require an external ground plane for proper functioning. The length of the ground plane behind the antenna (from the feed point of antenna to backwards) should be at least 25mm – the longer the ground plane the better the performance.

It is recommended to characterize the antenna portion using a Network Analyzer. Electrical performance of any chip antenna is influenced by the physical characteristics of the surrounding ground plane, feed line, other devices, and materials. This can be used as an advantage by manipulating certain parameters to affect resonant frequency and matching. These parameters are listed below:

1. Ground plane configuration
2. Distance from antenna
3. Topology around antenna
4. Feed point transmission line impedance
5. Trace width
6. Trace length
7. Matching Network
8. PCB substrate thickness
9. PCB substrate dielectric constant.

6 RS9116 AA0 module Storage, Handling and Soldering Conditions

6.1 Recommended Reflow Profile

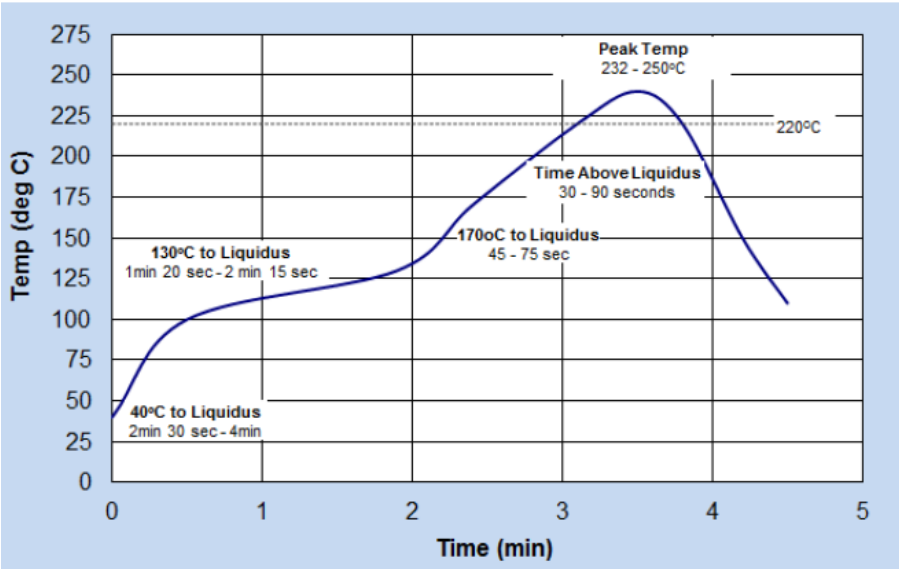


Figure 22 Reflow Diagram

Note:
The profile shown is based on SAC 305 solder (3% silver, 0.5% copper). We recommend the ALPHA OM-338 lead-free solder paste. This profile is provided mainly for guidance. The total dwell time depends on the thermal mass of the assembled board and the sensitivity of the components on it. The recommended belt speed is 50-60 Cm/Min. A finished module can go through two more reflow processes.

6.2 Baking Instructions

The packages are moisture sensitive (MSL3 grade) and devices must be handled appropriately. After the devices are removed from their vacuum-sealed packs, they should be taken through reflow for board assembly within 168 hours at room conditions or stored at under 10% relative humidity. If these conditions are not met, the devices must be baked before reflow. The recommended baking time is nine hours at 125°C.

7 RS9116 AA0 Module Package Description

7.1 Dimensions

Parameter	Typical	Units
Module Dimensions	14 x 15 x 2.1	mm
Tolerance	±0.2	mm

Table 39 Module Dimensions

7.2 Package Outline

7.2.1 Top View

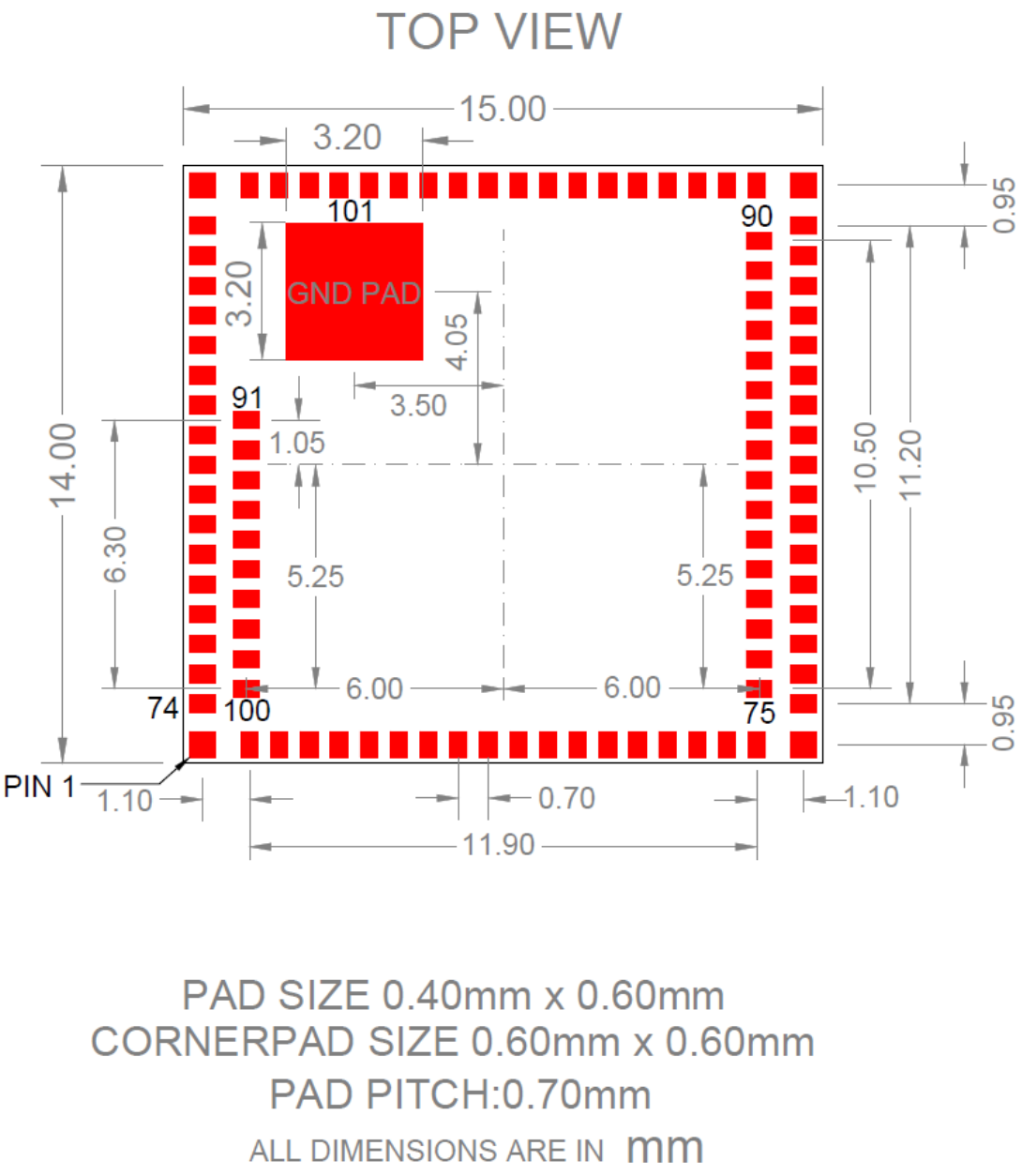
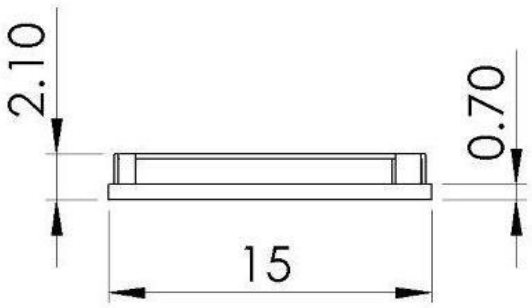


Figure 23 Package Outline

7.2.2 Side View



7.3 PCB Landing Pattern

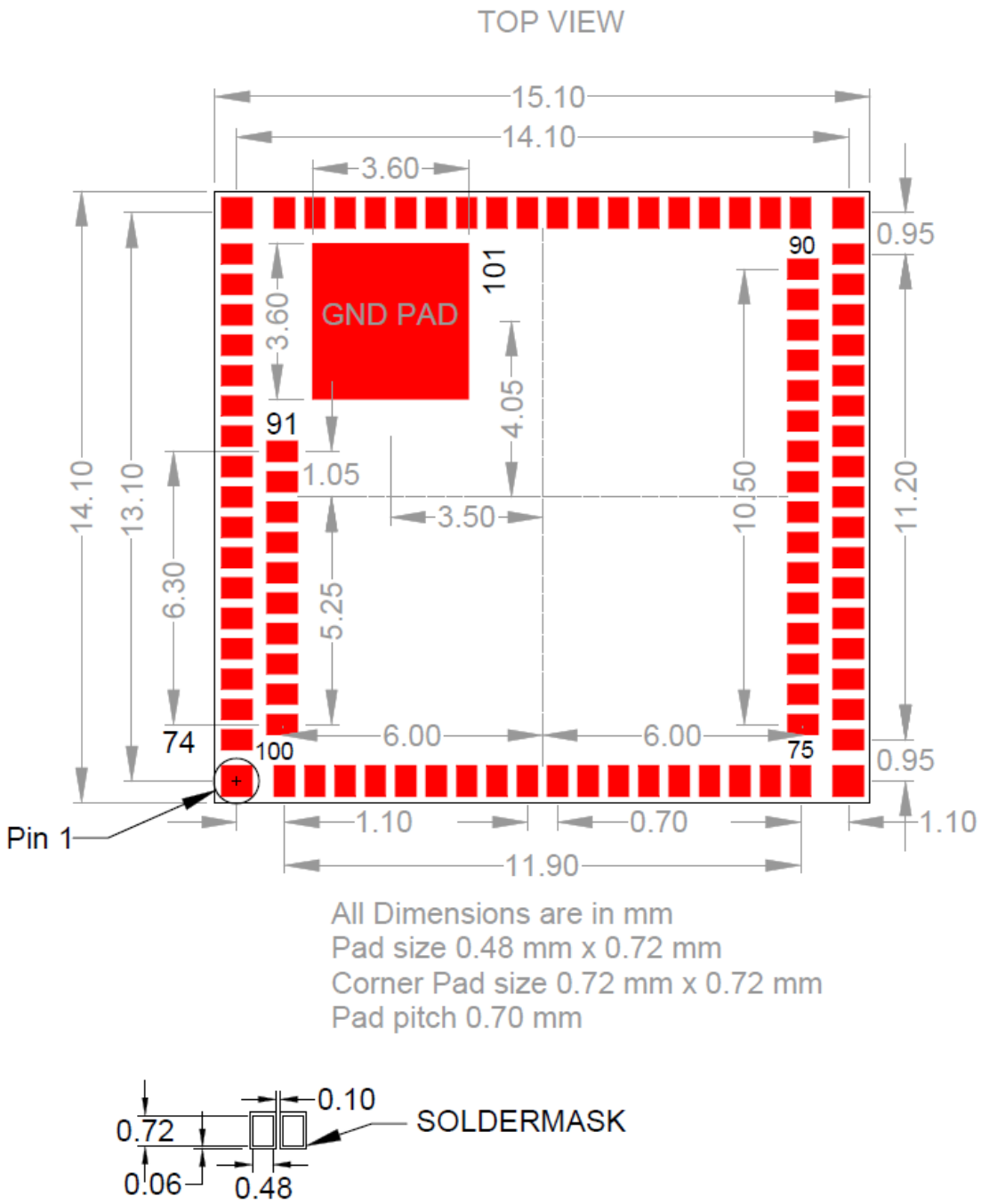


Figure 24 PCB Landing Pattern

7.3.1 Packing Information

7.3.1.1 Packing Information of Modules with Package Codes AA0

The modules are packaged and shipped in Trays.
Each tray for the AA0 package can accommodate 84 modules. The mechanical details of the tray for the AA0 packages are given in the figure below.

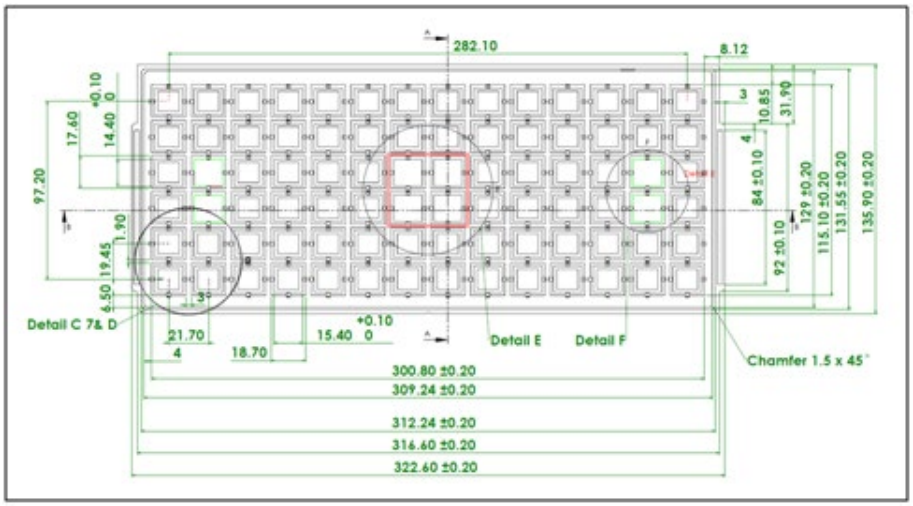


Figure 25 Packing Information of Modules with Package Codes AA0

8 RS9116 AA0 module Certification and Ordering Information

8.1 Certification Information

This section will outline the regulatory certification information for the RS9116 modules for the countries listed below. This information will be updated when available.

1. United States
2. Canada
3. Europe
4. Japan
5. Other Regulatory Jurisdictions

The RS9116 Single band AA0 modules from Redpine Signals have undergone modular certification for FCC, IC and CE/ETSI . Note that any changes to the module's configuration including (but not limited to) the programming values of the RF Transceiver and Baseband can cause the performance to change beyond the scope of the certification. These changes, if made, may result in the module having to be certified afresh. The table below lists the details of the regulatory certifications. The certification for geographies not listed in the table is in progress.

8.2 Compliance and Certification

M15SB module is FCC/IC/CE certified. This section outlines the regulatory information for the M15SB module. This allows integrating the module in an end product without the need to obtain subsequent and separate approvals from these regulatory agencies. This is valid in the case no other intentional or un-intentional radiator components are incorporated into the product and no change in the module circuitry. Without these certifications, an end product cannot be marketed in the relevant regions.

- RF Testing Software is provided for any end product certification requirements.

8.2.1 Federal Communication Commission Statement

Any changes or modifications not expressly approved by the party responsible for compliance could void your authority to operate the equipment.

Note

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

8.2.1.1 RF exposure statements

1. This Transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

2. This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20 centimeters between the radiator and your body or nearby persons.

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XF6-M15SB" or "Contains FCC ID: XF6-M15SB" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

8.2.1.2 Labeling and User Information

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. this device must accept any interference received, including interference that may cause undesired operation.

8.2.2 Industry Canada / ISED Statement

This product meets the applicable Innovation, Science and Economic Development Canada technical specifications.
Ce produit repond aux specifications techniques applicables a l'innovation, Science et Developpement economique Canada.

8.2.2.1 Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

Le present appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisee aux deux conditions suivantes :

1. l'appareil ne doit pas produire de brouillage;
2. l'utilisateur de l'appareil doit accepter tout brouillage radioelectrique subi, meme si le brouillage est susceptible d'en compromettre le fonctionnement.

8.2.2.2 Labeling and User Information

Innovation, Science and Economic Development Canada ICES003 Compliance Label: *CAN ICES-3 (B)/NMB-3(B)*

> The M15SB module has been labeled with its own IC ID number (8407A-M15SB) and if the IC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must also display a label referring to the enclosed module. This exterior label can use following wording: Contains Transmitter Module IC ID: 8407A-M15SB or Contains IC ID: 8407A-M15SB User manuals for license-exempt radio apparatus shall contain the above mentioned statement or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both

Warning:

1. The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
2. For devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;
3. For devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate; and

The high-power radars are allocated as primary users (i.e. priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

DFS (Dynamic Frequency Selection) products that operate in the bands 5250- 5350 MHz, 5470-5600MHz, and 5650-5725MHz.

This device is not capable of transmitting in the band 5600-5650 MHz in Canada.

Avertissement:

1. Le dispositif fonctionnant dans la bande 5150-5250 MHz est réservé uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux;
2. Le gain maximal d'antenne permis pour les dispositifs avec antenne(s) amovible(s) utilisant les bandes 5250-5350 MHz et 5470-5725 MHz doit se conformer à la imitation P.I.R.E.;
3. Le gain maximal d'antenne permis pour les dispositifs avec antenne(s) amovible(s) utilisant la bande 5725-5850 MHz doit se conformer à la limitation P.I.R.E spécifiée pour l'exploitation point à point et non point à point, selon le cas.

En outre, les utilisateurs devraient aussi être avisés que les utilisateurs de radars de haute puissance sont désignés utilisateurs principaux (c.-à-d., qu'ils ont la priorité) pour les bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer du brouillage et/ou des dommages aux dispositifs LAN-EL.

Les produits utilisant la technique d'atténuation DFS (sélection dynamique des réquences) sur les bandes 5250-5350 MHz, 5470-5600MHz et 5650-5725MHz.

Cet appareil ne peut pas émettre dans la bande 5600-5650 MHz au Canada.

8.2.3 CE

M15SB is in conformity with the essential requirements and other relevant requirements of the R&TTE Directive (1999/5/EC). The product is conformity with the following standards and/or normative documents.

- EMC (immunity only) EN 301 489-17 V.2.2.1 in accordance with EN 301 489-1 V1.9.2
- Radiated emissions EN 300 328 V1.9.1
- Safety standards: EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + A2:2013

8.2.4 TELEC

Telefication, operating as Conformity Assessment Body (CAB ID Number:201) with respect to Japan, declares that the M15SB complies with Technical Regulations Conformity Certification of specified Radio equipment (ordinance of MPT Nº 37,1981)

- The validity of this Certificate is limited to products, which are equal to the one examined in the type-examination
- when the manufacturer (or holder of this certificate) is placing the product on the Japanese market, the product must affixed with the following Specified Radio Equipment marking R201-190234

8.2.5 Qualified Antenna Types for M15SB

This device has been designed to operate with the antennas listed below. Antennas not included in this list or having a gain greater than listed gains in each region are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.

Antenna Model	Antenna Type	Gain	Qualified Region
RSIA15	PCB Trace Antenna	0.99 dBi	FCC/IC, CE, TELEC
WS.01.B.305151	Heavy Duty Screw Mount Antenna	4.1 dBi	FCC/IC, CE, TELEC
AEM6P-100000	Dipole Antenna	2 dBi	TELEC
AEM6P-100001	Dipole Antenna	2 dBi	TELEC
AEEE0-000000	Multilayer ceramic Antenna	2.13 dBi	TELEC
AEEE0-000001	Chip Antenna	4 dBi	TELEC
AEEE0-000002	Chip Antenna	4 dBi	TELEC

Antenna Model	Antenna Type	Gain	Qualified Region
AEP6P-100006X	PIFA Antenna	3 dBi	TELEC
AEP6P-100008X	PIFA Antenna	3 dBi	TELEC

Table 40 Qualified Antenna List

Any antenna that is of the same type and of equal or less directional gain can be used without a need for retesting. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication. Using an antenna of a different type or gain more than certified gain will require additional testing.

8.2.6 Module Marking Information

The figure and table below illustrates the marking on the Single band module, and explains the marking on the module.

Figure 26 Module Marking Information

Marking		Description
Model	M15SB	Model Number for Single-band modules
Firmware	RS9116X-SBX0-AAX	Software/Firmware supported – refer to the Part Ordering Section for more details.
FCC	XF6-M15SB	FCC Grant ID for Single-band modules.
IC	8407A-M15SB	IC Grant ID for Single-band modules.
Lot Code Information	XXX-WWYY	XXX – Internal usage WW – Week of manufacture YY – Year of manufacture
Compliance Marks	FC	FCC Compliance Mark
	CE	CE Compliance Mark
		TELEC Compliance Mark

8.3 Module Package

Package Code	Package Type, Pins	Dimensions (mm)	Frequency Band	Integrated Antenna	Notes
AA0	LGA,101	14 x 15 x 2.1	Single Band (2.4 GHz)	No	RS9113 Compatible

Table 41 Module Package

8.4 Ordering Information

Part Number	Wireless
Hosted Connectivity (n-Link)	
RS9116N-SB00-AA0-X00	SBW+BT5 with internal flash; Rev 1.3 Silicon
Embedded Connectivity (WiSeConnect)	
RS9116W-SB00-AA0-X24	SBW+BT5 with internal flash; Rev 1.3 Silicon; Firmware Version: 1.2.24

Table 42 Module Part Ordering Options

Note: SBW: Single Band Wi-Fi (2.4 GHz); DBW: Dual Band Wi-Fi (2.4/5 GHz)

8.4.1 Device Nomenclature

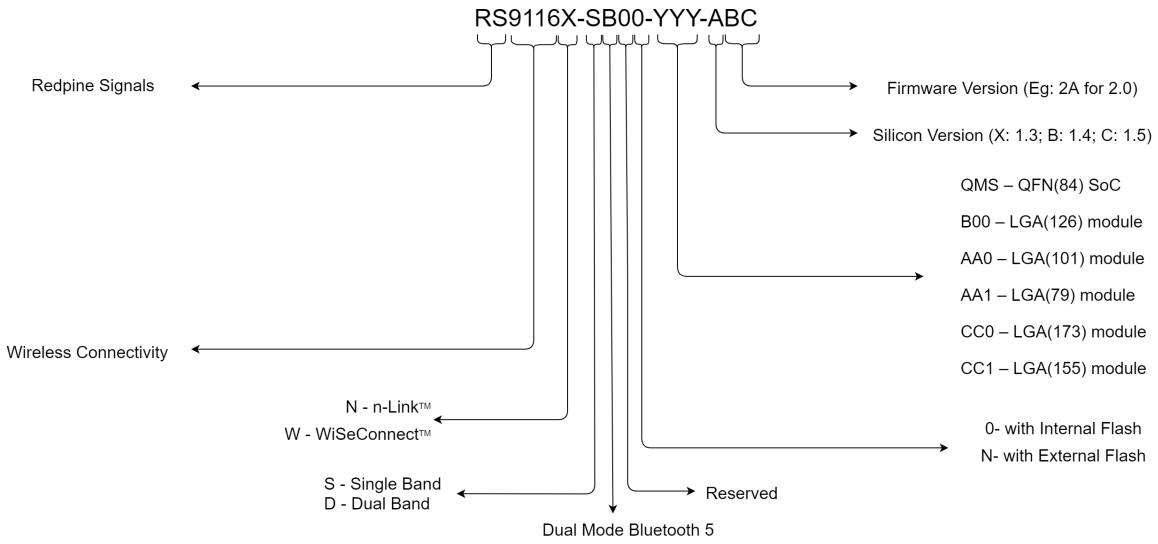


Figure 27 Device Nomenclature

9 RS9116 AA0 module Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using RS9116. These documents are available in RS9116 Document Library on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

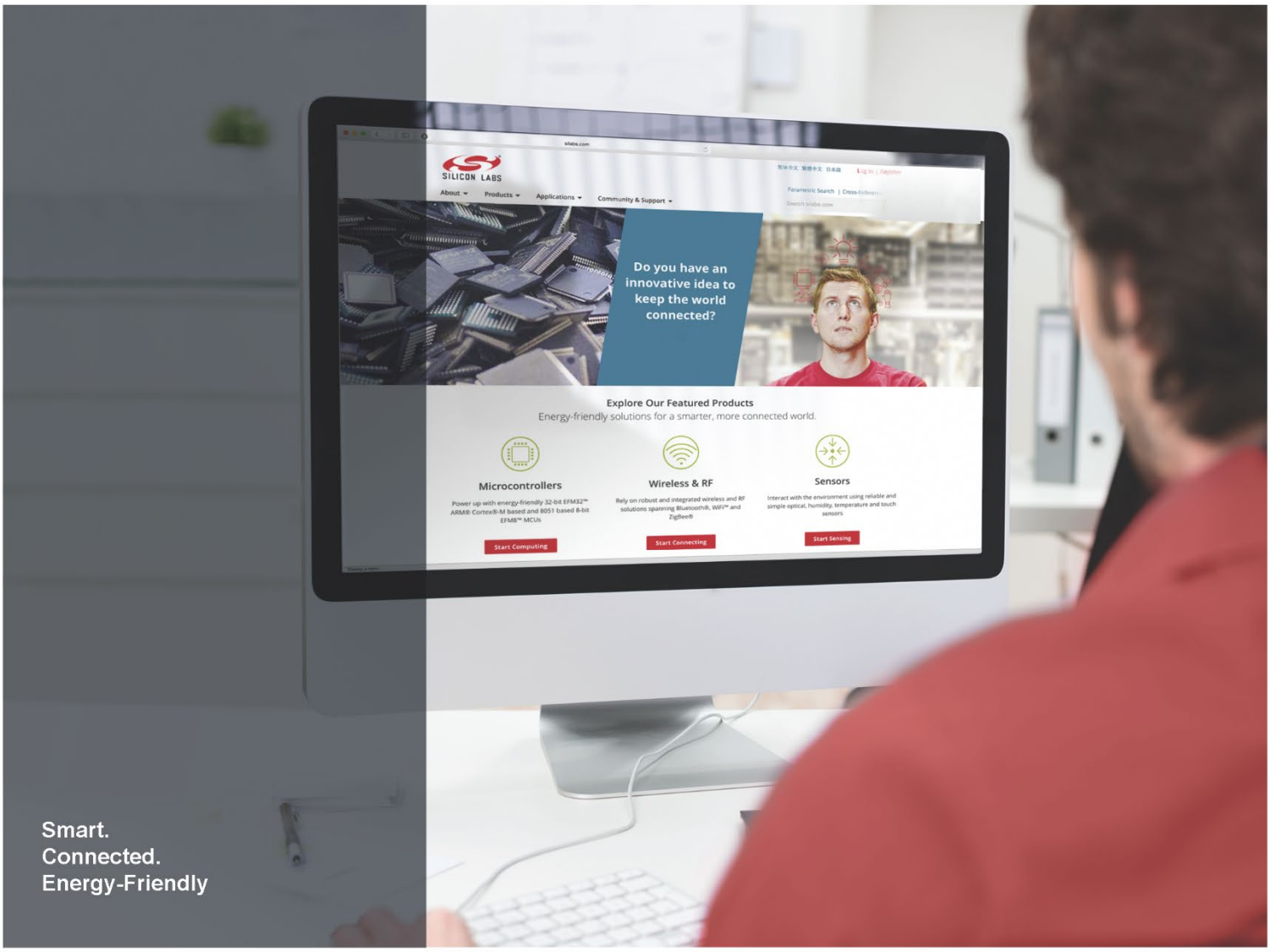
For further assistance, you can contact Silicon Labs Technical Support here.

10 RS9116 AA0 module Revision History

Revision No.	Version No.	Date	Changes
1	1.0	April, 2019	Initial version
2	1.0.1	May, 2019	• Updated host based schematics. Combined SDIO, SPI & UART host interfaces into one schematic.Combined USB and USB-CDC host interfaces into one schematic. • Updated 32 Khz external oscillator specifications • Updated antenna layout recommendations for single band antenna • Updated the Schematics for UART_RTS and UART_CTS Pin correction.
3	1.0.2	May, 2019	Removed 32KHz XTAL Pins and used UULP GPIO for feeding in the External Clock. Updated the below sections for the same • Pinout Description. • Specifications • Reference Schematics
4	1.0.3	July, 2019	• Corrected the description of 32KHz external clock in Specifications section, • Moved AVDD_1P9_3P3 to NC. • Renamed LP_WAKEUP to LP_WAKEUP_IN and changed its description in Pinout section. • Added host detection details and updated network processor memory details in Detailed description. • Corrected the initial state of SDIO_D3 to pullup and SDIO_D2 to HighZ.
5	1.0.4	November, 2019	Bluetooth ACI specs corrected (earlier version shows under Typ - should have been under “Min”)
6	1.0.5	July, 2020	• Added note about voltage applied on external Buck Regulator for Typical Current Consumption at 1.85V. • Updated Applications section. • Updated 40 MHz Clock specifications. • Updated LED0 software configuration note for ULP_GPIO_8 under Pin Description. • Mentioned need for weak pull up resistor under Pin Description to use Wake-on-Wireless feature on ULP_GPIO_6. • Updated "Digital Input Output Signals" to separate readings at 3.3V and 1.8V. • Included TELEC certification details and updated Module Marking Information. • Updated Wireless Co-Existence modes in Features list. • The number of center roles supported by BLE changed from 8 to 6.

Revision No.	Version No.	Date	Changes
			• Added a note under Pin Description regarding functionalities that are available on multiple Pins, and their proper usage. Eg. SLEEP_IND_FROM_DEV • Updated Generic PCB Layout Guidelines. • Updated Power Sequence Diagrams under DC Characteristics for POC_IN and POC_OUT. • Features list updated. • Reflow profile diagram updated. • Updated Typical values for BLE ACI characteristics. • Updated GPIO pin descriptions.
7	1.0.6	August, 2020	• Updated Features List, removed redundant information. • Updated Applications, and Software Architecture Diagrams. • Updated pin descriptions - ULP_GPIO_0 and ULP_GPIO_6. • Updated Software section with latest information. • Rebranded to Silicon Labs.
8	1.0.7	September, 2020	• Updated Device Information with new nomenclature to include Silicon revision, and firmware version. • Updated schematics to include the new nomenclature. • SoC Ordering information updated with new OPNs; Device Nomenclature diagram updated.

Table 43 Revision History



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