

Evaluating the **ADM2563E/ADM2863E** 3 kV RMS/5.7 kV RMS, 500 kbps Signal and Power Isolated RS-485 Transceivers with ± 15 kV IEC ESD

FEATURES

Simplified evaluation of the [ADM2563E](#) and the [ADM2863E](#) 500 kbps, signal and power isolated RS-485 transceivers
2-layer PCB compliant to EN 55032/CISPR 32 Class B radiated emissions
Footprint for 10.15 mm × 10.05 mm, 28-lead SOIC_W_FP package with >8.0 mm creepage and clearance
On-board [ADP7104](#) LDO regulator with jumper options for simplified evaluation in 5 V or 3.3 V configuration
Flexible, low voltage V_{IO} supply rail for interfacing with I/O nodes as low as 1.7 V
ESD protection on RS-485 A, B, Y, and Z pins
 $\geq \pm 12$ kV IEC61000-4-2 contact discharge
 $\geq \pm 15$ kV IEC61000-4-2 air discharge
SMA connector for TxD input signal
Optional on-board [LTC6900](#) oscillator for providing TxD signal
Screw terminal blocks for connecting power, digital signals, and RS-485 signals
Jumper selectable enable and disable for digital input signals
Resistors and footprints for loopback test and termination
Test points for measuring all signals

EVALUATION KIT CONTENTS

EVAL-ADM2563EEBZ or EVAL-ADM2863EEBZ

EQUIPMENT NEEDED

Oscilloscope
Signal generator
3 V to 5.5 V supply
1.62 V to 5.5 V supply

DOCUMENTS NEEDED

[ADM2563E](#) data sheet
[ADM2863E](#) data sheet

GENERAL DESCRIPTION

The EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ allow for the simplified, efficient evaluation of the 3 kV rms [ADM2563E](#) and the 5.7 kV rms [ADM2863E](#) 500 kbps signal and power isolated, full-duplex RS-485 transceivers, respectively.

The [ADM2563E](#) and the [ADM2863E](#) each feature an integrated, isolated, dc-to-dc converter that provides power to the isolated side of the device with no additional ICs required.

An on-board [ADP7104](#) low dropout (LDO) regulator accepts an input voltage of 3.3 V to 20 V and regulates the voltage to a selectable 3.3 V or 5 V supply for the V_{CC} pin of the [ADM2563E](#) and the [ADM2863E](#). The LDO regulator can be bypassed to power the V_{CC} pin of the [ADM2563E](#) and the [ADM2863E](#) directly.

A screw terminal block on the evaluation boards allows connection to the flexible V_{IO} logic supply pin of the [ADM2563E/ADM2863E](#). This connection allows the [ADM2563E/ADM2863E](#) to operate with a digital input/output (I/O) voltage from 1.7 V to 5.5 V, which enables communication with nodes using either a 1.8 V or 2.5 V power supply. The V_{IO} pin can also be supplied from the [ADP7104](#) regulated supply.

The EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ come with options to evaluate the [ADM2563E](#) or the [ADM2863E](#) in an individual system. Digital and RS-485 bus signals are easily accessible via the screw terminal blocks on each evaluation board. Each digital input is configured via the on-board jumper options.

Alternative methods can provide the transmit data input (TxD) signal to the [ADM2563E](#) or the [ADM2863E](#). An [LTC6900](#) oscillator is included on each evaluation board and can be optionally configured to provide a clock signal for the TxD digital input within a 10 kHz to 250 kHz range. For optimal signal integrity, use the on-board Subminiature Version A (SMA) connector to connect an external data signal.

The EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ footprint for the full-duplex, isolated RS-485 transceivers is in a 10.15 mm × 10.05 mm, 28-lead, small outline, wide body with fine pitch (SOIC_W_FP) package. The EVAL-ADM2563EEBZ board is populated with the [ADM2563E](#) 3 kV rms, isolated RS-485 transceiver. The EVAL-ADM2863EEBZ is populated with the [ADM2863E](#) 5.7 kV rms, isolated RS-485 transceiver. The two evaluation boards differ only by the isolated RS-485 device populated on U3.

For full details on the [ADM2563E](#) or the [ADM2863E](#), see the [ADM2563E](#) or the [ADM2863E](#) data sheet, which must be consulted in conjunction with this user guide when using the EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ.

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REVISION HISTORY

6/2020—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPHS

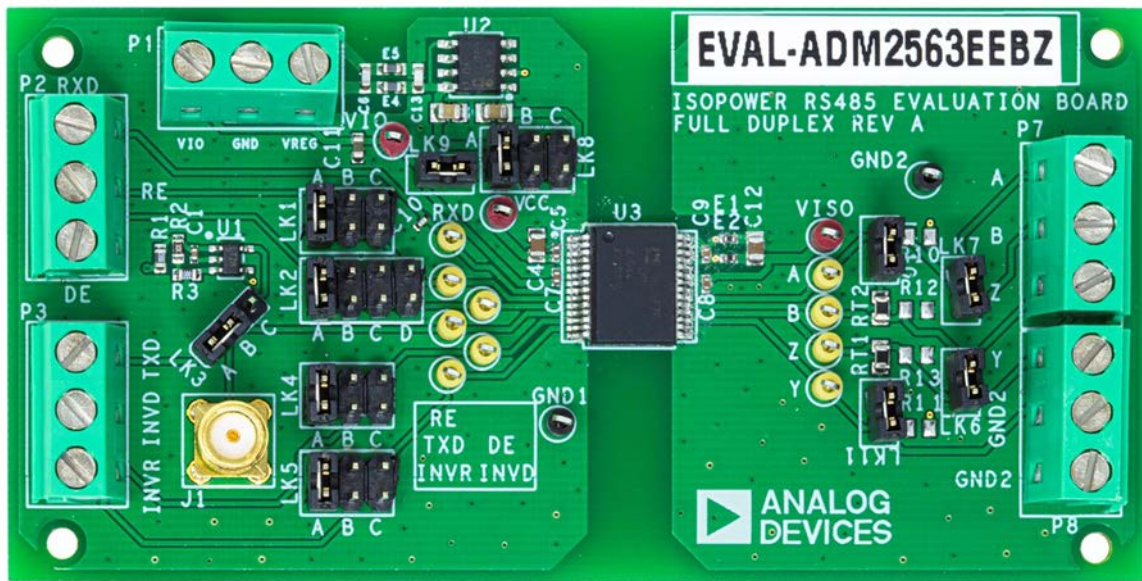


Figure 1. EVAL-ADM2563EEBZ

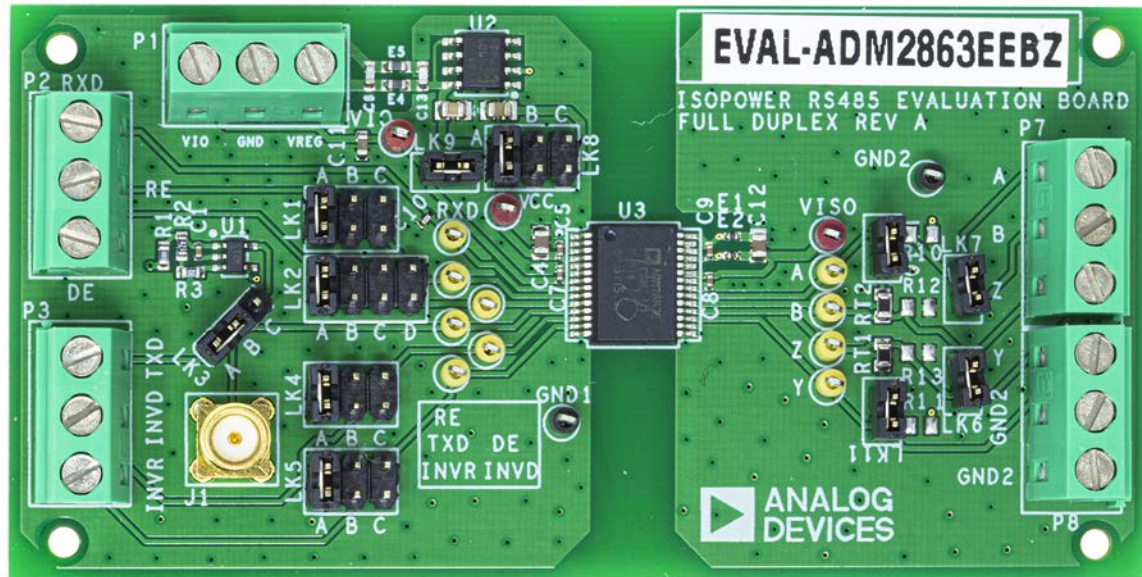


Figure 2. EVAL-ADM2863EEBZ

EVALUATION BOARD HARDWARE

SETTING UP THE EVALUATION BOARD

The EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ are powered via the VREG_IN connection on the P1 screw terminal connector. The voltage connected to the VREG_IN on the P1 screw terminal connector can either be regulated or connected directly to the V_{CC} pin of the [ADM2563E/ADM2863E](#). Insert the LK8 jumper into Position A to power the V_{CC} pin of the [ADM2563E/ADM2863E](#) directly from the VREG_IN terminal.

The on-board [ADP7104](#) voltage regulator accepts a voltage from 5.5 V to 20 V on the VREG_IN terminal and can supply either a 3.3 V or a 5 V regulated supply to the V_{CC} pin of the [ADM2563E/ADM2863E](#). Select the regulated voltage via the LK8 jumper. Insert the LK8 jumper into Position B to operate the device with a regulated V_{CC} supply of 3.3 V. Insert the LK8 jumper into Position C to operate the [ADM2563E/ADM2863E](#) with a regulated V_{CC} supply of 5.5 V. The V_{CC} pin is fitted with a 10 μF decoupling capacitor (C4) and a 0.1 μF decoupling capacitor (C5).

To power the V_{IO} supply pin of the [ADM2563E/ADM2863E](#) from the VCC terminal block and operate the V_{IO} and V_{CC} supply pins at the same voltage, insert Jumper LK9. To power the V_{IO} supply pin from a separate VIO terminal block, remove Jumper LK9.

In this configuration, the VIO input of the P1 screw terminal

connector can be connected to a separate, low voltage logic supply between 1.7 V and 5.5 V. A 0.1 μF decoupling capacitor (C7) is fitted at the connector between the [ADM2563E/ADM2863E](#) V_{IO} pin and GND₁ pins. A footprint for a second 10 μF capacitor (C11) can be used to provide additional decoupling capacitance to the V_{IO} pin.

The V_{SEL} pin of the [ADM2563E/ADM2863E](#) selects the isolated supply voltage for the RS-485 transceiver. To configure the device to output a 3.3 V isolated supply voltage, connect the [ADM2563E/ADM2863E](#) V_{SEL} pin to the GND_{ISO} pins. To configure the device to output a 5 V isolated supply voltage, connect the [ADM2563E/ADM2863E](#) V_{SEL} pin to the V_{ISOOUT} pin. The R6 and R7 resistors can be inserted or removed as needed to make these connections. Avoid inserting the R6 and R7 resistors together because this connection shorts the V_{ISOOUT} power pin to the GND_{ISO} ground pin.

See Table 1 and Table 2 for more details on the jumper and power supply connections. The corresponding labeled test points allow power supply monitoring on the EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ with the probe reference connected to ground.

Table 1. Jumper Configurations

Link	Jumper Connection	Description
LK1	A	Connects the ADM2563E/ADM2863E $\overline{\text{RE}}$ input pin to the V _{IO} pin. This setting disables the receiver.
	B	Connects the ADM2563E/ADM2863E $\overline{\text{RE}}$ input pin to the $\overline{\text{RE}}$ terminal on the P2 screw terminal connector.
	C	Connects the ADM2563E/ADM2863E $\overline{\text{RE}}$ input pin to the GND ₁ pins. This setting enables the receiver.
LK2	A	Connects the ADM2563E/ADM2863E DE input pin to the V _{IO} pin. This setting enables the driver.
	B	Connects the ADM2563E/ADM2863E DE input pin to the DE terminal on the P2 screw terminal connector.
	C	Connects the ADM2563E/ADM2863E DE input pin to the GND ₁ pins. This setting disables the driver.
	D	Connects the ADM2563E/ADM2863E DE input pin to the $\overline{\text{RE}}$ input signal. Therefore, the input for both $\overline{\text{RE}}$ and DE is set by the LK1 jumper. This setting ensures that when the driver is enabled, the receiver is disabled, or when the driver is disabled, the receiver is enabled.
LK3	A and B	Connects the ADM2563E/ADM2863E TxD input pin and J1 SMA connector to the TxD terminal on the P3 screw terminal connector.
	B and C	Connects the ADM2563E/ADM2863E TxD input pin and J1 SMA connector to the LTC6900 oscillator output. To configure the oscillator frequency to be between 10 kHz and 250 kHz, set the R2 and R3 resistors. Only use this option when the V _{IO} supply input is between 3 V to 5.5 V.
	Not inserted	Connects the ADM2563E/ADM2863E TxD input pin to the J1 SMA connector.
LK4	A	Connects the ADM2563E/ADM2863E INVD input pin to the V _{IO} pin. This setting is used for normal driver operation.
	B	Connects the ADM2563E/ADM2863E INVD input pin to the INVD terminal on the P3 screw terminal connector.
	C	Connects the ADM2563E/ADM2863E INVD input pin to the GND ₁ pins. This setting enables the driver inversion feature.
LK5	A	Connects the ADM2563E/ADM2863E INVR input pin to the V _{IO} pin. This setting is used for normal receiver operation.
	B	Connects the ADM2563E/ADM2863E INVR input pin to the INVR terminal on the P3 screw terminal connector.
	C	Connects the ADM2563E/ADM2863E INVR input pin to the GND ₁ pins. This setting enables the receiver inversion feature.

Link	Jumper Connection	Description
LK6	Inserted	Connects the ADM2563E/ADM2863E Pin B to Pin Z.
	Not inserted	Disconnects the ADM2563E/ADM2863E Pin B from Pin Z.
LK7	Inserted	Connects the ADM2563E/ADM2863E Pin A to Pin Y.
	Not inserted	Disconnects the ADM2563E/ADM2863E Pin A from Pin Y.
LK8	A	Connects the ADM2563E/ADM2863E V _{CC} pin to the VREG_IN terminal on the P1 screw terminal connector. This option bypasses the ADP7104 regulator and allows an external power supply to connect directly to the ADM2563E/ADM2863E V _{CC} pin.
	B	Powers the ADM2563E/ADM2863E V _{CC} pin with a regulated 3.3 V power supply from the ADP7104. The ADP7104 must be supplied with at least 4 V through the VREG_IN terminal on the P1 screw terminal connector.
	C	Powers the ADM2563E/ADM2863E V _{CC} pin with a regulated 5 V power supply from the ADP7104. The ADP7104 must be supplied with at least 6 V through the VREG_IN terminal on the P1 screw terminal connector.
LK9	Inserted	Connects the ADM2563E/ADM2863E V _{CC} pin to the V _{IO} pin.
	Not inserted	Disconnects the ADM2563E/ADM2863E V _{CC} pin from the V _{IO} pin. The V _{IO} pin is powered from the V _{IO} terminal on the P1 connector.
LK10	Inserted	Connects the 120 Ω RT2 termination resistor between the ADM2563E/ADM2863E Pin A and Pin B.
	Not inserted	Disconnects the 120 Ω RT2 termination resistor between the ADM2563E/ADM2863E Pin A and Pin B.
LK11	Inserted	Connects the 120 Ω RT1 termination resistor between the ADM2563E/ADM2863E Pin Y and Pin Z.
	Not inserted	Disconnects the 120 Ω RT1 termination resistor between the ADM2563E/ADM2863E Pin Y and Pin Z.

Table 2. Input Supply Configurations

Jumper LK8	V _{SEL} Pin	VREG_IN Input Voltage Range	V _{CC} Supply	V _{ISO} Supply
A	Low	Not used	Power V _{CC} directly on the P1 screw terminal connector with a supply voltage between 3 V and 5.5 V	3.3 V isolated output
	High	Not used	Power V _{CC} directly on connector the P1 screw terminal connector with a supply voltage between 4.5 V and 5.5 V	5 V isolated output
B	Low	4 V to 20 V	Regulator provides 3.3 V supply to V _{CC}	3.3 V isolated output
	High	Invalid condition, 5 V isolated output is not supported with V _{CC} < 4.5 V		
C	Low	6 V to 20 V	Regulator provides 5 V supply to V _{CC}	3.3 V isolated output
	High	6 V to 20 V	Regulator provides 5 V supply to V _{CC}	5 V isolated output

INPUT AND OUTPUT CONNECTIONS

Digital input and output signals are connected via the P2 and P3 screw terminal connectors to allow wire connections from the EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ to a signal generator. The evaluation boards include screw terminals for the transmit data input (TxD), receiver data output (RxD), receiver enable (RE), and driver enable (DE), driver inversion (INVD) and receiver inversion (INVR) signal. Alternatively, jumper connections can connect these signals to the V_{IO} pin or GND₁ pins of the ADM2563E/ADM2863E (see Table 1).

Connections to the RS-485 bus are made via the P7 and P8 screw terminal connectors. The EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ each have four bus input and output signals: Signal A for noninverting input signals, Signal B for inverting input signals, Signal Y for noninverting output signals, and Signal Z for inverting output signals. The bus cables also include a common ground connection and can be connected to the P8 screw terminal connector of the evaluation boards. Test points are available on the evaluation boards and are appropriately labeled for all digital and bus input and output signals.

RADIATED EMISSIONS

The EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ are 2-layer printed circuit boards (PCB) that meet the EN 55032 Class B radiated emissions requirements under full load while operating at the maximum data rate of 500 kbps. Advances in the isolated dc-to-dc converter eliminate the need for complex mitigation techniques, such as edge guarding and embedded stitching capacitance. Two 0402, surface-mount ferrite beads suppress high frequency noise and minimize the amount of noise radiated by the ADM2563E/ADM2863E device. The recommended ferrite beads have a high impedance in the 100 MHz to 1 GHz frequency range (see Table 3). The EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ is populated with the BLM15HD182SN1 ferrite beads on E1 and E2.

Table 3. Recommended Surface-Mount Ferrite Beads

Manufacturer	Device Number
Murata Electronics	BLM15HD182SN1
Taiyo Yuden	BKH1005LM182-T

To maximize the margin to the EN 55032 Class B specification, adhere to the following guidelines:

- Ensure that the decoupling capacitors are placed as close to the corresponding ADM2563E/ADM2863E pins as possible.
- Place a 10 μF capacitor (C4) and a 0.1 μF capacitor (C5) between the ADM2563E/ADM2863E V_{CC} pin and GND_1 pins.
- Place a 0.1 μF capacitor (C7) between the ADM2563E/ADM2863E V_{IO} pin and GND_1 pins.
- Connect the ADM2563E/ADM2863E Pin 24, Pin 26, and Pin 28 together to form a single GND_{ISO} net. Connect this net to the GND_2 net through the E1 ferrite bead.
- Place a 0.1 μF capacitor (C9) between the ADM2563E/ADM2863E V_{ISOOUT} supply pin and the GND_{ISO} net.
- Connect the ADM2563E/ADM2863E V_{ISOOUT} pin to the V_{ISOIN} pin through the E2 ferrite bead.
- Place a 10 μF capacitor (C12) and a 0.1 μF capacitor (C8) between the ADM2563E/ADM2863E V_{ISOIN} supply pin and the GND_2 pin (Pin 22).
- Remove any metal planes or floods from the area around or under the GND_{ISO} net and V_{ISOOUT} net.

The EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ is designed according to these guidelines and meets EN 55032 Class B requirements with margin. See Figure 3, Figure 9, and Figure 10 for further details on the recommended PCB layout.

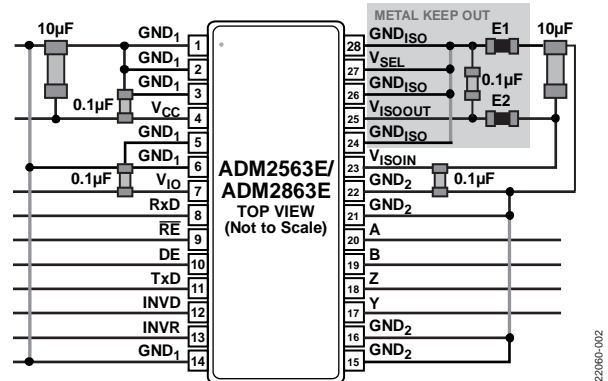


Figure 3. Layout Guidelines to Achieve EN 55032 Class B Requirements

EN 55032 RADIATED EMISSIONS TEST RESULTS

The EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ meets the EN 55032 and CISPR 32 Class B requirements for radiated emissions with margin. The testing was performed in worst case conditions under a full 54 Ω load with both the transmitter and receiver switching at 500 kbps. Figure 4 shows the results obtained in a 10 meter, semianechoic chamber, which are below the Class B limit.

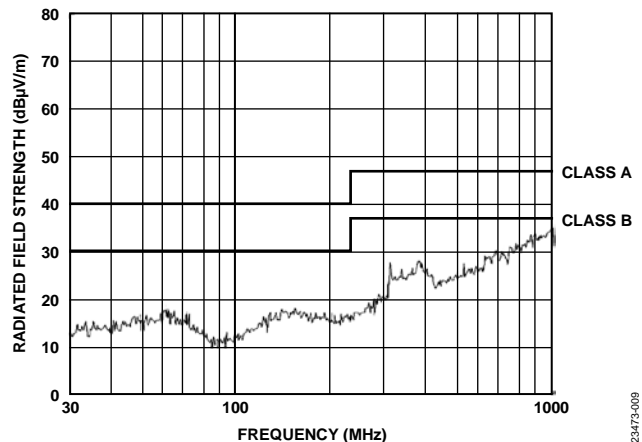


Figure 4. CISPR 32/EN 55032 Radiated Emissions Test Results

OTHER BOARD COMPONENTS

The EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ has footprints for the RT1 and RT2 termination resistors. The 120 Ω termination resistors are fitted to the evaluation boards, but these resistors can be removed or replaced with resistors of a different values as needed. Insert the LK11 jumper to add a 120 Ω load to the RS-485 driver. When LK6, LK7, and LK10 are inserted, an additional 120 Ω termination resistor is connected resulting in a 60 Ω load to the RS-485 driver.

Biasing Resistors for Bus Idle Fail-Safe

The [ADM2563E/ADM2863E](#) each have a built in receiver fail-safe for the bus idle condition, but there are footprints on the evaluation boards for fitting the R10 and R11 pull-up resistors to the V_{ISO} supply on the [ADM2563E/ADM2863E](#) Pin A and Pin Y, as well as the R12 and R13 pull-down resistors to the GND_2 supply pins on Pin B and Pin Z. These resistors can be fitted if the user is connecting to other devices that require external biasing resistors on the bus. The exact value required for a 200 mV minimum differential voltage in bus idle condition depends on the minimum supply voltage and the termination scheme. For 5 V transceiver operation, 1140 Ω is recommended. For 3.3 V transceiver operation, 900 Ω is recommended.

See the [AN-960 Application Note](#) for more information about the bus idle fail-safe.

On-Board LTC6900 Oscillator

An [LTC6900](#) oscillator is provided on the EVAL-ADM2563EEBZ and the EVAL-ADM2863EEBZ to allow efficient evaluation of the devices without the need for an external signal source.

To use the [LTC6900](#) oscillator for evaluation, insert the LK3 jumper between Position B and Position C. This setting connects the oscillator output ([LTC6900](#)) to the [ADM2563E/ADM2863E](#) TxD input pin.

The R2 and R3 resistors configure the switching frequency of the oscillator within the 10 kHz to 250 kHz range. Use the following equation to calculate the frequency:

$$f_{osc} = 10 \text{ MHz} \left(\frac{20 \text{ k}\Omega}{10(R2 + R3)} \right), 80 \text{ k}\Omega \leq (R2 + R3) \leq 2 \text{ M}\Omega$$

where f_{osc} is the output frequency of the [LTC6900](#) oscillator.

The [LTC6900](#) oscillator is powered from the V_{IO} supply, and must only be used when the V_{IO} supply voltage is between 2.7 V and 5.5 V. The [LTC6900](#) oscillator can be removed from the V_{IO} supply by removing the R1 0 Ω resistor.

ADP7104 LDO Regulator

The EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ features an on-board [ADP7104](#) LDO regulator that allows flexible power supply configurations during evaluation.

To use the on-board LDO regulator, insert the LK8 jumper into Position B or Position C. This setting connects the regulator output to the V_{CC} pin of the [ADM2563E/ADM2863E](#). In this configuration, power must be supplied to the VREG_IN input on the P1 screw terminal connector.

The [ADP7104](#) LDO regulator can be configured to provide regulated 3.3 V or 5 V power to the V_{CC} pin of the [ADM2563E/ADM2863E](#) via the LK8 jumper. When using the [ADP7104](#) regulator, insert the LK8 jumper at Position C to provide a regulated 5 V power supply to the V_{CC} pin of the [ADM2563E/ADM2863E](#). Insert the LK8 jumper at Position B to provide a 3.3 V power supply to the V_{CC} pin of the [ADM2563E/ADM2863E](#). Note that when LK8 is inserted at Position B, 5 V transceiver operation is not supported.

Insert the LK8 jumper into Position A to bypass the regulator and power the [ADM2563E/ADM2863E](#) directly from the VREG_IN input on the P1 screw terminal connector. In this configuration, the VREG input on the P1 screw terminal connector supports a voltage range of 3 V to 5.5 V.

Table 2 lists the supported power supply configurations and the associated jumper configurations.

RS-485 TRANSCEIVER LOOPBACK TEST

To set up a loopback test with the EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ, close the LK6 and LK7 jumpers. The details of this test are shown in Table 2 and in Figure 5. A signal generator is connected to the TxD pin, which allows verification of the bus signals and the receiver output. Note that the jumper position for LK1 is Position C, LK2 is Position A, LK4 is Position C, and LK5 is Position C on the evaluation boards. See Table 2 for the jumper configurations required for different input supply configurations. The LK10 and LK11 jumpers can be inserted to terminate the transmitter and the receiver with 120 Ω resistors. Connect both these jumpers while each evaluation board is configured for the loopback test to ensure that the driver is terminated with a standard RS-485 load of 60 Ω (bus terminated at both ends by 120 Ω).

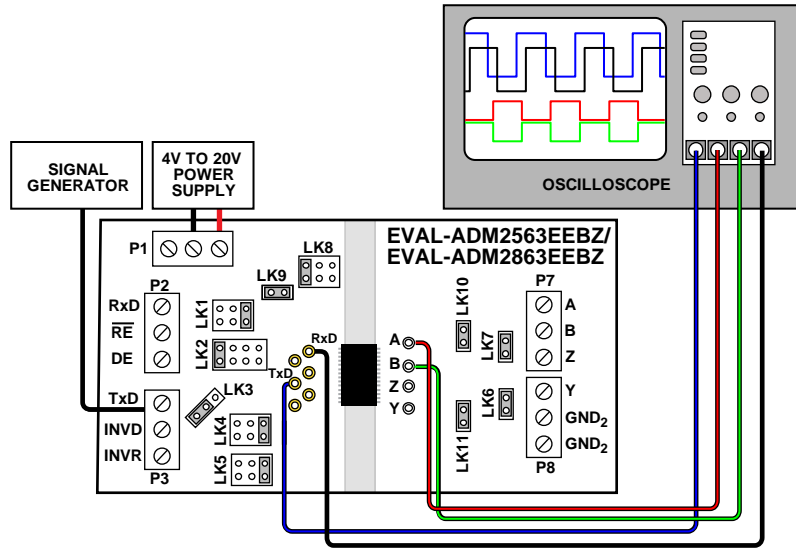


Figure 5. Full-Duplex RS-485 Transceiver Loopback Test

23473-004

IEC 61000-4-2 ELECTROSTATIC DISCHARGE (ESD) PROTECTION

The EVAL-ADM2563EEBZ or the EVAL-ADM2863EEBZ is tested to achieve protection against IEC 61000-4-2 ESD to $\geq \pm 12$ kV (contact) and $\geq \pm 15$ kV (air) on Pin A, Pin B, Pin Y, and Pin Z of the [ADM2563E/ADM2863E](#).

The IEC 61000-4-2 ESD standard describes testing using two coupling methods known as contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT).

During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT.

During testing, Pin A, Pin B, Pin Y, and Pin Z of the [ADM2563E/ADM2863E](#) are subjected to at least 10 positive and 10 negative single discharges with a 1 sec interval between each pulse. The highest specified IEC 61000-4-2 ESD test is Level 4, which defines a contact discharge voltage of ± 8 kV and an air discharge voltage of $\geq \pm 15$ kV.

Figure 6 shows the ESD waveform for an 8 kV contact discharge current waveform, as described in the [ADM2563E/ADM2863E](#) data sheet, which has a peak current (I_{PEAK}) of 30 A. IEC 61000-4-2 waveform parameters include rise times (t_R) of < 1 ns and pulse widths of ~ 60 ns.

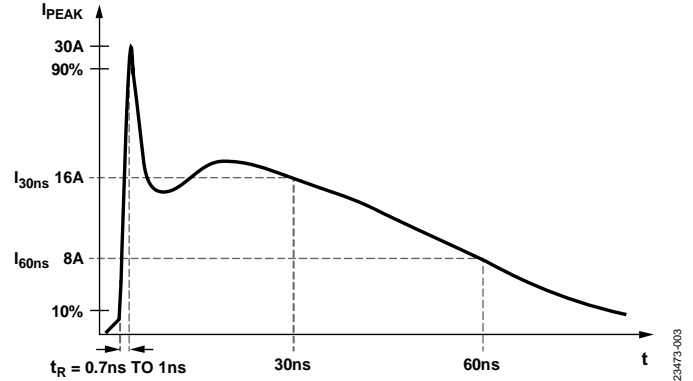


Figure 6. IEC 61000-4-2 ESD Waveform (8 kV)

EVALUATION BOARD SCHEMATICS AND ARTWORK

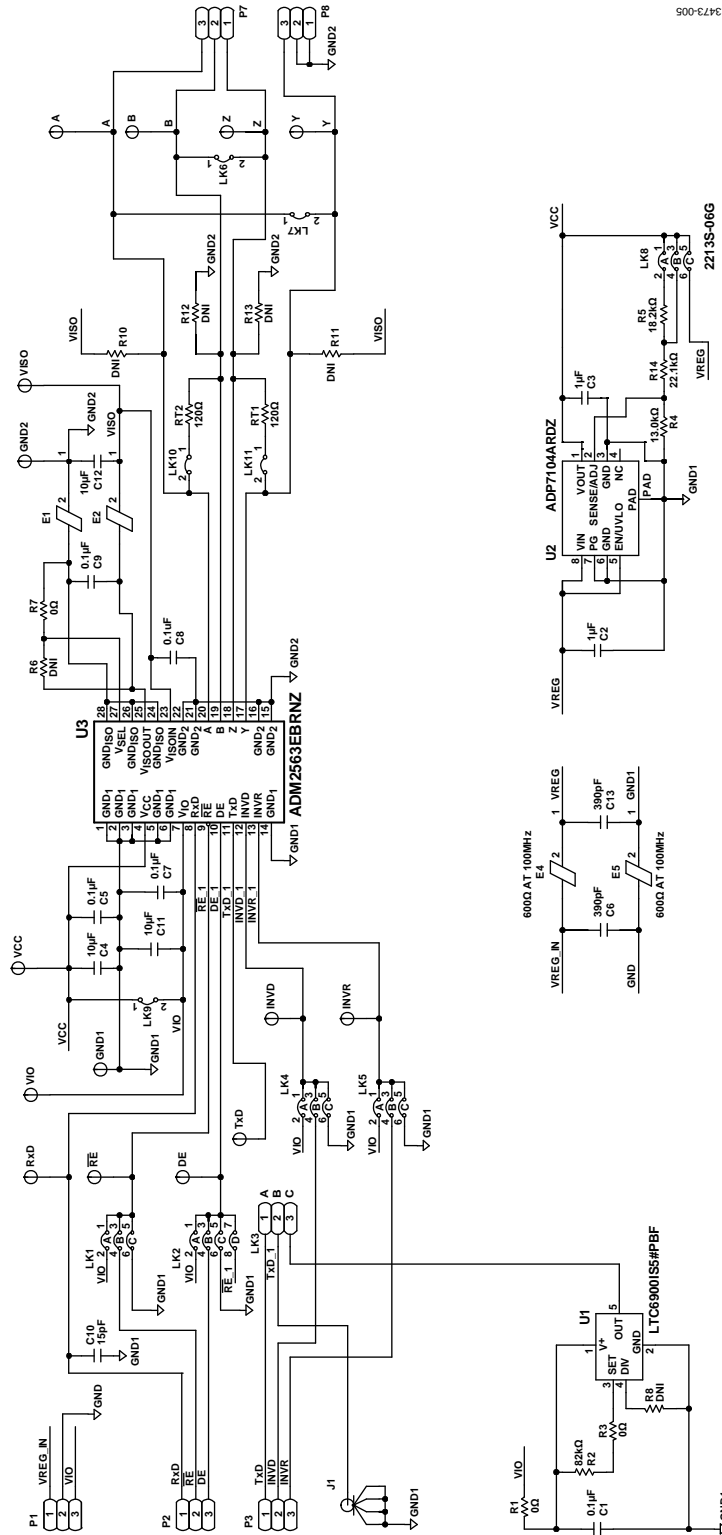


Figure 7. EVAL-ADM2563EEBZ Schematic

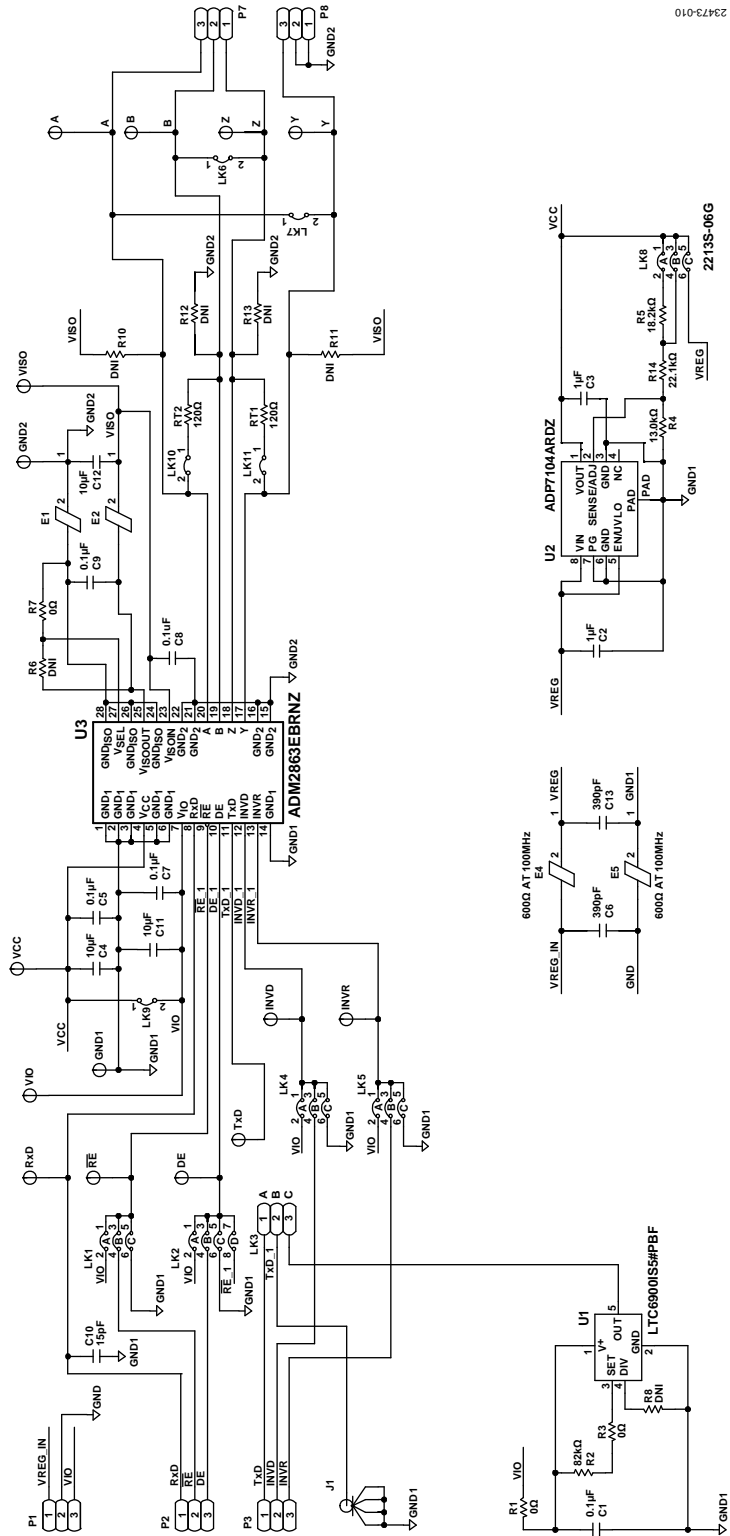


Figure 8. EVAL-ADM2863EEBZ Schematic

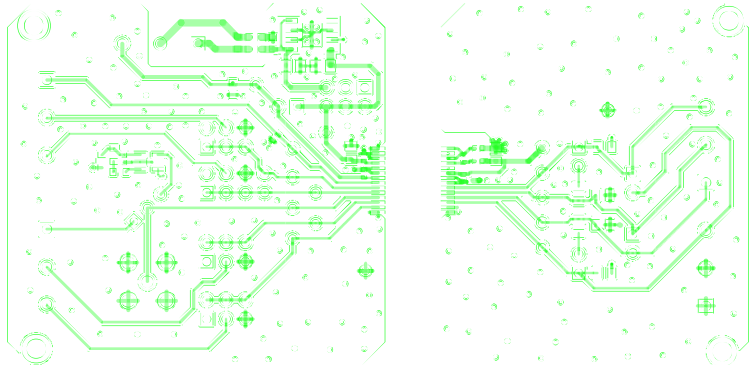


Figure 9. EVAL-ADM2563EEBZ/EVAL-ADM2863EEBZ Component Side, Layer 1

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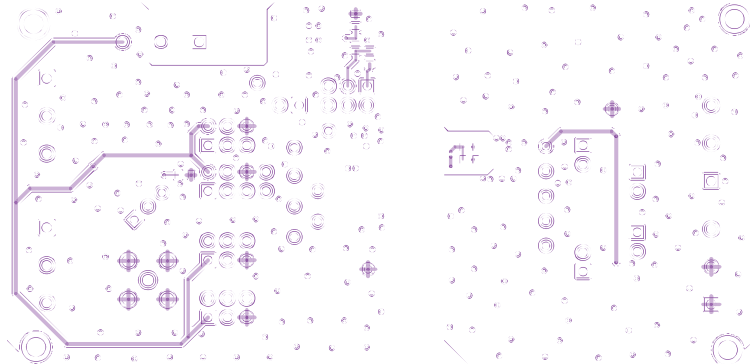


Figure 10. EVAL-ADM2563EEBZ/EVAL-ADM2863EEBZ, Layer 2

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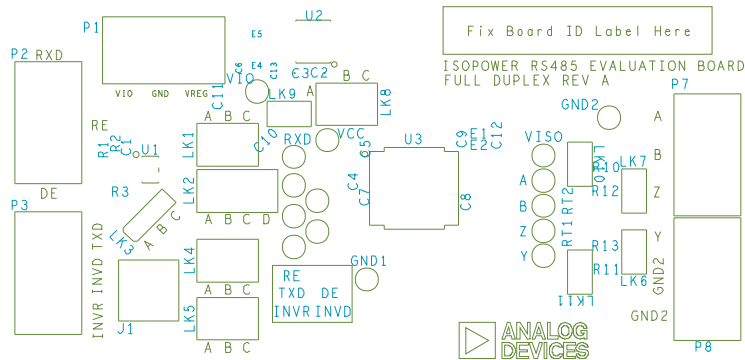


Figure 11. EVAL-ADM2563EEBZ/EVAL-ADM2863EEBZ, Silkscreen

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ORDERING INFORMATION

BILL OF MATERIALS

Table 4. EVAL-ADM2563EEBZ/EVAL-ADM2863EEBZ Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Part Number
10	A, B, DE, INVD, INVR, RE, RxD, TxD, Y, Z	Test points, yellow	Keystone Electronics	36-5004-ND
5	C1, C5, C7, C8, C9	Capacitors, 0.1 μ F, 0402	Kemet	C0402C104K4RACTU
2	C2, C3	Capacitors, 1 μ F, 0805	Murata	GCM21BR71E105KA56L
2	C4, C12	Capacitors, 10 μ F, 0805	TDK	C2012X5R1E106K085AC
2	C6, C13	Capacitors, 390 pF, 0603	AVX Corporation	0603YC391KAT2A
1	C10	Capacitor, 15 pF, 0402	Murata	GCM1555C1H150FA16D
1	C11	Capacitor, 10 μ F, 0603	TDK	C1608X5R1A106M080AC
2	E1, E2	Ferrite beads, 0402	Murata	BLM15HD182SN1D
2	E4, E5	Ferrite beads, 0603, 600 Ω at 100 MHz	Murata	BLM18HE601SN1D
2	GND1, GND2	Test points, black	Components Corporation	TP-105-01-00
1	J1	Coaxial, straight SMA connector	TE Connectivity	5-1814832-1
4	LK1, LK4, LK5, LK8	6-pin (3 \times 2), 0.1 inch header and shorting blocks	Multicomp	2213S-06G
1	LK2	8-pin (4 \times 2), 0.1 inch header and shorting block	Multicomp	2213S-08G
1	LK3	3-pin (3 \times 1), 0.1 inch header and shorting block	Molex	22-28-4033
5	LK6, LK7, LK9, LK10, LK11	2-pin (1 \times 2), 0.1 inch header and shorting blocks	Harwin	M20-9990246
5	P1 to P3, P7, P8	Three-way screw terminal connectors	Wurth Elektronik	691131710003
3	R1, R3, R7	Resistors, 0 Ω , 0603	Vishay	CRCW0603000ZRT1
1	R8	Resistor, do not install (DNI), 0603	Not applicable	Not applicable
1	R2	Resistor, 82 k Ω , 0603	Multicomp	MC0063W0603182K
1	R4	Resistor, 13 k Ω , 0603	Panasonic	ERJ-3EKF1302V
1	R5	Resistor, 18.2 k Ω , 0603	Panasonic	ERJ-3EKF1822V
1	R6	Resistor, DNI, 0603	Not applicable	Not applicable
1	R14	Resistor, 22.1 k Ω , 0603	Panasonic	ERJ-3EKF2212V
4	R10, R11, R12, R13	Resistors, DNI, 0805	Not applicable	Not applicable
2	RT1, RT2	Resistors, 120 Ω , 0805	Panasonic	ERJ-P6WF1200V
1	U1	Low power, 1 kHz to 20 MHz oscillator	Analog Devices, Inc.	LTC6900IS5#PBF
1	U2	Low noise CMOS LDO	Analog Devices	ADP7104ARDZ-R7
1	U3 ¹	500 kbps 3 kV signal and power isolated RS-485 transceiver	Analog Devices	ADM2563EEBZ
1	U3 ¹	500 kbps 5.7 kV signal and power isolated RS-485 transceiver	Analog Devices	ADM2863EEBZ
3	VCC, VIO, VISO	Test points, red	Components Corporation	TP-105-01-02

¹ The ADM2563E is the device for the EVAL-ADM2563EEBZ, and the ADM2863E is the device for the EVAL-ADM2863EEBZ board.

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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