ANALOG DEVICES

1986 Update And Selection Guide

Data Acquisition Databook Update And Selection Guide

ANALOG DEVICES

How to Use Data in This Databook

THIS VOLUME

A supplement to Volume 1984 Data Acquisition Databook. It will help you solve problems in data acquisition system design with Analog Devices ICs, modules, and subsystems. It contains 3 categories of useful information:

TECHNICAL DATA on more than 76 new IC products and 14 new modules and subsystems, introduced since publication of the Databook.

SELECTION GUIDES, with tabular data, classifying and comparing all products recommended for new designs. When you've chosen products to look at more closely, the handy indexes will help you find complete technical data, either in this volume (for new products) or Volumes I & II of the Databook (for other current products).

INDEXES, updated to help you find what you're looking for in these volumes.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index beginning on page 1-20 in the back of the book and look up the model number. You will find the Volume, Section, and Page location of data sheets bound into Volume I, Volume II, and this volume.

If you're looking for a form-and-function-compatible version of an integrated circuit or hybrid product originally brought to market by some other manufacturer (second source), add our "AD" prefix (or "ADSP", for digital signal processing ICs) and look it up in the index.

IF YOU DON'T KNOW THE MODEL NUMBER

Find the function in the Selection Guides Table of Contents on page 2–1 of this volume. Turn directly to the indicated page number. You will find one or more functional Selection Guides and comparative spec tables. The Selection Guide and/or spec tables will help you find the products that come closest to satisfying your need. Use them to compare all products in the category by salient criteria, no matter which Volume the technical data may reside in. Then refer to the Volume-Section-Page locations to find specific data sheet information.

THIS BOOK IS NOT A SUBSTITUTE FOR THE 1984 DATABOOK

There is much useful technical, specification, classification, and ordering information, in addition to product data, in the 1906 pages of Volumes I and II. If you don't have a set and would like to receive one, request it from any Analog Devices office listed in the Worldwide Service Directory, in the last pages of this Volume.

IF YOU CAN'T FIND IT . . . ASK!

See the Worldwide Service Directory, 1–18 and 1–19 at the back of this volume.

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Data Acquisition Databook Update and Selection Guide 1986

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General Introduction

Analog Devices designs, manufactures and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I^2L, CMOS, BiMOS and hybrid integrated circuits—and assembled products in the form of potted modules, printed-circuit boards and instrument packages.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. More than twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data acquisition products.

MAJOR PROGRESS

Since our two-volume 1984 *Data Acquisition Databook* appeared, more than 90 significant new products have been introduced, with entries from all our product lines; they run the gamut from brand-new product categories and technologies to new standard products (with improvements in price, performance, or design) to augmented second-source products. They are all documented in this Volume. Selection Guides place them in the context of the rest of the product line. Among the landmark new products introduced since publication of the 1984 Databook are: the first Word-Slice™ chips for microcoded DSP systems – the ADSP-1401 Program Sequencer and ADSP-1410 Address Generator; the 64-Bit ADSP-3210 & ADSP-3220 floating-point Multiplier & ALU; the 2S50 LVDT/RVDT-to-Digital Converter; the AD202/204 ultra-small, low cost isolation amplifiers; the single-chip AD538 multifunction [$Y(Z/X)^M$] Analog Computing Unit and the AD639 Analog Trig-Function Generator; the monolithic AD569 16-Bit Monotonic DAC; the AD7549 single-chip dual 12-Bit DAC; the AD7572 complete-on-a-chip 12-Bit CMOS A/D Converter; and the monolithic 12-bit AD574A ADC, available in both plastic and ceramic packaging.

THE DATABOOK SUPPLEMENT

This Supplement is intended to make it easy for users of our products to consider the new products, to compare them with other products in our line as possible solutions to measurement-and-control equipment and system design problems, and to gain ready access to technical data on any of our products, whether it appears in this update or in Volumes I and II.

To this end, the present supplement contains:

- Technical data on all of the new products (ICs in Section 3; Modules & Subsystems in Section 4)
- Updated Selection Guides, for comparing features and specifications of all products, including the new ones (Section 2)
- Two indexes to make product data easier to find, wherever it appears:
  - Index to Selection Guides in this volume (page 1-5)
  - Model-Number Index to product data in all 3 volumes (pages 1-20 through 1-25, at the back of the book)

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for precision measurement and control. Besides tutorial material and comprehensive data sheets, including the many in the Databook, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several serial publications; for example *Analog Productlog* provides brief information on new products being introduced, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, control and test. We maintain a mailing list of engineers, scientists and technicians with a serious interest in our products. In addition to databook catalogs—and updates, such as this one—we also publish several short-form catalogs, on specific product families. You will find typical publications described on pages 1-15 through 1-17 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our up-to-date Worldwide Service Directory appears on pages 1-18 and 1-19 at the back of the book.

RELIABILITY

The manufacture of reliable products is a key objective at Analog Devices. We maintain facilities that have been qualified under such standards as MIL-M-38510 for ICs and MIL-STD-1772 for hybrids. More than 15 of our products—both proprietary and second-source—have qualified for JAN part numbers; others are in the process. Most of our ICs are available in versions that comply with MIL-STD-883C Class B. We publish a *Military Products Databook* for designers who specify ICs and hybrids for military contracts (the 1985 issue contains data on nearly 100 available product families). A newsletter, *Analog Briefings*, provides current information about the status of reliability at ADI.

Our PLUS program makes available standard devices (commercial and industrial grades, plastic or ceramic packaging) for *any* user with demanding application environments, at a small premium. Subjected to stringent screening, similar to MIL-STD-883 test methods, they are often suffixed and are available from stock.

PRODUCTS NOT CATALOGUED IN THE DATABOOK

For maximum usefulness to designers of new equipment, we have limited the contents of the Databook to data sheets for products most likely to be used for the design of new circuits and systems. If the model number of a product you are interested in is not in any Index, turn to page 1-13 at the back of this volume where you will find a list of older products for which data sheets are available upon request. On page 1-14 you will find a guide to substitutions for products no longer available.

PRICES

Accurate, up-to-date prices are an important consideration in making a choice among the many available product families. Since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

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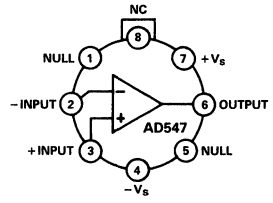
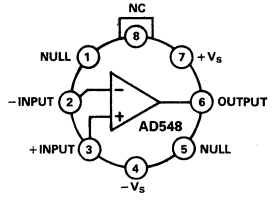
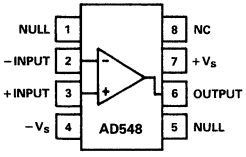


AD547

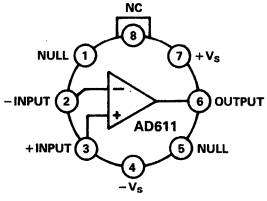
Ultra Low Drift: 1μV/°C – AD547L
Low Offset Voltage: 0.25mV – AD547L
Low Input Bias Currents: 25pA max, Warmed-Up
Low Quiescent Current: 1.5mA
Low Noise: 2μV p-p
High Open Loop Gain: 110dB

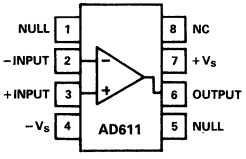




AD548

Low Quiescent Current: 200μA max
AC Specs: 1.8V/μs Slew Rate, 1MHz Unity Gain Bandwidth
Low Input Bias Current: 10pA max, Warmed-Up (AD548L)
Low Input Offset Current: 2pA typ (AD548L)
Low Offset Voltage: 250μV max (AD548L)
Low Drift: 2μV/°C max (AD548L)
Low Noise: 2μV p-p, 0.1 to 10Hz
Improved Replacement for LF441
Military Grade and Plus Parts Available





AD611

Low Offset Voltage: 0.5mV max (AD611K)
Low Offset Voltage Drift: 10μV/°C max (AD611K)
Low Bias Current: 50pA max (AD611K)
High Slew Rate: 8V/μs min
Low Supply Current: 2.5mA max
Fast Settling Time: 3μs
Available in Hermetically-Sealed CERDIP or Metal Can Packages

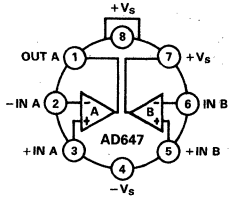
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	I_B pA	V_{OS} mV	V_{OS} TC μV/°C	Gain V/V k	CMR dB	Unity Gain BW MHz typ	Slew Rate V/μs typ	Temp. Range[2]	Volume* Section Page
AD547JH	50	1.0	5	100	76	1.0	3.0	C	I-4-87
AD547KH	25	0.5	2	250	80	1.0	3.0	C	I-4-87
AD547LH	25	0.25	1	250	80	1.0	3.0	C	I-4-87
AD547SH	25	0.5	5	250	80	1.0	3.0	E	I-4-87
AD548AH(AQ)(JN)	25	2	20	100	80	1.0	1.8	I/I/C	S-3-65
AD548BH(BQ)(KN)	10	0.5	5	100	80	1.0	1.8	I/I/C	S-3-65
AD548CH(CQ)	10	0.25	2	100	80	1.0	1.8	I/I	S-3-65
AD548SH	25	2	20	100	80	1.0	1.8	E	S-3-65
AD611JH(JQ)	100	2.0	20	30	74	2	13	C	I-4-91
AD611KH(KQ)	50	0.5	10	50	80	2	13	C	I-4-91

NOTES
[1]Suffix "H" – metal header; Suffix "Q" – cerdip; Suffix "N" – plastic mini-DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

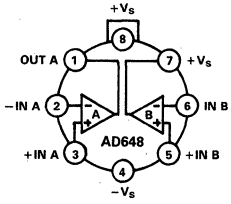
Operational Amplifiers

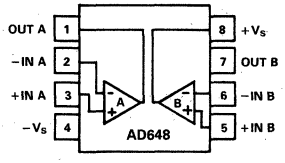
Dual BIFET



AD647

Low Offset Voltage Drift
Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk – 124dB at 1kHz
Low Bias Current: 35pA max Warmed-Up
Low Offset Voltage: 250/μV max
Low Input Voltage Noise: 2μV p-p
High Open Loop Gain: 108dB
Low Quiescent Current: 2.8mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out





AD648

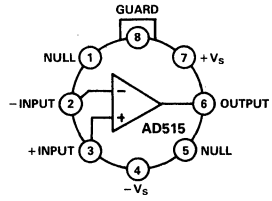
Low Quiescent Current: 400μA max
AC Specs: 1.8V/μs Slew Rate, 1MHz Unity Gain Bandwidth
Low Input Bias Current: 10pA max, Warmed-Up (AD648L)
Low Input Offset Current: 2pA typ (AD648L)
Low Offset Voltage: 250μV max (AD648L)
Low Drift: 2μV/°C max (AD648L)
Low Noise: 2μV p-p, 0.1 to 10Hz
Improved Replacement for LF441
Military Grade and Plus Parts Available

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	I_B pA	V_{OS} mV	V_{OS} TC μV/°C	Gain V/V V/V k	CMR dB	Unity Gain BW MHz typ	Slew Rate V/μs typ	Temp. Range[2]	Volume* Section Page
AD647JH	75	1.0	10	100	76	1.0	3.0	C	I-4-103
AD647KH	35	0.5	5	250	80	1.0	3.0	C	I-4-103
AD647LH	35	0.25	2.5	250	80	1.0	3.0	C	I-4-103
AD647SH	35	0.5	5	250	80	1.0	3.0	E	I-4-103
AD648AH(AQ)(JN)	25	2	20	100	80	1.0	1.8	I/I/C	S-3-135
AD648BH(BQ)(KN)	10	0.5	5	100	80	1.0	1.8	I/I/C	S-3-135
AD648CH(CQ)(LN)	10	0.25	2	100	80	1.0	1.8	I/I/C	S-3-135
AD648SH	25	2	20	100	80	1.0	1.8	E	S-3-135

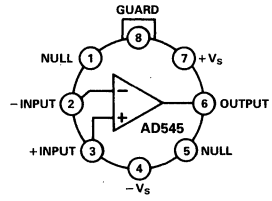
NOTES
[1]Suffix "H" – metal header; Suffix "Q" – cerdip; Suffix "N" – plastic mini-DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Electrometer



AD515

Ultra Low Bias Current: 0.075pA max (AD515L)
0.150pA max (AD515K)
0.300pA max (AD515J)
Low Power: 1.5mA max Quiescent Current (0.8mA typ)
Low Offset Voltage: 1.0mV max (AD515K & L)
Low Drift: 15μV/°C max (AD515K)
Low Noise: 4μV p-p, 0.1 to 10Hz



AD545

Low Offset Voltage: 0.5mV max (AD545L), 0.25mV max (AD545M)
Low Offset Voltage Drift: 5μV/°C max (AD545L), 3μV/°C max (AD545M)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545K, L, M)
Low Noise: 3μV p-p, 0.1 to 10Hz

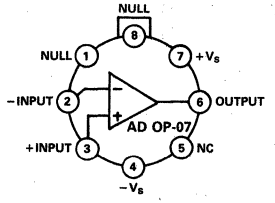
SPECIFICATIONS – Min or Max at T_A = +25°C

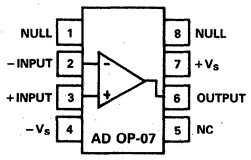
Model[1]	I_B pA	V_{OS} mV	V_{OS} TC μV/°C	Gain V/V	CMR dB	Unity Gain BW MHz typ	Slew Rate V/μs typ	Temp. Range[2]	Volume* Section Page
AD515JH	0.300	3.0	50	20k	66	0.35	0.3	C	I-4-59
AD515KH	0.150	1.0	15	40k	80	0.35	0.3	C	I-4-59
AD515LH	0.075	1.0	15	25k	70	0.35	0.3	C	I-4-59
AD545JH	2	1.0	25	20k	66	0.7	0.3	C	I-4-83
AD545KH	1	1.0	15	40k	70	0.7	0.3	C	I-4-83
AD545LH	1	0.5	5	40k	76	0.7	0.3	C	I-4-83
AD545MH	1	0.25	3	40k	76	0.7	0.3	C	I-4-83

NOTES
[1]Suffix "H" – metal header.
[2]C = 0 to +70°C, I = –25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules * Subsystems; S = This Volume.

Operational Amplifiers

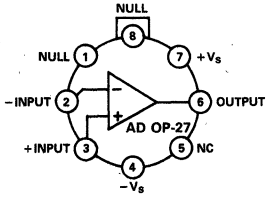
Precision

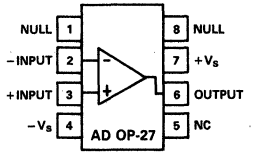




AD OP-07

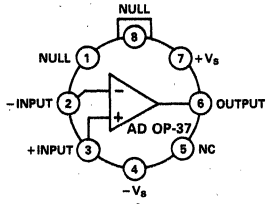
Ten Times More Gain Than Other OP-07 Devices (3.0M min)
Ultra-Low Offset Voltage: 10μV
Ultra-Low Offset Voltage Drift: 0.2μV/°C
Ultra-Stable vs. Time: 0.2μV/month
Ultra-Low Noise: 0.35μV p-p
No External Components Required
Monolithic Construction
High Common Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A, 741 Sockets

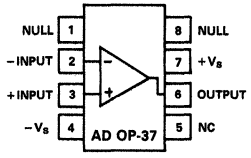




AD OP-27

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
High Slew Rate: 2.8V/μs
High Gain Bandwidth Product: 8MHz
Low Offset Voltage: 10μV
High CMRR: 126dB over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, 725, 714 and 741 Sockets





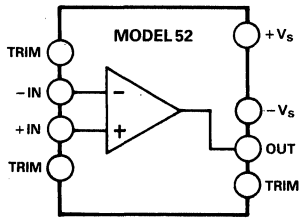
AD OP-37

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
High Speed: 17V/μs
High Gain Bandwidth Product: 63MHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, LH0044, 5130, 3510, 725, 714 and 741 Sockets in Gains ≥ 5

SPECIFICATIONS – Min or Max at T_A = +25°C

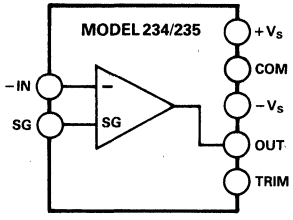
Model[1]	V_{OS} μV	V_{OS} TC μV/°C	Noise 0.1-10Hz μV, pp	Gain V/V k	I_B nA	GBW MHz typ	Slew Rate V/μs typ	CMR dB	Temp. Range[2]	Volume* Section Page
AD OP-07DH(DQ)(DN)	150	2.5	0.65	1200	12	0.6	0.17	94	C	I-4-129
AD OP-07CH(CQ)(CN)	150	1.8	0.65	1200	7	0.6	0.17	100	C	I-4-129
AD OP-07EH(EQ)(EN)	75	1.3	0.6	2000	4	0.6	0.17	106	C	I-4-129
AD OP-07H(Q)	75	1.3	0.6	2000	3	0.6	0.17	110	E	I-4-129
AD OP-07AH(AQ)	25	0.6	0.6	3000	2	0.6	0.17	110	E	I-4-129
AD OP-27GH(GQ)(GN)	100	1.8	0.25	700	80	8.0	2.8	100	I	I-4-135
AD OP-27FH(FQ)(FN)	60	1.3	0.18	1000	55	8.0	2.8	106	I	I-4-135
AD OP-27EH(EQ)(EN)	25	0.6	0.18	1000	40	8.0	2.8	114	I	I-4-135
AD OP-27CH(CQ)	100	1.8	0.25	700	80	8.0	2.8	100	E	I-4-135
AD OP-27BH(BQ)	60	1.3	0.18	1000	55	8.0	2.8	106	E	I-4-135
AD OP-27AH(AQ)	25	0.6	0.18	1000	40	8.0	2.8	114	E	I-4-135
AD OP-37GH(GQ)(GN)	100	1.8	0.25	700	80	63	17	100	I	S-3-339
AD OP-37FH(FQ)(FN)	60	1.3	0.18	1000	55	63	17	106	I	S-3-339
AD OP-37EH(EQ)(EN)	25	0.6	0.18	1000	40	63	17	114	I	S-3-339
AD OP-37CH(CQ)	100	1.8	0.25	700	80	63	17	100	E	S-3-339
AD OP-37BH(BQ)	60	1.3	0.18	1000	55	63	17	106	E	S-3-339
AD OP-37AH(AQ)	25	0.6	0.18	1000	40	63	17	114	E	S-3-339

NOTES
[1]Suffix "H" – metal header; Suffix "Q" – cerdip; Suffix "N" – plastic mini-DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



MODEL 52

Guaranteed Low Noise 1.5μV p-p max (0.01 to 1Hz)
Low Voltage Drift: 2μV/°C max (52K)
Low Bias Current: 3pA, max
High CMR: 100dB, min
High Voltage Gain: 120dB, min
Wide Power Supply Range: ±9V to ±18V
Excellent Long Term Stability: 5μV/month
Fast Thermal Response



MODEL 234

Low Drift: 0.1μV/°C, 1pA/°C
Offset Stability: 2μV per month
Submicrovolt Noise: 0.7μV p-p (0.01 to 1Hz B.W.)
Fast Response: 2.5MHz B.W., 4μs Settling (0.01%)

MODEL 235

Low Cost
Ultra-Low Noise: 0.5μV p-p, 1Hz B.W. (2μV, max)
Very Low Drift: 0.1μV/°C max, 0.5pA/°C max (235L)
Excellent Long Term Stability: 5μV/yr
Low Profile: 0.5" Height

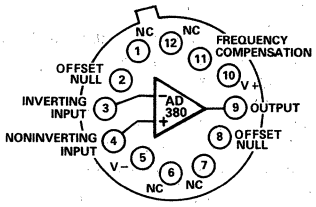
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	I_B pA	V_{OS} mV	V_{OS} TC μV/°C	Gain V/V	CMR dB	Unity Gain BW MHz typ	Slew Rate V/μs	Temp. Range[1]	Volume* Section Page
52J	3	0.5	3	1,000k	100	0.5	0.25	C	II-4-19
52K	3	0.5	2	1,000k	100	0.5	0.25	C	II-4-19
234J	100	0.05	1	10,000k	N/A	2.5	30	C	II-4-23
234K	100	0.02	0.3	10,000k	N/A	2.5	30	C	II-4-23
234L	100	0.02	0.1	10,000k	N/A	2.5	30	C	II-4-23
235J	100	0.025	0.5	50,000k	N/A	1	0.3	C	II-4-23
235K	50	0.025	0.25	50,000k	N/A	1	0.3	C	II-4-23
235L	50	0.015	0.1	50,000k	N/A	1	0.3	C	II-4-23

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

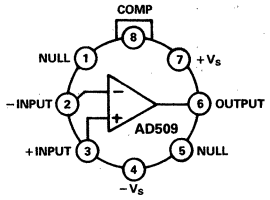
Operational Amplifiers

High Speed, Fast Settling



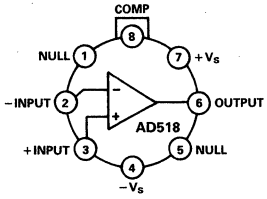
AD380

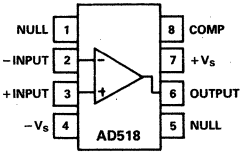
High Slew Rate: 330V/μs
Fast Settling to 0.01%: 250ns
High Output Current: 50mA
Low Input Bias Currents (10pA – AD380L)
Low Noise (3.3μV p-p)



AD509

Fast Settling Time
0.1% in 500ns max
0.01% in 2.5μs max
High Slew Rate: 100V/μs min
Low I_{OS}: 25nA max
Guaranteed V_{OS} Drift: 30μV/°C max
High CMRR: 80dB min
Drives 500pF
Low Price





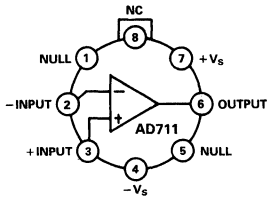
AD518

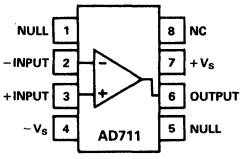
High Slew Rate: 70V/μs
Wide Bandwidth: 12MHz
60° Phase Margin (At Unity Gain Crossover)
Drives 300pF Load
Guaranteed Low Offset Drift:
15μV/°C max (AD518K)
Pin Compatible with 118-Type Op Amp Series
Mil-Standard Parts Available
8-Pin Plastic Mini-DIP or TO-99 Hermetic Metal Can

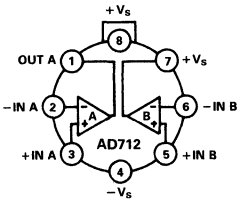
SPECIFICATIONS – Min or Max at T_A = +25°C

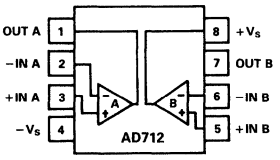
Model[1]	Unity Gain BW MHz typ	Slew Rate V/μs typ	Settling Time ns typ	Gain V/V k	I_B nA	V_{OS} mV	V_{OS} TC μV/°C	CMR dB	Temp. Range[2]	Volume* Section Page
AD380JH	40	330	250	40	0.1	2.0	50	60	C	I-4-27
AD380KH	40	330	250	40	0.1	1.0	20	60	C	I-4-27
AD380LH	40	330	250	40	0.1	1.0	10	60	C	I-4-27
AD380SH	40	330	250	40	0.1	1.0	50	60	E	I-4-27
AD509JH	20	120	200	7.5	250	10	–	74	C	I-4-51
AD509KH	20	120	200	10	200	8.0	30	80	C	I-4-51
AD509SH	20	120	200	10	200	8.0	30	80	E	I-4-51
AD518JH(JN)	12	70	800	25	500	10.0	–	70	C	I-4-71
AD518KH(KN)	12	70	800	50	250	4.0	15	80	C	I-4-71
AD518SH	12	70	800	50	250	4.0	20	80	E	I-4-71

NOTES
[1]Suffix "H" – metal header; Suffix "N" – plastic mini-DIP.
[2]C = 0 to +70°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.









AD711/712

Improved Replacement for LF411/LF412
Dual Version Available: AD712
AC Performance:
- **Settles to 0.01% in 1μs**
- **Slew Rate (Unity Gain): 18V/μs min (AD711B)**
- **Small Signal Bandwidth: 4MHz**

DC Performance:
- **Low Offset Voltage: 0.25mV max (AD711C)**
- **Low Offset Voltage Drift: 5μV/°C max (AD711C)**
- **Low Bias Current: 25pA max (AD711C)**
- **High Open Loop Gain: 100,000 V/V (100dB) min**
- **Low Noise: 3μV p-p, 0.1Hz to 10Hz max (AD711C)**

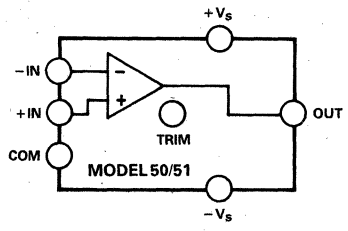
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Unity Gain BW MHz typ	Slew Rate V/μs	Settling Time ns	Gain V/V	I_B pA	V_{OS} mV	V_{OS} TC μV/°C	CMR dB	Temp. Range[2]	Volume* Section Page
AD711AH(AQ)(JN)	4	16	1000	100k	50	2	20	74	I/I/C	S-3-163
AD711BH(BQ)(KN)	4	18	1000	100k	50	0.5	10	76	I/I/C	S-3-163
AD711CH(CQ)	4	18	1000	100k	25	0.25	5	80	I/I	S-3-163
AD711SH(SQ)	4	16	1000	100k	50	2	20	74	E/E	S-3-163
AD712AH(AQ)(JN)	4	16	1000	100k	50	3	20	74	I/I/C	S-3-165
AD712BH(BQ)(KN)	4	18	1000	100k	50	1	10	76	I/I/C	S-3-165
AD712CH(CQ)	4	18	1000	100k	25	0.5	5	80	E/E	S-3-165
AD712SH(SQ)	4	16	1000	100k	50	3	20	74	E/E	S-3-165

NOTES
[1]Suffix "H" – metal header; Suffix "Q" – cerdip; Suffix "N" – plastic mini-DIP.
[2]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules * Subsystems; S = This Volume.

Operational Amplifiers

High Speed, Fast Settling



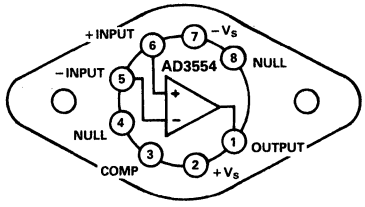
MODELS 50 & 51

Fast Settling: 200ns max, 0.05% (50J/K)
100ns max, 0.1% (50J/K)
100mA Output: dc to 8MHz (50J/K)
dc to 6MHz (51A/B)
All Hermetically-Sealed Semiconductors (51A/B)
−55°C to +125°C Temperature Range (51A/B)
100MHz Gain Bandwidth (50J/K)

SPECIFICATIONS – Min or Max at T_A = +25°C

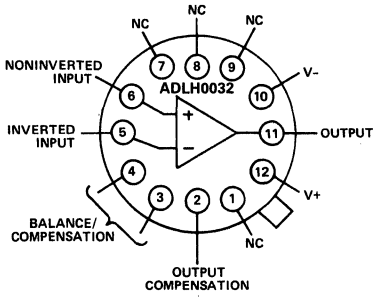
Model	I_B nA	V_{OS} mV	V_{OS} TC µV/°C	Gain dB	CMR dB	Unity Gain BW MHz typ	Slew Rate V/µs V/µs	Temp. Range[1]	Volume* Section Page
50J	2	3	50	88	60	100	500	C	II-4-17
50K	2	3	15	88	60	100	500	C	II-4-17
51A	2	3	50	94	60	80	400	I	II-4-17
51B	2	3	20	94	60	80	400	I	II-4-17

NOTES
[1]C = 0 to +70°C, I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



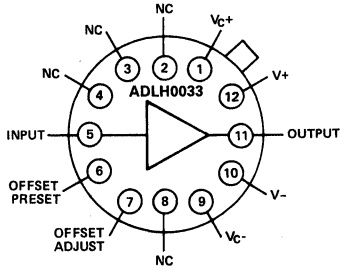
AD3554

Very High Slew Rate: 1000V/μs
Fast Settling: 150ns max to ±0.05%
Gain Bandwidth Product: 1.7GHz typical
High Output Current: 100mA min @ V_{OUT} = 10V
Full Differential Input



ADLH0032

2nd Source: Replaces All LH0032G
High Slew Rate: 500V/μs
Wide 70MHz Bandwidth
Operation Guaranteed −55°C to +125°C (ADLH0032G)
High Input Impedance of $10^{12}\Omega$
2mV Input Offset Voltage



ADLH0033

2nd Source: Replaces All LH0033G Series
Wide Bandwidth – dc to 100MHz
High Slew Rate – 1500V/μs
Operates on Single or Dual Power Supplies
Operation Guaranteed −55°C to +125°C (ADLH0033G)
High $10^{11}\Omega$ Input Impedance

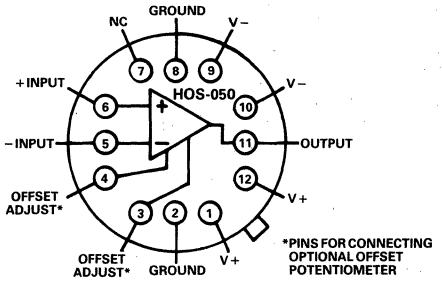
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Unity Gain BW MHz typ	Slew Rate V/μs	Settling Time ns typ	Gain V/V	I_B nA max	V_{OS} mV max	V_{OS}TC μV/°C max	CMR dB min	Temp. Range[2]	Volume* Section Page
AD3554AM	90	1000	120	100k	0.05	2	50	60	I	I-4-111
AD3554BM	90	1000	120	100k	0.05	1	15	60	I	I-4-111
AD3554SM	90	1000	120	100k	0.05	1	25	60	E	I-4-111
ADLH0032G	70	350	300	1k	0.1	5	50	50	E	I-4-121
ADLH0032GH	70	350	300	1k	0.2	15	50	50	I	I-4-121
ADLH0033G	100	1000	–	0.97	0.1	10	100	–	E	I-4-125
ADLH0033CG	100	1000	–	0.97	0.1	20	100	–	I	I-4-125

NOTES
[1]Suffix "M" – metal TO-3 style header; Suffix "G" – metal TO-8 style header.
[2]I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

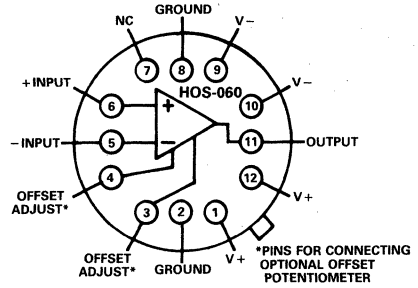
Operational Amplifiers

Wideband/Buffers



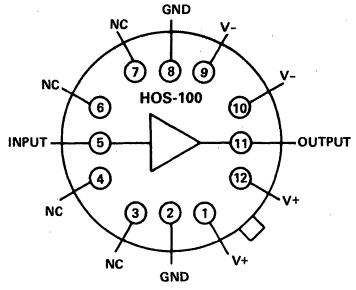
HOS-050

80ns Settling to 0.1%; 200ns to 0.01%
100MHz Gain Bandwidth Product
55MHz 3dB Bandwidth
100mA Output @ ± 10V



HOS-060

<1mV V_{OS}
Low Drift
80ns Settling to 0.1%; 200ns to 0.01%
100mA Output @ ± 10V



HOS-100

Wide Bandwidth – dc to 125MHz
High Slew Rate – 1500V/µs
Operation Guaranteed −55°C to !125°C (SH)
High Output Drive – ± 10V with 100Ω Load
MIL-STD-883 Processing Available

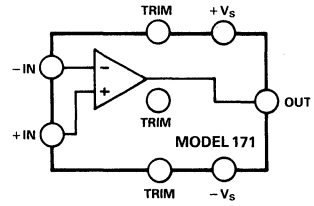
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Unity Gain BW MHz typ	Slew Rate V/µs typ	Gain V/V typ	I_B nA max	V_{OS} mV max	V_{OS} TC µV/°C max	CMR dB typ	Temp. Range[2]	Volume* Section Page
HOS-050	55	300	100k	2	35	150	70	E	I-4-147
HOS-050A	55	300	100k	2	35	35	70	E	I-4-147
HOS-050C	55	300	100k	2	65	200	70	I	I-4-147
HOS-060SH	55	300	100k	2	1	10(typ)	70	E	I-4-153
HOS-100SH	100	1000	0.95	20k	10	75	–	E	I-4-157
HOS-100AH	100	1000	0.94	25k	25	75	–	I	I-4-157

NOTES
[1]All HOS family devices packaged in TO-8 style metal headers.
[2]I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Operational Amplifiers

High Voltage



MODEL 171

High Output Voltage: ±140V
High CMR: 100dB min
Operates with a Wide Range of Power Supplies
±25V_{DC} to ±150V_{DC}
High CMV: ±(|V_S| −10V)
Full Power Response: 15kHz min

SPECIFICATIONS – Min or Max at T_A = +25°C

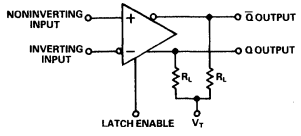
Model	I_B pA	V_{OS} mV	V_{OS} TC µV/°C	Gain V/V	CMR dB	Unity Gain BW MHz typ	Slew Rate V/µs	Temp. Range[1]	Volume* Section Page
171J	50	1	50	1,000k	100	3	10	C	II-4-21
171K	20	1	15	1,000k	100	3	10	C	II-4-21

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Comparators

Ultra-Fast

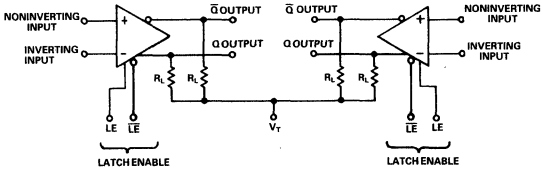
AD9685BD/BH FUNCTIONAL BLOCK DIAGRAM (SINGLE)



AD9685/9687

2.2ns Prop Delay (AD9685)
2.7ns Prop Delay (AD9687)
Typical 0.5ns Latch Setup
Standard +5V/−5.2V Power

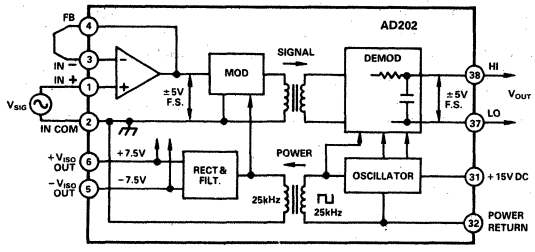
AD9687BD FUNCTIONAL BLOCK DIAGRAM (DUAL)



SPECIFICATIONS – Min or Max at T_A = +25°C

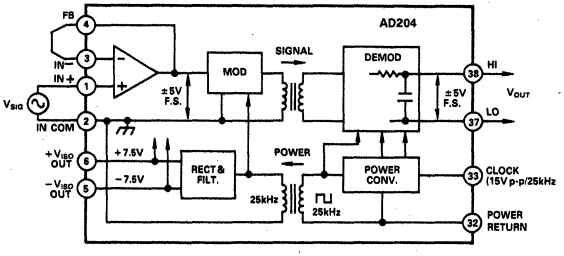
Model[1]	Input Offset mV	Input Offset µA	Input Bias µA	Prop Delay (ns) $t_{PD}+$ & $t_{PD}-$	Prop Delay (ns) $t_{PD}+(E)$ & $t_{PD}-(E)$	Minimum Setup/Hold (ns)	Volume* Section Page
AD9685BD/BH	±5	5	10	2.2	2.5	1/1	I-4-117
AD9687BD	±5	5	10	2.7	2.7	1/1	I-4-117

NOTES
[1]AD9685BD – 16-Pin DIP; AD9685BH – TO100; AD9687BD – 16-Pin DIP.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD202JY

Low Cost
Small Size: 4 Channels/Inch
Single Channel Design:
+15V Power Input
Functionally Complete
High Accuracy: ±0.05% max Nonlinearity
1000V Peak CMV Isolation
High CMR: 130dB (G=100V/V)
Low Output Drift: 20μV/°C (G=1V/V)
Uncommitted Input Amplifier:
Gain 1 to 100 V/V



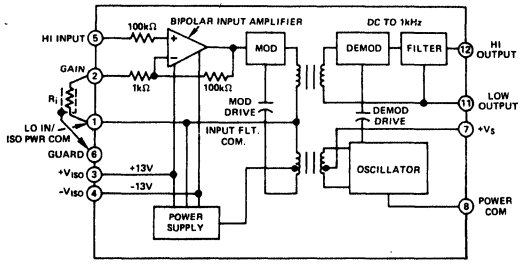
AD204JY

Low Cost
Small Size: 4 Channels/Inch
Multichannel Design:
25kHz Clock Input (AD246JY)
Functionally Complete
High Accuracy: ±0.05% max Nonlinearity
1000V Peak CMV Isolation
High CMR: 130dB (G=100V/V)
Low Output Drift: 20μV/°C (G=1V/V)
Isolated Output Power: ±7.5V @±2mA
Uncommitted Input Amplifier:
Gain 1 to 100 V/V

SPECIFICATIONS – Min or Max at T_A = +25°C

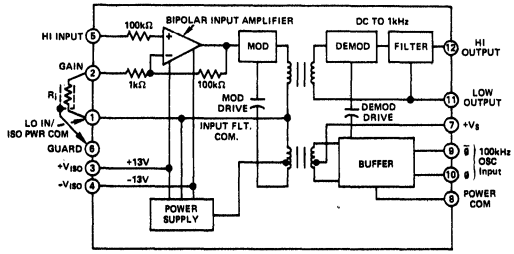
Model[1]	Gain Range V/V	Gain Nonlinearity %	CMV In/Out V pk	Input T.C.[2] μV/°C typ	Frequency Response kHz typ	Temp. Range[3]	Volume* Section Page
AD202JY	1 to 100	0.05	1000	10	5	C	S-3-5
AD204JY	1 to 100	0.05	1000	10	1.5	C	S-3-5

NOTES
[1]Y = Single in-line package.
[2]At gain = 100 V/V.
[3]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



MODEL 290A

Isolated Power Supply: ±13V dc @ ±5mA (290A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours: 0.01%/°C
Small Size: 1.5" x 1.5" x 0.62"
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V



MODEL 292A

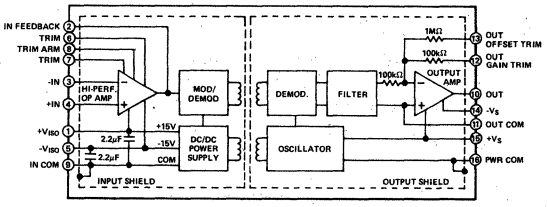
Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5" x 1.5" x 0.62"
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100/V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Gain Range V/V	Gain Nonlinearity % typ	CMV In/Out V pk	Input T.C.[1] μV/°C typ	Frequency Response kHz typ	Temp. Range[2]	Volume* Section Page
290A	1 to 100	0.25	1500	11.5	2.5	I	II-5-21
292A	1 to 100	0.25	1500	10.5	2.5	I	II-5-21

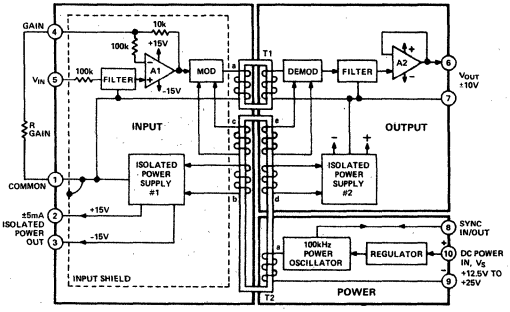
NOTES
[1]At gain = 100 V/V.
[2]I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Isolation Amplifiers



MODEL 277

Versatile Op Amp Front End: Inverting, Noninverting, Differential Applications
Low Nonlinearity: 0.025% max, Model 277K
Low Input Offset Voltage Drift: 1µV/°C max, Model 277K
Floating Power Supply: ±15V dc @ ±15mA
High CMR: 160dB min @ dc
High CMV: 3500V_{rms}



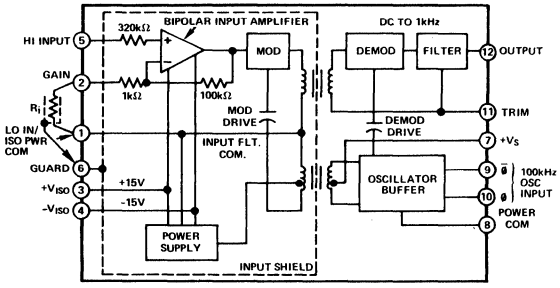
MODEL 289

Low Nonlinearity: ±0.012% max (289L)
Frequency Response: (−3dB) dc to 20kHz (Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2µA rms max, @115V ac, 60Hz

SPECIFICATIONS – Min or Max at T_A = +25°C

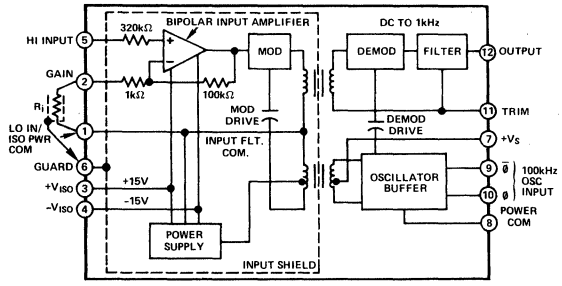
Model	Gain Range V/V	Gain Nonlinearity %	CMV In/Out V pk	Input T.C.[1] µV/°C	Frequency Response kHz typ	Temp. Range[2]	Volume* Section Page
289J	1 to 100	0.05	2500	22	20	C	II-5-17
289K	1 to 100	0.025	2500	16	20	C	II-5-17
289L	1 to 100	0.012	2500	10.5	20	C	II-5-17
277J	1 to 1000	0.05	2500	3	2.5	C	II-5-9
277K	1 to 1000	0.025	2500	1	2.5	C	II-5-9
277A	1 to 1000	0.05	2500	3	2.5	I	II-5-9

NOTES
[1]At maximum gain.
[2]C = 0 to +70°C, I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



MODEL 284J

High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
High CMR: 110dB min with 5kΩ Imbalance
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Low Input Offset Voltage Drift: 10μV/°C, G=100V/V
Resistor Programmed Gain: 1 to 10V/V (284J)
Isolated Power Supply: ±8.5V dc @ ±5mA (284J)
Meets EEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.0μA max (284J)



MODEL 286J

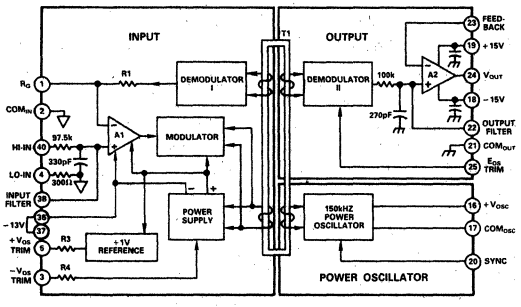
High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
High CMR: 110dB min with 5kΩ Imbalance
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Low Input Offset Voltage Drift: 10μV/°C, G=100V/V
Resistor Programmed Gain: 1 to 100V/V (286J)
Isolated Power Supply: ±15V dc @ ±15mA (286J)
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.5μA max (284J)

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Gain Range V/V	Gain Nonlinearity % typ	CMV In/Out V pk	Input T.C.[1] μV/°C typ	Frequency Response kHz	Temp. Range[2]	Volume* Section Page
284J	1 to 10	0.05	2500	35	1	C	II-5-11
286J	1 to 100	0.05	2500	10	1	C	II-5-11

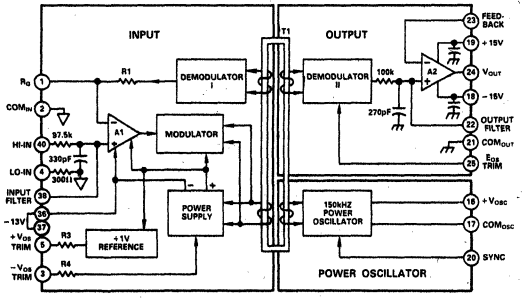
NOTES
[1]At maximum gain.
[2]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Isolation Amplifiers



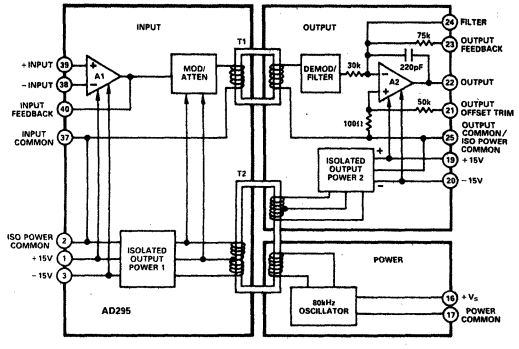
AD293

Hybrid Construction
High Common-Mode Voltage: AD293 ±2500V Peak max
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111



AD294

Hybrid Construction
High Common-Mode Voltage: ±8000V Peak max
Nonlinearity: ±0.05% of max
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz



AD295

Hybrid Construction
Low Nonlinearity: ±0.012% max (AD295C)
Low Gain Drift: ±60ppm/°C max
Floating Input and Output Power: ±15V dc @ 5mA
3-Port Isolation: ±2500V CMV (Input to Output)
Complies with NEMA ICS1-111
Gain Adjustable: 1V/V to 1000V/V
User Configurable Input Amplifier

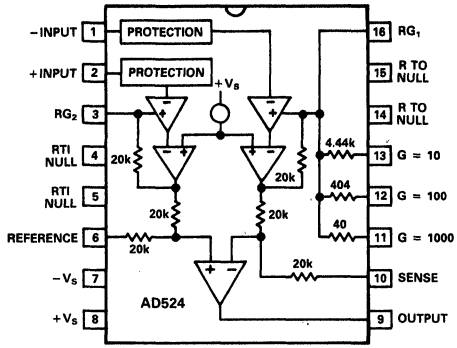
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Gain Range V/V	Gain Nonlinearity %	CMV In/Out V pk	Input T.C.[1] μV/°C	Frequency Response kHz typ	Temp. Range[2]	Volume* Section Page
AD293A	1 to 1000	0.1	2500	10.5	2.5	I	I-5-13
AD293B	1 to 1000	0.05	2500	5.2	2.5	I	I-5-13
AD294A	1 to 1000	0.1	3500	11	2.5	I	I-5-13
AD295A	1 to 1000	0.05	2500	10.4	4.5	I	S-3-13
AD295B	1 to 1000	0.025	2500	3.3	4.5	I	S-3-13
AD295C	1 to 1000	0.012	2500	1.6	4.5	I	S-3-13

NOTES
[1]At gain = 1000 V/V.
[2]I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

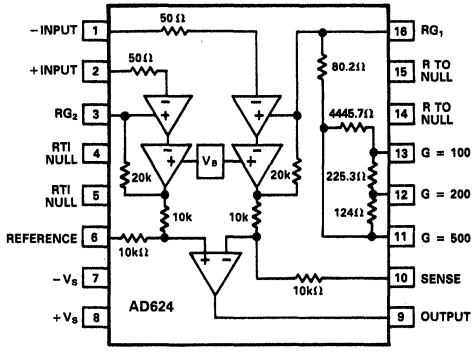
Instrumentation Amplifiers

Precision



AD524

Pin Programmable Gains of 1, 10, 100, 1000
Low Noise: 0.3μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Input Protection, Power On – Power Off
No External Components Required
Internally Compensated



AD624

Pin Programmable Gains of 1, 100, 200, 500, 1000
Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB max (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
No External Components Required
Internally Compensated

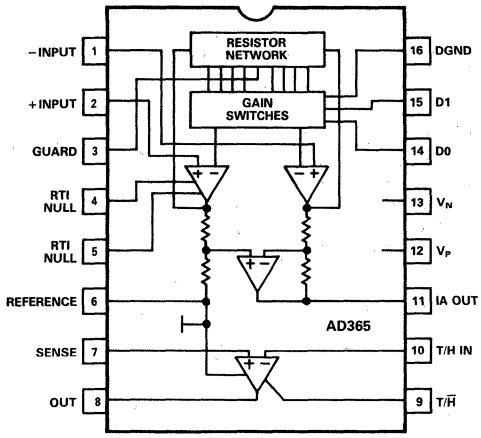
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Gain Error (G=100) %	Gain Tempco (G=100) ppm/°C	Nonlinearity (G=100) %	Input Offset Voltage μV	Input Offset Voltage Drift μV/°C	Small Signal Band-Width MHz	RTI Noise μV p-p[2]	Temp. Range[3]	Volume* Section Page
AD524AD	±0.5	35	±0.01	250	2	1	0.3	I	I-5-31
AD524BD	±0.35	25	±0.005	100	0.75	1	0.3	I	I-5-31
AD524CD	±0.25	25	±0.003	50	0.5	1	0.3	I	I-5-31
AD524SD	±0.5	25	±0.01	50	2.0	1	0.3	E	I-5-31
AD624AD	±0.25	10	±0.005	200	2	1	0.2	I	I-5-43
AD624BD	±0.15	10	±0.003	75	0.5	1	0.2	I	I-5-43
AD624CD	±0.1	10	±0.001	25	0.25	1	0.2	I	I-5-43
AD624SD	±0.25	10	±0.005	75	2	1	0.2	E	I-5-43

NOTES
[1]Suffix "D" – ceramic DIP.
[2]RTI Noise (0.1 to 10Hz) and G = 1000.
[3]I = −25°C to +85°C; E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

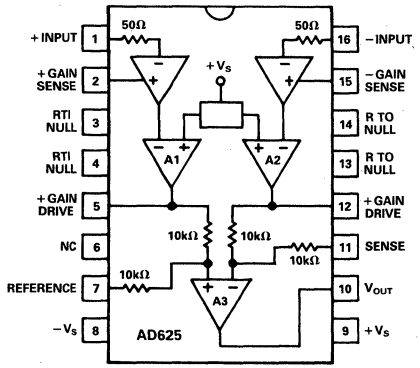
Instrumentation Amplifiers

Programmable Gain



AD365

Software Programmable Gain (1, 10, 100, 500)
Includes Fast Sample-and-Hold Amplifier
Low Input Noise (0.2μV p-p)
Low Gain Error (0.05% max)
Low Nonlinearity (0.005% max)
Low Gain Drift (10ppm/°C max)
Low Offset Drift (2μV/°C RTI max)
Fast Settling (15μs @ Gain 100)
Small 16-Pin Metal DIP



AD625

Resistor Programmable Gain Amp
Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.001% max (G=1 to 500)
High CMRR: 130dB max (G=500)
Low Offset Voltage: 25μV max
Low Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Internally Compensated
Versatile Gain Programming
Software Programmable Gain Amp

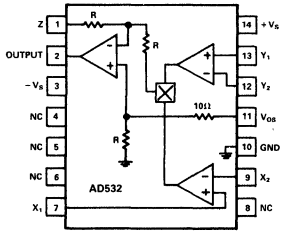
SPECIFICATIONS – Min or Max at T_A = +25°C

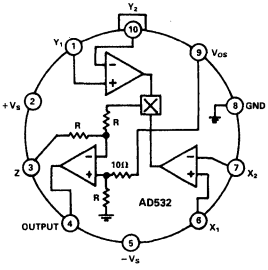
Model[1]	Gain Range	Gain Error %	Gain Tempco ppm/°C	Input Offset Voltage μV	Input Offset Voltage Drift μV/°C	Band-Width kHz	RTI Noise μV p-p[2]	Temp. Range[3]	Volume* Section Page
AD365AM	1,10,100,500	0.1	10	200	2	850	0.2	I	S-3-19
AD625AD(JN)	1 to 10,000	0.01	5	200	2	850	0.2	I/C	S-3-111
AD625BD(KN)	1 to 10,000	0.008	5	50	0.5/1	850	0.2	I/C	S-3-111
AD625CD	1 to 10,000	0.005	5	25	0.25	850	0.2	I	S-3-111
AD625SD	1 to 10,000	0.01	5	200	2	850	0.2	E	S-3-111

NOTES
[1]Suffix "M" – metal DIP; Suffix "D" – ceramic DIP; Suffix "N" – plastic mini-DIP.
[2]RTI noise specified at 0.1 to 10Hz, G = 500.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Analog Signal Processing Components

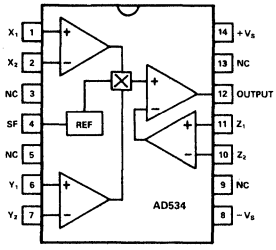
Multipliers/Dividers

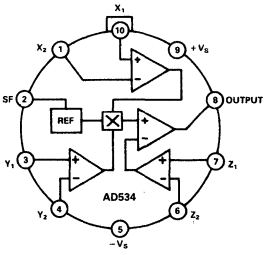




AD532

Pretrimmed to ±1.0% (AD532K)
No External Components Required
Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
Diff Inputs For $(X_1 - X_2)(Y_1 - Y_2)/10V$ Transfer Function
Monolithic Construction, Low Cost
MIL-M-38510 Slash Sheet Part





AD534

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1 - X_2)(Y_1 - Y_2)/10V] + z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability
MIL-M-38510 Slash Sheet Part

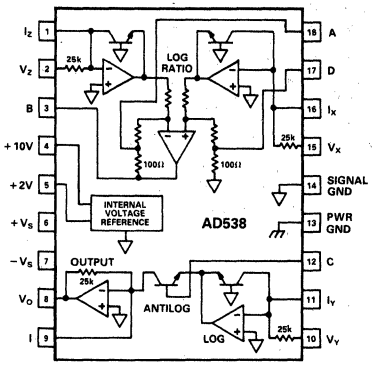
SPECIFICATIONS – Min or Max at $T_A = +25°C$

Model[1]	Full Scale Accuracy-% max	Accuracy vs. Temperature %/°C (typ)	X Nonlinearity % of Full Scale	Y Nonlinearity % of Full Scale (typ)	Bandwidth Small Signal MHz (typ)	Operating Power Supply V	Temp. Range[2]	Volume* Section Page
AD532JD(JH)	2	0.04	0.8	0.3	1	±10 to ±18	C	I-6-17
AD532KD(KH)	1	0.03	0.5	0.2	1	±10 to ±18	C	I-6-17
AD532SD(SH)	1	0.04 max	0.5	0.2	1	±10 to ±22	E	I-6-17
AD534JD(JH)	1	0.022	0.4	0.01	1	±8 to ±18	C	I-6-27
AD534KD(KH)	0.5	0.015	0.3 max	0.01 max	1	±8 to ±18	C	I-6-27
AD534LD(LH)	0.25	0.008	0.12 max	0.01 max	1	±8 to ±18	C	I-6-27
AD534SD(SH)	1	0.02 max	0.4	0.01	1	±8 to ±18	E	I-6-27
AD534TD(TH)	0.5	0.01 max	0.3 max	0.01 max	1	±8 to ±18	E	I-6-27

NOTES
[1]Suffix "H" – metal header; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Analog Signal Processing Components

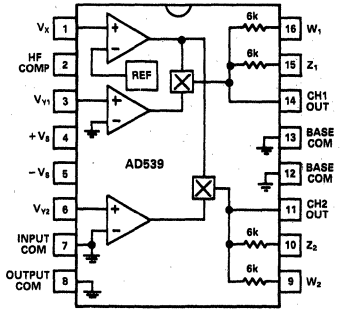
Multipliers/Dividers



AD538

Transfer Function $V_Y \left(\frac{V_Z}{V_X}\right)^M$

Wide Dynamic Range
Analog Multiplication and Division
Resistor Programmable Powers & Roots
Low Input Offsets <100μV
Excellent Gain and Nonlinearity – 0.25% of Reading
+2V and +10V On-Chip References
Monolithic Construction



AD539

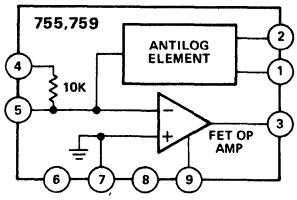
Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control-Bandwidth of 5MHz
Fully-Calibrated, Monolithic Circuit

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Multiplication Error % of Full Scale	Multiplication Error T_{min} to T_{max} % of Full Scale	Bandwidth Small Signal MHz, typ	Operating Power Supply V	Temp. Range[2]	Volume* Section Page
AD538AD	500μV + 1.0[3]	250μV + 2.0[3]	0.4	±10 to ±18	I	S-3-57
AD538BD	250μV + 0.5[3]	500μV + 1.0[3]	0.4	±10 to ±18	I	S-3-57
AD538SD	500μV + 1.0[3]	1000μV + 2.5	0.4	±10 to ±18	E	S-3-57
AD539JD (JN)	2.5	2 typ	30	±4.5 to ±16.5	C	I-6-49
AD539KD(KN)	1.5	1 typ	30	±4.5 to ±16.5	C	I-6-49
AD539SD	4	1 typ	30	±4.5 to ±16.5	E	I-6-49

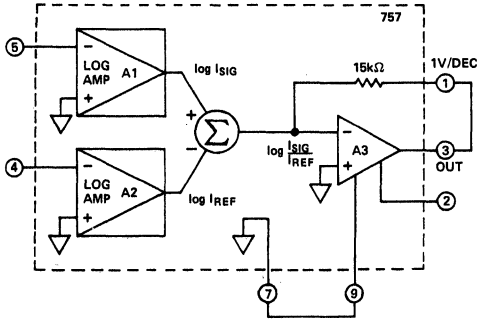
NOTES
[1]Suffix "D" – ceramic DIP; Suffix "N" – plastic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[3]Error specified in offset plus % of reading.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Log-Antilog Amplifiers



MODEL 755, MODEL 759

High Accuracy: Models 755N, 755P
Low Cost: Models 759N, 759P
Complete Log-Antilog Amplifiers: External Components not Required
Temperature-Compensated Internal Reference
6 Decades Current Operation: 1nA to 1mA
1% max Error: 1nA to 1mA (755)
20nA to 200μA (759)
4 Decades Current Operation: 1mV to 10V
1% max Error: 1mV to 10V (755)
1mV to 2V (759)



MODEL 757

6 Decade Operation – 1nA to 1mA
1/2% Log Conformity – 10nA to 100μA
Symmetrical FET Inputs
Voltage or Current Operation
Temperature Compensated
Complete Log Ratio Amplifier: External Components not Required

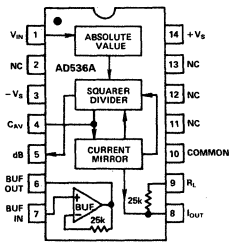
SPECIFICATIONS – Min or Max at T_A = +25°C

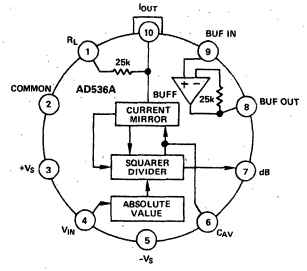
Model	Input Range	Log Conformity Error %RTI	Scale Factor V/Decade	Bandwidth −3dB kHz	Temp. Range[1]	Volume* Section Page
755N	+(10nA to 1mA)	0.5	2, 1, 2/3	10	C	II-8-7
755P	−(10nA to 1mA)	0.5	2, 1, 2/3	10	C	II-8-7
759N	+(20nA to 1mA)	1.0	2, 1, 2/3	200	C	II-8-7
759P	−(20nA to 1mA)	1.0	2, 1, 2/3	200	C	II-8-7
757N	+(10nA to 1mA)	0.5	1	25	C	II-8-11
757P	−(10nA to 1mA)	0.5	1	25	C	II-8-11

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Analog Signal Processing Components

RMS-to-DC Converters



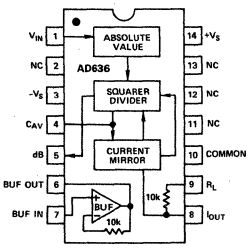


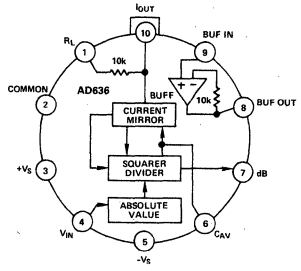
AD536A

True rms-to-dc Conversion
Laser-Trimmed to High Accuracy
- **0.2% max Error (AD536AK)**
- **0.5% max Error (AD536AJ)**

Wide Response Capability:
- **Computes rms of ac and dc Signals**
- **300kHz Bandwidth: V_{rms}>100mV**
- **2MHz Bandwidth: V_{rms}>1V**
- **Signal Crest Factor of 7 for 1% Error**

dB Output with 60dB Range
Low Power: 1mA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit



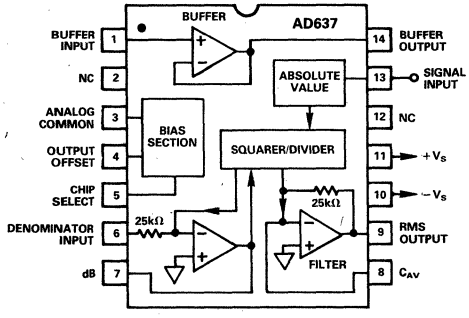


AD636

True rms-to-dc Conversion
200mV Full Scale
Laser-Trimmed to High Accuracy
- **0.5% max Error (AD636K)**
- **1.0% max Error (AD636J)**

Wide Response Capability'
- **Computes rms of ac and dc Signals**
- **1MHz −3dB Bandwidth: V_{rms}>100mV**
- **Signal Crest Factor of 6 for 0.5% Error**

dB Output with 50dB Range
Low Power: 800μA Quiescent Current
Single or Dual Supply Operation
Monolithic Integrated Circuit



AD637

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Additional Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

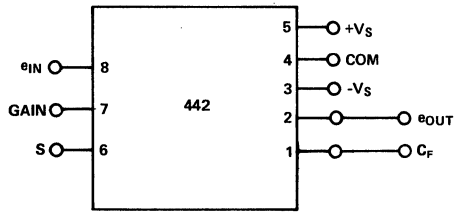
Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (−60dB Range)
Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Full Scale Range Vrms	Conversion Accuracy % of Reading	C/C Reversal Error % of Reading	Error vs. Crest Factor of 7 % of Reading, typ	Frequency Response[2] MHz, typ	dB Output Error dB, typ	Temp. Range[3]	Volume* Section Page
AD536AJD(JH)	±7	±5mV±0.5	±0.2	−1.0	2	±0.6	C/C	I-6-43
AD536ADK(KH)	±7	±2mV±0.2	±0.1	−1.0	2	±0.3	C/C	I-6-43
AD536ASD(SH)	±7	±5mV±0.5	±0.2	−1.0	2	±0.5	E/E	I-6-43
AD636JD(JH)	0.2	±0.5mV±1.0	±0.2	−0.5	1.3	±0.5	C/C	I-6-71
AD636KD(KH)	0.2	±0.2mV±0.5	±0.1	−0.5	1.3	±0.2	C/C	I-6-71
AD637JD(JQ)(SD)	±7	±1mV±0.5	±0.25	−0.8	8	±1	C/C/E	I-6-77
AD637KD(KQ)	±7	±0.5mV±0.2	±0.1	−0.8	8	±1	C/C	I-6-77

NOTES
[1]Suffix "H" – metal header; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]Frequency response given at ±3dB bandwidth and full scale.
[3]C = 0 to +70°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



MODEL 442

DC to 8MHz Response (−3dB)
High Accuracy:
With No Ext. Trim: ±2mV ±0.15% of Rdg., max
With Ext. Trim: ±1mV ±0.05% of Rdg., max
Low Drift: ±(35μV ±0.01% of Reading)/°C max, 442L
Fast Settling Time: 5ms to 1%
All Hermetically Sealed Semiconductors
No External Components Required to Meet Specifications

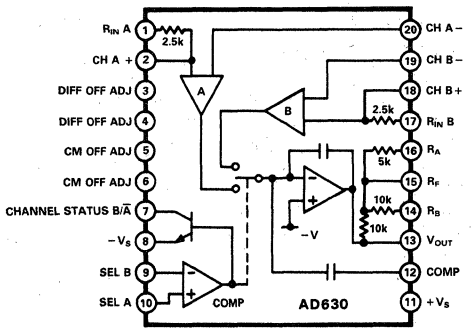
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Total Error No Ext Adjust mV	Total Error T.C. μV/C	Frequency Response 1% Error kHz	Frequency Response −3dB Error MHz	Temp. Range[1]	Volume* Section Page
442J	2 ±0.15% RDG.	100	800	7	C	II-7-7
442K	2 ±0.15% RDG.	50	800	7	C	II-7-7
442L	2 ±0.15% RDG.	35	800	7	C	II-7-7

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Analog Signal Processing Components

Special Functions



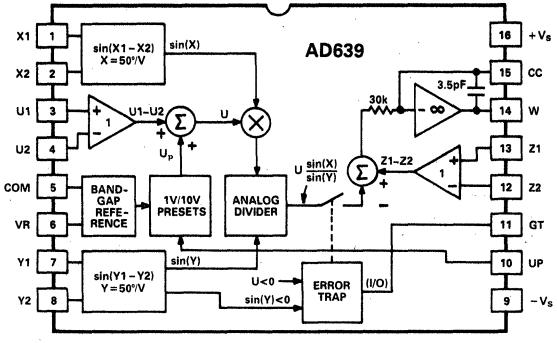
AD630

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
–120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Closed Loop Gain Error %	Input Offset Voltage μV	Input Bias Current nA	Switching Window mV	Response Time (–5μV to +5 mV Step) ns	Unity Gain Bandwidth MHz	Slew Rate V/μs	Temp. Range[2]	Volume* Section Page
AD630JN (AD)	0.1 typ	500	300	±1.5	200	2	45	C/I	I-6-57
AD630KN (BD)	0.05	100	300	±1.5	200	2	45	C/I	I-6-57
AD630SD	0.1 typ	500	300	±1.5	200	2	45	E	I-6-57

NOTES
[1]Suffix "N" – Plastic DIP; Suffix "D" – Ceramic DIP.
[2]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



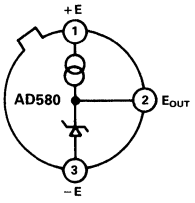
AD639

Complete, Fully-Calibrated Synthesis System
All Standard Functions: Sin, Cos, Tan, Cosec, Sec, Cot, Arcsin, Arccos, Arctan, etc.
Accurate Law Conformance (Sine to 0.02%)
Angular Range of ±500° (Sine Mode)
Function Programmable by Pin Strapping
1.5MHz Bandwidth (Sine Mode)
Multiplication via External Amplitude Input

SPECIFICATIONS – Min or Max at T_A = +25°C

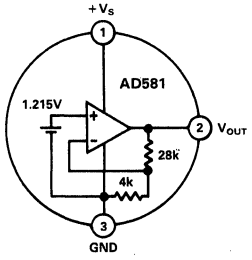
Model[1]	Law Conformance –90° to +90° %	Peak Error –180° to +180° % of F.S.	Scale Factor °/V	Bandwidth MHz	Slew Rate V/μs	Temp. Range[2]	Volume* Section Page
AD639AD	0.02	1.5	50	1.5	30	I	S-3-123
AD639BD	0.02	0.8	50	1.5	30	I	S-3-123
AD639SD	0.02	1.5	50	1.5	30	E	S-3-123

NOTES
[1]Suffix "D" – Ceramic DIP.
[2]I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



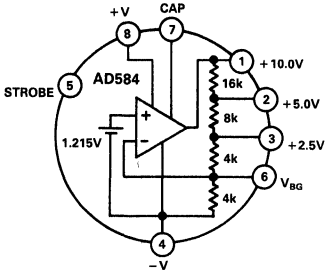
AD580

Laser-Trimmed to High Accuracy: 2.500V ±0.4%
3-Terminal Device: Voltage In/Voltage Out
Excellent Temperature Stability: 10ppm/°C (AD580M, U)
Excellent Long Term Stability: 250μV (25μV/Month)
Low Quiescent Current: 1.5mA max
Small, Hermetic IC Package: TO-52 Can



AD581

Laser-Trimmed to High Accuracy: 10.000 Volts ±5mV (L and U)
Trimmed Temperature Coefficient: 5ppm/°C max, 0 to +70°C (L) 10ppm/°C max, −55°C to +125°C (U)
Excellent Long-Term Stability: 25ppm/1000 hrs. (Non-Cumulative)
Negative 10 Volt Reference Capability
Low Quiescent Current: 1.0mA max
10mA Current Output Capability
3-Terminal TO-5 Package



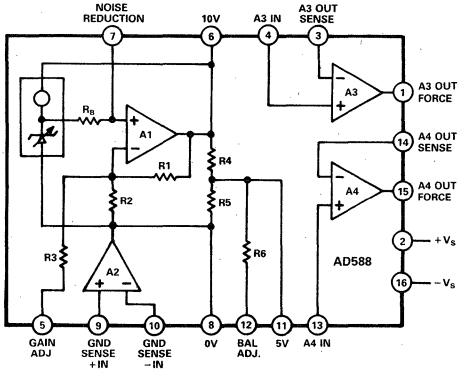
AD584

Four Programmable Output Voltages: 10.000V, 7.500V, 5.000V, 2.500V
Laser-Trimmed to High Accuracies
No External Components Required
Trimmed Temperature Coefficient: 5ppm/°C max, 0 to 70°C (AD584LH) 15ppm/°C max, −55°C to +125°C (AD584TH)
Zero Output Strobe Terminal Provided
Two Terminal Negative Reference Cabability (5V & Above)
Output Sources or Sinks Current
Low Quiescent Current: 1.0mA max
10mA Current Output Capability

SPECIFICATIONS – Min or Max at T_A = +25°C

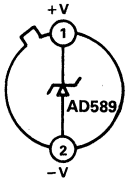
Model[1]	Output Voltage V	Output Voltage Tolerance % Error	Output Current mA	Temp. Stability ppm/°C, max	Time Stability typ	Temp. Range[2]	Volume* Section Page
AD580JH(KH)(LH)(MH)	2.5	3.0(1.0)(0.4)(0.4)	10	85(40)(25)(10)	25μV/Month 250μV Long Term	C	I-7-5
AD580SH(TH)(UH)	2.5	1.0(0.4)(0.4)	10	55(25)(10)	25μV/Month 250μV Long Term	E	I-7-5
AD581JH(KH)(LH)	10.00	±0.3(0.1)(0.05)	10	30(15)(5)	25ppm per 1000 Hours Noncumulative	C	I-7-9
AD581SH(TH)(UH)	10.00	±0.3(0.1)(0.05)	10	30(15)(10)	25ppm per 1000 Hours Noncumulative	E	I-7-9
AD584JH(SH)	Programmable	±0.3	10	30	25ppm per	C/E	I-7-17
AD584KH(TH)		±0.1	10	15	1000 Hours	C/E	I-7-17
AD584LH		±0.5	10	5	Noncumulative		I-7-17

NOTES
[1]Suffix "H" – metal header.
[2]C = 0 to +70°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



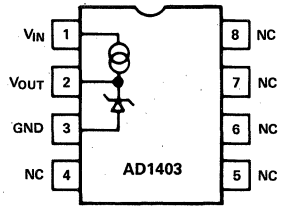
AD588

Ultra-Low Drift: 1ppm/°C
Ultra-Low Initial Error: 1mV
Pin-Programmable Output
+10V, +5V, ±5V Tracking, −5V, −10V
Flexible Output Force and Sense Terminals
Machine-Insertable DIP Packaging
Guaranteed Long-Term Stability:
25ppm/1000 hours



AD589

Superior Replacement for Other 1.2V References
Wide Operating Range: 50μA to 5mA
Low Power: 60μW Total P_D at 50μA
Low Temperature Coefficient:
10ppm/°C max, 0 to +70°C (AD589M)
25ppm/°C max, −55°C to +125°C (AD589U)
Two Terminal "Zener" Operation
Low Output Impedance: 0.6Ω
No Frequency Compensation Required



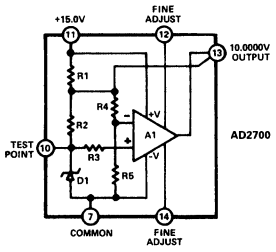
AD1403

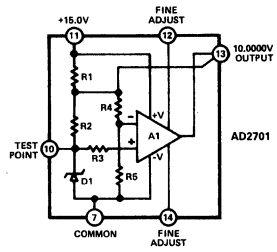
Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser-Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Output Voltage V	Output Voltage Tolerance % Error	Output Current mA	Temp. Stability ppm/°C	Time Stability max	Temp. Range[2]	Volume* Section Page
AD588JN(AD)(SD)	±10.0	0.03	10	3		C/I/E	S-3-99
AD588KN(BD)	±10.0	0.01	10	1		C/I	S-3-99
AD588LN(CD)	±10.0	0.01	10	1	25ppm per 1000 Hours	C/I	S-3-99
AD588TD	±10.0	0.03	10	3	25ppm per 1000 Hours	E	S-3-99
AD589JH(KH)(LH)(MH)	1.235	−2.8, +1.2	5	100(50)(25)(10)		C	I-7-25
AD589SH(TH)(UH)	1.235	−2.8, +1.2	5	100(50)(25)		E	I-7-25
AD1403N	2.50	1	10	40		C	I-7-29
AD1403AN	2.50	0.4	10	25		C	I-7-29

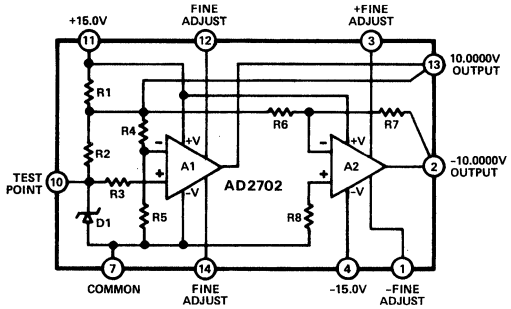
NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "H" – metal header.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.





AD2700/AD2701

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed −55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected



AD2702

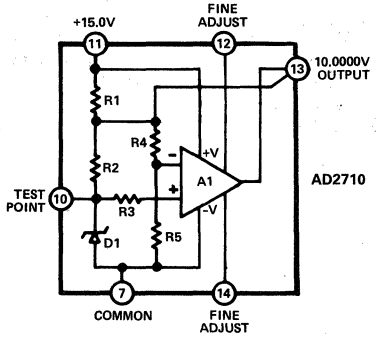
Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed −55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Output Voltage V	Output Voltage Tolerance % Error	Output Current mA	Temp. Stability ppm/°C	Time Stability typ	Temp. Range[1]	Volume* Section Page
AD2700J(S)	10.00	±0.05	10	10(3)	100ppm per	I/E	I-7-33
AD2700L(U)	10.00	±0.025	10	3	1000 Hours	I/E	I-7-33
AD2701J(S)	−10.00	±0.05	10	10(3)	100ppm per	I/E	I-7-33
AD2701L(U)	−10.00	±0.025	10	3	1000 Hours @ +55°C	I/E	I-7-33
AD2702J(S)	±10.00	±0.05	10	10(5)	100ppm per	I/E	I-7-33
AD2702L(U)	±10.00	±0.025	10	5(3)	1000 Hours @ +55°C	I/E	I-7-33

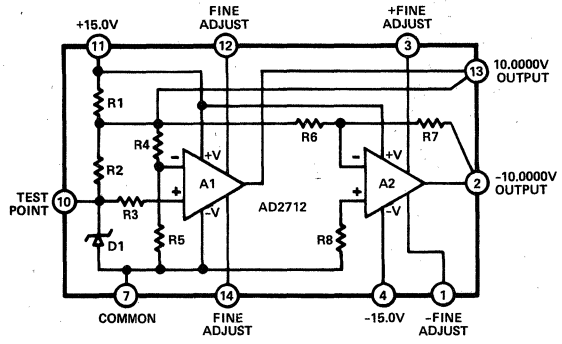
NOTES
[1]I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Voltage References



AD2710

Laser-Trimmed to High Accuracy: 10.000V ±1.0mV
Low Temperature Coefficient: 1ppm/°C (L Grade)
Excellent Long Term Stability: 25ppm/1000 hours
5mA Output Current Capability
Low Noise (30μV p-p)
Short Circuit Protected
No Heater Utilized



AD2712

Laser-Trimmed to High Accuracy: 10.000V ±1.0mV
Low Temperature Coefficient: 1ppm/°C (L Grade)
Excellent Long Term Stability: 25ppm/1000 hours
5mA Output Current Capability
Low Noise (30μV p-p)
Short Circuit Protected
No Heater Utilized

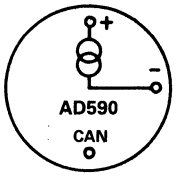
SPECIFICATIONS – Min or Max at T_A = +25°C

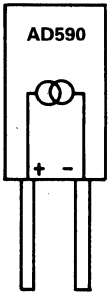
Model[1]	Output Voltage V	Output Voltage Tolerance % Error	Output Current mA	Temp. Stability ppm/°C	Temp. Range[2]	Volume* Section Page
AD2710KN(LN)	±10.00	±0.01	10	2(1)	C	I-7-37
AD2712KN(LN)	±10.00	±0.01	10	2(1)	C	I-7-37

NOTES
[1]Suffix "N" – plastic mini-DIP.
[2]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Temperature Measurement Components

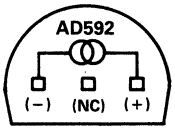
Temperature Transducers





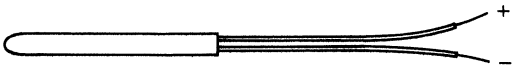
AD590

Linear Current Output: 1μA/K
Wide Range: −55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser-Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case



AD592

High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/Current Out
Minimal Self-Heating Errors



AC2626

Linear Current Output: 1μA/K
Wide Range: −55°C to +150°C
Laser Trimmed Sensor (AD590) to ±0.5°C Calibration Accuracy (AC2626M)
Excellent Linearity: ±0.3°C Over Full Range (AC2626M)
6 Inch or 4 Inch Standard, Stainless Steel Sheath
3/16 Inch in Outside Diameter
3 Feet Teflon Coated Lead Wire
Wide Power Supply Range +4V to +30V
Fast Response: 2 Seconds (In Stirred Water)
Sensor Isolated from Sheath

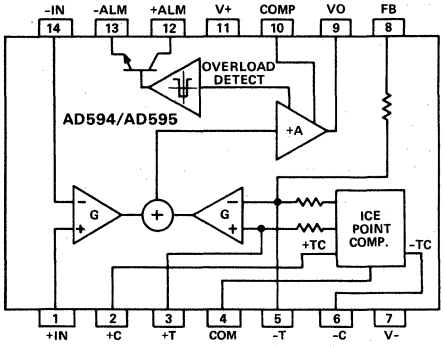
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Nominal Current Output μA	Temp. Coefficient μA/K	Calibration Error °C	Nonlinearity °C	Temp. Range[2]	Volume* Section Page
AD590IH(IF)	298.2	1	±20	±3.0	E	I-8-15
AD590JH(JF)	298.2	1	±10	±1.5	E	I-8-15
AD590KH(KF)	298.2	1	±5.5	±0.8	E	I-8-15
AD590LH(LF)	298.2	1	±3.0	±0.4	E	I-8-15
AD590MH(MF)	298.2	1	±1.7	±0.3	E	I-8-15
AD592AN	298.2	1	±3.0	±0.35	I	S-3-103
AD592BN	298.2	1	±1.5	±0.25	I	S-3-103
AD592CN	298.2	1	±0.8	±0.15	I	S-3-103
AC2626J4(J6)[3]	298.2	1	±5	±1.5	E	II-9-13
AC2626K4(K6)[3]	298.2	1	±2.5	±0.8	E	II-9-13
AC2626L4(L6)[3]	298.2	1	±1.0	±0.4	E	II-9-13
AD2626M4(M6)[3]	298.2	1	±0.5	±0.3	E	II-9-13

NOTES
[1]Suffix "H" – metal header; Suffix "F" – flat package; Suffix "N" – plastic mini-DIP.
[2]I = −25°C to +105°C, E = −55°C to +150°C.
[3]4 = 4-inch length; 6 = 6-inch length.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

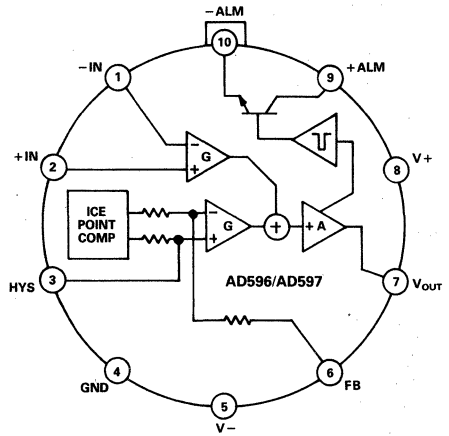
Temperature Measurement Components

Temperature Transducer Signal Conditioners



AD594/AD595

Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples
Can Be Used with Type T Thermocouple Inputs
Low Impedance Voltage Output: 10mV/°C
Built-In Ice Point Compensation
Wide Power Supply Range: +5V to ±15V
Low Power: <1mW typical
Thermocouple Failure Alarm
Laser Wafer-Trimmed to 1°C Calibration Accuracy
Set-Point Mode Operation
Self-Contained Celsius Thermometer Operation
High Impedance Differential Input
Side-Brazed DIP or Low Cost CERDIP



AD596/AD597

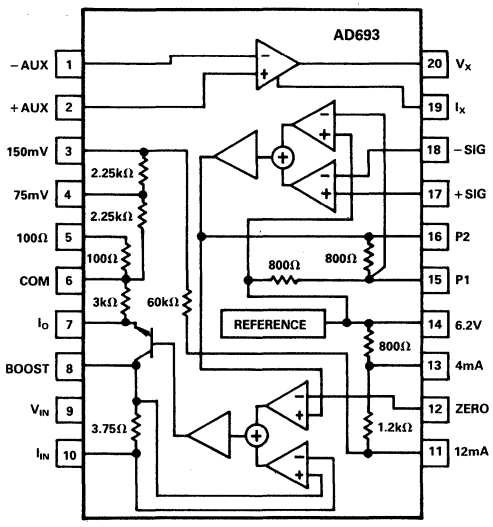
Low Cost
Operates with Type J (AD596) or Type K (AD597) Thermocouples
Built-In Ice Point Compensation
Temperature Proportional Operation – 10mV/°C
Temperature Set-Point Operation – ON/OFF
Programmable Switching Hysteresis
High Impedance Differential Input

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Nominal Transfer Function mV/°C	Closed Loop Gain	Calibration Error °C	Stability vs. Temperature °C/°C	Gain Error %	Volume* Section Page
AD594AD(AQ)	10	193.4	±3.0	±0.05	±1.5	I-8-31
AD594CD(CQ)	10	193.4	±1.0	±0.025	±0.75	I-8-31
AD595AD(AQ)	10	193.4	±3.0	±0.05	±1.5	I-8-31
AD595CD(CQ)	10	193.4	±1.0	±0.025	±0.75	I-8-31
AD596AH	10	180.6	±4.0	±0.05	±1.5	I-8-39
AD597AH	10	245.5	±4.0	±0.05	±1.5	I-8-39

NOTES
[1]Suffix "D" – ceramic DIP; Suffix "Q" – cerdip; Suffix "H" – metal header.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

4-20mA Sensor Transmitters



AD693

Loop-Powered Operation
Precalibrated 30mV or 60mV Input Spans
Precalibrated 100 Ω RTD Interface
Independently Adjustable Output Span and Zero
Precalibrated Output Spans: 4-20mA Unipolar
0-20mA Unipolar
12 ±8mA Bipolar
6.2V Reference with 3.5mA Current Available
Uncommitted Auxiliary Amp for Extra Flexibility
Optional External Pass Transistor to Reduce Self-Heating Errors

2

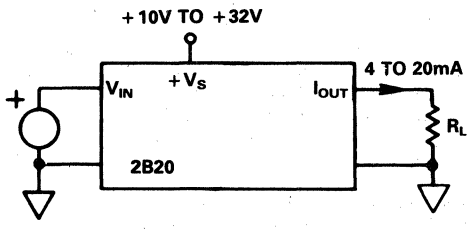
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	+V_S Range V	4mA Offset µA	Gain Accuracy 30mV +60mV FS %	Nonlinearity %	Bias Current nA	CMRR dB	PSRR dB	Temp. Range[2]	Volume* Section Page
AD693AD(AQ)	+12 to +34	80	0.5	0.02	20	95	100	I/I	S-3-161
AD693BD(BQ)	+12 to +34	40	0.25	0.02	10	95	100	I/I	S-3-161

NOTES
[1]Suffix "D" – ceramic DIP; Suffix "Q" – Cerdip.
[2]I = –40°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

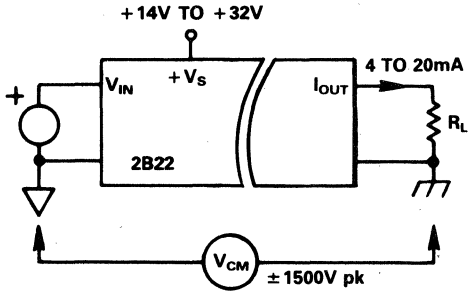
Temperature Measurement Components

Voltage-to-Current Converters



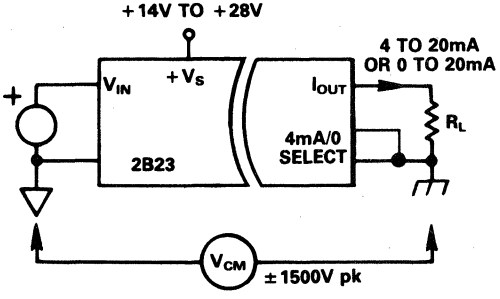
2B20

Complete, No External Components Needed
Small Size: 1.1″ × 1.1″ × 0.4″ Module
Input: 0 to +10V; Output 4 to 20mA
Low Drift: 0.005%/°C max: Nonlinearity: 0.005% max (2B20B)
Wide Temperature Range: −25°C to +85°C
Single Supply: +10V to +32V
Meets ISA Std. 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters



2B22

Wide Input Range: 0 to +1V to 0 to +10V
Standard Output Range: 4 to 20mA
High CMV Input/Output Isolation: 1500V dc Continuous
Low Nonlinearity: 0.05% max, 2B22L
Low Span Drift: 0.005%/°C max, 2B22L
Single Supply: +14V to +32V
Meets IEEE Std. 472: Transient Protection (SWC)
Meets ISA Std. 50.1: Isolated Current Loop Transmitters



2B23

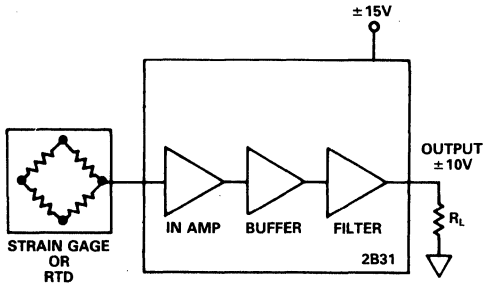
Wide Input Range, Resistor Programmable
Pin Programmable Output: 4 to 20mA or 0 to 20mA
High CMV Input/Output Isolation: ±1500V pk Continuous
Low Nonlinearity: ±0.05% max (2B23K)
Low Span Drift: ±0.005%/°C max (2B23K)
Single Supply Operation: +14V to +28V
Small Size: 1.8″ × 2.4″ × 0.6″
Meets IEEE Std. 472: Transient Protection (SWC)
Meets ISA ST. 50.1: Isolated Current Loop Transmitters

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Input Range V	Output Range mA	Gain Nonlinearity %	CMV In/Out V pk	Temp. Range[1]	Volume* Section Page
2B20A	0 to +10	4 to 20	0.025	N/A	I	II-9-15
2B20B	0 to +10	4 to 20	0.005	N/A	I	II-9-15
2B22J	0 to +10 0 to +1	4 to 20	0.2	1500	C	II-9-19
2B22K	0 to +10 0 to +1	4 to 20	0.1	1500	C	II-9-19
2B22L	0 to +10 0 to +1	4 to 20	0.05	1500	C	II-9-19
2B23J	0 to +10	4 to 20 0 to 20	0.1	1500	C	II-9-23
2B23K	0 to +10	4 to 20 0 to 20	0.05	1500	C	II-9-23

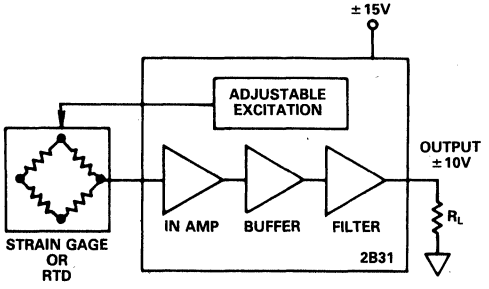
NOTES
[1]C = 0 to +70°C, I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Strain Gage/RTD Conditioners



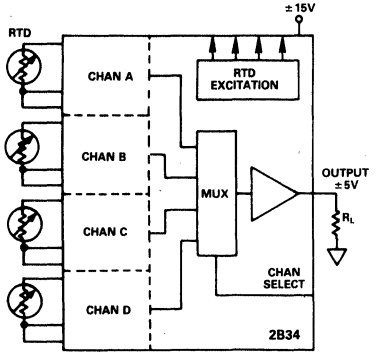
2B30

Complete Signal Conditioning Function
Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
Wide Gain Range: 1 to 2000V/V
Low Nonlinearity: 0.0025% max ("L")
High CMR: 140dB min (60Hz, G = 1000V/V)
Input Protected to 130V rms
Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)



2B31

Complete Signal Conditioning Function
Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
Wide Gain Range: 1 to 2000V/V
Low Nonlinearity: 0.0025% max ("L")
High CMR: 140dB min (60Hz, G = 1000V/V)
Input Protected to 130V rms
Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)
Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)



2B34

Low Input Offset Drift: ±1.0μV/°C
Low Gain Drift: ±25ppm/°C
Low Nonlinearity: ±0.01% max (±0.005% typ)
Differential Input Protection: ±130V rms
Channel Multiplexing: 3000 chan/sec Scanning Speed
Solid State Reliability
Internal RTD Excitation/Lead Wire Compensation

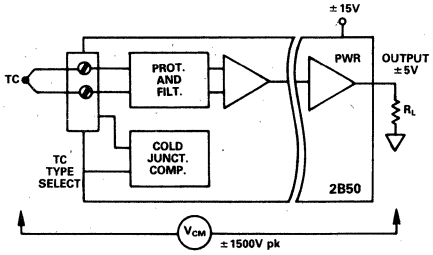
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Gain Range V/V	Gain Nonlinearity %	Input T.C. μV/C	Bandwidth −3dB kHz typ	Temp. Range[1]	Volume* Section Page
2B30J	1 to 2000	0.01	3	30	C	II-9-29
2B30K	1 to 2000	0.005	1	30	C	II-9-29
2B30L	1 to 2000	0.0025	0.5	30	C	II-9-29
2B31J	1 to 2000	0.01	3	30	C	II-9-29
2B31K	1 to 2000	0.005	1	30	C	II-9-29
2B31L	1 to 2000	0.0025	0.5	30	C	II-9-29
2B34J	50 to 1000	0.01	1	0.004	C	II-9-35

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

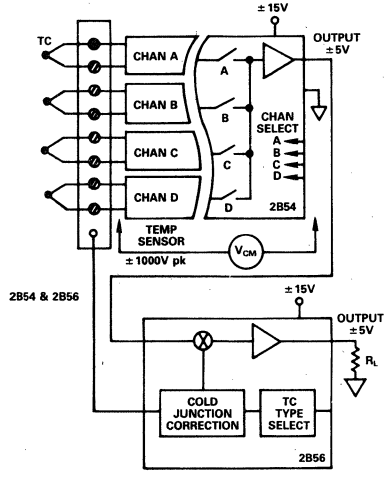
Temperature Measurement Components

Isolated Transducer Signal Conditioners



2B50

Accepts J, K, T, E, R, S or B Thermocouple Types
Internally Provided Cold Junction Compensation
High CMV Isolation: ±1500V pk
High CMR: 160dB min @ 60Hz
Low Drift: ±1μV/°C max (2B50B)
High Linearity: ±0.01% max (2B50B)
Input Protection and Filtering
Screw Terminal Input Connections

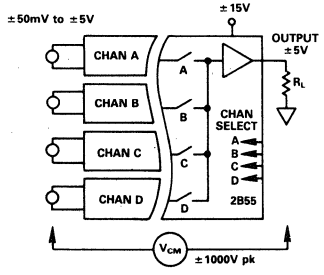


2B54

Low Cost
Wide Input Span Range: ±5mV to ±100mV
12-Bit Systems Compatible
High CMV Isolation: ±1000V dc; CMR = 156dB min @ 60Hz
Low Input Offset Voltage Drift: ±1μV/°C max (2B54B)
Low Gain Drift: ±25ppm/°C max (2B54B)
Low Nonlinearity: ±0.02% max (±0.012% typ)
Normal Mode Input Protection (130V rms) and Filtering
Channel Multiplexing: 400 chan/sec Scanning Speed
Solid State Reliability

2B56

Universal Thermocouple Compensation
Internally Provided: Types J, K, T
User Configurable: Types E, R, S, B
Digitally Programmable
High Accuracy: ±0.8°C max over +5°C to +45°C
High Ambient Rejection: 50 to 1 min
Low Cost
Small Size: 1.5" × 2" × 0.4"



2B55

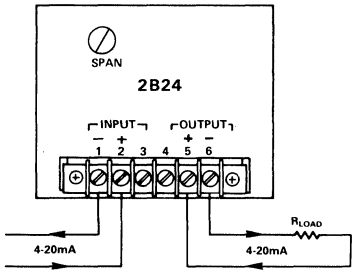
Low Cost
Wide Input Span Range: ±50mV to ±5V
12-Bit Systems Compatible
High CMV Isolation: ±1000V dc; CMR = 145dB min @ 60Hz
Low Input Offset Voltage Drift: ±5μV/°C max
Low Gain Drift: ±25ppm/°C max
Low Nonlinearity: ±0.02% max (G = 1 to 100)
Normal Mode Input Protection (130V rms) and Filtering
Channel Multiplexing: 400 chan/sec Scanning Speed
Solid State Reliability

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Gain Range V/V	Gain Nonlinearity %	Input T.C.[1] μV/C	CMR dB	CMV In/Out V pk	Temp. Range[2]	Volume* Section Page
2B50A	50 to 1000	0.025	2.5	160	1500	C	II-9-41
2B50B	50 to 1000	0.01	1	160	1500	C	II-9-41
2B54A	50 to 1000	0.03	2.5	156	1000	C	II-9-47
2B54B	50 to 1000	0.02	1	156	1000	C	II-9-47
2B55A	1 to 100	0.02	5	145	1000	C	II-9-47
2B56A	1	0.2°C[3]	15	N/A	N/A	C	II-9-53

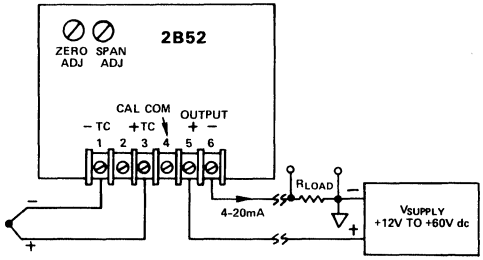
NOTES
[1]At maximum gain.
[2]C = 0 to +70°C.
[3]Total output error.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Two-Wire Transmitters



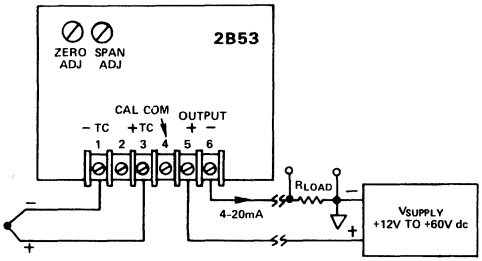
2B24

Self-Powered
Wide Input Range: 1-50mA (2B24B)
High CMV Isolation: ±1500V pk; CMR: 120dB
High Accuracy: ±0.1%
RFI/EMI Immunity
Low Cost



2B52

Accepts Type J, K or T Thermocouple Inputs
Compatible with Standard 4-20mA Loops
High Accuracy: ±0.1%
High CMV Isolation: 600V rms; CMR = 160dB
High Noise Rejection and RFI Immunity
Internal Cold Junction Compensation
Open Thermocouple Detection
Millivolt Signal Transmission
Low Cost
FM Approved



2B53

Accepts Type J, K or T Thermocouple Inputs
Compatible with Standard 4-20mA Loops
High Accuracy: ±0.1%
High Noise Rejection and RFI Immunity
Internal Cold Junction Compensation
Open Thermocouple Detection
Millivolt Signal Transmission
Low Cost

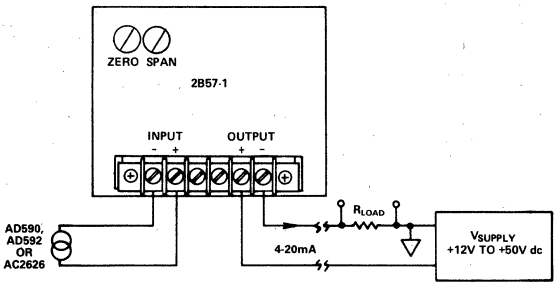
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Input mV or Sensor	Output Signal mA	Output Error %	CMV In/Out V pk	Temp. Range[1]	Volume* Section Page
2B24A	4 to 20	4 to 20	0.1	1500	I	II-9-27
2B24B	4 to 20	4 to 20	0.1	1500	I	II-9-27
	10 to 50	10 to 50				
2B52A	J/K/T	4 to 20	0.1	800	I	II-9-45
2B53A	J/K/T	4 to 20	0.1	N/A	I	II-9-45

NOTES
[1]I = –25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

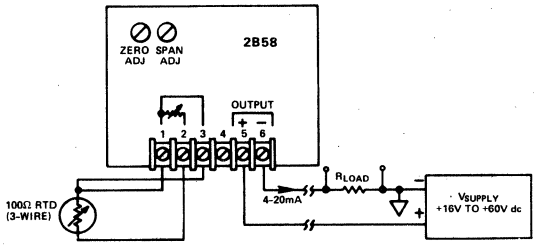
Temperature Measurement Components

Two-Wire Transmitters



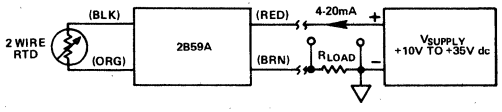
2B57 – 1

Compatible with Standard 4-20mA Loops
Low Span Drift: ±0.005%/°C max
Low Nonlinearity: ±0.05% max
RFI Immunity
Small Size: 1.5" × 1.5" × 0.4"
Low Cost Module Available
Model 2B57A



2B58A

Platinum RTD Input
Linearized 4-20mA Output
High Accuracy: ±0.1%
Low Drift: ±0.01°C/°C max
RFI Immunity
Low Cost
FM Approved



2B59A

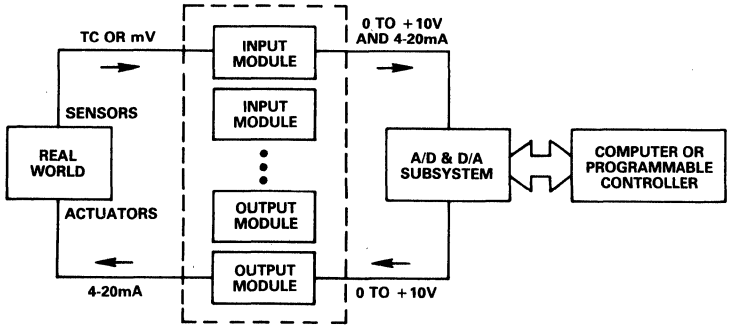
Low Cost
Standard RTD Input
Linearized 4-20mA Output
High Accuracy: ±0.1%
Small Size
Ease of Installation

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Package	Sensor Type	Output Range mA	Output Error %	Response Time ms	Temp. Range[1]	Volume* Section Page
2B57–1	Aluminum Case	AD590	4 to 20	0.05	150	I	II-9-57
2B57A	Module	AD590	4 to 20	0.05	150	I	II-9-57
2B58A	Aluminum Case	RTD	4 to 20	0.1	400	I	II-9-61
2B59A	Module	RTD	4 to 20	0.1	125	I	II-9-63

NOTES
[1]I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

3B Series Signal Conditioning I/O Subsystems



Input Module Selection

Input Type/Span	Voltage Output	Current Output	Nonisolated Modules	Isolated Modules	Volume* Section Page
dc, ± 10mV, ± 50mV, ± 100mV	± 10V	4-20mA/0-20mA	3B10	3B30	II-9-65
dc, ± 1V, ± 5V	± 10V	4-20mA/0-20mA	3B10	3B31	II-9-65
dc, ± 10V	± 10V	4-20mA/0-20mA	3B11	3B31	II-9-65
dc, 4-20mA, 0-20mA	0 to + 10V	4-20mA/0-20mA	3B12	3B32	II-9-65
Thermocouple Types J, K, T, E, R, S, B	0 to + 10V	4-20mA/0-20mA		3B37	II-9-65
Thermocouple Types J, K, T, E, R, S, B (linearized)	0 to + 10V	Not Available		3B47	II-9-65
AD590/AD592/AC2626 Solid State Temperature Transducer	0 to + 10V	4-20mA/0-20mA	3B13		II-9-65
100Ω Platinum RTD, 2-, 3-, 4-Wire $\alpha = 0.00385$ (linearized)	0 to + 10V	4-20mA/0-20mA	3B14	3B34	II-9-65
100Ω Platinum RTD, Kelvin 4-Wire $\alpha = 0.00385$ (linearized)	0 to + 10V	4-20mA/0-20mA	3B15		II-9-65
Strain Gage ± 30mV, ± 100mV	± 10V	4-20mA/0-20mA	3B16		II-9-65
Wideband Strain Gage	± 10V	4-20mA/0-20mA	3B18		II-9-65
LVDT, 4, 5, 6-Wire	± 10V	4-20mA/0-20mA	3B17		S-4-47
Wideband mV, V	± 10V	4-20mA/0-20mA		3B40/1	II-9-65
AC Input	0 to + 10V	4-20mA/0-20mA		3B42/3/4	II-9-65
Frequency Input	0 to + 10V	4-20mA/0-20mA		3B45/6	II-9-65

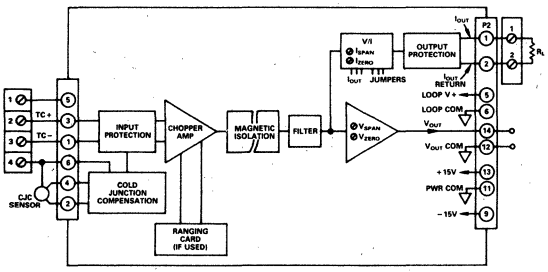
Output Module Selection

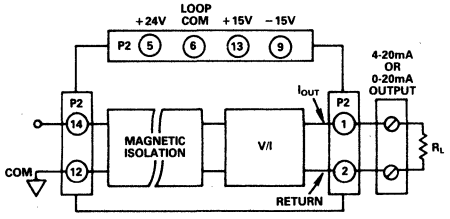
Input Type/Span	Current Output	Nonisolated Modules	Isolated Modules	Volume* Section Page
0 to + 10V, ± 10V	4-20mA/0-20mA	3B19	3B39	II-9-67

NOTE
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Temperature Measurement Components

3B Series I/O Subsystems





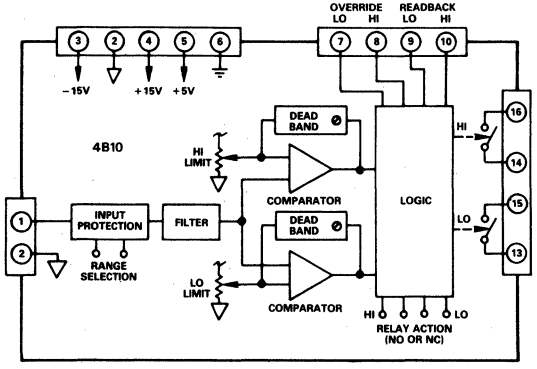
Input Modules

Wide Variety of Sensor Inputs: Thermocouples, RTD's, Strain Gages, AD590/AD592/AC2626, LVDT
Dual High Level Outputs
Voltage: 0 to +10V or ±10V
Current: 4-20mA/0-20mA
Mix and Match Input Capability
Sensor Signals, mV, V, 4-20mA, 0-20mA
High Accuracy: ±0.1%
High Noise Rejection and RFI/EMI Immunity
Reliable Transformer Isolation: ±1500V CMV
Meets IEEE-STD 472: Transient Protection (SWC)
Input Protection: 130V or 220V rms Continuous

Output Modules

High Level Voltage Input: (0 to +10V, ±10V)
Process Current Output: (4-20mA/0-20mA)
High Accuracy: ±0.1%
Reliable Transformer Isolation: ±1500V CMV, CMR=90dB
Meets IEEE-STD 472: Transient Protection (SWC)
Output Protection: 130V or 220V rms Continuous

4B Series Alarm Limit Subsystem

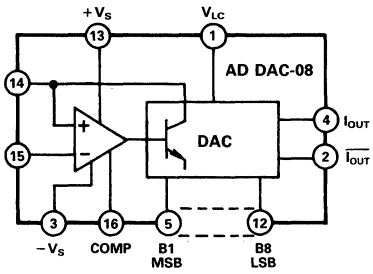


Features/Benefits

Low Cost, Completely Integrated 12-Channel Modular Alarm Limit Subsystem
Selection of Alarm Limit Modules
Rugged Industrial chassis, Rack or Surface Mounted
On-Board Power Supplies Available
Alarm Modules Accept High Level Voltage and Process Current Inputs
Complete Alarm Function per Module
High Accuracy of ±0.1%
Two Set Points, Adjustable Over 100% Span
Dead Band Adjustment per Set Point, Adjustable Over 0.5% – 10.0% Span
Alarm Types are Configurable for HI or LO Operation
Two Relay Outputs
Display Indicates Set Points and Process Variable
LED per Set Point Provides Local Alarm Indication
Input Protection
High RFI/EMI Immunity
Specifications Valid Over the 0 to +70°C Temperature Range
Easy to Install Calibrate and Service

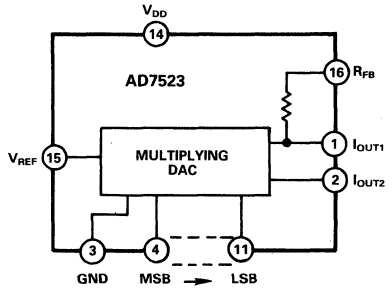
Digital-to-Analog Converters

General Purpose 8-Bit



AD DAC-08

Exact Replacement for Industry Standard DAC-08
Fast (85ns typical) Settling Time
Linearity Error ±1/4LSB (±0.1%) Guaranteed Over Full Temperature Range
Wide Output Voltage Compliance: −10V to +18V
Single Chip Monolithic Construction
16-Pin Cerdip Packaging



AD7523

8 Bits of Resolution
Fast Settling: 100ns
Low Power: CMOS
Low Feedthrough: 1/2LSB @ 200kHz
Full Four-Quadrant Multiplying

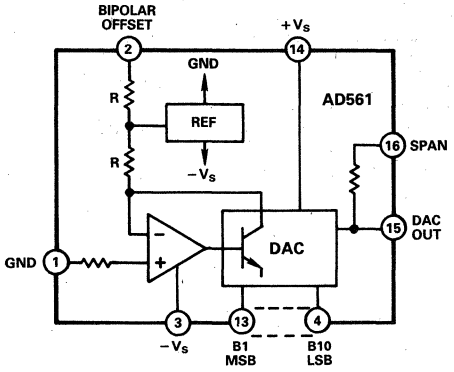
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy %	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time ns	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD DAC-08D	8	±0.19	Monotonicity	50	135	I	TTL &	E	I-9-265
AD DAC-08AD	8	±0.1	Guaranteed	50	135	I	CMOS	E	I-9-265
AD DAC-08CD	8	±0.39		80	135	I		C	I-9-265
AD DAC-08ED	8	±0.19		50	135	I		C	I-9-265
AD DAC-08HD	8	±0.1		50	135	I		C	I-9-265
AD7523JN	8	±0.2	Monotonicity	66/50/30	150 typ	I	CMOS	C	I-9-167
AD7523KN	8	±0.1	Guaranteed	66/50	150 typ	I		C	I-9-167
AD7523LN	8	±0.05		66/50	150 typ	I		C	I-9-167

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – cerdip.
[2]C = 0 to +70°C; E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

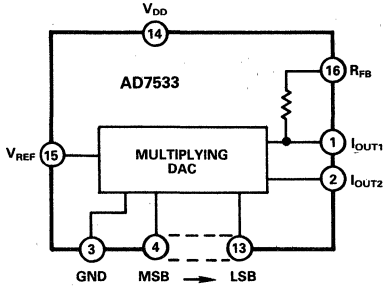
Digital-to-Analog Converters

General Purpose 10-Bit



AD561

Complete Current Output Converter
High Stability Buried Zener Reference
Laser Trimmed to High Accuracy (1/4 LSB Max Error, AD561K, T)
Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
Fast Settling – 250ns to 1/2LSB
Guaranteed Monotonicity Over Full Operating Temperature Range
TTL and CMOS Compatible (Positive True Logic)
Single Chip Monolithic Construction
Hermetically-Sealed Ceramic and Plastic DIPs



AD7533

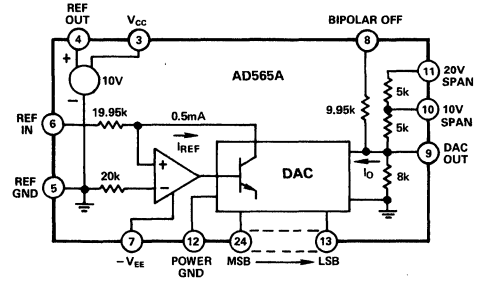
Lowest Cost 10-Bit DAC
Low Cost AD7520 Replacement
Linearity: 1/2, 1 or 2LSB
Low Power: CMOS
Full Four-Quadrant Multiplying DAC
CMOS/TTL Direct Interface
Latch-Free (Protection Schottky Not Required)
End-Point Linearity

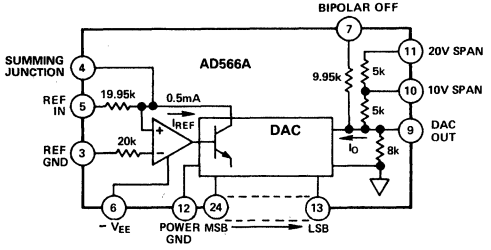
SPECIFICATIONS – Min or Max at T_A = +25°C

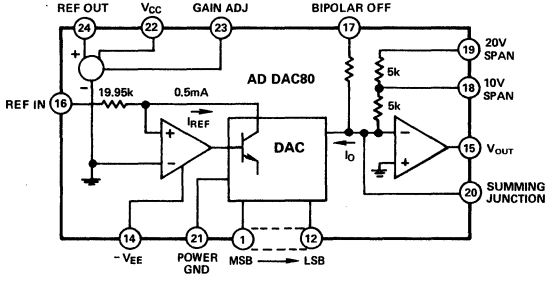
Model[1]	Resolution Bits	Relative Accuracy %	Differential Nonlinearity[2]	Gain T.C. ppm/°C	Settling Time ns	I/V Out	Input Logic	Temp. Range[3]	Volume* Section Page
AD561JN(JD)	10	±0.05	±1/2LSB	±80	250	I	TTL &	C	I-9-43
AD561KN(KD)	10	±0.025	±1/2LSB	±30	250	I	CMOS	C	I-9-43
AD561SD	10	±0.05	±1/2LSB	±60	250	I		E	I-9-43
AD561TD	10	±0.025	±1/2LSB	±30	250	I		E	I-9-43
AD7533JN(AD)(SD)	10	±0.2	±0.4%	22/16/10	600	I	CMOS &	C/I/E	I-9-195
AD7533KN(BD)(TD)	10	±0.1	±0.2%	22/16/10	600	I	TTL	C/I/E	I-9-195
AD7533LN(CD)(UD)	10	±0.05	±0.1%	22/16/10	600	I		C/I/E	I-9-195

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]GMOT – Guaranteed Monotonic Over Temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

General Purpose 12-Bit







AD565A

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 250ns max
Full Scale Switching Time: 30ns
High Stability Buried Zener Reference On Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD565AK, S)
Guaranteed for Operation with ±12V Supplies
Low Power: 225mW Including Reference
Pin-Out Compatible with AD563, AD565

AD566A

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 350ns max
Full Scale Switching Time: 30ns
Guaranteed for Operation with −12V Supply
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD566AK, S)
Low Power: 180mW
Pin-Out Compatible with AD562, AD566

AD DAC80 SERIES

Single Chip Construction
On-Board Output Amplifier
Low Power Dissipation: 300mW
Monotonicity Guaranteed Over Temperature
Guaranteed for Operation with ±12V Supplies
Improved Replacement for Standard DAC80
High Stability, High Current Output Buried Zener Reference
Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity
Low Cost Plastic Packaging
Current Out Models and Voltage Output Models Available

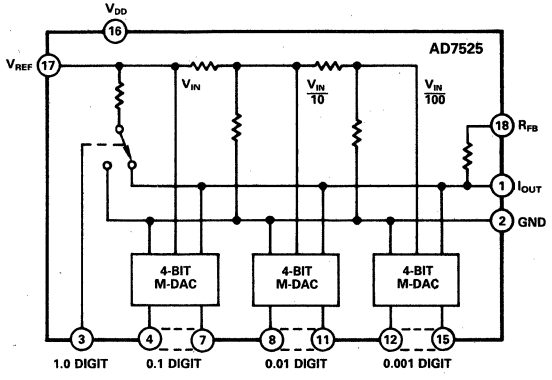
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD565AJD(SD)	12	±1/2	±3/4	50/30	250ns	I	TTL	C/E	I-9-57
AD565AKD	12	±1/4	±1/2	20/15	250ns	I	TTL	C	I-9-57
AD566AJD(SD)	12	±1/2	±3/4	10	350ns	I	TTL	C/E	I-9-65
AD566AKD	12	±1/4	±1/2	3	350ns	I	TTL	C	I-9-65
AD DAC80N-CBI-V[3]	12	±1/2	±3/4	30	3µs	V	TTL	C	I-9-277
AD DAC80D-CBI-V[3]	12	±1/2	±3/4	30	3µs	V	TTL	C	I-9-277
AD DAC80D-CBI-I[3]	12	±1/2	±3/4	30	300ns	I	TTL	C	I-9-277
AD DAC85D-CBI-V[3]	12	±1/2	±3/4	20	3µs	V	TTL	I	I-9-277
AD DAC87D-CBI-V[3]	12	±3/4	±3/4	20	3µs	V	TTL	E	I-9-277
AD DAC80Z-CBI-V[4]	12	±1/2	±3/4	30	3µs	V	TTL	C	I-9-277
AD DAC80Z-CBI-I[4]	12	±1/2	±3/4	30	300ns	I	TTL	C	I-9-277
AD DAC85-CBI-V	12	±1/2	±1/2 typ	20	3µs	V	TTL	I	I-9-277
AD DAC85-CBI-I	12	±1/2	±1/2 typ	20	300ns	I	TTL	I	I-9-277
AD DAC87-CBI-V	12	±1/2	±1/2 typ	20	3µs	V	TTL	E	I-9-277
AD DAC87-CBI-I	12	±1/2	±1/2 typ	20	300ns	I	TTL	E	I-9-277

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C; I = −25°C to +85°C; E = −55°C to +125°C.
[3]Monolithic Technology.
[4]"Z" Models specified for operation on ±12V supplies.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

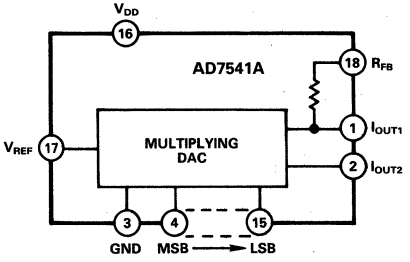
Digital-to-Analog Converters

General Purpose 12-Bit



AD7525

Resolution: 3 1/2 Digit BCD (1999 Counts)
Nonlinearity: ±1/2LSB T_{MIN} to T_{MAX}
Gain Error: ±0.05% FS
Excellent Repeatability Accuracy
Low Power: CMOS



AD7541A

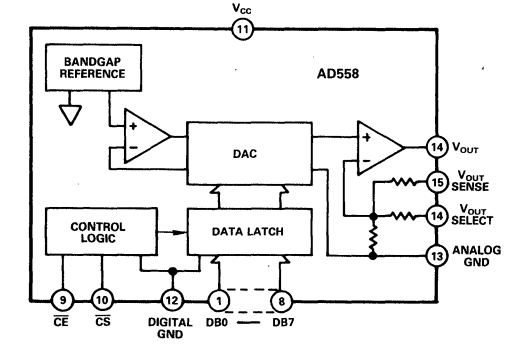
12 Bits of Resolution
Improved Version of AD7541
Full Four Quadrant Multiplication
12-Bit Linearity (End-Point)
±1LSB Gain Error
All Parts Guaranteed Monotonic
TTL/CMOS Compatible
Protection Schottky not Required
Low Logic Input Leakage
Low Power: CMOS

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7525KN(BD)(TD)	3 1/2 Digits	±1	±1	25	1μs	I	CMOS &	C/I/E	I-9-177
AD7525LN(CD)(UD)	3 1/2 Digits	±1/2	±1/2	25	1μs	I	TTL	C/I/E	I-9-177
AD7541AJN(AQ)(SD)	12 Bits	±1	±1	5	600ns typ	I	CMOS &	C/I/E	I-9-209
AD7541AKN(BQ)(TD)	12 Bits	±1/2	±1/2	5	600ns typ	I	TTL	C/I/E	I-9-209

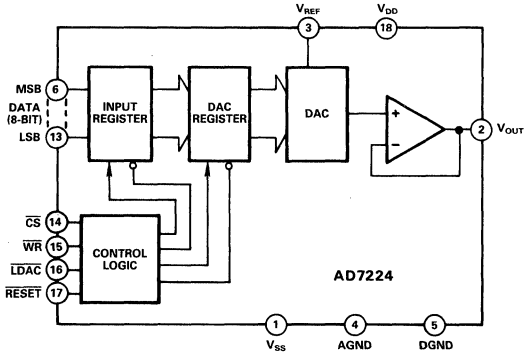
NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

8-Bit μP-Compatible



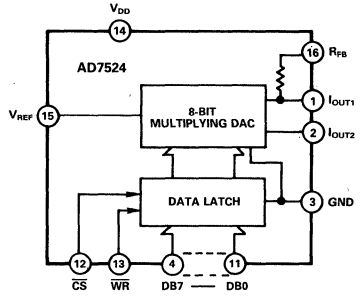
AD558

Complete 8-Bit DAC
Voltage Output −2 Calibrated Ranges
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V to +15V
Full Microprocessor Interface
Fast: 1μs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP Package or PLCC
Single Laser-Wafer-Trimmed Chip for Hybrids



AD7224

8-Bit DAC with Output Amplifier
Full Double Buffering
Microprocessor Compatible
Single Supply Operation
Multiplying Capability
No User Trims
Low Power: CMOS
0.3" Wide 18-Pin DIP



AD7524

Microprocessor Compatible (6800, 8085, Z80, Etc.)
TTL/CMOS Compatible Inputs
On-Chip Data Latches
End Point Linearity
Low Power: CMOS
Monotonicity Guaranteed (Full Temperature Range)
Latch-Free (No Protection Schottky Required)
4 Quadrant Multiplying

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Relative Accuracy	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time max	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD558JN(JD)(SD)	±1/2LSB	Monotonicity	±2LSB	3μs	V	TTL &	C/E	I-9-35
AD558KN(KD)(TD)	±1/4LSB	Guaranteed	±2LSB	3μs	V	CMOS	C/E	I-9-35
AD7224KN(BQ)(TQ)	±1LSB	Monotonicity Guaranteed	20	7μs	V	TTL & CMOS	C/I/E	S-3-175
AD7224LN(CQ)(UQ)	±1/2LSB	Monotonicity Guaranteed	20	7μs	V	TTL & CMOS	C/I/E	S-3-175
AD7524JN(AD)(SD)	±0.2%	Monotonicity	10	100ns	I	TTL &	C/I/E	I-9-171
AD7524KN(BD)(TD)	±0.1%	Guaranteed	10	100ns	I	CMOS	C/I/E	I-9-171
AD7524LN(CD)(UD)	±0.05%		10	100ns	I		C/I/E	I-9-171

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
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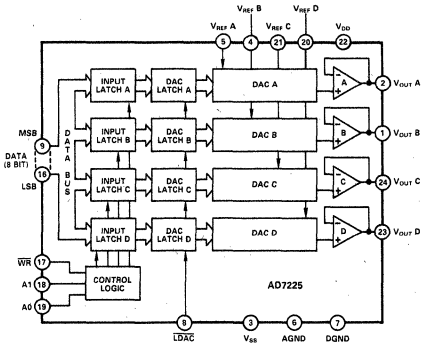
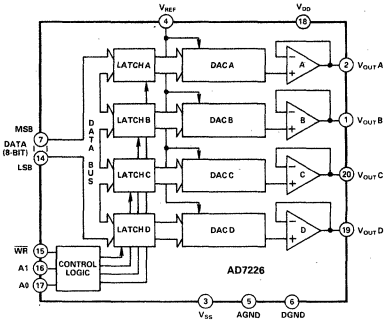
Digital-to-Analog Converters

8-Bit µP-Compatible



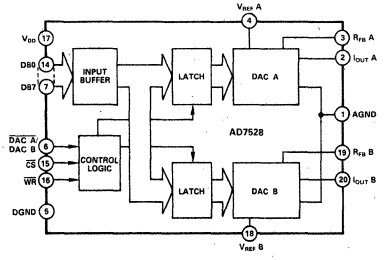
AD7225

Four 8-Bit DACs with Output Amplifiers
Separate Reference Input for Each DAC
µP Compatible with Double-Buffered Inputs
Simultaneous Update of All Four Outputs
Operates with Single or Dual Supplies
No User Trims Required
0.3" Wide, 24-Pin DIP



AD7226

Four 8-Bit DACs with Output Amplifiers
0.3" Wide, 20-Pin DIP
Microprocessor Compatible
TTL/CMOS Compatible
No User Trims
Single Supply Operation Possible
Monolithic CMOS Construction



AD7528

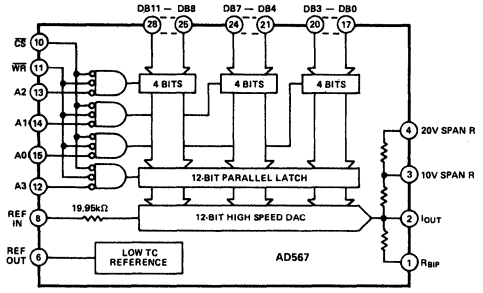
Dual D/A Converter
On-Chip Latches for Both DACs
+5V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch-Free (Protection Schottkys Not Required)
Low Power: CMOS

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Relative Accuracy LSB	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7225KN(BQ)(TQ)	±1	Monotonicity Guaranteed	5	5	V	TTL & CMOS	C/I/E	S-3-183
AD7225LN(CQ)(UQ)	±1/2	Monotonicity Guaranteed	5	5	V	TTL & CMOS	C/I/E	S-3-183
AD7226KN(BQ)(TQ)	±1	Monotonicity Gurauranteed	20	7µs	V	TTL & CMOS	C/I/E	I-9-133
AD7528JN(AQ)(SD)	±1	Monotonicity Guaranteed	35	200ns	C	TTL & CMOS	C/I/E	I-9-183
AD7528KN(BQ)(TD)	±1/2	Monotonicity Guaranteed	35	200ns	C	TTL & CMOS	C/I/E	I-9-183
AD7528LN(CQ)(UD)	±1/2	Monotonicity	35	200ns	C	TTL & CMOS	C/I/E	I-9-183

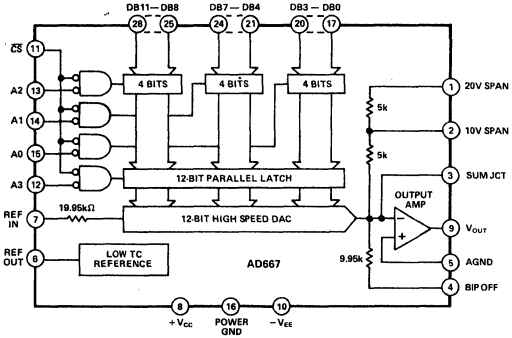
NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

12-Bit μP-Compatible



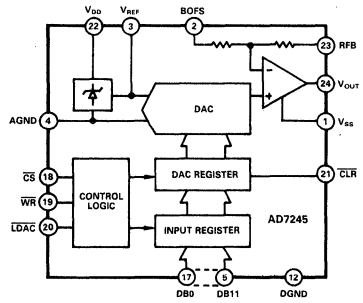
AD567

Single Chip Construction
Double-Buffered Latch for 8-Bit μP Compatibility
Fast Settling Time: 500ns max to ±1/2LSB
High Stability Buried Zener Reference on Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD567K)
Guaranteed for Operation with ±12V or ±15V Supplies
Low Power: 300mW Including Reference
TTL/5V CMOS Compatible Logic Inputs



AD667

Voltage Output
Single Chip Construction
Double-Buffered Latch for 8-Bit μP-Compatibility
Fast Settling Time: 3μs max to ±1/2LSB
High Stability Buried Zener Reference On Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD667K)
Guaranteed for Operation with ±12V or ±15V Supplies
Low Power: 300mW Including Reference
Plastic, Ceramic DIP and LCC Available



AD7245

Complete 12-Bit DAC on a Chip
On-Chip Reference
Buffered Output Voltage
Fast Digital Interface
Low Power CMOS: 60mW
Single or Dual Supply Operation
Unipolar or Bipolar Output
Small 24-Pin 0.3" DIP

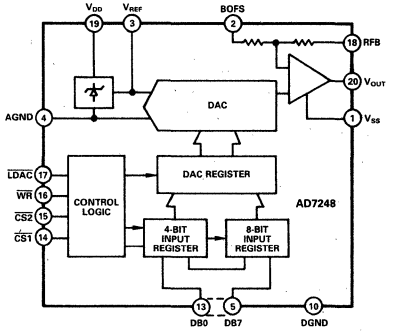
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD567JD(SD)	12	±1/2	±3/4	50/30	500ns	I	TTL &	C/E	I-9-73
AD567KD	12	±1/4	±1/2	20	500ns	I	CMOS	C/C	I-9-73
AD667JN(SD)	12	±1/2	±3/4	30	4μs	V	TTL &	C/E	I-9-83
AD667AD(AE)	12	±1/2	±3/4	30	4μs	V	CMOS	I/I	I-9-83
AD667KN(BD)(BE)	12	±1/4	±1/2	15	4μs	V		C/I/I	I-9-83
AD7245JN(AQ)(SQ)	12	±2	±1	5	5μs	V	TTL &	C/I/E	S-3-195
AD7245KN(BQ)(TQ)	12	±1	±1	5	5μs	V	CMOS	C/I/E	S-3-195

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "E" – leadless chip carrier; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Digital-to-Analog Converters

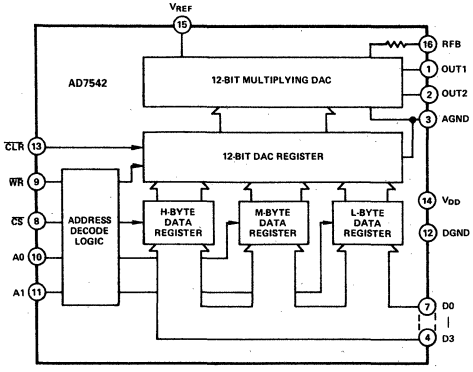
12-Bit µP-Compatible



AD7248

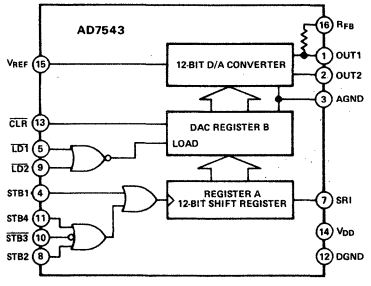
Complete 12-Bit DAC on a Chip
- **On-Chip Reference**
- **Buffered Output Voltage**
- **Fast Digital Interface**

Low Power CMOS: 60mW
Single or Dual Supply Operation
Unipolar or Bipolar Output
Small 20-Pin 0.3" DIP



AD7542

Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
Microprocessor Compatible
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough
Low Power: CMOS
Small Size: 16-Pin DIP



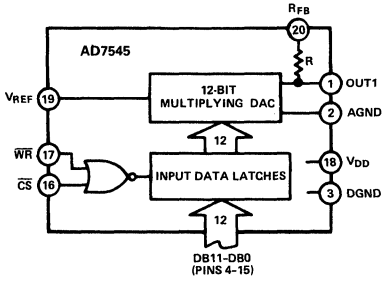
AD7543

Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
Serial Load on Positive or Negative Strobe
Asynchronous CLEAR Input for Initialization
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough: 1LSB max @ 10kHz
Requires no Schottky Diode Output Protection
Low Power: CMOS
+5V Supply
Small Size: 16-Pin DIP

SPECIFICATIONS – Min or Max at T_A = +25°C

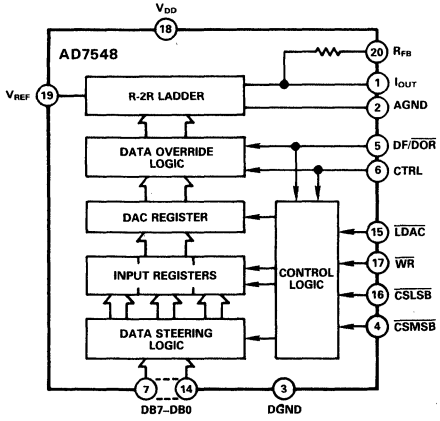
Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time µs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7248JN(AQ)(SQ)	12	±2	±1	5	5	V	TTL &	C/I/E	S-3-195
AD7248KN(BQ)(TQ)	12	±1	±1	5	5	V	CMOS	C/I/E	S-3-195
AD7542JN(AD)(SD)	12	±1	±2	5	–	I	CMOS	C/I/E	I-9-215
AD7542KN(BD)(TD)	12	±1/2	±1	5	–	I		C/I/E	I-9-215
AD7543JN(AD)(SD)	12	±1	±2	5	–	I	CMOS	C/I/E	I-9-223
AD7543KN(BD)(TD)	12	±1/2	±1	5	–	I		C/I/E	I-9-223

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



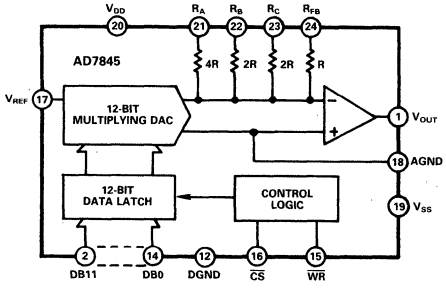
AD7545

Low Gain T.C.: 2ppm/°C typ
Fast TTL Compatible Data Latches
Single +5V to +15V Supply
Small 20-Pin 0.3" DIP
Latch Free (Schottky Protection Diode Not Required)
Ideal for Battery Operated Equipment
Low Power: CMOS



AD7548

8-Bit Bus Compatible 12-Bit DAC
All Grades 12-Bit Monotonic Over Full Temperature Ranges
Operation Specified at +5V, +12V or +15V Power Supply
Low Gain Drift of 5ppm/°C Maximum
Full 4-Quadrant Multiplication
Small 20-Pin Package
Low Power: CMOS



AD7845

12-Bit CMOS DAC with Output Amplifier
4-Quadrant Multiplication
Guaranteed Monotonic (T_{min} – T_{max})
Space Saving 0.3", 24-Pin Package
Low Power: CMOS

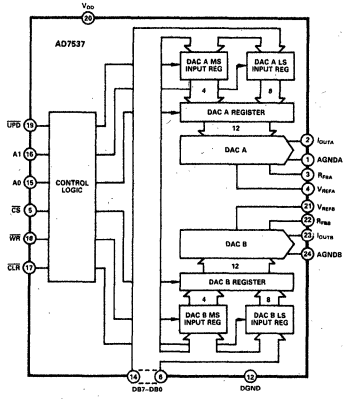
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time µs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7845JN(AQ)(SQ)	12	±2	±1	5	5	V	TTL &	C/I/E	S-3-313
AD7845KN(BQ)(TQ)	12	±1	±1	5	5	V	CMOS	C/I/E	S-3-313
AD7845LN(CQ)(UQ)	12	±1/2	±1	5	5	V		C/I/E	S-3-313
AD7545JN(AQ)(SD)	12	±2	±4	5	–	I	TTL &	C/I/E	I-9-231
AD7545KN(BQ)(TD)	12	±1	±1	5	–	I	CMOS	C/I/E	I-9-231
AD7545LN(CQ)(UD)	12	±1/2	±1	5	–	I		C/I/E	I-9-231
AD7548JN(AQ)(SD)	12	±1	±1	5	1	I	TTL &	C/I/E	I-9-247
AD7548KN(BQ)(TD)	12	±1/2	±1/2	5	1	I	CMOS	C/I/E	I-9-247

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" - cerdip.
[2]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

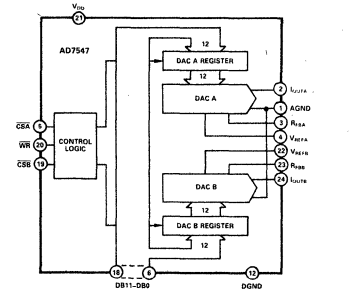
Digital-to-Analog Converters

12-Bit µP-Compatible



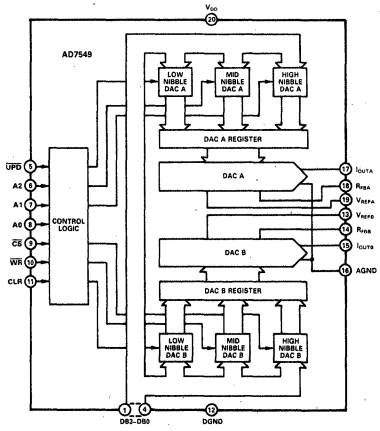
AD7537

Two 12-Bit DACs in One Package
Versatile 8-Bit Bus Interface
4-Quadrant Multiplication
Low Gain Error (1LSB max)
DAC Ladder Resistance Matching: 0.5%
Space Saving 0.3", 24-Pin Package



AD7547

Two 12-Bit DACs in One Package
12-Bit Parallel Load
Versatile 8-Bit Bus Interface
4-Quadrant Multiplication
Low Gain Error (1LSB max)
DAC Ladder Resistance Matching: 0.5%
Space Saving 0.3", 24-Pin Package



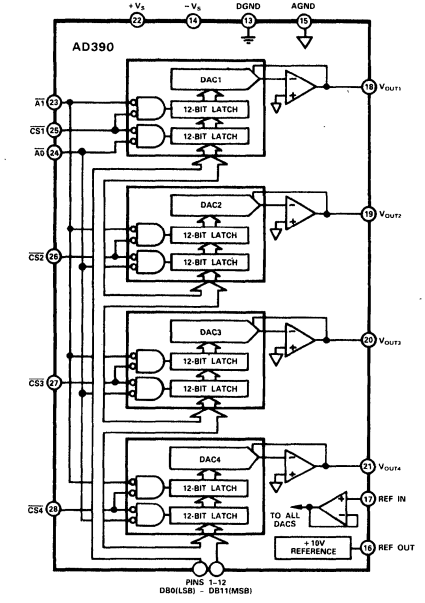
AD7549

Two 12-Bit DACs in One Package
Space Saving – 4-Bit Bus Interface
4-Quadrant Multiplication
Simultaneous Updating of Both DACs
DAC Ladder Resistance Matched to 1% Typical
Low Power: CMOS

SPECIFICATIONS – Min or Max at T_A = +25°C

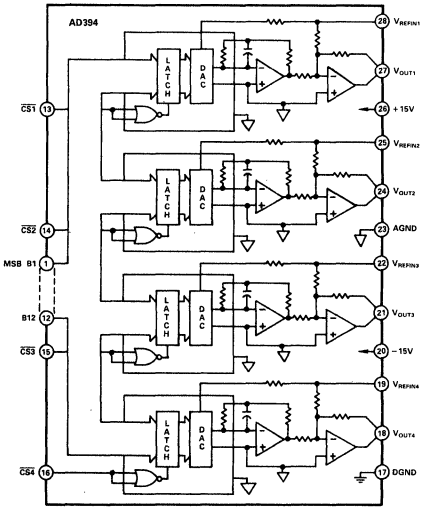
Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time µs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7537JN(AQ)(SQ)	12	±1	±1	5	1.5	I	TTL &	C/I/E	S-3-233
AD7537KN(BQ)(TQ)	12	±1/2	±1	5	1.5	I	CMOS	C/I/E	S-3-233
AD7547JN(AQ)(SQ)	12	±1	±1	5	1.5	I	TTL &	C/I/E	S-3-233
AD7547KN(BQ)(TQ)	12	±1/2	±1	5	1.5	I	CMOS	C/I/E	S-3-233
AD7549JN(AD)(SD)	12	±1	±1	5	1.5	I	TTL &	C/I/E	S-3-235
AD7549KN(BD)(TD)	12	±1/2	±1/2	5	1.5	I	CMOS	C/I/E	S-3-235

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD390

Four Complete 12-Bit DACs in One IC Package
Linearity Error ±1/2LSB T_{min} – T_{max} (AD390K, T)
Factory-Trimmed Gain and Offset
Buffered Voltage Output
Monotonicity Guaranteed Over Full Temperature Range
Double-Buffered Data Latches
Includes Reference and Buffer
Fast Settling: 8μs max to ±1/2LSB



AD394

Four Low Power 12-Bit CMOS DACs with Buffer Registers
Linearity Error ±1/2LSB T_{min}–T_{max} (AD394, AD395K, T)
Factory-Trimmed Gain and Offset
Precision Output Amplifiers for V_{OUT}
Full Four Quadrant Multiplication per DAC
Monotonicity Guaranteed Over Full Temperature Range
Fast Settling: 15μs max to ±1/2LSB

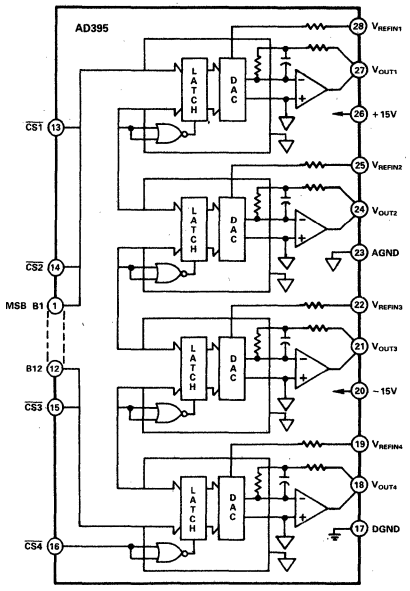
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time μs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD390JD(SD)	12	±3/4	±3/4	40[3]	8	V	TTL &	C/E	I-9-27
AD390KD(TD)	12	±1/2	±1/2	20[3]	8	V	CMOS	C/E	I-9-27
AD394JM(SM)	12	±3/4	±3/4	10	15	V	TTL &	C/E	S-3-49
AD394KM(TM)	12	±1/2	±1/2	5	15	V	CMOS	C/E	S-3-49

NOTES
[1]Suffix "D" – ceramic DIP; Suffix "M" – metal package.
[2]C = 0 to +70°C, E = –55°C to +125°C.
[3]With internal reference.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Digital-to-Analog Converters

12-Bit μP-Compatible



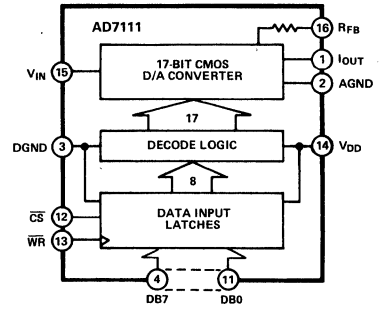
AD395

Four Complete 12-Bit CMOS DACs with Buffer Registers
Linearity Error ±1/2LSB T_{min}–T_{max} (AD394, AD395K, T)
Factory-Trimmed Gain and Offset
Precision Output Amplifiers for V_{OUT}
Two Quadrant Multiplication per DAC
Monotonicity Guaranteed Over Full Temperature Range
Fast Settling: 15μs max to ±1/2LSB

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time μs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD395JM(SM)	12	±3/4	±3/4	10	15	V	TTL &	C/E	S-3-49
AD395KM(TM)	12	±1/2	±1/2	5	15	V	CMOS	C/E	S-3-49

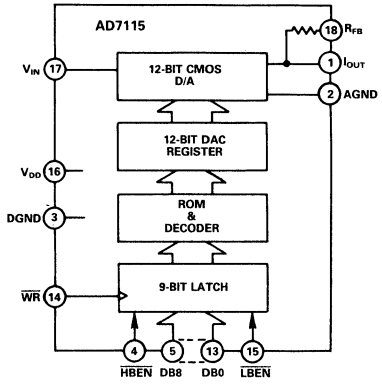
NOTES
[1]Suffix "M"–metal package.
[2]C = 0 to +70°C, E = −55°C to +125°C.
*I = Volume 1–Integrated Circuits; II = Volume 2–Modules & Subsystems; S = This Volume.



AD7111

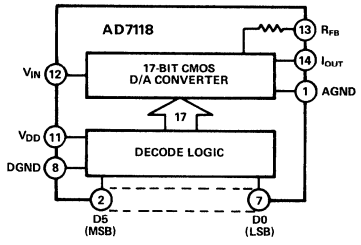
Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)
Low Power: CMOS

APPLICATIONS
Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators



AD7115

Dynamic Range: 0 to 19.9dB Plus Full Muting
Resolution: 0.1dB
2 1/2 Digit BCD Input Coding
On-Chip Data Latches
Full ±25V Input Range
Low Distortion and Noise
Latch-Up Free (No Protection Schottky Required)
TTL Compatible
Low Power: CMOS



AD7118

Dynamic Range 85.5dB
Resolution 1.5dB
Full ±25V Input Range Multiplying DAC
Extended Temperature Range −55°C to +125°C
Low Distortion
Low Power: CMOS
Latch-Proof Operation (Schottky Diodes Not Required)

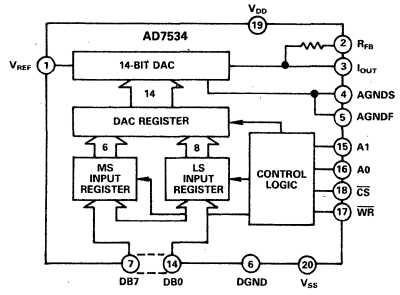
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution dB	Relative Accuracy dB	Differential Nonlinearity	Gain T.C. ppm/°C	Settling Time µs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7111KN(BQ)(TD)	0.375	±0.17	Monotonic	N/A	4.5	I	TTL &	C/I/E	I-9-109
AD7111LN(CQ)(UD)	0.375	±0.17	Monotonic	N/A	4.5	I	CMOS	C/I/E	I-9-109
AD7115KN(BQ)(TD)	0.1	±0.05	Monotonic	N/A	7	I	TTL & CMOS	C/I/E	I-9-115
AD7118KN(BD)(TD)	1.5	±1.0	Monotonic	N/A	1.8	I	TTL &	C/I/E	I-9-123
AD7118LN(CD)(UD)	1.5	±0.75	Monotonic	N/A	1.8	I	CMOS	C/I/E	I-9-123

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" - cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

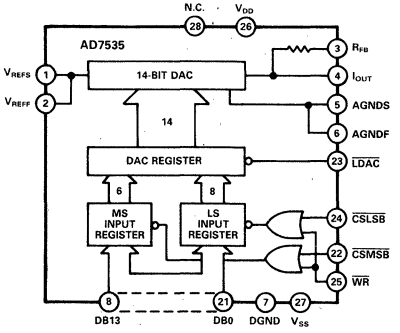
Digital-to-Analog Converters

High Resolution



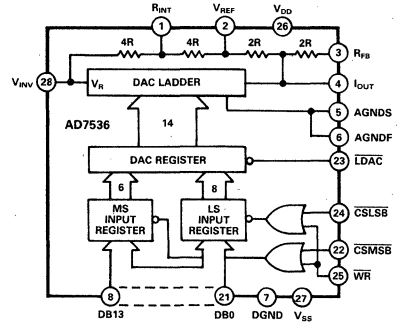
AD7534

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Full 4-Quadrant Multiplication
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Small 20-Pin Package
- Low Output Leakage (<20nA) over the Full Temperature Range
- Low Power: CMOS



AD7535

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Full 4 Quadrant Multiplication
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Low Output Leakage (<20nA) over the Full Temperature Range
- Low Power: CMOS



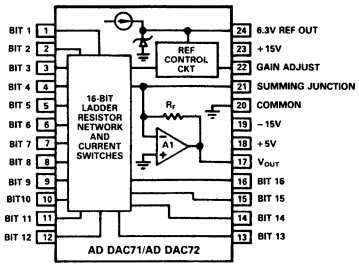
AD7536

- Full 4-Quadrant Multiplication without External Resistors
- All Grades 14-Bit Monotonic over the Full Temperature Range
- Low Output Leakage (<20nA) over the Full Temperature Range
- Low Gain Temperature Coefficient, 2ppm/°C

SPECIFICATIONS – Min or Max at T_A = +25°C

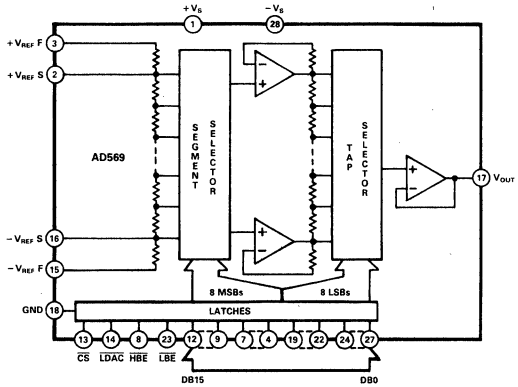
Model[1]	Resolution Bits	Relative Accuracy	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time µs	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD7534JN(AD)(SD)	14	±2LSB	±1	5	1.5	I	TTL &	C/I/E	S-3-197
AD7534KN(BD)(TD)	14	±1LSB	±1	2.5	1.5	I	CMOS	C/I/E	S-3-197
AD7535JN(AD)(SD)	14	±2LSB	±1	5	1.5	I	TTL &	C/I/E	S-3-209
AD7535KN(BD)(TD)	14	±1LSB	±1	2.5	1.5	I	CMOS	C/I/E	S-3-209
AD7536JN(AD)(SD)	14	±2LSB	±1	5	1.5	I	TTL &	C/I/E	S-3-221
AD7536KN(BD)(TD)	14	±1LSB	±1	5	1.5	I	CMOS	C/I/E	S-3-221

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD DAC71/AD DAC72

16-Bit Resolution
±0.003% Maximum Nonlinearity
Low Gain Drift ±7ppm/°C
0 to +70°C Operation (AD DAC71, AD DAC71H, AD DAC72C)
–25°C to +85°C Operation (AD DAC72)
Current and Voltage Models Available
Improved Second-Source



AD569

Guaranteed 16-Bit Monotonicity
Voltage Output, 6µs Settling Time
Monolithic BIMOS II Construction
±0.01% Nonlinearity
8- and 16-Bit Bus Compatible
3µs Settling Time to 16 Bits
Low Drift
Low Power: 200mW

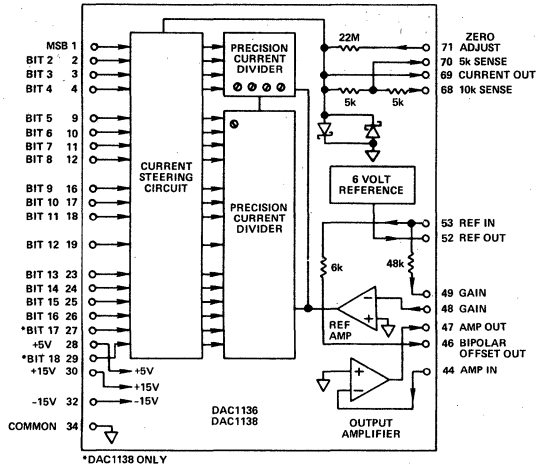
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time[2] µs	I/V Out	Input Logic	Temp. Range[3]	Volume* Section Page
AD DAC71–COB–I	16	±1 1/2	±2	15	5	I	TTL	C	I-9-271
AD DAC71–CSB–I	16	±1 1/2	±2	15	5	I	TTL	C	I-9-271
AD DAC71H–COB–I	16	±1 1/2	±2	15	5	I	TTL	C	I-9-271
AD DAC71H–CSB–I	16	±1 1/2	±2	15	5	I	TTL	C	I-9-271
AD DAC72C–COB–I	16	±1 1/2	±2	15	5	I	TTL	C	I-9-271
AD DAC72C–CSB–I	16	±1 1/2	±2	15	5	I	TTL	C	I-9-271
AD DAC72–COB–I	16	±1 1/2	±2	15	5	I	TTL	I	I-9-271
AD DAC72–CSB–I	16	±1 1/2	±2	15	5	I	TTL	I	I-9-271
AD DAC71–COB–V	16	±1 1/2	±2	15	5	V	TTL	C	I-9-271
AD DAC71–CSB–V	16	±1 1/2	±2	15	5	V	TTL	C	I-9-271
AD DAC71H–COB–V	16	±1 1/2	±2	15	5	V	TTL	C	I-9-271
AD DAC71H–CSB–V	16	±1 1/2	±2	15	5	V	TTL	C	I-9-271
AD DAC72C–COB–V	16	±1 1/2	±2	15	5	V	TTL	C	I-9-271
AD DAC72C–CSB–V	16	±1 1/2	±2	15	5	V	TTL	C	I-9-271
AD DAC72–COB–V	16	±1 1/2	±2	15	5	V	TTL	I	I-9-271
AD DAC72–CSB–V	16	±1 1/2	±2	15	5	V	TTL	I	I-9-271
AD569JN(AD)(SQ)	16	±26[4]	±1	–	3[5]	V	TTL	C/I/E	I-9-81
AD569KN(BD)	16	±13[4]	±1/2	–	3[5]	V	TTL	C/I/E	I-9-81

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]Settling time to 0.003%.
[3]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
[4]Relative accuracy specified as ±0.04% (J, A, S) and ±0.024% (K, B).
[5]Settling time to 0.001%.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Digital-to-Analog Converters

High Resolution

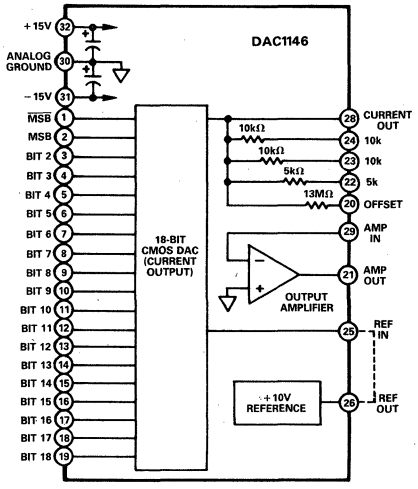


DAC1136

16-Bit Resolution and Accuracy
Nonlinearity 1/2SLB
Settling to 1/2LSB (0.0008%) in 8μs

DAC1138

18-Bit Resolution and Accuracy (38μV, 1 Part in 262,144)
Integral Nonlinearity 1/2LSB max
Differential Nonlinearity 1/2LSB max
Excellent Stability
Settling to 1/2LSB (0.0002%) in 10μs
Hermetically-Sealed Semiconductors



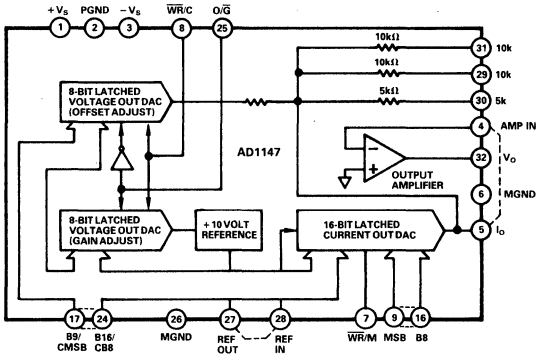
DAC1146

Low Cost, High Accuracy 18-Bit D/A Converter
Integral Nonlinearity: ±0.00076% FSR max
Differential Nonlinearity: ±0.00076% FSR max
Low Differential Nonlinearity T.C.: ±1ppm/°C max
Wide Power Supply Operation: ±11.5V to ±16V
Fast Settling: 6μs to ±0.00076% FSR
Small Size 2" × 2" × 0.4"

SPECIFICATIONS – Min or Max at T_A = +25°C

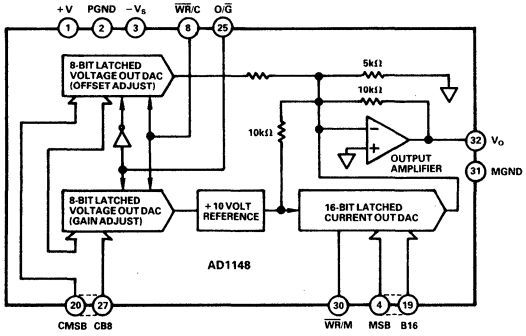
Model	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time μs	Input Logic	I/V Out	Temp. Range[1]	Volume* Section Page
DAC1136J	16	1	1	5 typ	8 typ	TTL & CMOS	I/V	C	II-10-27
DAC1136K	16	1/2	1/2	5 typ	8 typ	TTL & CMOS	I/V	C	II-10-27
DAC1136L	16	1/2	1/2	8	8 typ	TTL & CMOS	I/V	C	II-10-27
DAC1146	18	2	2	12	6 typ	TTL & CMOS	I/V	C	II-10-35
DAC1138J	18	1	1	0.8 typ	10 typ	TTL & CMOS	I/V	C	II-10-27
DAC1138K	18	1/2	1/2	0.8 typ	10 typ	TTL & CMOS	I/V	C	II-10-27

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD1147

16-Bit Hybrid: Microprocessor Compatible
Latched 8-Bit Input DACs:
Gain & Offset Correction via μP
Multiplexed with Main 16-Bit Input DAC
Nonlinearity: ±0.00076% max
Differential TC: ±1 ppm/°C max
Fast Settling: 18μs to ±0.00076%
Low Power: 375mW (Including Reference)
Current or Voltage Output
Full Four Quadrant Multiplying
Functionally Complete:
Internal +10V Reference; Output Amplifier; Input Latches



AD1148

16-Bit Hybrid: Microprocessor Compatible
Latched 8-Bit Input DACs:
Gain & Offset Correction via μP;
Separate from Main 16-Bit Input DAC
Differential Nonlinearity: ±0.00076% max
Differential TC: ±1 ppm/°C max
Fast Settling: 18μs to ±0.00076%
Low Power: 375mW (Including Reference)
Functionally Complete:
Internal +10V Reference; Output Amplifier; Input Latches

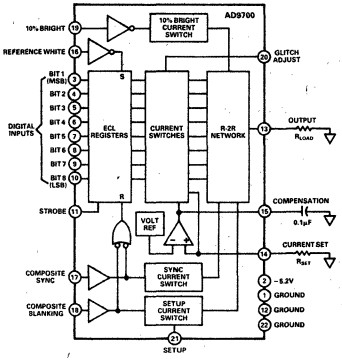
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Settling Time μs	Input Logic	I/V Out	Temp. Range[1]	Volume* Section Page
AD1147	16	1/2	1/2	10	18 typ	CMOS	I/V	I	S-3-167
AD1148	16	1	1/2	10	18 typ	CMOS	V	I	S-3-167

NOTES
[1]I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

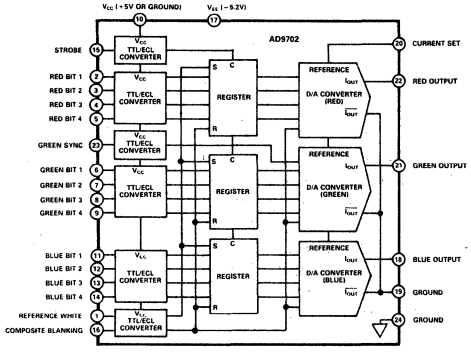
Digital-to-Analog Converters

Video Display



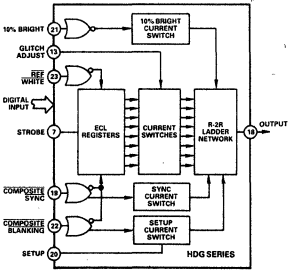
AD9700

Update Rates to 125MHz
Low Glitch Energy
Complete Composite Signals
On-Chip Reference Supply
Single −5.2V Power Supply



AD9702

ECL or TTL Compatible
Composite Inputs
125MHz Update Rates Minimum



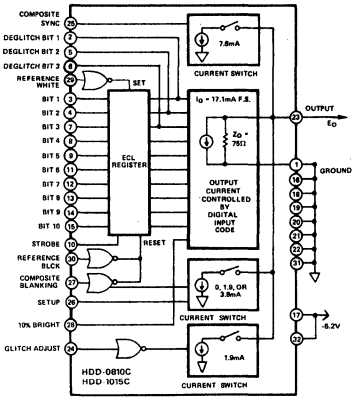
HDG SERIES

Update Rates to 150MHz
Low Glitch Energy
Complete Composite Inputs
Single −5.2V Power Supply
Military Temperature Range Available

SPECIFICATIONS – Min or Max at T_A = +25°C

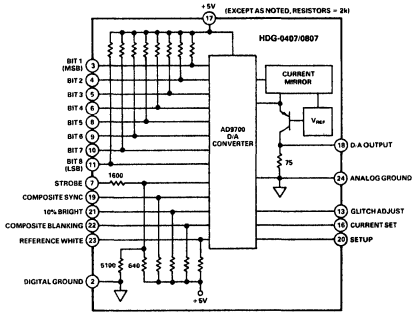
Model[1]	Resolution Bits	Relative Accuracy ±%GS	Differential Nonlinearity ±%GS	Gain T.C. ppm/°C	Settling Time ns	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
AD9700BD(BW)	8	0.2	0.2	50	10	I	ECL	I	S-3-315
AD9700SD	8	0.2	0.2	50	10	I	ECL	E	S-3-315
AD9702BD(BW)[3]	4(×3)	0.8	0.8	200	5	I	ECL & TTL	I	S-3-319
HDG-0405	4	3.2	3.2	50	4	I	ECL	I	I-9-310
HDG-0605	6	0.8	0.8	50	6	I	ECL	I	I-9-310
HDG-0805	8	0.2	0.2	50	8	I	ECL	I	I-9-310
HDG-0405BD(BW)	4	3.2	3.2	50	5	I	ECL	I	I-9-310
HDG-0605BD(BW)	6	0.8	0.8	50	7	I	ECL	I	I-9-310
HDG-0805BD(BW)	8	0.2	0.2	50	9	I	ECL	I	I-9-310
HDG-0405SD	4	3.2	3.2	50	5	I	ECL	E	I-9-310
HDG-0605SD	6	0.8	0.8	50	7	I	ECL	E	I-9-310
HDG-0805SD	8	0.2	0.2	50	9	I	ECL	E	I-9-310

NOTES
[1]No suffix – metal DIP; Suffix "D" – hermetic ceramic DIP; Suffix "W" – non-hermetic ceramic DIP.
[2]I = −25°C to +85°C; E = −55°C to +125°C.
[3]Contains (3) 4-bit D/As.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



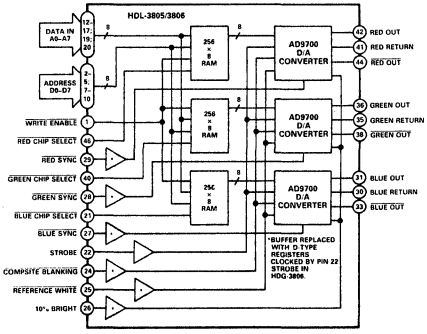
HDD SERIES

HDD-0810 – 8 Bits of Resolution
HDD-1015 – 10 Bits of Resolution
10ns Settling Time to 0.2% (HDD-0810)
15ns Settling Time to 0.1% (HDD-1015)
Internal Monolithic Reference
Low 200pV-s Glitch Impulse
Compatible with EIA Standards RS-170 and RS-343, Including 10% Brightness
Complete Composite Inputs ("C" Models)



HDG-0407/0807

Update Rates to 50MHz
Low Glitch
Complete Composite Inputs
Single +5V Power Supply
TTL-Compatible Inputs
Directly Drives 75Ω to Ground



HDL-3805/3806

Triple 8-Bit D/A with LUTs
115MHz Update Rates
RGB Composite Functions
Small Size (2.3" x 1.5")
Latched Composite Functions (HDL-3806)

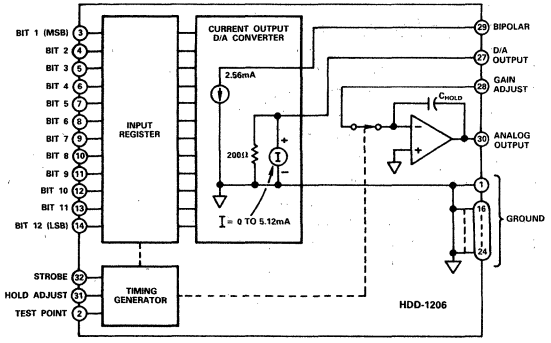
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy ±%( )[2]	Differential Nonlinearity ±%GS	Gain T.C. ppm/°C	Settling Time ns	I/V Out	Input Logic	Temp. Range[3]	Volume* Section Page
HDD-0810	8	0.1	–	80	10	V	ECL	C	I-9-295
HDD-0810C	8	0.1	–	80	10	V	ECL	C	I-9-295
HDD-0810M(CM)	8	0.1	–	80	10	V	ECL	I	I-9-295
HDG-0407BD(BW)	4	3.2	3.2	350	8	V	TTL	I	S-3-387
HDG-0807BD(BW)	8	0.2	0.2	350	14	V	TTL	I	S-3-387
HDL-3805BM	8	0.2	0.2	125	10	I	ECL	I	S-3-391
HDL-3806BM(CM)	8	0.2	0.2	125	10	I	ECL	I	S-3-391

NOTES
[1]HDDs and HDLs – metal DIP; Suffix "D" – hermetic ceramic DIP; Suffix "W" – non-hermetic ceramic DIP.
[2]Relative to full scale (FS) for binary versions; Gray scale (GS) for composite (C) versions.
[3]C = 0 to +70°C; I = –25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

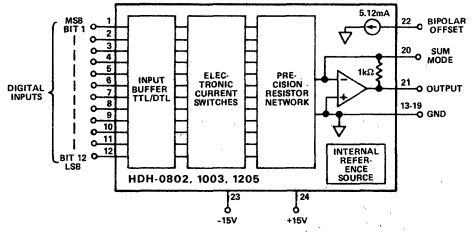
Digital-to-Analog Converters

Video Display



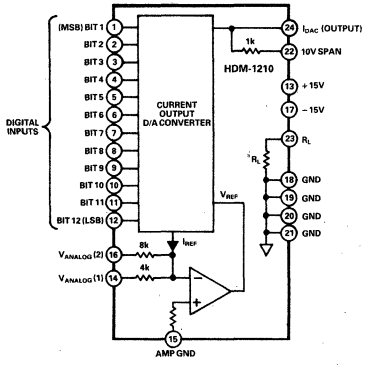
HDD-1206

12-Bit Resolution
6MHz Update Rates
Deglitched Voltage Output
Registers, D/A, and Amplifier in Single Hybrid
Available with 883 Screening



HDH SERIES

8-, 10-, and 12-Bit Resolution
300ns Voltage Settling to 0.1%
Guaranteed Monotonicity
Reliable Hybrid Construction



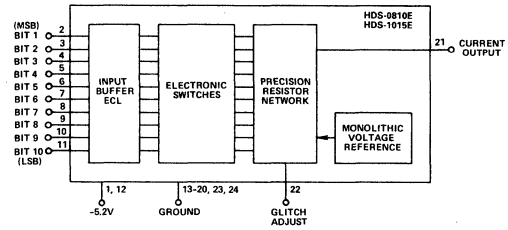
HDM-1210

12-Bit Multiplying Accuracy
Good Drive: 10mA
Highest Speed Available
Small Size: 24-Pin DIP

SPECIFICATIONS – Min or Max at T_A = +25°C

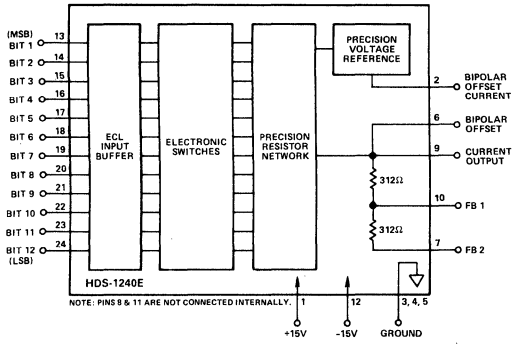
Model[1]	Resolution Bits	Relative Accuracy ±%FS	Differential Nonlinearity ±%GS	Gain T.C. ppm/°C	Settling Time ns	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
HDD-1206JW	12	0.0125	0.0125	40	60[3]	V	TTL	C	I-9-301
HDD-1206SM	12	0.0125	0.0125	40	60[3]	V	TTL	E	I-9-301
HDH-0802	8	0.1	0.1	30	150[4]	V	TTL	C	I-9-317
HDH-0802M	8	0.1	0.1	30	150[4]	V	TTL	E	I-9-317
HDH-1003	10	0.05	0.05	30	200[4]	V	TTL	C	I-9-317
HDH-1003M	10	0.05	0.05	30	200[4]	V	TTL	E	I-9-317
HDH-1205	12	0.0125	0.0125	30	350[4]	V	TTL	C	I-9-317
HDH-1205M	12	0.0125	0.0125	30	350[4]	V	TTL	E	I-9-317
HDM-1210	12	0.0125	DNA	20	60[5]	I	TTL	I	I-9-315

NOTES
[1]No suffix and suffix "W" – non-hermetic ceramic DIP; Suffix "M" – metal DIP.
[2]C = 0 to +70°C; I = −25°C to +85°C; E = −55°C to +125°C.
[3]One LSB change.
[4]5-volt output step settling to 0.4%, 0.1%, and 0.025% for 8-, 10-, and 12-bit units.
[5]Digital settling time to ±1%; major carry transition.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



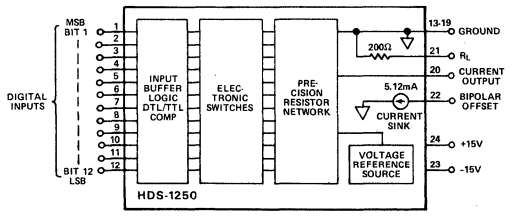
HDS-0810E/HDS-1015E

HDS-0810E: 8 Bits
HDS-1015E: 10 Bits
ECL Inputs
Settling Time to 10ns
Low Glitch Impulse
100MHz Update Rates
Low Power



HDS-1240E

12 Bits of Resolution
Settling Time of 40ns
Low Glitch Impulse
ECL Compatible



HDS-0820/HDS-1025/ HDS-1250

HDS-0820: 8 Bits
HDS-1025: 10 Bits
HDS-1250: 12 Bits
25ns Settling to 0.1%
10mA Current Out
Monotonic Over Temperature
Reliable Hybrid Packaging

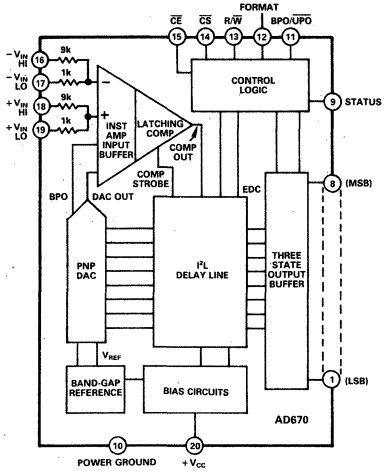
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy ±%FS	Differential Nonlinearity ±%FS	Gain T.C. ppm/°C	Settling Time ns	I/V Out	Input Logic	Temp. Range[2]	Volume* Section Page
HDS-0810E	8	0.1	0.2	80	10[3]	I	ECL	C	I-9-321
HDS-0810EM	8	0.1	0.2	80	10[3]	I	ECL	E	I-9-321
HDS-1015E	10	0.05	0.1	80	15[3]	I	ECL	C	I-9-321
HDS-1015EM	10	0.05	0.1	80	15[3]	I	ECL	E	I-9-321
HDS-1240E	12	0.0125	0.0125	25	40[3]	I	ECL	C	I-9-323
HDS-1240EM	12	0.0125	0.0125	25	40[3]	I	ECL	E[5]	I-9-323
HDS-0820	8	0.1	0.2	30	20[4]	I	TTL	C	I-9-317
HDS-0820M	8	0.1	0.2	30	20[4]	I	TTL	E	I-9-317
HDS-1025	10	0.05	0.1	30	25[4]	I	TTL	C	I-9-317
HDS-1025M	10	0.05	0.1	30	25[4]	I	TTL	E	I-9-317
HDS-1250	12	0.0125	0.05	30	35[4]	I	TTL	C	I-9-317
HDS-1250M	12	0.0125	0.05	30	35[4]	I	TTL	E	I-9-317

NOTES
[1]No suffix and suffix "E" – hermetic ceramic DIP; Suffix "EM" or "M" – metal DIP.
[2]C = 0 to +70°C; E = −55°C to +125°C.
[3]Settling time to 0.2%, 0.1%, and 0.0125%FS for 8-, 10-, and 12-bit units.
[4]Settling time to 0.4%, 0.1% and 0.025%FS for 8-, 10-, and 12-bit units.
[5] −55°C to +100°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

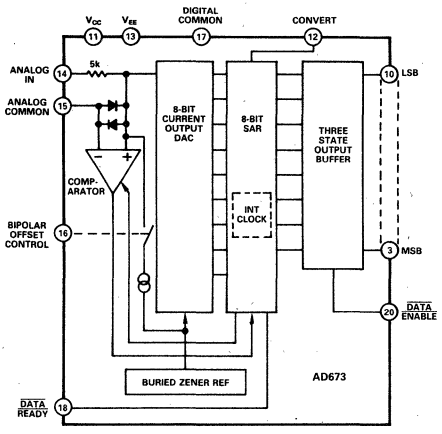
Analog-to-Digital Converters

8-Bit



AD670

Complete 8-Bit A/D Converter
Flexible Input Stage: Instrumentation Amp Front End Provides Differential Inputs and Good Common-Mode Rejection
Fast Conversion Time: 10μs max
Full Microprocessor Bus Interface
No User Trims Required
No Missing Codes Over Temperature
Single +5V Supply Required
Convenient Input Ranges, 256mV and 2.56V
Small 20-Pin Package



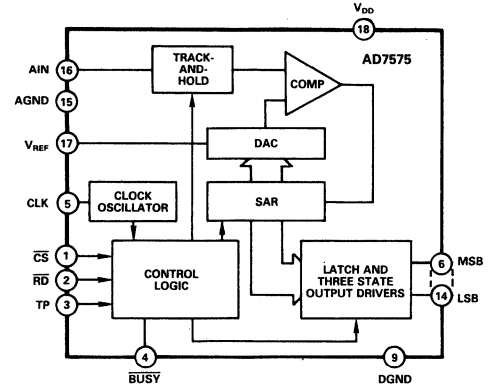
AD673

Complete 8-Bit A/D Converter with Reference, Clock and Comparator
Full Microprocessor Bus Interface
Fast Conversion Time – 30μs max
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Unipolar or Bipolar Input Range

SPECIFICATIONS – Min or Max at T_A = +25°C

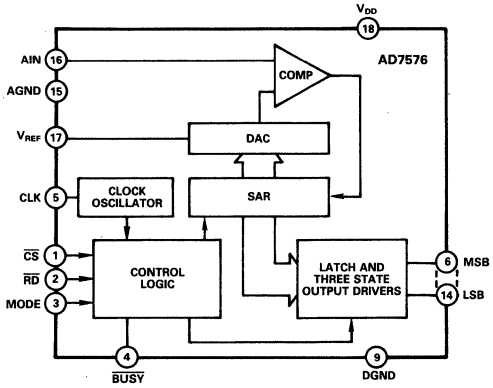
Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Full Scale Error T_{MIN}-T_{MAX} LSB	Conversion Time μs	Logic	Temp. Range[3]	Volume* Section Page
AD670(JN)(AD)(SD)	8	±1/4	NMCOT	2.5	10	TTL	C/I/E	I-10-85
AD670KN(BD)	8	±1/4	NMCOT	1.0	10	TTL	C/I	I-10-85
AD673JN(JD)(SD)	8	±1/2	NMCOT	2 typ	30	TTL	C/E	I-10-95

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −40°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD7575

Fast Conversion Time: 5μs
On-Chip Track/Hold
Low Total Unadjusted Error: 1LSB
Full Power Signal Bandwidth: 50kHz
Single +5V Supply
100ns Data Access Time
Low Power (15mW typ)
Low Cost
Small Package



AD7576

Single +5V Operation with External Positive Reference
Fast Conversion Time: 5μs
No Missed Codes Over Full Temperature Range
Microprocessor Compatible
Low Cost
Low Power: CMOS

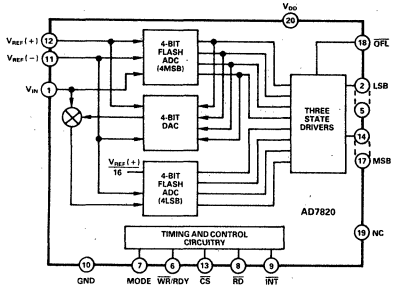
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Full Scale Error T_{MIN}-T_{MAX} LSB	Conversion Time μs	Logic	Temp. Range[3]	Volume* Section Page
AD7575JN(AQ)(SD)	8	±1	NMCOT	±1	5	CMOS	C/I/E	S-3-247
AD7575KN(BQ)(TD)	8	±1/2	NMCOT	±1	5	CMOS	C/I/E	S-3-247
AD7576JN(AQ)(SD)	8	±1	NMCOT	±1	5	CMOS	C/I/E	S-3-257
AD7576KN(BQ)(TD)	8	±1/2	NMCOT	±1	5	CMOS	C/I/E	S-3-257

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

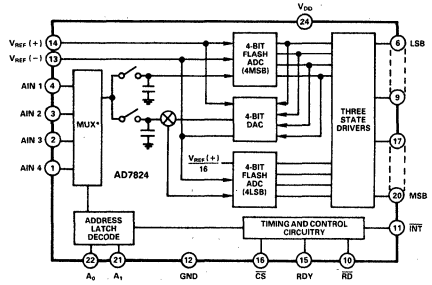
Analog-to-Digital Converters

8-Bit



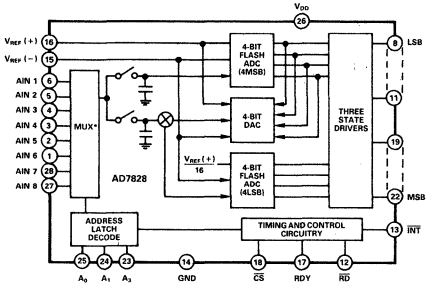
AD7820

Fast Conversion Time: 1.5μs Max
Built-In Track-and-Hold Function
No Missed Codes
No User Trims Required
Single +5V Supply
Low Power: CMOS



AD7824

4 Analog Input Channels
Built-In Track/Hold Function
10kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single +5V Supply
Low Power: 40mW
Fast Conversion Rate, 2.5μs/Channel
Tight Error Specification: 1/2LSB



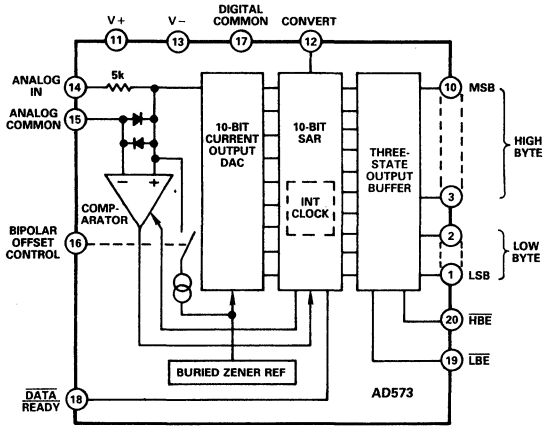
AD7828

8 Analog Input Channels
Built-In Track/Hold Function
10kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single +5V Supply
Low Power: 40mW
Fast Conversion Rate, 2.5μs/Channel
Tight Error Specification: 1/2LSB

SPECIFICATIONS – Min or Max at T_A = +25°C

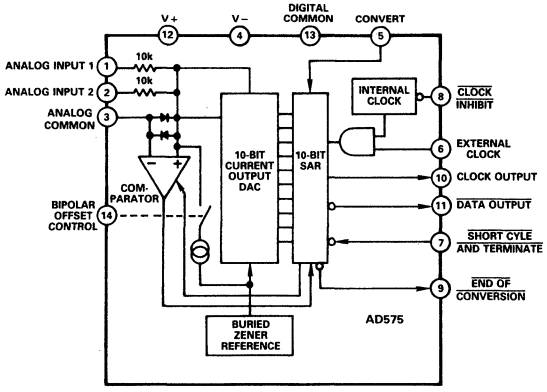
Model[1]	Resolution Bits	Total Unadjusted Error LSB	Differential Nonlinearity[2]	Channel-to-Channel Mismatch LSB	Conversion Time[3] μs	Logic	Temp. Range[4]	Volume* Section Page
AD7820KN(BQ)(TQ)	8	±1	NMCOT	N/A	1.6	TTL	C/I/E	S-3-289
AD7820LN(CQ)(UQ)	8	±1/2	NMCOT	N/A	1.6	TTL	C/I/E	S-3-289
AD7824KN(BQ)(TQ)	8	±1	NMCOT	±1/4	2.5	TTL	C/I/E	S-3-301
AD7824LN(CQ)(UQ)	8	±1/2	NMCOT	±1/4	2.5	TTL	C/I/E	S-3-301
AD7828KN(BQ)(TQ)	8	±1	NMCOT	±1/4	2.5	TTL	C/I/E	S-3-301
AD7828KN(CQ)(UQ)	8	±1/2	NMCOT	±1/4	2.5	TTL	C/I/E	S-3-301

NOTES
[1]Suffix "N" – plastic DIP; Suffix "Q" – cerdip.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]Conversion time expressed in μs/channel for AD7824 and AD7828.
[4]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD573

Complete 10-Bit A/D Converter with Reference, Clock and Comparator
Full 8- or 16-Bit Microprocessor Bus Interface
Fast Conversion Time – 30μs max
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Unipolar or Bipolar Input Range



AD575

Complete 10-Bit A/D Converter with Reference Clock and Comparator
Serial Output
Fast Successive Approximation Conversion: 30μs max
No Missing Codes Over Temperature
Operation on +5V and −12V to −15V Supplies
Unipolar or Bipolar Input Range

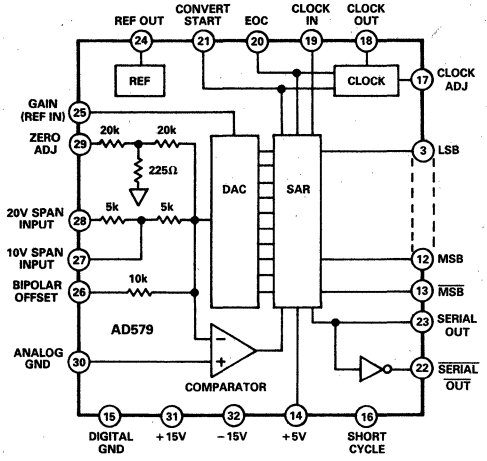
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Full Scale Error T_{MIN}-T_{MAX} LSB	Conversion Time μs	Logic	Temp. Range[3]	Volume* Section Page
AD573JN(JD)	10	±1	NMC	±4	30	TTL	C	I-10-47
AD573KN(KD)	10	±1/2	NMCOT	±2	30	TTL	C	I-10-47
AD573SD	10	±1	NMCOT	±5	30	TTL	E	I-10-47
AD575JN(JD)(SD)	10	±1	NMC(NMC)(NMCOT)	±4(±4)(±5)	30	TTL	C/C/E	S-3-79
AD575KN(KD)	10	±1/2	NMCOT	±2	30	TTL	C	S-3-79

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

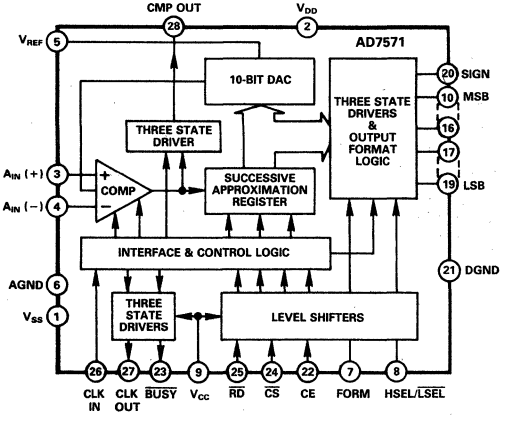
Analog-to-Digital Converters

10-Bit



AD579

Complete 10-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 1.8μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±40ppm/°C max
Max Nonlinearity: <±0.048%
Low Power: 775mW



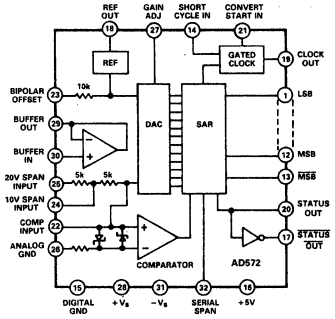
AD7571

10-Bit Plus Sign Resolution
No Missed Codes Over Full Temperature Range
Conversion Time 80μs
Differential Analog Voltage Inputs, ±10V Range
Serial and Parallel Data Outputs
Easy Interface to Most Microprocessors
Internal Clock Oscillator
Single Supply Operation for Positive-Only Signals
Low Power: CMOS

SPECIFICATIONS – Min or Max at T_A = +25°C

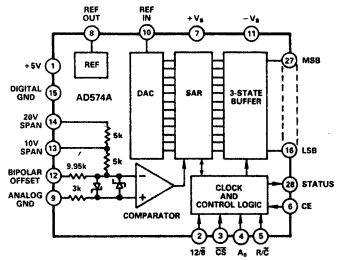
Model[1]	Resolution Bits	Relative Accuracy ‡ LSB	Differential Nonlinearity[2]	Gain T.C. ppm/°C	Conversion Time μs	Logic	Temp. Range[3]	Volume* Section Page
AD579JN	10	±1/2	NMCOT	40	2.2	TTL	C	I-10-79
AD579KN(TD)	10	±1/2	NMCOT	40	1.8	TTL	C/E	I-10-79
AD7571JN(AQ)(SD)	10 + SIGN	±1	NMCOT	5	80	TTL &	C/I/E	I-10-139
AD7571KN(BQ)(TD)	10 + SIGN	±1/2	NMCOT	5	80	CMOS	C/I/E	I-10-139

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



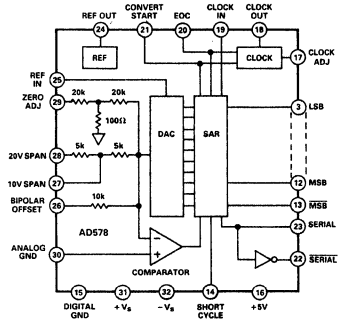
AD572

True 12-Bit Operation: Max Nonlinearity $< \pm 0.012\%$
Low Gain T.C.: $< \pm 15$ppm/°C (AD572B)
Low Power: 900mW
Fast Conversion Time: <25µs
Monotonic Feedback DAC Guarantees No Missing Codes



AD574A

Complete 12-Bit A/D Converter with Reference and Clock
Full 8-or 16-Bit Microprocessor Bus Interface
Industry Standard Pinout
Guaranteed Linearity Over Temperature
No Missing Codes Over Temperature
Conversion Time: 35µs max
Buried Zener Reference for Long-Term Stability and Low Gain T.C.
10ppm/°C max AD574AL
12.5ppm/°C max AD574AU
Precision 10V Reference for External Applications
Ceramic DIP, Plastic DIP or LCC Package
Low Power: 390mW



AD578

Complete 12-Bit A/D Converter with Reference and Clock
Fast Conversion: 3µs (max)
Buried Zener Reference for Long Term Stability and Low Gain T.C.: ± 30ppm/°C max
Max Nonlinearity: $< \pm 0.012\%$
Low Power: 75mW
Hermetic Package Available
Short Cycle Capability
Precision +10V Reference for External Applications
Adjustable Internal Clock
"Z" Models for ±12V Supplies

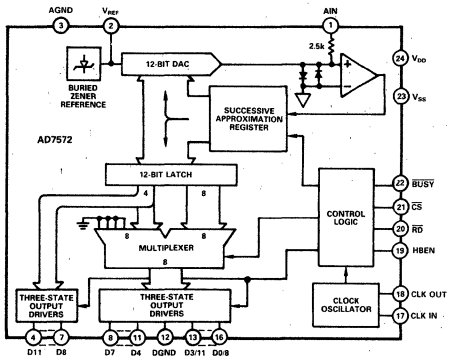
SPECIFICATIONS – Min or Max at $T_A = +25°C$

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Gain T.C. Gain T.C. ppm/°C	Conversion Time µs	Logic	Temp. Range[3]	Volume* Section Page
AD572AD(BD)(SD)	12	± 1/2	NMCOT	30(15)(25)	25	TTL	C/I/E	I-10-39
AD574AJD(SN)(SD)	12	± 1	NMC	50	35	TTL	C/C/E	I-10-55
AD574AKD(KN)(TD)	12	± 1/2	NMCOT	27(25)	35	TTL	C/C/E	I-10-55
AD574ALD(LN)(UD)	12	± 1/2	NMCOT	10(12.5)	35	TTL	C/C/E	I-10-55
AD578JD(JN)(SD)[4]	12	± 1/2	NMCOT	30(50)	6.0	TTL	C/E	S-3-87
AD578KD(KN)(TD)[4]	12	± 1/2	NMCOT	30	4.5	TTL	C/E	S-3-87
AD578LD(LN)[4]	12	± 1/2	NMCOT	30	3.0	TTL	C	S-3-87

NOTES
[1]Suffix "D" – ceramic DIP; Suffix "N" - polymer-sealed DIP.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[4]"Z" grade versions for ± 12V operation available.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

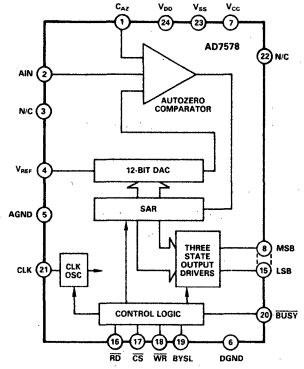
Analog-to-Digital Converters

12-Bit



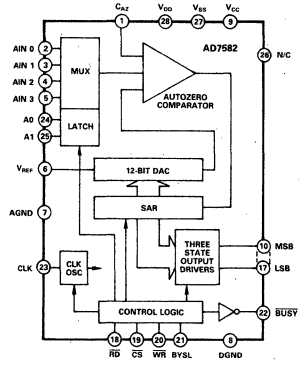
AD7572

12-Bit Resolution and Accuracy
Fast 5μs and 12μs Conversion Times
Complete with On-Chip Reference and Clock
No User Trims
High-Speed Digital Interface
Low Power (135mW typ.)
Small, 0.3" Wide, 24-Pin Package



AD7578

12-Bit Successive Approximation ADC
No Missed Codes Over Full Temperature Range
Low Total Unadjusted Error ±1LSB max
High Impedance Analog Input
Autozero Cycle for Low Offset Voltage
Low Power, 75mW typ
Small Size: 0.3", 24-Pin Package
Conversion Time of 100μs



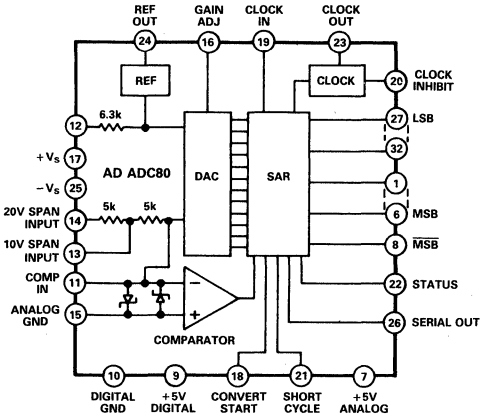
AD7582

12-Bit Successive Approximation ADC
Four High Impedance Input Channels
Analog Input Voltage Range of 0 to +5V with Positive Reference of +5V
Conversion Time of 100μs per Channel
No Missed Codes Over Full Temperature Range
Low Total Unadjusted Error ±1LSB max
Autozero Cycle for Low Offset Voltage
Low Power: CMOS

SPECIFICATIONS – Min or Max at T_A = +25°C

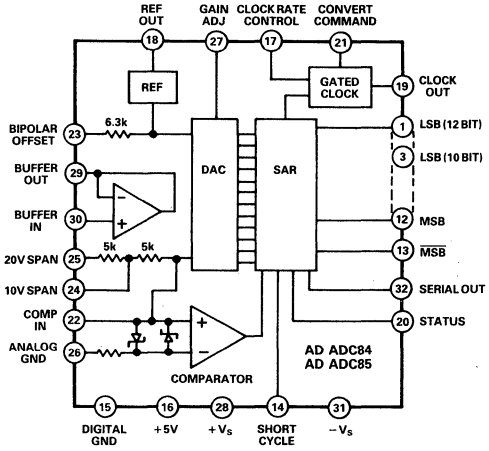
Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Full Scale Error @25° LSB	Full Scale Error TC ppm/°C	Conversion Time μs	Logic	Temp. Range[2]	Volume[a] Section Page
AD7572JN05(AQ05)(SQ05)	12	±1	±1	±15	45	5	TTL	C/I/E	S-3-243
AD7572KN05(BQ05)(TQ05)	12	±1	±1	±10	25	5	TTL	C/I/E	S-3-243
AD7572LN05(CQ05)(UQ05)	12	±1/2	±1	±10	25	5	TTL	C/I/E	S-3-243
AD7572JN12(AQ12)(SQ12)	12	±1	±1	±15	45	12	TTL	C/I/E	S-3-243
AD7572KN12(BQ12)(TQ12)	12	±1	±1	±10	25	12	TTL	C/I/E	S-3-243
AD7572LN12(CQ12)(UQ12)	12	±1/2	±1	±10	25	12	TTL	C/I/E	S-3-243
AD7578KN(BD)(TD)	12	±1	±3/4	±1/4	1 typ	100	TTL	C/I/E	S-3-265
AD7582KN(BD)(TD)	12	±1	±3/4	±1/4	5 typ	100	TTL	C/I/E	S-3-277

NOTES
[1]Suffix "N" – plastic DIP; Suffix "Q" – cerdip; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD ADC80

True 12-Bit Operation: Max Nonlinearity ±0.012%
Low Gain T.C.: ±30ppm/°C max
Low Power: 800mW
Fast Conversion Time: 25μs
Precision 6.3V Reference for External Application
Short-Cycle Capability
Serial or Parallel Data Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count – High Reliability
Industry Standard Pin Out
"Z" Models for ±12V Supplies



AD ADC84/AD ADC85

Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 10μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
Max Nonlinearity: <±0.012%
Low Power: 880mW Typical
Hermetic Package Available
Low Chip Count – High Reliability
Industry Standard Pin Out
"Z" Models for ±12V Operation Available

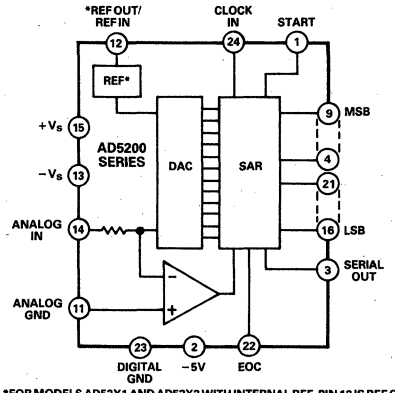
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Full Scale Error %FS	Full Scale Error TC ppm/°C	Conversion Time μs	Logic	Temp. Range[3]	Volume* Section Page
AD ADC80-10[4]	10	±1/2	NMCOT	0.1 typ	30	25	TTL	I	I-10-183
AD ADC80-12[4]	12	±1/2	NMCOT	0.1 typ	30	25	TTL	I	I-10-183
AD ADC84-10[4]	10	±1/2	NMCOT	0.25	30	6	TTL	C	I-10-191
AD ADC84-12[4]	12	±1/2	NMCOT	0.25	30	10	TTL	C	I-10-191
AD ADC85C-10[4]	10	±1/2	NMCOT	0.25	40	6	TTL	C	I-10-191
AD ADC85C-12[4]	12	±1/2	NMCOT	0.25	25	10	TTL	C	I-10-191
AD ADC85-10[4]	10	±1/2	NMCOT	0.25	20	6	TTL	I	I-10-191
AD ADC85-12[4]	12	±1/2	NMCOT	0.25	15	10	TTL	I	I-10-191
AD ADC85S-10[4]	10	±1/2	NMCOT	0.25	25	6	TTL	E	I-10-191
AD ADC85S-12[4]	12	±1/2	NMCOT	0.25	25	10	TTL	E	I-10-191

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[4]"Z" grade versions for ±12V operation available.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Analog-to-Digital Converters

12-Bit

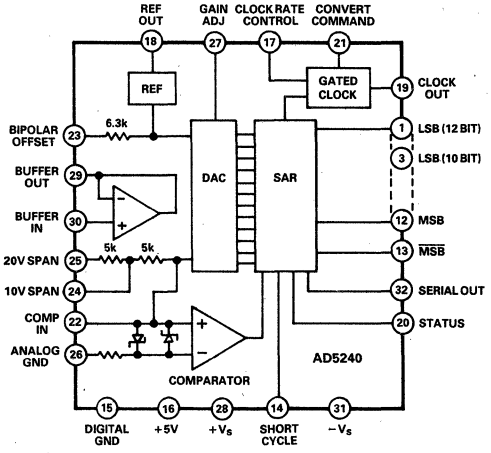


*FOR MODELS AD52X1 AND AD52X2 WITH INTERNAL REF, PIN 12 IS REF OUT.
FOR MODELS AD52X4 AND AD52X5 WITH INTERNAL REF, PIN 12 IS REF IN.

AD5200 SERIES

AD5200: 50μs Conversion Time
AD5210: 13μs Conversion Time

True 12-Bit Operation: ±1/2LSB max Nonlinearity
Totally Adjustment-Free
Guaranteed No Missing Codes Over the Specified Temperature Range
Hermetically-Sealed Package
Standard Temperature Range: +25°C to +85°C
Extended Temperature Range: −55°C to +125°C
Serial and Parallel Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count for High Reliability
Industry Standard Pin Out
Small 24-Pin DIP



AD5240

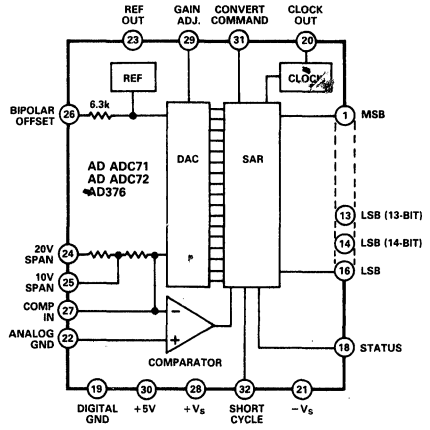
Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 5μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
Max Nonlinearity: <±0.012%
Low Power: 775mW Typical
Hermetic Package Available
Low Chip Count – High Reliability
Pin Compatible with AD ADC84/AD ADC85
"Z" Models for ±12V Supplies

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Absolute Accuracy LSB	Conversion Time μs	Logic	Temp. Range[3]	Volume* Section Page
AD5201BD(TD)	12	±1/2	NMCOT	2	50	TTL	I/E	I-10-105
AD5202BD(TD)	12	±1/2	NMCOT	2	50	TTL	I/E	I-10-105
AD5204BD(TD)	12	±1/2	NMCOT	2	50	TTL	I/E	I-10-105
AD5205BD(TD)	12	±1/2	NMCOT	2	50	TTL	I/E	I-10-105
AD5211BD(TD)	12	±1/2	NMCOT	2	13	TTL	I/E	I-10-105
AD5212BD(TD)	12	±1/2	NMCOT	2	13	TTL	I/E	I-10-105
AD5214BD(TD)	12	±1/2	NMCOT	2	13	TTL	I/E	I-10-105
AD5215BD(TD)	12	±1/2	NMCOT	2	13	TTL	I/E	I-10-105
AD5240KD	12	±1/2	NMCOT	N/A	5	TTL	C	I-10-111
AD5240BD	12	±1/2	NMCOT	N/A	5	TTL	I	I-10-111

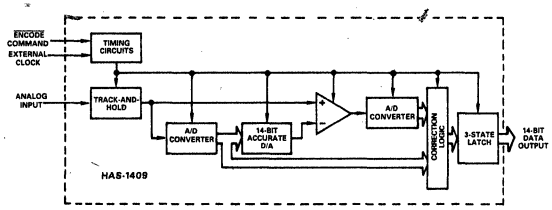
NOTES
[1]Suffix "D" – ceramic DIP.
[2]NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

High Resolution



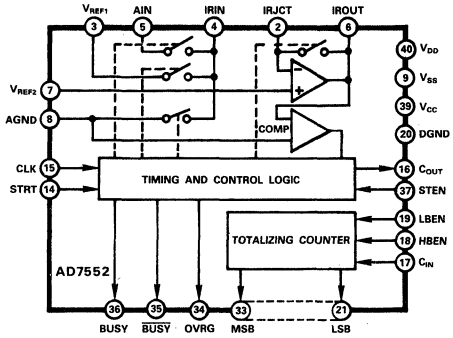
AD ADC71/AD ADC72 – AD376

AD376: 15µs Conversion Time
AD ADC71/AD ADC72: 45µs Conversion Time
Complete 16-Bit Converter with Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes over Temperature (AD376)
Short Cycle Capability
Industry Standard Pinout



HAS-1409

14-Bit Resolution
125kHz Word Rates
Internal Track-and-Hold
40-Pin DIP



AD7552

12-Bit Binary with Polarity and Overrange
Accuracy ±1LSB
Microprocessor Compatible
Ratiometric Operation
Low Power: CMOS

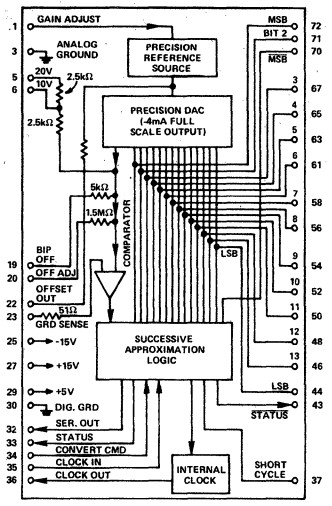
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy %	Differential Nonlinearity[2]	Gain T.C. ppm/°C	Conversion Time µs	Logic	Temp. Range[3]	Volume* Section Page
AD ADC71JN	16	±0.006	NMC to 13 Bits	15	50	TTL	C	I-10-175
AD ADC71KN	16	±0.003	NMC to 14 Bits	15	50	TTL	C	I-10-175
AD ADC72JN	16	±0.006	NMC to 13 Bits	20	50	TTL	C	I-10-175
AD ADC72KN	16	±0.003	NMC to 14 Bits	20	50	TTL	C	I-10-175
AD ADC72AN	16	±0.006	NMC to 13 Bits	15	50	TTL	I	I-10-175
AD ADC72BN	16	±0.003	NMC to 14 Bits	15	50	TTL	I	I-10-175
HAS-1409KM	14	±0.006	NMC	20	8	TTL	I	I-10-207
HAS-1409AKM	14	±0.006	NMC	20	8	TTL	I	I-10-207
HAS-1409LM	14	±0.006	NMC	20	8	TTL	I	I-10-207
AD7552KN	12 + SIGN	±0.012	NMCOT	1 typ	160	TTL & CMOS	C	I-10-127
AD376JM	16	±0.006	NMCOT	15	17	TTL	C	S-3-41
AD376KM	16	±0.003	NMCOT	15	17	TTL	C	S-3-41

NOTES
[1]Suffix "N" – plastic DIP; Suffix "M" – metal DIP.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = –25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

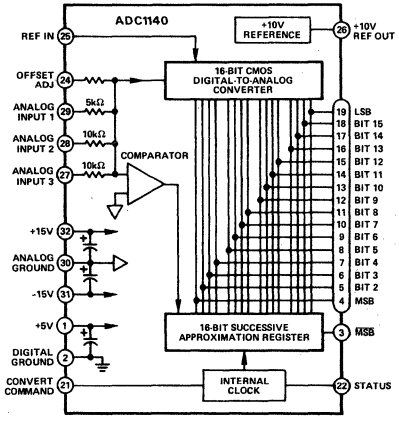
Analog-to-Digital Converters

High Resolution



ADC1130/ADC1131

14-Bit Resolution and Accuracy
Fast 12μs Conversion Time (ADC1131J/K)
Nonlinearity: ±0.003% max
Low 10ppm/°C Maximum Gain T.C.
User Choice of Input Range
No Missing Codes
Parallel and Serial Data Output



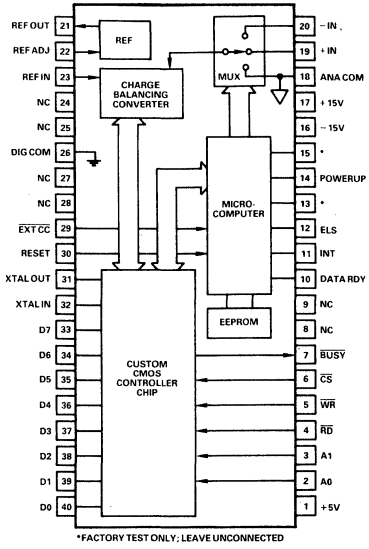
ADC1140

Low Cost 16-Bit A/D Converter
Guaranteed Nonlinearity: ±0.003% FSR[1] max
35μs Maximum Conversion Time
Small Size 2" × 2" × 0.4"
Wide Power Supply Operation: ±12V to ±17V

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Resolution Bits	Relative Accuracy % of FSR[1]	Differential Nonlinearity % of FSR[1]	Gain T.C. ppm/°C	Conversion Time μs	Output Logic	Temp. Range[2]	Volume* Section Page
ADC1130	14	±0.003	±0.006	12	25	TTL	C	II-11-27
ADC1131J	14	±0.003	±0.006	12	12	TTL	C	II-11-27
ADC1131K	14	±0.003	±0.003	10	12	TTL	C	II-11-27
ADC1140	16	±0.003	±0.003	12	35	TTL	C	II-11-31

NOTES
[1]FSR means Full Scale Range.
[2]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

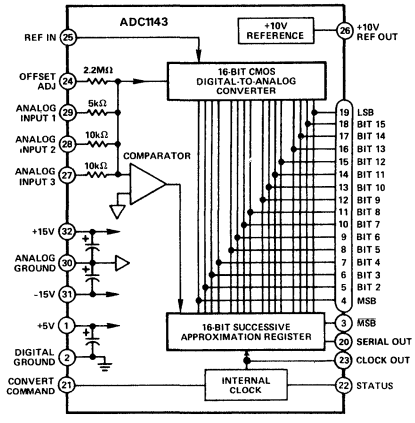


AD1170

Low Cost Integrating A/D Converter
Microcomputer-Based Design
- **Programmable Output Data Format:**
  - **7 to 18-Bit Resolution**
  - **Offset Binary or Two's Complement**
- **Programmable Integration Time:**
  - **1 to 350 Milliseconds**
- **Auto Zeroed and Electronic Calibration**

Low Integral Nonlinearity: ±10ppm FSR
High Normal Mode Rejection:
- **−54dB @ 60Hz**
- **−60dB @ 50Hz**

Microprocessor Compatible Interface
Small Size: 1.24″ × 2.5″ × 0.55″ maximum



ADC1143

High Performance 16-Bit A/D Converter
Low Power Consumption:
- **175mW max, V_S = ±15V**
- **150mW max, V_S = ±12V**

Guaranteed Nonlinearity:
- **±0.006% FSR max (ADC1143J)**
- **±0.003% FSR max (ADC1143K)**

Guaranteed Differential Nonlinearity:
- **±0.006% FSR max (ADC1143J)**
- **±0.003% FSR max (ADC1143K)**

Low Differential Nonlinearity T.C.:
- **±2ppm/°C max (ADC1143J)**
- **±1ppm/°C max (ADC1143K)**

Fast Conversion Time:
- **70µs max (ADC1143J)**
- **100µs max (ADC1143K)**

Wide Power Supply Operation:
- **V_S = ±11.4V to ±18.0V**
- **V_D = ±3.0V to +18.0V**

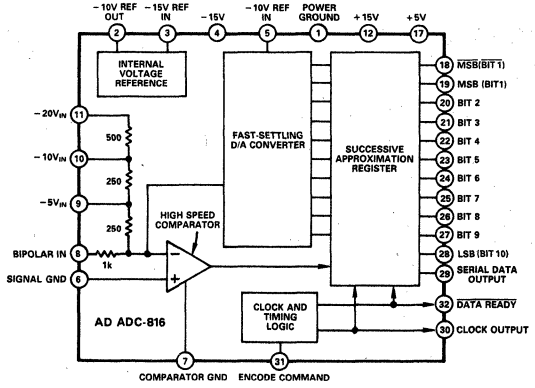
SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Resolution Bits	Relative Accuracy % of FSR[1]	Differential Nonlinearity % of FSR[1]	Gain T.C. ppm/°C	Conversion Time	Output Logic	Temp. Range[2]	Volume* Section Page
AD1170	18[3]	±0.001	±0.0008	5	1 to 350ms[4]	CMOS	C	S-3-173
ADC1143J	16	±0.0015	±0.0015	12	70µs	CMOS	C	II-11-35
ADC1143K	16	±0.0008	±0.0008	12	100µs	CMOS	C	II-11-35

NOTES
[1]FSR equals Full Scale Range.
[2]C = to +70°C.
[3]Resolution is user programmable from 7 to 22 Bits.
[4]Integration time is user programmable from 1 to 350 milliseconds.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

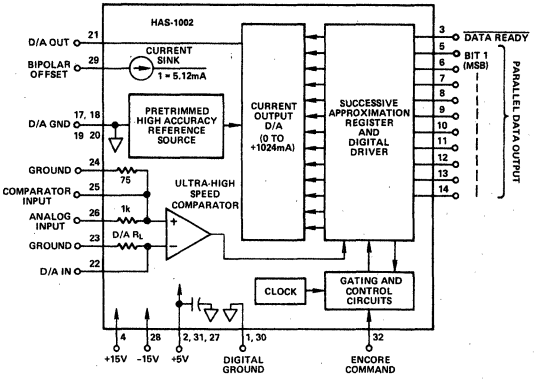
Analog-to-Digital Converters

High-Speed



AD ADC-816

10-Bit Resolution
800ns Conversion Time
Six Input Ranges
Unipolar or Bipolar



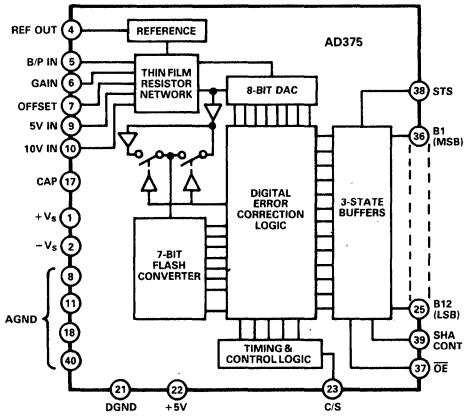
HAS-0802/HAS-1002

HAS-0802: 8 Bits Resolution
HAS-1002: 10 Bits Resolution
Low Power
Adjustment-Free Operation

SPECIFICATIONS – Min or Max at $T_A = +25°C$

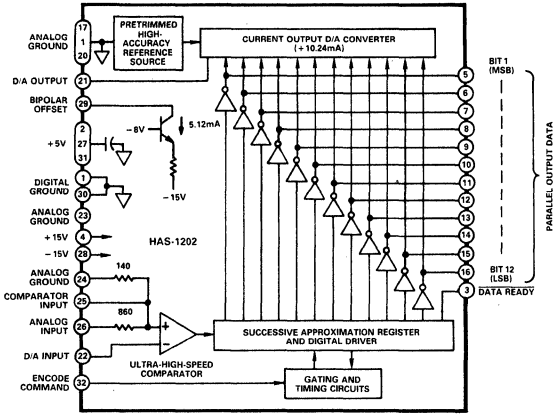
Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Gain T.C. ppm/°C	Conversion Time µs	Logic	Temp. Range[3]	Volume* Section Page
AD ADC-816KD	10	±1/2	NMC	28	800	TTL	C	S-3-323
AD ADC-816BD	10	±1/2	NMC	28	800	TTL	I	S-3-323
AD ADC-816SD	10	±1/2	NMC	28	800	TTL	E	S-3-323
HAS-0802	8	±1/2	NMCOT	30	1500	TTL	C	I-10-201
HAS-0802M	8	±1/2	NMCOT	30	1500	TTL	C	I-10-201
HAS-1002	10	±1/2	NMCOT	30	1700	TTL	C	I-10-201
HAS-1002M	10	±1/2	NMCOT	30	1700	TTL	C	I-10-201

NOTES
[1]No Suffix, Suffix "B", "D", "K", "S" – hermetic ceramic DIP; Suffix "M" – metal DIP.
[2]NMC – No missing codes; NMCOT – No missing codes over temperature.
[3]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD375

Guaranteed 12-Bit No Missing Codes Over Temperature
900ns Conversion Time
1MHz Throughput Rate
Small 40-Pin Hermetic Ceramic Package
T/H Control Line
Gain Accuracy 0.25% Untrimmed
Four Input Ranges (±2.5V, ±5V, 0 to +5V and 0 to +10V)
Tri-State Latched Output Data



HAS-1202/HAS-1202A

12-Bit Resolution
1.56µs Conversion Time
Conversion Rates to 641kHz

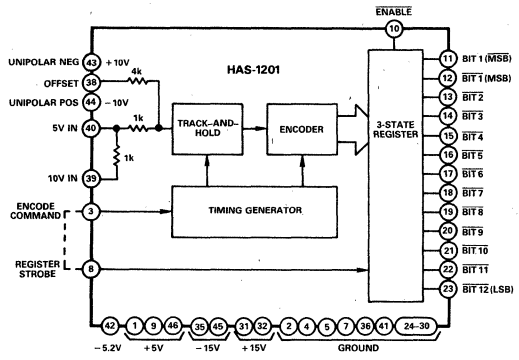
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity[2]	Gain T.C. ppm/°C	Conversion Time	Logic	Temp. Range[3]	Volume* Section Page
AD375KD	12	1	NMCOT	25	1000ns	TTL	C	S-3-39
HAS-1202	12	±1/2	NMC	60	2860µs	TTL	C	S-3-379
HAS-1202A	12	±1/2	NMC	60	1560µs	TTL	C	S-3-379
HAS-1202M	12	±1/2	NMC	60	2860µs	TTL	I	S-3-379
HAS-1202AM	12	±1/2	NMC	60	1560µs	TTL	I	S-3-379
HAS-1202MB	12	±1/2	NMC	60	2860µs	TTL	E[4]	S-3-379
HAS-1202AMB	12	±1/2	NMC	60	1560µs	TTL	E[4]	S-3-379

NOTES
[1]No Suffix, Suffix "A", "B", – hermetic ceramic DIP; Suffix "D" – Ceramic DIP; Suffix "M" – metal DIP.
[2]NMCOT – No missing codes over temperature; NMC – No missing codes.
[3]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
[4] – 55°C to +100°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

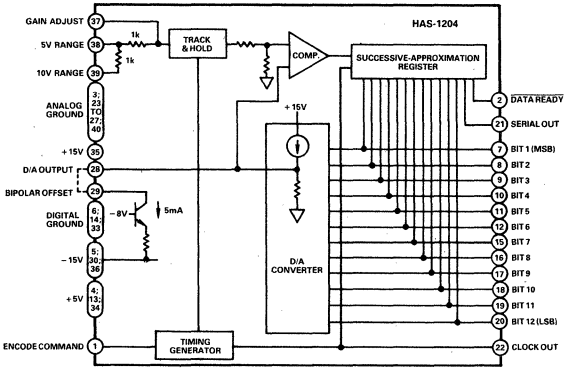
Analog-to-Digital Converters

High-Speed



HAS-1201

12-Bit Resolution
1MHz Word Rate
T/H and Timing Circuits
Single Hybrid Package



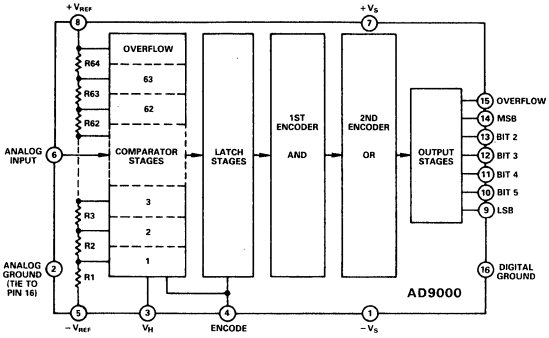
HAS-1204

12-Bit Resolution
500kHz Word Rate
Internal Track-and-Hold
Single 40-Pin DIP

SPECIFICATIONS – Min or Max at $T_A = +25°C$

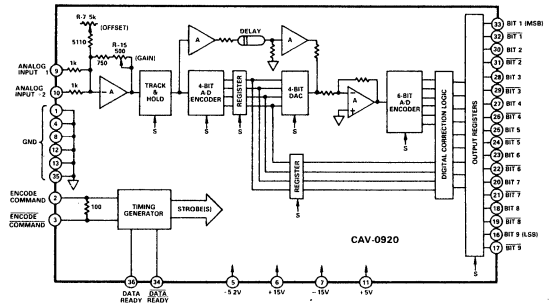
Model[1]	Resolution Bits	Relative Accuracy % FS	Linearity vs. Temp. ppm/°C	Small Signal BW (3dB)	Conversion Rate MHz	Logic	Temp. Range[2]	Volume* Section Page
HAS-1201KM	12	0.0125	10	2	1.05	TTL	C	S-3-377
HAS-1201SM(SMB)	12	0.0125	10	2	1.00	TTL	I[3]	S-3-377
HAS-1204BM	12	0.0125	3	7	0.5	TTL	I	S-3-381
HAS-1204SM	12	0.0125	3	7	0.5	TTL	E[4]	S-3-381

NOTES
[1]40-Pin Metal DIPs.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[3]HAS-1201SM/SMB will operate with derated performance over temperature range of −55°C to +100°C.
[4]−55°C to +100°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



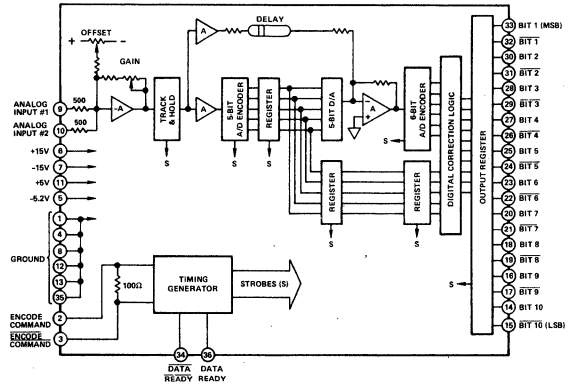
AD9000

6-Bit, 75MHz Minimum Rates
No T/H Required
−55°C to +125°C Temperature
Overflow Bit for Cascading



CAV-0920

9-Bit Resolution
20MHz Word Rates
Single 35-Inch² Card
ECL Compatible
No External Support Circuits



CAV-1040

10-Bit Resolution
40MHz Word Rates
Single 35-Inch² Card
ECL Compatible
No External Support Circuits

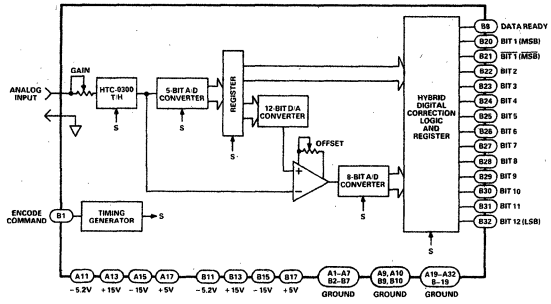
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy %FS	Linearity vs. Temp. ppm/°C	Small Signal BW (3dB)	Conversion Rate MHz	Logic	Temp. Range[2]	Volume* Section Page
AD9000JD	6	0.04	30	25	100	ECL	C	I-10-167
AD9000SD	6	0.04	30	25	100	ECL	E	I-10-167
CAV-0920	9	0.1	10	30	20	ECL	C	II-11-39
CAV-1040	10	0.05	10	30	40	ECL	C	S-4-9

NOTES
[1]AD9000 = 16-Pin ceramic DIP; CAV-0920 and CAV-1040 = 35-inch² card.
[2]C = 0 to +70°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

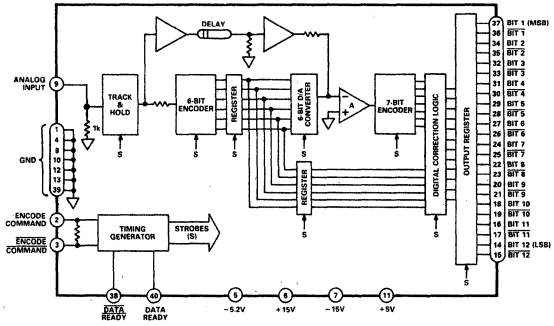
Analog-to-Digital Converters

Video



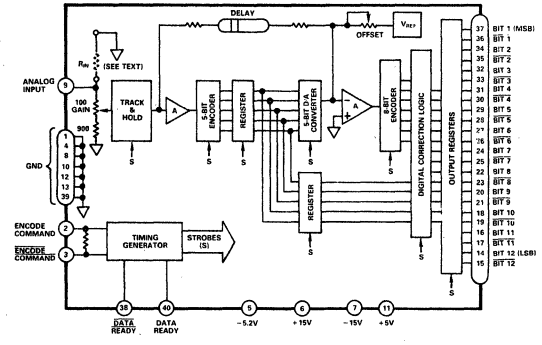
CAV-1202

12-Bit Resolution
2MHz Word Rates
Single Eurocard Size
TTL Compatible
No External Support Circuits



CAV-1210

12-Bit Resolution
10MHz Word Rates
Single 35-Inch² Card
ECL Compatible
No External Support Circuits



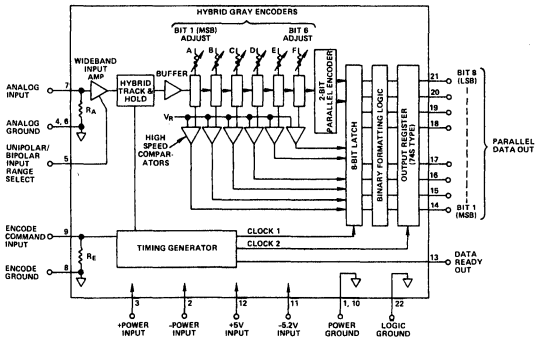
CAV-1220

12-Bit Resolution
20MHz Word Rates
Single 35-Inch² Card
ECL Compatible
No External Support Circuits

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy %FS	Linearity vs. Temp. ppm/°C	Small Signal BW (3dB)	Conversion Rate MHz	Logic	Temp. Range[2]	Volume* Section Page
CAV-1202	12	0.0122	10	5	2	TTL	C	S-4-11
CAV-1210	12	0.0125	10	35	10	ECL	C	II-11-45
CAV-1220	12	0.0125	10	40	20	ECL	C	S-4-13

NOTES
[1]CAV-1202 – Eurocard; CAV-1210 and CAV-1220 – 35-inch² card.
[2]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

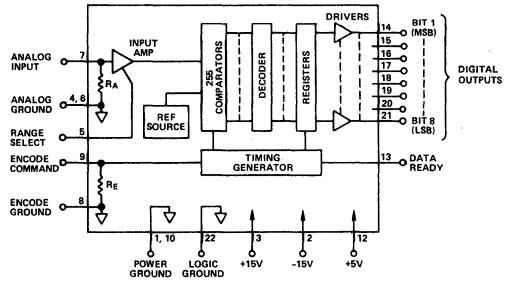


MATV-0811

8-Bit Resolution
11MHz Word Rates
Complete with T/H
Factory Repairable

MATV-0816

8-Bit Resolution
16MHz Word Rates
Complete with T/H
Factory Repairable



R_A AND R_E ARE DETERMINED BY THE ANALOG INPUT IMPEDANCE AND ENCODE COMMAND INPUT IMPEDANCE, RESPECTIVELY.

MATV-0820

8-Bit Resolution
20MHz Word Rates
Complete with T/H
Factory Repairable

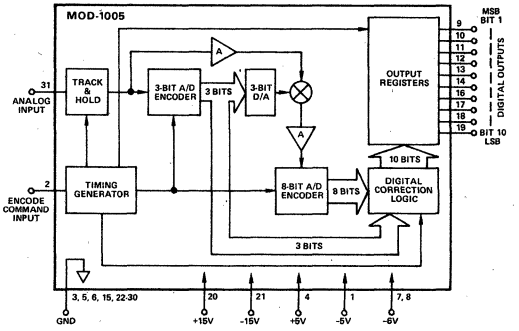
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy %FS	Linearity vs. Temp. ppm/°C	Small Signal BW (3dB)	Conversion Rate MHz	Logic	Temp. Range[2]	Volume* Section Page
MATV-0811	8	0.15	100	20	11	TTL	C	II-11-57
MATV-0816	8	0.15	100	20	16	TTL	C	II-11-57
MATV-0820	8	0.15	100	20	20	TTL	C	II-11-57

NOTES
[1]All units 5.5″ × 4.38″ × 0.85″.
[2]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

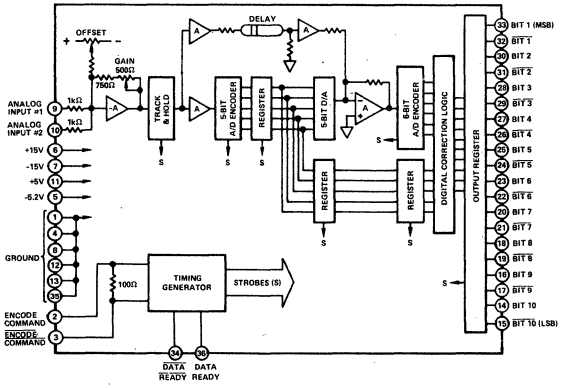
Analog-to-Digital Converters

Video



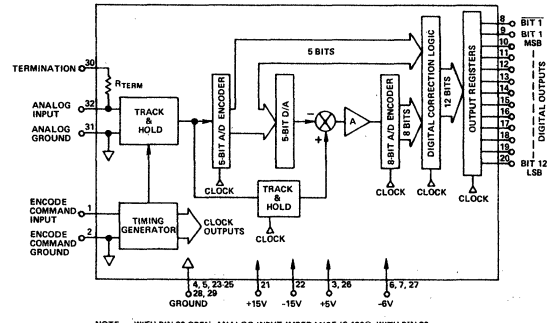
MOD-1005

10-Bit, 5MHz Word Rates
Complete with T/H
Single 27-Inch² Card
TTL Compatible



MOD-1020

10-Bit Resolution
20MHz Word Rates
Complete with T/H
ECL Compatible



NOTE: WITH PIN 30 OPEN, ANALOG INPUT IMPEDANCE IS 400Ω. WITH PIN 30 GROUNDED, ANALOG IMPEDANCE IS 50Ω.

MOD-1205

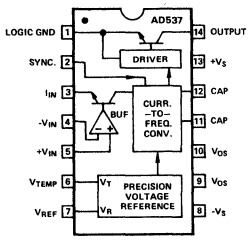
12-Bit Resolution
5MHz Word Rates
Built-In Track & Hold
TTL Compatible

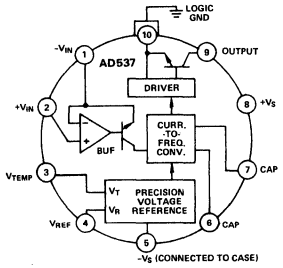
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Resolution Bits	Relative Accuracy %FS	Linearity vs. Temp. ppm/°C	Small Signal BW (3dB)	Conversion Rate MHz	Logic	Temp. Range[2]	Volume* Section Page
MOD-1005	10	0.05	5	20	5	TTL	C	II-11-61
MOD-1020	10	0.05	5	30	20	ECL	C	II-11-65
MOD-1205	12	0.0125	5	15	5	TTL	C	II-11-69

NOTES
[1]MOD-1005 – 27-inch² card; MOD-1020 and MOD-1205 – 35-inch² card.
[2]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

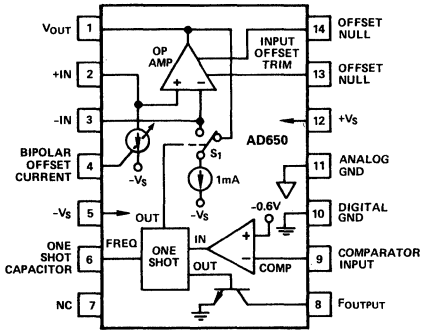
Voltage-to-Frequency Converters





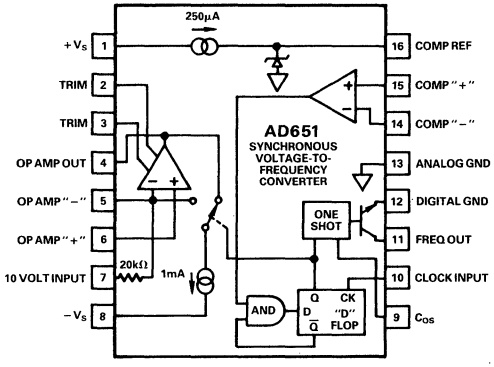
AD537

Low Cost A-D Conversion
Versatile Input Amplifier
Positive or Negative Voltage Modes
Negative Current Mode
High Input Impedance, Low Drift
Single Supply, 5 to 36 Volts
Linearity: ±0.05% FS
Low Power: 1.2mA Quiescent Current
Full Scale Frequency up to 100kHz
1.00 Volt Reference
Thermometer Output (1mV/K)
F-V Applications



AD650

V/F Conversion to 1MHz
Reliable Monolithic Construction
Very Low Nonlinearity
0.002% typ at 10kHz
0.005% typ at 100kHz
0.07% typ at 1MHz
Input Offset Trimmable to Zero
CMOS or TTL Compatible
Unipolar, Bipolar, or Differential V/F
V/F or F/V Conversion



AD651

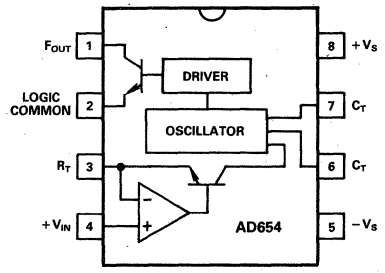
Full-Scale Frequency (Up to 2MHz) Set by External System Clock
No Critical External Components Required
Extremely Low Linearity Error
(0.005% max at 100kHz
0.02% max at 2MHz)
Low Drift (25ppm/°C max)
Dual or Single Supply Operation
Voltage or Current Input

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Full Scale Frequency MHz	Nonlinearity at f_{max} – % 10kHz,	100kHz,	250kHz,	500kHz,	1MHz,	2MHz	Logic Output	Temp. Range[2]	Volume* Section Page
AD537JH(JD)	0.15	0.15	0.25	–	–	–	–	Symmetrical	C/C	I-11-7
AD537KH(KD)	0.15	0.07	0.1	–	–	–	–	Symmetrical	C/C	I-11-7
AD537SH(SD)	0.15	0.07	0.1	–	–	–	–	Symmetrical	C/C	I-11-7
AD650JN(AD)	1.0	0.005	0.02	–	0.05	–	–	Pulse	C/I	I-11-15
AD650KN(BD)	1.0	0.005	0.02	–	0.05	0.1	–	Pulse	C/I	I-11-15
AD650SD	1.0	0.005	0.02	–	0.05	0.1	–	Pulse	E	I-11-15
AD651AQ(SQ)	2.0	–	0.02	–	0.02	0.02	0.05	Pulse	I/E	S-3-137
AD651BQ	2.0	–	0.005	–	0.005	0.005	0.02	Pulse	I	S-3-137

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP; Suffix "H" – metal header.
[2]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

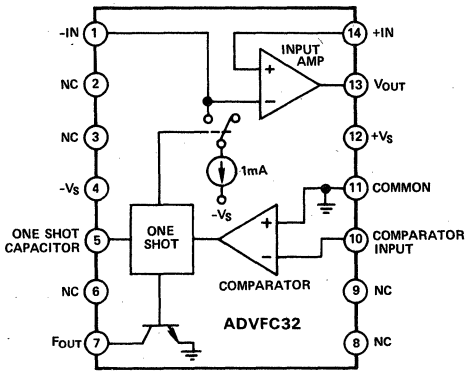
Voltage-to-Frequency Converters



AD654

Low Cost
Single or Dual Supply, 5 to 36 Volts, ±5V to ±18V
Full Scale Frequency Up to 500kHz
Minimum Number of External Components Needed
Versatile Input Amplifier
- **Positive or Negative Voltage Modes**
- **Negative Current Mode**
- **High Input Impedance, Low Drift**

Low Power: 2.0mA Quiescent Current
Low Offset: 1mV



ADVFC32

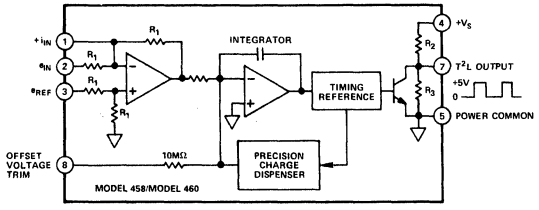
High Linearity
- **±0.01% max at 10kHz FS**
- **±0.05% max at 100kHz FS**
- **±0.2% max at 0.5MHz FS**

Output DTL/TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Full Scale Frequency MHz	Nonlinearity at f_{max} – % 10kHz,	100kHz,	250kHz,	500kHz,	1MHz,	2MHz	Logic Output	Temp. Range[2]	Volume* Section Page
AD654JN	0.5	–	–	0.1	0.4	–	–	Symmetrical	C	S-3-153
ADVFC32KN	0.5	0.01	0.05	–	0.2	–	–	Pulse	C	I-11-27
ADVFC32BH	0.5	0.01	0.05	–	0.2	–	–	Pulse	I	I-11-27
ADVFC32SH	0.5	0.01	0.05	–	0.2	–	–	Pulse	E	I-11-27

NOTES
[1]Suffix "N" – plastic DIP; Suffix "H" – metal header.
[2]C = 0 to +70°C, I = –25°C to +85°C, E = –55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



458/460

Model 458: Full Scale Output 100kHz
Model 460: Full Scale Output 1MHz
High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
High Linearity: ±0.01% max at 100kHz, Model 458
±0.015% max at 1MHz, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL Compatible Output
No External Components to Meet Rated Performance

SPECIFICATIONS – Min or Max at T_A = +25°C

Model	Input Range V	Input Range mA	Full Scale Output kHz	Nonlinearity Error %	Gain T.C. ppm/°C	Temp. Range[1]	Volume* Section Page
458J	0 to ±10	0 to +0.5	100	0.01	20	C	II-12-13
458K	0 to ±10	0 to +0.5	100	0.01	10	C	II-12-13
458L	0 to ±10	0 to +0.5	100	0.01	5	C	II-12-13
460J	0 to ±10	0 to +1	1000	0.015	50	C	II-12-13
460K	0 to ±10	0 to +1	1000	0.015	25	C	II-12-13
460L	0 to ±10	0 to +1	1000	0.015	15	C	II-12-13

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Synchro, Resolver, Inductosyn* and LVDT-to-Digital Converters

All of the products described below use the tracking conversion technique in which the digital output follows the synchro or resolver shaft automatically without the need for convert commands or wait loops. Apart from producing instantaneous angular data, this inherently ratiometric conversion method is also very tolerant of noise on the signal inputs as well as voltage drops between the transducer and the converter. Advantage can, therefore, be taken of the fact that angular data can be transmitted in analog format through noisy environments to a digital converter which may be a considerable distance away from the resolver, synchro or LVDT.

Many of the hybrid products and all of the modular products contain internal transformer isolation and much use is made of custom integrated circuits.

Applications for the products range from military and aerospace uses such as radar and sonar to industrial jobs such as robotics and CNC. Industrial applications have become very prominent in the last few years since it has been recognized that a brushless resolver and an R-to-D converter provide an unbeatable, cost effective and reliable method of obtaining an absolute digital representation of angular movement.

Resolution (Bits)	Product	Output Format[1]	Input Format[2]	Accuracy (arc mins)	Tracking Rate Options (revs/sec)[3]	Reference Frequency Options (Hz)	Signal Input Options (V rms)
10	1S10	BIN	I, R	±25	360, 680	2.6k → 5k, 5k → 10k	2.0
10	1S14	BIN	I, R	±25	680	2k → 10k	2.0
10	SDC/RDC1702	BIN	S, R	±21	5, 36, 75	60, 400, 2.6k	11.8, 26, 90
10	SDC/RDC1726	BIN	S, R	±21	5, 36, 50	60, 400, 2.6k	11.8, 26, 90
12	SDC/RDC1741	BIN	S, R	±15.3	18	400, 2.6k	11.8, 26, 90
12	SDC/RDC1742	BIN	S, R	±8.5	18	400, 2.6k	11.8, 26, 90
12	SDC/RDC1767	BIN	S, R	±8.5	36	400, 2.6k	11.8, 26, 90
12	1S20	BIN	I, R	±8.5	50, 90, 170	400 → 2.6k, 2.6k → 5k, 5k → 10k	2.0
12	1S24	BIN	I, R	±8.5	170	2k → 10k	2.0
12	2S20	BIN	I, R	±11[5]	100	1k → 10k	2.5
12	SDC/RDC1700	BIN	S, R	±8.5	5, 36, 75	60, 400, 2.6k	11.8, 26, 90
12	SDC/RDC1725	BIN	S, R	±8.5	5, 36, 50	60, 400, 2.6k	11.8, 26, 90
12	IRDC1730	BIN	I, R	±8.5	68, 87, 170	400, 2.6k, 5k, 10k	2.5
4000 Counts	IRDC1731	Serial	I, R	±2 Counts	100	5k	2.5
12	IRDC1732	BIN	I, R	±21	50, 100	400, 1k → 10k	2.5
12	IRDC1733	BIN	I, R	±8.5	68, 87, 170	400, 2.6k, 5k, 10k	2.5
14	SDC/RDC1740	BIN	S, R	±5.2	12	400, 2.6k	11.8, 26, 90
14	SDC/RDC1768	BIN	S, R	±5.3	12	400, 2.6k	11.8, 26, 90
14	1S40	BIN	I, R	±5.3	12.5, 22.5, 42.5	400 → 2.6k, 2.6k → 5k, 5k → 10k	2.0
14	1S44	BIN	I, R	±5.3	42.5	2k → 10k	2.0
14	SDC/RDC1704	BIN	S, R	±4	1.4, 12, 25	60,400, 2.6k	11.8, 26, 90
14	SBCD/RBCD1752	BCD	S, R	±0.2°	5, 36, 75	60, 400, 2.6k	11.8, 26, 90
14	SBCD/RBCD1753	BCD	S, R	±0.2°	5, 36, 75	60, 400, 2.6k	11.8, 26, 90
14	SBCD/RBCD1756	BCD	S, R	±0.2°	5, 36, 75	60, 400, 2.6k	11.8, 26, 90
14	SBCD/RBCD1757	BCD	S, R	±0.2°	5, 36, 75	60, 400, 2.6k	11.8, 26, 90
16	1S60	BIN	I, R	±4.0, ±2.6[5]	3, 5.5, 10.5	400 → 2.6k, 2.6k → 5k, 5k → 10k	2.0
16	1S61	BIN	I, R	±10, ±4.0[5]	3, 5.5, 10.5	400 → 2.6k, 2.6k → 5k, 5k → 10k	2.0
16	1S64	BIN	I, R	±4.0, ±2.6[5]	10.5	2k → 10k	2.0
16	SDC/RDC1711	BIN	S, R	±1.3	3	400	11.8, 26, 90
16	SDC/RDC1721	BIN	S, R	±0.67	3	360–2.9k	11.8, 26, 90
16, 14, 12, 10[6]	1S74	BIN	I, R	±2.6[7]	680[7]	2k → 10k	2.0
11	2S50	BIN	LVDT	0.1[8]	200LSB/ns[9]	400, 1k → 10k	2.5

NOTES

[1]BIN = Binary; BCD = Binary Coded Decimal; Serial = 4000 count serial output.

[2]S = Synchro; R = Resolver; I = Inductosyn.

[3]Revs/sec equivalent to pitches/sec in the case of an Inductosyn; in general higher reference frequency options have higher tracking rates.

[4]C = 0 to +70°C; E = −55°C to +125°C; MR = −55°C to +105°C.

[5]Consult Data Sheet.

[6]Resolution is User Selectable.

[7]Depends on Resolution Selected.

[8]LVDT Converter Accuracy given as % Full Scale.

[9]Slew Rate (min).

*Inductosyn is a registered trademark of Farrand Industries, Inc.

Reference Input Options (V rms)	Transformer I/P Isolation	Package Type	Operating Temperature (°C)[4]	Features
2.0	No	32-Pin Triple DIP	C, E	High Tracking Rate with Velocity, Error, Ripply Carry and Direction Outputs. Latched Tri-State Output. Low Cost
2.0	No	40-Pin Triple DIP	C, E	High Speed, Inductosyn/Resolver Converter with Tachogenerator Velocity Output
11.8, 26, 115	Yes	Module	C, MR	Industry Standard Modular Converter
11.8, 26, 115	Yes	Module	C, MR	Tri-State, Latched Output
11.8, 26, 115	Yes	32-Pin Triple DIP	C, E	Tri-State, Latched Output Internal Transformer Isolation
11.8, 26, 115	Yes	32-Pin Triple DIP	C, E	Tri-State, Latched Output Internal Transformer Isolation
11.8, 26, 115	Yes	32-Pin Triple DIP	C, E	Tri-State, Latched Output High Tracking Rate. Error Output Velocity Output. Internal Transformer Isolation
2.0	No	32-Pin Triple DIP	C, E	High Tracking Rate with Velocity, Error, Ripple Carry and Direction Outputs. Latched, Tri-State Output. Low Cost
2.0	No	40-Pin Triple DIP	C, E	High Speed, Inductosyn/Resolver Converter with Tachogenerator Velocity Output
2.5	No	32-Pin Triple DIP	C	Low Cost, High Speed, Inductosyn/Resolver Converter
11.8, 26, 115	Yes	Module	C, MR	Industry Standard Modular Converter
11.8, 26, 115	Yes	Module	C, MR	Tri-State, Latched Output
2.5	Yes	Module	C, MR	High Speed, Inductosyn/Resolver Converter
2.5	Yes	Module	C, MR	High Speed, Serial Output, Inductosyn/Resolver Converter
2.5	No	32-Pin Triple DIP	C, E	Low Cost, High Speed, Inductosyn/Resolver Converter
2.5	Yes	Module	C, MR	As IRDC1730 But No dc Velocity Output
11.8, 26, 115	Yes	32-Pin Triple DIP	C, E	Tri-State, Latched Output Internal Transformer Isolation
11.8, 26, 115	Yes	32-Pin Triple DIP	C, E	Tri-State, Latched Output, Error and Velocity Outputs. Internal Transformer Isolation.
2.0	No	32-Pin Triple DIP	C, E	High Tracking Rate with Velocity, Error, Ripple Carry and Direction Outputs. Latched, Tri-State Output. Low Cost
2.0	No	40-Pin Triple DIP	C, E	High Speed, Inductosyn/Resolver Converter with Tachogenerator Velocity Output
11.8, 26, 115	Yes	Module	C, MR	Industry Standard Modular Converter
11.8, 26, 115	Yes	Module	C, MR	± 180.0° BCD Output
11.8, 26, 115	Yes	Module	C, MR	0 to 360° BCD Output
11.8, 26, 115	Yes	Module	C, MR	± 180° BCD Output. + 15V and + 5V dc Power Supply
11.8, 26, 115	Yes	Module	C, MR	0 to 360° BCD Output. + 15V and + 5V dc Power Supply
2.0	No	32-Pin Triple DIP	C, E	High Tacking Rate with Velocity, Error, Ripple Carry and Direction Outputs. Latched, Tri-State Output. Low Cost
2.0	No	32-Pin Triple DIP	C, E	Lower Accuracy Version of 1S60. Low Cost
2.0	No	40-Pin Triple DIP	C, E	High Speed, Inductosyn/Resolver Converter with Tachogenerator Velocity Output
11.8, 26, 115	Yes	Module	C, MR	Low Profile Modular, 16-Bit Converter
11.8, 26, 115	Yes	Module	C, MR	Modular 16-Bit Converter
2.0	No	40-Pin Triple DIP	C, E	High Speed, Inductosyn/Resolver Converter with Tachogenerator Velocity Output and User Selectable Resolution
2.5	No	32-Pin Triple DIP	C, E	Direct Conversion of LVDT Signal, No External Trims Required, Tri-State Output

Digital-to-Synchro and Resolver Converters

In addition to the traditional industry standard modular digital-to-synchro and resolver converters, Analog Devices manufacture the DRC1745 and DRC1746. These hybrid converters feature internal 2VA power amplifiers, latched inputs, optional TransZorb* protection on the outputs and the facility of using a pulsating power supply for greatly reduced power dissipation. These products modulate an ac or dc reference voltage by the sine and cosine of an input digital angle. Along with the DRC1765 and DRC1766, which are similar but have no power output stage, these products can be used for a variety of applications including digital-to-synchro and resolver conversion and PPI waveform generation.

Resolution (Bits)	Product	Input Format[1]	Output Format[2]	Accuracy (arc mins)	Load Driving Capability	Reference Frequency Options (Hz)	Reference Input Voltage Options (V rms)	Signal Output Voltage Options (V rms)
DSC/DRC1706	12	BIN	S,R	±8	1.3VA	60,400	11.8,26,115	11.8,26,90
DTM1717	12	BIN	R	±3	5mA	dc →8000	0→7	0→7
DSC/DRC1705	14	BIN	S,R	±4	1.3VA	60,400	11.8,26,115	11.8,26,90
DTM1716	14	BIN	R	±3	5mA	dc →8000	0→7	0→7
DRC1745	14	BIN[4]	R	±2, ±4[5]	2.0VA[6]	dc →2600	0→3.4	0→6.8
DRC1765	14	BIN[4]	R	±2, ±4[5]	4.3mA	dc →2600	0→3.4	0→6.8
DRC1746	16	BIN[4]	R	±2, ±4[5]	2.0VA[6]	dc →2600	0→3.4	0→6.8
DRC1766	16	BIN[4]	R	±2, ±4[5]	4.3mA	dc →2600	0→3.4	0→6.8

NOTES
[1]BIN = Binary. [2]S = Synchro; R = Resolver. [3]C = 0 to +70°C; MR = −55°C to +105°C; E = −55°C to +125°C [4]Two byte latched input, CMOS or low power Schottky depending on option.

Transformers

Input transformers are of two types, Reference and Signal. Reference transformers are used to isolate the reference input to either a digital-to-resolver or a resolver-to-digital converter. Signal transformers are used to isolate the signal inputs to a resolver-to-digital converter.

Output transformers can be used with the digital-to-resolver converter products to provide an isolated synchro or resolver output. Converters without a power output stage will require the SPA1695 amplifier. All the modules except for the STM/RTM1683 contain an input reference transformer.

INPUT TRANSFORMERS

Product	Description	Frequency (Hz)	Accuracy (arc mins)	Input Voltage Options (V rms)[1]	Package Type	Package Size Inches (mm)
STM1680	Ref isolation for DRC1745 and DRC1746	400	N/A	11.8, 26, 11.5	Module	1.12×1.12×0.4 (28.5×28.5×10.2)
5S72	Ref isolation for 1S14/24/44/64/74 and 1S10/20/40/60/61	360 to 3000	N/A	11.8, 26, 11.5	Module	1.12×1.12×0.4 (28.5×28.5×10.2)
5S70	Signal input for 1S14/24/44/64/74 and 1S10/20/40/60/61	360 to 3000	±0.33 (typ) ±1.5 (max)	11.8, 26, 90	Module	2.25×1.12×0.4 (57.0×28.5×10.2)

OUTPUT TRANSFORMERS

Product	Description	Frequency (Hz)	Accuracy (arc mins)	Power Handling (VA)	Output Voltage Options (V rms)[1]	Package Type	Package Size Inches (mm)
STM/RTM1679	Output and ref for 60Hz DSC1705 and DSC1706 Options.	60	±2.0	1.3	11.8, 26, 90	Module	4.5×2.0×1.5 (114.3×50.8×38.1)
STM/RTM1681	Output and ref for DRC1745 and DRC1746	400	±2.5@ 1.4VA	2.0	11.8, 26, 90	Module	3.125×1.5×1.0 (79.4×38.1×25.4)
STM/RTM1683	Output for DRC1745 and DRC1746	400	±2.5@ 1.4VA	2.0	11.8, 26, 90	Module	2.25×1.13×0.4 (57.1×28.7×10.2)
STM/RTM1686	Output and ref for 400Hz DRC1765/1766 or DTM1716/1717 and SPA1695	400	±2.4	5.0	11.8, 90	Module	4.5×2.0×1.5 (114.3×50.8×38.1)
STM1687	Output and ref set for 60Hz DRC1765/1766, DTM1716/1717 and SPA1695	60	±2.4	5.0	90	Three Transformer set	See individual data sheet.
STM/RTM1696	Output and ref for 400Hz DRC1705/1706, and and SPA1695 combination	400	±2.4	5.0	11.8, 90	Module	4.5×2.0×1.5 (114.3×50.8×38.1)
STM1697	Output and ref set for 60Hz DRC1705/1706 and SPA1695 combination	60	±2.4	5.0	90	Three Transformer set	See individual data sheet.

NOTE
[1]Synchro and resolver format available on all models except STM1687 and STM1697.

Transformer Output Isolation	Package Type	Operating Temperature (°C)[3]	Features
Int. on 400Hz Options. Use STM1679 on 60Hz Options.	Module	C, MR	Industry Standard Modular Converter
No	Module	C, MR	Digital Vector Generator. Dc or ac Sin and Cos outputs. Used as D to S/R with Ext Amp, e.g., SPA1695 or for Display Applications.
Int. on 400Hz Options. Use STM1679 on 60Hz Options.	Module	C, MR	Industry Standard Modular Converter
No	Module	C, MR	14-Bit Version of DTM1717
Use Ext. STM1681 or STM1683 Transformer	40-Pin Triple DIP	E	Digital-to-Resolver Converter with Int. 2VA Power Amplifier. Optional Int. TransZorb Protection. 2 Byte Latched Inputs.
No	32-Pin Triple DIP	E	Hybrid Digital Vector Generator. Dc or ac Sin and Cos Outputs Can be Used for (PPI) Display or with Ext. Amp (e.g., SPA1695) for D to S/R Conversion.
Use Ext. STM1681 or STM1683 Transformer	40-Pin Triple DIP	E	16-Bit Version of DRC1745
No	32-Pin Triple DIP	E	16-Bit Version of DRC1765

[3]Depends on option. [4]Can be used with pulsating power supply for reduced dissipation. *TransZorb is a trademark of General Semiconductor Industries, Inc.

Inductosyn Ancillary Products

These oscillators and pre-amps are used with linear and rotary Inductosyns.

Product	Description	Package Type	Package Size Inches (mm)	Operating Temperature (°C)[1]
IPA1751	High gain pre-amp (sine and cos) to amplify Inductosyn slider or stator voltages to converter levels.	Module	2.0 × 2.0 × 0.4 (50.8 × 50.8 × 10.2)	C, MR
OSC1754	Drive oscillator for Inductosyn track or rotor. 10kHz. 5VA.	Module	3.125 × 2.625 × 1.0 (79.4 × 66.7 × 25.4)	C, MR
OSC1758	Drive oscillator for Inductosyn track or rotor. 1.5VA.	Hybrid IC	0.98 × 0.78 × 0.18 (24.9 × 19.8 × 4.6)	E
IPA1764	High gain pre-amp (sin and cos) to amplify Inductosyn slider or stator voltages to converter levels.	Hybrid IC	0.98 × 0.78 × 0.18 (24.9 × 19.8 × 4.6)	E

NOTES
[1]C = 0 to +70°C; MR = −55°C to +105°C; E = −55°C to +125°C.

Instruments and Systems

Product	Description	Dimensions Inches (mm)
API1620	Angle position indicator. Accepts synchro, magslip or resolver information and displays angular position in degrees/fractions to one arc-minute accuracy. Digital O/P on rear connector.	11.75 × 8 × 4 (300 × 204 × 102)
API1718	NATO codified version of API1620. (Code 6625–99–539–8389) degrees/minutes instead of degrees fractions.	11.75 × 8 × 4 (300 × 204 × 102)
MCI1794	Three channel resolver-to-digital converter board. Intel MULTIBUS* Compatible. Uses 3 IRDC1730 and includes 24-bit pitch counter for each channel.	6.25 × 12.00 (171.5 × 304.8)

NOTE
*MULTIBUS is a trademark of Intel Corporation.

Special Functions

These products provide additional interfacing capability to positional control and readout systems.

Product	Description	Package Type	Package Size Inches (mm)	Operating Temperature (°C)[1]
TSL1612	Combines the coarse and fine digital outputs of a two speed synchro or resolver system into a single composite digital word. Standard ratios of 9:1, 18:1, 36:1. Other ratios available.	Module	3.125 × 2.625 × 0.4 (79.4 × 66.7 × 10.2)	C, MR
BDM1615/1616	Binary angle to BCD converters. BDM1615 14-bits I/P, degrees/fractions O/P. BDM1616 14-bit, I/P, degrees/mins O/P.	Module	4.0 × 2.0 × 0.4 (101.6 × 51.0 × 10.2)	C, MR
BDM1617	Binary angle to BCD converter. 16-bit input, degrees/fractions output.	Module	3.125 × 2.625 × 0.8 (79.4 × 66.7 × 20.4)	C, MR
SSCT1621	Solid state control transformer. Give ac difference between synchro or resolver input and digital angle.	Module	3.125 × 2.625 × 0.8 (79.4 × 66.7 × 20.4)	C, MR
SCDX1623	Solid state control differential transmitter gives resolver format difference between synchro or resolver input and digital angle.	Module	3.125 × 2.625 × 0.8 (79.4 × 66.7 × 20.4)	C, MR
SPA1695	Two channel (sine and cos) power amp. 5VA.	Die Cast Metal Case	3.46 × 2.68 × 0.98 (88.0 × 68.0 × 25.0)	MR
SAC1763	Synchro or resolver input to dc linear output converter.	Module	3.125 × 2.625 × 0.8 (79.4 × 66.7 × 20.4)	C, MR

NOTE
[1]C = 0 to +70°C; MR = −55°C to +105°C.

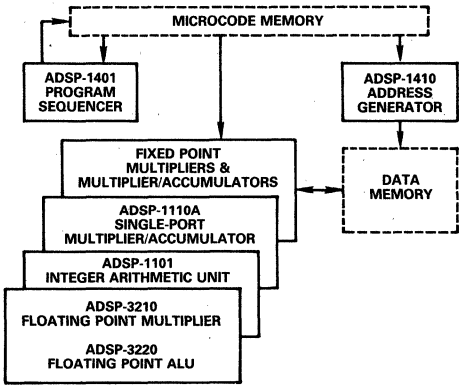
High-Speed DSP and Numerical Processing Components

Analog Devices offers the industry's most complete family of CMOS IC's for high-performance digital signal/numerical processors. Fabricated in 1.5 micron CMOS, this new generation of VLSI devices provides all the key functional elements required to build high-speed, math-intensive processors. The family consists of fixed point multipliers and multiplier/accumulators, floating point processors, a program sequencer, and an address generator.

The ADSP product family is designed to optimize system performance. ADSP products support a system cycle time of 10MHz (much more for some components). Powerful on-chip operations expand system functionality and flexibility – saving processing time and hardware. A wide range of data formats allows the designer to optimize system precision and throughput.

ADSP components reduce the cost and improve the reliability of systems. Functions which previously required many discrete components have been integrated into a few VLSI chips – yielding a substantial savings in board space. With a small number of CMOS components, power supply and cooling requirements are reduced. The low operating temperature of CMOS components provides increased reliability relative to bipolar components which run hotter due to much greater power dissipation. All ADSP components are available processed fully to MIL-STD-883B, Rev C, and can be safely specified for operation over their extended temperature range (−55°C to +125°C ambient).

ADSP PRODUCT FAMILY



ADSP-1401	16-Bit Program Sequencer
ADSP-1410	16-Bit Cascadable Address Generator
ADSP-1101	16-Bit Integer Arithmetic Unit

Floating Point Processors

ADSP-3210	64-Bit IEEE Floating Point Multiplier
ADSP-3220	64-Bit IEEE Floating Point ALU

Fixed Point Multipliers

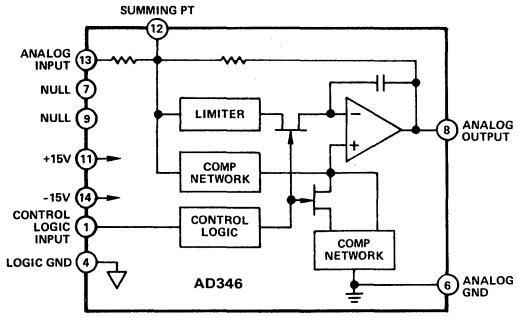
ADSP-1080A	8-Bit Multiplier (twos complement only)
ADSP-1081A	8-Bit Multiplier (unsigned only)
ADSP-1012A	12-Bit Multiplier
ADSP-1016A	16-Bit Multiplier
ADSP-1516	16-Bit Multiplier
ADSP-1102	16-Bit Pipelined Multiplier
ADSP-1517	16-Bit Multiplier
ADSP-1103	16-Bit Pipelined Multiplier
ADSP-1024A	24-Bit Multiplier

Fixed Point Multiplier/Accumulators

ADSP-1008A	8-Bit Multiplier/Accumulator
ADSP-1009A	12-Bit Multiplier/Accumulator
ADSP-1010A	16-Bit Multiplier/Accumulator
ADSP-1110A	16-Bit Single-port Multiplier/Accumulator

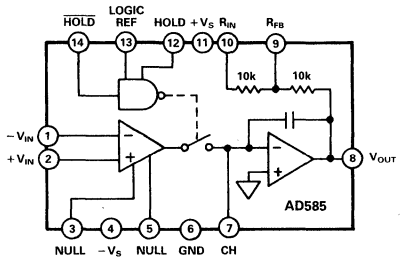
Sample/Track Hold Amplifiers

General Purpose



AD346

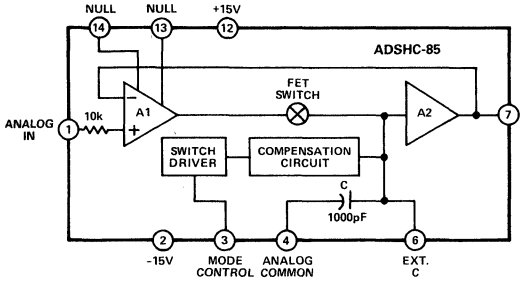
Fast 2.0μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor



AD585

Fast 2.5μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset: 1mV
Sample/Hold Offset Step: 1mV
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements



ADSHC-85

Improved SHC-85 Replacement
500ns Sample-to-Hold Transient
50μV rms Noise
Low Droop Rate of 0.2mV/ms

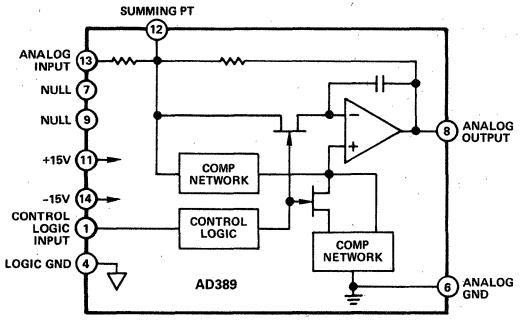
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Open Loop Gain V/V	Gain Bandwidth MHz	Acquisition Time (to 0.01%) μs	Aperture Time ns	Aperture Uncertainty ns	Droop Rate	Temp. Range[2]	Volume* Section Page
AD346JD	−1	1.4	2.0	60	0.4	0.5mV/μs	C	I-14-11
AD346SD	−1	1.4	2.0	60	0.4	0.5mV/μs	E	I-14-11
ADSHC-85	+1	3.0	4.5	25	0.5	0.2mV/ms	C	I-14-37
ADSHC-85ET	+1	3.0	4.5	25	0.5	0.2mV/ms	E	I-14-37
AD585AQ	200,000	2.0	3.0	35	0.5	1mV/ms	I	S-3-93
AD585SQ	200,000	2.0	3.0	35	0.5	1mV/ms	E	S-3-93

NOTES
[1]Suffix "D" – ceramic DIP; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

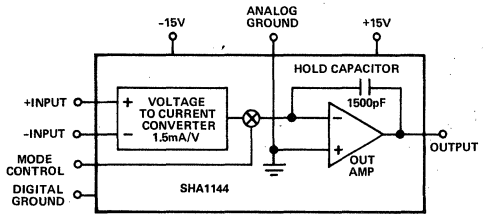
Sample/Track-Hold Amplifiers

High Resolution



AD389

Companion to High Resolution A/D Converters
Fast Acquisition Time: 2.5μs to ±0.003%
Low Droop Rate: 0.1μV/μs
Aperture Jitter: 400ps
Internal Hold Capacitor
Unity Gain Inverter
Low Power Dissipation: 300mW



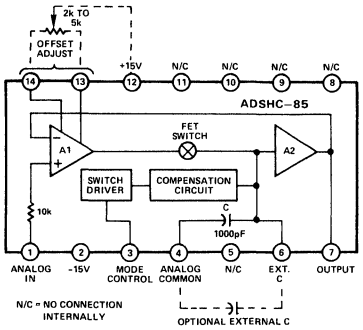
SHA1144

High Resolution 14-Bit Sample-and-Hold Amplifier
±10V Range
50ns Aperture Delay
0.5ns Aperture Jitter
Acquisition Time: 6μs to ±0.003%
6μs Settling Time
±0.001% Max Gain Linearity Error
Complete with Input Buffer: No External Components Required to Meet Rated Performance

SPECIFICATIONS – Min or Max at T_A = +25°C

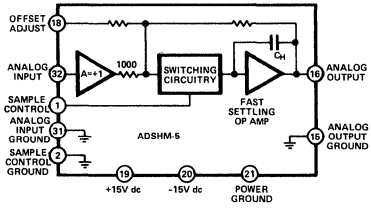
Model[1]	Open Loop Gain V/V	Gain Bandwidth MHz	Acquisition Time (0.01%) μs	Aperture Time ns	Aperture Uncertainty ns	Droop Rate μV/μs	Temp. Range[2]	Volume* Section Page
AD389KD	−1	1.5	2.5[3]	30	0.4	0.1	C	I-14-17
AD389BD	−1	1.5	2.5[3]	30	0.4	0.1	I	I-14-17
SHA1144	+1	1 typ	8	50	0.5	2	C	II-14-15

NOTES
[1]Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C.
[3]Accuracy to ±0.003%.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



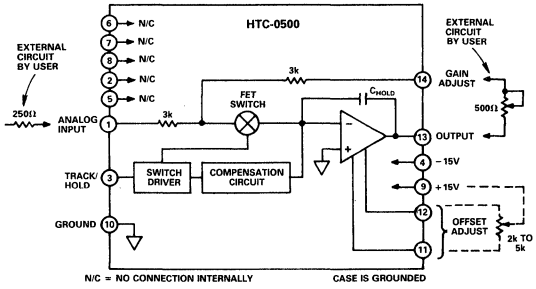
ADSHC-85

Improved ADSHC-85 Replacement
500ns Sample-to-Hold Time
50μV rms Noise
Low Droop Rate



ADSHM-5/ADSHM-5K

Improved SHM-5 Replacement
350ns Acquisition Time to ±0.01%
Aperture Uncertainty 250ps
250V/μs Slew Rate
2nA Input Bias Current



HTC-0500

700ns Acquisition Time
<750mW Power Dissipation
14-Pin DIP
0.01% Linearity

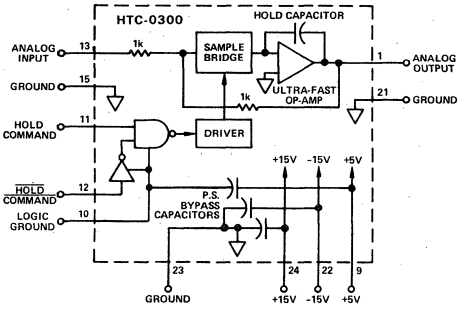
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Open Loop Gain V/V	Small Signal BW MHz	Acquisition Time–ns (0.01%)	Aperture Time ns	Aperture Jitter ps	Droop Rate μV/μs	Temp. Range[2]	Volume* Section Page
ADSHC-85	+1	3	4500	25	500	0.2	C	I-14-37
ADSHC-85ET	+1	3	4500	25	500	0.2	E	I-14-37
ADSHM-5	−1	5	1000	20	250	20	C	II-14-11
ADSHM-5K	−1	12	300	20	100	12	C	II-14-11
HTC-0500AM	−1	2	850	30	60	0.5	I	II-14-41
HTC-0500SM	−1	2	850	30	60	0.5	E	II-14-41

NOTES
[1]ADSHM-5 units are 2″ × 2″ × 0.4″ modules; ADSHC-85 and HTC-0500 units are 14-pin DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

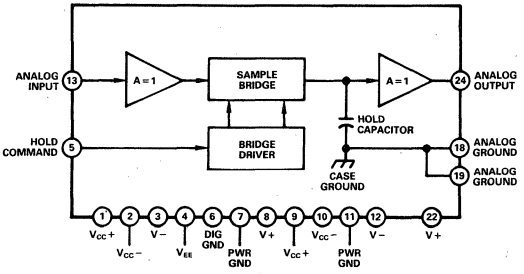
Sample/Track-Hold Amplifiers

Ultra High Speed



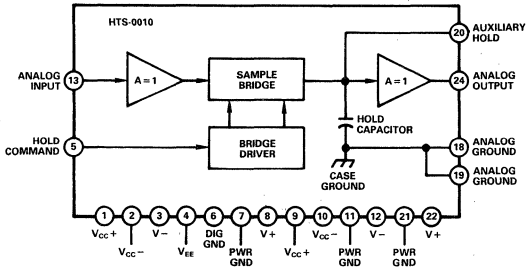
HTC-0300

Aperture Jitter of 100ps
Input Range ±10V
Output Current ±50mA
Max Droop Rate 5μV/μs



HTS-0025

Aperture Jitter of 20ps
Acquisition Time 25ns
Output Current ±50mA
250V/μs Slew Rate



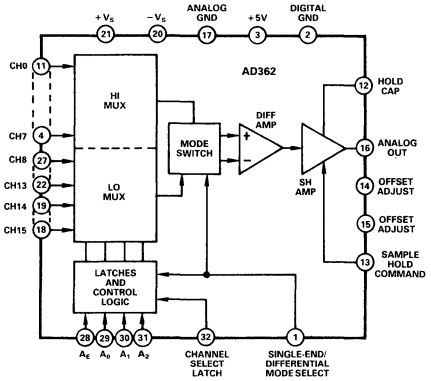
HTS-0010

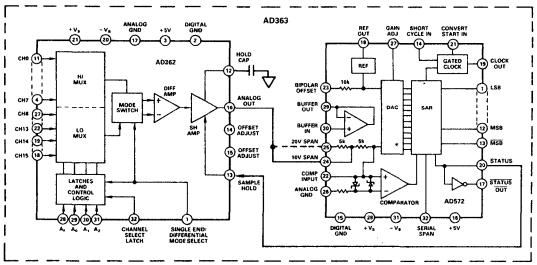
Aperture Jitter of 5ps
Acquisition Time 10ns
Output Current ±40mA
Slew Rate 300V/μs

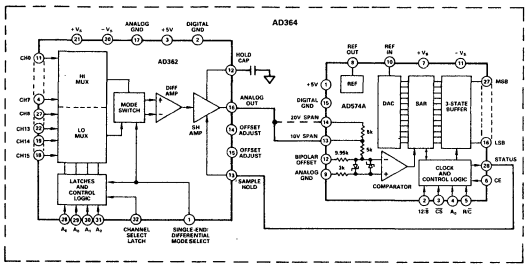
SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Open Loop Gain V/V	Small Signal BW MHz	Acquisition Time – ns (0.1%)	Aperture Time ns	Aperture Jitter ps	Slew Rate V/μs	Temp. Range[2]	Volume* Section Page
HTC-0300	−1	8	170	6	100	250	C	I-14-41
HTC-0300A	−1	8	150	6	100	260	C	I-14-41
HTC-0300M	−1	8	150	6	100	250	I[3]	I-14-41
HTC-0300AM	−1	8	150	6	100	250	E	I-14-41
HTS-0025	+0.95	30	30	5	20	250	C	I-14-55
HTS-0025SM	+0.95	30	30	5	20	250	I[3]	I-14-55
HTS-0010KD	+0.96	60	16	−2	5	300	C	I-14-49
HTS-0010SD	+0.96	60	16	−2	5	300	I[3]	I-14-49

NOTES
[1]Metal DIP – HTC-0300M, HTC-0300AM, HTS-0010 and HTS-0025; Ceramic DIP – HTC-0300 and HTC-0300A.
[2]C = 0 to +70°C, E = −55°C to +125°C.
[3]I = −25°C to +100°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.







AD362

- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Precision: Nonlinearity ≤ ±0.005%
- High Speed: 10μs Acquisition Time to 0.01%
- Complete and Calibrated: No Additional Parts Required
- Small, Reliable: 32-Pin Hermetic Metal DIP
- Versatile: Simple Interface to Popular Analog-to-Digital Converters
- High Differential Input Impedance ($10^{10}\Omega$) and Common-Mode Rejection (80dB)
- Fully Protected Multiplexer Inputs

AD363

- Complete System in Reliable IC Form
- Small Size
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- Versatile Input/Output/Control Format
- Short-Cycle Capability
- True 12-Bit Operation: Nonlinearity ≤ ±0.012%
- Guaranteed No Missing Codes Over Temperature Range
- High Throughput Rate: 30kHz
- Low Power: 1.7W

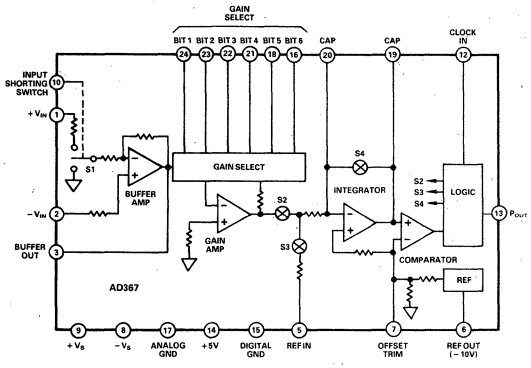
AD364

- Complete Data Acquisition System in 2-Package IC Form
- Full 8- or 16-Bit Microprocessor Bus Interface
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Operation: Nonlinearity ≤ ±0.012%
- Guaranteed No Missing Codes Over Specified Temperature Range
- High Throughput Rate: 20kHz
- Fast Successive Approximation Conversion: 25μs
- Buried Zener Reference for Long-Term Stablility and Low Gain TC
- Small Size: Requires Only 2.8 Square Inches
- Short Cycle Capability
- Low Power: 1.4W

SPECIFICATIONS – Min or Max at T_A = +25°C

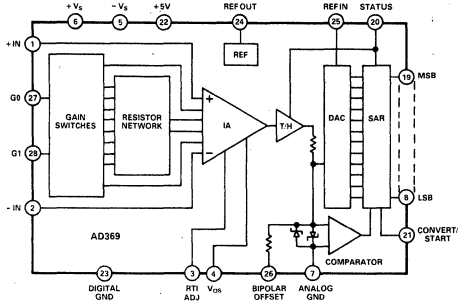
Model[1]	Resolution Bits	Input Range V	Linearity %	Gain Error %	Gain T.C. ppm/°C	Throughput Rate kHz	Temp. Range[2]	Volume* Section Page
AD362KD[3]	–	±10	0.005	0.02	4	56	C	I-15-5
AD362SD[3]	–	±10	0.005	0.02	2	56	E	I-15-5
AD363KD	12	+5, +10, ±2.5, ±5, ±10	0.025	0.05	30	25	C	I-15-13
AD363SD	12	+5, +10, ±2.5, ±5, ±10	0.025	0.05	25	25	E	I-15-13
AD364JD(SD)	12	+10, ±5, ±10	0.024	0.3	54	20	C/E	I-15-25
AD364KD(TD)	12	+10, ±5, ±10	0.012	0.3	31	20	C/E	I-15-25

NOTES
[1]Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, E = −55°C to +125°C.
[3]Analog front end for ADC, including sample-hold, 16-channel MUX, latches and logic.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD367

Differential Input – Programmable Gain Amplifier
6-Bit (1 of 64) Gain Control
Internal –10V Reference
15-Bit Integral Nonlinearity
±305μV Resolution
10ms or Programmable Conversion Time
External Integration Capacitor



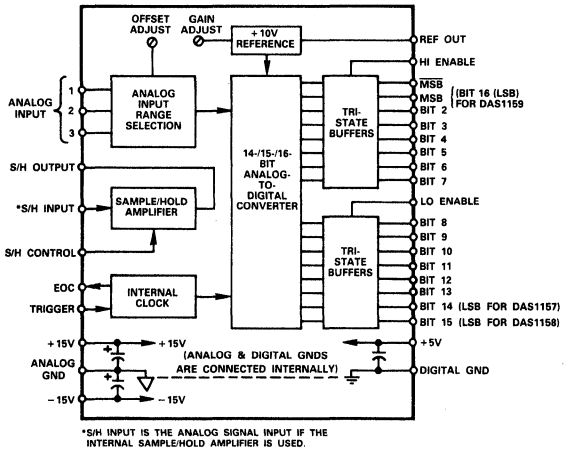
AD369

Includes: Programmable Gain Instrumentation Amplifier, Track and Hold Amplifier 12-Bit A/D Converter
Digitally-Controlled Gain (1, 10, 100, 500)
50kHz Throughput Rate
Small Size: 28-Pin Metal Hermetic Double DIP
Guaranteed No Missing Codes Over Temperature
True 12-Bit Linear: Error ≤1/2LSB (B-Grade)
Unipolar or Bipolar Operation
Low Power: 775mW
Differential Input
Internal Hold Capacitor

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Linearity %	Gain Ranges	Gain Accuracy %	Gain Drift ppm/°C	Temp. Range[2]	Volume* Section Page
AD367KM	0.00305	0.282 to 24 Binarily	2	10	C	S-3-27
AD369AM	0.0183	1,10,100,500	0.5	30	I	S-3-29
AD369BM	0.0122	1,10,100,500	0.2	30	I	S-3-29

NOTES
[1]Suffix "M" – metal DIP.
[2]C = 0 to +70°C, I = –25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



DAS1157, DAS1158, DAS1159

Complete with High Accuracy Sample/Hold and A/D Converter
Low Power Consumption: 650mW max, $V_S = \pm 15V$
Rated Performance: −25°C to +85°C
Low Nonlinearity (DAS1158 and DAS1159)
Differential: ±0.0015% FSR max
Integral: ±0.003% FSR max
Differential T.C.: ±1ppm/°C max
High Throughput Rate: 18kHz min
Byte-Selectable Tri-State Buffered Outputs
Internal Gain & Offset Potentiometers
All Hermetically-Sealed Semiconductors

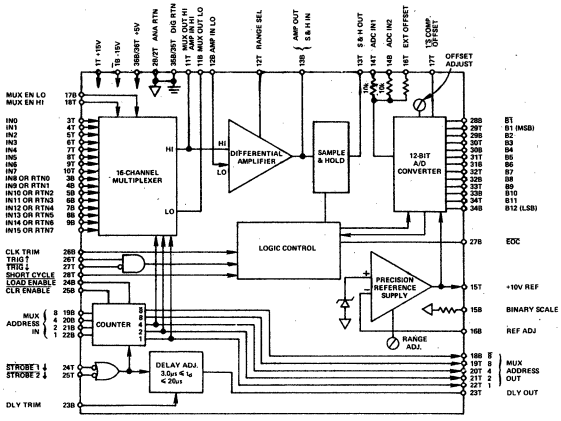
2

SPECIFICATIONS – Min or Max at $T_A = +25°C$

Model	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Throughput kHz	Output Logic	Temp. Range[1]	Volume* Section Page
DAS1157	14	1	1/2	8	16.6	TTL	I	S-4-15
DAS1158	15	1	1/2	8	16.6	TTL	I	S-4-15
DAS1159	16	2	1	8	16.6	TTL	I	S-4-15

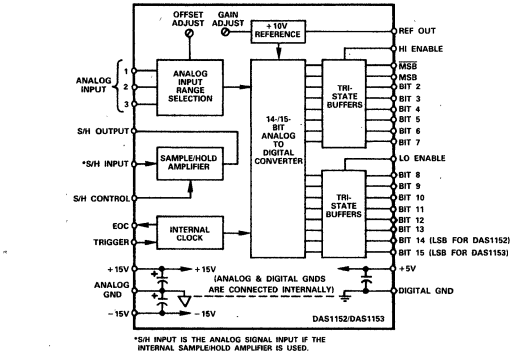
NOTES
[1]I = −25°C to +85°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Data Acquisition Subsystems



DAS1128

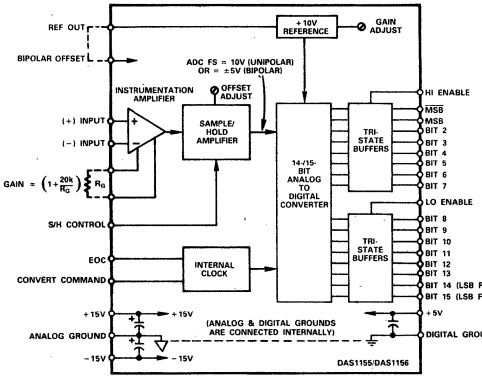
Complete Data Acquisition System
12-Bit Digital Output
16 Single or 8 Differential Analog Inputs
High Throughput Rate
Selectable Analog Input Ranges
Versatile Input/Output/Control Format
Low 3 Watt Power Dissipation
Small 3" × 4.6" × 0.375" Module



*S/H INPUT IS THE ANALOG SIGNAL INPUT IF THE INTERNAL SAMPLE/HOLD AMPLIFIER IS USED.

DAS1152/DAS1153

14-Bit & 15-Bit Sampling A/D Converter
Complete with High Accuracy Sample/Hold and A/D Converter
Differential Nonlinearity: ±0.002% FSR max (DAS1153)
Nonlinearity: DAS1152: ±0.005% FSR max
DAS1153: ±0.003% FSR max
Low Differential Nonlinearity T.C.: ±2ppm/°C max
High Throughput Rate: 25kHz min (DAS1152)
High Feedthrough Rejection: 96dB
Byte-Selectable Tri-State Buffered Outputs
Internal Gain & Offset Potentiometers
Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules



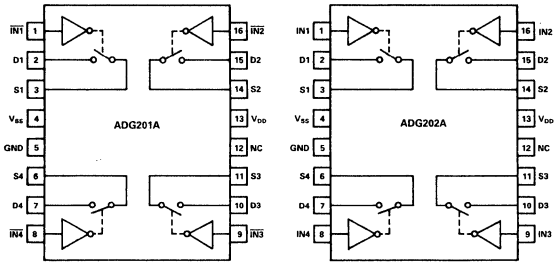
DAS1155/DAS1156

14-Bit & 15-Bit Low Level Data Acquisition System
Functionally Complete:
Includes Instrumentation Amplifier, Sample/Hold Amplifier, and Analog-to-Digital Converter
Differential Nonlinearity: ±0.002% FSR max (DAS1156)
Guaranteed Nonlinearity: ±0.005% FSR (DAS1155)
±0.003% FSR (DAS1156)
High Common-Mode Rejection: 80dB (up to 500Hz)
High Feedthrough Rejection: 96dB
Resistor Programmable Gain: 1V/V to 1000V/V
Byte Selectable Tri-State Buffer Outputs
Internal Gain and Offset Potentiometers

SPECIFICATIONS – Min or Max at T_A = +25°C

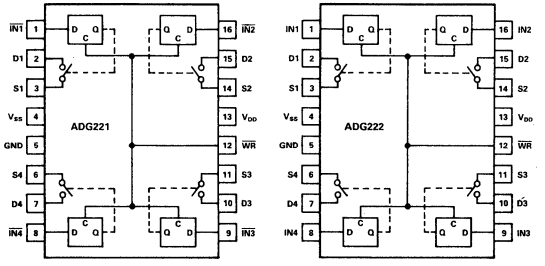
Model	Resolution Bits	Relative Accuracy LSB	Differential Nonlinearity LSB	Gain T.C. ppm/°C	Throughput kHz	Output Logic	Temp. Range[1]	Volume* Section Page
DAS1128	12	1/2 typ	1 typ	20	50	DTL & TTL	C	II-15-5
DAS1152	14	1	1/2	8	25	TTL	C	II-15-13
DAS1155	14	1	1/2	16 typ	25	TTL	C	II-15-17
DAS1153	15	1	1/2	8	20	TTL	C	II-15-13
DAS1156	15	1	1/2	16 typ	20	TTL	C	II-15-17

NOTES
[1]C = 0 to +70°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



ADG201A/ADG202A

44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω typ)
Low Power Dissipation (18mW)
TTL/CMOS Compatible
Superior Second Source:
ADG201A Replaces DG201A, HI-201
ADG202A Replaces DG202



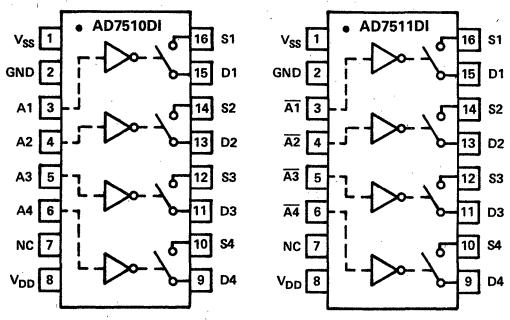
ADG221/ADG222

44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω typ)
Low Power Dissipation (18mW)
µP, TTL, CMOS Compatible
Superior DG221 Replacement

SPECIFICATIONS – Min or Max at T_A = +25°C

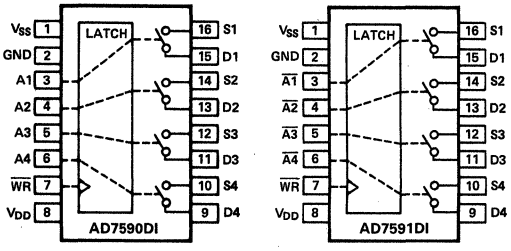
Model[1]	Function	R_{ON} Ω	Off Leakage nA	Logic	Temp. Range[2]	Volume* Section Page
ADG201AKN		90	2	C	TTL &	S-3-327
ADG201ABQ	Quad SPST	90	2	I	CMOS	S-3-327
ADG201ATQ		90	1	E		S-3-327
ADG202AKN	Quad SPST	90	2	C	TTL &	S-3-327
ADG202ABQ		90	2	I	CMOS	S-3-327
ADG202ATQ		90	1	E		S-3-327
ADG221KN(BQ)	Quad SPST	90	2	C/I	TTL &	S-3-333
ADG221TQ		90	1	E	CMOS	S-3-333
ADG222KN(BQ)	Quad SPST	90	2	C/I	TTL &	S-3-333
ADG222TQ		90	1	E	CMOS	S-3-333

NOTES
[1]Suffix "N" – plastic DIP; Suffix "Q" – cerdip.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[3]Dielectrically isolated features latchup-free overvoltage proof operation.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD7510DI/AD7511DI

Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Monolithic Dielectrically-Isolated CMOS



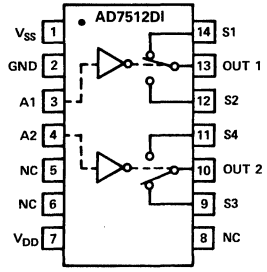
AD7590DI/AD7591DI

Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Buffered Switch Logic
TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series

SPECIFICATIONS – Min or Max at T_A = +25°C

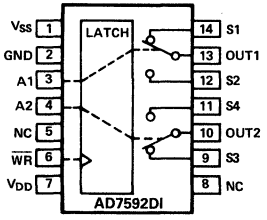
Model[1]	Function	R_{ON} Ω	Off Leakage nA	Logic	Temp. Range[2]	Volume* Section Price
AD7510DIJN(JD)	Quad SPST		5	CMOS	C/I	I-16-13
AD7510DIKN(KD)	Note 3	100	5	TTL/CMOS	C/I	I-16-13
AD7510DISD			3	TTL/CMOS	E	I-16-13
AD7511DIJN(JD)	Quad SPST		5	CMOS	C/I	I-16-13
AD7511DIKN(KD)	Note 3	100	5	TTL/CMOS	C/I	I-16-13
AD7511DISD			3	CMOS	E	I-16-13
AD7511DITD			3	TTL/CMOS	E	I-16-13
AD7590DIKN	Quad SPST	90	5	TTL/CMOS	C	I-16-21
AD7590DIBD	with Data	90	5	TTL/CMOS	I	I-16-21
AD7591DIKN	Latches	90	5	TTL/CMOS	C	I-16-21
AD7591DIBD		90	5	TTL/CMOS	I	I-16-21

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[3]Dielectrically isolated features latchup-free overvoltage proof operation.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.



AD7512DI

Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Monolithic Dielectrically-Isolated CMOS



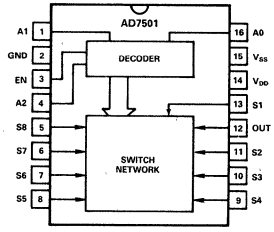
AD7592DI

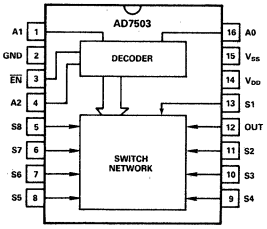
Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Buffered Switch Logic
µP, TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Function	R_{ON} Ω	Off Leakage nA	Output Leakage nA	Logic	Temp. Range[2]	Volume* Section Page
AD7512DIJN(JD)	Dual SPDT		5	15	CMOS	C/I	I-16-13
AD7512DIKN(KD)	Note 3	100	5	15	TTL & CMOS	C/I	I-16-13
AD7512DISD			3	9	CMOS	E	I-16-13
AD7512DITD			3	9	TTL & CMOS	E	I-16-13
AD7592DIKN	Dual SPDT	90	5	10	TTL & CMOS	C	I-16-21
AD7592DIBD	with Data Note 3	90	5	10	TTL & CMOS	I	I-16-21

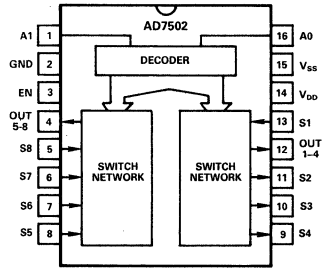
NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
[3]Dielectrically isolated features latchup-free overvoltage proof operation.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.





AD7501/AD7503

DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Output Enable
AD7503 Replaces HI-1818



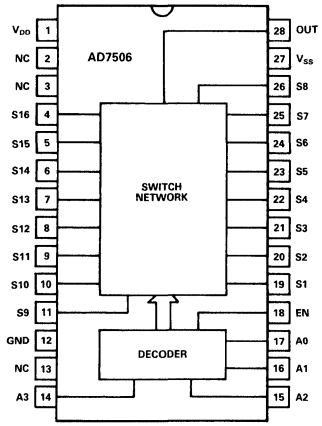
AD7502

DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Output "Enable" Control

SPECIFICATIONS – Min or Max at T_A = +25°C

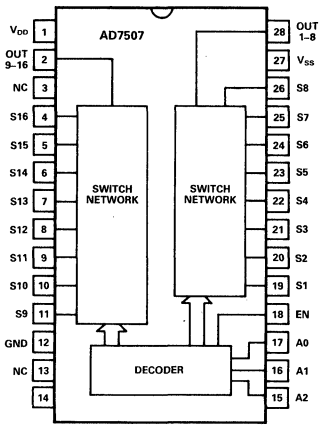
Model[1]	Function	R_{ON} Ω	Off Leakage nA	Logic	Temp. Range[2]	Volume* Section Page
AD7501JN(JD)			10	CMOS	C/I	I-16-5
AD7501KN(KD)	8-Channel	300	10	TTL & CMOS	C/I	I-16-5
AD7501SD			5	TTL & CMOS	E	I-16-5
AD7502JN(JD)	Dual		5	CMOS	C/I	I-16-5
AD7502KN(KD)	4-Channel	300	5	TTL & CMOS	C/I	I-16-5
AD7502SD	(differential)		3	TTL & CMOS	E	I-16-5
AD7503JN(JD)			10	CMOS	C/I	I-16-5
AD7503KN(KD)	8-Channel	300	10	TTL & CMOS	C/I	I-16-5
AD7503SD			5	TTL & CMOS	E	I-16-5

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.



AD7506

R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506



AD7507

R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG507

SPECIFICATIONS – Min or Max at T_A = +25°C

Model[1]	Function	R_{ON} Ω	Off Leakage nA	Logic	Temp. Range[2]	Volume* Section Page
AD7506JN(JD)		450	20	CMOS	C/I	I-16-9
AD7506KN(KD)	16-Channel	450	20	TTL/CMOS	C/I	I-16-9
AD7506SD		400	10	CMOS	E	I-16-9
AD7506TD		400	10	TTL/CMOS	E	I-16-9
AD7507JN(JD)	Dual	450	10	CMOS	C/I	I-16-9
AD7507KN(KD)	8-Channel	450	10	TTL/CMOS	C/I	I-16-9
AD7507SD	(differential)	400	5	CMOS	E	I-16-9
AD7507TD		400	5	TTL/CMOS	E	I-16-9

NOTES
[1]Suffix "N" – plastic DIP; Suffix "D" – ceramic DIP.
[2]C = 0 to +70°C, I = −25°C to +85°C, E = −55°C to +125°C.
*I = Volume 1 – Integrated Circuits; II = Volume 2 – Modules & Subsystems; S = This Volume.

Digital Panel Instruments

		LOGIC (+5V) POWERED DIGITAL PANEL METERS						
		AD2026-1	AD2006D	AD2010	AD2021	AD2004	AD2027	AD2028
Digits; F.S. Range	3; -99 to +999mV	•						
	3½; ±199.9mV			•	•			
	±1.999V		•		•			
	±19.99V				•			
	4½; ±1.9999V					•	•	
	±19.999V						•	
	4¾; ±3.9999V							•
	±39.999V							•
Input Type	Ltd. Differential	•		•	•		•	•
	Differential		•					
	Floating					•		
Data Outputs	Character Serial				•		•	•
	Parallel BCD		•					
	Parallel BCD Latched			•		•	•	•
Display Type	LED	•		•	•	•	•	•
	Gas Discharge		•					
Display Size in/mm		0.5/13	0.55/14	0.27/7	0.5/13	0.27/7	0.43/11	0.43/11
Max Case Depth[1] in/mm		0.65/17	4.8/122	1.4/36	1.9/48	3.3/84	4.8/122	4.8/122
*Volume, Section, Page		II-16-33	II-16-11	II-16-15	II-16-23	II-16-9	II-16-25	II-16-29

NOTES

[1] Case depth includes mating connector. All logic powered DPMs use industry standard case with 3.175" X 1.810" (80.65 X 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" X 1.682" (99.82 X 42.72mm) cutout. AD2006 uses same case as logic powered DPMs.

*I=Volume 1—Integrated Circuits; II=Volume 2—Modules & Subsystems; S=This Volume.

		AC-POWERED DIGITAL PANEL METERS					
		AD2026-2	AD2006	AD2016	AD2024	AD2025	AD2037
6-Channel Scanning							●
Digits; F.S. Range	3; -99 to +999mV	●					
	3½; ±199.9mV ±1.999V ±19.99V 199.9V 600V		●	● ● ●			● ●
	4½; ±1.9999V ±19.999V				● ●		
	4¾; ±3.9999V ±39.999V					● ●	
Input Type	Single Ended Ltd. Differential Differential		●	●	●	●	●
	Floating True RMS	●					●
Data Outputs	Character Serial Parallel BCD Parallel BCD Latched		●	● ●	● ●	● ●	●
Display Type	LED Gas Discharge	●	●	●	●	●	●
Display Size in/mm		0.5/13	0.55/14	0.5/13	0.43/11	0.43/11	0.5/13
Max Case Depth[2] in/mm		2.44/63	4.95/126	4.77/121	5.3/135	5.3/135	6.03/153
*Volume, Section, Page		II-16-33	II-16-11	II-16-19	II-16-25	II-16-29	II-16-37

NOTES

[1] Full scale inputs when reading out in dB are 500mV, 5V, 50V, 500V and 625V rms.

[2] Case depth includes mating connector. All logic powered DPMs use industry standard case with 3.175" X 1.810" (80.65 X 45.97mm) cutout. All ac-powered DPMs except AD2006 use industry standard case with 3.930" X 1.682" (99.82 X 42.72mm) cutout. AD2006 uses same case as logic powered DPMs.

*I=Volume 1—Integrated Circuits; II=Volume 2—Modules & Subsystems; S=This Volume.

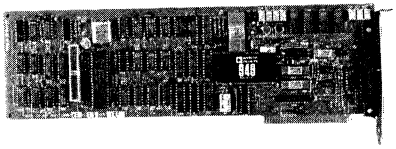
Digital Panel Instruments

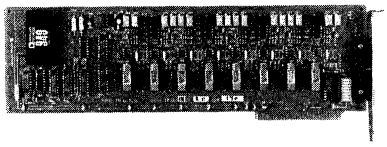
			DIGITAL TEMPERATURE/ TRANSDUCER METERS									
			AD2036	AD2037	AD2038	AD2040	AD2050	AD2051	AD2060	AD2061	AD2070	AD2071
Input	Number of Channels	1	•	•	•	•	•	•	•	•	•	•
		6										
Sensor (Determines Temperature Range)	Thermocouple Type	Switch Selected						•		•		•
		User Specified	•				•		•		•	
		J, K, T	•				•	•			•	•
		E, R, S					•	•			•	•
		C, B, J DIN, T DIN									•	•
	AD590, AD592 (−55°C to +150°C)				•	•						
	RTD			•					•	•		
	Thermistor			•					•	•		
Features	Self-Calibration						•	•	•	•	•	•
	Cold-Junction Compensation		•				•	•			•	•
	Linearization		•				•	•	•	•	•	•
	Isolation		•	•	•		•[1]	•[1]	•[1]	•[1]	•	•
Readout	Digits	3+, 2−				•						
		3½	•	•	•		•	•	•	•		
		4½									•	•
	LED Display Height	0.5", 13mm	•	•	•	•						
		0.56", 14.3mm					•	•	•	•	•	•
Digital Data Output	Isolated Parallel BCD, Latched		•	•	•							
	7-Bit Character-Serial ASCII						•	•	•	•	•	•
	Isolated, 20mA current loop						•	•			•	•
	RS232/TTL										•	•
Analog Output	Voltage		•	•	•		•	•	•	•	•	•
Power Supply	AC Line		•	•	•	•	•	•	•	•	•	•
	DC +7.5V to +28V						•	•	•	•	•	•
	+5V		•			•						
	+12V		•									
*Volume, Section, Page			II-16-35	II-16-37	II-16-37	II-16-39	II-16-43	II-16-43	II-16-45	II-16-45	S-4-5	S-4-5

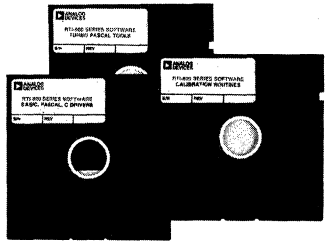
NOTES
[1] AC line-operated versions.
*I=Volume 1—Integrated Circuits; II=Volume 2—Modules & Subsystems; S=This Volume.

µC Compatible Analog and Digital I/O Subsystems

IBM/PC/XT/AT Compatible I/O Boards







The RTI-800 Series products are a group of analog and digital input/output boards compatible with the IBM PC/XT/AT* (or equivalent) computers. They are cost-effective and easy-to-use solutions to your real-time measurement or data acquisition and control applications and include optional signal conditioning and MS-DOS software. This allows you to get up and running fast when you interface your PC to the real (i.e., analog and digital) world.

RTI-800 HIGH PERFORMANCE ANALOG INPUT BOARD

- 16 Input Channels (expandable to 32)
- Software Programmable Gain Amplifier
- 12-Bit A/D Converter
- 8, 12 and 25µs A/D Conversion Times
- 16 Digital I/O Channels
- 3 Frequency/Timer Channels
- Supports DMA and Interrupt Capability

RTI-815 HIGH PERFORMANCE MULTIFUNCTION BOARD

- 16 Analog Input Channels (expandable to 32)
- Software Programmable Gain Amplifier
- 12-Bit A/D Converter
- 8, 12 and 25µs A/D Conversion Times
- 2 Analog Output Channels
- 12-Bit D/A Converter
- 16 Digital I/O Channels
- 3 Frequency/Timer Channels
- Supports DMA and Interrupt Capability

RTI-802 HIGH PERFORMANCE ANALOG OUTPUT BOARD

- 4 or 8 Analog Output Channels
- 12-Bit D/A Resolution
- Outputs Protected Against Shorts

RTI-817 LOW COST DIGITAL I/O BOARD

- 24 Channels of Digital Input/Output
- Input Latches and Selectable Strobe
- Interrupt on Change of State
- Compatible to Solid State Relay Subsystem

3B SERIES ANALOG SIGNAL CONDITIONING I/O SUBSYSTEM

- Complete Modular Analog I/O Signal Conditioning
- Direct Sensor Interface:
  Thermocouples, RTD's, Strain Gages, LVDT's
- Provides Isolation and Input Protection
- Cable Connection to RTI-800 Series Boards

MS-DOS DRIVER SOFTWARE

- Drivers for BASIC, Pascal, FORTRAN and Lattice C
- Turbo Pascal Software Tools
- Calibration Routines

Convenient and powerful software interface routines running under MS-DOS that support the RTI-800 Series products. These callable machine language routines provide analog and digital I/O, frequency and event counting, and pulse output functions.

APPLICATION SOFTWARE

Completely menu driven data acquisition and control software which provides an easy way to collect and analyze in real time, analog data along with implementing PID or setpoint control.

***IBM PC/XT/AT is a trademark of International Business Machines, Inc.**

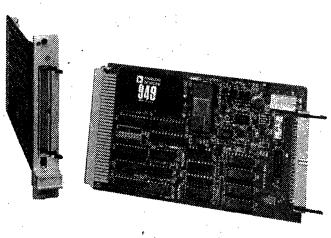
IBM/PC/XT/AT COMPATIBLE ANALOG AND DIGITAL I/O BOARDS

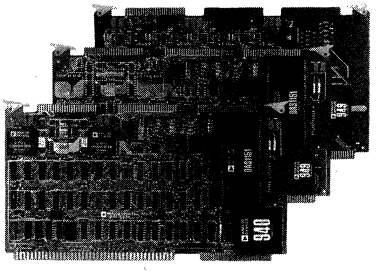
Model	Analog Input	Analog Output	Digital I/O	Counter/ Timer	High Speed Option	Channel Expansion Option
RTI-800	X		X	X	X	X
RTI-802		X				
RTI-815	X	X	X	X	X	X
RTI-817			X			

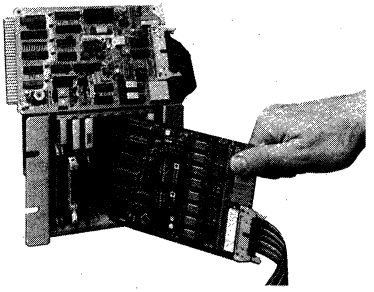
RTI-800 Series Function Chart

μC Compatible Analog and Digital I/O Subsystems

VME, MULTIBUS and STD Bus Compatible I/O Boards







SELECTION GUIDE

The Selection Guide provides selection information in capsule form, permitting board types to be matched to desired features. Additional information and complete specifications are provided on the individual boards or family data sheets.

		MICROCOMPUTER BUS COMPATIBILITY													
		VMEbus		MULTIBUS*			STD BUS (NMOS)					STD BUS (CMOS)			
	Analog Devices Part Number	RTI-600	RTI-602	RTI-711	RTI-724	RTI-732	RTI-1226	RTI-1225	RTI-1260	RTI-1262	RTI-1270	RTI-1280	RTI-1281	RTI-1282	RTI-1287
Board Type	Input	•		•		•	•	•	•		•	•	•		•
	Input/Output														
	Output		•		•			•		•				•	
Channel Capacity	Input	32/16		32/16		32/16	16/8	16/8	32/16		16/16	16/8	16/8		24
	(Single Ended/ Differential)					2		2		4			2	4 or 8	Digital I/O
	Output		4		4										
Input Resolution	10 Bits	•		•		•	•	•	•		•	•	•		
	12 Bits														
Output Resolution	8 Bits							•							
	12 Bits		•		•	•				•			•	•	
Additional Features															
Programmable Gain Amplification		•		•		•			•			•	•		
Single + 5V Operation		•	•	•	•	•	•	•	•	•	•	•	•	•	•
4-20mA Output			•			•				•				•	
Direct Sensor Interface Thermocouples, RTDs											•				
**Volume, Section, Page		II-17-5	II-17-5	II-17-7	II-17-7	II-17-7	II-17-9	II-17-9	II-17-17	II-17-17	II-17-19	S-4-45	S-4-45	S-4-45	S-4-45

NOTES

[1]RTI-1200, RTI-1230, RTI-1240, RTI-1250 series products not listed, but still available.

[2]This product includes sensor signal conditioning and on-board intelligence to perform scaling, linearization, and conversion to engineering units.

*MULTIBUS is a trademark of Intel Corporation.

** = Volume 1 - Integrated Circuits; II = Volume 2 - Modules & Subsystems; S = This Volume.

µMAC-4000 Measurement & Control Subsystems

FEATURES
Analog Inputs
Thermocouples, RTDs, Strain Gages, AD590s
High and Low Level Voltages, Current Loops
± 1000V Isolated and Nonisolated
Analog Outputs
Voltage and Current
± 1000V Isolated and Nonisolated
Digital Inputs/Outputs
Contact Closures
ac and dc Signals (High and Low Level)
Microcomputer Based
Linearization, Unit Conversion, Limit Checking
Powerful Command Set
Serial Communications
20mA or RS-232C
Integral Power Supply
ac or +24V dc

GENERAL DESCRIPTION

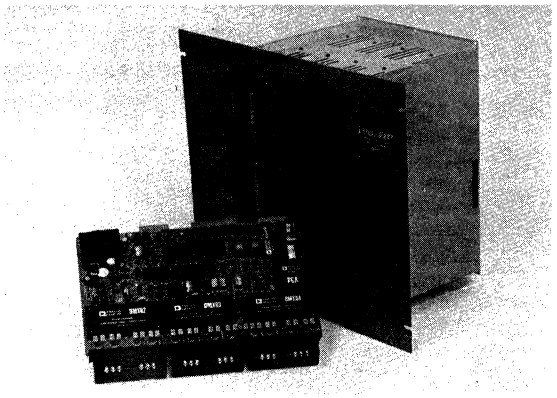
The µMAC-4000 Measurement and Control System is a complete, low cost solution designed to simplify process to computer interface in a wide range of industrial automation applications.

The µMAC-4000 offers an unprecedented set of hardware and software capabilities that can be easily tailored to virtually any automation application. Modular design permits expansion within the system and the flexibility to accept a variety of analog and digital input and output functions.

The µMAC-4000 is optimized for high performance measurement and control. Analog inputs handling capability offers reliable operation in harsh, electrically noisy, industrial environments. The high performance is assured by high quality signal conditioning featuring input protection, ± 1000V channel-to-channel and input-to-output isolation, high common mode rejection, filtering, low drift amplification and 13-bit A/D conversion. A unique plug-in module approach allows the selection of standard signal conditioning modules for direct connection to a wide range of sensors. The µMAC-4000 scales, linearizes and converts the input data to engineering units.

Both analog and digital control capability is provided by the µMAC-4000 system. Analog outputs feature 12-bit resolution, voltage and 4-20mA/0-20mA current outputs with ± 1000V isolation, as well as increment/decrement and bumpless transfer for precise control in either manual or computer mode. Digital I/O offers direct interface to contact closures, TTL levels or high level ac and dc voltages.

The µMAC-4000 system is designed to operate with any host computer which has a 20mA or RS-232C serial port. The µMAC-4000 can be either used as a local front end or located up to 10,000 feet from the host. A powerful command set is included in the µMAC's firmware which allows control via the serial interface bus. Once the command is executed, the results are transmitted back to the host in an ASCII format–at speeds up to 9600 baud.



The µMAC-4000 system requires either ac line power or +24V dc. Circuitry is provided to detect intermittent ac power losses and switch automatically to an external battery backup mode.

A wide variety of packaging options are available to match user requirements. These options include single board enclosures, card cage/rack mounting or NEMA enclosures.

APPLICATIONS

The µMAC-4000 is a versatile, self-contained measurement and control system designed for a broad range of industrial and laboratory applications. It is extremely useful in both control room and remote locations where monitoring and control of temperature, pressure, flow, analog and digital signals are required.

DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct sensor interface via screw terminal connectors, output in engineering units, powerful command set, make the µMAC-4000 extremely easy to use.

Integral Signal Conditioning: High quality signal conditioning provides input protection and isolation, cold junction compensation for thermocouples, RTD excitation, and sensor linearization and scaling, eliminating the need for expensive external signal conditioning.

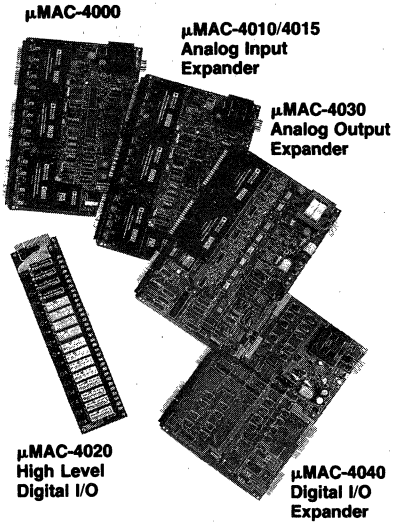
High Noise Rejection: The µMAC-4000 preserves high system accuracy in electrically noisy environments, providing excellent common mode and normal mode noise rejections and RFI/EMI immunity.

Control Capability: Analog and digital outputs are provided to control motor speeds, dictate valve positions and drive actuators.

Features such as isolation, bumpless transfer and DAC readback are included in the design.

Expandability: Expansion capability to 384 analog input channels, 256 analog output channels, 1088 digital inputs and 1088 digital outputs on one 20mA serial line using the µMAC-4000 with expander boards.

µMAC-4000 Measurement & Control Subsystems

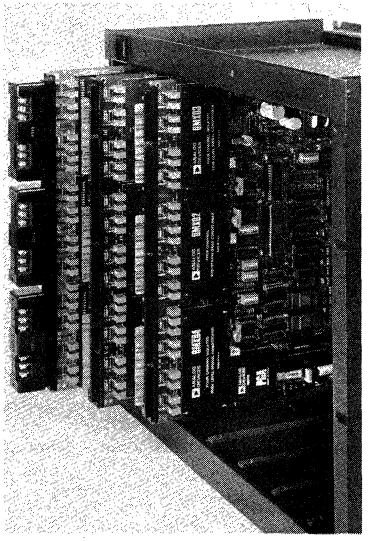


µMAC-4000 System Configuration

The µMAC-4000 system consists of a family of boards providing the measurement and control functions through interfaces to analog and digital inputs and outputs and the host computer.

The system includes: the µMAC-4000 Master Board, the µMAC-4010 Analog Input Expander, the µMAC-4030 Analog Output Expander, the µMAC-4040 Digital I/O Expander, and the µMAC-4020 High Level Digital I/O Subsystem. You select only the functions which are required.

A typical configuration can consist of a single µMAC-4000 Master Board which accepts 4, 8 or 12 analog inputs and includes 8 digital inputs and 8 digital outputs. A multiple board configuration (cluster) consists of one µMAC-4000 Master Board and up to six Expander Boards selected in any combination from up to three µMAC-4010's and/or µMAC-4015's, up to four µMAC-4030's and up to four µMAC-4040's. A µMAC-4000 Master Board must reside in each cluster since it contains the communications and intelligence.



µMAC-4000 System Specifications

INPUT/OUTPUT

Analog Inputs
Thermocouples: J, K, T, S
RTDs: 100Ω Platinum
Solid State Temperature Sensors: AD590 or AC2626
Strain Gage Transducers: ±30mV and ±100mV spans
dc Voltage: ±25mV, ±50mV, ±100mV, ±1V, ±5V, ±10V
dc Current: 4 to 20mA, 0 to ±1mA, 0 to ±20mA
Common Mode Voltage: ±1000V pk (chan/chan/gnd)–isolated input modules
Input Protection: 130V rms continuous IEEE-472 (SWC) transient
A/D Converter: 13-Bit Dual Slope
Scan Rate: 15 or 30 chan/sec

Analog Outputs
Voltage: ±5V, ±10V 0 to ±15V, 0 to ±10V
Current: 4 to 20mA, 0 to 20mA
Resolution: 12-Bits
Isolation: ±1000V pk (chan/chan/gnd)–current outputs
Output Protection: 130V rms

Digital Inputs
Compatibility: TTL signals or contact closures and µMAC-4020 for high level inputs
Isolation: ±300V pk

Digital Outputs
Compatibility: TTL signal and µMAC-4020 for high level outputs

Channel Capacity per Board
µMAC-4000 and µMAC-4010
12 Analog Inputs
8 Digital Inputs
8 Digital Outputs
µMAC-4015
12 Analog Inputs
µMAC-4030
8 Analog Outputs
µMAC-4040
32 Digital Inputs
32 Digital Outputs
µMAC-4020
16 High Level Digital Inputs and Outputs

Capacity per Cluster
48 Analog Inputs
32 Analog Outputs
152 Digital Inputs
152 Digital Outputs

Total System Capacity
8 addressable clusters on one serial communication port

COMMUNICATIONS
Mode: 4 wire full duplex 20mA current loop or RS-232C
Format: Serial Asynchronous ASCII
Rate: Selectable from 110 to 9600 baud
Distance: RS-232C: 50 ft (15m)
20mA, 10,000 ft (3048m)
Protocol: Command/Reply (prompted)

POWER
100/115/220/240V ac, 50/60Hz or +24V dc

MECHANICAL
Single Board: 9.5″ × 13″ (241.3 × 330.2mm)
4-Slot Card Cage: 14.8″ × 11.2″ × 10.3″ (376.0 × 284.5 × 261.6mm)
7-Slot Card Cage: (15.75″ × 19″ × 11″ (400.0 × 482.6 × 279.4mm)

ENVIRONMENTAL
Operating Temperature: 0 to +60°C
Humidity: meets MIL-STD 202, Method 103
Vibration: meets MIL-STD 167-1
Magnetic Field Immunity: 200 gauss
RFI Immunity: 5W @27MHz @3 ft.

μMAC-5000 Measurement & Control System

FEATURES/BENEFITS

Low Cost, Completely Integrated Measurement and Control System On a Single Board

- **Wide Selection of Functionally Complete Analog and Digital I/O**
- **Operates from ac or dc Power**

Integral Signal Conditioning Allows Direct Connection to a Wide Variety of Signal Sources

- **Sensors: Thermocouples, RTDs, Strain Gages, Load Cells, AD590/AC2626**
- **Millivolt and Voltage Sources**
- **4-20mA/0-20mA Process Current Inputs**
- **Counter or Pulse Inputs Provide for Frequency or Event Counting**

Powerful Measurement and Control μMACBASIC™ Language

- **Programs Developed and Run On Board**
- **Analog and Digital I/O Are Performed By Key Words In BASIC**
- **Program Storage in PROM or Battery Backed-Up RAM**

Advanced μMACBASIC Features

- **Functions and Procedures Allow User Defined Key Words**
- **Advanced Block Structures Allow Modular, Self-Documenting Programs**

Powerful Communications Capabilities

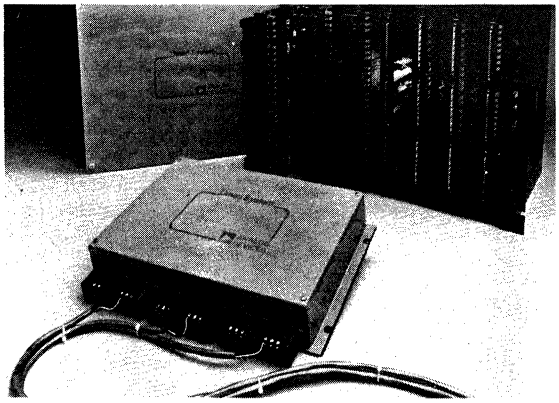
- **Supports Communications in RS-232C, 20mA, RS-422 and RS-423**
- **Supports Asynchronous Communications**
- **Protocol Emulation Easily Accomplished with μMACBASIC**

GENERAL DESCRIPTION

The μMAC-5000 Measurement and Control System is a complete, low cost solution designed to solve a broad range of industrial measurement and control problems. It can be used in applications requiring distributed intelligence or as a local front end.

The μMAC-5000 offers an unprecedented set of hardware and software capabilities that can be easily tailored to virtually any measurement and control application. Modular design permits expansion within the system and the flexibility to accept a variety of analog and digital input and output functions. A powerful Measurement and Control BASIC language, μMACBASIC, is provided with each product.

The μMAC-5000 is optimized for high performance measurement and control. Analog input handling capability offers reliable operation in harsh, electrically noisy, industrial environments. The high performance is assured by high quality signal conditioning featuring input protection, ± 1000V channel-to-channel and input-to-output isolation, high common mode noise rejection, filtering, low drift amplification and 14-bit A/D conversion (13 bits + sign). A unique plug-in module approach allows the selection of standard signal conditioning



modules for direct connection to a wide range of sensors. The μMAC-5000 scales, linearizes and converts the input data to engineering units.

Both analog and digital control capability are provided by the μMAC-5000 system. Analog outputs, provided by the μMAC-4030 Analog Output Expander, feature 12-bit resolution, voltage and 4-20mA/0-20mA current outputs with ± 1000V isolation, as well as the capability of either auto or manual operation with bumpless transfer and programmable slew rate.

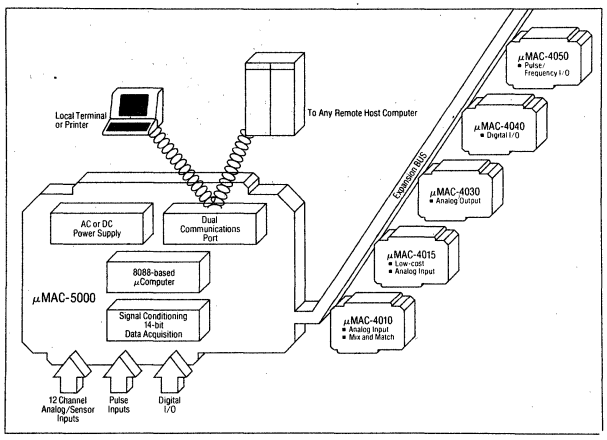
Analog outputs are also available directly on the μMAC-5000, using the QMXAO output module, for a single board input and output solution. Digital I/O offers direct interface to contact closures, TTL levels or high level ac and dc voltages. Two pulse accumulator or frequency inputs are available on the μMAC-5000 and both have a 32-bit counter and operate over a 0 to 20kHz frequency range.

The μMAC-5000 board is designed to operate efficiently in stand-alone applications. The μMAC-5000, which has two serial ports, can be used with any host computer. The local port can communicate in RS-232C, RS-422, or RS-423 and can be used for program development or for supporting a local printer or terminal. The remote port supports RS-232C, 20mA, RS-422, and RS-423. In supervisory control applications, the μMAC-5000 can be used either as a local front end or located up to 10,000 feet from a host and can operate at speeds up to 19.2K baud in asynchronous mode.

The μMACBASIC language was designed to address the needs of both the experienced and inexperienced programmers. The language provides the less experienced programmer with a powerful version of the popular BASIC programming language which allows programmers with only a fundamental knowledge of BASIC to easily write programs. μMACBASIC also provides the experienced programmer with a truly modular, structured language which simplifies the task of writing larger, more complex programs and provides higher quality programs.

μMACBASIC is a trademark of Analog Devices, Inc.

µMAC-5000 Measurement & Control System



SYSTEM CONFIGURATION

A single board system configuration consists of one µMAC-5000 Programmable Master Board which accepts 4, 8, or 12 analog inputs and includes 8 digital inputs and 8 digital outputs. Two of the digital inputs can optionally be used as pulse accumulators or frequency inputs.

A multiple board configuration (cluster) consists of one µMAC-5000 programmable Master Board and up to six Expander Boards. The µMAC-4000 Series of expander products provides a wide range of analog and digital I/O capability and a cost effective solution to large point applications (see Table I). A µMAC-5000 must reside in each cluster since it contains the communications capability and intelligence. A network using up to 16 clusters in a multidrop configuration allows your host computer to monitor and control up to 1344 analog or 4864 digital points or varying combinations of both types from a single 20mA or RS-422 communications line.

COMMUNICATIONS

The µMAC-5000 System is designed to operate in stand-alone applications and can communicate with any host computer or terminal that has a 20mA, RS-232C, RS-422, or RS-423 port. The µMAC-5000 has two serial communication ports. Both ports have 256 byte RAM-buffers. A full duplex USART is used to receive and transmit data at selectable baud rates. The µMAC-5000's serial link allows use of either a party line (Figure 1) or radial system configuration.

The local communications port is primarily used for program development and will support RS-232C, RS-422, and RS-423. It can also be used to support a printer or terminal in a run time environment. This port is capable of communicating from 150 to 19.2K baud in an asynchronous mode. The local port can be used in either a full duplex or half duplex mode and can be used in a party line configuration when RS-422 is used.

The remote communication port supports RS-232C, 20mA, RS-422 and RS-423. In the asynchronous mode, it can operate from 110 to 19.2K baud. This port can be used in either a full duplex or half duplex mode and can be used in either a party line or radial configuration. The remote port has control lines (RTS, DCD, DTR, and CTS) which allow connection to a modem for long distance communications. The 20mA loop is optically coupled for harsh industrial environments.

Model	Function	Description
µMAC-4010	–Analog input –Digital I/O	–Up to 12 channels using QMX modules –16 channels digital I/O
µMAC-4015	–Isolated analog input	–Low cost, 12 channels of same input type –1500V isolation
µMAC-4030	–8 channels analog output	–Voltage or isolated 4-20mA outputs –Readback, bumpless transfer
µMAC-4040	–Digital I/O	–32 channels isolated digital inputs –32 channels digital outputs (TTL)
µMAC-4050	–Multi-function digital I/O –8 channels, mixed function	–Pulse accumulator input –Frequency input –Pulse output –Time proportional output
µMAC-4020	–Interface subsystem to high level ac and dc voltages and currents	–Solid state relay subsystem 16 channels, mix of input and output functions

Table I. µMAC Series Expander Boards (See Data Sheet)

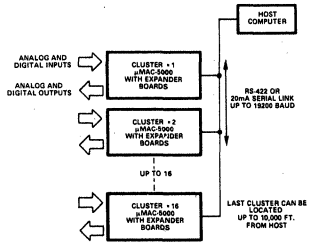


Figure 1. Party Line Connection (Multidrop)

SPECIFICATIONS

μMAC-5000 Board Features

Analog Inputs
12 channels, mix and match
Thermocouples: J,K,T,S,R,E,B,W (linearized)
RTD: 100Ω Platinum (linearized)
Strain Gage: 30mV and 100mV spans
DC Voltage: 25mV to 10V
Process Currents: 0-1mA, 4-20mA, 0-20mA
Inputs Selectable by 4-channel QMX module—3 per board
QMX03, 04 modules isolated to 1000V channel-to-channel, input-to-output with IEEE–472 (SWC) transient protection
A/D Converter: 14-bit integrating

Analog Outputs
Up to 6 outputs using the new QMXAO module
QMX input and output modules can be mixed
Each QMXAO provides 2 isolated channels of current or voltage output (1000 volts isolation)
12-bit D/A output resolution
Can be used for programmable excitation

Digital I/O
8 channels isolated digital or contact closure inputs
8 channels digital outputs
Connector-compatible with μMAC-4020 high-level solid-state relay subsystem

Pulse Inputs (optional use of two digital inputs)
2 channels of frequency or pulse accumulator inputs
32 bits pulse accumulation: 20kHz max frequency

Two Communication Ports.
Full/half duplex, X_{ON}–X_{OFF}
256 byte RAM buffered; asynchronous
Selectable baud rate: 110 to 19,200 baud
Distance: 20mA-10,000 ft. (3048m)
RS-232—50 ft. (15m)
RS-422—10,000 ft. (3045m)
RS-423—1,000 ft. (305m)

8088-Based Microcomputer
32K RAM – expandable to 128K
80K PROM
16K user EPROM – expandable to 32K

Power
On-board ac power supply: 100V/115V/220V/240V or +24V dc (used as primary power or back-up to ac line)

Environmental
Operating Temperature: 0 to +60°C
Humidity: meets MIL-STD 202, method 103
Vibration: meeds MIL-STD 167-1
Magnetic Field Immunity: 200 gauss
RFI Immunity: 5W @ 27MHz @ 3 feet

Mechanical
μMAC-5000 Board: 9.5″×13″(241.3×330.2mm)
μMAC-5000 Board Enclosure:
9.2″×14.3″×3″(234.2×363.2×76.2mm)
2-Board Enclosure: 10″×15″×6″(254.0×381.0×152.4mm)
4-Board Card Cage:
14.8″×11.2″×10.3″(376.0×284.5×261.6mm)
7-Board Card Cage: 15.75″×19″×11″(400.0×482.6×279.4mm)

μMAC-5000 APPLICATIONS

Industrial Process Control and Monitoring: Temperature, pressure, flow and digital I/O measurements, and PID loop control are readily performed on the μMAC-5000 in stand-alone applications. μMACBASIC allows for the creation of proprietary algorithms that can be hidden from the end user.

Machine/Boiler/Furnace Control: High immunity to electrical noise, 1000V isolation, 60°C operation, and single board packaging provide highly reliable operation in harsh industrial environments. The μMAC-5000 is an ideal replacement for programmable controllers where analog I/O is required in addition to digital I/O.

Remote Terminal Units for data acquisition and control in pipe line, utilities and oil field applications. μMAC-5000 can readily emulate existing protocols with μMACBASIC and is readily integrated into applications requiring distributed intelligence. μMAC-5000 can also be used with modems in remote applications.

Energy Management: The μMAC-5000 is a low cost solution for applications requiring a high degree of I/O flexibility in distributed monitoring and control applications – making it a natural for energy management applications.

Industrial, Government or University R&D: μMAC-5000's broad functionality, low cost and ease of use make it the logical choice for monitoring or controlling experiments or pilot plants in a lab environment. Programs can be developed and edited with a dumb terminal and stored in battery backed-up RAM or PROM.

Personal Computers as Data Loggers: The μMAC-5000 is an ideal intelligent "front end" to a personal computer which allows it to be used to acquire, log, process, store and display data from a lab experiment or remote process. The μMAC-5000 with a printer can be used as a stand-alone data logger with the capability of sending exception messages to a host. Personal Computers can also be used as program development work stations for the μMAC-5000.

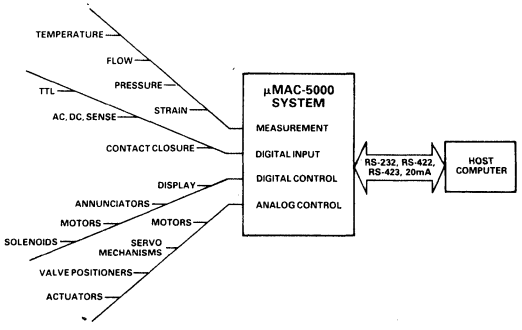
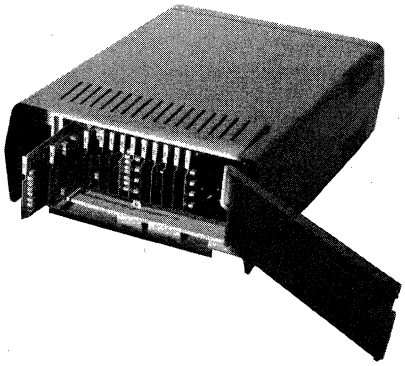


Figure 2. μMAC-5000 Measurement and Control Concept

MACSYM Measurement & Control Systems



MACSYM WORKSTATIONS

The Analog Devices' MACSYM® Workstation Product Family is designed to perform all of the important functions required in Automation Management and Control. Workstations are used as complete systems or in conjunction with our other system building blocks. Both the MACSYM 120 plant-floor workstation and the higher-performance MACSYM 150 laboratory or control room system are optimized for data acquisition, real-time analysis, supervisory control, man-machine interface and data management. As communication gateways, these workstations can also send timely and comprehensive information to higher-level computers or other vendors' equipment.

MACSYM Workstations serve as a foundation for a family of software products including a high-level language, menu-driven application software, and assembly language. MACBASIC™, a BASIC optimized for speed, incorporates extensive command extensions for analog, digital, pulse and frequency I/O along with easy-to-use graphics operations. Additionally, MACBASIC's exceptional mulitasking capabilities simplify implementation of real-time applications.

Application and Communication Software Products are available to work in conjunction with our Measurement and Control Units, other vendors' control units and higher-level computers. Both workstations utilize an industry-standard multitasking operating system which allows users to draw upon a large selection of popular software products.

Integral Measurement and Control I/O cards allow either workstation to be applied in smaller-scale applications typically found in laboratories, pilot plants or discrete parts testing operations. Hardware communications options make it easy to connect to other vendors' equipment.

Automation Management applications demand a variety of requirements from workstation products. MACSYM Workstations offer a selection of performance/features which will meet the demands of your application.

MACSYM 120

The MACSYM 120 is designed to operate within the temperature, dust, vibration and powerline conditions found in plant-floor environments. Manufactured for Analog Devices by IBM, this workstation is software and hardware compatible with the IBM PC/XT*. Packaging features such as a sealed membrane keyboard, special cooling system, protective door over the system disk drives, battery backed-up clock and system temperature sensor set this system apart from a standard office environment personal computer.

The MACSYM 120 Workstation accepts the Series 120 Family of I/O cards for local interface to analog and digital inputs and outputs, the ADI Family of Measurement and Control Units, peripherals and memory expansion cards. All of the hardware and software products offered by ADI with the MACSYM 120 are also available for use with IBM PC's.

The MACSYM 120 brings real workstation power to the plant floor. It combines the features of a sophisticated operator interface, a communications gateway and a control computer that implements advanced automation strategies. The MACSYM 120 delivers these capabilities to plant operating personnel.

MACSYM 150

The MACSYM 150 is a high-performance workstation designed for applications requiring more computational power, more memory, better graphics and more local I/O capacity than provided by the MACSYM 120. The system unit accepts the Series 100 Family of I/O cards for local interface to analog and digital inputs and outputs, the ADI Family of Measurement and Control Units, IEEE-48 instruments, peripherals and memory expansion cards.

Use the MACSYM 150 when a high-performance Measurement and Control Workstation is needed in a laboratory or control room. As a fast test and measurement system, instrument controller, supervisory controller and data collection and analysis system, this workstation provides an operator or higher-level computer with timely and comprehensive information.

WORKSTATION COMPARISON

	MACSYM 120	MACSYM 150
Peformance	Intel 8088 Microprocessor w/8087 Math Coprocessor	Intel 8086 Microprocessor w/8087 Math Coprocessor
	Computation Speed Factor = 1.0	Computation Speed Factor = 1.5
Memory	640KB RAM maximum	1MB RAM maximum
Graphics	High Resolution Monochrome	High Resolution Color
	Medium Resolution Color	High Speed Graphics Update
Option Slots	4 Slots for Series 120 Cards	6 Slots for Series 100 Cards
	Compatible with IBM PC/XT Options	
Environment	Plant	Lab/Control Room

WORKSTATION MEASUREMENT & CONTROL I/O

Analog Input
Analog Output
Digital Input and Output
Interface to Many Transducers Such as Thermocouples, RTD's or Strain Gages via the 3B Family

MEASUREMENT & CONTROL UNITS

MACSYM 200 and μMAC-4000 Interface Units
MACSYM 250, MACSYM 260 and μMAC-5000 Programmable Units

SYSTEM EXPANSION PRODUCTS

Memory Expansion Cards
Communications Expansion Cards
Monitors
Printers
Color Plotter

SOFTWARE PRODUCTS

High Level Language
Application Software: DAIS, MAS
MCComm™
Communications to Other Computers
Communications to Programmable Controllers

MEASUREMENT AND CONTROL UNITS

Analog Devices' Measurement and Control Units are system building blocks for a wide range of applications. Systems may be configured to meet requirements ranging from simple process monitoring to standalone control of complex processes or machine operations, to sophisticated product test systems. The product line includes rugged modules for factory-floor and process industry environments as well as units optimized for laboratory benchtop or pilot plant use.

Measurement and Control Units achieve their ability to interact with real-world sensors and actuators through comprehensive families of I/O boards. Inputs may be analog voltages or currents at high or low levels, thermocouples, strain gages, RTD's, relays, pulses, or frequencies. Analog and digital outputs control valves, actuators, and motors. Electrical isolation, fault protection, and signal conditioning for noisy real-world signals assure accurate, reliable measurements. Field wiring terminations promote serviceability and minimize hazards to equipment and personnel.

MACSYM 200

MACSYM 200 is a high-performance unit for high-speed burst-mode data acquisition and high point-count scanning. Its family of over 30 ADIO cards facilitates connection to most any type of sensor or actuator. The 16 slots available for these cards enable a large number of points to be measured and controlled from one chassis. Product test, process monitoring, and laboratory control are among the applications for which the MACSYM 200 is particularly effective. The MACSYM 200 is intended for laboratories, pilot plants, and industrial control rooms.

MACSYM 250

MACSYM 250 is used to form high-performance Measurement and Control Systems in conjunction with MACSYM Workstations or IBM Personal Computers. It features a large memory for program and data space, multi-tasking MACBASIC, and a high-speed integrated link to the workstation. It can acquire, analyze, and reduce data; implement and complex control strategies; respond to high-priority events; and report results. At the same time, the workstation can devote its full resources to operator-interface functions.

Use the MACSYM 250 in a laboratory, pilot plant, or control room setting for high-performance monitoring or product test applications.

MACSYM 260

MACSYM 260 is a rugged, high-performance unit capable of controlling complex operations in harsh plant environments. It has large memory capacity for sophisticated control strategies, arrays of test data, or multiple batch recipes. Programs may be stored in nonvolatile PROM for production applications. The MACSYM 260 has several forms of error-detection. Serviceability is designed-in with diagnostic indicator lights, and front panel replacement of all electronic assemblies. Multitasking MACBASIC simplifies the development of applications which require concurrent data acquisition, computation, control and communication. Multiple communication ports support terminals, printers, and data exchange with other computers.

The MACSYM 260 is used when significant measurement, control and computation power is required in a plant environment. These applications include high-performance product test stands, statistical process control of manufacturing, batch control, and control of complex equipment such as large extrusion machines.

MACSYM Measurement & Control Systems

MEASUREMENT & CONTROL INTERFACE UNITS COMPARISON

	MACSYM 200	MACSYM 250	MACSYM 260
Maximum Channel Capacity			
Analog I/O	512 S/E 256 Diff.	512 S/E 256 Diff.	512 S/E 256 Diff.
Digital I/O	256	256	256
Analog Sampling Speed (Burst Mode)			
Single Channel	33,000/Sec	33,000/Sec	33,000/Sec
Multiple Channel	6,000/Sec	7,000/Sec	7,000/Sec
Communication Ports			
Number	One	Two	Four
Type	RS-422, Sync.	RS-422, Sync. RS-232, Async.	RS-422, Sync. RS-232, Async. Isolated 20mA Current Loop
Maximum Memory	64K	512K	512K
Programmable	No	Yes	Yes
User EPROM	No	No	Yes
Operating Temperature	0-50°C	0-50°C	0-60°C

APPLICATION SOFTWARE

Application Software is a system building block that increases the level of solution provided by Analog Devices for Automation Management and Control. When combined with our other system building blocks, one can implement a fully-supported solution from a single vendor.

DAIS (Data Acquisition Information System) is a foundation for process monitoring applications involving hundreds of points. MAS (Micro Automation System) is designed for controlling small process units such as pilot plants. Both packages can be used without knowledge of programming because they are menu-driven.

DAIS

DAIS provides a simple operator interface, integral data base (for points, groups and logs), and extensive on-line point processing capability. DAIS accepts a wide range of process inputs, converts raw values to engineering units, performs three levels of alarm checking, saves historical data and provides printed reports. DAIS can be extended or customized via easy-to-use MACBASIC.

DAIS is used in a variety of applications where real-time process monitoring and supervisory control provide tighter control and improve operating efficiency.

MAS

MAS is a complete system integrating operator interface and control. It is complete because it has both continuous control and a high-level sequence control language, since many applications require more than just PID control. Via its menus, the operator has access to alarms, real-time trends, operator comment display, varying control parameters, and initiation or suspension of control. MAS is easily adapted to changing operating conditions and control requirements.

MAS improves repeatability and record keeping in small-scale automation projects.

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***IBM PC/XT is a trademark of International Business Machines Corporation.**

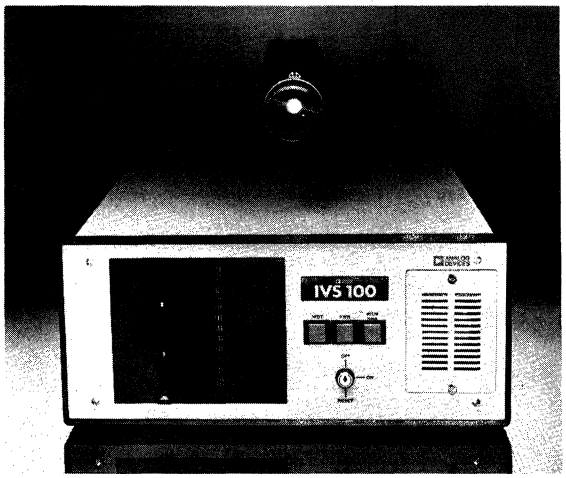
Machine Vision Systems

IVS-100 MACHINES VISION SYSTEMS

The IVS-100, (The Eye™), built from the ground up by Analog Devices, is a powerful and flexible machine vision development system. It features state-of-the-art hardware and software for machine vision. The system performs full gray scale processing and is capable of resolving both small and subtle defects at high speed. The IVS-100 system is designed with the flexibility to meet your specific needs. Hardware enable the system to be "built up" or "built down" to meet your requirements. An extensive library of machine vision routines is available as are "turnkey" software packages. This flexibility in both hardware and software ensures the delivery of the right, user-friendly, system at the lowest cost.

The IVS-100 is commonly used in applications requiring:

- Inspection, verification or sorting
- Alignment
- Character recognition
- Robot guidance.



Hardware Features of the Eye

- *256 gray level processing* (the highest in the industry) to accommodate varying or poor lighting conditions and to enable the IVS-100 to see small defects.
- *Dual process hardware.* The IVS-100 is the first vision system ever to employ the Intel* 80286/287 microprocessors and an Intel 80186 I/O processor. The I/O processor unburdens the main processor, from performing time consuming input/output tasks.
- *High resolution* (up to 512 × 512 pixels) is standard so The Eye can make accurate measurements and find small defects.
- *Built-in preprocessing.* With an arithmetic logic unit, a look-up table, and dual ram image storage, preprocessing can be performed. This image preprocessing is virtually cost free in a time sense and consequently saves the CPU time in not having to perform these tasks.
- *Two serial ports and one parallel port.* The IVS-100 communicates via one RS-232 serial port, one RS-422/423 serial port and one parallel port with 8 digital input lines and 8 digital output lines. It is capable of real-world interfacing and can communicate with host computers and a wide range of peripherals.
- *Up to eight cameras on one processing unit.* The Camera Multiplexer provides the IVS-100 with the capability of connecting up to 8 cameras to its framegrabber. With camera multiplexing capabilities, the user is able to create multiple workstations with one vision system.
- *Choice of storage space.* The IVS-100 is standardly configured with one 640K byte floppy drive and a 15M byte Winchester drive. In place of the 15M byte drive, a 68M byte Winchester is available. Increased Winchester storage is particularly useful for applications where image archiving or the performance of trend analysis for quality control is required.

Concurrent CP/M** Operating System and the Analog Devices Libraries of Machine Vision Software

- Concurrent CP/M (CCP/M) is a multitasking, real-time operating system. CCP/M is produced by Digital Research. On the IVS-100, CCP/M supports up to two physical consoles and eight virtual consoles. The machine vision software developed by Analog Devices is designed as a hierarchical structure of software building blocks to assist the machine vision programmer in fashion in efficient application programs. Having these building blocks available greatly increases productivity during program development.
- *IVS-100 Library.* The machine vision primitives are the lowest layer in the IVS-100 machine vision software structure. These are routines and drivers written in assembly language that implement a variety of low-level machine vision operations and are optimized for IVS-100 hardware.

  On the next level are machine vision functions, which are written in assembly language and C. These functions implement a wide range of machine vision algorithms for image processing, analysis and interpretation. Each of these routines were written to perform one function very fast (i.e. acquire an image, freeze an image, filter a line of pixel data, calculate a histogram).
- *Applications Library.* The Applications Library contains additional, higher level machine vision functions for image analysis and interpretation. Capabilities include windowing, blob location, automatic thresholding, centroid determination, etc. These routines are written primarily in C, and consist of combinations of the functions incorporated in the IVS-100 Library described above. Source code for the Applications Library is included with the library.
- *Applications Packages.* The final level of machine vision software available from Analog Devices are applications packages: complete menu-driven, user-friendly progrms performing specific machine vision tasks. Applications packages currently available from Analog Devices include: Optical Character Recognition and Verification, and Alignment.

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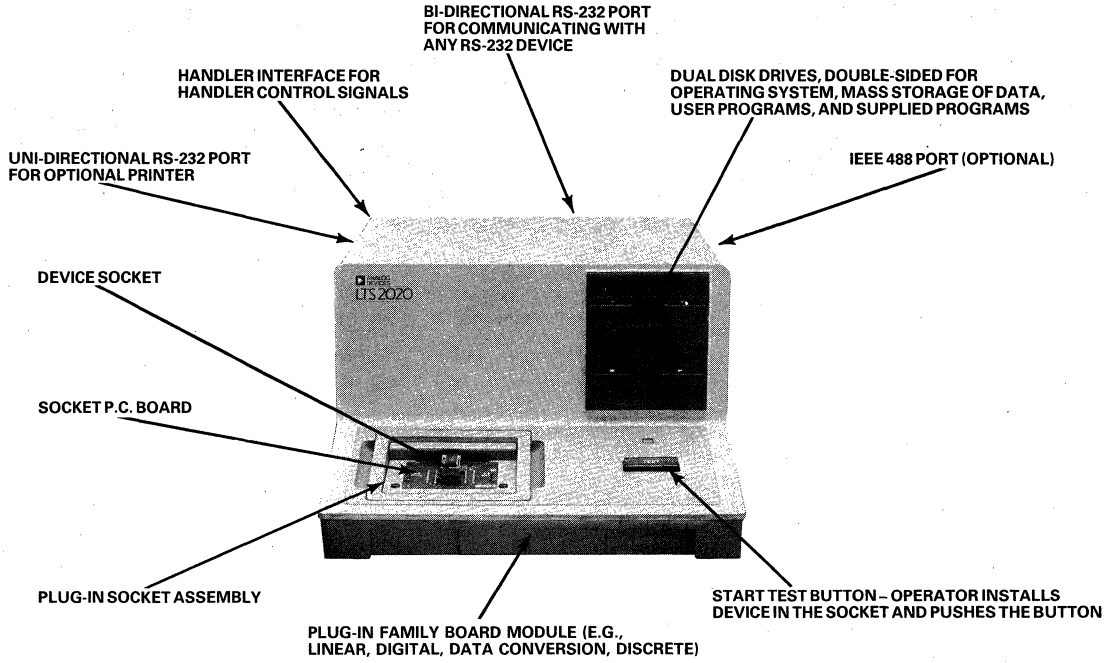
***Intel is a trademark of Intel Corporation.**
****Concurrent CP/M is a trademark of Digital Research, Inc.**

Component Test Systems



THE LTS SYSTEM CONCEPT

The LTS-2020 is a versatile component test system which allows you to test a multitude of components to the manufacturer's specifications (linear, digital, data conversion and discrete devices). The system also offers such features as RS232 ports for networking, IEEE for compatibility with handlers and probers, dual disk drives for mass storage of data, automatic self calibration, and a full statistical analysis software package.

The LTS-2020 provides several data output formats – data log, yield analysis and statistical analysis. The console provides the primary measurement and control functions to test a specific class of devices. The socket assembly is the mechanical and electronic interface for the family board and the DUT board. The DUT board plugs directly into the socket assembly and contains the circuitry and socket, specific to the actual device under test.

ANALOG DEVICES, Component Test Systems are the first benchtop testers that are programmable in BASIC and fill-in-the-blanks CREATE. CREATE is menu-driven software which prompts the user for data sheet limits and conditions, and builds a completed test program for the specified device. Turnkey program libraries are available for each of the device families.

Far more than just comprehensive production testers, they can handle complex engineering analysis and incoming inspection. They are the first systems that can provide all the capabilities of today's large centralized test systems at a cost that is approximately one-third that of a mainframe. The LTS-2020 not only provides the flexibility of distributed or decentralized testing, it allows for cost effective multiple system purchases. And they increase overall test reliability, since the threat of a single big failure is eliminated in a distributed testing environment.

LTS-2020 CONSOLE SPECIFICATIONS

Voltage Measurement Range	Current Range	Resolution	Accuracy
±10V	HI Z	10μV	±(0.0015% + 150μV)
Current Measurement Range	**Voltage Range**	**Resolution**	**Accuracy**
10mA to + 150mA	0 to +20V	2μA	±(2.5% + 100μA/V + 15μA)
−150mA to + 10mA	0 to −20V	2μA	±(2.5% + 100μA/V + 15μA)
−1.0mA to + 1.0mA	0 to + 10V	0.2μA	±(0.5% + 10μA)
−10mA to + 10mA	±10V	0.1μA	±(0.5% + 10μA)
Voltage Forcing Range	**Current Range**	**Resolution**	**Accuracy**
0 to +20V	−10mA to +150mA	100mV	±50mV
0 to −20V	−150mA to + 10mA	100mV	±50mV
0 to +10V	−1.0mA to + 1.0mA	50mV	±25mV
−10V to + 10V	−10mA to + 10mA	1mV	±500μV

Operating Voltage Range

105V to 125V AC @ 50Hz to 60Hz
210V to 250V AC @ 50Hz to 60Hz

System Reference Stability

10V ± 10 ppm/1000hrs. non-cumulative

Console Dimensions

W 19in. (48cm.) × D 26in. (66cm.) × H 12in. (31cm.)
Wt. 75 lbs. (39Kgs.)

Operating Temperature Range

0 to +40°C, +32°F to 104°F

SPECIFICATIONS (typical @ +25°C and 115V ac 60Hz unless otherwise noted)

	Type	Model	Output Voltage Volts	Output Current mA	Line Reg. Max %	Load Reg. Max %	Output Voltage Error Max	Ripple & Noise mV rms Max	Dimensions Inches
PC Board Mounted	Dual Output	915	±15	±25	0.2	0.2	±1%	1	3.5×2.5×0.875
		904	±15	±50	0.02	0.02	±200mV −0mV	0.5	3.5×2.5×0.875
		902	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		902-2	±15	±100	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×0.875
		920	±15	±200	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
		925	±15	±350	0.02	0.02	±1%	0.5	3.5×2.5×1.62
		921	±12	±240	0.02	0.02	+300mV −0mV	0.5	3.5×2.5×1.25
	Single Output	906	5	250	0.02	0.04	±1%	1	3.5×2.5×0.875
		903	5	500	0.02	0.04	±1%	1	3.5×2.5×1.25
		905	5	1000	0.02	0.05	±1%	1	3.5×2.5×1.25
		922	5	2000	0.02	0.05	±1%	1	3.5×2.5×1.62
		928	5	3000	0.05	0.10	±2%	5 (typ)	3.5×2.5×1.25
	Triple Output	923	±15	±100	0.02	0.02	±1%	0.5	3.5×2.5×1.25
			+5	500	0.02	0.05	±1%	0.5	
		926	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	300	0.02	0.10	±2%	1.0 (typ)	
		927	±15	±150	0.02	0.02	±2%	0.5 (typ)	3.5×2.5×1.62
			+5	1000	0.02	0.10	±2%	1.0 (typ)	
		2B35J	±15	±65	0.08	0.1	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.08	0.1		0.25	
		2B35K	±15	±65	0.01	0.02	(−0, +300mV)	0.5	3.5×2.5×1.25
			+1 to +15*	125	0.01	0.02		0.25	
Chassis Mounted	Dual Output	952	±15	±100	0.05	0.05	±2%	1	4.4×2.7×1.44
		970	±15	±200	0.05	0.05	±2%	1	4.4×2.7×1.44
		973	±15	±350	0.05	0.05	±2%	1	4.4×2.7×2.00
		975	±15	±500	0.05	0.05	±2%	1	4.4×2.7×2.00
	Single Output	955	5	1000	0.05	0.15	±2%	2	4.4×2.7×1.44
		976	5	3000	0.05	0.10	±2%	5 (typ)	4.75×2.7×2.00
	Triple Output	972	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	300	0.02	0.10	±2%	1.0 (typ)	
		974	±15	±150	0.02	0.02	±2%	0.5 (typ)	4.75×2.7×1.45
			+5	1000	0.02	0.10	±2%	1.0 (typ)	

*Resistor Programmable

SPECIFICATIONS (typical @ +25°C at nominal input voltage unless otherwise noted)

Model	Output Voltage Volts	Output Current mA	Input Voltage Volts	Input[1] Voltage Range Volts	Input Current Full Load	Output Voltage Error Max	Temperature Coefficient /°C Max	Efficiency Full Load Min	Dimensions Inches
943	5	1000	5	4.75/5.25	1.52A	±1%	±0.02%	62%	2.0×2.0×0.38
957*	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
958	5	100	5	4.5/5.5	200mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
941	±12	±150	5	4.75/5.25	1.17A	±0.5%	±0.01%	58%	2.0×2.0×0.38
959*	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
960	±12	±40	5	4.5/5.5	384mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
961*	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
962	±15	±33	5	4.5/5.5	396mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
963*	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
964	±15	±33	12V	10.8/13.2	165mA	±5%	±0.01% (typ)	50%	1.25×0.8×0.4
965	±15	±190	5V	4.65/5.5	1.7A	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
966	±15	±190	12V	11.2/13.2	710mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
967	±15	±190	24V	22.3/26.4	350mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
968	±15	±190	28V	26/30.8	300mA	±1%	±0.005% (typ)	62% (typ)	2.0×2.0×0.38
949	±15	±60**	5	4.65/5.5	0.6A	±2%	±0.03%	58%	2.0×1.0×0.375
940	±15	±150	5	4.75/5.25	1.35A	±0.5%	±0.01%	62%	2.0×2.0×0.38
953	±15	±150	12	11/13	0.6A	±0.5%	±0.01%	62%	2.0×2.0×0.38
945	±15	±150	28	23/31	250mA	±0.5%	±0.01%	61%	2.0×2.0×0.38
951	±15	±410	5	4.65/5.5	3.7A	±0.5%	±0.01%	62%	3.5×2.5×0.88

NOTES
*Unfiltered Models
**Single-ended or unbalanced operation is permissible such that total output current load does not exceed a total of 120mA.
[1]Models 940 and 941 will deliver up to 120mA output current (and model 943 will deliver up to 600mA) over an input voltage range of 4.65 and 5.5 V dc.

Integrated Circuits New Product Data Sheets

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ANALOG DEVICES

Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
Small Size: 4 Channels/Inch
Low Power: 35mW (AD204)
High Accuracy: ±0.05% max Nonlinearity
High CMR: 130dB (Gain = 100 V/V)
Wide Bandwidth: 5kHz Full-Power
High CMV Isolation: ±1000 V pk Continuous (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS
Multi-Channel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

GENERAL DESCRIPTION

The AD202 and AD204 are the first members of a new generation of low cost, high performance isolation amplifiers. A new circuit design, novel transformer construction, and the use of surface-mounted components in an automated assembly process result in remarkably compact, economical isolators whose performance in many ways exceeds that previously available from very expensive devices. The primary distinction between the AD202 and AD204 is that the AD202 is powered directly from +15V dc while the AD204 is powered by an externally supplied clock (AD246).

The AD202 and AD204 employ transformer coupling and do not require the design compromises that must be made when optical isolators are used: each provides a complete isolation function, with both signal and power isolation internal to the module, and they exhibit no long-term parameter shifts under sustained common-mode stress. Power consumption, nonlinearity, and drift are each an order of magnitude lower than can be obtained from other isolation techniques, and these advantages are obtained without sacrifice of bandwidth or noise performance.

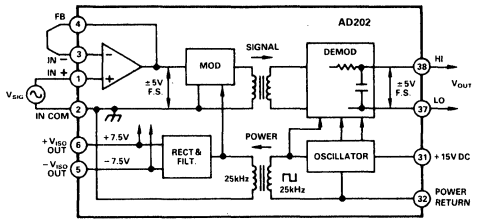
The design of the AD202 and AD204 emphasizes ease of use in a broad range of applications where signals must be measured or transmitted without a galvanic connection. In addition, the low cost and small size of these isolators makes component-level circuit applications of isolation practical for the first time.

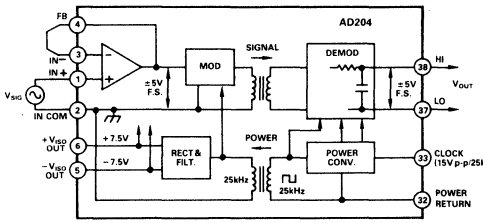
PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The new SIP form factor provides *complete* isolation (both signal and power) in a package just 0.25" wide, giving the user a channel density of four channels per inch. The isolation barrier is across the width of the package, which facilitates board layout and maximizes input-output spacing.

AD202/AD204 FUNCTIONAL BLOCK DIAGRAMS





High Accuracy: With a maximum nonlinearity of ±0.05% and low drift over temperature, the AD202 and AD204 can be used to provide isolation without loss of signal integrity.

Low Power: Power consumption of 35mW (AD204) and 75mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: Both models have ±1000V common mode voltage isolation and a total common-mode input capacitance of less than 5pF *inclusive* of power isolation. This results in CMR ranging from 130dB at a gain of 100 to 104dB (min. at unity gain) and very low leakage current (2μA max).

Flexible Input: An uncommitted op amp is provided at the input of both models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high-voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5V at 2mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or to power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5V at 0.4mA which is sufficient to operate adjustment networks or low-power references and op amps, or to provide an open-input alarm.

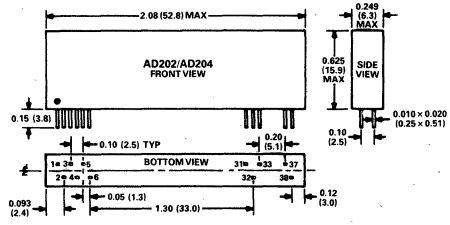
SPECIFICATIONS (typical @ +25°C, & V_S = +15V unless otherwise noted)

Model	AD204JY	AD202JY
GAIN		
Range	1V/V-100V/V	*
Error	±0.5% typ (4% max.)	*
vs. Temperature	±20ppm/°C typ (±45ppm/°C max)	*
vs. Time	±50ppm/1000 Hours	*
vs. Supply Voltage	±0.001%/V	±0.01%/V
Nonlinearity (G = 1V/V)	±0.025% typ (±0.05% max)	*
INPUT VOLTAGE RATINGS		
Linear Differential Range	±5V	*
Max. CMV Input to Output		
AC, 60Hz, Continuous	750V rms	*
Continuous DC	±1000V Peak	*
Common-Mode Rejection (CMR)		
R_S = ≤100Ω (HI & LO Inputs) G = 1	110dB	105dB
G = 100	130dB	*
R_S = ≤1kΩ (Input HI, LO, or Both) G = 1	104dB min	100dB min
G = 100	110dB min	*
Leakage Current Input to Output		
@240V rms, 60Hz	2μA rms max	*
INPUT IMPEDANCE		
Differential (G = 1V/V)	10^{12}Ω	*
Common Mode	2GΩ‖4.5pF	*
INPUT BIAS CURRENT		
Initial, @ +25°C	±30pA	*
vs. Temperature (0 to +70°C)	±10nA	*
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C	±5pA	*
vs. Temperature (0 to +70°C)	±2nA	*
INPUT NOISE		
Voltage, 0.1 to 100Hz	4μV p-p	*
f>200Hz	50nV/√Hz	*
FREQUENCY RESPONSE		
Bandwidth (V_O ≤10V p-p, G = 1-50V/V)	5kHz	1.5kHz
Settling Time, to ±10mV (10V Step)	1ms	*
OFFSET VOLTAGE (RTI)		
Initial, @ +25°C Adjustable to Zero	(±5 ±15/G)mV max	*
vs. Temperature (0 to +70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)$μV/°C	*
RATED OUTPUT		
Voltage (Out HI to Out LO)	±5V	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5V	*
Output Resistance	3kΩ	7kΩ
Output Ripple, 100kHz Bandwidth	10mV pk-pk	*
5kHz Bandwidth	0.5mV rms	*
ISOLATED POWER OUTPUT[1]		
Voltage, No Load	±7.5V	*
Accuracy	±10%	*
Current	2mA (Either Output)[2]	400μA Total
Regulation, No Load to Full Load	5%	*
Ripple	100mV pk-pk	*
OSCILLATOR DRIVE INPUT		
Input Voltage	15V pk-pk Nominal	N/A
Input Frequency	25kHz Nominal	N/A
POWER SUPPLY (AD202 Only)		
Voltage, Rated Performance	N/A	+15V ±5%
Voltage, Operating	N/A	+15V ±10%
Current, No Load (V_S = +15V)	N/A	5mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−25°C to +85°C	*
PACKAGE DIMENSIONS	2.08" × 0.249" × 0.625"	*

NOTES
*Specifications same as AD204JY.
[1]1.0μF min decoupling required.
[2]3mA with one supply loaded.
Specifications subject to change without notice.

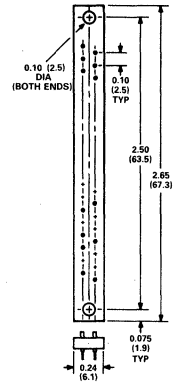
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



NOTE
PIN 31 IS PRESENT ONLY ON AD202.
PIN 33 IS PRESENT ONLY ON AD204.

AC1058 MATING SOCKET



AC1058 CAN BE USED AS A SOCKET FOR AD202, AD204 and AD246

AD202/AD204 PIN DESIGNATIONS

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
4	INPUT FEEDBACK
5	−V_{ISO} OUTPUT
6	+V_{ISO} OUTPUT
31	+15V POWER IN (AD202 ONLY)
32	CLOCK/POWER COM
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

CAUTION

ESD (Electro-Static-Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DIFFERENCES BETWEEN THE AD202 AND AD204

The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from +15V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) which can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of stand-alone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25kHz, 15V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multi-channel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3kΩ for the AD204 (7kΩ for AD202) and varies with signal level and temperature,

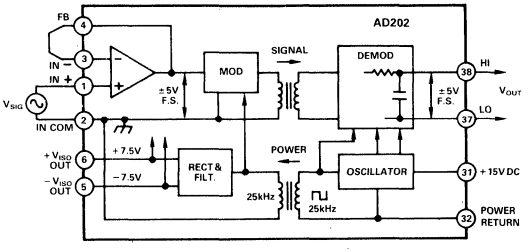


Figure 1a. AD202 Block Diagram

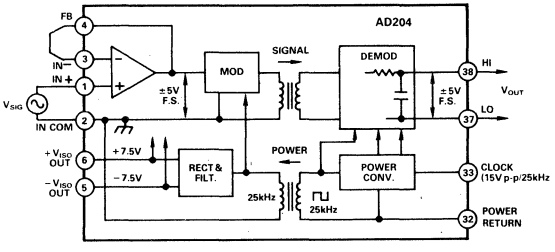


Figure 1b. AD204 Block Diagram

so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

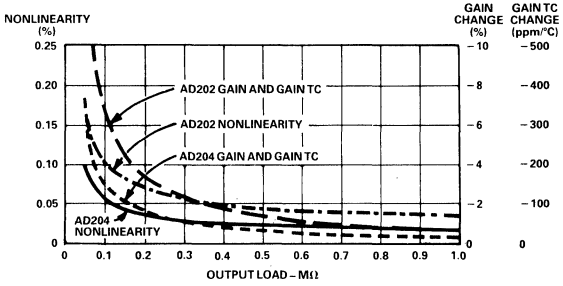


Figure 2. Effects of Output Loading

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single +15V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

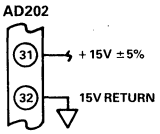


Figure 3a. Powering AD202

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15V p-p square wave with a nominal frequency of 25kHz) as shown in Figure 3b.

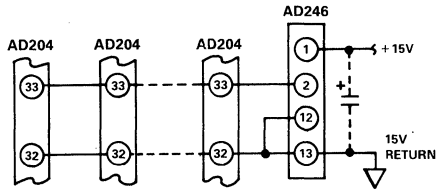


Figure 3b. Powering One or More AD204's

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock

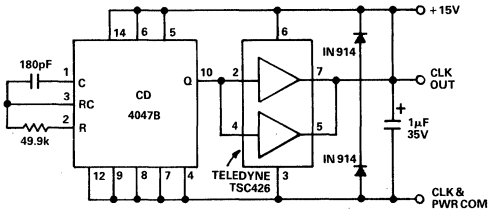


Figure 4. Clock Driver

circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25V and one additional isolator can be operated for each 40mV increase in supply voltage up to 15V. A supply bypass capacitor is included in the AD246, but if many AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1μF for every five isolators used. Place the capacitor as close as possible to the clock driver.

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be

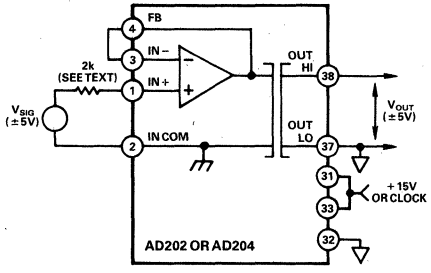


Figure 5. Basic Unity-Gain Application

handled, Figure 6 shows how to get gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20kΩ for best results. Whenever a gain of more than five is taken, a 100pF capacitor from pin 4 to pin 2 is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

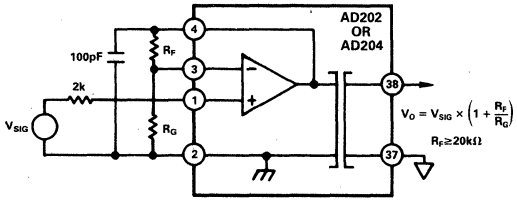


Figure 6. Input Connections for Gain > 1

The "noninverting" circuit of Figures 5 and 6 can also be used to advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the "noninverting" circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2kΩ resistor shown in series with pin 1 should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

Figure 7 shows how to accommodate current inputs or sum currents or voltages. This circuit can also be used when the input signal is larger than the ±5V input range of the isolator; for example, a ±50V input span can be accommodated with R_F = 20k and R_S = 200k. Once again, a capacitor from pin 4 to pin 2 is required for gains above 5.

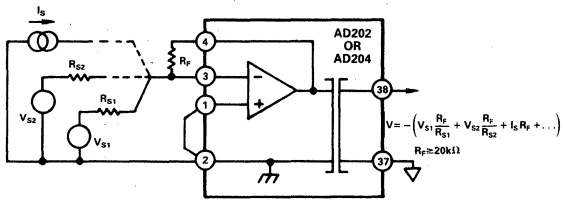


Figure 7. Connections for Summing or Current Inputs

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the "noninverting" connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

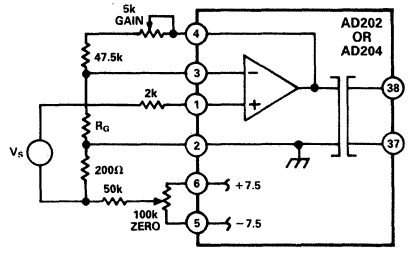


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

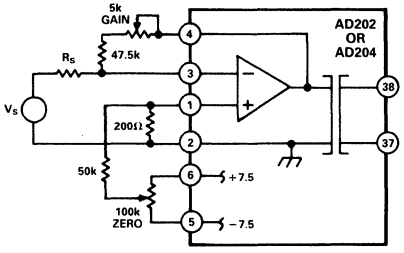


Figure 8b. Adjustments for Summing or Current Input

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

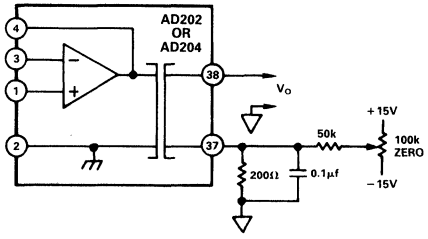


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that in the path from the source of the common-mode signal to pin 2 (IN COM). The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

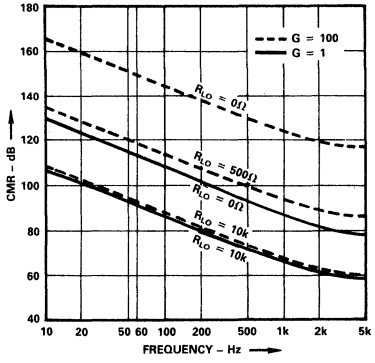


Figure 10a. AD204 Common-Mode Rejection vs. Frequency

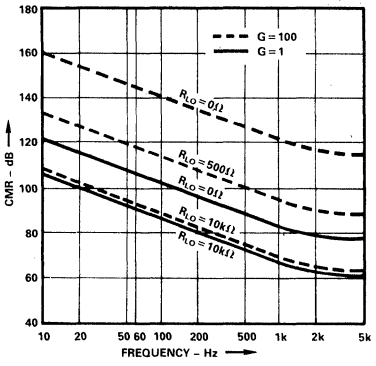


Figure 10b. AD202 Common-Mode Rejection vs. Frequency

Dynamics and Noise. Frequency response plots for the AD202 and AD204 are given in Figure 11. Since neither isolator is slew-rate limited, the plots apply for both large and small signals. Capacitive loads of up to 470pF will not materially affect frequency response. When large signals beyond a few hundred Hz will be present, it is advisable to bypass pins 5 and 6 to pin 2 with 1μF tantalum capacitors even if the isolated supplies are not loaded.

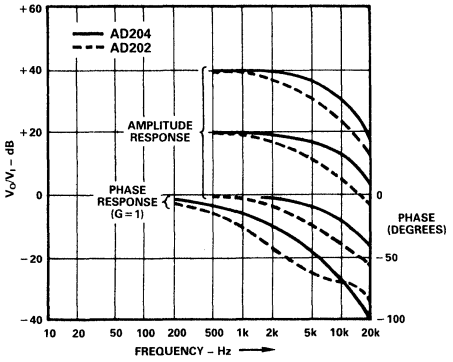


Figure 11. Frequency Response at Several Gains

The step response of the AD204 for very fast input signals can be improved by the use of an input filter, as shown in Figure 12. The filter limits the bandwidth of the input (to about 5.3kHz) so that the isolator does not see fast, out-of-band input terms that can cause small amounts (±0.3%) of internal ringing. The AD204 will then settle to ±0.1% in about 300 microseconds for a 10V step.

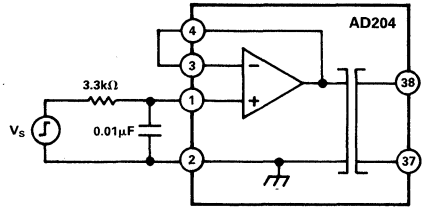


Figure 12. Input Filter for Improved Step Response

Except at the highest useful gains, the noise seen at the output of the AD202 and AD204 will be almost entirely comprised of carrier ripple at multiples of 25kHz. The ripple is typically 2mV p-p near zero output and increases to about 7mV p-p for outputs of ±5V (1MHz measurement bandwidth). Adding a capacitor across the output will reduce ripple at the expense of bandwidth: for example, 0.05μF at the output of the AD204 will result in 1.5mV ripple at ±5V, but signal bandwidth will be down to 1kHz.

When the full isolator bandwidth is needed, the simple two-pole active filter shown in Figure 13 can be used. It will reduce ripple to 0.1mV p-p with no loss of signal bandwith, and also serves as an output buffer.

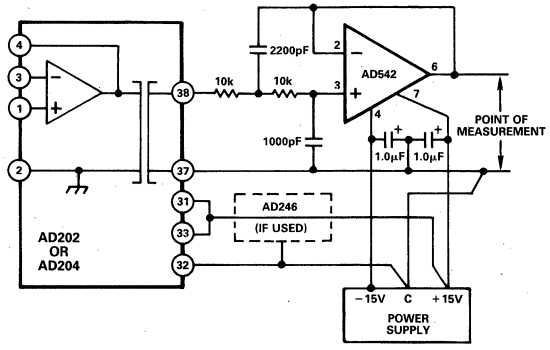


Figure 13. Output Filter Circuit Showing Proper Grounding

An output buffer or filter may sometimes show output spikes that do not appear at its input. This is usually due to clock noise appearing at the op amp's supply pins (since most op amps have little or no supply rejection at high frequencies). Another common source of carrier-related noise is the sharing of a ground track by both the output circuit and the power input. Figure 13 shows how to avoid these problems: the clock/supply port of the isolator does not share ground or 15V tracks with any signal circuits, and the op amp's supply pins are bypassed to signal common (note that the grounded filter capacitor goes here as well). Ideally, the output signal LO lead and the supply common meet where the isolator output is actually measured, e.g. at an A/D converter input. If that point is more than a few feet from the isolator, it may be useful to bypass output LO to supply common at the isolator with a 0.1μF capacitor.

Using Isolated Power. Both the AD202 and the AD204 provide ±7.5V power outputs referenced to input common. These may be used to power various accessory circuits which must operate at the input common-mode level; the input zero adjustment pots described above are an example, and several other possible uses are shown in the section titled Application Examples.

The isolated power output of the AD202 (400μA total from either or both outputs) is much more limited in current capacity than that of the AD204, but it is sufficient for operating micropower op amps, low power references (such as the AD589), adjustment circuits, and the like.

The AD204 gets its power from an external clock driver, and can handle loads on its isolated supply outputs of 2mA for each supply terminal (+7.5V and −7.5V) or 3mA for a single loaded output. Whenever the external load on either supply is more than about 200μA, a 1μF tantalum capacitor should be used to bypass each loaded supply pin to input common.

Up to 32 AD204s can be driven from a single AD246 (or equivalent) clock driver when the isolated power outputs of the AD204s are loaded with less than 200μA each, at a worst-case supply voltage of 14.25V at the clock driver. The number of AD204s that can be driven by one clock driver is reduced by one AD204 per 3.5mA of isolated power load current at 7.5V, distributed in any way over the AD204's being supplied by that clock driver. Thus a load of 1.75mA from $+V_{ISO}$ to $-V_{ISO}$ would also count as one isolator because it spans 15V.

It is possible to increase clock fanout by increasing supply voltage above the 14.25V minimum required for 32 loads. One additional isolator (or 3.5mA unit load) can be driven for each 40mV of increase in supply voltage up to 15V. Therefore if the minimum supply voltage can be held to 15V – 1%, it is possible to operate 32 AD204's and 52mA of 7.5V loads. Figure 14 shows the allowable combinations of load current and channel count for various supply voltages.

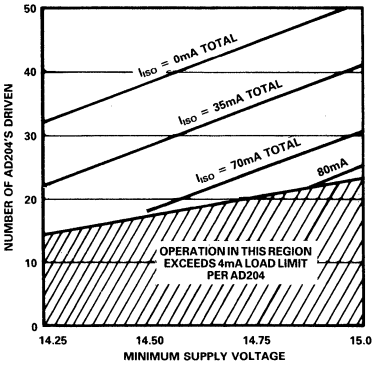


Figure 14. AD246 Fanout Rules

Operation at Reduced Signal Swing. Although the nominal output signal swing for the AD202 and AD204 is ±5V, there may be cases where a smaller signal range may be desirable. When that is done, the fixed errors (principally offset terms and output noise) become a larger fraction of the signal, but nonlinearity is reduced. This is shown in Figure 15.

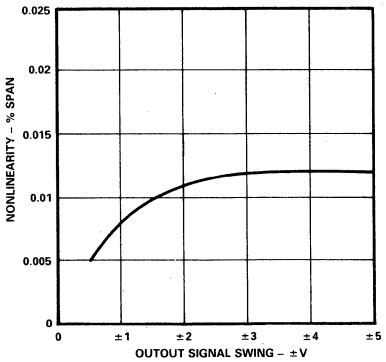


Figure 15. Nonlinearity vs. Signal Swing

PCB Layout for Multichannel Applications. The pinout of the AD204 has been designed to make very dense packing possible in multichannel applications. Figure 16a shows the recommended printed circuit board (PCB) layout for the simple voltage-follower connection. When gain-setting resistors are present, 0.25" channel centers can still be achieved, as shown in Figure 16b.

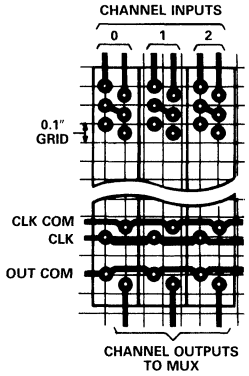


Figure 16a. PCB Layout for Multichannel Applications at G = 1

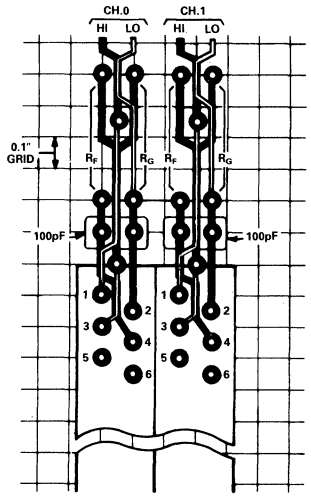


Figure 16b. PCB Layout for Multichannel Applications with Gain

Synchronization. Since AD204's operate from a common clock, synchronization is inherent. AD202s will normally not interact to produce beat frequencies even when mounted on 0.25-inch centers. Interaction may occur in rare situations where a large number of long, unshielded input cables are bundled together and channel gains are high. In such cases, shielded cable may be required or AD204's can be used.

APPLICATIONS EXAMPLES

Low-Level Sensor Inputs. In applications where the output of low-level sensors such as thermocouples must be isolated, a low-drift input amplifier can be used with an AD204, as shown in Figure 17. A three-pole active filter is included in the design to get normal-mode rejection of frequencies above a few Hz and to provide enhanced common-mode rejection at 60Hz. If offset adjustment is needed, it is best done at the trim pins of the OP-07 itself; gain adjustment can be done at the feedback resistor.

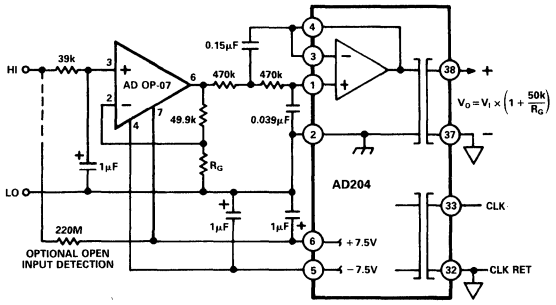


Figure 17. Input Amplifier & Filter for Sensor Signals

Note that the isolated supply current is large enough to mandate the use of 1μF supply bypass capacitors. This circuit can be used with an AD202 if a low-power op amp is used instead of the OP-07.

Process Current Input with Offset. Figure 18 shows an isolator receiver which translates a 4-20mA process current signal into a 0 to +10V output. A 1V to 5V signal appears at the isolator's output, and a −1V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

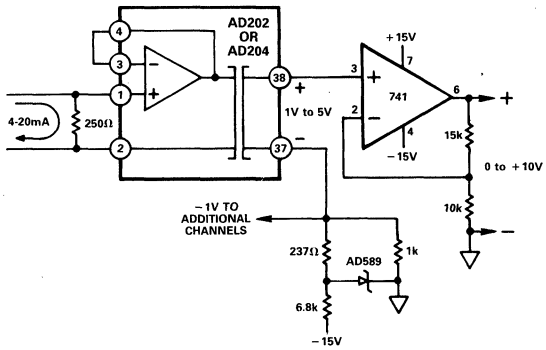


Figure 18. Process Current Input Isolator with Offset

The circuit as shown requires a source compliance of at least 5V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

Motor Control Isolator. The AD202 and AD204 perform very well in applications where rejection of fast common-mode steps is important but bandwidth must not be compromised. Current sensing in a full-wave bridge motor driver (Figure 19) is one example of this class of application. For 200V common-mode steps (1μs rise time) and a gain of 50 as shown, the typical response at the isolator output will be spikes of ±5mV amplitude, decaying to zero in less than 100μs. Spike height can be reduced by a factor of four with output filtering just beyond the isolator's bandwidth.

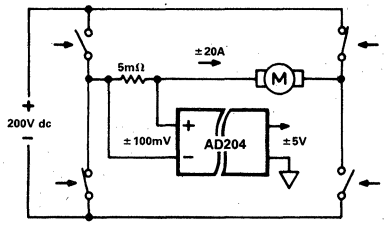


Figure 19. Motor Control Current Sensing

High-Compliance Current Source. In Figure 20, an isolator is used to sense the voltage across current-sensing resistor R to allow direct feedback control of a high-voltage transistor or FET used as a high-compliance current source. Since the isolator has virtually no response to dc common-mode voltage, the closed-loop current source has a static output resistance greater than $10^{14}\Omega$ even for output currents of several mA. The output current capability of the circuit is limited only by power dissipation in the source transistor.

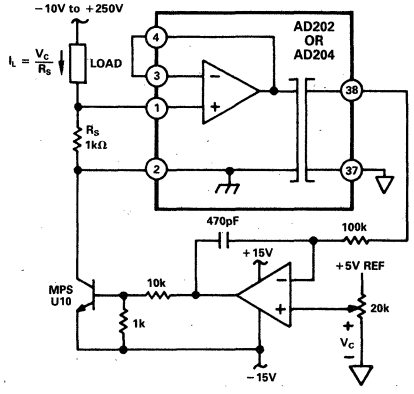


Figure 20. High-Compliance Current Source

Floating Current Source/Ohmmeter. When a small floating current is needed with a compliance range of up to ±1000V dc, the AD204 can be used to both create and regulate the current. This can save considerable power, since the controlled current does not have to return to ground. In Figure 21, an AD589 reference is used to force a small fixed voltage across R. That sets the current which the input op amp will have to return through the load to zero its input. Note that the isolator's output isn't needed at all in this application; the whole job is done by the input section. However, the signal at the output could be useful: it's the voltage across the load, referenced to ground. Since the load current is known, the output voltage is proportional to load resistance.

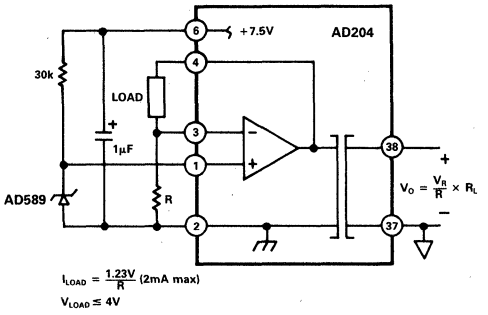


Figure 21. Floating Current Source

Photodiode Amplifier. Figure 22 shows a transresistance connection used to isolate and amplify the output of a photodiode. The photodiode operates at zero bias, and its output current is scaled by R_F to give a +5V full-scale output.

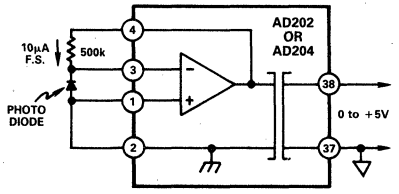


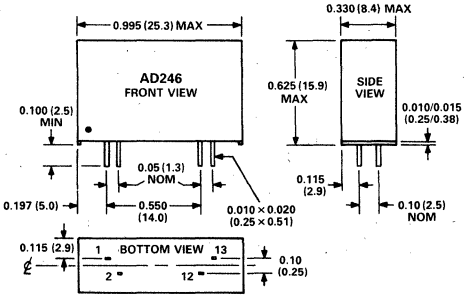
Figure 22. Photodiode Amplifier

SPECIFICATIONS

Model	AD246JY
OUTPUT	
Frequency	25kHz Nominal
Voltage	15V p-p Nominal
Fan-Out	32 max
POWER SUPPLY REQUIREMENTS	
Input Voltage	+15V ±5%
Supply Current	
Unloaded	3.5mA
Each AD204 Adds	2.2mA
Each 1mA Load On AD204	
$+V_{ISO}$ or $-V_{ISO}$ Adds	0.7mA

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION
1	+15V POWER IN
2	CLOCK OUTPUT
12	CLOCK COM
13	POWER COM

ANALOG DEVICES

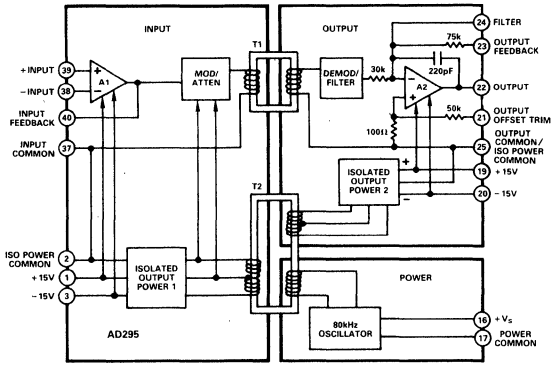
Precision Hybrid Isolation Amplifier

AD295

FEATURES
Low Nonlinearity: ±0.012% max (AD295C)
Low Gain Drift: ±60ppm/°C max
Floating Input and Output Power: ±15V dc @ 5mA
3-Port Isolation: ±2500V CMV (Input to Output)
Complies with NEMA ICS1-111
Gain Adjustable: 1V/V to 1000V/V
User Configurable Input Amplifier

APPLICATIONS
Motor Controls
Process Signal Isolator
High Voltage Instrumentation Amplifier
Multi-Channel Data Acquisition Systems
Off Ground Signal Measurements

AD295 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD295 is a high accuracy, high reliability hybrid isolation amplifier designed for industrial, instrumentation and medical applications. Three performance versions are available offering guaranteed nonlinearity error at 10V p-p output: ±0.05% max (AD295A), ±0.025% max (AD295B), ±0.012% max (AD295C). Using a pulse width modulation technique the AD295 provides 3-port isolation between input, output and power supply ports. Using this technique, the AD295 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. Additionally, floating (isolated) power ±15V dc @ 5mA is available at both the input and output. The AD295's gain can be programmed at the input, output or both sections allowing for user flexibility. An uncommitted input amplifier allows configuration as a buffer, inverter, subtractor or differential amplifier.

The AD295 is provided in an epoxy sealed ceramic 40-pin package that insures quality performance, high stability and accuracy. Input/output pin spacing complies with NEMA (ICS1-111) separation specifications required for many industrial applications.

WHERE TO USE THE MODEL AD295

Industrial: The AD295 is designed for measuring signals in harsh industrial environments. The AD295 provides high accuracy with complete galvanic isolation and protection from transients or where ground fault currents or high common-mode voltages are present. The AD295 can be applied in process controllers, current loop receivers, motor controls and weighing systems.

Instrumentation: In data acquisition systems the AD295 provides common-mode rejection for conditioning thermocouples, strain gauges or other low-level signals where high performance and system protection is required.

Medical: In biomedical and patient monitoring equipment like diagnostic systems and blood pressure monitors, the AD295 provides protection from lethal ground fault currents. Low level signal recording and monitoring is achieved with the AD295's low input noise (2μV p-p @ G=1000V/V) and high CMR (106dB @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Isolated power supply sections at the input and output provide ±15V dc @ 5mA. Isolated power is load regulated to 4%. This feature permits the AD295 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers at the input and external circuitry at the output. This eliminates the need for a separate dc/dc converter.

Input Amplifier: The uncommitted input amplifier allows the user to configure the input as a buffer, inverter, subtractor or differential amplifier to meet the application need.

Adjustable Gain: Gain can be selected at the input, output or both. Thus, circuit response can be tailored to the user's application. The AD295 provides the user with flexibility for circuit optimization without requiring external active components.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates the need for power supply and output ports being returned through a common ground.

Wide Operating Temperature: The AD295 is designed to operate over the −40°C to +100°C temperature range with rated performance over −25°C to +85°C.

Leakage: The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms at 115V ac, 60Hz. The AD295 meets standards established by UL STD 544.

SPECIFICATIONS (typical @ +25°C, & V_S = +15V unless otherwise noted)

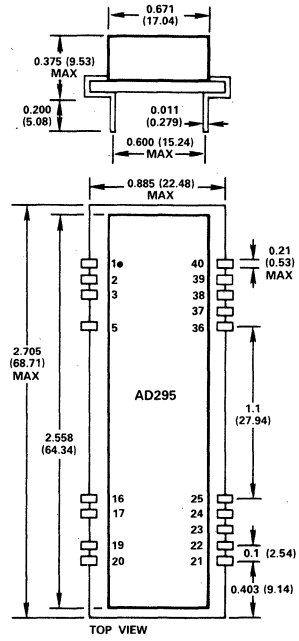
MODEL	AD295A	AD295B	AD295C
GAIN			
Range	1V/V to 1000V/V	*	*
Open Loop	100dB	*	*
Accuracy G = 1V/V	± 1.5%	*	*
vs. Temperature (−25°C to +85°C)			
G = 1V/V to 100V/V	± 60ppm/°C max	*	*
Nonlinearity (± 5V Swing) G = 1V–100V/V	± 0.05% max	± 0.025% max	± 0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range	± 10V min	*	*
Max Safe Differential Input	± 15V	*	*
Max CMV (Input to Output)			
Continuous ac or dc	± 2500V peak	*	*
ac, 60Hz, 1 Minute Duration	2500V rms	*	*
Max CMV (Input to Power Common/Output to Power Common)			
Continuous ac or dc	± 2000V peak	*	*
ac, 60Hz, 1 Minute Duration	2000V rms	*	*
CMR, Input to Output 60Hz, G = 1V/V			
$R_S \leq 1k\Omega$ Balanced Source Impedance	106dB	*	*
$R_S \leq 1k$ Source Impedance Imbalance	103dB min	*	*
Max Leakage Current, Input to Output			
@ 115V ac, 60Hz	2μA rms max	*	*
INPUT IMPEDANCE			
Differential	$5 \times 10^7\Omega \| 33pF$	*	*
Common Mode	$10^8\Omega \| 20pF$	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	5nA max	*	*
vs. Temperature (−25°C to +85°C)	−25pA/°C max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	± 2nA max	*	*
vs. Temperature (−25°C to +85°C)	± 5pA/°C max	*	*
INPUT NOISE (Gain = 1000V/V)			
Voltage			
0.01Hz to 10Hz	2μV p-p	*	*
10Hz to 1kHz	1μV rms	*	*
Current			
0.01Hz to 10Hz	10pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal (−3dB)			
G = 1V/V to 100V/V	4.5kHz	*	*
G = 1000V/V	600Hz	*	*
Full Power, 20V p-p Output			
G = 1V/V to 100V/V	1.4kHz	*	*
G = 1000V/V	200Hz	*	*
Slew Rate G = 1V/V to 100V/V	0.1V/μs	*	*
Settling Time G = 1V/V			
(to ± 0.1% for 10V Step)	550μs	*	*
(to ± 0.1% for 20V Step)	700μs	*	*
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial @ +25°C (Adjustable to Zero)	$\left(\pm 3 \pm \frac{15}{G_{IN}}\right)$ mV max	*	*
vs. Temperature (−25°C to +85°C)	$\left(\pm 10 \pm \frac{450}{G_{IN}}\right)$ μV/°C max	$\left(\pm 3 \pm \frac{300}{G_{IN}}\right)$ μV/°C max	$\left(\pm 1.5 \pm \frac{150}{G_{IN}}\right)$ μV/°C max
vs. Supply	$\left(\pm 1 \pm \frac{200}{G_{IN}}\right)$ μV/%	*	*
RATED OUTPUT			
Voltage, 2kΩ Load	± 10V min	*	*
Output Impedance	2Ω (dc to 100Hz)	*	*
Output Ripple (10Hz to 10kHz)	6mV p-p	*	*
(10Hz to 100kHz)	40mV p-p	*	*
ISOLATED POWER SUPPLIES[1] (V_{ISO1} & V_{ISO2})			
Voltage	± 15V dc	*	*
Accuracy	± 5%	*	*
Current[2]	± 5mA max	*	*
Load Regulation (No Load to Full Load)	−4%	*	*
Ripple, 100kHz BW	12mV p-p	*	*
POWER SUPPLY (+V_S)			
Voltage, Rated Performance	+15V dc ± 3%	*	*
Voltage, Operating	+12V dc to +16V dc	*	*
Current, Quiescent (V_S = +15V)	40mA	*	*
With V_{ISO} Loaded	45mA	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−40°C to +100°C	*	*
Storage	−40°C to +100°C	*	*
CASE DIMENSIONS	2.7" × 0.88" × 0.375"	*	*

NOTES
[1] V_{ISO2} accuracy and regulation 10%.
[2] ± 10mA can be supplied by V_{ISO1}, if V_{ISO2} is not used.

*Specifications same as AD295A.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TOP VIEW

RECOMMENDED MATING SOCKET: AC1220

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V (+V_{ISO1})	40	INPUT FEEDBACK
2	V_{ISO1} COM	39	+INPUT
3	−15V (−V_{ISO1})	38	−INPUT
		37	INPUT COM
5	NO CONNECTION	36	NO CONNECTION
16	+V_S	25	OUTPUT COM/ V_{ISO2} COM
17	POWER COMMON	24	FILTER
		23	OUTPUT FEEDBACK
19	+15V (+V_{ISO2})	22	OUTPUT
20	−15V (+V_{ISO2})	21	OUTPUT OFFSET TRIM

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD295, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable for the input signal to reduce inductive and capacitive pick-up. During circuit layout or interassembly connections, twisted wire pairs are recommended for power input and signal output. For basic isolator connections, see Figure 1. Capacitors C1-C5 are required in all applications to achieve the low noise rating and provide adequate filtering of the power supply.

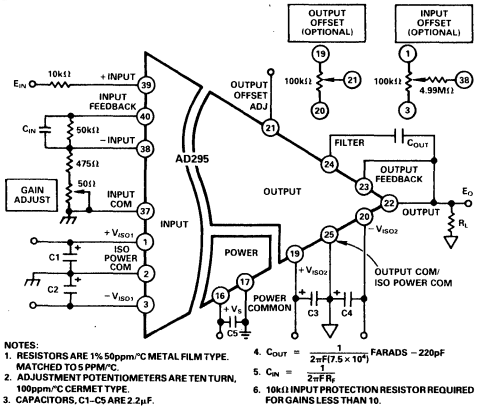


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD295 obtains its outstanding performance from a pulse width modulation technique using transformer coupling. This technique permits both signal and power transfer from input to the output stage of the isolator. Additionally, this technique provides higher noise immunity and lower nonlinearity than obtained from optically coupled or amplitude modulated transformer coupled techniques.

The three basic sections of the AD295 are shown in Figure 2. The power section 80kHz oscillator signal is transferred to the input and output sections via T2. The signal is then rectified and filtered providing dc power for that section's circuitry and for external application use. The input section consists of input amplifier A1 and the input modulator attenuator circuit. A triangular waveform derived from the 80kHz oscillator is sent to the modulator. If the input signal of A1 is zero, the triangle wave remains symmetrical. If A1 moves away from zero, the triangle wave moves positive or negative becoming asymmetrical. These modulated signals are converted to a pulsed waveform and transferred to the output section via T1. In the output section the signals are demodulated and filtered. The output amplifier A2 provides gain and additional filtering.

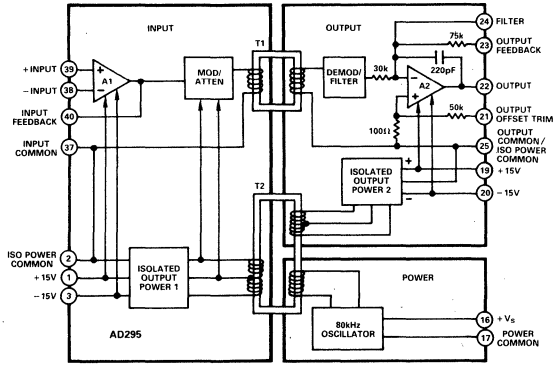


Figure 2. Basic Block Diagram

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance arises from stray coupling capacitance effects between the input terminals and signal output terminals. Each are shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates the AD295's capacitance between terminals.

Terminal Ratings: CMV performance is given in both continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequency. Figure 3 illustrates the AD295's ratings between terminals. Note that for the ±2500V rating between the input and output terminals to apply, the AD295 must be used in a three port configuration. If the output common is tied to the power common, the input to output CMV rating is ±2000V.

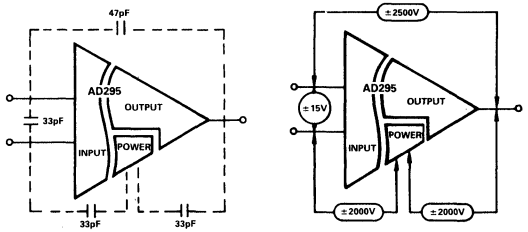


Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN ADJUSTMENT PROCEDURE

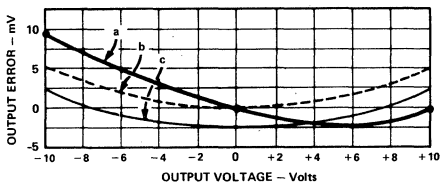
The calibration procedure, illustrated in Circuits 1 and 2, shows the recommended techniques that can be used to minimize output error. In this example, the output span is −10V to +10V.

Offset Adjustment

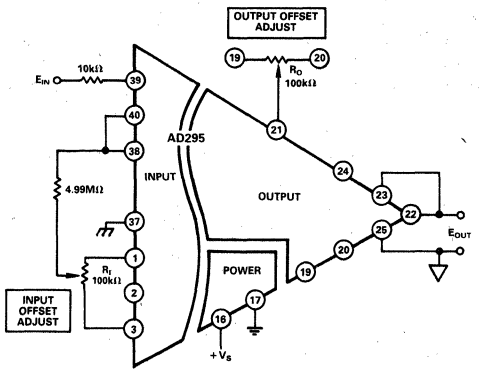
1. Configure the AD295 as shown in Circuit 1. G = 1.
2. Apply E_{IN} = 0V dc and adjust R_O for E_O = 0 volts.
3. Configure the AD295 as shown in Circuit 2. G = 100.
4. Apply E_{IN} = 0V dc and adjust R_I for E_O = 0 volts.
5. Repeat steps 1–4 if necessary.

Gain Adjust

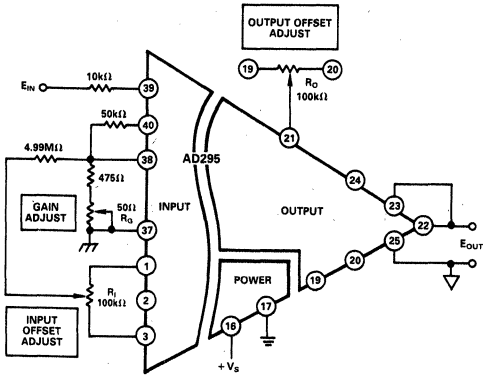
6. Apply E_{IN} = +0.1V dc adjust R_G for E_0 = +10.000V dc.
7. Apply E_{IN} = −0.1V dc and measure the output error (see Curve a.)



8. Adjust R_G until the output error is one half that measured in step 6 (see Curve b).
9. Apply $E_{IN} = +0.1V$ dc and adjust R_O until the output error is one half that measured in step 7 (see Curve c).
10. Repeat steps 6–9 if necessary.



Circuit 1. G = 1



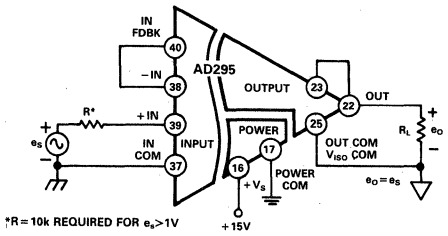
Circuit 2. G = 100

SELECTING GAIN

The AD295 basic gain is unity from input to output. All input signals are attenuated by 2.5 at the input modulator/attenuator then amplified at the output (see Figure 2).

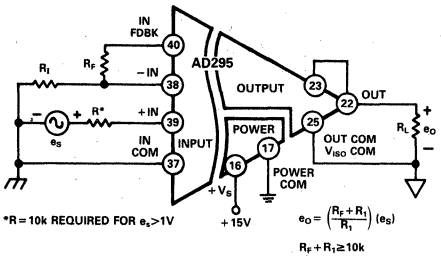
The AD295 contains both input and output amplifiers, the gains of which can be set independently. Figure 4 illustrates the basic gain configurations. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized since taking output gain multiplies output drift by the gain taken. Output gain can be used for improved linearity and frequency response at the expense of higher offset drift.

Figure 4a illustrates the basic unity gain configuration. With the uncommitted input amplifier configured as a buffer and pins 22 and 23 of the output amplifier jumpered, $e_O = e_S$.

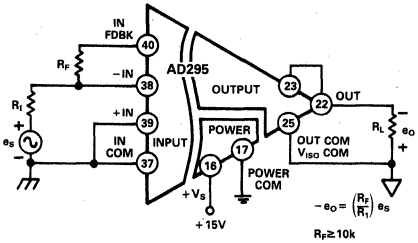


a. Basic Unity Gain Configuration

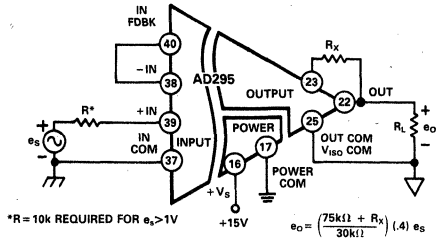
Input to output gain greater than unity can be independently set at the input, output, or both. For input gain configuration see Figures 4b and 4c. Output gain configuration is shown in Figure 4d.



b. Basic Gain Noninverting Configuration



c. Input Gain Inverting Configuration



d. Output Gain Noninverting Configuration

Figure 4. Input/Output Gain Configurations

PERFORMANCE CHARACTERISTICS

Phase Shift vs. Frequency: The phase shift vs. frequency response, for the AD295 is shown in Figure 5.

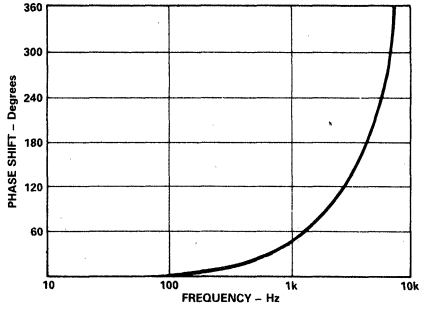


Figure 5. Typical AD295 – Phase Shift vs. Frequency

CMR vs. Frequency: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 60Hz and 1kΩ source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency for the AD295. CMR approaches 120dB at dc with a source impedance imbalance of 1kΩ.

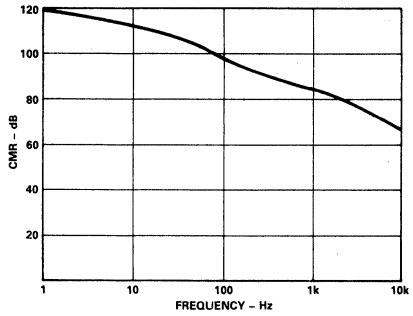


Figure 6. Typical AD295 – CMR vs. Frequency

Input Voltage Noise vs. Bandwidth: Voltage noise referred to the input is dependent on gain and bandwidth. Figure 7 illustrates the typical input noise in μV peak-to-peak in a 10Hz to 10kHz frequency range.

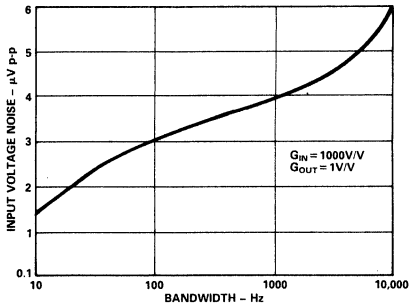


Figure 7. Typical AD295 – Input Voltage Noise vs. Bandwidth

Output Voltage Noise vs. Bandwidth: Voltage noise referred to the output is dependent on gain, bandwidth, input and output noise contributions. Figure 8 illustrates the typical output noise in mV peak-to-peak in a 10Hz to 10kHz frequency range.

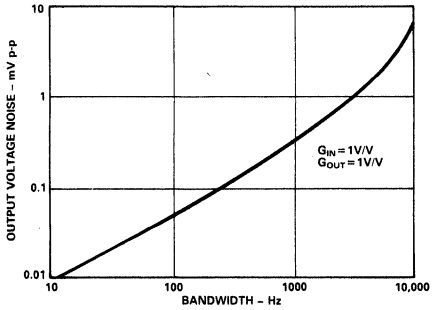


Figure 8. Typical AD295 – Output Voltage Noise vs. Bandwidth

Gain Nonlinearity vs. Output Swing: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as % peak-to-peak of output voltage span, e.g., nonlinearity of model AD295A operating at an output span of 10V peak-to-peak (±5V) is ±0.05% or ±5mV. Figure 9 illustrates the gain nonlinearity for output swing up to ±10V (20V peak-to-peak).

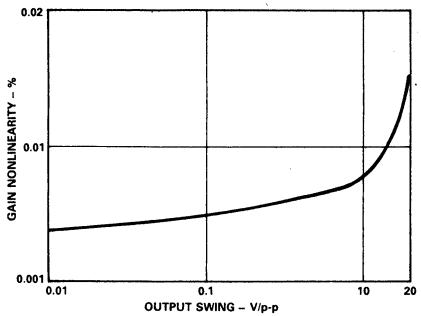


Figure 9. Typical AD295 – Gain Nonlinearity vs. Output Swing

Full Power Bandwidth vs. Gain: Figure 10 illustrates the full power bandwidth vs. gain for the AD295. A 1.4kHz full power response is possible with gain up to 100V/V.

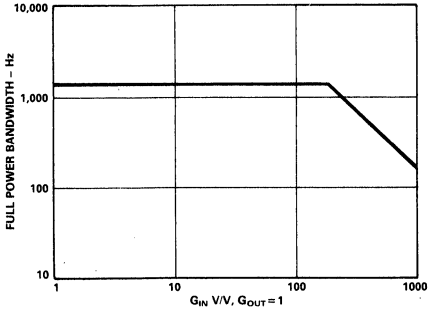


Figure 10. Typical AD295 – Full Power Bandwidth vs. Gain

Small Signal Bandwidth vs. Gain: Figure 11 illustrates the small signal bandwidth vs. gain for the AD295. The small signal response remains at 4.5kHz for gain up to 100V/V.

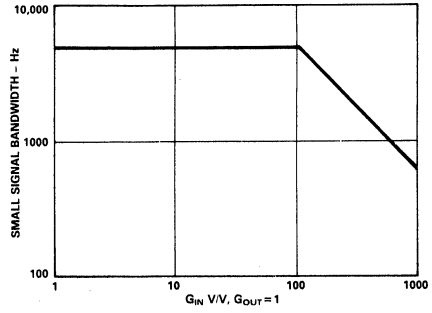


Figure 11. Typical AD295 – Small Signal Bandwidth vs. Gain

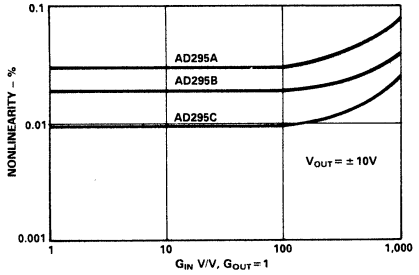


Figure 12. Typical AD295 – Gain Nonlinearity vs. Gain

Isolated Strain Gauge Using Front End of AD295

The AD295 can be used to condition and isolate differential signal sources like those present with strain gauge measurements. Figure 13 illustrates one possible configuration for conditioning a strain gauge. Amplifiers A1 and A2 are powered by the AD295's input isolated power supply. This eliminates the need for a separate dc/dc converter and provides a completely floated differential input. Input gain is selected via R_G and determined by the input gain formula.

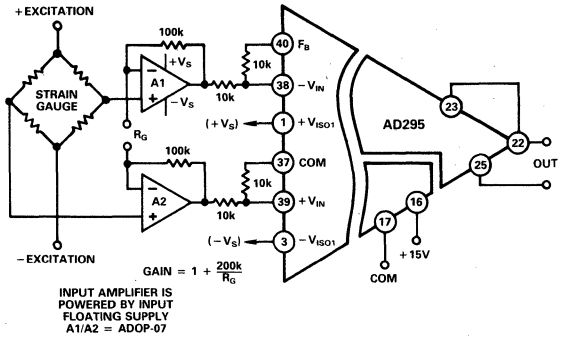


Figure 13. Isolated Strain Gauge Using Front End of AD295

Isolated Temperature Measurement with Cold Junction Compensation

The AD295 can be used to condition, isolate and provide cold junction compensation of thermocouples in temperature measurement applications. With the circuit shown in Figure 14, the AD590 must be thermally connected to the cold junction terminal for an accurate temperature measurement of the terminals. Using this circuit, accurate temperature measurements using the industry's popular J type thermocouple can be made.

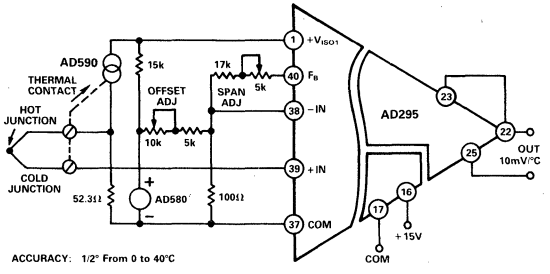


Figure 14. Isolated Temperature Measurement with Cold Junction Compensation

Isolated Voltage-to-Current Loop Converter

Illustrated in Figure 15, the AD295 is used to convert a 0 to +10V input signal to a standard 4-to-20mA current. Here high common-mode rejection and high common-mode voltage suppression are easily obtained with the AD295. The AD295 conditions the 0 to +10V input signal and provides a proportional voltage at the isolator's output. This output signal is converted to a 4-to-20mA current, which in turn is applied to the loop load R_{LOAD}.

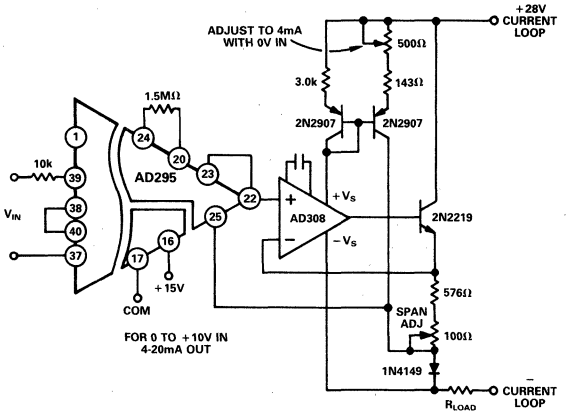


Figure 15. Isolated Voltage-to-Current Loop Converter

Noise Reduction in Data Acquisition Systems

In critical low noise applications like when an isolation amplifier precedes an analog to-digital converter, it may be desirable to add filtration, otherwise output ripple may cause inaccurate conversions. The 2-pole low-pass active filter shown in Figure 16 limits isolator bandwidth of the AD295. The filter will reduce output ripple and provide smoothing of discontinuous high frequency waveforms.

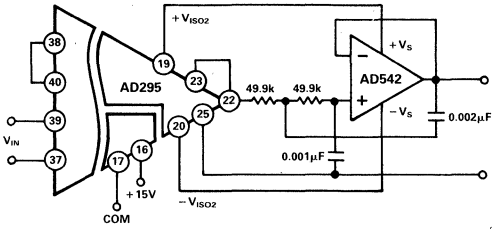


Figure 16. 2-Pole, 2kHz Active Filter

ANALOG DEVICES

Programmable Gain & T/H DAS Amplifier

AD365

FEATURES
Software Programmable Gain (1, 10, 100, 500)
Low Input Noise (0.2μV p-p)
Low Gain Error (0.05% max)
Low Nonlinearity (0.005% max)
Low Gain Drift (10ppm/°C max)
Low Offset Drift (2μV/°C RTI max)
Fast Settling (15μs @ Gain 100)
Small 16-Pin Metal DIP

APPLICATIONS
Digitally Controlled Gain Amplifier
Auto-Gain Ranging Amplifier
Wide Dynamic Range Measurement System
Gain Selection/Channel Amplifier
Transducer/Bridge Amplifier
Test Equipment

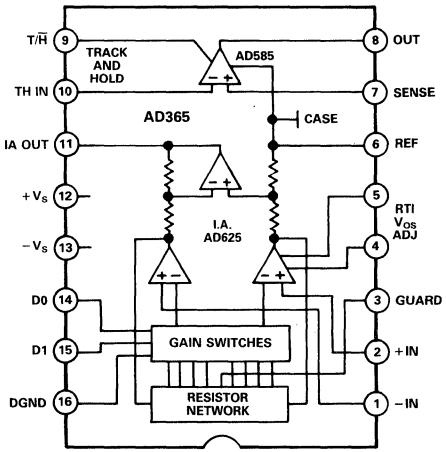
HIGHLIGHTS

The AD365 is a two stage data acquisition system (DAS) front end consisting of a digitally selectable gain amplifier followed by an independent track/hold amplifier. The programmable gain amplifier features differential inputs for excellent common-mode rejection, high open loop gain for superior linearity, and fast settling for use in multiplexed high speed systems. The track/hold amplifier features high open loop gain for 12-bit compatible linearity, internal hold capacitor for high reliability, and fast acquisition time for use with multichannel systems. Both amplifiers are capable of being used separately and are specified as independent function blocks.

GENERAL DESCRIPTION

The AD365 is comprised of the AD625 monolithic precision instrumentation amplifier to provide a precision differential input, the AD7502 monolithic CMOS multiplexer to handle gain switching, a precision thin-film resistor network, and the AD585 monolithic track and hold amplifier with internal hold capacitor.

AD365 FUNCTIONAL BLOCK DIAGRAM



The input stage provides high common-mode rejection, low noise, fast settling at all gains, and low drift over temperature. The gains of 1, 10, 100, and 500 are digitally selected with the two gain control lines which are 5V CMOS compatible.

The track and hold amplifier section is ideally suited for high speed 12-bit applications where fast settling, low noise, and low sample-to-hold offset are critical. The T/H mode is controlled with a single input line which can be tied to the status output line of the accompanying A/D converter.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

AD365AM	Min	Typ	Max	Units
PGA GAIN				
Inaccuracy[1]				
@ G = 1, 10, 100		0.02	0.05	%
@ G = 500		0.04	0.1	%
Nonlinearity				
@ G = 1, 10, 100			0.005	%
@ G = 500			0.01	%
Drift				
@ G = 1		1	5	ppm/°C
@ G = 10, 100, 500		3	10	ppm/°C
PGA OFFSET (May be Nulled at Input and Output)				
Input Offset Voltage (RTI)		25	200	µV
vs. Temperature		0.1	2	µV/°C
vs. Common-Mode Voltage		0.5	3.2	µV/V
vs. Supply Voltage		1	10	µV/V
Output Offset Voltage (RTO)		1	5	mV
vs. Temperature		30	150	µV/°C
vs. Common-Mode Voltage		60	316	µV/V
vs. Supply Voltage		60	316	µV/V
PGA INPUT				
Common- Mode and Differential Impedance		$10^9 \| 5$		Ω|pF
Differential Input Voltage, Linear	10	12		V
Common-Mode Voltage, Linear		$12 - V_{DIFF} \times G/2$		V
Input Stage Noise 0.1 to 10Hz		0.2		µV p-p
Input Stage Noise Density @ 1kHz		4		$nV/\sqrt{Hz}$
Bias Current		5	50	nA
vs. Temperature		50		pA/°C
Offset Current		2	20	nA
vs. Temperature		20		pA/°C
Noise Current (0.1 to 10Hz)		60		pA p-p
PGA OUTPUT				
Voltage 2kΩLoad	10	12		V
Output Impedance		0.2		Ω
Short Circuit Current		25		mA
Capacitive Load		500		pF
Output Stage Noise 0.1 to 10Hz		10		µV p-p
Output Stage Noise Density @ 1kHz		75		$nV/\sqrt{Hz}$
Guard Voltage		$(V_{+IN} + V_{-IN})/2$		V
Guard Offset		−550		mV
PGA DYNAMIC RESPONSE				
Small Signal − 3dB				
G = 1		800		kHz
G = 10		400		kHz
G = 100		150		kHz
G = 500		40		kHz
Full Power Bandwidth G = 1 @ V_O = 20V p-p		60		kHz
Slew Rate		4		V/µs
Settling Time to 0.01% @ V_O = 20V p-p				
G = 1, 10		8	10	µs
G = 100		12	15	µs
G = 500		40	50	µs
Gain Switching Time		1.5		µs
Overdrive Recovery Time V_{IN} = 15V @ G = 1		7		µs
PGA DIGITAL INPUTS				
Logic Low	0		0.8	V
Logic High	3.0		$+V_S$	V
Current, I_{INH} or I_{INL}		0.01	1	µA

AD365AM	Min	Typ	Max	Units
TRACK AND HOLD AMPLIFIER SECTION				
TRANSFER CHARACTERISTICS				
Open Loop Gain $V_O = 10V, R_L = 2k$	100k	200k		V/V
Nonlinearity @ G = +1			0.005	% FSR
Output Voltage $R_L = 2k\Omega$	10	12		V
Capacitive Load		100		pF
Short Circuit Current		25		mA
TRACK MODE DYNAMICS				
Acquisition Time to 0.01% 10V Step		2	3	μs
20V Step		4	5	μs
Small Signal Bandwidth −3dB		2		MHz
Full Power Bandwidth (20V p-p)		120		kHz
Slew Rate		10		V/μs
TRACK/HOLD SWITCHING				
Aperture Time		35		ns
Aperture Uncertainty		0.5		ns
Switching Transient		40		mV
Settling Time to 2mV		0.5		μs
HOLD MODE				
Droop Rate @ +25°C		0.3	1	V/sec
from $T_{AMBIENT}$ to T_{MAX}		Doubles/10°C		V/sec
Feedthrough		25		μV/V
Pedestal, Offset @ +25°C		2	3	mV
Over Temperature		3		mV
T/H ANALOG INPUT				
Bias Current		0.1	2	nA
Over Temperature		0.2	5	nA
Offset Voltage			2	mV
Over Temperature			3	mV
vs. Common Mode		25	100	μV/V
vs. Supplies		100	316	μV/V
Input Impedance		$10^{12} \| 10$		Ω‖pF
Noise Density @ 1kHz		50		$nV/\sqrt{Hz}$
Noise 0.1Hz to 10Hz		10		μV p-p
T/H DIGITAL INPUT CHARACTERISTICS				
Logic Low (Hold Mode)	0		0.8	V
Logic High (Track Mode)	2.0		$+V_S$	V
Input Current		10	50	μA
AD365 POWER REQUIREMENTS				
Positive Supply Range	+11		+17	V
Negative Supply Range	−11		−17	V
Quiescent Current		12	16	mA
Power Dissipation		360	550	mW
Warm-Up Time to Specification		5		Minutes
Ambient Operating Temperature	−25		+85	°C
Package Thermal Resistance (θ_{ja})		60		°C/W
AD365 ABSOLUTE MAXIMUM RATINGS				
Positive Supply $+V_S$	−0.3		+17	V dc
Negative Supply $-V_S$	+0.3		−17	V dc
Analog Input Voltage	$-V_S$		$+V_S$	V
Analog Input Current	−10		+10	mA
Digital Input Voltage	−0.3		$+V_S$	V
T/H Differential V_{IN}			±30	V
Storage Temperature	−65		+150	°C
Lead Soldering, 10 Sec			300	°C
Short Circuit Duration		Indefinite		

NOTE
[1]Gain = 10, 100 and 500 are trimmed and tested ratiometric to G = 1.

Specifications subject to change without notice.

TYPICAL CHARACTERISTICS (@ +25°unless otherwise noted)

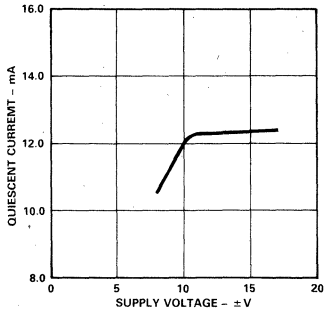


Figure 1. AD365 Quiescent Current vs. Supply Voltage

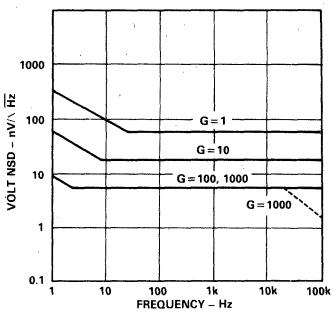


Figure 2. PGA RTI Noise Spectral Density vs. Gain

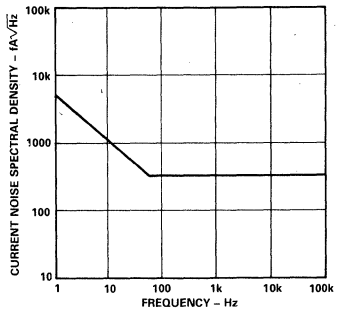


Figure 3. PGA Input Current Noise

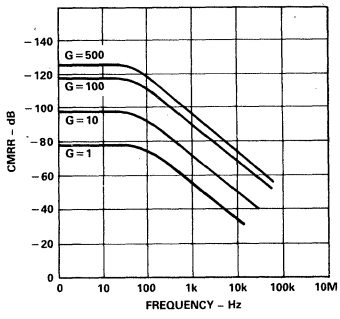


Figure 4. PGA CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

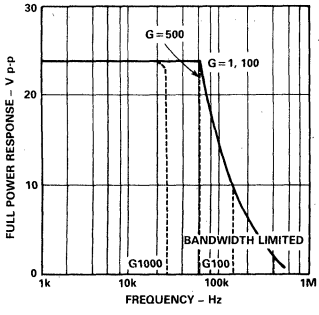


Figure 5. PGA Large Signal Frequency Response

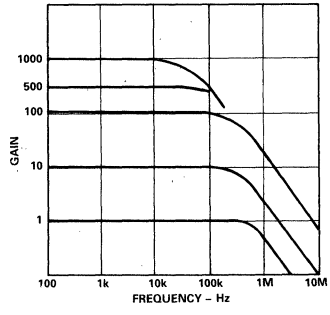


Figure 6. PGA Gain vs. Frequency

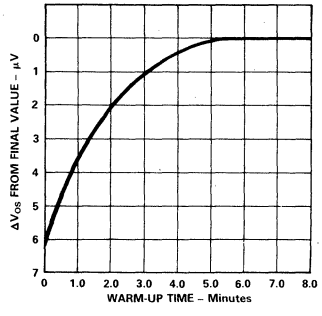


Figure 7. PGA Offset Voltage, RTI, Turn On Drift

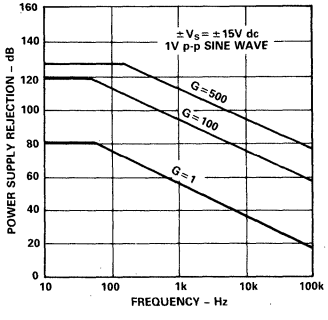


Figure 8. PGA PSRR vs. Frequency

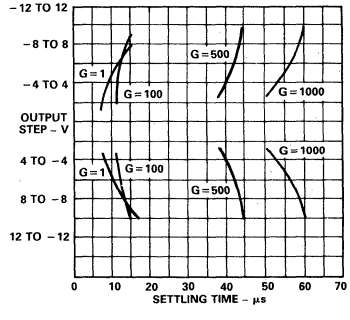


Figure 9. PGA Settling Time to 0.01%

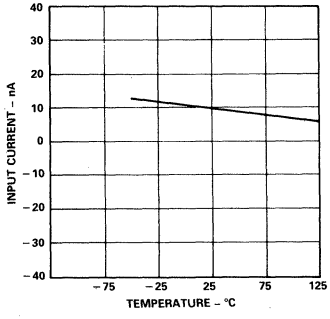


Figure 10. PGA Input Bias Current vs. Temperature

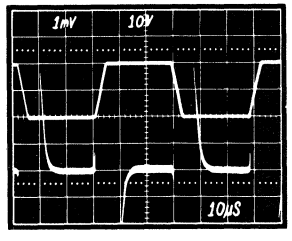


Figure 11. PGA Large Signal Pulse Response and Settling Time, G = 100

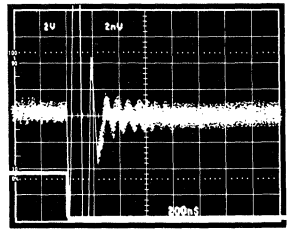


Figure 12. Sample-to-Hold Settling Time

The AD365 PGA section uses the AD625 monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp stage (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G + 1$) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

Digital gain control is provided using the D0 and D1 inputs (pins 14 and 15) which are decoded internally in the gain switching AD7502 as shown in Figure 15 below. The switch selects the resistance R_G from the laser trimmed resistor network according to the following gain select table.

D1	D0	PGA GAIN
0	0	1
0	1	10
1	0	100
1	1	500

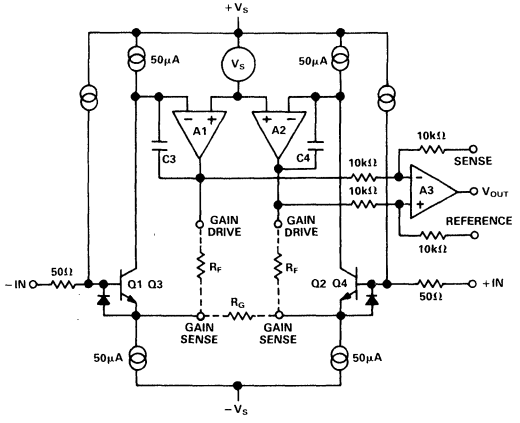


Figure 13. Simplified Circuit of the PGA

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the PGA; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is ($R_G + 300$)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 80Ω @ G = 500), the maximum overload voltage the PGA can withstand, continuously, is approximately ±5V. Figure 14 shows the external components

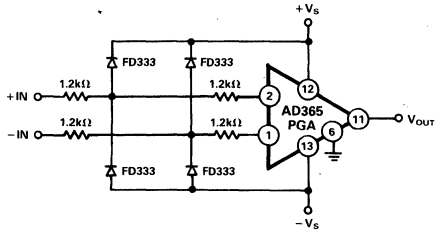


Figure 14. Input Protection Circuit for PGA

necessary to protect the PGA under all overload conditions at any gain. The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±2V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered, however, that the total output swing, to be shared between signal and reference offset, should be ±10 volts (from ground).

The PGA section reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625, a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega$ = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 15. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

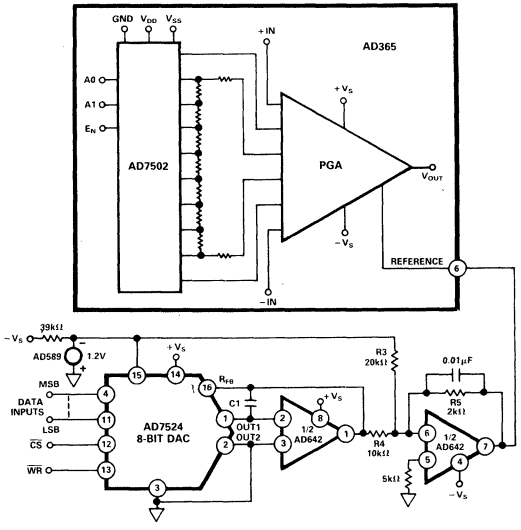


Figure 15. Software Controllable Offset

The circuit of Figure 15 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$. To be symmetrical about 0V, R_3 must be equal to $2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 15 is ±120mV, and the offset is incremented in steps of 0.9375mV/LSB.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains. Input errors dominate at high gains and output errors dominate at low gains.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain ×input error) + output error

The AD365 provides for input offset voltage adjustment (see Figure 16). This simplifies nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

Output offset adjustment is normally provided by the A/D converter offset adjustment which will compensate for the output offset of the PGA, offset of the T/H amplifier, and offset of the A/D.

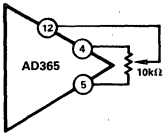


Figure 16. Input Voltage Offset Adjustment

COMMON-MODE REJECTION

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figure 17 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

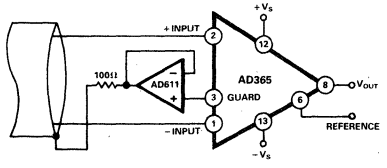


Figure 17. Common-Mode Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 18). Since the AD365 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

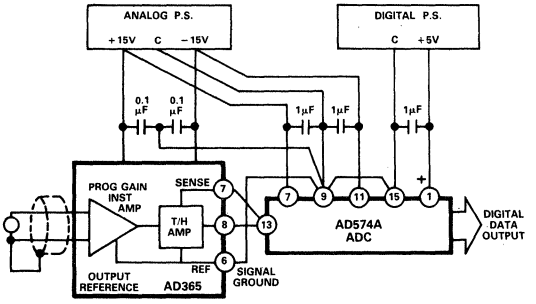


Figure 18. Basic Grounding Practice

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 19.

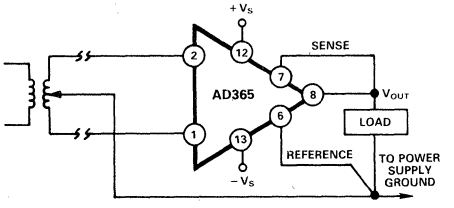


Figure 19a. Ground Returns for Bias Currents with Transformer Coupled Inputs

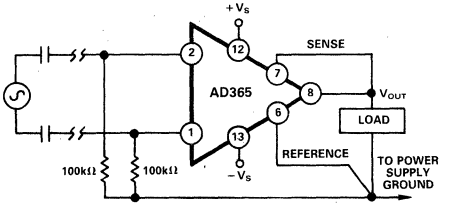


Figure 19b. Ground Returns for Bias Currents with ac Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 20 provides a hardware solution.

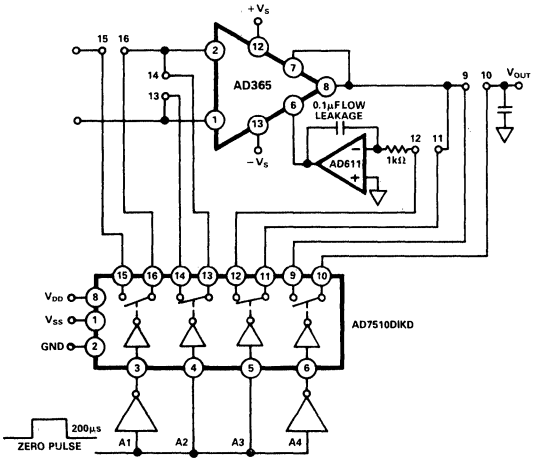


Figure 20. Auto-Zero Circuit

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD365) remain isothermal. This includes the input leads (1, 2). In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. In the case of a resistive transducer, a capacitor across the input working against the internal resistance of the transducer may suffice to provide an RC filter. These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 1 and 2, to preserve high ac CMR.

THEORY OF OPERATION – T/H SECTION

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 21 shows pictorially the track-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Track-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Track Transition.

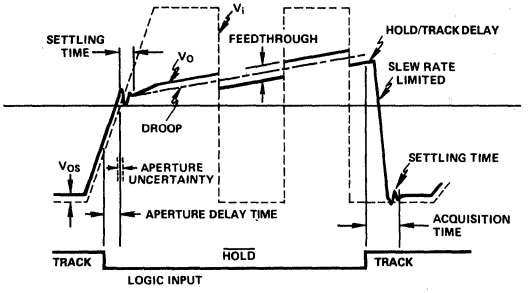


Figure 21. Pictorial Showing Various T/H Characteristics

TRACK-TO-HOLD TRANSITION

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 22 will result.

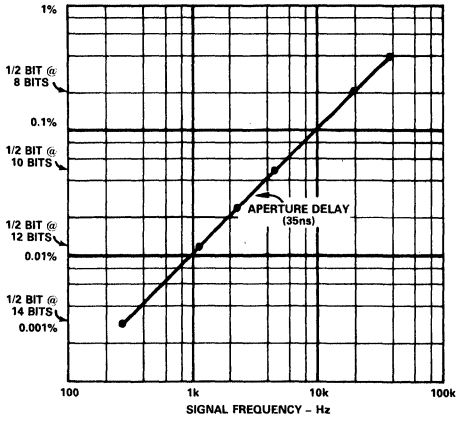


Figure 22. Aperture Delay Error vs. Frequency

To eliminate the aperture delay as an error source the track-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then T/H trigger uncertainty/jitter and internal aperture jitter which are the variations in aperture delay time from sample-to-sample remain. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi \text{ (Aperture Jitter)}}$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5\times10^{-9})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\,(\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF}} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V\text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt.

$$\frac{dV\text{ max}}{dt} = \frac{\Delta V\text{ max}}{t_{CONV}}$$

The maximum $\frac{dV\text{ max}}{dt}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{(\Delta T°C)}{10°C}} \le \frac{dV\text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

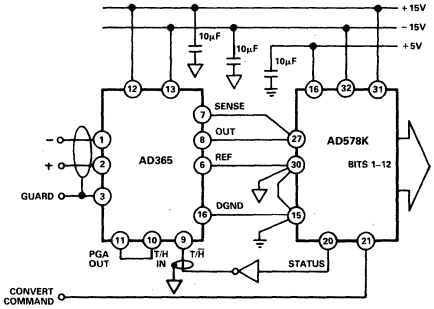


Figure 23. A/D Conversion System, 117.6kHz Throughput 58.8kHz Max Signal Input

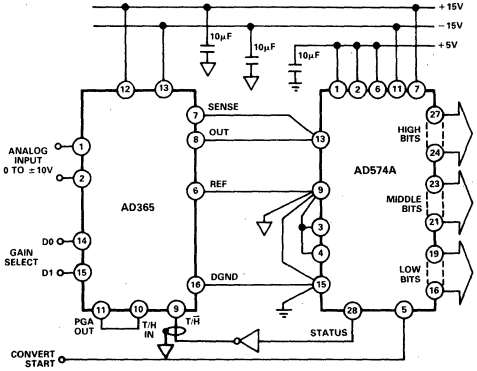
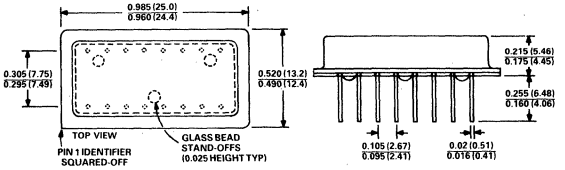


Figure 24. 12-Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN DUAL-IN LINE METAL PACKAGE



Hermetically Sealed 16-Pin Dual-In-Line (Gross Leak Tested per MIL-STD-883, Method 1014). Pin 6 is Electrically Connected to the Case. Case Has Metal Bottom Surface.

ANALOG DEVICES

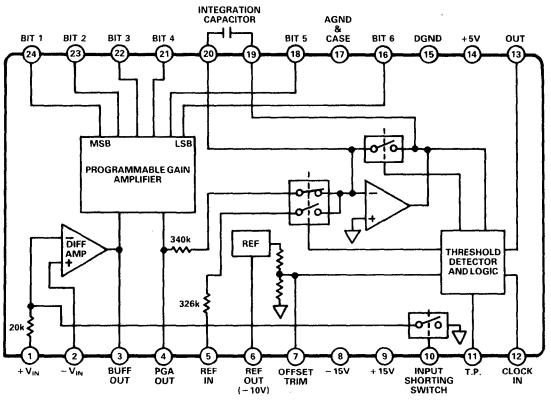
High Resolution Programmable Gain DAS

AD367

FEATURES
Differential Input – Programmable Gain Amplifier
6 Bit (1 of 64) Gain Control
Internal – 10V Reference
15 Bit Integral Nonlinearity
±305μV Resolution
10ms Conversion Time
External Integration Capacitor
Programmable Conversion Time

APPLICATIONS
Medical Instruments
Blood Analyzers
Analytical Instrumentation
Data Acquisition Systems
Chromatography
Process Control

AD367 FUNCTIONAL BLOCK DIAGRAM
AND PIN DESIGNATION



PRODUCT DESCRIPTION

The AD367 is a wide dynamic range integrated circuit which contains all the analog functions needed to construct a high resolution, high accuracy integrating Data Acquisition System. It utilizes hybrid technology to incorporate a programmable gain amplifier, integration amplifier, – 10V reference, comparator, and control logic in a 24-pin hermetic dual-in-line package.

The programmable gain amplifier provides 6 bits (1 of 64) gain control which are digitally selectable with CMOS voltage levels. The dual slope converter uses time to quantitize the analog input signal. The differential front-end allows true differential inputs with high common-mode rejection, or single-ended inputs with ground sense capability. This conversion technique has inherent high frequency noise immunity and excellent normal mode noise rejection at frequencies that are integal multiples of $1/T_1$ (T_1 = the signal integration period). The conversion accuracy is independent of both the integration capacitance and clock frequency, since they affect both the signal integration phase and reference integration phase in the same ratio. A microprocessor and software routine or any digitizing timer that accepts TTL inputs can be used to count clock pulses to digitize the AD367 output. The integration capacitor is external, therefore conversion time may be adjusted by the user. The nominal value is 0.012μF for an integration time of 4ms and total conversion time of 10ms. By choice of integration capacitor and clock frequency the integration time is programmed from a minimum of 2ms to a maximum of 20ms. The maximum conversion rate is 200 per second.

PRELIMINARY DATA SHEET

PRODUCT HIGHLIGHTS

1. The AD367KM provides true 15-bit (±0.00305% FSR maximum linearity error) performance with 305μV resolution.
2. The differential input programmable gain amplifier front end has 6-bit (1 of 64) gain control. This provides gains of 0.282V/V to 24V/V, or input full scale ranges of 0.417V to 10.0V for maximum flexibility.
3. The integration capacitor is external. Conversion time is user-programmable, from 2ms to 20ms. The maximum conversion rate is 200 conversions per second.
4. The dual slope integration conversion technique provides superior high frequency noise immunity, and excellent normal mode noise rejection of frequencies which are multiples of the inverse of the integration period.
5. An internal precision – 10.0V reference is provided, but an external reference may be used for multi-channel applications where use of a system reference is required.
6. The pulse-width output is easily converted to digital binary format by the addition of external IC counter-timers. The counter clock rate is independent of the integrator clock rate.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, +5V, T1 = 4.000ms, C_{INT} = 0.012µF unless otherwise noted)

Parameter	AD367KM Min	Typ	Max	Units
ACCURACY/RESOLUTION				
Integral Nonlinearity Error [1]			0.00305	% FSR
Resolution [2]	±305			µV
ANALOG INPUTS				
V_{INPUT}	0		10	V
Input Resistance	80			kΩ
Common Mode Rejection Ratio[3]	90	100		dB
V_{REF} Input Resistance	300			kΩ
Shorting Switch Isolation[4]	45	56		dB
DIGITAL INPUTS				
Clock				
V_{INH}	2			V
V_{INL}			0.7	V
Gain Bits[5]				
V_{INH}	14.5			V
V_{INL}			0.7	V
DIGITAL OUTPUT (LSTTL Compatible)				
V_{OH}	2.4			V
V_{OL}			0.4	V
I_{OH}	−370			µA
I_{OL}			6	mA
DYNAMIC PERFORMANCE				
Conversion Time			10	ms
Offset Pulse Width[6]	152	200	248	µs
Scale Factor	361	384	407	µs/V
Over Temperature		±10		ppm/°C
PSRR[7]				
+15V ± 3%		0.5		µs/V
−15V ± 3%		0.5		µs/V
+5V ± 3%		1		µs/V
PROGRAMMABLE GAIN AMPLIFIER[8]				
Maximum Gain		24		V/V
Minimum Gain		0.282		V/V
Resolution			6	Bits
Gain Error, Any Range			±2	%
Gain Linearity Error			±0.00305	% FSR
INTERNAL VOLTAGE REFERENCE				
V_{REF}	−9.95	−10	−10.05	V
vs. Temperature		10	15	ppm/°C
Maximum External Current without Degradation			500	µA
POWER REQUIREMENTS				
Positive Supply Range	14.55	15	15.45	V
Negative Supply Range	−14.55	−15	−15.45	V
Logic Supply Range	4.75	5	5.25	V
Supply Current				
+15V		18		mA
−15V		23		mA
+5V		27		mA
Power Dissipation		750	1100	mW
TEMPERATURE RANGE				
Specification	0		70	°C
Operating	−25		+85	°C
Storage	−55		+125	°C
PACKAGE	24-Pin Double-DIP			

NOTES

[1] Referenced to the input.

[2] Referenced to the output of the programmable gain stage (Pin 4).

[3] Source impedance <1Ω 0 to 10V

[4] A_{INL} (Pin 2) at analog ground.

[5] Open collector TTL and 15V CMOS compatible.

[6] Offset Pulse width (V_{IN} = 0V) = $\frac{V_{OS}C\,R_{INT2}}{V_{REF}} \cdot R_{INT2}$ = 327kΩ nominal.

[7] V_{IN} = 10V, Gain = 1.03.

[8] Gain = $\frac{24 \times (128 \times B1 + 64 \times B2 + 32 \times B3 + 16 \times B4 + 8 \times B5 + 4 \times B6 + 3)}{255}$

Specifications subject to change without notice.

Complete Programmable Gain 12-Bit Data Acquisition System

AD369

FEATURES

Includes: Programmable Gain Instrumentation Amplifier, Track and Hold Amplifier 12-Bit A/D Converter
Digitally Controlled Gain (1, 10, 100, 500)
50kHz Throughput Rate
Small Size: 28-Pin Metal Hermetic Double DIP
Guaranteed No Missing Codes Over Temperature
True 12-Bit Linear; Error ≤1/2LSB (B-Grade)
Unipolar or Bipolar Operation
Low Power: 775mW
Differential Input
Internal Hold Capacitor

APPLICATIONS

Computer Based Data Acquisition Systems
Wide Dynamic Range Measurement Systems
Test Equipment (ATE)
Analytic and Medical Instruments
Multi-Channel Systems With High/Low Level Signals

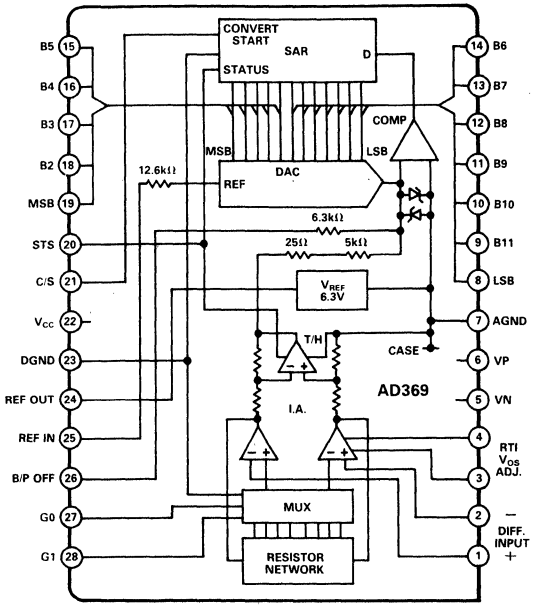
PRODUCT DESCRIPTION

The AD369 is a wide dynamic range data acquisition system IC which conditions and subsequently converts an analog signal to a 12-bit digital word. It utilizes hybrid technology to incorporate a programmable gain amplifier, a track-and-hold amplifier, and a 12-bit analog-to-digital converter into a 28-pin dual in-line package.

The software programmable gain amplifier (PGA) allows the user to choose full-scale voltage ranges of 10V, 1V, 100mV and 20mV. Signals of 5μV can be resolved in the G=500 mode, giving the AD369 a dynamic range of 126dB. Precision differential inputs provide the AD369 with an excellent common-mode rejection capability.

The track-and-hold amplifier (T/H) features excellent linearity, low noise and a fast acquisition time. The T/H has an internal hold capacitor.

AD369 FUNCTIONAL BLOCK DIAGRAM



The successive approximation analog-to-digital converter (ADC) features true 12-bit operation, with 0.012% max nonlinearity (B-grade). The ADC is guaranteed to have no missing codes within the temperature range of −25°C to +85°C. The user can select bipolar or unipolar operation to digitize both ac and dc input signals.

The AD369 provides a completely specified and tested function in a space saving 28-pin metal hermetic package for system designers with cost, space, and time constraints.

SPECIFICATIONS (typical @ +25°C, V_S = ±15V, +5V, R_{SPAN} = 63Ω and R(B/P) = 31Ω unless otherwise noted)

Parameter	AD369AM Grade Min	Typ	Max	AD369BM Grade Min	Typ	Max	Units
ANALOG INPUT							
Voltage Range, Unipolar (G = 1)	0		+10	*		*	V
Voltage Range, Bipolar (G = 1)	−5		+5	*		*	V
Common-Mode Voltage		12 − (V_{DIFF} × G/2)			*		V
Resistance		10^9			*		Ω
Capacitance		5			*		pF
Bias Current (I_B)		10	50		*	25	nA
I_B vs. Temperature		50			*		pA/°C
Input Offset Current (I_{OS})		2	20		*	10	nA
I_{OS} vs. Temperature		20			*		pA/°C
Noise Current (0.1 to 10Hz)		60			*		pA p-p
Output Offset Voltage (V_{OS})[1]		5 + 0.02 × G	25 + 0.2 × G		*	10 + 0.1 × G	mV
V_{OS} vs. Temperature		70 + 0.2 × G	300 + 2.0 × G		*	*	μV/°C
V_{OS} vs. Common-Mode Voltage[2]		60 + 0.5 × G	320 + 3.2 × G		*	150 + 1.5 × G	μV/V
V_{OS} vs. Supply Voltage[3]		100 + 1.0 × G	2300 + 10 × G		*	1000 + 4 × G	μV/V
Output Noise Voltage (rms)							
G = 1		250			*		μV
G = 10		260			*		μV
G = 100		340			*		μV
G = 500		600			*		μV
DIGITAL INPUTS[4]							
V_{IH}	3.0		V_{CC}	*		*	V
V_{IL}	0.0		0.8	*		*	V
I_{IH}, I_{IL}		0.01	1.0		*	*	μA
C/S Pulse Width	50			*			ns
DIGITAL OUTPUTS, 12-BIT PARALLEL							
V_{OH} @ I_{OH} = −40μA	3.6	5.0		*	*		V
V_{OL} @ I_{OL} = 1.6mA		0.2	0.4		*	*	V
SIGNAL DYNAMICS							
Conversion Time (t_C)		12	15		*	*	μs
t_C vs. Temperature		+20			*		ns/°C
System Throughput Rate[5]							
G = 1, 10			50			*	kHz
G = 100			50			*	kHz
G = 500			20			*	kHz
Gain Switching Time		1.5	2.0		*	*	μs
PGA Settling Time (to 1/2LSB)							
G = 1, 10		8	10		*	*	μs
G = 100		12	15		*	*	μs
G = 500		40	50		*	*	μs
Amplifier − 3dB Bandwidth							
G = 1		1000			*		kHz
G = 10		400			*		kHz
G = 100		150			*		kHz
G = 500		40			*		kHz
T/H Acquisition Time (t_{ACQ} to 1/2LSB)			3			*	μs
T/H Aperture Delay Time (t_{AP})		230	350		*	*	ns
t_{AP} vs. Temperature		+0.5			*		ns/°C
Aperture Jitter		1			*		ns
Feedthrough		25			*		μV/V
ACCURACY							
Integral Nonlinearity		0.30	0.75		*	0.5	LSB
Differential Nonlinearity (DNL)[6]		0.30	0.90		*	0.5	LSB
DNL at +85°C		0.4	1		0.4	0.8	LSB
Monotonic Temperature Range	−25		+85	*		*	°C
Total Gain Error @ G = 1		0.05	0.5		*	0.2	%
@ Other Gains Referred to G = 1		0.01	0.1		*	0.05	%
Gain vs. Temperature @ G = 1		3	30		*	*	ppm/°C
@ Other Gains Referred to G = 1		3	10		*	*	ppm/°C
Gain vs. Supply Voltage							
V_P ± 10%		10	30		*	*	ppm/%
V_N ± 10%		5	30		*	*	ppm/%
V_{CC} ± 10%		5	15		*	*	ppm/%

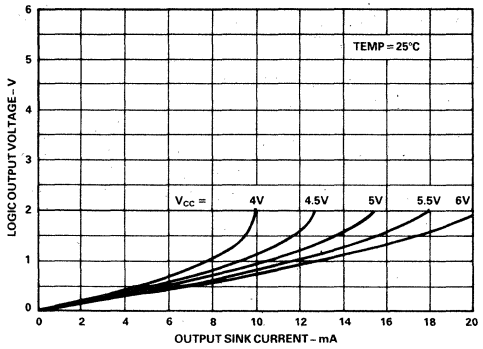
Parameter	AD369AM Grade Min	Typ	Max	AD369BM Grade Min	Typ	Max	Units
REFERENCE							
Voltage (V_{REF})	6.28	6.30	6.32	*	*	*	V
V_{REF} vs. Temperature			20			*	ppm/°C
Internal Resistance		2			*		Ω
External Load			0.5			*	mA
POWER REQUIREMENTS							
Positive Supply Range	+13.5	15	16.5	*	*	*	V
Negative Supply Range	−13.5	−15	−16.5	*	*	*	V
Logic Supply Range	4.5	5.0	5.5	*	*	*	V
Supply Current, V_{IN} = 10V, f_C = 50kHz							
+15V		20	25		*	*	mA
−15V	−35	−30		*	*		mA
+5V		5	10		*	*	mA
Power Consumption		775			*		mW
THERMAL RESISTANCE (J-A)		25			*		°C/W

NOTES
*Same specifications as AD369AM.
[1]Offset voltage applies to both bipolar and unipolar operating modes.
[2]V_{CM} = ±10V.
[3]V_S = ±10%.
[4]For digital inputs, pull-up resistors needed (typ 5kΩ) when interfacing with TTL/DTL logic.
[5]Assumes pipelining, i.e., signal is inputted to I.A. when T/H goes into hold mode, allowing voltage to settle concurrently with A/D conversion (see timing diagram).
[6]Includes T/H droop rate.
Specifications subject to change without notice.

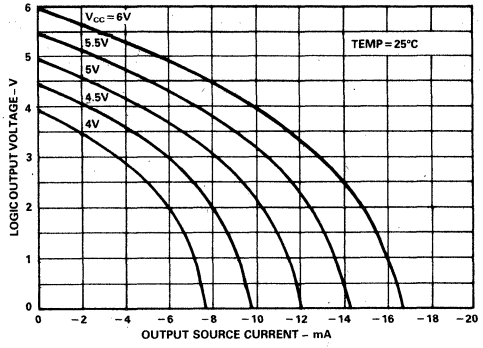
ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Positive Supply, V_P	−0.3	+17	V
Negative Supply, V_N	+0.3	−17	V
Digital-to-Analog Ground	−1	+1	V
Logic Supply	−0.3	+7	V
Analog Input (Either)	V_N	V_P	V
Analog Input Current	−20	+20	mA
Lead Soldering, 10 sec		+300	°C
Operating Temperature Range to Specifications	−25	+85	°C
Operating Temperature Range with Derated Specifications	−55	+125	°C
Storage Temperature	−65	+150	°C

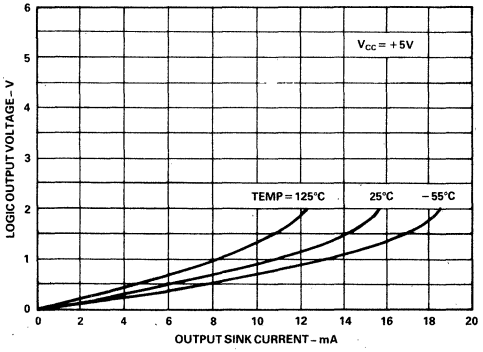
LOGIC OUTPUTS TYPICAL PERFORMANCE GRAPHS



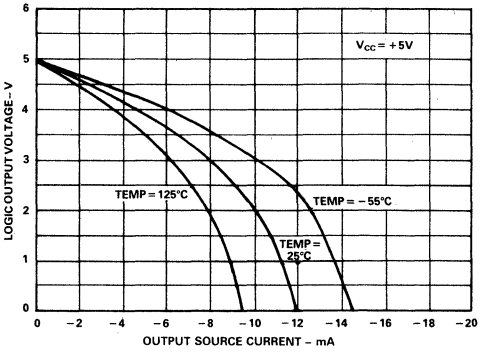
Logic Low Level Output Voltage vs. Sink Current



Logic High Level Output Voltage vs. Source Current

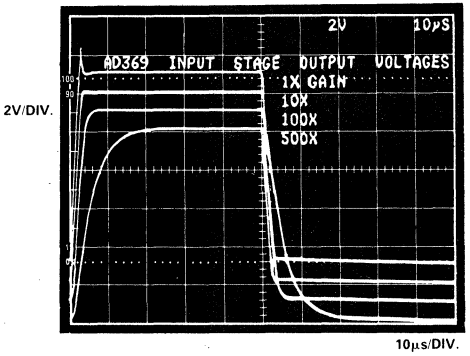


Logic Low Level Output Voltage vs. Sink Current

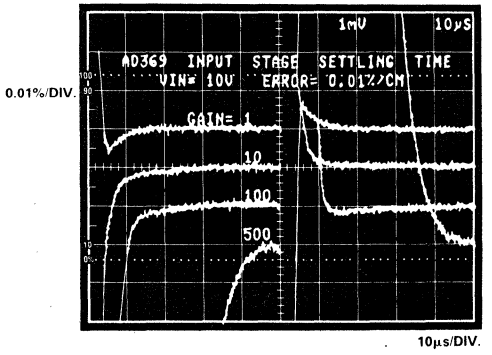


Logic High Level Output Voltage vs. Source Current

AMPLIFIER LARGE SIGNAL RESPONSE



AD369 Input Stage Output Voltage



AD369 Input Stage Settling Time

ANALOG INPUT

An analog multiplexer and resistor network form the gain switching circuit of the PGA. As shown in Table I, the user selects a gain according to the state of binary address inputs G0 and G1.

Also shown in the table is the input range data. The full-scale range of the DAS is 10V, and an LSB value is 4.88μV in the gain 500 mode; therefore, the dynamic range of the AD369 is 126dB.

The PGA uses a monolithic instrumentation amplifier, which is based on the classic three-op-amp approach. The differential analog input is amplified, according to gain selection, by two input op amps. The third amplifier, a unity gain subtractor, removes any common-mode signal and yields a single-ended output.

DATA CONVERSION

The track-and-hold amplifier is a monolithic device with an internal hold capacitor. It has an acquisition time of ≤3μs.

Input signals are digitized using a successive-approximation A/D converter. The rising (L to H) edge of the Convert Start pulse resets the internal flip-flops of the SAR. The falling (H to L) edge of the pulse initiates the conversion. After an aperture delay of 230ns, the track and hold amplifier goes into the hold mode, and the Status output goes High, indicating a conversion is in progress. Conversion time from the falling edge of the CS pulse is 15μs, maximum. A low output on the Status line indicates that the conversion is complete. The data at the output is valid at least 15ns before the Status goes low (see timing diagram). This gives sufficient setup time so that data may be latched to an external register on the falling edge of the Status pulse. The T/H amplifier returns to the tracking mode when the Status line goes low. Data is valid at the output until the next falling edge of a C/S pulse. After a maximum of 3μs acquisition time, a new C/S pulse may be issued to begin a new conversion. Timing diagrams are shown in Figure 1.

Figure 1a shows timing when a conversion sequence has first begun. All functions are being performed in series. This is the timing for the first data conversion, assuming a new gain must be selected.

The timing in Figure 1b assumes conversions are progressing continuously. After a conversion has been initiated by the falling edge of the C/S pulse, a new analog signal may be inputted to the DAS or a new gain may be selected. The figure shows that if a new gain is selected, no more than 2μs later, the new voltage begins settling at the PGA output. In the G = 500 mode, the determining factor for conversion speed is the amplifier settling time and, if necessary, the gain switching time. If the PGA gain is not switched, the conversion time for G = 500 becomes 50μs, maximum, and a minimum throughput rate of 20kHz can be achieved.

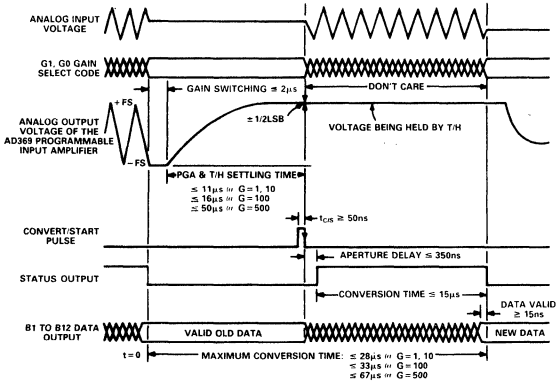


Figure 1a. AD369 Timing Diagram Without Pipelining

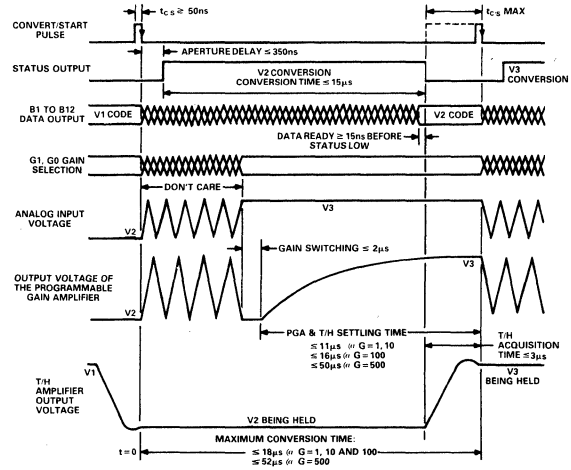


Figure 1b. AD369 Timing Diagram With Pipelining

Gain Code		Programmable Gain Amplifier	Analog Input Voltage Range				One Least Significant Bit (LSB) Value
G0	G1	Gain	Unipolar		Bipolar		
0	0	1	0	+10V	−5V	+5V	2.44mV
0	1	10	0	+1V	−0.5V	+0.5V	0.24mV
1	0	100	0	+100mV	−50mV	+50mV	24.4μV
1	1	500	0	+20mV	−10mV	+10mV	4.88μV

Table I. Input Voltage Range Selection

Using the AD369

CALIBRATING THE AD369 WITH TRIMPOTS

This is a calibration procedure which is implemented with potentiometers, resistors, and LEDs. The hardware can be incorporated on the board which utilizes the AD369 for convenient field calibration.

The ideal transfer function of the AD369 in Figure 2 shows that the output code steps up from all ones to all zeros as the analog input voltage increases from the minus full scale limit to the plus full scale limit. The purpose of the calibration is to put the first and last bit transitions where they belong; 1LSB above −FS and 1LSB below +FS respectively.

The transfer function shows that for each output code there is an associated quantization uncertainty of 1LSB. For a given code, there is an LSB wide range of possible analog input voltages. Only at the transition point between two adjacent codes is there a precise correlation between input voltage and digital output. This circumstance must be utilized in the calibration or the accuracy may be off by ±1/2LSB.

In reality, due to noise on the analog input, the transitions do not occur as sharply as illustrated in the figure. When changing codes, the output will toggle constantly while moving from one value to the next. The desired transition point is obtained when 50% of the time the output is above this point and 50% of the time the output is below it. This transition point may be observed on an oscilloscope. Another way to measure this 50% duty cycle is by using a light emitting diode (LED) as shown in Figure 3. The duty cycle is approximately 50% when the LED is about halfway between minimum and maximum brightness.

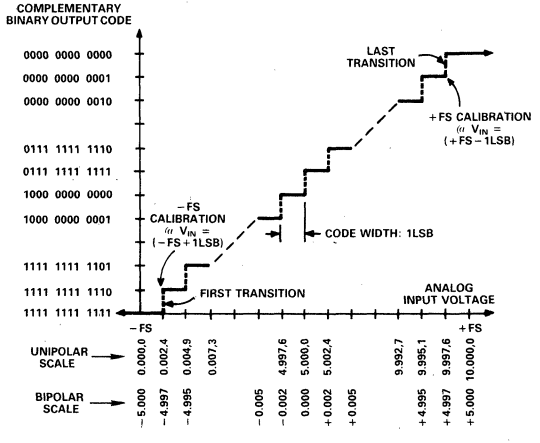


Figure 2. AD369 Transfer Function (G = 1)

UNIPOLAR MODE CALIBRATION

Figure 3 shows the AD369 in the unipolar mode of operation, with calibration hardware connected. The calibration begins with cancellation of the input stage offset by applying 0V to the input and manipulating R_{RTI} and R_{RTO} until the first transition occurs exactly at 0V, regardless of the amplifier gain. The next step in the calibration is to cancel the output stage offset by adjusting R_{RTO} to put the first transition at the proper input voltage of +1LSB. Finally, R_{SPAN} is adjusted and the last bit transition is put 1LSB below +FS.

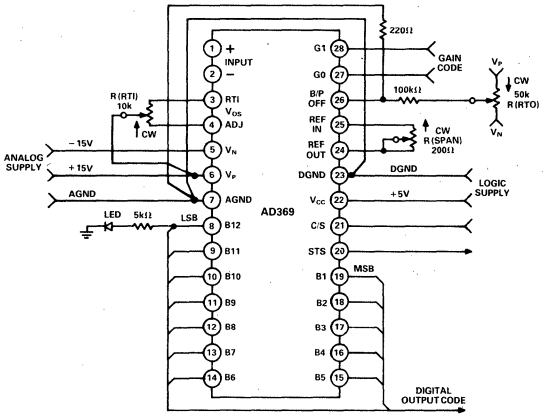


Figure 3. AD369 in the Unipolar Mode with RTI V_{OS}, RTO V_{OS} and Span Trimpots

Calibration steps for input stage offset voltage (V_{OS}) cancellation:

1. Connect the inputs to analog ground.
2. Set G = 500 and turn R_{RTI} all the way clockwise (CW). This shifts the transfer function to the right, causing the output code to be all ones. The LED will light up.
3. Now turn R_{RTI} counterclockwise (CCW) until the LED dims to half brightness. The first transition is now positioned at the V_{IN} = 0 line.
4. Switch to G = 1 and turn R_{RTO} all the way CW. This will cause the output code to be all ones again.
5. Turn R_{RTO} CCW until the LED dims; the first transition is at 0V again.
6. Switch the gain to G = 500, turn R_{RTI} CW just enough to assure an all ones code, then turn it CCW until the LED dims to half brightness.
7. Switch the gain back to one, turn R_{RTO} CW enough to assure an all ones code, then turn it CCW until the LED dims.
8. Repeat steps 5 and 6 until the LED brightness does not change when switching between G = 1 and G = 500. The input stage offset voltage is now zero.

Calibration steps for the output stage offset voltage (V_{OS}) cancellation:

1. Connect the inputs to a 2.44mV supply, as in Figure 4.
2. Set G = 1, turn R_{RTO} all the way CW, assuring an all ones output and lighting the LED.
3. Turn R_{RTO} CCW until the LED dims to half brightness. The first transition is now 1LSB above 0V.

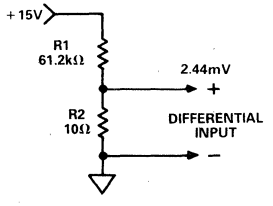


Figure 4. Input Connection for the R_{RTO} Calibration

Calibration steps for Gain Error (SPAN) cancellation:

1. Apply a precise 10V–2.44mV across the input of the AD369. A voltage divider as shown in Figure 5 can be employed; in conjunction with a precision voltmeter to verify an input of 9.997,56V.
2. Set G = 1, turn R_{SPAN} all the way CCW, assuring an output of all zeros.
3. Turn R_{SPAN} CW until the LED begins to light up (about half-brightness). At this point the last transition will be at +FS −1LSB.

The calibration in the unipolar mode is now complete.

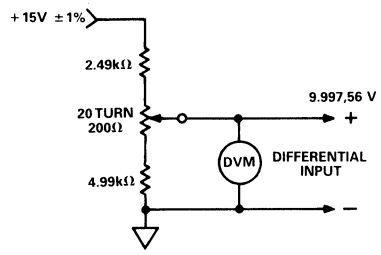


Figure 5. Input Connection for the R_{SPAN} Calibration

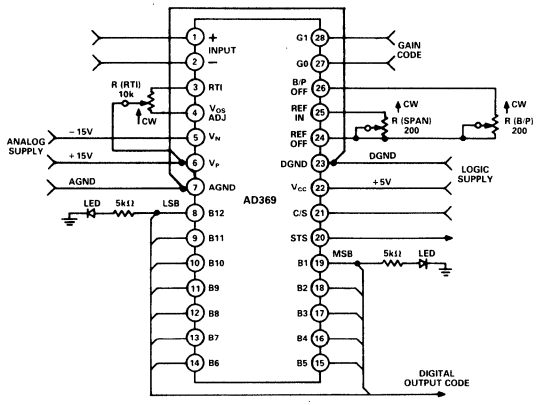


Figure 6. AD369 in the Bipolar Mode with Offset and Gain Trimpots

BIPOLAR MODE CALIBRATION

The AD369, with calibration hardware, is shown in Figure 6 for operation in the bipolar mode. The adjustments begin, as in the unipolar case, with the input stage V_{OS} cancellation. In this case however, the calibration is different because the 0V point is now at mid-scale; the MSB is used instead of the LSB. Next in the calibration is to adjust R_{RTO} and put the first LSB transition at an input voltage of −5V +1LSB. Last is the R_{SPAN} adjust to put the last bit transition 1LSB below +5V.

Input stage V_{OS} cancellation steps:

1. Connect the inputs to analog ground.
2. Select G = 500 and turn R_{RTI} until the MSB LED is at half-brightness.
3. Switch to G = 1 and adjust R_{RTO} until the LED is again at half-brightness.
4. Repeat steps 2. and 3. until the LED brightness does not change when gains are switched. This indicates that the input stage V_{OS} = 0V.

Output stage V_{OS} cancellation steps:

1. Set G = 1.
2. Connect the plus input to ground and the minus input to 4.997,56 volts using a voltage divider such as in Figure 7.
3. Turn R_{RTO} completely CW to assure an output code of all ones.
4. Now turn R_{RTO} CCW until the LSB LED dims to half-brightness. The first transition is now 1LSB above −FS.

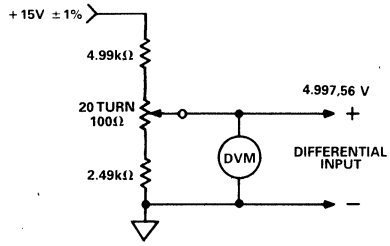


Figure 7. Voltage Divider to Derive RTO V_{OS} and Span Calibration Voltage

Gain Error cancellation steps:

1. Set G = 1.
2. Now connect the plus input to 4.997,56 Volts and the minus input to analog ground.
3. Turn R_{SPAN} completely CCW to assure an output code of all zeros.
4. Now turn R_{SPAN} CW until the LSB LED begins to light up. At this point the last bit transition will be at +FS −1LSB.

Calibration in the bipolar mode is now complete.

CALIBRATING THE AD369 WITHOUT TRIMPOTS

Figure 8 shows the AD369 in the unipolar mode with calibration hardware consisting of a Quad 8-Bit D/A Converter (AD7226) circuit instead of the previous trimpot configuration. The calibration procedure is basically the same as before except that instead of adjusting the potentiometers, three DACs are used to correct for offsets and gain error. Bipolar calibration may be accomplished by referring to Figure 6 and modifying Figure 8 accordingly.

This calibration routine has some excellent benefits in addition to the elimination of potentiometers. Dipswitches may be used initially to set the 8-bit word values needed for each connection; however, after the word values are determined, this data may be stored into a memory (i.e., RAM) for auto-calibration in the field. The entire calibration may be accomplished under microprocessor control. Temperature offsets may be cancelled by using a temperature sensor in conjunction with the microprocessor.

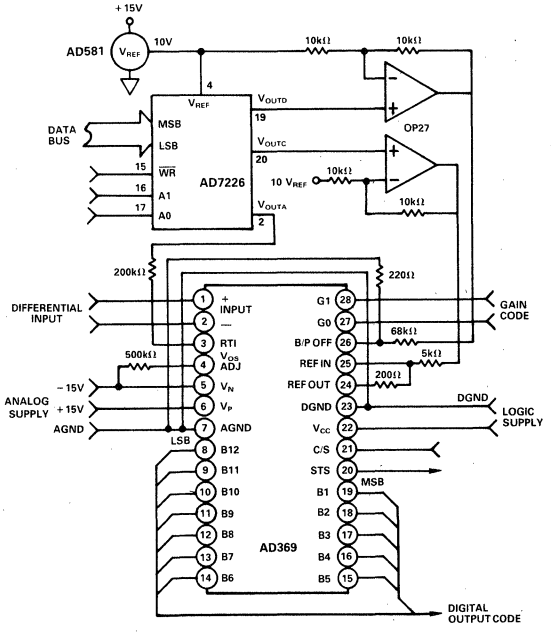


Figure 8. AD369 in the Unipolar Mode with D/A Circuit Replacing Trimpots

INPUT PROTECTION

There are two considerations when applying input protection for the PGA: 1) that maximum input current must be limited to less than 20mA and 2) that input voltages must not exceed the supplies. Outside the linear operating range, the input impedance of the AD369 becomes low and nonlinear due to the input transistors going into saturation. The graph in Figure 9 illustrates the input current vs. differential input voltage relationship without input protection.

Resistors of 1kΩ in series with each input would keep the currents within safe limits for input voltages in the range of $V_P = +15V$ to $V_N = -15V$. Figure 10 shows the external components necessary to protect the AD369 under all overload conditions at any gain. The diodes to the supplies are necessary if input voltages outside of the range of the supplies are encountered.

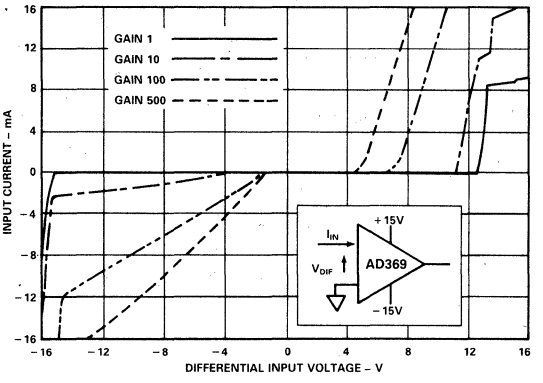


Figure 9. Input Current vs. Differential Input Voltage Without Input Protection

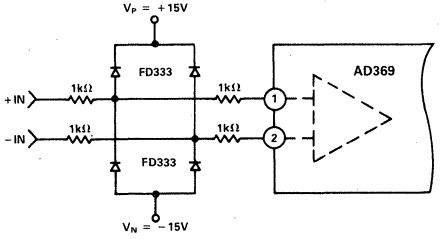


Figure 10. Input Protection Circuit for AD369

The equivalent noise resistance of the AD369 input stage is only 1kΩ. Input protection resistors, however, will quickly degrade the excellent noise performance of the DAS. To reduce the noise encountered with added resistors, FETs may be used to limit the input current. FETs, such as the 2N4416, with low I_{DSS} and low on-resistance should be used. Figure 11 shows the protection circuit and Figure 12 shows the input current vs. the differential input voltage with the FET protection circuit. The 20kΩ resistor is put in series with the gate to limit the "reverse" I_{DSS} current and does not add to the noise.

The above input protection circuits also protect the AD369 in case there is a voltage applied to the input while the supplies are shut off.

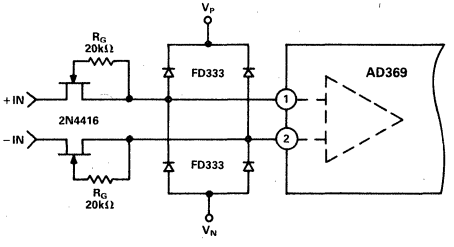


Figure 11. Low Noise Input Protection Circuit for AD369

If using multiplexers, proper device selection can provide AD369 input protection. Some MUXes limit the maximum current as well as the maximum output voltage to safe levels. Keep in mind that the on resistance of the MUX will add to the input stage noise.

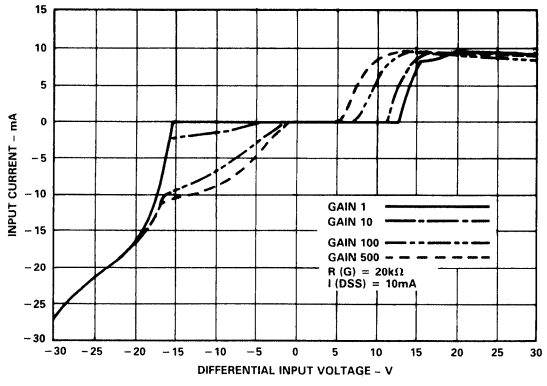


Figure 12. AD369 Input Protection with 2N4416 FETs and FD333 Clamping Diodes

GROUND RETURNS FOR INPUT BIAS CURRENTS

There must be a direct return path for the input bias currents of the PGA input transistors; otherwise, they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying floating input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 13.

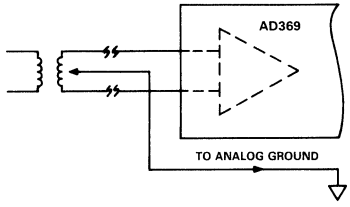


Figure 13a. Ground Returns for Bias Currents with Transformer Coupled Input

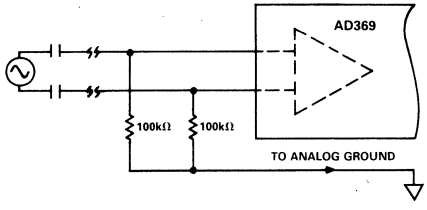


Figure 13b. Ground Returns for Bias Currents with ac Coupled Inputs

GROUND CONNECTIONS

The digital and analog ground pins of the AD369 should be tied together as close to the package as possible to avoid noise coupling from the digital ground to the analog circuit. When an application calls for separate grounding entirely, a 0.1μF capacitor should be connected between the AGND and DGND pins to filter out any noise.

POWER SUPPLY DECOUPLING

Each of the AD369 supply terminals should be capacitively decoupled as close to the IC as possible. A 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are decoupled to the analog ground pin and the Logic supply is decoupled to the digital ground pin.

TRACK-AND-HOLD ERRORS

The aperture delay time is the time required for the track-and-hold amplifier to switch from track to hold. Since this is effectively a constant, it may be tuned out by advancing the track-to-hold command with respect to the input signal.

Unlike the aperture delay time, aperture jitter is a true error source and must be considered. Aperture jitter is a result of noise within the switching network. It causes variations in the value of the analog input being held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input and may limit the signal bandwidth. The aperture jitter of the T/H in the AD369, however, is small enough that the instrumentation amplifier will limit the signal frequency well below the frequency at which the jitter error would be of concern.

Droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major contributors are switch leakage current and bias current. This dV_{OUT}/dT is equal to the ratio of the total leakage current, I_l to the hold capacitance, C_H. The droop rate of the T/H in the AD369 is included in the differential nonlinearity specification.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change. Care should be taken to assure that both input lines are balanced with regard to parasitic capacitances and source resistances; otherwise, the excellent common-mode rejection of the AD369 will be degraded.

ERRORS DUE TO BANDWIDTH LIMITATIONS OF THE AD369

When using the AD369 to digitize sine-wave signals, it is important to know the frequency at which the system response roll-off will cause an error of 1/2LSB.

The ratio of output to input voltage for the instrumentation amplifier of the AD369 is:

$$|V_O/V_I| = G/|(1+jf/f_a)| = G/[1+(f/f_a)^2]^{0.5}$$

where f_a equals the −3dB bandwidth and a single-pole roll-off is assumed.

It can be shown that the V_O/V_I ratio will have an error of 1/2LSB for a 12-bit A/D converter when:

$$f(1/2LSB) = f_a/\sqrt{2^{12}} = f_a/64.$$

The instrumentation amplifier will have reached the limit of 12-bit precision for signal frequencies of $f_a/64$. The frequency can be doubled at the expense of two bits of accuracy.

The frequency at which the amplitude of a 10V p-p sine wave is reduced by one half of an LSB is typically 10kHz, 3.5kHz, 1.7kHz, and 0.5kHz at gains of 1, 10, 100, and 500 respectively.

NOISE CONSIDERATIONS

Assuming normally distributed or white noise, the rms noise voltage E_n of a system is a function of its noise bandwidth BW_N. The correlation between −3dB bandwidth (BW) and BW_N is dependant upon the frequency response of the system under consideration.[1] For a 6dB/octave filter, the ratio is $\pi/2 = 1.57$. For a "brick wall" filter it is one. The noise correlation is simply: $E_N = e_N\sqrt{BW_N}$, where e_N is the noise density ($nV/\sqrt{Hz}$).

The noise of the input signal must also be added to the noise of the DAS. Again, in calculating the rms noise contribution of the signal, the BW_N of the source must be considered. If not filter limited before the AD369 input, the BW_N of the PGA, as stated above, must be used, which is about $\pi/2$ times its −3dB bandwidth.

Input protection resistors will also contribute to the total system noise. The rms noise voltage of a 1kΩ resistor over a noise bandwidth of 1Hz is 4nV. So, the noise voltage of a resistor, R(kΩ) and a noise bandwidth, BW_N(Hz) is: $E_N(R) = 4nV\sqrt{R \times BW_N}$.

The total system rms noise is given by the equation:

$$E_N(system) = \sqrt{E_N(AD369)^2 + [G \times E_N(R_{IN})]^2 + [G \times E_N(sig)]^2}$$

Once the system rms noise value is known, the probability of the peak-to-peak value of the noise exceeding an LSB is given in Table II.

LSB/E_N	Probability of Noise Exceeding 1LSB
1.0	62.0%
2.0	32.0%
3.0	13.0%
4.0	4.6%
5.0	1.2%
5.15	1.0%
6.0	0.27%
6.6	0.10%

Table II.

[1]See "Low Noise Electronic Design," by C. D. Motchenbacher, F. C. Fitchen.

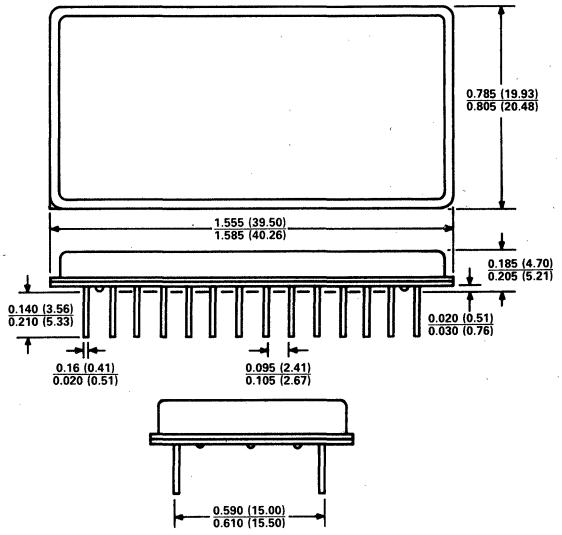
OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a voltage known as the "Seebeck" or thermocouple emf is generated when the two junctions are at different temperatures. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV/°C). This means that care must be taken to insure that all connections in the input circuit of the AD369 remain isothermal. In addition, the user should also avoid air currents over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise.

The base emitter junction of an input transistor can rectify out-of-band signals (i.e., RF interference). These rectified voltages act as small dc offset errors. In the case of a resistive transducer, a small capacitor (e.g. 150pF) across the input working against the internal resistance of the transducer may suffice to provide an RC filter without affecting system bandwidth. Again, every effort should be made to match the capacitance at pins 1 and 2, to preserve CMR.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



1MHz µC Compatible 12-Bit ADC

AD375

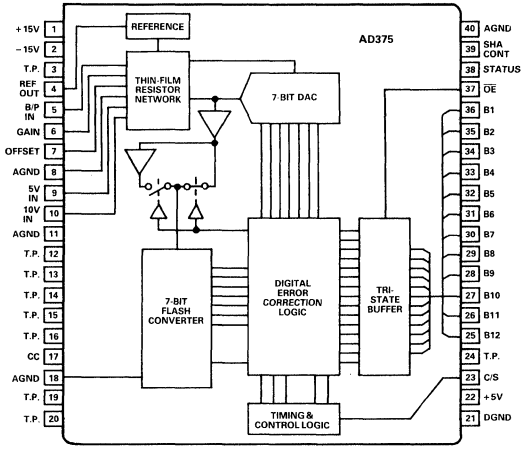
FEATURES

- Guaranteed 12-Bit No Missing Codes Over Temperature
- 1MHz Throughput Rate
- Small 40-Pin Hermetic Ceramic Package
- T/H Control Line
- Gain Accuracy 0.25%
- Four Pin-Programmable Input Ranges
- Tri-State Latched Output Data

APPLICATIONS

- High-Speed Measurement System
- Test Equipment (ATE)
- Board Level DAS for Computers
- Analytic and Medical Instruments
- Multichannel, High-Speed Systems
- Signal Processing
- Vibration Analysis
- Image Enhancement Systems
- Computer Aided Tomography and Magnetic Resonance Systems

AD375 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD375 is a small, 12-bit linear, 1MHz throughput analog-to-digital converter hybrid. Packaged in a 40-pin hermetic DIP, the AD375 provides a completely specified and tested ADC in a space-saving hybrid as an economical solution for system designers with space and time constraints. Designed for applications requiring a 1MHz throughput rate, the AD375 is designed with state-of-the-art integrated circuits. Laser trimmed for accuracy and manufactured on a modern certified high quality, hybrid assembly line the AD375 is a state-of-the-art microcircuit.

The AD375 features 12-bit no missing code performance over 0 to +70°C (ambient temperature, not case temperature). It is 100% tested for linearity, missing codes, offset and gain errors.

Because the flash converter is buffered in this design, an expensive external precision buffer is not required as in other flash designs. The T/H control line controls an external track-and-hold amplifier to take maximum advantage of the AD375 architecture. The external T/H is automatically sent back to track mode during the AD375 digital error correction cycle. No additional active components are needed, only power, an analog input signal, four decoupling caps, and a convert command is needed for operation.

The input range can be selected by connecting the input pin configuration required for the span desired. The digital output is updated after the status output transitions to the not busy state and is valid until the next conversion update takes place. All digital inputs and outputs are TTL compatible. Gain and offset errors may be externally trimmed to zero with optional trim adjustments for better accuracy. Linearity is specified using the more conservative end point linearity method. The AD375 is the superior part for new designs today.

ADC FUNCTIONAL DESCRIPTION

The AD375 uses a two stage flash technique. It is comprised of a 7-bit flash converter, a 7-bit D/A converter (DAC), a high-speed amplifier, switches and digital logic which handles timing and error correction. The analog input is digitized to 7-bit resolution. The digital output of the flash converter drives a 12-bit accurate D/A converter. The analog output of the DAC is subtracted from the analog input signal and the difference is multiplied by a gain factor of 32 (2^5).

The scaled difference signal is then digitized by the flash converter again to 7-bit resolution. This digital output is fed into the error correction logic along with the initial 7-bits of digital data to produce a 12-bit accurate digital output.

PRELIMINARY TECHNICAL DATA

SPECIFICATIONS (typical at +25°C and V_S = ±15V, +5V unless otherwise noted)

Parameter	Min	Typ	Max	Units
ANALOG INPUTS				
Impedance (10V FSR Span)		5k		Ω
(5V FSR Span)		2.5k		Ω
Input Ranges				
Bipolar		±2.5, 5		V
Unipolar		0 to 5, 10		V
DIGITAL INPUTS				
V_{INH}	2.4		5.0	V
V_{INL}	–		0.8	V
I_{INH}			20	μA
I_{INL}			0.4	mA
Convert/Start Pulse Width	50			ns
DYNAMICS				
Missing Codes @ 1MHz Rate		None	None	
Conversion Time			1000	ns
Delay, Falling Edge of Status to Data Valid			±10	ns
Delay, Falling Edge of Enable to Data Valid[1]			60	ns
ACCURACY @ +25°C				
Integral Nonlinearity		1/4	1	LSB
Diferential Nonlinearity		1/2	1	LSB
Gain		0.05		% FSR
Unipolar Offset		0.05		% FSR
Bipolar Offset		0.05		% FSR
DRIFT @ +70°C				
Integral Nonlineary Over Temperature		1/2	1	LSB
Gain Error Over Temperature		0.10		% FSR
Gain T.C.		25		ppm/°C
Unipolar Offset Over Temperature		0.10		% FSR
Unipolar T.C.		5		ppm/°C
Bipolar Offset Error Over Temperature		0.10		% FSR
Bipolar Offset T.C.		7		ppm/°C
Conversion Time Over Temperature			1000	ns
No-Missing-Code Temperature Range	0		+70	°C
DIGITAL OUTPUTS				
V_{OL} @ 1.6mA		0.4	0.8	V
V_{OH} @ −80μA	2.0	3.5		V
Unipolar Output Code		Straight Binary		
Bipolar Output Code		Offset Binary		
POWER REQUIREMENTS				
Positive Supply Range	+14.5	+15	+15.5	V
Negative Supply Range	−14.5	−15	−15.5	V
Logic Supply Range	4.75	5.0	5.25	V
Quiescent Current				
+15V		53	65	mA
−15V		83	95	mA
+5V		93	120	mA
Power Consumption		2.3	2.7	W
ABSOLUTE MAXIMUM RATINGS				
Positive Supply	−0.3		+18	V
Negative Supply	+0.3		−18	V
Logic Supply	−0.5		+7	V
Digital Inputs	−0.5		5.5	V
Analog Input	−15		+15	V
Analog Input Current	−10		+10	mA
Lead Soldering, 10 sec			+300	°C
Operating Temperature Range to Specification	0		+70	°C
Storage Temperature	−65		+150	°C
PACKAGE		40 Pin Double-DIP		

NOTE
[1]Bus access time.
Specifications subject to change without notice.

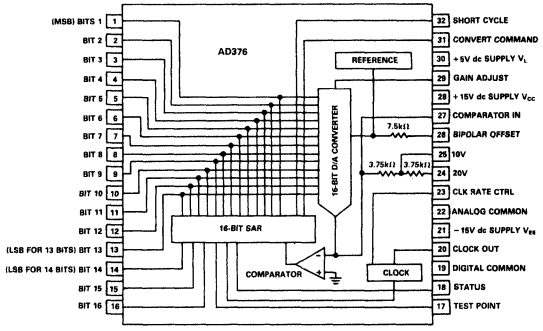
Complete High Speed 16-Bit A/D Converter

AD376

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits Over Temperature
Fast Conversion – 15μs (14 Bit)
Short Cycle Capability
Parallel Outputs
Low Power: 1100mW Typical
Industry Standard Pin Out
Available to MIL-STD-883

AD376 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD376 is a high resolution 16-bit hybrid IC analog-to-digital converter including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin metal DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR AD376KM (TM), and maximum 14-bit conversion time of 15μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD376 provides data in parallel form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD376 is excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multi-channel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD376 provides 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and S grades) at 25°C.
2. The AD376TM features guaranteed no missing code performance (14 bits) over the −55°C to +125°C temperature range.
3. Conversion time is 13.5μs typical to 14 bits with short cycle capability.
4. Two binary codes are available on the AD376 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting pin 1 (MSB).
5. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD376JM	AD376KM	AD376SM[1]	AD376TM[1]	Units
RESOLUTION	16 (max)	*	*	*	Bits
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±2.5, ±5, ±10	*	*	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	*	*	Volts
Impedance (Direct Input)					
0 to +5V, ±2.5V	1.88	*	*	*	kΩ
0 to +10V, ±5.0V	3.75	*	*	*	kΩ
0 to +20V, ±10V	7.50	*	*	*	kΩ
DIGITAL INPUTS[2]					
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion				
Logic Loading	1	*	*	*	LS TTL Load
TRANSFER CHARACTERISTICS[3]					
ACCURACY					
Gain Error	±0.05[4] (±0.2 max)	*	*	*	%
Offset Error					
Unipolar	±0.05[4] (±0.1 max)	*	*	*	% of FSR[5]
Bipolar	±0.05[4] (±0.2 max)	*	*	*	% of FSR
Linearity Error (max)	±0.006	±0.003	*	**	% of FSR
Inherent Quantization Error	±1/2	*	*	*	LSB
Differential Linearity Error	±0.003	*	*	*	% of FSR
3σ Noise at Transitions (pk-pk)	0.001 (0.003 max)[8]	*	*	*	% of FSR
POWER SUPPLY SENSITIVITY					
±15V dc (±0.75V)	0.001	*	*	*	% of FSR/% ΔV_S
+5V dc (±0.25V)	0.001	*	*	*	% of FSR/% ΔV_S
CONVERSION TIME[7]					
12 Bits	11.5 (13 max)	*	*	*	µs
14 Bits	13.5 (15 max)	*	*	*	µs
16 Bits	15.5 (17 max)	*	*	*	µs
WARM-UP TIME	1 minute	*	*	*	Minutes
DRIFT[8]					
Gain	±15 (max)	±5 (±15 max)	*	**	ppm/°C
Offset					
Unipolar	±2 (±4 max)	±2 (±4 max)	*	**	ppm of FSR/°C
Bipolar	±10 (max)	±3 (±10 max)	*	**	ppm of FSR/°C
Linearity	±2 (3 max)	±0.3 (2 max)	*	**	ppm of FSR/°C
Guaranteed No Missing Code					
Temperature Range[9]	0 to 70 (13 bits)	0 to 70 (14 bits)	−55 to +125 (13 Bits)	−55 to +125 (14 Bits)	°C
DIGITAL OUTPUT[2]					
(All Codes Complementary)					
Parallel					
Output Codes[10]					
Unipolar	CSB	*	*	*	
Bipolar	COB, CTC[11]	*	*	*	
Output Drive	2	*	*	*	TTL Loads
Status		Logic "1" During Conversion			
Status Output Drive	2 (max)	*	*	*	TTL Loads
Internal Clock[6]					
Clock Output Drive	2 (max)	*	*	*	TTL Loads
Frequency	1040	*	*	*	kHz
POWER SUPPLY REQUIREMENTS					
Power Consumption	1100	*	*	*	mW
Rated Voltage, Analog	±15 ±0.5 (max)	*	*	*	V dc
Rated Voltage, Digital	+5 ±0.25 (max)	*	*	*	V dc
Supply Drain +15V dc	+30	*	*	*	mA
Supply Drain −15V dc	−23	*			mA
Supply Drain +5V dc	+55	*			mA
TEMPERATURE RANGE					
Specification	0 to +70	*	−55 to +125	−55 to +125	°C
Operating	−25 to +85	*	–	–	°C
Storage	−55 to +125	*	−65 to +150	−65 to +150	°C

NOTES

[1]AD376 S and T grades are available to MIL-STD-883, Method 5008, Class B. See Analog Devices Military Products Databook for proper part number and detail specifications.

[2]Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.

[3]Tested on ±10V and 0 to +10V ranges.

[4]Adjustable to zero.

[5]Full Scale Range.

[6]With pin 23, clock rate controls tied to digital ground.

[7]Conversion time may be shortened with "Short Cycle" set for lower resolution.

[8]Guaranteed but not 100% production tested.

[9]For definition of "No Missing Codes", refer to Theory of Operation.

[10]CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Two's Complement.

[11]CTC coding obtained by inverting MSB (Pin 1).

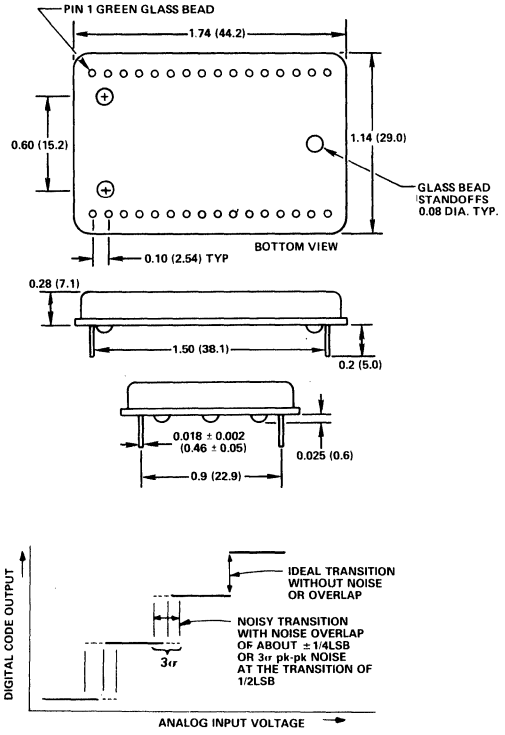
*Specifications same as AD376JM.

**Specifications same as AD376KM.

Specifications subject to change without notice.

OUTLINE DIMENSIONS

(Dimensions shown in inches and (mm).



Transition Noise Definition Based on Dynamic Cross Plot

ORDERING GUIDE

Model	Max Linearity Error	Temperature Range
AD376JM	0.006% FSR	0 to +70°C
AD376KM	0.003% FSR	0 to +70°C
AD376SM	0.006% FSR	−55°C to +125°C
AD376TM	0.003% FSR	−55°C to +125°C
AC1H72	Two 16-pin strip sockets	

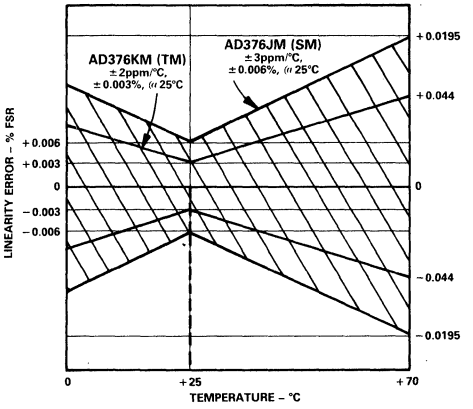


Figure 1. Linearity Error vs. Temperature

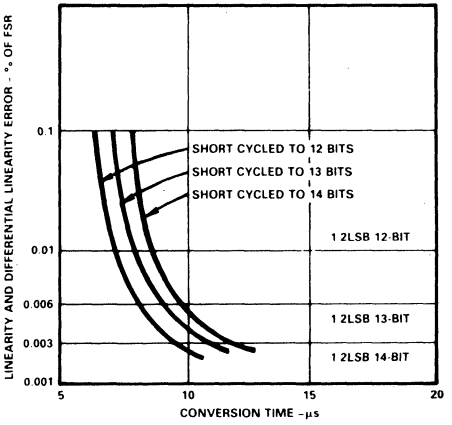


Figure 2. AD376 Nonlinearity vs. Conversion Time

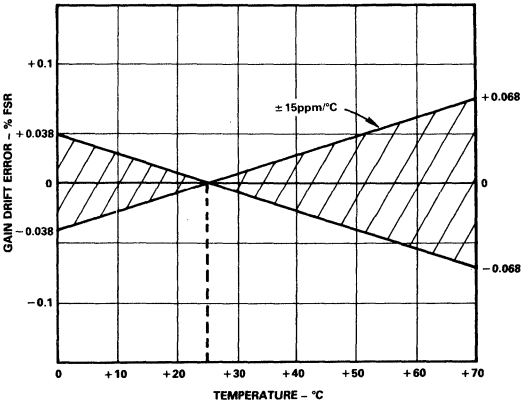


Figure 3. AD376 Gain Drift Error vs. Temperature

THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 5 and 7. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD376 is specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

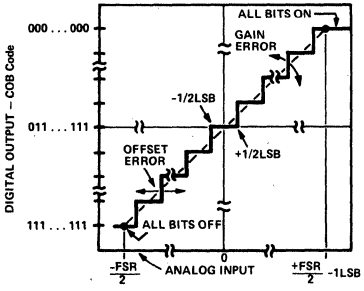


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD376 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 300kΩ resistor to the gain adjust pin 29 as shown in Figure 5.

If no external trim adjustment is desired, pins 27 (offset adj) and pin 29 (gain adj) may be left open.

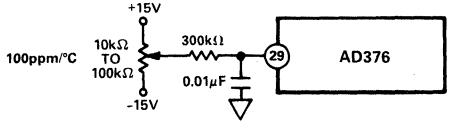
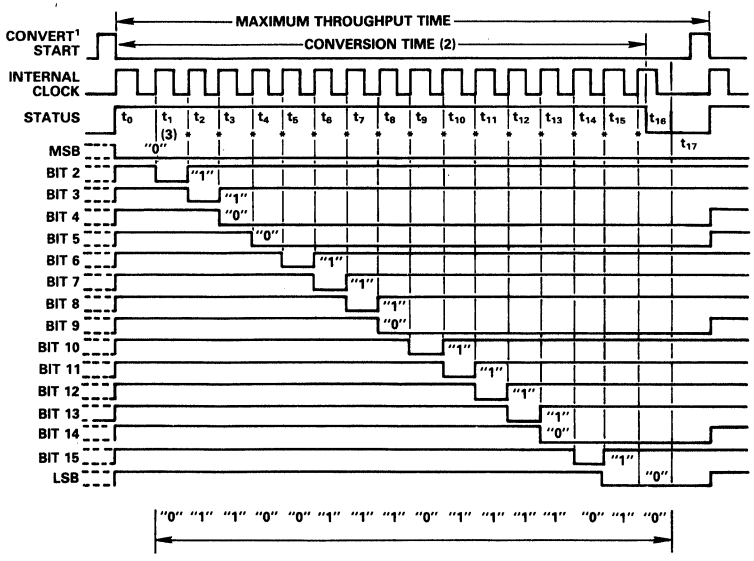


Figure 5. Gain Adjustment Circuit (±0.2% FSR)

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 27 for all ranges. As shown in Figure 7, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than



NOTES:
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 15μs FOR 14 BITS AND 14μs FOR 13 BITS (MAX).
3. MSB DECISION.
4. CLOCK REMAINS LOW AFTER LAST BIT DECISION.

Figure 6. Timing Diagram (Binary Code 0110011101110110)

$\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

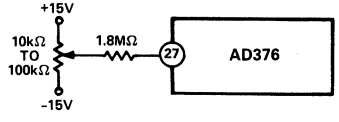


Figure 7. Offset Adjustment Circuit (±0.3% FSR)

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 8.

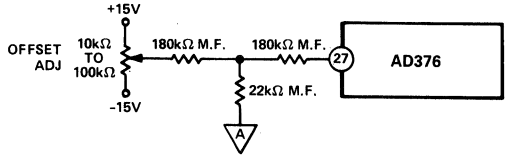


Figure 8. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to pin 27 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 27 is quite sensitive to external noise pick-up and should be guarded by analog common).

DIGITAL OUTPUT DATA

Parallel data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data outputs change state on positive-going clock edges.

Short Cycle Input: A Short Cycle Input, pin 32, permits the timing cycle shown in Figure 6 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, pin 32 is connected to Bit 11 output pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (timing diagram of Figure 6). Short cycle connections and associated 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I, for a 933kHz clock.

Resolution Bits	Resolution (%FSR)	Maximum Conversion Time (μs)	Status Flag Reset	Connect Short Cycle Pin 32 to Pin:
16	0.0015	17.1	t_{16}	N/C (Open)
15	0.003	16.1	t_{15}	16
14	0.006	15.0	t_{14}	15
13	0.012	13.9	t_{13}	14
12	0.024	12.9	t_{12}	13
10	0.100	10.7	t_{10}	11
8	0.390	8.6	t_8	9

Table I. Short Cycle Connections

INPUT SCALING

The AD376 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

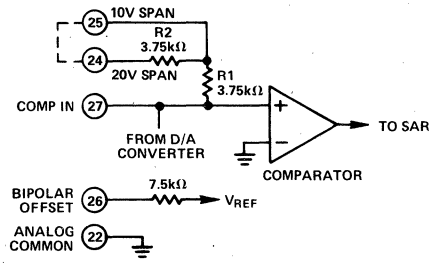


Figure 9. AD376 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Open	25
0V to +20V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and should be guarded by analog common.

Table II. AD376 Input Scaling Connections

Code Under Test			Low Side Transition Values				
MSB	LSB	Range	±10V	±5V	±2.5V	0 to +10V	0 to +5V
000 . . . 000*		+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111		Mid Scale	0-1/2LSB	0-1/2LSB	0-1/2LSB	+5V-1/2LSB	+2.5V-1/2LSB
111 . . . 110		− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Two's Complement – achieved by using an inverter to complement the most significant bit to produce $\overline{MSB}$.
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

CALIBRATION (14-Bit Resolution Examples)

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figure 5 and 7, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to $+1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = +9.9987V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to +10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset

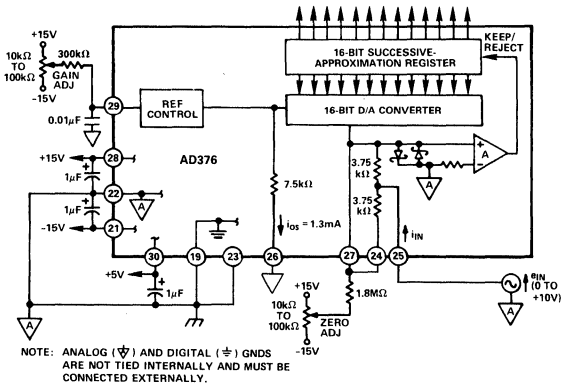


Figure 10. Analog and Power Connections for Unipolar 0 to +10V Input Range

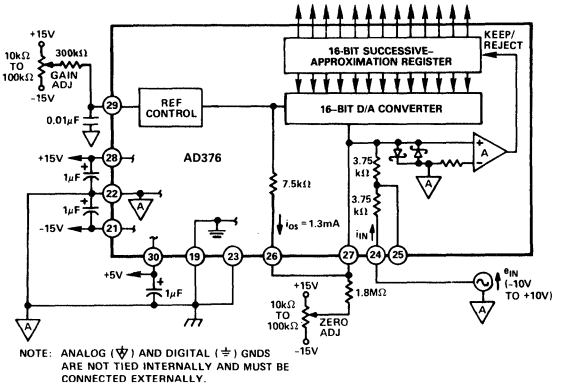


Figure 11. Analog and Power Connections for Bipolar +10V to +10V Input Range

binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in *"Analog-Digital Conversion Handbook"*, edited by D. H. Sheingold, Prentice-Hall, Inc., 1986.

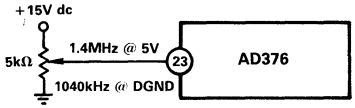


Figure 12. Clock Rate Control Circuit

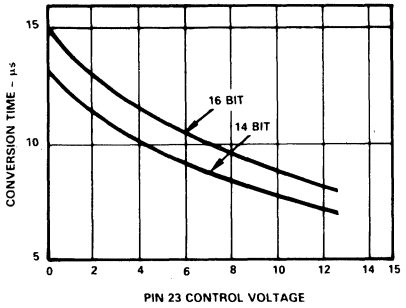


Figure 13. Converstion Time vs. Control Voltage

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (pins 19 and 22) must be tied together at one point for the AD376 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD376. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD376 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD376 supply terminals should be capacitively decoupled as close to the AD376 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal case is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the case. Glass beads standoff on the bottom will prevent shorting to board circuitry beneath the unit.

CLOCK RATE CONTROL

The AD376 may be operated at faster conversion times by connecting the Clock Rate Control (pin 23) to an external multiturn trim potentiometer (TCR <100ppm/°C) as shown in Figures 12 & 13. The integral linearity and differential linearity errors will vary with speed as shown in Figure 2.

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The AD389 is a companion T/H designed for use with the AD376 family. The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input which is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{(\text{Full Scale Voltage})\ (2^{-N})}{(\text{Full Scale Voltage})\ (2\pi)\ (\text{Aperture Jitter})}$$

For an application with a 14-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-14}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 24\text{kHz}$$

For an application with a 12-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-12}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 97\text{kHz}$$

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 15μs 14-bit A/D converter, the maximum droop rate will be 610μV/15μs or 40.7μV/μs during the 15μs conversion period.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects.

The linearity error should be less than 1LSB over the transfer function,as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the AD376 used with a companion AD389 T/H offers high accuracy sampling in high precision applications.

Spec	14 Bit	16 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.6	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	1.26	30	V/μs
Feedthrough (1LSB max)	−84.3	−96.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	10.2	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	3.0	0.1	μV/μs
Acquisition Time (to ±1LSB max) for 20kHz Signal w/15μs ADC	10	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−96.3	−86	dB
Gain Temperature Coefficient (max) for ±10°C Ambient Operation	6.1	1.5	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.3	0.1	mV
Linearity Error (max) 1LSB	±0.0061	0.0015	0.003	%FSR

Table V. T/H Amplifier Requirements vs. AD389 Specs

AD389 in Combination With an	Throughput Rate	Input Frequency Range	Acquisition Time & T/H Settling Time & A/D Conversion Time
AD376JM (13 bit)	48.8kHz	dc to 24.4kHz	20.5μs
AD376KM (14 bit)	52.6kHz	dc to 26.3kHz	23.0μs

Table VI. T/H & ADC Combinations and Maximum Throughput Rate

ANALOG DEVICES

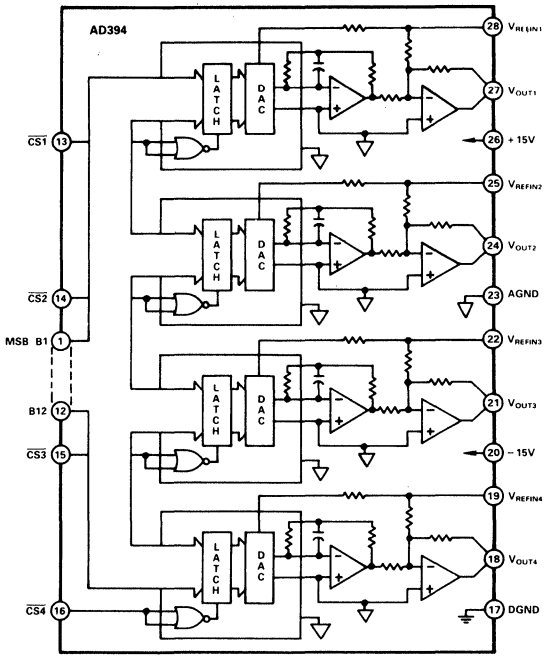
μP Compatible Multiplying Quad 12-Bit D/A Converter

AD394/AD395

FEATURES

Four Complete 12-Bit CMOS DACs with Buffer Registers
Linearity Error ±1/2LSB T_{min}-T_{max} (AD394, AD395K,T)
Factory-Trimmed Gain and Offset
Precision Output Amplifiers for V_{OUT}
Full Four Quadrant Multiplication per DAC
Monotonicity Guaranteed Over Full Temperature Range
Fast Settling: 15μs Max to ±1/2LSB
Available to MIL-STD-883 (See ADI Military Catalog)

AD394 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD394 and AD395 contain four 12-bit, high-speed, low power, voltage output multiplying digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit CMOS DAC chip which reduces chip count and provides high reliability. The AD394 and AD395 both are ideal for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

Both the AD394 and the AD395 are laser-trimmed to ±1/2LSB max differential and integral linearity (AD394, AD395K,T) and full scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with a single 12-bit wide word. The 12-bit parallel digital input interfaces to most 12- and 16-bit bus systems.

The AD394 outputs (V_{REFIN} = +10V) provide a ±10V bipolar output range with positive-true offset binary input coding. The AD395 outputs (V_{REFIN} = −10V) provide a 0V to +10V unipolar output range with straight binary input coding.

Both the AD394 and the AD395 are packaged in a 28-lead metal package and are available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD394, AD395 offer a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by both the AD394 and the AD395.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Two or four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DAC's reference (V_{REFIN}).
9. Both the AD394S,TD and AD395S,TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD394JM/SM[1] AD395JM/SM MIN	TYP	MAX	AD394KM/TM[1] AD395KM/TM MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			12			12	Bits
OUTPUT							
Voltage Range[3]							
AD394		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
AD395		0V to $-(V_{REFIN})$			0V to $-(V_{REFIN})$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero (AD394)		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ± 1/2LSB)							
V_{REFIN} = +10V, Change All Digital							
Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step,							
All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]							
AD395		5			5		mV p-p
AD394		See Figure 1			See Figure 1		
Digital-to-Analog Glitch Impulse[7]		250			250		nV sec
Crosstalk							
Digital Input (Static)[8]		0.1			0.1		LSB
Reference[9]		2.0			2.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	22		20	22	mA
$-V_S$		18	28		18	28	mA
Power Dissipation		570	750		570	750	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES

[1]AD394 and AD395 S and T grades are available to MIL-STD-883, Method 5008, Class B. See Analog Devices Military Catalog (1985) for proper part number and detail specification.

[2]Timing specifications appear in Table IV and Figure 5.

[3]Code tables and graphs appear on Theory of Operation page.

[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.

[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.

[6]For AD395 (unipolar), DAC register loaded with 0000 0000 0000, V_{REFIN} = 20V p-p, 10kHz sinewave. For AD394 (bipolar), V_{REFIN} = 20V p-p, 60 and 400Hz.

[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.

[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.

[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.

[10]The AD394 and the AD395 can be used with supply voltages as low as ±11.4V, Figure 10.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to DGND . . . . . −0.3V to +17V
$-V_S$ to DGND . . . . . +0.3V to −17V
Digital Inputs (Pins 1-16) to DGND . . . . . −0.3V to +7V
V_{REFIN} to DGND . . . . . ±25V
AGND to DGND . . . . . ±0.6V
Analog Outputs (Pins 18, 21, 24, 27)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stess rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

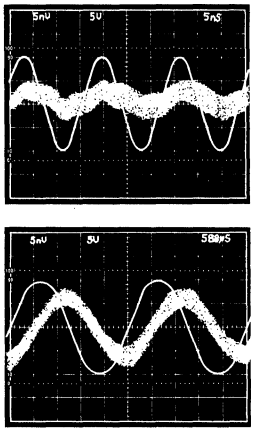


Figure 1. AD394 Feedthrough V_{REFIN} = 60Hz (top photo) and 400Hz (bottom photo) Sinewave. Digital code is set at 1000 000 0000.
SCALE: Reference Input 5V/DIV (Thin Trace)
Feedthrough Output 5mV/DIV
TIME: Top Photo 5ms/DIV
Bottom Photo 500µs/DIV

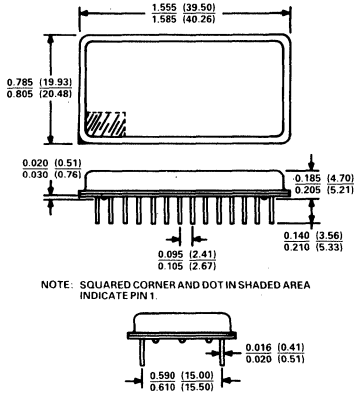
MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD394, AD395, with the inherent reliability of integrated circuit construction, were designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protect the chips from hazardous environments. To further insure reliability, the AD394, AD395 are both fully compliant to MIL-STD-883 Class B, Method 5008.

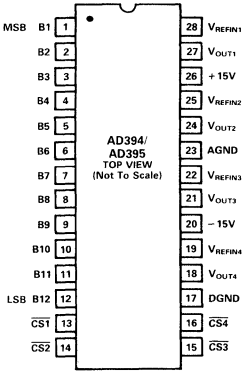
Consult Analog Devices Military Catalog for proper ordering part number and detail specification.

PACKAGE OUTLINE

Dimensions shown in inches and (mm).



PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}
AD394JM	0 to +70°C	±4LSB	±3/4LSB
AD395JM	0 to +70°C	±4LSB	±3/4LSB
AD394KM	0 to +70°C	±2LSB	±1/2LSB
AD395KM	0 to +70°C	±2LSB	±1/2LSB
AD394SM	−55°C to +125°C	±4LSB	±3/4LSB
AD395SM	−55°C to +125°C	±4LSB	±3/4LSB
AD394TM	−55°C to +125°C	±2LSB	±1/2LSB
AD395TM	−55°C to +125°C	±2LSB	±1/2LSB

Theory of Operation

The AD394 quad DAC provides four-quadrant multiplication. It is a hybrid IC comprised of four monolithic 12-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or an ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has a 12-bit wide data latch to buffer the converter when connected to a microprocessor data bus.

The AD395 quad DAC provides two-quadrant multiplication and is comprised of four 12-bit CMOS multiplying DACs and four precision output amplifiers. The two-quadrant-multiplication function arises from a straight-binary digital input multiplied by a bipolar analog input which results in two-quadrant multiplication. The AD395 can also operate as a standard unipolar DAC when a fixed dc reference is applied to V_{REFIN}.

MULTIPLYING MODE

The figures below show the transfer function for each model. The diagrams indicate an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in each diagram indicates the transfer function if a fixed reference is at the input. The digital codes above each diagram indicate the mid and endpoints of each function. The relationship between the reference input (V_{REFIN}) the digital input code and the analog output is given in Tables I and II below. Note that the reference input signal sets the slope of the transfer function (and determines the full scale output at code 111 . . 111) while the digital input selects the horizontal position in each diagram.

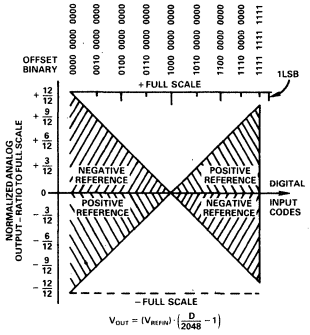


Figure 2. AD394 as a Four-Quadrant Multiplier of Reference Input and Digital Input

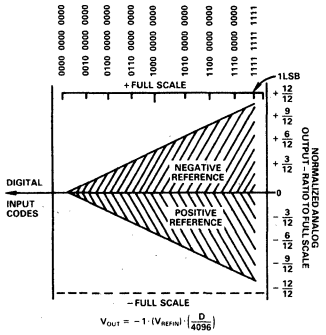


Figure 3. AD395 as a Two-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$+1 \cdot (V_{REFIN}) \left\{\frac{2047}{2048}\right\}$	+9.9951V	+FULL SCALE – 1LSB
1100	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0001	$+1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1 \cdot (V_{REFIN}) \left\{\frac{0}{2048}\right\}$	+0.000V	ZERO
0111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{2048}\right\}$	-4.88mV	-1LSB
0100	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{1024}{2048}\right\}$	-5.000V	-1/2 SCALE
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{2048}\right\}$	-10.000V	-FULL SCALE

Table I. AD394 Bipolar Code Table

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$-1 \cdot (V_{REFIN}) \left\{\frac{4095}{4096}\right\}$	-9.9976V	-FULL SCALE – 1LSB
1000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{2048}{4096}\right\}$	-5.000V	-1/2 SCALE
0000	0000	0001	$-1 \cdot (V_{REFIN}) \left\{\frac{1}{4096}\right\}$	-2.44mV	-1LSB
0000	0000	0000	$-1 \cdot (V_{REFIN}) \left\{\frac{0}{4096}\right\}$	0.000V	ZERO

Table II. AD395 Unipolar Code Table

DATA AND CONTROL SIGNAL FORMAT

The AD394 and AD395 accept 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$. As detailed in Table III, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident, all four DAC outputs will be updated to the value located on the data bus. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table III. DAC Select Matrix

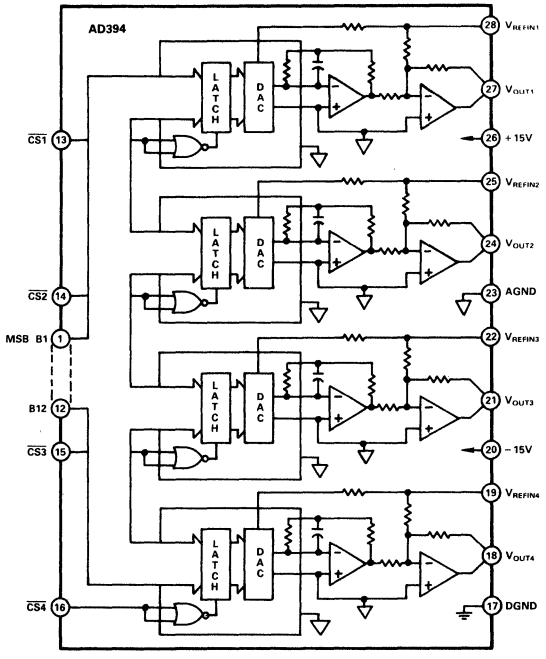


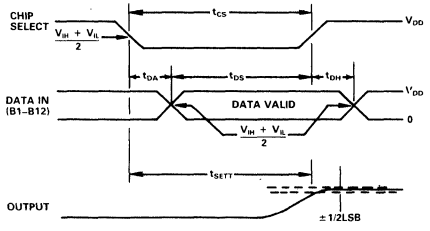
Figure 4. AD394 (Bipolar) Functional Block Diagram

TIMING

The AD394, AD395 control signal timing is very straightforward. $\overline{CS1}$-$\overline{CS4}$ must maintain a minimum pulsewidth of at least 400ns for a desired operation to occur. When loading data from a bus into a 12-bit wide data latch, the data must be stable for at least 210ns before returning CS to a high state. When the $\overline{CS}$ is low, the data latch is transparent allowing the data at the input to propagate through to the DAC. Data can change immediately after the chip select returns high. DAC settling time is measured from the falling edge of the active chip select.

Symbol	Parameter	Min	Typ	Max	Units
t_{CS}	Chip Select Pulse Width	400	150		ns
t_{DA}	Data Access Time	0			ns
t_{DS}	Data Set-Up Time	210	150		ns
t_{DH}	Data Hold Time	0			ns

Table IV. AD394, AD395 Timing Specifications, T_{min} to T_{max}



NOTES
TR = TF = 20ns, ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% to 90% of V_{DD} (+5V TYP)
TIMING MEASUREMENT REFERENCE LEVEL IS $(V_{IH} + V_{IL})/2$

MODE SELECTION

WRITE MODE	HOLD MODE
$\overline{CS}$ LOW, DAC RESPONDS TO DATA BUS (B1-B12) INPUTS	$\overline{CS}$ HIGH, DATA BUS (B1-B12) LOCKED OUT; DAC HOLDS LAST DATA PRESENT WHEN $\overline{CS}$ ASSUMED HIGH STATE.

Figure 5. Timing Diagram

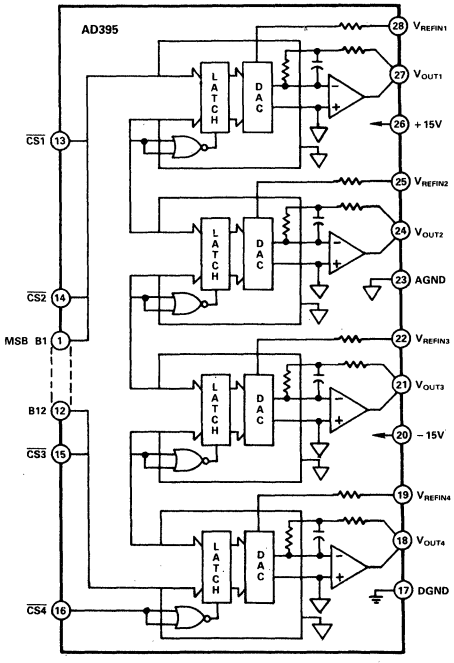


Figure 6. AD395 (Unipolar) Functional Block Diagram

Analog Circuit Details

GROUNDING RULES

The AD394 and AD395 include two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 17) and AGND (pin 23). The DGND pin is the return for the supply currents of the AD394, AD395 and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the circuitry which drives the digital inputs.

Pin 23, AGND, is the high-quality analog ground connection. This pin should serve as the reference point for all analog circuitry associated with the AD394, AD395. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 23 as shown in Figure 7.

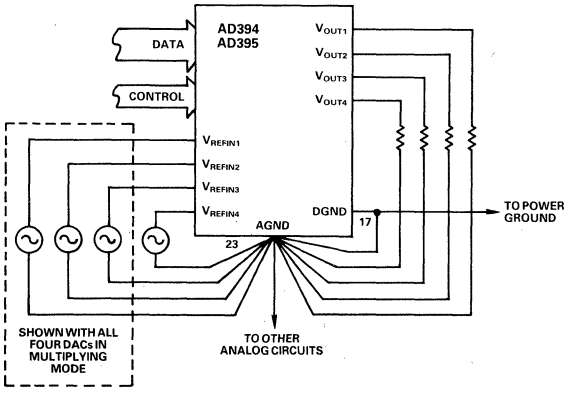


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the DAC outputs are accurately developed between the output pin and pin 23 (AGND), delivering these signals to remote loads

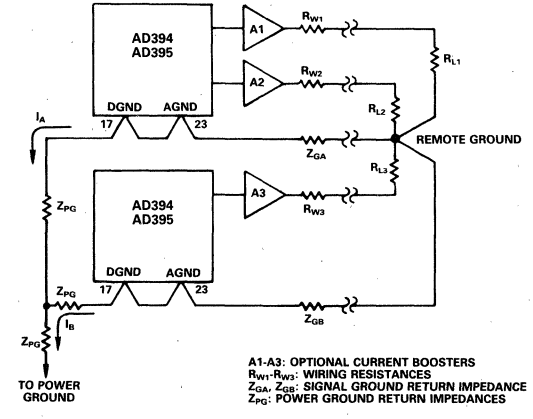


Figure 8. Grounding Errors in Multiple-AD394, AD395 Systems

can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD394, AD395 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

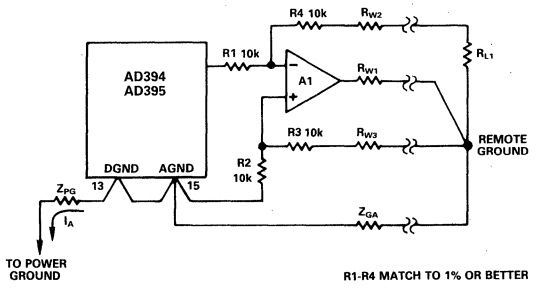


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

OPERATION FROM ±12 VOLT SUPPLIES

The AD394, AD395 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB).

Figure 10 shows a suggested circuit to set up a ±8.192V output range. To help prevent poor gain drift due to possible mismatch between R_{IN} and $R_{THEVENIN}$ of divider network it is recommended to buffer the potentiometer wiper voltage with an OP-07.

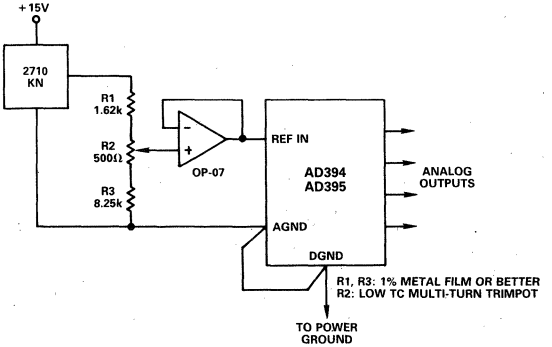


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

POWER SUPPLY DECOUPLING

The power supplies used with the AD394, AD395 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD394 supply pins and the AGND pin. If an output booster is used, its supplies should also be decoupled to the load ground.

IMPROVING FULL-SCALE STABILITY

In large systems using multiple DACs, it may be desirable for all devices to share a common reference. A precision reference can greatly improve system accuracy and temperature stability.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C. The combination of the AD2710LN and AD394, AD395 shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

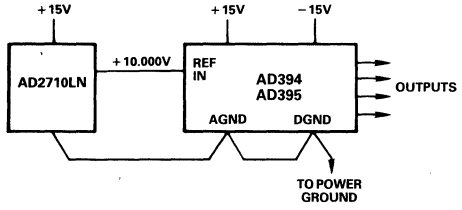


Figure 11. Low Drift AD394, AD395 Configuration

Applications

INTERFACING THE AD394, AD395 TO MICROPROCESSORS

The AD394, AD395 control logic provides simple interface to microprocessors. The individual latches allow for multi-DAC interfacing to a single data bus.

16-BIT PROCESSORS

The AD394, AD395 are 12-bit resolution DAC systems and are easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 12, a system write signal is used to control the decoded address lines and a 74LS139 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In the circuit of Figure 12, address lines A0 and A1 each select a single DAC of the four contained in the AD394 or AD395. The use of a separate address line for each DAC allows several DACs to be accessed simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address.

In the addressing scheme shown, A0 represents the least significant word address bit. Data may reside in either the 12MSBs (left-justified) or the 12LSBs (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

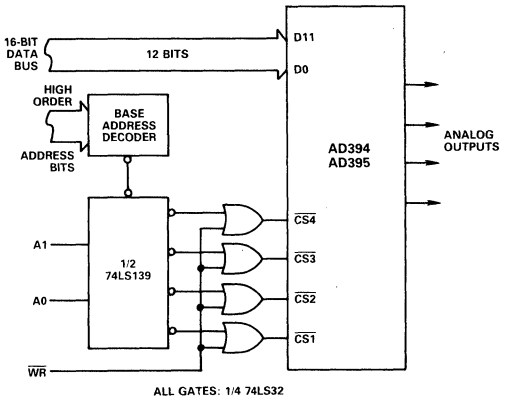
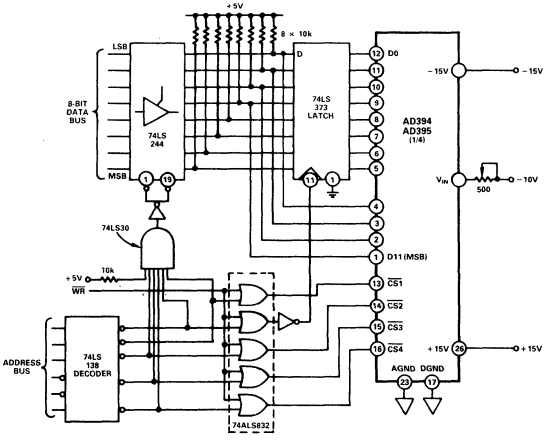


Figure 12. AD394, AD395 16-Bit Bus Interface

8-BIT PROCESSORS

The circuit of Figure 13 shows the general principles for connecting the AD394 or the AD395 to an 8-bit data bus. The 74LS244 buffers the data bus; its outputs are enabled when the DAC address appears on the address bus. The first byte sent to the DAC is loaded to the 74LS373 octal latch and, when the second byte is sent to the DAC, it is combined with the first byte to create a 12-bit word. The connections shown are for right-hand justified data. $\overline{CS}$ and $\overline{WR}$ inputs to the DAC are also gated, and when active, the DAC is loaded. Pull-up resistors at the output of the 74LS244 buffer ensure that the inputs to the DAC do not float at an ill-defined level when the DAC is not being addressed. This method of connecting 12-bit DACs to an 8-bit data bus is most cost effective when multiple DACs are utilized for 8-bit data bus applications.



NOTE:
UNUSED HEX INVERTER INPUTS SHOULD BE TIED LOW. ALL OTHER GATE INPUTS SHOWN SHOULD BE TIED HIGH TO +5V THROUGH A 10kΩ RESISTOR.

Figure 13. AD394, AD395 8-Bit Data Bus Interface

Applications

The functional density of the AD394 and AD395 permits complex analog functions to be produced under digital control, where board space requirements would otherwise be prohibitive. Multiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD394 or AD395 in a fraction of the space which would be needed if separate DACs were used.

USING THE AD394 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD394 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD394 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 14. The AD311 comparator compares the unknown input voltage to one of the AD394 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the

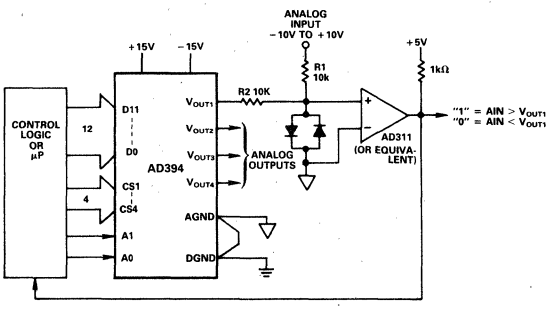


Figure 14. Using One AD394 Output for A/D Conversion

comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 15 microseconds, resulting in 12-bit successive approximation conversion in under 180 microseconds. The benefit of the AD394 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD394 and the comparator).

PROGRAMMABLE WINDOW COMPARATOR

The AD395 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD395.

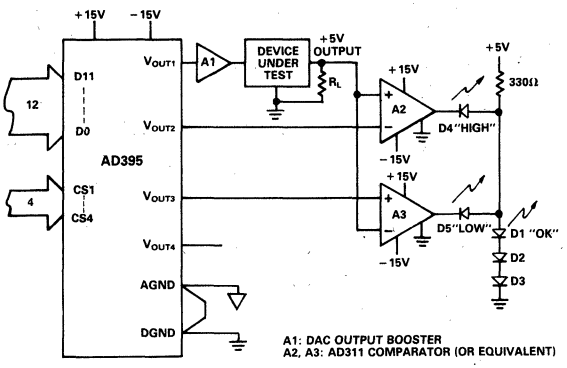


Figure 15. Programmable Window Comparator Used in Power-Supply Testing

In the circuit of Figure 15, two AD311 voltage comparators are used within AD395 to test the output of a 5 volt power-supply regulator. The AD395 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD395 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

AD395 AS A MULTIPLIER AND ATTENUATOR

So far, it has been assumed that the reference voltage V_{REFIN} is fixed. In fact, V_{REFIN} can be any voltage within the range ($-11V < V_{REFIN} < +11V$). It can be negative, positive, sinusoidal or whatever the user prefers. This leads to the name "Multiplying D/A Converters" because the output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the V_{REFIN} terminal.

$$V_{OUT} = -1 \cdot (V_{REFIN}) \cdot \frac{D}{(4096)} \qquad (0<D<4095)$$

D is the fractional binary value of the digital word applied to the converter. The AD395 multiplies the digital input value by the analog input voltage at V_{REFIN} for any value of V_{REFIN} up to 22V p-p. This in itself is a powerful tool. Any applications requiring precision multiplication with minimal zero offset and very low distortion should consider the AD395 as a candidate. One popular use for AD395 is as a audio frequency attenuator. The audio signal is applied to the V_{REFIN} input and the attenuation code is applied to the DAC; the output voltage is the product of the two – an attenuated version of the input. The maximum attenuation range obtainable utilizing 12-bits is 4096:1 or 72db.

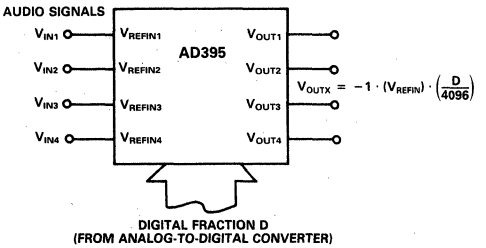


Figure 16. AD395 as a Multiplier or Attenuator

ANALOG DEVICES

Real-Time Analog Computational Unit (ACU)

AD538

FEATURES

$V_{OUT} = V_Y\left(\frac{V_Z}{V_X}\right)^m$ Transfer Function

Wide Dynamic Range (Denominator) – 1000:1
Simultaneous Multiplication and Division
Resistor-Programmable Powers & Roots
No External Trims Required
Low Input Offsets <100μV
Low Error ±0.25% of Reading (100:1 Range)
+2V and +10V On-Chip References
Monolithic Construction

APPLICATIONS

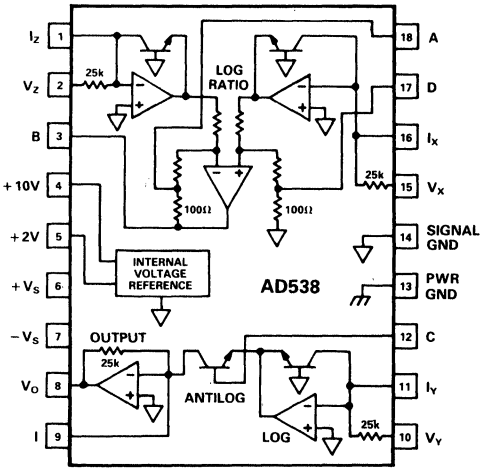
One- or Two-Quadrant Mult/Div
Log Ratio Computation
Squaring/Square Rooting
Trigonometric Function Approximations
Linearization Via Curve Fitting
Precision AGC
Power Functions

PRODUCT DESCRIPTION

The AD538 is a monolithic real-time computational circuit which provides precision analog multiplication, division and exponentiation. The combination of low input and output offset voltages and excellent linearity results in accurate computation over an unusually wide input dynamic range. Laser wafer trimming makes multiplication and division with errors as low as 0.25% of reading possible, while typical output offsets of 100μV or less add to the overall off-the-shelf performance level. Real-time analog signal processing is further enhanced by the device's 400kHz bandwidth.

The AD538's overall transfer function is $V_O = V_Y (V_Z/V_X)^m$. Programming a particular function is via pin strapping. No external components are required for one quadrant (positive input) multiplication and division. Two quadrant (bipolar numerator) division is possible with the use of external level shifting and scaling resistors. The desired scale factor for both multiplication and division can be set using the on-chip +2V or +10V references, or controlled externally to provide simultaneous multiplication and division. Exponentiation with an m value from 0.2 to 5 can be implemented with the addition of one or two external resistors.

AD538 FUNCTIONAL BLOCK DIAGRAM



Direct log ratio computation is possible by utilizing only the log ratio and output sections of the chip. Access to the multiple summing junctions adds further to the AD538's flexibility. Finally, a wide power supply range of ±4.5V to ±18V allows operation from standard ±5V, ±12V and ±15V supplies.

The AD538 is available in two accuracy grades (A and B) over the industrial (–25°C to +85°C) temperature range and one grade (S) over the military (–55°C to +125°C) temperature range. The device is packaged in an 18-pin TO-118 hermetic side-brazed ceramic DIP.

PRODUCT HIGHLIGHTS

1. Real-time analog multiplication, division and exponentiation.
2. High accuracy analog division with a wide input dynamic range.
3. On-chip +2V or +10V scaling reference voltages.
4. Both voltage and current (summing) input modes.
5. Monolithic construction with lower cost and higher reliability than hybrid and modular circuits.

SPECIFICATIONS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

Parameters	Conditions	AD538AD Min	AD538AD Typ	AD538AD Max	AD538BD Min	AD538BD Typ	AD538BD Max	AD538SD Min	AD538SD Typ	AD538SD Max	Units
MULTIPLIER/DIVIDER PERFORMANCE											
Nominal Transfer Function	$10V \geq V_X, V_Y, V_Z \geq 0$		$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$		
	$400\mu A \geq I_X, I_Y, I_Z \geq 0$		$V_O = 25k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$		
Total Error Terms	$100mV \leq V_X \leq 10V$		±0.5	**±1**		±0.25	**±0.5**		±0.5	**±1**	% of Reading +
100:1 Input Range[1]	$100mV \leq V_Y \leq 10V$		±200	**±500**		±100	**±250**		±200	**±500**	μV
	$100mV \leq V_Z \leq 10V$										
	$V_Z \leq 10V_X$, m = 1.0										
	$T_A = T_{min}$ to T_{max}		±1	**±2**		±0.5	**±1**		±1.25	**±2.5**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV
Wide Dynamic Range[2]	$10mV \leq V_X \leq 10V$		±1	**±2**		±0.5	**±1**		±1	**±2**	% of Reading +
	$1mV \leq V_Y \leq 10V$		±200	**±500**		±100	**±250**		±200	**±500**	μV +
	$0V \leq V_Z \leq 10V$		±100	**±250**		±750	**±150**		±200	**±250**	$\mu V \times (V_Y + V_Z)/V_X$
	$V_Z \leq 10V_X$, m = 1.0										
	$T_A = T_{min}$ to T_{max}		±1.5	**±3**		±1	**±2**		±2	**±4**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV +
			±450	**±750**		±350	**±500**		±750	**±1000**	$\mu V \times (V_Y + V_Z)/V_X$
Exponent (m) Range	$T_A = T_{min}$ to T_{max}	0.2		5	0.2		5	0.2		5	
OUTPUT CHARACTERISTICS											
Offset Voltage	$V_Y = 0, V_C = -600mV$		±200	**±500**		±100	**±250**		±200	**±500**	μV
	$T_A = T_{min}$ to T_{max}		±450	**±750**		±350	**±500**		±750	**±1000**	μV
Output Voltage Swing	$R_L = 2k\Omega$	−11		**±11**	−11		**+11**	−11		**+11**	V
Output Current		5	10		5	10		5	10		mA
FREQUENCY RESPONSE											
Slew Rate			1.4			1.4			1.4		V/μs
Small Signal Bandwidth	$100mV \leq V_Y, V_Z, V_X \leq 10V$		400			400			400		kHz
VOLTAGE REFERENCE											
Accuracy	$V_{REF} = 10V$ or 2V		±25	**±50**		±15	**±25**		±25	**±50**	mV
	$T_A = T_{min}$ to T_{max}		15	**30**		15	**30**		15	**30**	ppm/°C
Output Current	$V_{REF} = 10V$ to 2V	**1**	2.5		**1**	2.5		**1**	2.5		mA
Power Supply Rejection											
$+2V = V_{REF}$	$\pm 4.5V \leq V_S \leq \pm 18V$		300	**600**		300	**600**		300	**600**	μV/V
$+10V = V_{REF}$	$\pm 13V \leq V_S \leq \pm 18V$		200	**500**		200	**500**		200	**500**	μV/V
POWER SUPPLY											
Rated	$R_L = 2k\Omega$		±15			±15			±15		V
Operating Range[3]		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
PSRR	$\pm 4.5V < V_S < \pm 18V$		0.05	**0.1**		0.05	**0.1**		0.05	**0.1**	%/V
	$V_X = V_Y = V_Z = 1V$										
	$V_{OUT} = 1V$										
Quiescent Current			4.5	**7**		4.5	**7**		4.5	**7**	mA
TEMPERATURE RANGE											
Rated		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C

NOTES

[1]Over the 100mV to 10V operating range total error is the sum of a percent of reading term and an output offset. With this input dynamic range the input offset contribution to total error is negligible compared to the percent of reading error. Thus, it is specified indirectly as a part of the percent of reading error.

[2]The most accurate representation of total error with low level inputs is the summation of a percent of reading term, an output offset and an input offset multiplied by the incremental gain $(V_Y + V_Z)/V_X$.

[3]When using supplies below ± 13V the 10V reference pin *must* be connected to the 2V pin in order for the AD538 to operate correctly.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

RE-EXAMINATION OF MULTIPLIER/DIVIDER ACCURACY

Traditionally, the "accuracy" of (actually the errors of) analog multipliers and dividers have been specified in terms of percent of full scale. Thus specified, a 1% multiplier error with a 10V full scale output would mean a worst case error of +100mV at "any" level within its designated output range. While this type of error specification is easy to test, evaluate, and interpret, it can leave the user guessing as to how useful the multiplier actually is at low output levels, those approaching the specified error limit (in this case) 100mV.

The AD538's error sources do not follow the percent of full-scale approach to specification, thus it more optimally fits the needs of the very wide dynamic range applications for which it is best suited. Rather than as a percent of full scale, the AD538's error as a multiplier or divider for a 100:1 (100mV to 10V) input range is specified as the sum of two error components: a percent of reading (ideal output) term plus a fixed output offset. Following this format the AD538AD, operating as a multiplier or divider with inputs down to 100mV, has a maximum error of ±1% of reading ±500μV. Some sample total error calculations for both grades over the 100:1 input range are illustrated in the chart below. This error specification format is a familiar one to designers and users of digital voltmeters where error is specified as a percent of reading ± a certain number of digits on the meter readout.

For operation as a multiplier or divider over a wider dynamic range (>100:1), the AD538 has a more detailed error specification which is the sum of three components: a percent of reading term, an output offset term and an input offset term for the V_Y/V_X log ratio section. A sample application of this specification, taken from the chart below, for the AD538AD with V_Y = 1V, V_Z = 100mV and V_X = 10mV would yield a maximum error of ±2.0% of reading ±500μV ±(1V + 100mV)/10mV × 250μV or ±2.0% of reading ±500μV ± 27.5mV. This example illustrates that with very low level inputs the AD538's incremental gain $(V_Y + V_Z)/V_X$ has increased to make the input offset contribution to error substantial.

3

AD538 SAMPLE ERROR CALCULATION CHART (worst case)

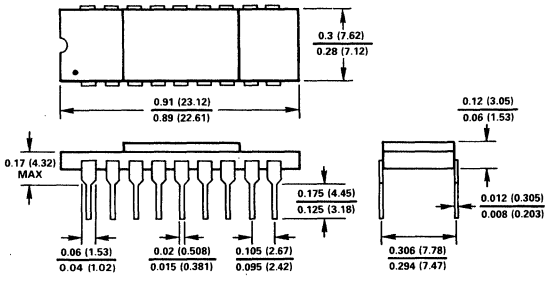
	V_Y Input (in V)	V_Z Input (in V)	V_X Input (in V)	Ideal Output (in V)	Total Offset Error Term (in mV)	% of Reading Error Term (in mV)	Total Error Summation (in mV)	Total Error Summation as a % of the Ideal Output
100:1 INPUT RANGE Total Error = ±% rdg ±Output V_{OS}	10	10	10	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	10	0.1	0.1	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	1	1	1	1	0.5 (AD) 0.25 (BD)	10 (AD) 5 (BD)	10.5 (AD) 5.25 (BD)	1.05 (AD) 0.5 (BD)
	0.1	0.1	0.1	0.1	0.5 (AD) 0.25 (BD)	1 (AD) 0.5 (BD)	1.5 (AD) 0.75 (BD)	1.5 (AD) 0.75 (BD)
WIDE DYNAMIC RANGE	1	0.10	0.01	10	28 (AD) 16.75 (BD)	200 (AD) 100 (BD)	228 (AD) 116.75 (BD)	2.28 (AD) 1.17 (BD)
Total Error = ±% rdg ±Output V_{OS} ±Input V_{OS} × $(V_Y+V_Z)/V_X$	10	0.05	2	0.25	1.76 (AD) 1 (BD)	5 (AD) 2.5 (BD)	6.76 (AD) 3.5 (BD)	2.7 (AD) 1.4 (BD)
	5	0.01	0.01	5	125.75 (AD) 75.4 (BD)	100 (AD) 50 (BD)	225.75 (AD) 125.4 (BD)	4.52 (AD) 2.51 (BD)
	10	0.01	0.1	1	25.53 (AD) 15.27 (BD)	20 (AD) 10 (BD)	45.53 (AD) 25.27 (BD)	4.55 (AD) 2.53 (BD)

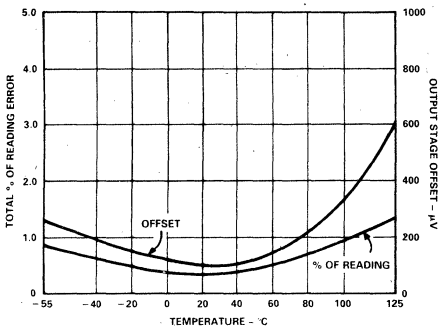
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation 250mW
Output Short Circuit-to-Ground . . . . . Indefinite
Input Voltages V_X, V_Y, V_Z . . . . . (+V_S−1V), −1V
Input Currents I_X, I_Y, I_Z, I_O 1mA
Operating Temperature Range . . . . . −25°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°
Lead Temperature, Storage . . . . . 60 sec, +300°C

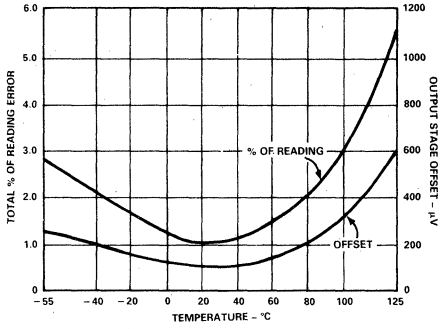
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

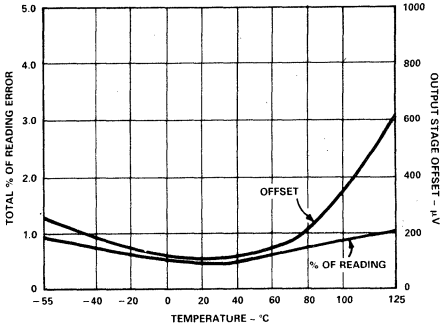




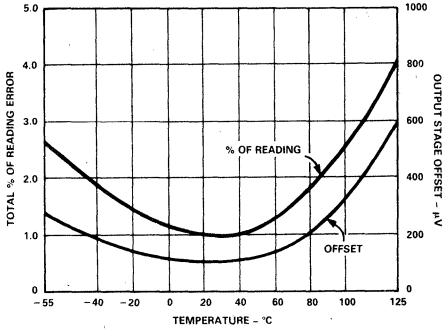
Multiplier Error vs. Temperature (100mV < V_X, V_Y, V_Z ≤ 10V)



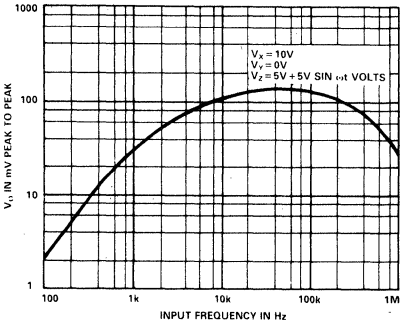
Multiplier Error vs. Temperature (10mV < V_X, V_Y, V_Z ≤ 100mV)



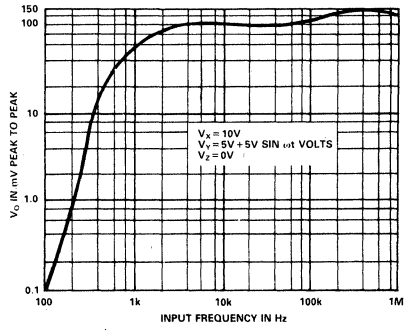
Divider Error vs. Temperature (100mV < V_X, V_Y, V_Z ≤10V)



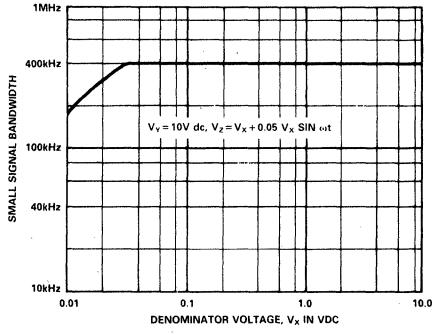
Divider Error vs. Temperature (10mV ≤ V_X, V_Y, V_Z ≤ 100mV)



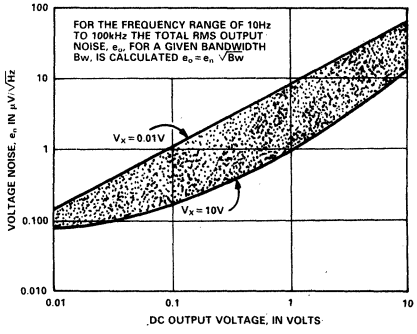
V_Z Feedthrough vs. Frequency



V_Y Feedthrough vs. Frequency



Small Signal Bandwidth vs Denominator Voltage (One-Quadrant Mult/Div)



1kHz Output Noise Spectral Density vs. dc Output Voltage

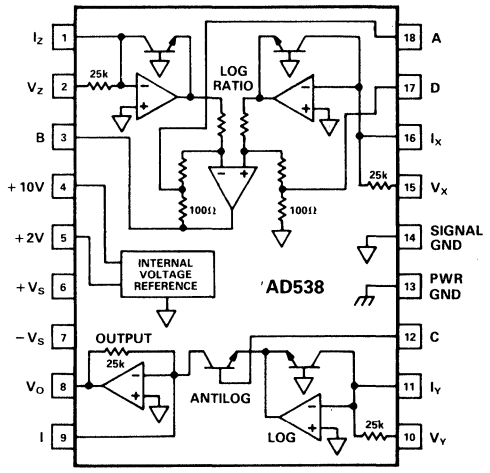


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figures 1 and 2, the V_Z and V_X inputs connect directly to the AD538's input log ratio amplifiers. This subsection provides an output voltage proportional to the natural log of input voltage V_Z, minus the natural log of input voltage V_X. The output of the log ratio subsection at B can be expressed by the transfer function:

$$V_B = \frac{kT}{q} \ln\left(\frac{V_Z}{V_X}\right)$$

(where $k = 1.3806 \times 10^{-23}$ J/K, $q = 1.6\ 0219 \times 10^{-19}$ C, T is in Kelvins)

The log ratio configuration may be used alone, if correctly temperature compensated and scaled to the desired output level (see Applications section).

Under normal operation, the log-ratio output will be connected directly to a second functional block at input C, the antilog subsection. This section performs the antilog according to the transfer function:

$$V_O = V_Y e^{\left(V_C \frac{q}{kT}\right)}$$

As with the log-ratio circuit included in the AD538, the user may use the antilog subsection by itself. When both subsections are combined, the output at B is tied to C, the transfer function of the AD538 computational unit is:

$$V_O = V_Y e^{\left[\left(\frac{kT}{q}\right)\left(\frac{q}{kT}\right)\ln\left(\frac{V_Z}{V_X}\right)\right]} \quad ; V_B = V_C$$

which reduces to:

$$V_O = V_Y\left(\frac{V_Z}{V_X}\right)$$

Finally, by increasing the gain or attenuating the output of the log ratio subsection via resistor programming, it is possible to raise the quantity V_Z/V_X to the m^{th} power. Without external programming, m is unity. Thus the overall AD538 transfer function equals:

$$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$$

where $0.2 < m < 5$

When the AD538 is used as an analog divider, the V_Y input can be used to multiply the ratio V_Z/V_X by a convenient scale factor. The actual multiplication by the V_Y input signal is accomplished by adding the log of the V_Y input signal to the signal at C which is already in the log domain.

STABILITY PRECAUTIONS

At higher frequencies, the multi-staged signal path of the AD538, as illustrated in Figure 2, can result in large phase shifts. If a condition of high incremental gain exists along that path (e.g., $V_O = V_Y \times V_Z/V_X = 10V \times 10mV/10mV = 10V$ so that $\Delta V_O/\Delta V_X = 1000$), then small amounts of capacitive feedback from V_O to the current inputs I_Z or I_X can result in instability. Appropriate care should be exercised in board layout to prevent capacitive feedback mechanisms under these conditions.

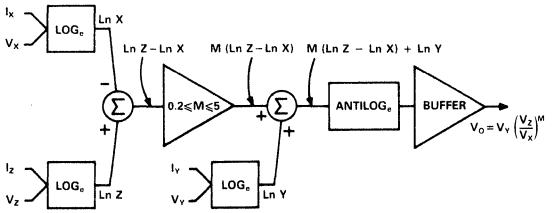


Figure 2. Model Circuit

USING THE VOLTAGE REFERENCES

A stable bandgap voltage reference for scaling is included in the AD538. It is laser-trimmed to provide a selectable voltage output of +10V buffered (Pin 4), +2V unbuffered (Pin 5) or any voltages between +2V and +10.2V buffered as shown in Figure 3. The output impedance at pin 5 is approximately 5kΩ. Note that any loading of this pin will produce an error in the +10V reference voltage. External loads on the +2V output should be greater than 500kΩ to maintain errors less than 1%.

In situations not requiring both reference levels, the +2V output can be converted to a buffered output by tying pins 4 and 5

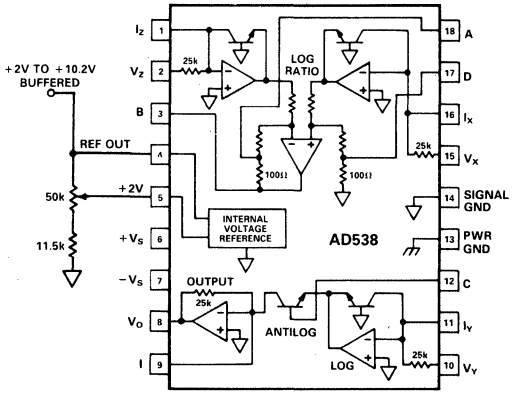


Figure 3. +2V to +10.2V Adjustable Reference

together. If both references are required simultaneously, the +10V output should be used directly and the +2V output should be externally buffered.

ONE-QUADRANT MULTIPLICATION/DIVISION

Figure 4 shows how the AD538 may be easily configured as a precision one-quadrant multiplier/divider. The transfer function $V_{OUT} = V_Y (V_Z/V_X)$ allows "three" independant input variables; a calculation not available with a conventional multiplier. In addition, the 1000:1 (i.e. 10mV to 10V) input dynamic range of the AD538 greatly exceeds that of analog multipliers computing one-quadrant multiplication and division.

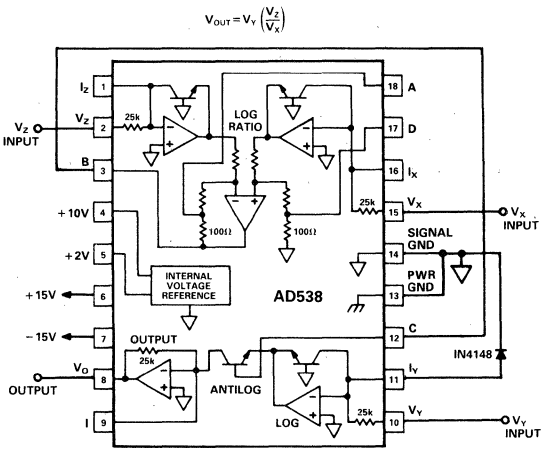


Figure 4. One-Quadrant Combination Multiplier/Divider

By simply connecting the input V_X (pin 15) to the +10V reference (pin 4), and tying the log-ratio output at B to the antilog input at C, the AD538 can be configured as a one-quadrant analog multiplier with 10 volt scaling. If 2 volt scaling is desired, V_X can be tied to the +2V reference.

When the input V_X is tied to the +10V reference terminal the multiplier transfer function becomes:

$$V_O = V_Y \left(\frac{V_Z}{10V}\right)$$

As a multiplier, this circuit provides a typical bandwidth of 400kHz with values of V_X, V_Y or V_Z varying over a 100:1 range (i.e. 100mV to 10V). The maximum error with a 100mV to 10V range for the two input variables will typically be +0.5% of reading. Using the optional Z offset trim scheme, as shown in Figure 5, this error can be reduced to +0.25% of reading.

By using the +10V reference as the V_Y input, the circuit of Figure 4 is configured as a one-quadrant divider with a fixed scale factor. As with the one-quadrant multiplier, the inputs accept only single (positive) polarity signals. The output of the one-quadrant divider with a +10V scale factor is:

$$V_O = 10V \left(\frac{V_Z}{V_X}\right)$$

The typical bandwidth of this circuit is 370kHz with 1V to 10V denominator input levels. At lower amplitudes, the bandwidth gradually decreases to approximately 200kHz at the 2mV input level.

TWO-QUADRANT DIVISION

The two-quadrant linear divider circuit illustrated in Figure 5 uses the same basic connections as the one-quadrant version. However, in this circuit the numerator has been offset in the positive direction by adding the denominator input voltage to it. The offsetting scheme changes the divider's transfer function from:

$$V_O = 10V \left(\frac{V_Z}{V_X}\right)$$

To:

$$V_O = 10V \frac{(V_Z + AV_X)}{V_X} = 10V \left(1A + \frac{V_Z}{V_X}\right)$$

$$= 10A + 10V \left(\frac{V_Z}{V_X}\right); \text{ where } A = \frac{35k\Omega}{25k\Omega}$$

As long as the magnitude of the denominator input is equal to or greater than the magnitude of the numerator input, the circuit will accept bipolar numerator voltages. However, under the conditions of a 0V numerator input, the output would incorrectly equal +14V. The offset can be removed by connecting the +10V reference through resistors R1 and R2 to the output section's summing node I at pin 9 thus providing a gain of 1.4 at the center of the trimpot. The pot R2 adjusts out or corrects this offset, leaving the desired transfer function of 10V (V_Z/V_X).

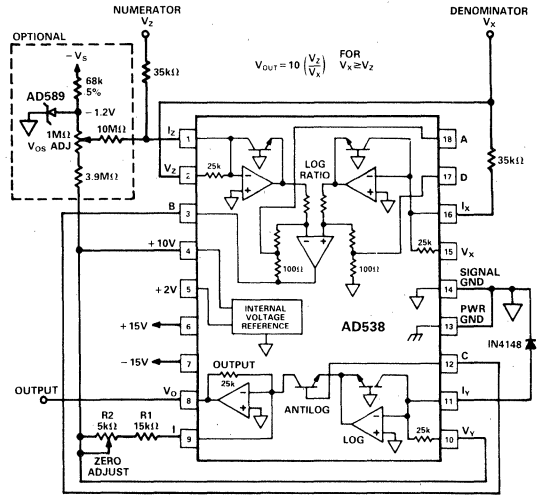


Figure 5. Two-Quadrant Division with 10V Scaling

LOG RATIO OPERATION

Figure 6 shows the AD538 configured for computing the log of the ratio of two input voltages (or currents). The output signal from B is connected to the summing junction of the output amplifier via two series resistors. The 90.9Ω metal film resistor effectively degrades the temperature coefficient of the ±3500ppm/°C resistor to produce a 1.09kΩ +3300ppm/°C equivalent value. In this configuration the V_Y input, must be tied to some voltage less than zero (−1.2V in this case) removing this input from the transfer function.

The 5kΩ potentiometer controls the circuit's scale factor adjustment providing a +1V per decade adjustment. The output offset potentiometer should be set to provide a zero output with $V_X = V_Z = 1V$. The input V_O adjustment should be set for an output of 3V with V_Z = 1mV and V_X = 1V.

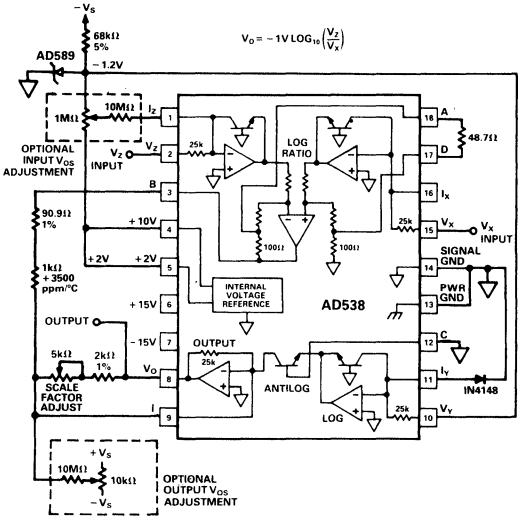
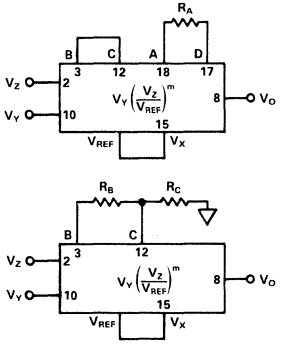


Figure 6. Log Ratio Circuit

The log ratio circuit shown achieves ±0.5% accuracy in the log domain for input voltages within three decades of input range: 10mV to 10V. This error is not defined as a percent of full-scale output, but as a percent of input. For example, using a 1V/decade scale factor, a 1% error in the positive direction at the INPUT of the log ratio amplifier translates into a 4.3mV deviation from the ideal OUTPUT (i.e., 1V × $\log_{10}$ (1.01) = 4.3214mV). An input error 1% in the negative direction is slightly different, giving an output deviation of 4.3648mV.

ANALOG COMPUTATION OF POWERS AND ROOTS

Often it is necessary to raise the quotient of two input signals to a power or take a root. This could be squaring, cubing, square-rooting or exponentiation to some noninteger power. Examples include power series generation. With the AD538, only one or two external resistors are required to set ANY desired power, over the range of 0.2 to 5. Raising the basic quantity V_Z/V_X to a power greater than one requires that the gain of the AD538's log ratio subtractor be increased, via an external resistor between pins A and D. Similarly, a voltage divider which attenuates the log ratio output between points B and C will program the power to a value less than one.



POWERS

m	R_A
2	196Ω
3	97.6Ω
4	64.9Ω
5	48.7Ω

ROOTS

m	R_B	R_C
1/2	100Ω	100Ω
1/3	100Ω	49.9Ω
1/4	150Ω	49.9Ω
1/5	162Ω	40.2Ω

Figure 7. Basic Configurations and Transfer Functions for the AD538

SQUARE ROOT OPERATION

The explicit square root circuit of Figure 8 illustrates a precise method for performing a real time square root computation. For added flexibility and accuracy this circuit has a scale factor adjustment.

The actual square rooting operation is performed in this circuit by raising the quantity V_Z/V_X to the 1/2 power via the resistor divider network consisting of resistors R_B and R_C. For maximum linearity, the two resistors should be 1% (or better) ratio-matched metal film types.

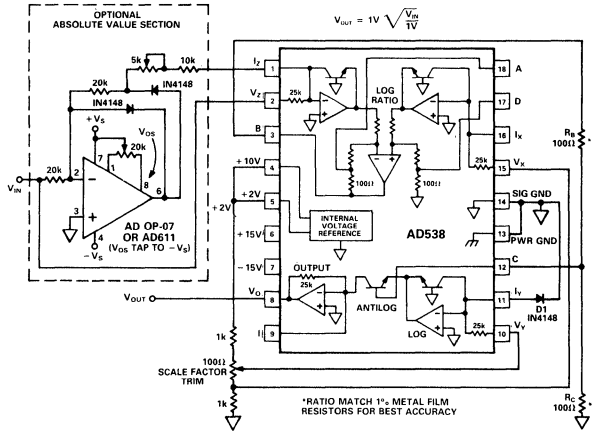


Figure 8. Square Root Circuit

One volt scaling is achieved by dividing-down the 2V reference and applying approximately 1V to both the V_Y and V_X inputs. In this circuit, the V_X input is intentionally set low, to about 0.95V, so that the V_Y input can be adjusted high; permitting a ±5% scale factor trim. Using this trim scheme, the output voltage will be within ±3mV ±0.2% of the ideal value over a 10V to 1mV input range (80dB). For a decreased input dynamic range of 10mV to 10V (60dB) the error is even less; here the output will be within ±2mV ±0.2% of the ideal value. The bandwidth of the AD538 square root circuit is approximately 280kHz with a 1V p-p sinewave with a +2V dc offset.

This basic circuit may also be used to compute the cube, fourth or fifth roots of an input waveform. All that is required for a given root is that the correct ratio of resistors, R_C and R_B, be selected such that their sum is between 150Ω and 200Ω.

The optional absolute value circuit shown preceding the AD538 allows the use of bipolar input voltages. Only one op-amp is required for the absolute value function, because the I_Z input of the AD538 functions as a summing junction. If it is necessary to preserve the sign of the input voltage, the polarity of the op-amp output may be sensed and used after the computation to switch the sign bit of a D.V.M. chip.

TRANSDUCER LINEARIZATION

Many electronic transducers used in scientific, commercial or industrial equipment monitor the physical properties of a device and/or its environment. Sensing (and perhaps compensating for) changes in pressure, temperature, moisture or other physical phenomenon can be an expensive undertaking, particularly where high accuracy and very low nonlinearity are important. In conventional analog systems accuracy may be easily increased by offset and scale factor trims, however, nonlinearity is usually the absolute limitation of the sensing device.

With the ability to easily program a complex analog function, the AD538 can effectively compensate for the nonlinearities of an inexpensive transducer. The AD538 can be connected between the transducer preamplifier output and the next stage of monitoring or transmitting circuitry. The recommended procedure for linearizing a particular transducer is first to find the closest function which best approximates the nonlinearity of the device and then, to select the appropriate exponent resistor value(s).

ARC-TANGENT APPROXIMATION

The circuit of Figure 9 is typical of those AD538 applications where the quantity V_Z/V_X is raised to powers greater than one. In an approximate arc-tangent function, the AD538 will accurately compute the angle that is defined by X and Y displacements represented by input voltages V_X and V_Z. With accuracy to within one degree (for input voltages between 100μV and 10 volts), the AD538 arc-tangent circuit is more precise than conventional analog circuits and is faster than most digital techniques. For a direct arc-tangent computation that requires fewer external components refer to the AD639 data sheet. The circuit shown is set-up for the transfer function:

$$V_\theta = (V_{\theta ref} - V_\theta)\left[\frac{(V_Z)}{(V_X)}\right]^{1.21}$$

$$\text{Where } \theta = \text{Tan}^{-1}\left(\frac{Z}{X}\right)$$

The $(V_{\theta ref} - V_\theta)$ function is implemented in this circuit by adding together the output, V_θ, and an externally applied reference voltage, $V_{\theta ref}$, via an external AD547 op-amp. The 1μF capacitor

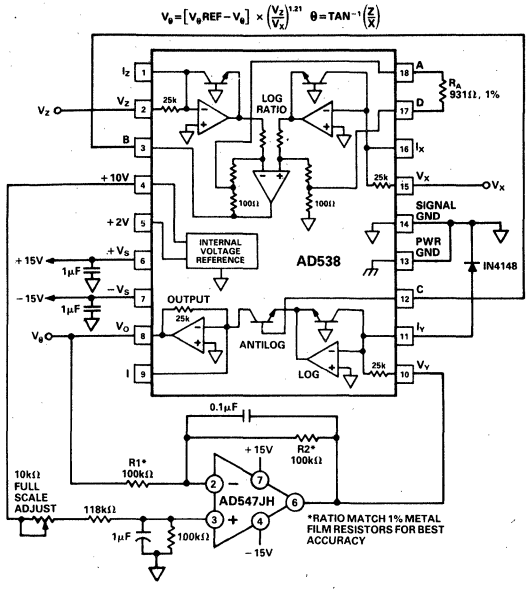


Figure 9. The Arc-Tangent Function

connected around the AD547's 100kΩ feedback resistor frequency compensates the loop (formed by the amplifier between V_θ and V_Y).

The V_B/V_A quantity is calculated in the same manner as in the one-quadrant divider circuit, except that the resulting quotient is raised to the 1.21 power. Resistor R_A (nominally 931Ω) sets the power or m factor.

For the highest arc-tangent accuracy the external resistors R1 and R2 should be ratio matched, however, the offset trim scheme shown in other circuits is not required, since nonlinearity effects are the predominant source of error. Also note, that instability will occur as the output approaches 90° because, by definition, the arc-tangent function is infinite and therefore, the AD538's gain will be extremely high.

ANALOG DEVICES

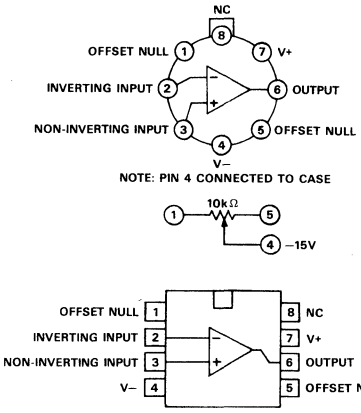
Low Power Precision BIFET Op Amp

AD548

FEATURES

- **Improved Replacement for LF441**
- **Low Quiescent Current: 200μA max**
- **Low Input Bias Current: 10pA max, Warmed-Up (AD548C)**
- **Low Offset Voltage: 250μV max (AD548C)**
- **Low Drift: 2μV/°C max (AD548C)**
- **Low Noise: 2μV p-p, 0.1 to 10Hz**
- **AC Specs: 1.8V/μs Slew Rate, 1MHz Unity Gain Bandwidth**
- **Available in Plastic, Hermetic CERDIP and Hermetic Header Packages**
- **MIL-STD-883B and Plus Parts Available**
- **Dual Version Available: AD648**

AD548 PIN CONFIGURATION



PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD548 is a low power, precision monolithic operational amplifier. It is fabricated with ion-implanted FET and laser wafer trimming technologies and offers both low bias current (25pA max, warmed-up) and low quiescent current (200μA max).

The economical J and A grades have a maximum guaranteed offset voltage of less than 2mV and an offset voltage drift of less than 20μV/°C. This level of dc precision is achieved utilizing Analog's exclusive laser wafer drift trimming process. The combination of low quiescent current and low offset drift minimizes changes in offset voltage due to self-heating effects. Four additional grades are offered, which provide increased performance over the commercial, industrial and military temperature ranges.

The AD548 is recommended for any op amp application requiring low power and excellent dc and ac performance. Battery-powered, precision instrument front ends and CMOS DAC buffers will benefit from this device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "B" and "C" versions) and high open-loop gain ensures better than 12-bit linearity in high impedance buffer applications.

Devices are pinned out in a standard op amp configuration and are available in six performance grades. The AD548J and AD548K are rated over the commercial temperature range of 0 to +70°C. The AD548A, AD548B and AD548C are rated over the industrial temperature range of −25°C to +85°C. The AD548S is rated over the military temperature range of −55°C to +125°C; and is available processed to MIL-STD-883B, Rev. C. Devices are available in an 8-pin CERDIP, a plastic Mini-DIP or a TO-99 metal can.

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD548 the ideal op amp for high performance, low power applications.
2. Pin compatible with industry standard op amps such as the LF441 and the AD542, the AD548 enables designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low offset voltage (2mV max) and drift (20μV/°C max) are achieved utilizing Analog Devices' Laser Wafer Drift Trimming (LWDT) Technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, thus insuring that the device will meet its published specifications in actual use.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD548J/A/S Min	AD548J/A/S Typ	AD548J/A/S Max	AD548K/B Min	AD548K/B Typ	AD548K/B Max	AD548C Min	AD548C Typ	AD548C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset			2			0.5			0.25	mV
Input Offset Voltage vs. Temp			20			5			2.0	µV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			200			100			100	dB
INPUT BIAS CURRENT										
Either Input[2], CMV = 0		10	25		5	10		5	10	pA
Offset Current		5			5			2		pA
INPUT IMPEDANCE										
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		Ω|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		Ω|pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	±10	±12		±10	±12		±10	±12		V
Common Mode Rejection	80			80			80			dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2		µV p-p
f = 1kHz		35			35			35		nV/√Hz
FREQUENCY RESPONSE										
Unity Gain Small Signal		1.0			1.0			1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain		1.8			1.8			1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN[4]										
V_O = ±10V, R_L = 10kΩ	100			100			100			dB
T_{min} to T_{max}, R_L = 10kΩ	100			100			100			dB
V_O = ±10V, R_L = 5kΩ	86			86			86			dB
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	±11	±13		±11	±13		±11	±13		V
Short Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		150	200		150	200		150	200	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD548J			AD548K					
Industrial (−25°C to +85°C)		AD548A			AD548B			AD548C		
Military (−55°C to +125°C)		AD548S								
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS	J Grade: Plastic (N8A) A Grade: CERDIP (Q) TO-99 Style (HO8B) S Grade: CERDIP (Q) TO-99 Style (HO8B)			K Grade: Plastic (N8A) B Grade: CERDIP (Q) TO-99 Style (HO8B)			C Grade: Cerdip (Q) TO-99 Style (HO8B)			

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[4]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

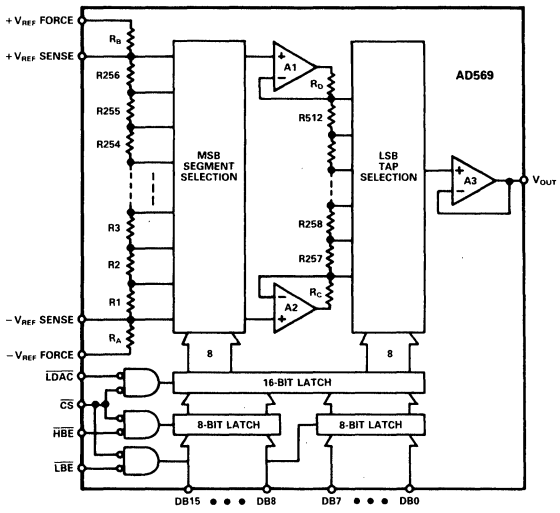
ANALOG DEVICES

BiMOS II Monotonic 16-Bit DAC

AD569

FEATURES
Guaranteed 16-Bit Monotonicity
Monolithic BiMOS II Construction
±0.01% Typical Nonlinearity
8- and 16-Bit Bus Compatible
3μs Settling to 16-Bits
Low Drift
Low Power: 200mW
Low Cost

AD569 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD569 is a monolithic 16-bit digital-to-analog converter (DAC) manufactured in Analog Devices' BiMOS II process. BiMOS II allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD569 includes two resistor strings, selector switches, decoding logic, buffer amplifiers, and double-buffered input latches on the same chip.

The AD569's voltage-segmented architecture insures 16-bit monotonicity over time and temperature. Integral linearity is maintained at ±0.01%, while differential linearity is ±0.0004%. The on-chip high-speed buffer amplifiers provide voltage output settling time of 3μs to within ±0.001% for a full-scale step.

The reference input voltage which determines the output range can be either unipolar or bipolar. Nominal reference range is ±5V and separate reference force and sense connections are provided for high accuracy applications. The AD569 can also be used with a variable or ac reference in multiplying applications.

Data may be loaded into the AD569's input latches from 8- and 16-bit buses. The double-buffered structure simplifies 8-bit bus interfacing, and allows multiple DACs to be loaded asynchronously and updated simultaneously. Four TTL/LSTTL/5V CMOS compatible signals control the latches: $\overline{CS}$, $\overline{LBE}$, $\overline{HBE}$, and $\overline{LDAC}$.

The AD569 is available in four grades: JN and KN versions are specified from 0 to +70°C and are packaged in a 28-pin plastic DIP; AD and BD versions are specified from −25°C to +85°C and are packaged in a 28-pin ceramic DIP. The SD version, also in a 28-pin ceramic DIP, is specified from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monotonicity to 16 bits is insured by the AD569's voltage-segmented architecture.
2. The output range is ratiometric to an external reference or ac signal. Gain error and gain drift of the AD569 are negligible.
3. The AD569's versatile data input structure allows loading from 8- and 16-bit buses.
4. The on-chip output buffer amplifier can supply ±5V into a 1kΩ load, and can drive capacitive loads of up to 1000pF.
5. Kelvin connections to the reference inputs preserve the gain and offset accuracy of the transfer function in the presence of wiring resistances and ground loops.

SPECIFICATIONS (T_A = +25°C, $+V_S$ = +12V, $-V_S$ = −12V, $+V_{REF}$ = +5V, $-V_{REF}$ = −5V, unless otherwise noted)

Model	AD569JN/AD			AD569KN/BD			AD569SD			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION			16			16			16	Bits
LOGIC INPUTS										
V_{IH} (Logic "1")	2.0		5.5	2.0		5.5	2.0		5.5	Volts
V_{IL} (Logic "0")	0		0.8	0		0.8	0		0.8	Volts
I_{IH} (V_{IH} = 5.5V)			10			10			10	μA
I_{IL} (V_{IL} = 0V)			10			10			10	μA
TRANSFER FUNCTION CHARACTERISTICS										
Integral Nonlinearity		±0.02	±0.04		±0.01	±0.024			±0.04	% FSR[1]
T_{min} to T_{max}		±0.02	±0.04		±0.020	±0.024			±0.04	% FSR
Differential Nonlinearity		±1/2	±1		±1/4	±1/2			±1	LSB
T_{min} to T_{max}		±1/2	±1		±1/2	±1			±1	LSB
Unipolar Offset[2]			±500			±350			±500	μV
T_{min} to T_{max}			±750			±450			±750	μV
Bipolar Offset[2]			±500			±350			±500	μV
T_{min} to T_{max}			±750			±450			±750	μV
Full Scale Error[2]			±350			±350			±350	μV
T_{min} to T_{max}			±450			±450			±450	μV
Bipolar Zero[2]			±0.04			±0.024			±0.04	% FSR
T_{min} to T_{max}			±0.04			±0.024			±0.04	% FSR
REFERENCE INPUT										
$+V_{REF}$ Range[3]	−5		+5	−5		+5	−5		+5	Volts
$-V_{REF}$ Range[3]	−5		+5	−5		+5	−5		+5	Volts
Resistance	15	20	25	15	20	25	15	20	25	kΩ[4]
OUTPUT CHARACTERISTICS										
Voltage	−5		+5	−5		+5	−5		+5	Volts
Capacitive Load			1000			1000			1000	pF
Resistive Load	1			1			1			kΩ
Short Circuit Current		10			10			10		mA
POWER SUPPLIES										
Voltage										
$+V_S$	+10.8	+12	+13.2	+10.8	+12	+13.2	+10.8	+12	+13.2	Volts
$-V_S$	−10.8	−12	−13.2	−10.8	−12	−13.2	−10.8	−12	−13.2	Volts
Current										
$+I_S$		+9	+13		+9	+13		+9	+13	mA
$-I_S$		−9	−13		−9	−13		−9	−13	mA
Power Supply Sensitivity[5]										
$+10.8V \leq +V_S \leq +13.2V$		±0.5	±2		±0.5	±2		±0.5	±2	ppm/%
$-10.8V \geq -V_S \geq -13.2V$		±1	±3		±1	±3		±1	±3	ppm/%
TEMPERATURE RANGE										
Specified										
JN, KN	0		+70	0		+70				°C
AD, BD	−25		+85	−25		+85				°C
SD							−55		+125	°C
Storage										
JN, KN	−65		+150	−65		+150				°C
AD, BD, SD	−65		+150	−65		+150	−65		+150	°C

NOTES

[1]FSR stands for Full-Scale Range, and is 10V for a −5 to +5V span.

[2]Refer to Definitions section.

[3]For operation with supplies other than ±12V, refer to the Power Supply and Reference Voltage Range Section.

[4]Measured between $+V_{REF}$ Force and $-V_{REF}$ Force.

[5]Sensitivity of Full-Scale Error due to changes in $+V_S$ and sensitivity of Offset to changes in $-V_S$.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance Only and are not subject to test.
$+V_S = +12V; -V_S = -12V; +V_{REF} = +5V; -V_{REF} = -5V$ except where stated.

Parameter	Limit	Units	Test Conditions/Comments
Output Voltage Settling (Time to ±0.001% FS For FS Step)	5	µs max	No Load Applied
	3	µs typ	(DAC output measured from falling edge of $\overline{LDAC}$.)
	6	µs max	V_{OUT} Load = 1kΩ, C_{LOAD} = 1000pF.
	4	µs typ	(DAC output measured from falling edge of $\overline{LDAC}$.)
Digital-to-Analog Glitch Impulse	500	nV-sec typ	Measured with V_{REF} = 0V. DAC registers alternatively loaded with input codes of 8000_H and $0FFF_H$ (worst-case transition). Load = 1kΩ.
Multiplying Feedthrough	−100	dB max	$+V_{REF}$ = 1V rms 10kHz sine wave, $-V_{REF}$ = 0V
Output Noise Voltage Density (1kHz-1MHz)	40	nV/$\sqrt{Hz}$ typ	Measured between V_{OUT} and $-V_{REF}$

TIMING CHARACTERISTICS ($+V_S = +12V, -V_S = -12V, T_{min}$ to T_{max})

Parameter	Limit	Units	Test Conditions/Comments
Case A[1]			150ns Pulse on $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$
t_{WC}	70	ns min	$\overline{CS}$ Pulse Width
t_{SC}	60	ns min	$\overline{CS}$ Data Setup Time
t_{HC}	0	ns min	$\overline{CS}$ Data Hold Time
Case B[2]			100ns Pulse on $\overline{CS}$
t_{WB}	60	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	30	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{WD}	70	ns min	$\overline{LDAC}$ Pulse Width
Case C[1]			100ns Pulse on $\overline{CS}$
t_{WS}	70	ns min	$\overline{LDAC}$ & $\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SS}	30	ns min	$\overline{LDAC}$ & $\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HS}	10	ns min	$\overline{LDAC}$ & $\overline{HBE}$, $\overline{LBE}$ Data Hold Time

NOTES
[1]Write strobe applied to $\overline{CS}$ as shown in Figure 19a. Address decoding defines which register(s) data is strobed into (see Figure 1).
[2]Write strobe applied to $\overline{HBE}$ and/or $\overline{LBE}$ as in Figure 18 or applied to $\overline{LDAC}$ separately. DAC base address applied to $\overline{CS}$ (see Figure 1).
[3]Write strobe applied to $\overline{LDAC}$ and either $\overline{HBE}$ or $\overline{LBE}$ for synchronous load of 16-bit DAC register with one of the 8-bit first-rank registers as shown in Figure 19b (see Figure 2).

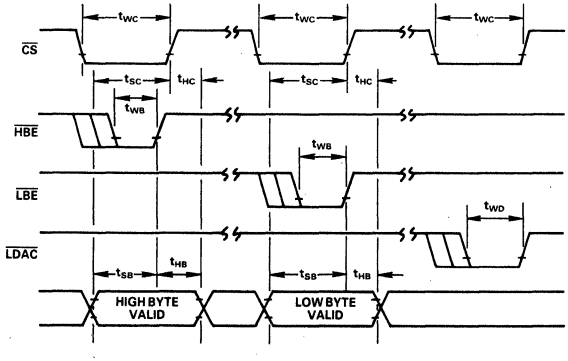


Figure 1. AD569 Timing Diagram

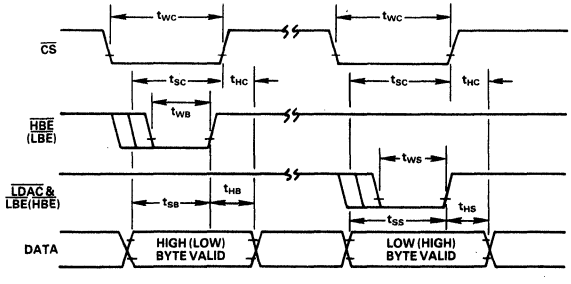


Figure 2. Timing for Synchronous Load of DAC Register

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

$+V_S$ (Pin 1) to GND (Pin 18)	+18V, −0.3V
$-V_S$ (Pin 28) to GND (Pin 18)	−18V, +0.3V
$+V_S$ (Pin 1) to $-V_S$ (Pin 28)	+26.4V, −0.3V
Digital Inputs (Pins 4-14, 19-27) to GND (Pin 18)	$+V_S$, −0.3V
$+V_{REF}$ Force (Pin 3) to $+V_{REF}$ Sense (Pin 2)	±16.5V
$-V_{REF}$ Force (Pin 15) to $-V_{REF}$ Sense (Pin 16)	±16.5V
V_{REF} Force (Pins 3, 15) to GND (Pin 18)	$\pm V_S$
V_{REF} Sense (Pins 2, 16) to GND (Pin 18)	$\pm V_S$
V_{OUT} (Pin 17)	Indefinite Short to GND, Momentary Short to $+V_S$, $-V_S$
Power Dissipation (Any Package)	1000mW
Operating Temperature Range	
Commercial Plastic (JN, KN Versions)	0 to +70°C
Industrial Ceramic (AD, BD Versions)	−25°C to +85°C
Extended Ceramic (SD Versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

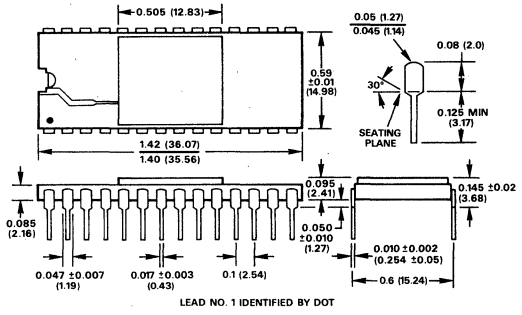
ESD SENSITIVITY

The AD569 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD569 has been classified as a Category A device.

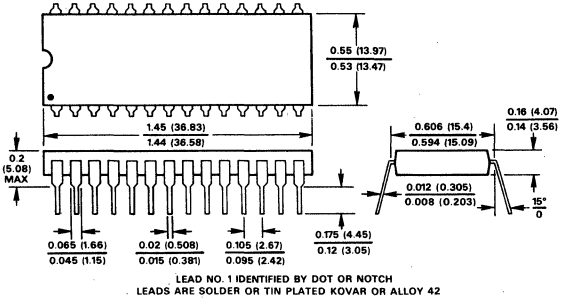
Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

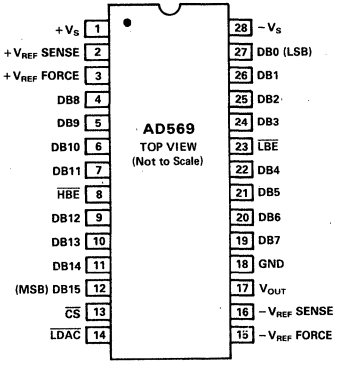


28-PIN CERAMIC DIP (D)



28-PIN PLASTIC (N)

PIN DESIGNATIONS



ORDERING INFORMATION

Integral Nonlinearity		Differential Nonlinearity		Temperature Range and Package		
+25°C	T_{min}–T_{max}	+25°C	T_{min}–T_{max}	Plastic 0 to +70°C	Ceramic −25°C to +85°	Ceramic −55°C to +125°C
±0.04%	±0.04%	±1LSB	±1LSB	AD569JN	AD569AD	AD569SD
±0.024%	±0.024%	±1/2LSB	±1LSB	AD569KN	AD569BD	–

FUNCTIONAL DESCRIPTION

The AD569 consists of two resistor strings, each of which is divided into 256 equal segments (see Figure 3). The 8MSBs of the digital input word select one of the 256 segments on the first string. The taps at the top and bottom of the selected segment are brought to the inputs of the two buffer amplifiers A1 and A2. These amplifiers exhibit extremely high CMRR and low bias current, and thus accurately preserve the voltages at the top and bottom of the segment. The buffered versions of the segment endpoints are applied across the second resistor string, where the 8LSBs of the digital input word select one of the 256 taps. Output amplifier A3 buffers this voltage and delivers it to the output, V_{OUT}.

Buffer amplifiers A1 and A2 leap-frog up the first string to preserve monotonicity at the segment boundaries. For example, when increasing the digital code from $00FF_H$ to 0100_H, (the first segment boundary), A1 remains connected to the same tap on the first resistor, while A2 jumps over it and is connected to the tap which becomes the top of the next segment. This allows monotonicity even if the amplifiers have large offsets. In fact, offset contributes only to integral linearity error.

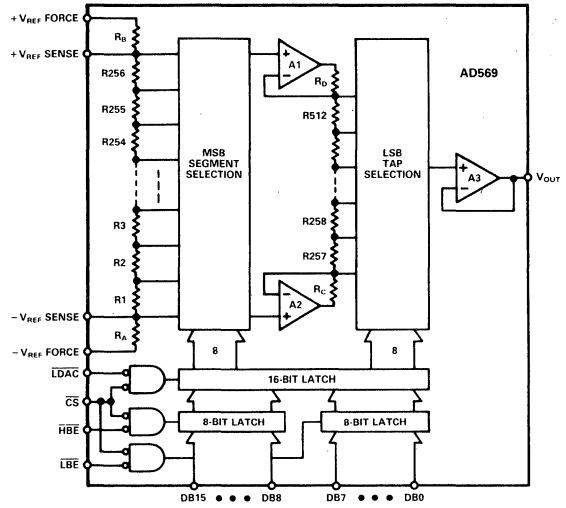


Figure 3. AD569 Block Diagram

CAUTION

It is generally considered good engineering practice not to insert integrated circuits into powered-up sockets. This is especially important with the AD569. A powered-up, empty socket configures the buffer amplifiers open-loop such that their outputs are at the positive or negative rail. At that point, insertion may result in a large current surge between the reference force and sense connections which could permanently damage the AD569.

ANALOG CIRCUIT DETAILS

Definitions

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal output (a straight line drawn from 0 to FS-1LSB) for any bit combination. The AD569's linearity is primarily limited by resistor uniformity in the first divider (upper byte of 16-bit input). The plot in Figure 4 shows the AD569's typical linearity error across the entire output range to be within ±0.01% of full scale. Maximum linearity error at 25°C for the AD569's JN and AD grades is specified as ±0.04%, and is ±0.024% for the KN and BD versions.

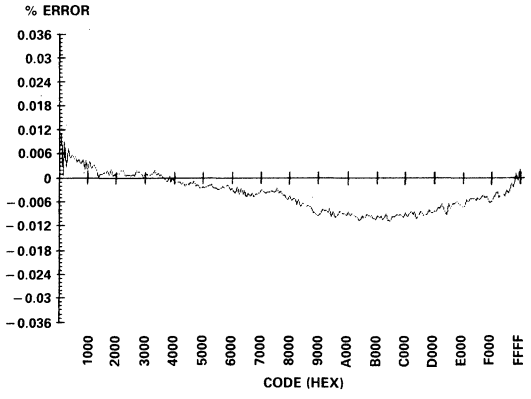


Figure 4. Typical Linearity

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs. All versions of the AD569 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. For example, for a ±5 volt output range, a change of 1LSB in digital input code should result in a 152μV change in the analog output (1LSB = 10V/65,536). If in actual use, however, the change is only 38μV, the differential linearity error would be −114μV, or −3/4LSB.

By leap-frogging the buffer amplifer taps on the first divider, the AD569 typically keeps DNL within ±38μV (±1/4LSB) around each of the 256 segment boundaries defined by the 16-bit input's upper byte (see Figure 5). Within the second divider, DNL also typically remains less than ±38μV as shown in Figure 6. Since the second divider is independent of absolute voltage, DNL is the same within the rest of the 256 segments.

OFFSET ERROR: The deviation of the analog output from the ideal ($-V_{REF}$) when the inputs are loaded with all zeroes is called an offset error. For the AD569, Unipolar Offset is specified with 0V applied to $-V_{REF}$ and Bipolar Offset is specified with −5V applied to $-V_{REF}$. Either offset is trimmed by adjusting the voltage applied to the $-V_{REF}$ terminals.

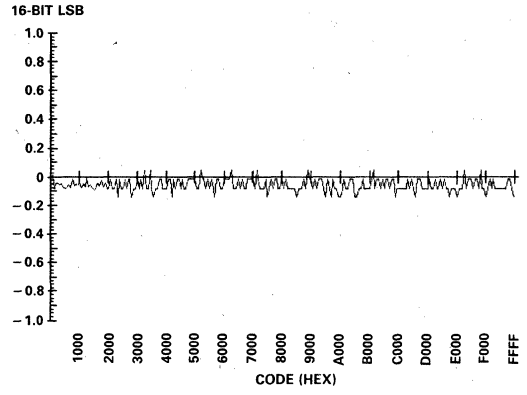
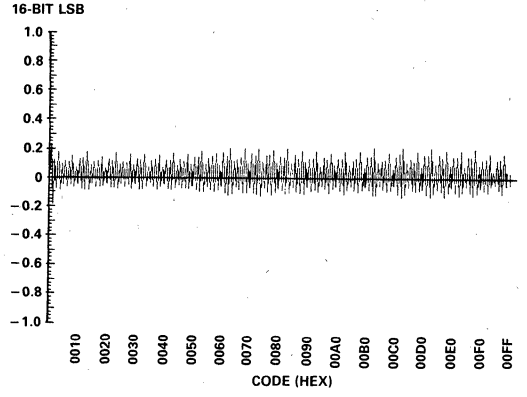
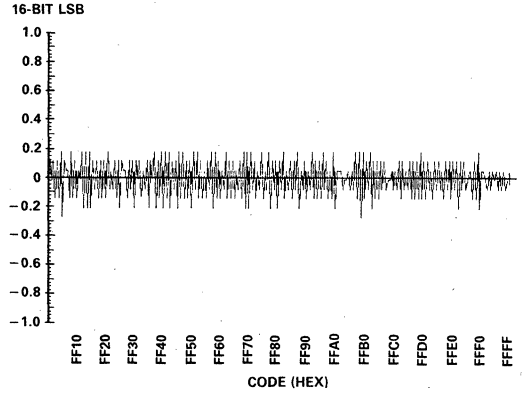


Figure 5. Typical DNL at Segment Boundary Transitions



a. Segment 1



b. Segment 256

Figure 6. Typical DNL Within Segments

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0.0000V when the inputs are loaded with 8000H is called the Bipolar Zero Error. It is tested on the AD569 with ±5 volts applied to the reference terminals.

MULTIPLYING FEEDTHROUGH ERROR: This is the error due to capacitive feedthrough from the reference to the output with the input registers loaded with all zeroes.

FULL-SCALE ERROR: The AD569's voltage dividing architecture gives rise to a fixed full-scale error which is independent of the reference voltage. This error is trimmed by adjusting the voltage applied to the $+V_{REF}$ terminals.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The charge injected into the analog output when a new input is latched into the DAC register gives rise to the Digital-to-Analog Glitch Impulse. Glitches can be due to either time skews between the input bits or charge injection from the internal switches. Glitch Impulse for the AD569 is mainly due to charge injection, and is thus measured with the reference connections tied to ground. It is specified as the area of the glitch in nV-secs.

TOTAL ERROR: The worst-case Total Error is the sum of the fixed full-scale and offset errors and the linearity error, which is ratiometric to the reference voltage.

POWER SUPPLY AND REFERENCE VOLTAGE RANGES

The AD569 is specified for operation with ±12 volt power supplies. With ±10% power supply tolerances, the maximum reference voltage range is ±5 volts. Reference voltages up to ±6 volts can be used but linearity will degrade if the supplies approach their lower limits of ±10.8 volts (12 volts – 10%).

If ±12 volt power supplies are unavailable in the system, two 3V zener diodes or voltage regulators can be used to drop ±15 volt supplies to ±12 volts. Also, a single 6V zener can drop one of the supplies to 9 volts with the other supply left at 15V. Asymmetrical power supplies can be used since the AD569's output is referenced to $-V_{REF}$ only and thus floats relative to logic ground (GND, pin 18). Assuming a worst-case ±1.5 volt tolerance on both supplies (10% of 15 volts), the maximum reference voltage ranges would be +6 and −2 volts for $+V_S$ = +15V and $-V_S$ = −9V, and +2 to −8 volts for $+V_S$ = 9V and $-V_S$ = −15V.

If both ±15 volt and ±5 volt supplies are available, they can be used without adjustment. A combination of $+V_S$ = +15V and $-V_S$ = −5V can support a maximum reference range of 0 to 6 volts, while supplies of $+V_S$ = +5V and $-V_S$ = −15V can be used for reference ranges up to 0 to −8 volts. Again, ±10% power supply tolerances are assumed.

NOTE: Operation with $+V_S$ = +5V alters the input latches' operating conditions causing minimum write pulse widths to extend to 1μs or more. Control signals $\overline{CS}$, $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ should, therefore, be tied low to render the latches transparent.

No timing problems exist with operation at $+V_S$ = 9V and $-V_S$ = −15V. However, 10% tolerances on these supplies generate a worst-case condition at $-V_S$ = −16.5V and $+V_S$ = +7.5V (assuming $+V_S$ is derived from a +15V supply). Under these conditions, write pulse widths can stretch to 200ns with similar degradation of data setup and hold times. However, ±0.75V tolerances (±5%) yield minimal effects on digital timing with write pulse widths remaining below 100ns.

ANALOG CIRCUIT CONNECTIONS

The AD569 is intended for use in applications where high resolution and stability are critical. Designed as a multiplying D/A converter, the AD569 may be used with a fixed dc reference or an ac reference. V_{REF} may be any voltage or combination of voltages at $+V_{FORCE}$ and $-V_{FORCE}$ that remain within the bounds set for reference voltages as discussed in the power

supply range section. Since the AD569 is a multiplying D/A converter, its output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the reference terminal. The transfer function is $V_{OUT} = D \cdot V_{REF}$ where D is the fractional binary value of the digital word applied to the converter using offset-binary coding. Therefore, the output will range from $-V_{REF}$ for a digital input code of all zeros (0000_H) to $+V_{REF}$ for an input code of all ones ($FFFF_H$).

For applications where absolute accuracy is not critical, the simple reference connection in Figure 7 can be used. Using only the reference force inputs, this configuration maintains linearity and 16-bit monotonicity, but introduces small, fixed offset and gain errors. These errors are due to the voltage drops across resistors R_A and R_B shown in Figure 8. With a 10V reference voltage, the gain and offset errors will range from 80 to 100mV. Note that the resistance between the force and sense terminals cannot be measured with an ohmmeter; the layout of the thin-film resistor string adds approximately 4kΩ of resistance (R_S) at the sense tap which is transparent in actual circuit operation.

Resistors R_A and R_B were included in the first resistor string to avoid degraded linearity due to uneven current densities at the string's endpoints. Similarly, linearity would degrade if the reference voltage were connected across the reference sense terminals. For those applications in which precision references and high accuracy are critical, buffer amplifiers are used at $+V_{REF}$ and $-V_{REF}$ as shown in Figure 9 to force the voltage across resistors R1 to R256. This insures that any errors induced by currents flowing through the resistances of the package pins, bond wires, aluminum interconnections, as well as R_A and R_B are minimized. Errors will arise, however, as the buffer amplifiers' bias currents flow through R_S (4kΩ). If the bias currents are sufficiently large to induce such errors, resistance can be inserted at the noninverting terminal (R_{BC}) of the buffer amplifiers to minimize the errors. Suitable amplifiers are the AD517, AD OP-07, AD OP-27, and AD711.

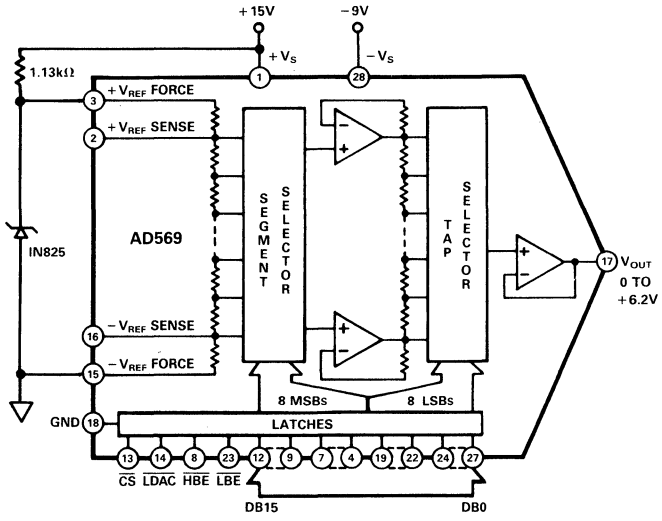


Figure 7. Simple Reference Connection

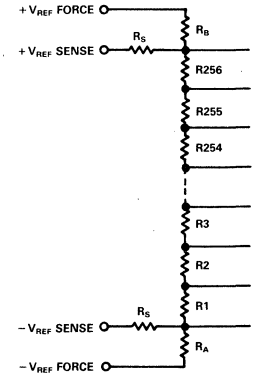


Figure 8. MSB Resistor Divider

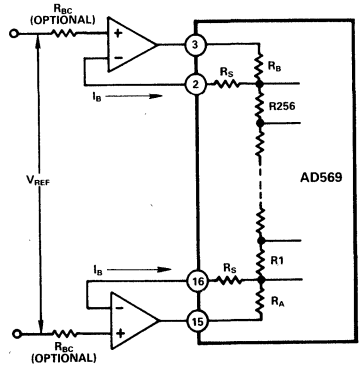


Figure 9. Reference Buffer Amplifier Connections

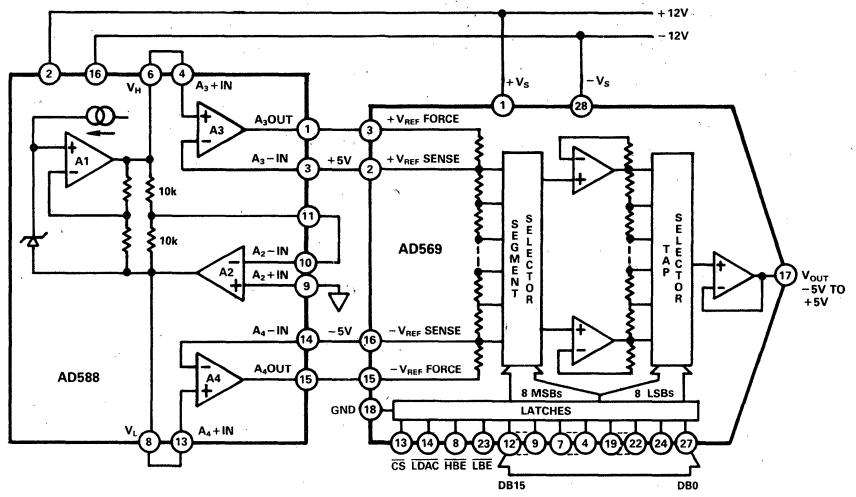


Figure 10. Ultra Low Drift ±5V Tracking Reference

Figures 10, 11, and 12 show reference configurations for various output ranges. The pin-programmable AD588 shown in Figure 10 provides a tracking ±5V option or single +5V and −5V outputs with 1-3ppm/°C temperature stability. Buffer amplifiers are included for direct connection to the AD569. The low-cost AD584 offers 2.5V, 5V, and 7.5V options and can be connected for ±5V tracking outputs as shown in Figure 12. If $-V_S$, rather than $+V_S$, is used to power the AD584, the same negative output ranges can be generated.

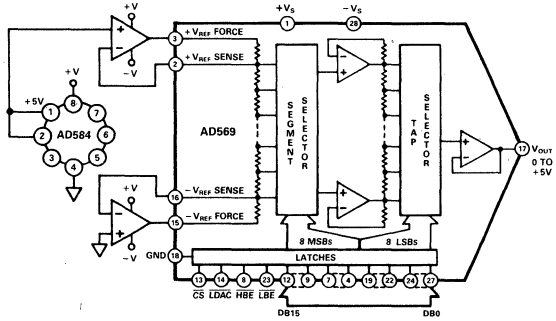


Figure 11. Low Cost Programmable Reference

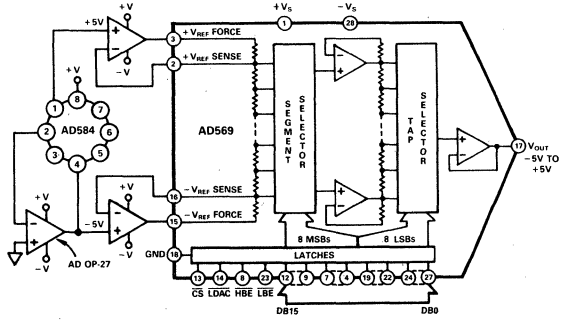
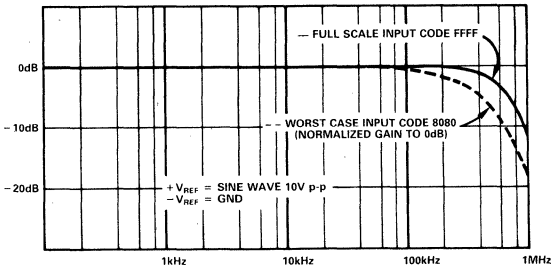


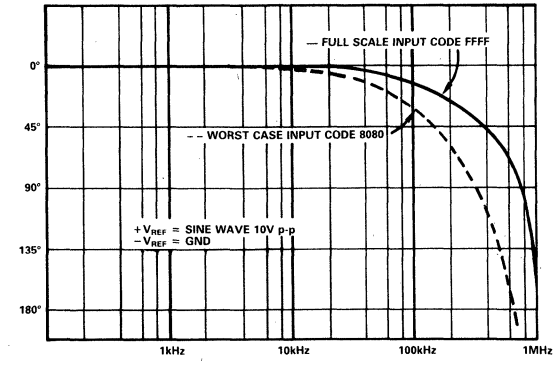
Figure 12. Low Cost ±5V Tracking Reference

MULTIPLYING PERFORMANCE

The AD569's multiplying mode gain and phase characteristics are illustrated in Figure 13. Figure 13a shows the full power multiplying bandwidth while Figure 13b shows the associated phase shift. Performance is plotted for both a full-scale input of $FFFF_H$ and an input of 8080_H. An input of 8080_H represents worst-case conditions since it places the buffer taps at the midpoints of both dividers. Figure 14 illustrates the AD569's ability to resolve 16-bits (where 1LSB is 96dB below full scale) while keeping the noise floor below −130dB with an ac reference of 1V rms at 200Hz.

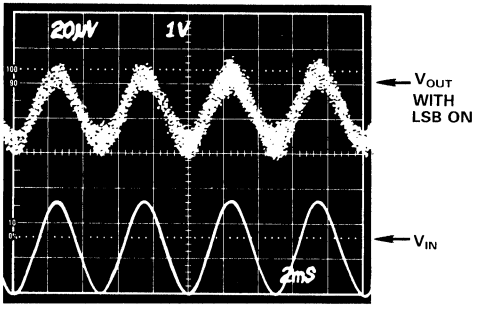


a. Bandwidth

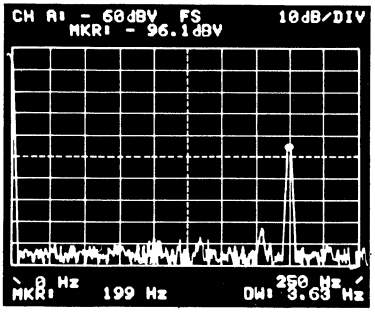


b. Phase Shift

Figure 13. Full Power Multiplying Performance



a. Time Domain



b. Frequency Domain

Figure 14. Multiplying Mode Performance (Input Code 0001_H)

Multiplying feedthrough is due to capacitive coupling between the reference inputs and the output. As shown in Figure 15, feedthrough remains below −100dB at ac reference frequencies up to 10kHz under worst-case conditions (hex input code 0000).

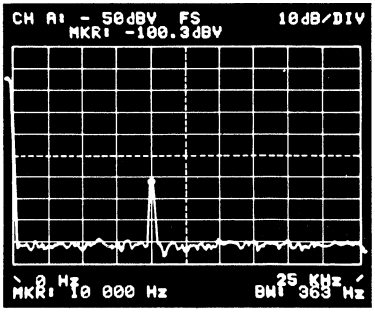


Figure 15. Multiplying Feedthrough

GROUNDING RULES

It is generally considered good engineering practice to use bypass capacitors on the device supply voltage pins and to insert small valued resistors in the supply lines to provide a measure of decoupling between various circuits in a system. With the AD569, bypass capacitors of 4.7μF or more and series resistors of 10Ω are needed to slow down fast rising edges on the supply lines which could latch the device. Referred to the reference connection only, the AD569's analog output floats relative to the device's ground pin. Therefore, the supplies should be decoupled to the load ground, which need not be at the same potential as pin 18. The GND pin only establishes the reference for the logic inputs.

NOISE

In many high resolution systems, noise is often the limiting factor. Using a 10 volt span, a 16-bit LSB (−96dB) is only 152μV, so the noise floor must remain below that in the frequency range of interest. The AD569's noise spectral density is shown in Figures 16 and 17. The lowband noise spectrum in Figure 16 shows the 1/f corner frequency at 1.2kHz, while Figure 17 shows the wideband noise to be below 40nV/$\sqrt{Hz}$.

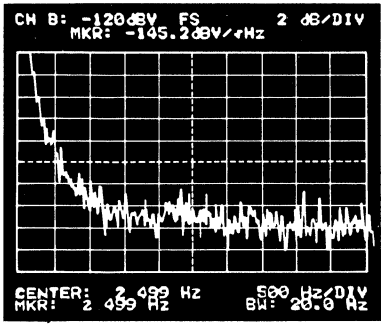


Figure 16. Lowband Noise Spectrum

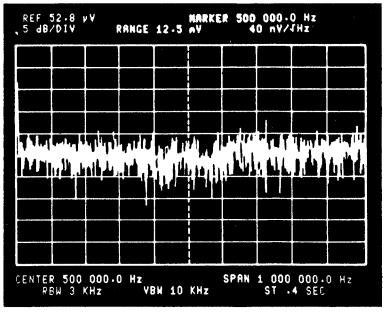


Figure 17. Wideband Noise Spectrum

DIGITAL CIRCUIT CONNECTIONS

The AD569's truth table appears in Table I. The High Byte Enable ($\overline{HBE}$) and Low Byte Enable ($\overline{LBE}$) inputs load the upper and lower bytes of the 16-bit input when Chip Select ($\overline{CS}$) is valid (low). A similar strobe to Load DAC ($\overline{LDAC}$) loads the 16-bit input into the DAC register and completes the DAC update. The DAC register can either be loaded with a separate write cycle or synchronously with either of the 8-bit registers in the first rank. The simultaneous update of several AD569's can be achieved by controlling their $\overline{LDAC}$ inputs with a single control signal.

$\overline{CS}$	$\overline{HBE}$	$\overline{LBE}$	$\overline{LDAC}$	OPERATION
1	X	X	X	No Operation
X	1	1	1	No Operation
0	0	1	1	Enable 8MSBs of First Rank
0	1	0	1	Enable 8LSBs of First Rank
0	1	1	0	Enable 16-Bit DAC Register
0	0	0	0	All Latches Transparent

Table I. AD569 Truth Table

All four control inputs are active low and TTL-compatible. The latches are level-triggered, so if the DAC register is loaded directly off the bus, any invalid data at the digital inputs will cause spurious analog outputs as $\overline{LDAC}$ goes valid. This can be avoided by using an extra write cycle to load the DAC register or by delaying the write strobe pulse until the data is valid. If the pulse is delayed, the appropriate data hold time must still be obeyed (see Timing Characteristics).

Whenever possible, the write strobe signal should be applied to $\overline{HBE}$ and $\overline{LBE}$ with the AD569's decoded address applied to $\overline{CS}$. With a minimum pulse width of 60ns at $\overline{HBE}$ and $\overline{LBE}$, this allows the AD569 to interface to the fastest microprocessors. Actually, data can be latched with narrower pulses, but the data setup and hold times must be lengthened.

16-Bit Microprocessor Interfaces

Since 16-bit microprocessors supply the AD569's complete 16-bit input in a single write cycle, the DAC register is often unnecessary. If so, it should be made transparent by grounding $\overline{LDAC}$. The DAC's decoded address should be applied to $\overline{CS}$, with the write strobe applied to $\overline{HBE}$ and $\overline{LBE}$ as shown in the 68000 interface in Figure 18.

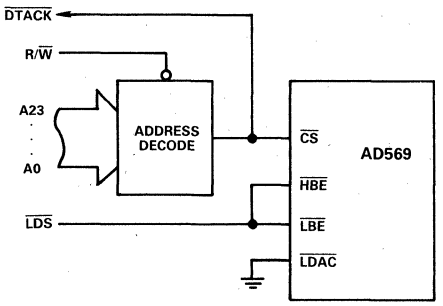
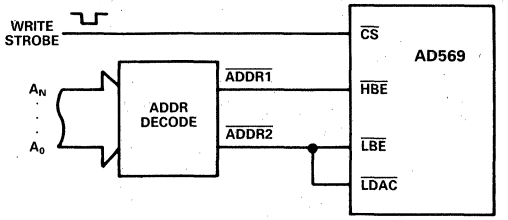
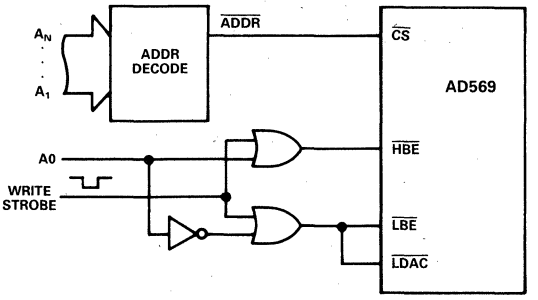


Figure 18. AD569/68000 Interface



a. Simple Interface



b. Fast Interface

Figure 19. 8-Bit Microprocessor Interface

8-Bit Microprocessor Interfaces

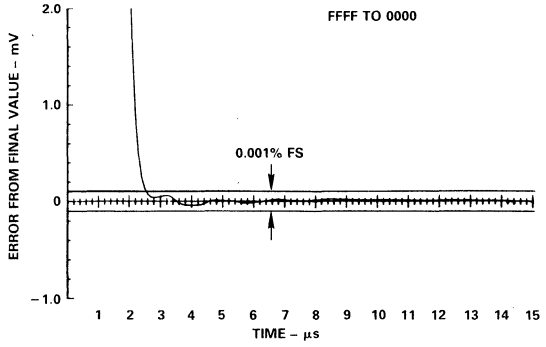
Since 8-bit microprocessors require two write cycles to provide the AD569's 16-bit input, the DAC register must be utilized. It is most often loaded as the second byte enters the first rank of latches. This synchronous load method, shown in Figure 19, requires $\overline{LDAC}$ to be tied to either $\overline{LBE}$ or $\overline{HBE}$, depending on the byte loading sequence. In either case, the propagation delay through the first rank gives rise to longer timing requirements as shown in Figure 2. If the DAC register ($\overline{LDAC}$) is controlled separately using a third write cycle, the minimum write pulse on $\overline{LDAC}$ is 70ns, as shown in Figure 1.

Two basic methods exist for interfacing the AD569 to an 8-bit microprocessor's address and control busses. In either case, at least one address line is needed to differentiate between the upper and lower bytes of the first rank ($\overline{HBE}$ and $\overline{LBE}$). The simplest method involves applying the two addresses directly to $\overline{HBE}$ and $\overline{LBE}$ and strobing the data using $\overline{CS}$ as shown in Figure 19a. However, the minimum pulse width on $\overline{CS}$ is 70ns with a minimum data setup time of 60ns. If operation with a shorter pulse width is required, the base address should be applied to $\overline{CS}$ with an address line gated with the strobe signal to supply the $\overline{HBE}$ and $\overline{LBE}$ inputs (see Figure 19b). However, since the write pulse sees a propagation delay, the data still must remain valid at least 20ns after the rising edge of the delayed write pulse.

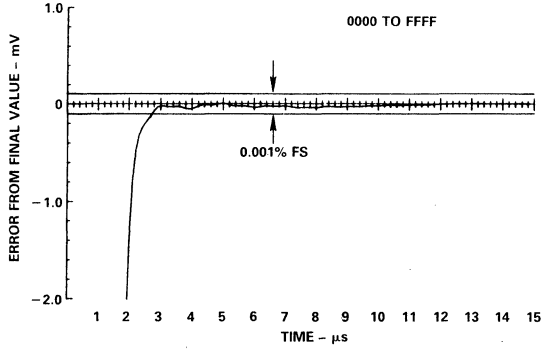
OUTPUT SETTLING

The AD569's output buffer amplifier typically settles to within ±0.001% FS of its final value in 3μs for a 10V step. Figure 20 shows settling for positive and negative full-scale steps with no load applied. Capable of sourcing or sinking 5mA, the output buffer can also drive loads of 1kΩ and 1000pF without loss of

stability. Typical settling to 0.001% under these worst-case conditions is 4μs, and is guaranteed to be a maximum of 6μs. The plots of Figure 20 were generated using the settling test procedure discussed in the next section.



a. Turn-On Settling



b. Turn-Off Settling

Figure 20. Full-Scale Output Settling

TESTING 16-BIT DAC SETTLING

Because the settling time of a 16-bit D-A converter is so difficult to measure accurately, manufacturers often estimate the value based on the appropriate number of time constants. However, a special technique, developed specifically for the AD569, resolves performance to within 100μV with 10μV repeatability.

The method, performed under program control, averages the output of a high-resolution strobed comparator and feeds that signal back to the noninverting input for use as an offset adjustment. An integrator compares the averaged output with a 1.4V reference several times, after which the comparator's output reflects an appropriate 50-50 balance of high and low results.

A programmable pulse generator drives the digital inputs of the converter with a pulse train whose period is long enough to ensure that the converter will properly settle (see Figure 21). The comparator's strobe input is also driven by a pulse train, one that is slightly offset in time from that applied to the converter.

The converter's output can then be mapped indirectly by varying the strobe delay time and measuring the change in the comparator's offset with a precision digital voltmeter. A 100-to-1 divider improves the meter's effective resolution. If a computer controls the two programmable pulse generators, the test procedure can be fully automated.

In practice, a measurement starts when the strobe signal is delayed long enough after the input signal to the converter to ensure that the device under test has settled. The loop offset value measured at this moment represents the final value. Next, the delay is shortened, and after the filtering loop has settled, the resultant offset change determines the converter's output change.

The strobe delay time is decreased in increments suitable for the resolution desired until the converter goes outside the desired error window. In the setup described, the generator can produce pulses as short as 1ns. The settling time is the strobe delay period when the offset change first becomes larger than the desired error band – typically 1/2LSB.

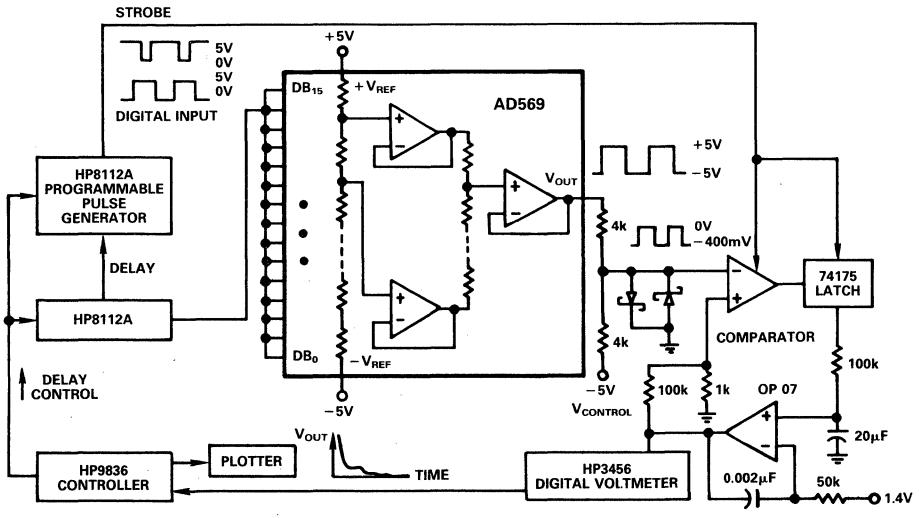


Figure 21. DAC Settling Test Fixture

Schottky diodes limit the input to the high-resolution comparator to ±500mV. A clamped node on that input is formed by two 4kΩ load resistors, and the voltage on the lower one must be set to a value equal in magnitude but opposite in polarity to the expected final value of the converter's output for a transition of interest.

Rather than tying together all the digital inputs for a full-scale transition test, the inputs can be driven by two inputs 180° out of phase. Gating the two pulse trains to the separate inputs allows any type of transition to be measured, for example, LSB transitions.

The measurement technique extends beyond D/A converter testing. For instance, it can evaluate the settling times of operational amplifiers to within 0.0007%. Here, the AD569 D/A converter could be used as a precision analog pulse generator.

APPLICATION

High-Speed, High-Resolution Subranging ADC

A D/A converter is an integral component in subranging ADCs. The conversion process involves sequentially performing two or three low resolution A/D "flash" conversions; each subsequent conversion is aimed at increasing the ADC's resolution. This method requires more hardware than the successive-approximation and integration approaches, but results in much shorter conversion times. On the other hand, "flash" ADCs are faster than subranging ADCs but the brute force flash technique is impossible at high resolutions.

The subranging ADC shown in Figure 22 completes a conversion in less than 20μs, including the sample-hold amplifier's sample time. The sample-hold amplifier is allocated 5μs to settle to 16 bits.

Before the first flash, the analog input signal is routed through the AD630 at a gain of +1. The lower AD7820 quantizes the signal to the 8-bit level within 1.4μs, and the 8-bit result is routed to the AD569 via a digital latch which holds the 8-bit word for the AD569 and the output logic.

The AD569's reference polarity is reversed so that a full-scale output is −5V and zero scale is 0V, thereby subtracting an 8-bit approximation from the original sampled signal. The residue from the analog subtraction is then quantized by the second 8-bit flash conversion to recover the 8LSBs. Even though only the AD569's upper 8MSBs are used, the AD569's accuracy defines the A/D converter's overall accuracy. Any errors are directly reflected in the output.

Preceding the second flash, the residue signal must be amplified by a factor of 256. The OP-37 provides a gain of 25.6 and the AD630 provides another gain of 10. In this case, the AD630 acts as a gain element as well as a channel control switch.

The second flash conversion yields a 9-bit word. This provides one extra bit of overlap for digital correction of any errors that occurred in the first flash. The correction bit is digitally added to the first flash before the entire 16-bit output is strobed into the output register.

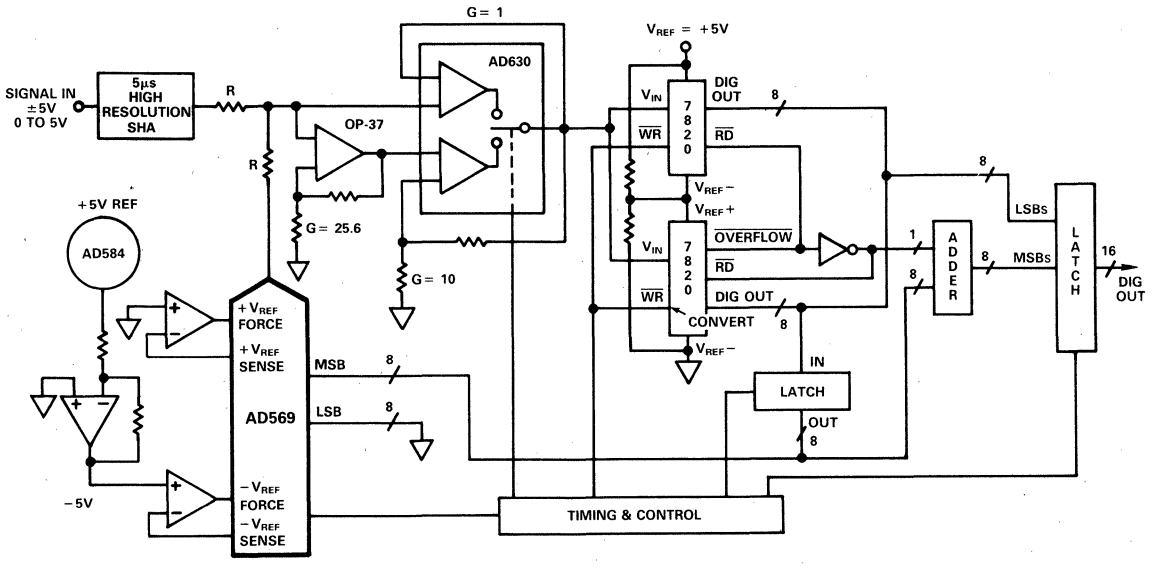


Figure 22. 16-Bit Subranging ADC

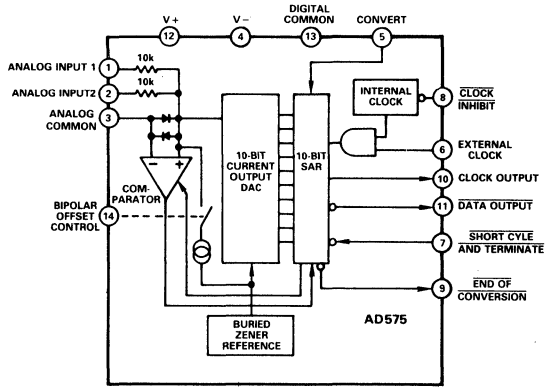
Complete 10-Bit A/D Converter with Serial Output

AD575*

FEATURES

Complete Serial Output 10-Bit A/D Converter with Reference, Clock and Comparator
30μs Conversion
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction
Internal or External Clock
Triggered or Continuous Conversions
Short Cycle Capability

AD575 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD575 is a complete 10-bit successive-approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and serial interface on a single chip. No additional components are required to perform a full-accuracy 10-bit conversion in 30μs.

The AD575 incorporates the most advanced integrated circuit design and processing technology available. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the SiCr thin-film resistor ladder network at the wafer stage insures high accuracy, which is maintained with a temperature-compensated sub-surface zener reference.

Operating on supplies of +5V and −12V to −15V, the AD575 will accept full scale analog inputs of 0V to +10V, 0V to +20V, −5V to +5V or −10V to +10V. The rising edge of a positive pulse on the CONVERT line initiates the conversion cycle. Eleven pulses will appear at the CLOCK OUTPUT pin with data valid on the falling edges of the clock waveform. The data is presented serially beginning with the MSB which is valid on the falling edge of the second clock pulse. The part may be programmed to perform 8-bit conversions or short cycled to 2-, 4-, 6- or 8-bit word lengths. $\overline{EOC}$ indicates that conversion is complete. The AD575 may be synchronized to an external clock if desired.

The AD575 is available in two versions for the 0 to +70°C temperature range, the AD575J and AD575K. The AD575S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

***Protected by U.S. Patent Nos. 3,940,760; 4,400,689; and 4,400,690.**

Two package types are available. All versions are offered in a 14-pin hermetically-sealed ceramic DIP. The AD575J and AD575K are also available in a 14-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD575 is a complete 10-bit A/D converter. No external active components or control signals are required to perform a conversion.
2. The serial output of the AD575 allows a wide range of microprocessor interfacing and data transmission possibilities.
3. The device offers true 10-bit relative accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD575 adapts to unipolar or bipolar analog inputs by grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.
6. The AD575 can be synchronized to an external clock.
7. Conversions can be initiated externally or internally.
8. The AD575 can be short-cycled to 8 bits by pin programming.
9. The Short Cycle and Terminate feature allows the user to program conversions of 2, 4, 6 or 8 bits.

SPECIFICATIONS (@ 25°C, V+ = +5V, V− = −12V or −15V, unless otherwise noted)

	AD575J			AD575K			AD575S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION										
For Which No Missing Codes is Guaranteed	10			10			10			Bits
T_{min} to T_{max}	9			10			10			Bits
UNIPOLAR OFFSET			±2			±1			±2	LSB
T_{min} to T_{max}			±2			±1			±2	LSB
BIPOLAR ZERO			±2			±1			±2	LSB
T_{min} to T_{max}			±2			±1			±2	LSB
GAIN ERROR[1]		±2				±2			±2	LSB
GAIN DRIFT[2]										
T_{min} to +25°C			±2			±1			±5	LSB
+25°C to T_{max}			±4			±2			±5	LSB
RELATIVE ACCURACY[3]			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
POWER SUPPLY REJECTION[4]										
Positive Supply:										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply:										
−15.75V≤V−≤−14.25V			±2			±1			±2	LSB
−12.6V≤V−≤−11.4V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE										
Pin 1, Pin 2	6	10	14	6	10	14	6	10	14	kΩ
ANALOG INPUT RANGES										
Unipolar		0 to 10			0 to 10			0 to 10		V
		0 to 20			0 to 20			0 to 20		V
Bipolar		−5 to +5			−5 to +5			−5 to +5		V
		−10 to +10			−10 to +10			−10 to +10		V
OUTPUT CODING										
Unipolar	NEGATIVE TRUE BINARY			NEGATIVE TRUE BINARY			NEGATIVE TRUE BINARY			
Bipolar	NEGATIVE TRUE OFFSET BINARY			NEGATIVE TRUE OFFSET BINARY			NEGATIVE TRUE OFFSET BINARY			
LOGIC OUTPUTS (T_{min} to T_{max})										
V_{OL} @ I_{SINK} = 3.2mA	0		0.4	0		0.4	0		0.4	V
V_{OH} @ I_{SOURCE} = 0.5mA	2.4		5.0	2.4		5.0	2.4		5.0	V
LOGIC INPUTS (T_{min} to T_{max})										
I_{INH} @ V_{IN} = 5V[5]			+50			+50			+50	μA
I_{INL} @ V_{IN} = 0V[5]	−800			−800			−800			μA
V_{INH}	2.0		5.5	2.0		5.5	2.0		5.5	V
V_{INL}	0		0.8	0		0.8	0		0.8	V
CONVERSION TIME (T_{min} to T_{max})										
Internal Clock	10	20	30	10	20	30	10	20	30	μs
External Clock	25			25			25			μs
POWER SUPPLY										
V+	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	V
V−	−11.4		−15.75	−11.4		−15.75	−11.4		−15.75	V
OPERATING CURRENT										
V+		15	25		15	25		15	25	mA
V−		9	15		9	15		9	15	mA

NOTES

[1]Gain Error is specified with a 15Ω resistor in series with the 10V input (Pins 1 and 2 tied together) or a 30Ω resistor in series with the 20V input (Pin 1 with Pin 2 tied to analog common). Gain Error is guaranteed trimmable to zero (see text).

[2]The gain drift is calculated from gain measurements at the extremes of the temperature range under consideration.

[3]Relative Accuracy, also referred to as Integral Linearity, is defined as the deviation of the code transition points from the ideal transfer points on a straight line from zero to full-scale. It is also a measure of the error which remains when offset and full scale errors are trimmed to zero in an application.

[4]Measured at full scale.

[5]These specifications apply to the CONV, XCL, and $\overline{SCAT}$ inputs. $\overline{CLI}$ is hardwired to DGND or $+V_S$ in most applications. Typically I_{INH} = +350μA and I_{INL} = 120μA for the $\overline{CLI}$ input.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Inputs	(V−) −0.3V to +22V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

NOTE
All pins must be kept more positive than (V−) −0.3V.

FUNCTIONAL DESCRIPTION

A block diagram of the AD575 is shown in Figure 1. A conversion is initiated by a positive pulse on the CONVERT line. $\overline{EOC}$ goes high within 150ns indicating that a conversion has started. The internal 10-bit current-output DAC is sequenced by the successive approximation register (SAR) from most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 10kΩ input resistor(s). The comparator determines whether the addition of each successively-weighted bit current causes the DAC current to be higher or lower than the input current. If the sum is less the bit is left on ($\overline{DO}$ set low). If the sum is more, the bit is turned off ($\overline{DO}$ set high). The result of each bit decision is passed to $\overline{DO}$ on the rising edge of CO.

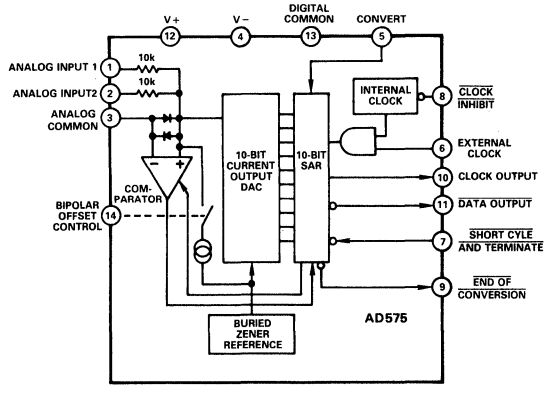


Figure 1. AD575 Functional Block Diagram

After all bits have been tested, the DAC output current will match the input signal current to within 0.05% (1/2LSB). $\overline{EOC}$ returns low after the final bit decision to indicate that the AD575 has been reset and is ready to perform a new conversion. The output data stream can be synchronized to an external clock using the XCL input and short cycled to any desired word length using the $\overline{SCAT}$ line.

The AD575 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is to connect the power supplies (+5V and −12V or −15V), and the analog input. The pinout is shown in Figure 2.

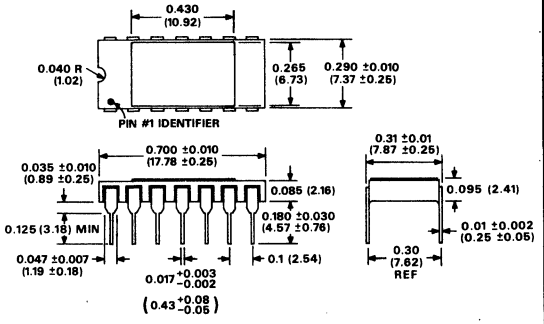
AD575 ORDERING GUIDE

Model	Package	Temperature Range−°C	Relative Accuracy
AD575JN	N14A	0 to +70	±1LSB max
AD575KN	N14A	0 to +70	±1/2LSB max
AD575JD	D14A	0 to +70	±1LSB max
AD575KD	D14A	0 to +70	±1/2LSB max
AD575SD	D14A	−55 to +125	±1LSB max

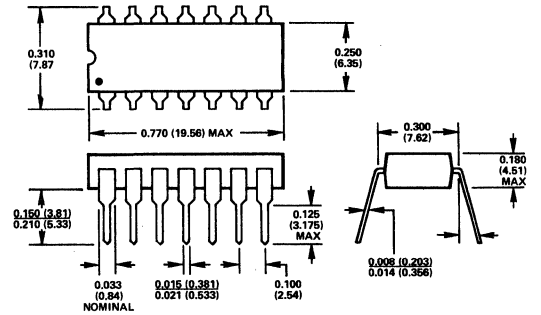
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-PIN CERAMIC DIP PACKAGE (D14A)



14-PIN PLASTIC DIP PACKAGE (N14A)



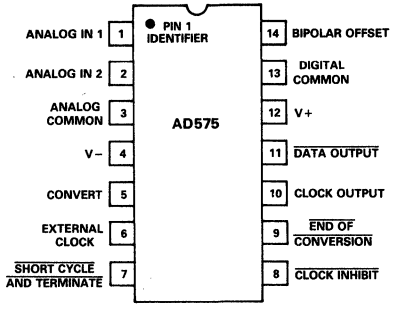


Figure 2. AD575 Pin Connections

ANALOG INPUT CONNECTIONS

The AD575 can be configured for unipolar or bipolar operation on 10V span or 20V span input signals. The appropriate input range is selected by connecting pins 2 and 14 according to the table of Figure 3.

The AD575's low offset and gain errors (shown in the Specifications) are adequate for most applications. For these cases, a fixed gain resistor (R2 in Figure 3) is the only external component, in addition to any power supply decoupling that may be required. Pins 3 and 13 should be connected directly together.

Figure 3 shows a trimming circuit that can be used to adjust the offset to zero, using the appropriate value of the R1 potentiometer as shown in the table. If gain trim is required, R2 should also be replaced by the appropriate potentiometer as shown in the table.

ANALOG INPUT RANGE	CONNECTIONS PIN 2	PIN 14	COMPONENTS R1 (OFFSET)	R2 (GAIN)
0V TO +10V	PIN 1	PIN 13	10Ω	15Ω FIXED OR 50Ω POT
0V TO +20V	PIN 3	PIN 13	20Ω	30Ω FIXED OR 100Ω POT
−5V TO +5V	PIN 1	OPEN	10Ω	15Ω FIXED OR 50Ω POT
−10V TO +10V	PIN 3	OPEN	20Ω	30Ω FIXED OR 100Ω POT

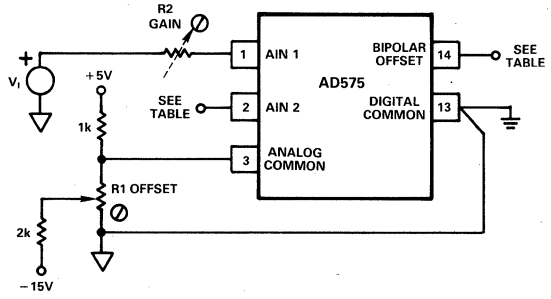


Figure 3. AD575 Input Circuit Showing Offset and Gain Adjustment

UNIPOLAR MODE OPERATION

In unipolar mode, the nominal location of the low side transition of the first code (1111111110) occurs at an input voltage of +1LSB (10mV for the 10V span, 20mV for the 20V span). The offset error of the AD575 can be trimmed out, if required, by applying an input voltage of +1LSB to the analog input and adjusting R1 until the low side transition of the first code occurs.

If the Gain Error needs to be trimmed, the gain resistor should be replaced with a potentiometer according to Figure 3. The nominal location of the low side transition of the full scale code (0000000000) in unipolar mode is full scale minus 1LSB (9.99V for 10V span, 19.98V for 20V span). Once the offset has been adjusted, the full scale range can be set by adjusting the gain potentiometer.

BIPOLAR CONNECTION

If the bipolar offset control (pin 14) is left open, the AD575 will accept bipolar input voltages with 0V as the nominal bipolar zero point. The input voltage corresponding to the low side transition of the mid-scale code (0111111111) is −1/2LSB (−5mV for 10V spans and −10mV for 20V spans). The nominal location of the code transitions are therefore offset by 1/2LSB as shown in Figure 4. This offset may be adjusted using the trim scheme shown in Figure 3 with a 1.2kΩ resistor in place of the 1kΩ resistor shown.

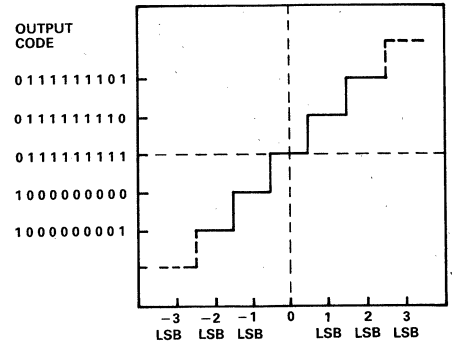


Figure 4. AD575 Transfer Characteristic (Bipolar Operation)

The gain error should be adjusted after any offset adjustment. An input voltage of full scale minus 1 1/2LSBs is applied (4.985V for −5V to +5V range, 9.971V for −10V to +10V range) and R2 is adjusted until the low-side transition of the full scale code (0000000000) occurs.

The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 5.

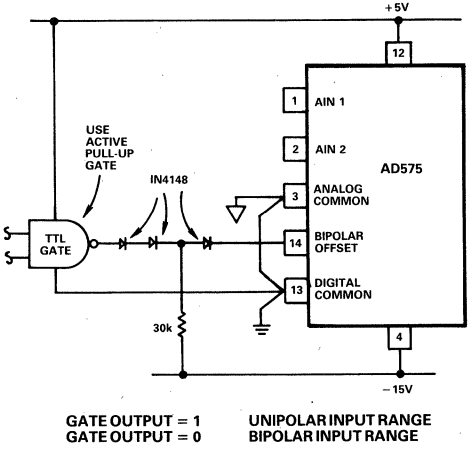


Figure 5. Bipolar Offset Controlled by Logic Gate

CONTROL AND TIMING OF THE AD575

The AD575 has a flexible control architecture which supports several operating modes. It can provide its own clock or it can be synchronized to an external clock. Conversions can be initiated externally, or the part can perform continuous conversions yielding a stream of output data. In addition, the AD575 can be short-cycled to any of several convenient data word lengths to tailor the output to the specific input requirements of the system. Figure 6 shows the control logic diagram of the AD575. The four inputs which control the operation of the AD575 are CONV (convert), $\overline{CLI}$ (clock inhibit), XCL (external clock), and $\overline{SCAT}$ (short cycle and terminate). Three outputs are provided: $\overline{DO}$ (Data Out), CO (Clock Out), and $\overline{EOC}$ (End of Conversion).

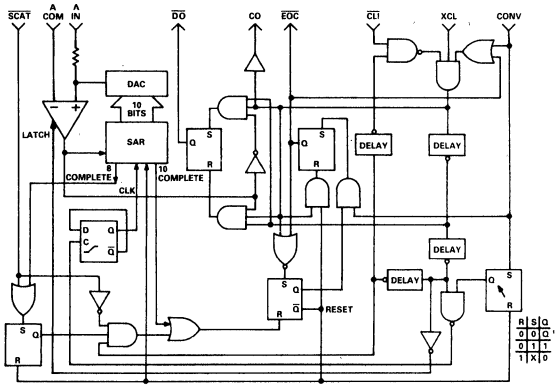


Figure 6. AD575 Control Logic Diagram

EXTERNALLY INITIATED CONVERSIONS

Figure 7 is the timing diagram which illustrates the operation of the AD575 with an externally applied convert signal. Conversions are initiated by a positive-going pulse applied to the CONV (convert) input. This pulse should be at least 250ns wide and should return low before $\overline{EOC}$ returns low to prevent the initiation of a second conversion. If the internal clock is used, the clock will start on the rising edge of the convert start pulse. If an external clock is used, the falling edge of the clock must occur no earlier than 900ns following the rising edge of the convert command.

INTERNAL CLOCK MODE

The AD575 can be configured for internal clock operation by tying $\overline{CLI}$ and XCL to +5V. CO (clock output) provides the necessary synchronizing information in this mode. Data is transferred to $\overline{DO}$ on the rising clock edge and is stable on the falling edge. The duty cycle of the CO waveform in this mode will be in the range of 30% to 70%.

EXTERNAL CLOCK MODE

When $\overline{CLI}$ is connected to digital common, an external clock can be applied to XCL. The external clock should have a maximum frequency of 450kHz with a minimum of 900ns in the high or low phase. Arbitrarily slow clocks may be used as long as these minimum high and low periods are observed. Conversion time will increase as clock frequency decreases. Each data bit will be stable within 150ns of the rising edge of the associated external clock pulse and will remain stable until the rising edge of the subsequent clock pulse. Data is guaranteed to be stable on the falling edge of the clock pulse.

The state of the $\overline{DO}$ output during the first clock period is undefined but it is stable until the rising edge of the second clock period. The MSB appears at $\overline{DO}$ during the second clock period. The subsequent data bits are then clocked out until the N^{th} bit or LSB is clocked out on the $(N+1)^{th}$ clock pulse. $\overline{EOC}$ returns low within 150ns of the rising edge of this final clock pulse. In internal clock mode, the output clock pulse associated with the LSB is shorter than the others but the LSB is guaranteed to be stable on the falling edge of this pulse. The LSB will remain stable until a new conversion is initiated. The value of N will be 10 unless the conversion has been short cycled (see "short cycle and terminate" text).

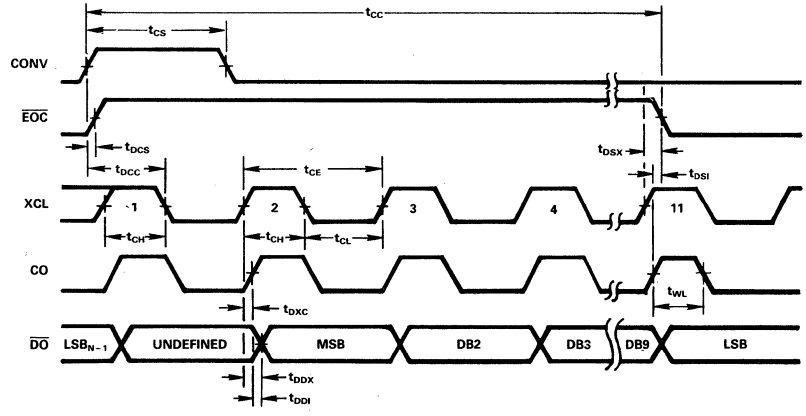


Figure 7. Externally Initiated Conversions

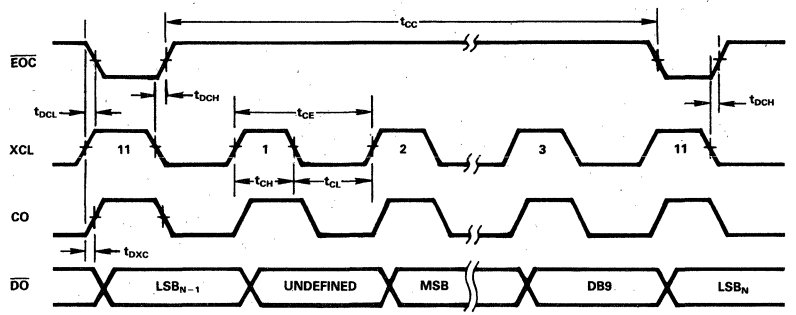


Figure 8. Continuous Conversion Mode (CONV. Held High)

CONTINUOUS CONVERSIONS

Figure 8 is the timing diagram associated with the continuous conversion mode of operation. If CONV is high when $\overline{EOC}$ goes low, another conversion will begin immediately. $\overline{EOC}$ will be set (high) following the falling edge of the $(N+1)^{st}$ CO pulse and conversion commences with the rising edge of the next CO pulse. The $(N+1)^{st}$ CO pulse is not shortened in this mode. If CONVERT is held high the AD575 will put out a continuous stream of conversions, punctuated by $\overline{EOC}$ which will mark the last clock pulse of a conversion. $\overline{EOC}$ will remain low until the falling edge of CO, the output clock, in this mode. Therefore, the rising edge of $\overline{EOC}$ may be used to signal that conversion is complete and that data is transferred. This sequence is useful for initiating parallel dumps from a serially loaded shift register.

SHORT CYCLE AND TERMINATE

For normal 10-bit operation, the Short Cycle and Terminate ($\overline{SCAT}$) line should be tied high. If 8-bit conversions are required, $\overline{SCAT}$ should be tied low. In this mode, $\overline{EOC}$ will go low after the rising edge of the ninth clock pulse to indicate that the eighth and final data bit is valid. This mode is useful when parallel loads to 8-bit data buses are desired since it avoids the complication of suppressing the 9th and 10th data bits.

Conversions of 2, 4, 6 or 8 bits can be performed by pulling $\overline{SCAT}$ low during the negative clock phase prior to the positive clock associated with the desired LSB. Figure 9 illustrates the timing associated with this mode of operation. For example, to terminate the conversion after six data bits, $\overline{SCAT}$ should be driven low during the negative clock phase following the sixth clock pulse. $\overline{EOC}$ will then go low following the rising edge of the seventh clock pulse to indicate that the sixth and final data bit is valid.

This terminate feature can also be used to program conversions of 1, 3, 5, 7 or 9 bits. However, the conversion immediately following a conversion of an odd number of data bits will be spurious. All subsequent conversions will be normal until the conversion following another odd data word length conversion.

The negative edge of the $\overline{SCAT}$ signal should always occur during the negative phase of a clock cycle and it should be held low for a minimum of 900ns. $\overline{SCAT}$ may be held low into the next conversion but it must be restored high at least one clock cycle prior to being used to terminate a conversion. If $\overline{SCAT}$ is not restored high prior to the eighth clock pulse, $\overline{EOC}$ will go low and an 8-bit short cycle will occur. Care should be taken not to pulse $\overline{SCAT}$ from high to low between conversions (when $\overline{EOC}$ is low). This would initiate a terminate sequence which will execute on the rising edge of the first clock pulse following the next Convert command.

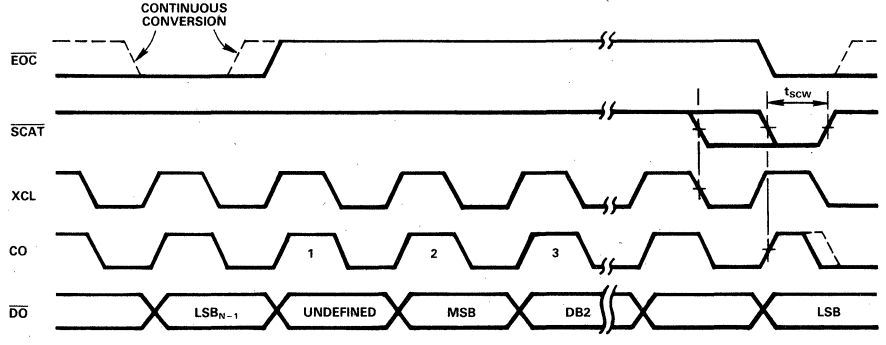


Figure 9. Short Cycle and Terminate Operation

Parameter	Symbol	Min	Typ	Max	Units
EXTERNALLY-INITIATED CONVERSIONS					
Convert Pulse Width	t_{CS}	250			ns
Convert to $\overline{EOC}$ Delay	t_{DCS}			150	ns
CO LSB Clock Pulse Width	t_{WL}	400			ns
XCL to $\overline{EOC}$ Reset	t_{DSX}	50		150	ns
↑ CO to ↓ $\overline{EOC}$ Reset Delay	t_{DSI}	20		150	ns
CONTINUOUS CONVERSIONS					
↑ XCL to ↓ $\overline{EOC}$ Reset Delay	t_{DCL}	50		150	ns
↓ XCL to ↑ $\overline{EOC}$ Delay	t_{DCH}	50		1000	ns
INTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	10	20	30	µs
CO to $\overline{DO}$ Output Delay	t_{DDI}	−100		+100	ns
EXTERNAL CLOCK TIMING					
Conversion Time	t_{CC}	25			µs
↑ XCL to $\overline{DO}$ Output	t_{DDX}	30		150	ns
XCL to CO Output	t_{DXC}	30		160	ns
↑ Convert to ↓ XCL Set-Up Time	t_{DCC}	900			ns
XCL Period	t_{CE}	2.2			µs
XCL High	t_{CH}	900			ns
XCL Low	t_{CL}	900			ns
SHORT CYCLE TIMING					
$\overline{SCAT}$ Pulse Width	t_{SCW}	900			ns

Table I. AD575 Timing Specifications

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD575

Many data acquisition systems for digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A/D converter. A SHA can be used to accurately define the exact point in time at which the signal is sampled. A SHA can also serve as a high input-impedance buffer for the AD575.

Figure 10 shows the AD575 connected to the AD585 monolithic SHA. In this configuration, the AD585 will acquire a 10V signal in less than 2µs and droop less than 1mV/ms using the on-chip hold capacitor.

$\overline{EOC}$ goes high after the conversion is initiated to indicate that a conversion is underway. In Figure 10 it is also used to put the AD585 into the hold mode while the AD575 begins its conversion cycle. (The AD585 output settles to final value well in advance of the first comparator decision within the AD575.) $\overline{EOC}$ goes low when the conversion is complete placing the AD585 back in the sample mode.

Configured as shown in Figure 10, the next conversion can be initiated after a 2µs delay to allow for signal acquisition by the AD585.

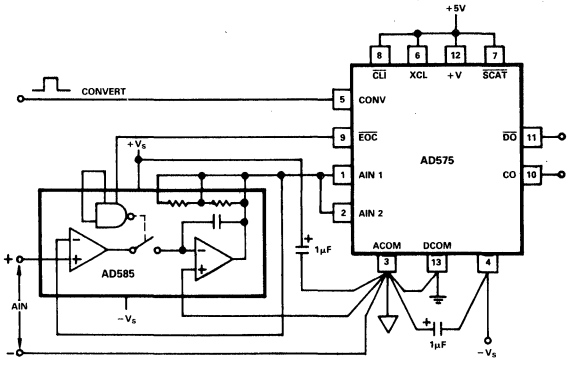


Figure 10. AD575 to AD585 Sample and Hold Interface

SUPPLY DECOUPLING AND LAYOUT

For proper operation, the AD575's power supplies should be free from high-frequency noise. The stability of the transfer function is especially sensitive to noise on the V− supply. Noise on the V+ supply can also propagate to the digital outputs.

If decoupling is required, tantalum capacitors are suggested. Best results will be obtained if the capacitors are connected directly to the appropriate pins of the AD575. Decoupling capacitors for V− should be connected between pin 4 and Analog Common (pin 3). Decoupling capacitors for V+ should be connected between pin 12 and Digital Common (pin 13).

Good circuit layout practice suggests that the AD575 and its associated analog input circuitry be kept separate from system logic circuitry to avoid unwanted interactions.

GROUNDING CONSIDERATIONS

The AD575 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common-mode voltage between the two commons. The absolute maximum voltage rating between the two commons is ±1V. A parallel pair of back-to-back protection diodes should be connected between the commons if they are not connected locally.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

AD575 TO 8085 INTERFACE

The 8085 has both serial output (SOD) and serial input (SID) capability. A simple 3 hardware line interface can be constructed between the AD575 and 8085. These leads can be opto-coupled in order to establish galvanic isolation between the two devices as shown in Figure 11.

The software routine in Table II will read a complete 10-bit data word from the AD575 in 180μs (3MHz 8085). The software generates the clock for the AD575 in order to synchronize the data output with the 8085 serial read operation.

The DATA procedure loads appropriate constants into the 8085 registers and initiates the conversion. The CONV procedure assumes that the AD575 clock was in the high state when the CONVERT pulse was generated (upon completion, this sample routine leaves the SOD line in the appropriate state to insure this). A low clock pulse is generated, and the data bit is read into the MSB of the accumulator. The data bit is then shifted into the LSB of the temporary register (L), the clock is set high, and the procedure is repeated.

After the loop has executed three times, a logical AND is performed to set the first bit (the undefined bit) to zero, and the result is placed into the high byte (H) register. The loop counter is then reset, and the CONV procedure is executed 8 more times. Upon completion of the sample routine, 10 bits of right-justified data will reside in the HL register pair.

Note that the opto-isolators invert the clock and data lines. If these are not used (no inversion present), the constants in the D and E registers should be swapped, a CMA instruction should be inserted after the RIM instruction, and an inverter should be connected between the address decoder and the CONVERT pin. Also, the results of the first pass through the routine should be ignored following power up and reset cycles to insure that the AD575 has been reset.

LABEL	MNEMONIC	OPERAND	COMMENT
DATA	MVI	B,03	Set inner loop counter to 3
	MVI	C,02	Set outer loop counter to 2
	MVI	D,CO	Setup register D for clock low
	MVI	E,40	Setup register E for clock high
	MVI	H,10	AD575 address location
	MVI	L,00	Clear temp register
	MOV	M,B	Generate CONVERT pulse
CONV	MOV	A,D	Setup ACC for clock low
	SIM		Output clock low
	RIM		Read AD575 data bit into ACC
	RAL		Shift data bit into Carry
	MOV	A,L	Move temp to ACC
	RAL		Shift data bit from Carry to ACC
	MOV	L,A	Replace temp
	MOV	A,E	Setup ACC for clock high
	SIM		Output clock high
	DCR	B	Decrement inner loop counter
	JNZ	CONV	Repeat CONV until done
	DCR	C	Decrement outer loop counter
	JZ	DONE	Skip to DONE on 2nd pass
	MOV	A,L	Move temp to ACC
	ANI	03	Mask undefined bit
	MOV	H,A	Store temp in H register
	MVI	B,OB	Set inner loop counter to 8
	JMP	CONV	Repeat CONV for 8 LSBs
DONE	RET		10 bits of right-justified data now reside in HL; return

Table II. Sample Assembly Code for AD575 to 8085 Isolated Interface

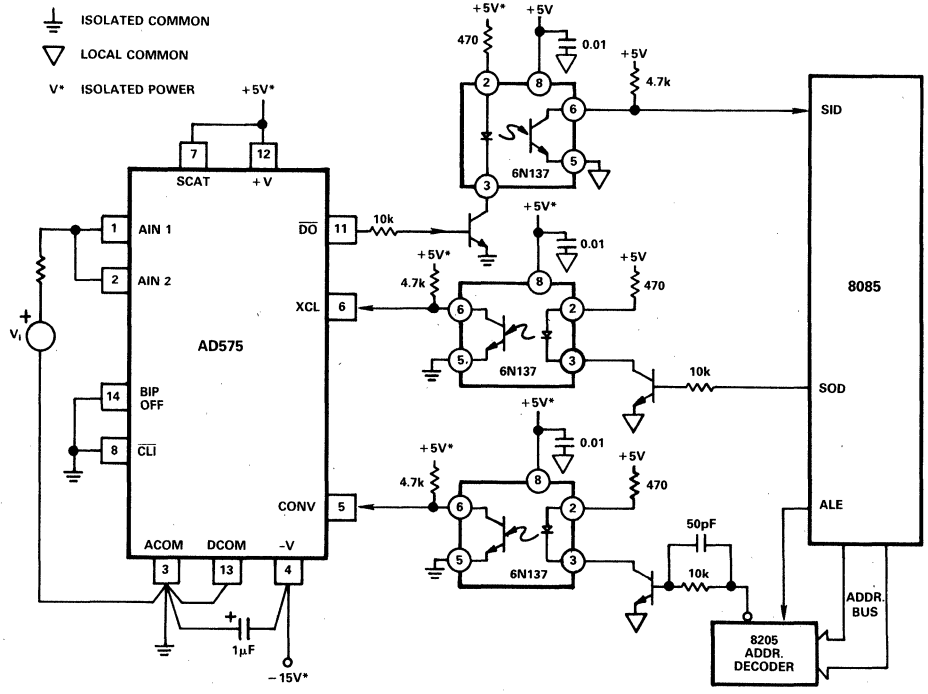


Figure 11. AD575 to 8085 Isolated Interface

ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD578

FEATURES

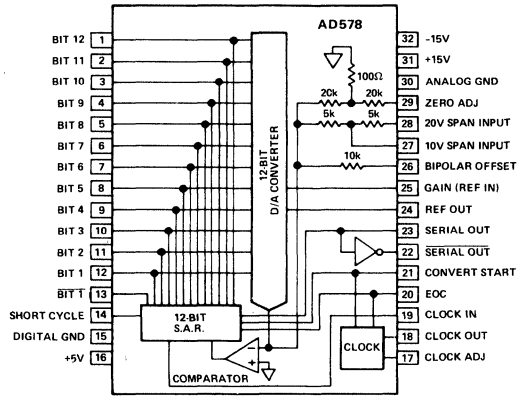
Performance

- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Fast Conversion: 3μs (max)**
- **Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max**
- **Max Nonlinearity: <±0.012%**
- **No Missing Codes Over Temperature**
- **Low Power: 875mW**
- **Hermetic Package Available**
- **Available to MIL-STD-883**

Versatility

- **Positive-True Parallel or Serial Logic Outputs**
- **Short Cycle Capability**
- **Precision +10V Reference for External Applications**
- **Adjustable Internal Clock**
- **"Z" Models for ±12V Supplies**

AD578 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 is a high speed 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD578 include a maximum linearity error at +25°C of ±0.012%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 875mW and maximum conversion time of 3μs.

The fast conversion speeds of 3μs (L grade) 4.5μs (K, T grades) and 6μs (J, S grades) make the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 333kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578 is available with either the polymer seal (N) for use in benign environmental applications or hermetic solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

The AD578S, T are available processed to MIL-STD-883 Level B, Method 5008.

PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital signal processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±1.0% and ±15ppm/°C typical T.C. The reference is available for external use and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The component count is minimized, resulting in low bond wire and chip count and high MTBF.
6. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
7. The integrated package construction provides high quality and reliability with small size and weight.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Model	AD578J	AD578K	AD578L	AD578SD[1]	AD578TD[1]
RESOLUTION	12 Bits	*	*	*	*
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±5.0V, ±10V	*	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*	*
Input Impedance					
0 to +10V, ±5V	5kΩ	*	*	*	*
±10V, 0 to +20V	10kΩ	*	*	*	*
DIGITAL INPUTS					
Convert Command[2]	1LSTTL Load	*	*	*	*
Clock Input	1LSTTL Load	*	*	*	*
TRANSFER CHARACTERISTICS					
Gain Error[3,4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Unipolar Offset[4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Bipolar Error[4,5]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Linearity Error, 25°C	±1/2LSB max	*	*	*	*
T_{min} to T_{max}	±3/4LSB	*	*	±3/4LSB max	±3/4LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)					
+25°C	12 Bits	*	*	*	*
T_{min} to T_{max}	12 Bits	*	*	*	*
POWER SUPPLY SENSITIVITY					
+15V ±10%	0.005%/%ΔV_S max	*	*	*	*
−15V ±10%	0.005%/%ΔV_S max	*	*	*	*
+5V ±10%	0.005%/%ΔV_S max	*	*	*	*
TEMPERATURE COEFFICIENTS					
Gain	±15ppm/°C typ	*	*	*	*
	±30ppm/°C max	*	*	±50ppm/°C max	±30ppm/°C max
Unipolar Offset	±3ppm/°C typ	*	*	*	*
	±10ppm/°C max	*	*	±15ppm/°C max	±10ppm/°C max
Bipolar Offset	±8ppm/°C typ	*	*	*	*
	±20ppm/°C max	*	*	±25ppm/°C max	±20ppm/°C max
Differential Linearity	±2ppm/°C typ	*	*	*	*
CONVERSION TIME[6,7,8](max)	6.0μs	4.5μs	3μs	6.0μs	4.5μs
PARALLEL OUTPUTS					
Unipolar Code	Binary	*	*	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*	*	*
Output Drive	2LSTTL Loads	*	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)					
Unipolar Code	Binary/Complementary Binary	*	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*	*
Output Drive	2LSTTL Loads	*	*	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*	*	*
Output Drive	8LSTTL Loads	*	*	*	*
INTERNAL CLOCK[8]					
Output Drive	2LSTTL Loads	*	*	*	*
INTERNAL REFERENCE					
Voltage	10.000 ±100mV	*	*	*	*
Drift	±12ppm/°C, ±20ppm/°C max	*	*	*	*
External Current	±1mA max	*	*	*	*
POWER SUPPLY REQUIREMENTS[9]					
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*
Supply Current +15V	3mA typ, 8mA max	*	*	*	*
−15V	22mA typ, 35mA max	*	*	*	*
+5V	100mA typ, 140mA max	*	*	*	*
Power Dissipation	875mW typ	*	*	*	*
TEMPERATURE RANGE					
Operating	0 to +70°C	*	*	−55°C to +125°C	−55°C to +125°C
Storage	−55°C to +150°C	*	*	−65°C to +150°C	−65°C to +150°C

NOTES

[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.

[2]Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[3]With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[4]Adjustable to zero.

[5]With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

[7]Each grade is specified at the conversion speed shown.

[8]Externally adjustable by a resistor or capacitor (see Figure 7).

[9]For "Z" models order AD578ZJ, ZK, ZL (±11.6V to ±16.5V).

*Specifications same as AD578J.

Specifications subject to change without notice.

THEORY OF OPERATION

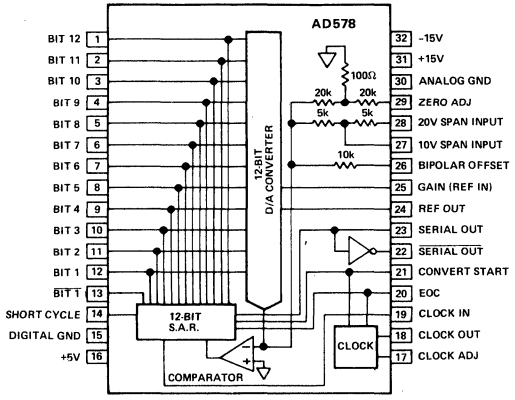


Figure 1. AD578 Functional Diagram and Pinout

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The parallel data bits become valid on the rising edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within $\pm$ 1/2LSB.

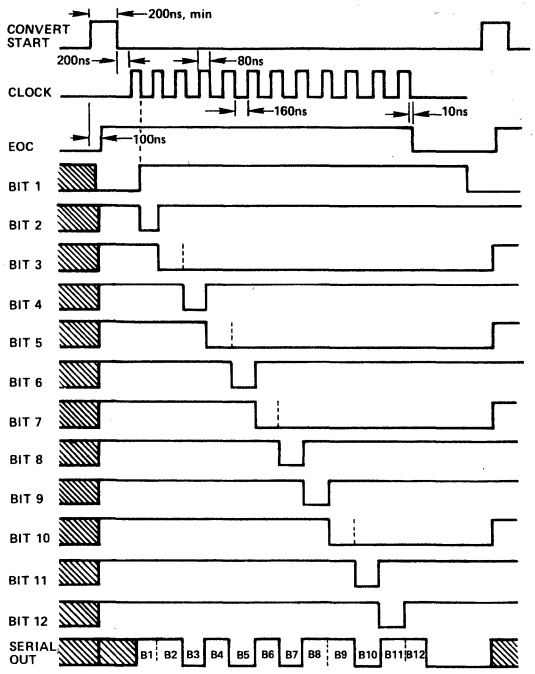
The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts $\pm$1.0%, it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately $\pm$25mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963V for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2. AD578 3μs Timing Diagram

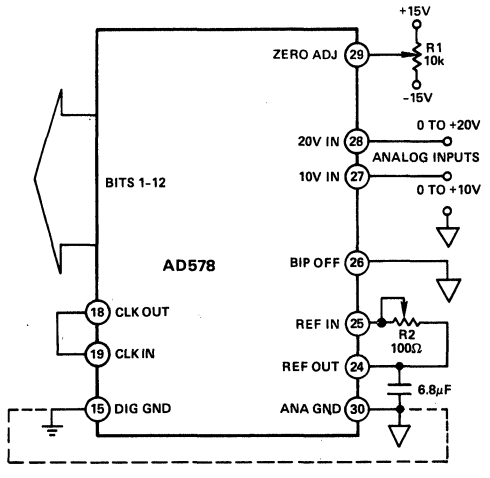


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (−4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

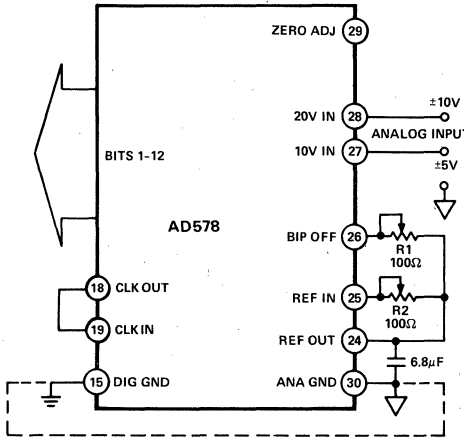


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD578's supply terminals should be capacitively decoupled as close to the AD578 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

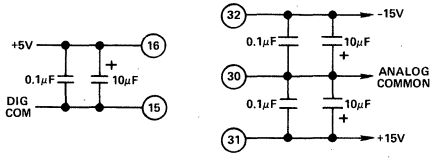


Figure 5. Basic Grounding Practice

To minimize noise the reference output (pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

The curves in Figure 6 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grade's conversion speed specification has been exceeded.

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table II.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	−5V to +5V Range	−10V to +10V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

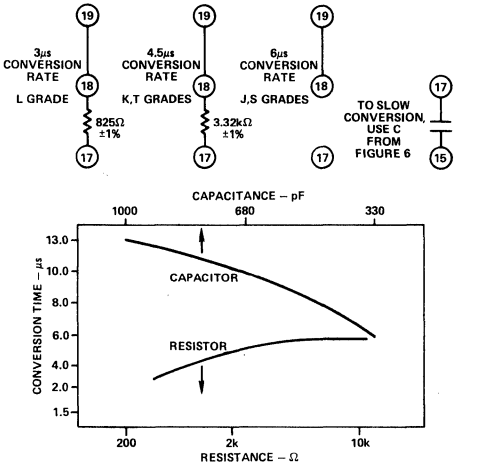


Figure 6. Conversion Times vs. R or C Values

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier – In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD711 should be used.

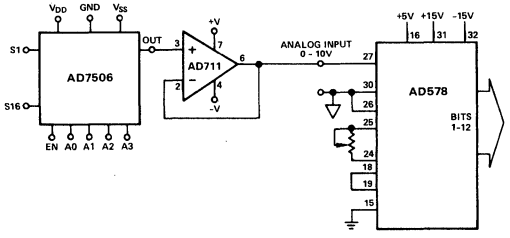


Figure 7. Input Buffer

MICROPROCESSOR INTERFACING

The 3μs conversion times of the AD578 suggests several different methods of interface to microprocessors. In systems where the AD578 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

In many multichannel data acquisition systems, the processor spends a good deal of time waiting for the ADC to complete its cycle. Converters with total conversion times of 25μs to 100μs are not slow enough to justify use of interrupts, nor fast enough to finish converting during one instruction and are usually timed out with loops, or continuously polled for status. The AD578 allows the microprocessor to time out the converter with just a few dummy instructions. For example, an 8085 system running at a 5MHz clock rate will time out an AD578 by pushing a register pair onto the stack and popping the same pair back off the stack. Such a time-out routine only occupies two bytes of program memory but requires 22 clock cyles (4.4μs). The time saved by not having to wait for the converter allows the processor to run much more efficiently particularly in multichannel systems.

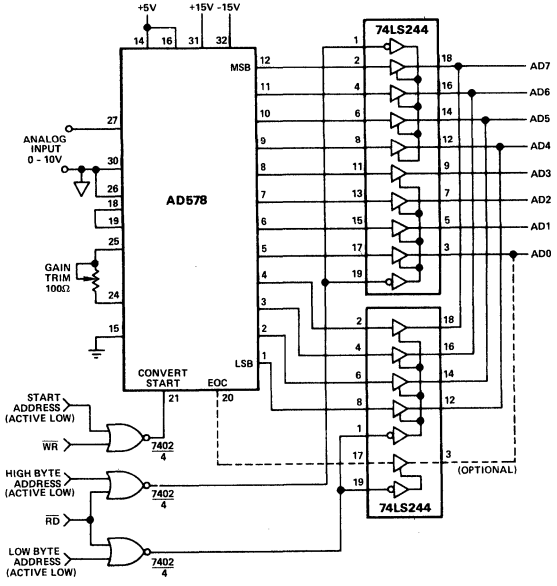


Figure 8. AD578–8085A Interface Connections

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSBs reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSBs in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

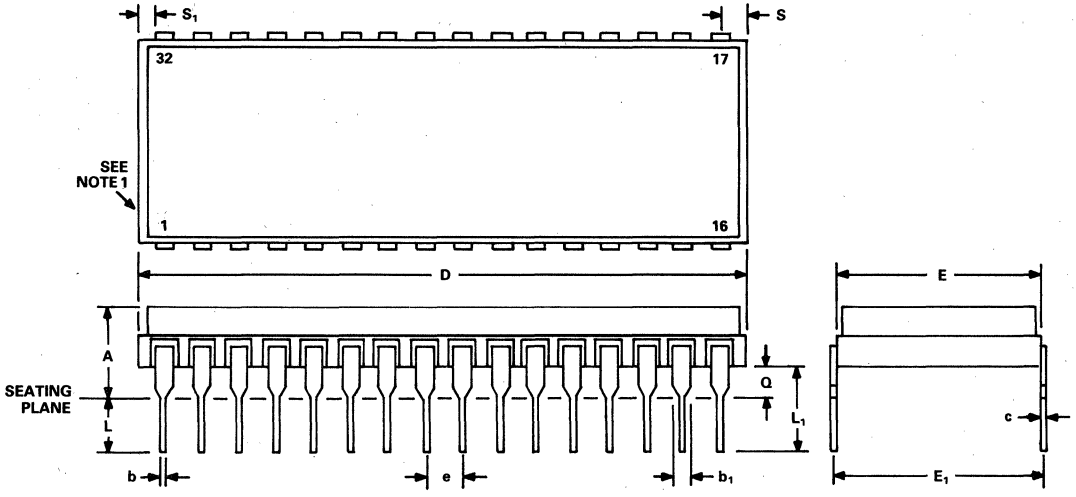
Figure 8 shows a typical connection to an 8085-type bus, using left-justified data format for unipolar inputs. Status polling is

optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD578 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields an offset binary-coded output. If two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

SAMPLED DATA SYSTEMS

The conversion speed of the AD578 allows accurate digitization of high frequency signals and high throughput rates in multi-channel data acquisition systems. The AD578LD, for example, is capable of a full accuracy conversion in 3μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 4μs. This means a sample rate of 250kHz can be realized, allowing a signal with no frequency components above 125kHz to be sampled with no loss of information. Note that the EOC signal from the AD578 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.280		7.11	
b	0.016	0.020	0.41	0.51	
b_1	0.035	0.045	0.89	1.14	2
c	0.009	0.012	0.23	0.31	
D		1.69		42.93	
E	0.545	0.585	13.84	14.86	
E_1	0.590	0.610	14.99	15.49	6
e	0.100 BSC		2.54 BSC		4,7
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015	0.060	1.02	1.52	3
S		0.098		2.49	5
S_1	0.005		0.13		5

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. The minimum limit for dimension b_1 may be 0.023" (0.58mm) for all four corner leads only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is 0.100" (2.54mm) between centerlines.
5. Applies to all four corners.
6. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads.
7. Thirty spaces.

AD578 ORDERING GUIDE*

	Conversion Speed	Temperature Range	Package
AD578JN(JD)	6.0μs	0 to +70°C	Polymer (Solder) Seal
AD578KN(KD)	4.5μs	0 to +70°C	Polymer (Solder) Seal
AD578LN(LD)	3.0μs	0 to +70°C	Polymer (Solder) Seal
AD578SD	6.0μs	−55°C to +125°C	Solder Seal
AD578TD	4.5μs	−55°C to +125°C	Solder Seal

*For ±12V operation "Z" version order: AD578ZJN, . . .

ANALOG DEVICES

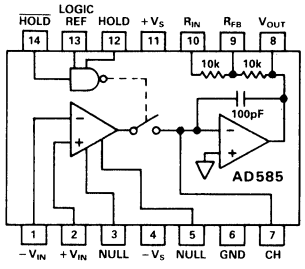
High-Speed Precision Sample-and-Hold Amplifier

AD585

FEATURES
Fast 3.0μs Acquisition Time to ±0.01% max
Low Droop Rate: 1.0mV/ms max
Sample/Hold Offset Step: 3mV max
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor
Internal Application Resistors

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements

AD585 FUNCTIONAL BLOCK DIAGRAM



3

PRODUCT DESCRIPTION

The AD585 is a complete monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and matched applications resistors have been provided for high precision and applications flexibility.

The performance of the AD585 makes it ideal for high speed 10- and 12-bit data acquisition systems, where fast acquisition time, low sample-to-hold offset, and low droop are critical. The AD585 can acquire a signal to ±0.01% in 3μs maximum, and then hold that signal with a maximum sample-to-hold offset of 3mV and less than 1mV/ms droop, using the on-chip hold capacitor. If lower droop is required, it is possible to add a larger external hold capacitor.

The high-speed analog switch used in the AD585 exhibits aperture jitter of 0.5ns, enabling the device to sample full-scale (20V peak-to-peak) signals at frequencies up to 78kHz with 12-bit precision.

The AD585 can be used with any user-defined feedback network to provide any desired gain in the sample mode. On-chip precision thin-film resistors can be used to provide gains of +1, −1, or +2. Output impedance in the hold mode is sufficiently low to maintain an accurate output signal even when driving the dynamic load presented by a successive-approximation A/D converter. However, the output is protected against damage from accidental short circuits.

The control signal for the HOLD command can be either active high or active low. The differential HOLD signal is compatible with all logic families, if a suitable reference level is provided. An on-chip TTL reference level is provided for TTL compatibility.

The device is available in two versions: the "A" specified for the −25°C to +85°C industrial temperature range, and the "S" specified over the extended temperature range −55°C to +125°C. The "A" and "S" versions are available in a 14-pin cerdip package.

PRODUCT HIGHLIGHTS

1. The fast acquisition time (3μs) and low aperture jitter (0.5ns) make it the first choice for very high speed data acquisition systems.
2. The droop rate is only 1.0mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
3. The low charge transfer of the analog switch keeps sample-to-hold offset below 3mV with the on-chip 100pF hold capacitor, eliminating the trade-off between acquisition time and S/H offset required with other SHAs.
4. The AD585 has internal pretrimmed application resistors for applications versatility.
5. The AD585 is complete with an internal hold capacitor for ease of use. Capacitance can be added externally to reduce the droop rate when long hold times and high accuracy are required.
6. The AD585 is recommended for use with 10- and 12-bit successive-approximation A/D converters such as AD571, AD572, AD573, AD574A, AD575, AD578, AD579, AD ADC80, AD ADC85.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V, and C_H = Internal, A = +1, $\overline{HOLD}$ active unless otherwise specified)

Model	AD585AQ Min	AD585AQ Typ	AD585AQ Max	AD585SQ Min	AD585SQ Typ	AD585SQ Max	Units
SAMPLE/HOLD CHARACTERISTICS							
Acquisition Time, 10V Step to 0.01%			3			3	µs
20V Step to 0.01%			5			5	µs
Aperture Time, 20V p-p Input $\overline{HOLD}$ 0V		35			35		ns
Aperture Jitter, 20V p-p Input, $\overline{HOLD}$ 0V		0.5			0.5		ns
Settling Time, 20V p-p Input, $\overline{HOLD}$ 0V, to 0.01%		0.5			0.5		µs
Droop Rate			1			1	mV/ms
Droop Rate T_{min} to T_{max}	Doubles Every 10°C			Doubles Every 10°C			
Charge Transfer			0.3			0.3	pC
Sample-to-Hold Offset	−3		3	−3		3	mV
Feedthrough 20V p-p, 10kHz Input		0.5			0.5		mV
TRANSFER CHARACTERISTICS							
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k		200,000			200,000		V/V
Application Resistor Mismatch			0.3			0.3	%
Common Mode Rejection V_{CM} = ±10V	80			80			dB
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p		2.0			2.0		MHz
Full Power Bandwidth V_{OUT} = 20V p-p		160			160		kHz
Slew Rate V_{OUT} = 20V p-p		10			10		V/µs
Output Resistance (Sample Mode) I_{OUT} = ±10mA			0.05			0.05	Ω
Output Short Circuit Current		50			50		mA
Output Short Circuit Duration		Indefinite			Indefinite		
ANALOG INPUT CHARACTERISTICS							
Offset Voltage			2			2	mV
Offset Voltage, T_{min} to T_{max}			3			3	mV
Bias Current			2			2	nA
Bias Current T_{min} to T_{max}			5		20	50[1]	nA
Input Capacitance, f = 1MHz		10			10		pF
Input Resistance, Sample or Hold 20V p-p Input, A = +1		10^{12}			10^{12}		Ω
DIGITAL INPUT CHARACTERISTICS							
TTL Reference Output	1.2	1.4	1.6	1.2	1.4	1.6	V
Hold Input Voltage With Respect to Logic Reference							
Hold Mode, T_{min} to T_{max}			−0.4			−0.4	V
Sample Mode, T_{min} to T_{max}			0.4			0.4	V
Logic Input Current (Either Input)			50			50	µA
POWER SUPPLY CHARACTERISTICS							
Operating Voltage Range	+5, −12		±18	+5, −12		±18	V
Supply Current, R_L = ∞	6		10	6		10	mA
Power Supply Rejection, Sample Mode	70			70			dB
TEMPERATURE RANGE							
Specified Performance	−25		+85	−55		+125	°C

NOTES

[1]Not tested at −55°C.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

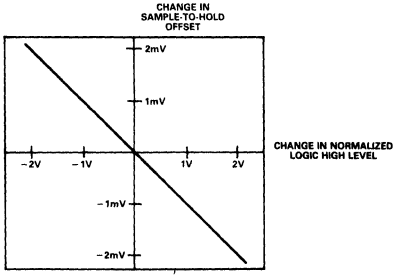


Figure 1. Sample-to-Hold Offset vs. Logic Level (HOLD Active)

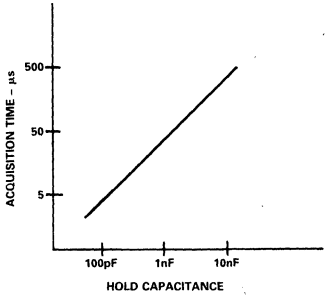


Figure 2. Acquisition Time vs. Hold Capacitance (10V Step to 0.01%)

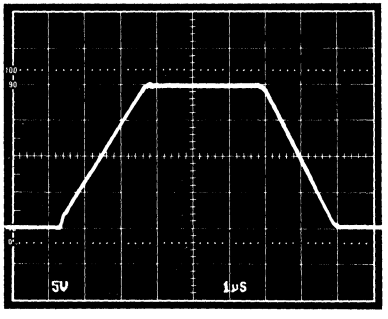


Figure 3. Large Signal Response, Sample Mode

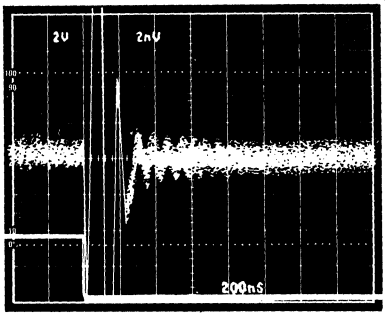


Figure 4. Sample-to-Hold Settling Time (HOLD Active)

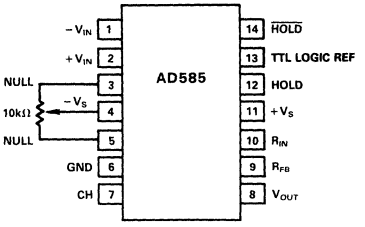


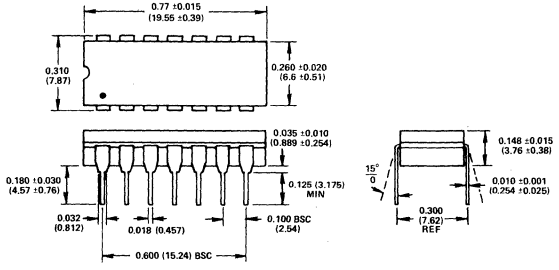
Figure 5. Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Supplies (+Vs, −Vs)	±18V
Logic Inputs	$\pm V_S$
Analog Inputs	$\pm V_S$
R_{IN}, R_{FB} Pins	$\pm V_S$
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering)	300°C
Output Short Circuit to Ground	Indefinite
TTL Logic Reference Short Circuit to Ground	Indefinite

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



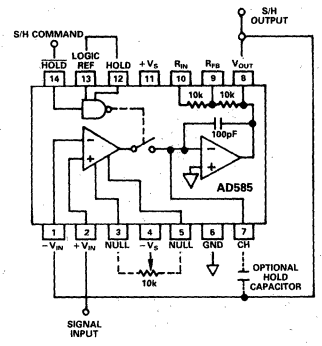


Figure 6. Connection Diagram, Gain = +1, $\overline{HOLD}$ Active

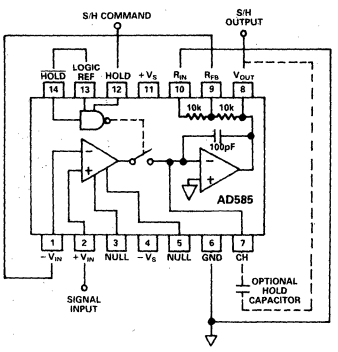


Figure 7. Connection Diagram, Gain = +2, HOLD Active

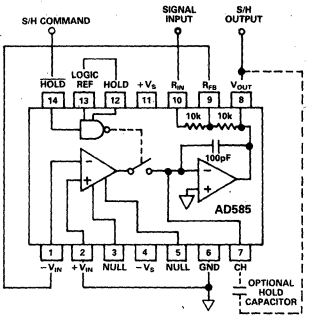


Figure 8. Connection Diagram Gain = −1, $\overline{HOLD}$ Active

SAMPLED DATA SYSTEMS

In sampled data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 9 shows pictorially the sample-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Sample-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Sample Transition.

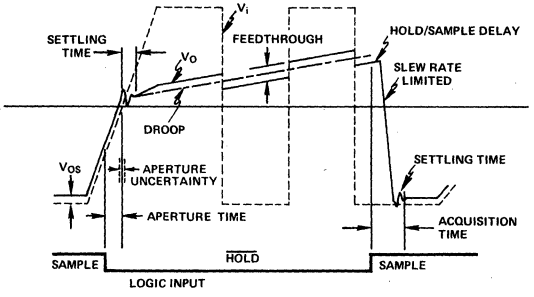


Figure 9. Pictorial Showing Various S/H Characterstics

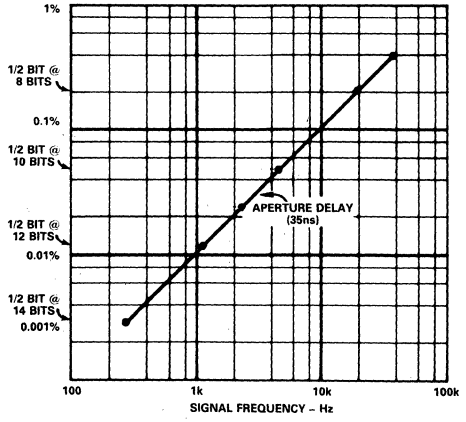


Figure 10. Aperture Delay Error vs. Frequency

SAMPLE-TO-HOLD TRANSITION

The aperture delay time is the time required for the sample-and-hold amplifier to switch from sample to hold. Since this is effectively a constant then it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 10 will result.

To eliminate the aperture delay as an error source the sample-to-hold command may be advanced with respect to the input signal.

Once the aperture delay time has been eliminated as an error source then the aperture jitter which is the variation in aperture delay time from sample-to-sample remains. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the N-bit A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi\ (\text{Aperture Jitter})}$$

For an application with a 10-bit A/D converter with a 10V full scale to a 1/2LSB error maximum.

$$F_{max} = \frac{2^{-(10+1)}}{\pi\ (0.5 \times 10^{-9})}$$

F_{max} = 310.8kHz.

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\ (0.5 \times 10^{-9})}$$

F_{max} = 77.7kHz.

Figure 11 shows the entire range of errors induced by aperture jitter with respect to the input signal frequency.

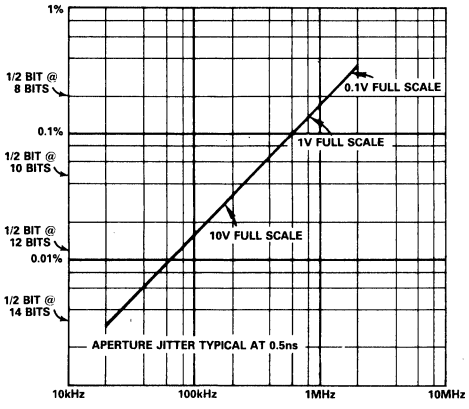


Figure 11. Aperture Jitter Error vs. Frequency

Sample-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting sample-to-hold offset is a function of the logic level.

The logic inputs were designed for application flexibility and, therefore, a wide range of logic thresholds. This was achieved by using a differential input stage for HOLD and $\overline{\text{HOLD}}$. Figure 1 shows the change in the sample-to-hold offset voltage based upon an independently programmed reference voltage. Since the input stage is a differential configuration, the offset voltage is a function of the control voltage range around the programmed threshold voltage.

The sample-to-hold offset can be reduced by adding capacitance to the internal 100pF capacitor and by using $\overline{\text{HOLD}}$ instead of HOLD. This may be easily accomplished by adding an external capacitor between Pins 7 and 8. The sample-to-hold offset is then governed by the relationship:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H \text{ Total (pF)}}$$

For the AD585 in particular it becomes:

$$\text{S/H Offset (V)} = \frac{0.3 \text{ pC}}{100\text{pF} + (C_{EXT})}$$

The addition of an external hold capacitor also affects the acquisition time of the AD585. The change in acquisition time with respect to the C_{EXT} is shown graphically in Figure 2.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a sample and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current.

The rate of voltage change on the capacitor dV/dT is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dT} \text{ (Volts/Sec)} = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD585 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF} + (C_{EXT})}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion. The hold-mode droop rate can be traded-off with acquisition time to provide the best combination of droop error and acquisition time. The tradeoff is easily accomplished by varying the value of C_{EXT}.

Since a sample and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (T_{CONV}) is required to calculate the maximum allowable dV/dT.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{T_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dT}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) $= \Delta T$.

$$\frac{dV\ 25°C}{dT} \times 2^{\frac{(\Delta T°C)}{10°C}} \leq \frac{dV \text{ max}}{dT}$$

HOLD-TO-SAMPLE TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD585 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD585 can be used with a number of different A/D converters to achieve high throughput rates. Figures 12 and 13 show the use of an AD585 with the AD578 and AD574A.

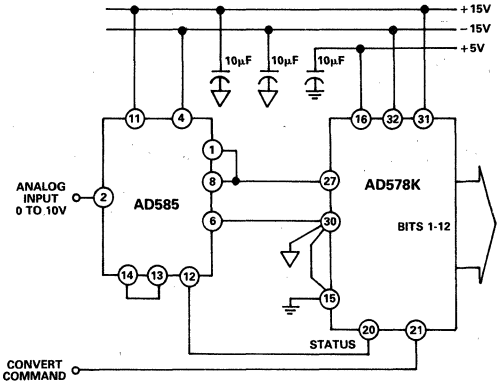


Figure 12. A/D Conversion System, 117.6kHz Throughput 58.8kHz max Signal Input

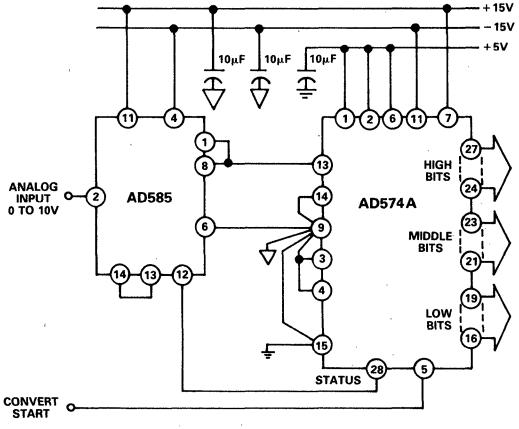


Figure 13. 12 Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz max Signal Input

LOGIC INPUT

The sample-and-hold logic control was designed for versatile logic interfacing. The HOLD and $\overline{\text{HOLD}}$ inputs may be used with both low and high level CMOS, TTL and ECL logic systems. Logic threshold programmability was achieved by using a differential amplifier as the input stage for the digital inputs. A predictable logic threshold may be programmed by referencing either HOLD or $\overline{\text{HOLD}}$ to the appropriate threshold voltage. For example, if the internal 1.4V reference is applied to $\overline{\text{HOLD}}$ an input signal to HOLD between $+1.8$V and $+V_S$ will place the AD585 in the hold mode. The AD585 will go into the sample mode for this case when the input is between $-V_S$ and $+1.0$V. The range of references which may be applied is from $(-V_S + 4V)$ to $(+V_S - 3V)$.

OPTIONAL CAPACITOR SELECTION

If an additional capacitor is going to be used in conjunction with the internal 100pF capacitor it must have a low dielectric absorption. Dielectric absorption is just that; it is the charge absorbed into the dielectric that is not immediately added to or removed from the capacitor when rapidly charged or discharged. The capacitor with dielectric absorption is modeled in Figure 14.

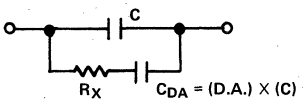


Figure 14. Capacitor Model with Dielectric Absorption

If the capacitor is charged slowly, C_{DA} will eventually charge to the same value as C. But unfortunately, good dielectrics have very high resistances, so while C_{DA} may be small, R_X is large and the time constant $R_X C_{DA}$ typically runs into the millisecond range. In fast-charge, fast-discharge situations the effect of dielectric absorption resembles "memory". In a data acquisition system where many channels with widely varying data are being sampled the effect is to have an ever changing offset which appears as a very nonlinear sample-to-hold offset since the difference between the voltage being measured and the voltage previously measured determines the fraction by which the dielectric absorption figure is multiplied. It is impossible to readily correct for this error source. The only solution is to use a capacitor with dielectric absorption less than the maximum tolerable error. Capacitor types such as polystyrene, polypropylene or Teflon are recommended.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD585. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

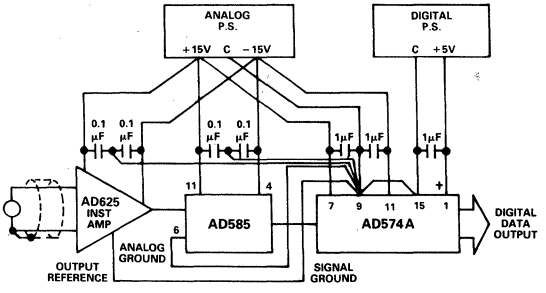


Figure 15. Basic Grounding Practice

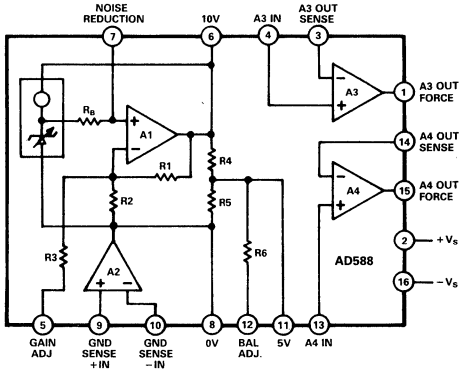
ANALOG DEVICES

Ultra High Precision Voltage Reference

AD588

FEATURES
Ultra Low Drift – 1ppm/°C
Ultra Low Initial Error – 1mV
Pin-Programmable Output
+10V, +5V, ±5V Tracking, −5V, −10V
Flexible Output Force and Sense Terminals
High Impedance Ground Sense
Machine-Insertable DIP Packaging
Guaranteed Long-Term Stability – 25ppm/1000 hours

AD588 FUNCTIONAL BLOCK DIAGRAM



3

PRELIMINARY TECHNICAL DATA

PRODUCT DESCRIPTION

The AD588 represents a major advance in the state-of-the-art in monolithic voltage references. It offers a combination of low initial error and low temperature drift previously found only in hybrid units at much higher cost. The AD588 uses a proprietary ion-implanted buried zener diode, and laser-wafer-drift-trimming of high stability thin-film resistors to provide outstanding performance at low cost.

The AD588 includes the basic reference cell and three additional amplifiers which provide pin-programmable output ranges. The amplifiers are laser-trimmed for low offset and low drift and maintain the accuracy of the reference. The amplifiers are configured to allow Kelvin connections to the load and/or boosters for driving long lines or high-current loads while maintaining full accuracy.

The low initial error allows the AD588 to be used as a system reference in applications requiring 12-bit absolute accuracy. In such systems, the AD588 can provide a known voltage for system calibration in software and the low drift allows compensation for the drift of other components in a system. Manual system calibration and the cost of periodic recalibration can therefore be eliminated. Furthermore, the mechanical instability of a trimming potentiometer and the potential for improper calibration can be eliminated by using the AD588 and autocalibration software.

The AD588 is available in seven versions. The AD588JN, KN, and LN are specified for the 0 to +70°C temperature range and are packaged in a 16-pin plastic DIP. The AD588AD, BD, and CD grades are packaged in a 16-pin side-brazed ceramic DIP and are specified for the −25°C to +85°C industrial temperature range. The ceramic AD588SD and TD grades are specified for the full military/aerospace temperature range.

PRODUCT HIGHLIGHTS

1. The AD588 offers 12-bit absolute accuracy without any user adjustments. Optional fine-trim connections are provided for applications requiring higher precision. The fine-trimming does not alter the operating conditions of the zener or the buffer amplifiers and thus does not increase the temperature drift.
2. Long-term stability is excellent and the LN, CD, and TD versions are 100% tested and guaranteed for 25 parts-per-million stability in a 1000-hour period.
3. Output noise of the AD588 is very low – typically 10μV p-p. A pin is provided for additional noise filtering using an external capacitor.
4. A precision ±5V tracking mode with Kelvin output connections is available with no external components. Tracking error is less than one millivolt and a fine-trim is available for applications requiring exact symmetry between the +5V and −5V outputs.
5. Pin strapping capability allows configuration of a wide variety of outputs: ±5V, +5V & +10V, −5V & −10V dual outputs or +5V, −5V, +10V, −10V single outputs.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V unless otherwide noted)

	AD588JN/AD/SD/TD			AD588KN/LN/BD/CD			
	Min	Typ	Max	Min	Typ	Max	Units
OUTPUT VOLTAGE ERROR							
+10V, −10V Outputs	−3		3	−1		+1	mV
+5V, −5V Outputs	−1.5		1.5	−0.5		+0.5	mV
OUTPUT VOLTAGE DRIFT							
25 to T_{min} or T_{max}	−3		3	−1		+1	ppm/°C
25 to T_{min} or T_{max} (T Grade)	−5		5				ppm/°C
LINE REGULATION							
+10V Output,							
$+11.4V < +V_S < +18V$	−100		100	−100		100	μV/V
−10V Output,							
$-18V < -V_S < -11.4V$	−100		100	−100		100	μV/V
LOAD REGULATION							
+10V, −10V Outputs,							
$0 < I_{OUT} < 10mA$	−100		100	−100		100	μV/mA
QUIESCENT CURRENT		7	10		7	10	mA
OUTPUT NOISE (Any Output)							
0.1 to 10Hz		10			10		μV p-p
Spectral Density, 100Hz		100			100		nV/√Hz
LONG-TERM STABILITY (@ +25°C)							
J, K, A, B, S Grades		25			25		ppm/1000hr
L, C, T Grades			25			25	ppm/1000hr
±5V TRACKING MODE							
Symmetry Error	−1.5		1.5	−0.5		+0.5	mV
BUFFER AMPLIFIERS							
Offset Voltage		100			100		μV
Bias Current		20			20		nA
Open Loop Gain		110			110		dB
Output Current A3, A4	−10		+10	−10		+10	mA
SHORT-CIRCUIT CURRENT		20			20		mA
TEMPERATURE RANGE							
Specified Performance							
J, K, L Grades	0		+70	0		+70	°C
A, B, C Grades	−25		+85	−25		+85	°C
S, T Grades	−55		+125				°C

NOTE
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

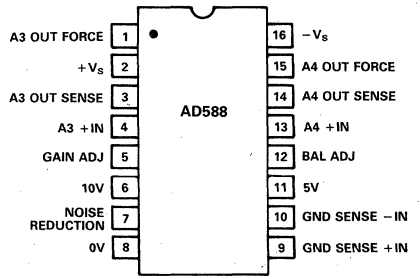
ABSOLUTE MAXIMUM RATINGS

$+V_S$ to $-V_S$ 36V
Power Dissipation (+25°C)
D Package 600mW
N Package 600mW
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10sec) . . . . . 300°C
Package Thermal Resistance
D (θ_{jn}/θ_{jc}) . . . . . 90/25°C/W
N (θ_{jn}/θ_{jc}) . . . . . 137/53°C/W
Output Protection: All outputs safe if shorted to ground

ORDERING GUIDE

Part Number	Initial Error	Temperature Coefficient	Temperature Range °C	Package
AD588JN	3mV	3ppm/°C	0 to +70	Plastic
AD588KN	1mV	1ppm/°C	0 to +70	Plastic
AD588LN	1mV	1ppm/°C	0 to +70	Plastic
AD588AD	3mV	3ppm/°C	−25 to +85	Ceramic
AD588BD	1mV	1ppm/°C	−25 to +85	Ceramic
AD588CD	1mV	1ppm/°C	−25 to +85	Ceramic
AD588SD	3mV	3ppm/°C	−55 to +125	Ceramic
AD588TD	3mV	5ppm/°C	−55 to +125	Ceramic

AD588 PIN CONFIGURATION



Theory of Operation

The AD588 consists of a buried zener diode reference, amplifiers used to provide pin programmable output ranges, and associated thin film resistors as shown in the block diagram of Figure 1. The temperature compensation circuitry provides the device with a temperature coefficient of 1ppm/°C or less.

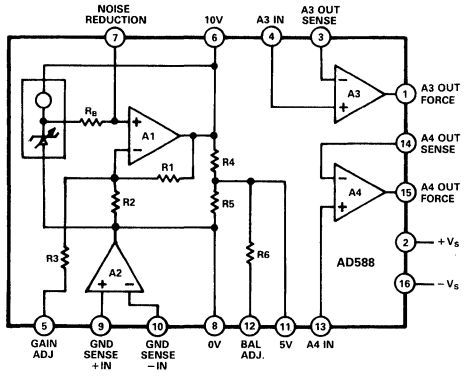


Figure 1. AD588 Functional Block Diagram

Amplifier A1 performs several functions. A1 primarily acts to amplify the zener voltage from 6.5V to the required 10V output. In addition, A1 also provides for external adjustment of the 10V output through pin 5, the GAIN ADJUST. Using the bias compensation resistor between the zener output and the non-inverting input to A1, a capacitor can be added at the NOISE REDUCTION pin (pin 7) to form a low pass filter and reduce the noise contribution of the zener to the circuit. Two matched thin film resistors (R4 & R5) divide the 10V output in half. The 5V pin (pin 11) provides access to this voltage and pin 12 (BALANCE ADJUST) can be used for fine adjustment of this division.

Ground sensing for the circuit is provided by amplifier A2. The non-inverting input (pin 9) senses the system ground which will be transferred to the point on the circuit where the inverting input (pin 10) is connected. This may be pin 6, 8 or 11. The output of A2 drives pin 8 to the appropriate voltage. Thus, if pin 10 is connected to pin 8, the 0V pin will be the same voltage as the system ground. Alternatively, if pin 10 is connected to the 5V pin, it will be ground and pin 6 and pin 8 will be +5V and −5V respectively.

Amplifiers A3 and A4 are internally compensated and are used to buffer the voltages at pins 6, 8, and 11 as well as to provide a full Kelvin output. Thus, the AD588 has a full Kelvin capability by providing the means to sense a system ground and provide forced and sensed outputs referenced to that ground.

Applying the AD588

The AD588 may be configured in a number of different ways to provide dual reference outputs (+5V and +10V, +5V and −5V, or −5V and −10V) or any of the following single reference outputs: +5V, +10V, −5V or −10V. The various options are set up by using the inverting input (pin 10) of A2. Table I details the appropriate pin connections for each output range.

Single Outputs

Pin 9 should be connected to the system ground and power is applied to pins 2 and 16. Figure 2 and Table I show the connections for each of the options. The unused output amplifiers A3 and/or A4 should have the output force and sense pins connected and their input tied to pin 6 or pin 8.

Dual Outputs

With power applied to pins 2 and 16 and pin 9 connected to the system ground, the AD588 will produce the appropriate output ranges when connected as shown in Table 1 and Figure 2. Depending upon the voltages required, the unbuffered outputs are available at pins 6, 8 and 11. Either signal may be buffered by amplifiers A3 and A4. At this point, the GAIN ADJUST and BALANCE ADJUST pins may be used as described in the CALIBRATION section. If desired, two outputs of the same voltage may be obtained by connecting both output buffers to the appropriate output pins. This is shown in Table I.

RANGE	CONNECT PIN 10 TO PIN:	UNBUFFERED OUTPUT ON PINS −10V	−5V	0V	+5V	+10V	BUFFERED OUTPUT CONNECTIONS	BUFFERED OUTPUT ON PINS −10V	−5V	0V	+5V	+10V
SINGLE OUTPUTS												
+5V or +10V	8	–	–	8	11	6	11-13 & 14-15	–	–	–	15	–
							or					
							6-4 & 3-1	–	–	–	–	1
−5V or +5V	11	–	8	11	6	–	8-13 & 14-15	–	15	–	–	–
							or					
							6-4 & 3-1	–	–	–	1	–
−5V or −10V	6	8	11	6	–	–	11-13 & 14-15	–	15	–	–	–
							or					
							8-4 & 3-1	1	–	–	–	–
DUAL OUTPUTS												
+5V		–	–	–	11	–	11-13 & 14-15	–	–	–	15	–
	8											
+10V		–	–	–	–	6	6-4 & 3-1	–	–	–	–	1
+5V		–	–	–	6	–	6-4 & 3-1	–	–	–	1	–
	11											
−5V		–	8	–	–	–	8-13 & 14-15	–	15	–	–	–
−5V		–	11	–	–	–	11-4 & 3-1	–	1	–	–	–
	6											
−10V		8	–	–	–	–	8-13 & 14-15	15	–	–	–	–
+5V		–	–	–	11	–	11-13 & 14-15	–	–	–	15	–
	8											
+5V		–	–	–	11	–	11-4 & 3-1	–	–	–	1	–
+10V		–	–	–	–	6	6-13 & 14-15	–	–	–	–	15
	8											
+10V		–	–	–	–	6	6-4 & 3-1	–	–	–	–	1
−5V		–	11	–	–	–	11-4 & 3-1	–	1	–	–	–
	6											
−5V		–	11	–	–	–	11-13 & 14-15	–	15	–	–	–
−10V		8	–	–	–	–	8-4 & 3-1	1	–	–	–	–
	6											
−10V		8	–	–	–	–	8-13 & 14-15	15	–	–	–	–

Table I. AD588 Connections

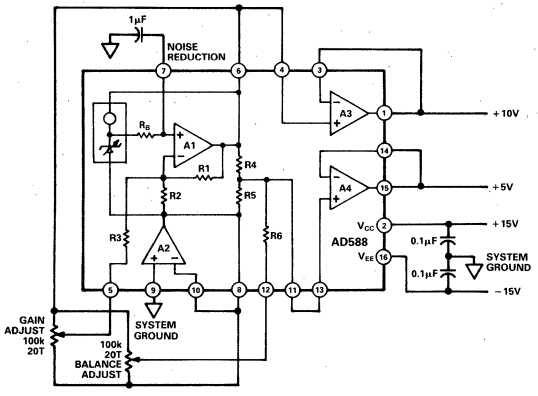


Figure 2a. +10V and +5V Outputs

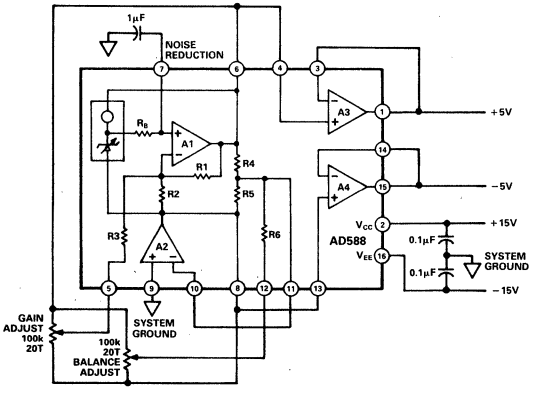


Figure 2b. +5V and −5V Outputs

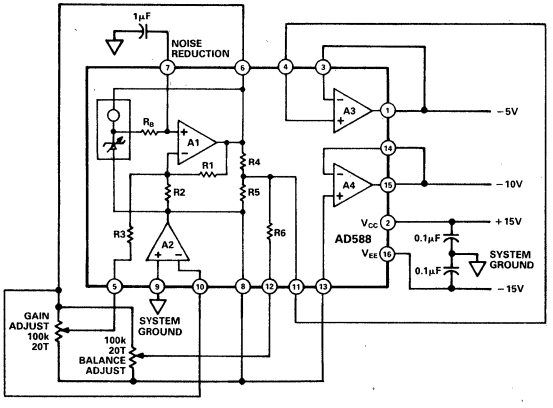


Figure 2c. −5V and −10V Outputs

CALIBRATION

Generally, the AD588 will meet the requirements of a precision system without additional adjustment. Initial output voltage error of 1mV and output noise specs of 10μV p-p allow for accuracies of 12-16 bits. However, in applications where an even greater level of accuracy is required, additional calibration may be called for. Provision for trimming has been made through the use of the GAIN ADJUST and BALANCE ADJUST pins (pins 5 and 12 respectively).

Gain adjustment can be accomplished by using a 100k, 20 turn potentiometer connected between pins 6 and 8. The wiper should be connected to GAIN ADJUST pin 5 as shown in Figures 2a, b, c. The typical adjustment range of this setup is −3.5mV to +7.5mV with a resolution of approximately 550μV/turn.

Trimming the AD588 introduces no additional errors over temperature so a precision potentiometer is not required.

For the ±5V range, an additional adjustment, the BALANCE trim, may be required. Adjustments of these outputs independently control the gain (pin 6 – pin 8) and the symmetry or balance of the output. Gain adjustment is identical to the one described above. The balance adjustment also uses a 100K, 20 turn potentiometer connected between pins 6 and 8. The tap is connected to pin 12, BALANCE ADJUST, and provides a range of ±4.5mV with a resolution of 450μV/turn.

For single output voltage ranges, or in cases when BALANCE ADJUST is not required, pin 12 should be connected to pin 11. If GAIN ADJUST is not required, pin 5 should be left floating.

NOISE REDUCTION

The noise generated by the AD588 is typically less than 10μV p-p over the 0.1 to 10Hz band. Noise in a 1MHz bandwidth is approximately 800μV p-p. The dominant source of this noise is the buried zener which contributes approximately 100nV/$\sqrt{\text{Hz}}$. In comparison, the op amp's contribution is negligible.

If further noise reduction is desired, an optional capacitor may be added to the NOISE REDUCTION pin. This will form a low pass filter on the output of the zener cell. A 1μF capacitor will have a 3dB point at 40Hz and will reduce the high frequency 1MHz noise to about 200μV p-p. Figures 2a, b, and c show a noise reduction capacitor connected. The NOISE REDUCTION function must not be used when configuring the device when pin 10 is connected to pin 6 (−10V output).

ANALOG DEVICES

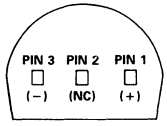
Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES
High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

AD592 CONNECTING DIAGRAM

(BOTTOM VIEW)



*PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED

3

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

The AD592 can be employed in applications between −25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

Typical application areas include; appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

*Covered by Patent No. 4,123,698.

The AD592 is available in three performance grades; the AD592AN, AD592BNand AD592CN. All devices are packaged in a plastic TO-92 case rated from −45°C to +125°C. Performance is specified from −25°C to +105°C. AD592 chips are also available, contact the factory for details.

PRODUCT HIGHLIGHTS

1. With a single supply (4V to 30V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (−25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.

SPECIFICATIONS (typical @ 25°C, V_S = 5V, unless otherwise noted)

Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @25°C[1]		1.5	**2.5**		0.7	**1.0**		0.3	**0.5**	°C
T_A = 0 to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = −25 to +105°C										
Error over Temperature[3]		2.0	**3.5**		0.9	**2.0**		0.5	**1.0**	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	−25		+105	−25		+105	−25		+105	°C
Package Temperature[6]	−45		+125	−45		+125	−45		+125	°C
Forward Voltage (+ to −)			**44**			**44**			**44**	V
Reverse Voltage (− to +)			**20**			**20**			**20**	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4V<V_S<+5V			**0.5**			**0.5**			**0.5**	°C/V
+5V<V_S<+15V			**0.2**			**0.2**			**0.2**	°C/V
+15V<V_S<+30V			**0.1**			**0.1**			**0.1**	°C/V

NOTES

[1]An external calibration trim can be used to zero the error @25°C.

[2]Defined as the maximum deviation from a mathematically best fit line.

[3]Parameter tested on all production units at +105°C only. C grade at −25°C also.

[4]Maximum deviation between +25°C readings after a temperature cycle between −45°C and +125°C. Errors of this type are noncummulative.

[5]Operation @125°C, error over time is noncummulative.

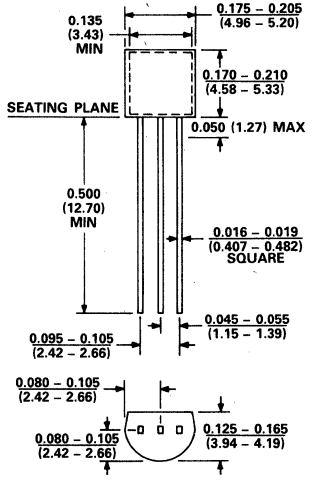
[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

Specifications subject to change without notice.

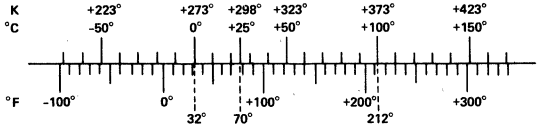
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

PHYSICAL DIMENSIONS

Dimensions shown in inches and (mm).



TO-92 (N)

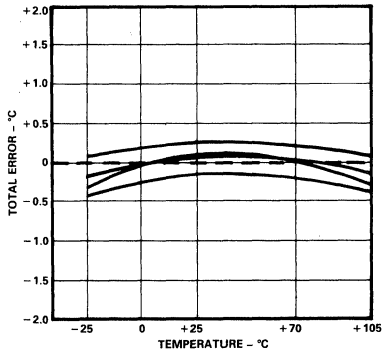


TEMPERATURE SCALE CONVERSION EQUATIONS

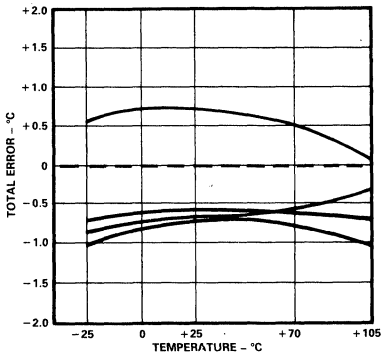
$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

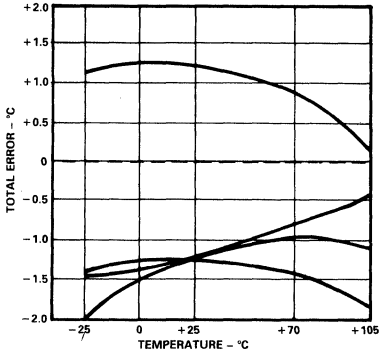
Typical @ V_S = +5V



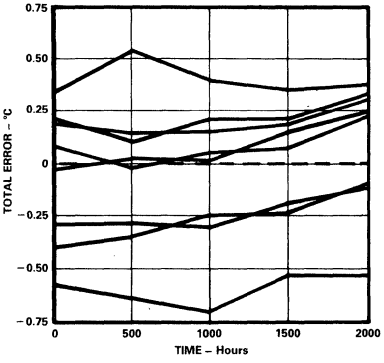
AD592CN Accuracy Over Temperature



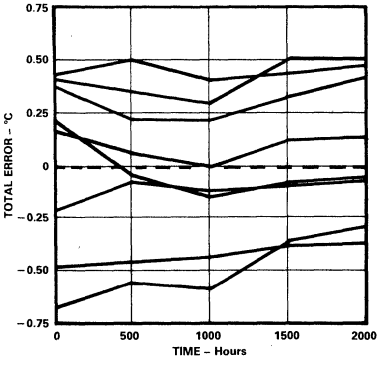
AD592BN Accuracy Over Temperature



AD592AN Accuracy Over Temperature



Long-Term Stability @ 85°C and 85% Relative Humidity



Long-Term Stability @ 125°C

AD592 ORDERING GUIDE

Model	Package	Max Cal Error @ 25°C	Max Error −25°C to +105°C	Max Nonlinearity −25°C to +105°C
AD592CN	TO-92	0.5°C	1.0°C	0.35°C
AD592BN	TO-92	1.0°C	2.0°C	0.4°C
AD592AN	TO-92	2.5°C	3.5°C	0.5°C

THEORY OF OPERATION

The AD592 uses a fundamental property of silicon transistors to realize its temperature proportional output. If two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron are constant, the resulting voltage is directly Proportional To Absolute Temperature (PTAT). In the AD592 this difference voltage is converted to a PTAT current by low temperature coefficient thin film resistors. This PTAT current is then used to force the total output current to be proportional to degrees Kelvin. The result is a current source with an output equal to a scale factor times the temperature (K) of the sensor. A typical V-I plot of the circuit at +25°C and the temperature extremes is shown in Figure 1.

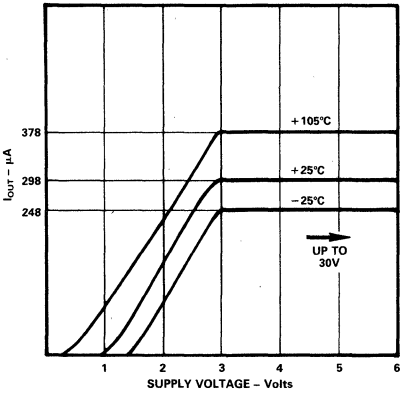


Figure 1. V–I Characteristics

Factory trimming of the scale factor to 1µA/K is accomplished at the wafer level by adjusting the AD592's temperature reading so it corresponds to the actual temperature. During laser trimming the IC is at a temperature within a few degrees of 25°C and is powered by a 5V supply. The device is then packaged and automatically temperature tested to specification.

FACTORS AFFECTING AD592 SYSTEM PRECISION

The accuracy limits given on the Specifications page for the AD592 makes it easy to apply in a variety of diverse applications. To calculate a total error budget in a given system it is important to correctly interpret the accuracy specifications, nonlinearity errors, the response of the circuit to supply voltage variations and the effect of the surrounding thermal environment. As with other electronic designs external component selection will have a major effect on accuracy.

CALIBRATION ERROR, ABSOLUTE ACCURACY AND NONLINEARITY SPECIFICATIONS

Three primary limits of error are given for the AD592 such that the correct grade for any given application can easily be chosen for the overall level of accuracy required. They are the calibration accuracy at 25°C, and the error over temperature from 0 to 70°C and −25°C to +105°C. These specifications correspond to the actual error the user would see if the current output of a AD592 were converted to a voltage with a precision resistor. Note that the maximum error at room temperature, over the commercial IC temperature range, or an extended range including the boiling point of water, can be directly read from the Specifications Table. All three error limits are a combination of initial error, scale factor variation and nonlinearity deviation from the ideal 1µA/K output. Figure 2 graphically depicts the guaranteed limits of accuracy for an AD592CN.

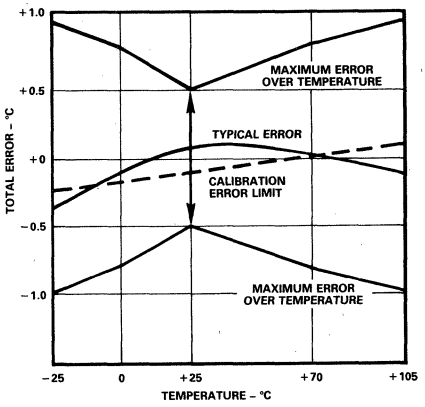


Figure 2. Error Specifications (AD592CN)

The AD592 has a highly linear output in comparison to older technology sensors (i.e., thermistors, RTDs and thermocouples), thus a nonlinearity error specification is separated from the absolute accuracy given over temperature. As a maximum deviation from a best-fit straight line this specification represents the only error which cannot be trimmed out. Figure 3 is a plot of typical AD592CN nonlinearity over the full rated temperature range.

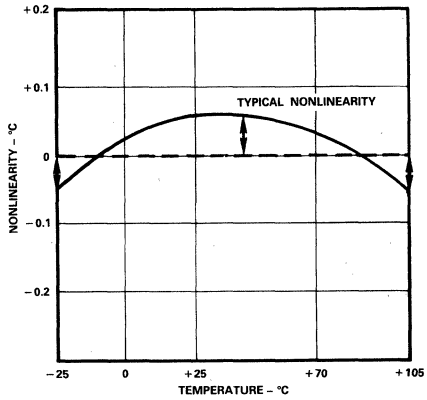


Figure 3. Nonlinearity Error (AD592CN)

TRIMMING FOR HIGHER ACCURACY

Calibration error at 25°C can be removed with a single temperature trim. Figure 4 shows how to adjust the AD592's scale factor in the basic voltage output circuit.

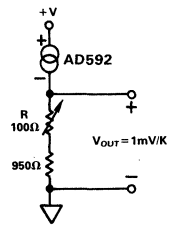


Figure 4. Basic Voltage Output (Single Temperature Trim)

To trim the circuit the temperature must be measured by a reference sensor and the value of R should be adjusted so the output (V_{OUT}) corresponds to 1mV/K. Note that the trim procedure should be implemented as close as possible to the temperature highest accuracy is desired for. In most applications if a single temperature trim is desired it can be implemented where the AD592 current-to-output voltage conversion takes place (e.g., output resistor, offset to an op amp). Figure 5 illustrates the effect on total error when using this technique.

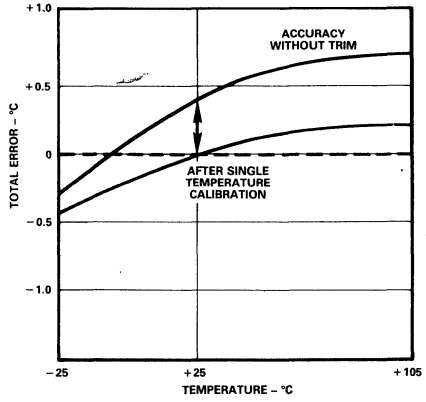


Figure 5. Effect of Scale Factor Trim on Accuracy

If greater accuracy is desired, initial calibration and scale factor errors can be removed by using the AD592 in the circuit of Figure 6.

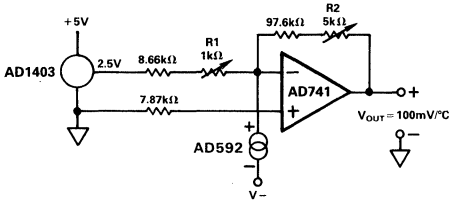


Figure 6. Two Temperature Trim Circuit

With the transducer at 0°C adjustment of R1 for a 0V output nulls the initial calibration error and shifts the output from K to °C. Tweaking the gain of the circuit at an elevated temperature by adjusting R2 trims out scale factor error. The only error remaining over the temperature range being trimmed for is nonlinearity. A typical plot of two trim accuracy is given in Figure 7.

SUPPLY VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection characteristics of the AD592 minimizes errors due to voltage irregularity, ripple and noise. If a supply is used other than 5V (used in factory trimming), the power supply error can be removed with a single temperature trim. The PTAT nature of the AD592 will remain unchanged. The general insensitivity of the output allows the use of lower cost unregulated supplies and means that a series resistance of several hundred ohms (e.g., CMOS multiplexer, meter coil resistance) will not degrade the overall performance.

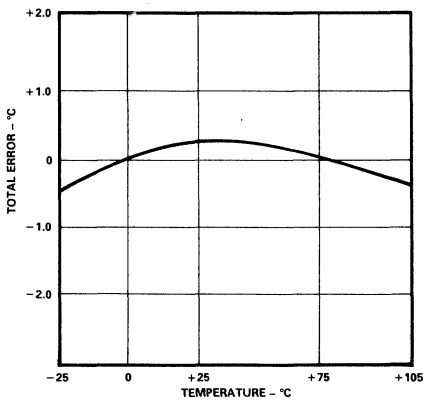


Figure 7. Typical Two Trim Accuracy

The thermal environment in which the AD592 is used determines two performance traits: the effect of self-heating on accuracy and the response time of the sensor to rapid changes in temperature. In the first case, a rise in the IC junction temperature above the ambient temperature is a function of two variables; the power consumption level of the circuit and the thermal resistance between the chip and the ambient environment (θ_{JA}). Self-heating error in °C can be derived by multiplying the power dissipation by θ_{JA}. Because errors of this type can vary widely for surroundings with different heat sinking capacities it is necessary to specify θ_{JA} under several conditions. Table I shows how the magnitude of self-heating error varies relative to the environment. In typical free air applications at 25°C with a 5V supply the magnitude of the error is 0.2°C or less. A common clip-on heat sink will reduce the error by 25% or more in critical high temperature, large supply voltage situations.

Medium	**θ_{JA} (°C/watt)**	**τ (sec)***
Still Air		
Without Heat Sink	175	60
With Heat Sink	130	55
Moving Air		
Without Heat Sink	60	12
With Heat Sink	40	10
Fluorinert Liquid	35	5
Aluminum Block**	30	2.4

*τ is an average of five time constants (99.3% of final value). In cases where the thermal response is not a simple exponential function, the actual thermal response may be better than indicated.
**With thermal grease.

Table I. Thermal Characteristics

Response of the AD592 output to abrupt changes in ambient temperature can be modeled by a single time constant τ exponential function. Figure 8 shows typical response time plots for several media of interest.

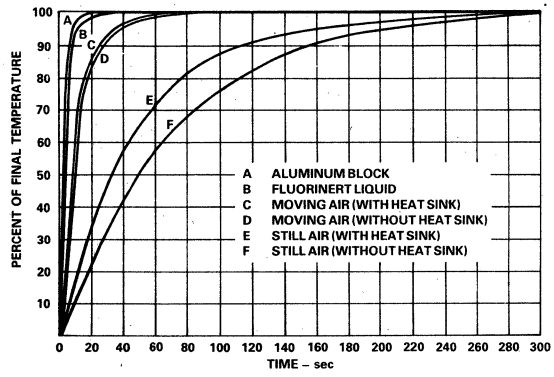


Figure 8. Thermal Response Curves

The time constant, τ, is dependent on θ_{JA} and the thermal capacities of the chip and the package. Table I lists the effective τ (time to reach 63.2% of the final value) for several different media. Copper printed circuit board connections where neglected in the analysis, however, they will sink or conduct heat directly through the AD592's solder dipped Kovar leads. When faster response is required a thermally conductive grease or glue between the AD592 and the surface temperature being measured should be used. In free air applications a clip-on heat sink will decrease output stabilization time by 10–20%.

MOUNTING CONSIDERATIONS

If the AD592 is thermally attached and properly protected, it can be used in any temperature measuring situation where the maximum range of temperatures encountered is between −25°C and +105°C. Because plastic IC packaging technology is employed, excessive mechanical stress must be safeguarded against when fastening the device with a clamp or screw-on heat tab. Thermally conductive epoxy or glue is recommended under typical mounting conditions. In wet or corrosive environments any electrically isolated metal or ceramic well can be used to shield the AD592. Condensation at cold temperatures can cause leakage current related errors and should be avoided by sealing the device in nonconductive epoxy paint or dips.

APPLICATIONS

Connecting several AD592 devices in parallel adds the currents through them and produces a reading proportional to the average temperature. Series AD592s will indicate the lowest temperature because the coldest device limits the series current flowing through the sensors. Both of these circuits are depicted in Figure 9.

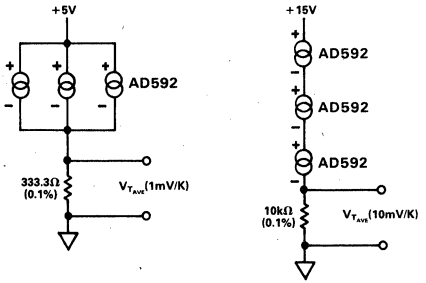


Figure 9. Average and Minimum Temperature Connections

The circuit of Figure 10 demonstrates a method in which a voltage output can be derived in a differential temperature measurement.

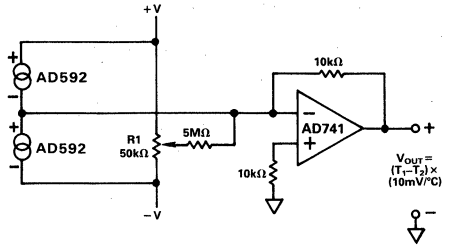


Figure 10. Differential Measurements

R1 can be used to trim out the inherent offset between the two devices. By increasing the gain resistor (10kΩ) temperature measurements can be made with higher resolution. If the magnitude of V+ and V− is not the same, the difference in power consumption between the two devices can cause a differential self-heating error.

Cold junction compensation (CJC) used in thermocouple signal conditioning can be implemented using an AD592 in the circuit configuration of Figure 11. Expensive simulated ice baths or hard to trim, inaccurate bridge circuits are no longer required.

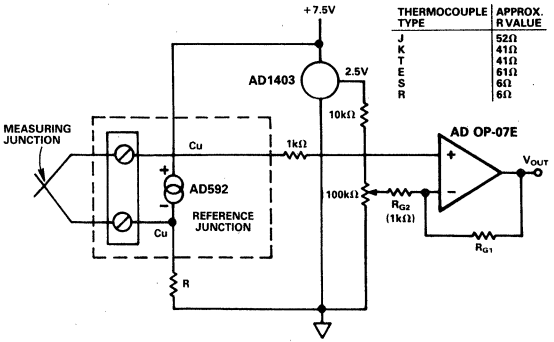


Figure 11. Thermocouple Cold Junction Compensation

The circuit shown can be optimized for any ambient temperature range or thermocouple type by simply selecting the correct value for the scaling resistor – R. The AD592 output (1μA/K) times R should approximate the line best fit to the thermocouple curve (slope in V/°C) over the most likely ambient temperature range. Additionally, the output sensitivity can be chosen by selecting the resistors R_{G1} and R_{G2} for the desired noninverting gain. The offset adjustment shown simply references the AD592 to °C. Note that the TC's of the reference and the resistors are the primary contributors to error. Temperature rejection of 40 to 1 can be easily achieved using the above technique.

Although the AD592 offers a noise immune current output, it is not compatible with process control/industrial automation current loop standards. Figure 12 is an example of a temperature to 4-20mA transmitter for use with 40V, 1kΩ systems.

In this circuit the 1μA/K output of the AD592 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. Rt is trimmed for proper reading at an

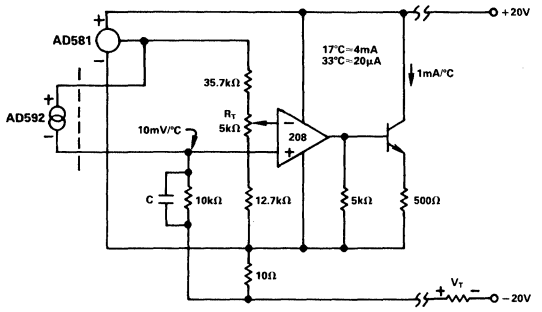


Figure 12. Temperature to 4–20mA Current Transmitter

intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD592 may be chosen.

Reading temperature with an AD592 in a microprocessor based system can be implemented with the circuit shown in Figure 13.

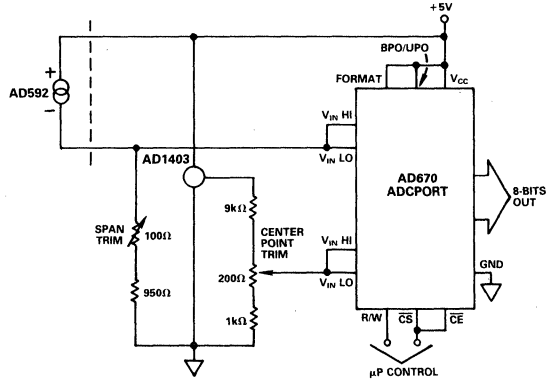


Figure 13. Temperature to Digital Output

By using a differential input A/D converter and choosing the current to voltage conversion resistor correctly any range of temperatures (up to the 130°C span the AD592 is rated for) centered at any point can be measured using a minimal number of components. In this configuration the system will resolve up to 1°C.

A variable temperature controlling thermostat can easily be built using the AD592 in the circuit of Figure 14.

R_{HIGH} and R_{LOW} determine the limits of temperature controlled by the potentiometer R_{SET}. The circuit shown operates over the full temperature range (−25°C to +105°C) the AD592 is rated for. The reference maintains a constant set point voltage and insures that approximately 7V appears across the sensor. If it is necessary to guardband for extraneous noise hysteresis can be added by tying a resistor from the output to the ungrounded end of R_{LOW}.

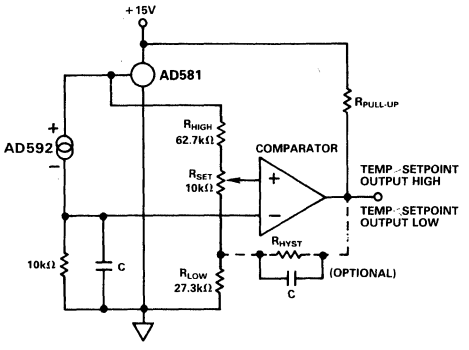


Figure 14. Variable Temperature Thermostat

Multiple remote temperatures can be measured using several AD592s with a CMOS multiplexer or a series of 5V logic gates because of the device's current-mode output and supply-voltage compliance range. The on-resistance of a FET switch or output impedance of a gate will not effect the accuracy, as long as 4V is maintained across the transducer. MUXs and logic driving circuits should be chosen to minimize leakage current related errors. Figure 15 illustrates a locally controlled MUX switching the signal current from several remote AD592s. CMOS or TTL gates can also be used to switch the AD592 supply voltages, with the multiplexed signal being transmitted over a single twisted pair to the load.

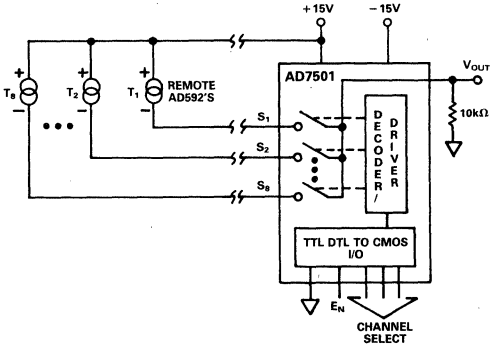


Figure 15. Remote Temperature Multiplexing

To minimize the number of MUXs required when a large number of AD592s are being used, the circuit can be configured in a matrix. That is, a decoder can be used to switch the supply voltage to a column of AD592s while a MUX is used to control which row of sensors are being measured. The maximum number of AD592s which can be used is the product of the number of channels of the decoder and MUX.

An example circuit controlling 80 AD592s is shown in Figure 16. A 7-bit digital word is all that is required to select one of the sensors. The enable input of the multiplexer turns all the sensors off for minimum dissipation while idling.

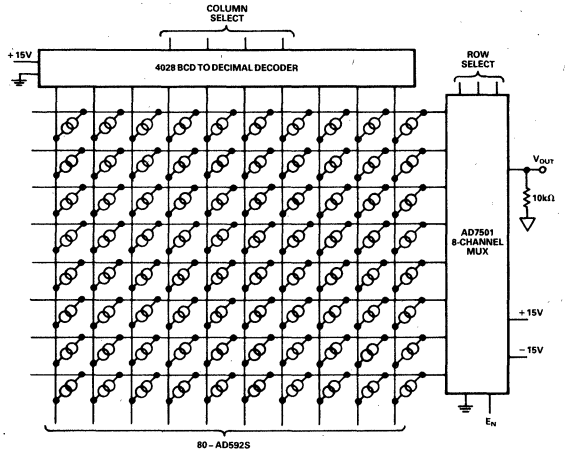
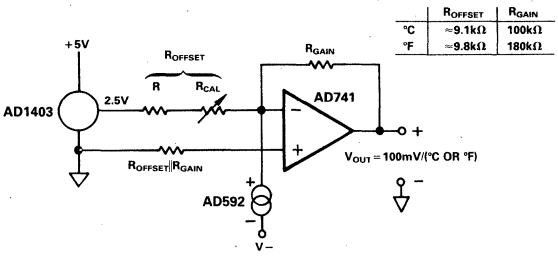


Figure 16. Matrix Multiplexer

To convert the AD592 output to °C or °F a single inexpensive reference and op amp can be used as shown in Figure 17. Although this circuit is similar to the two temperature trim circuit shown in Figure 6, two important differences exist. First, the gain resistor is fixed alleviating the need for an elevated temperature trim. Acceptable accuracy can be achieved by choosing an inexpensive resistor with the correct tolerance. Second, the AD592 calibration error can be trimmed out at a known convenient temperature (i.e., room temperature) with a single pot adjustment. This step is independent of the gain selection.



	R_{OFFSET}	R_{GAIN}
°C	≈9.1kΩ	100kΩ
°F	≈9.8kΩ	180kΩ

Figure 17. Celsius or Fahrenheit Thermometer

ANALOG DEVICES

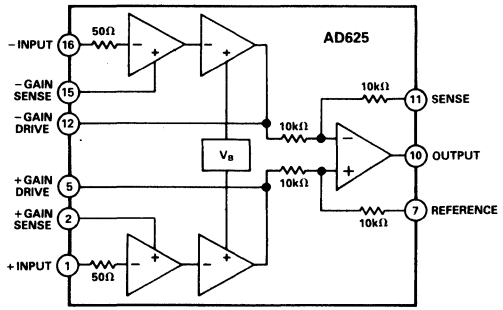
Programmable Gain Instrumentation Amplifier

AD625

FEATURES

User Programmed Gains of 1 to 10,000
Low Gain Error: 0.02% max
Low Gain TC: 5ppm/°C max
Low Nonlinearity: 0.001% max
Low Offset Voltage: 25μV
Low Noise 4nV/√Hz (at 1kHz) RTI
Gain Bandwidth Product: 25MHz
16-Pin Ceramic or Plastic DIP Package
MIL-Standard Parts Available
Low Cost

AD625 FUNCTIONAL BLOCK DIAGRAM



3

PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier specifically designed to fulfill two major areas of application:
1) Circuits requiring nonstandard gains (i.e., gains not easily achievable with devices such as the AD524 and AD624).
2) Circuits requiring a low cost, precision software programmable gain amplifier.

For low noise, high CMRR, and low drift the AD625JN is the most cost effective instrumentation amplifier solution available. An additional three resistors allow the user to set any gain from 1 to 10,000. The error contribution of the AD625JN is less than 0.05% gain error and under 5ppm/°C gain TC; performance limitations are primarily determined by the external resistors. Common-mode rejection is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network. Because the ON resistance of the switches is removed from the signal path, an AD625 based SPGA will deliver 12-bit precision, and can be programmed for any set of gains between 1 and 10,000, with completely user selected gain steps.

For the highest precision the AD625C offers an input offset voltage drift of less than 0.25μV/°C, output offset drift below 15μV/°C, and a maximum nonlinearity of 0.001% at G = 1. All grades exhibit excellent ac performance; a 25MHz gain bandwidth product, 5Vμs slew rate and 15μs settling time.

The AD625 is available in three accuracy grades (A, B, C) for industrial (−25°C to +85°C) temperature range, two grades (J, K) for commercial (0 to +70°C) temperature range, and one (S) grade rated over the extended (−55°C to +125°C) temperature range.

PRODUCT HIGHLIGHTS

1. The AD625 affords up to 16-bit precision for user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A 12-bit software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The gain accuracy and gain temperature coefficient of the amplifier circuit are primarily dependent on the user selected external resistors.
4. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
5. The proprietary design of the AD625 provides input voltage noise of 4nV/√Hz at 1kHz.
6. External resistor matching is not required to maintain high common-mode rejection.

SPECIFICATIONS (typical @ $V_S = \pm 15V$, $R_L = 2k\Omega$ and $T_A = +25°C$ unless otherwise specified)

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
GAIN										
Gain Equation		$\frac{2\ R_F}{R_G} + 1$			$\frac{2\ R_F}{R_G} + 1$			$\frac{2\ R_F}{R_G} + 1$		
Gain Range	1		10,000	1		10,000	1		10,000	
Gain Error[1]		±.035	**±0.05**		±0.02	**±0.03**		±0.01	**±0.02**	%
Nonlinearity, Gain = 1-256			±0.005			±0.002			±0.001	%
Gain>256			±0.01			±0.008			±0.005	%
Gain vs. Temp. Gain<1000[1]			5			5			5	ppm/°C
GAIN SENSE INPUT										
Gain Sense Current		300	**500**		150	**250**		50	**100**	nA
vs. Temperature		5	20		2	15		2	10	nA/°C
Gain Sense Offset Current		150	**500**		75	**250**		50	**100**	nA
vs. Temperature		2	15		1	10		1	5	nA/°C
VOLTAGE OFFSET (May be Nulled)										
Input Offset Voltage		50	**200**		25	**50**		10	**25**	µV
vs. Temperature		1	2/2		0.25	**0.50/1**		0.1	**0.25**	µV/°C
Output Offset Voltage		4	5		2	**3**		1	**2**	mV
vs. Temperature		20	50/**50**		10	**25/40**		10	**15**	µV/°C
Offset Referred to the Input vs. Supply										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	85	95		90	100		95	105		dB
G = 100	95	100		105	110		110	120		dB
G = 1000	**100**	110		**110**	120		**115**	140		dB
INPUT CURRENT										
Input Bias Current		±30	**±50**		±20	**±25**		±10	**±15**	nA
vs. Temperature		±50			±50			±50		pA/°C
Input Offset Current		±2	**±35**		±1	**±15**		±1	**±5**	nA
vs. Temperature		±20			±20			±20		pA/°C
INPUT										
Input Impedance										
Differential Resistance		1			1			1		GΩ
Differential Capacitance		4			4			4		pF
Common-Mode Resistance		1			1			1		GΩ
Common-Mode Capacitance		4			4			4		pF
Input Voltage Range										
Differ. Input Linear (V_D)			±10			±10			±10	V
Common Mode Linear (V_{CM})		$12V - \left(\frac{G}{2} \times V_D\right)$			$12V - \left(\frac{G}{2} \times V_D\right)$			$12V - \left(\frac{G}{2} \times V_D\right)$		
Common-Mode Rejection Ratio dc to 60Hz with 1kΩ Source Imbalance										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	90	95		95	105		100	115		dB
G = 100	100	105		105	115		110	125		dB
G = 1000	**110**	115		**115**	125		**120**	140		dB
OUTPUT RATING		±10V @ 5mA			±10V @ 5mA			±10V @ 5mA		
DYNAMIC RESPONSE										
Small Signal – 3dB										
G = 1 (R_F = 20kΩ)		650			650			650		kHz
G = 10		400			400			400		kHz
G = 100		150			150			150		kHz
G = 1000		25			25			25		kHz
Slew Rate		5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step										
G = 1 to 200		15			15			15		µs
G = 500		35			35			35		µs
G = 1000		75			75			75		µs
NOISE										
Voltage Noise, 1kHz										
R.T.I.		4			4			4		$nV/\sqrt{Hz}$
R.T.O.		75			75			75		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz										
G = 1		10			10			10		µV p-p
G = 10		1.0			1.0			1.0		µV p-p
G = 100		0.3			0.3			0.3		µV p-p
G = 1000		0.2			0.2			0.2		µV p-p
Current Noise										
0.1Hz to 10Hz		60			60			60		pA p-p
SENSE INPUT										
R_{IN}		10			10			10		kΩ
I_{IN}		30			30			30		µA
Voltage Range	±10			±10			±10			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%

Model	AD625A/J/S Min	Typ	Max	AD625B/K Min	Typ	Max	AD625C Min	Typ	Max	Units
REFERENCE INPUT										
R_{IN}		20			20			20		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
TEMPERATURE RANGE										
Specified Performance										
J/K Grades	0		+70	0		+70				°C
A/B/C Grades	−25		+85	−25		+85	−25		+85	°C
S Grade	−55		+125							°C
Storage	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY										
Power Supply Range		±5 to ±18			±5 to ±18			±5 to ±18		V
Quiescent Current		3.5	5		3.5	5		3.5	5	mA

NOTES

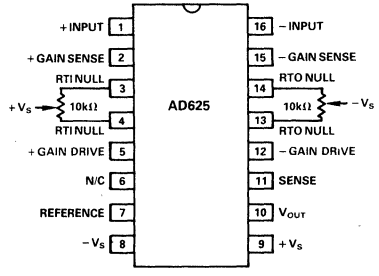
[1]Gain Error and Gain TC are for the AD625 only. Resistor Network errors will add to the specified errors.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All mim and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

3

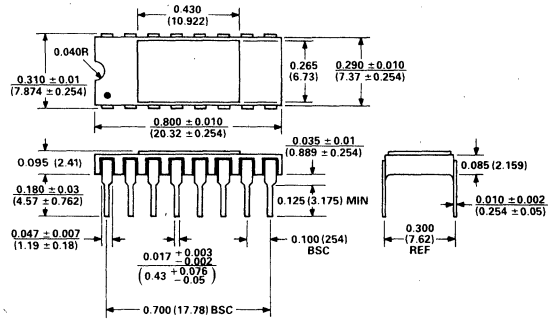
PIN CONFIGURATION



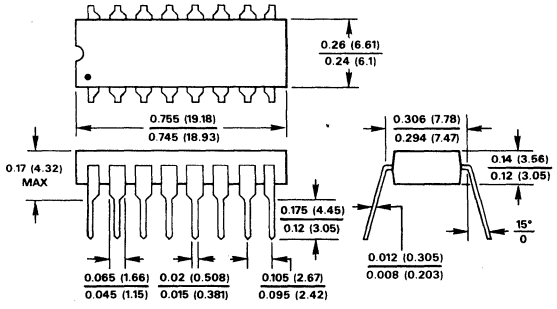
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-PIN CERAMIC PACKAGE



N16B
16-PIN PLASTIC DIP PACKAGE



Typical Characteristics

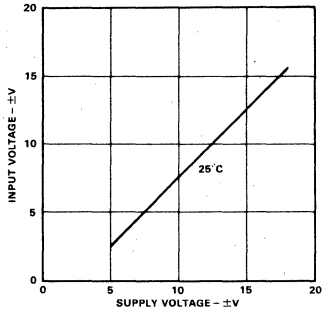


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

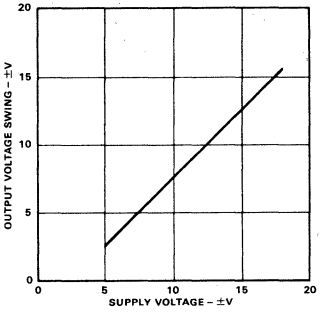


Figure 2. Output Voltage Swing vs. Supply Voltage

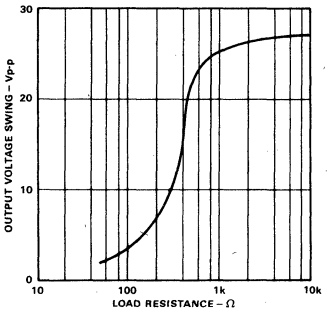


Figure 3. Output Voltage Swing vs. Resistive Load

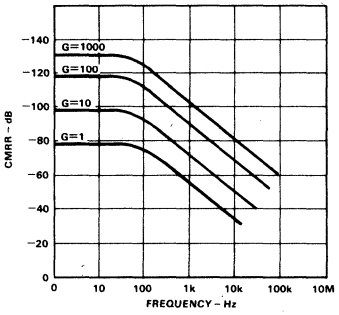


Figure 4. CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

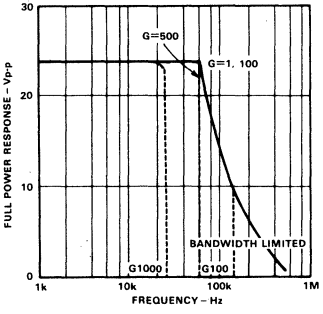


Figure 5. Large Signal Frequency Response

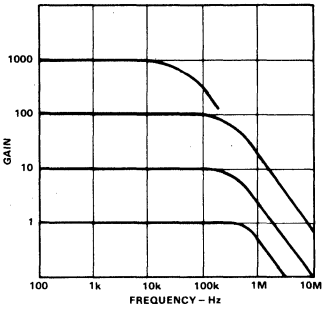


Figure 6. Gain vs. Frequency

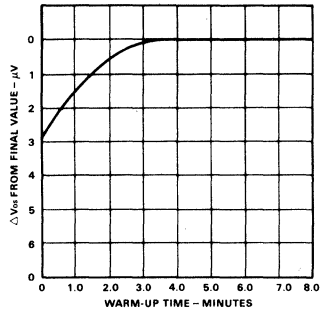


Figure 7. Offset Voltage, RTI, Turn On Drift

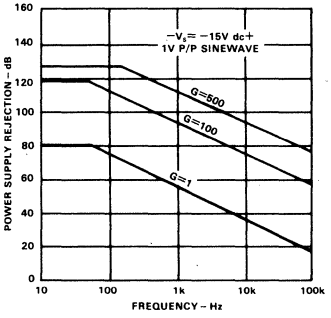


Figure 8. Negative PSRR vs. Frequency

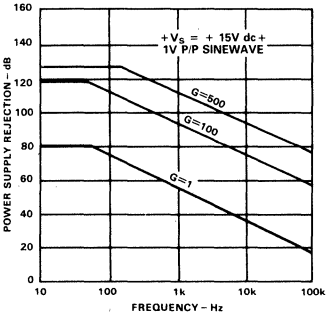


Figure 9. Positive PSRR vs. Frequency

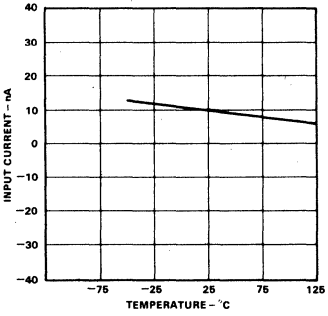


Figure 10. Input Bias Current vs. Temperature

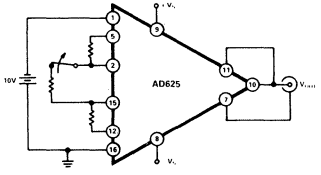


Figure 11. Overange and Gain Switching Test Circuit (G=8, G=1)

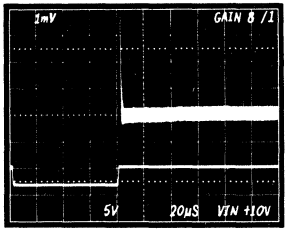


Figure 12. Gain Overange Recovery

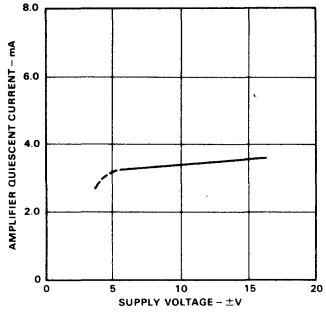


Figure 13. Quiescent Current vs. Supply Voltage

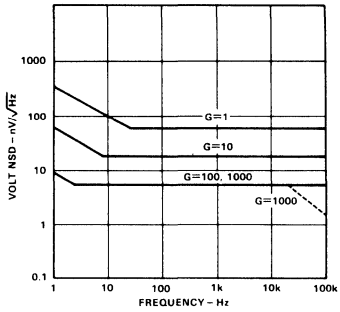


Figure 14. RTI Noise Spectral Density vs. Gain

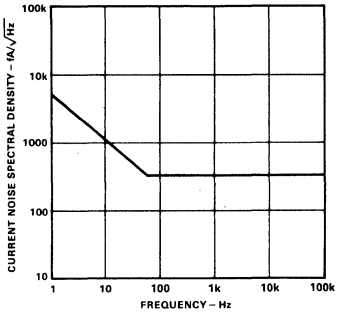


Figure 15. Input Current Noise

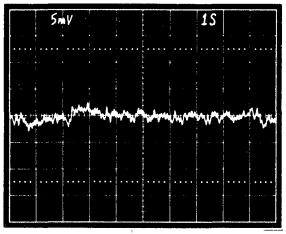


Figure 16. Low Frequency Voltage Noise, G=1 (System Gain=1000)

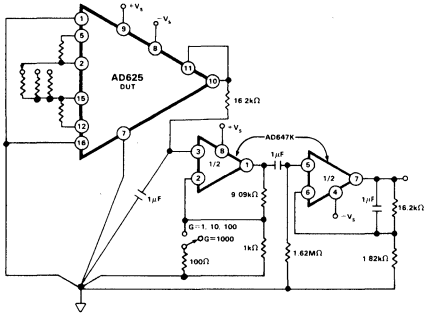


Figure 17. Noise Test Circuit

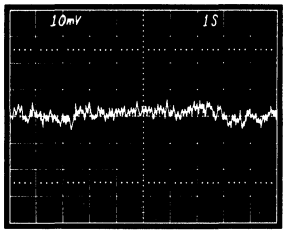


Figure 18. Low Frequency Voltage Noise, G=1000 (System Gain=100,000)

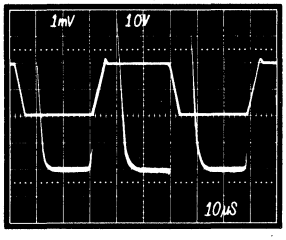


Figure 19. Large Signal Pulse Response and Settling Time, G=1

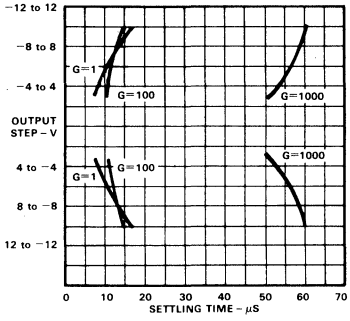


Figure 20. Settling Time to 0.01%

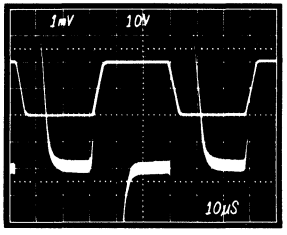


Figure 21. Large Signal Pulse Response and Settling Time, G = 100

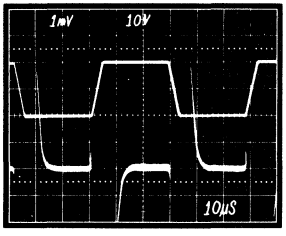


Figure 22. Large Signal Pulse Response and Settling Time, G = 10

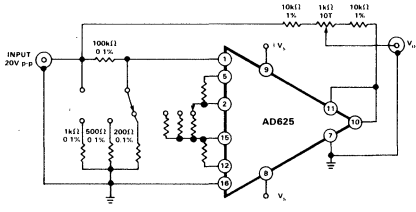


Figure 23. Settling Time Test Circuit

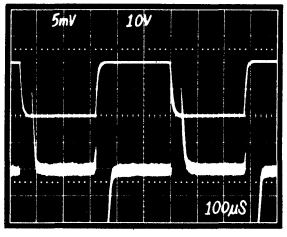


Figure 24. Large Signal Pulse Response and Settling Time, G=1000

Theory of Operation

The AD625 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp section (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G + 1$) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

The value of R_G is the determining factor of the transconductance of the input preamp stage. As R_G is reduced for larger gains the transconductance increases. This has three important advantages. First, this approach allows the circuit to achieve a very high open-loop gain of (3×10^8 at programmed gains $\geq$ 500) thus reducing gain related errors. Second, the gain-bandwidth product, which is determined by C3, C4, and the input transconductance, increases with gain, thereby, optimizing frequency response. Third, the input voltage noise is reduced to a value determined by the collector current of the input transistors ($4nV/\sqrt{Hz}$).

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the AD625; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is ($R_G + 100$)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 40Ω), the maximum overload voltage the AD625 can withstand, continuously, is approximately ±2.5V. Figure 26A shows the external components necessary to protect the AD625 under all overload conditions at any gain.

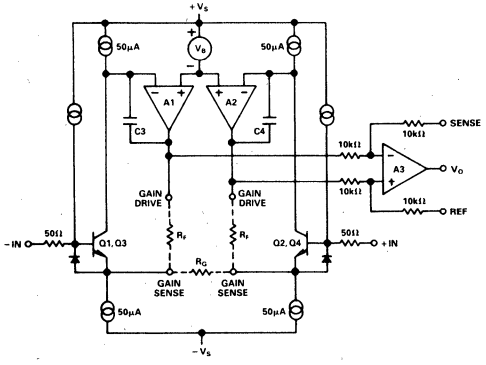


Figure 25. Simplified Circuit of the AD625

The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered. In higher gain applications where differential voltages are small, back-to-back zener diodes and smaller resistors, as shown in Figure 26b, provides adequate protection. Figure 26c shows low cost FETs with a maximum ON resistance of 300Ω configured to offer input protection with minimal degradation to noise, ($5.2nV/\sqrt{Hz}$ compared to normal noise performance of $4nV/\sqrt{Hz}$).

During differential overload conditions, excess current will flow through the gain sense lines (pins 2 and 15). This will have no effect in fixed gain applications. However, if the AD625 is being used in an SPGA application with a CMOS multiplexer, this current should be taken into consideration. The current capabilities of the multiplexer may be the limiting factor in allowable overflow current. The ON resistance of the switch should be included as part of R_G when calculating the necessary input protection resistance.

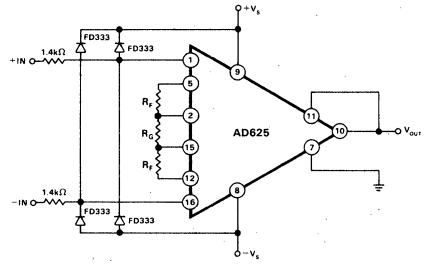


Figure 26a. Input Protection Circuit

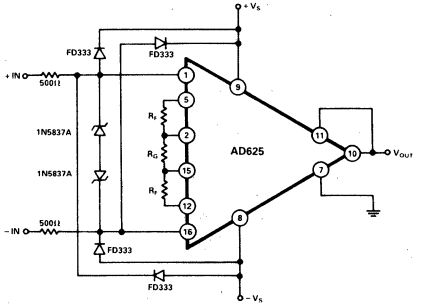


Figure 26b. Input Protection Circuit for G>5

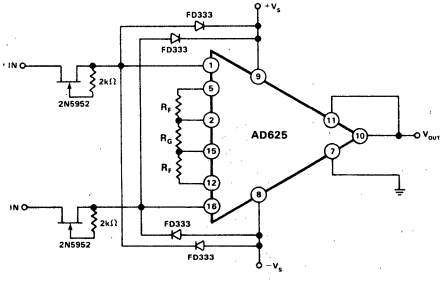


Figure 26c. Input Protection Circuit

Any resistors in series with the inputs of the AD625 will degrade the noise performance. For this reason the circuit in Figure 26b should be used if the gains are all greater than 5. For gains less than 5, either the circuit in Figure 26a or in Figure 26c can be used. The two 1.4kΩ resistors in Figure 26a will degrade the noise performance to:

$$\sqrt{4kTR_{ext} + (4nV/\sqrt{Hz})^2} = 7.9nV/\sqrt{Hz}$$

RESISTOR PROGRAMMABLE GAIN AMPLIFIER

In the resistor-programmed mode (Figure 27), only three external resistors are needed to select any gain from 1 to 10,000. Depending on the application, discrete components or a pretrimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625C contributes less than 0.02% to gain error and under 5ppm/°C gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors, R_F.

Selecting Resistor Values

As previously stated each R_F provides feedback to the input stage and sets the unity gain transconductance. These feedback resistors are provided by the user. The AD625 is tested and specified with a value of 20kΩ for R_F. Since the magnitude of RTO errors increases with increasing feedback resistance, values much above 20kΩ are not recommended (values below 10kΩ for R_F may lead to instability). Refer to the graph of RTO noise, offset, drift, and bandwidth (Figure 28) when selecting the feedback resistors. The gain resistor (R_G) is determined by the formula $R_G = 2R_F/(G-1)$.

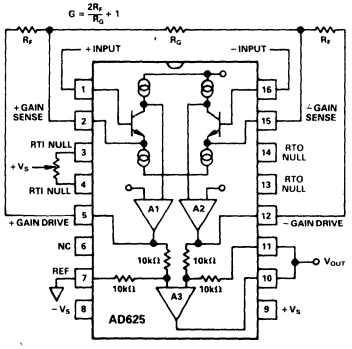


Figure 27. AD625 in Fixed Gain Configuration

A list of standard resistors which can be used to set some common gains is shown in Table I.

For single gain applications, only one offset null adjust is necessary; in these cases the RTI null should be used.

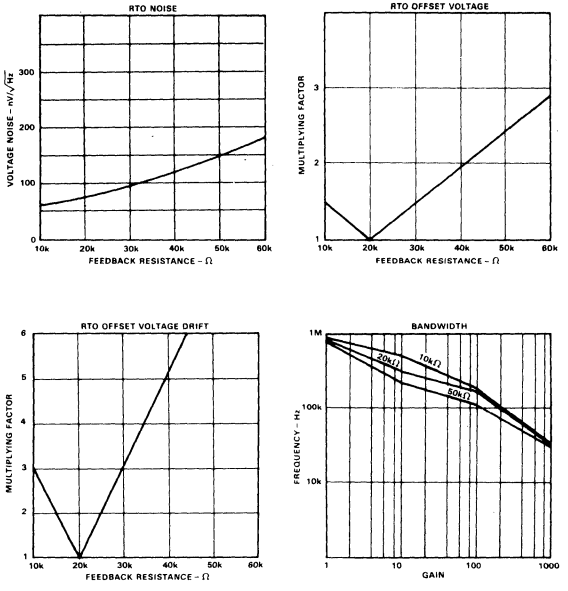


Figure 28. RTO Noise, Offset, Drift, and Bandwidth vs. Feedback Resistance Normalized to 20kΩ

GAIN	R_F	R_G
1	20kΩ	∞
2	19.6kΩ	39.2kΩ
5	20kΩ	10kΩ
10	20kΩ	4.42kΩ
20	20kΩ	2.1kΩ
50	19.6kΩ	806Ω
100	20kΩ	402Ω
200	20.5kΩ	205Ω
500	19.6kΩ	78.7Ω
1000	19.6kΩ	39.2Ω
4	20kΩ	13.3kΩ
8	19.6kΩ	5.62kΩ
16	20kΩ	2.67kΩ
32	19.6kΩ	1.27kΩ
64	20kΩ	634Ω
128	20kΩ	316Ω
256	19.6kΩ	154Ω
512	19.6kΩ	76.8Ω
1024	19.6kΩ	38.3Ω

Table I. Common Gains Nominally within ±0.5% Error Using Standard 1% Resistors

SENSE TERMINAL

The sense terminal is the feedback point for the AD625 output amplifier. Normally it is connected directly to the output. If heavy load currents are to be drawn through long leads, voltage drops through lead resistance can cause errors. In these instances the sense terminal can be wired to the load thus putting the I × R drops "inside the loop" and virtually eliminating this error source.

Typically, IC instrumentation amplifiers are rated for a full ± 10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 29 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier. By using an external power boosting circuit, the power dissipated by the AD625 will remain low, thereby, minimizing the errors induced by self-heating. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the AD625's output amplifier.

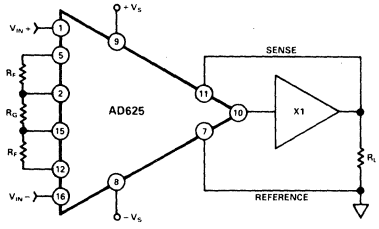


Figure 29. AD625 Instrumentation Amplifier with Output Current Booster

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ± 10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. However, it must be remembered that the total output swing is ± 10 volts, from ground, to be shared between signal and reference offset.

The AD625 reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 30. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

The circuit of Figure 30 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$, however, to be symmetrical about 0V $R_3 = 2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 30 is ± 120mV, and the offset is incremented in steps of 0.9375mV/LSB.

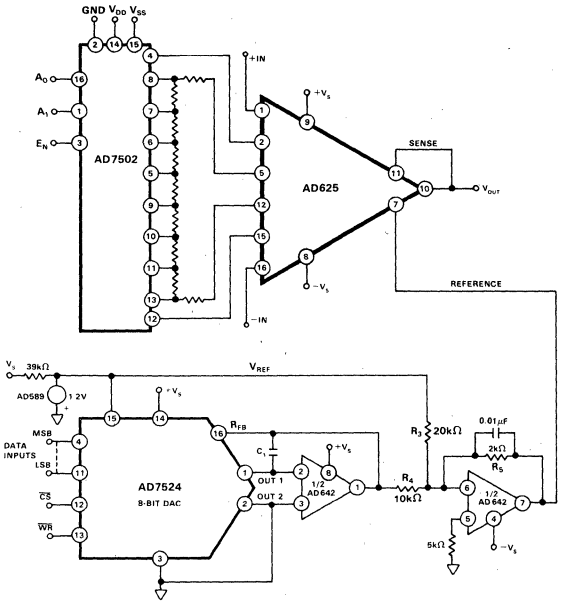


Figure 30. Software Controllable Offset

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 31.

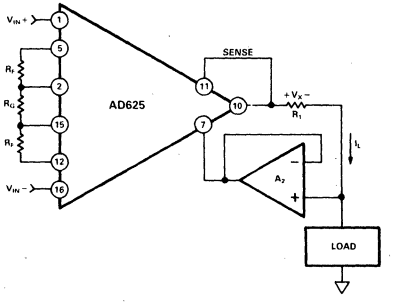


Figure 31. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A1, the forced current I_L will largely flow through the load. Offset and drift specifications of A2 must be added to the output offset and drift specifications of the In-Amp.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains.

The input offset and drift are multiplied by the gain, while the output terms are independent of gain, therefore, input errors dominate at high gains and output errors dominate at low gains. The output offset voltage (and drift) is normally specified at G = 1 (where input effects are insignificant), while input offset (and drift) is given at a high gain (where output effects are negligible). All input-related parameters are specified referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Offset voltage vs. power supply is also specified as an RTI error.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain × input error) + output error

The AD625 provides for both input and output offset voltage adjustment. This simplifies nulling in very high perecision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 show active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

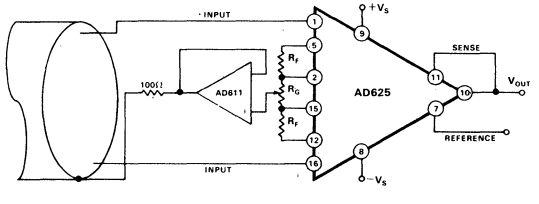


Figure 32. Common-Mode Shield Driver

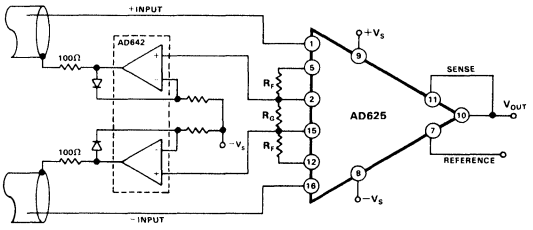


Figure 33. Differential Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 34). Since the AD625 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

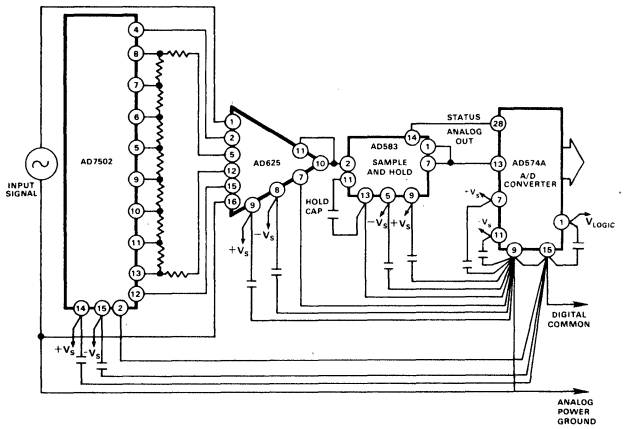


Figure 34. Basic Grounding Practice for a Data Acquisition System

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 35.

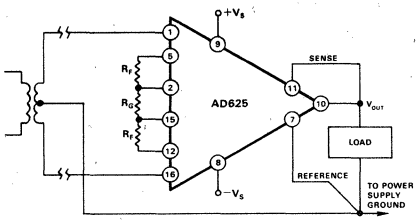


Figure 35a. Ground Returns for Bias Currents with Transformer Coupled Inputs

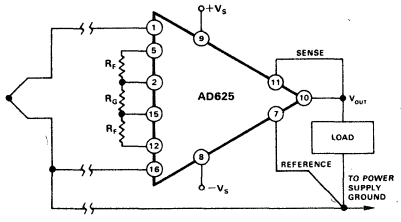


Figure 35b. Ground Returns for Bias Currents with Thermocouple Input

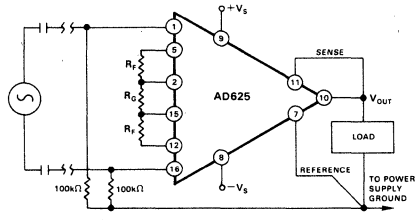


Figure 35c. Ground Returns for Bias Currents with AC Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 36 provides a hardware solution.

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD625) remain isothermal. This includes the input leads (1, 16) and the gain sense lines (2, 15). These pins were chosen for symmetry, helping to desensitize the input circuit to thermal gradients. In addition, the user should also avoid air currents

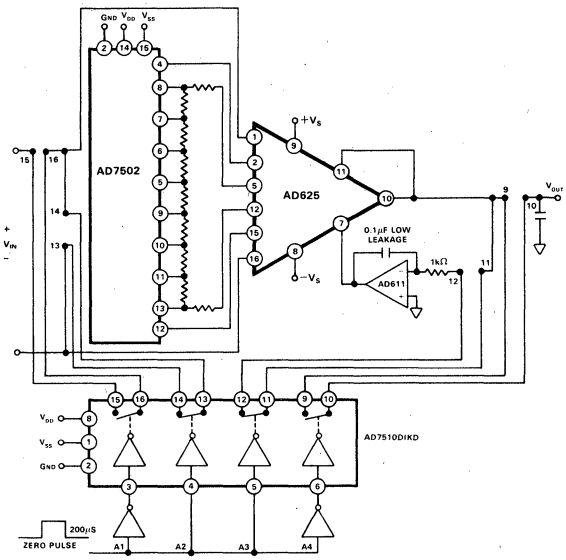


Figure 36. Auto-Zero Circuit

over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise. In SPGA applications relay contacts and CMOS mux leads are both potential sources of additional thermocouple errors.

The base emitter junction of an input transistor can rectify out of band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. The AD625 allows direct access to the input transistors' bases and emitters enabling the user to apply some first order filtering to these unwanted signals. In Figure 37, the RC time constant should be chosen for desired attenuation of the interfering signals. In the case of a resistive transducer, the capacitance alone working against the internal resistance of the transducer may suffice.

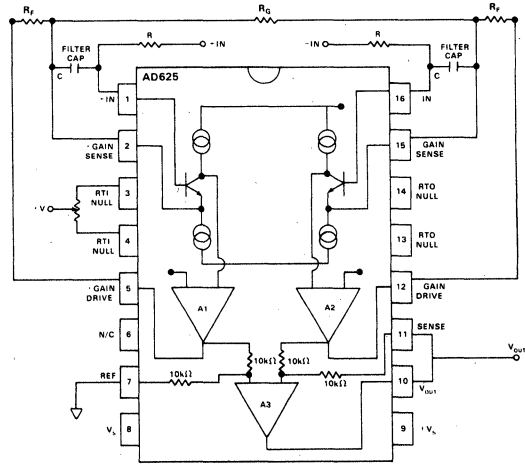


Figure 37. Circuit to Attenuate RF Interference

These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 15 and 2, and pins 1 and 16, to preserve high ac CMR.

SOFTWARE PROGRAMMABLE GAIN AMPLIFIER

An SPGA provides the ability to externally program precision gains from digital inputs. Historically, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain drive and gain sense pins available (pins 2, 15, 5, 12; see Figure 39). Consequently the multiplexer's ON resistance is removed from the signal current path. This transforms the ON resistance error into a small nullable offset error. To clarify this point, an error budget analysis has been performed in Table II based on the SPGA configuration shown in Figure 39.

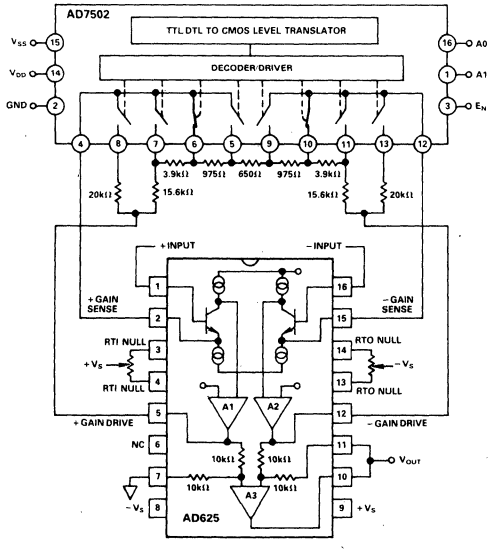


Figure 38. SPGA in a Gain of 16

Figure 38 shows an AD625 based SPGA with possible gains of 1, 4, 16, 64. R_G equals the resistance between the gain sense lines (pins 2 and 15) of the AD625. In Figure 38, R_G equals the sum of the two 975Ω resistors and the 650Ω resistor, or 2600Ω. R_F equals the resistance between the gain sense and the gain drive pins (pins 12 and 15, or pins 2 and 5), that is R_F equals the 15.6kΩ resistor plus the 3.9kΩ resistor, or 19.5kΩ. The gain, therefore equals:

$$\frac{2R_F}{R_G} + 1 = \frac{2(19.5k\Omega)}{(2.6k\Omega)} + 1 = 16$$

As the switches of the differential multiplexer proceed synchronously, R_G and R_F change, resulting in the various programmed gain settings.

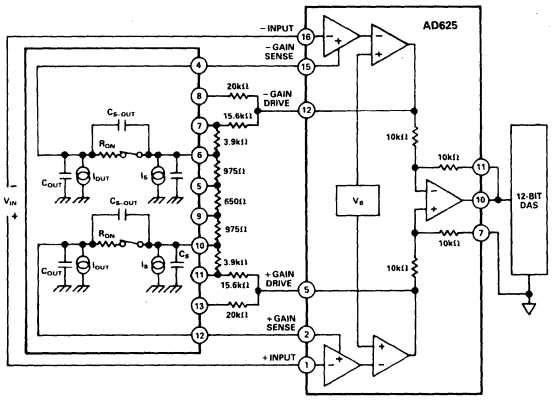


Figure 39. SPGA with Multiplexer Error Sources

Figure 39 shows a complete SPGA feeding a 12-bit DAS with a 0–10V input range. This configuration was used in the error budget analysis shown in Table II. The gain used for the RTI calculations is set at 16. As the gain is changed, the ON resistance of the multiplexer and the feedback resistance will change, which will slightly alter the values in the table.

Induced Error	Specification AD625C	Specification AD7502KN	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 40nA	Switch Resistance 170Ω	40nA × 170Ω = 6.8μV	6.8μV
RTI Offset Voltage	Gain Sense Current 60nA	Differential Switch Resistance 6.8Ω	60nA × 6.8Ω = 0.41μV	0.41μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current (I_S)[2] +0.2nA −0.2nA	2(0.2nA × 20kΩ) = 8μV/16	0.5μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current (I_{OUT})[2] +1nA −1nA	2(1nA × 20kΩ) = 40μV/16	2.5μV
Total error induced by a typical CMOS multiplexer to an SPGA at 25°C				**10.21μV**

NOTES

[1]The resistor for this calculation is the user provided feedback resistance (R_F). 20kΩ is recommended value (see resistor programmable gain amplifier section).

[2]The leakage currents (I_S and I_{OUT}) will induce an offset voltage, however, the offset will be determined by the difference between the leakages of each "half" of the differential multiplexer. The differential leakage current is multiplied by the feedback resistance (see Note 1),to determine offset voltage. Because differential leakage curent is not a parameter specified on multiplexer data sheets, the most extreme difference (one most positive and one most negative) was used for the calculations in Table II. Typical performance will be much better.

*The frequency response and settling will be affected by the ON resistance and internal capacitance of the multiplexer. Figure 40 shows the settling time vs. ON resistance at different gain settings for an AD625 based SPGA.

**Switch resistance and leakage current errors can be reduced by using relays.

Table II. Errors Induced by Multiplexer to an SPGA

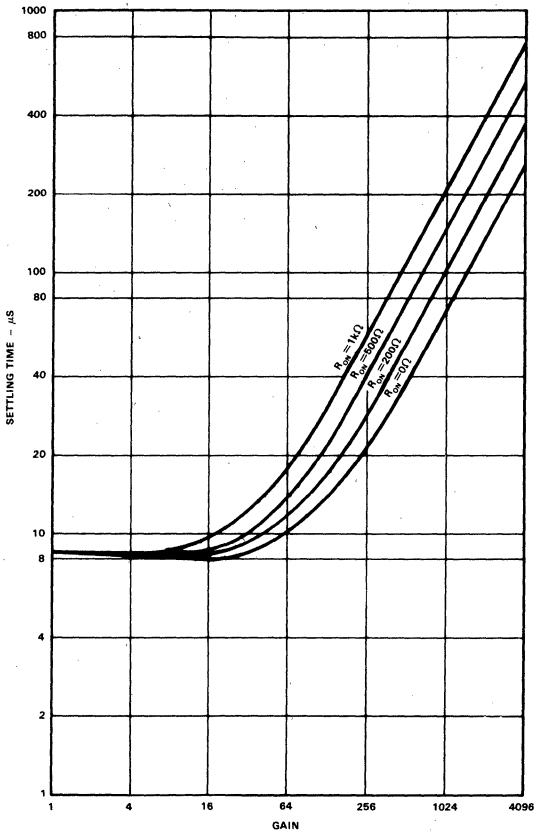


Figure 40. Settling Time to 0.01% of a 20V Step Input for SPGA with AD625

DETERMINING SPGA RESISTOR NETWORK VALUES

The individual resistors in the gain network can be calculated sequentially using the formula given below. The equation determines the resistors as labeled in Figure 41. The feedback resistors and the gain setting resistors are interactive, therefore; the formula must be a series where the present term is dependent on the preceding term(s). The formula

$$R_{F_{i+1}} = (20k\Omega - \sum_{j=0}^{i} R_{F_j})\left(1 - \frac{G_i}{G_{i+1}}\right) \qquad \begin{matrix} G_0 = 1 \\ R_{F_0} = 0 \end{matrix}$$

can be used to calculate the necessary feedback resistors for any set of gains. This formula yields a network with a total resistance of 40kΩ. A dummy variable (j) serves as a counter to keep a running total of the preceding feedback resistors. To illustrate how the formula can be applied, an example similar to the calculation used for the resistor network in Figure 38 is examined below.

1) Unity gain is treated as a separate case. It is implemented with separate 20kΩ feedback resistors as shown in Figure 41. It is then ignored in further calculations.

2) Before making any calculations it is advised to draw a resistor network similar to the network in Figure 41. The network will have (2 × M) + 1 resistors, where M = number of gains. For Figure 38 M = 3 (4, 16, 64), therefore, the resistor string will have 7 resistors (plus the two 20kΩ "side" resistors for unity gain).

3) Begin all calculations with $G_0 = 1$ and $R_{F_0} = 0$.

$R_{F_1} = (20k\Omega - R_{F_0})\,(1 - 1/4)$: $R_{F_0} = 0 \therefore R_{F_1} = 15k\Omega$

$R_{F_2} = [20k\Omega - (R_{F_0} + R_{F_1})]\,(1 - 4/16)$:

$R_{F_0} + R_{F_1} = 15k\Omega \therefore R_{F_2} = 3.75k\Omega$

$R_{F_3} = [20k\Omega - (R_{F_0} + R_{F_1} + R_{F_2})]\,(1 - 16/64)$:

$R_{F_0} + R_{F_1} + R_{F_2} = 18.75k\Omega \therefore R_{F_3} = 937.5\Omega$

4) The center resistor (R_G of the highest gain setting), is determined last. Its value is the remaining resistance of the 40kΩ string, and can be calculated with the equation:

$$R_G = (40k\Omega - 2\sum_{j=0}^{M} R_{F_j})$$

$$R_G = 40k\Omega - 2(R_{F_0} + R_{F_1} + R_{F_2} + R_{F_3})$$

$$40k\Omega - 39.375k\Omega = 625\Omega$$

5) If different resistor values are desired, all the resistors in the network can be scaled by some convenient factor. However, raising the impedance will increase the RTO errors, lowering the total network resistance below 20kΩ can result in amplifier instability. More information on this phenomenon is given in the RPGA section of the data sheet. The scale factor will not affect the unity gain feedback resistors. The resistor network in Figure 38 has a scaling factor of 650/625 = 1.04, if this factor is used on R_{F_1}, R_{F_2}, R_{F_3}, and R_G, then the resistor values will match exactly.

6) Round off errors can be cumulative, therefore, it is advised to carry as many significant digits as possible until all the values have been calculated.

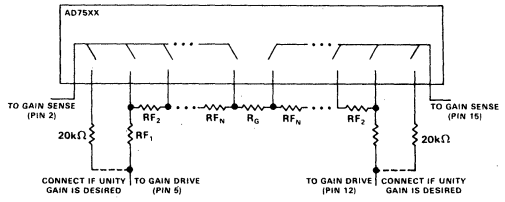


Figure 41. Resistors for a Gain Setting Network

ANALOG DEVICES

Universal Trigonometric Function Generator

AD639*

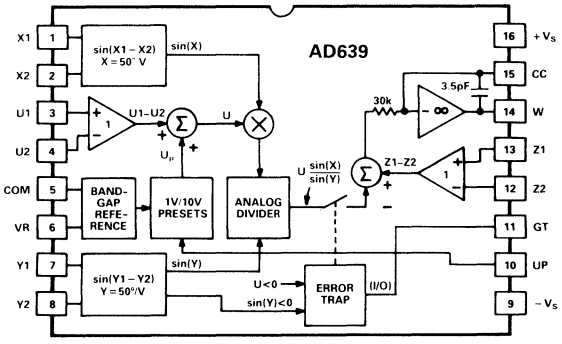
FEATURES

Complete, Fully-Calibrated Synthesis System
All Standard Functions: Sin, Cos, Tan, Cosec, Sec, Cot, Arcsin, Arccos, Arctan, etc.
Accurate Law Conformance (Sine to 0.02%)
Angular Range of ±500° (Sine Mode)
Function Programmable by Pin Strapping
1.5MHz Bandwidth (Sine Mode)
Multiplication via External Amplitude Input

APPLICATIONS

Continuous Wave Sine Generators
Synchro Sine/Cosine Multiplication
Coordinate Conversion and Vector Resolution
Imaging and Scanning Linearization Circuits
Quadrature and Variable Phase Oscillators

AD639 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD639 is a high accuracy monolithic function generator which provides all the standard trigonometric functions and their inverses via pin-strapping. Law conformance and total harmonic distortion surpass that previously attained using analog shaping techniques. Speed also exceeds that possible using ROM look-up tables and a DAC; in the sine mode, bandwidth is typically 1.5MHz. Unlike other function synthesis circuits, the AD639 provides a smooth and continuous sine conformance over a range of −500° to +500°. A unique sine generation technique results in 0.02% law conformance errors and distortion levels of −74dB in triwave to sinewave conversion.

The AD639 is available in three performance grades. The A and B are specified from −25°C to +85°C and the S is guaranteed over the extended temperature range of −55°C to +125°C. All versions are packaged in a hermetic TO-116, 16-pin ceramic DIP.

PRODUCT HIGHLIGHTS

The AD639 generates a basic function which is the ratio of a pair of independent sines:

$$W = U \frac{\sin (x_1 - x_2)}{\sin (y_1 - y_2)}$$

*Protected by U.S. Patent Numbers 3,887,863; 4,475,169; 4,476,538.

The differential angle arguments are proportional to the input voltages X and Y scaled by 50°/V. Using the 1.8V on-board reference any of the angular inputs can be preset to 90°. This provides the means to set up a fixed numerator or denominator (sin 90° = 1) or to convert either sine function to a cosine (cosθ = sin (90° − θ)). Using the ratio of sines, all trigonometric functions can be generated (see Table I).

The amplitude of the function is proportional to a voltage U, which is the sum of an external differential voltage ($U_1 - U_2$) and an optional internal preset voltage (U_p). The control pin UP selects a 0V, 1V or 10V laser-trimmed preset amplitude which may be used alone ($U_1 - U_2 = 0$) or internally added to the $U_1 - U_2$ analog input. At the output, a further differential voltage Z can be added to the ratio of sines to obtain the offset trigonometric functions versine (1 − cos θ), coversine (1 − sin θ) and exsecant (1 − sec θ). A gating input is available which may be used to enable or disable the analog output. This pin also acts as an error flag output in situations where a combination of inputs will cause the output to saturate or to be undefined.

In the inverse modes, the argument can be the ratio of two input signals. This allows the user to compute the phase angle between the real and imaginary components of a signal using the arctangent mode.

SPECIFICATIONS (typical @T_A = 25°C, V_S = ±15V, U or U_p = 10V unless otherwise specified)

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SYSTEM PERFORMANCE											
SINE AND COSINE											
MODE ACCURACY											
Law Conformance[1]	−90° to +90°, U = 10V		0.02			0.02			0.02		%
Total Harmonic											
Distortion[2]	@10kHz, U = 10V		−74			−74			−74		dB
Mismatch of Six Peaks	−540° to +540°		0.05			0.05			0.05		%
Output Noise	@10kHz, U = 10V		2.8			2.8			2.8		$\mu V/\sqrt{Hz}$
	@10kHz, U = 1V		0.5			0.5			0.5		$\mu V/\sqrt{Hz}$
PEAK ABSOLUTE ERROR											
Sine Mode	−90° to +90°, U_p = 10V		0.4	**0.8**		0.2	**0.4**		0.4	**0.8**	%FS
	T_{min} to T_{max}		1.0			0.8	**1.8**		2.0	**3.0**	%FS
Cosine Mode	−90° to +90°, U_p = 10V		0.6	**1.2**		0.4	**0.7**		0.6	**1.2**	%FS
	T_{min} to T_{max}		1.5			1.2	**2.0**		2.0	**3.3**	%FS
Sine or Cosine	−180° to +180°, U_p = 10V		0.8	**1.5**		0.5	**0.8**		0.8	**1.5**	%FS
	T_{min} to T_{max}		1.7			1.3	**2.5**		2.8	**4.0**	%FS
	−360° to +360°, U_p = 10V		1.2			1.0			1.2		%FS
	−90° to +90°, U_p = 1V		1.3	**2.5**		1.0	**1.7**		1.3	**2.5**	%FS
	T_{min} to T_{max}		1.5			1.0	**2.3**		2.0	**3.5**	%FS
	−180° to +180°, U_p = 1V		1.5	**3.0**		1.2	**2.0**		1.5	**3.0**	%FS
	T_{min} to T_{max}		1.7			1.3	**2.5**		2.3	**4.2**	%FS
	−360° to +360°, U_p = 1V		2.0			1.8			2.0		%FS
vs Supply	−360° to +360°, U_p = 10V V_s = ±15V ±1V		0.02			0.02			0.02		%FS/V
	−360° to +360°, U_p = 1V V_s = ±15V ±1V		0.07			0.07			0.07		%FS/V
TANGENT MODE ACCURACY											
Peak Error[3]	−45° to +45°, U_p = 10V		2.0	**3.5**		1.0	**2.0**		2.0	**3.5**	%FS
	T_{min} to T_{max}		2.5			1.5	**2.8**		3.0		%FS
	−45° to +45°, U_p = 1V		3.0	**5.0**		1.5	**3.0**		3.0	**5.0**	%FS
	T_{min} to T_{max}		4.0			2.0	**5.0**				%FS
ARCTANGENT MODE ACCURACY											
Peak Angular Error											
Fixed Scale	U_p = 1V		1.5			1.5			1.5		Degrees
Variable Scale	U = 0.1V, −11V≤Z≤+11V		2.5			2.5			2.5		Degrees
	U = 10V, −11V≤Z≤+11V		0.5			0.5			0.5		Degrees
SECTIONAL SPECIFICATIONS											
ANGLE INPUTS (X1 & X2, Y1 & Y2)[4]											
Input Resistance to COM			3.6			3.6			3.6		kΩ
Nominal Scaling Factor			50			50			50		°/V
X1 & X2 Inputs											
Angular Range For											
Specified Error(X1 − X2)		−360		+360	−360		+360	−360		+360	Degrees
Scaling Error X1 or X2			0.2	**0.65**		0.2	**0.65**		0.2	**0.65**	%
Angular Offset X1 = X2 = 0			0.1	**0.3**		0.1	**0.3**		0.1	**0.3**	Degrees
Y1 & Y2 Inputs											
Angular Range For											
Specified Error (Y1 − Y2)		0		+180	0		+180	0		+180	Degrees
Scaling Error Y1 or Y2			1.0	**2.0**		1.0	**2.0**		1.5	**2.0**	%
Angular Offset Y1 = Y2 = 0			0.5	**1.0**		0.5	**1.0**		0.5	**1.0**	Degrees
AMPLITUDE INPUTS (U1 & U2)											
Input Resistance to COM			50			50			50		kΩ
Nominal Gain	X = Y = VR, W to Z1		1			1			1		V/V
Gain Error	U = 0.1 to 10V		0.01	**0.5**		0.01	**0.5**		0.01	**0.5**	%
	T_{min} to T_{max}		0.08			0.08			0.25		%
Voltage Offset	$U_1 = U_2 = 0V$		3.0	**10**		3.0	**10**		3.0	**10**	mV
	T_{min} to T_{max}		3.0			3.0			4.0		mV
Linearity Error	$0 \le U_1 - U_2 \le 10V$		0.1			0.1			0.1		%
AMPLITUDE PRESET (UP)											
1V Preset Enabled	UP tied to $-V_S$										
Amplitude Accuracy			0.4	**2.0**		0.4	**2.0**		0.4	**2.0**	%
	T_{min} to T_{max}		1.5			1.5			2.0		%
10V Preset Enabled	UP tied to $+V_S$										
Amplitude Accuracy			0.1	**0.55**		0.1	**0.55**		0.1	**0.55**	%
	T_{min} to T_{max}		1.0			1.0			1.5		%
INVERSE INPUTS (Z1 & Z2)											
Input Resistance to COM			50			50			50		kΩ

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SIGNAL OUTPUT (W)	$R_L \geq 2k\Omega$, $C_L \leq 100pF$										
Small Signal Bandwidth W to Z1											
	Cc = 0		1.5			1.5			1.5		MHz
	Cc = 200pF		30			30			30		kHz
Slew Rate	Cc = 0		30			30			30		V/μS
Output Voltage Swing		**±11**	±13		**±11**	±13		**±11**	±13		V
Short Circuit Current		**20**	30	**45**	**20**	30	**45**	**20**	30	**45**	mA
Output Offset	$Z_1 = Z_2 = 0$, $U_p = 10$		5	**30**		5	**30**		5	**30**	mV
	T_{min} to T_{max}		10			10					mV
	$Z_1 = Z_2 = 0$, $U_p = 1V$			**20**			**20**			**20**	mV
	T_{min} to T_{max}		7			7					mV
VOLTAGE REFERENCE (VR)											
$R_L \geq = 1.8K\Omega$											
Nominal Output			+1.8			+1.8			+1.8		V
Output Voltage Tolerance			0.05	**0.45**		0.05	**0.45**		0.05	**0.45**	%
	T_{min} to T_{max}		0.08			0.08	**0.5**		0.2	**0.7**	%
Supply Regulation	$+V_S$ = 5V to 18V		150			150			150		μV/V
Maximum Output Current			4			4			4		mA
GATE I/O (GT)											
Switching Threshold as an Input	Output Valid		+1.5			+1.5			+1.5		V
	Output Invalid		0.1			0.1			0.1		V
Voltage Output	Error, R_L = 5kΩ		+2.25			+2.25			+2.25		V
	No Error, R_L = 5kΩ		−0.25			−0.25			−0.25		V
POWER SUPPLIES											
Operating Range		**±4.75**		**±18**	**±4.75**		**±18**	**±4.75**		**±18**	V
$+V_S$ Quiescent Current	U = X = 0V, Y = Vr		7.5	**10**		7.5	**10**		7.5	**10**	mA
$-V_S$ Quiescent Current	U = X = 0V, Y = Vr		4.0	5		4.0	5		4.0	5	mA
TEMPERATURE RANGE											
Operating, Rated Performance		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C

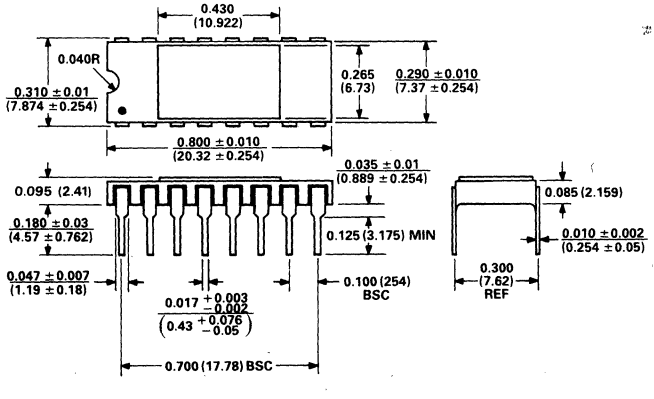
NOTES
[1]Intrinsic accuracy measured at an amplitude of 10V using external adjustments to absorb residual errors in angular scaling, angular offset, amplitude scaling and output offset.
[2]Using a time and amplitude symmetric triangular wave of +3.6V peak-to-peak and external adjustments to absorb residual errors in angular scaling and offset.
[3]Full-scale is defined as the ideal output when the angle input is at either end of the limit specified.
[4]Specifications for the X inputs apply for range U = 1V to 10V, while the Y input errors are specifically given for U = 1V.

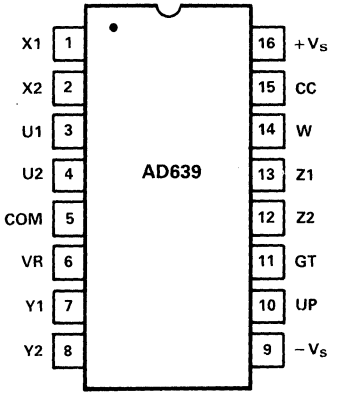
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.
Shaded area denotes preliminary technical data. Contact the factory for details.

PIN CONFIGURATION & DIMENSIONS

Dimensions shown in inches and (mm).

D16A
16-Lead Ceramic Package





ABSOLUTE MAXIMUM RATINGS

	AD639A,B	AD639S
Supply Voltage	±18V	*
Internal Power Dissipation	300mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages X_1, X_2, Y_1, Y_2[1]	±12V	*
Input Voltages U_p, U_1, U_2, Z_1, Z_2[1]	±25V	*
Operating Temperature Range	−25°C to +85°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, Soldering	60sec, +300°C	*

NOTES
*Same as AD639A,B Specifications
[1]These inputs are purely resistive and the maximum inputs are determined by resistor dissipation limits, not the supply voltages.

$\sin(\theta)$	$= \frac{\sin(\theta)}{1} = \frac{\sin(\theta-0)}{\sin(90°-0)}$		$\text{cosec}(\theta)$	$= \frac{1}{\sin(\theta)} = \frac{\sin(90°-0)}{\sin(\theta-0)}$	
$\cos(\theta)$	$= \frac{\cos(\theta)}{1} = \frac{\sin(90°-\theta)}{\sin(90°-0)}$		$\sec(\theta)$	$= \frac{1}{\cos(\theta)} = \frac{\sin(90°-0)}{\sin(90°-\theta)}$	
$\tan(\theta)$	$= \frac{\sin(\theta)}{\cos(\theta)} = \frac{\sin(\theta-0)}{\sin(90°-\theta)}$		$\text{cotan}(\theta)$	$= \frac{\cos(\theta)}{\sin(\theta)} = \frac{\sin(90°-\theta)}{\sin(\theta-0)}$	

Table I.

Principles Of Operation

Figure 1 is a functional equivalent of the AD639, intended to assist in understanding and utilizing the device: it is not a literal representation of the internal circuitry[1]. Two similar sine-shaping networks accept input voltages X_1, X_2, Y_1 and Y_2, proportional to the corresponding angles x_1, x_2, y_1 and y_2, with a scaling factor of 50°/V (20mV/°).

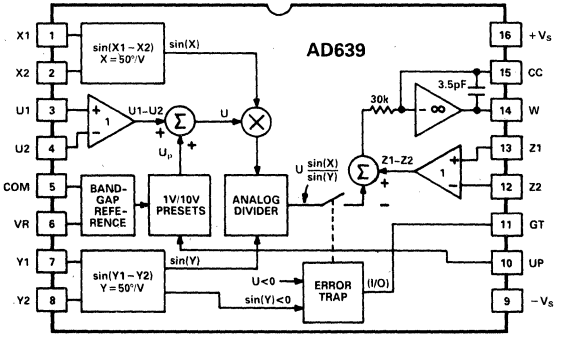


Figure 1. Equivalent Block Schematic of the AD639

The first of these networks generates an output proportional to the sine of $x = (x_1 - x_2)$ over a useful operating range in excess of −500° to +500° (see Figure 3). The accuracy of the function over the central ±180° is excellent, a consequence of the optimized network design, further enhanced by precision laser wafer trimming during manufacture. The output of the X-network is multiplied by the amplitude-control voltage, U. This may be provided by applying inputs to U1 or U2, or pre-selected to be 1V or 10V by a control input to UP, or in combination; that is, the function amplitude is $U = (U_1 - U_2) + U_p$.

The second network generates an output proportional to the sine of $y = (y_1 - y_2)$. Although the X and Y networks are similar, other design considerations result in a smaller angular range for the Y-input. The principal range is from 0° to +180°; in the adjacent ranges (+180° to +360° and 0° to −180°) the error trap is activated.

The ratio of the two sines is generated by *implicit* division, rather than by use of a separate analog divider as indicated in Figure 1, and is summed with the voltage $Z = (Z_1 - Z_2)$. The difference is applied to the high-gain output op-amp. In the *normal* modes (see below) Z1 is connected to the output W, and Z2 is grounded. Under these conditions, the function is

$$W = U \frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)}$$

Either sine function can be converted to the cosine by applying the input to X2 or Y2 and introducing a +90° offset, since

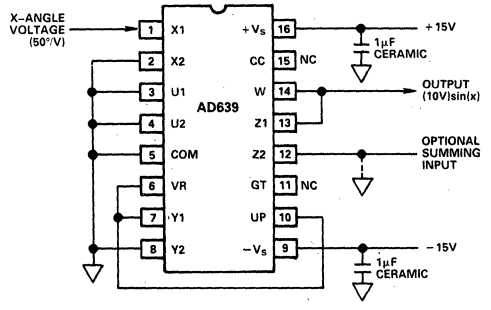


Figure 2. Connections for the Sine Mode with Amplitude Preset to 10V

[1]For details of the sine-network theory and design, see "A Monolithic Micro-system for Analog Synthesis of Trigonometric Functions and their Inverses," Barrie Gilbert, *IEEE Journal of Solid-State Circuits*, Vol. SC-17, No. 6, Dec. 1982, pp 1179-1191. Reprints available.

cos (θ) = sin(90° − θ). For example, by connecting the +1.8V reference output at pin 6 (VR) to X1 and the angle voltage, V_θ, to X2 the numerator becomes the cosine of angle θ. Alternatively, by connecting VR to either X1 or Y1 and grounding X2 or Y2, the numerator or denominator, respectively, becomes unity, since sin(90° − 0) = 1. By these means, the full set of *normal* functions shown in Table I can be generated. All functions can be sign-inverted by interchanging the X-inputs. The Z2 input can be used to sum another function to the output, W, with unity gain.

In addition to the *normal* modes providing sine, cosine, tangent, cosecant, secant and cotangent functions, the AD639 can generate the *offset* functions such as the versine, 1 − cos (θ), discussed below. The *inverse* functions such as arc-sine, arc-cosine and arc-tangent, are also supported by the AD639, by closing the feedback loop through the corresponding *normal* function. The output angle is limited to the principal range (for example, −90° to +90° for the arc-sine and arc-tangent, 0° to +180° or −180° to 0° for the arc-cosine).

TERMINOLOGY

When discussing a device having as many inputs and operating modes as the AD639, it is important to clarify the nomenclature and scaling conventions. In all cases *angles* are denoted by lower-case letters (x, y, θ) and have the dimension of angular degrees. Upper-case letters (A, V, U, W, X, Y and Z) refer to *voltages*; subscripts are used to refer to one or the other of a differential pair such as $X_1 - X_2$, or the preset value U_p. Numbered upper-case letters refer to the variable name or the package pin.

THE ANGLE INPUTS: X1, X2, Y1, Y2

The angles $x = (x_1 - x_2)$ and $y = (y_1 - y_2)$ are directly proportional to the differential voltages $X = (X_1 - X_2)$ and $Y = (Y_1 - Y_2)$ respectively, with a scaling factor of 50°/V. The X-inputs can be driven to ±12V pk, that is ±600°. The Y-input should be limited to 0 to +3.6V (0° to +180°) to satisfy certain internal requirements. The resistance at these inputs is nominally 3.6kΩ to COM.

The sine function exhibits odd-order symmetry: sin(−θ) = −sin(θ). By simply interchanging the X-inputs, the overall sign of any function can be inverted. The Y-inputs can also be interchanged to allow operation with a negative input voltage (0 to −3.6V) while maintaining the correct angular range.

It may occasionally be desirable to reduce the angular scaling factor. For example, to convert a triwave of ±10V amplitude into a continuous sinewave requires a scaling factor of 9°/V (since ±10V corresponds to ±90°). This can be achieved by using a resistor (in this case, about 16.4kΩ) in series with the X1 input; a resistor of equal value must be inserted in series with the X2 input to minimize angular offset error. Note that the on-chip thin-film resistors are not trimmed to absolute value, so a scaling adjustment is needed; however, once set, scaling will be stable.

THE AMPLITUDE-CONTROL INPUTS: U1, U2, UP

The amplitude of the function can be determined either by the application of an external voltage to the U1 and U2 inputs, or by enabling the internal preset voltage U_p by taking the control pin UP low or high, or via a combination of these modes. The net amplitude is $U = (U_1 - U_2) + U_p$. This sum must be greater than zero and less than $|-V_s|$; voltages beyond these limits activate the error trap.

In the external mode, the differential voltage $(U_1 - U_2)$ will generally be in the range 10mV to 10V. Positive inputs are applied to U1 while U2 is grounded; for negative inputs, interchange U1 and U2. The input resistance at U1 and U2 is nominally 50kΩ to analog common. A nominal bias current of −50μA is needed at the U-inputs; zero-valued inputs must therefore be connected to common to prevent offset error. The gain from the U-interface to the output is trimmed to be unity for sin(x)/sin(y) = 1. The effective gain can be lowered using a series resistor; to avoid offset an equal resistor must be used in the zero-valued input.

The UP control pin may be left unconnected (or grounded) to disable the internal amplitude preset, connected to $+V_s$ to set $U_p = 10V$, or to $-V_s$ to set $U_p = 1V$. An external resistor of 75kΩ ($\pm V_s = 5V$) to 360kΩ ($\pm V_s = 15V$) can be inserted in series with UP (which also has an input resistance of typically 50kΩ) to minimize power dissipation. Alternatively, V_r can be used to enable $U_p = 10V$. The UP input can be used to switch the output on or off under logic control, but requires a relatively long response time. The GT interface is more suitable for this purpose and it allows gating to any amplitude, U not just to the preset values of 1V or 10V.

THE REFERENCE OUTPUT: VR

The voltage V_r is laser-trimmed to +1.8V with respect to analog common. It can be used to fix the angle x or y to 90° and thus set sin(x) or sin(y) to unity. It can also provide a 90° offset to convert the numerator or denominator to a cosine function. Stable offsets less than 90° may be introduced using a voltage-dividing series-resistor (nominally 3.6kΩ for 45°). V_r can also be used as the amplitude input voltage $U_1 - U_2$, or as a convenient control input to set $U_p = 10V$. This output is short-circuit protected and can provide up to 4mA total load current.

THE ERROR-TRAP AND GATE: GT

In some applications it may be useful to know that the output is severely in error due to a dynamic combination of inputs. For example, the tangent, cotangent, secant and cosecant all exhibit regions where the function increases sharply for small angular changes, and the output may easily saturate. Consider the case where (10V) tan (θ) is being generated. W is 10V for θ = 45°, and the theoretical output of 17.3V at θ = 60° cannot be achieved using ±15V supplies. Likewise, the output is invalid whenever the angle y is outside of a valid range (principally 0 to +180°), or when $U < 0$ or $U > |-V_s|$. Under such conditions the AD639 generates a HIGH output at pin 11 and simultaneously clamps the analog output to zero (in fact, to the voltage Z_2). Grounding GT disables the error trap.

The GT pin may also be used as an *input* to gate the function output. This is achieved by raising pin 11 to a voltage above +1.5V. Response time is typically 500ns for a logic drive of 0 to +2V, and the ON/OFF ratio is greater than 83dB when used as a continuous-wave sine converter with a single-sided ±1.8V triwave drive at frequencies up to 10kHz, or 63dB at 100kHz; the feedthrough is entirely capacitive, and is equivalent to 5pF between X1 or X2 and the op-amp summing node. Feedthrough can be minimized by using a balanced drive to X1 and X2.

Operation In Normal Modes

In *normal* modes, the Z-input establishes a feedback path around the output op-amp, by connecting Z1 to the output, W, and Z2 to the ground associated with the load circuit. For the highest accuracy Z1 can be used to sense the output at the load terminals. Similarly, zero-valued angle inputs and the angle common (pin 5) should be connected to the ground associated with the source circuitry.

SINE MODE

The AD639 can generate either (1) a low-distortion continuous sinewave from a repetitive triwave input or (2) a high-accuracy sine function for use in computational applications. In most cases, the choice of preset or externally-controlled amplitude will make little difference to distortion or accuracy, and both methods are used in this section. In all of the *normal* modes, the Z2 input can be used either to sum a further signal to the output (or introduce an optional output offset trim). The denominator is set to unity by making $y = 90°$, using the $+1.8V$ output. Figure 2 shows typical connections. The 10V preset is selected, using V_r as a control input to UP, and the ideal output is (10V)sin(x). In practice, five basic types of error arise:

1. *X-angle scaling error*: The amount by which the angle generated for each volt of X-input differs from 50°. In triwave-to-sinewave (CW) applications this introduces odd-order harmonic distortion, and is indistinguishable from an incorrect triwave amplitude.
2. *X-angle offset error*: The actual angle generated when $X = (X_1 - X_2) = 0$. In CW applications this introduces even-order harmonic distortion, as a non-zero mean in the triwave would.
3. *Amplitude scaling error*: The amount by which the peak-to-peak amplitude of the sinewave differs from the ideal value, U/sin(y). This error is usually critical only in computational applications. Errors associated with the Y-network also affect the amplitude in the sine mode.
4. *Output offset error*: The amount by which the *mean value* of the sinewave differs from zero (strictly, the voltage on Z2). This error is only important in computational applications. Note that the output may also be non-zero due to angular offset on the X-input. For example, the typical specified X-angle offset of 0.1° introduces an output error of 17.45mV when U/sin(y) = 10V, more than three times the specified mean offset component of 5mV.
5. *Law-conformance error*: The residual deviation between the output function and the ideal function when all of the above errors have been removed by trimming during manufacture or further external trimming, limiting the ultimate accuracy of the function.

Figure 3 shows the function when driven well beyond the specified angular range, using a differential X-input of ±18V peak. This also shows the AD639's ability to drive ±15V into a 600Ω load, with supplies of ±18V. Using an accurate data-acquisition system the output can be compared to a computer-generated sine function. When the first four types of errors are trimmed out, the peak error over the full input range is typically less than 0.5%. Over the central −90° to +90°, the peak law-conformance error is typically only 0.02%. Figure 4 shows the law conformance for four typical samples of AD639. The differential signal interfaces simplify the inclusion of optional offset correction to any of the variables.

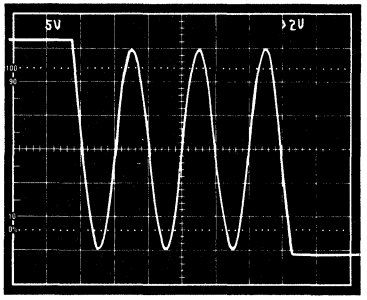


Figure 3. Output Function for Peak X-Input of ± 18V, with U = 15V, $R_L = 600\Omega$ ($\pm V_S = 18V$)

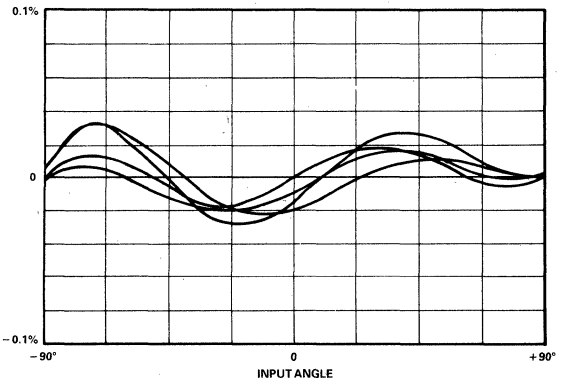


Figure 4. Residual Error Over Central 180° Using External Trimming

HARMONIC DISTORTION

The AD639 can generate continuous sinewaves of very low distortion using a linear, highly-symmetric triangle-wave of ±1.8V amplitude. Imperfections in the triwave will cause the following errors:

1. *Incorrect amplitude*: This causes odd-order distortion. Each 1% error (either too large or too small) generates 0.25% of HD3, 0.0833% of HD5 and a total harmonic distortion (THD) of 0.27% (−51.42dBs).
2. *Baseline offset*: This causes even-order distortion. Each millivolt of offset in a 1.8V triwave generates 0.037% of HD2, 0.0074% of HD4 and a THD of 0.038%, as well as a DC offset of 0.055% of the output amplitude.
3. *Time-asymmetry*: The run-up time, t_1, and run-down time, t_2, of the triwave may be unequal. This causes both odd- and even-order harmonics. Let the asymmetry in percent be $p = 100(t_1 - t_2)/(t_1 + t_2)$. The even-order terms are proportional to p; the odd-order terms increase as p^2. A 1% time-asymmetry generates 0.57% of HD2, 0.00625% of HD3, 0.043% of HD4 and 0.00167% of HD5, and a THD of −44dBs. There is no DC term.
4. *Amplitude-nonlinearity*: This can take on many forms, such as an exponential nonlinearity in the triwave, amplitude compression, and so on. Distortion can be calculated for various special cases. Fortunately, it is fairly easy to avoid these types of imperfections in the triwave generator using appropriate design methods.

When triwave errors are minimized, harmonic distortion can be as low as 0.01%. Figure 5 shows the output spectrum at 10kHz, with an output amplitude of 20V pk-pk and a load resistance of 10kΩ. An HP3325A synthesizer/function generator was used to produce the triwave. Distortion rises only slightly when using the minimum specified load of 2kΩ; in fact, the AD639 can drive loads down to 600Ω. At $\pm V_s = \pm 18V$, sine amplitudes of ±15V (10.6V rms, or 225mW of load power) can be generated, with typically 0.03% HD2 and HD3. When driving loads of less than 2kΩ, a 25pF capacitor from pin 15 to pin 9 avoids possible instability, although this is unnecessary when C_L is greater than 150pF.

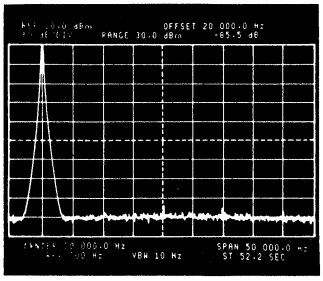


Figure 5. Spectrum of 10V Sine Output at 10kHz; HD2 = −88dBs, HD3 = −85.5dBs

COSINE MODE

The cosine function is generated by offsetting the sine by 90° using V_r. The X-input is connected to X2 and VR to X1; then

$$W = U \frac{\sin(90° - x)}{\sin(90° - 0)} = U \cos(x)$$

Connections for the cosine are shown in Figure 6: the amplitude in this case is determined externally, by way of illustration. The angular range now extends from −400° to +600°, with highest accuracy between 0° and +180°.

TANGENT AND COTANGENT MODES

The tangent function is provided by the connections shown in Figure 7. The angle voltage, corresponding to θ, is applied both to the numerator, set to the sine mode, and the denominator, set to the cosine of the same angle:

$$W = U \frac{\sin(\theta - 0)}{\sin(90° - \theta)} = U \frac{\sin(\theta)}{\cos(\theta)} = U \tan(\theta)$$

Most applications require accurate operation for angles up to nearly ±90° and accordingly U is preset to 1V (rather than 10V). Under these conditions, W = 1V when θ = 45° and 11.43V when θ = 85°. Using 15V supplies, the output op-amp will be unable to generate the tangent much beyond this point: at only 86° it would theoretically need to reach 14.3V. For an input exceeding 90° in either direction the denominator becomes negative, and the error trap is enabled. Figure 8 shows the function for inputs up to ±2.5V (±125°).

The errors associated with the sine mode, (see above) apply to the tangent mode also, but the total error in the tangent, cosecant, secant and cotangent modes (when the Y-input is also varied) are higher, since the Y network is not trimmed and the angular

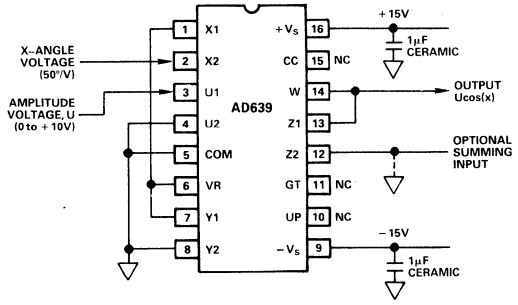


Figure 6. Connections for the Cosine Mode with External Amplitude Control

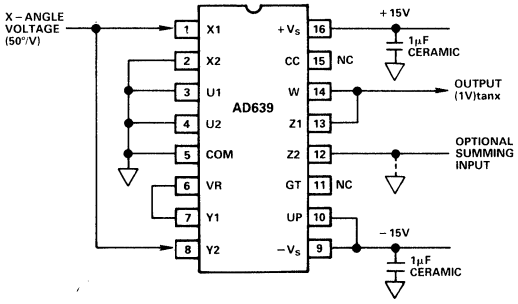


Figure 7. Connections for Tangent Mode with Amplitude Preset to 1V

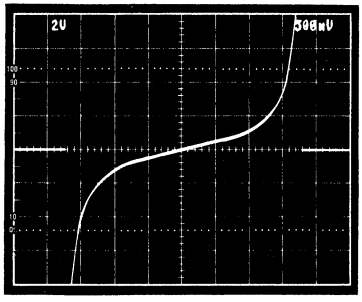


Figure 8. The Tangent Output for Angle Inputs Up to ±125° (Error Trap Activated Above 85°)

scaling and offset errors of this network are absorbed during trimming of the output in the sine mode.

The cotangent is generated by interchanging numerator and denominator. The principal range is now from 0 to +180°, and the output (1V)cot (θ) ranges from +11.43V at θ = 5°, through zero at θ = 90°, to −11.43V at θ = 175°.

SECANT AND COSECANT MODES

In secant and cosecant modes, the numerator is fixed to unity by connecting X1 to VR and X2 to analog common. For the secant, angle voltage A is connected to Y2 and Y1 is tied to VR; then

$$W = U\frac{\sin(90° - 0)}{\sin(90° - \theta)} = U\frac{1}{\cos(\theta)} = U\sec(\theta)$$

The principal range is $-90°$ to $+90°$. The most practical amplitude scaling is provided using the U-preset of 1V, when the output ranges from $+11.47$V at $\theta = -85°$ and $+85°$, to $+1$V at $\theta = 0$. The cosecant differs only slightly: the angle input is connected to Y1 and Y2 is connected to analog common, making the denominator sin (θ). The principal range is now 0 to $+180°$. When $U = 1$V the output is $+11.47$V at $\theta = +5°$ and $+175°$, and $+1$V at $\theta = 90°$.

OFFSET MODES

The versine, vers $(\theta) = 1 - \cos(\theta)$, coversine, covers $(\theta) = 1 - \sin(\theta)$, and exsecant, exsec $(\theta) = 1 - \sec(\theta)$ involve the addition of a constant term to one of the normal trigonometric functions. These can be generated with the AD639 using the Z2 input to add a voltage to the output proportional to the amplitude of the basic function. In the versine and coversine modes this is simply the same voltage as applied to U1 (U2 grounded) to set up the amplitude of the sign-inverted cosine or sine function, respectively:

$$W = U - Uf(\theta) = U(1 - f(\theta))$$

In these two modes the output starts at zero and has a peak value of twice the amplitude voltage, U.

For the exsecant a *negative* voltage is added at Z2 and this same voltage is applied to U2 with U1 grounded; this satisfies the requirement that the sign of $U_1 - U_2$ be positive. (See comments on the Amplitude Control Inputs). The angle inputs are set up for the secant; the principal range is still $-90°$ to $+90°$, but the output is now zero when the input angle is zero.

OPERATION AT LOW SUPPLY VOLTAGES

The signal ranges at the angle interfaces are essentially independent of the supply voltages. In almost all cases, the primary limitation to the function's range will arise at the output, W, which can swing to within approximately 2V of either supply. For example, the X-input may have a peak value of ± 12V ($\pm 600°$) even when using ± 5V supplies.

Inverse Function Modes

The AD639 generates the inverse trigonometric functions by closing the feedback loop around the output op-amp through the *angle* inputs, rather than through the Z-interface, resulting in a nonlinear feedback system. To understand this, note first that the *general* transfer function (with UP disabled) is

$$W = A_{OL}\left[(U_1 - U_2)\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} - (Z_1 - Z_2)\right]$$

where A_{OL} is the open-loop gain of the output op-amp (typically 85dB). Provided that the overall feedback remains negative, the loop can be closed in many ways, so as to force the quantity inside the brackets to a null, when

$$\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} = \frac{(Z_1 - Z_2)}{(U_1 - U_2)}$$

whatever combinations of variables are used to set up the feedback path. In particular, when the *angle* inputs are used the system will have one of the *normal* functions in the feedback path. The input to this system is now the *ratio* (Z/U), and the output is a voltage corresponding to the angle generated by the *inverse* of the function in the feedback path.

Since all of the normal functions are periodic, and the maximum value of the op-amp output can be equivalent to angles as large as $\pm 650°$, the closed-loop system could arrive at false "solutions" to the above equation, that is, at angles outside of the principal range. Also, the feedback can become positive in the wrong angular range, causing latch-up. Hence, it is essential to limit the magnitude of the feedback voltage. Ideally, this is done using precise active clamps, but the saturated value of the output at given supply voltages, in combination with a simple resistive divider to the angle inputs, is usually sufficient to limit operation to the principal range. The voltage at the angle inputs will be accurate, but the op-amp output will in general have inaccurate scaling and may show large offsets, due to the bias currents at the angle inputs. The error-trap should be disabled in the inverse modes by grounding GT.

ARCTANGENT MODE

The arctangent is the most useful of the inverse modes. With the connections shown in Figure 9 the loop solves the equation

$$\frac{\sin(0 - \theta)}{\sin(90° - \theta)} = -\tan(\theta) = \frac{(Z_1 - Z_2)}{(U_1 - U_2)}$$

where θ is the angle corresponding to voltage A, scaled by 50°/V. It follows that

$$\theta = \tan^{-1}\frac{(Z_2 - Z_1)}{(U_1 - U_2)}$$

The reversal of Z_1 and Z_2 in the numerator is due to the negative sign in the tangent function. The numerator may be either positive or negative, and the connections can be interchanged to alter the overall sign of the function. The denominator must be positive, but U1 and U2 may be interchanged to accept a negative input voltage. The ability of the AD639 to form the ratio of two

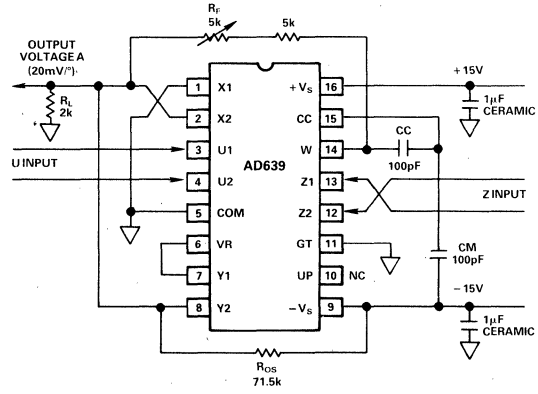


Figure 9. Connections for the General Arctangent Mode

variables prior to the arctangent operation is very useful in many applications, for example, in real-time Cartesian-to-polar conversion (see Applications section). The denominator can also be preset to 1V or 10V using the UP input; when U = 1V, the angle a is simply the arctangent of the voltage value of $Z_2 - Z_1$. Figure 10 shows an X-Y plot of the output for Z = −10V to +10V (horizontal axis of photograph) with four values of U (0.3V, 1V, 3V, 10V).

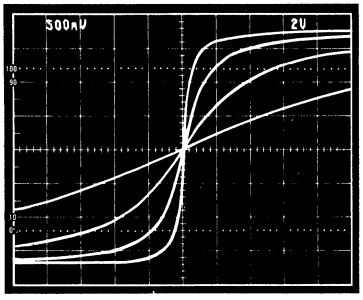


Figure 10. The Arctangent Output for Z = ±10V and U = 0.3V, 1V, 3V and 10V

Range-Limiting and Loading

Resistor R_f in Figure 9 forms a divider with the parallel sum of the input resistance at X2 and Y2 and the load resistance, shown here as 2kΩ, which prevents the output angle voltage A from exceeding ±1.7V (θ = ±85°), using ±15V supplies. This voltage is not *directly* affected by the load resistance (that is, the output behaves as a low-impedance node) but the angular range limits are. Consequently, the nominal value of R_f should be calculated for specific values of load resistance, angular range and supply voltages, and a trim range of about ±10% included to set up the angle limits correctly. R_{cc} is needed to compensate the input bias currents and thus equalize the clipping limits; it does not cause an offset in θ. The direct output at pin 14 is also the arctangent but with imprecise scaling. Although this can be trimmed by R_f there will also be a supply-dependent offset due to R_{os}. For these reasons, the direct output should not be used in this mode.

HF Compensation

The output op-amp is internally compensated to be stable in all the normal modes when feedback is via the unity-gain difference amplifier associated with the Z-interface. The dominant pole is determined by the 30kΩ resistor and on-chip 3.5pF capacitor (see Figure 1) for a closed-loop bandwidth of 1.5MHz. In the arc-tangent mode, however, the gain of the feedback path is much greater than unity for practical angle values and is theoretically unbounded. For example, if the forward path is set up to generate (1V)tan(θ), the incremental gain near θ = 0 is slightly less than unity (since a 20mV change in voltage A causes a change of (1V)tan(1°) or 17.5mV in output W) but at θ = 85° the gain is 115. While the resistive divider used to limit the angle voltage A will lower the loop gain, it can still exceed unity. The capacitors C_c and C_m in Figure 9 provide the HF compensation required for operation up to ±85°, with all values of U.

ARCSINE AND ARCCOSINE MODES

The basic principles for the arcsine and arccosine are similar to those described for the arctangent. As before, the argument of the function is the ratio (−Z/U), where U may be preset to 1V or 10V, the loop gain must be negative over the principal angular range of the output, and the feedback voltage must be limited to ensure that this range is not exceeded. The loop stability is easier to ensure, since the peak gain is bounded. With U = 10V the maximum incremental gain of the forward path (at 0° for the sine and +90° for the cosine) is 8.75 and the peak loop gain is much less than this because of the attenuation used to limit the angular range. Thus relatively little additional HF compensation is required.

Connections for the arcsine are similar to the arctangent (Figure 9) except that Y2 is grounded, and C_c and C_m can be reduced or even omitted. R_f is adjusted for a peak angular range of ±90° at the (attenuated) output; if too high, the function will still be correct, but the maximum angle will be less than 90°; if too low, the function will exhibit hysteresis near the peak output. Adjustments will be needed for other values of load resistance and supply voltages. Note that the general limitation on the amplitude input ($U <= |-V_s|$) must be observed. Figure 11 shows an X-Y plot of the arcsine output for Z = −10V to +10V (horizontal axis of photograph) with three values of U (2V, 5V and 10V). The arcsine can be inverted by reversing the Z-interface.

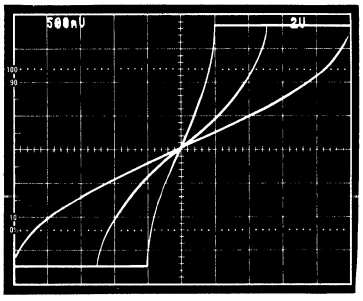


Figure 11. The Arcsine Output for Z = ±10V and U = 2V, 5V and 10V

For the arccosine, use the arcsine connections with X1 tied to V_r and insert a small-signal diode in series with R_f, having its cathode on the angle-interface side. This allows the output to move only in a positive direction. Z1 now becomes the positive numerator input, and the principal range is from 0° (when Z/U = −1) to +180°. The function is similar in appearance to the arcsine, except for the +90° output pedestal and the reversal of phase along the horizontal axis. Note that

$$\cos^{-1}(Z/U) = 90° - \sin^{-1}(Z/U) = 90° + \sin^{-1}(-Z/U).$$

To generate the negative arccosine, reverse the X- and Z-interfaces and the polarity of the diode. The output now runs from −180° for an input of Z = (Z1 − Z2) = −10V (with U = 10V) to 0° at Z = +10V.

It is strongly recommended that X-Y oscilloscope methods are used to investigate functional behavior during the development of any of these modes of operation: time-domain displays can easily become confusing.

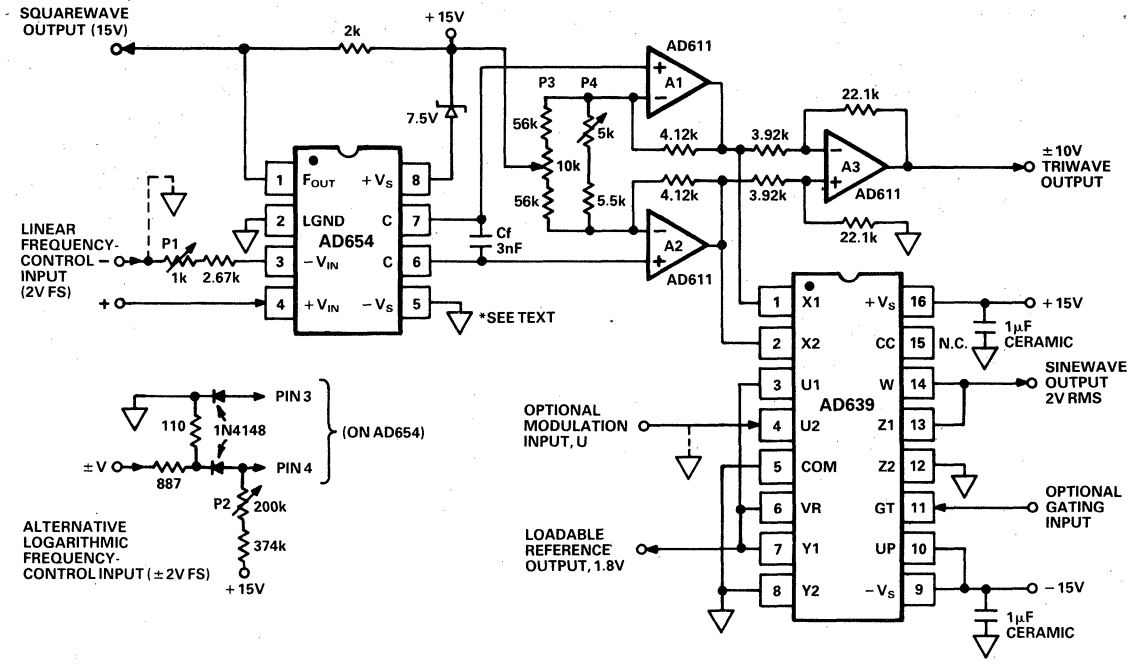


Figure 12. General-Purpose Function Generator

Applications

WIDE-RANGE WAVEFORM GENERATOR

Figure 12 shows an inexpensive signal generator, providing voltage control of frequency from 20Hz to 20kHz and a pre-set sine amplitude of 2.8V (within 0.1dB of 2V rms). This output may be further modulated by an input of up to ±2.8V to U2, or gated off by an input of +1.5V or more to GT; Figure 13 shows the gated response. If required, a further input can be summed into Z2. The sine output can be set to 10V amplitude by connecting UP to VR and grounding U1.

An AD654 is used to generate the triwave which appears across the timing capacitor C_f, and is buffered, amplified and level-shifted by A1 and A2. Using a spectrum analyzer, P3 and P4 are adjusted to minimize even- and odd-harmonic distortion, respectively. The triwave linearity is not good enough to realize the inherent capabilities of the AD639, but total harmonic distortion is in the −50dB to −60dB range. A3 provides further gain for a ±10V triwave output. The square-wave output is taken directly from the AD654 and is unbuffered. It swings between ground and +15V; if pins 2 and 5 of the AD654 are connected to −15V, this output is 30V pk-pk.

The frequency scaling with the linear input (shown) is 10kHz/V, calibrated using P1. The frequency can be controlled manually, using a potentiometer and the V_r output of the AD639. P1 has sufficient trim range to provide a full-scale frequency of 20kHz with the 1.8V peak input. The alternative input scheme provides a "log-sweep" response with an approximate scaling of 10^V kHZ (when V is in volts). The range is now from about 10Hz to 100kHz; the frequency should be set to 1kHz with V = 0, using P2. The frequency is now sensitive to variations in both temperature and the +15V supply, but stability will be adequate for many applications.

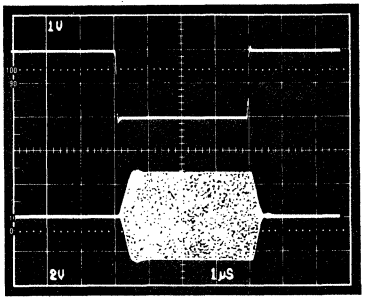


Figure 13. Gated Output. Top Trace: 0 to +2V Gate Input. Bottom Trace: 2V rms Gated Sine Output

Frequency Multiplication

Because of the exceptionally wide angular range of the numerator function of the AD639, it is possible to generate sinewave outputs with 2, 3, 4 or 5 times the triwave frequency using the cosine mode for even multiples or the sine mode for odd multiples.[2] For example, to multiply the output frequency by 3, use the sine function with the X-input driven to ±5.4V (±270°). Distortion remains low; all harmonics are typically under −50dBs, even for the frequency-quintupling mode.

[2]For full details see "A Remarkable Monolithic Microsystem Generates Trigonometric Functions," Barrie Gilbert, *Industrial Electronics Equipment Design*, September 1984, pp. 19-24. Reprints available.

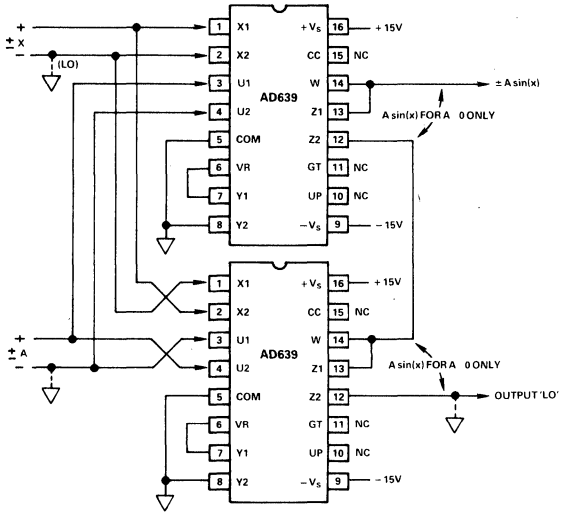


Figure 14. Four-Quadrant Sine Multiplier; for Cosine, Interchange X1 and X2 and Connect Angle 'Lo' Input to VR

FOUR-QUADRANT SINE/COSINE MULTIPLICATION

In synchro applications it is often necessary to multiply an AC sinusoidal 'carrier' by a further sine 'modulation' function. This can be achieved in two ways; the first is suitable only when there is a large ratio between the carrier frequency and the modulation frequency. Using a single AD639, the carrier input Asin(ωt) is applied to U2, and a DC bias voltage established on U1 (which can be provided by a series resistor connected to $+V_s$). The modulation input, x, is applied to angle inputs connected for $-\sin(x)$. The output is then $W = -\sin(x)(U_1 - A\sin(\omega t))$. Using AC-coupling to the load, the voltage Asin(x)sin(ωt) results. Since the peak value of W is $(U_1 + A)$, a maximum of about 6V amplitude can be achieved before output saturation. A further limitation of this approach is that the AC-coupling may allow excessive transmission of the sine modulation function. However, with typical values of 400Hz for the carrier and 10Hz for the upper modulation frequency, this simple approach is practical. Cosine modulation is similarly achieved.

An alternative method is DC-coupled and thus imposes no frequency-ratio limitations; it also allows an input/output amplitude of up to 12V. Two AD639s are used (Figure 14), the second having both the X- and U-interfaces phase-inverted relative to the first, and the two outputs are summed. The figure shows a general bipolar input, A, applied to the U-inputs. The first device generates Asin(x) when A is positive and zero when A is negative. The second device generates $-A\sin(x)$ (actually $A\sin(-x)$) when A is negative and zero when A is positive. The instantaneous sum of the two half-sines is Asin(x). The switching speed of the U-interface is adequate to handle a sinusoidal input $A = (10V)\sin(\omega t)$ at frequencies up to at least 1kHz, without significant crossover distortion. In synchro applications errors as small as 5 arc-minutes can be achieved.

Polar-to-Cartesian Conversion

Using a pair of AD639s connected as shown in Figure 14, and a second pair connected similarly for the cosine function, a vector of magnitude A and angle x can be resolved into its orthogonal components Asin(x) and Acos(x), with unrestricted operation in all quadrants and very high accuracy.

Cartesian-to-Polar Conversion

A point Z,U in a plane can be converted to a magnitude component, A, and an angle component, θ. A suitable vector summation circuit can be found in the AD637 data sheet. The AD639 in the arctangent mode can provide the angle output $\theta = \tan^{-1}(Z/U)$. If U is bipolar, an absolute-value circuit using an AD630 should be added.

Sine/Cosine (Quadrature) Oscillators

Quadrature oscillators generate a pair of sinusoudal outputs displaced by 90°, and invariably are based on a "state-variable" loop consisting of two integrators and a sign-inverter. Practical difficulties in this approach are (1) considerable additional circuitry is required to control the amplitude of the oscillation; (2) a trade-off arises between the settling-time of this control circuitry and the distortion level, particularly troublesome at low frequencies; (3) the amplitude balance of the two outputs is dependent on the matching of two time-constants; (4) two tracking analog multipliers or multiplying DACs are needed if the frequency is to be programmable.

These problems are avoided using a function-shaping technique based on a triwave oscillator, which requires only one time-constant, and whose frequency can thus be more easily controlled. The need for an amplitude control system is eliminated using the scheme shown in Figure 15. The two outputs have accurate amplitudes of 10V (without the need for an external reference source) or can be individually controlled by external voltages, without any effect on frequency. Variable-amplitude sine and cosine outputs can be added (using the Z-input discussed earlier) to provide continuously-variable phase-control of the output.

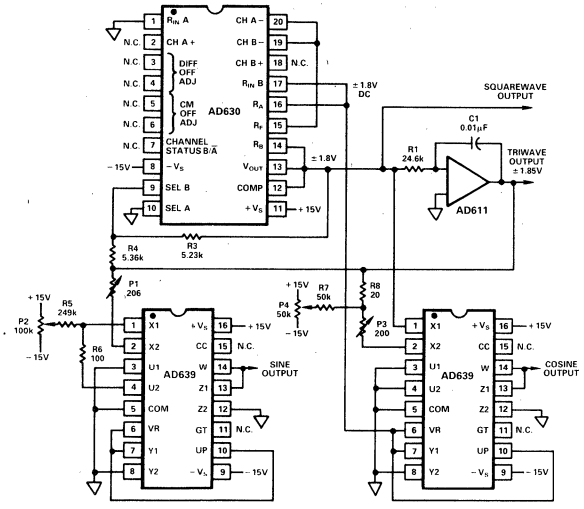


Figure 15. Quadrature Oscillator

The triwave oscillator comprises an AD630, which alternates the sign of the 1.8V reference from one of the AD639s to generate a square-wave output of ±1.8V amplitude, and an integrator formed by R1, C1 and the op-amp, which generates the triwave. The amplitude of the triwave is determined by the ratio of R3 and R4, and is nominally ±1.845V, 2.5% higher than needed at the inputs of the AD639s, providing the adjustment range needed to minimize distortion. In many applications, all adjustments can be eliminated; to do this, make R3 = R4 = 5kΩ, omit P2, P4, R5 and R7 and replace P1, P3, R6, and R8 with short circuits. The frequency is nominally $1/4C_1R_1$, and is 1kHz with the component values shown. A variety of methods may be used to provide external control of frequency, including the use of another AD630 in series with R1, or the use of a multiplying DAC.

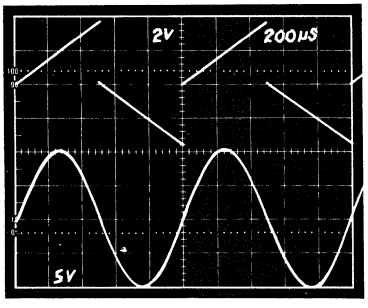


Figure 16. Top Waveform: Difference Voltage Between Triwave and Squarewave. Bottom Waveform: Resulting Output

The sine output is generated using the triwave directly. P1 and P2 should be adjusted using a spectrum analyzer for minimum odd-order and even-order harmonics, respectively. The cosine output is generated by using the *difference* between the triwave and the square-wave, shown in the upper waveform in Figure 16. This composite voltage first generates a sine-function over the range 0 to +180°, then over the range 0 to −180°, to produce the function shown in the lower waveform, which can be seen to be 90° out of phase with the triwave. The complete set of waveforms available from this generator are shown in Figure 17.

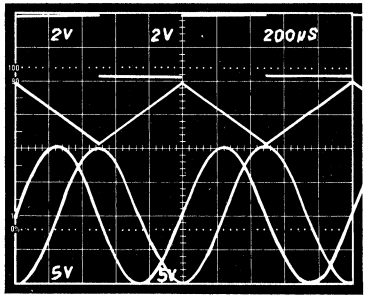


Figure 17. Timing Relationships Between All Outputs of the Quadrature Oscillator

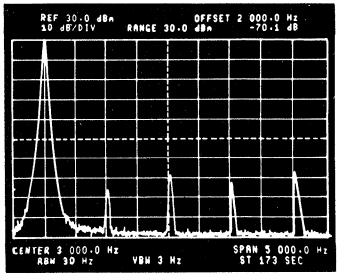


Figure 18. Spectrum of Cosine Output at 1kHz

P3 and P4 are adjusted for minimum odd-order and even-order cosine harmonics, respectively; Figure 18 shows the cosine spectrum for a well-adjusted circuit.

Due to the finite transition time back to the baseline in the drive voltage to the cosine generator, a brief spike occurs at the zero-crossing of this output. The frequency components will be beyond the bandwidth of the output amplifier in the AD639, and the energy contained in these spikes will not generally be troublesome. They may be further reduced, if necessary, by adding a capacitor between pins 14 and 15, to roll off the AD639 output response.

ANALOG DEVICES

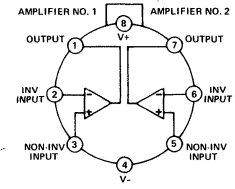
Low Power Precision Dual BIFET Op Amp

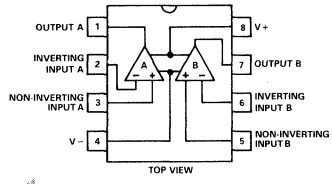
AD648

FEATURES

- **Improved Replacement for LF442**
- **Low Quiescent Current: 400μA max**
- **Low Input Bias Current: 10pA max, Warmed-Up (AD648C)**
- **Low Offset Voltage: 250μV max (AD648C)**
- **Low Drift: 2μV/°C max (AD648C)**
- **Low Noise: 2μV p-p, 0.1 to 10Hz**
- **AC Specs: 1.8V/μs Slew Rate, 1MHz Unity Gain Bandwidth**
- **Available in Plastic, Hermetic CERDIP and Hermetic Header Packages**
- **MIL-STD-883B and Plus Parts Available**

AD648 PIN CONFIGURATION





3

PRODUCT DESCRIPTION

The AD648 is a low power, dual precision monolithic operational amplifier. It is fabricated with ion-implanted FET and laser wafer trimming technologies and offers both low bias current (25pA max, warmed-up) and low quiescent current (400μA max).

The economical J and A grades have a maximum guaranteed offset voltage of less than 2mV and an offset voltage drift of less than 20μV/°C. This level of dc precision is achieved utilizing Analog's exclusive laser wafer drift trimming process. The combination of low quiescent current and low offset drift minimizes changes in offset voltage due to self-heating effects. Four additional grades are offered, which provide increased performance over the commercial, industrial and military temperature ranges.

The AD648 is recommended for any op amp application requiring low power and excellent dc and ac performance. Battery-powered, precision instrument front ends and CMOS DAC buffers will benefit from this device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "B" and "C" versions) and high open-loop gain ensures better than 12-bit linearity in high impedance buffer applications.

Devices are pinned out in a standard op amp configuration and are available in six performance grades. The AD648J and AD648K are rated over the commercial temperature range of 0 to +70°C. The AD648A, AD648B and AD648C are rated over the industrial temperature range of −25°C to +85°C. The AD648S is rated over the military temperature range of −55°C to +125°C, and is available processed to MIL-STD-883B, Rev. C. Devices are available in an 8-pin CERDIP, a plastic Mini-DIP or a TO-99 metal can.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. A combination of low supply current, excellent dc and ac performance and low drift makes the AD648 the ideal op amp for high performance, low power applications.
2. Pin compatible with industry standard op amps such as the LF442 and the AD642, the AD648 enables designers to improve performance while achieving a reduction in power dissipation of up to 85%.
3. Guaranteed low offset voltage (2mV max) and drift (20μV/°C max) are achieved utilizing Analog Devices' Laser Wafer Drift Trimming (LWDT) Technology, eliminating the need for external trimming.
4. Analog Devices specifies each device in the warmed-up condition, thus insuring that the device will meet its published specifications in actual use.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD648J/A/S Min	AD648J/A/S Typ	AD648J/A/S Max	AD648K/B Min	AD648K/B Typ	AD648K/B Max	AD648C Min	AD648C Typ	AD648C Max	Units
INPUT OFFSET VOLTAGE[1]										
Initial Offset			**2**			**0.5**			**0.25**	mV
Input Offset Voltage vs. Temp			**20**			**5**			**2.0**	µV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**	dB
INPUT BIAS CURRENT										
Either Input[2], CMV = 0		10	25		5	10		5	10	pA
Offset Current		5			5			2		pA
INPUT IMPEDANCE										
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		Ω|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		Ω|pF
INPUT VOLTAGE RANGE										
Differential[3]		±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**80**			**80**			**80**			dB
INPUT VOLTAGE NOISE										
Voltage 0.1Hz to 10Hz		2			2			2		µV p-p
f = 1kHz		35			35			35		$nV/\sqrt{Hz}$
FREQUENCY RESPONSE										
Unity Gain Small Signal		1.0			1.0			1.0		MHz
Full Power Response		30			30			30		kHz
Slew Rate, Unity Gain		1.8			1.8			1.8		V/µs
Settling Time to ±0.01%		8			8			8		µs
OPEN LOOP GAIN[4]										
V_O = ±10V, R_L = 10kΩ	**100**			**100**			**100**			dB
T_{min} to T_{max}, R_L = 10kΩ	100			100			100			dB
V_O = ±10V, R_L = 5kΩ	86			86			86			dB
MATCHING CHARACTERISTICS[5]										
Input Offset Voltage			2.0			0.5			0.25	mV
Input Offset Voltage, T_{min} to T_{max}			20			5			2	µV/°C
Input Bias Current			25			10			10	pA
Cross Talk		−124			−124			−124		dB
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±11**	±13		**±11**	±13		**±11**	±13		V
Short Circuit Current		25			25			25		mA
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±4.5		±18	±4.5		±18	±4.5		±18	V
Quiescent Current		300	**400**		300	**400**		300	**400**	µA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD648J			AD648K					
Industrial (−25°C to +85°C)		AD648A			AD648B			AD648C		
Military (−55°C to +125°C)		AD648S								
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS	J Grade: Plastic (N8A) A Grade: CERDIP (Q), TO-99 Style (HO8B) S Grade: CERDIP (Q), TO-99 Style (HO8B)			K Grade: Plastic (N8A) B Grade: CERDIP (Q), TO-99 Style (HO8B)			C Grade: Cerdip (Q), TO-99 Style (HO8B)			

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[4]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[5]Matching is defined as the difference between parameters of the two amplifiers.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

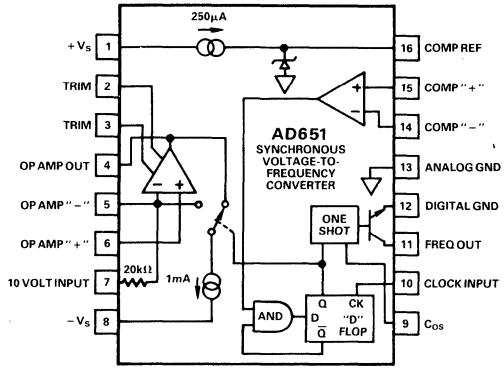
Monolithic Synchronous Voltage-to-Frequency Converter

AD651

FEATURES

- **Full-Scale Frequency (Up to 2MHz) Set by External System Clock**
- **No Critical External Components Required**
- **Extremely Low Linearity Error (0.005% max at 100kHz FS, 0.02% max at 2MHz FS)**
- **Low Drift (25ppm/°C max)**
- **Dual or Single Supply Operation**
- **Voltage or Current Input**
- **Low Cost**

AD651 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD651 Synchronous Voltage-to-Frequency Converter (SVFC) uses a variation of the popular charge-balancing technique to perform the conversion function. The AD651 uses an external clock to define the full-scale output frequency, rather than relying on the stability of an external one-shot capacitor. The result is a more stable, more linear transfer function, with significant application benefits in both single- and multi-channel systems.

The AD651 is a powerful building block for precision analog-to-digital conversion, offering typical nonlinearity of 0.002% (0.005% maximum) at a 100kHz output frequency. The inherent monotonicity of the transfer function and wide range of clock frequencies allows the conversion time and resolution to be optimized for specific applications.

Gain drift is minimized using a precision low-drift buried zener reference and low-TC on-chip thin-film scaling resistors. Furthermore, the initial gain error is reduced to less than 0.5% by the use of laser-wafer-trimming.

The analog and digital sections of the AD651 have been designed to allow operation from a single-ended power source, simplifying its use with isolated power supplies.

The AD651 is available in three performance grades. The 16-pin cerdip-packaged AQ and BQ grades are specified for operation over the −25°C to +85°C industrial temperature range, and the AD651SQ is available for operation over the full −55°C to +125°C extended temperature range.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. The use of an external clock to set the full-scale frequency allows the AD651 to achieve linearity and stability far superior to any other monolithic VFC. By using the same clock to drive the AD651 and (through a suitable divider) also set the counting period, conversion accuracy is maintained independent of variations in clock frequency.
2. The AD651 Synchronous VFC requires only a single external component (a noncritical integrator capacitor) for operation.
3. The clock input of the AD651 is TTL and CMOS compatible and can also be driven by sources referred to the negative power supply. The flexible open-collector output stage provides sufficient current sinking capability for TTL and CMOS logic, as well as optical couplers and pulse transformers. A capacitor-programmable one-shot is provided for selection of optimum output pulse width for power reduction.
4. The AD651 can also be configured for use as a synchronous F/V converter for isolated analog signal transmission.

SPECIFICATIONS (typical @ T_A = +25°C, V_S = ±15V, unless otherwise noted)

	AD651AQ/SQ			AD651BQ			
	Min	Typ	Max	Min	Typ	Max	Units
VOLTAGE-TO-FREQUENCY MODE							
Gain Error							
f_{OUT} = 100kHz		±0.5	±1		±0.25	±0.5	%
f_{OUT} = 500kHz		±0.5	**±1**		±0.25	**±0.5**	%
f_{OUT} = 2MHz		±0.5	**±1.5**		±0.25	**±0.75**	%
Gain Drift[1]							
f_{OUT} = 100kHz		±25	±50		±15	±25	ppm/°C
f_{OUT} = 500kHz		±25	**±50**		±15	**±25**	ppm/°C
f_{OUT} = 2MHz		±25	**±75**		±15	**±50**	ppm/°C
Power Supply Rejection		0.001	**0.01**		0.001	**0.01**	%/V
Linearity Error							
f_{OUT} = 100kHz		±0.002	±0.02		±0.002	±0.005	%
f_{OUT} = 500kHz		±0.002	**±0.02**		±0.002	**±0.005**	%
f_{OUT} = 1MHz		±0.01	±0.02		±0.002	±0.005	%
f_{OUT} = 2MHz		±0.02	**±0.05**		±0.01	**±0.02**	%
Offset[2]		±1	**±4.5**		±1	**±2.5**	mV
(Transfer Function, RTI)							
Offset Drift		±10	**±50**		±10	**±30**	µV/°C
FREQUENCY-TO-VOLTAGE MODE							
Gain Error							
f_{IN} = 100kHz FS		±0.5	±1		±0.25	±0.5	%
Linearity Error							
f_{IN} = 100kHz FS		±0.002	±0.02		±0.002	±0.01	%
Input Resistor	19.8	20.0	20.2	19.8	20.0	20.2	kΩ
Temperature Coefficient		±20	**±50**		±20	**±50**	ppm/°C
INTEGRATOR OP AMP							
Input Bias Current							
Inverting Input (Pin 5)		±8	**±20**		±8	**±20**	nA
Noninverting Input (Pin 6)		40	**100**		40	**100**	nA
Input Offset Current		40	**120**		40	**120**	nA
Input Offset Voltage		±1	**±4**		±1	**±2**	mV
Open Loop Gain		86			86		dB
Common Mode Input Range	**−10**		**10**	**−10**		**10**	V
Output Voltage Range	**−1**		**(+V_S−4)**	**−1**		**(+V_S−4)**	V
(Referred to Pin 6, R_1 > = 5k)							
COMPARATOR							
Input Bias Current		0.5	5		0.5	5	µA
Common Mode Voltage	−V_S+4		+V_S−4	−V_S+4		+V_S−4	V
CLOCK INPUT							
Maximum Frequency	**4**	5		**4**	5		MHz
Threshold Voltage		1.4			1.4		V
T_{min}-T_{max}	**0.8**		**2.0**	**0.8**		**2.0**	V
(Referred to Pin 12)							
Input Current							
(−V_S<V_{CLK}< +V_S)		5	**20**		5	**20**	µA
Voltage Range	−V_S		+V_S	−V_S		+V_S	V
OUTPUT STAGE							
V_{OL} (I_{OUT} = 10mA)			**0.4**			**0.4**	V
I_{OL}							
V_{OL}<0.8V			**15**			**15**	mA
V_{OL}<0.4V, T_{min}-T_{max}			**8**			**8**	mA
I_{OH} (Off Leakage)		0.01	**10**		0.01	**10**	µA
Delay Time, Positive Clock Edge to Output Pulse	**100**	150	**200**	**100**	150	**200**	ns
Fall Time (Load = 500pF and I_{SINK} = 5mA)		100			100		ns
Output Capacitance		5			5		pF
OUTPUT ONE-SHOT							
Pulse Width							
C_{OS} = 300pF	**1**	1.5	2	**1**	1.5	2	µs
C_{OS} = 1000pF	4	5	6	4	5	6	µs

	AD651AQ/SQ			AD651BQ			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
REFERENCE OUTPUT							
Voltage	5.4	6.8	8.2	5.4	6.8	8.2	V
Drift		50	100		25	50	ppm/°C
POWER SUPPLY							
Rated Voltage		±15			±15		V
Operating Range							
Dual Supplies	±6	±15	±18	±6	±15	±18	V
Single Supply ($-V_S = 0$)	+12		+36	+12		+36	V
Quiescent Current		±9	±15		±9	±15	mA
Digital Common	$-V_S$		$+V_S-4$	$-V_S$		$+V_S-4$	V
Analog Common	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
TEMPERATURE RANGE							
Specified Performance							
"Q" Package	−25		+85	−25		+85	°C
"SQ" Grade	−55		+125				°C

NOTES
[1]Gain Drift is the average drift from T_{min} to T_{max}, and is measured at +25°C, T_{min} and T_{max}.
[2]Offset is guaranteed adjustable to zero using a 20K potentiometer on pins 2 and 3 with the wiper connected to $+V_S$ through a 250k resistor.

Specifications in **boldface** are 100% tested at final test and are used to measure outgoing quality levels.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage (Figure 6) 36V
Maximum Output Current (Open Collector Output) . . 50mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Storage Temperature Range: Cerdip . . . . −65°C to +150°C

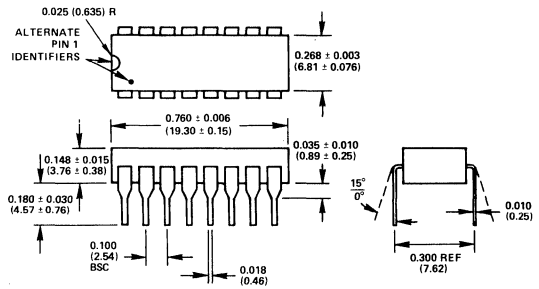
ORDERING GUIDE

Part Number	Gain Drift ppm/°C 100kHz	1MHz Linearity %	Specified Temperature Range °C	Package
AD651AQ	50 max	0.02 max	−25 to +85	Cerdip
AD651BQ	25 max	0.005 max	−25 to +85	Cerdip
AD651SQ	50 max	0.02 max	−55 to +125	Cerdip

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

"Q" PACKAGE
16-Pin CERDIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH

DEFINITIONS OF SPECIFICATIONS

GAIN ERROR – The gain of a voltage-to-frequency converter is that scale factor setting that provides the nominal conversion relationship, e.g. 1MHz full scale. The "gain error" is the difference in slope between the actual and ideal transfer functions for the V-F converter.

LINEARITY ERROR – The "linearity error" of a V-F is the deviation of the actual transfer function from a straight line passing through the endpoints of the transfer function.

THEORY OF OPERATION

A synchronous VFC is similar to other voltage-to-frequency converters in that an integrator is used to perform a charge-balance of the input signal with an internal reference current. However, rather than using a one-shot as the primary timing element which requires a high quality and low drift capacitor, a synchronous voltage-to-frequency converter (SVFC) uses an external clock; this allows the designer to determine the system stability and drift based upon the external clock selected. A crystal oscillator may also be used if desired.

The SVFC architecture provides other system advantages besides low drift. If the output frequency is measured by counting pulses gated to a signal which is derived from the clock, the clock stability is unimportant and the device simply performs as a voltage controlled frequency divider, producing a high resolution A/D. If a large number of inputs must be monitored simultaneously in a system, the controlled timing relationship between the frequency output pulses and the user supplied clock greatly simplifies this signal acquisition. Also, if the clock signal is provided by a VFC, then the output frequency of the SVFC will be proportional to the product of the two input voltages. Hence, multiplication and A-to-D conversion on two signals are performed simultaneously.

The pinout of the AD651 SVFC is shown in Figure 1. A block diagram of the device configured as a SVFC, along with various system waveforms, is shown in Figure 2.

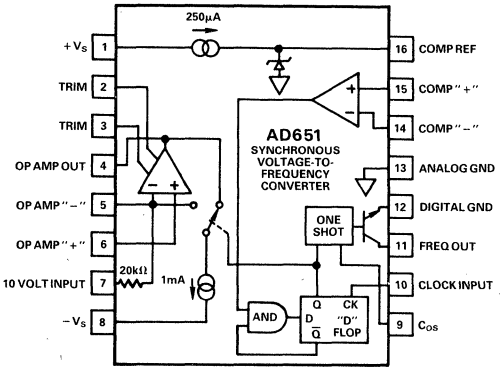


Figure 1. AD651 Pin Configuration

Figure 2 shows the typical up-and-down ramp integrator output of a charge-balance VFC. After the integrator output has crossed the comparator threshold and the output of the AND gate has gone high, nothing happens until a negative edge of the clock comes along to transfer the information to the output of the D-FLOP. At this point, the clock level is low, so the latch does not change state. When the clock returns high, the latch output goes high and drives the switch to reset the integrator. At the same time the latch drives the AND gate to a low output state. On the very next negative edge of the clock the low output state of the AND gate is transferred to the output of the D-FLOP and then when the clock returns high, the latch output goes low and drives the switch back into the Integrate Mode. At the same time the latch drives the AND gate to a mode where it will truthfully relay the information presented to it by the comparator.

Since the reset pulses applied to the integrator are exactly one clock period long, the only place where drift can occur is in a variation of the symmetry of the switching speed with temperature. Since each reset pulse is identical to every other, the AD651 SVFC produces a very linear voltage to frequency transfer relation. Also, since all of the reset pulses are gated by the clock, there are no problems with dielectric absorption causing the duration of a reset pulse to be influenced by the length of time since the last reset.

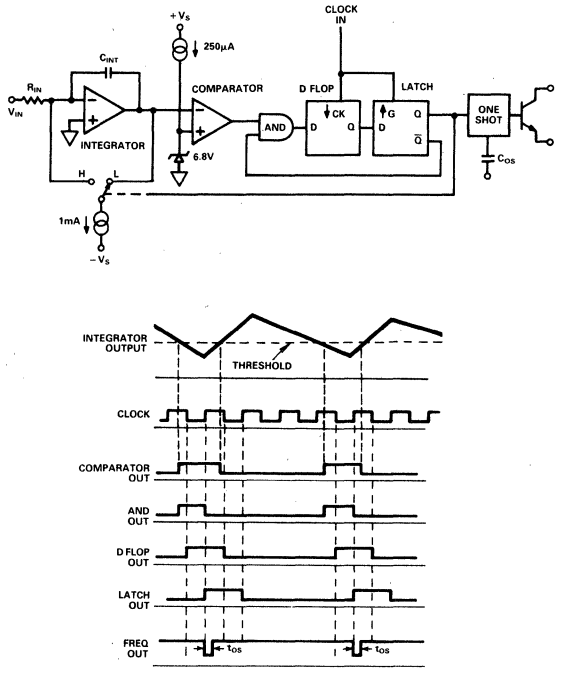


Figure 2. AD651 Block Diagram and System Waveforms

Referring to Figure 2, it can be seen that the period between output pulses is constrained to be an exact multiple of the clock period. Consider an input current of exactly one quarter of the value of the reference current. In order to achieve a charge balance, the output frequency will equal the clock frequency divided by four; one clock period for reset and three clock periods of integrate. This is shown in Figure 3. If the input current is increased by a very small amount, the output frequency should also increase by a very small amount. Initially, however, no output change is observed for a very small increase in the input current. The output frequency continues to run at one quarter of the clock, delivering an average of 250μA to the

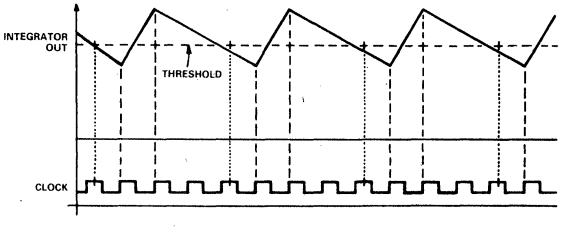


Figure 3. Integrator Output for $I_{IN} = 250\mu A$

summing junction. Since the input current is slightly larger than this, charge accumulates in the integrator and the sawtooth signal starts to drift downward. As the integrator sawtooth drifts down, the comparator threshold is crossed earlier and earlier in each successive cycle, until finally, a whole cycle is lost. When the cycle is lost, the Integrate Phase lasts for two periods of the clock instead of the usual three periods. Thus, among a long string of divide-by-four's an occasional divide-by-three occurs; the average of the output frequency is very close to one quarter of the clock, but the instantaneous frequency can be very different. Because of this, it is very difficult to observe the waveform on an oscilloscope. During all of this time, the signal at the output of the integrator is a sawtooth wave with an envelope which is also a sawtooth. This is shown in Figure 4.

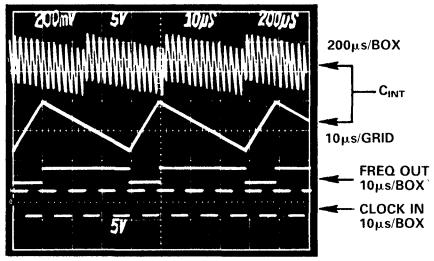


Figure 4. Integrator Output for I_{IN} Slightly Greater than 250μA

Another way to view this is that the output is a frequency of approximately one quarter of the clock that has been phase modulated. A constant frequency can be thought of as accumulating phase linearly with time at a rate equal to $2\pi f$ radians per second. Hence, the average output frequency which is slightly in excess of a quarter of the clock will require phase accumulation at a certain rate. However, since the SVFC is running at exactly one quarter of the clock, it will not accumulate enough phase (see Figure 5). When the difference between the required phase (average frequency) and the actual phase equals 2π, a step in phase is taken where the deficit is made up instantaneously. The output frequency is then a steady carrier which has been phase modulated by a sawtooth signal (see Figure 5). The period of the sawtooth phase modulation is the time required to accumulate a 2π difference in phase between the required average frequency and one quarter of the clock frequency. The amplitude of the sawtooth phase modulation is 2π.

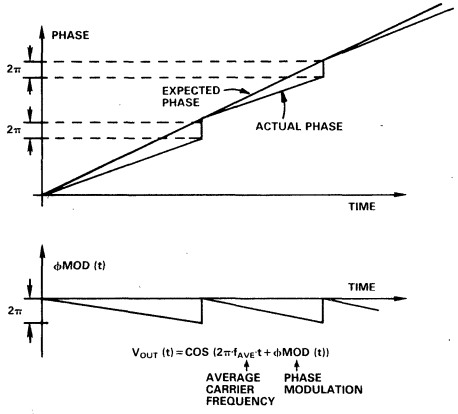


Figure 5. Phase Modulation

The result of this synchronism is that the rate at which data may be extracted from the series bit stream produced by the SVFC is limited. The output pulses are typically counted during a fixed gate interval and the result is interpreted as an average frequency. The resolution of such a measurement is determined by the clock frequency and the gate time. For example, if the clock frequency is 4MHz and the gate time is 4.096ms, then a maximum count of 8,192 is produced by a full-scale frequency of 2MHz. Thus, the resolution is 13 bits.

OVERRANGE

Since each reset pulse is only one clock period in length, the full-scale output frequency is equal to one-half the clock frequency. At full scale the current steering switch spends half of the time on the summing junction; thus, an input current of 0.5mA can be balanced. In the case of an overrange, the output of the integrator op amp will drift in the negative direction and the output of the comparator will remain high. The logic circuits will then simply settle into a "divide-by-two" of the clock state.

SVFC CONNECTION FOR DUAL SUPPLY, POSITIVE INPUT VOLTAGES

Figure 6 shows the AD651 connection scheme for the traditional dual supply, positive input mode of operation. The $\pm V_S$ range is from ± 6 to ± 18 volts. When $+V_S$ is lower than 9 volts, it is necessary to shunt pin 16 to pin 13 in order to maintain a minimum of 2 volts between pin 16 and $+V_S$. Pin 16 may be shorted directly to pin 13, or an external resistor may be shunted between the two pins. Shorting these pins will make analog ground the comparator reference; in this case pins 16 and 15 are tied directly to pin 13. If an external resistor is used then the comparator reference will be set by the 250μA current and this resistor.

The diode (IN4148 or similar) across pins 5 and 6 prevents any parasitic internal junctions from becoming forward biased under fault conditions. Opaque diodes should be used to prevent variances in the AD651 transfer function caused by photo injection.

The AD651 accepts either a 0 to 10V or 0 to 0.5mA full-scale input signal. The temperature drift of the AD651 is specified

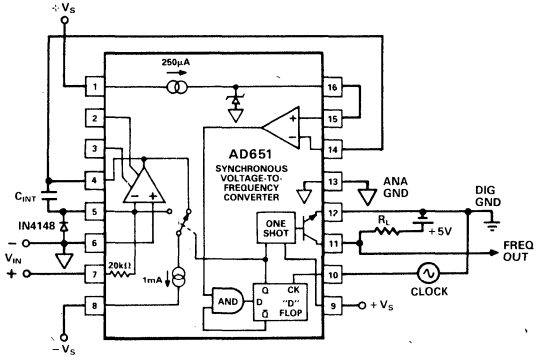


Figure 6. Standard V/F Connection for Positive Input Voltage with Dual Supply

for a 0 to 10V input range using the internal 20kΩ resistor. If a current input is used, the gain drift will be degraded by approximately 50ppm/°C (the TC of the 20kΩ resistor). If an external resistor is connected to pin 5 to establish a different input voltage range, drift will be induced to the extent that the external resistor's TC differs from −50ppm/°C. The external resistor used to establish a different input voltage range should be selected as to provide a full-scale current of 0.5mA (i.e., 10kΩ for 0 to 5V).

SVFC CONNECTIONS FOR NEGATIVE INPUT VOLTAGES

Voltages which are negative with respect to ground may be used as the input to the AD651 SVFC. In this case, pin 7 is grounded and the input voltage is applied to pin 6 (see Figure 7). In this mode the input voltage can go as low as 4 volts above $-V_S$. In this configuration the input is a high impedance, and only the 40nA (typical) input bias current of the op amp need be supplied by the input signal. This is contrasted with the more usual positive input voltage configuration, which has a 20kΩ input impedance and requires 0.5mA from the signal source.

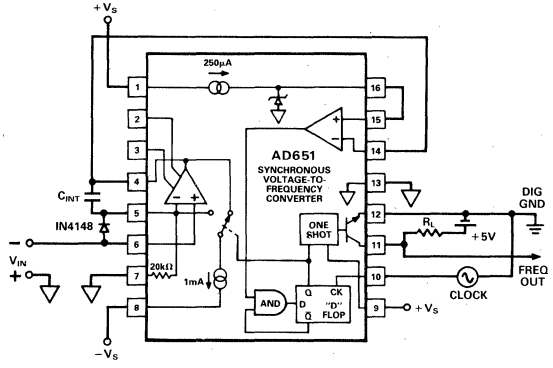


Figure 7. Negative Voltage Input

SVFC CONNECTION FOR BIPOLAR INPUT VOLTAGES

A bipolar input voltage of ±5V can be accommodated by injecting a 250μA current into pin 5. A −5V signal will then provide a zero sum current at the integrator summing junction which will result in a zero output frequency, while a +5V signal will provide a 0.5mA (full- scale) sum current which will result in the full-scale output frequency.

The 250μA bipolar offset current is best provided by an external reference voltage and resistor. However, if necessary, the comparator reference may be used. Since the current source feeding the zener diode is only 250μA, it is necessary to provide an additional 250μA from $+V_S$ for the bipolar offset current. This is shown in Figure 8.

GAIN AND OFFSET CALIBRATION

The gain error of the AD651 is laser trimmed to within ±0.5%. If higher accuracy is required, the internal 20kΩ resistor must be shunted with a 2MΩ resistor to produce a parallel equivalent which is 1% lower in value than the nominal 20kΩ. Full scale adjustment is then accomplished using a 500Ω series trimmer. See Figure 9. When negative input voltages are used, this 500Ω trimmer will be tied to ground and pin 6 will be the input pin.

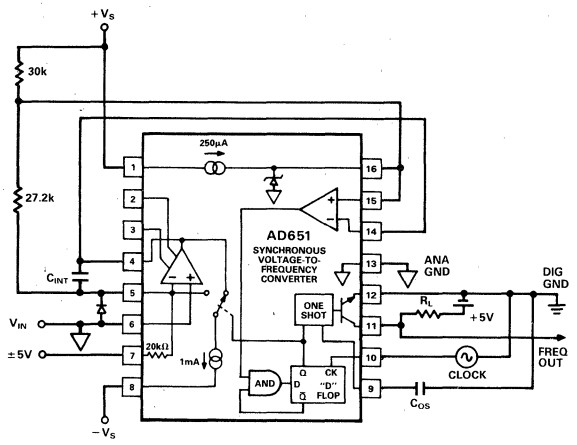


Figure 8. Bipolar Offset

This gain trim should be done with an input voltage of 9V, and the output frequency should be adjusted to exactly 45% of the clock frequency. Since the device settles into a divide-by-two mode for an input overrange condition, adjusting the gain with a 10V input is impractical; the output frequency would be exactly one-half the clock frequency if the gain were too high and would not change with adjustment until the exact proper scale factor was achieved. Hence, the gain adjustment should be done with a 9V input.

The offset voltage of the op amp may be trimmed to zero with a 20kΩ potentiometer across pins 2 and 3 and the wiper connected to $+V_S$ through a 250kΩ resistor. This is also shown in Figure 9. The offset is then trimmed by grounding pin 7 and observing the waveform at pin 4. If the offset voltage of the op amp is positive, then the integrator will have saturated and the voltage at pin 4 will be at the positive rail. If the offset voltage is negative, then there will be a small effective input current that will cause the AD651 to oscillate and a sawtooth waveform will be observed at pin 4. The trimpot should be adjusted until the downward slope of this sawtooth becomes very slow, down to a frequency of 1Hz or less.

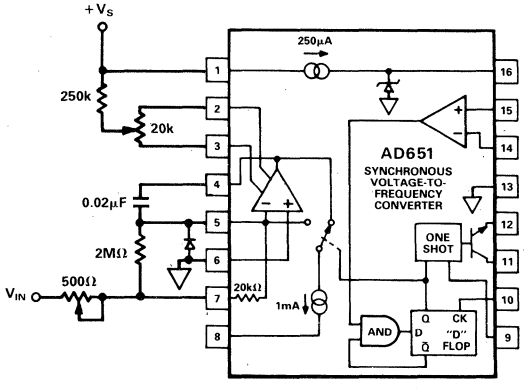


Figure 9. Gain and Offset Trim

GAIN PERFORMANCE

The AD651 gain error is specified as the difference in slope between the actual and the ideal transfer function over the full-scale frequency range. Figure 10 shows a plot of the typical gain error changes vs. the clock input frequency, normalized to 100kHz. If after using the AD651 with a full-scale clock frequency of 100kHz it is decided to reduce the necessary gating time by increasing the clock frequency, this plot shows the typical gain changes normalized to the original 100kHz gain.

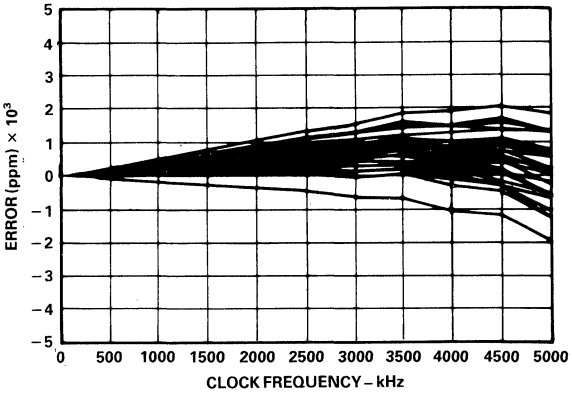


Figure 10. Gain vs. Clock Input

DIGITAL INTERFACING CONSIDERATIONS

The AD651 clock input is a high impedance input with a threshold voltage of two diode voltages with respect to Digital Ground at pin 12 (approximately 1.2 volts at room temp). When the clock input is low, 5-10μA flows out of this pin. When the clock input is high, no current flows.

The frequency output is an open collector pull-down and is capable of sinking 8mA with a maximum voltage of 0.4 volts. This will drive 5 standard TTL inputs. The open collector pull up voltage can be as high as 36 volts above digital ground.

COMPONENT SELECTION

The AD651 integrating capacitor should be 0.02μF. If a large amount of normal mode interference is expected (more than 0.1 volts) and the clock frequency is less than 500kHz, an integrating capacitor of 0.1μF should be used. Mylar, polypropylene, or polystyrene capacitors should be used.

The open collector pull-up resistor should be chosen to give adequately fast rise times. At low clock frequencies (100kHz) larger resistor values (several kΩ) and slower rise times may be tolerated. However, at higher clock frequencies (1MHz) a lower value resistor should be used. The loading of the logic input which is being driven must also be taken into consideration. For example, if 2 standard TTL loads are to be driven then a 3.2mA current must be sunk, leaving 4.8mA for the pull-up resistor if the maximum low level voltage is to be maintained at 0.4 volts. A 960Ω resistor would thus be selected ((5–0.4)V/4.8mA) = 960Ω.

The one-shot capacitor controls the pulse width of the frequency output. The pulse is initiated by the rising edge of the clock signal. The delay time between the rising edge of the clock and the falling edge of the frequency output is typically 150ns. The width of the pulse is 5ns/pF and the minimum width is about 100ns with pin 9 floating. If the one-shot period is accidentally chosen longer than the clock period, the width of the pulse will default to equal the clock period. The one-shot can be disabled by connecting pin 9 to $+V_S$ (Figure 11); the output pulse width will then be equal to the clock period. The one-shot is activated (Figure 12) by connecting a capacitor from pin 9 to $+V_S$, $-V_S$, or Digital Ground($+V_S$ is preferred).

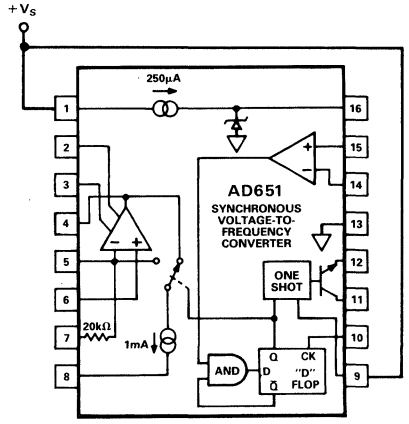


Figure 11. One Shot Disabled

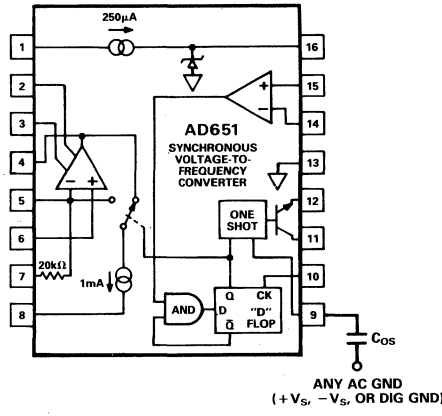


Figure 12. One Shot Enabled

DIGITAL GROUND

Digital Ground can be at any potential between $-V_S$ and ($+V_S$ -4 volts). This can be very useful a system with derived grounds rather than stiff supplies. For example, in a small isolated power circuit, often only a single supply is generated and the "ground" is set by a divider tap. Such a ground cannot handle the large currents associated with digital signals. With the AD651 SVFC, it is possible to connect the DIG GND to $-V_S$ for a solid logic reference, as shown in Figure 13.

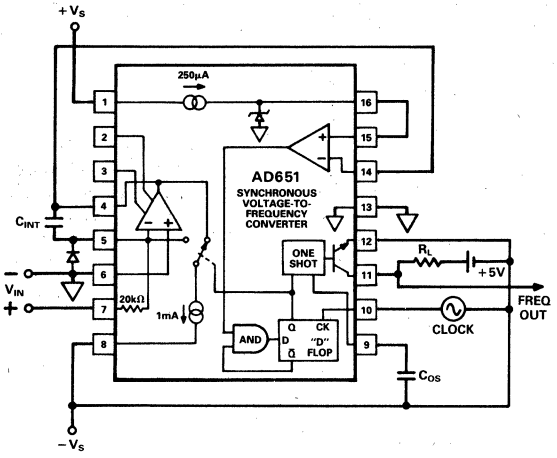


Figure 13. Digital GND at $-V_S$

SINGLE SUPPLY OPERATION

In addition to the Digital Ground being connected to $-V_S$, it is also possible to connect Analog Ground to $-V_S$ of the AD651. Hence, the device is truly operating from a single supply voltage that can range from +12V to +36V. This is shown in Figure 14 for a positive voltage input and Figure 15 for a negative voltage input.

In Figure 14, the comparator reference is used as a derived ground, and the input voltage is referred to this point as well as the op amp common mode (pin 6 is tied to pin 16). It is necessary to place a pull up resistor between pin 16 and $+V_S$ to provide at least 0.5mA of current into pin 16. Since the input signal source must drive 0.5mA of full-scale signal current into pin 7, it must also draw the exact same current from the input reference potential. Since the internal current source driving the zener diode comparator reference is only 250μA, it cannot supply the current needed; hence the reason for the pull-up resistor between pin 16 and $+V_S$. The exact amount of extra current that must be supplied by the external resistor is not critical, so long as it is more than the 0.5mA full-scale signal current.

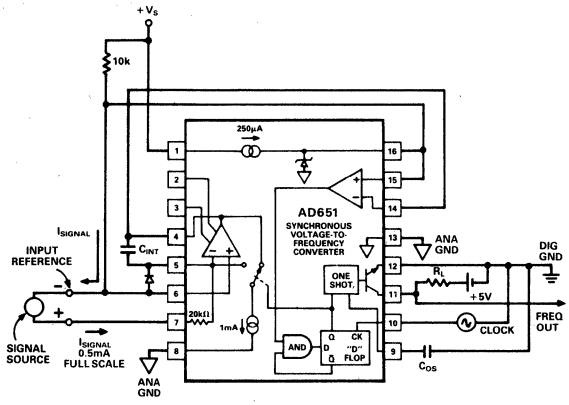


Figure 14. Single Supply Positive Voltage Input

Figure 15 shows the negative voltage input configuration for use of the AD651 in the single supply mode. Again, an external resistor is needed to supply the signal current being drawn out of the input reference. However, in this mode the signal source is driving the "+" input of the op amp which requires only 40nA (typical), rather than the 0.5mA required in the positive input voltage configuration. The voltage at pin 6 may go as low as 4 volts above ground ($-V_S$, pin 8). Since the input reference is about 6.5 volts above ground, this leaves a 2.5V window for the input signal. In order to drive the integrating capacitor with a 0.5mA full-scale current, it is necessary to shunt the internal 20kΩ resistor with an external 5kΩ resistor. This results in a 4kΩ equivalent resistor and a 2V input range. The external 5kΩ resistor should be a low-TC metal-film type for lowest drift degradation.

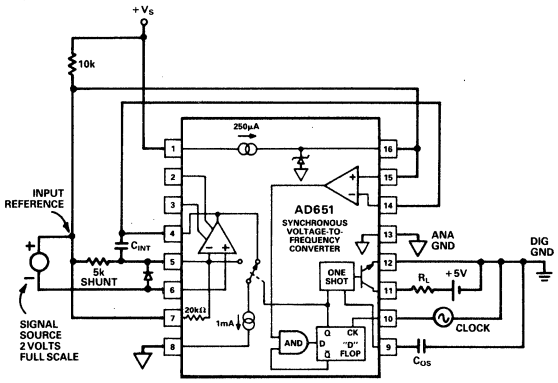


Figure 15. Single Supply Negative Voltage Input

FREQUENCY-TO-VOLTAGE CONVERTER

The AD651 SVFC also works as a frequency-to-voltage converter. Figure 16 shows the connection diagram for F/V conversion. In this case the "−" input of the comparator is fed the input pulses. Either comparator input may be used so that an input pulse of either polarity may be applied to the F/V. In Figure 16 the "+" input is tied to a 1.2V reference and low level TTL pulses are used as the frequency input. The pulse must be low on the falling edge of the clock. On the subsequent rising edge the 1mA current source is switched to the integrator summing junction and ramps up the voltage at pin 4. Due to the action of the AND gate, the 1mA current is switched off after only one clock period. The average current delivered to the summing junction varies from 0 to 0.5mA; using the internal 20kΩ resistor this results in a full-scale output voltage of 10V at pin 4.

The frequency response of the circuit is determined by the capacitor; the −3dB frequency is simply the RC time constant. A tradeoff exists between ripple and response. If low ripple is desired, a large value capacitor must be used (1μF), if fast response is needed, a small capacitor is used (1nF minimum).

The op amp can drive a 5kΩ resistor load to 10V, using a 15V positive power supply. If a large load capacitance (0.01μF) must be driven, then it is necessary to isolate the load with a 50Ω resistor as shown. Since the 50Ω resistor is 0.25% of the full scale, and the specified gain error with the 20kΩ resistor is ±0.5%, this extra resistor will only increase the total gain error to +0.75% max.

The circuit shown is unipolar and only a 0 to +10V output is allowed. The integrator op amp is not a general purpose op amp, rather it has been optimized for simplicity and high speed.

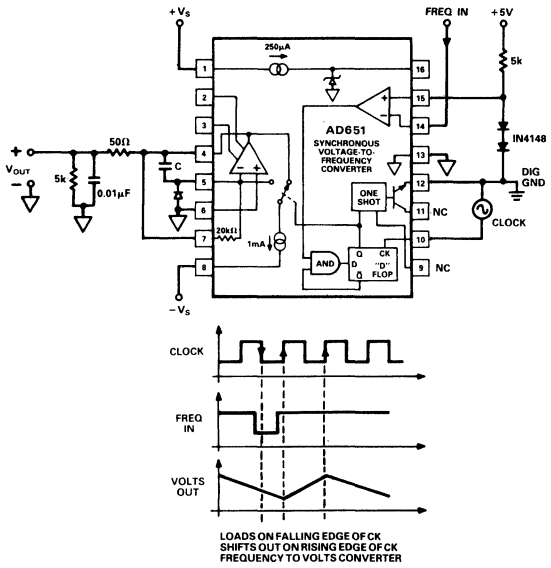


Figure 16. Frequency-to-Voltage Converter

The most significant difference between this amplifier and a general purpose op amp is the lack of an integrator (or level shift) stage. Consequently, the voltage on the output (pin 4) must always be more positive than 1 volt below the inputs (pins 6 and 7). For example, in the F-to-V conversion mode, the noninverting input of the op amp (pin 6) is grounded which means that the output (pin 4) cannot go below −1 volt. Normal operation of the circuit as shown will never call for a negative voltage at the output.

A second difference between this op amp and a general purpose amplifier is that the output will only sink 1.5mA to the negative supply. The only pulldown other than the 1mA current used for voltage-to-frequency conversion is a 0.5mA source. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 4 volts of the positive supply when not sourcing external current. When sourcing 10mA, the output voltage may be driven to within 6 volts of the positive supply.

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD651.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD651 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD651.

Separate digital and analog grounds are provided on the AD651. The emitter of the open collector frequency output transistor and the clock input threshold only are returned to the digital ground. Only the comparator reference zener diode is connected to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. Much noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At high full scale, it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA. This much current being switched will cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD651 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD651 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground, pin 12. The pull-up resistor should be connected directly to the frequency output, pin 11. The lead lengths on the bypass capacitor and the pull-up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull-up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 12) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current. There may be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause a problem. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 6) at the package. More information on proper grounding and reduction of interference can be found in reference 1.

[1]"Noise Reduction Techniques in Electronic Systems", by H.W. Ott, (John Wiley, 1976).

Applications

FREQUENCY OUTPUT MULTIPLIER

The AD651 can serve as a frequency output multiplier when used in conjunction with a standard voltage-to-frequency converter. Figure 17 shows the low cost AD654 VFC being used as the clock input to the AD651. Also shown is a second AD651 in the F/V mode. The AD654 is set up to produce an output frequency of 0-500kHz for an input voltage (V_1) range of 0-10V. The use of R4, C1, and the XOR gate doubles this output frequency from 0-500kHz to 0-1MHz.

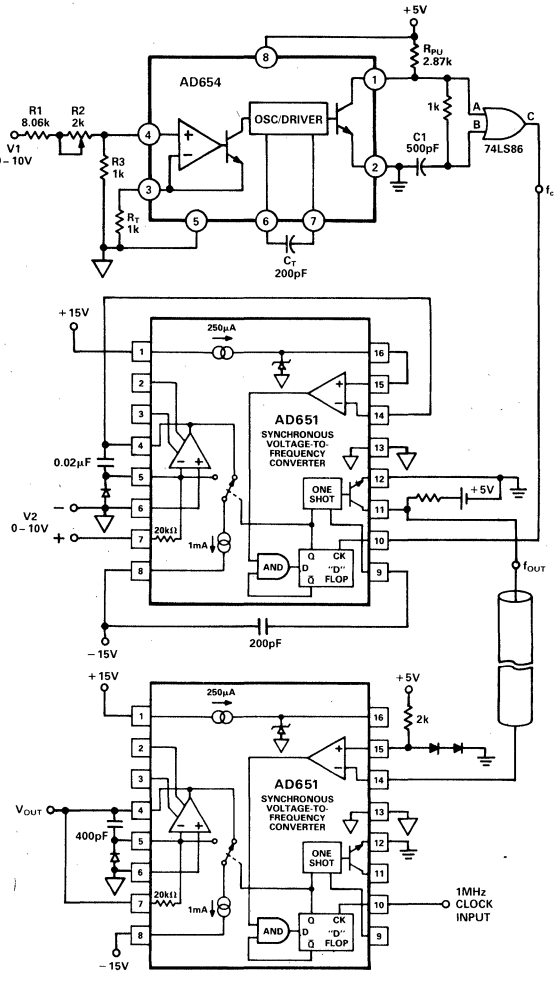


Figure 17. Frequency Output Multiplier

This 1MHz full-scale frequency is then used as the clock input to the AD651 SVFC. Since the AD651 full-scale output frequency is one-half the clock frequency, the 1MHz FS clock frequency establishes a 500kHz maximum output frequency for the AD651 when its input voltage (V_2) is +10V. The user thus has an output frequency range from 0-500kHz which is proportional to the product of V_1 and V_2.

This can be shown in equation form, where f_C is the AD654 output frequency and f_{OUT} is the AD651 output frequency:

$$f_C = V_1 \frac{1MHz}{10V}$$

$$f_{OUT} = V_2 \left(\frac{f_C/2}{10V}\right)$$

$$f_{OUT} = V_1 V_2 \left(\frac{1MHz}{2(10V)\,(10V)}\right)$$

$$f_{OUT} = V_1 \cdot V_2 \cdot 5kHz/V^2$$

The scope photo in Figure 18 shows V_1 and V_2 (top two traces) and the output of the F-V (bottom trace).

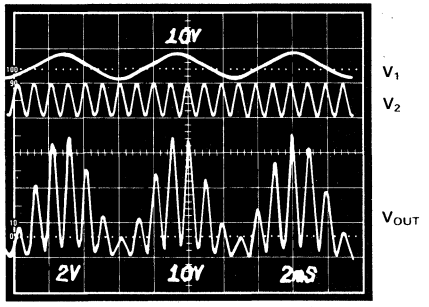


Figure 18. Multiplier Waveforms

SINGLE-LINE MULTIPLEXED DATA TRANSMISSION

It is often necessary to measure several different signals and relay the information to some remote location using a minimum amount of cable. Multiple AD651 SVFC devices may be used with a multiphase clock to combine these measurements for serial transmission and demultiplexing. Figure 19 shows a block diagram of a single-line multiplexed data transmission system with high noise immunity. Figures 20, 21 and 22 show the SVFC multiplexer, a representative means of data transmission, and an SVFC demultiplexer respectively.

Multiplexer

Figure 20 shows the SVFC multiplexer. The clock inputs for the several SVFC channels are generated by a TIM9904A four phase clock driver, and the frequency outputs are combined by strapping all the frequency output pins together (a "wire or" connection). The one-shot in the AD651 sets the pulse width of the frequency output pulses to be slightly shorter than one quarter of the clock period. Synchronization is achieved by applying one of the four available phases to a fixed TTL one-shot ('121) and combining the output with an external transistor. The width of this sync pulse is shorter than the width of the frequency output pulses to facilitate decoding the signal. The RC lag network on the input of the one-shot provides a slight delay between the rising edge of the clock and the sync pulse in order to match the 150ns delay of the AD651 between the rising edge of the clock and the output pulse.

Transmitter

The multiplexer signal can be transmitted in any manner suitable to the task at hand. A pulse transformer or an opto-isolator can

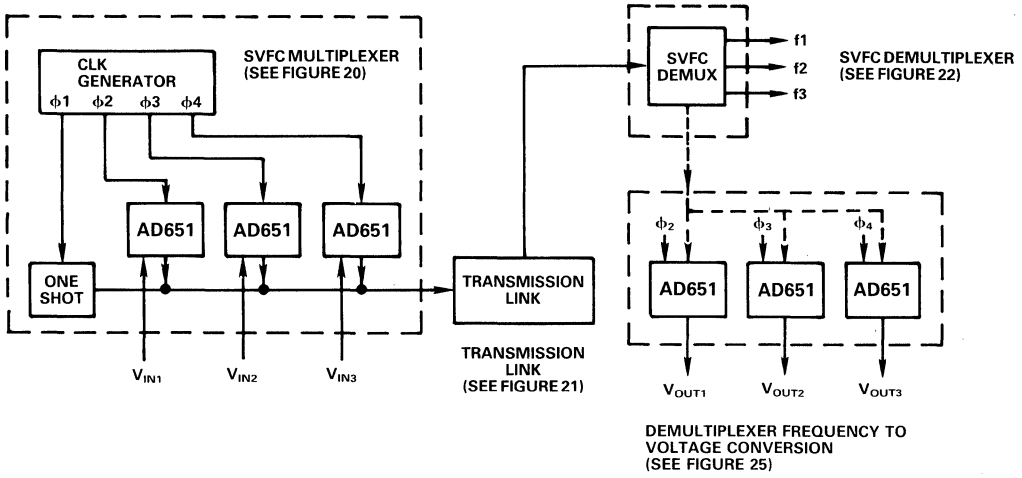


Figure 19. Single Line Multiplexed Data Transmission Block Diagram

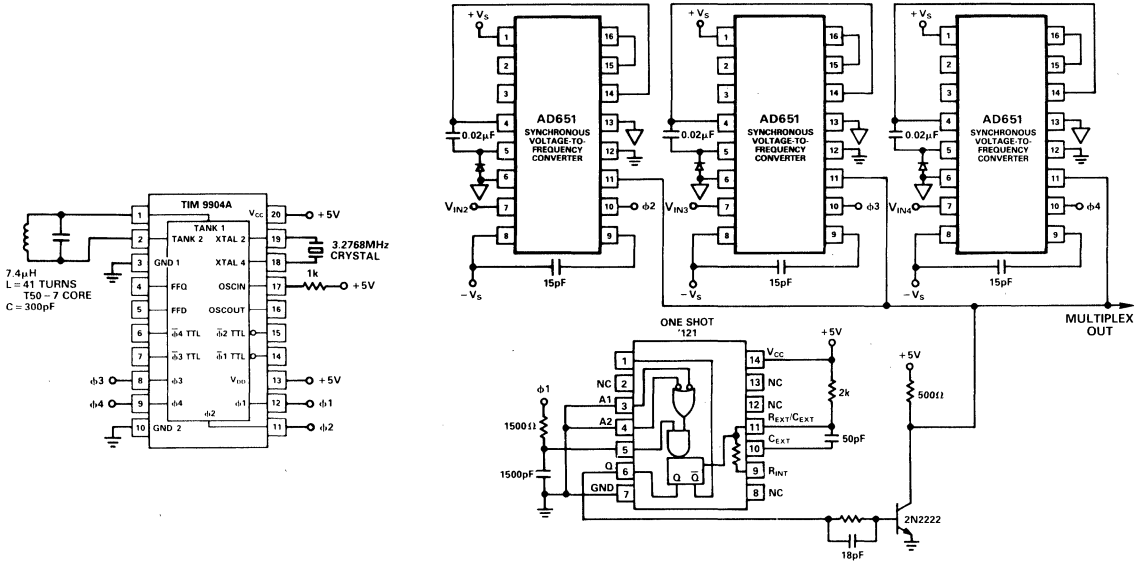


Figure 20. SVFC Multiplexer

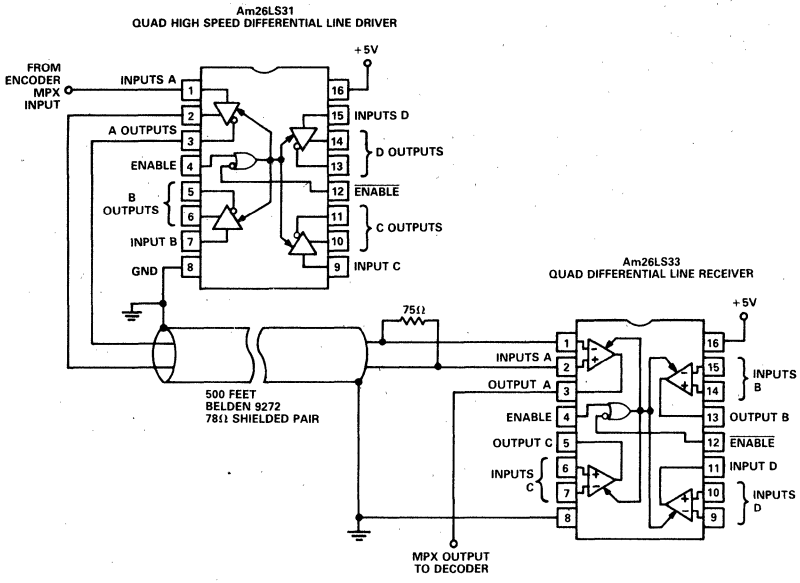


Figure 21. RS-422 Standard Data Transmission

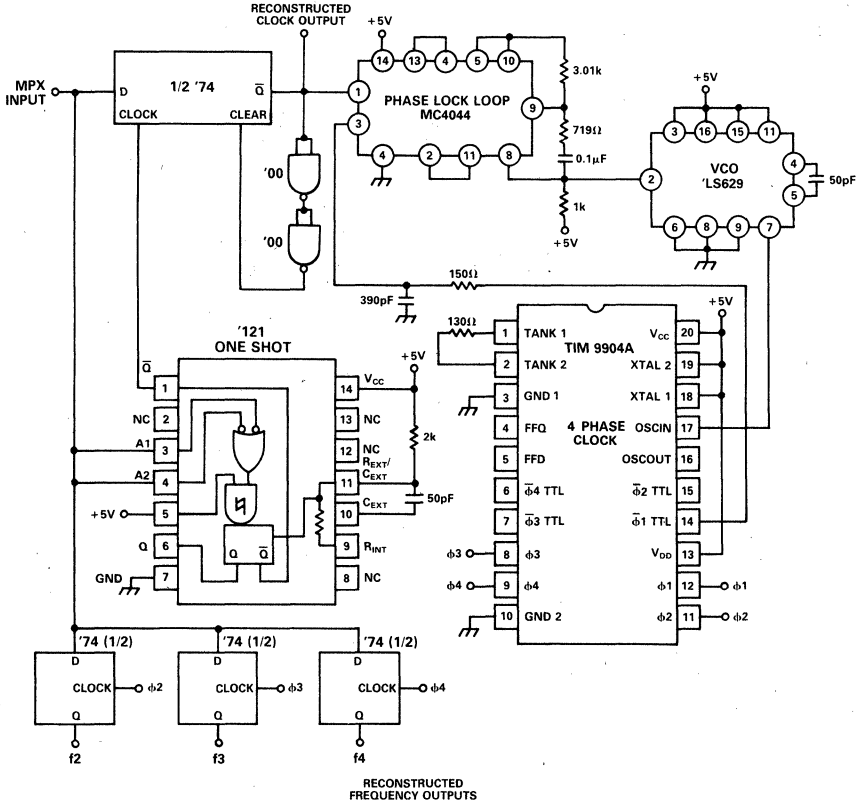


Figure 22. SVFC Demultiplexers

provide galvanic isolation; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The circuit shown in Figure 21 uses an EIA RS-422 standard for digital data transmission over a balanced line. Figure 23 shows the waveforms of the four clock phases and the multiplex output signal. Note that the sync pulse is present every clock cycle, but the data pulses are no more frequent than every other clock cycle since the maximum output frequency from the SVFC is half the clock frequency. The clock frequency used in this circuit is 819.2 kHz and will provide more than 16 bits of resolution if 100 millisecond gate time is allowed for counting pulses of the decoded output frequencies.

SVFC Demultiplexer

The demultiplexer needed to separate the combined signals is shown in Figure 22. A phase locked loop drives another four phase clock chip to lock onto the reconstructed clock signal. The sync pulses are distinguished from the data pulses by their shorter duration. Each falling edge on the multiplex input signal triggers the one-shot, and at the end of this one-shot pulse the multiplex input signal is sampled by a D-type flip-flop. If the signal is high, then the pulse was short (a sync pulse) and the $\overline{Q}$ output of the D-flop goes low. The D-flop is cleared a short time (two gate delays) later, and the clock is reconstructed as a stream of short, low-going pulses. If the Multiplex input is a data pulse, then when the D-flop samples at the end of the one-shot period, the signal will still be low and no pulse will appear at the reconstructed clock output. These waveforms are shown in Figure 24.

If it is desired to recover the individual frequency signals, then the multiplex input is sampled with a D-flop at the appropriate time as determined by the rising edge of the various phases generated by the clock chip. These frequency signals can be counted as a ratio relative to the reconstructed clock, so it is not even necessary for the transmitter to be crystal controlled as shown here.

Analog Signal Reconstruction

If it is desired to reconstruct the analog voltages from the multiplex signal, then three more AD651 SVFC devices are used as frequency-to-voltage converters, as shown in Figure 25. The comparator inputs of all the devices are strapped together, and the "+" inputs are held at a 1.2 volt TTL threshold, while the "−" inputs are driven by the multiplex input. The three clock inputs are driven by the $\overline{\phi}$ outputs of the clock chip. Remember that data at the comparator input of the SVFC is loaded on the falling edge of the clock signal and shifted out on the next rising edge. Note that the frequency signals for each data channel are available at the frequency output pin of each FVC.

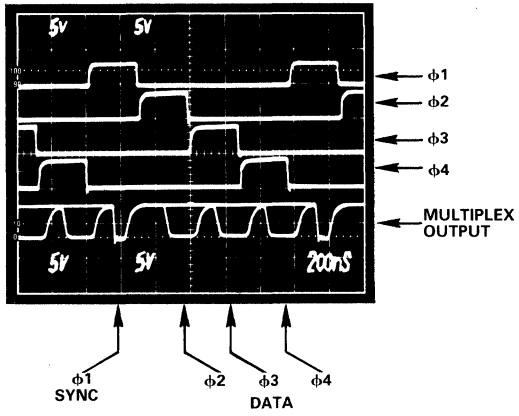


Figure 23. Multiplexer Waveforms

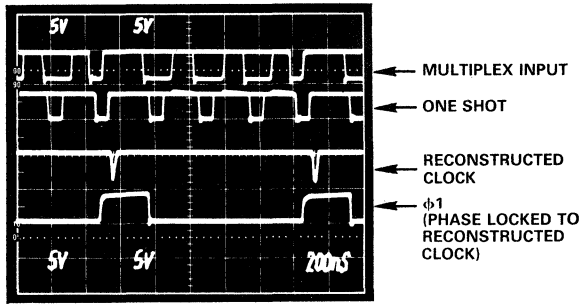


Figure 24. Demultiplexer Waveforms

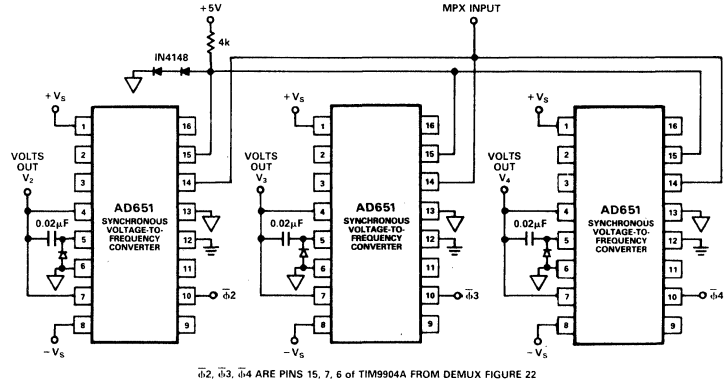


Figure 25. Demultiplexer Frequency-to-Voltage Conversion

ISOLATED FRONT END

In some applications it may be necessary to have complete galvanic isolation between the analog signals being measured and the digital portions of the circuit. The circuit shown in Figure 26 runs off a single 5 volt power supply and provides a self-contained, completely isolated analog measurement system. The power for the AD651 SVFC is provided by a chopper and a transformer, and is regulated to ±15 volts.

Both the chopper frequency and the AD651 clock frequency are 125kHz, with the clock signal being relayed to the SVFC through the transformer. The frequency output signal is relayed through an opto-isolator and latched into a D-flop. The chopper frequency is generated from an AD654 VFC and is frequency divided by two to develop differential drive for the chopper transistors, and to ensure an accurate 50 percent duty cycle. The pull-up resistors on the D-flop outputs provide a well defined high level voltage to the choppers to equalize the drive in each direction. The 10μH inductor in the +5V lead of the transformer primary is necessary to equalize any residual imbalance in the drive on each half-cycle and thus prevent saturation of the core. The capacitor across the primary resonates the system so that under light loading conditions on the secondary the wave shape will be sinusoidal and the clock frequency will be relayed to the SVFC. To adjust the chopper frequency, disconnect any load on the secondary and tune the AD654 for a minimum in the supply current drawn from the 5 volt supply.

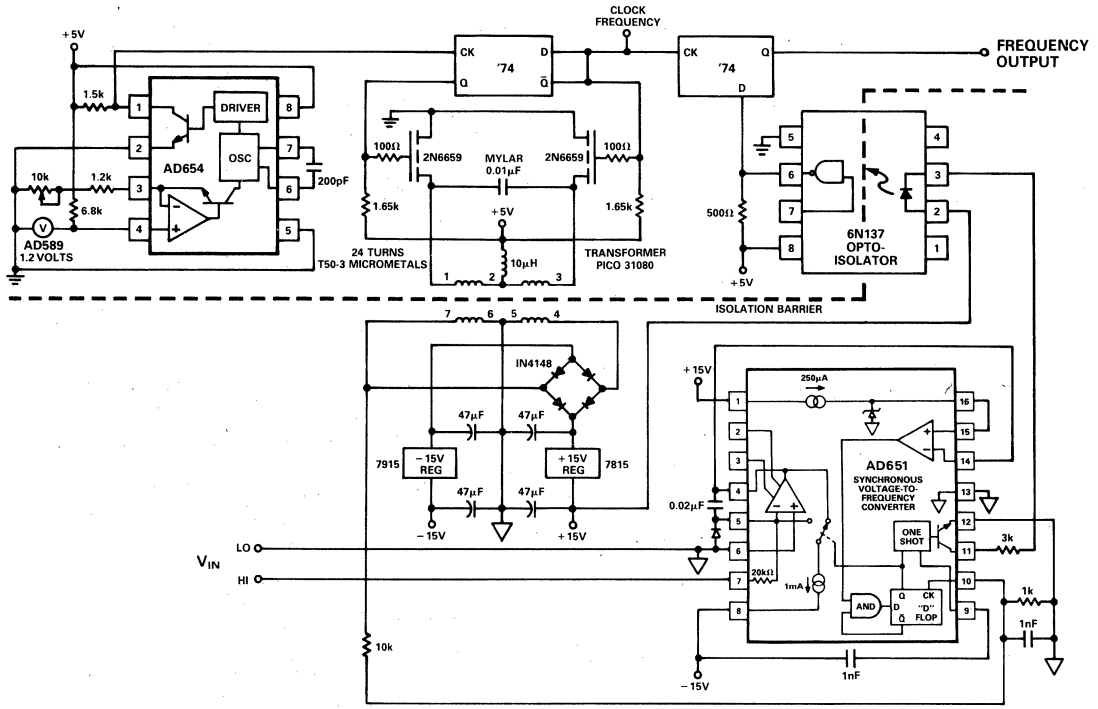


Figure 26. Isolated Synchronous VFC

A-TO-D CONVERSION

In performing an A-to-D conversion, the output pulses of a VFC are counted for a fixed gate interval. To achieve maximum performance with the AD651, the fixed gate interval should be generated using a multiple of the SVFC clock input. Counting in this manner will eliminate any errors due to the clock (whether it be jitter, drift with time or temperature, etc.) since it is the ratio of the clock and output frequencies that is being measured.

The resolution of the A-to-D conversion measurement is determined by the clock frequency and the gate time. If, for instance, a resolution of 12 bits is desired and the clock frequency is 1MHz (resulting in an AD651 FS frequency of 500kHz) the gate time will be:

$$\left(\frac{\text{FS Freq}}{N}\right)^{-1} = \left(\frac{1}{2}\,\frac{\text{Clock Freq}}{N}\right)^{-1} = \left(\frac{1\text{MHz}}{2(4096)}\right)^{-1}$$

$$= \frac{8192}{1\times10^{6}}\ \text{sec} = 8.192\text{ms}$$

: Where N is the total number of codes for a given resolution.

Figure 27 shows the AD651 SVFC as an A-to-D converter in block diagram form.

To provide the ÷ 2N block a single chip counter such as the 4020B can be used. The 4020B is a 14-stage binary ripple counter which has a clock and master reset for inputs, and buffered outputs from the first stage and the last eleven stages. The output of the first stage is $f_{CLOCK} \div 2^1 = f_{CLOCK}/2$, while the output of the last stage is $f_{CLOCK} \div 2^{14} = f_{CLOCK}/16384$. Hence using this single chip counter as the ÷ 2N block, 13-bit resolution can be achieved. Higher resolution can be achieved by cascading D-type flip-flops or another 4020B with the counter.

Table I shows the relationship between clock frequency and gate time for various degrees of resolution. Note that if the variables are chosen such that the gate times are multiples of 50, 60 or 400Hz, normal-mode rejection (NMR) of those line frequencies will occur.

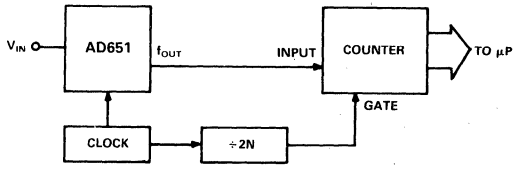


Figure 27. Block Diagram of SVFC A-to-D Converter

3

Resolution	N	Clock	Conversion or Gate Time	Typ Lin	Comments
12 Bits	4096	81.92kHz	100ms	0.002%	50, 60, 400Hz NMR
12 Bits	4096	2MHz	4.096ms	0.01%	
12 Bits	4096	4MHz	2.048ms	0.02%	
4 Digits	10000	200kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	327.68kHz	100ms	0.002%	50, 60, 400Hz NMR
14 Bits	16384	1.966MHz	16.66ms	0.01%	60Hz NMR
14 Bits	16384	1.638MHz	20ms	0.01%	50Hz NMR
4 1/2 Digits	20000	400kHz	100ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	655.36kHz	200ms	0.002%	50, 60, 400Hz NMR
16 Bits	65536	4MHz	32.77ms	0.02%	

Table I.

DELTA MODULATOR

The circuit of Figure 28 shows the AD651 configured as a delta modulator. A reference voltage is applied to the input of the integrator (pin 7), which sets the steady state output frequency at one-half of the AD651 full-scale frequency (1/4 of the clock frequency). As a 0 to 10V input signal is applied to the comparator (pin 15), the output of the integrator attempts to track this signal. For an input in an idling condition (dc) the output frequency will be one-half full scale. For positive going signals the output frequency will be between one-half full scale and full scale, and for negative going signals the output frequency will be between zero and one-half full scale. The output frequency will correspond to the slope of the comparator input signal.

Since the output frequency corresponds to the slope of the input signal, the delta modulator acts as a differentiator. A delta modulator is thus a direct way of finding the derivative of a signal. This is useful in systems where, for example, a signal corresponding to velocity exists and it is desired to determine acceleration.

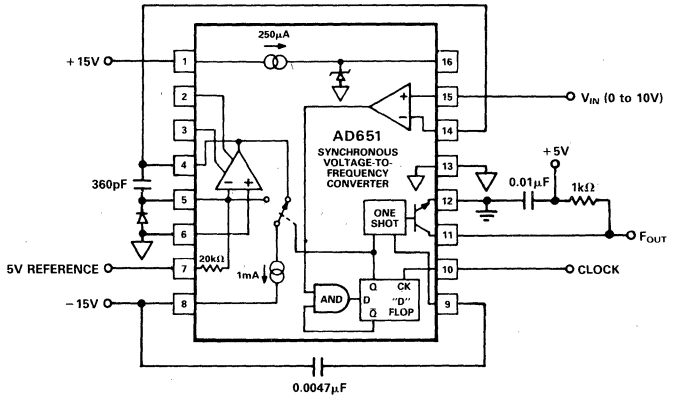


Figure 28. Delta Modulator

Figure 29 is a scope photo showing a 20kHz, 0 to 10V sine wave used as the input to the comparator and its ramp-wise approximation at the integrator output. The clock frequency used as 2MHz and the integrating capacitor was 360pF. Figure 30 shows the same input signal and its ramp-wise approximation, along with the output frequency corresponding to the derivative of the input signal. In this case the clock frequency was 850kHz.

The choice of an integrating capacitor is primarily dictated by the input signal bandwidth. Figure 31 shows this relationship. It should be noted that as the value of C_{INT} is lowered, the ramp size of the integrator approximation becomes larger. This can be compensated for by increasing the clock frequency. The effect of the clock frequency on the ramp size is demonstrated in Figures 29 and 30.

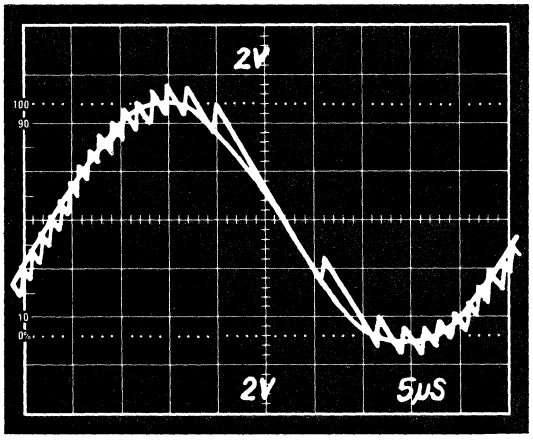


Figure 29. Delta Modulator Input Signal and Ramp-Wise Approximation

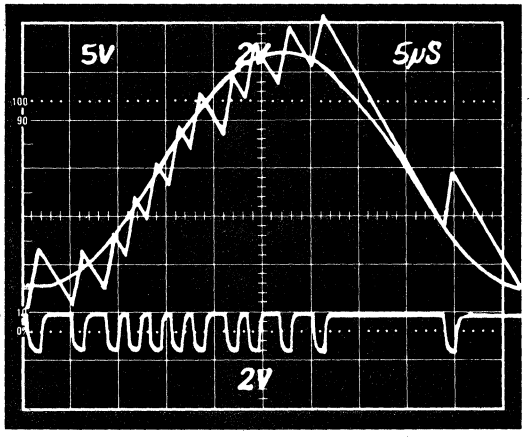


Figure 30. Delta Modulator Input Signal, Ramp-Wise Approximation and Output Frequency

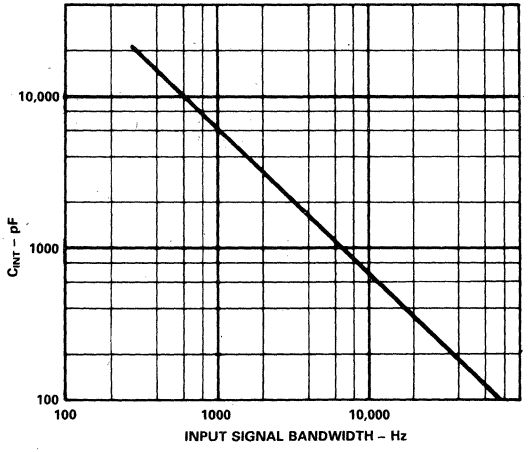


Figure 31. Maximum Integrating Cap Value vs. Input Signal Bandwidth

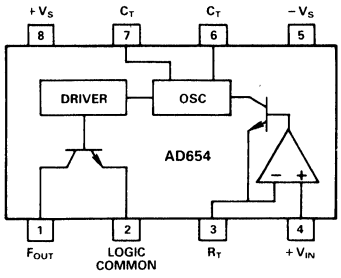
ANALOG DEVICES

Low Cost Monolithic Voltage-to-Frequency Converter

AD654

FEATURES
Low Cost
Single or Dual Supply, 5 to 36 Volts, ±5V to ±18V
Full Scale Frequency Up to 500kHz
Minimum Number of External Components Needed
Versatile Input Amplifier
Positive or Negative Voltage Modes
Negative Current Mode
High Input Impedance, Low Drift
Low Power: 2.0mA Quiescent Current
Low Offset: 1mV

AD654 PIN CONFIGURATION



3

PRODUCT DESCRIPTION

The AD654 is a monolithic V/F converter consisting of an input amplifier, a precision oscillator system, and a high current output stage. A single RC network is all that is required to set up any full scale (F.S.) frequency up to 500kHz and any F.S. input voltage up to ±30V. Linearity error is only 0.03% for a 250kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±50ppm/°C. The AD654 operates from a single supply of 5 to 36V and consumes only 2.0mA quiescent current.

The low drift (4μV/°C typ) input amplifier allows operation directly from small signals such as thermocouples or strain gauges while offering a high (250MΩ) input resistance. Unlike most V/F converters, the AD654 provides a square-wave output, and can drive up to 12 TTL loads, opto-couplers, long cables, or similar loads.

PRODUCT HIGHLIGHTS

1. Packaged in an 8-pin mini-DIP, the AD654 is a complete V/F converter requiring only an RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of the timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.

2. A minimum number of low cost external components are necessary. A single RC network is all that is required to set up any full scale frequency up to 500kHz and any full scale input voltage up to ±30V.

3. Plastic packaging allows low cost implementation of the standard VFC applications: A/D conversion, isolated signal transmission, F/V conversion, phase-locked loops, and tuning switched-capacitor filters.

4. Power supply requirements are minimal; only 2.0mA of quiescent current is drawn from the single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to $(+V_S - 4)$ volts. Negative inputs can easily be connected for below ground operation.

5. The versatile open-collector output stage can sink more than 10mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

SPECIFICATIONS (@ +25°C and V_S (total) = 5 to 16.5V, unless otherwise specified. All testing done @ 5V).

Model	AD654JN Min	Typ	Max	Units
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0		500	kHz
Nonlinearity[1]				
f_{max} = 250kHz		0.03	**0.1**	%
f_{max} = 500kHz		0.20	0.4	%
Full Scale Calibration Error				
C = 390pF, I_{IN} = 1.000mA	**−10**		**10**	%
vs. Supply ($f_{max} \leq$ 250kHz)				
V_S = +4.75 to +5.25V		0.20	**0.40**	%/V
V_S = +5.25 to +16.5V		0.05	**0.10**	%/V
vs. Temp (0 to 70°C)		50		ppm/°C
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0		(+V_S −4)	V
Dual Supply	−V_S		(+V_S −4)	V
Input Bias Current				
(Either Input)		30	**50**	nA
Input Offset Current		5		nA
Input Resistance (Non-Inverting)		250		MΩ
Input Offset Voltage		0.5	**1.0**	mV
vs. Supply				
V_S = +4.75 to +5.25V		0.1	**0.25**	mV/V
V_S = +5.25 to +16.5V		0.01	0.1	mV/V
vs. Temp (0 to 70°C)		4		μV/°C
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"[2]				
V_{OUT} = 0.4V max, 25°C	**10**	20		mA
V_{OUT} = 0.4V max, 0 to 70°C	5	10		mA
Output Leakage Current in Logic "1"		10	**100**	nA
0 to 70°C		50	500	nA
Logic Common Level Range	−V_S		(+V_S −4)	V
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA		0.2		μs
I_{IN} = 1μA		1		μs
POWER SUPPLY				
Voltage, Rated Performance	4.5		16.5	V
Voltage, Operating Range				
Single Supply	4.5		36	V
Dual Supply	±5		±18	V
Quiescent Current				
V_S (Total) = 5V		1.5	**2.5**	mA
V_S (Total) = 30V		2.0	**3.0**	mA
TEMPERATURE RANGE				
Rated Performance	0		70	°C
Operating Range	−40		85	°C

NOTES

[1]At f_{max} = 250kHz; R_T = 1kΩ, C_T = 390pF, I_{IN} = 0-1mA.
f_{max} = 500kHz; R_T = 1kΩ, C_T = 200pF, I_{IN} = 0-1mA.

[2]The sink current is the amount of current that can flow into Pin 1 of the AD654 while maintaining a maximum voltage of 0.4V between Pin 1 and Logic Common.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

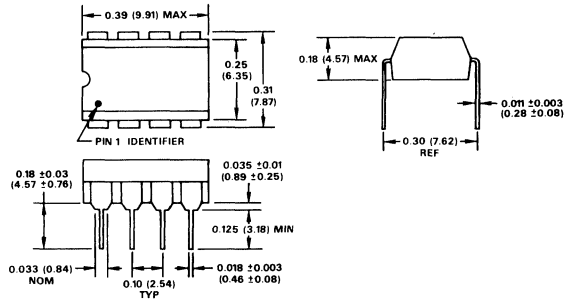
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Maximum Input Voltage
(Pins 3, 4) to $-V_S$ . . . . . $-300mV$ to $+V_S$
Maximum Output Current
Instantaneous 50mA
Sustained 25mA
Logic Common to $-V_S$ . . . . . $-500mV$ to $(+V_S - 4)$
Storage Temperature Range . . . . . $-65°C$ to $+150°C$

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



3

CIRCUIT OPERATION

The AD654's block diagram appears in Figure 1. A versatile operational amplifier serves as the input stage; its purpose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter (an astable multivibrator). The drive current provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 100nA to 2mA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a level other than $-V_S$.

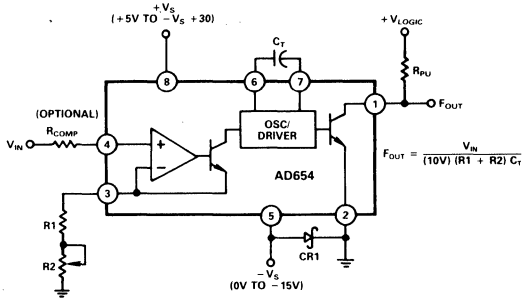


Figure 1. Standard V-F Connection for Positive Input Voltages

V/F CONNECTION FOR POSITIVE INPUT VOLTAGES

In the connection scheme of Figure 1, the input amplifier presents a very high (250MΩ) impedance to the input voltage, which is converted into the proper drive current by the scaling resistors at pin 3. Resistors R1 and R2 are selected to provide a 1mA full scale current with enough trim range to accommodate the AD654's 10% FS error and the components' tolerances. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive. The AD654's positive input voltage range spans from $-V_S$ (ground in single supply operation) to four volts below the positive supply. Power supply rejection degrades as the input exceeds $(+V_S - 3.75V)$ and at $(+V_S - 3.5V)$ the output frequency goes to zero.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. Good V/F linearity requires the use of a capacitor with low dielectric absorption (DA), while the most stable operation over temperature calls for a component having a small tempco. Polystyrene, polypropylene, or Teflon* capacitors are preferred for tempco and dielectric absorption; other types will degrade linearity. The capacitor should be wired very close to the AD654. In Figure 1, Schottky diode CR1 (MBD101) preyents logic common from dropping more than 500mV below $-V_S$. This diode is not required if $-V_S$ is equal to logic common.

V/F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

The AD654 can accommodate a wide range of negative input voltages with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance because the signal source must supply the 1mA F.S. drive current. However, large negative voltages beyond the supply can be handled easily by modifying the scaling resistors appropriately. If the input is a true current source, R1 and R2 are not used. Again, diode CR1 prevents latch-up by insuring Logic Common does not drop more than 500mV below $-V_S$. The clamp diode (MBD101) protects the AD654 input from "below $-V_S$" inputs.

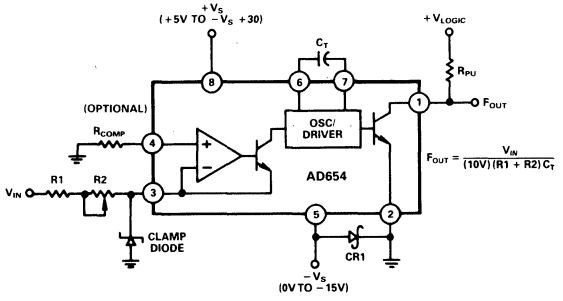


Figure 2. V-F Connections for Negative Input Voltages or Current

*Teflon is a trademark of E. I. Du Pont de Nemours & Co.

OFFSET CALIBRATION

In theory, two adjustments calibrate a V/F: scale and offset. In practice, most applications find the AD654's 1mV max voltage offset sufficiently low to forgo offset calibration. However, the input amplifier's 30nA (typ) bias currents will generate an offset due to the difference in DC source resistance between the input terminals. This offset can be substantial for large values of $R_T = R_1 + R_2$ and will vary as the bias currents drift over temperature. Therefore, to maintain the AD654's low offset, the application may require balancing the DC source resistances at the inputs (pins 3 and 4).

For positive inputs, this is accomplished by adding a compensation resistor nominally equal to R_T in series with the input as shown in Figure 3a. This limits the offset to the product of the 30nA bias current and the mismatch between the source resistance R_T and R_{COMP}. A second, smaller offset arises from the inputs' 5nA offset current flowing through the source resistance R_T or R_{COMP}. For negative input voltage and current connections, the compensation resistor is added at pin 4 as shown in Figure 3b in lieu of grounding the pin directly. For both positive and negative inputs, the use of R_{COMP} may lead to noise coupling at pin 4 and should therefore be bypassed for lowest noise operation.

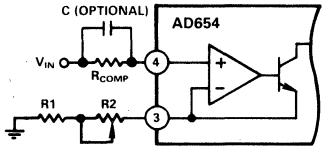


Figure 3a. Bias Current Compensation – Positive Inputs

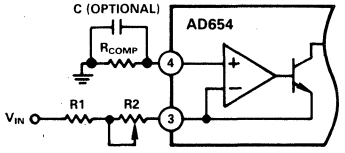


Figure 3b. Bias Current Compensation – Negative Inputs

If the AD654's 1mV offset voltage must be trimmed, the trim must be performed external to the device. Figure 3c shows an optional connection for positive inputs in which R_{OFF1} and R_{OFF2} add a variable resistance in series with R_T. A variable source of ±0.6V applied to R_{OFF1} then adjusts the offset ±1mV. Similarly, a ±0.6V variable source is applied to R_{OFF} in Figure 3d to trim offset for negative inputs. The ±0.6V bipolar source could simply be an AD589 reference connected as shown in Figure 3e.

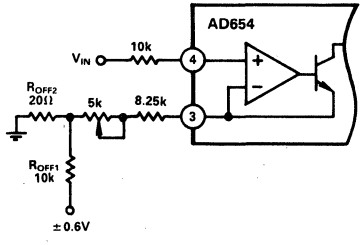


Figure 3c. Offset Trim Positive Input (10V FS)

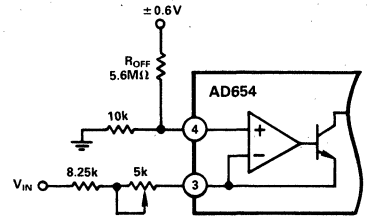


Figure 3d. Offset Trim Negative Input (– 10V FS)

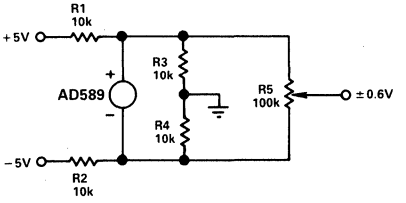


Figure 3e. Offset Trim Bias Network

FULL SCALE CALIBRATION

Full scale trim is the calibration of the circuit to produce the desired output frequency with a full scale input applied. In most cases this is accomplished by adjusting the scaling resistor R_T. Precise calibration of the AD654 requires the use of an accurate voltage standard set to the desired FS value and an accurate frequency meter. A scope is handy for monitoring output waveshape. Verification of converter linearity requires the use of a switchable voltage source or DAC having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. Since each AD654 is factory tested for linearity, it is unnecessary for the end-user to perform this tedious and time consuming test on a routine basis.

Sufficient FS calibration trim range must be provided to accommodate the worst-case sum of all major scaling errors. This includes the AD654's 10% full scale error, the tolerance of the fixed scaling resistor, and the tolerance of the timing capacitor. Therefore, with a resistor tolerance of 1% and a capacitor tolerance of 5%, the fixed part of the scaling resistor should be a maximum of 84% of nominal, with the variable portion selected to allow 116% of the nominal.

If the input is in the form of a negative current source, the scaling resistor is no longer required, eliminating the capability of trimming FS frequency in this fashion. Since it is usually not practical to smoothly vary the capacitance for trimming purposes, an alternative scheme such as the one shown in Figure 4 is needed. Designed for a FS of 1mA, this circuit divides the input into two current paths. One path is through the 100Ω

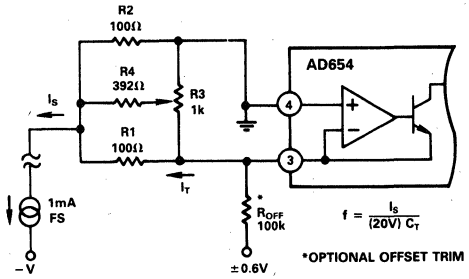


Figure 4. Current Source FS Trim

resistor R1, and flowing into pin 3; it constitutes the signal current I_T to be converted. The second path, through another 100Ω resistor R2, carries the same nominal current. Two equal valued resistors offer the best overall stability, and should be either 1% discrete film units, or a pair from a common array.

Since the 1mA FS input current is divided into two 500μA legs (one to ground and one to pin 3), the total input signal current (I_S) is divided by a factor of two in this network. To achieve the same conversion scale factor, C_T must be reduced by a factor of two. This results in a transfer unique to this hookup:

$$f = \frac{I_S}{(20V)\,C_T}$$

For calibration purposes, resistors R3 and R4 are added to the network, allowing a ±15% trim of scale factor with the values shown. By varying R4's value the trim range can be modified to accommodate wider tolerance components or perhaps the calibration tolerance on a current output transducer such as the AD592 temperature sensor. Although the values of R1 – R4 shown are valid for 1mA FS signals only, they can be scaled upward proportionately for lower FS currents. For instance, they should be increased by a factor of ten for a FS current of 100μA.

In addition to the offsets generated by the input amplifier's bias and offset currents, an offset voltage induced parasitic current arises from the current fork input network. These effects are minimized by using the bias current compensation resistor R_{OFF} and offset trim scheme shown in Figure 3e.

Although device warmup drifts are small, it is good practice to allow the devices operating environment to stabilize before trim, and insure the supply, source and load are appropriate. If provision is made to trim offset, begin by setting the input to 1/10,000 of full scale. Adjust the offset pot until the output is 1/10,000 of full scale (for example, 25Hz for a FS of 250kHz). This is most easily accomplished using a frequency meter connected to the output. The FS input should then be applied and the gain pot should be adjusted until the desired FS frequency is indicated.

INPUT PROTECTION

The AD654 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions. Thus $+V_{IN}$ and R_T pins should not be driven more than 300mV below $-V_S$. Likewise, Logic Common should not drop more than 500mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. In addition to the diode shown in Figures 1 and 2 protecting Logic Common, a second Schottky diode (MBD101) can protect the AD654's inputs from "below $-V_S$" inputs as shown in Figure 5. It is also desirable not to drive $+V_{IN}$ and R_T above $+V_S$. In operation, the converter will exhibit a zero output for inputs above ($+V_S$ – 3.5V). Also, control currents above 2mA will increase nonlinearity.

The AD654's 80dB dynamic range guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to input. For example, when scaled to accept an FS input of 1V, the −80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes

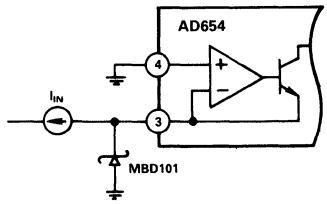


Figure 5. Input Protection

of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter or a guard ring around the R_T pin. The filter can be assembled using the bias current compensation resistor discussed in the previous section. For an FS of 10kHz, a single-pole filter with a time constant of 100ms will be suitable, but the optimum configuration will depend on the application and the type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA full integration of additive input noise occurs. Like the inputs, the capacitor terminals are sensitive to interference from other signals. The timing capacitor should be located as close as possible to the AD654 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in the system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD654. A proper ground scheme appears in Figure 6.

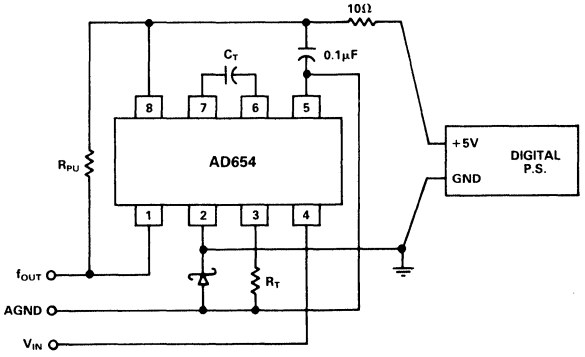


Figure 6. Proper Ground Scheme

OUTPUT INTERFACING CONSIDERATIONS

The output stage's design allows easy interfacing to all digital logic families. The output NPN transistor's emitter and collector are both uncommitted. The emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$, and the open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can sink over 10mA at a maximum saturation voltage of 0.4V. The stage limits the output current at 25mA and can handle this limit indefinitely without damaging the device.

NONLINEARITY SPECIFICATION

The preferred method of specifying nonlinearity error is in terms of maximum deviation from the ideal relationship after calibrating the converter at full scale. This error will vary with the full scale frequency and the mode of operation. The AD654 operates best at a 250kHz full scale frequency with a negative voltage input; the linearity is typically within 0.03%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicated in the Specifications Table. The shape of typical linearity plot is given in Figure 7.

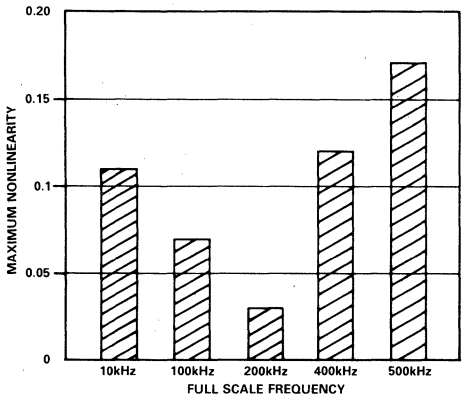


Figure 7. Typical Nonlinearities at Different Full-Scale Frequencies

TWO-WIRE TEMPERATURE-TO-FREQUENCY CONVERSION

Figure 8 shows the AD654 in a two-wire temperature-to-frequency conversion scheme. The twisted pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation.

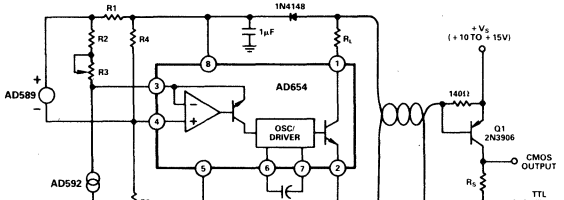


Figure 8. Two-Wire Temperature-to-Frequency Converter

The positive supply line is fed to the remote V/F through a 140Ω resistor. This resistor is selected such that the quiescent current of the AD654 will cause less than one V_{BE} to be dropped. As the V/F oscillates, additional switched current is drawn through R_L when pin 1 goes low. The peak level of this additional current causes Q1 to saturate, and thus regenerates the AD654's output square wave at the collector. The supply voltage to the AD654 then consists of a DC level, less the resistive line drop, plus a one V_{BE} p-p square wave at the output frequency of the AD654. This ripple is reduced by the diode/capacitor combination.

To set up the receiver circuit for a given voltage, the R_S and R_L resistances are selected as shown in Table I. CMOS logic stages can be driven directly from the collector of Q1, and a single TTL load can be driven from the junction of R5 and R6.

$+V_S$	R_S	R_L
10V	270Ω	1.8k
15V	680Ω	2.7k

Table I.

	$(+V_S)$	R1	R2	R3	R4	R5	
K	10V	–	–	–	100k	127k	F = 10Hz/K
	15V	–	–	–	100k	127k	
°C	10V	6.49k	4.02k	1k	95.3k	22.6k	F = 10Hz/°C
	15V	12.7k	4.02k	1k	78.7k	36.5k	
°F	10V	6.49k	4.42k	1k	154k	22.6k	F = 5.55Hz/°F
	15V	12.7k	4.42k	1k	105k	36.5k	

Table II.

At the V/F end, the AD592C temperature transducer is interfaced with the AD654 in such a manner that the AD654 output frequency is proportional to temperature. The output frequency can be scaled and offset from K to °C or °F using the resistor values shown in Table II. Since temperature is the parameter of interest, an NPO ceramic capacitor is used as the timing capacitor for low V/F TC.

When scaling per K, resistors R1 – R3 and the AD589 voltage reference are not used. The AD592 produces a 1μA/K current output which drives pin 3 of the AD654. With the timing capacitor of 0.01μF this produces an output frequency scaled to 10Hz/K. When scaling per °C and °F, the AD589 and resistors R1 – R3 offset the drive current at pin 3 by 273.2μA for scaling per °C and 255.42μA for scaling per °F. This will result in frequencies scaled at 10Hz/°C and 5.55Hz/°F, respectively.

OPTOISOLATOR COUPLING

A popular method of isolated signal coupling is via optoelectronic isolators, or optocouplers. In this type of device, the signal is coupled from an input LED to an output photo-transistor, with light as the connecting medium. This technique allows DC to be transmitted, is extremely useful in overcoming ground loop problems between equipment, and is applicable over a wide range of speeds and power.

Figure 9 shows a general purpose isolated V/F circuit using a low cost 4N37 optoisolator. A +5V power supply is assumed for both the isolated (+5V isolated) and local (+5V local) supplies. The input LED of the isolator is driven from the collector output of the AD654, with a 9mA current level established by R1 for high speed, as well as for a 100% current transfer ratio.

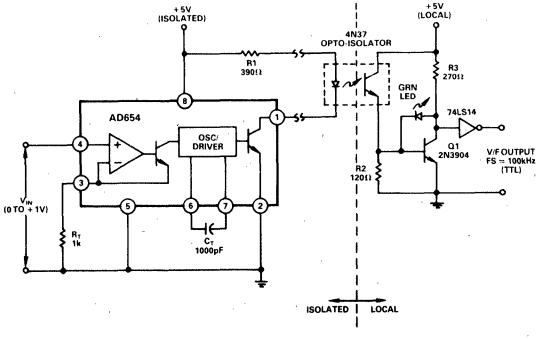


Figure 9. Optoisolator Interface

At the receiver side, the output transistor is operated in the photo-transistor mode; that is with the base lead (pin 6) open. This allows the highest possible output current. For reasonable speed in this mode, it is imperative that the load impedance be as low as possible. This is provided by the single transistor stage current-to-voltage converter, which has a dynamic load impedance of less than 10 ohms and interfaces with TTL at the output.

USING A STAND-ALONE FREQUENCY COUNTER/LED DISPLAY DRIVER FOR VOLTMETER APPLICATIONS

Figure 10 shows the AD654 used with a stand-alone frequency counter/LED display driver. With C_T = 1000pF and R_T = 1kΩ the AD654 produces an FS frequency of 100kHz when V_{IN} = +1V. This signal is fed into the ICM7226A, a universal counter system that drives common anode LED's. With the FUNCTION pin tied to D1 through a 10kΩ resistor the ICM7226A counts the frequency of the signal at A_{IN}. This count period is selected by the user and can be 10ms, 100ms, 1s, or 10 seconds, as shown on pin 21. The longer the period selected, the more resolution the count will have. The ICM7226A then displays the frequency on the LED's, driving them directly as shown. Refreshing of the LED's is handled automatically by the ICM7226. The entire circuit operates on a single +5V supply and gives a meter with 3, 4, or 5 digit resolution.

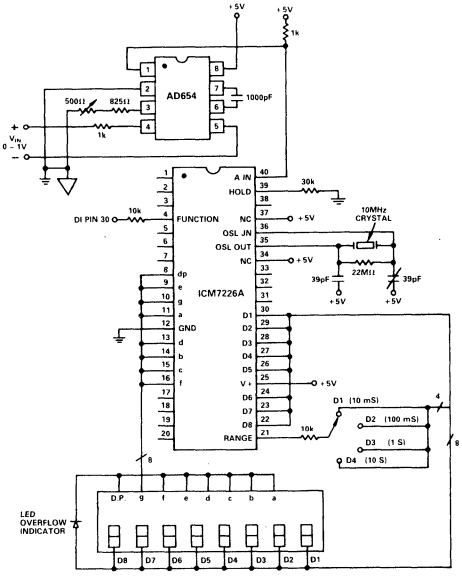


Figure 10. AD654 With Stand-Alone Frequency Counter/LED Display Driver

Longer count periods not only result in the count having more resolution, they also serve as an integration of noisy analog signals. For example, a normal-mode 60Hz sine wave riding on the input of the AD654 will result in the output frequency increasing on the positive half of the sine wave and decreasing on the negative half of the sine wave. This effect is cancelled by selecting a count period equal to an integral number of noise signal periods. A 100ms count period is effective because it not only has an integral number of 60Hz cycles (6), it also has an integral number of 50Hz cycles (5). This is also true of the 1 second and 10 second count period.

AD654-BASED ANALOG-TO-DIGITAL CONVERSION USING A SINGLE CHIP MICROCOMPUTER

The AD654 can serve as an analog-to-digital converter when used with a single component microcomputer that has an interval timer/event counter such as the 8048. Figure 11 shows the AD654, with a full scale input voltage of +1V and a full scale output frequency of 100kHz, connected to the timer/counter input pin T1 of the 8048. Such a system can also operate on a single +5V supply.

The 8748 counter is negative edge triggered; after the STRT CNT instruction is executed subsequent high to low transitions on T1 increment the counter. The maximum rate at which the counter may be incremented is once per three instruction cycles; using a 6MHz crystal, this corresponds to once every 7.5μs, or a maximum frequency of 133kHz. Because the counter overflows every 256 counts (8 bits), the timer interrupt is enabled. Each overflow then causes a jump to a subroutine where a register is incremented. After the STOP TCNT instruction is executed, the number of overflows that have occurred will be the number in this register. The number in this register multiplied by 256 plus the number in the counter will be the total number of negative edges counted during the count period. The count period is handled simply by decrementing a register the number of times necessary to correspond to the desired count time. After the register has been decremented the required number of times, the STOP TCNT instruction is executed.

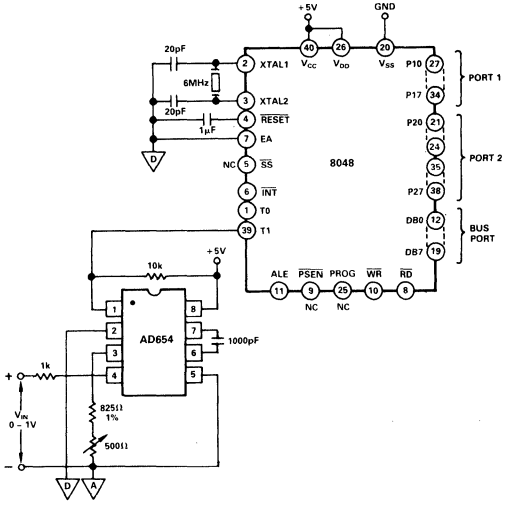


Figure 11. AD654 VFC as an ADC

The total number of negative edges counted during the count period is proportional to the input voltage. For example, if a 1V full-scale input voltage produces a 100kHz signal and the count period is 100ms, then the total count will be 10,000. Scaling from this maximum is then used to determine the input voltage, i.e., a count of 5000 corresponds to an input voltage of 0.5V. As with the ICM7226, longer count times result in counts having more resolution; and they result in the integration of noisy analog signals.

FREQUENCY DOUBLING

Since the AD654's output is a square-wave rather than a pulse train, information about the input signal is carried on both halves of the output waveform. The circuit in Figure 12 converts the output into a pulse train, effectively doubling the output frequency, while preserving the better low frequency linearity of the AD654. This circuit also accommodates an input voltage that is greater than the AD654 supply voltage.

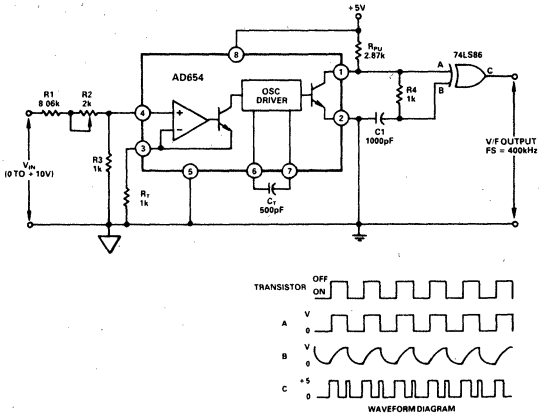


Figure 12. Frequency Doubler

Resistors R1 – R3 are used to scale the 0 to +10V input voltage down to 0 to +1V as seen at pin 4 of the AD654. Recall that V_{IN} must be less than V_{SUPPLY} −4V, or in this case less than 1V. The timing resistor and capacitor are selected such that this 0 to +1V signal seen at pin 4 results in a 0 to 200kHz output frequency.

The use of R4, C1 and the XOR gate doubles this 200kHz output frequency to 400kHz. The AD654 output transistor is basically used as a switch, switching capacitor C1 between a charging mode and a discharging mode of operation. The voltages seen at the input of the 74LS86 are shown in the waveform diagram. Due to the difference in the charge and discharge time constants, the output pulse widths of the 74LS86 are not equal. The output pulse is wider when the capacitor is charging due to its longer rise time than fall time. The pulses should therefore be counted on their rising, rather than falling, edges.

OPERATION AT HIGHER OUTPUT FREQUENCIES

Operation of the AD654 via the conventional output (pins 1 and 2) is speed limited to approximately 500kHz for reasons of TTL logic compatibility. Although the output stage may become speed limited, the multivibrator core itself is able to oscillate to 1MHz or more. The designer may take advantage of this feature in order to operate the device at frequencies in excess of 500kHz.

Figure 13 illustrates this with a circuit offering 2MHz full scale. In this circuit the AD654 is operated at a full scale (FS) of 1mA, with a C_T of 100pF. This achieves a basic device FS frequency of 1MHz across C_T. The P channel JFETs, Q1 and Q2, buffer the differential timing capacitor waveforms to a low impedance level where the push-pull signal is then AC coupled to the high speed comparator A2. Hysteresis is used, via R7, for non-ambiguous switching and to eliminate the oscillations which would otherwise occur at low frequencies.

The net result of this is a very high-speed circuit which does not compromise the AD654 dynamic range. This is a result of the FET buffers typically having only a few pA of bias current. The high end dynamic range is limited, however, by parasitic package and layout capacitances in shunt with C_T, as well as those from each node to AC ground. Minimizing the lead length between A2–6/A2–7 and Q1/Q2 in PC layout will help. A ground plane will also help stability. Figure 14 shows the waveforms V1 – V4 found at the respective points shown in Figure 13.

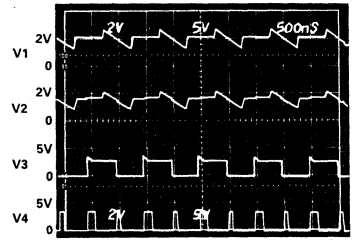


Figure 14. Waveforms of 2MHz Frequency Doubler

The output of the comparator is a complementary square wave at 1MHz FS. Unlike pulse train output V/F converters, each half-cycle of the AD654 output conveys information about the input. Thus it is possible to count edges, rather than full cycles of the output, and double the effective output frequency. The XOR gate following A2 acts as an edge detector producing a short pulse for each input state transition. This effectively doubles the V/F FS frequency to 2MHz. The final result is a 1V full scale input V/F with a 2MHz full-scale output capability; typical nonlinearity is 0.5%.

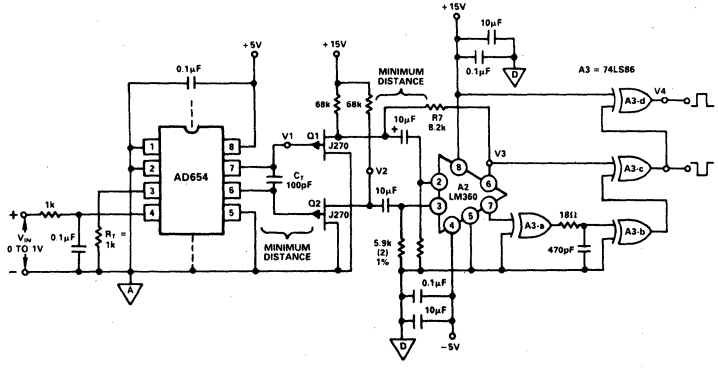


Figure 13. 2MHz, Frequency Doubling V/F

ANALOG DEVICES

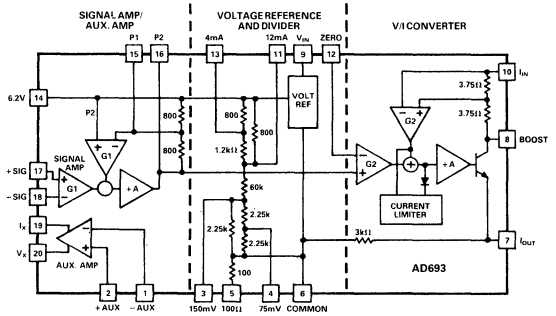
4-20mA Sensor Transmitter

AD693

FEATURES

- **Loop-Powered Operation**
- **Precalibrated 30mV or 60mV Input Spans**
- **Precalibrated 100Ω RTD Interface**
- **Independently Adjustable Output Span and Zero**
- **Precalibrated Output Spans: 4-20mA Unipolar**
  0-20mA Unipolar
  12 ± 8mA Bipolar
- **6.2V Reference with Max 3.5mA Current Output**
- **Uncommitted Auxiliary Amp for Extra Flexibility**
- **Optional External Pass Transistor to Reduce Self-Heating Errors**

AD693 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD693 is a monolithic signal conditioning circuit which accepts low-level inputs from a variety of transducers to control a 4-20mA, 2-wire current loop. An on-chip reference and auxiliary amplifier are provided for transducer excitation; up to 3.5mA of excitation current is available when the device is operated in the loop-powered mode. Alternatively, the device may be locally powered for 3-wire applications when 0-20mA operation is desired.

Input spans precalibrated for 0-30mV and 0-60mV, may be set by simple pin strapping; other spans may be realized with the addition of an external resistor. The auxiliary amplifier may be used in combination with on-chip voltages to provide six precalibrated ranges for 100Ω RTDs. Output span and zero are also determined by pin strapping to obtain the standard ranges: 4-20mA, 12 ± 8mA and 0-20mA.

Active laser trimming of the on-chip thin film resistors result in high levels of accuracy without the need for additional adjustments and calibration. The AD693 also allows for the use of an external pass transistor to further reduce errors caused by self-heating.

Transmission of analog data over a 4-20mA 2-wire current loop offers advantages over other techniques: 1) immunity both to voltage drops over long distances and high electrical noise often encountered in harsh industrial environments and 2) no ambiguity between a "zero" and open circuit condition. Where this data represents low-level signals from a variety of transducers, such as RTD's, bridges, and pressure transducers, the monolithic AD693 offers the most cost-effective signal conditioning solution. For these reasons, the device is recommended for a variety of applications in process control, factory automation and system monitoring.

The AD693 is packaged in a 20-pin hermetic DIP and specified over the −40°C to +85°C industrial temperature range.

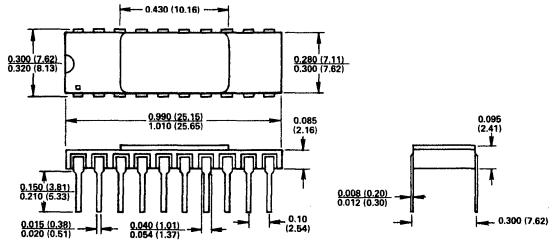
PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

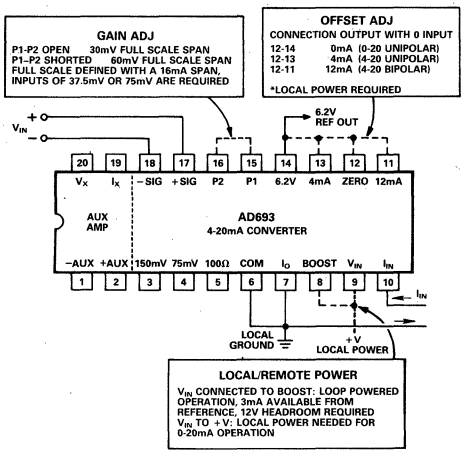
1. The AD693 is a complete monolithic voltage-to-current signal conditioner.
2. Flexible output spans derived from zero scale options include 4-20mA, 0-20mA, and 12 ± 8mA in two and three wire configurations.
3. Simple resistor programming adds a continuum of ranges to the basic 30 and 60mV input spans.
4. The common mode range of the instrumentation amplifier input extends from below "ground" to beyond the positive reference voltage.
5. Provisions for transducer excitation includes a 6.2V reference output and an auxiliary amplifier which may be configured for voltage or current output as well as signal amplification.
6. The circuit configuration permits simple linearization of bridge, RTD, and other transducer signals.
7. The chip provides a monitored output to drive an external pass transistor. This feature offloads power dissipation to extend the temperature range of operation and to minimize self-heating errors.
8. Laser trimming at the wafer stage results in low unadjusted errors and affords precalibrated input and output spans.

OUTLINE DIMENSIONS

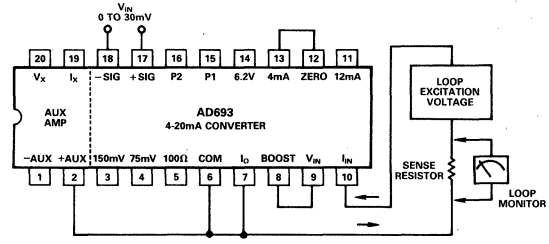
Dimensions shown in inches and (mm).



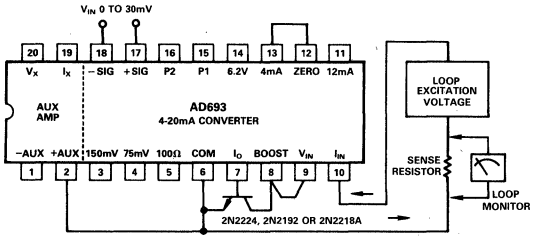
APPLICATION/CONNECTION INFORMATION



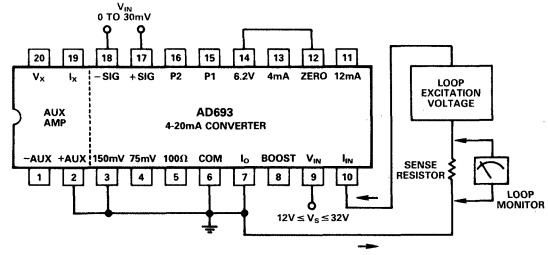
AD693 Features via Pin-Strapping



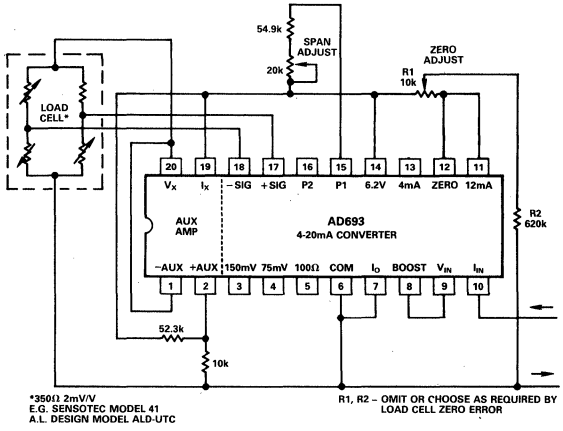
Minimal Connection for 0-30mV Unipolar Input, 4-20mA Output



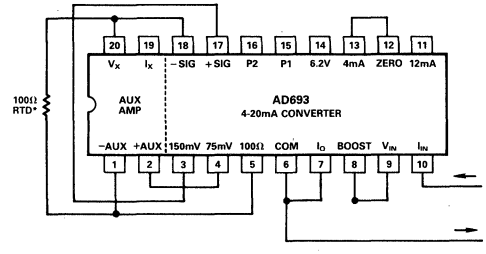
Using an External Pass Transistor to Minimize Self-Heating Errors



Local-Powered Operation with 0-37.5mV Unipolar Input and 0-20mA Output



Utilizing the Aux Amp to Drive a Load Cell



ZERO PIN CONNECTION (PIN 12)

INPUT SPAN	6.2V (PIN 14)	4mA (PIN 13)	12mA (PIN 11)
30mV (PINS 15-16 –OPEN)	25.9°C → 130.5°C	0 → 103.9°C	–50.8°C → 51.6°C
60mV PINS 15-16 JOINED)	51.6°C → 266.4°C	0 → 211.3°C	–100.6°C → 103.9°C

*α = 0.00385

Direct RTD to 4-20mA Interface

ANALOG DEVICES

Low Cost, High-Speed BIFET Op Amp

AD711

FEATURES

Improved Replacement for LF411

AC PERFORMANCE:
- **Settles to 0.01% in 1μs**
- **Slew Rate (Unity Gain): 18V/μs min (AD711K)**
- **Small Signal Bandwidth: 4MHz**

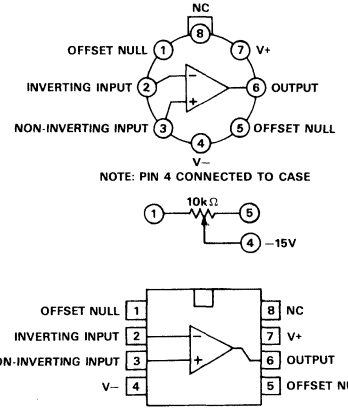
DC PERFORMANCE:
- **Low Offset Voltage: 0.25mV max (AD711C)**
- **Low Offset Voltage Drift: 5μV/°C max (AD711C)**
- **Low Bias Current: 25pA max (AD711C)**
- **High Open Loop Gain: 100,000 V/V (100dB) min**
- **Low Noise: 3μV p-p, 0.1Hz to 10Hz max (AD711C)**

AVAILABLE IN PLASTIC, HERMETIC CERDIP AND HERMETIC HEADER PACKAGES

MIL-STD-883B and PLUS Parts Available

Dual Version Available: AD712

AD711 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD711 is a high-speed, precision monolithic FET-input operational amplifier combining Analog's expertise in precision op amp design and laser wafer trimming technology. The AD711's high-speed, very low offset voltage and drift and low noise allow designers to easily upgrade existing designs using older precision BIFETs and, in many cases, bipolar op amps.

This low cost op amp offers excellent ac and dc performance. With a slew rate of 18V/μs and a settling time of 1μs to 0.01%, the AD711 is ideal as a buffer for 12-bit D/A and A/D Converters and as a high-speed integrator. The AD711's settling time is unmatched by any similar IC amplifier. The combination of excellent noise performance and low input current also make it useful for photo diode preamps. The device's CMRR of 80dB and open loop gain of 100,000V/V (100dB) ensure 12-bit performance even in high-speed unity gain buffer circuits.

Devices are pinned out in a standard op amp configuration and are available in six performance grades. The AD711J and AD711K are rated over the commercial temperature range of 0 to +70°C. The AD711A, AD711B and AD711C are rated over the industrial temperature range of −40°C to +85°C. The AD711S is specified over the military temperature range of −55°C to +125°C; and is available processed to MIL-STD-883B, Rev C. Devices are available in an 8-pin CERDIP, Plastic Mini-DIP or a TO-99 Metal Can.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. Analog Devices' advanced processing technology and 100% testing guarantees a low input offset voltage (0.50mV max, C grade, 3.0mV max, A grade). Offset voltage is specified in the warmed-up condition. Analog Devices' proprietary laser wafer drift trimming process reduces offset voltage drifts to 5μV/°C max on the AD712C.
2. Along with precision dc performance, the AD712 offers excellent dynamic response. It settles to 0.01% in 1μs and has a guaranteed and 100% tested minimum slew rate of 18V/μs, making this device ideal for applications requiring a combination of superior ac and dc performance, such as DAC buffers.
3. Guaranteed and tested maximum voltage noise of 3μV p-p, 0.1 to 10Hz (AD712C) enhances AD712's performance as a dual precision op amp.
4. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD712C) and input offset current of 10pA max (AD712C). Input bias current and input offset current are guaranteed with the devices fully warmed-up at an ambient temperature of 25°C.
5. The AD712 offers excellent overall performance at very competitive prices. It may be used as an automatic upgrade or alternate source for all grades of the LF412.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD711J/A/S Min	AD711J/A/S Typ	AD711J/A/S Max	AD711K/B Min	AD711K/B Typ	AD711K/B Max	AD711C Min	AD711C Typ	AD711C Max	Units
OPEN LOOP GAIN[1]										
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**100,000**			**100,000**			**100,000**			V/V
T_A = min to max $R_L \geq 2k\Omega$	**100,000**			**100,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$ T_{min} to T_{max}	±11	±13		±11	±13		±11	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain Small Signal		4			4			4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%		1			1			1		µs
Total Harmonic Distortion f = 1kHz $R_L \geq 2k\Omega$, V_O = 3V rms		0.0025			0.0025			0.0025		%
INPUT OFFSET VOLTAGE[2]										
Initial Offset			**2.0**			**0.5**			**0.25**	mV
Input Offset Voltage Over Temp			4.0			**2.0**			**1.0**	mV
Input Offset Voltage vs. Temp			20			**10**			5	µV/°C
Input Offset Voltage vs. Supply	**74**			**76**			**80**			dB
T_{min} to T_{max}	74			**76**			**80**			dB
INPUT BIAS CURRENT[3]										
Either Input, V_{CM} = 0		25	**50**		20	**50**		20	**25**	pA
Either Input, V_{CM} + 10V to − 10V			100			100			50	pA
Input Offset Current		10	**25**		5	**25**		5	**10**	pA
INPUT IMPEDANCE										
Differential		$10^{12}\|\|6$			$10^{12}\|\|6$			$10^{12}\|\|6$		Ω||pF
INPUT VOLTAGE RANGE[4]										
Differential		±20			±20			±20		V
Common-Mode Voltage Over Max Operating Range	$-V_S+4V$		$+V_S-4V$	$-V_S+4V$		$+4_S-4V$	$-V_S+4V$		$+V_S-4V$	V
Common-Mode Rejection, V_{IN} = >10V, T_{min} to T_{max}	**74**			**76**			**80**			dB
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		1.5			1.5			1.5	**3.0**	µV p-p
f = 10Hz		35			35			35		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
EQUIVALENT INPUT NOISE CURRENT @ f = 1kHz		0.01			0.01			0.01		pA/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		2.5	**3.4**		2.5	**3.0**		2.5	**2.8**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD711J			AD711K					
Industrial (−40°C to +85°C)		AD711A			AD711B					
Military (−55°C to +125°C)		AD711S						AD711C		
STORAGE	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS	J: Plastic (AD712JN) N8A A: Cerdip (AD712AQ) Q8A Header (AD712AH) HO8B S: Cerdip (AD712SQ) Q8A Header (AD712SH) HO8B			K: Plastic (AD712KN) N8A B: Cerdip (AD712BQ) Q8A Header (AD712BH) HO8B			C: Cerdip (AD712CQ) Q8A Header (AD712CH) HO8B			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ANALOG DEVICES

High-Speed Precision Dual BIFET Op Amp

AD712

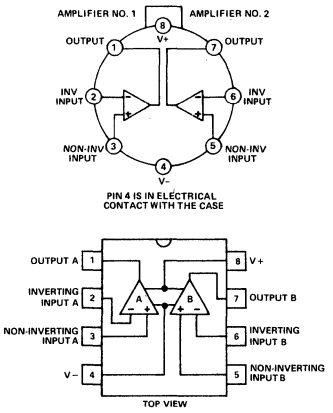
FEATURES
Improved Replacement for LF412

AC PERFORMANCE:
- **Settles to 0.01% in 1μs**
- **Slew Rate (Unity Gain): 18V/μs min (AD712K)**
- **Small Signal Bandwidth: 4MHz**

DC PERFORMANCE:
- **Low Offset Voltage: 0.5mV max (AD712C)**
- **Low Offset Voltage Drift: 5μV/°C max (AD712C)**
- **Low Bias Current: 25pA max (AD712C)**
- **High Open Loop Gain: 100,000 V/V (100dB) min**
- **Low Noise: 3μV p-p, 0.1Hz to 10Hz max (AD712C)**

AVAILABLE IN PLASTIC, HERMETIC CERDIP AND HERMETIC HEADER PACKAGES
MIL-STD-883B and PLUS Parts Available

AD712 PIN CONFIGURATION



3

PRODUCT DESCRIPTION

The AD712 is a high-speed, dual precision monolithic FET-input operational amplifier combining Analog's expertise in precision op amp design and laser wafer trimming technology. The AD712's high-speed, very low offset voltage and drift and low noise allow designers to easily upgrade existing designs using older precision BIFETs and, in many cases, bipolar op amps.

This low cost op amp offers excellent ac and dc performance. With a slew rate of 18V/μs and a settling time of 1μs to 0.01%, the AD712 is ideal as buffers for 12-bit D/A and A/D Converters and as high-speed integrators. The AD712's settling time is unmatched by any similar IC amplifier. The combination of excellent noise performance and low input current also make it useful for photo diode preamps. The device's CMRR of 80dB and open loop gain of 100,000V/V (100dB) ensure 12-bit performance even in high-speed unity gain buffer circuits.

Devices are pinned out in a standard op amp configuration and are available in six performance grades. The AD712J and AD712K are rated over the commercial temperature range of 0 to +70°C. The AD712A, AD712B and AD712C are rated over the industrial temperature range of −40°C to +85°C. AD712S is specified over the military temperature range of −55°C to +125°C; and is available processed to MIL-STD-883B, Rev C. Devices are available in an 8-pin CERDIP, Plastic Mini-DIP or a TO-99 Metal Can.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. Analog Devices' advanced processing technology and 100% testing guarantees a low input offset voltage (0.25mV max, C grade, 2.0mV max, A grade). Offset voltage is specified in the warmed-up condition. Analog Devices' proprietary laser wafer drift trimming process reduces offset voltage drifts to 5μV/°C max on the AD711C.
2. Along with precision dc performance, the AD711 offers excellent dynamic response. It settles to 0.01% in 1μs and has a guaranteed and 100% tested minimum slew rate of 18V/μs, making this device ideal for applications requiring a combination of superior ac and dc performance, such as DAC buffers.
3. Guaranteed and tested maximum voltage noise of 3μV p-p, 0.1 to 10Hz (AD711C) enhances AD711's performance in low noise applications.
4. Analog Devices' well-matched, ion-implanted JFETs ensure a guaranteed input bias current (at either input) of 25pA max (AD711C) and input offset current of 10pA max (AD711C). Input bias current and input offset current are guaranteed with the devices fully warmed-up at an ambient temperature of 25°C.
5. The AD711 offers excellent overall performance at very competitive prices. It may be used as an automatic upgrade or alternate source for all grades of the LF411.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD712J/A/S Min	AD712J/A/S Typ	AD712J/A/S Max	AD712K/B Min	AD712K/B Typ	AD712K/B Max	AD712C Min	AD712C Typ	AD712C Max	Units
OPEN LOOP GAIN[1]										
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	**100,000**			**100,000**			**100,000**			V/V
T_A = min to max $R_L \geq 2k\Omega$	**100,000**			**100,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ $R_L \geq 2k\Omega$ T_{min} to T_{max}	±11	±13		±11	±13		±11	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain Small Signal		4			4			4		MHz
Full Power Response		200			200			200		kHz
Slew Rate, Unity Gain	**16**	20		**18**	20		**18**	20		V/µs
Settling Time to 0.01%		1			1			1		µs
Total Harmonic Distortion f = 1kHz										
$R_L \geq 2k\Omega$, V_O = 3V rms		0.0025			0.0025			0.0025		%
INPUT OFFSET VOLTAGE[2]										
Initial Offset			**3.0**			**1.0**			**0.5**	mV
Input Offset Voltage Over Temp			4.0			**2.0**			**1.0**	mV
Input Offset Voltage vs. Temp			20			**10**			5	µV/°C
Input Offset Voltage vs. Supply	**74**			**76**			**80**			dB
T_{min} to T_{max}	74			**76**			**80**			dB
INPUT BIAS CURRENT[3]										
Either Input, V_{CM} = 0		25	**50**		20	**50**		20	**25**	pA
Either Input, V_{CM} + 10V to − 10V			100			100			50	pA
Input Offset Current		10	**25**		5	**25**		5	**10**	pA
INPUT IMPEDANCE										
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		Ω‖pF
INPUT VOLTAGE RANGE[4]										
Differential		±20			±20			±20		V
Common-Mode Voltage										
Over Max Operating Range	$-V_S+4V$		$+V_S-4V$	$-V_S+4V$		$+4_S-4V$	$-V_S+4V$		$+V_S-4V$	V
Common-Mode Rejection,										
V_{IN} = >10V	**74**			**76**			**80**			dB
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		1.5			1.5			1.5	**3.0**	µV p-p
f = 10Hz		35			35			35		nV/√Hz
f = 100Hz		22			22			22		nV/√Hz
f = 1kHz		18			18			18		nV/√Hz
f = 10kHz		16			16			16		nV/√Hz
EQUIVALENT INPUT NOISE CURRENT @ f = 1kHz		0.01			0.01			0.01		pA/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating Range	**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
Quiescent Current		2.5	**6.8**		2.5	**6.0**		2.5	**5.6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance										
Commercial (0 to +70°C)		AD712J			AD712K					
Industrial (−40°C to +85°C)		AD712A			AD712B			AD712C		
Military (−55°C to +125°C)		AD712S								
STORAGE	−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS	J: Plastic (AD712JN) N8A A: Cerdip (AD712AQ) Q8A Header (AD712AH) HO8B S: Cerdip (AD712SQ) Q8A Header (AD712SH) HO8B			K: Plastic (AD712KN) N8A B: Cerdip (AD712BQ) Q8A Header (AD712BH) HO8B			C: Cerdip (AD712CQ) Q8A Header (AD712CH) HO8B			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

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Microprocessor – Compatible 16-Bit D/A Converter

AD1147/AD1148

FEATURES

Low Nonlinearity
- **Differential: ±0.00076% max**
- **Integral: ±0.00076% max**
- **Differential TC: ±1ppm/°C max**

Fast Settling
- **Full Scale: 18μs to ±0.00076%**
- **LSB: 3μs to ±0.00076%**

Low Power: 375mW Including Reference

Functionally Complete
- **Internal Reference, Output Voltage Amplifier, Input Latches and 8-Bit Latched Input DACs for Offset and Gain Correction.**

Full Four Quadrant Multiplying

Low Cost

APPLICATIONS

Automatic Test Equipment

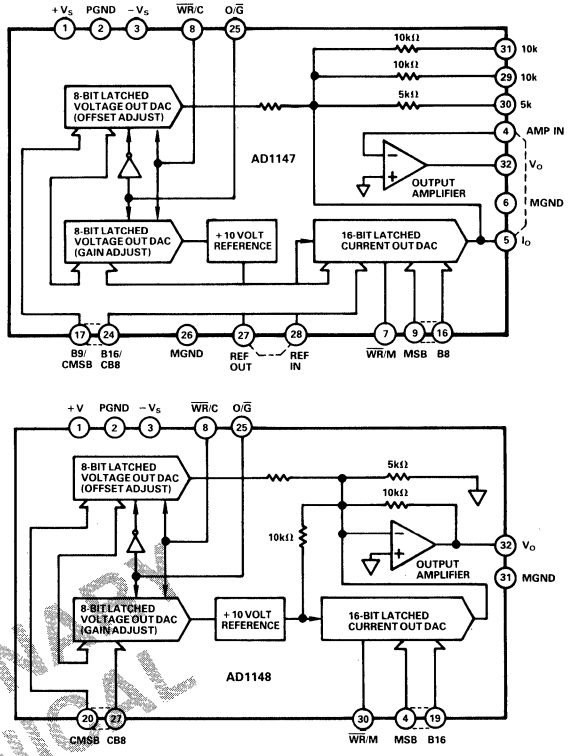
Scientific Instrumentation

Beam Positioners

Robotics

Graphics Displays

AD1147 and AD1148 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD1147 and AD1148 are 16-bit resolution, hybrid, latched input, digital-to-analog converters. Their two 8-bit latched input DACs allow direct offset and gain correction via microprocessor interface.

The AD1147 and AD1148 are constructed as hybrids in a compact 32-pin, triple wide dual-in-line package. Precision CMOS switches and a laser-trimmed thin-film resistor network are used to provide 16-bit accuracy and excellent temperature stability.

The Main (16-bit) DAC is loaded as a 16-bit word. The offset and gain correction DACs are each loaded as 8-bit words. The AD1147 multiplexes both correction DACs' inputs with the Main DAC's eight LSBs. This pin sharing allows for additional pin connections providing: external reference input, a current output and feedback resistors for voltage output ranges of 0 to +5V, 0 to +10V, +5V and +10V.

The AD1148 correction DACs' inputs are separate from the Main DAC's. The gain correction DAC's inputs are multiplexed with the offset DAC's 8-bit inputs. This allows for a separate 8-bit bus interface with the correction DACs – common in applications such as Automatic Test Equipment.

PRELIMINARY TECHNICAL DATA

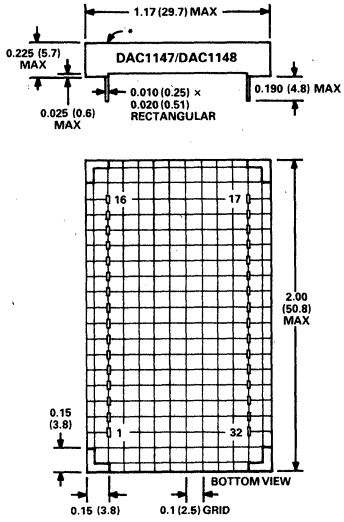
SPECIFICATIONS (typical @ +25°C and rated supplies unless otherwise specified)

MODEL	AD1147	AD1148
RESOLUTION	16 Bits	*
ACCURACY		
Integral Nonlinearity	±0.00076% FSR[1] (max)	±0.00076% FSR[1] (typ)
Differential Nonlinearity	±0.00076% FSR[1] (max)	±0.00076% FSR[1] (typ)
Monotonic (16 Bits)	Guaranteed	*
Offset	Adjustable to Zero	*
Gain	Adjustable to Full Scale	*
STABILITY		
Differential Nonlinearity	±1ppm/°C (max)	*
Offset	±20μV/°C (max)	**
Bipolar Offset	±6ppm/°C (max)	*
Gain (Includes Int. Ref.)	±10ppm/°C (max)	*
REFERENCE VOLTAGE		
Output Voltage	+10.00V, ±0.3% (max)	**
Output Current	2mA (max)	**
Ext. Ref Voltage Range[2]	−12V to +12V	**
Input Resistance	12kΩ	**
DYNAMIC PERFORMANCE		
Settling Time to ±0.00076%		
Voltage, Full-Scale Step	20μs	*
Voltage, LSB Step	3μs	*
Current	2μs	**
DIGITAL INPUT CODES	5 Volt CMOS/TTL Compatible	
Main DAC		
Unipolar	Binary (BIN)	**
Bipolar	Offset Binary (OBN)	*
Correction DACs	Binary (BIN)	*
ANALOG OUTPUT		
Voltage	+5V, +10V, ±5V, ±10V	±10V
Current	−2mA, ±1mA	**
Voltage Compliance	±500mV	**
Noise (100kHz BW)	60μV rms	*
POWER REQUIREMENTS		
Voltage (Rated Performance)	±15V (±5%)	*
Voltage (Operating)	±12.5V to ±17V	*
Supply Current Drain	±15mA (max)	*
Total Power @V_S = ±15V	375mW	*
POWER SUPPLY SENSITIVITY		
Offset	±10ppm/V	*
Gain	±10ppm/V	*
OFFSET ADJUSTMENT		
Range	±0.05% FSR	*
Resolution (@±10V)	1/4LSB	*
GAIN ADJUSTMENT		
Range (Unipolar/Bipolar)	±0.2% FSR[1]/±0.1% FSR[1]	NA/*
Resolution (Unipolar/Bipolar)	1LSB/1/2LSB	NA/*
TEMPERATURE RANGE		
Rated Performance	−25°C to +85°C	*
Storage Temperature	−40°C to +100°C	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*
SIZE	2.00" × 1.17" × 0.225" (all maximums) (50.8 × 29.7 × 5.7mm)	

NOTES
*Specifications same as AD1147.
**AD1148 does not provide pin connections to current output, reference input, reference output or the internal feedback resistors. Output voltage range is fixed at ±10V.
[1]FSR means Full-Scale Range.
[2]Rated performance is specified with +10V reference.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



* PIN 1 LOCATION IS IDENTIFIED BY A WHITE DOT ON THE TOP SURFACE.

AD1147 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$+V_S$	32	V_O
2	PGND	31	10k
3	$-V_S$	30	5k
4	AMP IN	29	10k
5	I_O	28	REF IN
6	MGND	27	REF OUT
7	$\overline{WR}$/M	26	MGND
8	$\overline{WR}$/C	25	O/$\overline{G}$
9	MSB	24	B16/CB8
10	B2	23	B15/CB7
11	B3	22	B14/CB6
12	B4	21	B13/CB5
13	B5	20	B12/CB4
14	B6	19	B11/CB3
15	B7	18	B10/CB2
16	B8	17	B9/CMSB

AD1148 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	$+V_S$	32	V_O
2	PGND	31	MGND
3	$-V_S$	30	$\overline{WR}$/M
4	MSB	29	$\overline{WR}$/C
5	B2	28	O/$\overline{G}$
6	B3	27	CB8
7	B4	26	CB7
8	B5	25	CB6
9	B6	24	CB5
10	B7	23	CB4
11	B8	22	CB3
12	B9	21	CB2
13	B10	20	CMSB
14	B11	19	B16
15	B12	18	B15
16	B13	17	B14

ANALOG OUTPUT RANGE

The AD1148 is internally connected for ±10 volts output range.

The AD1147 is pin programmable to provide a variety of analog outputs, either current or voltage. A unipolar output current of 0 to −2mA is available at pin 5, and can be offset by 1mA (by connecting pin 28 to pin 29) for a bipolar output of ±1mA. Output voltage ranges (+5V, +10V, ±5V and ±10V) are available at pin 32 by connecting the current output (pin 5) to the amplifier input (pin 4) and the appropriate internal feedback resistors to the amplifier output (pin 32) as shown in Figure 1.

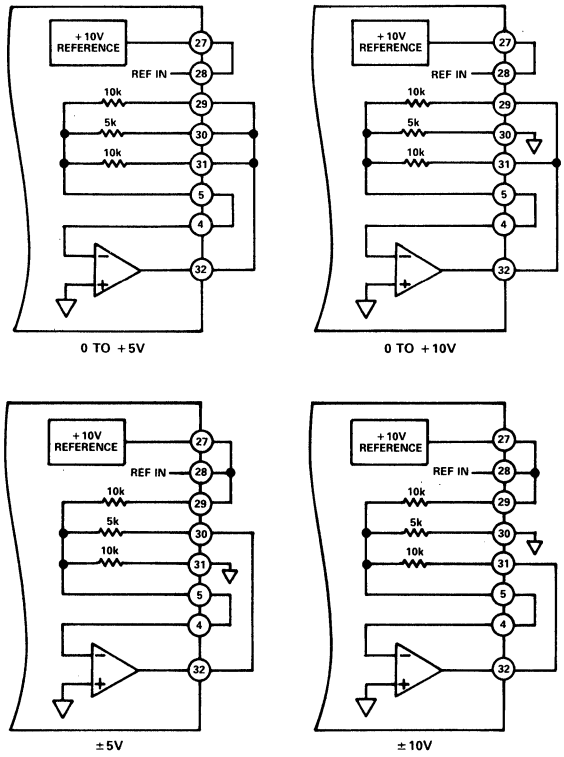


Figure 1. AD1147 Analog Output Range Pin Programming

TIMING DIAGRAM

The timing requirements for the models AD1147 and AD1148 are shown in Table I. The timing diagrams for the MAIN 16-bit DAC and the 8-bit Correction DACs are shown in Figure 2. The three control lines operate as follows:

$\overline{WR}$/M is the write line for the main DAC. The latches are transparent when the write line is low, and latched when the write line goes high.

$\overline{WR}$/C is the write line for the correction DACs. Operation is the same as above.

O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC. A high level on this pin selects the offset DAC. A low level selects the gain DAC.

SYMBOL	PARAMETER	REQUIREMENT
Main DAC		
t_{DS}	Data Setup Time	140ns min
t_{DH}	Data Hold Time	10ns min
t_{WR}	Write Pulse Width	250ns min
Correction DACs		
t_{CS}	O/$\overline{G}$ To Write Setup Time	200ns min
t_{CH}	O/$\overline{G}$ To Write Hold Time	20ns min
t_{DS}	Data Valid To Write Setup Time	110ns min
t_{DH}	Data Valid To Write Hold	0ns min
t_{WR}	Write Pulse Width	100ns min

Table I. Timing Requirements

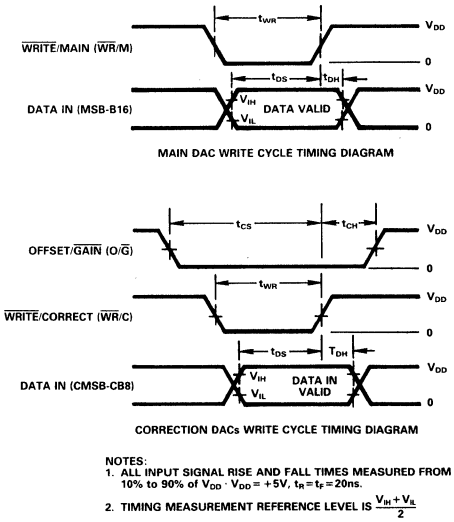


Figure 2. AD1147 and AD1148 Timing Diagrams

OFFSET AND GAIN CALIBRATION

Initial offset and gain errors can be adjusted to zero using the two internal 8-bit calibration DAC's. There are three control lines used in the calibration sequence: $\overline{WR}$/M is the write line for the Main (16-bit) DAC – the latches are transparent when the write line is low, and latched when the write line goes high; $\overline{WR}$/C is the write line for the correction DACs and operates the same as $\overline{WR}$/M; O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC – a high level on this pin selects the offset DAC and a low level selects the gain DAC.

Offset and Gain calibrations are performed as follows:

1. With $\overline{WR}$/M low, set the digital inputs of the Main DAC to "000....00" (in unipolar mode) or "100....00" (in bipolar mode).
2. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
3. With $\overline{WR}$/C low and O/$\overline{G}$ high, adjust the digital inputs of the offset correction DAC until the Main DAC's output

voltage (pin V_O) is as close to 0.000000 volts as possible. Note that incrementing the digital input produces a more negative voltage output.

4. Set $\overline{WR}$/C high to latch the digital input into the offset correction DAC.
5. With $\overline{WR}$/M low, set the digital input of the Main DAC to "111....11".
6. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
7. With $\overline{WR}$/C low and O/$\overline{G}$ low, adjust the digital inputs of the gain correction DAC until the Main DAC's output voltage (pin V_O) is as close as possible to the positive full-scale voltage shown below in Table II. Note that incrementing the digital input produces a more negative voltage output.
8. Set $\overline{WR}$/C high to latch the digital input into the gain correction DAC.
9. Calibration is complete. Set $\overline{WR}$/M low and begin/resume normal digital-to-analog conversion via the Main DAC.

Output Voltage Range	Positive Full-Scale Voltage
0 to +5 volts	+4.999924 volts
0 to +10 volts	+9.999847 volts
±5 volts	+4.999847 volts
±10 volts	+9.999695 volts

Table II. Gain Calibration

GROUNDING AND GUARDING

The current from the measurement ground pin (MGND) is constant, independent of digital input, for ease of making measurements. This is the high quality ground for the AD1147 and AD1148. It should be connected to the high quality ground in the application. Power ground (PGND) should be connected to measurement ground (MGND) at the measurement point.

The current output pin (I_O) of the AD1147 is sensitive to interference from the digital input lines. It should be surrounded by a grounded guard at all times. When using the AD1147 in the voltage output mode, both the "I_O" and "AMP IN" pins should be guarded (see Figure 3).

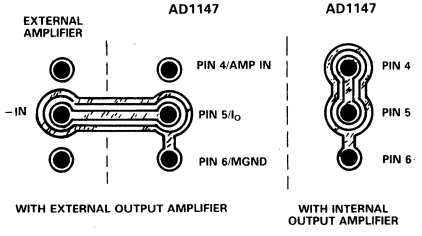


Figure 3. Typical Guarding Techniques

EXTERNAL AMPLIFIER FOR LOW DRIFT VOLTAGE OUTPUT OR HIGH OUTPUT CURRENT

The internal output amplifier of the AD1147 is designed for high-speed applications that require fast settling times. An external precision operational amplifier like the AD OP-07C can be applied when lower offset (less than 20μV/°C) is important (see Figure 4). Simply connect the current output (Pin 5) to the inverting input of the amplifier and connect the proper feedback resistors as shown in Figure 1. Be certain to keep the current output-amplifier's input connection short and surrounded by a grounded guard. To avoid degrading the gain drift performance of the DAC, always use the internal feedback resistors, since they are matched to the internal current weighting resistors of the DAC. It is also good practice to connect the negative input (Pin 4, AMP IN) of the unused internal output amplifier to its output (Pin 32, V_O).

The current drift of the AD1147 is typically 350pA/°C from +15°C to +35°C. When using the AD OP-07, the total offset drift of the output signal will typically be less than 2μV/°C.

As a second example, a high output current amplifier can be connected to the AD1147 to create a programmable power supply. The configuration is the same as shown for the AD OP-07C in Figure 4.

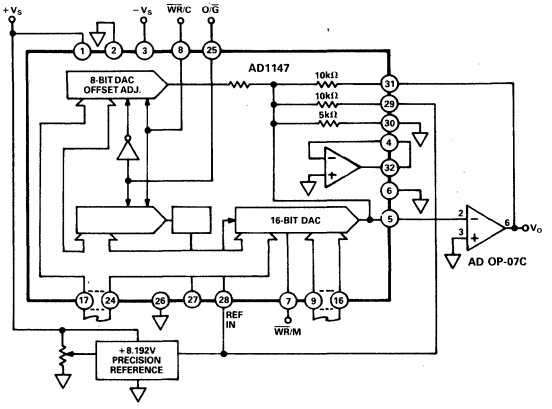


Figure 4. Precision DAC with ±8.192 F.S. Output Voltage

FULL FOUR-QUADRANT MULTIPLYING DAC

The AD1147 is a full four-quadrant multiplying DAC and can be used with references varying between +12 and −12 volts. Typical linearity vs. external reference voltage is shown in Figure 5. Output voltage ranges other than those provided can be obtained by connecting the appropriate reference voltage to "REF IN" (Pin 28), (see Figure 4). The DAC output voltage can be calculated as follows:

$$\text{UNIPOLAR } V_O = \frac{\text{DIGITAL INPUT}}{2^{16}} \times \frac{V_{REF}}{5k} \times R_{fb}$$

$$\text{BIPOLAR } V_O = \frac{\text{DIGITAL INPUT}}{2^{16}} \times \frac{V_{REF}}{5k} \times R_{fb} - \frac{V_{REF}}{10k}$$

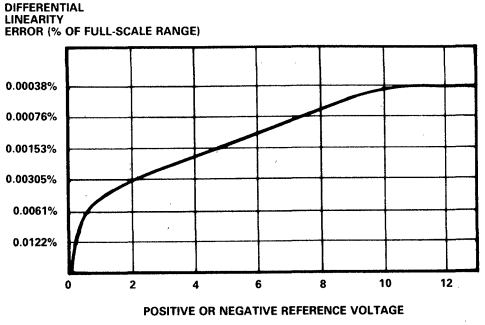


Figure 5. Typical Differential Linearity vs. External Reference Voltage

8-BIT MICROPROCESSOR INTERFACE

The AD1147/AD1148 can easily be operated with an 8-bit bus by the addition of an octal latch. The 16-bit Main DAC is loaded from the 8-bit bus as two 8-bit bytes. Figure 6 shows the configuration when using a 74HC573 octal latch.

The eight most significant bits are latched into the 74HC573 by setting the "latch enable" control line low. The eight least significant bits are then placed on the bus. Now all sixteen bits can be simultaneously latched into the Main DAC by setting $\overline{WR}$/M high.

The offset and gain correction DAC's are calibrated as they were for 16-bit microprocessor applications. See the "OFFSET AND GAIN CALIBRATION" section of this data sheet.

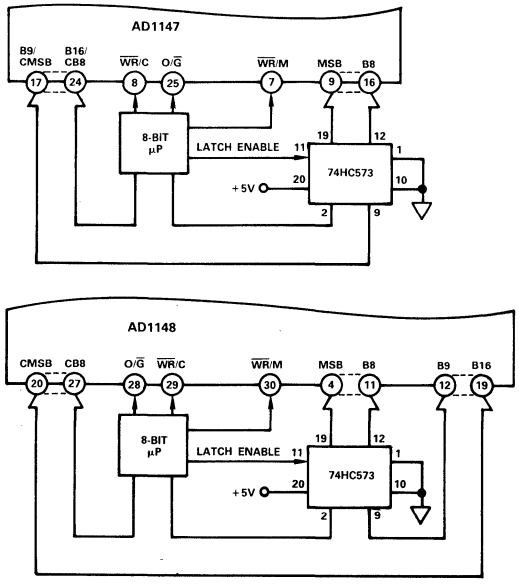


Figure 6. Connections for 8-Bit Bus Interface

AUTOMATIC TESTING OF 12-BIT ADC'S AND DAC'S

The AD1147 and AD1148 can be used as a reference DAC to automatically test the integral and differential linearity of 12-bit ADCs and DACs. An ideal reference DAC should be an order of magnitude more accurate than the devices to be tested. The AD1147 and AD1148 are sixteen times more accurate than the devices to be tested and therefore can be considered ideal.

The general test procedures for ADCs and DACs are shown below. Before actual testing proceeds, calibrate the offset and gain of the AD1147 or AD1148 (see "OFFSET AND GAIN CALIBRATION" section of this data sheet).

ADC TESTING (refer to Figures 7 and 8).

The differential nonlinearity of ADC's is the difference between the actual code widths of the analog input voltage vs. the ideal, one LSB, code widths of a perfect converter. A code width is the range of analog input voltage which produces the desired digital output word.

A code width can be measured by determining the analog input voltage at which the transition occurs from the code under test to its next lower digital output code and then differencing that analog value with the same determined for the transition from the code under test to its next higher digital output code.

Virtually all converters exhibit a degree of noise. This will necessitate an averaging technique to determine the analog input value for a code transition – where a reduction in analog input voltage produces a majority of the lower digital code decisions and an analog input increase produces a majority of the higher digital code decisions.

Begin testing by calibrating the offset and gain of the ADC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC to the nominal value of the desired transition edge (produces an analog input to the device under test that is either 1/2LSB below or 1/2LSB above the ideal analog input for the code under test). Increment or decrement this digital input until the Device Under Test (D.U.T.) outputs the digital code below the transition 50% of the time and the digital code above the transition 50% of the time. Record this digital input and repeat the procedure for the next transition of the nominal code to be measured. Compare this second digital input with the recorded input. The difference between these two digital values is the width of the code being measured. A perfect code width is 16 counts of the reference DAC. Each count more, or less than 16, corresponds to a differential linearity error of 1/16LSB for the D.U.T. The arithmetic average of the two digital input values is the center of the code being tested. Each count of difference between this actual code center and the ideal, nominal code center represents an integral linearity error of 1/16LSB.

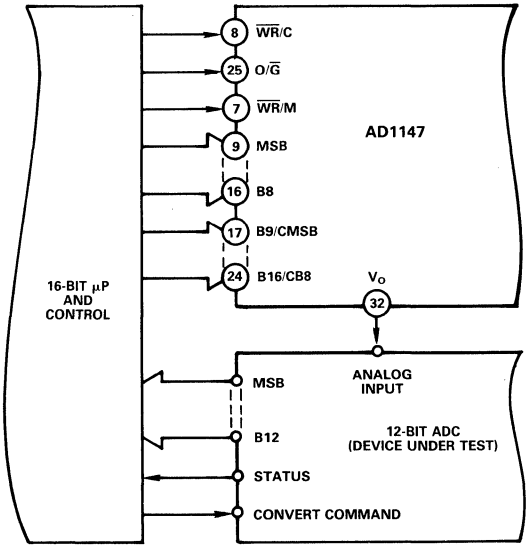


Figure 7. ADC Testing

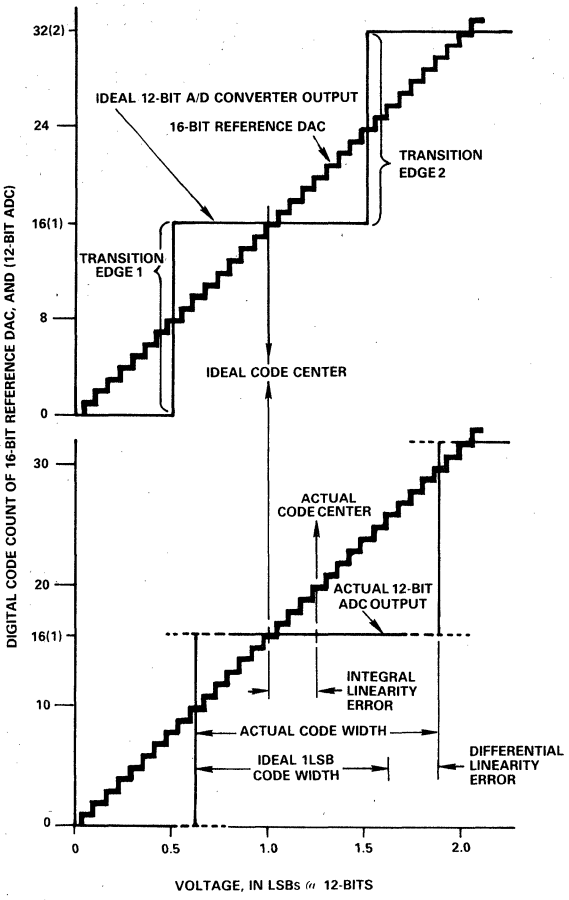


Figure 8. 12-Bit ADC Linearity Testing

DAC TESTING (refer to Figure 9).
To test 12-bit DACs begin with offset and gain calibration of the DAC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC and the D.U.T. to the desired code. Latch this digital input into the reference DAC. The DACs' outputs are differenced and amplified by an AD524A instrumentation amplifier. The voltage error between the DACs is the integral linearity error.

Now null the meter and then increment or decrement the digital input to the D.U.T. only, by one LSB. The meter reading will correspond to the code width of the new digital input word. The deviation of this voltage from the ideal value of one LSB is the differential linearity error of the D.U.T.

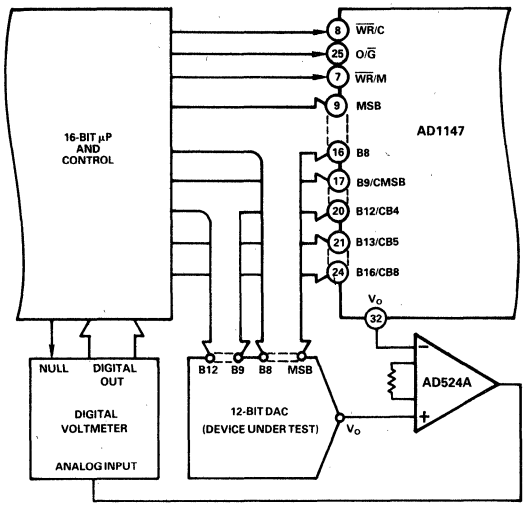


Figure 9. DAC Testing

ANALOG DEVICES

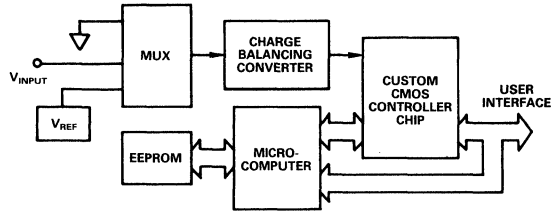
High Resolution, Programmable, Integrating A/D Converter

AD1170

FEATURES
- **Low Nonlinearity: ±0.001%**
- **Microcomputer – Based Design**
  - **Programmable Integration Time: 1 to 350ms with Usable Resolution up to 18 Bits**
  - **Programmable Output Data Format**
  - **Auto-Zeroed Operation and Electronic Calibration (No External Trims)**
  - **Microprocessor Compatible Interface**
- **High Normal-Mode Rejection: 54dB at 60Hz, 60dB at 50Hz**

APPLICATIONS
- **Data Acquisition System**
- **Scientific Instruments**
- **Medical Instruments**
- **Weighing Systems**
- **Automatic Test Equipment**

AD1170 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD1170 is a high resolution integrating A/D converter intended for applications requiring high accuracy and throughput at low cost. A novel conversion architecture is employed to provide the user with outstanding accuracy, stability and ease of use.

The AD1170 contains a complete microcomputer based measurement subsystem, composed of three major elements: a highly precise charge balancing converter, a single chip microcomputer, and a custom CMOS controller chip. The AD1170 offers independently programmable integration time (from one millisecond to 350 milliseconds) and data format (offset binary or two's complement, from 7 to 22 bits). The converter is fully auto-zeroed and exhibits a span drift of 5ppm/°C, assuring stable, accurate readings.

The AD1170 interfaces to the user system via an 8-bit microprocessor compatible data bus. The AD1170's advanced features are controlled via simple commands sent to it via this bus.

The converter utilizes surface mount technology and is housed in a small 1.2″×2.5″×0.55″ package. It operates from ±15V dc and +5V dc power.

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. The AD1170, unlike dual slope converters, offers the user the capability of programming the integration time by selecting one of seven present integration periods or by loading an arbitrary integration period over the interface bus.
2. The AD1170 architecture provides for user programmable data format independent of the integration time. All data is computed to 22-bit resolution and the user may specify any resolution from 7 to 22 bits. Usable resolution will typically be limited to 18 bits due to measurement and calibration noise error.
3. Electronic digital calibration eliminates the need for trim potentiometers. The calibration data is stored in an internal nonvolatile memory chip.
4. The conversion rate is greater than 50 conversions per second when using 60Hz line cycle integration. The maximum conversion rate is greater than 250 conversions per second, using a one millisecond integration period.
5. The AD1170 contains an 8-bit microprocessor compatible interface structure with all necessary control lines. It may be interfaced to any microcomputer based system in a memory mapped or I/O mapped fashion.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V, V_D = +5V unless otherwise specified)

Model	AD1170 Min	Typ	Max	Units
RESOLUTION	7		18	Bits
ACCURACY				
Integral Nonlinearity		±10		ppm FSR
THROUGHPUT RATE				
Time (Integrate) = 1ms	250			conv/sec
Time (Integrate) = 16.667ms	50			conv/sec
Time (Integrate) = 100ms	9			conv/sec
NOISE ERROR (peak-to-peak)				
T_{INT} @ T_{CAL}				
1ms 10ms		±100		ppm FSR
16.667ms 100ms		±8		ppm FSR
300ms 300ms		±3		ppm FSR
STABILITY				
Gain		±5		ppm/°C
POWER SUPPLY REJECTION RATIO				
(Span Error vs. Analog Supply Voltage)		−86		dB
INPUT CHARACTERISTICS				
Analog Input Range				
dc	−5		+5	Volts
dc Plus Normal-Mode Voltage	−6		+6	Volts
Absolut Maximum (Without Damage)	−30		+30	Volts
Normal-Mode Rejection				
@ 60Hz		54		dB
@ 50Hz		60		dB
Input Bias Current		10		nA
Input Impedance		100		Ω
DIGITAL LEVELS				
Inputs				
Low			0.4	Volts
High	2.4			Volts
Outputs				
Low (@ 4mA)			0.45	Volts
High (@ 100μA)	2.4			Volts
WARMUP TIME		5		Minutes
POWER REQUIREMENTS				
$+V_S$ and $-V_S$	9	15	18	Volts
$+V_D$	4.75	5	5.25	Volts
Supply Current Drain				
@ ±15V		20		mA
@ +5V		170		mA
TEMPERATURE RANGE				
Rated Performance	0		+70	°C
SIZE	1.24″ × 2.5″ × 0.55″ max (31.4 × 63.5 × 14.0mm)			

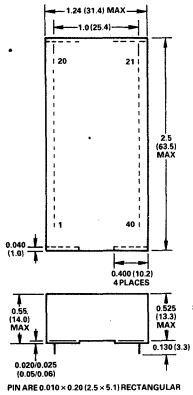
NOTE

[1]Noise error determines the usable resolution of the converter. Noise error is a function of T_{INT} and T_{CAL}, and improves as these times are lengthened.

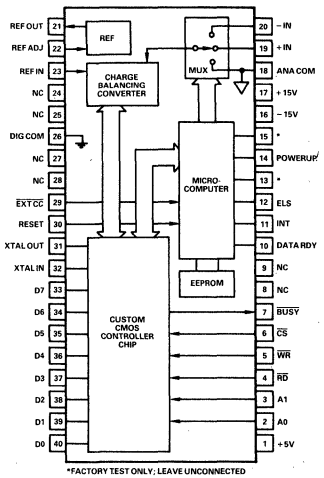
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).



PIN REFERENCE DIAGRAM



*FACTORY TEST ONLY; LEAVE UNCONNECTED

PIN DESCRIPTIONS

PIN	SIGNAL	DESCRIPTION
1	+5V	Digital Power Supply
2, 3	A0, A1	Address Lines
4	RD	Read Strobe
5	WR	Write Strobe
6	CS	Device Select
7	BUSY	When Low, Indicates Device Busy
10	DTA RDY	When High, Indicates Data Ready
11	INT	When High, Indicates Device is Currently Integrating the Input Signal
12	ELS	External Line Sample Input
16	−15V Pwr	Negative Analog Power Supply
17	+15V Pwr	Positive Analog Power Supply
18	ANA COM	Analog Common; the Reference Point for the Analog Power Supplies
19	+IN	Positive Signal Input
20	−IN	Negative Signal Input
21	REF OUT	Output of Internal Reference Voltage
22	REF ADJ	Used If Span Potentiometer Desired
23	REF IN	Reference Input; Usually Connected to the REF OUT PIN
26	DIG COM	Digital Common; the Reference Point for All Digital Signals and the +5V Supply
29	EXT CC	External Convert Command Input
30	RESET	Reset Input; Usually Connected to an RC Network for Automatic Powerup Reset
31, 32	XTAL OUT XTAL IN	Connections for 12MHz Crystal
33–40	D7–D0	Bidirectional Data Bus
13–15	–	Factory Test Only; Do Not Connect
8, 9, 24 25, 27, 28		No Connect

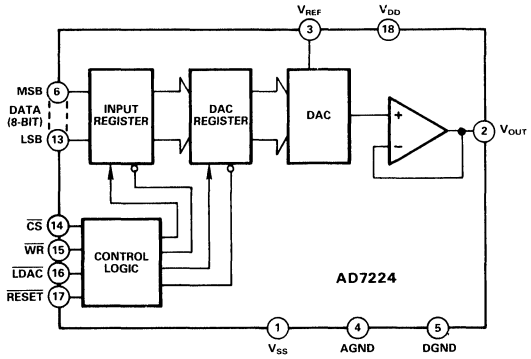
ANALOG DEVICES

LC²MOS 8-Bit DAC With Output Amplifier

AD7224

FEATURES
8-Bit CMOS DAC with Output Amplifier
Operates with Single or Dual Supplies
Low Total Unadjusted Error:
Less than 1 LSB Over Temperature
µP-Compatible with Double Buffered Input
Small, 0.3" Wide, 18-Pin DIP

AD7224 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD7224 is a precision 8-bit, voltage-output, digital-to-analog converter with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers– an input register and a DAC register. Only the data held in the DAC register determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224's. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. The output amplifier is capable of developing +10V across a 2kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip:
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35mW typical with single supply).
2. Low Total Unadjusted Error:
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC² MOS) process, coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1LSB over the full operating temperature range.
3. Single or Dual Supply Operation:
   The voltage-mode configuration of the AD7224 allows operation from a single power supply rail. The part can also be operated with dual supplies giving enhanced performance for some parameters.
4. Versatile Interface Logic
   The high speed logic allows direct interfacing to most microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7224 in multiple DAC systems. The part also features a zero override function.

DUAL SUPPLY SPECIFICATIONS

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} −4V)[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7224K,B,T[2]	AD7224L,C,U[2]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy[3]	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error[3]	±3/2	±1	LSB max	
Full Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	±20	mV max	
Zero Code Error Temperature Coefficient	±50	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	8	8	kΩ min	
Input Capacitance[4]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2.5	2.5	V/µs min	
Voltage Output Settling Time[4]				
Positive Full Scale Change	5	5	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Negative Full Scale Change	7	7	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	4.5/5.5	4.5/5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}				
@25°C	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{min} to T_{max}	5	5	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4]				
t_1				
@25°C	150	150	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_2				
@25°C	150	150	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	100	100	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7224KN, LN 0 to +70°C
AD7224BQ, CQ −25°C to +85°C
AD7224TD, UD −55°C to +125°C
[3]See Terminology.
[4]Sample Tested at 25°C by Product Assurance to ensure compliance.
Specifications subject to change without notice.

SINGLE SUPPLY SPECIFICATIONS

(V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7224K,B,T[2]	AD7224L,C,U[2]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error[3]	±2	±2	LSB max	
Differential Nonlinearity[3]	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[4]	100	100	pF max	Occurs when DAC is loaded with all 1's.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2	2	V/μs min	
Voltage Output Settling Time[4]				
Positive Full Scale Change	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	20	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}				
@25°C	4	4	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
T_{min} to T_{max}	6	6	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4]				
t_1				
@25°C	150	150	ns min	Chip Select/Load DAC Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_2				
@25°C	150	150	ns min	Write/Reset Pulse Width
T_{min} to T_{max}	200	200	ns min	
t_3				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{min} to T_{max}	0	0	ns min	
t_4				
@25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{min} to T_{max}	0	0	ns min	
t_5				
@25°C	90	90	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	100	100	ns min	
t_6				
@25°C	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7224KN, LN 0 to +70°C
AD7224BQ, CQ −25°C to +85°C
AD7224TD, UD −55°C to +125°C
[3]See Terminology.
[4]Sample Tested at 25°C by Product Assurance to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C
Operating Temperature	
Commerical	0 to +70°C
Industrial	−25°C to +85°C
Extended	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES
[1]The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full scale error, relative accuracy and zero code error. Maximum output voltage is V_{REF} − 1LSB (ideal) where 1LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error, relative to LSB size, will increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY

Relative Accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero code error and full scale error and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output due to a change in the digital input code. It is specified in nV secs and is measured at V_{REF} = 0V.

FULL SCALE ERROR

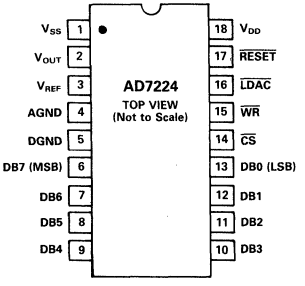
Full Scale Error is defined as:
Measured Value – Zero Code Error – Ideal Value

ORDERING INFORMATION

Total Unadjusted Error	Temperature Range and Package		
	Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Side Brazed Ceramic −55°C to +125°C
±2LSB	AD7224KN	AD7224BQ	AD7224TD
±1LSB	AD7224LN	AD7224CQ	AD7224UD

NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

PIN CONFIGURATION



CIRCUIT INFORMATION

D/A SECTION

The AD7224 contains an 8-bit voltage-mode digital-to-analog converter. The output voltage from the converter has the same polarity as the reference voltage allowing single supply operation. A novel DAC switch pair arrangement on the AD7224 allows a reference voltage range from +2V to +12.5V.

The DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS single pole, double-throw switches. The simplified circuit diagram for this DAC is shown in Figure 1.

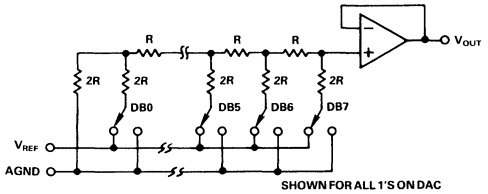


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin is code dependent and can vary from 8kΩ minimum to infinity. The lowest input impedance occurs when the DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminal is also code dependent and typically varies from 25pF to 50pF.

The V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUT} = D \cdot V_{REF}$$

where D is a fractional representation of the digital input code and can vary from 0 to 255/256.

OP-AMP SECTION

The voltage-mode D/A converter output is buffered by a unity gain non-inverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF.

The AD7224 can be operated single or dual supply resulting in different performance in some parameters from the output amplifier. In single supply operation (V_{SS} = 0V = AGND) the sink capability of the amplifier, which is normally 400μA, is reduced as the output voltage nears AGND. The full sink capability of 400μA is maintained over the full output voltage range by tying V_{SS} to −5V. This is indicated in Figure 2.

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

Additionally, the negative V_{SS} gives more head-room to the output amplifier which results in better zero code performance and improved slew-rate at the output, than can be obtained in the single supply mode.

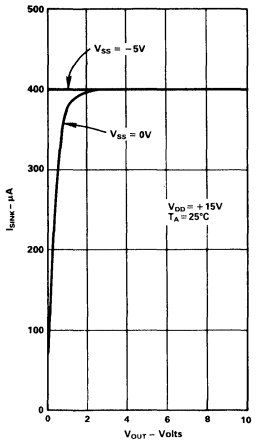


Figure 2. Variation of I_{SINK} with V_{OUT}

DIGITAL SECTION

The AD7224 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

Table I shows the truth table for AD7224 operation. The part contains two registers, an input register and a DAC register. $\overline{CS}$ and $\overline{WR}$ control the loading of the input register while $\overline{LDAC}$ and $\overline{WR}$ control the transfer of information from the input register to the DAC register. Only the data held in the DAC register will determine the analog output of the converter.

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↓	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↓	H	DAC Register Latched
L	X	X	X	Both Registers Loaded With All Zeros
↓	H	H	H	Both Register Latched With All Zeros and Output Remains at Zero
↓	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care

Table I. AD7224 Truth Table

All control signals are level-triggered and therefore either or both registers may be made transparent; the input register by keeping $\overline{CS}$ and $\overline{WR}$ "LOW", the DAC register by keeping $\overline{LDAC}$ and $\overline{WR}$ "LOW". Input data is latched on the rising edge of $\overline{WR}$.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line functions like a zero override with the output brought to 0V for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on $\overline{RESET}$ will latch all 0's into the registers and the output remains at 0V after the $\overline{RESET}$ line has returned "HIGH". The $\overline{RESET}$ line can be used to ensure power-up to 0V on the AD7224 output and is also useful, when used as a zero override, in system calibration cycles. Figure 3 shows the input control logic for the AD7224.

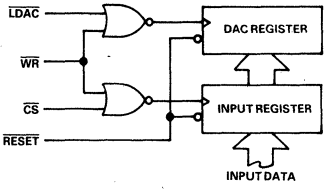
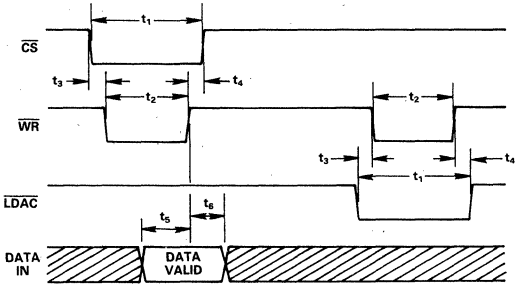


Figure 3. Input Control Logic



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% of V_{DD}. $t_r = t_f$ = 20ns OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$

Figure 4. Write Cycle Timing Diagram

SPECIFICATION RANGES

For the DAC to maintain specified accuracy, the reference voltage must be at least 4V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

With dual supply operation, the AD7224 has an extended V_{DD} range from +12V ±5% to +15V ±10% (i.e., from +11.4V to +16.5V). Operation is also specified for a single V_{DD} power supply of +15V ±5%.

Performance is specified over a wide range of reference voltages from 2V to (V_{DD} −4V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5V bandgap reference and the AD584, a precision +10V reference. Note that in order to achieve an output voltage range of 0V to +10V, a nominal +15V ±5% power supply voltage is required by the AD7224.

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7224. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7224 AGND and DGND pins (IN914 or equivalent).

Applying the 7224

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7224, with the output voltage having the same positive polarity as V_{REF}. The AD7224 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 5. The voltage at V_{REF} must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

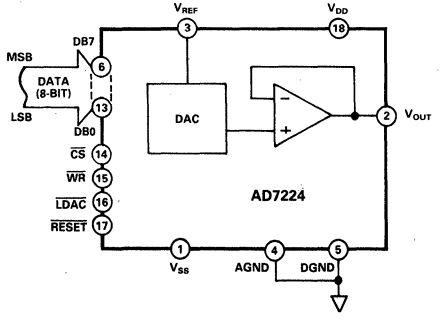


Figure 5. Unipolar Output Circuit

DAC Register Contents MSB LSB	Analog Output, V_{OUT}
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

The AD7224 can be configured to provide bipolar output operation using one external amplifier and two resistors. Figure 6 shows a circuit used to implement offset binary coding. In this case

$$V_O = \left(1 + \frac{R2}{R1}\right) \cdot (D\ V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_O = (2D - 1) \cdot V_{REF}$$

where D is a fractional representation of the digital word in the DAC register.

Mismatch between R1 and R2 causes gain and offset errors; therefore, these resistors must match and track over temperature. Once again, the AD7224 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 6 with R1 = R2.

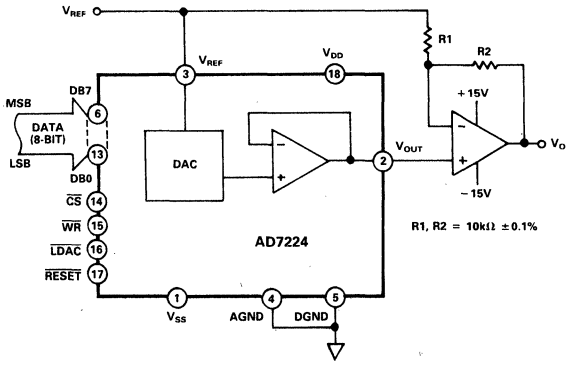


Figure 6. Bipolar Output Circuit

DAC Register Contents MSB LSB	Analog Output, V_O
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar (Offset Binary) Code Table

AGND BIAS

The AD7224 AGND pin can be biased above system GND (AD7224 DGND) to provide an offset "zero" analog output voltage level. Figure 7 shows a circuit configuration to achieve this. The output voltage, V_{OUT}, is expressed as:

$$V_{OUT} = V_{BIAS} + D \cdot (V_{IN})$$

where D is a fractional representation of the digital word in the DAC register and can vary from 0 to 255/256.

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

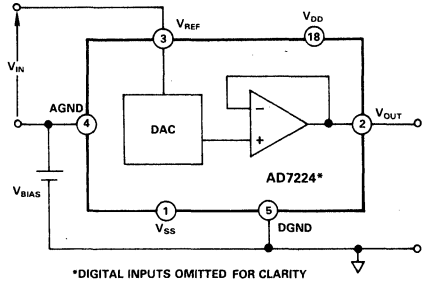


Figure 7. AGND Bias Circuit

Microprocessor Interface

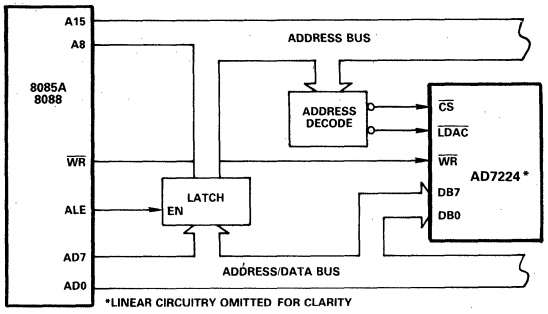


Figure 8. AD7224 to 8085A/8088 Interface

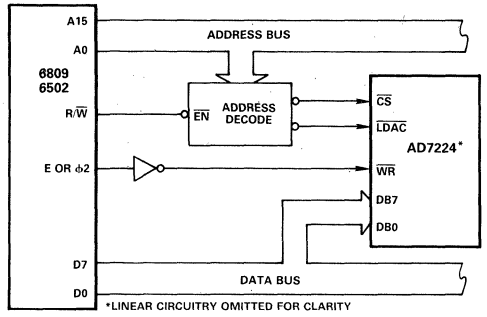


Figure 9. AD7224 to 6809/6502 Interface

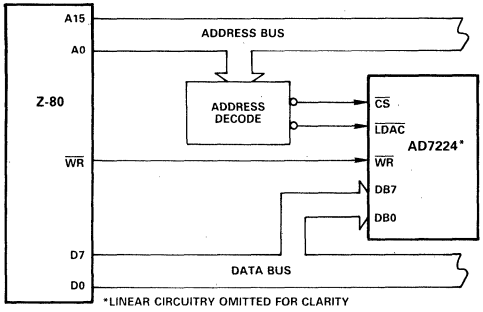


Figure 10. AD7224 to Z-80 Interface

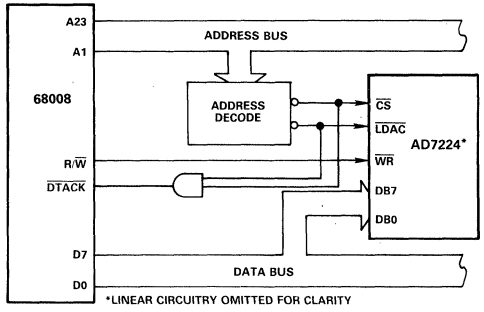
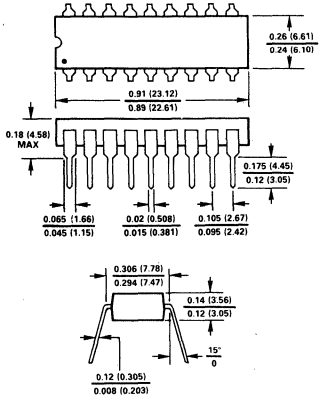


Figure 11. AD7224 to 68008 Interface

MECHANICAL INFORMATION
OUTLINE DIMENSIONS

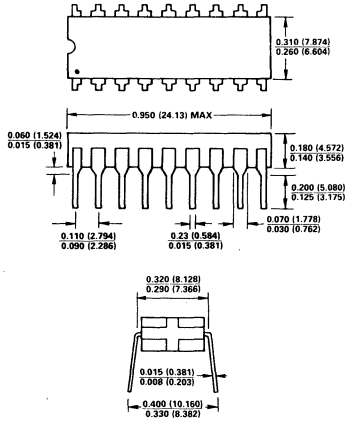
Dimensions shown in inches and (mm).

18-PIN PLASTIC DIP (SUFFIX N)



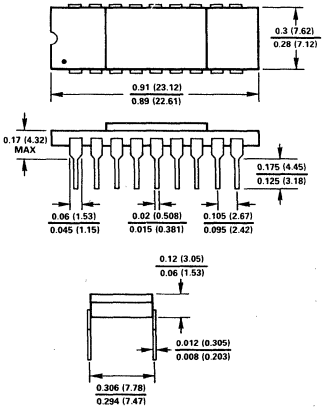
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERDIP (SUFFIX Q)



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERAMIC (SUFFIX D)



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

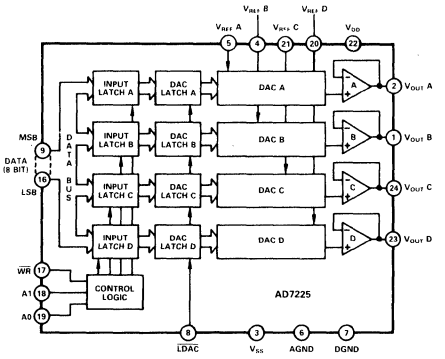
ANALOG DEVICES

LC²MOS
Quad 8-Bit DAC with Separate References

AD7225

FEATURES
Four 8-Bit DACs with Output Amplifiers
Separate Reference Input for Each DAC
µP Compatible with Double-Buffered Inputs
Simultaneous Update of All Four Outputs
Operates with Single or Dual Supplies
No User Trims Required
0.3" Wide, 24-Pin DIP

AD7225 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each D/A converter has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel–an input register and a DAC register. Control inputs A0 and A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V when using dual supplies. The part is also specified for single supply operation using a reference of +10V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7225 is fabricated on an all ion-implanted high-speed Linear Compatible CMOS (LC² MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip:
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single or Dual Supply Operation:
   The voltage-mode configuration of the AD7225 allows single supply operation. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Versatile Interface Logic:
   The AD7225 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. The double-buffered interface allows simultaneous update of the four outputs.
4. Separate Reference Input for Each DAC:
   The AD7225 offers great flexibility in dealing with input signals with a separate reference input provided for each DAC and each reference having variable input voltage capability.

DUAL SUPPLY SPECIFICATIONS

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} −4V)[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7225KN[2] AD7225BD	AD7225LN AD7225CD	AD7225TD	AD7225UD	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy[3]	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full Scale Error[3]	±1	±1/2	±1	±1/2	LSB max	
Full Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error @ 25°C	±25	±15	±25	±15	mV max	
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Zero Code Error Temp Coeff.	±30	±30	±30	±30	μV/°C typ	
REFERENCE INPUT						
Voltage Range	2 to (V_{DD} −4)	2 to (V_{DD} −4)	2 to (V_{DD} −4)	2 to (V_{DD} −4)	V_{min} to V_{max}	
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[4]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3,4]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3,4,5]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[4]	2.5	2.5	2.5	2.5	V/μs min	
Voltage Output Settling Time[4]						
Positive Full Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	5	5	5	5	μs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Feedthrough[3,4,5]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3,5]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	11.4/16.5	11.4/16.5	11.4/16.5	11.4/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	10	10	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7225KN, LN 0 to +70°C
AD7225BD, CD −25°C to +85°C
AD7225TD, UD −55°C to +125°C
[3]See Terminology.
[4]Sample Tested at 25°C to ensure compliance.
[5]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.
Specifications subject to change without notice.

SINGLE SUPPLY SPECIFICATIONS

(V_{DD} = +15V ±5%, V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7225KN[2] AD7225BD	AD7225LN AD7225CD	AD7225TD	AD7225UD	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT						
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[4]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1's.
Channel-to-Channel Isolation[3,4]	60	60	60	60	dB min	V_{REF} = 10V p-p Sine Wave @ 10kHz
AC Feedthrough[3,4,5]	−70	−70	−70	−70	dB max	V_{REF} = 10V p-p Sine Wave @ 10kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[4]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[4]	2	2	2	2	V/μs min	
Voltage Output Settling Time[4]						
Positive Full Scale Change	5	5	5	5	μs max	Settling Time to ±1/2LSB
Negative Full Scale Change	7	7	7	7	μs max	Settling Time to ±1/2LSB
Digital Feedthrough[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0's to all 1's.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES						
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V_{min}/V_{max}	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
SWITCHING CHARACTERISTICS[4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{min} to T_{max}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{min} to T_{max}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{min} to T_{max}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{min} to T_{max}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7225KN, LN 0 to +70°C
AD7225BD, CD −25°C to +85°C
AD7225TD, UD −55°C to +125°C
[3]See Terminology.
[4]Sample Tested at 25°C to ensure compliance.
[5]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	500mW
Derates above 75°C by	2.0mW/C
Operating Temperature	
Commercial	0 to +70°C
Industrial	−25°C to +85°C
Extended	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES

[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full scale error, relative accuracy, and zero code error. Maximum output voltage is V_{REF} − 1LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY

Relative Accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero code error and full scale error and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output of the DAC due to a change in its digital input code. It is specified in nV secs and is measured at V_{REF} = 0V.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter. It is specified in nV secs and is measured at V_{REF} = 0V.

AC FEEDTHROUGH

AC Feedthrough is the proportion of reference input signal which appears at the output of a converter when that DAC is loaded with all 0's.

CHANNEL-TO-CHANNEL ISOLATION

Channel-to-channel isolation is the proportion of input signal from the reference of one DAC (loaded with all 1's) which appears at the output of one of the other three DACs (loaded with all 0's). The figure given is the worst case for the three other outputs and is expressed as a ratio in dBs.

FULL SCALE ERROR

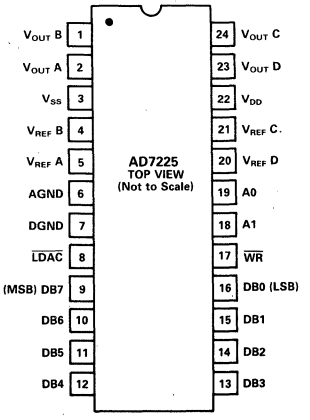
Full Scale Error is defined as:

Measured Value – Zero Code Error – Ideal Value

ORDERING INFORMATION

Total Unadjusted Error	Temperature Range and Package: Plastic 0 to +70°C	Side Brazed Ceramic −25°C to +85°C	Side Brazed Ceramic −55°C to +125°C
±2LSB	AD7225KN	AD7225BD	AD7225TD
±1LSB	AD7225LN	AD7225CD	AD7225UD

PIN CONFIGURATION



$T_A = 25°C$, $V_{DD} = +15V$, $V_{SS} = -5V$ unless otherwise stated.

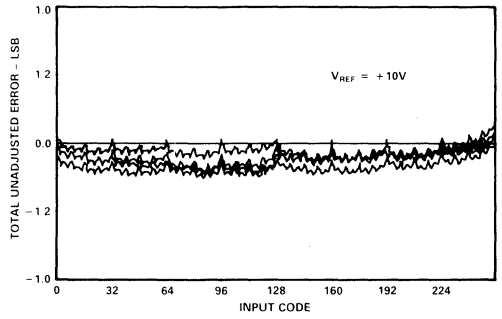


Figure 1. Channel-to-Channel Matching

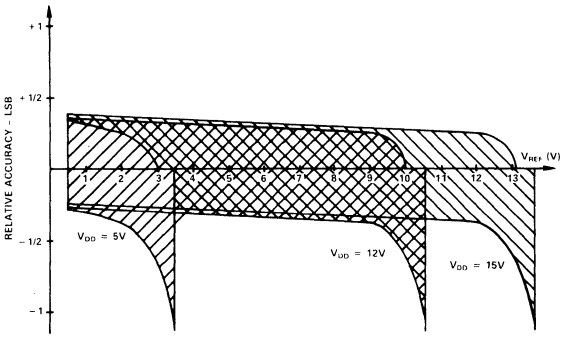


Figure 2. Relative Accuracy vs. V_{REF}

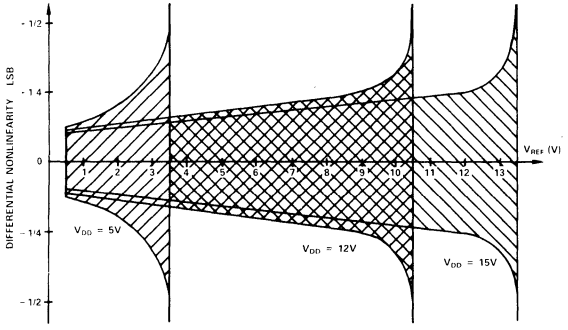


Figure 3. Differential Nonlinearity vs. V_{REF}

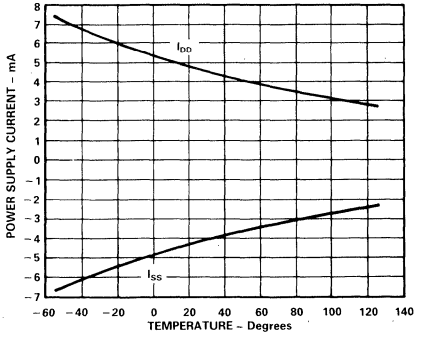


Figure 4. Power Supply Current vs. Temperature

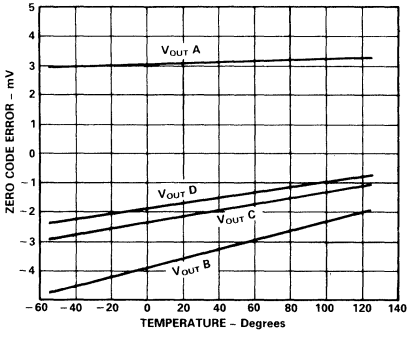


Figure 5. Zero Code Error vs. Temperature

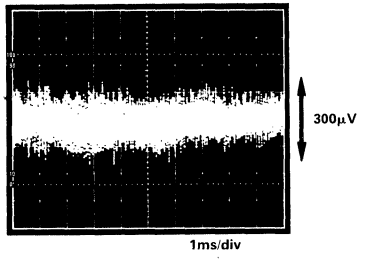


Figure 6. Broadband Noise

CIRCUIT INFORMATION

D/A SECTION

The AD7225 contains four, identical, 8-bit voltage-mode digital-to-analog converters. Each D/A converter has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, allowing single supply operation. A novel DAC switch pair arrangement on the AD7225 allows a reference voltage range from +2V to +12.5V on each reference input.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high-speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for channel A is shown in Figure 7. Note that AGND (Pin 6) is common to all four DACs.

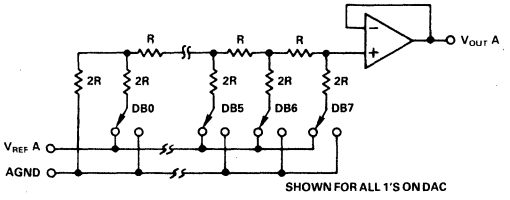


Figure 7. D/A Simplified Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 11kΩ minimum to infinity. The lowest input impedance at any reference input occurs when that DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 15pF to 35pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTX} = D_X \cdot V_{REFX}$$

where D_X is fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

OP-AMP SECTION

Each voltage mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF.

The AD7225 can be operated single or dual supply; operating with dual supplies results in enhanced performance in some parameters which cannot be achieved with single supply operation. In single supply operation (V_{SS} = 0V = AGND) the sink capability of the amplifier, which is normally 400μA, is reduced as the output voltage nears AGND. The full sink capability of 400μA is maintained over the full output voltage range by tying V_{SS} to −5V. This is indicated in Figure 8.

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

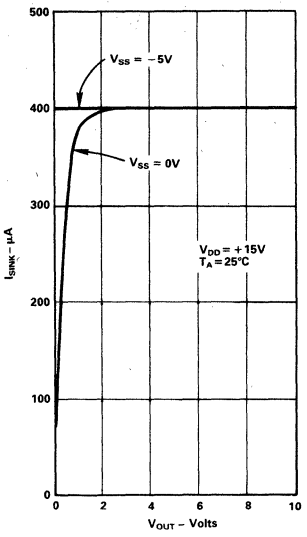


Figure 8. Variation of I_{SINK} with V_{OUT}

Additionally, the negative V_{SS} gives more headroom to the output amplifiers which results in better zero code performance and improved slew-rate at the output, than can be obtained in the single supply mode.

DIGITAL SECTION

The AD7225 digital inputs are compatible with either TTL or 5V CMOS levels. All logic inputs are static-protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the input port. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table I shows the addressing for the input registers on the AD7225.

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and therefore the DAC registers may be made transparent by tying $\overline{LDAC}$ LOW (in

A1	A0	Selected Input Register
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table I. AD7225 Addressing

this case the outputs of the converters will respond to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), then $\overline{LDAC}$ must stay LOW for t_6 or longer after $\overline{WR}$ goes HIGH to ensure correct data is latched through to the output. Table II shows the truth table for AD7225 operation. Figure 9 shows the input control logic for the part and the write cycle timing diagram is given in Figure 10.

$\overline{WR}$	$\overline{LDAC}$	Function
H	H	No Operation. Device not selected
L	H	Input Register of Selected DAC Transparent
↓	H	Input Register of Selected DAC Latched
H	L	All Four DAC Registers Transparent (i.e. Outputs respond to data held in respective input registers) Input Registers are Latched
H	↓	All Four DAC Registers Latched
L	L	DAC Registers and Selected Input Register Transparent Output follows Input Data for Selected Channel.

Table II. AD7225 Truth Table

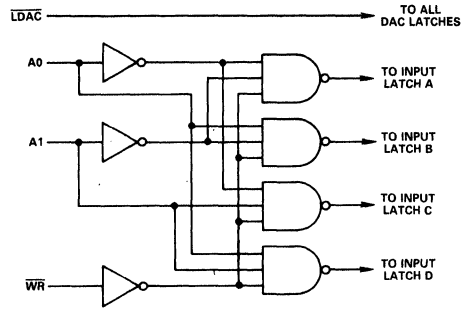


Figure 9. Input Control Logic

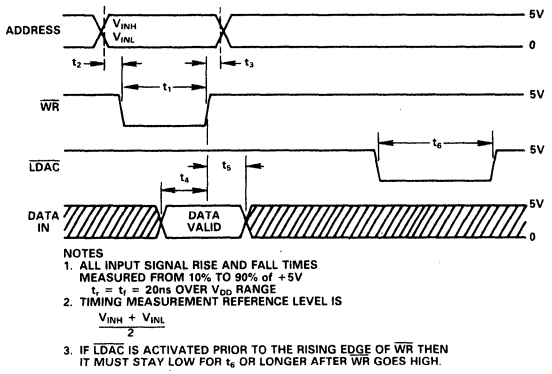


Figure 10. Write Cycle Timing Diagram

GROUND MANAGEMENT AND LAYOUT

Since the AD7225 contains four reference inputs which can be driven from ac sources (see AC REFERENCE SIGNAL section) careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends upon the optimum choice of board layout. Figure 11 shows the relationship between input frequency and channel-to-channel isolation. Figure 12 shows a printed circuit board layout which is aimed at minimizing crosstalk and feedthrough. The four input signals are screened by AGND. V_{REF} was limited to between 2V and 3.24V to avoid slew rate limiting effects from the output amplifier during measurements.

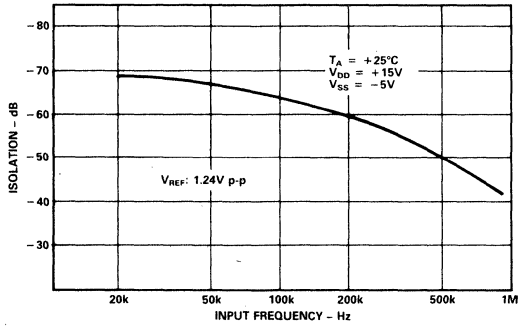


Figure 11. Channel-to-Channel Isolation

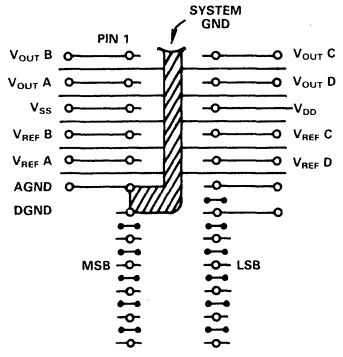


Figure 12. Suggested PCB Layout for AD7225. Layout Shows Component Side (Top View).

SPECIFICATION RANGES

For the AD7225 to operate to rated specifications, its input reference voltage must be at least 4V below the V_{DD} power supply voltage. This voltage differential is the overhead voltage required by the output amplifiers.

The AD7225 is specified to operate over a V_{DD} range from +12V ±5% to +15V ±10% (i.e., from +11.4V to +16.5V) with a V_{SS} of −5V ±10%. Operation is also specified for a single +15V ±5% V_{DD} supply. Applying a V_{SS} of −5V results in improved zero code error, improved output sink capability with outputs near AGND and improved negative going settling time.

Performance is specified over a wide range of reference voltages from 2V to (V_{DD} − 4V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5V bandgap reference and the AD584, a precision +10V reference. Note that an output voltage range of 0V to +10V requires a nominal +15V ±5% power supply voltage.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7225, with the output voltage having the same positive polarity as V_{REF}. The AD7225 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 13. The voltage at any of the reference inputs must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table III.

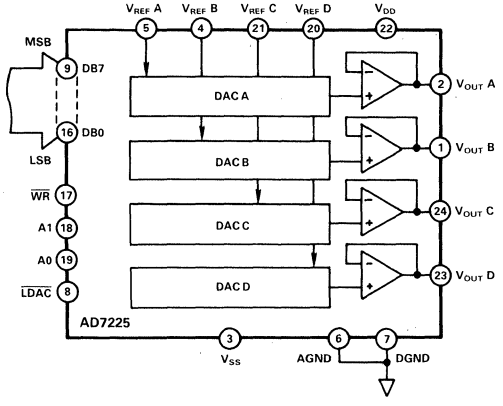


Figure 13. Unipolar Output Circuit

DAC Latch Contents MSB	LSB	Analog Output
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table III. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

Each of the DACs of the AD7225 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 14 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7225. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A. ($0 \leq D_A \leq 255/256$)

Mismatch between R1 and R2 causes gain and offset errors and, therefore, these resistors must match and track over temperature. Once again the AD7225 can be operated in single supply or from positive/negative supplies. Table IV shows the digital code versus output voltage relationship for the circuit of Figure 14 with R1 = R2.

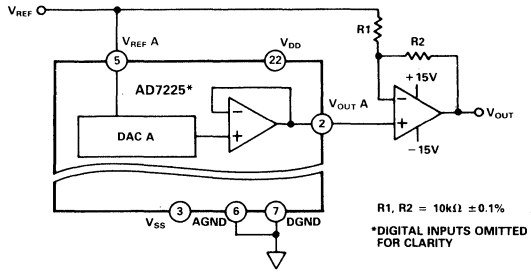


Figure 14. AD7225 Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table IV. Bipolar (Offset Binary) Code Table

AGND BIAS

The AD7225 AGND pin can be biased above system GND (AD7225 DGND) to provide an offset "zero" analog output voltage level. Figure 15 shows a circuit configuration to achieve this for channel A of the AD7225. The output voltage, V_{OUT} A, can be expressed as:

$$V_{OUT}\,A = V_{BIAS} + D_A\,(V_{IN})$$

where D_A is a fractional representation of the digital word in DAC latch A. ($0 \leq D_A \leq 255/256$).

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4V to ensure specified operation. Note that because the AGND pin is common to all four DACs, this method biases up the output

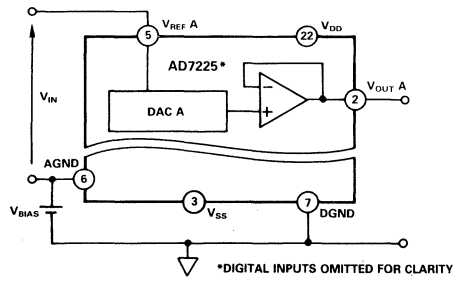


Figure 15. AGND Bias Circuit

voltages of all the DACs in the AD7225. Note that V_{DD} and V_{SS} of the AD7225 should be referenced to DGND.

AC REFERENCE SIGNAL

In some applications it may be desirable to have ac reference signals. The AD7225 has multiplying capability within the upper (V_{DD} – 4V) and lower (2V) limits of reference voltage when operated with dual supplies. Therefore ac signals need to be ac coupled and biased up before being applied to the reference inputs. Figure 16 shows a sine wave signal applied to V_{REF} A. For input signal frequencies up to 50kHz the output distortion typically remains less than 0.1%. The typical 3dB bandwidth figure for small signal inputs is 800kHz.

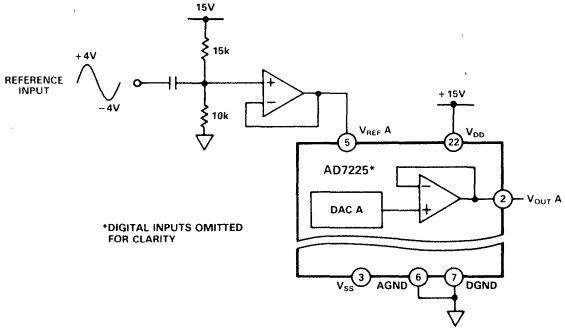


Figure 16. Applying an AC Signal to the AD7225

APPLICATIONS

PROGRAMMABLE TRANSVERSAL FILTER

A discrete-time filter may be described by either multiplication in the frequency domain or convolution in the time domain i.e.

$$Y(\omega) = H(\omega)X(\omega) \quad \text{or} \quad y_n = \sum_{k=1}^{N} h_k x_{n-k+1}$$

The convolution sum may be implemented using the special structure known as the transversal filter (Figure 17). Basically, it consists of an N-stage delay line with N taps weighted by N coefficients, the resulting products being accumulated to form the output. The tap weights or coefficients h_k are actually the non-zero elements of the impulse response and therefore determine the filter transfer function. A particular filter frequency response is realized by setting the coefficients to the appropriate values. This property leads to the implementation of transversal filters whose frequency response is programmable.

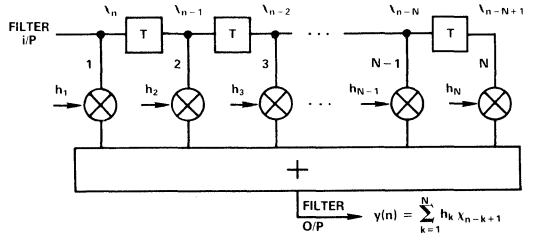


Figure 17. Transversal Filter

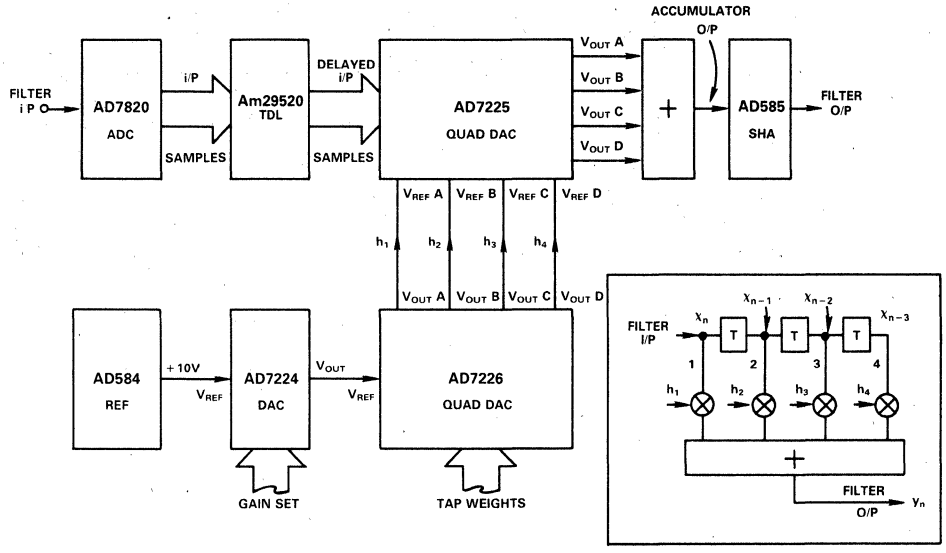


Figure 18. Programmable Transversal Filter

A 4-tap programmable transversal filter may be implemented using the AD7225 (Figure 18). The input signal is first sampled and converted to allow the tapped delay line function to be provided by the Am29520. The multiplication of delayed input samples by fixed, programmable tap weights is accomplished by the AD7225, the four coefficients or reference inputs being set by the digital codes stored in the AD7226. The resultant products are accumulated to yield the convolution sum output sample which is held by the AD585.

Low pass, bandpass and highpass filters may be synthesized using this arrangement. The particular tap weights needed for any desired transfer function may be obtained using the standard Remez Exchange Algorithm. Figure 19 shows the theoretical low pass frequency response produced by a 4-tap transversal filter with the coefficients indicated. Although the theoretical prediction does not take into account the quantization of the input samples and the truncation of the coefficients, nevertheless, there exists a good correlation with the actual performance of the transversal filter (Figure 20).

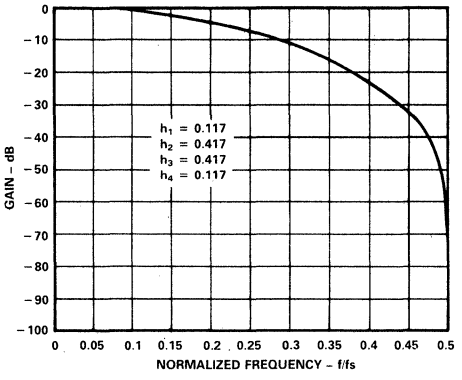


Figure 19. Predicted (Theoretical) Response

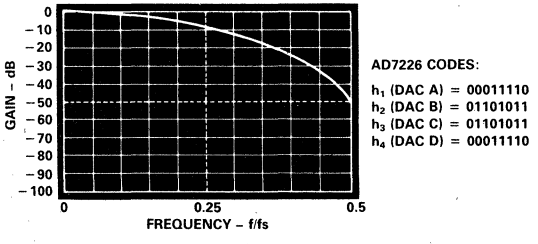


Figure 20. Actual Response

DIGITAL WORD MULTIPLICATION

Since each DAC of the AD7225 has a separate reference input, the output of one DAC can be used as the reference input for another. This means that multiplication of digital words can be performed (with the result given in analog form). For example, if the output from DACA is applied to V_{REF} B then the output from DACB, V_{OUT} B, can be expressed as:

$$V_{OUT}\ B = D_A \cdot D_B \cdot V_{REF}\ A$$

where D_A and D_B are the fractional representations of the digital words in DAC latches A and B respectively.

If $D_A = D_B = D$ then the result is $D^2 \cdot V_{REF}$ A

In this manner, the four DACs can be used on their own or in conjunction with an external summing amplifier to generate complex waveforms. Figure 21 shows one such application. In this case the output waveform, Y, is represented by:

$$Y = -(x^4 + 2x^3 + 3x^2 + 2x + 4) \cdot V_{IN}$$

where x is the digital code which is applied to all four DAC latches.

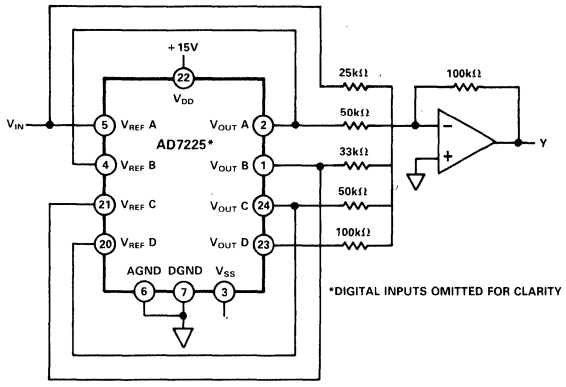


Figure 21. Complex Waveform Generation

3

MICROPROCESSOR INTERFACE

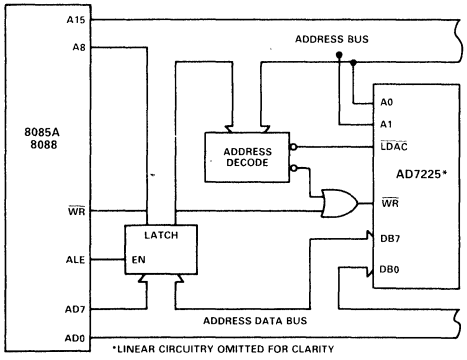


Figure 22. AD7225 to 8085A/8088 Interface, Double-Buffered Mode

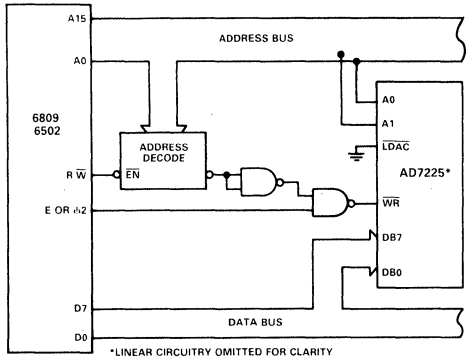


Figure 23. AD7225 to 6809/6502 Interface, Single-Buffered Mode

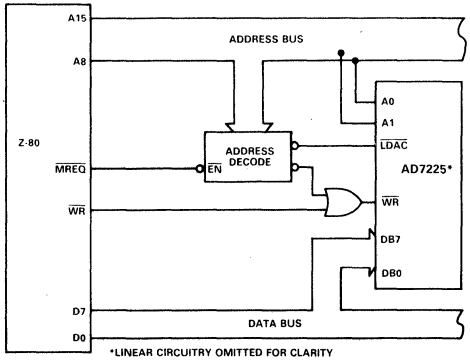


Figure 24. AD7225 to Z-80 Interface Double-Buffered Mode

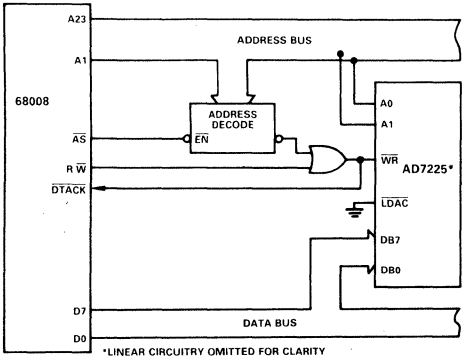


Figure 25. AD7225 to 68008 Interface, Single-Buffered Mode

V_{SS} GENERATION

Operating the AD7225 from dual supplies results in enhanced performance over single supply operation on a number of parameters as previously outlined. Some applications may require this enhanced performance, but may only have a single power supply rail available. The circuit of Figure 26 shows a method of generating a negative voltage using one CD4049, operated from a V_{DD} of +15V. Two inverters of the hex inverter chip are used as an oscillator. The other four inverters are in parallel and used as buffers for higher output current. The square-wave output is level translated to a negative-going signal, then rectified and filtered. The circuit configuration shown will provide an output voltage of −5.1V for current loadings in the range 0.5mA to 9mA. This will satisfy the AD7225 I_{SS} requirement over the commercial operating temperature range.

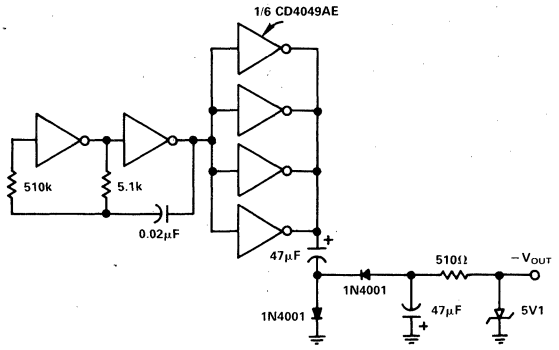
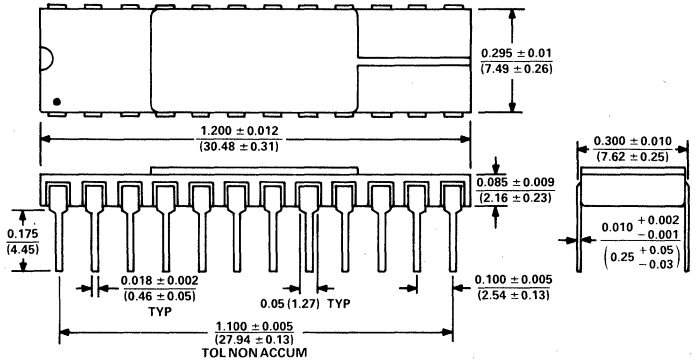


Figure 26. V_{SS} Generation Circuit

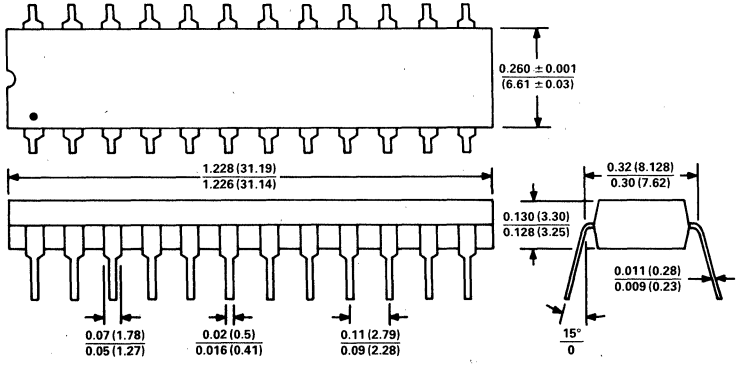
MECHANICAL INFORMATION
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-PIN CERAMIC (SUFFIX D)



24-PIN PLASTIC (SUFFIX N)



ANALOG DEVICES

LC²MOS 12-Bit DACPORT™

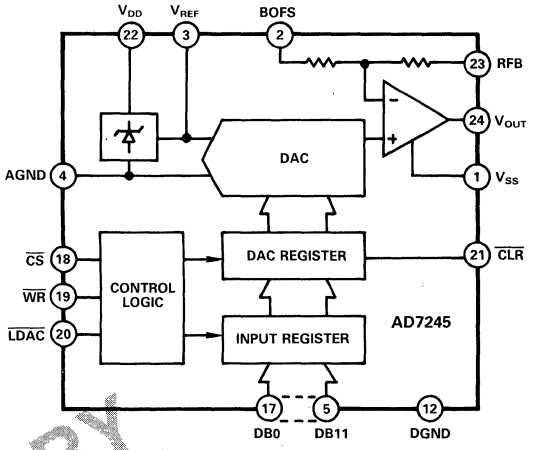
AD7245/48

FEATURES

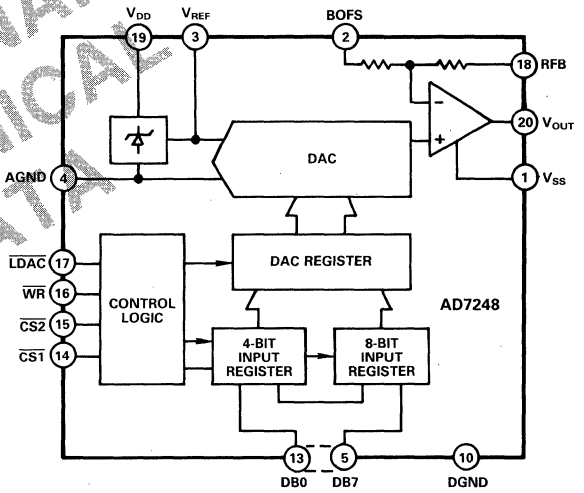
Complete 12-Bit DAC on Single Chip
- **On-Chip Reference**
- **Buffered Voltage Output**
- **Fast Digital Interface**

Low Power (60mW)
Single or Dual Supply Operation
Unipolar or Bipolar Output
0.3" Skinny DIP

AD7245 FUNCTIONAL BLOCK DIAGRAM



AD7248 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7245/48 is a complete, 12-bit, voltage-output, digital-to-analog converter with output amplifier and zener voltage reference on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The parts feature double-buffered interface logic with a 12-bit input register and 12-bit DAC register. Data is loaded to the AD7245 input register in one 12-bit load while data for the AD7248 input register is loaded in an 8-bit load followed by a 4-bit load. A separate $\overline{\text{LDAC}}$ signal transfers data from the input register to the DAC register. Only data held in the DAC register determines the analog output of the converter. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most microprocessors.

The on-chip zener diode provides a low-noise, temperature compensated reference for the DAC. The gain setting resistors allow a number of ranges at the output; 0 to +10V, −5V to +5V and 0 to +5V, when operated in dual supplies. The part can also be operated in single supply providing unipolar output ranges. The output amplifier is capable of developing +10V across a 2kΩ load.

PRODUCT HIGHLIGHTS

1. Complete 12-bit DAC:
   The AD7245/48 is a complete voltage output 12-bit DAC on one chip. This single-chip design of the DAC, reference and output amplifier is inherently more reliable than multi-chip designs.
2. Single or Dual Supply Operation:
   The voltage-mode configuration of the AD7245/48 allows operation from a single power supply rail. The part can also be operated from dual supplies to allow bipolar outputs.

DACPORT is a trademark of Analog Devices, Inc.

3. Low-Power Consumption:
   Fabrication on a high-speed Linear Compatible CMOS (LC^2MOS) process allows on-chip reference and amplifier circuits while retaining low-power consumption (60mW typical in single supply).
4. Fast Digital Interface:
   The high-speed logic allows direct interfacing to 16-bit microprocessors for the AD7245 and to most 8-bit microprocessors for the AD7248. An asynchronous $\overline{\text{CLR}}$ function on the AD7245 allows features such as power-on reset to be implemented.

PRELIMINARY TECHNICAL DATA

SPECIFICATIONS

(V_{DD} = +12V to +15V, ±5%. V_{SS} = −12V to −15V ±5%. AGND = DGND = 0V; BOFS, AGND connected unless otherwise stated. All specifications T_{min} to T_{max} unless otherwise stated).

Parameter	AD7245/48JN[1] AD7245/48AD	AD7245/48KN AD7245/48BD	AD7245/48SD	AD7245/48TD	Units	Test Conditions/Comments
STATIC PERFORMANCE						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Unipolar Offset Error	±2	±1	±2	±1	LSB max	
Bipolar Offset Error at 25°C	±2	±1	±2	±1	LSB max	BOFS connected to V_{REF}
Offset Error Temp. Coeff.	50	30	50	30	μV/°C max	
Full-Scale Error at 25°C	±2	±1	±2	±1	LSB max	
Full-Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Current						
I_{INH} at 25°C	−1	−1	−1	−1	μA max	
T_{min} to T_{max}	−10	−10	−10	−10	μA max	
I_{INL} at 25°C	100	100	100	100	μA max	
T_{min} to T_{max}	100	100	100	100	μA max	
Input Capacitance	8	8	8	8	pF max	
ANALOG OUTPUT						
Ranges	+5, +10	+5, +10	+5, +10	+5, +10	V	$R_L = 2k\Omega, C_L = 100pF$
	±5	±5	±5	±5	V	
D.C. Output Impedance	0.5	0.5	0.5	0.5	Ω typ	
Short Circuit Current	40	40	40	40	mA max	
Reference Output	4.95/5.05	4.95/5/05	4.95/5.05	4.95/5.05	V min/V max	Typically 5V
Reference Temperature Coefficient	20	20	20	20	ppm/°C typ	
Reference External Current	1	1	1	1	mA min	
DYNAMIC PERFORMANCE						
Output Voltage Settling Time						Settling Time to ± 1/2LSB
Positive Full-Scale Change	5	5	5	5	μs max	DAC Register all 0's to all 1's.
Negative Full-Scale Change	5	5	5	5	μs max	DAC Resgister all 1's to all 0's.
Negative Full-Scale Change (V_{SS} = 0V)	10	10	10	10	μs max	DAC Resister all 1's to all 0's.
Output Voltage Slew Rate	2	2	2	2	V/μs min	
Digital Feedthrough	50	50	50	50	nV secs typ	
POWER SUPPLIES						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	
V_{SS} Range	−11.4/−15.75	−11.4/−15.75	−11.4/−15.75	−11.4/−15.75	V min/V max	
I_{DD}						
at 25°C	5	5	5	5	mA max	
T_{min} to T_{max}	10	10	10	10	mA max	
I_{SS}						
at 25°C	4	4	4	4	mA max	
T_{min} to T_{max}	8	8	8	8	mA max	

NOTES

[1]Temperature ranges are as follows:
AD7245/48JN, KN 0 to 70°C
AD7245/48AD, BD −25°C to +85°C
AD7245/48SD, TD −55°C to +125°C

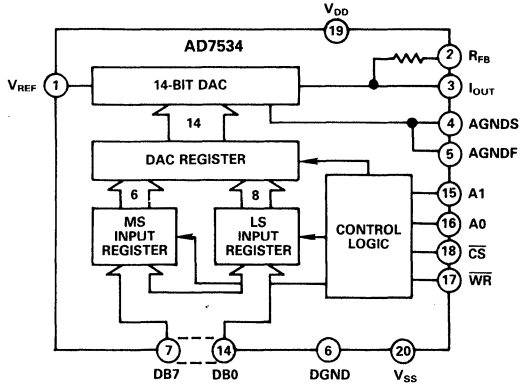
Specifications subject to change without notice.

LC²MOS
µP Compatible 14-Bit DAC
AD7534

FEATURES
- **All Grades 14-Bit Monotonic over the Full Temperature Range**
- **Full 4-Quadrant Multiplication**
- **Microprocessor Compatible with Double Buffered Inputs**
- **Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ**
- **Small 20-Pin Package**
- **Low Output Leakage (<20nA) over the Full Temperature Range**

APPLICATIONS
- **Microprocessor Based Control Systems**
- **Digital Audio Reconstruction**
- **High Precision Servo Control**
- **Control and Measurement in High Temperature Environments**

AD7534 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD7534 is a 14-bit monolithic CMOS D/A converter which uses thin-film resistors and laser trimming to achieve excellent linearity.

The device is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DAC. Address lines A0 and A1 control internal register loading and transfer.

A novel low leakage configuration (patent pending) enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp. The AD7534 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Montonicity
   The AD7534 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (pin 20) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3" 20-pin package.

SPECIFICATIONS[1]

(V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated)

Parameter	AD7534JN AD7534AD	AD7534KN AD7534BD	AD7534SD	AD7534TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic over temperature.
Differential Nonlinearity	±1	±1	±1	±1	LSB max	
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5 10	3.5 10	3.5 10	3.5 10	kΩ min kΩ max	Typical Input Resistance = 6kΩ
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over this range.
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	
I_{DD}	3 500	3 500	3 500	3 500	mA max μA max	All digital inputs V_{IL} or V_{IH} All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.
(V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV, Output Amplifier is AD544 except where stated).

Parameter	V_{DD} = +11.4V to +15.75V T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	100	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/√Hz typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AD, BD Versions: −25°C to +85°C
SD, TD Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	60	70	80	ns min	Data Setup Time
t_4	20	20	30	ns min	Data Hold Time
t_5	0	0	0	ns min	Chip Select to Write Setup Time
t_6	0	0	0	ns min	Chip Select to Write Hold Time
t_7	170	200	240	ns min	Write Pulse Width

NOTES
[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AD, BD Versions: −25°C to +85°C
SD, TD Versions: −55°C to +125°C

Specifications subject to change without notice.

3

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (Pin 19) to DGND . . . . . −0.3V, +17V
V_{SS} (Pin 20) to AGND . . . . . −15V, +0.3V
V_{REF} (Pin 1) to AGND . . . . . ±25V
V_{RFB} (Pin 2) to AGND . . . . . ±25V
Digital Input Voltage (Pins 7–18) to DGND . . −0.3V, V_{DD}
V_{PIN3} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial Plastic (JN, KN, versions) . . . . . 0 to +70°C
Industrial Ceramic (AD, BD, versions) . . −25°C to +85°C
Extended Ceramic (SD, TD, versions) . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

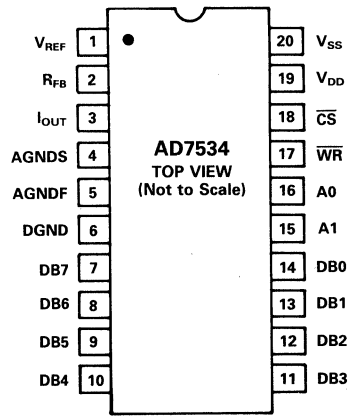
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Full Scale Error T_{min} to T_{max}	Temperature Range and Package: Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±2LSB	±8LSB	AD7534JN	AD7534AD	AD7534SD
±1LSB	±4LSB	AD7534KN	AD7534BD	AD7534TD

PIN CONFIGURATION



TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR
Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero with an external potentiometer.

DIGITAL TO ANALOG GLITCH IMPULSE
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. The measurement takes place with V_{REF} = AGND.

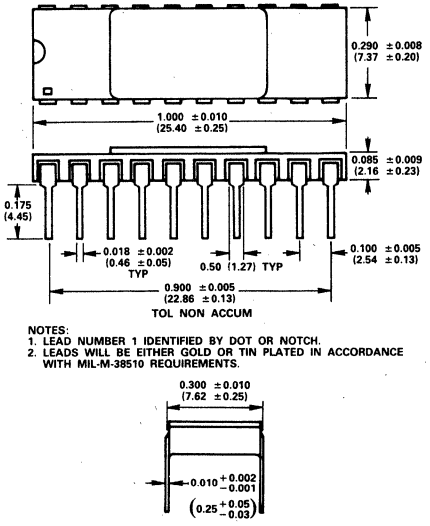
OUTPUT CAPACITANCE
Capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT
Current which appears at I_{OUT} with the DAC register loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

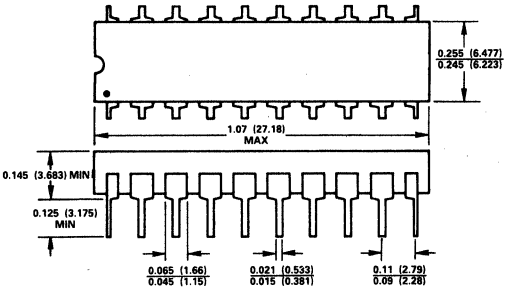
MECHANICAL INFORMATION
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

20-PIN CERAMIC DIP (SUFFIX D)

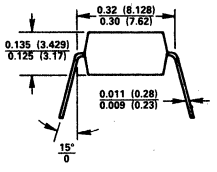


NOTES:
1. LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
2. LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

20-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

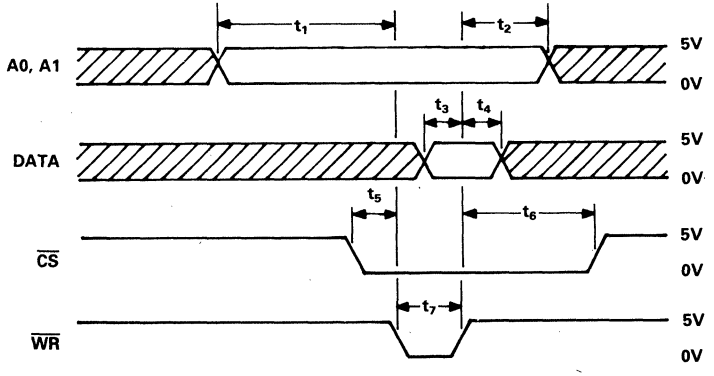


Pin	Function	Description
1	V_{REF}	Reference Input Voltage
2	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
3	I_{OUT}	Current Output Terminal
4	AGNDS	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
5	AGNDF	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
6	DGND	Digital Ground
7	DB7	Data Bit 7
8	DB6	Data Bit 6
9	DB5	Data Bit 5 or Data Bit 13 (DAC MSB)
10	DB4	Data Bit 4 or Data Bit 12
11	DB3	Data Bit 3 or Data Bit 11
12	DB2	Data Bit 2 or Data Bit 10
13	DB1	Data Bit 1 or Data Bit 9
14	DB0	Data Bit 0 or Data Bit 8
15	A1	Address line 1
16	A0	Address line 0
17	$\overline{WR}$	Write input. Active low.
18	$\overline{CS}$	Chip Select Input. Active low.

$\overline{WR}$	$\overline{CS}$	A1	A0	Function
X[1]	1	X	X	Device not selected
1	X	X	X	No data transfer
0	0	0	0	DAC loaded directly from Data Bus[2]
0	0	0	1	MS Input Register loaded from Data Bus
0	0	1	0	LS Input Register loaded from Data Bus
0	0	1	1	DAC Register loaded from Input Registers.

NOTES
1. X = Don't Care
2. When $A_1 = 0$, $A_0 = 0$ all DAC registers are transparent, so by placing all 0's or all 1's on the data inputs the user can load the DAC to zero or full scale output in one write operation. This facility simplifies system calibration.

19	V_{DD}	+12V to +15V supply input.
20	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figures 4, 5 or 6 for recommended circuitry.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD7534 Timing Diagram

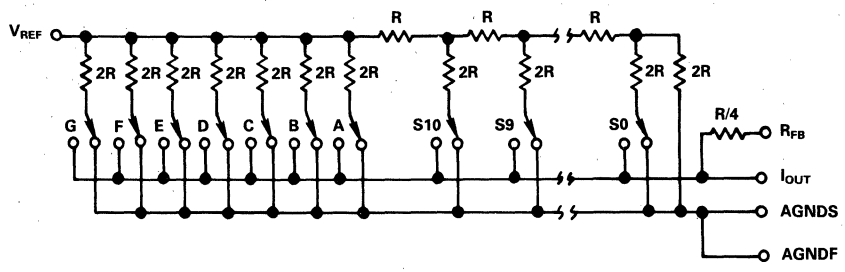


Figure 2. Simplified Circuit Diagram for the AD7534 D/A Section

CIRCUIT INFORMATION – D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7534 D/A section. The three MSB's of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSB's of the Data Word drive an inverted R-2R ladder which steers the binarily weighted current available to it between I_{OUT} and AGNDF.

If I is taken as the input current at V_{REF} the input current to the R-2R ladder is I/8. 7/8 I flows in the parallel ladder structure. Switches A-G steer binarily weighted current between I_{OUT} and AGNDF.

The input resistance at V_{REF} is constant and may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7534 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference

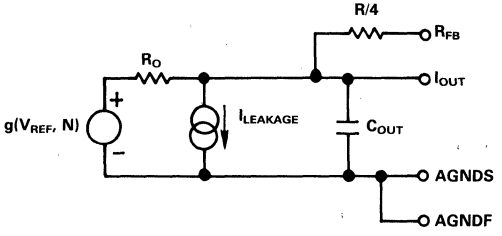


Figure 3. AD7534 Equivalent Analog Output Circuit

input voltage, V_{REF}, and the transfer function of the R-2R ladder, N.

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

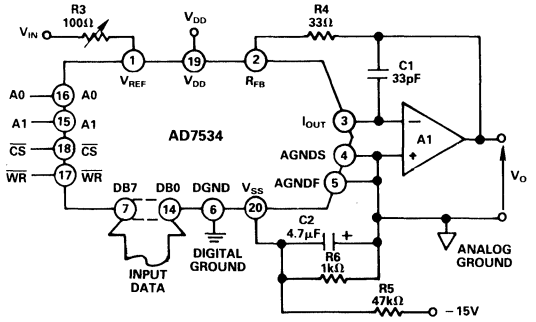


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7534

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 4.

Calibration codes for zero and full scale adjust (all 0's, all 1's) can be loaded in one write operation (see Pin Function Description).

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e., ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R3 so that $V_O = -V_{IN}\left(\frac{16383}{16384}\right)$

In fixed reference applications full scale can also be adjusted by omitting R3 and R4 and trimming the reference voltage magnitude.

For high temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7534, Gain Error trimming is not necessary.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R3 for V_O = 0V. Alternatively, one can omit R3 and R4 and adjust the ratio of R7 and R8 for V_O = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R9.

Resistors R7, R8 and R9 should be matched to 0.003%. Mismatch of R7 and R8 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficient match.

The code table for Figure 5 is given in Table II.

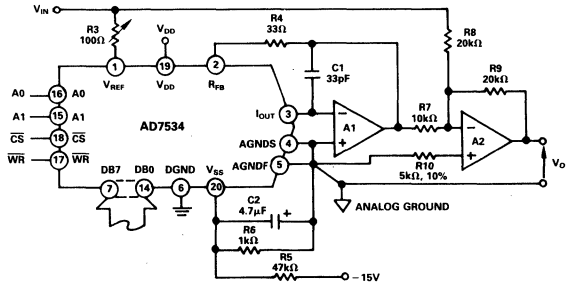


Figure 5. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

GROUNDING TECHNIQUES

Since the AD7534 is specified for high accuracy, it is important to use a proper grounding technique. The two AGND pins (AGNDF and AGNDS) provide flexibility in this respect. In Figure 4, AGNDS and AGNDF are externally shorted and A2 is not used. Voltage drops due to bond wire resistances are not compensated for in this circuit. This means that an extra linearity error of less than 0.1LSB is added to the DAC linearity error. If the user wishes to eliminate this extra error, then the circuit of Figure 6 should be used. Here, A2 is used to maintain AGNDS at Signal Ground potential. By using the Force, Sense technique all switch contacts on the DAC are at exactly the same potential and any error due to bond wire resistance is eliminated.

Figure 7 shows a Printed Circuit Board layout for the AD7534 with a single output amplifier. The input to V_{REF} (pin 1) is shielded to reduce ac feedthrough while the digital inputs are shielded to minimize digital feedthrough. The tracks connecting I_{OUT} and AGNDS to the inverting and noninverting op amp inputs are kept as short as possible. Gain trim components, R3 and R4, have been omitted.

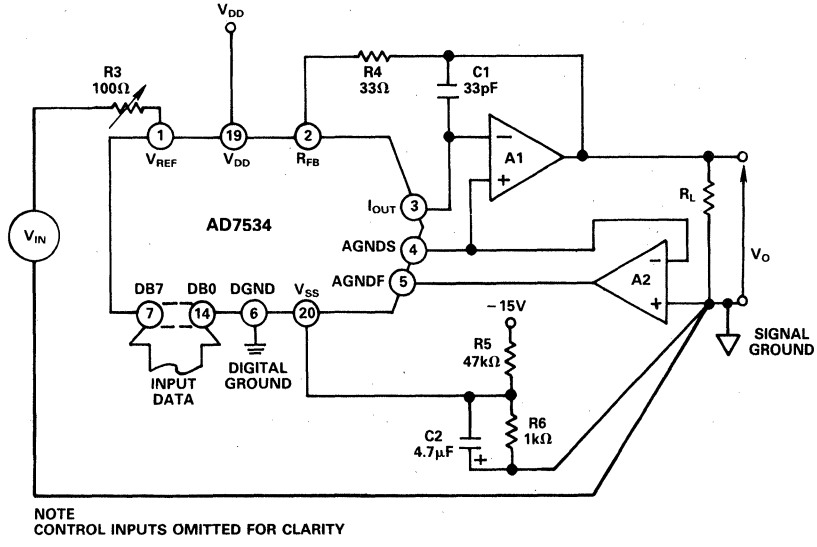


Figure 6. Unipolar Binary Operation with Forced Ground

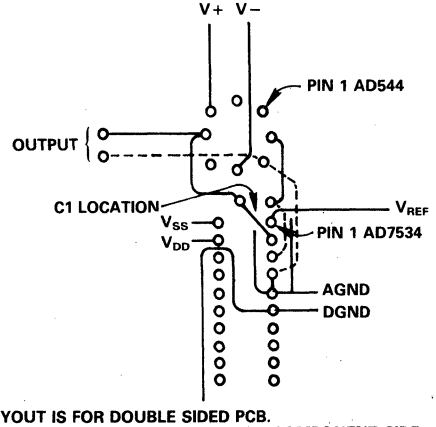


Figure 7. Suggested Layout for AD7534 Incorporating Output Amplifier

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 6

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A2 for minimum potential at AGNDS. This potential should be ≤30μV with respect to Signal Ground.
3. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R3 so that $V_O = -V_{IN}\left(\frac{16383}{16384}\right)$

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7534 features a leakage reduction configuration to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (pin 20) is tied to AGND then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately $-0.3V$ as in Figures 4, 5 and 6. A simple resistor divider (R5, R6) produces $-312mV$ from $-15V$. The capacitor C2 in parallel with R6 is an integral part of the low leakage configuration and must be $4.7\mu F$ or greater. Figure 8 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

OP AMP SELECTION

In choosing an amplifier to be used with the AD7534, three parameters are of prime importance. These are Input Offset Voltage (V_{OS}), Input Bias Current, (I_{BIAS}) and Offset Voltage Drift. To maintain specified accuracy with V_{REF} at 10V, V_{OS} must be less than $30\mu V$ while I_{BIAS} should be less than 2nA. Also the open loop gain of the amplifier must be sufficiently high to keep $V_{OS} \leq 30\mu V$ for the full output voltage range. Thus for a max output of 10V, A_{VOL} must be greater than 340,000.

An amplifier with low offset voltage drift is required to give the desired system accuracy over an operating temperature range.

At low frequencies the AD OP-07 satisfies the above requirements and in most cases will not need an offset adjust potentiometer.

For high frequency operation, one may use a wide bandwidth amplifier such as the AD544 or the LF356 with either an offset adjust potentiometer or automatic nulling circuitry.

The choice of amplifier depends entirely on the required system accuracy, the required temperature range, and the operating frequency.

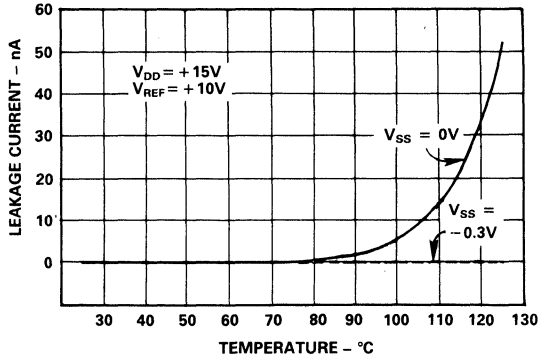


Figure 8. Graph of Typical Leakage Current vs. Temperature for AD7534

MICROPROCESSOR INTERFACING

AD7534 – 8085A INTERFACE

A typical interface circuit for the AD7534 and the 8085A microprocessor is given in Figure 9. The microprocessor sees the DAC as four memory locations, identified by address lines A0, A1. In standard operation, three of these memory locations are used. A sample program for loading the DAC with a 14-bit word is given in Table III. The AD7534 has address locations 3000–3003.

The six MSBs are written into location 3001, and the eight LSBs are written to 3002. Then with a write instruction to 3003 the full 14-bit word is loaded to the DAC register and the analog equivalent appears at the output.

AD7534 – 8086 INTERFACE

The AD7534 may be interfaced to the 16-bit 8086 microprocessor using the circuit of Figure 10. The bottom 8 bits (AD0–AD7) of the 16-bit data bus are connected to the DAC data bus. The 14-bit word is loaded in two bytes using the MOV instruction. A further MOV loads the DAC register and causes the analog data to appear at the converter output. For the example given here, the appropriate DAC register addresses are D002, D004, D006. The program for loading the DAC is given below in Table IV.

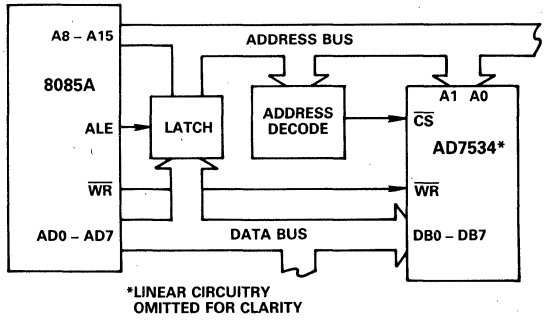


Figure 9. AD7534 – 8085A Interface

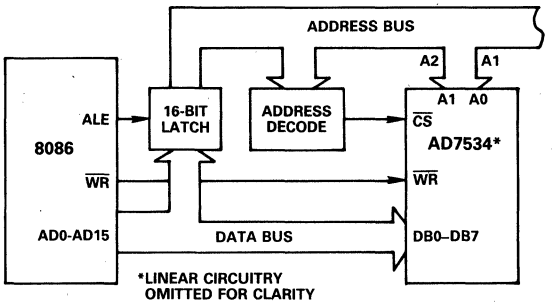


Figure 10. AD7534 – 8086 Interface Circuit

Address	Op-Code	Mnemonic
2000	26	MVI H,# 30
01	30	
02	2E	MVI L,# 01
03	01	
04	3E	MVI A,# "MS"
05	"MS"	
06	77	MOV M,A
07	2C	INR L
08	3E	MVI A,# "LS"
09	"LS"	
0A	77	MOV M, A
0B	2C	INR L
0C	77	MOV M,A
200D	CF	RST I

Table III. Program Listing for Figure 9

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CX, CS	: DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	: TO CODE SEGMENT REGISTER
04	BF02D0	MOV DI, # D002	: LOAD DI WITH D002
07	C605"MS"	MOV MEM,# "MS"	: MS INPUT REGISTER LOADED WITH "MS"
0A	47	INC DI	
0B	47	INC DI	
0C	C605"LS"	MOV MEM,# "LS"	: LS INPUT REGISTER LOADED WITH "LS"
0F	47	INC DI	
10	47	INC DI	
11	C60500	MOV MEM, # 00	: CONTENTS OF INPUT REGISTERS ARE LOADED TO THE DAC REGISTER.
14	EA0000	JMP MEM	: CONTROL IS RETURNED TO THE MONITOR
17	00FF		PROGRAM

Table IV. Sample Program for Loading AD7534 from 8086

AD7534 – MC6809 INTERFACE

Figure 11 shows an interface circuit which enables the AD7534 to be programmed using the MC6809 8-bit microprocessor. By making use of the 16-bit D Accumulator, the transfer of data is simplified. The two key processor instructions are:

LDD Load D Accumulator from memory.
STD Store D Accumulator to memory.

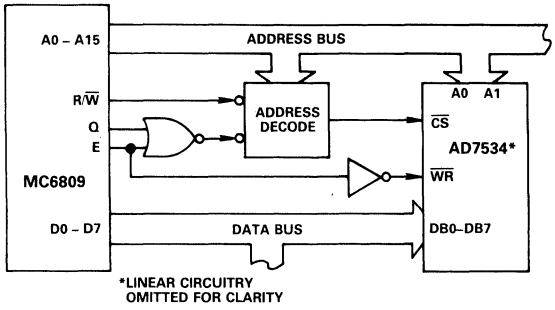


Figure 11. AD7534 – MC6809 Interface Circuit

AD7534 – 6502 INTERFACE

The interface circuit for the 6502 microprocessor is shown in Figure 12.

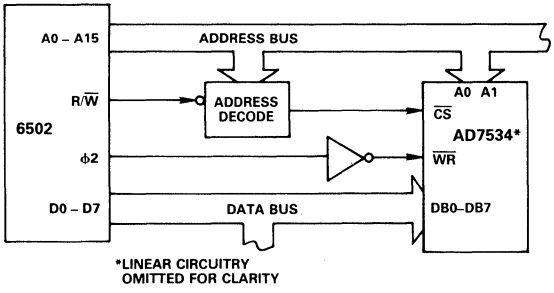


Figure 12. AD7534 – 6502 Interface

AD7534 – Z80 INTERFACE

Interfacing to the Z80 microprocessor requires a minimal amount of extra components. The circuit consists of the Z80 processor, the AD7534 and an address decoder for the DAC. Figure 13, below, illustrates the circuit.

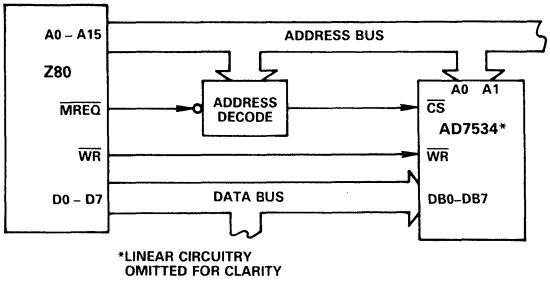


Figure 13. AD7534 – Z80 Interface

AD7534 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7534 is accomplished using the circuit of Figure 14. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

```
                ·A2 E003                    Address Register 2 is loaded with E003.
01000           MOVE.W      # W, D0         The desired DAC data, W, is loaded
                                            into Data Register 0. W may be any value
                                            between 0 and 16383 (decimal) or 0
                                            and 3FFF (hexadecimal).
                MOVEP.W     D0,$0000 (A2)   The data W is transferred between D0
                                            and the Input Registers of the DAC.
                                            The high order byte of data is trans-
                                            ferred first. The memory address is
                                            specified using the address register in-
                                            direct plus displacement addressing
                                            mode. The address used in this instance
                                            (E003) is odd and so data is transferred
                                            on the low order half of the data bus
                                            (D0-D7).
                MOVE.W      D0,$E006        This instruction provides appropriate
                                            signals to transfer the data W from the
                                            DAC Input Registers to the DAC Regis-
                                            ter, which controls the switches in the
                                            14-bit D/A structure.
                MOVE.B      # 228,D7       Control is returned to the System Monitor
                                            Program using these two insructions.
                TRAP        # 14
```

Since only the lower half of the Data Bus is used in this interfacing system, it is also suitable for use with the MC68008. This provides the user with an eight bit data bus instead of the MC68000's sixteen bit data bus.

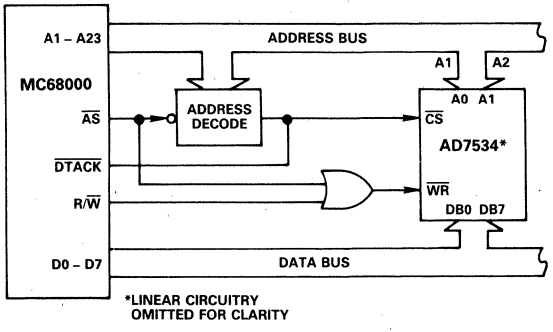


Figure 14. AD7534 – MC68000 Interface

DIGITAL FEEDTHROUGH

In the preceeding interface configurations, most digital inputs to the AD7534 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 15 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.

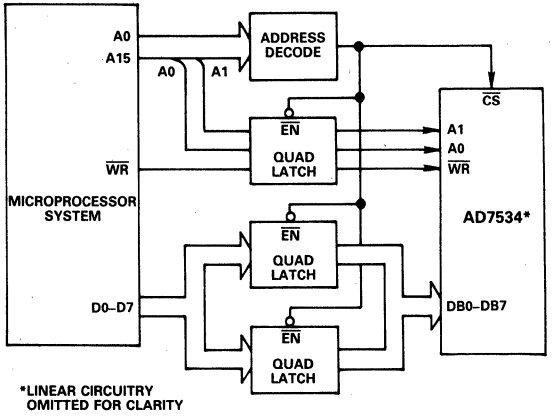


Figure 15. AD7534 Interface Circuit Using Latches to Minimize Digital Feedthrough

ANALOG DEVICES

LC²MOS
µP Compatible 14-Bit DAC

AD7535

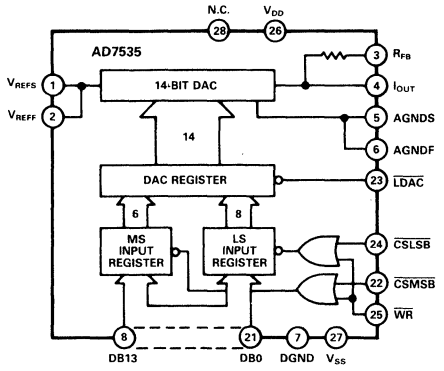
FEATURES

All Grades 14-Bit Monotonic over the Full Temperature Range
Full 4 Quadrant Multiplication
Microprocessor Compatible with Double Buffered Inputs
Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

Microprocessor Based Control Systems
Digital Audio
Precision Servo Control
Control and Measurement in High Temperature Environments

AD7535 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7535 is a 14-bit monolithic CMOS D/A converter which uses laser trimmed thin-film resistors to achieve excellent linearity.

Standard Chip Select and Memory Write logic is used to access the DAC.

A novel low leakage configuration (patent pending) enables the AD7535 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp. The AD7535 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Monotonicity
   The AD7535 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (pin 27) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors. When interfacing to 8-bit processors $\overline{CSMSB}$ and $\overline{CSLSB}$ are separate and the 8-bit data bus is connected to both the MS Input Register and the LS Input Register. For straight 14-bit parallel loading $\overline{CSMSB}$ and $\overline{CSLSB}$ are tied together giving one chip select to load the 14-bit word.

SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN4} = V_{PIN5} = 0V, V_{SS} = −300mV All specifications T_{min} to T_{max} unless otherwise stated.)

Parameter	AD7535JN AD7535AD	AD7535KN AD7535BD	AD7535SD	AD7535TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]; ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 4)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input resistance, pin 1	3.5 10	3.5 10	3.5 10	3.5 10	kΩ min kΩ max	Typical Input Resistance = 6kΩ
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV, Output Amplifier is AD544 except where stated).

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital to Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AD, BD Versions: −25°C to +85°C
SD, TD Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Guaranteed by Product Assurance testing.

[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1]

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	LDAC Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

NOTES
[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AD, BD Versions: −25°C to +85°C
SD, TD Versions: −55°C to +125°C

Specifications subject to change without notice.

3

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (pin 26) to DGND . . . . . −0.3V, +17V
V_{SS} (pin 27) to AGND . . . . . −15V, +0.3V
V_{REFS} (pin 1) to AGND . . . . . ±25V
V_{REFF} (pin 2) to AGND . . . . . ±25V
V_{RFB} (pin 3) to AGND . . . . . ±25V
Digital Input Voltage (pins 8–25) to DGND . . −0.3V, V_{DD}
V_{PIN4} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any package)
To +75°C 1000mW
Derates above +75°C . . . . . 10mW/°C

Operating Temperature Range
Commercial Plastic (JN, KN versions) . . . . . 0 to +70°C
Industrial Ceramic (AD, BD versions) . . −25°C to +85°C
Extended Ceramic (SD, TD versions) . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

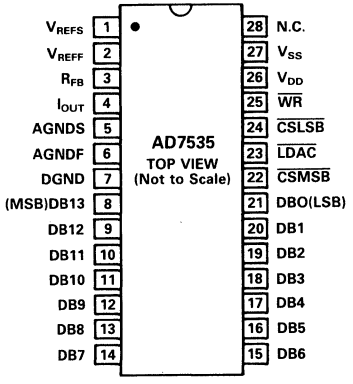
CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Full Scale Error T_{min} to T_{max}	Temperature Range and Package: Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±2LSB	±8LSB	AD7535JN	AD7535AD	AD7535SD
±1LSB	±4LSB	AD7535KN	AD7535BD	AD7535TD

PIN CONFIGURATION



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

FULL-SCALE ERROR

Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero with an external potentiometer.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE

This is the capacitance from I_{OUT} to AGND.

OUTPUT LEAKAGE CURRENT

Output Leakage Current is current which appears at I_{OUT} with the DAC register loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

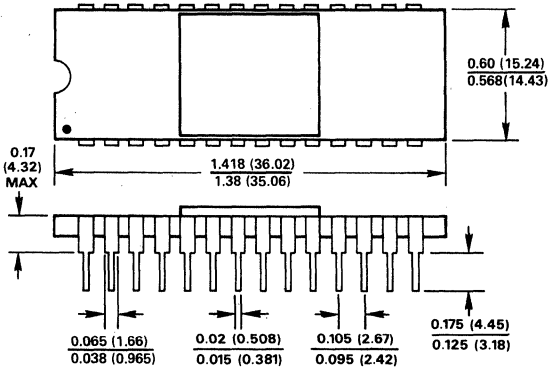
This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded to all zeros.

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

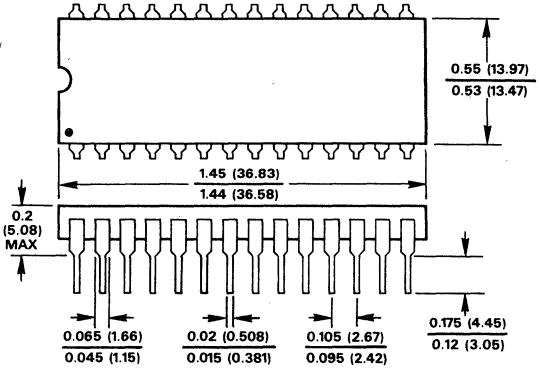
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)

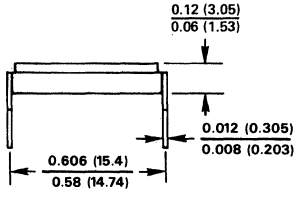


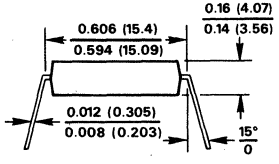
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

28-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42



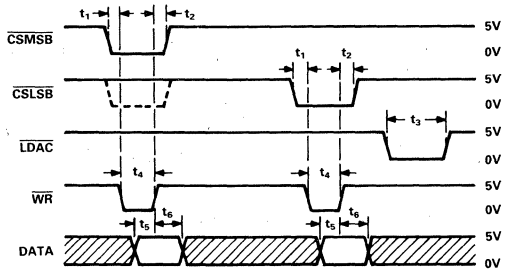


Pin	Function	Description
1	V_{REFS}	Voltage Reference sense pin
2	V_{REFF}	Voltage Reference force pin. If a remote voltage reference is being used V_{REFF} and V_{REFS} can be used in a Kelvin configuration to compensate for IR drop along the V_{REF} line. See Figure 7.
3	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
4	I_{OUT}	Current Output Terminal.
5	A_{GNDS}	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
6	A_{GNDF}	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
7	DGND	Digital Ground
8	DB13	Data Bit 13. DAC MSB
9	DB12	Data Bit 12
10	DB11	Data Bit 11
11	DB10	Data Bit 10
12	DB9	Data Bit 9
13	DB8	Data Bit 8
14	DB7	Data Bit 7
15	DB6	Data Bit 6
16	DB5	Data Bit 5
17	DB4	Data Bit 4
18	DB3	Data Bit 3
19	DB2	Data Bit 2
20	DB1	Data Bit 1
21	DB0	Data Bit 0. DAC LSB
22	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active LOW input.
23	$\overline{LDAC}$	Asynchronous Load DAC input. Active LOW.
24	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input.
25	$\overline{WR}$	Write input. Active LOW.

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

26	V_{DD}	+ 12V to + 15V supply input
27	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 4, 5, 6 or 7 for recommended circuitry.
28	N.C.	No connection



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7535 Timing Diagram

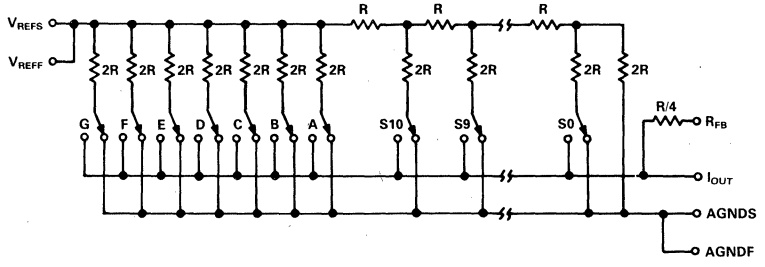


Figure 2. Simplified Circuit Diagram for the AD7535 D/A Section

CIRCUIT INFORMATION – D/A SECTION

Figure 2 shows a simplified circuit diagram for the AD7535 D/A section. The three MSB's of the 14-bit Data Word are decoded to drive the seven switches A-G. The 11 LSB's of the Data Word consist of an R-2R ladder operated in a current steering configuration.

The R-2R ladder current is 1/8 of the total reference input current. 7/8 I flows in the parallel ladder structure. Switches A-G steer equally weighted currents between I_{OUT} and A_{GNDF}.

Since the input resistance at V_{REF} is constant, it may be driven by a voltage source or a current source of positive or negative polarity.

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7535 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O denotes the equivalent output resistance of the DAC which varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference

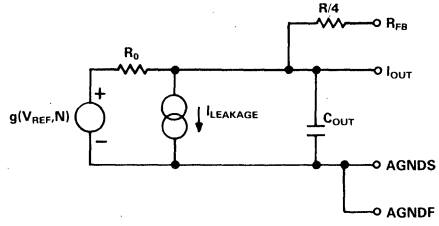


Figure 3. AD7535 Equivalent Analog Output Circuit

input voltage, V_{REF}, and the transfer function of the DAC ladder, N.

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2 quadrant multiplication. The code table for Figure 4 is given in Table I.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when high speed op-amps are used.

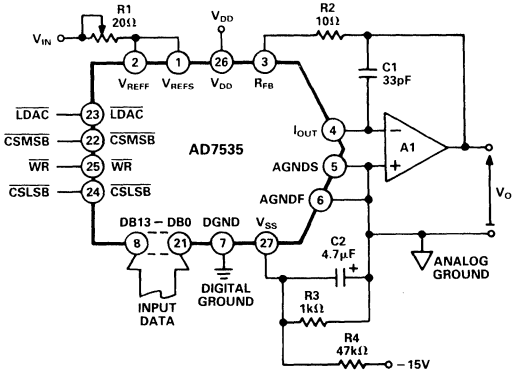


Figure 4. Unipolar Binary Operation

Binary Number In DAC Register	Analog Output, V_{OUT}
MSB LSB	
11 1111 1111 1111	$-V_{IN}\left(\frac{16383}{16384}\right)$
10 0000 0000 0000	$-V_{IN}\left(\frac{8192}{16384}\right) = -1/2\,V_{IN}$
00 0000 0000 0001	$-V_{IN}\left(\frac{1}{16384}\right)$
00 0000 0000 0000	0V

Table I. Unipolar Binary Code Table for AD7535

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 4.

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R1 so that $V_O = -V_{IN}\frac{(16383)}{(16384)}$

In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

For high temperature applications resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Gain T.C. and Gain Error specifications of the AD7535, Gain Error trimming is not necessary.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 5. Offset binary coding is used.

With the DAC loaded to 10 0000 0000 0000, adjust R1 for $V_O = 0V$. Alternatively, one can omit R1 and R2 and adjust the ratio of R5 and R6 for $V_O = 0V$. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R7.

Resistors R5, R6 and R7 should be ratio matched to 0.006%. Mismatch of R5 and R6 causes both offset and full scale error. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

A range of precision voltage dividers, manufactured by Vishay, offers a suitable solution to implementing the bipolar circuit described above. The resistor networks are TCR and Ratio Matched, giving excellent performance over temperature.

The code table for Figure 5 is given in Table II.

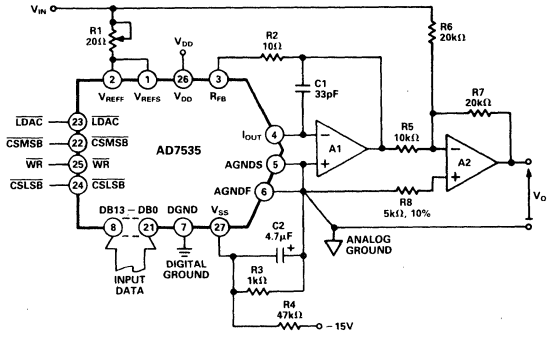


Figure 5. Bipolar Operation

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
01 1111 1111 1111	$-V_{IN}\left(\frac{1}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 5.

GROUNDING TECHNIQUES

Since the AD7535 is specified for high accuracy it is important to use a proper grounding technique. The two AGND pins (AGNDF and AGNDS) provide flexibility in this respect. In Figure 4, the AD7535 is connected with the signal ground for the load located close to the DAC. There is no possibility of a voltage drop along the signal ground due to track resistance.

If the signal ground for the load is located at a distance from the DAC then the configuration of Figure 6 should be used. A_2 compensates for the error due to IR voltage drop between the DAC's internal Analog ground and the load signal ground.

Figure 7 shows a remote voltage reference driving the AD7535. Op-amps A2 and A3 compensate for voltage drops along the reference input line and the analog ground line.

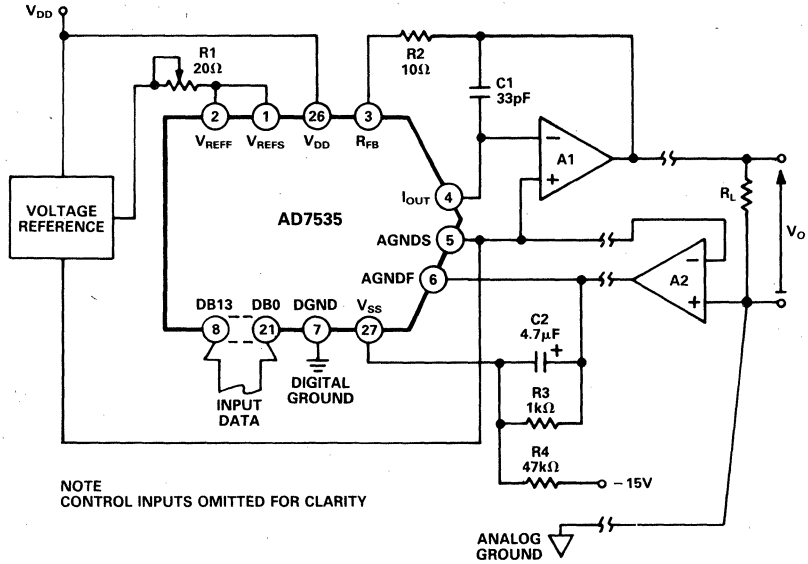


Figure 6. Unipolar Binary Operation with Forced Ground for Remote Load

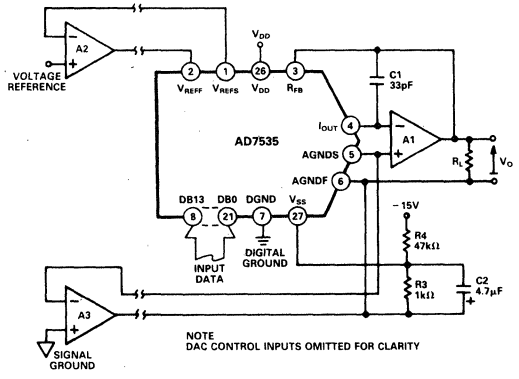


Figure 7. Driving the AD7535 with a Remote Voltage Reference

ZERO OFFSET AND GAIN ADJUSTMENT FOR FIGURE 6

Zero Offset Adjustment

1. Load DAC register with all 0's.
2. Adjust offset of amplifier A2 for a minimum potential at AGNDS. This potential should be ≤30μV with respect to Signal Ground. Adjust offset of amplifier A1 so that V_O is at a minimum (i.e. ≤30μV).

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R1 so that $V_O = -V_{IN}\frac{(16383)}{(16384)}$

LOW LEAKAGE CONFIGURATION

For CMOS Multiplying D/A converters, as the device is operated at higher temperatures the output leakage current increases. For a 14-bit resolution system, this can be a significant source of error. The AD7535 features a leakage reduction configuration (patent pending) to keep the leakage current low over an extended temperature range. One may operate the device with or without this configuration. If V_{SS} (pin 27) is tied to A_{GND} then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to a voltage of approximately $-0.3V$ as in Figures 4, 5, 6 and 7. A simple resistor divider (R3, R4) produces approximately $-300mV$ from $-15V$. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be $4.7\mu F$ or greater. Figure 8 is a plot of leakage current versus temperature for both conditions. It clearly shows the improvement gained by using the low leakage configuration.

OP-AMP SELECTION

In choosing an amplifier to be used with the AD7535, three parameters are of prime importance. These are (1) Input Offset Voltage (V_{OS}), (2) Input Bias Current (I_B), (3) Offset Voltage Drift (TC V_{OS}). To maintain specified accuracy with V_{REF} at 10V, V_{OS} must be less than $30\mu V$ while I_B should be less than 2nA. It is important that the amplifier Open Loop Gain, A_{VOL}, be sufficiently large to keep $V_{OS} \leq 30\mu V$ for the full output voltage range. For a maximum output of 10V, A_{VOL} must be greater than 340,000.

The AD OP-07 series of op-amps have a very low V_{OS} ($25\mu V$) and can be used as the output amplifier for the AD7535 without any external adjustment of Offset Voltage. In the Forced Ground configuration of Figure 6, one can use an AD OP-07 for amplifier A2. Settling time to 0.003% for the AD OP-07 is typically greater than $50\mu s$.

For faster settling time, one can use the AD544 series of op amps. Typically this settles to 0.003% (14-bits) in $5\mu s$. Even faster settling time can be achieved using the HA-2620 series of op-amps.

For operation over a wide temperature range Offset Voltage Drift and Bias Current Drift are critical parameters. The OP-27 and OP-37 series of op-amps exhibit extremely low Offset Voltage Drift and the AD544 has very low Bias Current Drift.

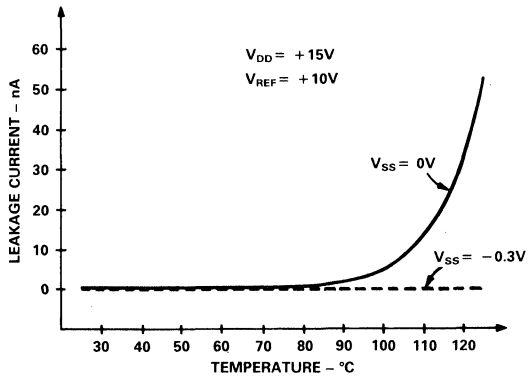


Figure 8. Graph of Typical Leakage Current vs Temperature for AD7535

MICROPROCESSOR INTERFACING

AD7535 – 8086A INTERFACE

The versatility of the AD7535 loading structure allows interfacing to both 8- and 16-bit microprocessor systems. Figure 9 shows the 8086 16-bit processor interfacing to a single device. In this setup the double buffering feature of the DAC is not used. AD0–AD13 of the 16-bit data bus are connected to the DAC data bus (DB0–DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 9 is given in Table III.

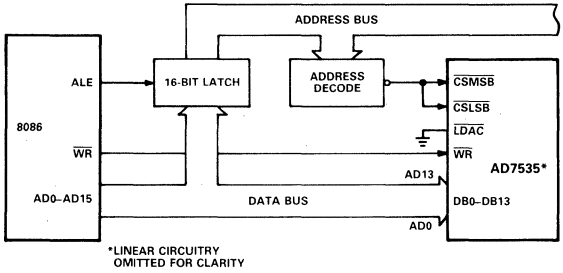


Figure 9. AD7535 – 8086 Interface Circuit

In a multiple DAC system the double buffering of the AD7535 allows the user to simultaneously update all DAC's. In Figure 10, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e. $\overline{\text{LDAC}}$) is brought low, updating all the DACs simultaneously.

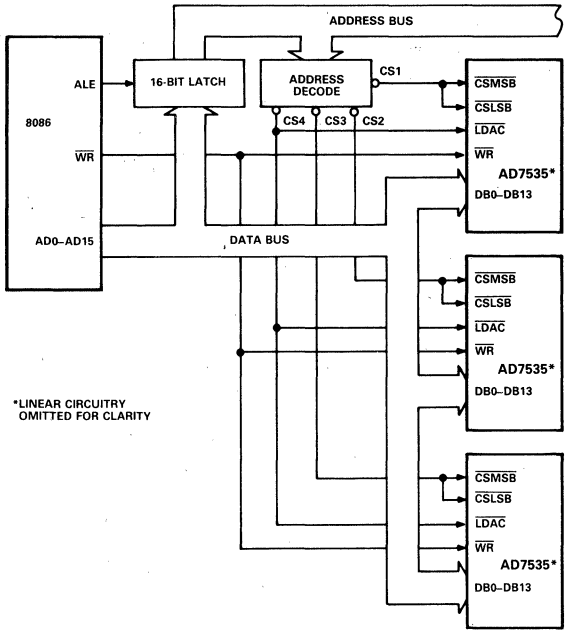


Figure 10. AD7535 – 8086 Interface: Multiple DAC System

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CX, CS	:	DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	:	TO CODE SEGMENT REGISTER
04	BF00D0	MOV DI, # D000	:	LOAD DI WITH D000
07	C705"YZWX"	MOV MEM, # YZWX"	:	DAC LOADED WITH WXYZ
0B	EA0000		:	CONTROL IS RETURNED TO THE
0E	00FF			MONITOR PROGRAM

Table III. Sample Program for Loading AD7535 from 8086

AD7535 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7535 is accomplished using the circuit of Figure 11. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

01000	MOVE.W	#W,D0	The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 16383 (decimal) or 0 and 3FFF (hexademical).
	MOVE.W	D0,$E000	The data W is transferred between D0 and the DAC Register.
	MOVE.B	#228,D7	Control is returned to the System Monitor Program using these two instructions.
	TRAP	#14	

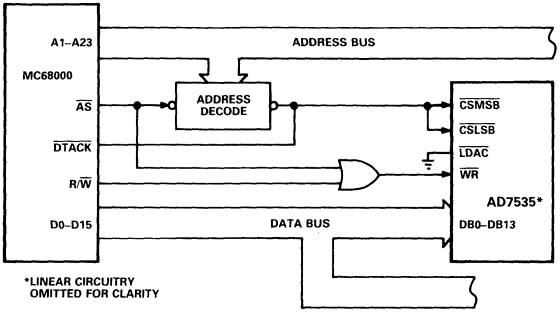


Figure 11. AD7535 – MC68000 Interface

AD7535 – Z80 INTERFACE

Though the AD7535 is primarily intended for use either with 16-bit microprocessors or in stand alone applications, it can also be interfaced to 8-bit processor systems. Figure 12 is an interface circuit for the Z80 microprocessor.

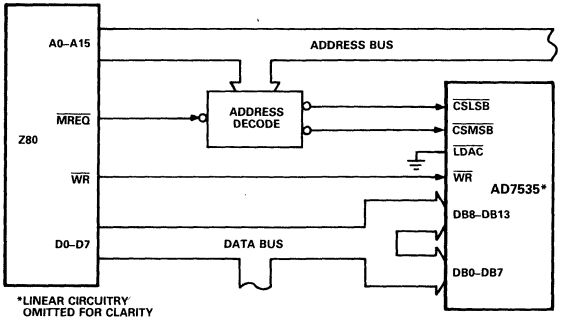


Figure 12. AD7535 – Z80 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7535 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

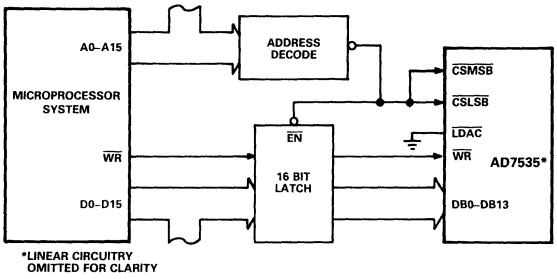


Figure 13. AD7535 Interface Circuit Using Latches to Minimize Digital Feedthrough

ANALOG DEVICES

LC²MOS
14-Bit µP Compatible DAC
AD7536

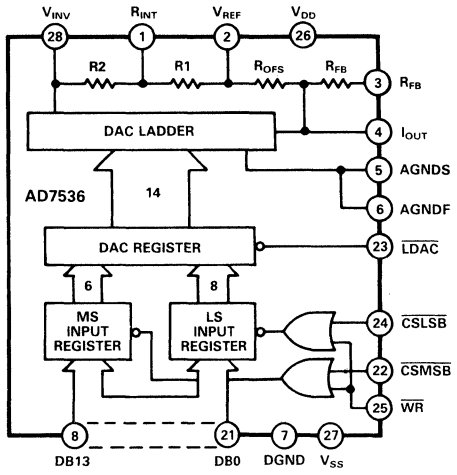
FEATURES
- **Full 4-Quadrant Multiplication without External Resistors**
- **All Grades 14-Bit Monotonic over the Full Temperature Range**
- **Low Output Leakage (<20nA) over the Full Temperature Range**
- **Low Gain Temperature Coefficient, 2ppm/°C**

APPLICATIONS
- **Control and Measurement in High Temperature Environments**
- **Digital Audio**
- **Precision Servo Control**
- **All Microprocessor Based Control Systems**

GENERAL DESCRIPTION
The AD7536 is a 14-bit monolithic CMOS D/A converter. The part is laser trimmed and specified as a dedicated bipolar DAC. The resistors needed for 4-quadrant multiplication are contained on the chip. Thus, the user requires only the AD7536, a voltage reference and two op-amps for bipolar operation. The AD7536 has the same low leakage configuration (patent pending) as the other members of the 14-bit CMOS DAC family. The excellent output leakage current characteristics also ensure exceptional stability of linearity and gain error over the full temperature range.

The device is speed compatible with most microprocessors and accepts TTL or 5V CMOS logic level inputs. There is standard Chip Select and Memory Write logic for easy interfacing. The AD7536 has full protection against CMOS "latch-up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp.

AD7536 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS
1. Bipolar Operation
   The AD7536 gives the user 4-Quadrant Multiplication without any external resistors.
2. Guaranteed Monotonicity
   14-Bit monotonicity is guaranteed over the full temperature range for all grades.
3. Low Output Leakage
   The device has excellent output leakage current characteristics at all temperatures.

SPECIFICATIONS[1] (V_{DD} = +11.4V to +15.75V[2], V_{REF} = +10V; V_{PIN4} = V_{PIN5} = 0V, V_{SS} = −300mV All specifications T_{min} to T_{max} unless otherwise stated. See Figure 6 for Suggested Specification Circuit[3])

Parameter	AD7536JN AD7536AD	AD7536KN AD7536BD	AD7536SD	AD7536TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	1LSB = $2V_{REF}/2^{14}$
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Gain Error	±16	±8	±16	±8	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Offset Error	±4	±4	±4	±4	LSB max	Error due to mismatch between R_{FB} and offset resistor. It also includes leakage current to I_{OUT} and is measured when DAC is loaded with all 0's.
Gain Temperature Coefficient[4], ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical Value is 2ppm/°C
Offset Temperature Coefficient[4] ΔOffset/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical Value is 1ppm/°C
INPUT RESISTANCES						
V_{REF} Input Resistance, Pin 2	3	3	3	3	kΩ min	Typical Input Resistance = 6kΩ
	13	13	13	13	kΩ max	
V_{INV} Input Resistance, Pin 28	2	2	2	2	kΩ min	Typical Input Resistance = 4kΩ
	8	8	8	8	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[4]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V_{min}/V_{max}	Specification guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range.
I_{DD}	4	4	4	4	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}
Power Supply Rejection ΔGain/ΔV_{DD}	±0.02	±0.02	±0.02	±0.02	% per % max	ΔV_{DD} = V_{DD} max − V_{DD} min

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. (V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V OR −300mV, See Figure 6 for Suggested Specification Circuit[3]).

Parameter	T_A = 25°C	T_A = T_{min}, T_{max}	Units	Test Conditions/Comments
Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	50	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[5]	4	–	mV p-p typ	V_{REF} = ±10V, 1kHz sine wave DAC register loaded with 10 0000 0000 0000
Output Capacitance				
C_{OUT} (Pin 4)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 4)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	50	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AD, BD Versions: −25°C to +85°C
SD, TD Versions: −55°C to +125°C

[2]Specifications are guaranteed for a V_{DD} of +11.4V to +15.75V. At V_{DD} = 5V, the device is fully functional with degraded specifications.

[3]Only the D.U.T. (i.e., AD7536) is subjected to full temperature conditions.

[4]Guaranteed by Product Assurance testing.

[5]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

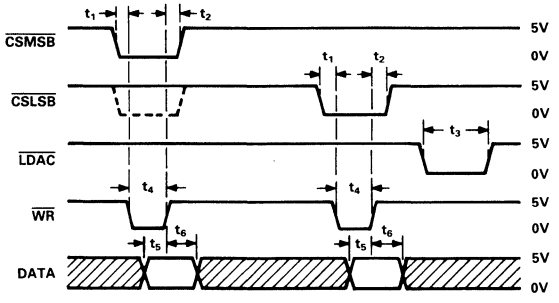
Specifications subject to change without notice.

TIMING CHARACTERISTICS

(V_{DD} = +11.4V to +15.75V, V_{REF} = +10V, V_{PIN4} = V_{PIN5} = 0V, V_{SS} = 0V or −300mV
All specifications T_{min} to T_{max} unless otherwise stated. See Figure 1 for Timing Diagram.)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_3	170	200	240	ns min	LDAC Pulse Width
t_4	170	200	240	ns min	Write Pulse Width
t_5	140	160	180	ns min	Data Setup Time
t_6	20	20	30	ns min	Data Hold Time

Specifications subject to change without notice.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$
3. IF $\overline{LDAC}$ IS ACTIVATED PRIOR TO THE RISING EDGE OF $\overline{WR}$, THEN IT MUST STAY LOW FOR t_3 OR LONGER AFTER $\overline{WR}$ GOES HIGH.

Figure 1. AD7536 Timing Diagram

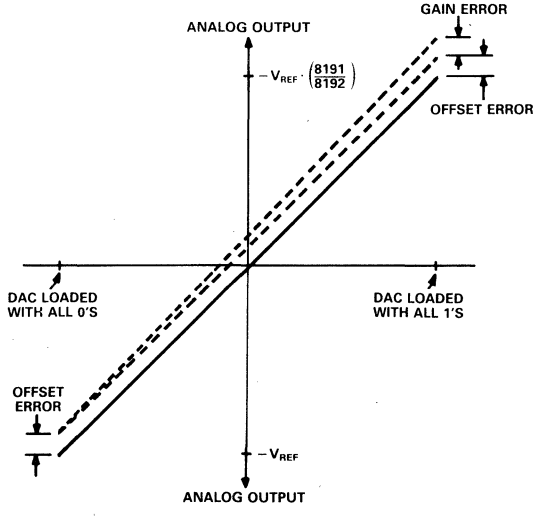
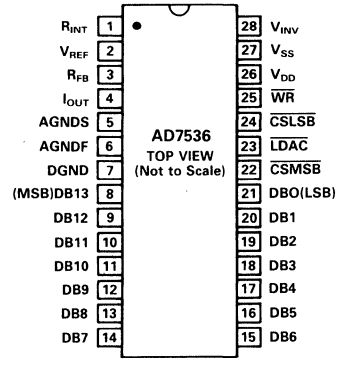


Figure 2. AD7536 Transfer Function

PIN CONFIGURATION



ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error T_{min} to T_{max}	Temperature Range and Package Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±2LSB	±16LSB	AD7536JN	AD7536AD	AD7536SD
±1LSB	±8LSB	AD7536KN	AD7536BD	AD7536TD

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise stated)

V_{DD} (pin 26) to DGND	−0.3V, +17V
V_{SS} (pin 27) to AGND	−15V, +0.3V
V_{REF} (pin 28) to AGND	±25V
V_{INV} (pin 2) to AGND	±25V
R_{INT} (pin 1) to AGND	±25V
V_{FB} (pin 3) to AGND	±25V
Digital Input Voltage (pins 8–25) to DGND	−0.3V, V_{DD}
V_{PIN4} to DGND	−0.3V, V_{DD}
AGND to DGND	−0.3V, V_{DD}
Power Dissipation (Any package)	
To +75°C	1000mW
Derates above +75°C	10mW/°C
Operating Temperature Range	
Commercial Plastic (JN, KNversions)	0 to +70°C
Industrial Ceramic (AD, BD versions)	−25°C to +85°C
Extended Ceramic (SD, TD versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

This is the analog weighting of 1 bit of the digital word in a DAC. For the AD7536 1LSB = $\frac{2V_{REF}}{2^{14}}$

RELATIVE ACCURACY

Relative accuracy or end point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for both endpoints (i.e., Offset and Gain Error are adjusted out) and is normally expressed in Least Significant Bits or as a percentage of full scale range.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of +1LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output with all one's loaded after offset error has been adjusted out. Gain error is adjustable to zero with an external potentiometer.

OFFSET ERROR

Offset error is a measure of the mismatch between R_{FB} and the internal offset resistor, R_{OFS}. It also includes the leakage component from the DAC (see Figure 8). It is present for all codes and is expressed in Least Significant Bits.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected from the digital inputs to the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage. It is measured with V_{REF} = AGND.

OUTPUT CAPACITANCE

This is the capacitance from I_{OUT} to AGND.

LEAKAGE CURRENT

Leakage current flows into I_{OUT} from the 14-bit DAC when all the DAC switches are off. It contributes to the Linearity, Gain and Offset error (see Figure 8).

MULTIPLYING FEEDTHROUGH ERROR

This is the ac error due to capacitive feedthrough from V_{REF} terminal to I_{OUT} with DAC register loaded with 10 0000 0000 0000.

Pin	Function	Description
1	R_{INT}	Contact point for internal resistors R1 and R2 which perform the inverting function on V_{REF} with external op-amp. See Figure 3.
2	V_{REF}	Reference input to the DAC. It is internally connected to R_{OFS} and R1. See Figure 3.
3	R_{FB}	Feedback resistor. Used to close the loop around an external op-amp.
4	I_{OUT}	Current Output Terminal.
5	A_{GNDS}	Analog ground sense line. Reference point for external circuitry. This pin should carry minimal current.
6	A_{GNDF}	Analog ground force line; carries current from internal analog ground connections. A_{GNDF} and A_{GNDS} are tied together internally.
7	DGND	Digital Ground
8	DB13	Data Bit 13. DAC MSB
9	DB12	Data Bit 12
10	DB11	Data Bit 11
11	DB10	Data Bit 10
12	DB9	Data Bit 9
13	DB8	Data Bit 8
14	DB7	Data Bit 7
15	DB6	Data Bit 6
16	DB5	Data Bit 5
17	DB4	Data Bit 4
18	DB3	Data Bit 3
19	DB2	Data Bit 2
20	DB1	Data Bit 1
21	DB0	Data Bit 0. DAC LSB
22	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active LOW input.
23	$\overline{LDAC}$	Asynchronous Load DAC input. Active LOW.
24	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input.
25	$\overline{WR}$	Write input. Active LOW.

$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{WR}$	Operation
0	1	1	0	Load MS Input Register
1	0	1	0	Load LS Input Register
0	0	1	0	Load MS and LS Input Registers
1	1	0	X	Load DAC Register from Input Registers
0	0	0	0	All Registers are transparent
1	1	1	X	No operation
X	X	1	1	No operation

NOTE X = Don't Care

26	V_{DD}	Power supply input. Specifications apply for V_{DD} = +12V ±5% to +15V ±5%.
27	V_{SS}	Bias pin for High Temperature Low Leakage configuration. To implement low leakage system, the pin should be at a negative voltage. See Figure 5 or 6 for recommended circuitry.
28	V_{INV}	This pin must be connected to the output of the external inverting op-amp. See Figure 3.

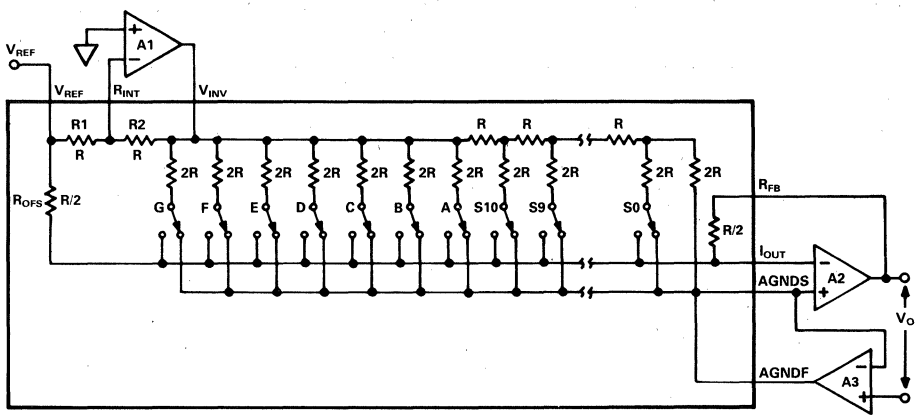


Figure 3. Simplified Circuit Diagram of the AD7536 D/A Section Showing Connection of External Op-Amps

CIRCUIT INFORMATION – D/A SECTION

Figure 3 is a simplified circuit diagram of the AD7536 D/A section and it also shows the external op-amp connection. The device is a 14-bit DAC with three extra resistors on chip for bipolar operation. It is configured so that the coding is Offset Binary. The 14-bit DAC consists of an R-2R ladder for the lower eleven bits (switches S0–S10). The three MSB's are decoded to drive switches A–G sequentially. Each of these carries an equally weighted current which is also equal to the current in the R-2R ladder. R_{OFS} has the same magnitude as R_{FB} so that the output is offset by a constant $-V_{REF}$. R1 and R2 (together with external op-amp A1) invert V_{REF} and apply it to the 14-bit DAC (V_{INV}). See Table I for complete Offset Binary Code Table.

To eliminate any slight variations in analog ground potential with changing code, there are two analog ground pins. AGNDF sinks all the current flowing through the switches to ground while AGNDS is used as a reference point with minimal current flowing in it. Figure 3 shows A3 maintaining AGNDS at Signal Ground. The connection of AGNDS and AGNDF may be changed depending on required system accuracy and output drive requirements (see Figures 5 and 6).

EQUIVALENT CIRCUIT ANALYSIS

Figure 4 shows an equivalent output circuit for the analog section of the AD7536 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R0 denotes the equivalent output resistance of the DAC and associated resistors. This varies with input code. C_{OUT} is the capacitance due to the current steering switches and varies from about 90pF to 180pF (typical values) depending on the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the circuit transfer function, N.

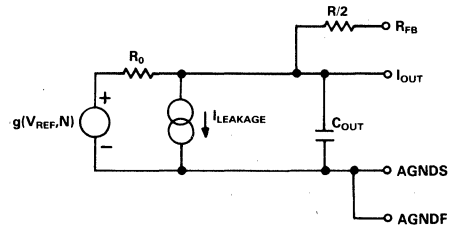


Figure 4. AD7536 Equivalent Analog Output Circuit

CIRCUIT INFORMATION – DIGITAL SECTION

The digital inputs are designed to be both TTL and 5V CMOS compatible. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close as possible to 0 and 5V logic levels.

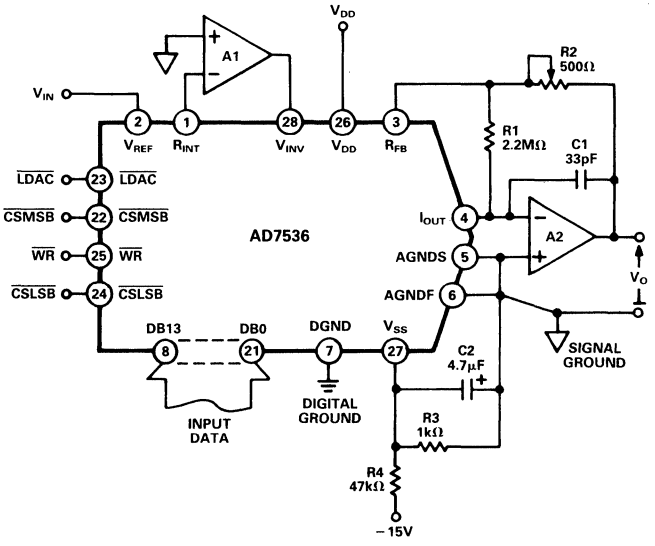


Figure 5. AD7536 Operation

BIPOLAR OPERATION
(4-Quadrant Multiplication)

Figure 5 shows the AD7536 connected for bipolar operation. Specified accuracy is attained without the need for expensive closely matched external resistors. R1 and R2 provide an optional gain adjustment and capacitor C1 helps prevent overshoot and ringing when high-speed op-amps are used. The −300mV bias voltage for V_{SS} is derived from R3, R4 and C2. Op-amp A3 (Figure 3 and Figure 6) is omitted from Figure 5. AGNDS and AGNDF are externally shorted to Signal Ground.

Table I shows the Offset Binary Code Table obtained with the circuit of Figure 5. It should be noted that the user can get a 2's Complement transfer function by inverting the MSB of the DAC word.

Binary Number in DAC Register MSB LSB	Analog Output V_{OUT}
11 1111 1111 1111	$+V_{IN}\left(\frac{8191}{8192}\right)$
10 0000 0000 0001	$+V_{IN}\left(\frac{1}{8192}\right)$
10 0000 0000 0000	0V
00 0000 0000 0001	$-V_{IN}\left(\frac{8191}{8192}\right)$
00 0000 0000 0000	$-V_{IN}\left(\frac{8192}{8192}\right) = -V_{IN}$

Table I. Offset Binary Code Table for AD7536

OFFSET AND GAIN ADJUSTMENT FOR FIGURE 5.

Offset Adjustment

1. Adjust offset of amplifier A1 so that potential at R_{INT} is $<10\mu V$ with respect to Signal Ground.
2. Load DAC register with all 0's.
3. Adjust offset of amplifier A2 until $V_0 = -V_{IN} \pm 10\mu V$.

Gain Adjustment

1. Load DAC register with all 1's.
2. Trim potentiometer R2 so that $V_O = +V_{IN}\frac{(8191)}{(8192)}$

For high-temperature applications, resistors and potentiometers should have a low Temperature Coefficient. In many applications, because of the excellent Offset Error, Full Scale Error and Gain T.C. specifications of the AD7536, trimming of the Offset and Gain is not necessary.

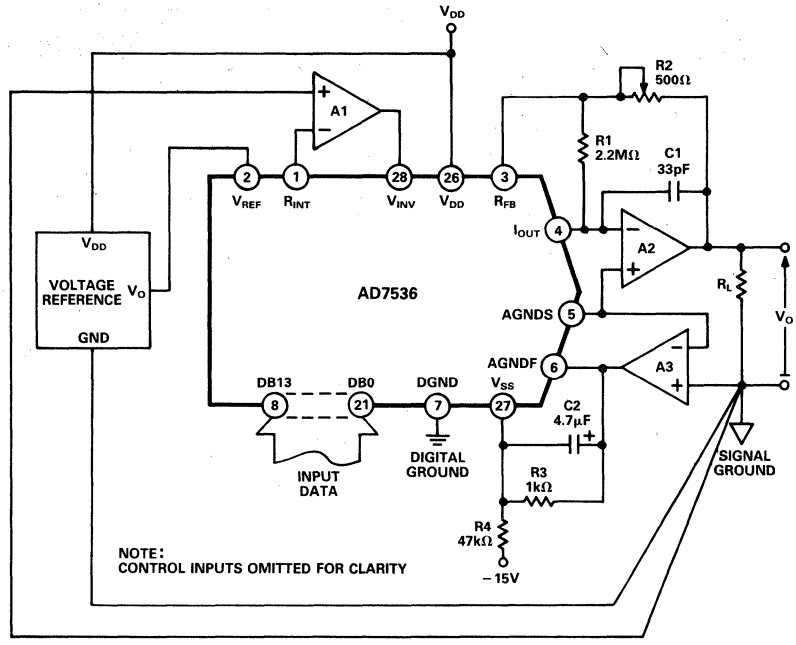


Figure 6. AD7536 Operation with Forced Ground

GROUNDING CONSIDERATIONS

In the circuits of Figures 5 and 6, with $V_{REF} = +10V$, 1LSB has a value of 1.2mV. So, factors which are not important in less accurate systems must, in this case, be given careful consideration. Among these, the whole question of grounding is crucial. Voltage reference ground, the I_{OUT} pin on the DAC, the noninverting pin of A1 and SIGNAL GROUND must all be at the same potential. Note that in Figure 5, AGNDS and AGNDF are externally shorted and A3 is not used. Voltage drops due to bond wire resistance are not compensated for in this circuit. This means that an extra linearity error of less than 0.1LSB is added to the DAC linearity error. If the user wishes to eliminate this extra error, then the circuit of Figure 6 should be used. Here, A3 is used to maintain AGNDS at Signal Ground potential. I_{OUT} is also at Signal Ground potential. By using the Force, Sense technique all switch contacts on the DAC are at exactly the same potential and any error due to bond wire resistance is eliminated. If A3 is not a low offset voltage (<100μV) op-amp, it should be trimmed with a potentiometer until the voltage at AGNDS is <10μV with respect to SIGNAL GROUND. Figure 7 shows how the circuit of Figure 5 might be be laid out. Gain trim components R1 and R2 have been omitted for clarity. Note how the input to V_{REF} (pin 2) is shielded to reduce ac feedthrough while the digital inputs are shielded to minimize digital feedthrough.

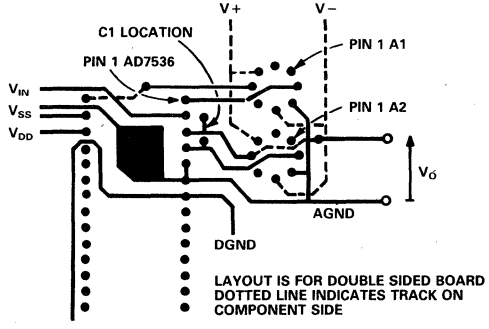


Figure 7. Suggested Layout for AD7536 Circuit of Figure 5

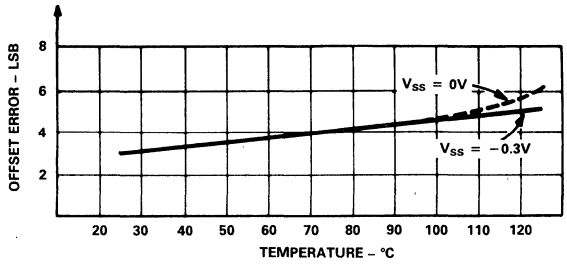


Figure 8. Typical Graph of Offset Error vs. Temperature With and Without Low Leakage Configuration

LOW LEAKAGE CONFIGURATION

Leakage current in CMOS D/A converters has two components. Current leaks from V_{DD} into the I_{OUT} line and is present at all DAC codes. There is also leakage across the off switches in the DAC. The polarity of this current depends on V_{INV} and its magnitude is related to the code in the DAC register. At high temperatures (above 90°C) it is normal for the leakage current to increase dramatically. By its nature it will affect all critical dc parameters (Linearity Error, Gain Error and Offset Error). The AD7536 features a leakage reduction configuration (patent pending) to keep the leakage current low (typically <10nA) over an extended temperature range. This ensures that the DAC maintains its 25°C performance very well at temperatures up to 125°C.

The AD7536 can be operated with or without the leakage reduction configuration. If V_{SS} (pin 27) is tied to AGND, then the DAC will exhibit normal output leakage current at high temperatures. To use the low leakage facility, V_{SS} should be tied to −0.3V as in Figures 5 and 6. The current taken by V_{SS} is very low (<10μA) allowing a simple resistor divider (R3, R4) to produce the required −300mV from −15V. The capacitor C2 in parallel with R3 is an integral part of the low leakage configuration and must be 4.7μF or greater. Figure 8 is a plot of Offset Error versus temperature for both conditions. It clearly shows the improvement when the low leakage configuration is used.

OP-AMP SELECTION

In choosing an amplifier to be used with the AD7536, three parameters are of prime importance. These are:

1. Input Offset Voltage (V_{OS})
2. Input Bias Current (I_B)
3. Offset Voltage Drift (TC V_{OS}).

To maintain specified accuracy with V_{REF} at 10V, A1 and A2 of Figures 5 and 6 must have V_{OS} <100μV and I_B <2nA. It is important that the amplifier Open Loop Gain, A_{VOL}, be sufficiently large to keep V_{OS} <100μV for the full output voltage range. For a maximum output of 10V, A_{VOL} must be greater than 100,000.

In the Forced Ground configuration of Figure 6, one can use an AD OP-07 for amplifier A3, without any external adjustment for V_{OS}. In low frequency or fixed reference applications where fast output settling time is not required, the AD OP-07 is also recommended for A1 and A2. Because of its low V_{OS} no external potentiometers are needed. For faster settling time, one can use the AD544 series of op-amps.

Offset Voltage Drift and Bias Current drift are critical parameters for operation over a wide temperature range. The AD OP-07, AD OP-27 and AD OP-37 all exhibit very low offset drift while the AD544 has very low bias current drift. Table II summarizes the important specifications of the op-amps mentioned above.

Op-Amp	Input Offset Voltage (V_{OS})	Input Bias Current (I_B)	Offset Voltage Drift (TC V_{OS})	Settling Time to 0.003% FS
AD544L	500μV	25pA	5μV/°C	5μs
AD OP-07H	75μV	3nA	0.6μV/°C	50μs typ
AD OP-27CH	100μV	80nA	0.6μV/°C	6μs typ
AD OP-37CH	100μV	80nA	0.6μV/°C	1μs typ
HA-2620	4mV	35nA	20μV/°C	0.8μs typ

Table II. Guide to Op-Amp Selection

MICROPROCESSOR INTERFACING

AD7536 – 8086A INTERFACE

The versatility of the AD7536 loading sturcture allows interfacing to both 8- and 16-bit microprocessor systems. Figure 9 shows the 8086 16-bit processor interfacing to a single device. In this circuit the double buffering feature of the DAC is not used. AD0-AD13 of the 16-bit data bus are connected to the DAC data bus (DB0-DB13). The 14-bit word is written to the DAC in one MOV instruction and the analog output responds immediately. In this example the DAC address is D000. A software routine for Figure 9 is given in Table III. In a multiple DAC system the double buffering of the AD7536 allows the user to simultaneously update all DAC's. In Figure 10, a 14-bit word is loaded to the Input Registers of each of the DACs in sequence. Then, with one instruction to the appropriate address, CS4 (i.e., $\overline{LDAC}$) is brought low, updating all the DACs simultaneously.

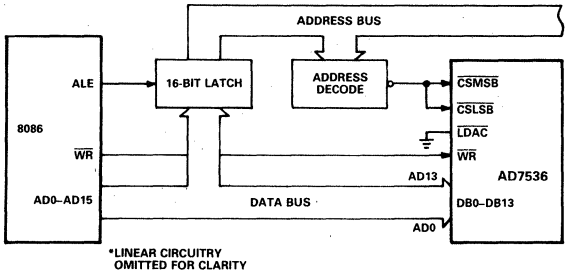


Figure 9. AD7536 – 8086 Interface Circuit

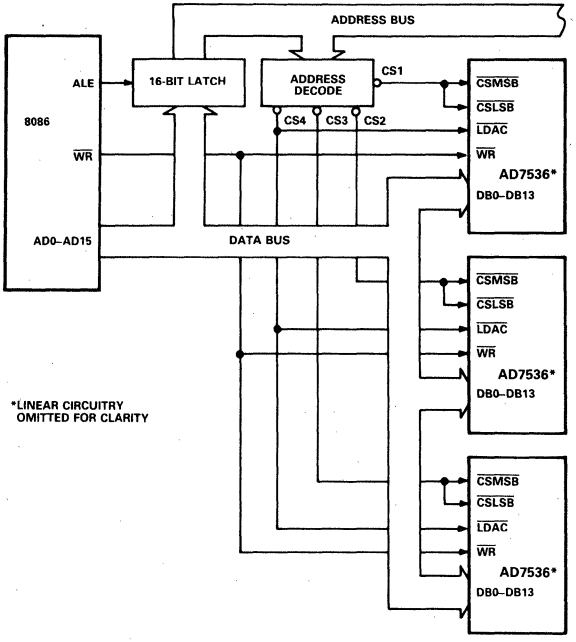


Figure 10. AD7536 – 8086 Interface: Multiple DAC System

ASSUME DS: DACLOAD, CS : DACLOAD
DACLOAD SEGMENT AT 000

00	8CC9	MOV CX, CS	:	DEFINE DATA SEGMENT REGISTER EQUAL
02	8ED9	MOV DS, CX	:	TO CODE SEGMENT REGISTER
04	BF00D0	MOV DI, # D000	:	LOAD DI WITH D000
07	C705"YZWX"	MOV MEM,# YZWX"	:	DAC LOADED WITH WXYZ
0B	EA0000		:	CONTROL IS RETURNED TO THE
0E	00FF			MONITOR PROGRAM

Table III. Sample Program for Loading AD7536 from 8086

AD7536 – MC68000 INTERFACE

Interfacing between the MC68000 and the AD7536 is accomplished using the circuit of Figure 11. The following routine writes data to the DAC input registers and then outputs the data via the DAC register.

01000	MOVE.W	#W, D0	The desired DAC data, W, is loaded into Data Register 0. W may be any value between 0 and 16383 (decimal) or 0 and 3FFF (hexademical).
	MOVE.W	D0,$E000	The data W is transferred between D0 and the DAC Register.
	MOVE.B	#228,D7	Control is returned to the System Monitor Program using these tow instructions.
	TRAP	#14	

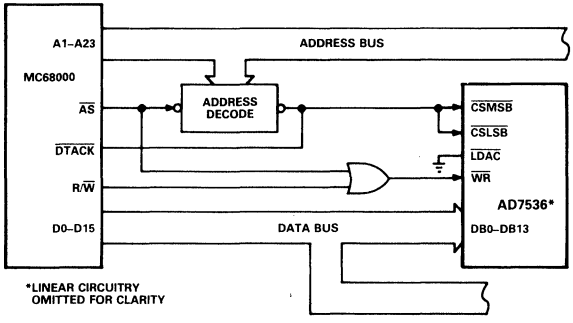


Figure 11. AD7536 – MC68000 Interface

AD7536 – Z80 INTERFACE

Though the AD7536 is ideally suited for use either with 16-bit microprocessors or in stand-alone applications, it can also be interfaced to 8-bit processor systems. Figure 12 is an interface circuit for the popular Z80 microprocessor.

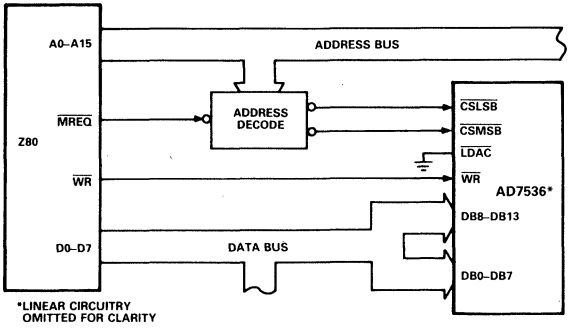


Figure 12. AD7536 – Z80 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7536 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this Digital Feedthrough isolate the DAC from the noise source. Figure 13 shows an interface circuit which physically isolates the DAC from the bus. One may also use other means, such as peripheral interface devices, to reduce the Digital Feedthrough.

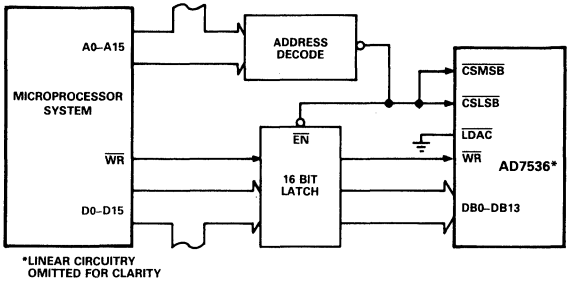
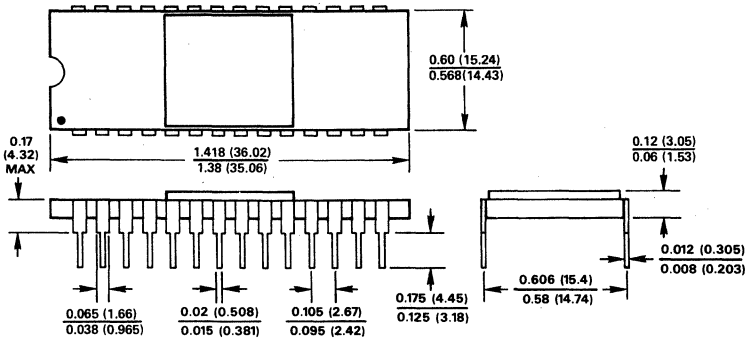


Figure 13. AD7536 Interface Circuit Using Latches to Minimize Digital Feedthrough

MECHANICAL INFORMATION
OUTLINE DIMENSIONS

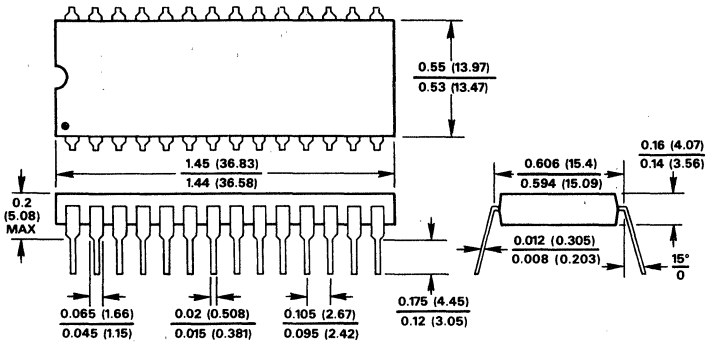
Dimensions shown in inches and (mm).

28-PIN CERAMIC DIP (SUFFIX D)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

28-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

ANALOG DEVICES

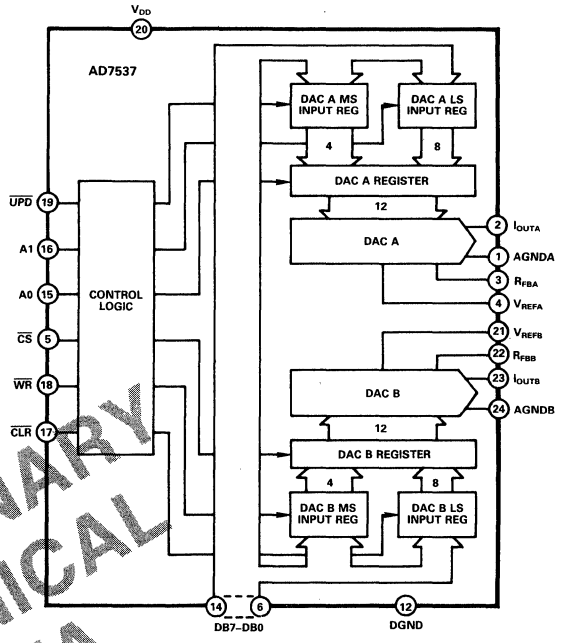
Dual 12-Bit DACs

AD7537/47

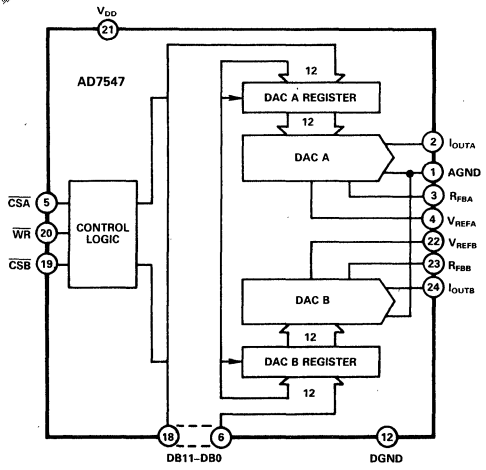
FEATURES
- Two 12-Bit DACs in One Package
- 4-Quadrant Multiplication
- Low Gain Error (3LSBs max)
- Versatile Interface Logic
- DAC Ladder Resistance Matching: 1%
- Space-Saving 0.3", 24-Pin Package

APPLICATIONS
- Programmable Filters
- Audio Applications
- Synchro Applications
- Automatic Test Equipment
- Microcomputer-Based Process Control
- Programmable Power Supplies

AD7537 FUNCTIONAL BLOCK DIAGRAM



AD7547 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7537 and AD7547 are monolithic, dual, 12-bit, current output D/A converters. The AD7537 has eight data inputs with a two-byte (8+4) loading structure suitable for interfacing with 8-bit microprocessors. The AD7547 has twelve data inputs and a single-word loading structure. This is ideal when using the DACs with 16-bit microprocessors or in a stand-alone configuration.

The devices are packaged in a 0.3", 24-pin package. Both DACs provide 4-quadrant multiplication capabilities with a separate reference input and feedback resistor for each DAC. The monolithic construction ensures excellent thermal tracking and gain error tracking between the two DACs. Because of its 8+4 loading structure, the AD7537 also offers: 1) A separate AGND line for each DAC; 2) a $\overline{CLR}$ pin to asynchronously clear both DACs; 3) a $\overline{UPD}$ pin which provides a double-buffering facility.

The AD7537 and AD7547 are manufactured using the Linear Compatible CMOS (LC^2MOS) process. They are speed compatible with most microprocessors and accept TTL, 74HC and 5V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. DAC to DAC Matching:
   Since both DACs are fabricated on the same chip, precise matching and tracking is inherent. This allows applications which would not be practical using two dicrete DACs.
2. Small Package Size:
   The AD7537 and AD7547 are packaged in a small 24-pin, 0.3" DIP.

PRELIMINARY TECHNICAL DATA

SPECIFICATIONS (V_{DD} = +12V to +15V, ±10%, $V_{REFA} = V_{REFB}$ = 10V; $V_{IOUTA} = V_{IOUTB} = V_{AGND}$ = 0V. All specifications T_{min} to T_{max} unless otherwise stated).

Parameter	AD7537/47JN[1] AD7537/47AQ	AD7537/47KN AD7537/47BQ	AD7537/47SQ	AD7537/47TQ	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Full-Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[2];						
ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current						
I_{OUTA}						
+25°C	20	20	20	20	nA max	DAC A Register loaded
T_{min} to T_{max}	150	150	250	250	nA max	with all 0's.
I_{OUTB}						
+25°C	20	20	20	20	nA max	DAC B Register loaded
T_{min} to T_{max}	150	150	250	250	nA max	with all 0's.
REFERENCE INPUT						
Input Resistance						
(V_{REFA}, V_{REFB})	7	7	7	7	kΩ min	Typical Input Resistance =
	18	18	18	18	kΩ max	11kΩ
V_{REFA}/V_{REFB}						
Input Resistance Match	±3	±2	±3	±2	% max	Typically ±1%
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	$V_{IN} = V_{DD}$
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V min/V max	
I_{DD}	5	5	5	5	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +12V to +15V; $V_{REFA} = V_{REFB}$ = +10V, $V_{IOUTA} = V_{IOUTB} = V_{AGND}$ = 0V. Output Amplifiers are AD644 except where stated.)

Parameter	T_A = +25°C	$T_A = T_{min}, T_{max}$	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full-scale range. I_{OUT} load = 100Ω. C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical Value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	10	–	nV-s typ	Measured with $V_{REFA} = V_{RFB}$ = 0V. I_{OUTA}, I_{OUTB}, load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[3]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{REFA}, V_{REFB} = 20Vp-p 10kHz sinewave
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0's.
Power Supply Rejection				
ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	$\Delta V_{DD} = V_{DD}$ max − V_{DD} min
Output Capacitance				
C_{OUTA}	80	80	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	80	80	pF max	
C_{OUTA}	160	160	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	160	160	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−62	–	dB typ	V_{REFA} = 20V p-p 100kHz sinewave, V_{REFB} = 0V
V_{REFB} to I_{OUTA}	−62	–	dB typ	V_{REFB} = 20V p-p 100kHz sinewave, V_{REFA} = 0V
Digital Crosstalk	10	–	nV-s typ	Measured for a Code Transition of all 0's to all 1's
Output Noise Voltage Density (10Hz-100kHz)	15	–	nV/√Hz typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}
Harmonic Distortion	−90	–	dB typ	V_{IN} = 6V rms, 1kHz

NOTES

[1]Temperature range as follows: JN, KN Versions: 0 to +70°C.
AQ, BQ Versions: −25°C to +85°C.
SQ, TQ Versions: −55°C to +125°C.

[2]Guaranteed by Product Assurance testing.

[3]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

ANALOG DEVICES

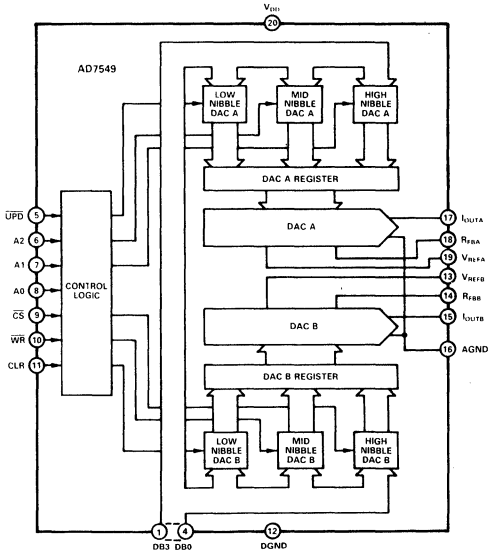
LC² MOS
Dual 12-Bit µP Compatible DAC

AD7549

FEATURES
Two Doubled Buffered 12-Bit DACs
4-Quadrant Multiplication
Low Gain Error (3LSBs max)
DAC Ladder Resistance Matching: 1%
Space Saving 0.3" 20-Pin Package
Latch-up Proof

APPLICATIONS
Programmable Filters
Automatic Test Equipment
Microcomputer Based Process Control
Audio Systems
Programmable Power Supplies
Synchro Applications

AD7549 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7549 is a monolithic dual, 12-bit, current output D/A converter. It is packaged in a 0.3" wide 20-pin package. Both DACs provide four quadrant multiplication capabilities with a separate reference input and feedback resistor for each DAC. The monolithic construction ensures excellent thermal tracking and gain error tracking between the two DACs.

The DACs in the AD7549 are each loaded in three 4-bit nibbles. The control logic is designed for easy processor interfacing. Input and DAC register loading is accomplished using address lines A0, A1, A2 and $\overline{CS}$, $\overline{WR}$ lines. A logic high level on the CLR input clears all registers. Both DACs may be simultaneously updated using the $\overline{UPD}$ input.

The AD7549 is manufactured using the Linear Compatible CMOS(LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL, 74HC or 5V CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Small package size: the loading structure adopted for the AD7549 enables two 12-Bit DACs to be packaged in a small 20-pin 0.3" DIP.
2. DAC to DAC matching: since both DACs are fabricated on the same chip, precise matching and tracking is inherent. This opens up applications which otherwise would not be considered, i.e., Programmable Filters, Audio Systems, etc.

SPECIFICATIONS[1] (V_{DD} = +15V ± 5%[2], V_{REFA} = V_{REFB} = 10V; V_{PIN15} = V_{PIN17} = V_{PIN16} = 0. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	AD7549JN AD7549AD	AD7549KN AD7549BD	AD7549SD	AD7549TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	All grades guaranteed monotonic over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC.
Gain Temperature Coefficient[3]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 1ppm/°C
Output Leakage Current						
I_{OUTA} (Pin 17)						
+25°C	20	20	20	20	nA max	DAC A Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
I_{OUTB} (Pin 15)						
+25°C	20	20	20	20	nA max	DAC B Register loaded with all 0's
T_{min} to T_{max}	150	150	250	250	nA max	
REFERENCE INPUT						
Input Resistance (Pin 19, Pin 13)	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	18	18	18	18	kΩ max	
V_{REFA}/V_{REFB} Input Resistance Match	±3	±2	±3	±2	% max	Typically ±1%
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
I_{DD}	5	5	5	5	mA max	

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.

(V_{DD} = +15V; V_{REFA} = V_{REFB} = +10V, V_{PIN15} = V_{PIN17} = V_{PIN16} = 0V, Output Amplifiers are AD644 except where stated)

Parameter	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.01% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC output measured from falling edge of $\overline{WR}$. Typical value of Settling Time is 0.8μs.
Digital-to-Analog Glitch Impulse	10	–	nV-sec typ	Measured with V_{REFA} = V_{RFB} = 0V. I_{OUTA}, I_{OUTB} load = 100Ω, C_{EXT} = 13pF. DAC registers alternately loaded with all 0's and all 1's.
AC Feedthrough[4]				
V_{REFA} to I_{OUTA}	−70	−65	dB max	V_{RFFA}, V_{REFB} = 20V p-p 10kHz sine wave.
V_{REFB} to I_{OUTB}	−70	−65	dB max	DAC registers loaded with all 0s.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance				
C_{OUTA}	80	80	pF max	DAC A, DAC B loaded with all 0's.
C_{OUTB}	80	80	pF max	
C_{OUTA}	160	160	pF max	DAC A, DAC B loaded with all 1's.
C_{OUTB}	160	160	pF max	
Channel-to-Channel Isolation				
V_{REFA} to I_{OUTB}	−62	–	dB typ	V_{REFA} = 20V p-p 100kHz sine wave, V_{REFB} = 0V
V_{REFB} to I_{OUTA}	−62	–	dB typ	V_{REFB} = 20V p-p 100kHz sine wave, V_{REFA} = 0V
Digital Crosstalk	10	–	nV-sec typ	Measured for a Code Transition of all 0's to all 1's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV/$\sqrt{Hz}$ typ	Measured between R_{FBA} and I_{OUTA} or R_{FBB} and I_{OUTB}
Harmonic Distortion	−90	–	dB typ	V_{IN} = 6V rms 1kHz

NOTES

[1]Temperature range as follows: JN, KN, Versions: 0 to +70°C
AD, BD, Versions: −25°C to +85°C
SD, TD, Versions: −55°C to +125°C

[2]At V_{DD} = 5V, the device is fully functional with degraded performance.

[3]Guaranteed by Product Assurance testing.

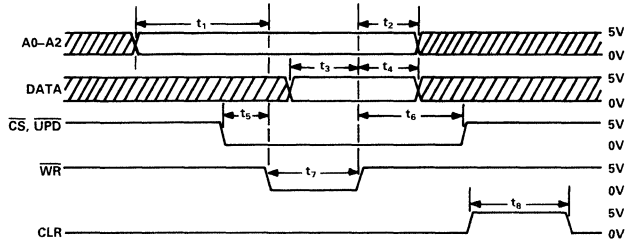
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +15V, V_{REFA} = V_{RFB} = +10V, V_{PIN15} = V_{PIN17} = V_{PIN16} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit at T_A = 0 to +70°C T_A = −25°C to +85°C	Limit at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_1	50	80	110	ns min	Address Valid to Write Setup Time
t_2	0	0	0	ns min	Address Valid to Write Hold Time
t_3	150	190	240	ns min	Data Setup Time
t_4	0	0	0	ns min	Data Hold Time
t_5	20	20	20	ns min	Chip Select or Update to Write Setup Time
t_6	0	0	0	ns min	Chip Select or Update to Write Hold Time
t_7	170	200	250	ns min	Write Pulse Width
t_8	170	200	250	ns min	Clear Pulse Width

Specifications subject to change without notice.



NOTES
1. All INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20$ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. Timing Diagram for AD7549

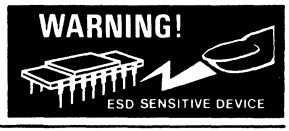
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (pin 20) to DGND . . . . . −0.3V, +17V
V_{REFA}, V_{REFB} (pins 19, 13) to AGND . . . . . ±25V
V_{RFBA}, V_{RFBB} (pins 18, 14) to AGND . . . . . ±25V
Digital Input Voltage (pins 1–11) to DGND . . −0.3V, V_{DD}
V_{PIN15}, V_{PIN17}, to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (JN, KN versions) . . . . . 0 to +70°C
Industrial Ceramic (AD, BD versions) . . −25°C to +85°C
Extended Ceramic (SD, TD versions) . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ORDERING INFORMATION

Relative Accuracy T_{MIN} to T_{MAX}	Full Scale Error T_{MIN} to T_{MAX}	Temperature Range and Package		
		Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±1LSB	±6LSB	AD7549JN	AD7549AD	AD7549SD
±1/2LSB	±3LSB	AD7549KN	AD7549BD	AD7549TD

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero error and full scale error and is normally expressed in Least Significant Bits or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of 1LSB max over the operating temperature range ensures montonicity.

FULL-SCALE ERROR
Full scale error or gain error is a measure of the output error between an ideal DAC and the actual device output. Full scale error is adjustable to zero.

OUTPUT CAPACITANCE
This is the capacitance from I_{OUTA} or I_{OUTB} to AGND.

DIGITAL-TO-ANALOG GLITCH IMPULSE:
The amount of charge injected into the analog output when the inputs change state is called Digital-to-Analog Glitch Impulse. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Digital charge injection is measured with V_{REFA} and V_{REFB} equal to AGND.

OUTPUT LEAKAGE CURRENT
Output Leakage Current is current which appears at I_{OUTA} or I_{OUTB} with the DAC registers loaded to all zeros.

MULTIPLYING FEEDTHROUGH ERROR
This is the error due to capacitive feedthrough from V_{REFA} to I_{OUTA} or V_{REFB} to I_{OUTB} with the DAC registers loaded to all zeros.

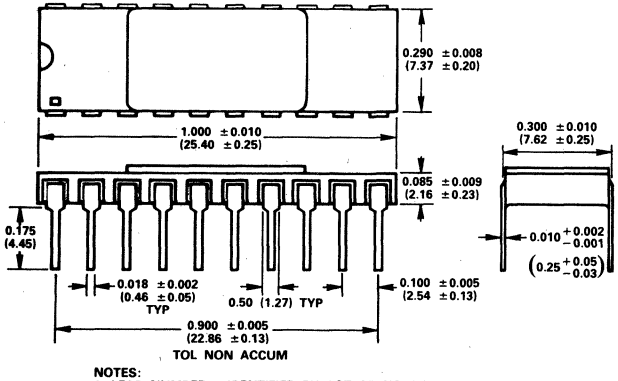
CHANNEL-TO-CHANNEL ISOLATION
Channel-to-Channel Isolation refers to the proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

DIGITAL CROSSTALK
The glitch impulse transferred to the output of one converter due to a change in digital input code to the other converter is defined as Digital Crosstalk and is specified in nV-secs.

MECHANICAL INFORMATION

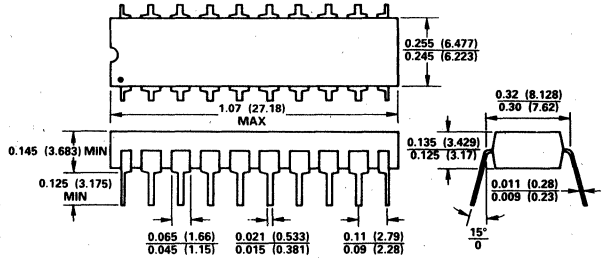
OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

20-PIN CERAMIC DIP (SUFFIX D)



NOTES:
1. LEAD NUMBER 1 IDENTIFIED BY DOT OR NOTCH.
2. LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

20-PIN PLASTIC DIP (SUFFIX N)



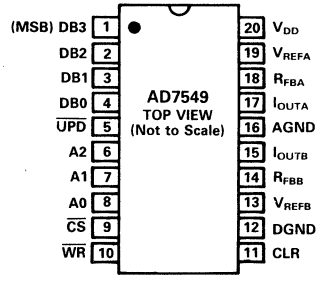
PIN	FUNCTION	DESCRIPTION
1	DB3	Data Bit 3, Data Bit 7 or Data Bit 11 (MSB)
2	DB2	Data Bit 2, Data Bit 6 or Data Bit 10.
3	DB1	Data Bit 1, Data Bit 5 or Data Bit 9.
4	DB0	Data Bit 0, Data Bit 4 or Data Bit 8.
5	$\overline{UPD}$	Updates DAC Registers from 4-bit input registers. DAC A and DAC B both updated simultaneously.
6	A2	Address line 2.
7	A1	Address line 1.
8	A0	Address line 0.
9	$\overline{CS}$	Chip Select Input. Active low.
10	$\overline{WR}$	Write Input. Active low.
11	CLR	Clear Input. Active High. Clears all registers.
12	DGND	Digital Ground.
13	V_{REFB}	Voltage reference input to DAC B.
14	R_{FBB}	Feedback resistor of DAC B.
15	I_{OUTB}	Current output terminal of DAC B.
16	AGND	Analog ground.
17	I_{OUTA}	Current output terminal of DAC A.
18	R_{FBA}	Feedback resistor of DAC A.
19	V_{REFA}	Voltage reference input to DAC A.
20	V_{DD}	+15V supply input.

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer.
0	1	1	X	X	X	X	No data transfer.
1	X	X	X	X	X	X	All registers cleared.
0	1	0	⊓	0	0	0	DAC A LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	0	1	DAC A MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	0	DAC A HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	0	1	1	DAC A Register loaded from Input Registers.
0	1	0	⊓	1	0	0	DAC B LOW NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	0	1	DAC B MID NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	0	DAC B HIGH NIBBLE REGISTER loaded from Data Bus.
0	1	0	⊓	1	1	1	DAC B Register loaded from Input Registers.
0	0	1	⊓	X	X	X	DAC A, DAC B Registers updated simultaneously from Input Registers.

NOTE: X = Don't Care

Table I. AD7549 Truth Table

PIN CONFIGURATION



UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 2 shows the circuit diagram for unipolar binary operation. With an ac input, the circuit performs 2-quadrant multiplication. The code table for Figure 2 is given in Table II.

Operational amplifiers A1 and A2 can be in a single package (i.e. AD644) or separate packages (AD544). Capacitors C1 and C2 provide phase compensation to help prevent overshoot and ringing when high speed op-amps are used.

For zero offset adjustment, the appropriate DAC register is loaded with all O's and amplifier offset adjusted so that V_{OUTA} or V_{OUTB} is at a minimum (i.e. $\leq 120\mu V$). Full scale trimming is accomplished by loading the DAC register with all 1's and adjusting R1 (R3) so that V_{OUTA} (V_{OUTB}) = $-V_{IN}$ (4095/4096). In fixed reference applications, full scale can also be adjusted by omitting R1, R2, R3, R4 and trimming the reference voltage magnitude.

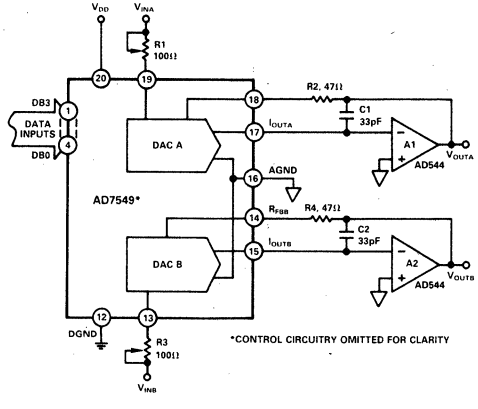


Figure 2. AD7549 Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit diagram for bipolar operation is shown in Figure 3. Offset binary coding is used.

With the appropriate DAC register loaded to 1000 0000 0000, adjust R1 (R3) so that V_{OUTA} (V_{OUTB}) = 0V. Alternatively, R1, R2 (R3, R4) may be omitted and the ratios of R6, R7 (R9, 10) varied for V_{OUTA} (V_{OUTB}) = 0V. Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5 (R8).

Resistors R5, R6, R7 (R8, R9, R10) must be ratio matched to 0.01%. When operating over a wide temperature range, it is important that the resistors be of the same type so that their temperature coefficients match.

The code table for Figure 3 is given in Table III.

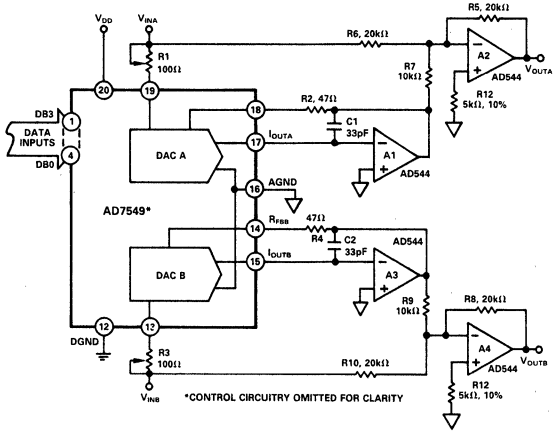


Figure 3. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 2

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUTA} or V_{OUTB}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 3

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 2 and 3 exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD644L, AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Temperature Coefficients: The gain temperature coefficient of the AD7549 has a maximum value of 5ppm/°C and typical value of 1ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.4LSBs respectively over a 100°C temperature range. When trim resistors R1(R3) and R2(R4) are used to adjust full scale range, the temperature coefficient of R1(R3) and R2(R4) should also be taken into account.

High Frequency Considerations: AD7549 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7549 depends upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 2 is shown in Figure 4 which minimizes feedthrough from V_{REFA}, V_{REFB} to the output in multiplying applications.

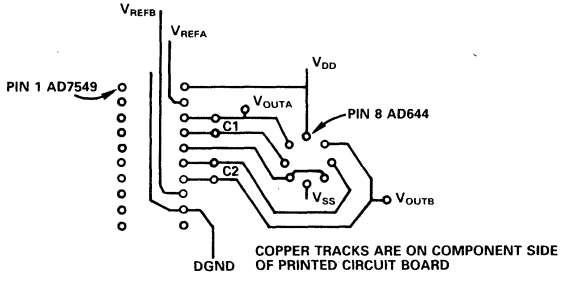


Figure 4. Suggested Layout for AD7549 with AD644 (Dual Op Amp)

AD7549 – 8085A INTERFACE

A typical interface circuit for the AD7549 and the 8085A microprocessor is given in Figure 5. Only the bottom 4 bits of the microprocessor data bus are used. The address decoder provides both the $\overline{CS}$ and $\overline{UPD}$ signals for the DAC. Address lines A0, A1, A2 select one of six DAC Input Registers for accepting data. In applications where simultaneous loading of the DACs is required then the $\overline{UPD}$ pin must be used to strobe both DAC registers. Otherwise, $\overline{UPD}$ may be tied high and address lines A0-A2, in conjunction with $\overline{CS}$ and $\overline{WR}$ signals, will select each DAC register separately (see Pin Function Description).

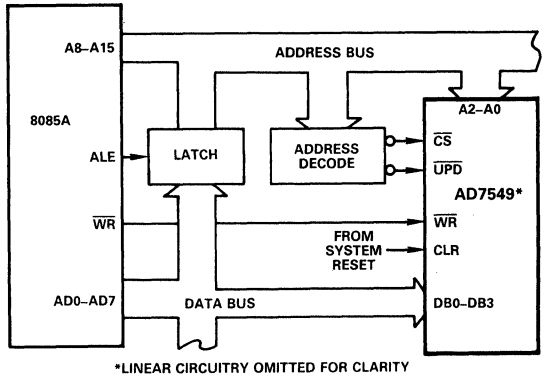


Figure 5. AD7549–8085A Interface

AD7549 – Z80 INTERFACE

Figure 6 shows the AD7549 connected to the Z80 microprocessor. The interface structure is similar to that for the 8085A.

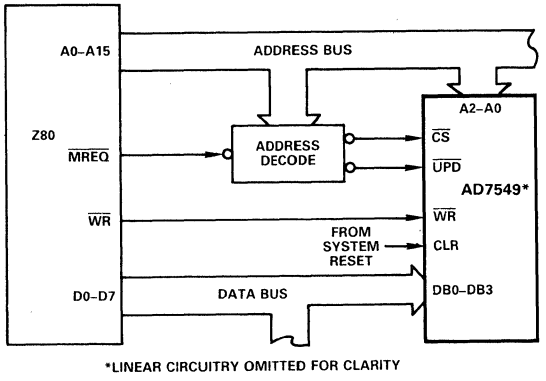


Figure 6. AD7549–Z80 Interface

AD7549 – 8048 INTERFACE

The AD7549 can be interfaced to the 8048 single component microcomputer using the circuit of Figure 7. A minimum number of I/O lines are needed. The system is easily expanded by using extra port lines to provide Chip Selects for more AD7549's. The advantage of this interface lies in its simplicity. In either single or multiple DAC applications both the software and chip select decoding are simplified over what would be required if the devices were memory mapped in a conventional manner.

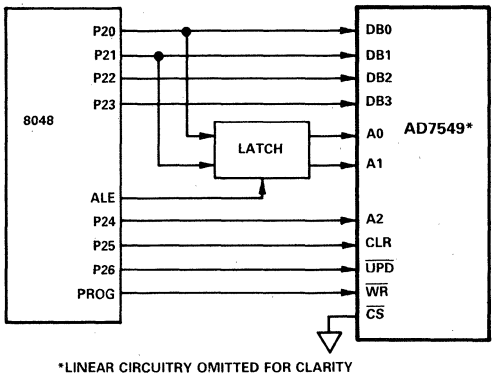


Figure 7. AD7549–8048 Interface

The combination of 8048 system and AD7549 is particularly suitable for dedicated control applications. By adding reference and output circuitry a complete control system can be configured with a minimum number of components.

AD7549 – MC6809 INTERFACE

Figure 8 is the interface circuit for the popular MC6809 8-bit microprocessor. $\overline{CS}$ and $\overline{UPD}$ signals are decoded from the address for the simultaneous update facility while the $\overline{WR}$ pulse is provided by inverting the microprocessor clock, E.

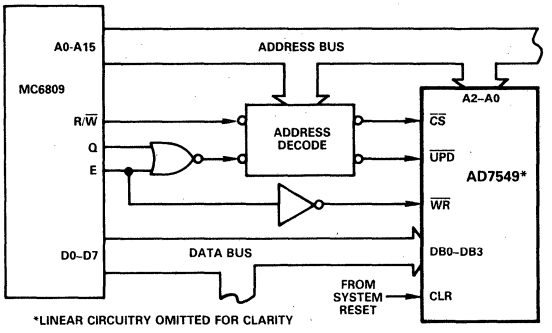


Figure 8. AD7549–MC6809 Interface

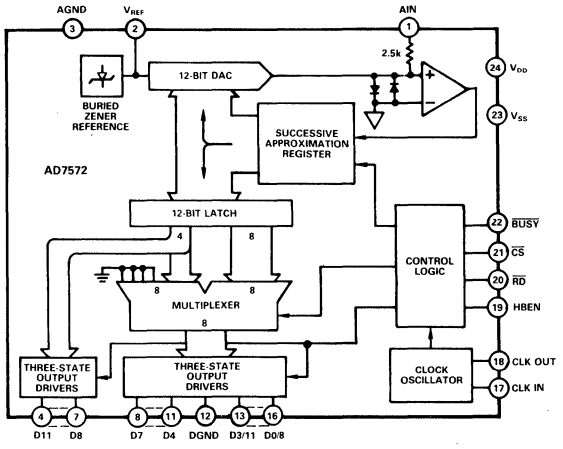
ANALOG DEVICES

LC²MOS Complete, High-Speed 12-Bit ADC

AD7572

FEATURES
12-Bit Resolution and Accuracy
Fast Conversion Time
AD7572XX05: 5μs
AD7572XX12: 12.5μs
Complete with On-Chip Reference
Fast Bus Access Time: 90ns
Low Power: 135mW
Small, 0.3", 24-pin Package

AD7572 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7572 is a complete, 12-bit ADC that offers high-speed performance combined with low, CMOS power levels. The AD7572 uses an accurate, high-speed DAC and comparator in a successive-approximation loop to achieve a fast conversion time. An on-chip, buried zener diode provides a stable reference voltage to give low drift performance over the full temperature range and the specified accuracy is achieved without any user trims. An on-chip clock circuit is provided, which may be used with a crystal for stand-alone operation, or the clock input may be driven from an external clock source such as a divided-down microprocessor clock. The only other external components required for basic operation of the AD7572 are decoupling capacitors for the supply voltages and reference output.

The AD7572 has a high-speed digital interface with three-state data outputs and can operate under the control of standard microprocessor Read ($\overline{RD}$) and decoded address ($\overline{CS}$) signals. Interface timing is sufficiently fast to allow the AD7572 to operate with most popular microprocessors, with three-state enable times of only 90ns and bus relinquish times of 75ns.

The AD7572 is fabricated in Analog Devices Linear Compatible CMOS process (LC²MOS), an advanced, all ion-implanted process that combines fast CMOS logic and linear, bipolar circuits on a single chip, thus achieving excellent linear performance while still retaining low CMOS power levels.

The AD7572 is packaged in a 0.3", 24-pin DIP and is also available in 28-pin leadless ceramic chip carrier (LCC).

PRODUCT HIGHLIGHTS

1. Fast, 5μs and 12.5μs conversion times make the AD7572 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any wideband data acquisition system.
2. On-chip buried-zener reference has temperature coefficient as low as 25ppm/°C, giving low full-scale drift over the operating temperature range.
3. Stable DAC and comparator give excellent linearity and low zero error over the full temperature range.
4. Fast, easy-to-use digital interface has three-state bus access times of 90ns and bus relinquish times of 75ns, allowing the AD7572 to interface to most popular microprocessors.
5. LC²MOS circuitry gives low power drain (135mW) from +5, −15 volt supplies.
6. 24-pin 0.3" package offers space saving over parts in 28-pin 0.6" DIP.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS

(V_{DD} = 5V ±5%, V_{SS} = −15V ±5%, f_{CLK}: 2.5MHz for AD7572XX05, 1MHz for AD7572XX12. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode).

Parameter	AD7572JN[1] AD7572AQ AD7572SQ	AD7572KN AD7572BQ AD7572TQ	AD7572LN AD7572CQ AD7572UQ	Units	Test Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Integral Nonlinearity	±1	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	LSB max	
Minimum Resolution for which no Missing Codes are guaranteed	12	12	12	Bits	
Offset Error @ +25°C	±4	±3	±2	LSB max	
T_{min} to T_{max}	±8	±6	±4	LSB max	Typical Change over Temp is ±2LSBs
Full Scale (FS) Error[2] @ +25°C	±15	±10	±10	LSB max	V_{DD} = 5V; V_{SS} = −15V; FS = 5V Ideal Last Code Transition = FS − 3/2LSBs
Full Scale TC[3,4]	45	25	25	ppm/°C max	
ANALOG INPUT					
Input Voltage Range	0 to +5	0 to +5	0 to +5	Volts	For bipolar operation, refer to Figures 10 &
Input Current	3.5	3.5	3.5	mA max	12 of full 12-page data sheet.
INTERNAL REFERENCE VOLTAGE					
V_{REF} Output @ +25°C	−5.2/−5.3	−5.2/−5.3	−5.2/−5.3	V min/V max	−5.25V ±1%
V_{REF} Output TC	40	20	20	ppm/°C typ	
Output Current Sink Capability	500	500	500	µA max	(External Load Should Not Change During Conversion)
POWER SUPPLY REJECTION					
V_{DD} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{SS} = −15V V_{DD} = +4.75V to +5.25V
V_{SS} Only	±1/2	±1/2	±1/2	LSB typ	FS Change, V_{DD} = 5V V_{SS} = −14.25V to −15.75V
LOGIC INPUTS					
$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN					
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	V min	
C_{IN},[5] Input Capacitance	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$, HBEN					
I_{IN}, Input Current	±10	±10	±10	µA max	V_{IN} = 0 to V_{DD}
CLK IN					
I_{IN}, Input Current	±20	±20	±20	µA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS					
D11–D0/8, $\overline{BUSY}$, CLK OUT					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OL}, Output High Voltage	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200µA
Floating State Leakage Current					
D11–D0/8	±10	±10	±10	µA max	
Floating State Output Capacitance[5]	15	15	15	pF max	
CONVERSION TIME					
AD7572XX05					
Synchronous Clock	5	5	5	µs max	f_{CLK} = 2.5MHz. See Under
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	µs min/max	Control Inputs Synchronization
AD7572XX12					
Synchronous Clock	12.5	12.5	12.5	µs max	f_{CLK} = 1MHz
Asynchronous Clock	12/13	12/13	12/13	µs min/max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V NOM	±5% for Specified Performance
V_{SS}	−15	−15	−15	V NOM	±5% for Specified Performance
I_{DD}[6]	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V
I_{SS}[6]	12	12	12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V
Power Dissipation	135	135	135	mW typ	
	215	215	215	mW max	

NOTES

[1]Temperature range as follows: AD7572JN, KN, LN; 0 to +70°C.
AD7572AQ, BQ, CQ; −25°C to +85°C.
AD7572SQ, TQ, UQ; −55°C to +125°C.

[2]Includes internal voltage reference error.

[3]Full Scale TC = ΔFS/ΔT, where ΔFS is Full Scale change from T_A = +25°C to T_{min} or T_{max}.

[4]Includes internal voltage reference drift.

[5]Sample tested to ensure compliance.

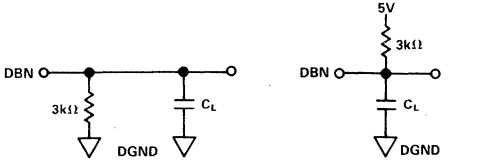
[6]Power supply current is measured when AD7572 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5V, V_{SS} −5V)

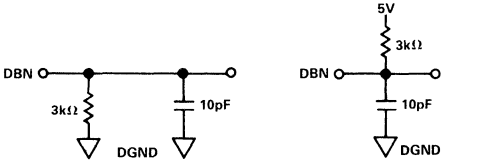
Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, L, A, B, C Grades)	Limit at T_{min}, T_{max} (S, T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L = 20pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L = 100pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	0	0	0	ns min	HBEN to $\overline{RD}$ Setup Time
t_9	0	0	0	ns min	HBEN to $\overline{RD}$ Hold Time
t_{10}	500	500	500	ns min	Delay Between Successive Read Operations

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6) *b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)*

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Output Float Delay

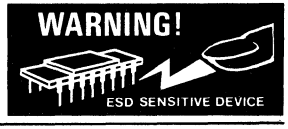
ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3V to +7V
V_{SS} to DGND . . . . . +0.3V to −17V
AGND to DGND . . . . . −0.3V, V_{DD} + 0.3V
AIN to AGND . . . . . −15V to +15V
Digital Input Voltage to DGND
(Pins 17, 19–21 . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND
(Pins 4–11, 13–16, 18, 22 . . . . . −0.3V, V_{DD} +0.3V
Operating Temperature Range
JN, KN, LN . . . . . 0 to +70°C
AQ, BQ, CQ . . . . . −25°C to +85°C
SQ, TQ, UQ . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation (Any Package) to +75°C 1,000mW
Derates above +75°C by . . . . . 10mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.



ORDERING INFORMATION[1,2]

CONVERSION TIME = 5μs

Full Scale TC	Temperature Range and Package: Integral Nonlinearity T_{min} to T_{max}	Plastic 0 to +70°C	Hermetic[3] −25°C to +85°C	Hermetic[3] −55°C to +125°C
45ppm/°C	±1	AD7572JN05	AD7572AQ05	AD7572SQ05
25ppm/°C	±1	AD7572KN05	AD7572BQ05	AD7572TQ05
25ppm/°C	±1/2	AD7572LN05	AD7572CQ05	AD7572UQ05

CONVERSION TIME = 12.5μs

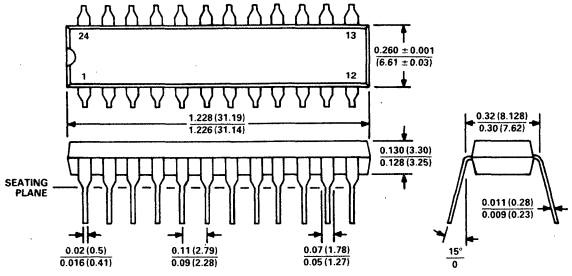
Full Scale TC	Temperature Range and Package: Integral Nonlinearity T_{min} to T_{max}	Plastic 0 to +70°C	Hermetic[3] −25°C to +85°C	Hermetic[3] −55°C to +125°C
45ppm/°C	±1	AD7572JN12	AD7572AQ12	AD7572SQ12
25ppm/°C	±1	AD7572KN12	AD7572BQ12	AD7572TQ12
25ppm/°C	±1/2	AD7572LN12	AD7572CQ12	AD7572UQ12

NOTES
[1]To order military standard 883B REV. C processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]Leadless Ceramic Chip Carrier versions are available. To order, replace Q with E.
[3]Analog Devices reserves the right to ship either ceramic or cerdip hermetic packages.

OUTLINE DIMENSIONS

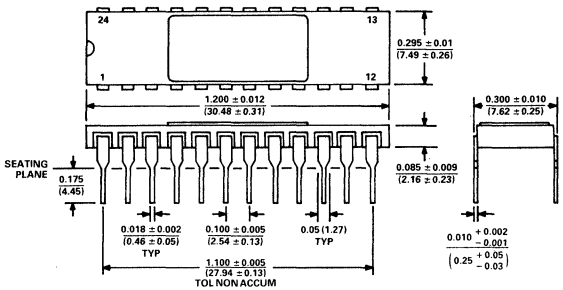
Dimensions shown in inches and (mm).

24-PIN PLASTIC (SUFFIX N)



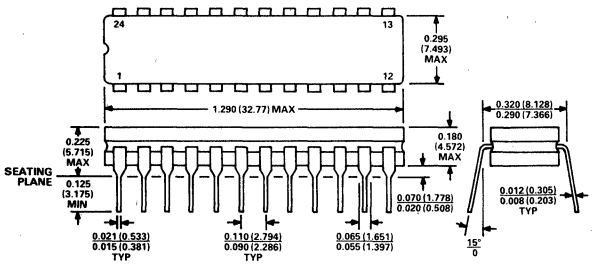
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN/LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-PIN CERAMIC (SUFFIX Q)



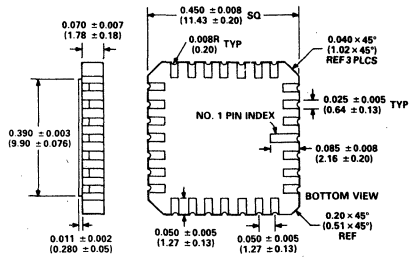
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.
3. METAL LID IS CONNECTED TO DGND

24-PIN CERDIP (SUFFIX Q)



NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-TERMINAL LEADLESS CHIP CARRIER



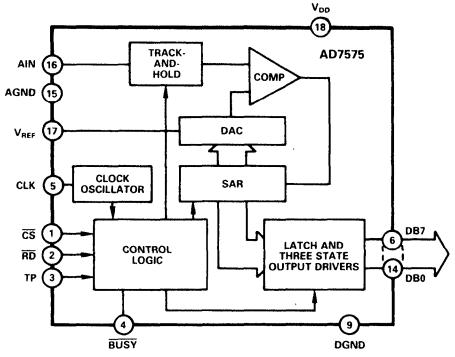
ANALOG DEVICES

LC²MOS
5μs 8-Bit ADC with Track/Hold

AD7575

FEATURES
Fast Conversion Time: 5μs
On-Chip Track/Hold
Low Total Unadjusted Error: 1LSB
Full Power Signal Bandwidth: 50kHz
Single +5V Supply
100ns Data Access Time
Low Power (15mW typ)
Low Cost
Small Package

AD7575 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7575 is a high-speed 8-bit ADC with a built-in track/hold function. The successive approximation conversion technique is used to achieve a fast conversion time of 5μs, while the built-in track/hold allows full-scale signals up to 50kHz (386mV/μs slew rate) to be digitized. The AD7575 requires only a single +5V supply and a low-cost, 1.23V bandgap reference in order to convert an input signal range of 0 to $2V_{REF}$.

The AD7575 is designed for easy interfacing to all popular 8-bit microprocessors using standard microprocessor control signals ($\overline{CS}$ and $\overline{RD}$) to control starting of the conversion and reading of the data. The interface logic allows the AD7575 to be easily configured as a memory mapped device and the part can be interfaced as SLOW-MEMORY or ROM. All data outputs of the AD7575 are latched and three-state buffered to allow direct connection to a microprocessor data bus or I/O port.

The AD7575 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process and is packaged in a small, 0.3" wide, 18-pin DIP.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time/Low Power
   The fast, 5μs conversion time of the AD7575 makes it suitable for digitizing wideband signals at audio and ultrasonic frequencies, while retaining the advantage of low CMOS power consumption.
2. On-Chip Track/Hold
   The on-chip track/hold function is completely self-contained and requires no external hold capacitor. Signals with slew rates up to 386mV/μs (e.g., 2.46V peak-to-peak 50kHz sine waves) can be digitized with full accuracy.
3. Low Total Unadjusted Error
   The zero, full-scale and linearity errors of the AD7575 are so low that the total unadjusted error at any point on the transfer function is less than 1LSB and offset and gain adjustments are not required.
4. Single Supply Operation
   Operation from a single +5V supply with a low-cost +1.23V bandgap reference allows the AD7575 to be used in 5V microprocessor systems without any additional power supplies.
5. Fast Digital Interface
   Fast interface timing allows the AD7575 to interface easily to the fast versions of most popular microprocessors such as the Z80H, 8085A-2, 6502B, 68B09 and the DSP processor, the TMS32010.

SPECIFICATIONS

(V_{DD} = +5V; V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 4MHz external; All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7575JN[1] AD7575AQ	AD7575KN AD7575BQ	AD7575SQ	AD7575TQ	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which						
No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 16
DC Input Impedance	10	10	10	10	MΩ min	
Slew Rate, Tracking	0.386	0.386	0.386	0.386	V/μs max	
SNR[3]	45	45	45	45	dB min	V_{IN} = 2.46V p-p @ 10kHz; See Figure 11
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	μA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	μA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	μA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	μA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40μA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	μA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	5	5	5	5	μs	f_{CLK} = 4MHz
With Internal Clock, T_A = 25°C	5	5	5	5	μs min	Using recommended clock
	15	15	15	15	μs max	components shown in Figure 15.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES

[1]Temperature Ranges are as follows:
AD7575JN, KN 0 to +70°C
AD7575AQ, BQ −25°C to +85°C
AD7575SQ, TQ −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7575 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = logic HIGH.

Specifications subject to change without notice.

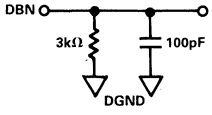
TIMING SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S, T Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	100	100	120	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	100	100	120	ns max	Data Access Time after $\overline{RD}$
t_4	100	100	120	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	80	80	100	ns max	Data Access Time after $\overline{BUSY}$
t_7[3]	10	10	10	ns min	Data Hold Time
	80	80	100	ns max	
t_8	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay

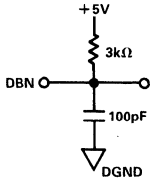
NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

3

Test Circuits

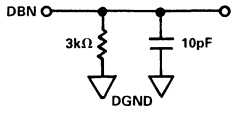


a. High-Z to V_{OH}

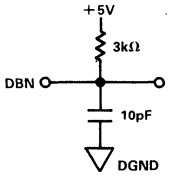


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

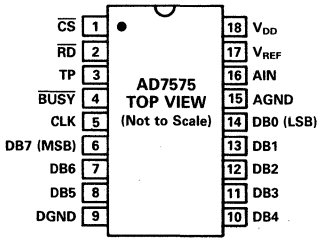
V_{DD} TO AGND	−0.3V, +7V
V_{DD} TO DGND	−0.3V, +7V
AGND TO DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (Pins 1, 2)	−0.3V, V_{DD}
Digital Output Voltage to DGND (Pins 4, 6-8, 10-14)	−0.3V, V_{DD}
CLK Input Voltage (Pin 5) to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
AIN TO AGND	−0.3V, V_{DD}
Operating Temperature Range	
JN, KN	0 to +70°C
AQ, BQ	−25°C to +85°C
SQ, TQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



ORDERING INFORMATION[1]

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[2] −25°C to +85°C	Cerdip[2] −55°C to +125°C
±1LSB	AD7575JN	AD7575AQ	AD7575SQ
±½LSB	AD7575KN	AD7575BQ	AD7575TQ

NOTES
[1]For information regarding /883B versions, contact your local Analog Devices sales office for military data sheet.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bits resolution can resolve 1 part in 2^8 (i.e., 256) of full scale. For the AD7575 with +2.46V full scale one LSB is 9.61mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes full scale error, relative accuracy and offset error.

RELATIVE ACCURACY

Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full scale transition point.

SNR

Signal-to-Noise Ratio (SNR) is the ratio of the desired signal to the noise produced in the sampled and digitized analog signal. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave input is given by SNR = (6.02N + 1.76)dB
where N is the number of bits in the ADC.

FULL SCALE ERROR (GAIN ERROR)

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2LSB's.

ANALOG INPUT RANGE

With V_{REF} = +1.23V the maximum analog input voltage range is 0 to +2.46V. The output data in LSB's is related to the analog input voltage by the integer value of the following expression:

$$\text{Data (LSB's)} = \frac{256\ AIN}{2V_{REF}} + 0.5$$

SLEW RATE

Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. Slew Rate limitations may restrict the analog signal bandwidth for full-scale analog signals below the bandwidth allowed from sampling theorem considerations.

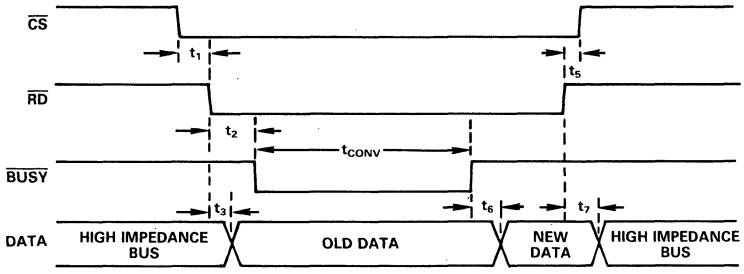


Figure 3. Slow Memory Interface Timing Diagram

TIMING AND CONTROL OF THE AD7575

The two logic inputs on the AD7575, $\overline{CS}$ and $\overline{RD}$, control both the starting of conversion and the reading of data from the part. A conversion is initiated by bringing both these control inputs LOW. Two interface options then exist for reading the output data from the AD7575. These are the Slow Memory Interface and ROM Interface and their operation is outlined below. It should be noted that the TP pin of the AD7575 must be hardwired HIGH to ensure correct operation of the part. This pin is used in testing the device and should not be used as a feedthrough pin in double-sided printed circuit boards.

SLOW MEMORY INTERFACE

The first interface option is intended for use with microprocessors which can be forced into a WAIT STATE for at least 5μs (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7575 address bringing $\overline{CS}$ and $\overline{RD}$ LOW. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor into a WAIT state. The input signal, which had been tracked by the analog input, is held on the third falling clock edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW (see Figure 12). The AD7575 then performs a conversion on this acquired input signal value. When the conversion is complete ($\overline{BUSY}$ goes HIGH), the processor completes the memory READ and acquires the newly-converted data. The timing diagram for this interface is shown in Figure 3.

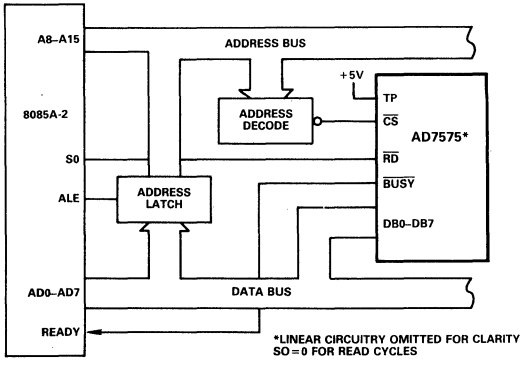


Figure 4. AD7575 to 8085A-2 Slow Memory Interface

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT and then READ data with a single READ instruction. The fast conversion time of the AD7575 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7575 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is LOW for a READ cycle) provides the READ signal to the AD7575. The connection diagram for the AD7575 to 8085A-2 Slow-Memory interface is shown in Figure 4.

ROM INTERFACE

The alternative interface option on the AD7575 avoids placing the microprocessor into a WAIT state. In this interface, a conversion is started with the first READ instruction and the second READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5. It is possible to avoid starting another conversion on the second READ (see below).

Conversion is initiated by executing a memory READ instruction to the AD7575 address causing $\overline{CS}$ and $\overline{RD}$ to go LOW. Data is also obtained from the AD7575 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW indicating that conversion is in progress and returns HIGH when conversion is complete. Once again the input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor or monitored to indicate that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7575 conversion time. For the AD7575 to operate correctly in the ROM interface mode $\overline{CS}$ and $\overline{RD}$ should not go LOW before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

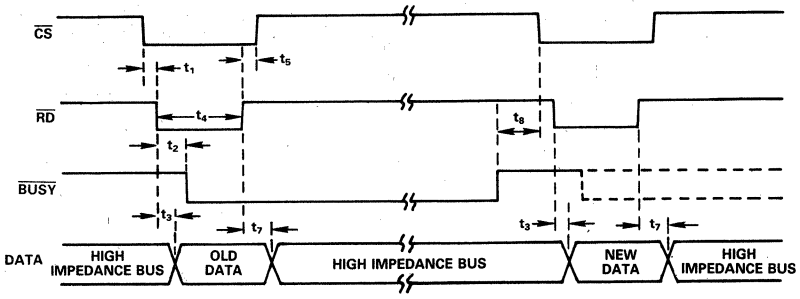


Figure 5. ROM Interface Timing Diagram

Figures 6 and 7 show connection diagrams for interfacing the AD7575 in the ROM Interface mode. Figure 6 shows the AD7575 interface to the 6502/6809 microprocessors while the connection diagram for interfacing to the Z-80 is shown in Figure 7.

As a result of its very fast interface timing the AD7575 can also be interfaced to the DSP processor, the TMS32010. The AD7575 will interface (within specifications) to the TMS32010 running at up to 18MHz but will typically work over the full clock frequency range of the TMS32010. Figure 8 shows the connection diagram for this interface. The AD7575 is mapped at a port address. Conversion is initiated using an IN A, PA instruction where PA is the decoded port address for the AD7575. The conversion result is obtained from the part using a second IN A, PA instruction and the resultant data is placed in the TMS32010 accumulator.

In many applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. The interfaces outlined previously require that for sampling at equi-distant intervals the user must count clock cycles or match software delays. This is especially difficult in interrupt driven systems where uncertainty in interrupt servicing delays would require that the AD7575 would have to have priority interrupt status and even then redundant software delays may be necessary to equalize loop delays.

This problem can be overcome by using a real time clock to control the starting of conversion. This can be derived from the clock source used to drive the AD7575 CLK pin. Since the sampling instant occurs three clock cycles after $\overline{CS}$ and $\overline{RD}$ go LOW then the input signal sampling intervals are equi-distant. The resultant data is placed in a FIFO latch which can be accessed by the microprocessor at its own rate whenever it requires the data. This ensures that data is not READ from the AD7575 during a conversion. If a data READ is performed during a conversion, valid data from the previous conversion will be accessed but the conversion in progress may be interfered with and an incorrect result is likely.

If $\overline{CS}$ and $\overline{RD}$ go LOW within 20ns of a falling clock edge the AD7575 may or may not see that falling edge as the first of the three falling clock edges to the sampling instant. In this case the sampling instant could vary by one clock period. If it is important to know the exact sampling instant, $\overline{CS}$ and $\overline{RD}$ should not go LOW within 20ns of a falling clock edge.

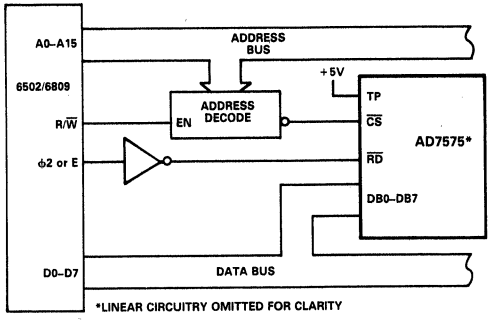


Figure 6. AD7575 to 6502/6809 ROM Interface

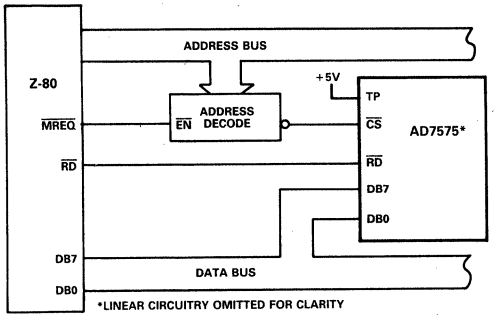


Figure 7. AD7575 to Z-80 ROM Interface

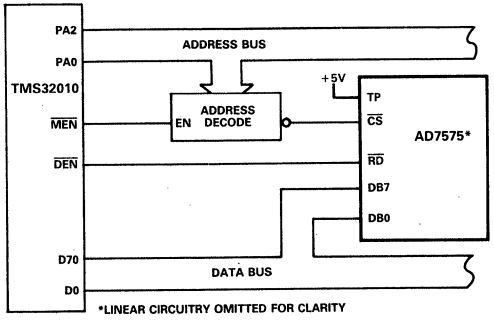


Figure 8. AD7575 to TMS32010 ROM Interface

A SAMPLED-DATA INPUT

The AD7575 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 9. When a conversion starts, switch S1 is closed and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500Ω and an input capacitance of typically 2pF the input time constant is 1ns. Thus C_{IN} becomes charged to within ±1/4LSB in 6.9 time constants or about 7ns. Since the AD7575 requires two input clock cycles (at a clock frequency of 4MHz) before going into the compare mode, there is ample time for the input voltage to settle before the first comparator decision is made. Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. The average current flowing through any source impedance can cause full-scale errors.

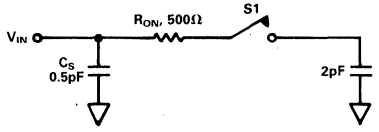


Figure 9. AD7575 Equivalent Input Circuit

REFERENCE INPUT

The reference input impedance on the AD7575 is code dependent and varies by a ratio of approximately 3-to-1 over the digital code range. The typical resistance range is from 6kΩ to 18kΩ. As a result of the code dependent input impedance, the V_{REF} input must be driven from a low impedance source. Figure 10 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23V.

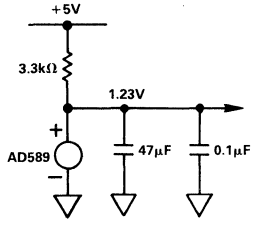


Figure 10. Reference Circuit

TRACK-AND-HOLD

The on-chip track-and-hold on the AD7575 means that input signals with slew rates up to 386mV/µs can be converted without error. This corresponds to an input signal bandwidth of 50kHz for a 2.46V peak-to-peak sine wave. Figure 11 shows a typical plot of signal-to-noise ratio versus input frequency, over the input bandwidth of the AD7575. The SNR figures are generated using a 200kHz sampling frequency and the reconstructed sine wave passes through a filter with a cutoff frequency of 50kHz.

The improvement in the SNR figures seen at the higher frequencies is due to the sharp cut-off of the filter (50kHz, 8th order Chebyshev) used in the test circuit.

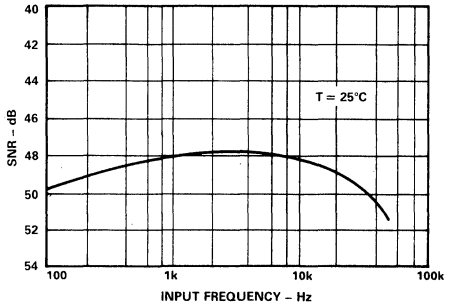


Figure 11. SNR vs. Input Frequency

The input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ go LOW. This is indicated in Figure 12 for the Slow Memory Interface. In between conversions the input signal is tracked by the AD7575 track-and-hold. Since the sampled signal is held on a small, on-chip capacitor it is advisable that the data bus be kept as quiet as possible during a conversion.

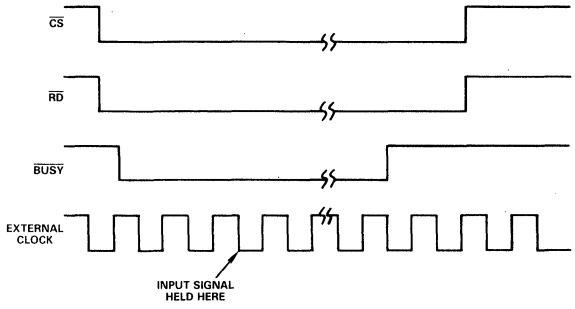


Figure 12a. Track-and-Hold (Slow Memory Interface) with External Clock

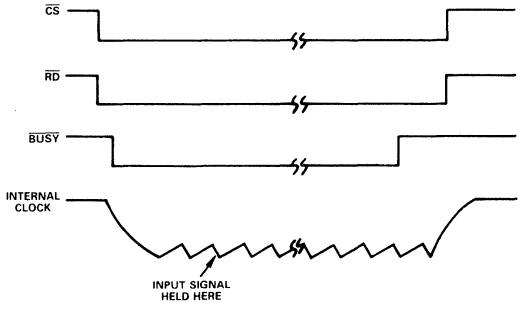


Figure 12b. Track-and-Hold (Slow Memory Interface) with Internal Clock

INTERNAL/EXTERNAL CLOCK

The AD7575 can be used with either its own internal clock or with an externally applied clock. In either case, the clock signal appearing at the CLK pin is divided internally by two to provide an internal clock signal for the AD7575. A single conversion lasts for 20 input clock cycles (10 internal clock cycles).

INTERNAL CLOCK

Clock pulses are generated by the action of the external capacitor (C_{CLK}) charging through an external resistor (R_{CLK}) and discharging through an internal switch. When a conversion is complete, the internal clock stops operating. In addition to conversion, the internal clock also controls the automatic internal reset of the SAR. This reset occurs at the start of each conversion cycle during the first internal clock pulse.

Nominal conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 13.

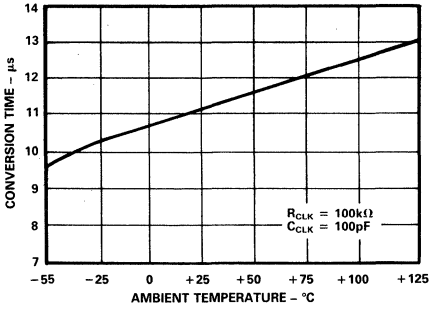


Figure 13. Typical Conversion Times vs. Temperature Using Internal Clock

The internal clock is useful in that it provides a convenient clock source for the AD7575. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ±50%. For this reason it is recommended that an external clock be used in the following situations;

1. Applications requiring a conversion time which is within 50% of 5µs, the minimum conversion time for specified accuracy. A clock frequency of 4MHz at the CLK pin gives a conversion time of 5µs.
2. Applications where time related software constraints cannot accommodate time differences which may occur due to unit to unit clock frequency variations or temperature.

EXTERNAL CLOCK

The CLK input of the AD7575 may be driven directly from 74HC, 4000B series buffers (such as 4049) or from LS TTL with a 5.6kΩ pull-up resistor. When conversion is complete, the internal clock is disabled even if the external clock is still applied. This means that the external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

The AD7575 is specified for operation at a 5µs conversion rate with a 4MHz input clock frequency. If the part is operated at slower clock frequencies, it may result in slightly degraded accuracy performance from the part. This is a result of leakage effects on the hold capacitor. Figure 14 shows a typical plot of accuracy versus conversion time for the AD7575.

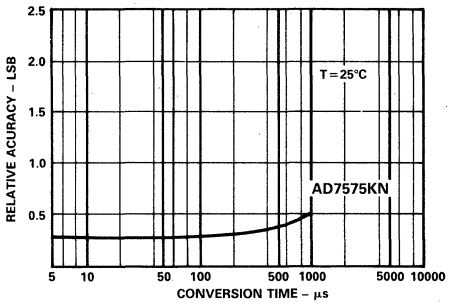


Figure 14. Accuracy vs. Conversion Time

UNIPOLAR OPERATION

The basic operation for the AD7575 is in the unipolar single supply mode. Figure 15 shows the circuit connections to achieve this while the nominal transfer characteristic for unipolar operation is given in Figure 16. Since the offset and full-scale errors on the AD7575 are very small, in many cases it will not be necessary to adjust out these errors. If calibration is required the procedure is as follows:

Offset Adjust

Offset error adjustment in single-supply systems is easily achievable by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal, AIN. The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V (e.g., TLC271). To adjust for zero offset the input signal source is set to +4.8mV (i.e., 1/2LSB) while the op-amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

Full Scale Adjust

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage − 3/2LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111 . . . 11.

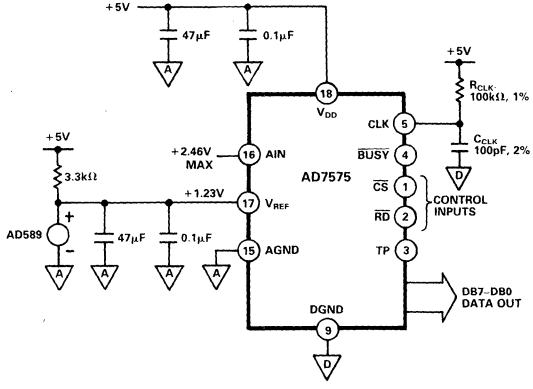


Figure 15. AD7575 Unipolar Configuration

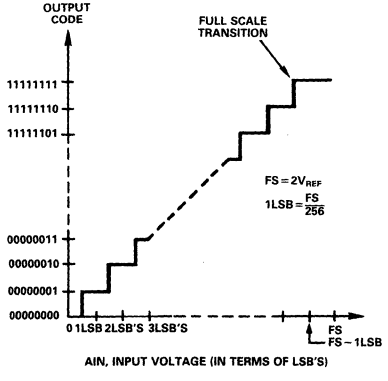


Figure 16. Nominal Transfer Characteristic for Unipolar Operation

BIPOLAR OPERATION

The circuit of Figure 17 shows how the AD7575 can be configured for bipolar operation. The output code provided by the AD7575 is offset binary. The analog input voltage range is ±2.46V, although the voltage appearing at the AIN pin of the AD7575 is in the range 0V to +2.46V. Figure 18 shows the transfer function for bipolar operation. The LSB size is now 19.22mV. Calibration of the bipolar operation is outlined below. Once again, because the errors are small it may not be necessary to adjust them. To maintain specified performance without the calibration all resistors should be 0.1% tolerance with R4 and R5 replaced by one 10kΩ resistor and R2 and R3 replaced by one 1kΩ resistor.

Offset Adjust

Offset error adjustment is achieved by applying an analog input voltage of +2.43V (+FS − 3/2LSB). Resistor R5 is then adjusted until the output code flickers between 111 . . . 10 and 111 . . . 11.

Full Scale Adjust

Full scale or gain adjustment is made by applying an analog input voltage of −2.45V (−FS + 1/2LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

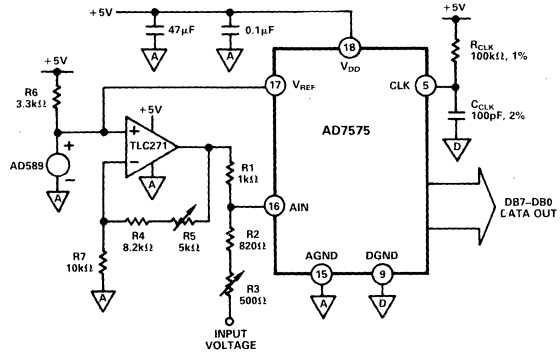


Figure 17. AD7575 Bipolar Configuration

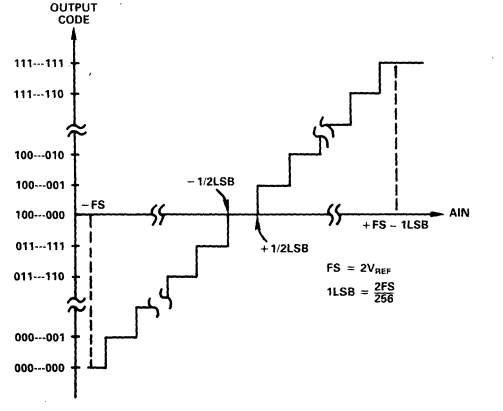


Figure 18. Nominal Transfer Characteristic for Bipolar Operation

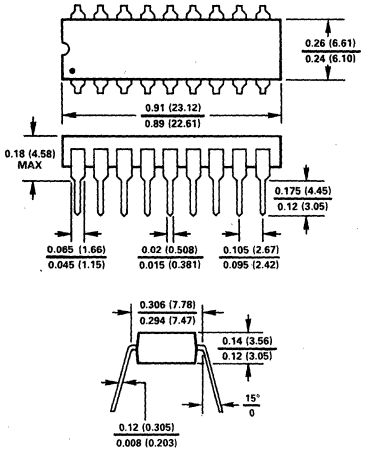
APPLICATION HINTS

1. NOISE: Both the input signal lead to AIN, and the signal return lead from AGND should be kept as short as possible to minimize input-noise coupling. In applications where this is not possible, either a shielded cable or a twisted pair transmission line between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. In general, the source resistance should be kept below 2kΩ. Larger values of source resistance can cause undesired system noise pickup.
2. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. Both the analog input and the reference input should be screened by AGND. A single point analog ground which is separate from the logic system ground should be established at or near the AD7575. This single point analog ground subsystem should be connected to the digital system ground by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

MECHANICAL INFORMATION
OUTLINE DIMENSIONS

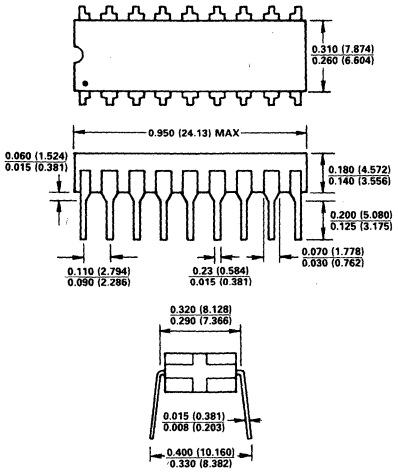
Dimensions shown in inches and (mm).

18-PIN PLASTIC DIP (SUFFIX N)



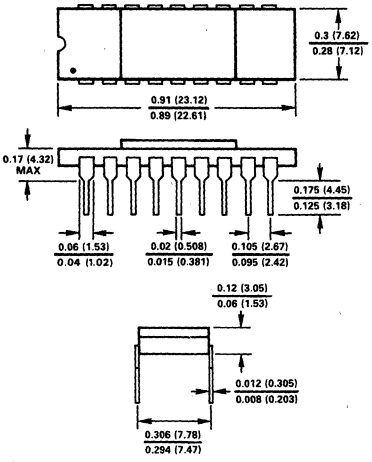
NOTE
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.

18-PIN CERDIP (SUFFIX Q)



NOTE
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.

18-PIN CERAMIC



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

ANALOG DEVICES

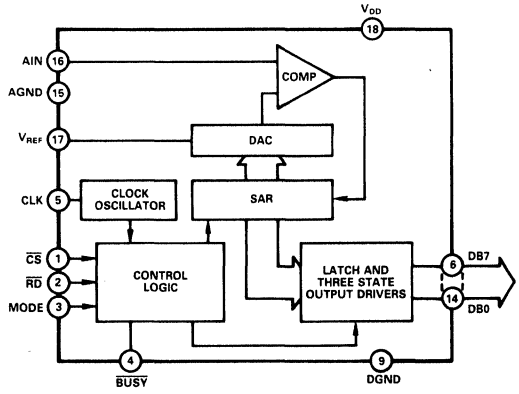
LC²MOS 10µs µP Compatible 8-Bit ADC

AD7576

FEATURES

Single +5V Operation with External Positive Reference
Fast Conversion Time: 10µs
No Missed Codes Over Full Temperature Range
Microprocessor Compatible
Low Cost
Low Power (15mW)
100ns Data Access Time

AD7576 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD7576 is a low cost, low power, microprocessor compatible 8-bit analog-to-digital converter, which uses the successive approximation technique to achieve a fast conversion time of 10µs. The device is designed to operate with an external reference of +1.23V (standard bandgap reference) and converts input signals from 0V to $2V_{REF}$.

The part is designed for ease of microprocessor interface with three control inputs ($\overline{CS}$, $\overline{RD}$ and MODE) controlling all ADC operations such as starting conversion and reading data. The interface logic allows the part to be easily configured as a memory mapped device. All data outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. The output latches serve to make the conversion process transparent to the microprocessor.

The part is designed for single +5V operation, has on-board comparator, interface logic, and internal/external clock option. This makes the AD7576 ideal for most ADC/µP interface applications.

The AD7576 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process and is packaged in a small, 0.3" wide, 18-pin DIP.

PRODUCT HIGHLIGHTS

1. Single Supply Operation
   Operation from a single +5V supply with a +1.23V reference allows operation of the AD7576 with microprocessor systems without any additional power supplies.
2. Low Power
   CMOS fabrication of the AD7576 results in a very low power dissipation figure of 15mW typical.
3. Versatile Interface Logic
   The AD7576 can be configured to perform continuous conversions or to convert on command. It can be interfaced as SLOW-MEMORY or ROM, allowing versatile interfacing to most microprocessors.
4. Fast Conversion Time
   The fabrication of the AD7576 on Analog Devices' Linear Compatible CMOS (LC²MOS) process enables fast conversion times of 10µs, eliminating the need for expensive Sample-and-Holds in many low frequency applications.

SPECIFICATIONS

(V_{DD} = +5V; V_{REF} = +1.23V; AGND = DGND = 0V; f_{CLK} = 2MHz external; All specifications T_{min} to T_{max} unless otherwise noted.)

Parameter	AD7576JN[1] AD7576AQ	AD7576KN AD7576BQ	AD7576SQ	AD7576TQ	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±½	±1	±½	LSB max	
Minimum Resolution for which No Missing Codes is Guaranteed	8	8	8	8	Bits max	
Full Scale Error						
25°C	±1	±1	±1	±1	LSB max	Full Scale TC is typically 5ppm/°C
T_{min} to T_{max}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
25°C	±½	±½	±½	±½	LSB max	Offset TC is typically 5ppm/°C
T_{min} to T_{max}	±½	±½	±½	±½	LSB max	
ANALOG INPUT						
Voltage Range	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	0 to $2V_{REF}$	Volts	1LSB = $2V_{REF}$/256; See Figure 4
DC Input Impedance	10	10	10	10	MΩ min	
REFERENCE INPUT						
V_{REF} (For specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	µA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, MODE						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
25°C	±1	±1	±1	±1	µA max	V_{IN} = 0 or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	µA max	V_{INL} = 0V
I_{INH}, Input High Current	700	700	800	800	µA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40µA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	µA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	10	10	10	10	µs	f_{CLK} = 2MHz
With Internal Clock, T_A = 25°C	10	10	10	10	µs min	Using recommended clock
	20	20	20	20	µs max	components shown in Figure 3.
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3mA with V_{DD} = +5V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±¼	±¼	±¼	±¼	LSB max	4.75V≤V_{DD}≤5.25V

NOTES

[1]Temperature Ranges are as follows:
AD7576JN, KN 0 to +70°C
AD7576AQ, BQ −25°C to +85°C
AD7576SQ, TQ −55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition which occurs at 1/2LSB.

[3]Sample tested at 25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

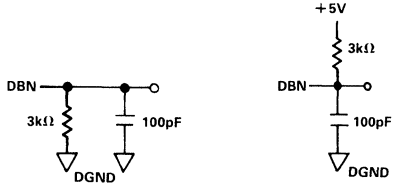
[5]Power supply current is measured when AD7576 is inactive i.e. when $\overline{CS}$ = $\overline{RD}$ = MODE = $\overline{BUSY}$ = logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +1.23V, AGND = DGND = 0V)

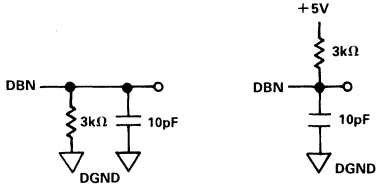
Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A, B Grades)	Limit at T_{min}, T_{max} (S, T Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	100	100	120	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	100	100	120	ns max	Data Access Time after $\overline{RD}$
t_4	100	100	120	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	80	80	100	ns max	Data Access Time after $\overline{BUSY}$
t_7[3]	10	10	10	ns min	Data Hold Time
	80	80	100	ns max	
t_8	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 2. Load Circuits for Data Hold Time Test

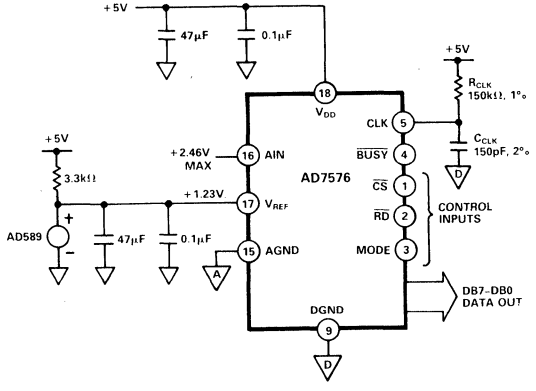


Figure 3. AD7576 Operational Diagram

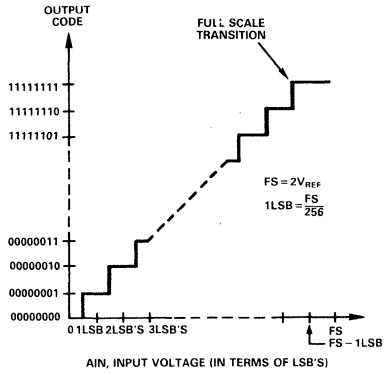


Figure 4. Nominal Transfer Characteristic for Unipolar Operation

ABSOLUTE MAXIMUM RATINGS*

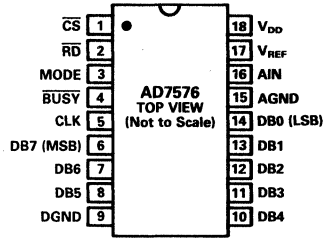
V_{DD} TO AGND	−0.3V, +7V
V_{DD} TO DGND	−0.3V, +7V
AGND TO DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (Pins 1-3)	−0.3V, V_{DD}
Digital Output Voltage to DGND (Pins 4, 6-8, 10-14)	−0.3V, V_{DD}
CLK Input Voltage (Pin 5) to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
AIN TO AGND	−0.3V, V_{DD}
Operating Temperature Range	
JN, KN	0 to +70°C
AQ, BQ	−25°C to +85°C
SQ, TQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 secs)	300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above 75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Cerdip[1] −55°C to +125°C
±1LSB	AD7576JN	AD7576AQ	AD7576SQ
±½LSB	AD7576KN	AD7576BQ	AD7576TQ

NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

TERMINOLOGY

LEAST SIGNIFICANT BIT (LSB)

An ADC with 8-bits resolution can resolve 1 part in 2^8 (i.e., 256) of full scale. For the AD7576 with +2.46V full scale one LSB is 9.61mV.

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes full scale error, relative accuracy and offset error.

RELATIVE ACCURACY

Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full scale transition point.

FULL SCALE ERROR (GAIN ERROR)

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2LSB's.

ANALOG INPUT RANGE

With V_{REF} = +1.23V the maximum analog input voltage range is 0 to +2.46V. The output data in LSB's is related to the analog input voltage by the integer value of the following expression:

$$\text{Data (LSB's)} = \frac{256\ \text{AIN}}{2V_{REF}} + 0.5$$

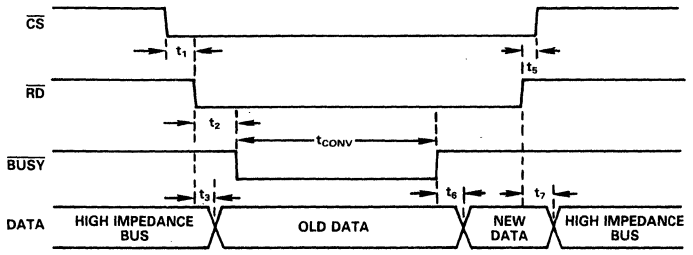


Figure 5. Slow Memory Interface Timing Diagram

TIMING AND CONTROL OF THE AD7576

The AD7576 is capable of two basic operating modes which are outlined in the timing diagrams below. These two operating modes are an Asynchronous Conversion Mode and a Synchronous Conversion Mode. The selection of the required operating mode is determined by the status of the MODE pin. When this pin is HIGH, the device performs conversions only when the required control signals ($\overline{CS}$ and $\overline{RD}$) are applied; with this pin LOW the device performs continuous conversions and $\overline{CS}$ and $\overline{RD}$ are used only to access the output data.

SYNCHRONOUS CONVERSION MODE

In the Synchronous Conversion mode the AD7576 will perform a conversion when requested to do so by the microprocessor. The MODE pin of the AD7576 is tied HIGH to place the device in Synchronous Conversion operation. Two interface options exist for reading the output data from the AD7576.

Slow Memory Interface

The first of these interface options is intended for use with microprocessors which can be forced into a WAIT STATE for at least 10μs (such as the 8085A). The microprocessor starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7576 address. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW) placing the processor in a WAIT state. When conversion is complete ($\overline{BUSY}$ goes HIGH) the processor completes the memory READ.

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the AD7576 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time. The timing diagram for this interface is shown in Figure 5.

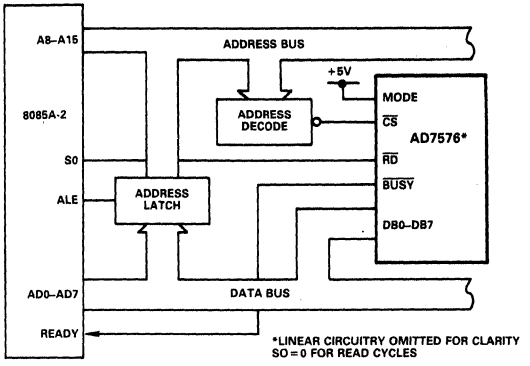


Figure 6. AD7576 to 8085A-2 Slow Memory Interface

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7576 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is 0 for a READ cycle) provides the READ signal to the AD7576. The AD7576 connection diagram to the 8085A-2 is shown in Figure 6.

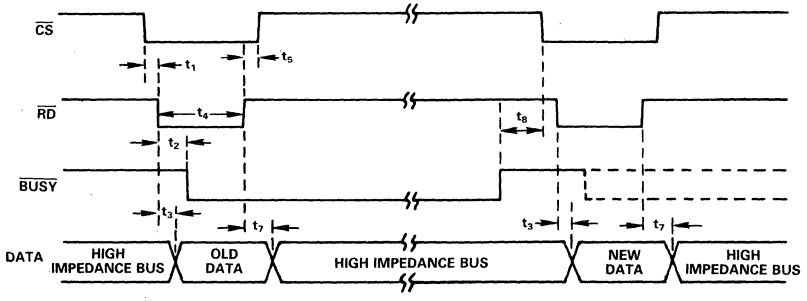


Figure 7. ROM Interface Timing Diagram

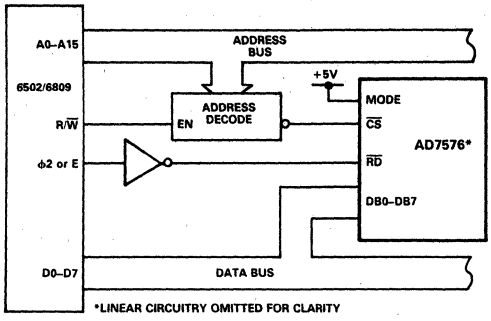


Figure 8. AD7576 to 6502/6809 ROM Interface

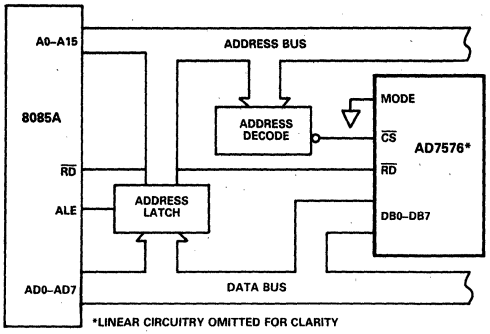


Figure 10. AD7576 to 8085A Asynchronous Conversion Mode Interface

ROM Interface

The alternative interface option in the Synchronous Conversion mode avoids placing the microprocessor into a WAIT state. In this interface, conversion is started with the first read instruction and a second read instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 7 while Figure 8 shows the connection diagram for the AD7576 with the 6502/6809 microprocessors.

Conversion is initiated by executing a memory READ instruction to the AD7576 address. Data is also obtained from the AD7576 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW during conversion and returns HIGH when conversion is complete.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor indicating that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7576 conversion time. For the AD7576 to operate correctly in the ROM Interface mode $\overline{CS}$ and $\overline{RD}$ should not go low before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH then a second conversion does not occur.

ASYNCHRONOUS CONVERSION MODE

When the MODE pin of the AD7576 is tied LOW, the device performs continuous conversions, and the control lines $\overline{CS}$ and $\overline{RD}$ are used only to read the data from the converter. The timing diagram for this operating mode is outlined in Figure 9, with the connection diagram to the 8085A shown in Figure 10.

Data is obtained from the AD7576 by executing a memory READ instruction to its address. The A/D process is completely transparent to the microprocessor and the AD7576 will behave like a ROM. Data may be read at any time completely independent of the clock. This is especially useful in internal clock applications where the user no longer has to worry about synchronizing the clock with the READ line of the microprocessor.

The data latches are normally updated by $\overline{BUSY}$ going HIGH. However, if $\overline{CS}$ and $\overline{RD}$ are LOW when $\overline{BUSY}$ goes HIGH, the contents of the data latches are frozen until $\overline{CS}$ or $\overline{RD}$ returns HIGH. This ensures that incorrect data cannot be read from the AD7576. The output latches are updated when $\overline{CS}$ or $\overline{RD}$ return HIGH and the converter is re-enabled. If $\overline{CS}$ or $\overline{RD}$ do not return HIGH the AD7576 will stop performing continuous conversions, and will not start again until either line goes HIGH.

The advantage of this mode is its simplicity. The disadvantage of this mode is that the data which is read is not clearly defined in time. However, it will not be older than one conversion period and if this uncertainty is a problem it can be overcome by monitoring the $\overline{BUSY}$ line.

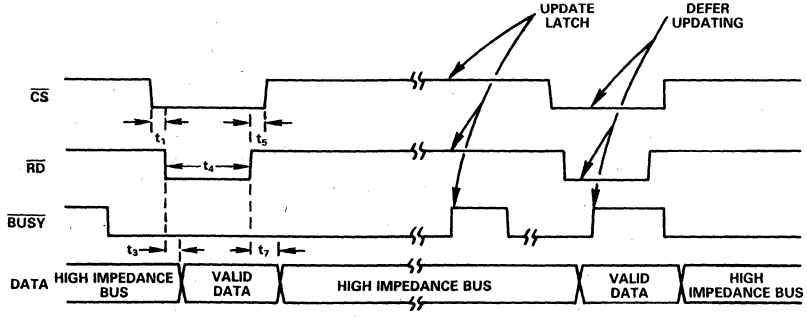


Figure 9. Asynchronous Conversion Mode Timing Diagram

Mode Pin	Operating Mode	Device Operation
High	Synchronous Conversion	1. $\overline{\text{BUSY}}$ connected to µP ready input. Memory Read instruction starts conversion. µP is driven into wait state for duration of AD7576 conversion. 2. Memory Read instruction starts conversion. $\overline{\text{BUSY}}$ generates interrupt when conversion is complete. Second Memory Read instruction reads newly-converted data. Alternatively, when software delay between the two read instructions is longer than conversion time, the second read instruction will access the newly-converted data. In both cases the second read normally starts a second conversion.
Low	Asynchronous Conversion	AD7576 performs continuous conversions. The data may be read from the device independent of CLK by executing a Memory Read instruction.

Table I. AD7576 Operating Modes

A SAMPLED-DATA INPUT

The AD7576 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 11. When a conversion starts, switch S1 is closed and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500Ω and an input capacitance of typically 2pF the input time constant is 1ns. Thus C_{IN} becomes charged to within ± ¼ LSB in 6.9 time constants or about 7ns. Since the comparator switches are operating at one half the input clock frequency of 2MHz, there is ample time for the input voltage to settle before the comparator decision is made (at the end of a clock period). Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. This average current flowing through any source impedance can cause full-scale errors.

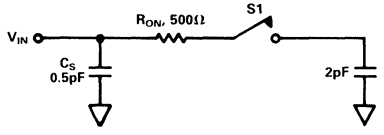


Figure 11. AD7576 Equivalent Input Circuit

INTERNAL/EXTERNAL CLOCK

The AD7576 can be used with either its own internal clock or with an externally applied clock. In either case, the clock signal appearing at the CLK pin is divided internally by two to provide an internal clock signal for the AD7576. A single conversion lasts for 20 input clock cycles (10 internal clock cycles).

INTERNAL CLOCK

Clock pulses are generated by the action of the external capacitor (C_{CLK}) charging through an external resistor (R_{CLK}) and discharging through an internal switch. When a conversion is complete, the internal clock stops operating. In addition to conversion, the internal clock also controls the automatic internal reset of the SAR. This reset occurs at the start of each conversion cycle during the first internal clock pulse.

Nominal conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 12.

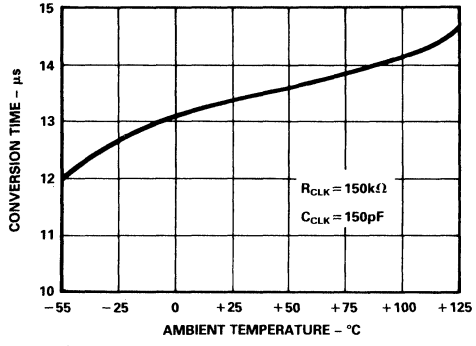


Figure 12. Typical Conversion Time vs. Temperature Using Internal Clock

The internal clock is useful in that it provides a convenient clock source for the AD7576. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ± 30%. For this reason it is recommended that an external clock be used in the following situations;

1. Applications requiring a conversion time which is within 30% of 10µs, the minimum conversion time for specified accuracy. A clock frequency of 2MHz at the CLK pin gives a conversion time of 10µs.
2. Applications where time related software constraints cannot accommodate time differences which may occur due to unit to unit clock frequency variations or temperature.

EXTERNAL CLOCK

The CLK input of the AD7576 may be driven directly from 74HC, 4000 B-series buffers (such as 4049) or from LS TTL with a 5.6kΩ pull-up resistor. When conversion is complete the internal clock is disabled even if the external clock is still applied. This means that the external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

APPLICATION HINTS

1. NOISE: Both the input signal lead to AIN, and the signal return lead from AGND should be kept as short as possible to minimize input-noise coupling. In applications where this is not possible, either a shielded cable or a twisted pair transmission line between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. In general, the source resistance should be kept below 2kΩ. Larger values of source resistance can cause undesired system noise pickup.
2. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

Both the analog input and the reference input should be screened by AGND. A single point analog ground which is separate from the logic system ground should be established at or near the AD7576. This single point analog ground subsystem should be connected to the digital system ground by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

3. OFFSET ERROR: Offset error adjustment in single-supply systems may be easily achieved by means of the offset null facility of an op-amp when used as a voltage follower for the analog input signal AIN (see Figure 13). The op-amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0V, e.g. TL091. To adjust for zero offset error the input signal source is set to +4.8mV (i.e., ½ LSB) while the 100kΩ potentiometer is varied until the ADC output code flickers between 000...00 and 000....01.
4. FULL-SCALE ADJUST: The full-scale or gain adjustment is made by forcing the analog input AIN to +2.445V (i.e., Full-Scale Voltage – 3/2 LSB). The magnitude of the reference voltage V_{REF} is then adjusted until the ADC output code flickers between 111...10 and 111...11.
5. REFERENCE CIRCUIT: Figure 14 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23V.

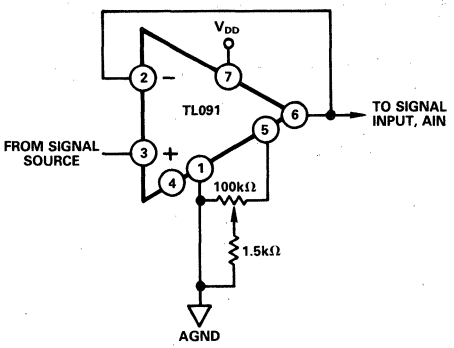


Figure 13. Offset Adjust Circuit

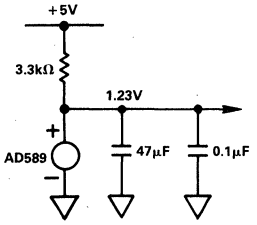
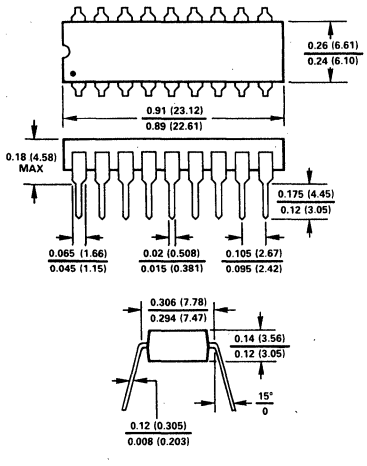


Figure 14. Reference Circuit

MECHANICAL INFORMATION
OUTLINE DIMENSIONS

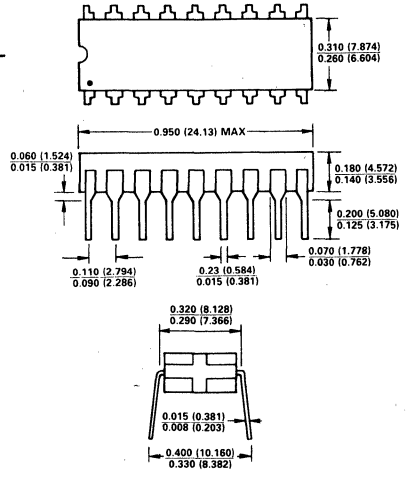
Dimensions shown in inches and (mm).

18-PIN PLASTIC DIP (SUFFIX N)



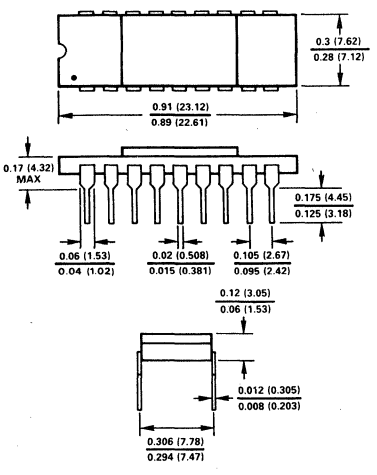
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERDIP (SUFFIX Q)



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-PIN CERAMIC



NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

ANALOG DEVICES

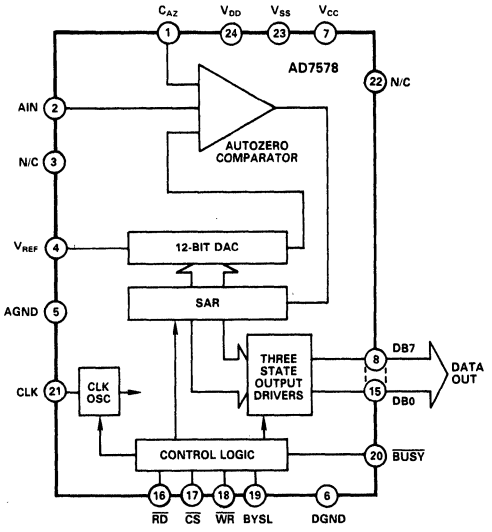
CMOS 12-Bit Successive Approximation ADC

AD7578

FEATURES

12-Bit Successive Approximation ADC
No Missed Codes Over Full Temperature Range
Low Total Unadjusted Error ±1LSB max
High Impedance Analog Input
Autozero Cycle for Low Offset Voltage
Low Power, 75mW typ
Small Size: 0.3", 24-Pin Package
Conversion Time of 100μs

AD7578 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7578 is a medium speed, monolithic 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interfacing using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$).

Conversion results are available in two bytes, 8LSBs and 4MSBs, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V.

PRODUCT HIGHLIGHTS

1. The AD7578 is a complete 12-bit A/D converter in a 24-pin package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.
4. Monolithic construction for increased reliability and small 0.3", 24-pin package.

SPECIFICATIONS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5.0V f_{CLK} = 140kHz external, all specifications T_{min} to T_{max} unless otherwise noted).

Parameter	AD7578KN[1]	AD7578BD	AD7578TD	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	
Differential Nonlinearity	±3/4	±3/4	±3/4	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)	±1/4	±1/4	±1/4	LSB max	Full Scale TC is typically 1ppm/°C
Offset Error	±1/4	±1/4	±1/4	LSB max	Offset Error TC is typically 1ppm/°C
ANALOG INPUT					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, Input Capacitance	8	8	8	pF typ	
I_{AIN}, Input Leakage Current					AIN; 0 to +5V
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 16), $\overline{CS}$ (Pin 17), $\overline{WR}$ (Pin 18)					
BYSL (Pin 19)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	μA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	μA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 21)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	μA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 8–15), $\overline{BUSY}$ (Pin 20)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200μA
Floating State Leakage Current					
(Pins 8–15)	±1	±1	±1	μA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	μs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	100/150	100/150	100/150	μs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	μA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES

[1]Temperature Range as follows: AD7578KN; 0 to +70°C
AD7578BD; −25°C to +85°C
AD7578TD; −55°C to +125°C

[2]Includes Full Scale Error, Offset Error and Relative Accuracy.

[3]Sample tested to ensure compliance.

[4]I_{SINK} for $\overline{BUSY}$ (pin 20) is 1.0 milliamp.

[5]Conversion Time includes autozero cycle time.

[6]Power supply current is measured when AD7578 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2(INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2(EXT)[2]	10	10	10	µs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_6	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_7	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{10}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{11}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{12}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	160	180	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10µs. See "External Clock Operation".
[3]t_{11} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{12} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

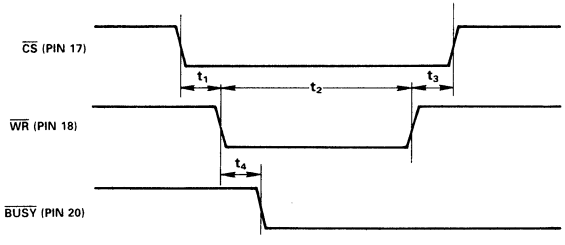
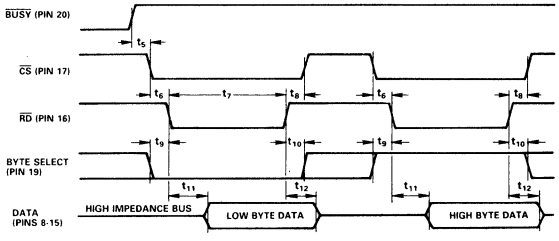
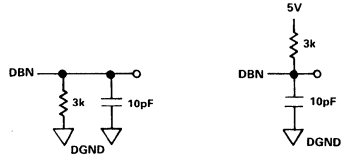


Figure 1. Start Cycle Timing



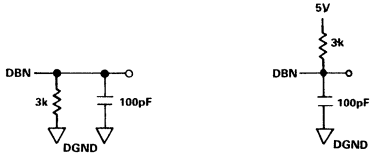
NOTES
THE TWO-BYTE CONVERSION RESULT CAN BE READ IN EITHER ORDER. FIGURE IS FOR LOW BYTE, HIGH BYTE ORDER. IF BYSL CHANGES WHILE CS & RD ARE LOW THE DATA WILL CHANGE TO REFLECT THE BYSL INPUT.

Figure 2. Read Cycle Timing



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Test (t_{11})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay Test (t_{12})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND	−0.3V, +17V
V_{SS} to DGND	+0.3V, −7V
AGND to DGND	−0.3V, V_{REF} +0.3V
V_{CC} to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
AIN to AGND	−0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 16-19, 21)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 8-15, 20)	−0.3V, V_{DD} +0.3V

Operating Temperature Range	
KN	0 to +70°C
BD	−25°C to +85°C
TD	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation (any Package) to +75°C	1,000mW
Derate above +75°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

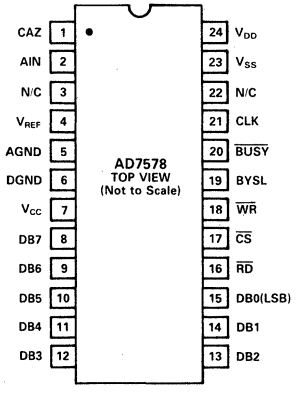
CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

Total Unadjusted Error (T_{min} to T_{max})	Temperature Range and Package		
	Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±1LSB	AD7578KN	AD7578BD	AD7578TD

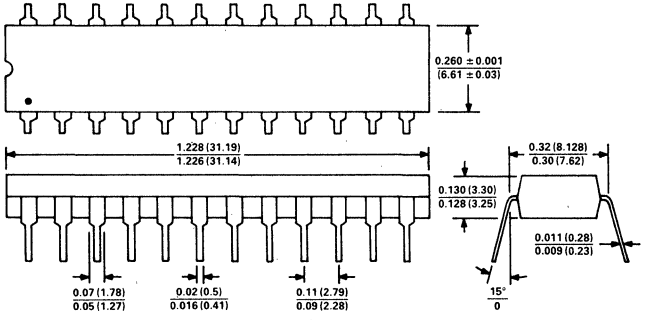
PIN CONFIGURATION



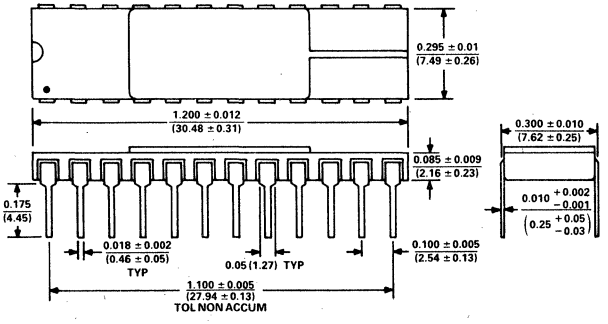
MECHANICAL INFORMATION
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-PIN PLASTIC (SUFFIX N)



24-PIN CERAMIC (SUFFIX D)



PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN	Analog Input
3	N/C	No Connect pin
4	V_{REF}	Voltage reference input. The AD7578 is specified with $V_{REF} = +5.0V$.
5	AGND	Analog Ground
6	DGND	Digital Ground
7	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
8-15		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 8	BUSY[1]	DB7
Pin 9	LOW[2]	DB6
Pin 10	LOW[2]	DB5
Pin 11	LOW[2]	DB4
Pin 12	DB11 (MSB)	DB3
Pin 13	DB10	DB2
Pin 14	DB9	DB1
Pin 15	DB8	DB0 (LSB)

[1]BUSY (Pin 8) is a converter status flag and is HIGH during a conversion.
[2]Pins 9-11 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

16	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
17	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
18	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion. When the AD7578 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
19	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 8-15.
20	$\overline{BUSY}$	$\overline{BUSY}$ indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
21	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
22	N/C	No connect pin.
23	V_{SS}	Negative supply, −5V.
24	V_{DD}	Positive supply, +15V.

Operating Information

OPERATIONAL DIAGRAM

An operational diagram for the AD7578 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7578 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

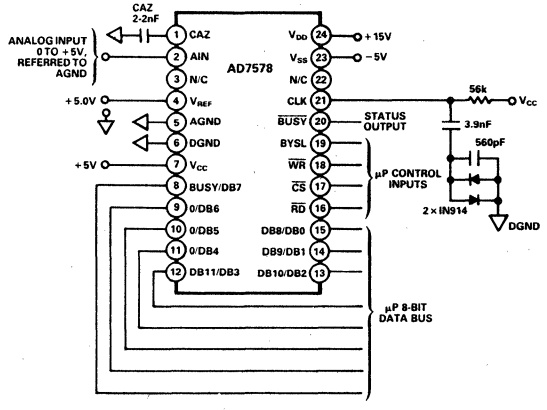


Figure 5. AD7578 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7578 operating waveforms are shown in Figure 7.

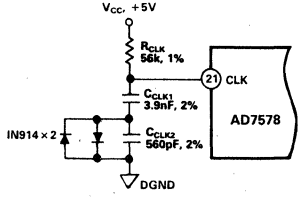


Figure 6. Circuitry Required for Internal Clock Operation

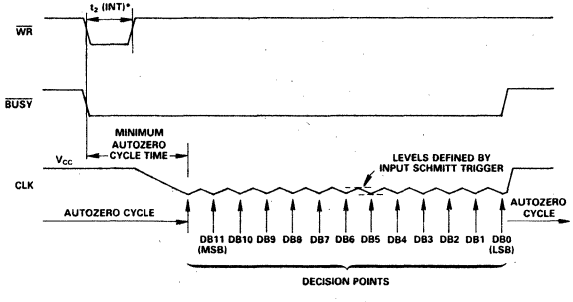


Figure 7. Operating Waveforms – Internal Clock

Between conversions ($\overline{BUSY}$ = HIGH) the AD7578 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the autozero capacitor C_{AZ} charges to AIN – V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10µs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7578. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH. The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The AD7578 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10µs since this is no longer provided automatically by the AD7578. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). The $\overline{CS}$ input must now remain valid for the extended $\overline{WR}$ pulse width. One approach to stretching the available µP signals is shown in the general 8-bit µP interface circuit of Figure 20. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

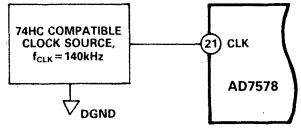


Figure 8. External Clock Operation

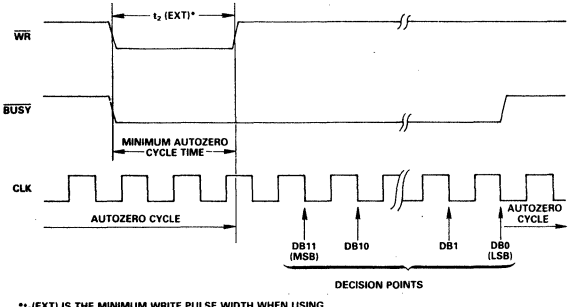


Figure 9. Operating Waveforms – External Clock

READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7578 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7578 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7578 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 10 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{\text{BUSY}}$ (pin 20) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction to the AD7578 while a conversion is in progress will restart the conversion.

COMPONENT SELECTION

1. Autozero Capacitor, C_{AZ}
   The autozero capacitor must be a low leakage, low dielectric absorption type such as polystyrene, polypropylene or teflon. To minimize noise connect the outside foil of C_{AZ} to AGND (pin 5), the analog system ground. C_{AZ} should be 2,200pF.
2. Clock Oscillator Components, R_{CLK}, C_{CLK1} and C_{CLK2}
   Clock pulses are generated by the action of series connected capacitors, C_{CLK1} and C_{CLK2} charging through an external resistor R_{CLK} and discharging through an internal switch. Nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK1}/C_{CLK2} combination is shown in Figure 10. Due to process variations, the actual operating frequency for this R_{CLK} and C_{CLK1}/C_{CLK2} combination can vary from device to device by up to 20%. For this reason, Analog Devices recommends using an external clock in the following situations:
   a. Applications requiring a conversion time which is within 20% of 100μs, the minimum conversion time for specified accuracy (a 140kHz clock frequency gives a 100μs conversion time).
   b. Applications which cannot accommodate conversion time differences which may occur due to unit clock frequency variations or temperature variations.

      It is possible to replace the fixed R_{CLK} resistor with a 50k potentiometer in series with a fixed 22kΩ resistor to allow individual adjustment of internal clock frequency in applications where 100μs conversion times are required. Reducing the value of R_{CLK} from 56k to 47k decreases the conversion time by typically 15μs.

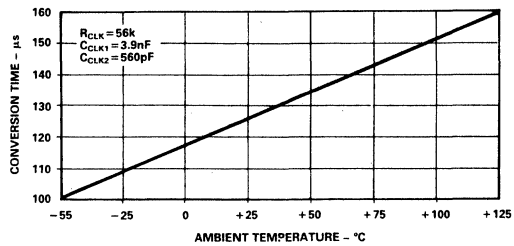


Figure 10. Typical Conversion Time vs. Temperature Using Internal Clock

Applying the AD7578

APPLYING THE AD7578

The high input impedance of the analog input, AIN, allows simple analog interfacing. Zero to +5V signal sources can be connected directly to the analog input without additional buffering for source impedances up to 5kΩ (see Figure 11). The input/output transfer characteristic and transition points for this input signal range are shown in Figure 12 and Table I respectively. The designed transition points on the AD7578 transfer characteristic occur on integer multiples of 1LSB. The output code is Natural Binary with 1LSB = (F.S.) (1/4096) = (5/4096)V = 1.22mV.

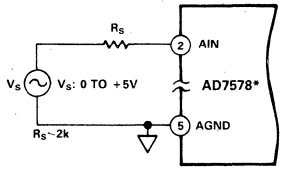


Figure 11. Unipolar 0 to +5V Operation

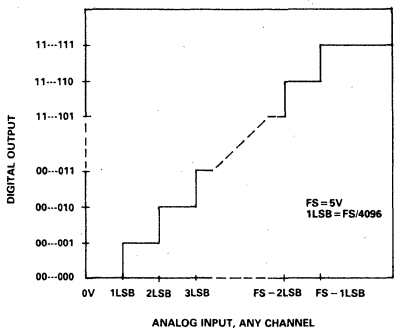


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Analog Input, Volts	Digital Output
0.00122	000 001
0.00244	000 010
2.49878	011 111
2.50000	100 000
2.50122	100 001
4.99756	111 110
4.99878	111 111

Table I. Transition Points for Unipolar 0 to +5V Operation

Signal ranges other than 0 to +5V are easily accommodated by using resistor divider networks to produce 0 to +5V signal ranges at the AD7578 input pins. Figure 13 shows a divider network to allow an input signal range of 0 to +10V. The input resistors must be selected to match within 0.01% and should be the same type and from the same manufacturer so that their temperature coefficients match. Note that since the source impedance has not been included in the resistor divider ratio, it must now be as low as possible. For Figure 13 with a source impedance of 0.5Ω the maximum error across the network is approximately 0.5LSB. The LSB size is (F.S.)(1/4096) = (10/4096)V = 2.44mV.

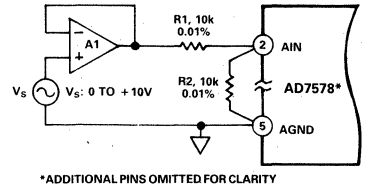


Figure 13. Unipolar 0 to +10V Operation

Bipolar signal ranges of −5V to +5V are accommodated by referencing the resistor divider network to V_{REF} as shown in Figure 14. With the resistor values shown, the signal source must be capable of sinking 0.5mA. The input/output transfer characteristic and transition points for this ±5V signal range are shown in Figure 15 and Table II respectively. The output code is Offset Binary with an LSB size of (F.S.)(1/4096) = (10/4096)V = 2.44mV.

With an analog input (V_S) of −1.22mV, the input offset voltage of A1 should be adjusted until the ADC output flickers between 0111 1111 1111 and 1000 0000 0000. Alternatively the −1/2LSB signal offset can be included in the signal conditioning electronics.

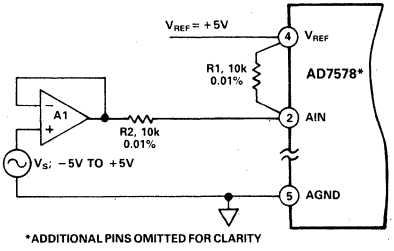


Figure 14. Bipolar −5V to +5V Operation

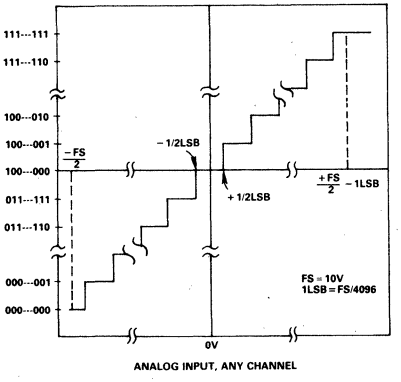


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

Analog Input, Volts	Digital Output
−4.99878	000 001
−4.99634	000 010
−0.00122	100 000
+0.00122	100 001
+4.99389	111 110
+4.99634	111 111

Table II. Transition Points for Bipolar −5V to +5V Operation

Applications

Power Supply Decoupling: All power supplies to the AD7578 should be bypassed with either 10μF tantulum or electrolytic capacitors. To ensure good high frequency performance, each capacitor should be bypassed with an 0.01μF disc ceramic capacitor. All capacitors should be placed as close as possible to the AD7578.

Reference Circuit: Figure 16 shows how to configure an AD584LH to produce a reference voltage of 5.00V. R2 provides a typical adjustment range of ±75mV. The AD584LH will contribute less than 1LSB of gain error over the commercial temperature range.

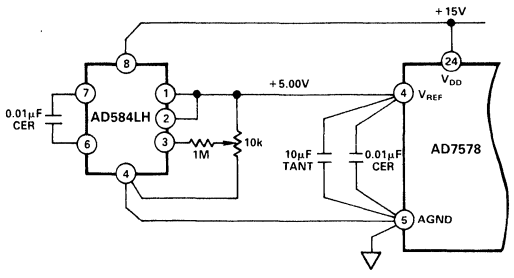


Figure 16. AD584LH as Reference Generator

Transient currents flow at the V_{REF} input during a conversion. To avoid dynamic errors place a 10μF smoothing capacitor, either tantalum or electrolytic, in parallel with a 0.01μF disc ceramic from the V_{REF} pin to AGND.

Proper Layout: Layout for a printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or close to the autozero capacitor. The analog inputs, the reference input and the autozero input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established at pin 5 (AGND) or as close as possible to the AD7578. This single point analog ground should be connected to the digital system ground, to which pin 6 (DGND) is connected, at one point only and as close to the AD7578 as possible. The autozero capacitor, bypass capacitors for the reference input and the analog supplies, AIN common and any input signal screening should be returned to the analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN and signal return leads from AGND (pin 5) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7578 data outputs are connected to a continuously busy (and noisy) microprocessor bus it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor bus to the autozero comparator. The problem exists only for ceramic package versions of the AD7578, the electrically isolated metal lid acting like a conductor to distribute the digital noise around the package.

Grounding the lid to DGND eliminates this problem. Alternatively the AD7578 can be isolated from the microprocessor bus by means of three-state buffers.

Microprocessor Interfacing

MICROPROCESSOR INTERFACING

When the AD7578 is used with its own internal clock oscillator, microprocessor interfacing is straightforward and requires at most a few external gates (see Figures 17 through 19, 21 and 22). When the AD7578 is used with an external clock source, additional circuitry is required to extend the μP control signals (see Figure 20).

MC6800, MC6809 and 6502 MICROPROCESSORS

A typical interface to the AD7578 with any of the above microprocessors is shown in Figure 17. The decoder can be enabled high using VMA in 6800 systems or enabled low by NOR'ing ϕ_0 and ϕ_2 in 6502 systems or by NOR'ing E and Q in 6809 systems. Address line A2 of the 6800 has been tied to BYSL of the AD7578. Assuming the AD7578 is assigned a memory block starting at address 8000H, a write instruction to any address in this block will start a conversion. To read the conversion results, it is necessary only to bring control inputs $\overline{CS}$ and $\overline{RD}$ low. The BYSL input (tied to A2 of the μP) determines whether the data high or low byte is placed onto the 8-bit data bus. A read instruction to address 8000H will result in the low byte of data being transferred to the μP (BYSL = Low). Similarly a read instruction to any address having A2 HIGH and within the assigned memory block, e.g., 8004H, transfers the high byte of data to the μP. The converter status flag BUSY can be polled at intervals to check whether the present conversion has finished and valid 12-bit data is available. This is accomplished by the following instructions on the 6800:

```
LDA  A  $8004     Load Flag from AD7578
ASL  A            Shift Flag into Carry
BCC     FETCH     Branch to Data Fetch
                  Subroutine if BUSY is LOW
```

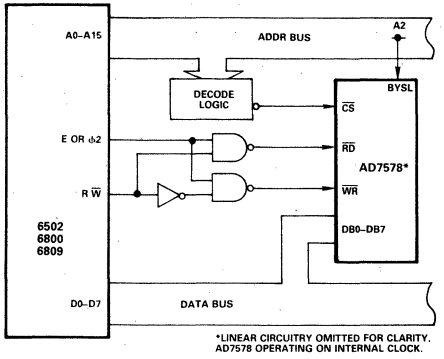


Figure 17. AD7578 – MC6800, 6809, 6502 Interface

8085A, Z80 MICROPROCESSORS

A typical interface to either of these microprocessors is shown in Figure 18. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. This interface uses slightly different low-level address decoding than the previous interface. Address line A0 of the μP has been tied to BYSL of the AD7578. This allows the 16-bit data move instructions on both the 8085A and the Z80 to be used when reading conversion results. Assuming the AD7578 is again assigned a memory block starting at address 8000H, a write instruction to any address in this block will start a conversion. The 12-bit conversion results can be read (low byte first then high byte) by a single read instruction;

On the 8085A

LHLD 8000

moves the conversion results into register pair HL

On the Z80

LD BC, (8000)

moves the conversion results into register pair BC

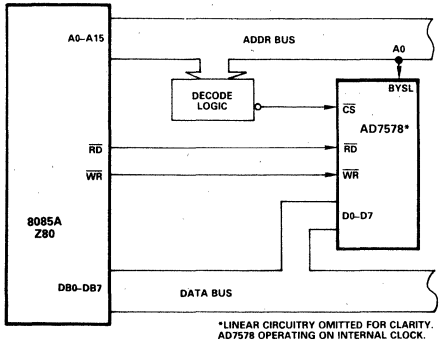


Figure 18. AD7578 – 8085A, Z80 Interface

MC68000, MC68008 MICROPROCESSOR

Figure 19 shows an AD7578–MC68000/MC68008 interface. Address line A1 of the μP has been connected to BYSL of the AD7578. With the simple decoding logic shown in Figure 19, the AD7578 is decoded in a memory block from C000H to FFFFH. A write instruction to any one of these addresses will start a conversion, i.e.,

MOVE. W D0 $C004

starts a conversion. When the conversion is complete, the μP acquires the result by reading from the AD7578, i.e,

MOVEP. W $000 (A2), D0

This instruction places the conversion data in the D0 register of the μP. Address register A2 should contain an odd-order address (having A1 high) for the AD7578, e.g., $C003.

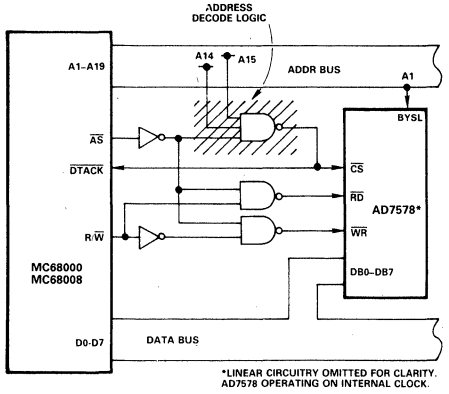


Figure 19. AD7578 – MC68000/MC68008 Interface

MICROPROCESSOR INTERFACE TO AD7578 WITH EXTERNAL CLOCK

Figure 20 shows the additional circuitry generally required to interface an 8-bit μP to the AD7578 operating from an external clock source. During a write operation, the 74121 monostable (one-shot) is triggered to latch the low level on the $\overline{CS}$ input into the 7477, a 4-bit bistable latch. The monostable timing components (not shown in Figure 20) should be chosen to provide an output pulse width corresponding to t_2 (EXT), the minimum autozero cycle time. To avoid any possibility of spurious triggering, the monostable should be enabled by a valid memory address signal. During a data read cycle, the 7477 latch is transparent and data is read normally. Note that the μP write and read cycle times are unaffected by the interface circuitry.

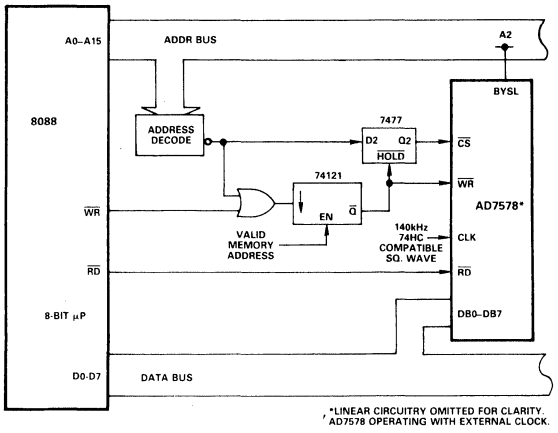


Figure 20. Interface to AD7578 Using External Clock

8088, 8086 MICROPROCESSORS

Figure 21 shows an AD7578–8088 interface.

Address line A0 of the µP is connected to BYSL of the AD7578. With the simple decoding shown in Figure 21 the AD7578 is decoded in a memory block from 4000H to 7FFFH.

A write instruction to any one of these addresses will start a conversion, i.e,

MOV 4004, AX

starts a conversion. When the conversion is finished the 8088 acquires the result by reading from the AD7578, i.e.,

MOV AX, 4000

places the conversion data in the accumulator.

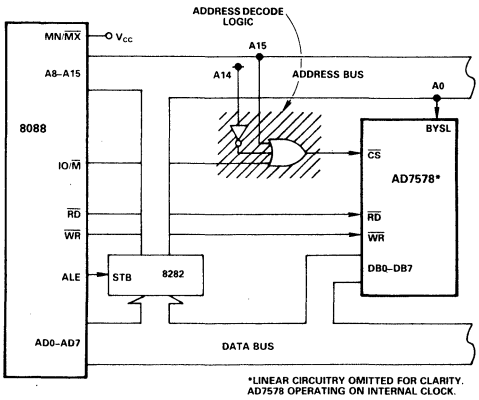


Figure 21. AD7578 – 8088 Interface

Figure 22 shows an AD7578–8086 interface. Address line A1 of the µP is connected to BYSL of the AD7578. The AD7578 is again decoded in a memory block from 4000H to 7FFFH.

A write instruction to any one of these addresses will start a conversion, i.e,

MOV 4008, AX

starts a conversion. When the conversion is finished, the 8086 acquires the result by reading from the AD7578 in two read cycles, i.e.,

MOV AL, 4000
MOV AH, 4002

places the conversion data in the accumulator.

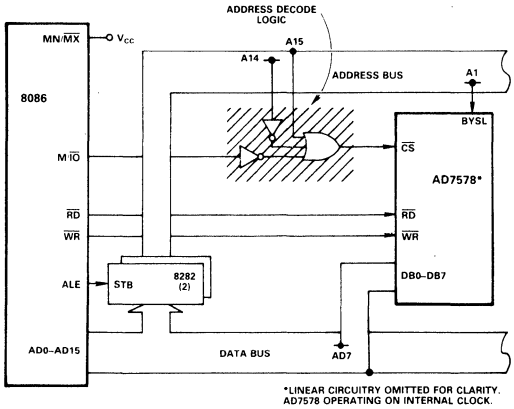


Figure 22. AD7578 – 8086 Interface

AD7578-AD585 SAMPLE-HOLD INTERFACE

Figure 23 shows an AD585 Sample-Hold Amplifier driving the analog input of the AD7578. At a sampling frequency of 8kHz the maximum input signal frequency is 4kHz. The AD7578 is configured for bipolar operation to allow an input signal swing of ±5V. No clock components are shown for the AD7578 but the conversion time should be adjusted for 100 microseconds. With an external hold capacitor of 100pF, the acquisition time for the sample-hold amplifier is 10 microseconds. The circuit operates from 0°C to +70°C.

To take a sample of the input, a WRITE instruction is executed to the AD7578 control inputs. The converter busy flag, $\overline{BUSY}$, is driven low indicating that a conversion is in progress. The falling edge of this $\overline{BUSY}$ signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7578. After 100 microseconds the conversion is finished and the $\overline{BUSY}$ signal is brought high. This allows a time of 25 microseconds for the AD585 to come out of the hold mode and acquire the input signal in time for the next sample. Between the end of one conversion and the start of the next, the conversion results must be read from the converter.

Careful circuit layout and power supply decoupling are necessary to obtain maximum performance from the system. Decoupling capacitors in the diagram are all 10μF electroytics in parallel with 0.01μF disc ceramics.

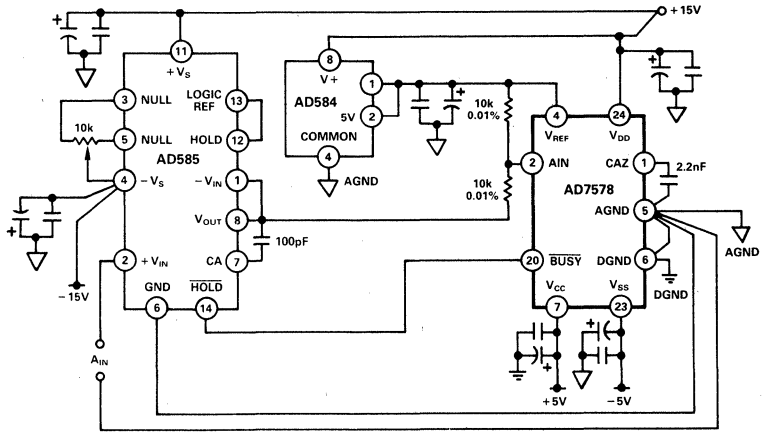


Figure 23. AD7578-AD585 Interface

ANALOG DEVICES

CMOS 12-Bit Successive Approximation ADC

AD7582

FEATURES

12-Bit Successive Approximation ADC
Four High Impedance Input Channels
Analog Input Voltage Range of 0 to +5V with Positive Reference of +5V
Conversion Time of 100μs per Channel
No Missed Codes Over Full Temperature Range
Low Total Unadjusted Error ±1LSB max
Autozero Cycle for Low Offset Voltage
Monolithic Construction

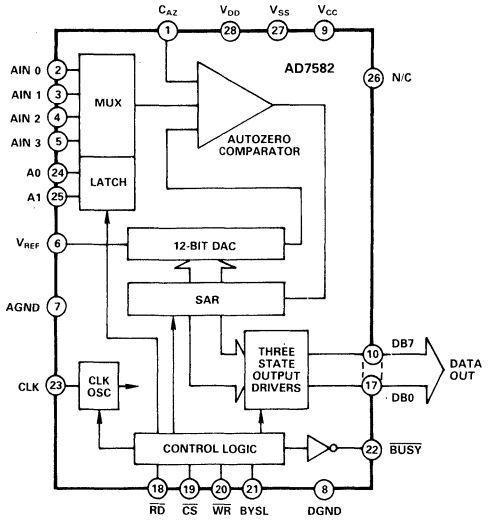
GENERAL DESCRIPTION

The AD7582 is a medium speed, 4-channel 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs per channel. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interface using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$). The 4-channel input multiplexer is controlled via address inputs A0 and A1.

Conversion results are available in two bytes, 8LSB's and 4MSB's, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V. The four analog inputs are all high impedance inputs with tight channel-to-channel matching–typically 0.1LSBs.

AD7582 FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

1. The AD7582 is a complete 4 channel 12-bit A/D converter in a 28-pin package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. The four channel input multiplexer (user addressable) features high input impedance and excellent channel-to-channel matching.
4. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.

SPECIFICATIONS

(V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5.0V f_{CLK} = 140kHz external, all specifications T_{min} to T_{max} unless otherwise noted).

Parameter	AD7582KN[1]	AD7582BD	AD7582TD	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	All channels, AIN0–AIN3
Differential Nonlinearity	±3/4	±3/4	±3/4	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Full Scale TC is typically 5ppm/°C
Offset Error	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Offset Error TC is typically 5ppm/°C
Channel to Channel Mismatch	±1/4	±1/4	±1/4	LSB max	
ANALOG INPUTS					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, On Channel Input Capacitance	8	8	8	pF typ	
I_{AIN}, Input Leakage Current					AIN0–AIN3; 0 to +5V
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 18), $\overline{CS}$ (Pin 19), $\overline{WR}$ (Pin 20)					
BYSL (Pin 21), A0 (Pin 24), A1 (Pin 25)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	μA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	μA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 23)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	μA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 10–17), $\overline{BUSY}$ (Pin 22)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200μA
Floating State Leakage Current (Pins 10–17)	±1	±1	±1	μA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	μs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	100/150	100/150	100/150	μs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	μA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES

[1]Temperature Range as follows: AD7582KN; 0 to +70°C
AD7582BD; −25°C to +85°C
AD7582TD; −55°C to +125°C

[2]Includes Full Scale Error, Offset Error and Relative Accuracy.

[3]Sample tested to ensure compliance.

[4]I_{SINK} for $\overline{BUSY}$ (pin 22) is 1.0 milliamp.

[5]Conversion Time includes autozero cycle time.

[6]Power supply current is measured when AD7582 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2 (INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2 (EXT)[2]	10	10	10	µs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	A0, A1 Valid to $\overline{WR}$ Setup Time
t_6	20	20	20	ns min	A0, A1 Valid to $\overline{WR}$ Hold Time
t_7	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_9	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{11}	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{12}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{13}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{14}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	160	180	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 20$ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10µs. See "External Clock Operation".
[3]t_{13} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{14} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

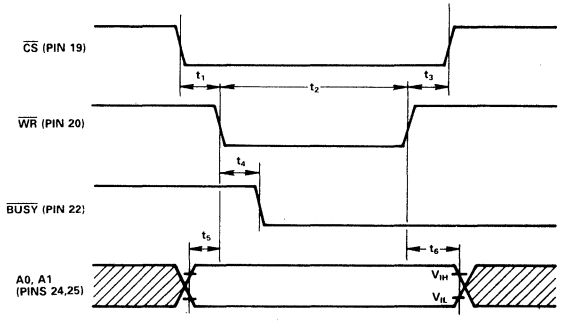


Figure 1. Start Cycle Timing

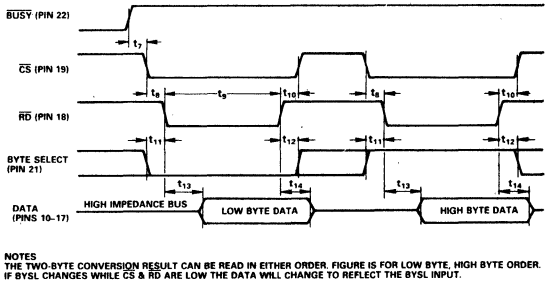
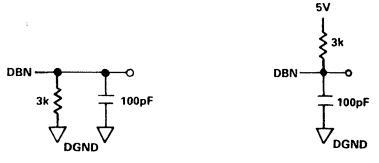
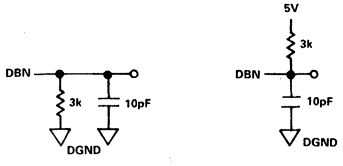


Figure 2. Read Cycle Timing



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Test (t_{13})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay Test (t_{14})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND	−0.3V, +17V
V_{SS} to DGND	+0.3V, −7V
AGND to DGND	−0.3V, V_{REF} +0.3V
V_{CC} to DGND	−0.3V, V_{DD} +0.3V
V_{REF} to AGND	−0.3V, V_{DD} +0.3V
AIN (0-3) to AGND	−0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND (Pins 18-21, 23-25)	−0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND (Pins 10-17, 22)	−0.3V, V_{DD} +0.3V
Operating Temperature Range	
KN	0 to +70°C
BD	−25°C to +85°C
TD	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Dissipation (any Package) to +75°C	1,000mW
Derate above +75°C by	10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

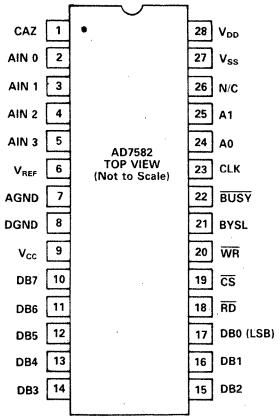
CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

Total Unadjusted Error (T_{min} to T_{max})	Temperature Range and Package: Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±1LSB	AD7582KN	AD7582BD	AD7582TD

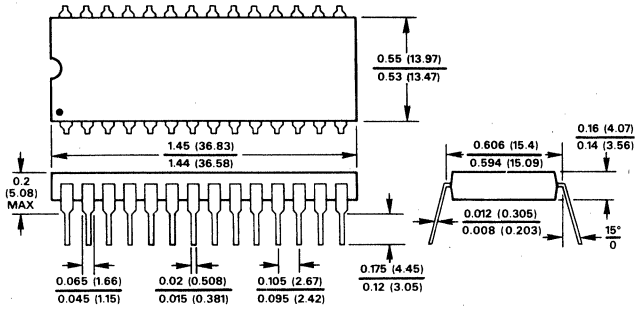
PIN CONFIGURATION



MECHANICAL INFORMATION

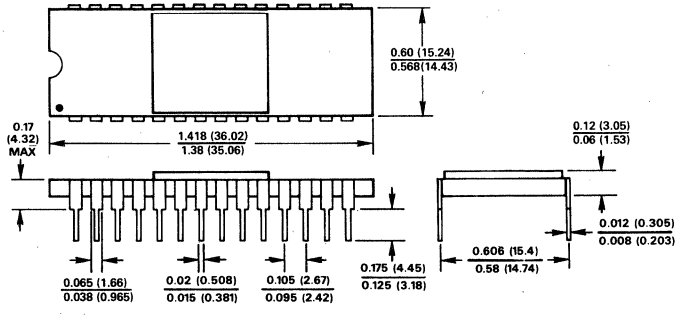
Dimensions shown in inches and (mm).

28-PIN PLASTIC DIP (SUFFIX N)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

28-PIN CERAMIC DIP (SUFFIX D)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD PLATED (50 MICROINCHES MIN) KOVAR OR ALLOY 42

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN 0	Analog Input, channel 0
3	AIN 1	Analog Input, channel 1
4	AIN 2	Analog Input, channel 2
5	AIN 3	Analog Input, channel 3
6	V_{REF}	Voltage reference input. The AD7582 is specified with $V_{REF} = +5.0V$.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
10-17		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 10	BUSY[1]	DB7
Pin 11	LOW[2]	DB6
Pin 12	LOW[2]	DB5
Pin 13	LOW[2]	DB4
Pin 14	DB11 (MSB)	DB3
Pin 15	DB10	DB2
Pin 16	DB9	DB1
Pin 17	DB8	DB0 (LSB)

[1]BUSY (Pin 10) is a converter status flag and is HIGH during a conversion.
[2]Pins 11-13 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

18	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
19	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
20	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion on a selected channel. When the AD7582 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
21	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 10-17.
22	$\overline{BUSY}$	$\overline{BUSY}$ indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
23	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
24	AO	Address Input AO. See pin 25 description.
25	A1	Address Input A1. Address inputs AO and A1 select the input channel to be converted. The address input latch is transparent when $\overline{CS}$ & $\overline{WR}$ are LOW. The address inputs are latched by $\overline{WR}$ returning HIGH.

A1	A0	CHANNEL SELECTED
0	0	AIN 0
0	1	AIN 1
1	0	AIN 2
1	1	AIN 3

26	N/C	No connect pin.
27	V_{SS}	Negative supply, −5V.
28	V_{DD}	Positive supply, +15V.

Operating Information

OPERATIONAL DIAGRAM

An operational diagram for the AD7582 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7582 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

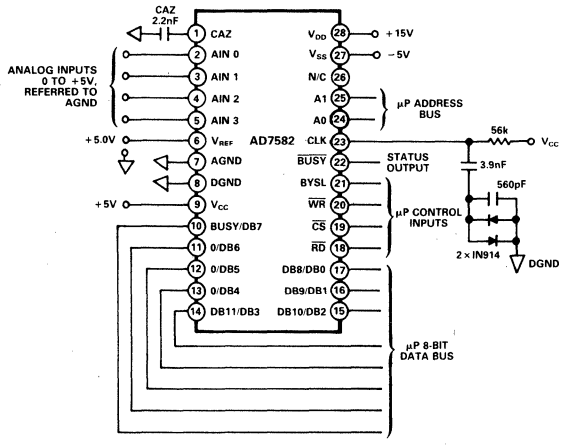


Figure 5. AD7582 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7582 operating waveforms are shown in Figure 7.

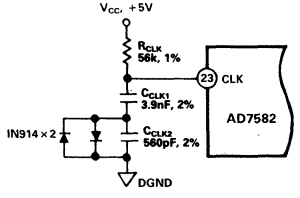


Figure 6. Circuitry Required for Internal Clock Operation

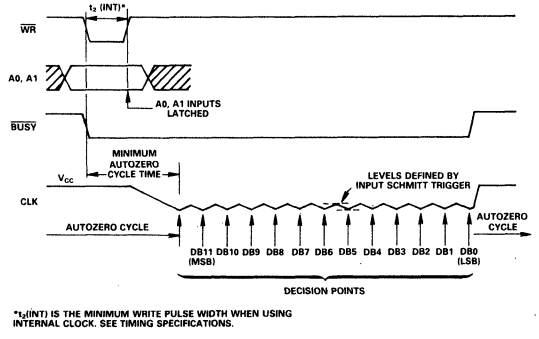


Figure 7. Operating Waveforms – Internal Clock

Between conversions ($\overline{BUSY}$ = HIGH) the AD7582 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the input multiplexer is switched to the selected channel N, via address inputs A0, A1. The autozero capacitor C_{AZ} now charges to AIN N–V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10μs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7582. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH; $\overline{WR}$ returning HIGH also latches the multiplexer address inputs A0, A1 (see Figure 7). The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The AD7582 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10μs since this is no longer provided automatically by the AD7582. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). Multiplexer address inputs A0 and A1, in addition to the $\overline{CS}$ input must now remain valid for the external $\overline{WR}$ pulse width. One approach to stretching the available μP signals is shown in the general 8-bit μP interface circuit of Figure 20. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

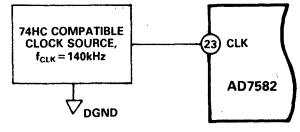


Figure 8. External Clock Operation

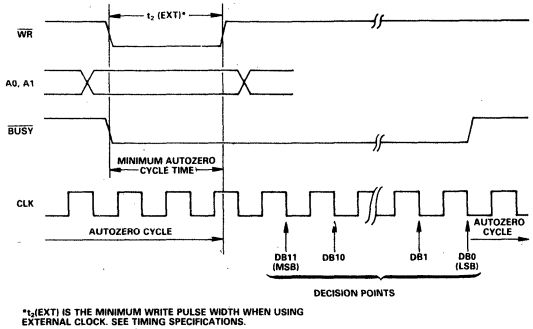


Figure 9. Operating Waveforms – External Clock

READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7582 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7582 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7582 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 10 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{\text{BUSY}}$ (pin 22) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction while conversion is in progress will restart the conversion.

COMPONENT SELECTION

1. Autozero Capacitor, C_{AZ}
   The autozero capacitor must be a low leakage, low dielectric absorption type such as polystyrene, polypropylene or teflon. To minimize noise connect the outside foil of C_{AZ} to AGND (pin 7), the analog system ground. C_{AZ} should be 2,200pF.
2. Clock Oscillator Components, R_{CLK}, C_{CLK1} and C_{CLK2}
   Clock pulses are generated by the action of series connected capacitors, C_{CLK1} and C_{CLK2} charging through an external resistor R_{CLK} and discharging through an internal switch. Nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK1}/C_{CLK2} combination is shown in Figure 10. Due to process variations, the actual operating frequency for this R_{CLK} and C_{CLK1}/C_{CLK2} combination can vary from device to device by up to 20%. For this reason, Analog Devices recommends using an external clock in the following situations:
   a. Applications requiring a conversion time which is within 20% of 100μs, the minimum conversion time for specified accuracy (a 140kHz clock frequency gives a 100μs conversion time).
   b. Applications which cannot accommodate conversion time differences which may occur due to unit clock frequency variations or temperature variations.

   It is possible to replace the fixed R_{CLK} resistor with a 50k potentiometer in series with a fixed 22kΩ resistor to allow individual adjustment of internal clock frequency in applications where 100μs conversion times are required. Reducing the value of R_{CLK} from 56k to 47k decreases the conversion time by typically 15μs.

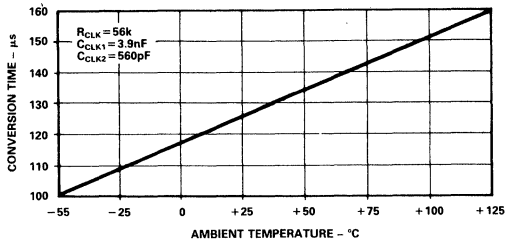


Figure 10. Typical Conversion Time vs. Temperature Using Internal Clock

Applying the AD7582

APPLYING THE AD7582

The high input impedance of the analog channels, AIN0–AIN3, allows simple analog interfacing. Zero to +5V signal sources can be connected directly to the analog input channels without additional buffering for source impedances up to 5kΩ (see Figure 11). The input/output transfer characteristic and transition points for this input signal range are shown in Figure 12 and Table I respectively. The designed transition points on the AD7582 transfer characteristic occur on integer multiples of 1LSB. The output code is Natural Binary with 1LSB = (F.S.) (1/4096) = (5/4096)V = 1.22mV.

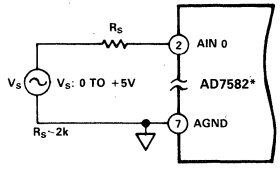


Figure 11. Unipolar 0 to +5V Operation

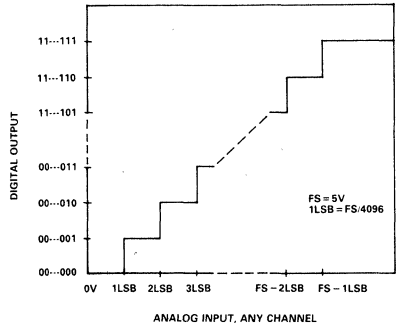


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Analog Input, Volts	Digital Output
0.00122	000 001
0.00244	000 010
2.49878	011 111
2.50000	100 000
2.50122	100 001
4.99756	111 110
4.99878	111 111

Table I. Transition Points for Unipolar 0 to +5V Operation

Signal ranges other than 0 to +5V are easily accommodated by using resistor divider networks to produce 0 to +5V signal ranges at the AD7582 input pins. Figure 13 shows a divider network on channel 0 to allow an AIN 0 signal range of 0 to +10V. The input resistors must be selected to match within 0.01% and should be the same type and from the same manufacturer so that their temperature coefficients match. Note that since the source impedance has not been included in the resistor divider ratio, it must now be as low as possible. For Figure 13 with a source impedance of 0.5Ω the maximum error across the network is approximately 0.5LSB. The LSB size is (F.S.)(1/4096) = (10/4096)V = 2.44mV.

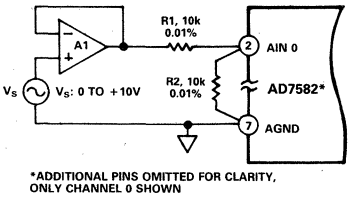


Figure 13. Unipolar 0 to +10V Operation

Bipolar signal ranges of −5V to +5V are accommodated by referencing the resistor divider network to V_{REF} as shown in Figure 14 for channel 0. With the resistor values shown, the signal source must be capable of sinking 0.5mA. The input/output transfer characteristic and transition points for this ±5V signal range are shown in Figure 15 and Table II respectively. The output code is Offset Binary with an LSB size of (F.S.)(1/4096) = (10/4096)V = 2.44mV.

With an analog input (V_S) of −1.22mV, the input offset voltage of A1 should be adjusted until the ADC output flickers between 0111 1111 1111 and 1000 0000 0000. Alternatively the −1/2LSB signal offset can be included in the signal conditioning electronics.

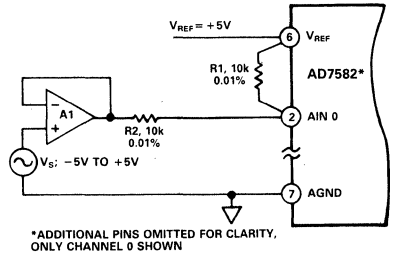


Figure 14. Bipolar −5V to +5V Operation

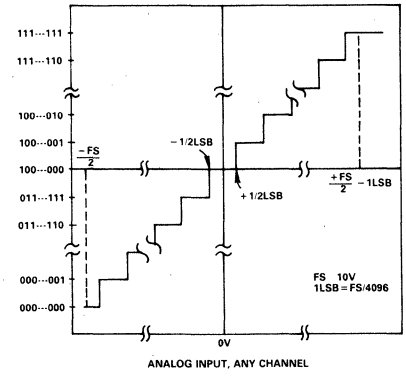


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

Analog Input, Volts	Digital Output
−4.99878	000 001
−4.99634	000 010
−0.00122	100 000
+0.00122	100 001
+4.99389	111 110
+4.99634	111 111

Table II. Transition Points for Bipolar −5V to +5V Operation

Applications

Power Supply Decoupling: All power supplies to the AD7582 should be bypassed with either 10μF tantulum or electrolytic capacitors. To ensure good high frequency performance, each capacitor should be bypassed with an 0.01μF disc ceramic capacitor. All capacitors should be placed as close as possible to the AD7582.

Reference Circuit: Figure 16 shows how to configure an AD584LH to produce a reference voltage of 5.00V. R2 provides a typical adjustment range of ±75mV. The AD584LH will contribute less than 1LSB of gain error over the commercial temperature range.

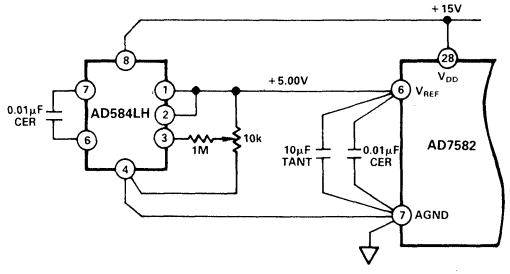


Figure 16. AD584LH as Reference Generator

Transient currents flow at the V_{REF} input during a conversion. To avoid dynamic errors place a 10μF smoothing capacitor, either tantalum or electrolytic, in parallel with a 0.01μF disc ceramic from the V_{REF} pin to AGND.

Proper Layout: Layout for a printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or close to the autozero capacitor. The analog inputs, the reference input and the autozero input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established at pin 7 (AGND) or as close as possible to the AD7582. This single point analog ground should be connected to the digital system ground, to which pin 8 (DGND) is connected, at one point only and as close to the AD7582 as possible. The autozero capacitor, bypass capacitors for the reference input and the analog supplies, AIN commons and any input signal screening should be returned to the analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN 0-3 and signal return leads from AGND (pin 7) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7582 data outputs are connected to a continuously busy (and noisy) microprocessor bus it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor bus to the autozero comparator. The problem exists only for ceramic package versions of the AD7582, the electrically isolated metal lid acting like a conductor to distribute the digital noise around the package.

Grounding the lid to DGND eliminates this problem. Alternatively the AD7582 can be isolated from the microprocessor bus by means of three-state buffers.

Microprocessor Interfacing

MICROPROCESSOR INTERFACING

When the AD7582 is used with its own internal clock oscillator, microprocessor interfacing is straightforward and requires at most a few external gates (see Figures 17 through 19, 21 and 22). When the AD7582 is used with an external clock source, additional circuitry is required to extend the μP control signals (see Figure 20).

MC6800, MC6809 and 6502 MICROPROCESSORS

A typical interface to the AD7582 with any of the above microprocessors is shown in Figure 17. The decoder can be enabled high using VMA in 6800 systems or enabled low by NOR'ing ϕ_0 and ϕ_2 in 6502 systems or by NOR'ing E and Q in 6809 systems. Address lines A0, A1, and A2 of the 6800 have been tied to A0, A1 and BYSL respectively of the AD7582. Assuming the AD7582 is assigned a memory block starting at address 8000H, the input multiplexer is addressed as follows:

8000H	Channel 0
8001H	Channel 1
8002H	Channel 2
8003H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel. To read the conversion results, it is necessary only to bring control inputs $\overline{CS}$ and $\overline{RD}$ low. The BYSL input (tied to A2 of the μP) determines whether the data high or low byte is placed onto the 8-bit data bus. A read instruction to any one of the previous channel addresses will result in the low byte of data being transferred to the μP (BYSL = Low). Similarly a read instruction to any address having A2 HIGH and within the assigned memory block, e.g., 8004H, transfers the high byte of data to the μP. The converter status flag BUSY can be polled at intervals to check whether the present conversion has finished and valid 12-bit data is available. This is accomplished by the following instructions on the 6800:

```
LDA  A  $8004    Load Flag from AD7582
ASL  A           Shift Flag into Carry
BCC      FETCH   Branch to Data Fetch
                 Subroutine if BUSY is LOW
```

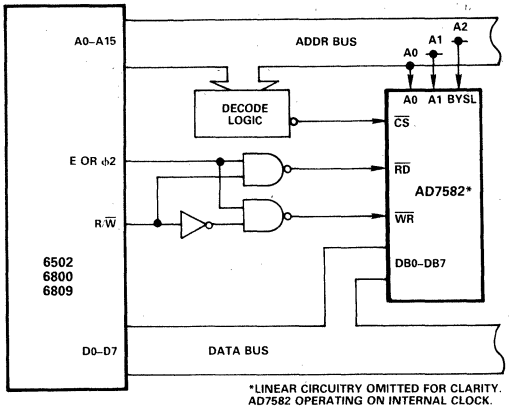


Figure 17. AD7582 – MC6800, 6809, 6502 Interface

8085A, Z80 MICROPROCESSORS

A typical interface to either of these microprocessors is shown in Figure 18. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. This interface uses slightly different low-level address decoding than the previous interface. Address lines A0, A1 & A2 of the μP have been tied to BYSL, A0 & A1 respectively of the AD7582. This allows the 16-bit data move instructions on both the 8085A and the Z80 to be used when reading conversion results. Assuming the AD7582 is again assigned a memory block starting at address 8000H the input multiplexer is now addressed as follows:

8000H	Channel 0
8002H	Channel 1
8004H	Channel 2
8006H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel. The 12-bit conversion results can be read (low byte first then high byte) by a single read instruction;

On the 8085A

LHLD 8000

moves the conversion results into register pair HL

On the Z80

LD BC, (8000)

moves the conversion results into register pair BC

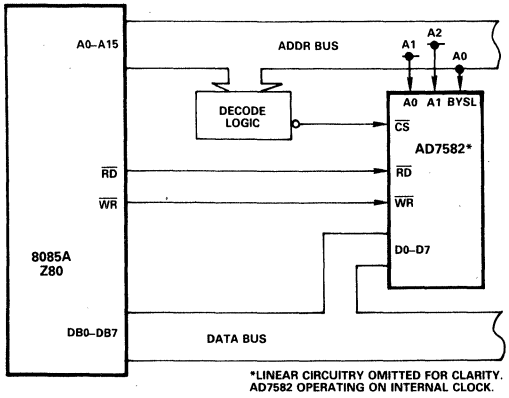


Figure 18. AD7582 – 8085A, Z80 Interface

MC68000, MC68008 MICROPROCESSOR

Figure 19 shows an AD7582–MC68000/MC68008 interface.

Address lines A1, A2 and A3 of the μP are connected to BYSL, A0 & A1 inputs respectively of the AD7582.

With the simple decoding logic shown in Figure 19, the AD7582 is decoded in a memory block from C000H to FFFFH. The input multiplexer is now addressed as follows:

C000H	Channel 0
C004H	Channel 1
C008H	Channel 2
C00CH	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e.,

MOVE. W D0 $C004

starts a conversion of channel 1. When the conversion is complete, the μP acquires the result by reading from the AD7582, i.e,

MOVEP. W $000 (A2), D0

This instruction places the conversion data in the D0 register of the μP. Address register A2 should contain an odd-order address for the AD7582, e.g., $C003.

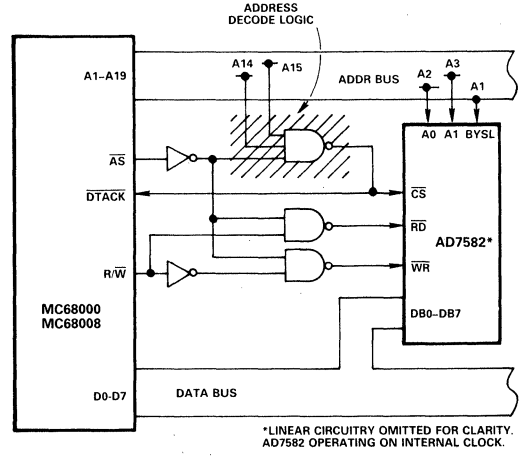


Figure 19. AD7582 – MC68000/MC68008 Interface

MICROPROCESSOR INTERFACE TO AD7582 WITH EXTERNAL CLOCK

Figure 20 shows the additional circuitry generally required to interface an 8-bit μP to the AD7582 operating from an external clock source. During a write operation, the 74121 monostable (one-shot) is triggered to latch the data (A0, A1 and $\overline{CS}$) in the 7477, a 4-bit bistable latch. The monostable timing components (not shown in Figure 20) should be chosen to provide an output pulse width corresponding to t_2 (EXT), the minimum autozero cycle time. To avoid any possibility of spurious triggering, the monostable should be enabled by a valid memory address signal. During a data read cycle, the 7477 latch is transparent and data is read normally. Note that the μP write and read cycle times are unaffected by the interface circuitry.

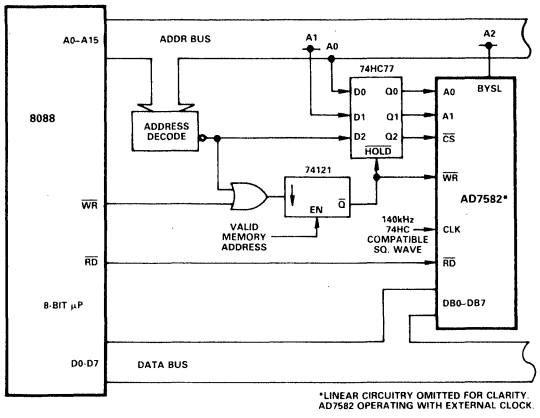


Figure 20. Interface to AD7582 Using External Clock

8088, 8086 MICROPROCESSORS

Figure 21 shows an AD7582–8088 interface.

Address lines A0, A1 and A2 are connected to BYSL, A0 and A1 inputs respectively of the AD7582. With the simple decoding shown in Figure 21 the AD7582 is decoded in a memory block from 4000H to 7FFFH. The input multiplexer is now addressed as follows:

4000H	Channel 0
4002H	Channel 1
4004H	Channel 2
4006H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e,

MOV 4004, AX

starts a conversion of channel 2. When the conversion is finished the 8088 acquires the result by reading from the AD7582, i.e.,

MOV AX, 4000

places the conversion data in the accumulator.

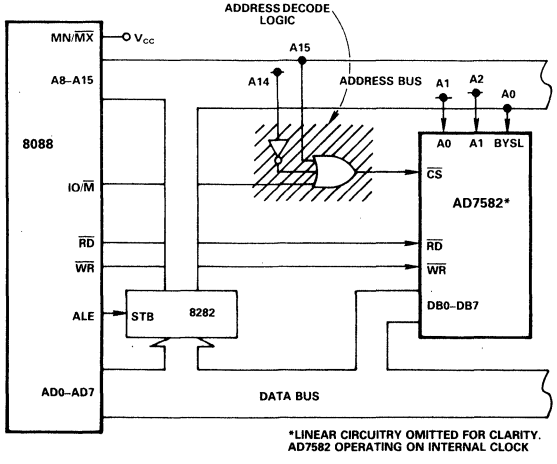


Figure 21. AD7582 – 8088 Interface

Figure 22 shows an AD7582–8086 interface. Address lines A1, A2 and A3 are connected to BYSL, A0 and A1 inputs respectively of the AD7582. The AD7582 is again decoded in a memory block from 4000H to 7FFFH. The input multiplexer is now addressed as follows:

4000H	Channel 0
4004H	Channel 1
4008H	Channel 2
400CH	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e,

MOV 4008, AX

starts a conversion of channel 2. When the conversion is finished, the 8086 acquires the result by reading from the AD7582 in two read cycles, i.e.,

MOV AL, 4000
MOV AH, 4002

places the conversion data in the accumulator.

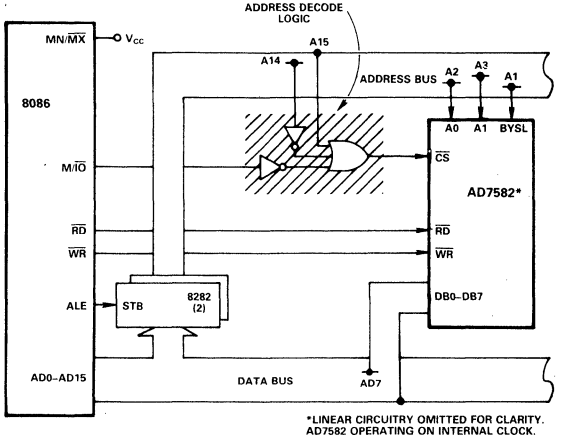


Figure 22. AD7582 – 8086 Interface

AD7582-AD585 SAMPLE-HOLD INTERFACE

Figure 23 shows an AD585 Sample-Hold Amplifier driving A_{IN1} of the AD7582. At a sampling frequency of 8kHz the maximum input signal frequency is 4kHz. The AD7582 is configured for bipolar operation to allow an input signal swing of ±5V. No clock components are shown for the AD7582 but the conversion time of the AD7582 should be adjusted for 100 microseconds. With an external hold capacitor of 100pF, the acquisition time for the sample-hold amplifier is 10 microseconds. The circuit operates from 0°C to +70°C.

To take a sample of the input, a WRITE instruction is executed to the AD7582 control inputs. The converter busy flag, $\overline{BUSY}$, is driven low indicating that a conversion is in progress. The falling edge of this $\overline{BUSY}$ signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7582. After 100 microseconds the conversion is finished and the $\overline{BUSY}$ signal is brought high. This allows a time of 25 microseconds for the AD585 to come out of the hold mode and acquire the input signal in time for the next sample. Between the end of one conversion and the start of the next, the conversion results must be read from the converter.

Careful circuit layout and power supply decoupling are necessary to obtain maximum performance from the system. Decoupling capacitors in the diagram are all 10μF electroytics in parallel with 0.01μF disc ceramics.

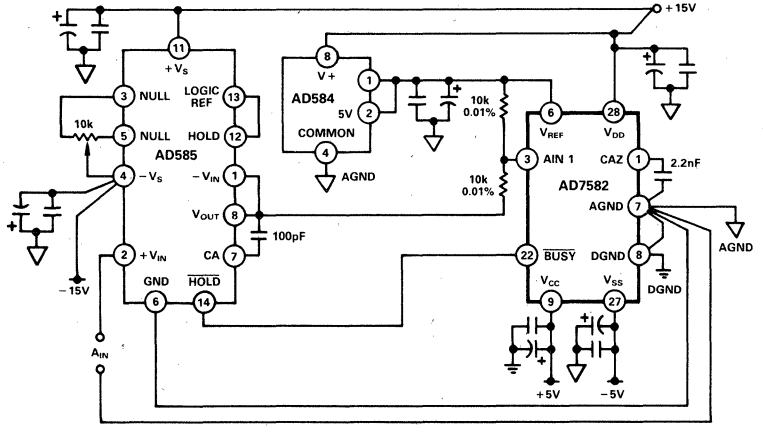


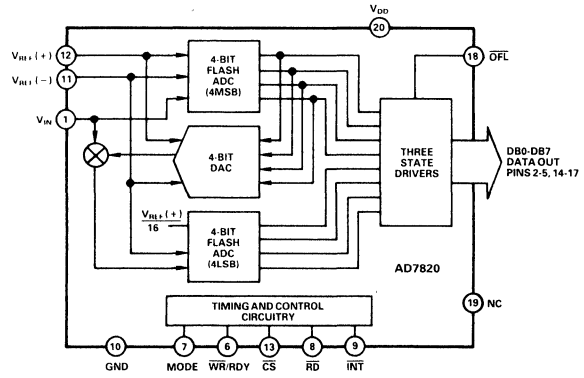
Figure 23. AD7582-AD585 Interface

LC² MOS High Speed µP Compatible 8-Bit ADC with Track/Hold Function

AD7820

FEATURES
Fast Conversion Time: 1.36µs Max
Built-In Track-and-Hold Function
No Missed Codes
No User Trims Required
Single +5V Supply
Ratiometric Operation
No External Clock
0.3" Wide, 20-Pin DIP

AD7820 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD7820 is a high speed, microprocessor compatible 8-bit analog-to-digital converter which uses a half-flash conversion technique to achieve a conversion time of 1.36µs. The converter has a 0V to +5V analog input voltage range with a single +5V supply.

The half-flash technique consists of 31 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC. The input to the AD7820 is tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold for signals with slew rates less than 100 mV/µs.

The part is designed for ease of microprocessor interface with the AD7820 appearing as a memory location or I/O port without the need for external interfacing logic. All digital outputs use latched, three-state output buffer circuitry to allow direct connection to a microprocessor data bus or system input port. A non-three state overflow output is also provided to allow cascading of devices to give higher resolution.

The AD7820 is fabricated in an advanced, all ion-implanted, high speed, Linear Compatible CMOS (LC^2MOS) process and features a low maximum power dissipation of 75mW. It is packaged in a 0.3"wide, 20-pin DIP.

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The half-flash conversion technique, coupled with fabrication on Analog Devices' LC^2MOS process, enables very fast conversion times. The maximum conversion time for the WR-RD mode is 1.36µs, with 1.6µs the maximum for the RD mode.
2. Total Unadjusted Error
   The AD7820 features an excellent total unadjusted error figure of less than ½ LSB over the full operating temperature range. The part is also guaranteed to have no missing codes over the entire temperature range.
3. Built-In Track-and-Hold
   The analog input circuitry uses sampled-data comparators, which by nature have a built-in track-and-hold function. As a result, input signals with slew rates up to 100mV/µs can be converted to 8-bits without external sample-and-hold. This corresponds to a 5V peak-to-peak, 7kHz sine wave signal.
4. Single Supply
   Operation from a single +5V supply with a positive voltage reference allows operation of the AD7820 in microprocessor systems without any additional power supplies.

SPECIFICATIONS (V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(−) = GND = 0V unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for RD Mode (Pin 7 = 0V)

Parameter	AD7820KN[1]	AD7820LN	AD7820BQ AD7820TQ	AD7820CQ AD7820UQ	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB	
Minimum Resolution for which						
No Missing Codes are guaranteed	8	8	8	8	Bits	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF}(+) Input Voltage Range	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V_{REF}(−)/V_{DD}	V min/V max	
V_{REF}(−) Input Voltage Range	GND/V_{REF}(+)	GND/V_{REF}(+)	GND/V_{REF}(+)	GND/V_{REF}(+)	V min/V max	
ANALOG INPUT						
Input Voltage Range	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V_{REF}(−)/V_{REF}(+)	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	
Input Capacitance[3]	45	45	45	45	pF typ	
LOGIC INPUTS						
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH} ($\overline{CS}$, $\overline{RD}$)	1	1	1	1	μA max	
I_{INH} ($\overline{WR}$)	3	3	3	3	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
MODE						
V_{INH}	3.5	3.5	3.5	3.5	V min	
V_{INL}	1.5	1.5	1.5	1.5	V max	
I_{INH}	200	200	200	200	μA max	50 μA typ
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7, $\overline{OFL}$, $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0–DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.2	0.2	0.2	0.2	V/μs typ	
	0.1	0.1	0.1	0.1	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[4]	15	15	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 0V
Power Dissipation	40	40	40	40	mW typ	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

NOTES

[1]Temperature Ranges are as follows:

AD7820 KN, LN	0 to +70°C
AD7820 BQ, CQ	−25°C to +85°C
AD7820 TQ, UQ	−55°C to +125°C

[2]Total Unadjusted Error includes offset, full-scale and linearity errors.

[3]Sample tested at 25°C by Product Assurance to ensure compliance.

[4]See Typical Performance Characteristics.

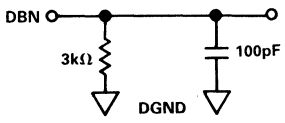
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(−) = GND = 0V unless otherwise stated)

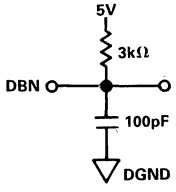
Parameter	Limit at 25°C (All grades)	Limit at T_{min}, T_{max} (K,L,B,C grades)	Limit at T_{min}, T_{max} (T,U grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Setup Time
t_{CSH}	0	0	0	ns min	$\overline{CS}$ TO $\overline{RD}$/$\overline{WR}$ Hold Time
t_{RDY}[2]	70	90	100	ns max	$\overline{CS}$ to $\overline{RDY}$ Delay. Pull-Up Resistor 2kΩ.
t_{CRD}	1.6	2.0	2.5	µs max	Conversion Time (RD Mode)
t_{ACC0}[3]	t_{CRD} + 20	t_{CRD} + 35	t_{CRD} + 50	ns max	Data Access Time (RD Mode)
t_{INTH}[2]	125	–	–	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)
	175	225	225	ns max	
t_{DH}[4]	60	80	100	ns max	Data Hold Time
t_P	500	600	600	ns min	Delay Time between Conversions
t_{WR}	600	600	600	ns min	Write Pulse Width
	50	50	50	µs max	
t_{RD}	600	700	700	ns min	Delay Time between $\overline{WR}$ and $\overline{RD}$ Pulses
t_{ACC1}[3]	160	225	250	ns max	Data Access Time (WR–RD Mode, see Fig. 5b)
t_{RI}	140	200	225	ns max	$\overline{RD}$ to $\overline{INT}$ Delay
t_{INTL}[2]	700	–	–	ns typ	$\overline{WR}$ to $\overline{INT}$ Delay
	1000	1400	1700	ns max	
t_{ACC2}[3]	70	90	110	ns max	Data Access Time (WR–RD Mode, see Fig. 5a)
t_{IHWR}[2]	100	130	150	ns max	$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone Operation)
t_{ID}	50	65	75	ns max	Data Access Time after $\overline{INT}$ (Stand-Alone Operation)

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

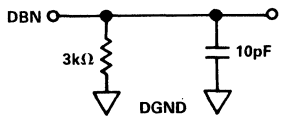


a. High-Z to V_{OH}

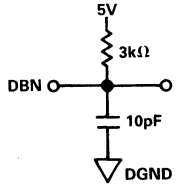


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

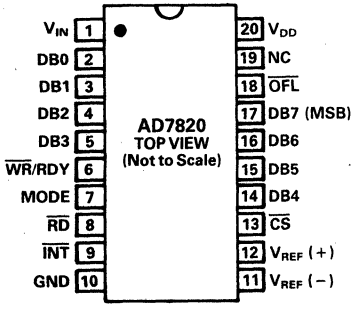
V_{DD} to GND	0V, +7V
Digital Input Voltage to GND (Pins 6-8, 13)	−0.3V, V_{DD}
Digital Output Voltage to GND (Pins 2-5, 9, 14-18)	−0.3V, V_{DD}
V_{REF} (+) to GND	V_{REF} (−), V_{DD}
V_{REF} (−) to GND	0V, V_{REF} (+)
V_{IN} to GND	−0.3V, V_{DD}
Operating Temperature Range	
KN, LN	0 to +70°C
BQ, CQ	−25°C to +85°C
TQ, UQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



ORDERING INFORMATION

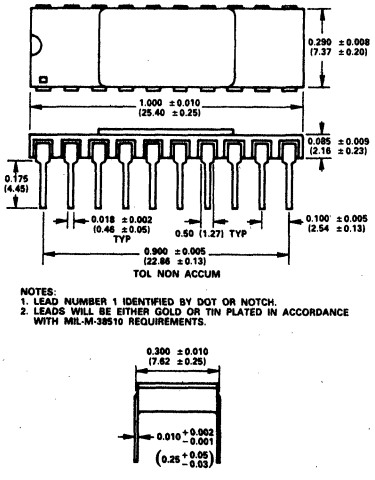
Total Unadjusted Error	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[1] −25°C to +85°C	Cerdip[1] −55°C to +125°C
±1/2LSB	AD7820LN	AD7820CQ	AD7820UQ
±1LSB	AD7820KN	AD7820BQ	AD7820TQ

NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

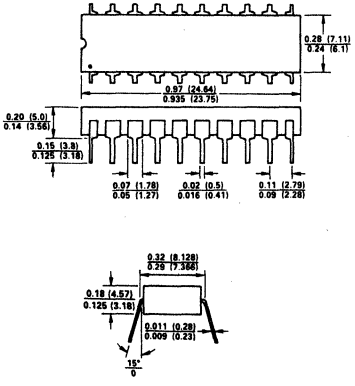
MECHANICAL INFORMATION
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

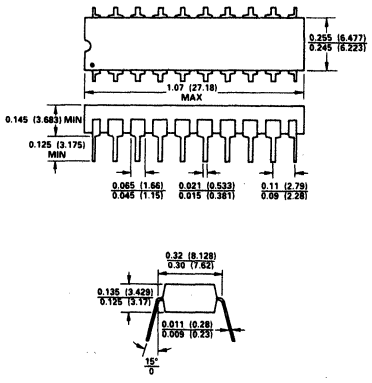
20-PIN CERAMIC[1]



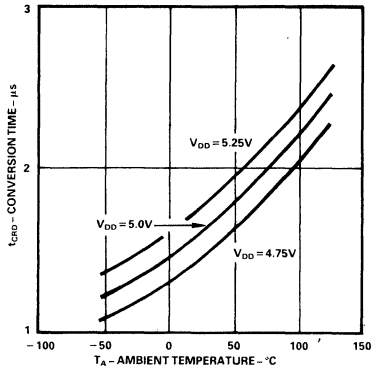
20-PIN CERDIP (SUFFIX Q)



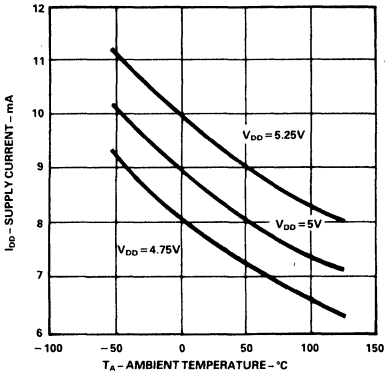
20-PIN PLASTIC DIP (SUFFIX N)



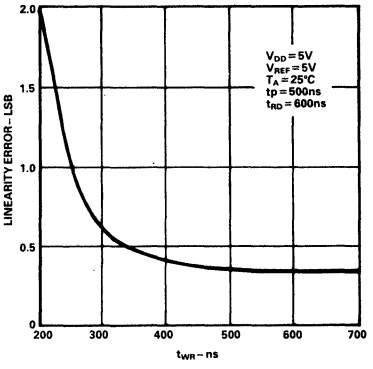
NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.



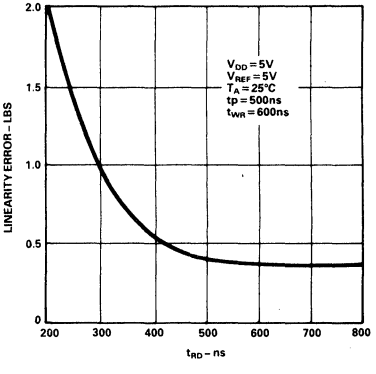
Conversion Time (RD Mode) vs. Temperature



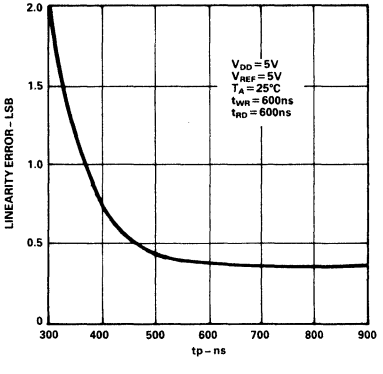
Power Supply Current vs. Temperature (not including reference ladder)



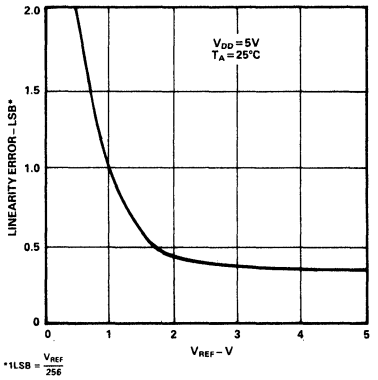
Accuracy vs. t_{WR}



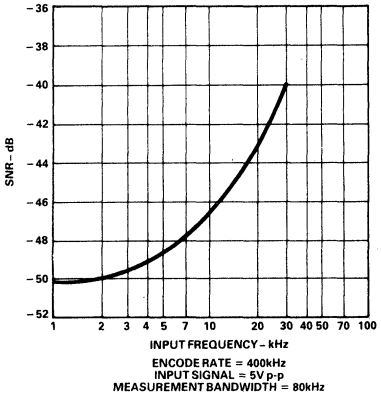
Accuracy vs. t_{RD}



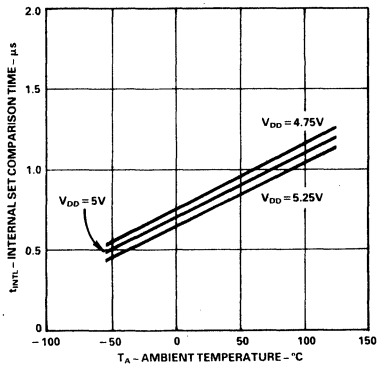
Accuracy vs. tp



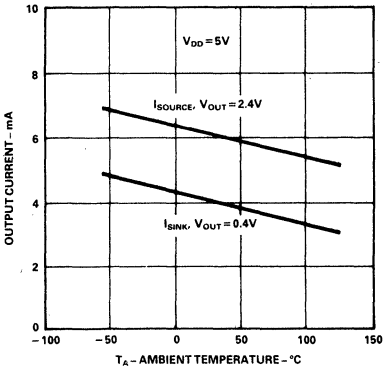
Accuracy vs V_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]



Signal-Noise Ratio vs. Input Frequency



t_{INTL}, Internal Time Delay vs. Temperature



Output Current vs. Temperature

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{IN}	Analog Input. Range: $V_{REF}(-)$ to $V_{REF}(+)$.
2	DB0	Data Output. Three State Output, bit 0 (LSB)
3	DB1	Data Output. Three State Output, bit 1
4	DB2	Data Output. Three State Output, bit 2
5	DB3	Data Output. Three State Output, bit 3
6	$\overline{WR}$/RDY	WRITE control input/READY status output. See Digital Interface section.
7	Mode	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50μA current source. See Digital Interface section.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT Output. $\overline{INT}$ going low indicates that the conversion is complete. $\overline{INT}$ returns high on the rising edge of $\overline{RD}$ or $\overline{CS}$. See Digital Interface section.
10	GND	Ground
11	$V_{REF}(-)$	Lower limit of reference span. Range: $GND \leq V_{REF}(-) \leq V_{REF}(+)$
12	$V_{REF}(+)$	Upper limit of reference span. Range: $V_{REF}(-) \leq V_{REF}(+) \leq V_{DD}$
13	$\overline{CS}$	Chip Select Input. $\overline{CS}$, the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	Data Output. Three State Output, bit 4
15	DB5	Data Output. Three State Output, bit 5
16	DB6	Data Output. Three State Output, bit 6
17	DB7	Data Output. Three State Output, bit 7 (MSB)
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF}(+) - 1/2$LSB), $\overline{OFL}$ will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution.
19	NC	No connection.
20	V_{DD}	Power supply voltage, + 5V

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7820 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4 MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data. The MS flash ADC also has one additional comparator to detect input overrange.

OPERATING SEQUENCE

The operating sequence for the AD7820 in the WR-RD mode is shown in Figure 3. A set-up time of 500ns is required prior to the falling edge of $\overline{WR}$. (This 500ns is required between reading data from the AD7820 and starting another conversion). When $\overline{WR}$ is low the input comparators track the analog input signal, V_{IN}. On the rising edge of $\overline{WR}$, the input signal is sampled and the result for the four most significant bits is latched. $\overline{INT}$ goes low approximately 700ns after the rising edge of $\overline{WR}$. This indicates that conversion is complete and the data result is already in the output latch. $\overline{RD}$ going low then accesses the output data. If a faster conversion time is required, the $\overline{RD}$ line can be brought low 600ns after $\overline{WR}$ goes high. This latches the lower 4 bits of data and accesses the output data on DB0–DB7.

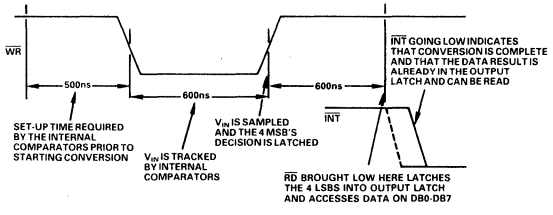


Figure 3. Operating Sequence (WR-RD Mode)

DIGITAL INTERFACE

The AD7820 has two basic interface modes which are determined by the status of the MODE pin. When this pin is low the converter is in the RD mode, with this pin high the AD7820 is set up for the WR-RD mode.

RD Mode

The timing diagram for the RD mode is shown in Figure 4. In the RD mode configuration, conversion is initiated by taking $\overline{RD}$ low. The $\overline{RD}$ line is then kept low until output data appears. It is very useful with microprocessors which can be forced into a WAIT state, with the microprocessor starting a conversion, waiting, and then reading data with a single READ instruction. In this mode, pin 6 of the AD7820 is configured as a status output, RDY. This RDY output can be used to drive the processor READY or WAIT input. It is an open drain output (no internal pull-up device) which goes low after the falling edge of $\overline{CS}$ and goes high impedance at the end of conversion. An $\overline{INT}$ line is also provided which goes low at the completion of conversion. $\overline{INT}$ returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

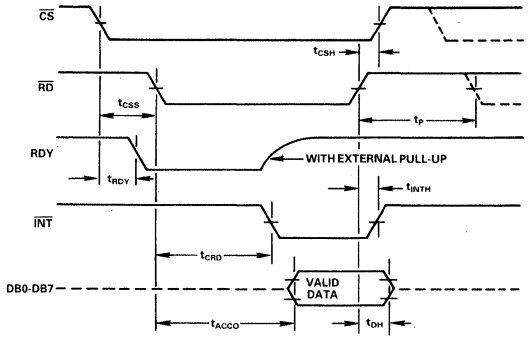


Figure 4. RD Mode

WR–RD Mode

In the WR–RD mode, pin 6 is configured as the WRITE input for the AD7820. With $\overline{CS}$ low, conversion is initiated on the falling edge of $\overline{WR}$. Two options exist for reading data from the converter.

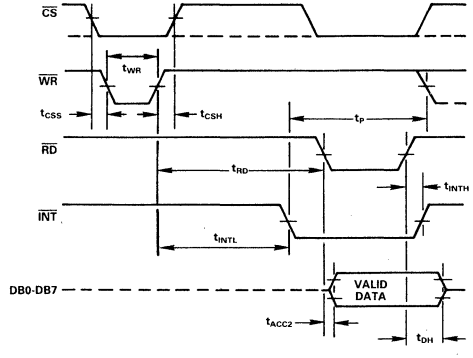


Figure 5a. WR-RD Mode ($t_{RD}>t_{INTL}$)

In the first of these options the processor waits for the $\overline{INT}$ status line to go low before reading the data (see Figure 5a). $\overline{INT}$ typically goes low 700ns after the rising edge of $\overline{WR}$. It indicates that conversion is complete and that the data result is in the output latch. With $\overline{CS}$ low, the data outputs (DB0-DB7) are activated when $\overline{RD}$ goes low. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$.

The alternative option can be used to shorten the conversion time. To achieve this, the status of the $\overline{INT}$ line is ignored and $\overline{RD}$ can be brought low 600ns after the rising edge of $\overline{WR}$. In this case $\overline{RD}$ going low transfers the data result into the output latch and activates the data outputs (DB0-DB7). $\overline{INT}$ also goes low on the falling edge of $\overline{RD}$ and is reset on the rising edge of $\overline{RD}$ or $\overline{CS}$. The timing for this interface is shown in Figure 5b.

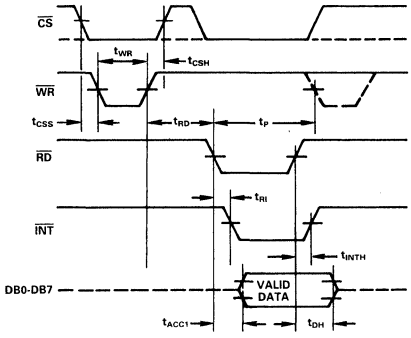


Figure 5b. WR-RD Mode ($t_{RD}<t_{INTL}$)

The AD7820 can also be used in stand-alone operation in the WR-RD mode. $\overline{CS}$ and $\overline{RD}$ are tied low and a conversion is initiated by bringing $\overline{WR}$ low. Output data is valid approximately 600ns after the rising edge of $\overline{WR}$. The timing diagram for this mode is shown in Figure 6.

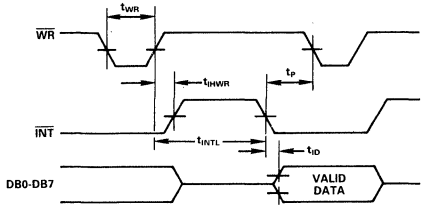


Figure 6. WR-RD Mode Stand-Alone Operation, $\overline{CS}=\overline{RD}=0$

APPLYING THE AD7820

REFERENCE AND INPUT

The two reference inputs on the AD7820 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input can easily be varied since this range is equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing the reference span, $V_{REF}(+)-V_{REF}(-)$, to less than 5V the sensivity of the converter can be increased (i.e., if $V_{REF} = 2V$ then 1LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Therefore, although V_{IN} is not itself differential, it will have nearly differential-input capability in most measurement applications because of the reference design. Figure 7 shows some of the configurations that are possible.

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7820, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7820 is shown in Figure 8a. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, and V_{IN} is connected to the most significant and least significant comparators. Therefore, V_{IN} is connected to thirty one 1pF input capacitors at the same time.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 2kΩ to 5kΩ). In addition, about 12pF of input stray capacitance must be charged. For large source resistances, the analog input can be modelled as an RC network as shown in Figure 8b. As R_S increases, it takes longer for the input capacitance to charge.

In the RD mode, the time for which the input comparators track the analog input is 600ns at the start of conversion. In the WR-RD mode the input comparators track V_{IN} for the duration of the $\overline{WR}$ pulse. Since other factors cause this time to be at least 600ns, input time constants of 100ns can be accommodated without special consideration. Typical total input capacitance values of 45pF allow R_S to be 1.5kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

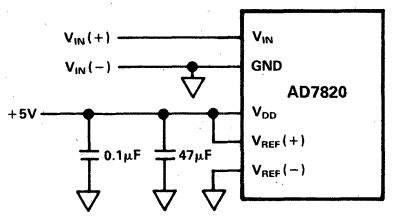


Figure 7a. Power Supply as Reference

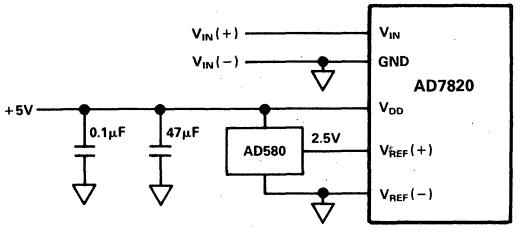


Figure 7b. External Reference 2.5V Full-Scale

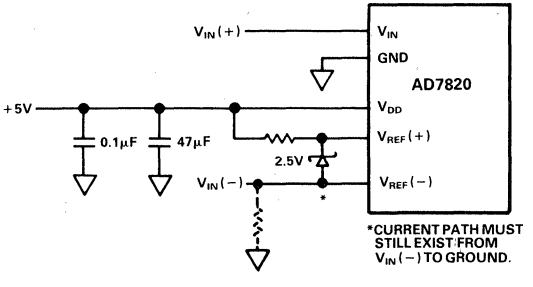


Figure 7c. Input Not Referenced to GND

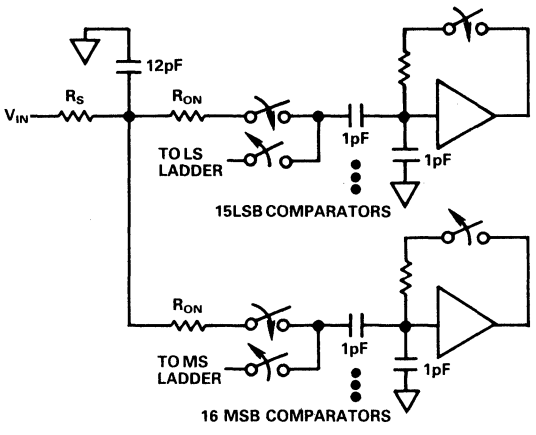


Figure 8a. AD7820 Equivalent Input Circuit

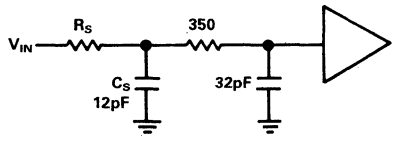


Figure 8b. RC Network Model

INPUT FILTERING

It should be made clear that transients on the analog input signal, caused by charging current flowing into V_{IN} will not normally degrade the ADC's performance. In effect, the AD7820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients with an external capacitor at the V_{IN} terminal.

INHERENT SAMPLE-HOLD

A major benefit of the AD7820's input structure is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least ½LSB throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7820 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for the AD7820 is 1.36µs, the time through which V_{IN} must be ½LSB stable is much smaller. The AD7820 "samples" V_{IN} only when $\overline{WR}$ is low. The value of V_{IN} approximately 100ns (internal propogation delay) after the rising edge of $\overline{WR}$ is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

Input signals with slew rates typically below 200mV/µs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the AD7820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1µs would still not be able to measure a 5V, 1kHz sine wave without the aid of an external sample-and-hold. The AD7820 with no such help, can typically measure 5V, 10kHz waveforms.

Applications

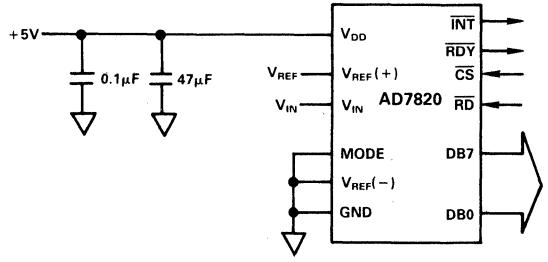


Figure 9a. 8-Bit Resolution

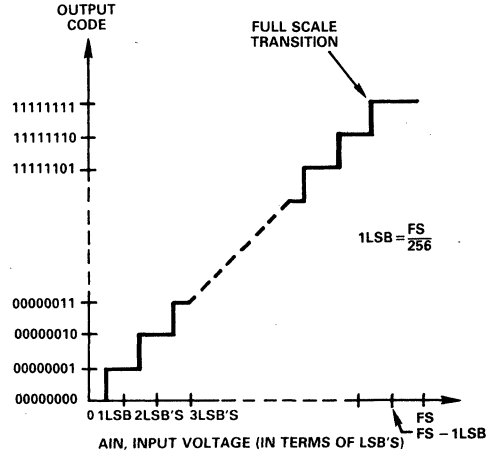


Figure 9b. Nominal Transfer Characteristic for 8-Bit Resolution Circuit

Applications

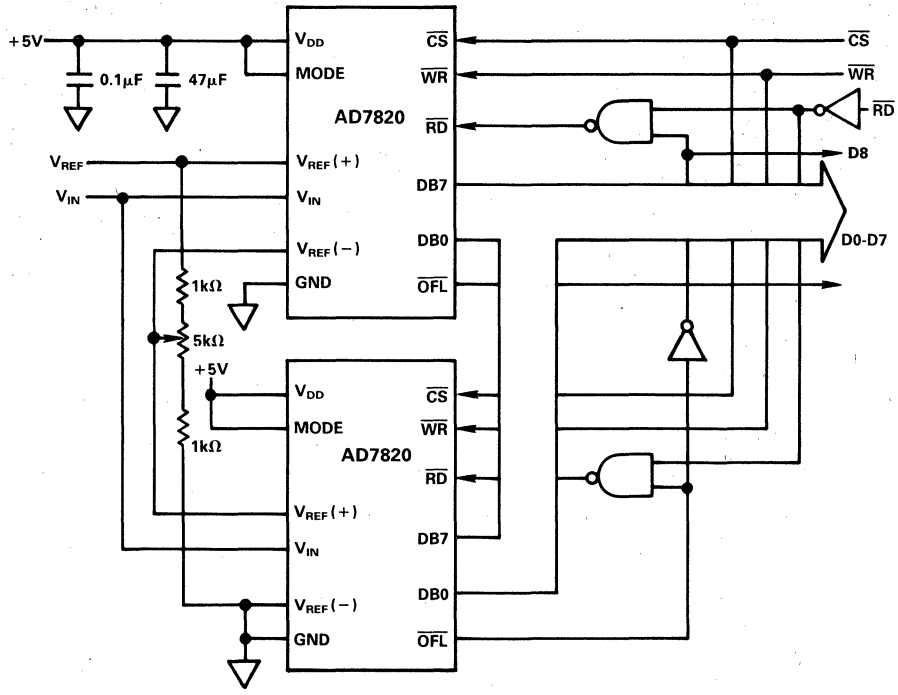


Figure 10. 9-Bit Resolution

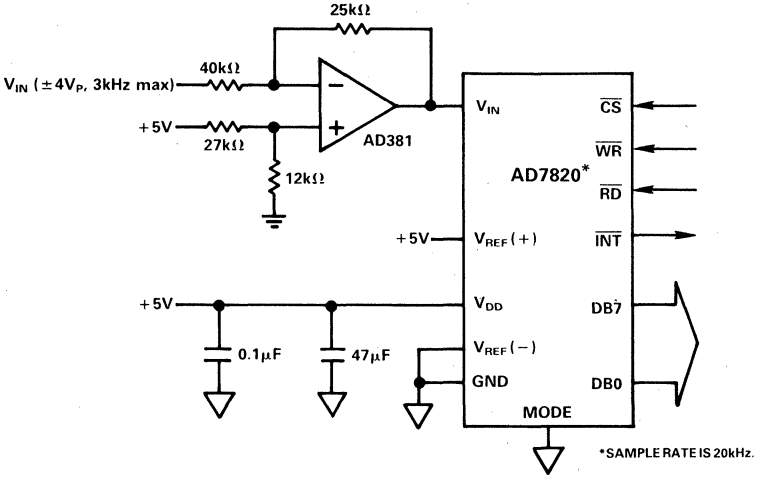


Figure 11. Telecom A/D Converter

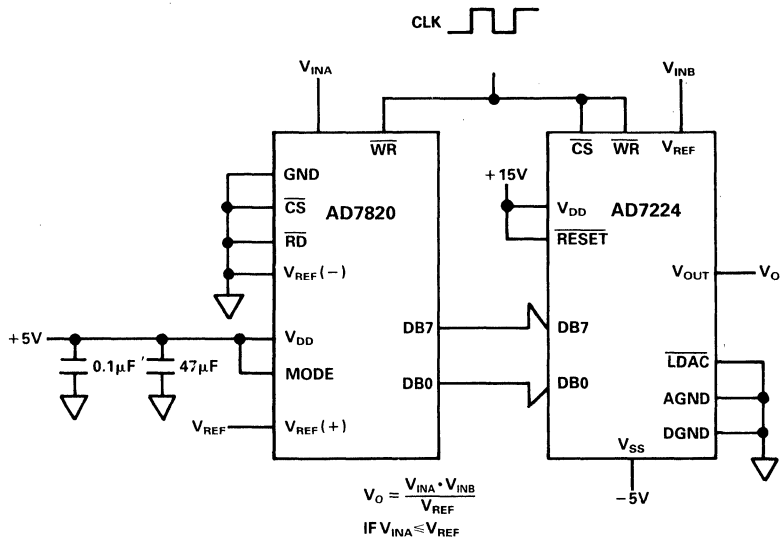


Figure 12. 8-Bit Analog Multiplier

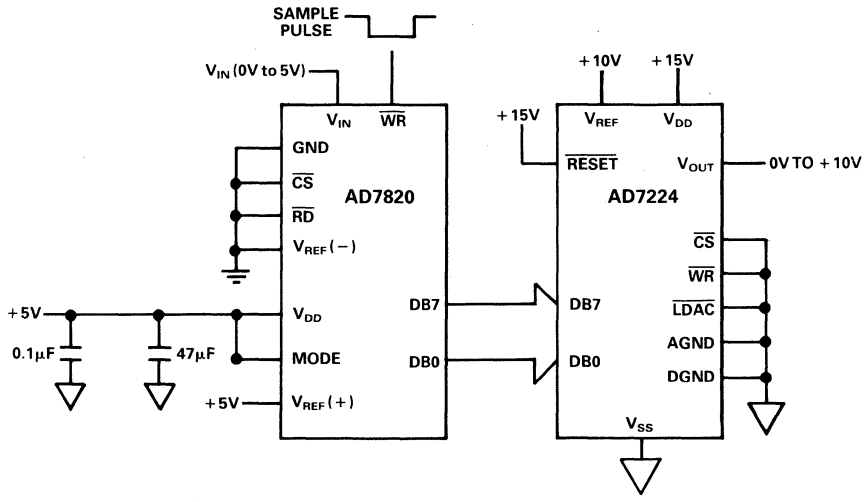


Figure 13. Fast Infinite Sample-and-Hold

ANALOG DEVICES

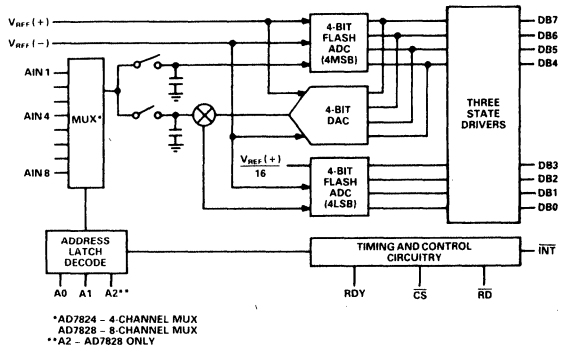
LC²MOS
High Speed 4- & 8-Channel 8-Bit ADCs

AD7824/AD7828

FEATURES

4- or 8-Analog Input Channels
Built-In Track/Hold Function
10kHz Signal Handling on Each Channel
Fast Microprocessor Interface
Single +5V Supply
Low Power: 40mW
Fast Conversion Rate, 2.5μs/Channel
Tight Error Specification: 1/2LSB

AD7824/AD7828 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7824 and AD7828 are high-speed, multichannel, 8-bit ADCs with a choice of 4 (AD7824) or 8 (AD7828) multiplexed analog inputs. A half-flash conversion technique gives a fast conversion rate of 2.5μs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of up to 10kHz (157mV/μs slew rate) on all channels. The AD7824 and AD7828 operate from a single +5V supply and have an analog input range of 0 to +5V, using an external +5V reference.

Microprocessor interfacing of the parts is simple, using standard Chip Select ($\overline{CS}$) and Read ($\overline{RD}$) signals to intitiate the conversion and read the data from the three-state data outputs. The half-flash conversion technique means that there is no need to generate a clock signal for the ADC. The AD7824 and AD7828 can be interfaced easily to most popular microprocessors.

The AD7824 and AD7828 are fabricated in an advanced, all ion-implanted, Linear-Compatible CMOS process (LC²MOS) and have low power dissipation of 40mW (typ). The AD7824 is available in a 0.3" wide, 24-pin "skinny" DIP, while the AD7828 is packaged in a 0.6" wide, 28-pin DIP.

PRODUCT HIGHLIGHTS

1. 4- or 8-channel input multiplexer gives cost-effective space-saving multichannel ADC system.
2. Fast conversion rate of 2.5μs/channel features a per channel sampling frequency of 100kHz for the AD7824 or 50kHz for the AD7828.
3. Built-in track-hold function allows handling of 4- or 8-channels up to 10kHz bandwidth (157mV/μs slew rate).
4. Tight total unadjusted error spec and channel-to-channel matching eliminate the need for user trims.
5. Single +5V supply simplifies system power requirements.
6. Fast, easy-to-use digital interface allows connection to most popular microprocessors with minimal external components. No clock signal is required for the ADC.

SPECIFICATIONS

(V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(−) = GND = 0V unless otherwise stated). All specifications T_{min} to T_{max} unless otherwise specified. Specifications apply for Mode 0.

Parameter	AD7824KN[1] AD7828KN[1]	AD7824LN AD7828LN	AD7824BQ AD7824TQ AD7828BQ AD7828TQ	AD7824CQ AD7824UQ AD7828CQ AD7828UQ	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[2]	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for which						
No Missing Codes are guaranteed	8	8	8	8	Bits	
Channel to Channel Mismatch	±1/4	±1/4	±1/4	±1/4	LSB max	
REFERENCE INPUT						
Input Resistance	1.0/4.0	1.0/4.0	1.0/4.0	1.0/4.0	kΩ min/kΩ max	
V_{REF}(+) Input Voltage Range	V_{REF}(−)/ V_{DD}	V_{REF}(−)/ V_{DD}	V_{REF}(−)/ V_{DD}	V_{REF}(−)/ V_{DD}	V min/V max	
V_{REF}(−) Input Voltage Range	GND/ V_{REF}(+)	GND/ V_{REF}(+)	GND/ V_{REF}(+)	GND/ V_{REF}(+)	V min/V max	
ANALOG INPUT						
Input Voltage Range	V_{REF}(−)/ V_{REF}(+)	V_{REF}(−)/ V_{REF}(+)	V_{REF}(−)/ V_{REF}(+)	V_{REF}(−)/ V_{REF}(+)	V min/V max	
Input Leakage Current	±3	±3	±3	±3	μA max	Analog Input Any Channel
Input Capacitance[3]	45	45	45	45	pF typ	0 to +5V
LOGIC INPUTS						
$\overline{RD}$, $\overline{CS}$, A0, A1 & A2						
V_{INH}	2.4	2.4	2.4	2.4	V min	
V_{INL}	0.8	0.8	0.8	0.8	V max	
I_{INH}	1	1	1	1	μA max	
I_{INL}	−1	−1	−1	−1	μA max	
Input Capacitance[3]	8	8	8	8	pF max	Typically 5pF
LOGIC OUTPUTS						
DB0-DB7 & $\overline{INT}$						
V_{OH}	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 360μA
V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6mA
I_{OUT} (DB0-DB7)	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance[3]	8	8	8	8	pF max	Typically 5pF
RDY						
V_{OL}[4]	0.4	0.4	0.4	0.4	V max	I_{SINK} = 2.6mA
I_{OUT}	±3	±3	±3	±3	μA max	Floating State Leakage
Output Capacitance	8	8	8	8	pF max	Typically 5pF
SLEW RATE, TRACKING[3]	0.7	0.7	0.7	0.7	V/μs typ	
	0.157	0.157	0.157	0.157	V/μs max	
POWER SUPPLY						
V_{DD}	5	5	5	5	Volts	±5% for Specified Performance
I_{DD}[5]	16	16	20	20	mA max	$\overline{CS}$ = $\overline{RD}$ = 2.4Ω
Power Dissipation	40	40	40	40	mW typ	
	80	80	100	100	mW max	
Power Supply Sensitivity	±1/4	±1/4	±1/4	±1/4	LSB max	±1/16LSB typ V_{DD} = 5V ±5%

NOTES

[1]Temperature Ranges are as follows:
AD7824/AD7828KN, LN 0 to +70°C
AD7824/AD7828BQ, CQ −25°C to +85°C
AD7824/AD7828TQ, UQ −55°C to +125°C

[2]Total Unadjusted Error includes offset, full-scale and linearity errors.

[3]Sample tested at 25°C by Product Assurance to ensure compliance.

[4]RDY is an open drain output.

[5]See Typical Performance Characteristics.

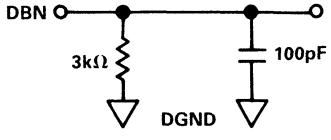
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V; V_{REF} (+) = +5V; V_{REF} (−) = GND = 0V unless otherwise stated)

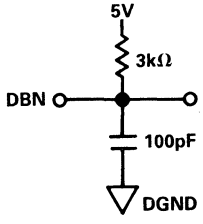
Parameter	Limit at 25°C (All grades)	Limit at T_{min},T_{max} (K,L,B,C grades)	Limit at T_{min},T_{max} (T,U grades)	Units	Conditions/Comments
t_{CSS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_{CHS}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{AS}	0	0	0	ns min	Multiplexer Address Setup Time
t_{AH}	30	35	40	ns min	Multiplexer Address Hold Time
t_{RDY}[2]	40	60	60	ns max	$\overline{RD}$ to RDY Delay. Pull-Up Resistor 5kΩ.
t_{CRD}	2.0	2.4	2.8	µs max	Conversion Time, Mode 0
t_{ACC1}[3]	85	110	120	ns max	Data Access Time after RD
t_{ACC2}[3]	50	60	70	ns min	Data Access Time after INT, Mode 0
t_{INTH}[2]	40	65	70	ns typ	$\overline{RD}$ to $\overline{INT}$ Delay
	75	100	100	ns max	
t_{DH}[4]	60	70	70	ns max	Data Hold Time
t_P	500	500	600	ns min	Delay Time between Conversions
t_{RD}	60	80	80	ns min	Read Pulse Width, Mode 1
	600	500	400	ns max	

NOTES
[1]Sample tested at 25°C to ensure compliance. All input control signals are specified with tr = tf = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]C_L = 50pF.
[3]Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

Test Circuits

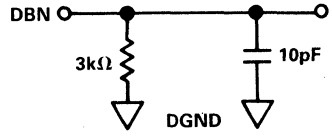


a. High-Z to V_{OH}

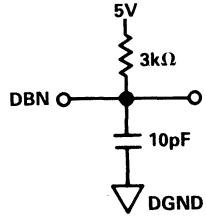


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z



b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

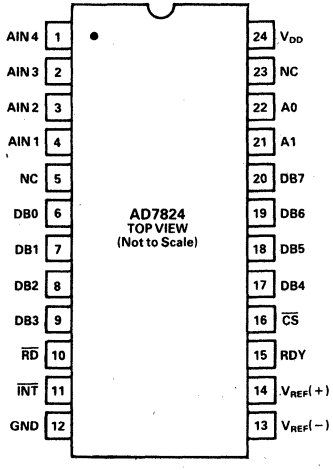
V_{DD}	0V, +7V
Digital Input Voltage to GND	
($\overline{RD}$, $\overline{CS}$, A0, A1 & A2)	−0.3V, V_{DD}
Digital Output Voltage to GND	
(DB0, DB7, RDY & $\overline{INT}$)	−0.3V, V_{DD}
V_{REF} (+) to GND	V_{REF} (−), V_{DD}
V_{REF} (−) to GND	0V, V_{REF} (+)
Analog Input (Any Channel)	−0.3V, V_{DD}
Operating Temperature Range	
KN, LN	0 to +70°C
BQ, CQ	−25°C to +85°C
TQ, UQ	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C

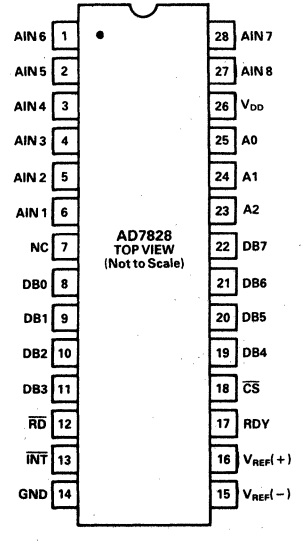
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION





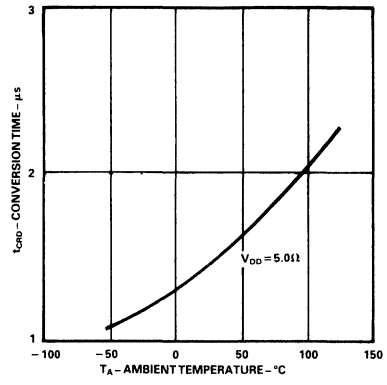
ORDERING INFORMATION

Total Unadjusted Error	Temperature Range and Package		
	Plastic 0 to +70°C	Hermetic[1] −25°C to +85°C	Hermetic[1] −55°C to +125°C
±1/2LSB	AD7824LN	AD7824CQ	AD7824UQ
±1LSB	AD7824KN	AD7824BQ	AD7824TQ

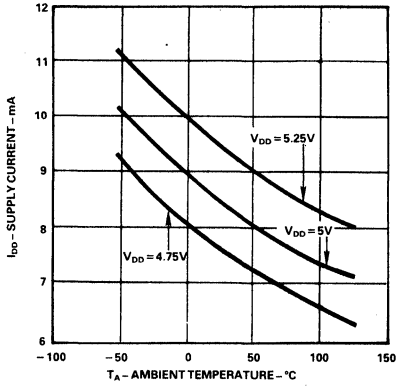
NOTES
[1] Analog Devices reserves the right to ship either cerdip or ceramic hermetic packages.
[2] For information regarding /883B versions, contact your local Analog Devices Sales Office for Military data sheet.

Total Unadjusted Error	Temperature Range and Package		
	Plastic 0 to +70°C	Hermetic[1] −25°C to +85°C	Hermetic[1] −55°C to +125°C
±1/2LSB	AD7828LN	AD7828CQ	AD7828UQ
±1LSB	AD7828KN	AD7828BQ	AD7828TQ

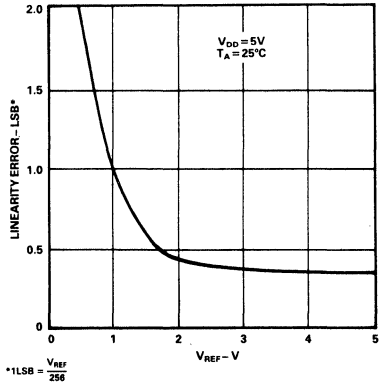
NOTES
[1] Analog Devices reserves the right to ship either cerdip or ceramic hermetic packages.
[2] For information regarding /883B versions, contact your local Analog Devices Sales Office for Military data sheet.



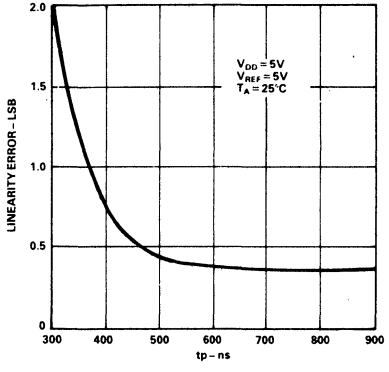
Conversion Time vs. Temperature



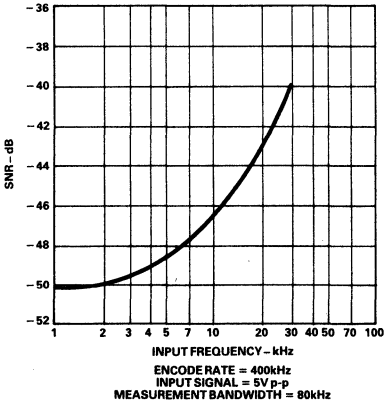
Power Supply Current vs. Temperature (not including reference ladder)



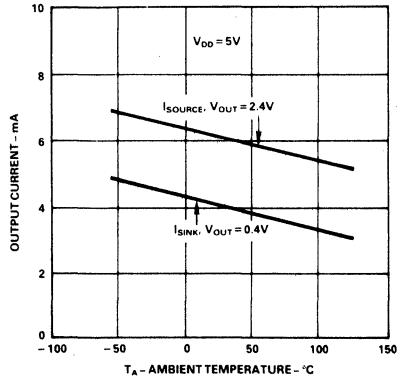
Accuracy vs V_{REF}
$[V_{REF} = V_{REF}(+) - V_{REF}(-)]$



Accuracy vs. tp



Signal-Noise Ratio vs. Input Frequency



Output Current vs. Temperature

OPERATIONAL DIAGRAM

The AD7824 is a 4-channel 8-bit A/D converter and the AD7828 is an 8-channel 8-bit A/D converter. Operational diagrams for both of these devices are shown in Figures 3 and 4. The addition of just a +5V reference allows the devices to perform the analog-to-digital function.

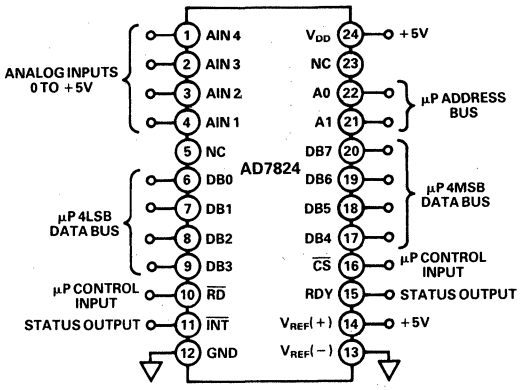


Figure 3. AD7824 Operational Diagram

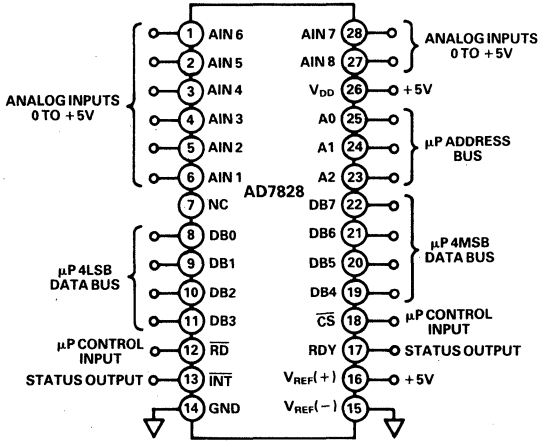


Figure 4. AD7828 Operational Diagram

CIRCUIT INFORMATION

BASIC DESCRIPTION

The AD7824/AD7828 uses a half-flash conversion technique whereby two 4-bit flash A/D converters are used to achieve an 8-bit result. Each 4-bit flash ADC contains 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. For a full 8-bit reading to be realized, the upper 4-bit flash, the most significant (MS) flash, performs a conversion to provide the 4 most significant data bits. An internal DAC, driven by the 4MSBs, then recreates an analog approximation of the input voltage. This analog result is subtracted from the input, and the difference is converted by the lower flash ADC, the least significant (LS) flash, to provide the 4 least significant bits of the output data.

APPLYING THE AD7824/AD7828

REFERENCE AND INPUT

The two reference inputs on the AD7824/AD7828 are fully differential and define the zero to full-scale input range of the A/D converter. As a result, the span of the analog input voltage for all channels can easily be varied. By reducing the reference span, $V_{REF}(+) - V_{REF}(-)$, to less than 5V the sensitivity of the converter can be increased (e.g., if V_{REF} = 2V then 1LSB = 7.8mV). The input/reference arrangement also facilitates ratiometric operation.

This reference flexibility also allows the input channel voltage span to be offset from zero. The voltage at $V_{REF}(-)$ sets the input level for all channels which produces a digital output of all zeroes. Therefore, although the analog inputs are not themselves differential, they have nearly differential-input capability in most measurement applications because of the reference design. Figures 5 to 7 show some of the configurations that are possible.

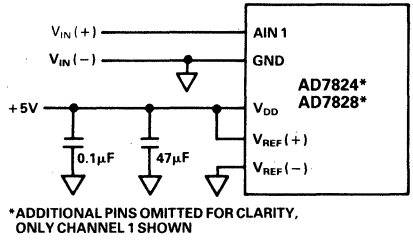


Figure 5. Power Supply as Reference

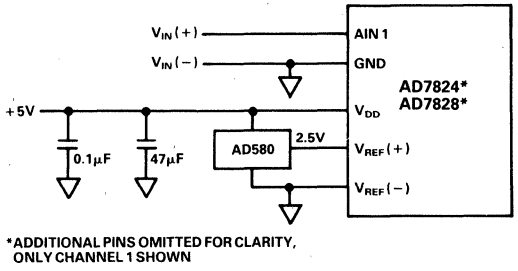


Figure 6. External Reference Using the AD580, Full-Scale Input is 2.5V

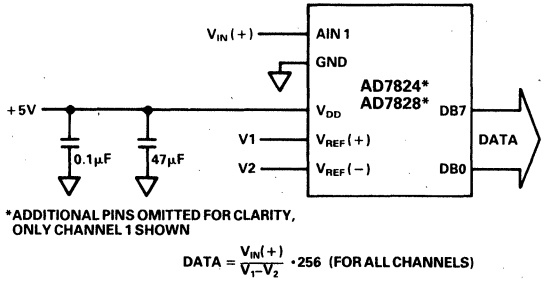


Figure 7. Input Not Referenced to GND

INPUT CURRENT

Due to the novel conversion techniques employed by the AD7824/AD7828, the analog input behaves somewhat differently than in conventional devices. The ADC's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

The equivalent input circuit of the AD7824/AD7828 is shown in Figure 8. When a conversion starts ($\overline{CS}$ and $\overline{RD}$ going low), all input switches close, and the selected input channel is connected to the most significant and least significant comparators. Therefore, the analog input is connected to thirty-one 1pF input capacitors at the same time.

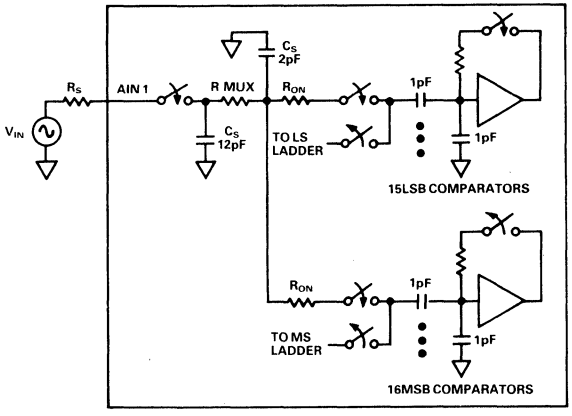


Figure 8. AD7824 AD7828 Equivalent Input Circuit

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 3k to 6k). In addition, about 14pF of input stray capacitance must be charged. The analog input for any channel can be modelled as an RC network as shown in Figure 9. As R_S increases, it takes longer for the input capacitance to charge.

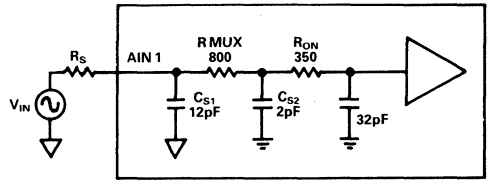


Figure 9. RC Network Model

The time for which the input comparators track the analog input is approximately 1μs at the start of conversion. Because of input transients on the analog inputs, it is recommended that a source impedence of not greater than 100 ohms be connected to the analog inputs. The output impedence of an op-amp is equal to the open loop output impedence divided by the loop gain at the frequency of interest. It is important that the amplifier driving the AD7824/AD7828 analog inputs have sufficient loop gain at the input signal frequency as to make the output impedance low.

Suitable op-amps for driving the AD7824/AD7828 are the AD544 or AD644.

INHERENT SAMPLE-HOLD

A major benefit of the AD7824's and AD7828's analog input structure is its ability to measure a variety of high-speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain stable to at least 1/2LSB throughout the conversion process if rated accuracy is to be maintained. Consequently, for many high-speed signals, this signal must be externally sampled and held stationary during the conversion. The AD7824/AD7828 input comparators, by nature of their input switching inherently accomplish this sample-and-hold function. Although the conversion time for AD7824/ AD7828 is 2μs, the time for which any selected analog input must be 1/2LSB stable is much smaller. The AD7824/AD7828 tracks the selected input channel for approximately 1μs after conversion start. The value of the analog input at that instant (1μs from conversion start) is the measured value. This value is then used in the least significant flash to generate the lower 4-bits of data.

SINUSOIDAL INPUTS

The AD7824/AD7828 can measure input signals with slew rates as high as 157mV/μs to the rated specifications. This means that the analog input frequency can be up to 10kHz without the aid of an external sample and hold. Furthermore, the AD7828 can measure eight 10kHz signals without a sample and hold. The Nyquist criterion requires that the sampling rate be twice the input frequency (i.e., 2×10kHz). This requires an ideal anti-aliasing filter with an infinite roll-off. To ease the problem of anti-aliasing filter design, the sampling rate is usually much greater than the Nyquist criterion. The maximum sampling rate (F_{max}) for the AD7824/AD7828 can be calculated as follows:

$$F_{max} = \frac{1}{t_{CRD} + t_p}$$

$$F_{max} = \frac{1}{2E-6+0.5E-6} = 400\text{kHz}$$

t_{CRD} = AD7824/AD7828 Conversion Time
t_P = Minimum Delay Between Conversion

This permits a maximum sampling rate of 50kHz for each of the 8 channels when using the AD7828 and 100kHz for each of the 4 channels when using the AD7824.

UNIPOLAR OPERATION

The analog input range for any channel of the AD7824/AD7828 is 0 to 5V as shown in the unipolar operational diagram of Figure 10. Figure 11 shows the designed code transitions which occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSB, 5/2LSB, FS-3/2LSBs). The output code is Natural Binary with 1LSB = FS/256 = (5/256)V = 19.5mV.

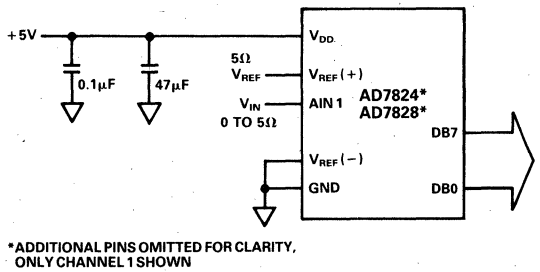


Figure 10. AD7824/AD7828 Unipolar 0 to 5V Operation

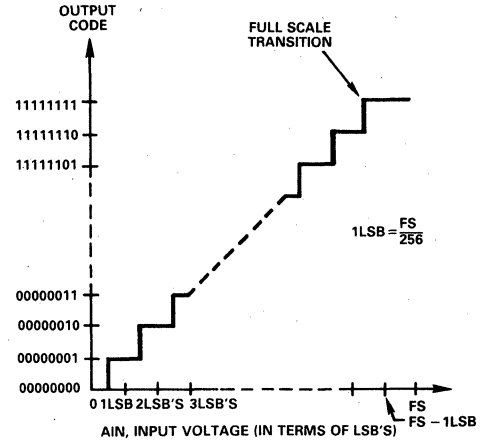


Figure 11. Ideal Input/Output Transfer Characteristic for Unipolar 0 to +5V Operation

BIPOLAR OPERATION

The circuit of Figure 12 is designed for bipolar operation. An AD544 op-amp conditions the signal input (V_{IN}) so that only positive voltages appear at AIN 1. The closed loop transfer function of the op-amp for the resistor values shown is given below:

$$AIN\ 1 = (2.5 - 0.625\ V_{IN})\ Volts$$

The analog input range is ±4V and the LSB size is 31.25mV. The output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 13.

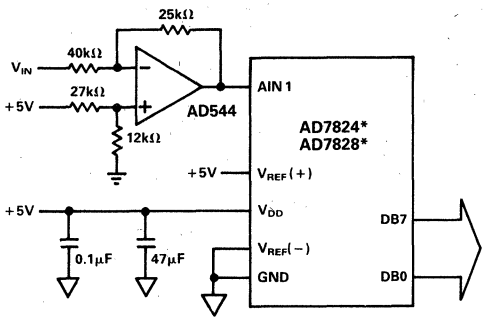


Figure 12. AD7824/AD7828 Bipolar ±4V Operation

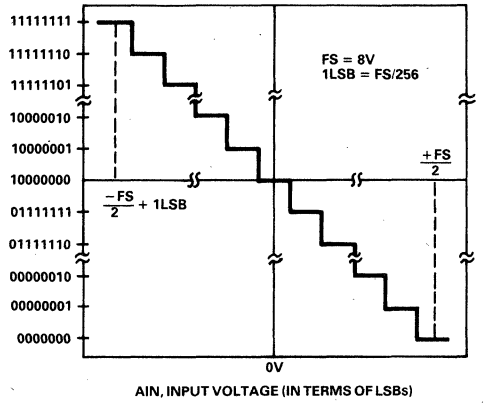


Figure 13. Ideal Input/Output Transfer Characteristic for ±4V Operation

TIMING AND CONTROL

The AD7824/AD7828 has two digital inputs for timing and control. These are Chip Select ($\overline{CS}$) and Read ($\overline{RD}$). A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion and latches the multiplexer address inputs (see Table I). There are two modes of operation as outlined by the timing diagrams of Figures 14 and 15. Mode 0 is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when conversion is complete. Mode 1 does not require microprocessor WAIT states. A READ operation initiates a conversion and reads the previous conversion results.

AD7824		AD7828			CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

Table I. Truth Table for Input Channel Selection

MODE 0

Figure 14 shows the timing diagram for Mode 0 operation. This mode can only be used for microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which latches the analog multiplexer address inputs and starts a conversion. The data bus (DB7-DB0) remains in the three-state condition until conversion is complete. There are two converter status outputs on the AD7824/AD7828, interrupt ($\overline{INT}$) and ready (RDY) which can be used to drive the microprocessor READY/WAIT input. The RDY is an open drain output (no internal pull-up device) which goes low on the falling edge of $\overline{CS}$ and $\overline{RD}$ and goes high impedance at the end of conversion, when the 8-bit conversion result appears on the data outputs. If the RDY output status is not required, then the external pull-up resistor can be omitted. The $\overline{INT}$ input goes low when conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

MODE 1

Mode 1 operation is designed for applications where the microprocessor is not forced into a WAIT state. A READ operation takes $\overline{CS}$ and $\overline{RD}$ low, which latches the multiplexer address inputs and triggers a conversion (see Figure 15). Data from the previous conversion is read from the three-state data outputs (DB7-DB0). This data may be disregarded if not required. The RDY output (open drain output) is low for the duration of the READ operation and goes high impedance on the rising edge of $\overline{CS}$ or $\overline{RD}$. If the RDY output status is not required, then the external pull-up resistor can be omitted. At the end of conversion $\overline{INT}$ goes low. A second READ operation is required to access the new conversion result. This READ operation latches a new address into the multiplexer inputs and starts another conversion. $\overline{INT}$ returns high at the end of the second READ operation, when $\overline{CS}$ and $\overline{RD}$ returns high. A delay of 2.5μs must be allowed between READ operations.

3

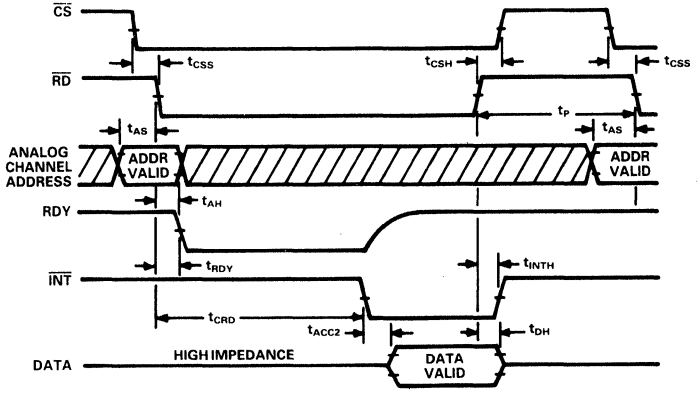


Figure 14. Mode 0 Timing Diagram

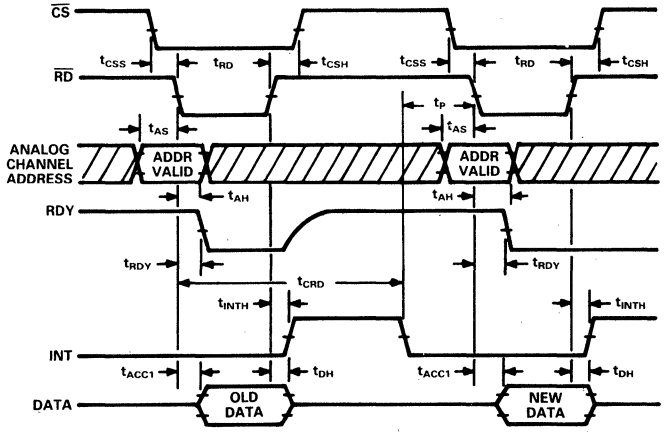


Figure 15. Mode 1 Timing Diagram

MICROPROCESSOR INTERFACING

The AD7824/AD7828 is designed to interface to microprocessors as Read Only Memory (ROM). Analog channel selection, conversion start and data read operations are controlled by $\overline{CS}$, $\overline{RD}$ and the channel address inputs. These signal are common to all memory peripheral devices.

Z80 MICROPROCESSOR

Figure 16 shows a typical AD7824/AD7828 – Z80 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is assigned a memory block starting at address C000. The following LOAD instruction to any of the addresses listed in Table II will start a conversion of the selected channel and read the conversion result.

LD B, (C000)

At the beginning of the instruction cycle when the ADC address is selected, RDY asserts the WAIT input, so that the Z80 is forced into a WAIT state. At the end of conversion RDY returns high and the conversion result is placed in the B register of the microprocessor.

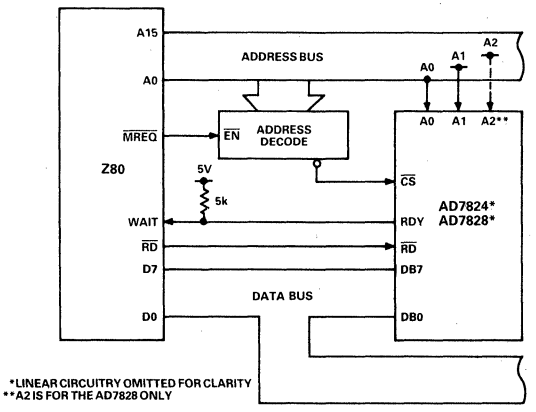


Figure 16. AD7824/AD7828 – Z80 Interface

ADDRESS	AD7824 Channel	AD7828 Channel
C000	1	1
C001	2	2
C002	3	3
C003	4	4
C004	–	5
C005	–	6
C006	–	7
C007	–	8

Table II. Address Channel Selection

MC68000 MICROPROCESSOR

Figure 17 shows a MC68000 interface. The AD7824/AD7828 is operating in Mode 0. Assume the ADC is again assigned a memory block starting at address C000. A MOVE instruction to any of the addresses in Table II starts a conversion and reads the conversion result.

MOVE•B $C000,D0

Once conversion has begun, the MC68000 inserts WAIT states, until INT goes low asserting DTACK at the end of conversion. The microprocessor then places the conversion results in the D0 register.

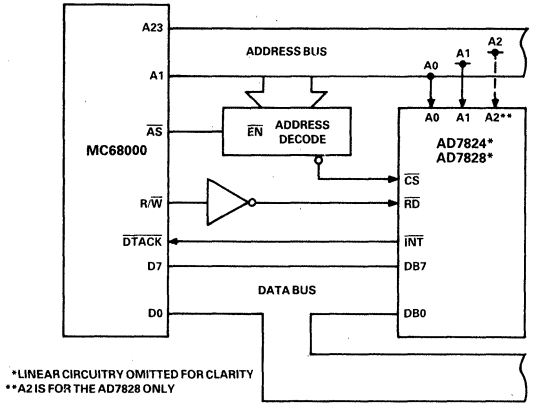


Figure 17. AD7824/AD7828 – MC68000 Interface

TMS32010 MICROCOMPUTER

A TMS32010 interface is shown in Figure 18. The AD7824/AD7828 is operating in Mode 1 (i.e., no μP WAIT states). The ADC is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into the accumulator.

IN, A PA (PA = PORT ADDRESS)

The port address (000 to 111) selects the analog channel to be converted. When conversion is complete a second I/O instruction (IN, A PA) reads the up-to-date data into the accumulator and starts another conversion. A delay of 2.5μs must be allowed between conversions.

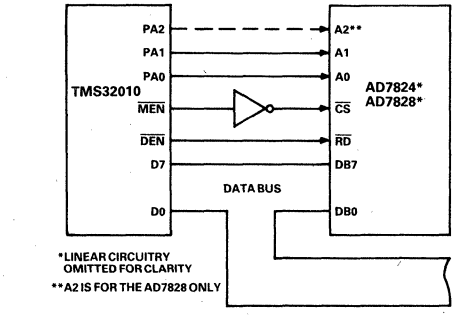


Figure 18. AD7824/AD7828 – TMS32010 Interface

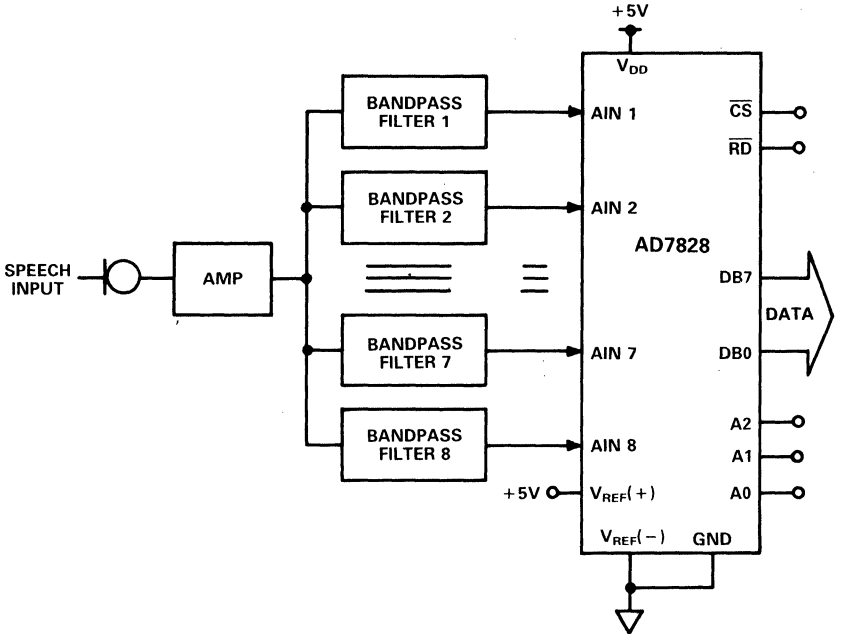


Figure 19. Speech Analysis Using Real-Time Filtering

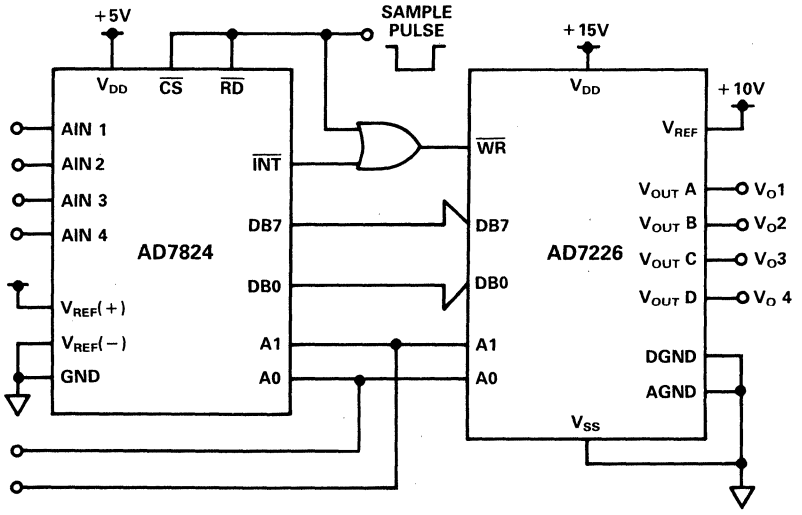
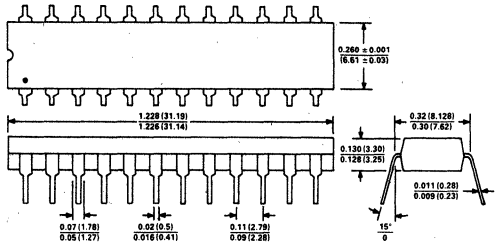


Figure 20. 4-Channel Fast Infinite Sample-and-Hold

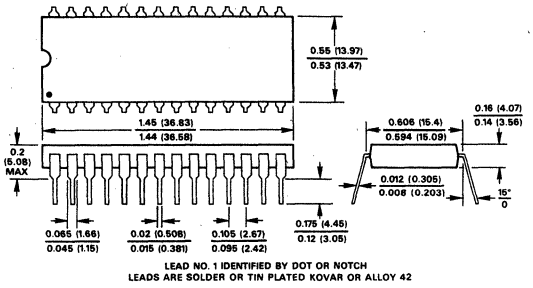
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-PIN PLASTIC (SUFFIX N)

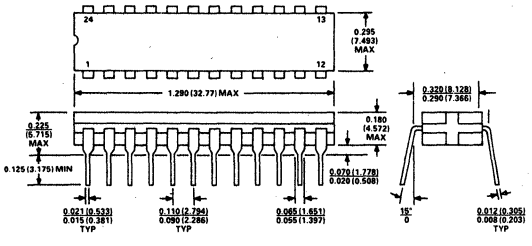


28-PIN PLASTIC DIP (SUFFIX N)

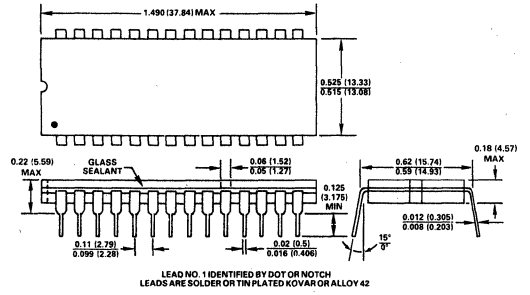


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

24-PIN CERDIP (SUFFIX Q)[1]

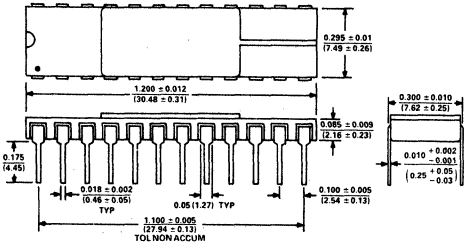


28-PIN CERDIP (SUFFIX Q)[1]

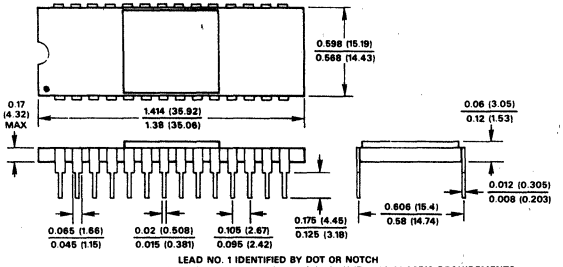


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN PLATED KOVAR OR ALLOY 42

24-PIN CERAMIC (SUFFIX Q)[1]



28-PIN CERAMIC DIP (SUFFIX Q)[1]



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

NOTE

[1]Analog Devices reserves the right to ship either cerdip or ceramic hermetic packages.

ANALOG DEVICES

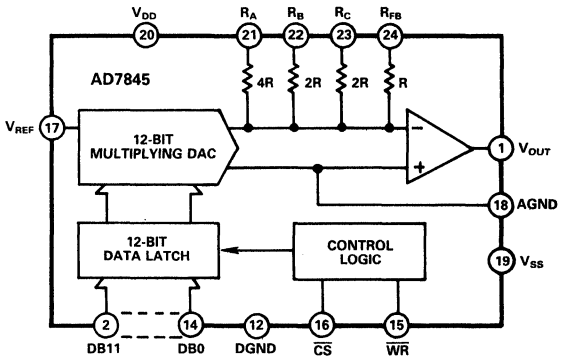
LC²MOS 12-Bit Multiplying DAC

AD7845

FEATURES
12-Bit CMOS MDAC with Output Amplifier
4-Quadrant Multiplication
Guaranteed Monotonic (T_{min} to T_{max})
Space-Saving 0.3", 24-Pin Package
Application Resistors on Chip for Gain Ranging, Etc.
Low Power LC²MOS

APPLICATIONS
Automatic Test Equipment
Digital Attenuators
Programmable Power Supplies
Programmable Gain Amplifiers
Digital to 4-20mA Converters

AD7845 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The AD7845 is the industry's first full 4-quadrant multiplying D/A converter with an on-chip amplifier. It also contains data latches for easy microprocessor interfacing and application resistors for gain ranging, offsetting the output voltage, etc.

The Linear Compatible CMOS (LC²MOS) process used in the manufacture of the AD7845 has been specifically developed to allow high-speed digital logic inputs and precision analog circuits to be integrated on the same chip.

The device is housed in a 0.3", 24-pin package. The 12 data inputs drive latches which are controlled by standard $\overline{CS}$ and $\overline{WR}$ signals, making microprocessor interfacing simple. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs can be tied to ground, making all latches transparent. All digital inputs are TTL and 5V CMOS compatible.

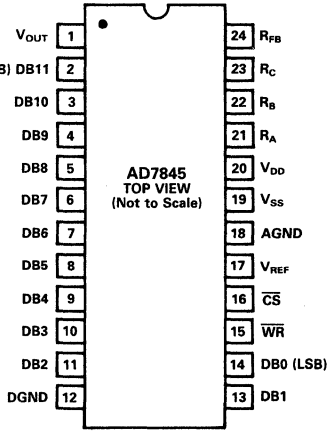
The output amplifier can supply ±10V into a 2kΩ load. It is internally compensated and its input offset voltage is very low due to laser trimming at wafer level. For normal operation, R_{FB} is tied to V_{OUT} but the user may alternatively choose R_A, R_B or R_C to scale the output voltage range.

PRODUCT HIGHLIGHTS

1. Voltage Output Multiplying DAC:
   The AD7845 is the first DAC which has a full 4-Quadrant multiplying capability and an output amplifier on-chip. All specifications include amplifier performance.
2. Space Saving:
   The AD7845 saves space in two ways. The integration of the output amplifier on-chip means that chip count is reduced. The part is housed in a new 24-pin, 0.3" package which takes up half the space of the old 24-pin double DIP package.

PRELIMINARY TECHNICAL DATA

PIN CONFIGURATION



SPECIFICATIONS[1] (V_{DD} = +12V to +15V, ±10%. V_{SS} = −12V to −15V, ±10%. V_{REF} = +10V, AGND = DGND = 0V, V_{OUT} (Pin 1) connected to R_{FB} (Pin 24). All specifications T_{min} to T_{max} unless otherwise stated).

Parameter	AD7845JN AD7845AQ	AD7845KN AD7845BQ	AD7845LN AD7845CQ	AD7845SQ	AD7845TQ	AD7845UQ	Units	Test Conditions/Comments
ACCURACY								$\frac{V_{REF}}{}$
Resolution	12	12	12	12	12	12	Bits	1LSB = 2^{12} = 2.4mV
Relative Accuracy	±2	±1	±1/2	±2	±1	±1/2	LSB max	All grades are guaranteed
Differential Nonlinearity	±1	±1	±1	±1	±1	±1	LSB max	monotonic over temperature.
Zero Code Offset Error	±2	±1	±1	±2	±1	±1	mV max	DAC register loaded with all 0's.
Offset Temperature Coefficient; (ΔOffset/ΔTemperature)[2]	±5	±5	±5	±5	±5	±5	µV/°C max	
Gain Error	±16	±4	±1	±16	±4	±1	LSB max	R_{FB}, V_{OUT} connected.
	+16	±4	±1	±16	±4	±1	LSB max	R_C, V_{OUT} connected, V_{REF} = +5V
	±16	±4	±1	±16	±4	±1	LSB max	R_B, V_{OUT} connected, V_{REF} = +5V
	±16	±4	±1	±16	±4	±1	LSB max	R_A, V_{OUT} connected, V_{REF} = 2.5V
Gain Temperature Coefficient; (ΔGain/ΔTemperature)[2]	±5	±5	±5	±5	±5	±5	ppm/°C max	Typical value is 1 ppm/°C
REFERENCE INPUT								
Input Resistance, Pin 17	5	5	5	5	5	5	kΩ min	Typical input resistance = 10kΩ
	20	20	20	20	20	20	kΩ max	
DIGITAL INPUTS								
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	0.8	0.8	V max	
V_{IN} (Input Current)								
+25°C	±1	±1	±1	±1	±1	±1	µA max	Digital Inputs at 0V
T_{min} to T_{max}	±10	±10	±10	±10	±10	±10	µA max	and V_{DD}
C_{IN} (Input Capacitance)	7	7	7	7	7	7	pF max	
POWER SUPPLY								
V_{DD} Range	10.2/ 16.5	10.2/ 16.5	10.2/ 16.5	10.2/ 16.5	10.2/ 16.5	10.2/ 16.5	V min/V max	Specifications guaranteed over this range.
V_{SS} Range	−10.8/ −16.5	−10.8/ −16.5	−10.8/ −16.5	−10.8/ −16.5	−10.8/ −16.5	−10.8/ −16.5	V min/V max	
Power Supply Rejection								
ΔGain/ΔV_{DD}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	$\Delta V_{DD} = V_{DDmax} - V_{DDmin}$
ΔGain/ΔV_{SS}	±0.2	±0.2	±0.2	±0.2	±0.2	±0.2	% per % max	$\Delta V_{SS} = V_{SSmax} - V_{SSmin}$
I_{DD}	5	5	5	5	5	5	mA max	$\overline{CS}$ low, all other digital inputs high, V_{OUT} unloaded.
I_{SS}	4	4	4	4	4	4	mA max	V_{OUT} unloaded.
DYNAMIC PERFORMANCE								
Output Voltage Settling Time	5	5	5	5	5	5	µs max	To 0.01% of full-scale range. V_{OUT} load = 2kΩ, 100pF. DAC register alternately loaded with all 0's and all 1's.
Slew Rate	5	5	5	5	5	5	V/µs typ	V_{OUT} load = 2kΩ, 100pF
Digital-to-Analog Glithc Impulse	1000	1000	1000	1000	1000	1000	nV-sec typ	Measured with V_{REF} = 0V, DAC Register alternately loaded with all 0's and all 1's.
Multiplying Feedthrough Error	5	5	5	5	5	5	mVp-p typ	V_{REF} = ±10V, 10kHz sinewave. DAC register loaded with all 0's. At T_A = 25°C, error is 3mVp-p typ.
Unity Gain Small Signal Bandwidth	1	1	1	1	1	1	MHz typ	DAC Register loaded with all 1's. V_{REF} = ±100mV sinewave.
Full-Power Bandwidth	100	100	100	100	100	100	kHz typ	DAC register loaded with all 1's. V_{REF} = ±10V sinewave R_L = 2kΩ. C_L = 100pF
Total Harmonic Distortion	−80	−80	−80	−80	−80	−80	dB typ	V_{REF} = 6V RMS, 1kHz sinewave
OUTPUT CHARACTERISTICS								
Open Loop Gain	90	90	90	90	90	90	dB min	V_{OUT}, R_{FB} not connected. V_{OUT} = ±10V, R_L = 2kΩ
Output Voltage Swing	±10	±10	±10	±10	±10	±10	V min	R_L = 2kΩ, C_L = 100pF
Output Resistance	0.5	0.5	0.5	0.5	0.5	0.5	Ω typ	
Short Circuit Current	40	40	40	40	40	40	mA typ	V_{OUT} shorted to AGND.
Output Noise Voltage Density (10Hz-100kHz)	50	50	50	50	50	50	nV/$\sqrt{Hz}$ typ	Includes noise due to output amplifier and Johnson Noise of R_{FB}.

NOTES

[1]Temperature ranges are as follows: JN, KN, LN Versions: 0 to +70°C
AQ, BQ, CQ Versions: −25°C to +85°C
SQ, TQ, UQ Versions: −55°C to +125°C

[2]Guaranteed by Product Assurance testing.

[3]The metal lid on the ceramic package is connected to Pin 12 (DGND).

Specifications subject to change without notice.

ANALOG DEVICES

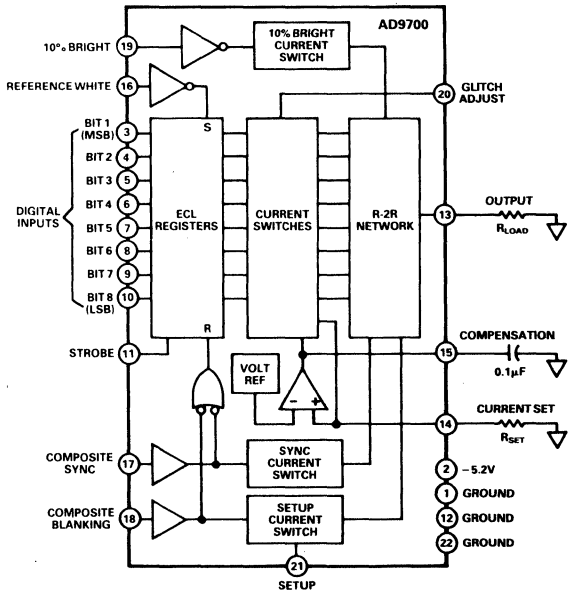
Monolithic Video D/A Converter

AD9700

FEATURES
Update Rates to 125MHz
Low Glitch Energy
Complete Composite Inputs
On-Chip Reference Voltage
Single −5.2V Power Supply

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

AD9700 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9700 digital-to-analog converter is a monolithic device capable of accepting eight bits of digital data at update rates as high as 125MHz. On-chip registers on the data lines help minimize "glitches" in the output signal.

Incorporating the AD9700 into system designs is eased by its blanking, sync, 10% brightness, and reference white control signals. An on-board reference eliminates the need for external circuits, making it considerably easier to design the AD9700 into high-speed applications than it is for converters which do not have this feature.

The unit is housed in a 22-pin package; operates from a single −5.2V power supply; and dissipates only 650mW, making this the smallest, lowest power D/A converter available to design engineers who need true "graphics ready" converters for raster scan, color graphics, and other high-speed systems.

This device is a natural extension of the Analog Devices advanced technology that produced the first hybrid converters which included composite capabilities. Like the earlier HDG-Series D/A converters, the AD9700 is designed to have general output compatibility with EIA Standards RS-170 and RS-343.

Five versions of the AD9700 are available. The AD9700BW (non-hermetic) and AD9700BD (hermetic) are DIP units operating over a temperature range of −25°C to +85°C; the hermetic DIP AD9700SD is for use over a temperature range of −55°C to +125°C. The AD9700BE and AD9700SE are leadless chip carrier (LCC) devices for temperature ranges of −25°C to +85°C and −55°C to +125°C, respectively. The SD and SE versions are available screened to military requirements; contact the factory for details.

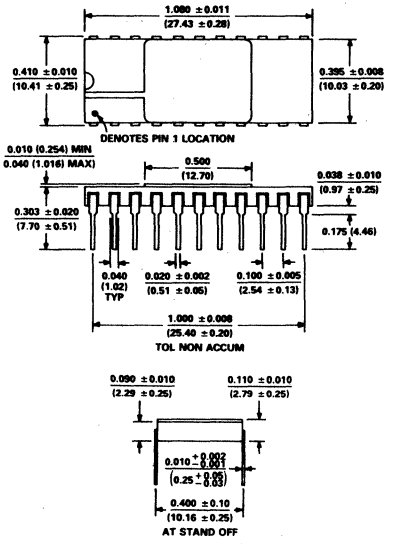
This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	AD9700BD/BW[1]	AD9700SD[2]
RESOLUTION	Bits	8	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (adjustable)	mV	2.5	*
Current (adjustable)	μA	67	*
ACCURACY (GS = Gray Scale; FS = Full Scale)			
Linearity	±% GS	0.2	*
Differential Linearity	±% GS, max	0.2	*
Integral Linearity	±% GS, max	0.2	*
Zero Offset (Initial) Voltage	mV (max)	0.3 (0.9)	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C (max)	15	*(30)
Gain	ppm/°C (max)	50	*(125)
Zero Offset	ppm/°C (max)	10	*(15)
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[3]			
Settling Time to 0.4% GS; 0V to 637.5mV GS change			
Voltage	ns (max)	10 (12)	*
Update Rate[4]	MHz (min)	125 (100)	*
Slew Rate	V/μs	300	*
Rise Time	ns	2	*
Glitch Impulse[5]	pV-s	80	*
DIGITAL DATA INPUTS			
Logic Compatibility		ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT			
Logic Compatibility		ECL	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
Setup Time (Data)	ns, min	2.5	*
Hold Time (Data)	ns, min	1.5	*
Propagation Delay	ns (max)	4 (5)	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		ECL	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS			
Settling Time to 10% of Final Value for:			
10% Bright	ns, max	10	*
Reference White	ns, max	10	*
Composite Sync	ns, max	10	*
Composite Blanking	ns, max	10	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	53.25 (7.5)	*
1k to −5.2V	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*

MECHANICAL DIMENSIONS

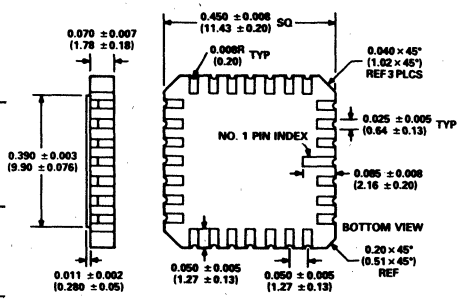
Dimensions shown in inches and (mm).



Models AD9700BD, AD9700BW, and AD9700SD

28-TERMINAL LEADLESS CHIP CARRIER JEDEC TYPE C

Dimensions shown in inches and (mm).



Models AD9700BE and AD9700SE

(Pins numbered clockwise)

Parameter	Units	AD9700BD/BW[1]	AD9700SD[2]
ANALOG OUTPUT			
GS Current[6]	mA	0 to −17	*
GS Voltage[7]	mV (±1%)	0 to −637.5	*
Compliance	V	−1.2 to +0.1	*
Internal Impedance	Ω (min/max)	800 (680/920)	*
REFERENCE WHITE[8]			
Current			
Logic "1"	mA (±4%)	Normal Operation	*
Logic "0"	mA (±4%)	0 or −1.9	*
Voltage			
Logic "1"	mV (±4%)	Normal Operation	*
Logic "0"	mV (±4%)	0 or −71	*
10% BRIGHT[9]			
Current			
Logic "1"	mA (±5%)	−1.9	*
Logic "0"	mA (±5%)	0	*
Voltage			
Logic "1"	mV (±5%)	−71	*
Logic "0"	mV (±5%)	0	*
COMPOSITE SYNC[9,10]			
Current			
Logic "1"	mA (±4%)	0	*
Logic "0"	mA (±4%)	−7.6	*
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	−285	*
COMPOSITE BLANKING[9,10] (Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)			
Current			
Logic "1"	mA (±4%)	0	*
Logic "0"	mA (±4%)	−1.4	*
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	−53.25	*
VOLTAGE REFERENCE TOLERANCE (Deviation from Nominal −1.26V)	mV (max)	±20 (±60)	*
POWER REQUIREMENTS			
−5.2V ±0.25V	mA (max)	125 (140)	*
Power Supply Rejection Ratio	%/V	0.025/0.25	*
Power Dissipation	mW (max)	650 (728)	*
TEMPERATURE RANGE			
Operating (Case)	°C	−25 to +85	−55 to +125
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[11]			
Junction to Air, θja (Free Air)	°C/W, max	55	*
Junction to Case, θjc	°C/W, max	15	*
MTBF[12]			
Mean Time Between Failures	Hours	1.95×10^5	*

NOTES
[1]Electrical specifications for AD9700BE same as AD9700BD/BW.
[2]Electrical specifications for AD9700SE same as AD9700SD.
[3]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.
[4]Minimum update rate limited by full-scale settling time for eight bits. Unit can be updated to 125MHz.
[5]Glitch can be reduced with glitch adjustment.
[6]FS current = GS current + video functions = 30mA.
[7]LSB value of 2.5mV used for calibration. This causes Gray Scale output to to be 637.5mV rather than 643mV shown in idealized composite waveform elsewhere in this data sheet; both values are well within the output and EIA Standard RS-170 tolerances. $I_{OUT} = (1.26/R_{SET}) \times 4$ when $R_{SET} = 300\Omega$.
[8]Effect on analog output of logic "0" at Reference White input depends on signal at 10% Bright input (see Table I).
[9]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray Scale analog output at Pin 13.
[10]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White.
[11]Maximum junction temperature = 150°C.
[12]Calculated using MIL HNBK-217; Ground Fixed; +25°C Ambient.
*Specifications same as AD9700BD/BW.
Specifications subject to change without notice.

PIN DESIGNATIONS
MODELS AD9700BD, AD9700BW, and AD9700SD

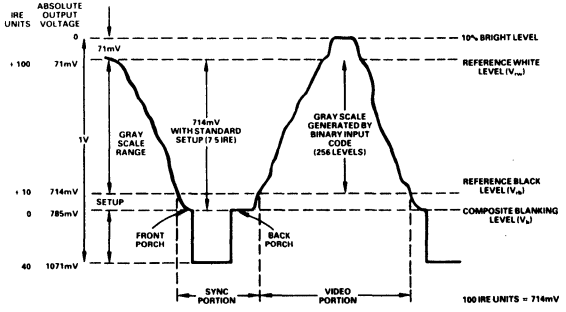
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	12	GROUND
2	−5.2V	13	OUTPUT
3	BIT 1 (MSB)	14	CURRENT SET
4	BIT 2	15	COMPENSATION
5	BIT 3	16	REFERENCE WHITE
6	BIT 4	17	COMPOSITE SYNC
7	BIT 5	18	COMPOSITE BLANKING
8	BIT 6	19	10% BRIGHT
9	BIT 7	20	GLITCH ADJUST
10	BIT 8 (LSB)	21	SETUP
11	STROBE	22	GROUND

NOTE: CONNECT PINS 1, 12, AND 22 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

PIN DESIGNATIONS
MODELS AD9700BE, AD9700SE

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	15	GROUND
2	GROUND	16	OUTPUT
3	GROUND	17	−5.2V
4	−5.2V	18	CURRENT SET
5	BIT 1 (MSB)	19	COMPENSATION
6	BIT 2	20	REFERENCE WHITE
7	BIT 3	21	COMPOSITE SYNC
8	BIT 4	22	NO CONNECTION
9	BIT 5	23	COMPOSITE BLANKING
10	BIT 6	24	10% BRIGHT
11	BIT 7	25	GLITCH ADJUST
12	BIT 8	26	SETUP
13	STROBE	27	−5.2V
14	NC	28	V_{EE}

NOTE: CONNECT PINS 1, 2, 3, AND 15 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.



Idealized Composite Output Waveform

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	−690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	−975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	−1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.50[4]

NOTES
[1]Setup (Pin 21) grounded (0 IRE units).
[2]Setup (Pin 21) open (7.5 IRE units).
[3]Setup (Pin 21) to −5.2V through 1k (10 IRE units).
[4]Setup (Pin 21) to −5.2V (20 IRE units).

Analog output values shown are based on LSB value of 2.5mV used for ease of calibration; this causes Gray Scale output to be 637.5mV rather than 643mV shown elsewhere in this data sheet in sketch of idealized composite output. Both values are well within the output and EIA Standard RS-170 tolerances.

Table I.

USING AD9700 AS RASTER SCAN D/A

Refer to the block diagram of the AD9700 D/A converter.

The digital input bits represent the Gray Scale value of the 256 (2^8) discrete levels between Reference Black and Reference White in a composite video signal, and are applied to Pins 3 through 10.

The output analog signal (at Pin 13) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, Reference White, Composite Sync, and Composite Blanking; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs and various combinations of control inputs are selected.

Refer to Table I.

As the footnote to this figure points out, the full-scale (−637.5mV) output of the AD9700 is different from the −643mV output of the idealized composite waveform shown elsewhere in this data sheet. The reason for this discrepancy is Analog Devices' use of 2.5mV for the value of the LSB; that choice of LSB weighting eases calibration of the converter. The disparity does not cause any problems in using the device, since both values are well within the tolerances of the output and the RS-170 standard.

Referring again to the block diagram, the Strobe input applied to the AD9700 clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize pertubations or "glitches" in the analog output signal.

The signal applied to the Reference White input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the AD9700 goes to 0V or to −71mV, depending upon whether or not the 10% Bright signal is also operated.

A logic "0" applied to either the Composite Sync or Composite Blanking input will reset the input registers to 00000000. The analog output at Pin 13 will be −922.5mV (−637.5mV plus −285mV) if the Composite Sync input is operated; this is not affected by the value of IRE units at the setup input.

When Composite Blanking is operated, the analog output will go to its full-scale value of −637.5mV plus some additional amount, as determined by the voltage at setup. The −53.25mV example used in the specifications section of the data sheet is based on the setup input floating, which is equivalent to 7.5 IRE units. (For this example, the analog output would be 690.75mV.)

The internal voltage reference shown in the block diagram is a bandgap type. Including this reference within the converter eliminates the need for external circuits, making it markedly easier to design the AD9700 into various applications. The internal precision reference also provides superior power supply rejection and gain tempco.

Details on the connections for using the AD9700 in composite video applications are shown in Figure 1.

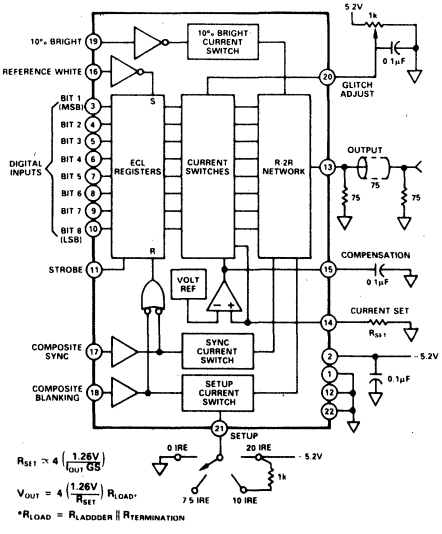


Figure 1. AD9700 D/A Connections

ANALOG DEVICES

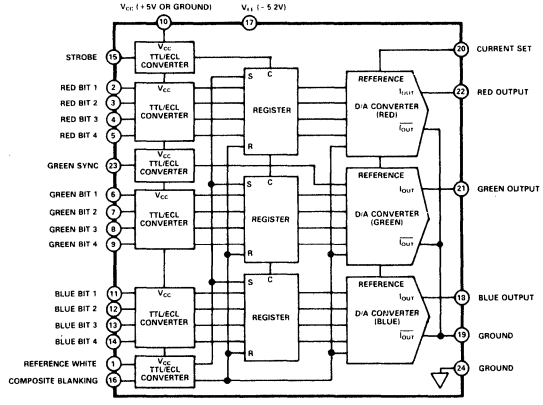
Triple 4-Bit D/A Converter

AD9702

FEATURES
ECL or TTL Compatible
Composite Inputs
125MHz Update Rates Minimum

APPLICATIONS
Raster Scan Displays
Color Graphics Systems
General Video Reconstruction

AD9702 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9702 D/A Converter is a single monolithic IC containing three separate 4-bit digital-to-analog (D/A) converters for red, green, blue (RGB) graphics display applications; 4,096 colors are available to the user. Composite blanking, green sync, and reference white digital control inputs are also included. On-chip data registers and a capability for varying output drive make this a *total* functional solution for graphics displays.

A unique TTL/ECL interface allows the designer a choice of logic compatibility for all inputs; this can be accomplished by applying either +5V or ground to the V_{CC} pin. Internally, the registers and control switching signals operate at ECL logic levels to help assure low glitch impulse at the DAC outputs.

The unit is housed in a 24-pin ceramic package and operates with −5.2V applied for the ECL mode; and −5.2V and +5V for TTL mode. Power dissipation is 1.3 watts for ECL operation and 1.5 watts for TTL.

Monolithic devices are inherently less expensive and more reliable than hybrids. When combined with its small size and outstanding electrical characteristics, these attributes make the AD9702 D/A Converter the first choice for designers of next-generation, medium-resolution displays.

3

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

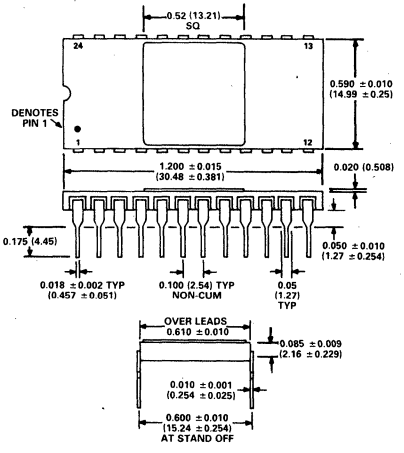
Parameter	Units	AD9702BD/BW
RESOLUTION	Bits	4
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Voltage (Adjustable)	mV	40
Current (Adjustable)	mA	1
ACCURACY (GS = Gray Scale; FS = Full Scale)		
Linearity	±% GS	0.8
Differential Linearity	±% GS, max	0.8
Zero Offset (Initial)	mV, max	0.5
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C (max)	20 (30)
Zero Offset	ppm/°C (max)	10 (15)
Gain	ppm/°C (max)	200 (400)
Gain Tracking	ppm/°C	100
DYNAMIC CHARACTERISTICS		
Settling Time – Voltage[1]		
ECL Mode (to ±3.2% GS)	ns, max	5
TTL Mode (to ±3.2% GS)	ns, max	6
Update Rate		
ECL Mode	MHz, min	125
TTL Mode	MHz, min	75
Rise Time	ns	3
Glitch Impulse	pV-s	80
DIGITAL INPUTS		
Logic Compatibility		ECL/TTL
Coding		Binary (BIN)
ECL Logic Levels		
"1"	V (min/max)	−0.9 (−1.1/−0.6)
"0"	V (min/max)	−1.7 (−2.0/−1.5)
TTL Logic Levels		
"1"	V (min/max)	+3.5 (+2.0/+5.0)
"0"	V (min/max)	+0.2 (+0.0/+0.8)
Loading (Each Bit; with Typical Input Logic Levels)		
ECL "1"	μA/pF	50/5
ECL "0"	μA/pF	−100/5
TTL "1"	μA/pF	10/5
TTL "0"	mA/pF	1.5/5
Setup Time (Data)		
ECL	ns, max	2.5
TTL	ns, max	3.5
Hold Time (Data)		
ECL	ns, max	2
TTL	ns, max	3
Propagation Delay		
ECL	ns (max)	4 (5)
TTL	ns (max)	5 (6)
SPEED PERFORMANCE – CONTROL INPUTS		
ECL and TTL Settling Time to 10% of GS for:		
$\overline{\text{Reference White}}$	ns, max	10
$\overline{\text{Composite Blanking}}$	ns, max	10
$\overline{\text{Green Sync}}$	ns, max	10
10% Bright	ns	10
RED, GREEN, AND BLUE ANALOG OUTPUTS		
Gray Scale Current	mA	0 to −16
$\overline{\text{Ref White}}$[2] = "0"	mA	0
$\overline{\text{Ref White}}$ = "1"	mA	Normal Operation[3]
$\overline{\text{Composite Blanking}}$[4] = "0"	mA	−1.4
$\overline{\text{Composite Blanking}}$ = "1"	mA	Normal Operation
$\overline{\text{Green Sync}}$[5] = "0"	mA	−7.6
$\overline{\text{Green Sync}}$ = "1"	mA	Normal Operation
Gray Scale Voltage	mV	0 to −600 (±1%)
$\overline{\text{Ref White}}$[2] = "0"	mV	0
$\overline{\text{Ref White}}$ = "1"	mV	Normal Operation[3]
$\overline{\text{Composite Blanking}}$[4] = "0"	mV	−53
$\overline{\text{Composite Blanking}}$ = "1"	mV	Normal Operation
$\overline{\text{Green Sync}}$[5] = "0"	mV	−285
$\overline{\text{Green Sync}}$ = "1"	mV	Normal Operation

ABSOLUTE MAXIMUM RATINGS

	ECL Lower	ECL Upper	TTL Lower	TTL Upper
Supply Voltages				
V_{CC} (Pin 10)	−0.1V	+1.0V	0.0V	+6.0V
V_{EE} (Pin 17)	−6.0V	+0.3	−6.0V	+0.3V
Power Dissipation (Nominal Voltages)	1.5W		1.8W	
D/A Output Current	30mA		30mA	
Temperature				
Operating (Case)	−55°C to +125°C		−55°C to +125°C	
Storage	−55°C to +150°C		−55°C to +150°C	

MECHANICAL DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
24	GROUND	1	$\overline{\text{REFERENCE WHITE}}$
23	$\overline{\text{GREEN SYNC}}$	2	RED BIT 1 (MSB)
22	RED OUTPUT	3	RED BIT 2
21	GREEN OUTPUT	4	RED BIT 3
20	CURRENT SET	5	RED BIT 4 (LSB)
19	GROUND	6	GREEN BIT 1 (MSB)
18	BLUE OUTPUT	7	GREEN BIT 2
17	V_{EE} (−5.2V)	8	GREEN BIT 3
16	$\overline{\text{COMPOSITE BLANKING}}$	9	GREEN BIT 4 (LSB)
15	STROBE	10	V_{CC} (+5V OR GROUND)
14	BLUE BIT 4 (LSB)	11	BLUE BIT 1 (MSB)
13	BLUE BIT 3	12	BLUE BIT 2

NOTE: FOR NORMAL OPERATION, CONNECT PINS 19 AND 24 TOGETHER AND TO LOW-IMPEDANCE GROUND PLANE AS CLOSE TO CASE AS POSSIBLE.

Parameter	Units	AD9702BD/BW
RED, GREEN, AND BLUE ANALOG OUTPUTS (Cont.)		
Output Impedance	Ω (min/max)	10k (5k/15k)
Compliance	V	+3.0 to −1.2
Matching (Between any Two Gray Scale Outputs)	±% GS	1.0
RGB Outputs Time Skew	ns, max	2
RGB Outputs Crosstalk[6] (100MHz Bandwidth)	mV	20
Clock Noise on Outputs (100MHz Bandwidth)	mV	5
POWER REQUIREMENTS		
−5.2V ±0.25V[7]	mA (max)	250 (288)
+5V ±0.25V (TTL Only)	mA (max)	50 (60)
Power Supply Rejection Ratio	mV/mV	0.115
ECL Power Dissipation	W (max)	1.3 (1.5)
TTL Power Dissipation	W (max)	1.55 (1.8)
TEMPERATURE RANGE		
Operating (Case)	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[8]		
Junction to Air, θ_{JA} (Free Air)	°C/W, max	40
Junction to Case, θ_{JC}	°C/W, max	12

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.
[2]Digital "0" at $\overline{\text{Reference White}}$ control input (Pin 1) sets registers; red, green, and blue outputs go to zero.
[3]In "normal operation," GS current or GS voltage outputs for red, green, and/or blue are established by RGB digital inputs.
[4]Digital "0" at $\overline{\text{Composite Blanking}}$ control input (Pin 16) resets registers; value shown is added to full-scale outputs at red, green, and blue outputs. $\overline{\text{Reference White}}$ and $\overline{\text{Composite Blanking}}$ should not be operated simultaneously.
[5]$\overline{\text{Green Sync}}$ control signal (@ Pin 23) affects only Green Output (@ Pin 21); value shown is added to Green Output established by Green digital inputs (and by $\overline{\text{Composite Blanking}}$ if digital "0" is simultaneously applied to Pin 16).
[6]Logic "0" digital inputs applied to D/A under test; full scale step function "toggling" applied to active D/A.
[7]Power supplies should have less than 10mV p-p ripple.
[8]Maximum junction temperature = 150°C.
Specifications subject to change without notice.

3

THEORY OF OPERATION

Refer to the Block Diagram of the AD9702 D/A Converter.

The digital inputs are applied through TTL/ECL converters to registers within the AD9702; the purpose of the registers is to eliminate time skew from the inputs and help reduce glitch impulse in the output signals. The switching of the inputs through the registers to the three internal D/A converters is controlled by the Strobe, $\overline{\text{Green Sync}}$, $\overline{\text{Reference White}}$, and $\overline{\text{Composite Blanking}}$ signals.

When operating with ECL-compatible logic, V_{EE} (−5.2V) is applied to Pin 17 and Pin 10 is connected to ground. Under these conditions, the TTL/ECL converters at the input are transparent to incoming signals and the signals are applied directly to the registers. Regardless of the logic levels of the digital inputs, the registers and control logic internal to the AD9702 are operated at ECL levels to help assure maximum switching speed and minimum glitch on the analog outputs.

For TTL logic, V_{CC} (+5V) is applied to Pin 10 and −5.2V is applied to Pin 17. The positive voltage is used only on the TTL/ECL converters, and adds to the flexibility of the AD9702 by allowing it to be compatible with both forms of logic generally encountered in graphics displays.

There is an alternate method of operating with TTL logic without a need for −5.2V supplies. In this arrangement, Pins 10, 19, and 24 are connected to +5V; and Pin 17 is grounded. In addition, digital inputs (RGB Bits 1 – 4) are connected to +5V through 2k resistors on each input line.

The disadvantage of this technique is that the output is referenced to the +5V supply instead of ground. When this happens, the dc component of the output may exceed the general requirements of RS-170 and RS-343. In addition, any noise which is on the power supply can be coupled directly onto the video signal.

One method of overcoming these potential problems is illustrated in Figure 1, Using AD9702 in TTL Mode.

In this arrangement, the strobe signal is attenuated and shifted positively by a resistor network to minimize feedthrough of the clock signal. The digital input signals do not require the same kind of attenuation because their larger TTL swings do not present any problems.

The pull-up resistors which are used on the inputs help assure proper digital "1" logic levels regardless of which TTL logic family is used.

The PNP level shifter shown at the analog output in Figure 1 eliminates the possible problems of TTL operation cited above. Most of the noise which might be present on the +5V supply is cancelled by common mode rejection in this circuit; and level shifting helps insure the dc component of the output meets video standards.

Minor linearity degradation and temperature drift which might be introduced by the level shifter are not discernible on most video displays. The level shifter circuit is repeated three times for the Red, Green, and Blue analog outputs of the AD9702.

As shown in the block diagram and discussed in the Specifications section, a digital "0" level of the $\overline{\text{Reference White}}$ signal (at Pin 1) is used to set the registers within the converter. This action causes the three (RGB) analog outputs to go to zero output.

The $\overline{\text{Composite Blanking}}$ signal is applied to Pin 16; when a digital "0" level is used, it resets the registers and causes the three analog outputs to be −17.4mA or −653mV because of the amount added to the normal full-scale outputs.

The $\overline{\text{Green Sync}}$ signal at Pin 23 has an effect only on the Green Output of the AD9702 (at Pin 21). When this control and $\overline{\text{Composite Blanking}}$ are at a digital "0" level, the value of the Green analog output will be −25mA or −938mV.

When control inputs $\overline{\text{Reference White}}$, $\overline{\text{Composite Blanking}}$, and $\overline{\text{Green Sync}}$ are at digital "1" levels, the RGB analog outputs at Pins 22, 21, and 18 will be a function of their corresponding

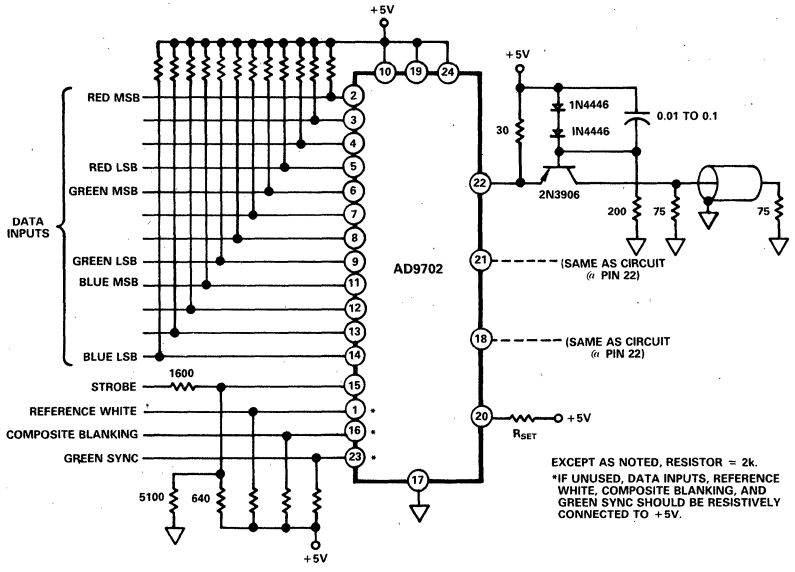


Figure 1. Using AD9702 in TTL Mode (Single Supply)

digital inputs. This is the "normal operation" referred to in the Specifications Table.

Resistor R_{SET} is connected between Pin 20, Current Set, and ground to establish the Gray Scale (GS) value of the RGB outputs. The value to be used is based on the desired full-scale GS output and the following equations:

$$I_{GS} = 5 \times I_{SET}$$

$$R_{SET} = \frac{4.4}{I_{SET}}$$

$$V_{OUT} = \frac{22 \times R_{LOAD}}{R_{SET}}$$

When using these equations, typical values of I_{SET} and V_{OUT} (Gray Scale output) will be within ±5%.

The idealized green analog output is illustrated in Figure 1.

The red and blue analog outputs are similar to the waveform shown in Figure 1, with the exception no sync portion is present on the Red and Blue outputs.

Sync control inputs are not required for Red and Blue outputs because of the RGB signals being synchronized within the AD9702. The majority of applications for the AD9702 in graphics displays use the green sync as the synchronizing signal for the monitor.

ORDERING INFORMATION

The standard AD9702 triple four-bit D/A converter is supplied in hermetic and non-hermetic units. Both versions operate over a case temperature range of −25°C to +85°C. The hermetically-sealed ceramic DIP configuration is model number AD9702BD; the non-hermetic unit is AD9702BW. For special applications or units for military applications, contact the factory for details.

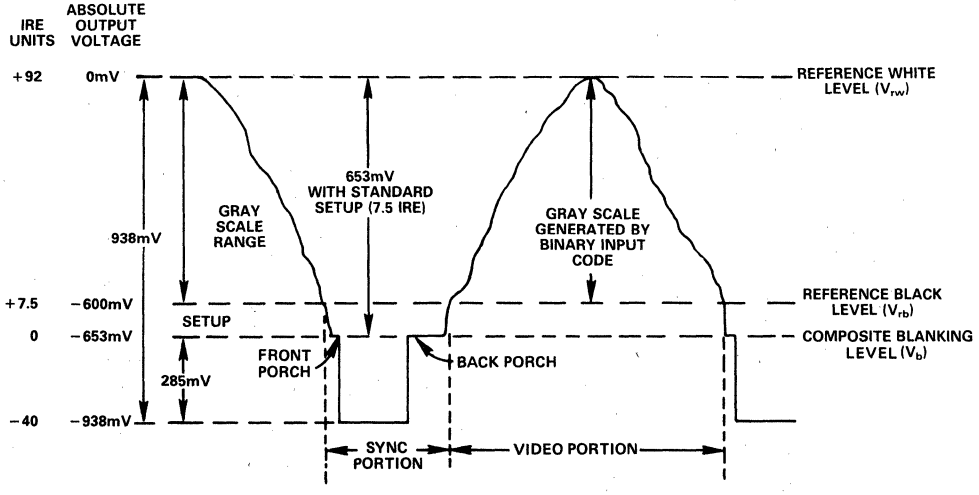


Figure 2. Idealize Green Output Waveform

ANALOG DEVICES

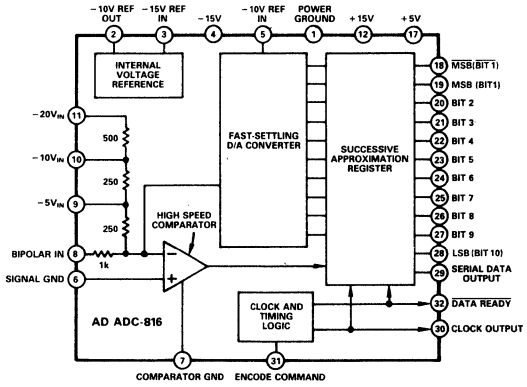
Ultra High-Speed 10-Bit A/D Converters

AD ADC-816

FEATURES
10-Bit Resolution
800ns Conversion Time
Six Input Ranges
Unipolar and Bipolar Operation

APPLICATIONS
Data Acquisition Systems
Radar Systems
Analytical Instruments
Real-Time Waveform Analysis

AD ADC-816 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD ADC-816 A/D Converter is an ultra high-speed successive approximation converter capable of 10 bits of resolution with a conversion time of only 800ns.

It is a thin-film hybrid, hermetically packaged in a 32-pin DIP. Three models span temperature ranges of 0 to +70°C, −25°C to +85°C, and −55°C to +125°C.

The design offers the user flexibility in both input and output configurations. Six different analog inputs are available with strap options: 0V to −5V; 0V to −10V; 0V to −20V; ±2.5V; ±5V; and ±10V. Output data are available in either serial or parallel format, also with external connections.

The AD ADC-816 can be incorporated into a wide variety of circuit and system applications with a minimum of external components and design effort. When used with the HTC-0300, HTC-0300A, HTC-0500, or other Analog Devices' high-performance track-and-hold units, the AD ADC-816 A/D can be a cost-effective solution for a broad range of digitizing problems.

Model number suffixes designate the various temperature ranges. The AD ADC-816KD operates over a range of 0 to +70°C; the AD ADC-816BD is for −25°C to +85°C; and the AD ADC-816SD is for use in operating environments between −55°C and +125°C.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER GROUND	17	+5V POWER
2	−10V REFERENCE OUT	18	$\overline{\text{MSB}}$ ($\overline{\text{BIT 1}}$)
3	−15V REFERENCE IN	19	MSB (BIT 1)
4	−15V POWER	20	BIT 2
5	−10V REFERENCE IN	21	BIT 3
6	SIGNAL GROUND	22	BIT 4
7	COMPARATOR GROUND	23	BIT 5
8	BIPOLAR INPUT	24	BIT 6
9	−5V ANALOG INPUT	25	BIT 7
10	−10V ANALOG INPUT	26	BIT 8
11	−20V ANALOG INPUT	27	BIT 9
12	+15V POWER	28	LSB (BIT 10)
13	NC	29	SERIAL DATA OUT
14	NC	30	CLOCK OUTPUT
15	NC	31	ENCODE COMMAND
16	NC	32	$\overline{\text{DATA READY}}$ OUTPUT

POWER GROUND (PIN 1), SIGNAL GROUND (PIN 6), AND COMPARATOR GROUND (PIN 7) MUST BE CONNECTED TOGETHER AND TO LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical at +25°C with nominal power supplies, unless otherwise noted)

Parameter	Units	AD ADC-816KD	AD ADC-816BD	AD ADC-816SD
RESOLUTION (FS = Full Scale)	Bits	10	*	*
	%FS	0.1	*	*
LSB WEIGHT				
5V p-p FS	mV	4.88	*	*
10V p-p FS	mV	9.76	*	*
20V p-p FS	mV	19.53	*	*
ACCURACY				
Nonlinearity	LSB, max	±1/2	*	*
Differential Nonlinearity	LSB, max	±1/2	*	*
Monotonicity		Guaranteed	*	*
Nonlinearity Over Operating Temperature Range	LSB	1/2	*	<1
DYNAMIC CHARACTERISTICS				
Conversion Time	ns, max[1]	800	*	900[2]
Conversion Time Tempco	%/°C (max)	±0.06 (0.07)	*	*
INPUT CHARACTERISTICS				
Analog Voltage Ranges				
Unipolar[3]				
Input Pin 9	V, p-p FS	5	*	*
Input Pin 10	V, p-p FS	10	*	*
Input Pin 11	V, p-p FS	20	*	*
Bipolar				
Inputs Pins 8 and 9	V, p-p FS	±2.5	*	*
Inputs Pins 8 and 10	V, p-p FS	±5	*	*
Inputs Pins 8 and 11	V, p-p FS	±10	*	*
−10V Reference Input (Pin 5)	V (max)	−10 (±0.2)	*	*
Impedance				
Unipolar 5V Input	Ω	250	*	*
Unipolar 10V Input	Ω	500	*	*
Unipolar 20V Input	Ω	1000	*	*
Bipolar Input	Ω	1000	*	*
Reference	Ω	2000	*	*
Gain Error Before Adjustment				
Unipolar	% of FS	0.3	*	*
Bipolar	% of FS	0.2	*	*
Gain Error vs. Temperature				
Unipolar	ppm/°C max	±37	*	*
Bipolar	ppm/°C max	±28	*	*
Zero Error Before Adjustment				
Unipolar	% of FS	0.2	*	*
Zero Error vs. Temperature				
Unipolar	ppm/°C max	±1/2	*	*
Offset Error Error Before Adjustment				
Bipolar	% of FS	0.1	*	*
Offset Error vs. Temperature				
Bipolar	ppm/°C max	±23	*	*
Reference Output Tempco	ppm/°C max	±20	*	*
ENCODE COMMAND INPUT[4]				
Logic Levels,	V (max)	"0" = +0.4(+0.8)	*	*
TTL-Compatible	V, min (max)	"1" = +2.0(+5.5)	*	*
Loading	TTL Loads	1	*	*
Rise and Fall Times	ns	10	*	*
Width	ns, min	40	*	*
Frequency	MHz	1.25	*	1.14
DIGITAL OUTPUT CHARACTERISTICS				
Parallel				
@ Pins 19–28 + Pin 18	Bits	11 (10 + $\overline{\text{MSB}}$)	*	*
Time Skew	ns, max	5	*	*
Format	Non-Return-to-Zero (NRZ)		*	*
Series				
@ Pin 29	Bits	11 (10 + $\overline{\text{MSB}}$)	*	*
Timing	Successive decision pulses with MSB (or $\overline{\text{MSB}}$) first; at internal clock frequency		*	*
Format	Non-Return-to-Zero (NRZ)		*	*
Coding[5]				
Unipolar Input	Binary (BIN)		*	*
Bipolar Input	Offset Binary (OBN) or 2's Complement (2SC)[6]		*	*
Logic Levels,	V, max	"0" = +0.4	*	*
TTL-Compatible	V, min	"1" = +2.4	*	*
Loading	TTL Loads	2	*	*

Parameter	Units	AD ADC-816KD	AD ADC-816BD	AD ADC-816SD
CLOCK OUTPUT				
Format		Series Train	*	*
Amplitude				
Minimum/Maximum	V	0/+5	*	*
Width	ns (min)	25 (20)	*	*
Frequency	MHz	14.3	*	*
REFERENCE OUTPUT[7]				
Voltage	V (max)	10 (±0.02)	*	*
Current (sink only)	mA	0 to +20	*	*
Impedance	Ohms, max	10	*	*
DATA READY OUTPUT				
Signal Status	Logic "1" during reset and conversion		*	
	Logic "0" when conversion is complete		*	*
Logic Levels,	V, max	"0" = +0.4	*	*
TTL-Compatible	V, min	"1" = +2.4	*	*
Loading	TTL Loads	4	*	*
Rise and Fall Times	ns, max	5	*	*
POWER REQUIREMENTS[8]				
+15V ±2% (Pin 12, Power)	mA, max	105	*	*
−15V ±3% (Pin 4, Power)	mA, max	25	*	*
−15V ±3% (Pin 3, Reference)	mA, max	35	*	*
+5V ±5% (Pin 17)	mA, max	180	*	*
Power Consumption[9]	W, max	2.9	*	*
Power Supply Rejection Ratio				
(PSSR) for Rated Supplies	LSB, max	1/2	*	
TEMPERATURE RANGE				
Operating[10]	°C	0 to +70	−25 to +85	−55 to +125
Storage	°C	−65 to +150	*	*
THERMAL RESISTANCE[11]				
Junction to Air, θja				
(Free Air)	°C/W	32	*	*
Junction to Case, θjc	°C/W	13	*	*
MTBF[12]				
Mean Time Between Failures	Hours			1.65×10^5

NOTES
[1]Measured from leading edge Encode Command to trailing edge $\overline{\text{Data Ready}}$; use trailing edge to strobe output data into external circuits.
[2]AD ADC-816SD maximum conversion time shown is at full operating temperature.
[3]Bipolar input (Pin 8) must be tied to ground.
[4]Logic "1" resets converter; logic "0" initiates conversion.
[5]All coding is inverted analog.
[6]Two's Complement available for parallel output only.
[7]To use internal reference, connect −15V REFERENCE IN (Pin 3) to −15V POWER (Pin 4); and −10V REFERENCE OUT (Pin 2) to −10V REFERENCE IN (Pin 5). To use external reference, leave Pins 2 and 3 open or grounded; connect external reference to Pin 5. If Pin 3 is left open or grounded, internal reference is disabled and power decreases approximately 200mW.
[8]Bypass power supplies with 1μF electrolytic capacitors and 0.1μF ceramic capacitors as close to supply pins as possible.
[9]Power dissipation shown is based on 0V analog input.
[10]Minimum air flow of 400 linear feet per minute (LFPM) is recommended for operating temperatures above +70°C. At elevated temperatures, unit should be mounted directly to printed circuit board (PCB) without a socket; good thermal contact must be maintained between bottom of device and PCB.
[11]Maximum junction temperature is +150°C.
[12]Calculated for "SD" version using MIL-HNBK 217; Ground Fixed; +70°C case temperature.
*Specifications same as AD ADC-816KD.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Positive Supply (Pin 12)	+16V dc
Negative Supply (Pins 3 & 4)	−16V dc
Logic Supply (Pin 17)	+7V dc
Logic Inputs	+7V dc
Analog Inputs	±2 × Selected Analog Input Range

UNIPOLAR OPERATION

ANALOG INPUT			DIGITAL OUTPUT
0 to −20V	0 to −10V	0 to −5V	MSB LSB
−19.9805	−9.9902	−4.9951	1 111 111 111
−17.5000	−8.7500	−4.3750	1 110 000 000
−15.0000	−7.5000	−3.7500	1 100 000 000
−10.0000	−5.0000	−2.5000	1 000 000 000
−5.0000	−2.5000	−1.2500	0 100 000 000
−2.5000	−1.2500	−0.6250	0 010 000 000
−0.0198	−0.0098	−0.0049	0 000 000 001
0.0000	0.0000	0.0000	0 000 000 000

BIPOLAR OPERATION

ANALOG INPUT			DIGITAL OUTPUT	
			Offset Binary	2's Complement
±10V	±5V	±2.5V	MSB LSB	$\overline{\text{MSB}}$ LSB
−9.9805	−4.9902	−2.4951	1 111 111 111	0 111 111 111
−7.5000	−3.7500	−1.8750	1 110 000 000	0 110 000 000
−5.0000	−2.5000	−1.2500	1 100 000 000	0 100 000 000
0.0000	0.0000	0.0000	1 000 000 000	0 000 000 000
+5.0000	+2.5000	+1.2500	0 100 000 000	1 100 000 000
+7.5000	+3.7500	+1.8750	0 010 000 000	1 010 000 000
+9.9805	+4.9902	+2.4951	0 000 000 001	1 000 000 001
+10.0000	+5.0000	+2.5000	0 000 000 000	1 000 000 000

AD ADC-816 Coding Tables

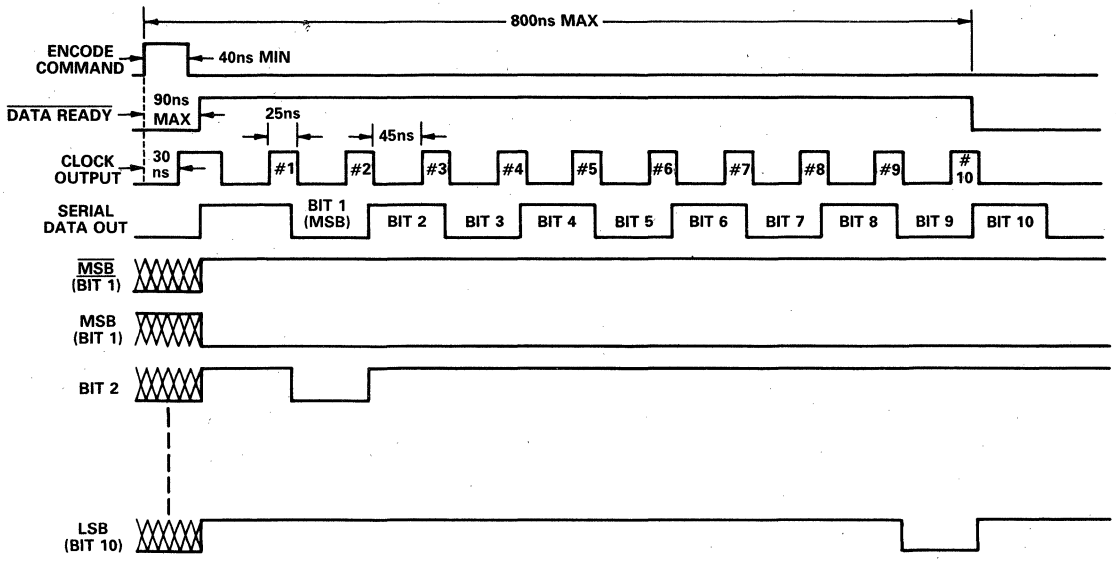


Figure 1. AD ADC-816KD/BD Timing Diagram

AD ADC-816 TIMING

Refer to Figure 1, AD ADC-816KD/BD Timing Diagram.

As shown elsewhere in this data sheet, operating temperatures for the AD ADC-816KD and AD ADC-816BD are 0 to +70°C and −25°C to +85°C, respectively. The operating temperature for the AD ADC-816SD is −55°C to +125°C. These differences in temperature cause slight differences in timing among the three models of converters, but all times are referenced to the leading edge of the ENCODE COMMAND pulse supplied by the user.

For the AD ADC-816SD, the maximum time of 800ns shown to the falling edge of the DATA READY pulse is 900ns; these intervals are the maximum times if operating at the maximum word rate, with an encode command no wider than 70ns. In addition to this change in conversion time, spacing between CLOCK OUTOUT pulses increases from a typical 45ns to 55ns.

Figure 1 illustrates timing intervals for the KD and BD devices. In the diagram, ENCODE COMMAND width is 45ns, and this becomes the width of the set-up pulse which occurs before clock pulse #1.

The serial output data are in NRZ format with the MSB appearing first, and are synchronized by using the CLOCK OUTPUT pulses at Pin 30. The trailing (negative-going) edge of each clock pulse is recommended for use as a strobe to clock out its associated bit information.

Delaying the clock pulses 15ns-20ns before using them as strobes will help assure sufficient set-up time for the serial data output to stabilize. For users who prefer positive-edge triggering, the clock pulses can be inverted via additional logic circuits and the trailing edges of those pulses could still be used as strobes.

Input connections for the AD ADC-816 are shown in Figure 2 (Unipolar Operation) and Figure 3 (Bipolar Operation).

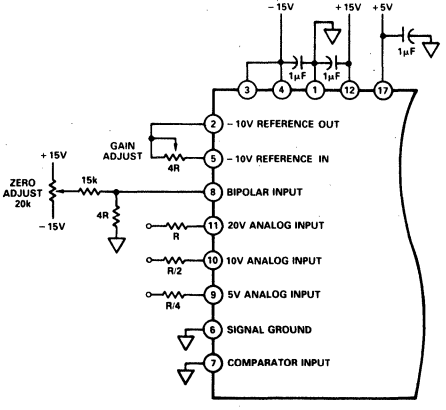


Figure 2. Unipolar Operation

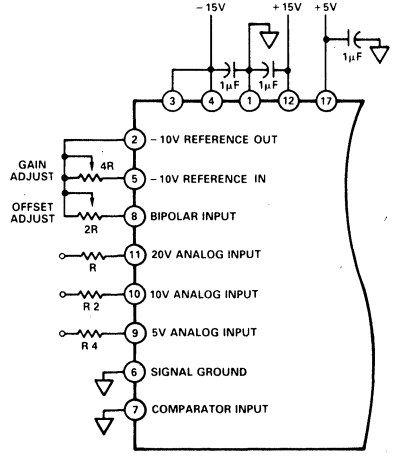


Figure 3. Bipolar Operation

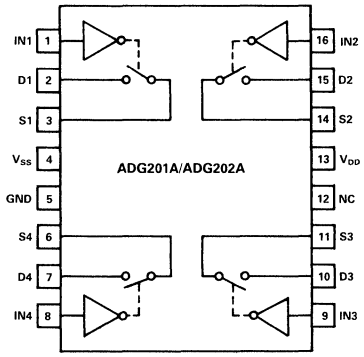
ANALOG DEVICES

CMOS Quad SPST Switches

ADG201A/ADG202A

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω)
Low Leakage (0.5nA)
Low Power Dissipation (45mW)
TTL/CMOS Compatible
Superior Second Source:
ADG201A Replaces DG201A, HI-201
ADG202A Replaces DG202

ADG201A/ADG202A PIN CONFIGURATION
(TOP VIEW)



3

GENERAL DESCRIPTION

The ADG201A and ADG202A are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC^2MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG201A and ADG202A consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

ADG201A IN	ADG202A IN	SWITCH CONDITION
0	1	ON
1	0	OFF

Table I. Truth Table

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. Extended Signal Range:
   These switches are fabricated on an enhanced LC^2MOS process, resulting in high breakdown and an increased analog signal range of ±15V.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted)

Parameter	ADG201AKN ADG202AKN 25°C	ADG201AKN ADG202AKN 0 to +70°C	ADG201ABQ ADG202ABQ 25°C	ADG201ABQ ADG202ABQ −25°C to +85°C	ADG201ATQ ADG202ATQ 25°C	ADG201ATQ ADG202ATQ −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}[1]	60		60		60		Ω typ	−10V<V_S<+10V
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA
								Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)[1]	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S ∓14V; Test Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)[1]	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)[1]	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}[1] High Threshold		2.4		2.4		2.4	V min	
V_{INL}[1] Low Threshold		0.8		0.8		0.8	V max	
I_{INL}[1] or I_{INH}[1]		1		1		1	μA min	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[2]	300		300		300		ns max	Test Circuit 4
t_{OFF}[2]	250		250		250		ns max	
OFF Isolation	80		80		80		dB typ	V_S = 2V(p-p); f = 100kHz
								R_L = 1kΩ; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_{DS} (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V
								Test Circuit 5
POWER SUPPLY								
I_{DD}	0.5		0.5		0.5		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}[1]		2		2		2	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}[1]		0.2		0.2		0.2	mA max	
Power Dissipation		45		45		45	mW max	

NOTES
[1]Max rating is 100% tested.
[2]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to V_{SS}	44V
V_{DD} to GND	25V
V_{SS} to GND	−25V
Analog Inputs[1]	
Voltage at S, D	V_{SS} to V_{DD}
Continuous Current, S or D	30mA
Pulsed Current S or D	
1ms Duration, 10% Duty Cycle	70mA
Digital Inputs[1]	
Voltage at IN	V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First
Power Dissipation (Package)	
Plastic DIP	
Up to +75°C	470mW
Cerdip	
Up to +75°C	900mW/°C
Derates above +75°C by	12mW/°C
Operating Temperature	
Plastic (KN Version)	0 to +70°C
Cerdip (BQ Version)	−25°C to +85°C
Cerdip (TQ Version)	−55°C to +125°C

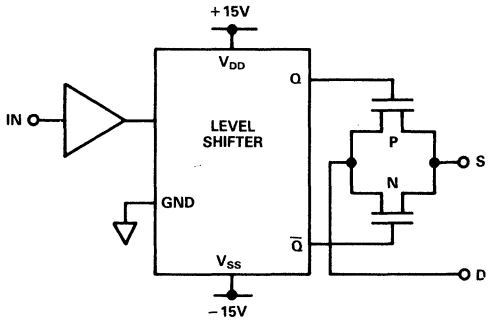
NOTE
[1]Overvoltage at IN, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ADG201A/ADG202A FUNCTIONAL DIAGRAM



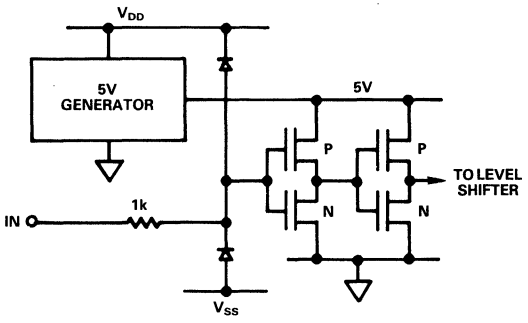


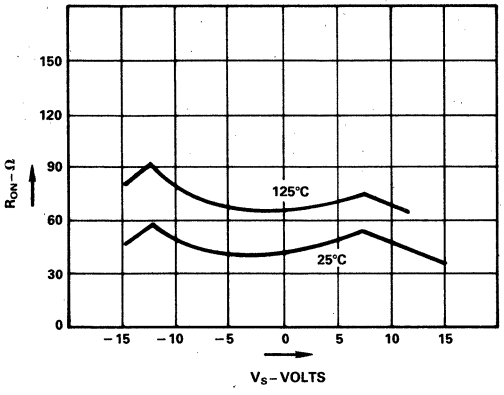
Figure 1. Typical Digital Input Cell

ORDERING INFORMATION[1]

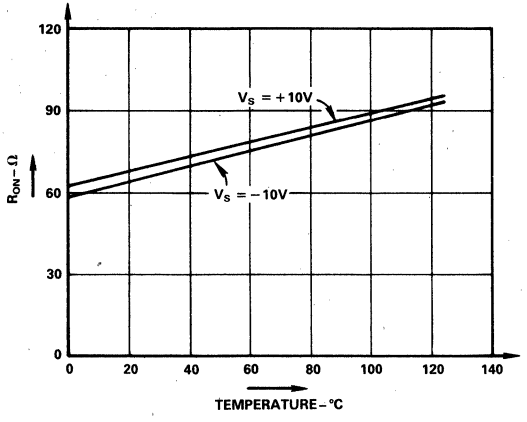
Plastic 0 to +70°C	Cerdip[2] −25°C to +85°C	Cerdip[2] −55°C to +125°C
ADG201AKN	ADG201ABQ	ADG201ATQ
ADG202AKN	ADG202ABQ	ADG202ATQ

NOTES
[1]For information regarding /883B versions, contact your local Analog Devices Sales Office for Military Data Sheet.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

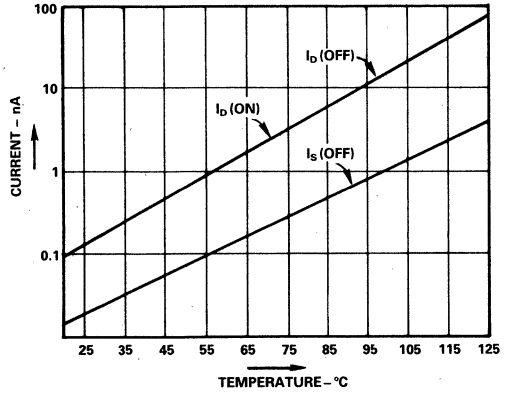
Typical Performance Characteristics



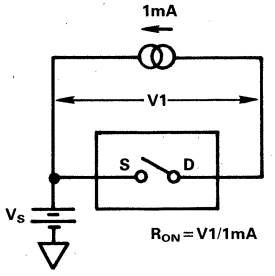
R_{ON} as a Function of V_D (V_S)



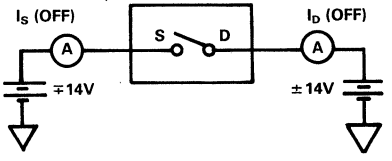
R_{ON} as a Function of Temperature



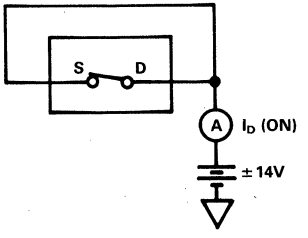
Leakage Current as a Function of Temperature



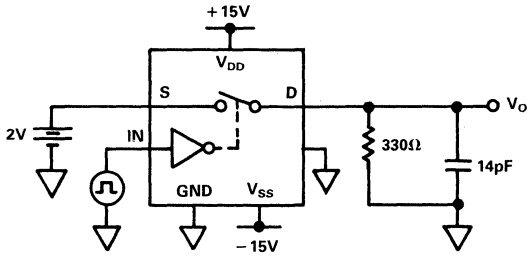
Test Circuit 1

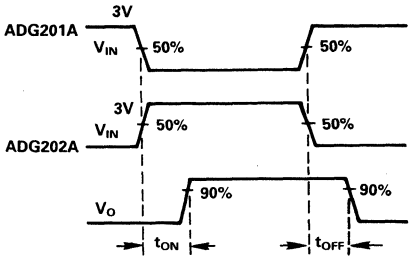


Test Circuit 2

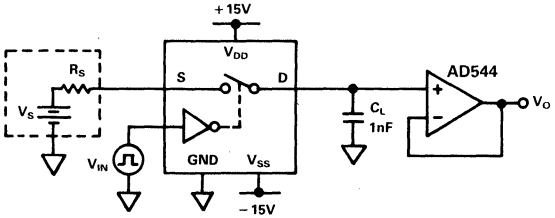


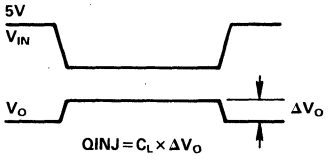
Test Circuit 3



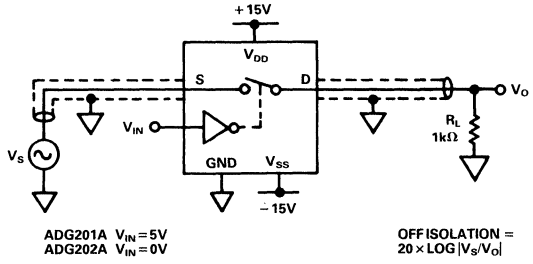


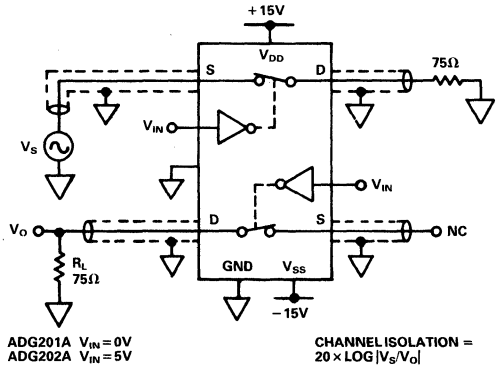
Test Circuit 4





Test Circuit 5. Charge Injection





Test Circuit 6. Off Isolation

Test Circuit 7. Channel to Channel Isolation

TERMINOLOGY

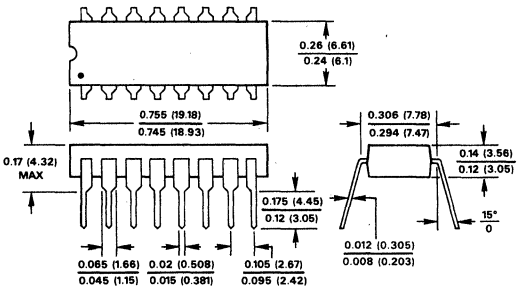
R_{ON}	Ohmic resistance between terminals OUT and S
R_{ON} Match	Difference between the R_{ON} of any two channels
I_S (OFF)	Source terminal leakage current when the switch is off
I_D (OFF)	OUT terminal leakage current when the switch is off
I_D (ON)	Leakage current that flows from the closed switch into the body
V_D (V_S)	Analog voltage on terminal D, S
C_S (OFF)	Switch input capacitance "OFF" condition
C_D (OFF)	Switch output capacitance "OFF" condition
C_{IN}	Digital input capacitance
C_{DS} (ON)	Input to output capacitance when the switch is on
t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
V_{INL}	Threshold voltage for low state
V_{INH}	Threshold voltage for high state
I_{INL} (I_{INH})	Input current of the digital input
V_{DD}	Most positive voltage supply
V_{SS}	Most negative voltage supply
I_{DD}	Positive supply current
I_{SS}	Negative supply current

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

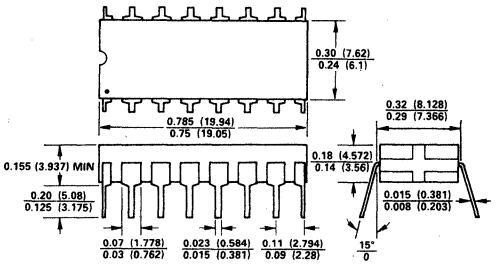
Dimensions shown in inches and (mm).

16-PIN PLASTIC (SUFFIX N)

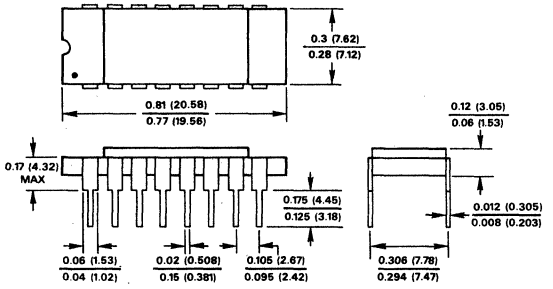


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERDIP (SUFFIX Q)



16-PIN CERAMIC DIP[1]



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M38510 REQUIREMENTS

NOTE
[1]ANALOG DEVICES RESERVES THE RIGHT TO SHIP CERAMIC PACKAGES IN LIEU OF CERDIP PACKAGES.

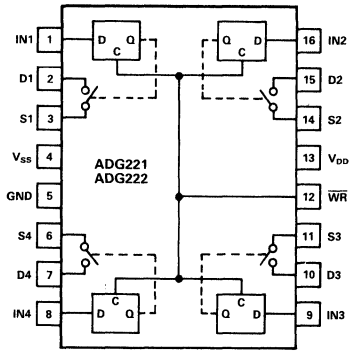
ANALOG DEVICES

CMOS Quad SPST Switches

ADG221/ADG222

FEATURES
44V Supply Maximum Rating
±15V Analog Signal Range
Low R_{ON} (60Ω)
Low Leakage (0.5nA)
Low Power Dissipation (37.5mW)
µP, TTL, CMOS Compatible
Superior DG221 Replacement

ADG221/ADG222 PIN CONFIGURATION
(TOP VIEW)



GENERAL DESCRIPTION

The ADG221 and ADG222 are monolithic CMOS devices comprising four independently selectable switches. On-chip latches facilitate microprocessor interfacing. They are designed on an enhanced LC²MOS process which gives an increased signal handling capability of ±15V. These switches also feature high switching speeds and low R_{ON}.

The ADG221 and ADG222 consist of four SPST switches. They differ only in that the digital control logic is inverted. All devices exhibit break before make switching action. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

$\overline{WR}$	ADG221 IN	ADG222 IN	SWITCH CONDITION
0	0	1	ON
0	1	0	OFF
1	X	X	Retains Previous Switch Condition

Table I. Truth Table

PRELIMINARY TECHNICAL DATA

PRODUCT HIGHLIGHTS

1. Easily Interfaced:
   Digital inputs are latched with a $\overline{WR}$ signal for microprocessor interfacing. A 5V regulated supply is internally generated permitting wider tolerances on the supplies without affecting the TTL digital input switching levels.
2. Single Supply Operation:
   For applications where the analog signal is unipolar (0V to 15V), the switches can be operated from a single +15V supply.
3. Low Leakage:
   Leakage currents in the range of 500pA make these switches suitable for high precision circuits. The added feature of Break before Make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted)

Parameter	ADG221KN ADG222KN 25°C	ADG221KN ADG222KN 0 to +70°C	ADG221BQ ADG222BQ 25°C	ADG221BQ ADG222BQ −25°C to +85°C	ADG221TQ ADG222TQ 25°C	ADG221TQ ADG222TQ −55°C to +125°C	Units	Test Conditions
ANALOG SWITCH								
Analog Signal Range	±15	±15	±15	±15	±15	±15	Volts	
R_{ON}[1]	60		60		60		Ω typ	−10V<V_S<+10V
	90	145	90	145	90	145	Ω max	I_{DS} = 1.0mA Test Circuit 1
R_{ON} vs. V_D (V_S)	20		20		20		% typ	
R_{ON} Drift	0.5		0.5		0.5		%/°C typ	
R_{ON} Match	5		5		5		% typ	V_S = 0V, I_{DS} = 1mA
I_S (OFF)[1]	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S ∓14V; Circuit 2
OFF Input Leakage	2	100	2	100	1	100	nA max	
I_D (OFF)[1]	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 2
OFF Output Leakage	2	100	2	100	1	100	nA max	
I_D (ON)[1]	0.5		0.5		0.5		nA typ	V_D = ±14V; V_S = ∓14V; Test Circuit 3
ON Channel Leakage	2	200	2	200	1	200	nA max	
DIGITAL CONTROL								
V_{INH}[1] High Threshold		2.4		2.4		2.4	V min	
V_{INL}[1] Low Threshold		0.8		0.8		0.8	V max	
I_{INL}[1] or I_{INH}[1]		1		1		1	μA max	
DYNAMIC CHARACTERISTICS								
t_{OPEN}	30		30		30		ns typ	
t_{ON}[2]	300		300		300		ns max	Test Circuit 4
t_{OFF}[2]	250		250		250		ns max	
t_W[2] Write Pulse Width		100		100		100	ns min	See Figure 2
t_S[2] Digital Input Setup Time		100		100		100	ns min	See Figure 2
t_H[2] Digital Input Hold Time		0		0		0	ns min	See Figure 2
OFF Isolation	80		80		80		dB typ	V_S = 2V (p-p); f = 100kHz R_L = 1kΩ; Test Circuit 6
Channel-to-Channel Crosstalk	80		80		80		dB typ	Test Circuit 7
C_S (OFF)	5		5		5		pF typ	
C_D (OFF)	5		5		5		pF typ	
C_{DS} (ON)	16		16		16		pF typ	
C_{IN} Digital Input Capacitance	5		5		5		pF typ	
Q_{INJ} Charge Injection	20		20		20		pC typ	R_S = 0Ω; C_L = 1000pF; V_S = 0V Test Circuit 5
POWER SUPPLY								
I_{DD}	0.5		0.5		0.5		mA typ	Digital Inputs = V_{INL} or V_{INH}
I_{DD}[1]		1.5		1.5		1.5	mA max	
I_{SS}	0.1		0.1		0.1		mA typ	
I_{SS}[1]		0.2		0.2		0.2	mA max	
Power Dissipation		37.5		37.5		37.5	mW max	

NOTES
[1]Max rating is 100% tested.
[2]Sample tested at 25°C to ensure compliance.
t_{ON}, t_{OFF} are the same for both IN and $\overline{WR}$ digital input changes.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to V_{SS} 44V
V_{DD} to GND 25V
V_{SS} to GND . . . . . −25V
Analog Inputs[1]
  Voltage at S, D . . . . . V_{SS} to V_{DD}
  Continuous Current, S or D 30mA
  Pulsed Current S or D
    1ms Duration, 10% Duty Cycle 70mA
Digital Inputs[1]
  Voltage at IN, $\overline{WR}$ . . . . . V_{SS} −2V to V_{DD} +2V or 20mA, Whichever Occurs First

Power Dissipation (Package)
  Plastic DIP
    Up to +75°C 470mW
  Cerdip
    Up to +75°C . . . . . 900mW/°C
    Derates above +75°C by . . . . . 12mW/°C
Operating Temperature
  Plastic (KN Version) . . . . . 0 to +70°C
  Cerdip (BQ Version) . . . . . −25°C to +85°C
  Cerdip (TQ Version) . . . . . −55°C to +125°C

NOTE
[1]Overvoltage at IN, $\overline{WR}$, S or D will be clamped by diodes. Current should be limited to the Maximum Rating above.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

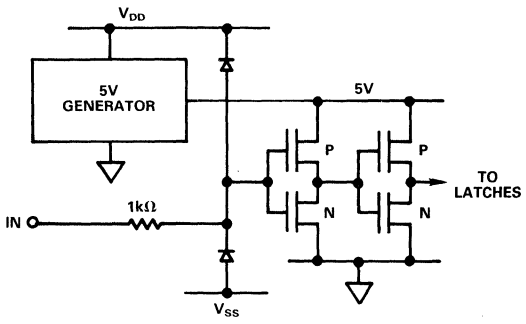


Figure 1. Typical Digital Input Cell

TIMING AND CONTROL SEQUENCE

Figure 2 shows the timing sequence for latching the switch digital inputs (IN1 – IN4). The latches are level sensitive and, therefore, while $\overline{WR}$ is held low the latches are transparent and the switches respond to the digital inputs. The digital inputs are latched on the rising edge of $\overline{WR}$.

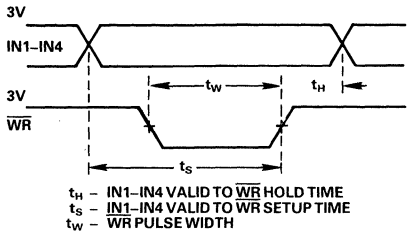


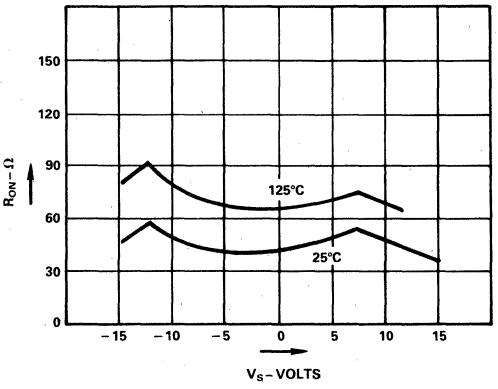
Figure 2. Timing and Control Sequence

ORDERING INFORMATION[1]

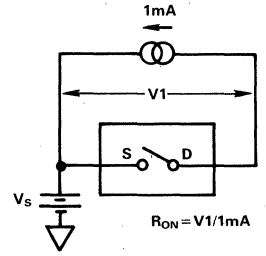
Plastic 0 to −70°C	Cerdip[2] −25°C to +85°C	Cerdip[2] −55°C to +125°C
ADG221KN	ADG221BQ	ADG221TQ
ADG222KN	ADG222BQ	ADG222TQ

NOTES
[1]For information regarding /883B versions, contact your local Analog Devices Sales Office for Military Data Sheet.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

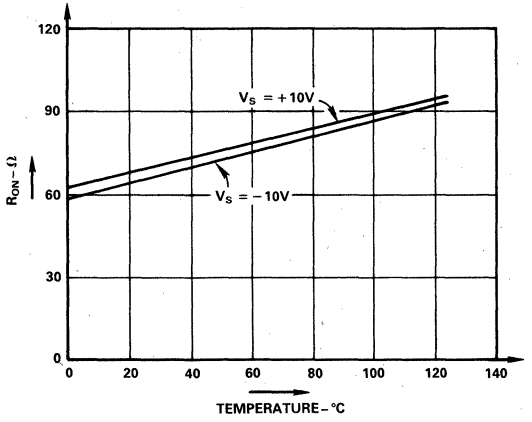
Typical Performance Characteristics



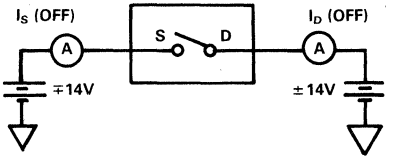
R_{ON} as a Function of V_D (V_S)



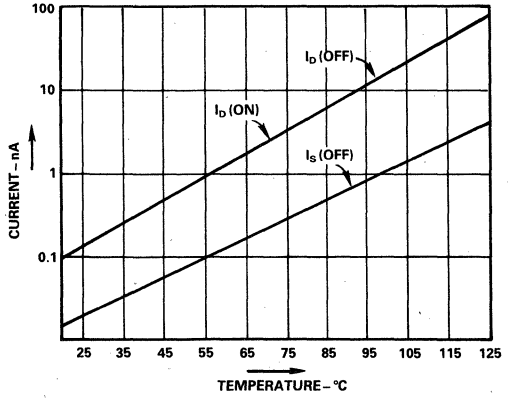
Test Circuit 1



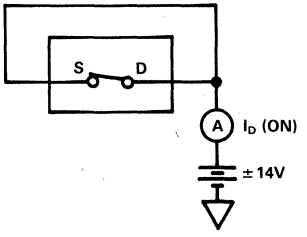
R_{ON} as a Function of Temperature



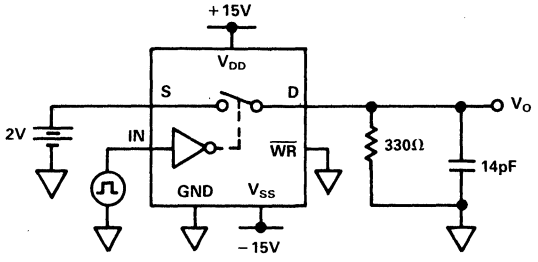
Test Circuit 2

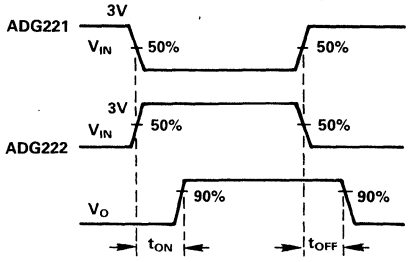


Leakage Current as a Function of Temperature

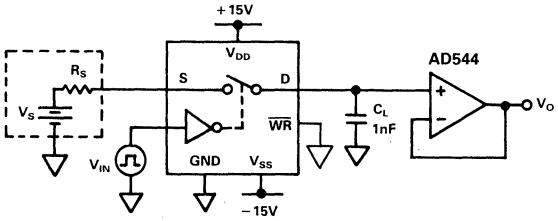


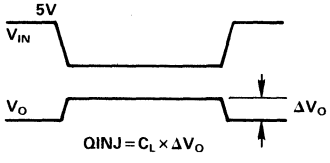
Test Circuit 3



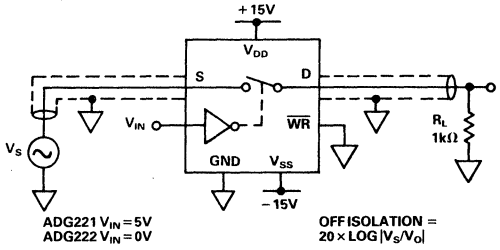


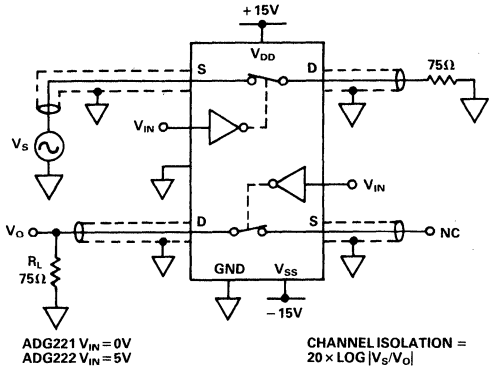
Test Circuit 4





Test Circuit 5. Charge Injection





Test Circuit 6. Off Isolation

Test Circuit 7. Channel to Channel Isolation

TERMINOLOGY

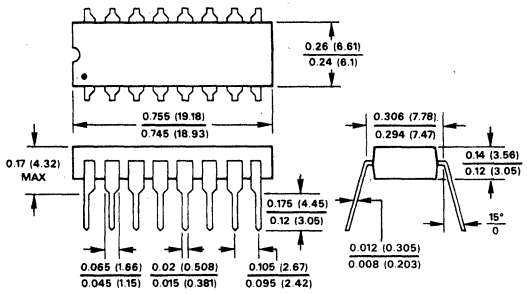
R_{ON}	Ohmic resistance between terminals OUT and S	t_{ON}	Delay time between the 50% and 90% points of the digital input and switch "ON" condition
R_{ON} Match	Difference between the R_{ON} of any two channels	t_{OFF}	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition
I_S (OFF)	Source terminal leakage current when the switch is off	t_{OPEN}	"OFF" time measured between 50% points of both switches when switching from one address state to another
I_D (OFF)	OUT terminal leakage current when the switch is off	V_{INL}	Threshold voltage for low state
I_D (ON)	Leakage current that flows from the closed switch into the body	V_{INH}	Threshold voltage for high state
V_D (V_S)	Analog voltage on terminal D, S	I_{INL} (I_{INH})	Input current of the digital input
C_S (OFF)	Switch input capacitance "OFF" condition	V_{DD}	Most positive voltage supply
C_D (OFF)	Switch output capacitance "OFF" condition	V_{SS}	Most negative voltage supply
C_{IN}	Digital input capacitance	I_{DD}	Positive supply current
C_{DS} (ON)	Input to output capacitance when the switch is on	I_{SS}	Negative supply current

MECHANICAL INFORMATION

OUTLINE DIMENSIONS

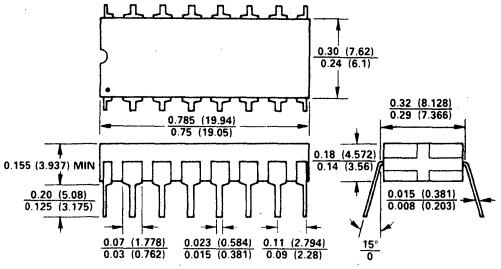
Dimensions shown in inches and (mm).

16-PIN PLASTIC (SUFFIX N)

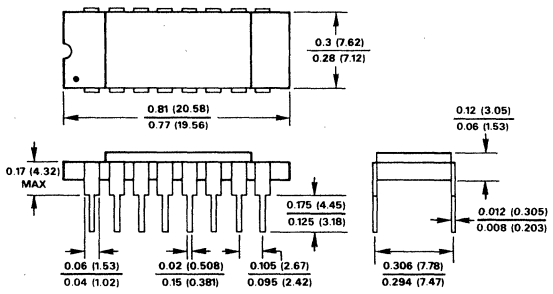


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERDIP (SUFFIX Q)



16-PIN CERAMIC DIP[1]



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M38510 REQUIREMENTS

NOTE
[1]ANALOG DEVICES RESERVES THE RIGHT TO SHIP CERAMIC PACKAGES IN LIEU OF CERDIP PACKAGES.

ANALOG DEVICES

Ultra-Low Noise, High Speed Precision Op Amp ($A_{VCL} \geq 5$)

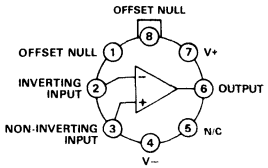
AD OP-37

FEATURES

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
High Speed: 17V/μs
High Gain Bandwidth Product: 63MHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, LH0044, 5130, 3510, 725, 714 and 741 Sockets in Gains ≥ 5
Military Grade and Plus Parts Available
8-Pin Plastic Mini-DIP, CERDIP or TO-99 Hermetic Metal Can
Available in Wafer-Trimmed Chip Form

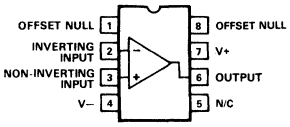
CONNECTION DIAGRAMS
(Top View)

TO-99 (H) Package



NOTE: PIN 4 CONNECTED TO CASE

Plastic Mini-DIP (N) Package and CERDIP (Q) Package



PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. High speed accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than or equal to five. This instrumenation grade op amp features industry standard dc performance; typical input offset voltages of 10μV and typical input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p (typ) of 80nV (0.1Hz to 10Hz), an e_n (typ) of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a typical 17V/μs slew rate and a typical 63MHz gain bandwidth product. Long-term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA (typ) and an input offset current of 7nA (typ). An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA (typ) and 15nA (typ), respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of 120dB.

The AD OP-37 is available in six performance grades. The AD OP-37E, AD OP-37F and AD OP-37G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-37A, AD OP-37B and AD OP-37C are specified for −55°C to +125°C operation. All devices are available in either the TO-99 hermetically-sealed metal cans or the hermetically-sealed CERDIP packages, while the industrial grades are also available in plastic Mini-DIPs.

PRODUCT HIGHLIGHTS

1. High speed accurate amplification (gains ≥ 5) of very low level low frequency voltage inputs is enhanced by a high gain bandwidth product and ultra-low input voltage noise.
2. The AD OP-37 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common-mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-37G			AD OP-37F			AD OP-37E		
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		**700**	1,300		**750**	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		**±11.4**	±13.5		**±11.7**	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	45	63		45	63		45	63	
		–	40		–	40		–	40	
Slew Rate	SR	11	17		11	17		11	17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	**140**		20	**60**
Average Drift	TCV_{OS}		0.4	1.8		0.3	**1.3**		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	**±95**		±14	**±60**
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	75		9	50		7	35
			20	135		14	85		10	50
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		**±10.5**	±11.8	
Common-Mode Rejection										
Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		**102**	121		**110**	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	**5.6**		3.0	**4.6**		3.0	**4.6**
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	**32**		2	**16**		2	**15**
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
	T_{min}, T_{max}	−25		+85	−25		+85	−25		+85
PACKAGE OPTIONS										
Plastic Mini-DIP (N8A)			AD OP-37GN			AD OP-37FN			AD OP-37EN	
CERDIP (Q8A)			AD OP-37GQ			AD OP-37FQ			AD OP-37EQ	
TO-99 (H08A)			AD OP-37GH			AD OP-37FH			AD OP 37EH	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]Long-Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

Specifications subject to change without notice.

AD OP-37C			AD OP-37B			AD OP-37A			CONDITIONS	UNITS
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
400	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
45	63		45	63		45	63		$f_o = 10kHz$	MHz
–	63		–	40		–	40		$f_o = 1MHz$	MHz
11	17		11	17		11	17		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	**1.8**		0.3	**1.3**		0.2	**0.6**	T_a = min to max	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 2)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**± 55**		±10	**±40**		nA
	±35	**±150**		±28	**± 95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	nV/√Hz
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	nV/√Hz
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	nV/√Hz
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	pA/√Hz
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	pA/√Hz
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	pA/√Hz
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		**±10.3**	±11.5		**±10.3**	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	**5.6**		3.0	**4.6**		3.0	**4.6**	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-37CQ AD OP-37CH			AD OP-37BQ AD OP-37BH			AD OP-37AQ AD OP-37AH				

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 3) . . . . . ±0.7V
Differential Input Current (Note 3) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-37A, AD OP-37B, AD OP-37C . −55°C to +125°C
AD OP-37E, AD OP-37F, AD OP-37G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
MINI-DIP (N)	36°C	5.6mW/°C
CERDIP (Q)	75°C	6.7mW/°C

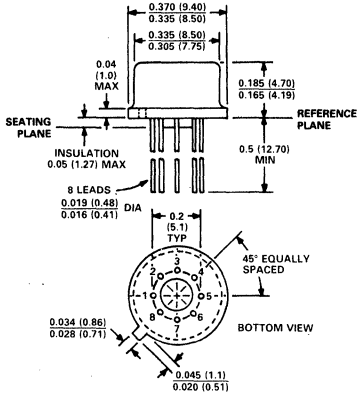
Note 2: For supply voltages less than ± 18V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: The AD OP-37's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ± 0.7V, the input current should be limited to 25mA.

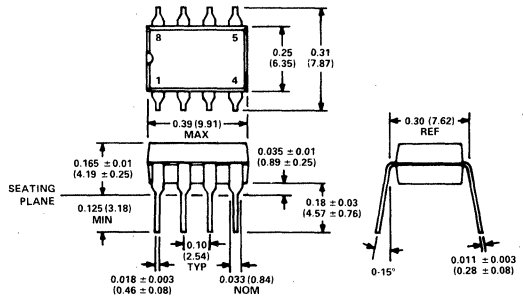
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

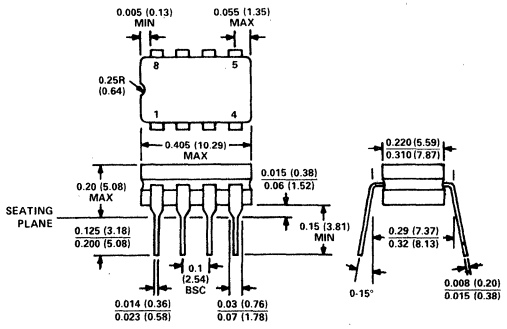
TO-99 (H) Package



MINI-DIP (N) Package

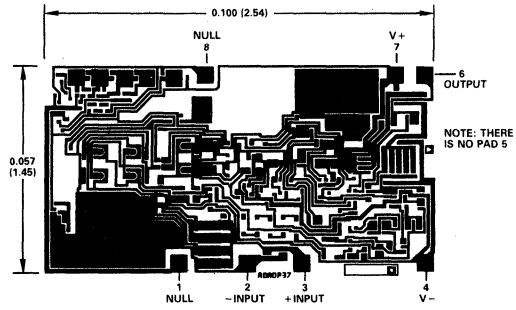


CERDIP (Q) PACKAGE



CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



THE AD OP-37 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM. CONSULT THE FACTORY FOR DETAILS.

AD OP-37 ORDERING GUIDE

Model	Package	Temperature Range (°C)	Max Initial Offset (µV)	Max Offset Drift (µV/°C)
AD OP-37GH	TO-99	−25 to +85	100	1.8
AD OP-37GN	MINI-DIP	−25 to +85	100	1.8
AD OP-37GQ	CERDIP	−25 to +85	100	1.8
AD OP-37FH	TO-99	−25 to +85	60	1.3
AD OP-37FN	MINI-DIP	−25 to +85	60	1.3
AD OP-37FQ	CERDIP	−25 to +85	60	1.3
AD OP-37EH	TO-99	−25 to +85	25	0.6
AD OP-37EN	MINI-DIP	−25 to +85	25	0.6
AD OP-37EQ	CERDIP	−25 to +85	25	0.6
AD OP-37CH	TO-99	−55 to +125	100	1.8
AD OP-37CQ	CERDIP	−55 to +125	100	1.8
AD OP-37BH	TO-99	−55 to +125	60	1.3
AD OP-37BQ	CERDIP	−55 to +125	60	1.3
AD OP-37AH	TO-99	−55 to +125	25	0.6
AD OP-37AQ	CERDIP	−55 to +125	25	0.6

APPLICATION NOTES FOR THE AD OP-37

The AD OP-37 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for correct AD OP-37 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

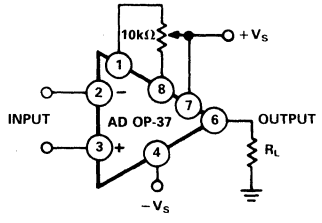


Figure 1. Optional Offset Nulling Circuit

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-37. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature.

Output stability with the AD OP-37 is possible with capacitive loads of up to 1000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor inside the feedback loop.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-37 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

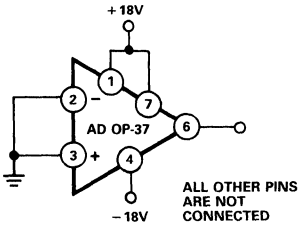


Figure 2. Burn-In Circuit

3

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-37 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

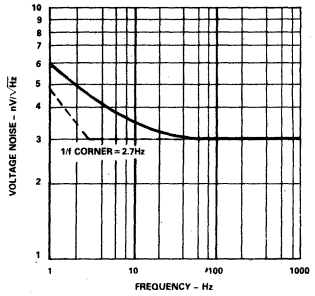
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

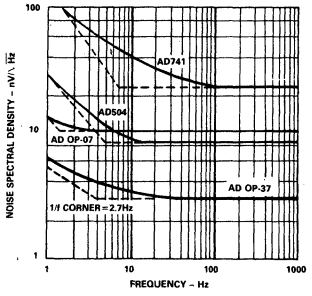
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the l/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee l/f and white noise performance over the rated frequency spectrum.

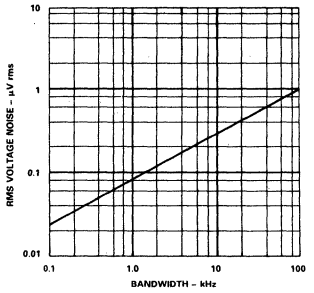
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



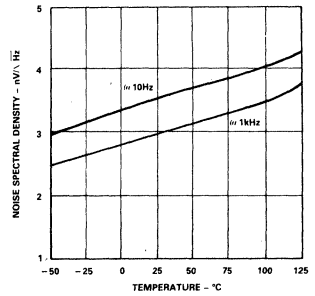
Input Voltage Noise Spectral Density



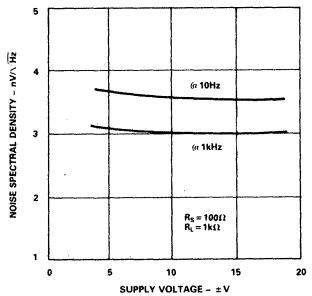
Comparison of Op Amp Input Voltage Noise Spectrums



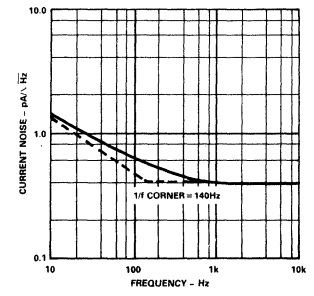
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



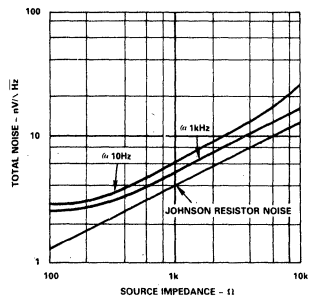
Input Voltage Nose vs. Temperature



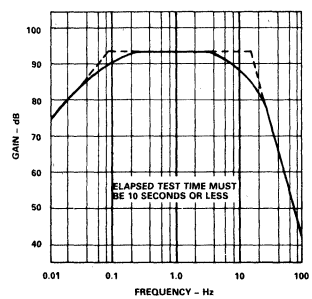
Input Voltage Noise vs. Supply Voltage



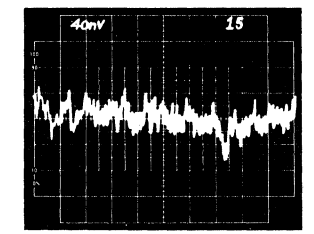
Input Current Noise Spectral Density



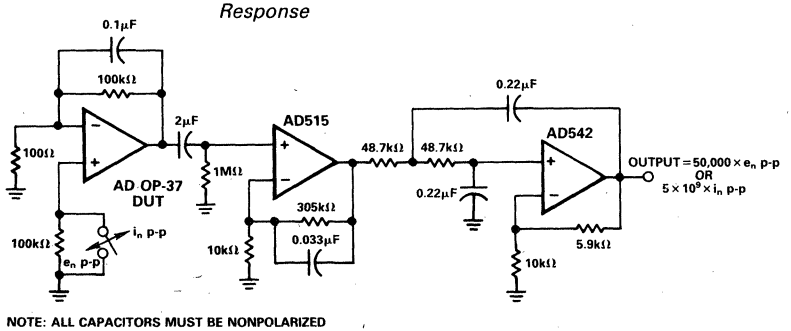
Total Noise vs. Source Impedance



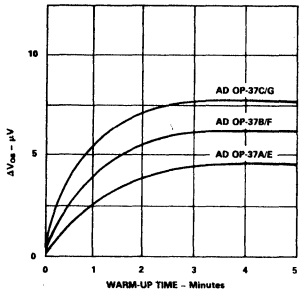
0.1Hz to 10Hz Noise Test Frequency Response



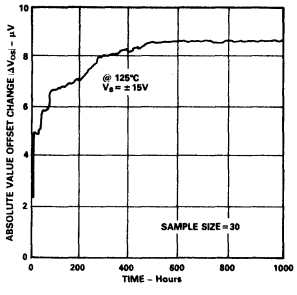
0.1Hz to 10Hz p-p Voltage Noise



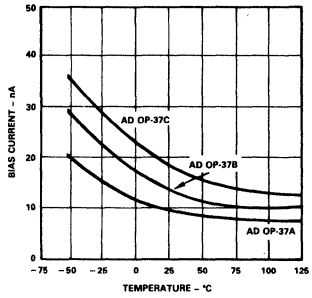
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



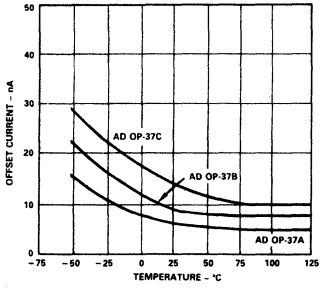
Input Offset Voltage Turn-On Drift vs. Time



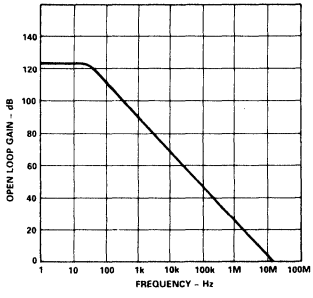
Long Term Offset Stability @ Temperature



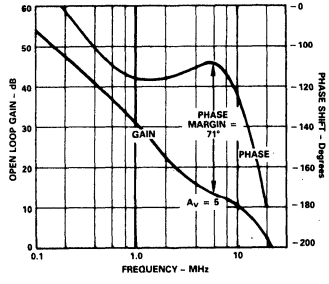
Input Bias Current vs. Temperature



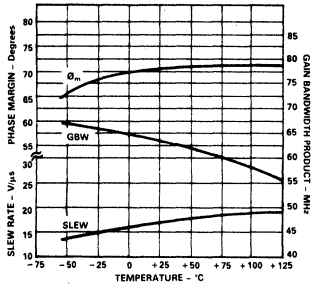
Input Offset Current vs. Temperature



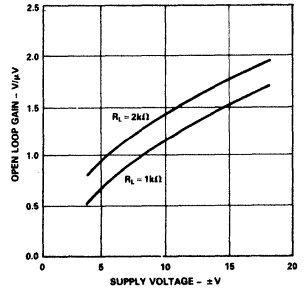
Open Loop Frequency Response



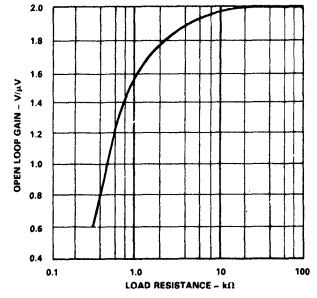
Open Loop Gain and Phase Shift vs. Frequency



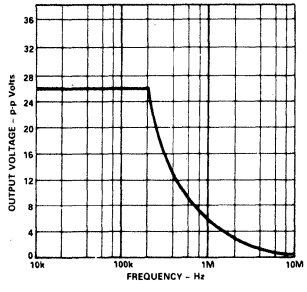
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



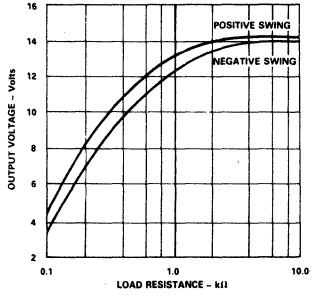
Open Loop Gain vs. Supply Voltage



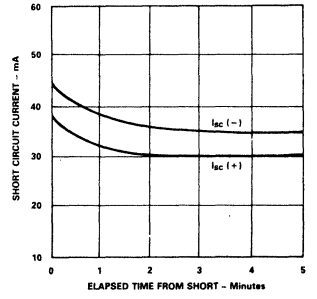
Open Loop Gain vs. Resistive Load



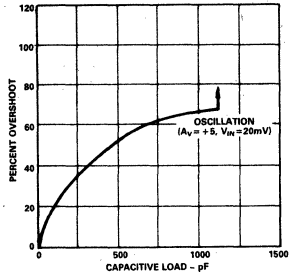
Undistorted Output Swing vs. Frequency



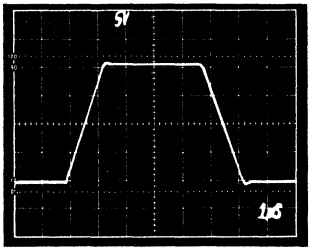
Output Swing vs. Resistive Load



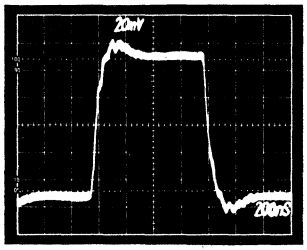
Output Short Circuit Current vs. Time



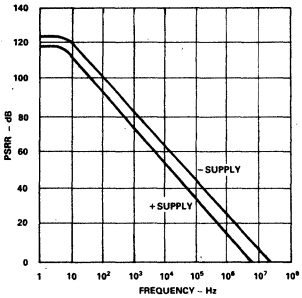
Small Signal Overshoot vs. Capacitive Load



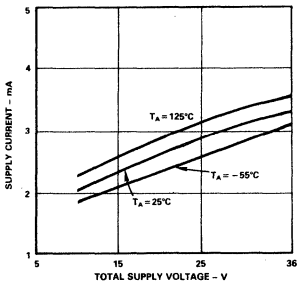
Unity Gain Follower Pulse Response (Large Signal)



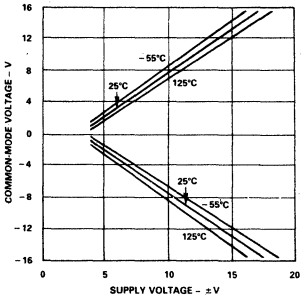
Unity Gain Follower Pulse Response (Small Signal)



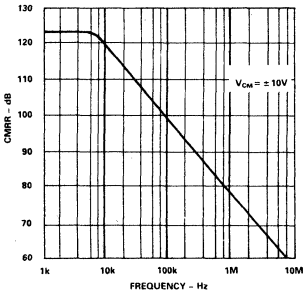
Power Supply Rejection Ratio vs. Frequency



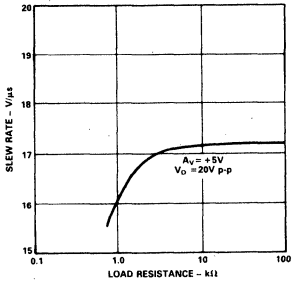
Supply Current vs. Supply Voltage



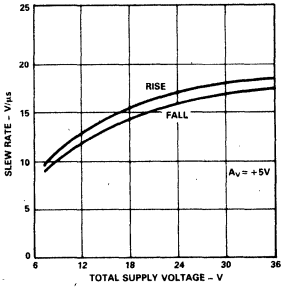
Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency



Slew Rate vs. Resistive Load



Slew Rate vs. Supply Voltage

8 × 8-Bit CMOS Multiplier/Accumulator

ADSP-1008A

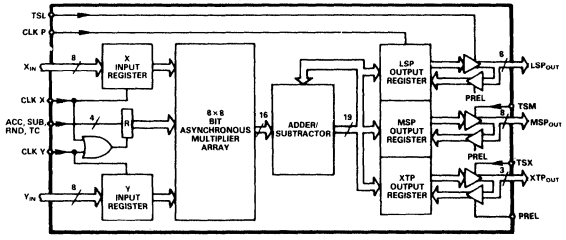
FEATURES

8 × 8-Bit Parallel Multiplication/Accumulation
100mW Power Dissipation with TTL-Compatible 1.5 Micron CMOS Technology
55ns Multiply/Accumulate Time
Improved TDC1008J4 Second Source
Twos-Complement or Unsigned Magnitude
Available in Hermetically-Sealed 48-Pin Ceramic DIP or 48-Pin Plastic DIP
Single +5V Power Supply
Specified from −55°C to +125°C Ambient

APPLICATIONS

Matrix Manipulations
Fourier Transformations
Digital Filtering
Image Processing

ADSP-1008A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1008A is a TTL compatible high-speed low-power 8 × 8-bit multiplier accumulator (MAC) that is pin for pin compatible with TRW's TDC1008J4. The ADSP-1008A is a very fast (55ns) 8 × 8 MAC, with low power consumption (100mW max). Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus, unlike existing bipolar and ECL devices, it is safe to both specify and operate the ADSP-1008A over the full MIL temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using CMOS technology. The high speed is obtained by the use of three time-saving techniques. A modified Booth algorithm reduces time-consuming operations. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage of the multiplier.

The ADSP-1008A has two 8-bit input buses, two 8-bit product buses and a 3 bit extra product bus. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1008A to operate on an 8-bit bus.

The ADSP-1008A has a RND control which rounds the product to the 11 most significant bits by adding a 1 to the MSB of the LSP. The preload control is used in conjunction with the three state control to initialize the contents of the output registers. The ACC and SUB controls are used to determine whether a multiply/add, a multiply/subtract, or a straight multiply is performed. The TC control is used to distinguish between two's complement or unsigned magnitude inputs.

The ADSP-1008A is available in a hermetically-sealed 48-pin ceramic DIP or 48-pin plastic DIP.

This one-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

ANALOG DEVICES

12 × 12-Bit CMOS Multiplier/Accumulator

ADSP-1009A

FEATURES

12 × 12-Bit Parallel Multiplication/Accumulation
70ns Multiply/Accumulate Time
375mW Power Dissipation with TTL-Compatible 1.5 Micron CMOS Technology
Pin-Compatible with ADSP-1009, TDC1009J1, and TMC2009J3
Twos Complement or Unsigned Magnitude
Preloadable Accumulation Registers
Available in Hermetically-Sealed 64-Pin DIP, Hermetically-Sealed 68-Pin Grid Array, or Plastic 64-Pin DIP
Available Specified from −55°C to +125°C Ambient

APPLICATIONS

Digital Signal Processing
Digital Filtering
Fourier Transformations
Correlations
Image Processing
Telecommunications

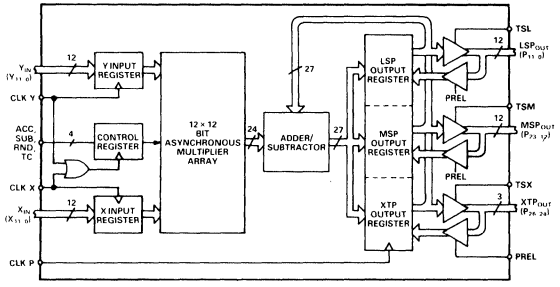
GENERAL DESCRIPTION

The ADSP-1009A is a high-speed, low-power 12 × 12-bit parallel multiplier/accumulator fabricated in 1.5 micron CMOS.

The ADSP-1009A has two 12-bit input ports, a 12-bit Most Significant Product (MSP) port, a 12-bit Least Significant Product (LSP) port, and a 3-bit Extended Product (XTP) port. Inputs can be represented in either twos-complement or unsigned-magnitude formats. The ADSP-1009A produces a 24-bit product whose MSP can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP. After multiplying, the ADSP-1009A can latch its product directly into the output registers or update the output registers with their previous contents added to or subtracted from the product. The output registers can also be initialized prior to multiplication/accumulation with data preloaded from the output ports.

All input pins are diode-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. A third clock line controls the product registers. Each of the three product registers has its own three-state output control. Three-state outputs and independently clocked inputs allow the ADSP-1009A to be connected directly to a single 12-bit bus.

ADSP-1009A FUNCTIONAL BLOCK DIAGRAM



The ADSP-1009A is a pin-for-pin replacement for Analog Devices' ADSP-1009 and is also pin-for-pin compatible in a DIP package with TRW's TDC1009J1 and TMC2009J3. The ADSP-1009A's multiply/accumulate time is over twice as fast as either TRW device.

The power consumption of the ADSP-1009A is 375mW maximum, less than 10% of the power required by equivalent bipolar devices. The differential between the ADSP-1009A's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, unlike equivalent bipolar devices, the ADSP-1009A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

The ADSP-1009A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1009A is available in either a 64-pin hermetically sealed ceramic DIP, a space-saving, hermetically sealed 68-pin grid array, or a plastic 64-pin DIP.

This one-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

ANALOG DEVICES

16 × 16-Bit CMOS Multiplier/Accumulator

ADSP-1010A

FEATURES

- **16 × 16-Bit Parallel Multiplication/Accumulation**
- **200mW Power Dissipation With TTL-Compatible CMOS Technology**
- **85ns Multiply/Accumulate Time**
- **Pin Compatible with ADSP-1010, TDC1010J1, and TMC2010J3**
- **Twos-Complement or Unsigned Magnitude Data Formats**
- **Single +5V Power Supply**
- **Available in Hermetically-Sealed 64-Pin Ceramic DIP, 68-Pin Grid Array or Plastic 64-Pin DIP**
- **Available Specified from −55°C to +125°C Ambient**

APPLICATIONS

- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
  - **Power Series Expansions**
- **Matrix Manipulations**
- **Microprocessor Acceleration**

GENERAL DESCRIPTION

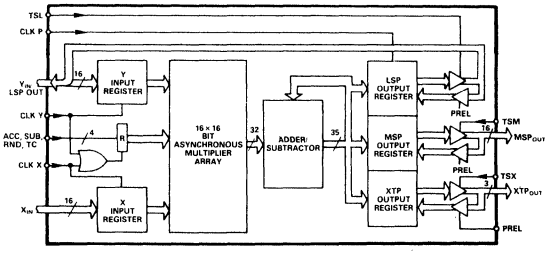
The ADSP-1010A is a TTL-compatible high-speed low-power 16 × 16-bit monolithic multiplier/accumulator that, in DIP form, is pin for pin compatible with the ADSP-1010, TDC1010J1, and TMC2010J3. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus, unlike bipolar and ECL multipliers, it is safe to both specify and operate the ADSP-1010A over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using CMOS technology. The high speed is obtained by the use of a 1.5 micron CMOS process and three time-saving techniques. A modified Booth algorithm is used. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage of the multiplier.

The ADSP-1010A has two 16-bit input buses, a 16-bit MSP product bus, a 16-bit LSP product bus, the output port of which is shared with the Y input port, and a 3-bit extended product bus. All inputs are diode protected. The independently controlled input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1010A to operate on a single 16-bit bus.

This one-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

ADSP-1010A FUNCTIONAL BLOCK DIAGRAM



The ADSP-1010A has a RND control that rounds the product to the 16 most significant bits by adding a 1 to the MSB of the 16 LSBs of the multiplier array. The preload control is used in conjunction with the three-state controls to initialize the contents of the output registers. The ADSP-1010A will perform either a multiplication and addition or multiplication and subtraction or a straight multiplication depending upon the status of the ACC and SUB controls. The TC control provides the capability for either twos-complement or unsigned magnitude data formats.

The ADSP-1010A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally the ADSP-1010A is available in either a hermetically sealed 64-pin ceramic DIP, a 68-pin Grid Array or a 64-pin plastic DIP.

ANALOG DEVICES

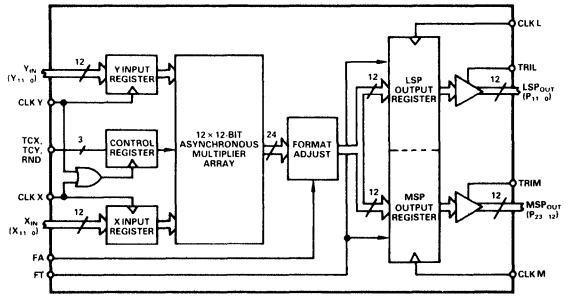
12 × 12-Bit CMOS Multiplier

ADSP-1012A

FEATURES
- **12 × 12-Bit Parallel Multiplication**
- **65ns Multiply Time**
- **200mW Power Dissipation with TTL-Compatible CMOS Technology**
- **Twos-Complement, Unsigned-Magnitude, and Mixed-Mode Data Formats**
- **Available in Hermetically-Sealed 64-Pin DIP, Hermetically-Sealed 68-Pin PGA, or Plastic 64-Pin DIP**
- **Available Specified from −55°C to +125°C Ambient**
- **Pin-Compatible with ADSP-1012 and MPY012HJ1**

APPLICATIONS
- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Image Processing**

ADSP-1012A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1012A is a high-speed, low-power 12 × 12-bit parallel multiplier fabricated in 1.5 micron CMOS.

The ADSP-1012A has two 12-bit input ports, a 12-bit Most Significant Product (MSP) port, and a 12-bit Least Significant Product (LSP) port. Input data is interpreted in twos-complement format. The ADSP-1012A produces a 24-bit result whose twos-complement MSP can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP.

All input pins are diode-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. Both of the product registers have their own independent clock lines and their own independent three-state output controls. Three-state outputs and independently clocked inputs allow the ADSP-1012A to be connected directly to a single 12-bit bus.

The ADSP-1012A is a pin-for-pin replacement for Analog Devices' ADSP-1012 and is also pin-for-pin compatible in a DIP package with TRW's MPY012HJ1. The ADSP-1012A's multiply time is less than half that of the TRW device.

The power consumption of the ADSP-1012A is 200mW maximum, 10% of the power required by equivalent bipolar devices. The differential between the ADSP-1012A's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, the ADSP-1012A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

The ADSP-1012A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1012A is available in either a 64-pin hermetically sealed ceramic DIP, a hermetically sealed ceramic 68-pin grid array, or a plastic 64-pin DIP.

PRELIMINARY DATA

ANALOG DEVICES

16 × 16-Bit CMOS Multiplier

ADSP-1016A

FEATURES

- **16 × 16-Bit Parallel Multiplication**
- **70ns Multiply Time**
- **300mW Power Dissipation with TTL-Compatible CMOS Technology**
- **Twos-Complement, Unsigned-Magnitude and Mixed-Mode Data Formats**
- **Available in Hermetically-Sealed 64-Pin DIP, Hermetically Sealed 68-Pin PGA, or Plastic 64-Pin DIP**
- **Available Specified from −55°C to +125°C Ambient**
- **Pin-Compatible with ADSP-1016 and MPY016HJ1**

APPLICATIONS

- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Image Processing**
- **General Purpose Computing**

GENERAL DESCRIPTION

The ADSP-1016A is a high-speed low-power 16 × 16-bit parallel multiplier fabricated in 1.5 micron CMOS.

The ADSP-1016A has two 16-bit input ports, a 16-bit Most Significant Product (MSP) port, and a 16-bit Least Significant Product (LSP) port. Input data is interpreted in twos-complement, unsigned-magnitude, or mixed-mode formats. The ADSP-1016A produces a 32-bit result whose MSP can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP.

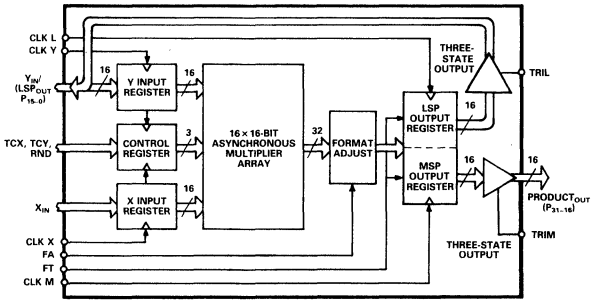
All input pins are diode-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. Both of the product registers have their own independent clock lines and their own independent three-state output controls. Three-state outputs and independently clocked inputs allow the ADSP-1016A to be connected directly to a single 16-bit bus.

The ADSP-1016A is a pin-for-pin replacement for Analog Devices' ADSP-1016 and is also pin-for-pin compatible in a DIP package with TRW's MPY016HJ1. The ADSP-1016A's multiply time is more than twice as fast as the TRW device.

The power consumption of the ADSP-1016A is 300mW maximum, less than 10% of the power required by equivalent bipolar devices. The differential between the ADSP-1016A's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, the ADSP-1016A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

This one-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

ADSP-1016A FUNCTIONAL BLOCK DIAGRAM



The ADSP-1016A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS") parts. MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1016A is available in either a 64-pin hermetically sealed ceramic DIP, a hermetically sealed ceramic 68-pin grid array, or a plastic 64-pin DIP.

ANALOG DEVICES

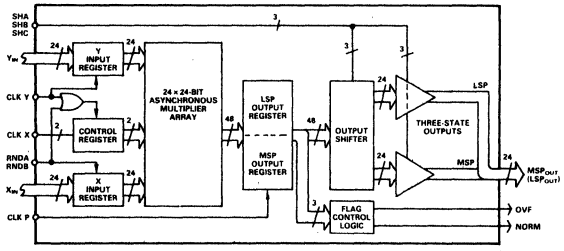
24 × 24-Bit CMOS Multiplier

ADSP-1024A

FEATURES
- **24 × 24-Bit Parallel Multiplication**
- **90ns Multiply Time**
- **300mW Power Dissipation with TTL-Compatible CMOS Technology**
- **Twos-Complement Data Format**
- **Rounding Options at Three Positions**
- **Left-Shifts of 0, 1, or 2 Bits on Output**
- **Overflow and Normalization Status Flags**
- **Single-Cycle Output of Both 24-Bit Output Words**
- **Available in Hermetically-Sealed 84-Pin Grid Array**
- **Available Specified from −55°C to +125°C Ambient**
- **Pin-Compatible with ADSP-1024**

APPLICATIONS
- **High-Resolution Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Voice Recognition**
- **Mantissa Multiplication for Floating-Point Operations**

ADSP-1024A FUNCTIONAL BLOCK DIAGRAM



The power consumption of the ADSP-1024A is 300mW maximum. The differential between the ADSP-1024A's junction temperature and the ambient temperature stays small because of this low-power dissipation. Thus, the ADSP-1024A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

The ADSP-1024A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. The ADSP-1024A is available in a hermetically-sealed ceramic 84-pin grid array.

GENERAL DESCRIPTION

The ADSP-1024A is a high-speed, low-power 24 × 24-bit parallel multiplier fabricated in 1.5 micron CMOS. The ADSP-1024A is a pin-for-pin replacement for Analog Devices' ADSP-1024.

The ADSP-1024A is a three-port device which has two 24-bit input buses and two 24-bit product buses. The Most Significant Product (MSP) bus and the Least Significant Product (LSP) bus share the output port. In a single cycle, both MSP and LSP can be output. Input data must be in two's-complement format. The ADSP-1024A produces a 48-bit result whose two's-complement MSP can be rounded with controls which cause a 1 to be added to either bit 23, 22, or 21 of the LSP.

All input pins are diode-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. A third clock line controls the product registers. Both of the product registers have their own three-state output controls. Three-state outputs and independently clocked inputs allow the ADSP-1024A to be connected directly to a single 24-bit bus.

PRELIMINARY TECHNICAL DATA

ANALOG DEVICES

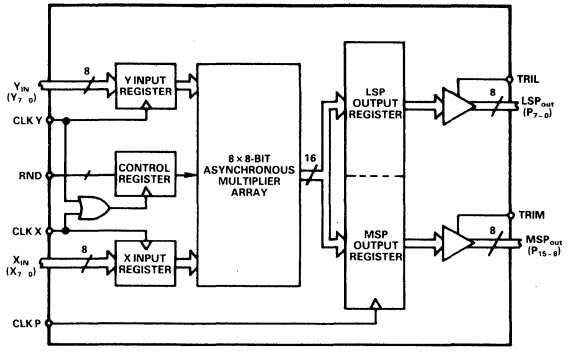
8 × 8-Bit CMOS Multiplier

ADSP-1080A

FEATURES
- **8 × 8-Bit Parallel Multiplication**
- **30MHz Multiplication Rate**
- **275mW Power Dissipation with TTL-Compatible 1.5 Micron CMOS Technology**
- **Twos-Complement Data Format**
- **Available in Hermetically-Sealed 40-Pin DIP or Plastic 40-Pin DIP**
- **Available Specified from −55°C to +125°C Ambient**
- **Pin-Compatible with ADSP-1080 and MPY008HJ5**

APPLICATIONS
- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Image Processing**

ADSP-1080A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1080A is a high-speed, low-power 8 × 8-bit parallel multiplier fabricated in 1.5 micron CMOS.

The ADSP-1080A has two 8-bit input ports, an 8-bit Most Significant Product (MSP) port, and an 8-bit Least Significant Product (LSP) port. Input data is interpreted in twos-complement format. The ADSP-1080A produces a 16-bit result whose twos-complement MSP can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP.

All input pins are diode-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. A third clock line controls the product registers. Both of the product registers have their own three-state output controls. Three-state outputs and independently clocked inputs allow the ADSP-1080A to be connected directly to a single 8-bit bus.

The ADSP-1080A is a pin-for-pin replacement for Analog Devices' ADSP-1080 and is also pin-for-pin compatible in a DIP package with TRW's MPY008HJ5 and MPY008HJ5-1. The ADSP-1080A's multiply time is faster than either TRW device.

The power consumption of the ADSP-1080A is 275mW maximum, 5% of the power required by equivalent bipolar devices. The differential between the ADSP-1080A's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, the ADSP-1080A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

The ADSP-1080A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1080A is available in either a 40-pin hermetically-sealed ceramic DIP or a plastic 40-pin DIP.

This one-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

ANALOG DEVICES

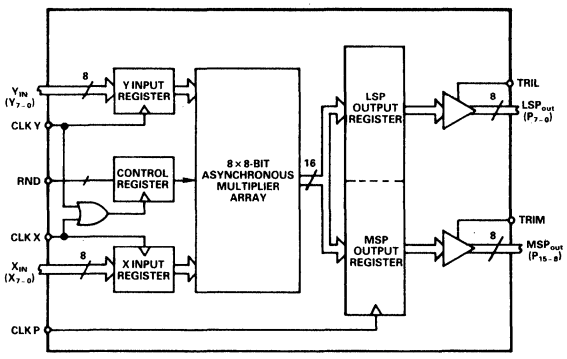
8 × 8-Bit CMOS Multiplier

ADSP-1081A

FEATURES
- **8 × 8-Bit Parallel Multiplication**
- **30MHz Multiplication Rate**
- **275mW Power Dissipation with TTL-Compatible CMOS Technology**
- **Unsigned-Magnitude Data Format**
- **Available in Hermetically-Sealed 40-Pin DIP or Plastic 40-Pin DIP**
- **Available Specified from −55°C to +125°C Ambient**
- **Pin-Compatible with ADSP-1081 and MPY08HUJ5**

APPLICATIONS
- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
- **Image Processing**

ADSP-1081A FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1081A is a high-speed, low-power 8 × 8-bit parallel multiplier fabricated in 1.5 micron CMOS.

The ADSP-1081A has two 8-bit input ports, an 8-bit Most Significant Product (MSP) port, and an 8-bit Least Significant Product (LSP) port. Input data is interpreted in unsigned-magnitude format. The ADSP-1081A produces a 16-bit result whose unsigned-magnitude MSP can be rounded with a control which causes a 1 to be added to the Most Significant Bit (MSB) of the LSP.

All input pins are diode-protected. The input and output registers are all D-type positive-edge-triggered flip-flops. The input registers are controlled by independent clock lines. A third clock line controls the product registers. Both of the product registers have their own three-state output controls. Three-state outputs and independently-clocked inputs allow the ADSP-1081A to be connected directly to a single 8-bit bus.

The ADSP-1081A is a pin-for-pin replacement for Analog Devices' ADSP-1081 and is also pin-for-pin compatible in a DIP package with TRW's MPY08HUJ5 and MPY08HUJ5-1. The ADSP-1081A's multiply time is less than either TRW device.

The power consumption of the ADSP-1081A is 275mW maximum, less than 15% of the power required by equivalent bipolar devices. The differential between the ADSP-1081A's junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, the ADSP-1081A can be safely specified for operation at environmental temperatures over its extended temperature range (−55°C to +125°C ambient).

The ADSP-1081A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Additionally, the ADSP-1081A is available in either a 40-pin hermetically-sealed ceramic DIP or a plastic 40-pin DIP.

This one-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

ANALOG DEVICES

Integer Arithmetic Unit

ADSP-1101

FEATURES

- 16 × 16-Bit Parallel Multiplication/Accumulation
- 70ns Cycle Time
- 40-Bit Adder/Subtracter Unit with Status Flags
- 16-Bit Logic Unit
- Dual 40-Bit Accumulators with Status Flags
- 7-Bit Right/Left Shift on Output
- Flexible Load/Bypass of Six Input Registers
- Flexible Preload of Both Accumulators
- Feedback from Accumulators to Adder/Subtracter with Left/Right-Shift Control
- Feedback from Adder/Subtracter to Y Input Registers and Logic Unit/Multiplier
- On-Chip, Low Overhead Block Floating-Point Control
- Autonormalized Output with Exponent
- Output with Saturation
- Three 16-Bit Data Ports (Two Input and One Output) Can Each Transfer Two 16-Bit Words Per Cycle
- Twos-Complement and Unsigned Magnitude Multiplication
- Independent Microcode Control of Each Functional Unit
- Low-Power TTL-Compatible 1.5 Micron CMOS Technology, 300mW Max Power Dissipation
- 100-Pin Grid Array

GENERAL DESCRIPTION

The Integer Arithmetic Unit is a versatile 16-bit integer processor which performs a full complement of arithmetic, logic, and shift functions. The ADSP-1101 performs complex, arithmetic, and low-overhead block floating-point operations completely on-chip. Sustainable single-cycle operations of the form $y = mx + b$ are also supported.

The ADSP-1101 is ideally suited for fast integer arithmetic. Multiple ADSP-1101s can be cascaded to perform single-cycle FIR filters without external memory or other hardware. The ADSP-1101 performs six-cycle radix-2 butterfly operations entirely on-chip. Sums of products algorithms, including Taylor series, can also be performed on-chip.

The ADSP-1101 has two input ports. Each port can transfer two 16-bit words per cycle. The Y registers may be loaded from either input port. One pair of X input registers is loadable from the X-Port, the second pair, from the Y-Port. Both accumulators may be loaded from the Y-Port.

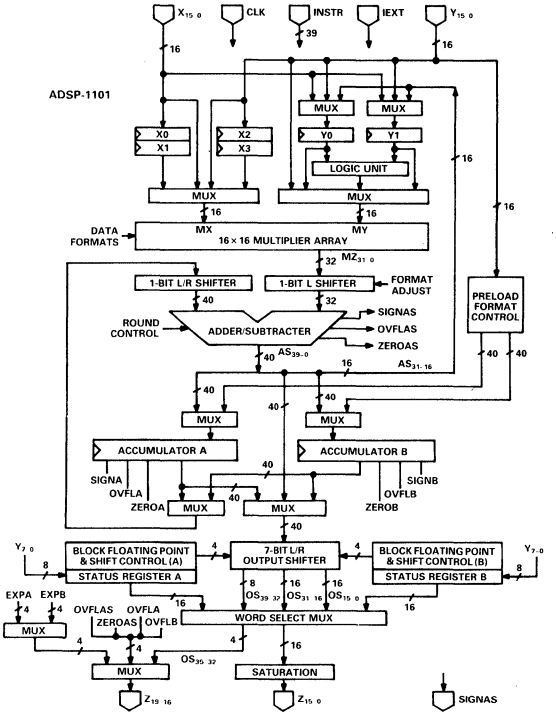
Y input register values can be passed through the Logic Unit prior to entering the Multiplier Array. The Adder/Subtractor result may be routed to either or both accumulators, the Y registers, or the output port (via the 7-Bit Right/Left Output Shifter). Accumulator contents may be routed to the Adder/Subtracter and/or the output port (via the Output Shifter). Block Floating-Point Control is implemented entirely on-chip.

The ADSP-1101's 20-bit Z-Port can output a 16-bit data word or Status Register on its lower-order 16-bits and extension data, status flags, or autonormalized output exponents on its high-order 4 bits. The 16-bit data word can come from either accumulator or directly from the Adder/Subtracter. Like the two input ports, the output port can transfer data at twice the clock rate.

The ADSP-1101's 39-bit instruction is partitioned to allow independent control of its functional elements. Subfields that do not change can be removed from the system microcode word. Many instructions may be conditioned on internal or external status flags.

The ADSP-1101 is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B.

ADSP-1101 FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

ORDERING INFORMATION

ADSP-1101TG/883B
- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

Package
G – Pin Grid Array

Processing
Blank – Standard
+ – High Reliability
883B – MIL-STD-883

Performance/ Temperature
J – Standard, 0 to +70°C
K – High Speed, 0 to +70°C
S – Standard, −55°C to +125°C
T – High Speed, −55°C to +125°C

16 × 16-Bit CMOS Multipliers with Optional Pipeline

ADSP-1102/1103/1516/1517

FEATURES

High Speed
- **35ns Pipelined Multiply Time (ADSP-1102/1103)**
- **65ns Multiply Time**

250mW Power Dissipation with TTL-Compatible CMOS Technology

Improved Second Sources to Am29516, Am29517, MPY016HJ1 and MPY016KJ1

Twos-Complement, Unsigned-Magnitude or Mixed-Mode Multiplication

Single +5 Volt Power Supply Operation

Available in Hermetically-Sealed 64-Pin DIP, Hermetically-Sealed 68-Pin Grid Array, or Plastic 64-Pin DIP

Available Specified from −55°C to +125°C Ambient

APPLICATIONS

Fourier Transformations

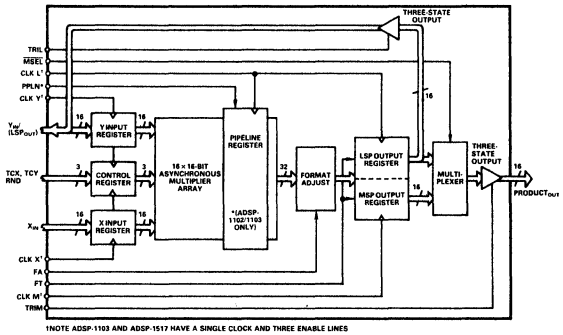
Digital Filtering

Matrix Manipulations

Video Processing

Array Processing

ADSP-1102/1103 AND ADSP-1516/1517
FUNCTIONAL BLOCK DIAGRAM



1NOTE ADSP-1103 AND ADSP-1517 HAVE A SINGLE CLOCK AND THREE ENABLE LINES

GENERAL DESCRIPTION

The ADSP-1102, ADSP-1103, ADSP-1516, and ADSP-1517 are high-speed, low-power 16 × 16-bit multipliers fabricated in double-metal, 1.5 micron CMOS. The ADSP-1102 and ADSP-1516 are pin-for-pin compatible (in a DIP package) with Advanced Micro Devices' Am29516. The ADSP-1103 and ADSP-1517 are pin-for-pin compatible (in a DIP package) with AMD's Am29517.

The ADSP-1102/1103 have internal pipeline registers (enabled by the PPLN control) that nearly halve their 65ns maximum clocked multiply time to a throughput rate of 35ns. The lower-cost ADSP-1516/1517 lack this pipeline register and are functionally identical to the Am29516/29517. The ADSP-1102/1516 differ from the ADSP-1103/1517 only in how internal registers are clocked.

The power consumption of each of these four multipliers is at or below 200mW, less than 5% of the power required by equivalent bipolar and ECL multipliers. The differential between these devices' junction temperature and the ambient temperature stays small because of this low power dissipation. Thus, unlike most equivalent bipolar and ECL devices, they can be safely specified for operation at environmental temperatures over their extended range (−55°C to +125°C ambient).

The four multipliers each have two 16-bit input ports and a 16-bit product output port. The inputs can be twos-complement, unsigned-magnitude or mixed-mode. The internal multiplier product is 32 bits in width and consists of a 16-bit Most Significant Product (MSP) and a 16-bit Least Significant Product (LSP).

The LSP can be routed back through the Y input port, multiplexed through the product output port, or both. A pin used for supply GND in the MPY016HJ1, MPY016KJ1, ADSP-1016, and ADSP-1016A is functionally redefined as a MSP select control pin. When low, the MSP select control multiplexes the MSP to the three-state driver at the product port, insuring the compatibility of the ADSP-1102 and ADSP-1516 with the MPY016HJ1, MPY016KJ1, ADSP-1016, and ADSP-1016A. When high, the MSP select control makes the LSP available at the product port.

All input pins are diode-protected. The input, LSP, and MSP registers are D-type postive-edge-triggered flip-flops. With the ADSP-1102/1516, all four registers are controlled by independent clock lines. With the ADSP-1103/1517, there is a single clock, enabled by three independent register enables for the two input registers and the pair of product registers. Independent controls for the input registers simplify repeated multiplication by a constant. Three-state outputs and clocked inputs allow the four multipliers to be connected directly to a 16-bit bus.

The RND control rounds the product to the 16 most significant bits by adding a 1 to the Most Significant Bit (MSB) of the LSP. The FA control format-adjusts twos-complement output by shifting the MSP and the MSB of the LSP left one bit and then repeating the sign bit in the MSB of the LSP. For asynchronous output, the feed-through (FT) control allows the LSP and MSP to bypass the output registers and flow directly to the three-state output drivers.

These four multipliers are all available for both commercial and MIL temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL grade parts are available processed and tested fully to MIL-STD-883, Class B. Additionally, all versions are available in either a 64-pin hermetically-sealed ceramic DIP, a hermetically-sealed 68-pin grid array, or a plastic 64-pin DIP.

PRELIMINARY TECHNICAL DATA

16 × 16-Bit CMOS Single-Port Multiplier/Accumulator

ADSP-1110A

FEATURES

- **16 × 16-Bit Parallel Multiplication/Accumulation**
- **40-Bit Wide Accumulator with Overflow Flag, Saturation Arithmetic, and Shift-Left Control**
- **Twos-Complement or Unsigned Magnitude Inputs**
- **85ns Multiply/Accumulate Time**
- **Low-Power TTL-Compatible 1.5 Micron CMOS Technology**
- **150mW Max Power Dissipation**
- **28-Pin DIP (Ceramic or Low-Cost Plastic)**

GENERAL DESCRIPTION

The ADSP-1110A is a high-speed, low-power, single-port 16 × 16-bit multiplier/accumulator (MAC), with processing throughput comparable to existing three-port MACs. Its single-bus structure offers unique advantages: more compact packaging in a 28-pin DIP, simpler interface to a single-bus system, and significantly reduced cost. In addition, innovative on-chip features extend the ADSP-1110A's capabilities and eliminate external hardware.

The ADSP-1110A is optimal for applications where board space is limited but high throughput is required. In addition, a microprocessor-based system can realize greater throughput by utilizing the ADSP-1110A in an accelerator.

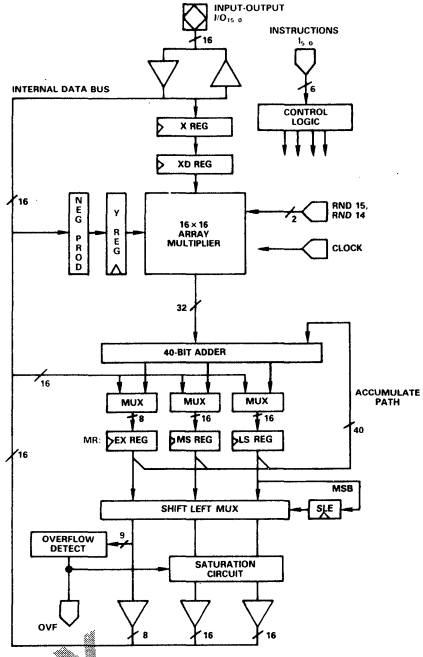
All inputs to and outputs from the ADSP-1110A pass through its single 16-bit I/O port. All I/O operations are single-cycle. A multiply or multiply/accumulate operation requires two cycles to complete—consistent with the two cycles required to load input pairs to the multiplier. An internal pipeline register enables new inputs to be loaded as the previous multiply/accumulate is computed—allowing the device's full 11.8MHz computational bandwidth to be utilized.

A six-bit microcode instruction word governs the ADSP-1110A's operation. The instruction set centers around I/O and multiply/accumulate operations. Additional instructions allow extra precision in single- and double-precision operations to be obtained efficiently.

Multiplier products are accumulated in a 40-bit wide Multiplier Result (MR) register, which consists of a 16-bit MS (Most Significant) and LS (Least Significant) register, and an 8-bit EX (Extension) register. Either multiplier input can be a twos-complement or unsigned magnitude number. Overflow from the lower 32 bits of the MR into the upper eight guard bits is detected and can be monitored externally. Outputs can, conditional upon overflow status, be saturated to full scale. An MR register can be shifted left by one bit upon output; two independent controls allow rounding consistent with output formatting.

The ADSP-1110A is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Packaging options include a 28-pin ceramic DIP and a low-cost 28-pin plastic DIP.

ADSP-1110A SINGLE-PORT MAC BLOCK DIAGRAM



PRELIMINARY TECHNICAL DATA

ORDERING INFORMATION

ADSP-1110ATD/883B—

- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

Package

D – Ceramic DIP
N – Plastic DIP

Processing

Blank – Standard
\+ – High Reliability
883B – MIL-STD-883

Performance/ Temperature

J – Standard, 0 to +70°C
K – High Speed, 0 to +70°C
S – Standard, −55°C to +125°C
T – High Speed, −55°C to +125°C

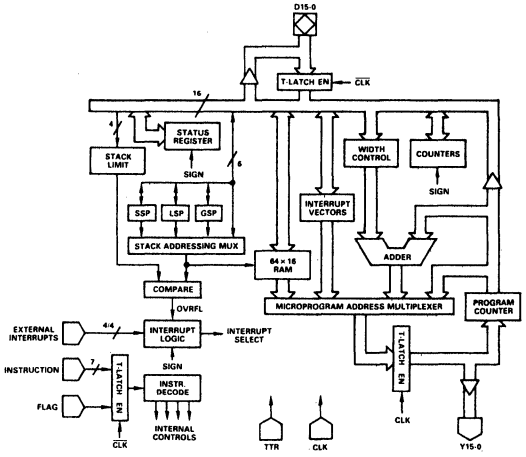
ANALOG DEVICES

Program Sequencer

ADSP-1401

FEATURES
- **16-Bit Addressing Capability**
- **Look-Ahead™ Pipeline**
- **Extensive Interrupt Handling**
  - **Ten On-Chip Interrupt Vectors**
- **70ns Cycle Time**
- **35ns Clock-to-Address Delay**
- **64-Word RAM for Storing**
  - **Subroutine Linkage**
  - **Jump Addresses**
  - **Counters**
  - **Status Register**
- **Low-Power TTL-Compatible 1.5 Micron CMOS Technology**
- **150mW Max Power Dissipation**
- **48-Pin DIP (Ceramic or Low-Cost Plastic)**

ADSP-1401 PROGRAM SEQUENCER



GENERAL DESCRIPTION

The ADSP-1401 is a high-speed microprogram controller optimized for the demanding sequencing tasks found in digital signal processors and general purpose computers (e.g. looping, jumping, branching, subroutines, condition testing and interrupts). In addition to high speed and large addressing range, it has unique features that make it highly versatile:

- on-chip control of ten prioritized and maskable interrupts
- four decrementing event counters
- absolute, relative and indirect addressing capability
- download capability (writeable control store)
- a dynamically configurable 64-word RAM.

During each micro-instruction, the ADSP-1401 monitors status indicators and the current instruction to determine the next microprogram address. This address can come from one of several sources: the stack, the jump address space in the RAM, the data port, the interrupt vectors, or the microprogram counter. An extensive set of conditional instructions is available, including jumps, branches, subroutines, interrupts, and writeable control store.

The ADSP-1401's internal 64-word RAM is used for interrupt and subroutine linkage via the stack. It also provides the ability to associate counters, jump addresses, and the status register with nested interrupts and subroutines.

Interrupts are handled entirely on chip. The ADSP-1401's internal interrupt control logic includes registers for eight external interrupt vectors, a mask register, and a priority decoder. Two additional vectors are reserved for internally-generated interrupts resulting from counter underflow and stack limit violation.

The ADSP-1401's four decrementing 16-bit counters are used to track loops and events. These counters are referenced by several conditional instructions and can also trigger an internal interrupt.

The ADSP-1401's Look-Ahead pipeline eliminates the need for an external microcode pipeline register by internally latching instructions and addresses. A complementary latching arrangement allows a new instruction to be decoded (in preparation for the following cycle) while the program memory address for the current cycle is held constant.

The ADSP-1401 is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Packaging options include a 48-pin ceramic DIP and a low-cost 48-pin plastic DIP.

PRELIMINARY TECHNICAL DATA

ORDERING INFORMATION

ADSP-1401TD/883B	— Processing	**Package**	**Performance/ Temperature**
	Package	D – Ceramic DIP N – Plastic DIP	J – Standard, 0 to +70°C K – High Speed, 0 to +70°C S – Standard, −55°C to +125°C T – High Speed, −55°C to +125°C
	Performance, Temp. Range	**Processing**	
	Part Number	Blank – Standard + – High Reliability 883B – MIL-STD-883	
	Analog Devices Digital Signal Processing		

Look-Ahead is a trademark of Analog Devices, Inc.

ANALOG DEVICES

Address Generator

ADSP-1410

FEATURES
16-Bit Addresses with Higher Precision Options
Look-Ahead™ Pipeline
80ns Cycle Time
20ns Clock-to-Address Delay
Versatile Addressing Hardware:
30 16-Bit Registers
16-Bit ALU with Left/Right Shift & Carry I/O
Comparator
Bit Reverser
Dual Ports
Powerful Single-Cycle Looping Instructions
Low-Power TTL-Compatible 1.5 Micron CMOS Technology
175mW Max Power Dissipation
48-Pin DIP (Ceramic or Low-Cost Plastic)

GENERAL DESCRIPTION

The ADSP-1410 is a fast, flexible address generator optimized for digital signal processors and general purpose computers. This low-power CMOS device rapidly generates the data memory addresses required by routines such as digital filters, FFTs, matrix operations, and DMAs.

The ADSP-1410's 10-bit microcode instructions include commands for looping, register read/writes, internal data transfers, and logical/shift operations. An internal Alternate Instruction Register (AIR) can also provide the instruction under external control, allowing microcode to be conserved in many applications.

In a single instruction cycle, the ADSP-1410 can:

- output a 16-bit memory address
- modify this memory address
- conditionally reinitialize the address based on a comparison with a preset value.

Consequently, circular buffers and modulo addressing of data memories can be implemented without overhead.

The ADSP-1410's architecture features a 16-bit ALU, a comparator, and 30 16-bit registers. The registers are organized into four files: sixteen address registers, six offset registers, four compare registers, and four initialization registers.

The ADSP-1410 has a 16-bit address (Y) port for outputting addresses and a 16-bit data (D) port for I/O between internal and external registers. A value provided by the data port may serve as an input to the 1410's ALU or may be directly output over the address port.

ORDERING INFORMATION

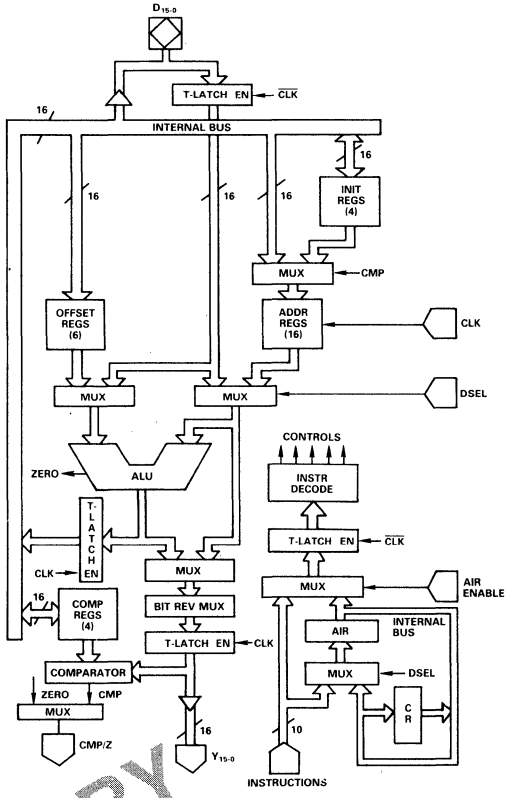
ADSP-1410TD/883B — Processing
Package
Performance, Temp. Range
Part Number
Analog Devices Digital Signal Processing

Package
D – Ceramic DIP
N – Plastic DIP

Processing
Blank – Standard
+ – High Reliability
883B – MIL-STD-883

Performance/ Temperature
J – Standard, 0 to + 70°C
K – High Speed, 0 to + 70°C
S – Standard, – 55°C to + 125°C
T – High Speed, – 55°C to + 125°C

ADSP-1410 ADDRESS GENERATOR



The ADSP-1410's Look-Ahead pipeline eliminates the need for an external microcode pipeline register by internally latching instructions and addresses. A complementary latching arrangement allows a new instruction to be decoded (in preparation for the following cycle) while the data memory address for the current cycle is held constant.

Double-precision (30-bit), single-cycle addressing can be performed by cascading two ADSP-1410's. Alternatively, a single ADSP-1410 can provide one double-precision address every two clock cycles.

The ADSP-1410 is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B. Packaging options include a 48-pin ceramic DIP and a low cost 48-pin plastic DIP.

Look-Ahead is a trademark of Analog Devices, Inc.

PRELIMINARY TECHNICAL DATA

ANALOG DEVICES

IEEE Floating Point Multiplier

ADSP-3210

FEATURES

- Fully Compatible with IEEE Standard 754
- Three Data Formats:
  - 32-Bit Single-Precision Floating Point
  - 64-Bit Double-Precision Floating Point
  - 32-Bit Fixed Point
- High Speed:
  - Single-Precision Throughput of 100ns/10 MEGAFLOPS
  - Double-Precision Throughput of 400ns/2.5 MEGAFLOPS
  - Fixed Point Throughput of 100ns/10MHz
  - Low Latency for Scalar Operations:
    - 300ns Single-Precision Latency
    - 600ns Double-Precision Latency
    - 300ns Fixed-Point Latency
- Two-Port Structure Supports Full Data Transfer Rate
- One Internal Pipeline Stage
- Low-Power TTL-Compatible 1.5 Micron CMOS Technology
- 400mW Max Power Dissipation
- Fully Registered I/O and Controls
- Three-State Outputs with Separate Enables
- 100-Lead Pin Grid Array

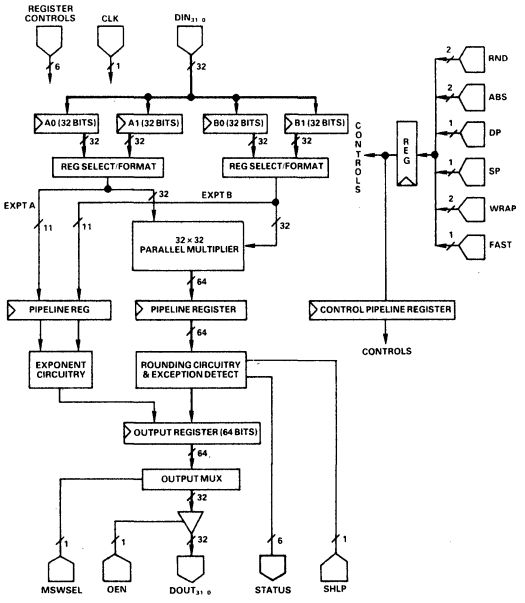
GENERAL DESCRIPTION

The ADSP-3210 is a high-speed floating point multiplier. The ADSP-3210 and its companion ALU, the ADSP-3220 are basic building blocks for high-speed numerical processors. These devices offer a full set of operations on three data formats: 32-bit single-precision floating point, 64-bit double-precision floating point, and 32-bit twos-complement fixed point.

The ADSP-3210 provides a high-speed, low-power solution to floating point multiplication requirements. Pipelined results are produced every 100ns for single-precision floating point and fixed-point data formats. The direct operand feed mode allows a low total latency of 300ns[1]. Pipelined double-precision floating point results are produced every 400ns. Maximum power dissipation is less than 400mW, worst case.

The ADSP-3210's data formats and floating point operations conform to the proposed IEEE Standard 754. The ADSP-3210 supports all four rounding modes in the standard for all three data formats. All four exception conditions—overflow, underflow, invalid operation, and inexact result—are flagged by dedicated status pins.

ADSP-3210 IEEE FLOATING POINT MULTIPLIER



The ADSP-3210 has a two-port structure: one 32-bit input port and one 32-bit output port. Two 32-bit registers are available for each of the A and B operands. Data inputs and outputs transfer at twice the cycle rate, allowing two 32-bit input operations and one 64-bit output operation on every cycle. All inputs and outputs are registered.

The ADSP-3210 is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B.

[1]Data setup + processing + output delay of most significant output word.

PRELIMINARY TECHNICAL DATA

ORDERING INFORMATION

ADSP-3210TG/883B
- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

Package
G – Pin Grid Array

Processing
Blank – Standard
+ – High Reliability
883B – MIL-STD-883

Performance/ Temperature
J – Standard, 0 to +70°C
K – High Speed, 0 to +70°C
S – Standard, –55°C to +125°C
T – High Speed, –55°C to +125°C

ANALOG DEVICES

IEEE Floating Point ALU

ADSP-3220

FEATURES

- Fully Compatible with IEEE Standard 754
- Three Data Formats:
  - 32-Bit Single-Precision Floating Point
  - 64-Bit Double-Precision Floating Point
  - 32-Bit Fixed Point
- Three Classes of Operations:
  - Arithmetic
  - Logical – Negate, AND, OR, XOR, Pass, Clear
  - Data Conversion – Between All Formats
- Performs Operations on Denormalized Numbers
- High Speed: 10MHz Throughput for All Operations on All Data Formats
- Low Latency
  - 250ns for Single-Precision Operations
  - 350ns for Double-Precision Operations
- Three-Port Structure Supports Full Data Transfer Rate
- One Internal Pipeline Stage
- Low-Power TTL-Compatible 1.5 Micron CMOS Technology
- 400mW Max Power Dissipation
- Fully Registered I/O and Controls
- Three-State Outputs with Separate Enables
- 144-Lead Pin Grid Array

GENERAL DESCRIPTION

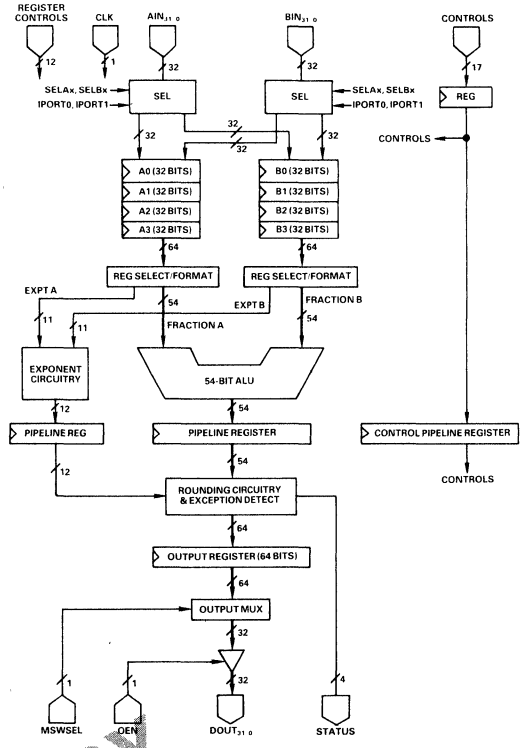
The ADSP-3220 is a floating point ALU with a full complement of arithmetic, logical and data conversion operations. The ADSP-3220 and its companion multiplier, the ADSP-3210, are basic building blocks for high-speed numerical processors with operations on three data formats: 32-bit single-precision floating point, 64-bit double-precision floating point, and 32-bit twos complement fixed point.

The ADSP-3220 provides a high-speed, low-power solution to floating point processing requirements. Pipelined results of all operations are produced every 100ns for all data formats. The direct operand feed mode allows a low total latency of 250ns[1]. Maximum power dissipation is less than 400mW, worst case.

The ADSP-3220's data formats and floating point operations conform to the proposed IEEE Standard 754. The ADSP-3220 supports all four rounding modes in the standard for all three data formats. All four exception conditions—overflow, underflow, invalid operation, and inexact result—are flagged by dedicated status pins.

[1]Data setup + processing + output delay of most significant output word.

ADSP-3220 FLOATING POINT ALU



The ADSP-3220's three-port structure accommodates the full 10 MEGAFLOPS throughput rate for double-precision operations, loading two 64-bit operands on each cycle and operating internally with 64-bit wide data paths. Four input registers are available for each of the A and B operands. Each input port can load any of the eight input registers, allowing the ADSP-3220 to be configured with one input port.

The ADSP-3220 is available for both commercial and military temperature ranges. Extended temperature range parts are available with high-reliability processing ("PLUS" parts). MIL-grade parts are available processed fully to MIL-STD-883, Class B.

PRELIMINARY TECHNICAL DATA

ORDERING INFORMATION

ADSP-3220TG/883B
- Processing
- Package
- Performance, Temp. Range
- Part Number
- Analog Devices Digital Signal Processing

Package
G – Pin Grid Array

Processing
Blank – Standard
+ – High Reliability
883B – MIL-STD-883

Performance/ Temperature
J – Standard, 0 to + 70°C
K – High Speed, 0 to + 70°C
S – Standard, – 55°C to + 125°C
T – High Speed, – 55°C to + 125°C

ANALOG DEVICES

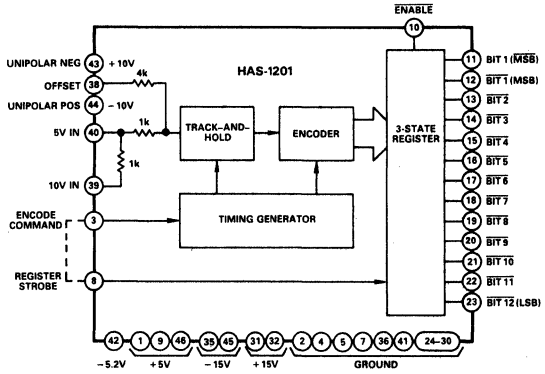
12-Bit, 1MHz Analog-to-Digital Converter

HAS-1201

FEATURES
12-Bit Resolution
1MHz Word Rate
T/H and Timing Circuits Included
Single Hybrid Package

APPLICATIONS
Radar Systems
Medical Instrumentation
Electro-Optics Systems
Test Systems
Digital Oscilloscopes

HAS-1201 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HAS-1201 A/D Converter combines high resolution and speed in a single hybrid package. This is a *complete* 12-bit, 1MHz unit which includes a track-and-hold and timing circuits. It's a total solution for the system designer who needs to perform the entire analog-to-digital conversion function in the smallest possible space.

This remarkable converter is a full answer to the question of digitizing analog signals into high-resolution data outputs and doing it in the most cost-effective way. The HAS-1201 is the ideal choice for the designer who needs state-of-the-art performance in high-resolution, high-speed A/D conversion.

Full-scale analog inputs are 5 or 10 volts; and the unit can operate with either bipolar or unipolar ranges. Analog input impedance is 1,000 ohms or 2,000 ohms and the three-state digital outputs are TTL compatible. The user needs to supply only an encode command and external power supplies for operation.

All models of the HAS-1201 A/D Converter are housed in 46-pin metal hybrid packages. The HAS-1201KM operates over a temperature range of 0 to +70°C. The HAS-1201SM is rated over an operating temperature range of −25°C to +85°C, but will operate with derated performance over a range of −55°C to +100°C. For units operating from −25°C to +85°C and military screening, order HAS-1201SMB; contact the factory for details about derated performance and military screening.

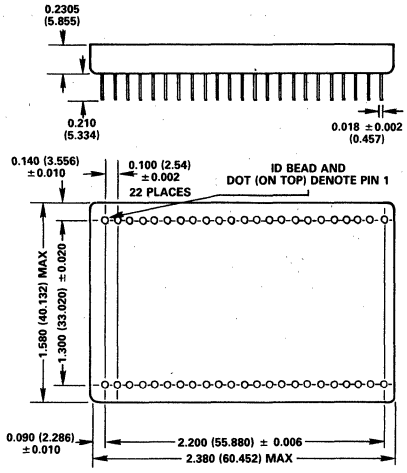
This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HAS-1201KM	HAS-1201SM/SMB
RESOLUTION (FS = Full Scale)	Bits	12	*
	% FS	0.025	*
ACCURACY			
Gain	% FS	±3	*
Gain vs. Temperature	ppm/°C	80	*
Linearity @ dc	% FS ± 1/2LSB	0.0125	*
Diff. Nonlinearity vs. Temp.	ppm/°C	10	15
Monotonicity		Guaranteed	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
(dc to 100kHz)	dB below FS (min)	80 (75)	*
(100kHz to 500kHz)	dB below FS	75	*
Conversion Rate	MHz, max	1.05	1.00
Conversion Time[2]	ns, max	950	*
Over Temperature	ns, max	950	1000
Aperture Uncertainty (Jitter)	ps, rms	30	*
Aperture Time (Delay)	ns	25	*
Signal to Noise Ratio (SNR)[3]	dB (min)	68 (65)	*
Transient Response[4]	ns (max)	600 (1000)	*
Overvoltage Recovery[5]	ns	1000	*
Input Bandwidth			
Small Signal, −3dB[6]	MHz	2	*
Large Signal, −3dB[7]	MHz	2	*
Two-Tone Linearity (@ input frequencies)			
(75kHz; 105kHz)	dB below FS	80	*
ANALOG INPUT			
Voltage Ranges	V, p-p FS	5.0/10.0	*
	V, max	±15	*
Impedance (5V/10V Input)	Ω (max)	1000/2000 (±1%)	*
Bipolar Offset[8]			
Initial (5V Input)	mV (max)	±2 (±10)	*
vs. Temperature	FS ppm/°C (max)	50 (200)	*
DIGITAL INPUTS			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
	V	"1" = +2.4 to +5	*
Impedance	LS TTL Loads	3	*
Rise and Fall Times	ns, max	10	*
Frequency	MHz, max	1.05	1.00
Encode Command Width[9]			
Min	ns	50	*
Max	ns	Encode Period − 350ns	*
Register Strobe Width			
Min	ns	50	*
Max	ns	Encode Period − 350ns	*
Enable Width			
Min	ns	100	*
DIGITAL OUTPUTS			
Format	Bit 1, Bit 1 − Bit 12	3-State; NRZ	*
Logic Levels, TTL-Compatible[10]	V	"0" = 0 to +0.5	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	1	*
Time Skew	ns, max	10	*
Delay: Register Strobe to Output Data Validity	ns	30	*
Coding		Complementary Binary (CBIN)	*
		Complementary Offset Binary (COB)	*
		Complementary 2's Complement (C2SC)	*
POWER REQUIREMENTS			
+15V ±5%	mA (max)	55 (70)	*
−15V ±5%	mA (max)	65 (80)	*
+5V ±5%	mA (max)	195 (235)	*
−5.2V ±5%	mA (max)	35 (40)	*
Power Consumption	W (max)	3.0 (3.6)	*
TEMPERATURE RANGE[11]			
Operating	°C	0 to +70	−25 to +85
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[12]			
Junction to Air, θja (Free Air)	°C/W	12	*
Junction to Case, θjc	°C/W	2.5	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



HAS-1201 PIN DESIGNATION

PIN	FUNCTION	PIN	FUNCTION
46	+5V	1	+5V
45	−15V	2	GROUND
44	UNIPOLAR POSITIVE	3	ENCODE COMMAND
43	UNIPOLAR NEGATIVE	4	GROUND
42	−5.2V	5	GROUND
41	GROUND	6	DO NOT CONNECT*
40	5V RANGE IN	7	GROUND
39	10V RANGE IN	8	REGISTER STROBE
38	OFFSET	9	+5V
37	DO NOT CONNECT*	10	$\overline{\text{ENABLE}}$
36	GROUND	11	BIT 1 (MSB)
35	−15V	12	$\overline{\text{BIT 1}}$ (MSB)
34	NO CONNECTION	13	$\overline{\text{BIT 2}}$
33	NO CONNECTION	14	$\overline{\text{BIT 3}}$
32	+15V	15	$\overline{\text{BIT 4}}$
31	+15V	16	$\overline{\text{BIT 5}}$
30	GROUND	17	$\overline{\text{BIT 6}}$
29	GROUND	18	$\overline{\text{BIT 7}}$
28	GROUND	19	$\overline{\text{BIT 8}}$
27	GROUND	20	$\overline{\text{BIT 9}}$
26	GROUND	21	$\overline{\text{BIT 10}}$
25	GROUND	22	$\overline{\text{BIT 11}}$
24	GROUND	23	$\overline{\text{BIT 12}}$ (LSB)

NOTE:
PINS 2, 4, 5, 7, 24-30, 36 and 41 NEED TO BE CONNECTED TO THE SAME COMMON GROUND AS CLOSE TO CASE AS POSSIBLE. POWER SUPPLY VOLTAGES NEED TO BE CONNECTED TO ALL DESIGNATED PINS.
***FOR FACTORY USE ONLY.**

NOTES

[1] In-Band Harmonics expressed in terms of spurious in-band signals generated at 1MHz encode rate at analog inputs shown in ( ).
[2] Measured from leading edge of Encode Command to time associated data are valid.
[3] RMS signal to rms noise ratio with 100kHz analog input.
[4] For full-scale step input, 12-bit accuracy attained in specified time.
[5] Recovers to specified performance in specified time after 2 × FS input overvoltage.
[6] With analog input 40dB below FS.
[7] With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 500kHz.)
[8] Externally adjustable to zero.
[9] Transition from digital "0" to digital "1" initiates encoding.
[10] Output data are TTL-compatible when analog input is within specified range. Negative over-voltage inputs cause tri-state output to drift to "high" condition and may create erroneous output (see text).
[11] Case Temperature. Models HAS-1201SM/SMB will operate with derated performance over temperature range of −55°C to +100°C; contact factory for details.
[12] Maximum junction temperature is +150°C.

Specifications subject to change without notice.

ANALOG DEVICES

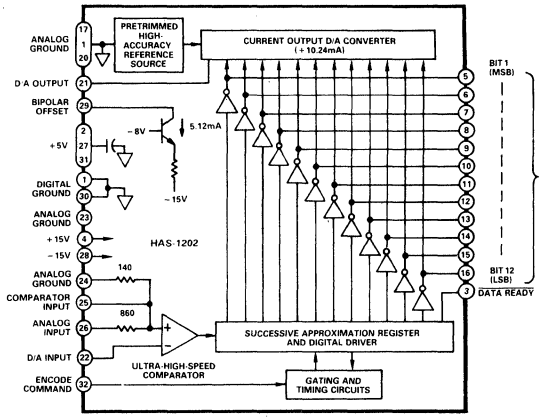
Ultra-Fast Hybrid Analog-to-Digital Converters

HAS-1202/1202A

FEATURES
Conversion Time of 1.56μs (HAS-1202A)
12-Bit Resolution
Conversion Rates to 641kHz
Adjustment-Free Operation

APPLICATIONS
Waveform Analysis
Fast Fourier Transforms
Radar Systems

HAS-1202 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HAS-1202 and improved HAS-1202A A/D Converters are thick-film hybrid 12-bit converters housed in 32-pin ceramic or metal DIP packages. They can be used with high-performance track-and-hold (T/H) amplifiers to solve high-speed, high-resolution digitizing problems economically and feature conversion times of 2.86μs (HAS-1202) and 1.56μs (HAS-1202A).

These converters and the Analog Devices Model HTC-0300A T/H offer designers an opportunity to go from analog to digital with savings in power, board space, design time, and component costs.

They are ideally suited for applications which require excellent performance with a minimum of adjustments. Included in these potential uses are radar systems, PCM, data acquisition systems, and digital signal processing (DSP) systems of various kinds.

The HAS-1202 and HAS-1202A are rated over an operating temperature range of 0 to +70°C and are packaged in 32-pin DIP ceramic housings. The HAS-1202M and HAS-1202AM are rated over a range of −25°C to +85°C and are packaged in metal cases. For metal case units with an operating range of −55°C to +100°C and military screening, order part numbers HAS-1202MB or HAS-1202AMB. Their performance characteristics are identical except for differences in conversion rates; the HAS-1202 is specified for a maximum rate of 349kHz, while the HAS-1202A is capable of operating up to 641kHz.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

		HAS-1202A	HAS-1202
MAXIMUM RATINGS			
Positive Supply (Pin 4)		+16VDC	*
Negative Supply (Pin 28)		−16VDC	*
Logic Supply (Pins 2, 27, 31)		+7VDC	*
Analog Input (Pin 26)		20V	*
Logic Input (Encode Command @ Pin 32)		+7V	*
Temperature			
Operating (Case)		−55°C to +100°C	*
Storage		−55°C to +125°C	*
Parameter	**Units**	**HAS-1202A**	**HAS-1202**
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0.025)	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT	mV	2.5	*
ACCURACY			
Monotonicity		Guaranteed	*
Integral Nonlinearity	LSB	±1/2	*
Differential Nonlinearity	LSB	±1/2	*
Nonlinearity vs. Temperature	ppm/°C	3.5	*
Gain Error	%FS, max	0.8 (0.18)	*
Gain vs. Temperature	ppm/°C	60	*
Gain vs. Power Supply Changes	ppm/mV	2.2	*
DYNAMIC CHARACTERISTICS			
Conversion Rate	kHz, max	641	349
Conversion Time[1]	µs, max	1.56	2.86
vs. Temperature	%/°C	0.08	*
ANALOG INPUT			
Voltage Ranges			
Bipolar	V	±5.12	*
Unipolar	V	0 to +10.24	*
Overvoltage	V, max	20	*
Impedance	Ω, max	1,000 (±20)	*
Offset[2]			
Initial	mV, max	7 (38)	*
vs. Temperature			
Unipolar Input	ppm/°C	7	*
Bipolar Input	ppm/°C	35	*
ENCODE COMMAND INPUT[3]			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Impedance	TTL Loads	1 "S" and 1 "LS"	*
Rise and Fall Times	ns, max	10	*
Width			
Min	ns	50	*
Frequency	kHz	dc to 641	dc to 349
DIGITAL OUTPUT			
Format	Data Bits / Data Ready	12 Parallel; NRZ / 1; RZ	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	5 Standard	*
Coding		Binary (BIN) Offset Bin. (OBN)	
POWER REQUIREMENTS			
+15V ±0.5V	mA (max)	48 (60)	*
−15V ±0.5V	mA (max)	30 (46)	*
+5V ±0.25V	mA (max)	150 (232)	*
Power Dissipation	W, max	1.9 (2.75)	*
TEMPERATURE RANGE[4]			
Operating	°C	0 to +70	*

NOTE: For operating range of −25°C to +85°C, specify HAS-1202M or HAS-1202AM; for operating range of −55°C to +100°C and military screening, specify HAS-1202MB or HAS-1202AMB.

THERMAL RESISTANCE[5]			
Junction to Air, θja (Free Air)	°C/W	38	*
Junction to Case, θjc	°C/W	18	*

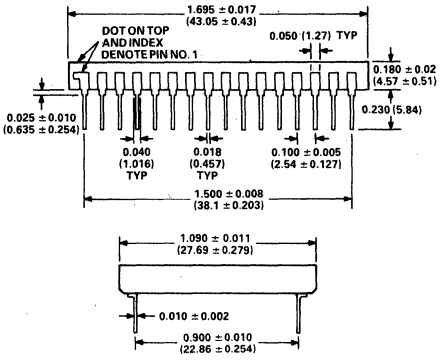
NOTES
*Specifications same as HAS-1202A.
[1]Measured from leading edge of Encode Command to trailing edge of Data Ready with 50ns encode pulse. Conversion time increases equally with increasing width of Encode Command.
[2]Externally adjustable to zero.
[3]Transition from digital "0" to digital "1" initiates encoding.
[4]Case temperature. Metal case HAS-1202M/HAS-1202AM have operating ranges of −25°C to +85°C; HAS-1202MB/HAS-1202AMB have operating ranges of −55°C to +100°C and military screening.
[5]Maximum junction temperature = 150°C.

Specifications subject to change without notice.

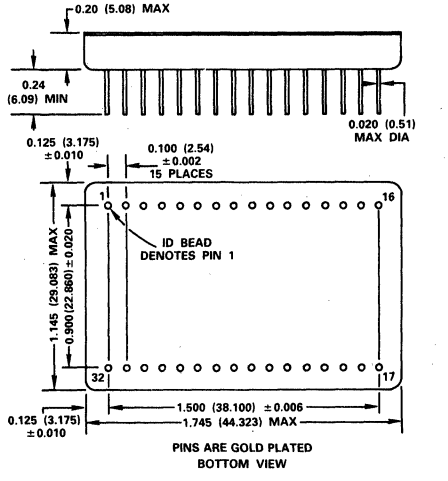
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

CERAMIC PACKAGE



METAL PACKAGE



HAS-1202/1202A PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
32	ENCODE COMMAND	1	DIGITAL GROUND
31	+5V	2	+5V
30	DIGITAL GROUND	3	DATA READY
29	BIPOLAR OFFSET	4	+15V
28	−15V	5	BIT 1 (MSB)
27	+5V	6	BIT 2
26	ANALOG INPUT	7	BIT 3
25	COMPARATOR INPUT	8	BIT 4
24	ANALOG GROUND	9	BIT 5
23	ANALOG GROUND	10	BIT 6
22	D/A INPUT	11	BIT 7
21	D/A OUTPUT	12	BIT 8
20	ANALOG GROUND	13	BIT 9
19	ANALOG GROUND	14	BIT 10
18	ANALOG GROUND	15	BIT 11
17	ANALOG GROUND	16	BIT 12

NOTE
Analog Ground (Pins 17-20; 23; 24) and Digital Ground (Pins 1 and 30) Are Electrically Independent of Each Other. Connect Together Externally and to Low-Impedance Ground Plane as Close to Device as Possible.

ANALOG DEVICES

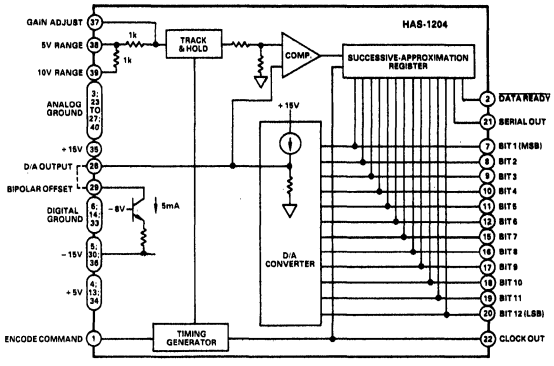
Ultra High-Speed 12-Bit A/D Converter

HAS-1204

FEATURES
12-Bit Resolution
500kHz Word Rates
Internal Track-and-Hold
Single 40-Pin DIP

APPLICATIONS
Medical Instrumentation
Radar Systems
Test Systems
Waveform Analysis
Fast Fourier Transforms

HAS-1204 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HAS-1204 A/D Converter is a *complete* 12-bit hybrid A/D converter in a single 40-pin metal DIP. In this context, "complete" means the unit includes a track-and-hold (T/H) amplifier, encoder, and all the necessary timing circuits. It is a remarkable, self-contained device ready to perform the conversion function without the need for external circuits.

The maximum conversion time of the HAS-1204 is 2.0 microseconds, including the acquisition time of the internal T/H. The large-signal bandwidth of the T/H is 4MHz and the small-signal bandwidth is 7MHz. This combination of characteristics assures that the HAS-1204 will operate at word rates from dc through 500kHz, digitizing analog signals containing frequency components to 250kHz with minimum attenuation or distortion.

Integrating the T/H, encoder, and timing circuits into a single package allows optimum matching of T/H-encoder parameters to obtain the best possible performance. It also lowers the overall power dissipation to 2.85 watts, making the HAS-1204 an ideal choice for designers who face space and/or power restrictions for their designs.

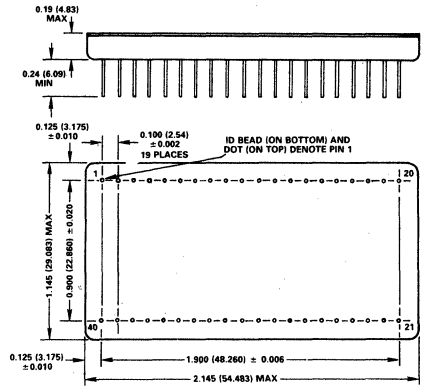
This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Model	Units	HAS-1204BM	HAS-1204SM
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0.024)	*
LSB WEIGHT			
5V Input Range	mV	1.22	*
10V Input Range	mV	2.44	*
ACCURACY			
Linearity @ dc	%FS ± 1/2LSB	0.0125	*
Monotonicity		Guaranteed	*
Nonlinearity vs. Temperature	ppm/°C	3	*
Gain Error	%FS (max)	0.1 (0.7)	*
Gain vs. Temperature	ppm/°C	35	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
(dc to 60kHz)	dB below FS	75	*
(60kHz to 120kHz)	dB below FS	75	*
(120kHz to 200kHz)	dB below FS	70	*
Conversion Rate	kHz	500	*
Conversion Time	µs, max	2.0	*
Aperture Uncertainty (Jitter)	ps	60	*
Aperture Time (Delay)	ns (min/max)	10 (4/18)	*
Signal to Noise Ratio (SNR)[2]	dB	69	*
Transient Response[3]	ns	400	*
Overvoltage Recovery[4]	ns	900	*
Input Bandwidth			
Small Signal, −3dB[5]	MHz	7	*
Large Signal, −3dB[6]	MHz	4	*
Two-Tone Linearity (@ Input Frequencies)[7]			
(37.5kHz; 52.5kHz)	dB below FS	85	*
ANALOG INPUT			
Voltage Ranges	V, FS	0 to −5; 0 to −10 ±5; ±2.5	*
Overvoltage	V, max	2 × FS	*
Impedance			
5V Ranges	Ω (max)	1,000 (±10)	*
10V Ranges	Ω (max)	2,000 (±20)	*
Offset[8]			
Initial–10V Input	mV (max)	10 (60)	*
vs. Temperature (Unipolar)	FS ppm/°C	15	*
vs. Temperature (Bipolar)	FS ppm/°C	50	*
ENCODE COMMAND INPUT[9]			
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Impedance	LS TTL Loads	2	*
Rise and Fall Times	ns, max	10	*
Width			
Min	ns	90	*
Max	ns	160	*
Frequency	kHz	dc to 500	*
DIGITAL OUTPUT[10]			
Format	Data Bits	12 Parallel; NRZ	*
	Data Ready	1; RZ	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*
		"1" = +2.4 to +5	*
Drive	TTL Loads	1 Standard	*
Coding			
Unipolar Mode		Complementary Binary (CBN)	*
Bipolar Mode		Complementary Offset Binary (COB)	*
POWER REQUIREMENTS			
+15V ±0.5V	mA, max	76	*
−15V ±0.5V	mA, max	55	*
+5V ±0.5V	mA, max	177	*
Power Dissipation[11]	W, max	2.85	*
TEMPERATURE RANGE[12]			
Operating	°C	−25 to +85	−55 to +100
Storage	°C	−65 to +150	*
THERMAL RESISTANCE[13]			
Junction to Air, θja			
(Free Air)	°C/W	25	*
Junction to Case, θjc	°C/W	16	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



HAS-1204 PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION
40	ANALOG GROUND	1	ENCODE COMMAND
39	10V RANGE	2	DATA READY
38	5V RANGE	3	ANALOG GROUND
37	GAIN ADJUST	4	+5V
36	−15V	5	−15V
35	+15V	6	DIGITAL GROUND
34	+5V	7	BIT 1 (MSB)
33	DIGITAL GROUND	8	BIT 2
32	FACTORY USE ONLY	9	BIT 3
31	FACTORY USE ONLY	10	BIT 4
30	−15V	11	BIT 5
29	BIPOLAR OFFSET	12	BIT 6
28	D/A OUTPUT	13	+5V
27	ANALOG GROUND	14	DIGITAL GROUND
26	ANALOG GROUND	15	BIT 7
25	ANALOG GROUND	16	BIT 8
24	ANALOG GROUND	17	BIT 9
23	ANALOG GROUND	18	BIT 10
22	CLOCK OUT	19	BIT 11
21	SERIAL OUT	20	BIT 12 (LSB)

NOTES

*Specification same as HAS-1204BM

[1]In-band harmonics expressed in terms of spurious in-band signals generated at 500kHz encode rate at analog input frequencies shown in ( ).

[2]RMS signal to rms noise ratio with 50kHz analog input and encode rate of 500kHz; input signal at −1.0dB.

[3]For full-scale step input, 12-bit accuracy attained in specified time.

[4]Recovers to specified performance in specified time after 2 × FS input voltage.

[5]With analog input 40dB below FS.

[6]With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 1MHz).

[7]Each input frequency applied at a level 7dB below full scale.

[8]Externally adjustable to zero.

[9]Transition from digital "0" to digital "1" initiates encoding.

[10]Use trailing edge of Data Ready pulse to strobe digital outputs into external circuits.

[11]Power dissipation shown is at zero input.

[12]T = Case temperature.

[13]Maximum junction temperature = 150°C. Operating unit requires 500 cubic feet per minute (CFPM) moving air.

Specifications subject to change without notice.

ANALOG DEVICES

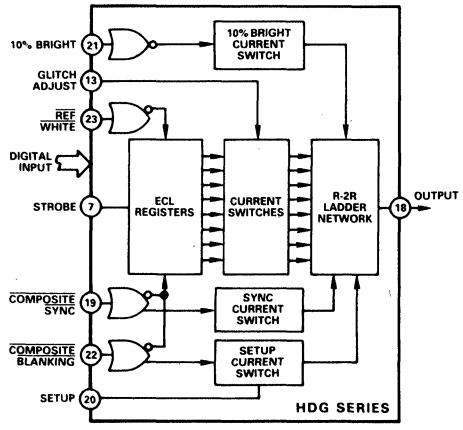
Hybrid Video Digital-to-Analog Converters

HDG SERIES

FEATURES
Update Rates to 150MHz
Low Glitch Energy
Complete Composite Inputs
Single −5.2V Power Supply
Military Temperature Range Available

APPLICATIONS
Raster Scan Displays
Color Graphics
Analytical Instrumentation
TV Video Reconstruction

HDG SERIES FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDG-Series D/A Converters have become the standard of comparison for fast-settling D/A's with complete composite inputs.

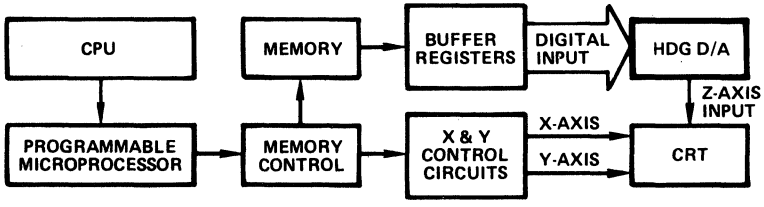
The units are available in three resolutions, or levels, of Gray Scale output. The HDG-0405 accepts four bits (16 levels) of digital input; the HDG-0605 has six bits (64 levels); and the HDG-0805 is an eight-bit (256 levels) device.

All versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Their performance is enhanced even more with a 10% bright input capability.

Output inpedance on all units is 75 ohms and their full-scale output current is capable of developing standard video levels across video loads. In addition to all of these characteristics which make them easy to incorporate into circuits, the need for a single −5.2V power supply also adds to their attractiveness.

Model numbers without suffixes designate the "original" HDG Series D/A Converters and are housed in 24-pin metal packages. Model numbers which include suffixes make use internally of the Analog Devices Model AD9700 to obtain better performance at a lower price; these devices are housed in ceramic DIP packages.

The "BD" and "BW" versions in the newer (suffixed) units are close equivalents to the original design, but a number of advantages accrue by using the newer units. Note particularly the parameters for linearity tempco; strobe input loading; Composite Sync and Composite Blanking outputs; Power Supply Rejection Ratio (PSRR); supply current; and power dissipation. Conversely, the original design is slightly better in terms of voltage settling time, glitch energy, and output compliance.



Typical Raster Scan Display System

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

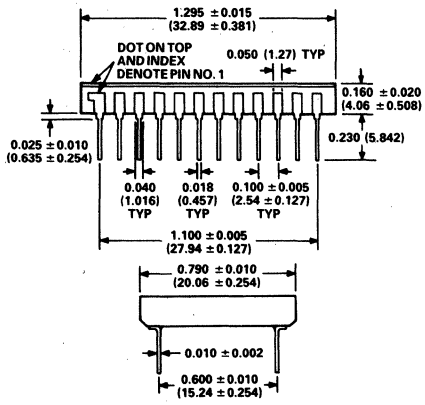
Parameter	Units	HDG-0405	HDG-0605	HDG-0805	HDG-0405BD/BW/SD	HDG-0605BD/BW/SD	HDG-0805BD/BW/SD
RESOLUTION	Bits	4	6	8	4	6	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT							
Voltage (adjustable)	mV	40	10	2.5	40	10	2.5
Current (adjustable)	μA	1067	267	67	1067	267	67
ACCURACY							
(GS = Gray Scale; FS = Full-Scale)							
Linearity	±% GS	3.2	0.8	0.2	3.2	0.8	0.2
Differential Linearity	±% GS, max	3.2	0.8	0.2	3.2	0.8	0.2
Zero Offset (Initial)							
Voltage	mV, max	0.9	*	*	*	*	*
Monotonicity		Guaranteed	*	*	*	*	*
TEMPERATURE COEFFICIENTS							
Linearity	ppm/°C (max)	20 (35)	*	*	15 (30)	**	**
Gain	ppm/°C (max)	50 (125)	*	*	*	*	*
Zero Offset	ppm/°C (max)	10 (15)	*	*	*	*	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]							
Settling Time (0V to FS GS change)	% GS;	6.4	1.6	0.4	6.4	1.6	0.4
Voltage	ns (max)	4 (5)	6 (8)	8 (10)	5 (6)	7 (9)	9 (11)
Update Rate[2]	MHz (min)	150 (125)	*	*	*	*	*
Slew Rate	V/μs	200	*	*	*	*	*
Rise Time	ns	2	*	*	*	*	*
Glitch Energy[3]	pV-s	50	*	*	80	**	**
DIGITAL DATA INPUTS							
Logic Compatibility		ECL	*	*	*	*	*
Coding		Complementary Binary (CBN)	*	*	*	*	*
Logic Levels							
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*	*	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*	*	*	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*	*	*	*	*
STROBE INPUT							
Logic Compatibility		ECL	*	*	*	*	*
Logic Levels							
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*	*	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*	*	*	*
Loading		50pF and 5kΩ to −5.2V	*	*	5pF and 50kΩ to −5.2V	**	**
Setup Time (Data)	ns, min	2.5	*	*	*	*	*
Hold Time (Data)	ns, min	1.5	*	*	*	*	*
Propagation Delay	ns (max)	3 (4)	*	*	*	*	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS							
Logic Compatibility		ECL	*	*	*	*	*
Logic Levels							
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*	*	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*	*	*	*
Loading		5pF and 50kΩ to −5.2V	*	*	*	*	*
SPEED PERFORMANCE – CONTROL INPUTS							
Settling Time to 10% of Final Value for:							
10% Bright	ns (max)	8 (10)	*	*	*	*	*
Reference White	ns (max)	8 (10)	*	*	*	*	*
Composite Sync	ns (max)	8 (10)	*	*	*	*	*
Composite Blanking	ns (max)	8 (10)	*	*	*	*	*
SETUP CONTROL							
Ground	mV (IRE Units)	0 (0)	*	*	*	*	*
Open	mV (IRE Units)	71 (10)	*	*	*	*	*
−5.2V	mV (IRE Units)	142 (20)	*	*	*	*	*
ANALOG OUTPUT							
GS Current	mA (±1%)	0 to −16	0 to −16.8	0 to −17	0 to −16	0 to −16.8	0 to −17
GS Voltage[4]	mV	0 to −600	0 to −630	0 to −637.5	0 to −600	0 to −630	0 to −637.5
Compliance	V	−1.1 to +1.1	*	*	−1.2 to +0.1	**	**
Internal Impedance	Ω (min/max)	75 (71/79)	*	*	*	*	*

Parameter	Units	HDG-0405	HDG-0605	HDG-0805	HDG-0405BD/ BW/SD	HDG-0605BD/ BW/SD	HDG-0805BD/ BW/SD
OUTPUT – REFERENCE WHITE[5]							
Current							
Logic "1"	mA (±4%)	Normal Operation	*	*	*	*	*
Logic "0"	mA (±4%)	0 or −1.9	*	*	*	*	*
Voltage							
Logic "1"	mV (±4%)	Normal Operation	*	*	*	*	*
Logic "0"	mV (±4%)	0 or −71					
OUTPUT – 10% BRIGHT[6]							
Current							
Logic "1"	mA (±5%)	−1.9	*	*	*	*	*
Logic "0"	mA (±5%)	0	*	*	*	*	*
Voltage							
Logic "1"	mV (±5%)	−71	*	*	*	*	*
Logic "0"	mV (±5%)	0	*	*	*	*	*
OUTPUT – COMPOSITE SYNC[6,7]							
Current							
Logic "1"	mA (±4%)	0	*	*	*	*	*
Logic "0"	mA (±4%)	−7.6	*	*	−8.6	−7.8	−7.6
Voltage							
Logic "1"	mV (±4%)	0	*	*	*	*	*
Logic "0"	mV (±4%)	−285	*	*	−322.5	−292.5	−285
OUTPUT – COMPOSITE BLANKING[6,7] (Assumes Setup is Open, Which is Equiavalent to 10 IRE Units)							
Current							
Logic "1"	mA (±4%)	0	*	*	*	*	*
Logic "0"	mA (±4%)	−1.9	*	*	−2.9	−2.1	−1.9
Voltage							
Logic "1"	mV (±4%)	0	*	*	*	*	*
Logic "0"	mV (±4%)	−71	*	*	−108.7	−78.7	−71
POWER REQUIREMENTS							
−5.2V ±0.25V[8]	mA (max)	200 (225)	260 (290)	320 (360)	125 (140)	**	**
Power Supply Rejection Ratio	%/%	1/1	*	*	0.005/1	**	**
Power Dissipation	mW (max)	1040 (1170)	1350 (1510)	1665 (1875)	650 (730)	**	**
TEMPERATURE RANGE							
Operating (Case)[9]	°C	−25 to +85	*	*	* (BD and BW)	* (BD and BW)	* (BD and BW)
Operating ("SD" Case)	°C				−55 to +125	−55 to +125	−55 to +125
Storage	°C	−55 to +150	*	*	*	*	*
THERMAL RESISTANCE[10]							
Junction to Air, θ_{ja} (free air)	°C/W, max	45	*	*	*	*	*
Junction to Case, θ_{jc}	°C/W, max	12	*	*	*	*	*
MTBF[11] Mean Time Between Failures	Hours						3.23×10^5

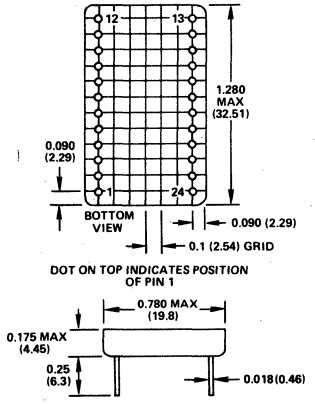
NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]Minimum update rates limited by full-scale settling time for useable number of bits for each converter.
Units can be updated to 150MHz with settling degradation.
[3]Glitch can be reduced with glitch adjustment.
[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.
[5]Effect on analog output of logic "0" at Reference White input depends on 10% Bright signal input.
[6]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 18.
[7]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White.
[8]Power supply must have less than 5mV p-p ripple.
[9]Operating temperature −55°C to +125°C on "SD" units.
[10]Maximum junction temperature = 150°C.
[11]Calculated for HDG-0805SDB using MIL HNBK-217; Ground Fixed; +25°C Ambient.
* Specification same as HDG-0405.
** Specification same as HDG-0405BD/BW/SD.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



24-PIN CERAMIC DIP PACKAGE



24-PIN METAL CASE HYBRID PACKAGE

PIN DESIGNATIONS

Pin	Function	Pin	Function
12	GROUND	13	GLITCH ADJUST
11	BIT 8 (LSB)	14	GROUND
10	BIT 7	15	GROUND
9	BIT 6	16	GROUND
8	BIT 5	17	GROUND
7	STROBE	18	ANALOG OUTPUT
6	BIT 4	19	COMPOSITE SYNC
5	BIT 3	20	SETUP
4	BIT 2	21	10% BRIGHT
3	BIT 1 (MSB)	22	COMPOSITE BLANKING
2	−5.2V	23	REFERENCE WHITE
1	GROUND	24	−5.2V

NOTES: For HDG-0605 units, Pin 9 is LSB; Pins 10 and 11 are present but not used. For HDG-0405 units, Pin 6 is LSB; Pins 8, 9, 10, and 11 are present but not used. Connect Pins 1, 12, and 14–17 together and to low-impedance ground plane as close to case as possible.

USING HDG-SERIES UNIT FOR RASTER SCAN

Refer to the block diagram of the HDG-Series D/A Converter and the idealized composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. For HDG-0405 units, there are 16 (2^4) of these levels; for the HDG-0605, 64 (2^6) levels; and for the HDG-0805, 256 (2^8) levels.

The input bits are applied to Pins 3–6 (only, for the HDG-0405), and Pins 8 and 9 for the HDG-0605; or Pins 8–11 for the HDG-0805.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, Reference White, Composite Sync, and Composite Blanking; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

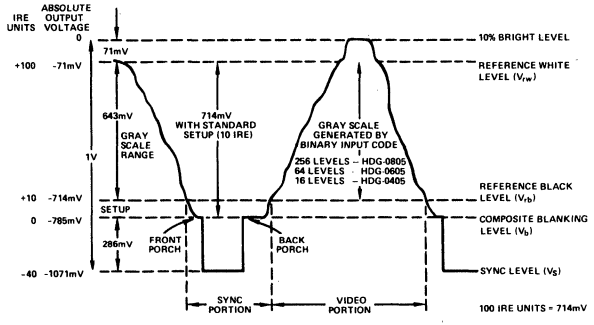


Figure 1. Composite Output Waveform

ANALOG DEVICES

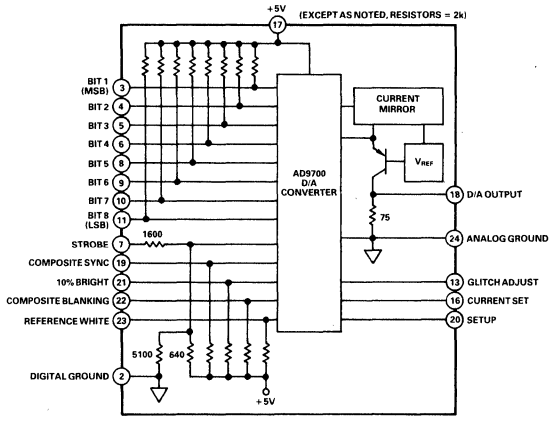
Hybrid Video Digital-to-Analog Converters

HDG-0407/0807

FEATURES
- Update Rates to 50MHz
- Low Glitch
- Complete Composite Inputs
- Single +5V Power Supply
- TTL-Compatible Inputs
- Directly Drives 75Ω to Ground

APPLICATIONS
- Raster Scan Displays
- Color Graphics
- Analytical Instrumentation
- TV Video Reconstruction

HDG-0807 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

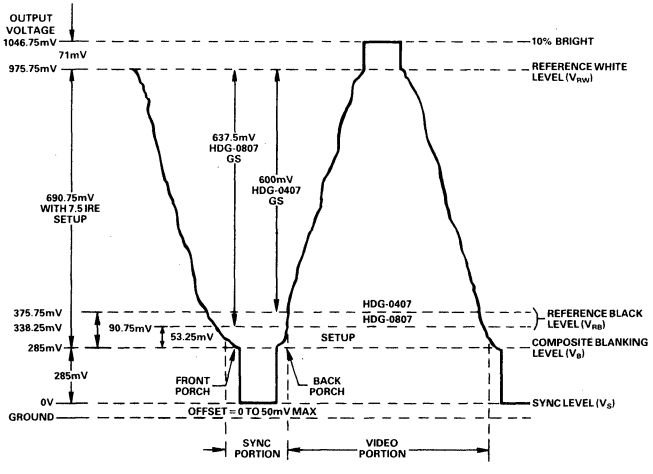
The HDG-0807/0407 D/A Converters are extensions of the technology and capabilities of the HDG-Series high-speed raster scan D/A converters. They offer the user increased flexiblity because of their ability to operate on a single +5V power supply, and their compatibility with TTL signals.

The units are available in two resolutions, or levels, of Gray Scale output. The HDG-0407 accepts four bits (16 levels) of digital input; and the HDG-0807 is an eight-bit (256 levels) device.

All versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Performance is enhanced even more with a 10% bright input capability.

Output impedance is 75Ω and the full-scale output current is capable of developing standard video levels across video loads. An output current mirror shifts the output to ground reference while attenuating power supply noise by means of common-mode rejection.

Model numbers with "BW" suffixes are housed in 24-pin non-hermetic ceramic dual-in-line packages. Versions with "BD" suffixes are housed in hermetically-sealed ceramic DIP packages.



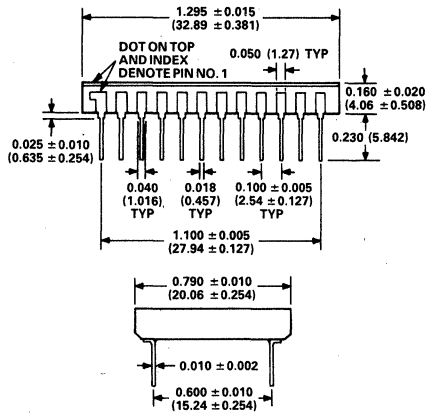
HDG-0407/0807 Composite Waveform

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDG-0407BD/BW	HDG-0807BD/BW
RESOLUTION	Bits	4	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (adjustable)	mV	40	2.5
Current (adjustable)	μA	1067	67
ACCURACY			
(GS = Gray Scale; FS = Full-Scale)			
Linearity	±% GS	3.2	0.2
Differential Linearity	±% GS, max	3.2	0.2
Zero Offset (Initial)			
Voltage	mV, max	50	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C (max)	15 (30)	*
Gain	ppm/°C (max)	350 (1,000)	*
Zero Offset	mV/°C (max)	1.0 (2.0)	*
DYNAMIC CHARACTERISTICS – GS OUTPUT[1]			
Settling Time	% GS;	6.4	0.4
1LSB Midscale Voltage Change	ns (max)	8 (10)	14 (16)
0V to FS GS Voltage Change	ns (max)	10 (12)	15 (18)
Slew Rate	V/μs	250	*
Rise Time	ns	2.2	*
Glitch Impulse[2]	pV-s	50	*
DIGITAL DATA INPUTS			
Logic Compatibility		TTL	*
Coding		Binary (BIN)	*
Logic Levels[3]			
"1"	V (min/max)	(+3.8/+5.0)	*
"0"	V (min/max)	(0/+3.0)	*
Loading (each bit)		5pF and 2kΩ to +5V	*
Data Update Rate	MHz (Guaranteed)	50 (45)	*
STROBE INPUT			
Logic Compatibility		TTL	*
Logic Levels			
"1"	V (min/max)	(+2.5/+5.0)	*
"0"	V (min/max)	(0/+1.5)	*
Loading		1pF and 2.2kΩ to +4.4V	*
Setup Time (Data)	ns, min	3	*
Hold Time (Data)	ns, min	3	*
Propagation Delay	ns (max)	8	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		TTL	*
Logic Levels			
"1"	V (min/max)	(+3.8/+5)	*
"0"	V (min/max)	(0/+3.5)	*
Loading		5pF and 2kΩ to +5V	*
SPEED PERFORMANCE – CONTROL INPUTS			
Settling Time to 10% of Final Value for:			
10% Bright	ns (max)	15	*
Reference White	ns (max)	15	*
Composite Sync	ns (max)	15	*
Composite Blanking	ns (max)	15	*
SETUP CONTROL			
+5V	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	53.25 (7.5)	*
ANALOG OUTPUT			
GS Voltage p-p[4]	mV (±4%)	600	637.5
Compliance	V	−3 to +3	−3 to +3
Internal Impedance	Ω (min/max)	75 (71/79)	*
OUTPUT – REFERENCE WHITE[5] (Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)			
Voltage			
Logic "1"	mV (±4%)	Normal Operation	*
Logic "0"			
10% Bright @ "0"	mV	1046.75	*
10% Bright @ "1"	mV	975.75	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



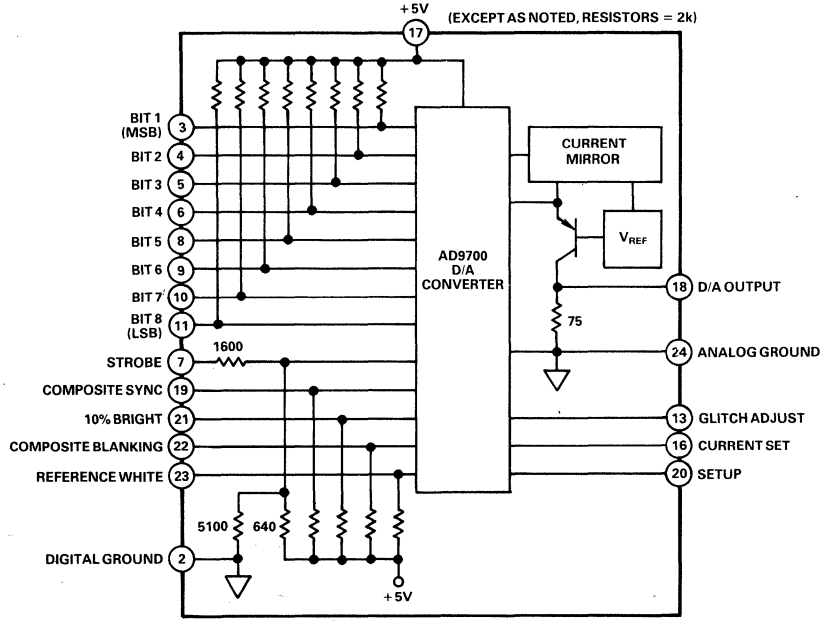
PIN DESIGNATIONS (As Viewed from Bottom)

Pin	Function	Pin	Function
24	ANALOG GROUND	1	+5V
23	REFERENCE WHITE	2	DIGITAL GROUND
22	COMPOSITE BLANKING	3	BIT 1 (MSB)
21	10% BRIGHT	4	BIT 2
20	SETUP	5	BIT 3
19	COMPOSITE SYNC	6	BIT 4
18	ANALOG OUTPUT	7	STROBE
17	+5V	8	BIT 5
16	+5V	9	BIT 6
15	+5V	10	BIT 7
14	+5V	11	BIT 8 (LSB)
13	GLITCH ADJUST	12	+5V

NOTES: For HDG-0407 units, Pin 6 is LSB; Pins 8, 9, 10 and 11 are present but not used. For both units, connect Pins 2 and 24 together and to low-impedance ground plane as close to case as possible. +5V must be applied to all designated pins.

Parameter	Units	HDG-0407BD/BW	HDG-0807BD/BW
OUTPUT – $\overline{\text{10\% BRIGHT}}$[6]			
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	71	*
OUTPUT – $\overline{\text{COMPOSITE SYNC}}$[6,7]			
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	285	*
OUTPUT – $\overline{\text{COMPOSITE BLANKING}}$[6,7]			
(Assumes Setup is Open)			
Voltage			
Logic "1"	mV (±4%)	0	*
Logic "0"	mV (±4%)	90.75	53.25
POWER REQUIREMENTS			
+5V to ±0.25V	mA (max)	185 (225)	185 (225)
Power Supply			
Rejection Ratio	%/V	0.025/0.25	0.025/0.25
Power Dissipation	mW (max)	925 (1125)	925 (1125)
TEMPERATURE RANGE			
Operating (Case)	°C	−25 to +85	*
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[8]			
Junction to Air, θ_{ja} (free air)	°C/W, max	45	*
Junction to Case, θ_{jc}	°C/W, max	12	*

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]Glitch can be reduced with glitch adjustment.
[3]Internal 2k pull-up resistors help assure compatibility with logic levels of multiple TTL families.
[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.
[5]Effect on analog output of logic "0" at Reference White input depends on 10% Bright signal input.
[6]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 18 and are measured with respect to sync level (V_S) shown in waveform.
[7]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White, which sets input registers.
[8]Maximum junction temperature = 150°C.
* Specification same as HDG-0407.
Specifications subject to change without notice.



HDG-0807 Block Diagram

THEORY OF OPERATION

Refer to the block diagram of the HDG-0807 D/A Converter and the HDG-0407/0807 composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. For HDG-0407 units, there are 16 (2^4) of these levels; and for the HDG-0807, 256 (2^8) levels.

Input bits are applied to Pins 3-6 and Pins 8-11 for the HDG-0807; for the HDG-0407, only Pins 3-6 are used.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the TTL levels at the control inputs of $\overline{10\%\ Bright}$, $\overline{Reference\ White}$, $\overline{Composite\ Sync}$, and $\overline{Composite\ Blanking}$; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs, and various combinations of control inputs are selected.

Refer to Table I.

Analog Devices uses 2.5mV for weighting the LSB during calibration of the converter, which causes the full-scale 637.5mV output of the HDG-0807 to be different from the ideal 643mV output shown in the composite waveform in the RS-170 standard.

This disparity does not cause any problems in using the device, since both the ideal value and the actual value are well within the tolerances of the output and the RS-170 standard.

Referring again to the block diagram, the Strobe input applied to the HDG D/A clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize perturbations or "glitches" in the analog output signal.

A logic "0" applied to either the $\overline{Composite\ Sync}$ or $\overline{Composite\ Blanking}$ input resets the input registers to 00 000 000. A logic "0" signal applied to the $\overline{Reference\ White}$ input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the converter goes to 1046.75mV or to 975.75mV, depending upon whether or not the $\overline{10\%\ Bright}$ signal is also operated.

When $\overline{Composite\ Blanking}$ is operated, the analog output will go to a Reference Black value of 338.25mV less some amount, as determined by the voltage at Setup. The 53.25mV example used in the Specifications section of the data sheet is based on the Setup input floating, which is equivalent to 7.5 IRE units. (For this example, the analog output would be 285mV.)

DIGITAL INPUTS VS. ANALOG OUTPUT

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	$\overline{10\%\ BRIGHT}$	$\overline{REF.\ WHITE}$	$\overline{BLANK\text{-}ING}$	$\overline{COMP.\ SYNC}$	ANALOG OUTPUT IN mV[1] (HDG-0807)
1	1	1	1	1	1	1	1	0	1	1	1	1046.75
1	1	1	1	1	1	1	1	1	1	1	1	975.75
1	0	0	0	0	0	0	0	0	1	1	1	729.25
0	0	0	0	0	0	0	0	0	1	1	1	409.25
0	0	0	0	0	0	0	0	1	1	1	1	338.25
X	X	X	X	X	X	X	X	0	0	1	1	1046.75
X	X	X	X	X	X	X	X	1	0	1	1	975.75
X	X	X	X	X	X	X	X	0	1	0	1	338.25[2]
X	X	X	X	X	X	X	X	0	1	0	1	285[3]
X	X	X	X	X	X	X	X	0	1	0	0	124.25[2]
X	X	X	X	X	X	X	X	0	1	0	0	71[3]
X	X	X	X	X	X	X	X	1	1	0	0	53.25[2]
X	X	X	X	X	X	X	X	1	1	0	0	0[3]

NOTES
[1]Values are for Gray Scale output of HDG-0807 measured with respect to Sync level. HDG-0407 Gray Scale output is 37.5mV less tha 8-bit output.
[2]Setup (Pin 20) to +5V. (0 IRE units)
[3]Setup (Pin 20) open. (7.5 IRE units)

Table I. Digital Inputs vs. Analog Output

APPLICATIONS

The HDG-0407 and HDG-0807 are specifically designed for operation in raster scan graphics applications, in which digital input data are being changed at a relatively high rate.

The D/A output is generally ac-coupled to the monitor, which eliminates the changing dc offset associated with the thermal drift of the level shift circuits. This offset drift, which is a function of output level, is held to a maximum of 50mV and will not affect dynamic video levels.

For optimum performance, ground pins 2 and 24 should be connected together and to a large ground plane near the unit. As indicated in the footnotes on the pin designations table, +5V must be applied to all pins which are called out to receive it.

The performance of the HDG devices can be enhanced with external bypass capacitors which will supplement the internal components. Low-frequency bypassing should be provided with 1μF (or larger) tantalum capacitors between the +5V supply pins and ground. High-frequency bypassing can be provided with ceramic capacitors of 0.1μF or larger. All bypass capacitors should be tied as closely as possible to the hybrid power supply pins.

A 200Ω potentiometer between +5V and ground with the center arm connected to Pin 13 changes the threshold of the internal current switches; this can reduce the amount of glitch from the typical 50pV-s to a lesser value when required.

For best performance, standard 24-pin hybrid sockets should be avoided. Individual pin sockets are preferable for evaluating devices and are available from Analog Devices; in final designs, the D/A should be soldered directly into the printed circuit board without sockets.

If it is necessary to route digital signals and/or strobe signals for distances greater than one inch (2.54cm), microstrip techniques should be used. Otherwise, the performance of the D/A converter may be affected adversely.

ORDERING INFORMATION

There are two versions of the 4-bit converter, and two versions of the 8-bit device; all units operate over a temperature range of −25°C to +85°C. For 4-bit operation, order the HDG-0407BD or HDG-0407BW; for 8-bit converters, the model numbers are HDG-0807BD or HDG-0807BW. In these model numbers, the "D" in the suffix indicates a ceramic, hermetically-sealed DIP; and the "W" indicates a non-hermetic ceramic DIP.

Versions are available screened to military requirements; contact the factory for details. It is also possible to order units with synchronous functions on a "special order" basis; detailed information is available from the factory.

ANALOG DEVICES

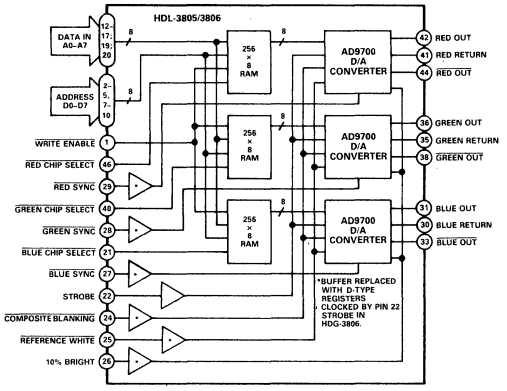
Hybrid Video Digital-to-Analog Converters

HDL-3805/3806

FEATURES
Triple 8-Bit D/A with LUTs
115MHz Update Rates
RGB Composite Functions
Small Size (2.3" × 1.5")
Latched Composite Functions (HDL-3806)

APPLICATIONS
Raster Scan Displays
Color Graphics Systems

HDL-3805/3806 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

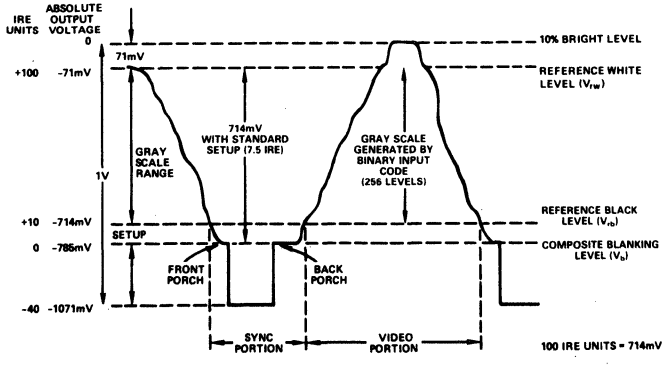
The HDL-3805 D/A Converter is a thick-film hybrid which includes three AD9700 IC D/A converters and three ECL random access memory (RAM) look-up tables in a single package. It is the smallest, lowest-power RGB (red, green, blue) video generator available to video designers of high-resolution raster scan graphics displays.

With eight bits of Gray scale resolution per channel, the user has a total palette of 16.7 million colors. Since each of the three DACs has a 256 × 8 RAM, a total of 256 colors is available on each sweep. The write speed of the RAMS is sufficiently high to rewrite the color map completely during vertical retrace, or update smaller blocks of data during horizontal retrace.

Composite functions in the HDL units include Red Sync, Green Sync, Blue Sync, Composite Blanking, Reference White, and 10% Bright. The ability of the devices to drive 75Ω loads directly with a 1V composite signal combines with these functions to assure the outputs will be compatible with the general requirements of EIA Standards RS-170 and RS-343.

The model HDL-3806 D/A Converter is a variation of the HDL-3805 which includes synchronous composite functions and offers increased flexibility for the designer in a pin-for-pin compatible package.

All models of the HDL-3805 and HDL-3806 are housed in 46-pin metal hybrid packages. Standard versions are rated over an operating temperature range of −25°C to +85°C; for units with this range and military screening, consult factory.



Idealized Composite Output Waveform

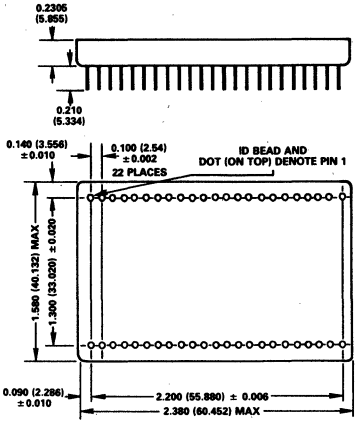
This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDL-3805BM	HDL-3806BM	HDL-3806CM
RESOLUTION	Bits	8	*	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT				
Voltage	mV	2.5	*	*
Current	µA	67	*	*
ACCURACY				
(GS = Gray Scale; FS = Full-Scale)				
Linearity	±% GS	0.2	*	*
Differential Linearity	±% GS	0.2	*	*
Integral Linearity	±% GS, max	0.2	*	*
Zero Offset (Initial)	mV, max	1.5	*	*
Monotonicity		Guaranteed		
TEMPERATURE COEFFICIENTS				
Linearity	ppm/°C (max)	30	*	*
Gain	ppm/°C (max)	125	*	*
Zero Offset	ppm/°C (max)	15	*	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]				
Settling Time to 0.4% GS; 0V to 637.5mV GS Change				
Voltage	ns (max)	10 (12)	*	*
Output Time Skew				
(Among RGB Outputs)	ns, max	2	*	*
Update Rate	MHz (min)	100 (85)	*	(115)
Slew Rate	V/µs, min	300	*	*
Rise Time	ns (max)	2 (3)	*	*
Glitch Energy	pV-s	80	*	*
Crosstalk				
(Among RGB Outputs)	±% GS	0.2	*	*
Clock Noise on RGB Outputs				
(With 100MHz Filter)	mV	10	*	*
DIGITAL DATA INPUTS				
Logic Compatibility		ECL	*	*
Coding		Complementary Binary (CBN)	*	*
Logic Levels				
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*
Loading				
Data and Address	µA/pF	650/45	*	*
$\overline{\text{RGB Chip Select}}$	µA/pF	880/18	*	*
$\overline{\text{Write Enable}}$	µA/pF	650/65	*	*
$\overline{\text{RGB Sync, Composite Blanking}}$				
Reference White, or 10% Bright	µA/pF	290/10	*	*
Strobe	µA/pF	50/5	*	*
SPEED PERFORMANCE – CONTROL INPUTS				
(Standard Setup Control = 7.5 IRE Units = 53.25mV)				
Settling Time to 10% of Final Value for:				
10% Bright	ns, max	10	*	*
$\overline{\text{Reference White}}$	ns, max	10	*	*
$\overline{\text{RGB Sync}}$	ns, max	10	*	*
$\overline{\text{Composite Blanking}}$	ns, max	10	*	*
ANALOG OUTPUTS (Red, Green, and Blue)				
GS Current[2]	mA	0 to −17	*	*
GS Voltage[3]	mV (±1%)	0 to −637.5	*	*
Compliance	V	−1.2 to +0.1	*	*
Internal Impedance	Ω (min/max)	75 (71/79)	*	*
$\overline{\text{REFERENCE WHITE}}$[4]				
Current				
Logic "1"	mA (±5%)	Normal Operation	*	*
Logic "0"	mA (±5%)	0 or −1.9	*	*
Voltage				
Logic "1"	mV (±5%)	Normal Operation	*	*
Logic "0"	mV (±5%)	0 or −71	*	*
10% BRIGHT[5]				
Current				
Logic "1"	mA (±5%)	−1.9	*	*
Logic "0"	mA (±5%)	0	*	*
Voltage				
Logic "1"	mV (±5%)	−71	*	*
Logic "0"	mV (±5%)	0	*	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

(Bottom View)

PIN	FUNCTION	PIN	FUNCTION
46	$\overline{\text{RED CHIP SELECT}}$	1	WRITE ENABLE
45	DIGITAL GROUND	2	ADDRESS A_7 (MSB)
44	$\overline{\text{RED OUT}}$	3	ADDRESS A_6
43	V_{EE} (−5.2V)	4	ADDRESS A_5
42	RED OUT	5	ADDRESS A_4
41	RED RETURN	6	V_{EE} (−5.2V)
40	$\overline{\text{GREEN CHIP SELECT}}$	7	ADDRESS A_3
39	DIGITAL GROUND	8	ADDRESS A_2
38	$\overline{\text{GREEN OUT}}$	9	ADDRESS A_1
37	V_{EE} (−5.2V)	10	ADDRESS A_0 (LSB)
36	GREEN OUT	11	DIGITAL GROUND
35	GREEN RETURN	12	DATA IN D_7 (MSB)
34	DIGITAL GROUND	13	DATA IN D_6
33	$\overline{\text{BLUE OUT}}$	14	DATA IN D_5
32	V_{EE} (−5.2V)	15	DATA IN D_4
31	BLUE OUT	16	DATA IN D_3
30	BLUE RETURN	17	DATA IN D_2
29	$\overline{\text{RED SYNC}}$	18	V_{EE} (−5.2V)
28	$\overline{\text{GREEN SYNC}}$	19	DATA IN D_1
27	$\overline{\text{BLUE SYNC}}$	20	DATA IN D_0 (LSB)
26	10% BRIGHT	21	$\overline{\text{BLUE CHIP SELECT}}$
25	$\overline{\text{REFERENCE WHITE}}$	22	STROBE
24	$\overline{\text{COMPOSITE BLANKING}}$	23	DIGITAL GROUND

NOTES: GROUNDS ARE NOT CONNECTED INTERNALLY. CONNECT PINS 11, 23, 30, 34, 35, 39, 41, AND 45 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE. −5.2V MUST BE APPLIED TO ALL DESIGNATED PINS.

Parameter	Units	HDL-3805BM	HDL-3806BM	HDL-3806CM
COMPOSITE SYNC[5,6]				
(Applied to RED SYNC, GREEN SYNC, or BLUE SYNC Input Pins)				
Current				
Logic "1"	mA (±4%)	0	*	*
Logic "0"	mA (±4%)	−7.6	*	*
Voltage				
Logic "1"	mV (±4%)	0	*	*
Logic "0"	mV (±4%)	−285	*	*
COMPOSITE BLANKING[5,6]				
(Standard Setup Control = 7.5 IRE Units = 53.25mV)				
Current				
Logic "1"	mA (±4%)	0	*	*
Logic "0"	mA (±4%)	−1.4	*	*
Voltage				
Logic "1"	mV (±4%)	0	*	*
Logic "0"	mV (±4%)	−53.25		
POWER REQUIREMENTS				
−5.2V ±0.25V	mA, max	1450	*	*
Power Dissipation[7]	W, max	7.55	*	*
Power Supply Rejection Ratio	%GS/V	0.025/0.25	*	*
TEMPERATURE RANGE				
Operating (Case)	°C	−25 to +85	*	*
Storage	°C	−55 to +150	*	*
THERMAL RESISTANCE[8]				
Junction to Air, θ_{ja} (Free Air)	°C/W, max	12	*	*
Junction to Case, θ_{jc}	°C/W, max	2.5	*	*

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]GS current = FS current − video functions.
[3]LSB value of 2.5mV used for calibration. This causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform elsewhere in this data sheet; both values are well within the output and EIA Standard RS-343 tolerances.
[4]Effect on analog output of Logic "0" at Reference White input depends on 10% Bright signal input.
[5]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 31, 36, or 42.
[6]Red Sync, Green Sync, Blue Sync, or Composite Sync control signals reset input registers. Neither the RGB Sync signals nor the Composite Sync should be operated simultaneously with Reference White.
[7]Air flow of 500 LFPM required when operating unit.
[8]Maximum junction temperature = 150°C.
*Specification same as HDL-3805BM.
Specifications subject to change without notice.

ORDERING INFORMATION

There is one standard model of the HDL-3805 D/A converter, and two model numbers for the HDL-3806 version. Specifically, the designations are HDL-3805BM; and HDL-3806BM and HDL-3806CM. The HDL-3805 unit operates with unlatched asynchronous composite inputs; and both models of the HDL-3806 operate with latched synchronous signals.

In terms of speed, the HDL-3805BM and HDL-3806BM are identical with minimum update rates of 85MHz, and typical word rates of 100MHz. The HDL-3806CM is specified at a minimum update rate of 115MHz.

Standard units operate over a case temperature range of −25°C to +85°C; units with the same temperature range and military screening are also available. For these, consult the factory.

Theory of Operation

Refer to the block diagram of the HDL-3805/3806 D/A Converter.

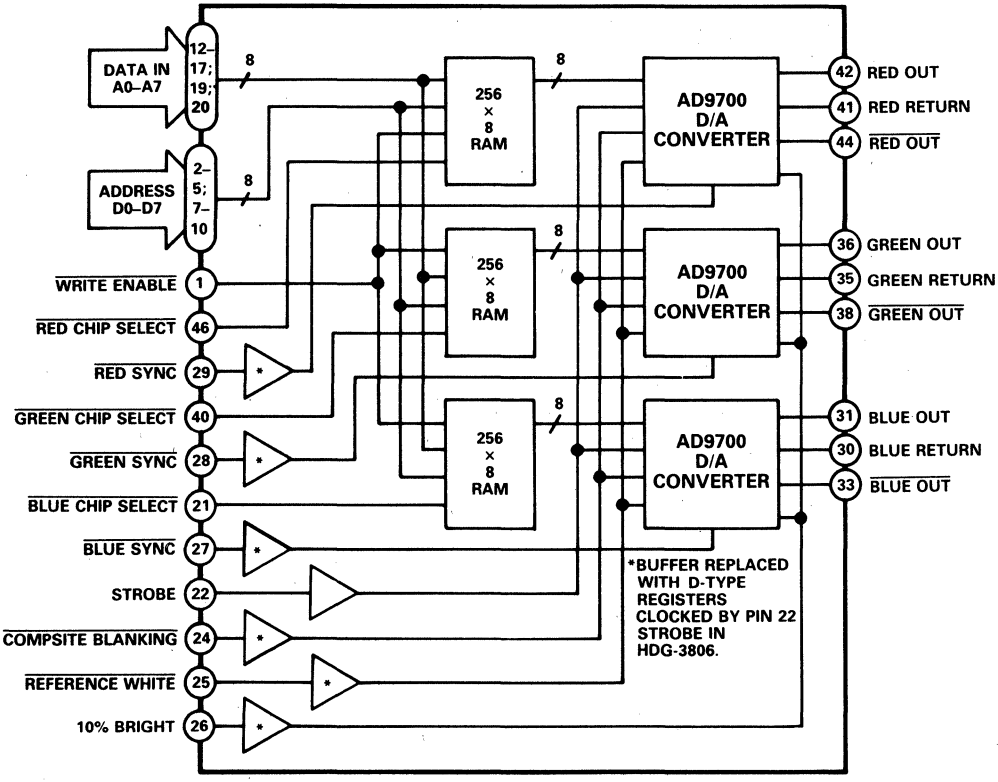
As shown, the unit is comprised of three each random access memories (RAMs) and AD9700 current output D/A converters. These components operate as three pairs in controlling the red, green, and blue (RGB) analog outputs of the device; and greatly simplify the interface between the frame buffers and the monitor in raster scan graphics systems.

RGB digital data information can be loaded into the RAMs during retrace periods. During horizontal retrace intervals, small blocks of data can be entered; the complete color map can be rewritten during the longer vertical retrace times.

Intensities for the RGB outputs are updated by a single 8-bit address word and a Strobe signal during the RAM read operations.

The routing of the digital data to the correct RAM and its associated D/A is controlled by the digital Address input Signals; and by the $\overline{\text{Red Chip Select}}$, $\overline{\text{Green Chip Select}}$, $\overline{\text{Blue Chip Select}}$, and $\overline{\text{Write Enable}}$ signals.

In addition to digital input and address information, the user of the HDl-3805/3806 also has control over composite functions with $\overline{\text{Red Sync}}$, $\overline{\text{Green Sync}}$, $\overline{\text{Blue Sync}}$, $\overline{\text{Composite Blanking}}$, $\overline{\text{Reference White}}$, and 10% Bright.



HLD-3805/3806 Block Diagram

ANALOG DEVICES

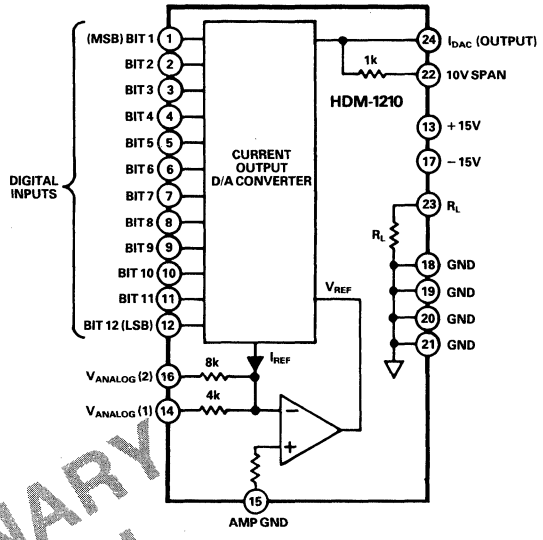
Ultra High-Speed Multiplying D/A Converter

HDM-1210

FEATURES
Small Size: 24-Pin DIP
12-Bit Multiplying Accuracy
Good Drive: 10.24mA
Highest Speed Available

APPLICATIONS
CRT Displays
Waveform Generation
Vector Generation
MHz-Rate Digital Attenuators

HDM-1210 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDM-1210 converter is an ultra-high-speed current output multiplying converter which offers circuit designers a chance to obtain high speed, good drive, and flexible design parameters in a DIP package. It can accept 12 bits of digital input data and combine them with two analog inputs into a multiplied output for use in a wide variety of applications.

Typical analog settling time to 1% is only 150ns; and 3dB analog bandwidth is 10MHz. Digital settling time to 1% accuracy at the major carry transition is an incredible 60ns, making the HDM-1210 D/A extremely attractive for a range of high-speed multiplying functions.

In one mode of operation, its output current is precisely proportional to the analog input signal, multiplied by the digital input code. The analog signal being multiplied can be a sine wave, triangle wave, sawtooth, or any one of a variety of complex waveforms. The output is an accurate scaled version of the input, with the digital input used as the scale factor.

In another mode of operation, the analog input voltage can be used as the scale factor for the digital input code. In addition to this kind of flexibility, the HDM-1210 also has various offsetting capabilities which allow the analog input, digital input, analog output, and/or an external amplifier to be combined. With these features, the HDM-1210 can be used to accommodate unipolar or bipolar operation; and provide either one-quadrant or two-quadrant multiplication.

PRELIMINARY TECHNICAL DATA

SPECIFICATIONS (typical @ +25°C with nominal power supplies; V_{ANALOG} (1) = −5V; and V_{ANALOG} (2) = 0V unless otherwise noted)

Parameter	HDM-1210BD	HDM-1210SD/SDB	Units
RESOLUTION	12	*	Bits
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Current	2.5	*	μA
Voltage	250	*	μV
ACCURACY (FS = Full Scale)			
Differential Linearity	±1/2	*	LSB
Integral Linearity	±1/2	*	LSB
Gain	±0.2 (±0.5)	*	% FS (max)
Monotonicity	Guaranteed	*	
TEMPERATURE COEFFICIENTS			
Differential Linearity	±3 (±6)	*	ppm/°C (max)
Integral Linearity	±3	*	ppm/°C
Gain	±20 (±50)	*	ppm/°C (max)
Offset[1,2]	±2 (±5)	*	ppm/°C (max)
Offset[1,3]	±3.5 (±8)	*	ppm/°C (max)
DYNAMIC CHARACTERISTICS			
Settling Time – Voltage			
Digital			
(To ±1%; Major Carry Transition)	60 (70)	*	ns (max)
Analog Settling to ±1% FS			
(V_{ANALOG} (1) = 0V to −5V Step;			
All Digital Inputs (@ "1")	150 (175)	*	ns (max)
Update Rate	8.3	*	MHz
Glitch Impulse	700	*	pV-s
DIGITAL DATA INPUTS			
Logic Compatability	TTL	*	
Logic Levels			
"1"	+3.5 (+2.4/+5.0)	*	V (min/max)
"0"	+0.2 (0.0/+0.6)	*	V (min/max)
Loading (Each Bit; with Typical			
Input Logic Levels)			
TTL "1"	40/4.8	*	nA/pF
TTL "0"	5/4.8	*	mA/pF
Coding			
Unipolar	Binary (BIN)	*	
Bipolar	Offset Binary (OBN)	*	
All "1's" Input	Maximum Positive Output	*	
All "0's" Input	Maximum Negative Output	*	
OUTPUT[4] (FS = Full Scale)			
Current Range[1] (±0.5% Accurate @ FS)	0 to +10.24 FS	*	mA
Voltage Range[5] (±1% Accurate @ FS)	0 to +1.024 FS	*	V
Zero Offset[1,2]	0.5 (2.5)	*	μA (max)
Zero Offset[1,3]	2.5 (10)	*	μA (max)
Voltage Noise, rms (0.1Hz to 15MHz)	15	*	μV
Compliance	+1.5; −2	*	V
Impedance[5,6]	100 (2)	*	Ω (±)
MULTIPLYING CHARACTERISTICS[7]			
V_{ANALOG} (1) Input Impedance	4 (±0.4)	*	kΩ (max)
V_{ANALOG} (2) Input Impedance	8 (±0.8)	*	kΩ (max)
V_{ANALOG} (1) Input Range (Pin 14):			
V_{ANALOG} (2) = 0V	0 to −5 FS	*	V
to	to		
V_{ANALOG} (2) = −5V	+2.5 to −2.5 FS	*	V
to	to		
V_{ANALOG} (2) = −10V	+5 to 0 FS	*	V
V_{ANALOG} (2) Input Range (Pin 16):			
V_{ANALOG} (1) = 0V	0 to −10 FS	*	V
to	to		
V_{ANALOG} (1) = −2.5V	+5 to −5 FS	*	V
to	to		
V_{ANALOG} (1) = −5V	+10 to 0 FS	*	V
Analog Feedthrough at I_{DAC}			
(V_{ANALOG} (1) = 0V to −5V, 1.4MHz;			
All Digital Inputs @ "0")	1	*	LSB
FS Analog Bandwidth (3dB)	10	*	MHz
Feedthrough at 10MHz (0V to −5V)	0.1	*	% FS
POWER REQUIREMENTS			
+15V ±5%	60 (72)	*	mA (max)
−15V ±5%	25 (35)	*	mA (max)
Power Dissipation	1.3 (1.6)	*	W (max)
Power Supply			
Rejection Ratio	0.01	*	%/V
TEMPERATURE RANGE			
Operating (Case)	−25 to +85	−55 to +100	°C
Storage	−55 to +150	*	°C

NOTES
[1]Current output into short circuit.
[2]Bit inputs at "0" and V_{ANALOG} (1) @ −5V.
[3]Bit inputs at "1" and V_{ANALOG} (1) @ −0V.
[4]FS accuracies are ±1% when using V_{ANALOG} (2) input.
[5]R_L (Pin 23) connected to I_{DAC} (Pin 24).
[6]Trimmed to value.
[7]Two-quadrant multiplying requires external op amp operating in bipolar mode.
Specifications subject to change without notice.

HDM-1210 PIN DESIGNATIONS

(As Viewed from Bottom)

PIN	FUNCTION	PIN	FUNCTION
24	I_{DAC} (OUTPUT)	1	BIT 1 (MSB)
23	R_L	2	BIT 2
22	10V SPAN	3	BIT 3
21	GROUND	4	BIT 4
20	GROUND	5	BIT 5
19	GROUND	6	BIT 6
18	GROUND	7	BIT 7
17	−15V	8	BIT 8
16	V_{ANALOG} (2)	9	BIT 9
15	AMPLIFIER GROUND	10	BIT 10
14	V_{ANALOG} (1)	11	BIT 11
13	+15V	12	BIT 12 (LSB)

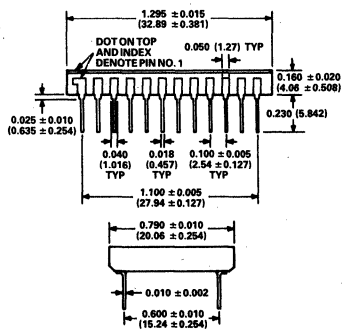
NOTE
PINS 15, 18, 19, 20 AND 21 NEED TO BE CONNECTED TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

Voltage @ V_{ANALOG} (1) (Pin 14)	Voltage @ V_{ANALOG} (2) (Pin 16)	D/A Output ± Pin 24 With All "1" Digital Input	With All "0" Digital Input
0V	Ground	0mA	0mA
−5V		+1.024mA	0mA
+2.5V	−5V	0mA	0mA
−2.5V		+1.024mA	0mA
Ground	0V	0mA	0mA
	−10V	+1.024mA	0mA
−2.5V	+5V	0mA	0mA
	−5V	+0.24mA	0mA

Table I. Output vs. Inputs

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ANALOG DEVICES

Hybrid Inductosyn Preamplifier

IPA1764

FEATURES

Hybrid Construction
Phase Shift <5°
Phase Match <1°
Load Capacity 10,000pF
Full Military Temperature Range

APPLICATIONS

The IPA1764 is recommended for use with the 1S10/20, 1S14/24 and other 10- and 12-bit Inductosyn*/Resolver-to-Digital Converters.

GENERAL DESCRIPTION

The output signals from an Inductosyn slider are at a low level of the order millivolts and require amplification and buffering before transmission to an Inductosyn-to-digital converter. The IPA1764 provides the necessary gain and output impedance for this purpose.

Any gain mismatch in the two channels amplifying the sine and cosine outputs of the Inductosyn slider contributes to the system error. The IPA1764 with a 0.15% gain match over the temperature range only contributes an error of 0.23 micron using a 2mm pitch Inductosyn. By carefully controlling phase mismatch to less than 1°, the error contribution is only 0.2 micron in a 2mm pitch Inductosyn.

The IPA1764 with an output resistance of less than 3 ohms and a capability of driving a cable capacity of 10,000pF is totally suited to machine tool applications where the Inductosyn-to-digital converter is remote from the measuring Inductosyn.

The IPA1764 is of hybrid manufacturing techniques, and available in two temperature range versions–industrial temperature range (0 to +70°C) and extended temperature range (−55°C to +125°C).

APPLICATION

The diagram on the following page shows a "hookup" with the preamplifier, power oscillator and a 1S20 with an Inductosyn. Precise application information is not possible as the Inductosyn in its application has many variables.

Current Set Resistor

This resistor is used to match the voltage output of the oscillator to the Inductosyn track resistance and provide the manufacturer's recommended current. By variation of the voltage outputs and current resistance, track by this up to approximately 10 feet (3 meters) can be accommodated.

Decoupling

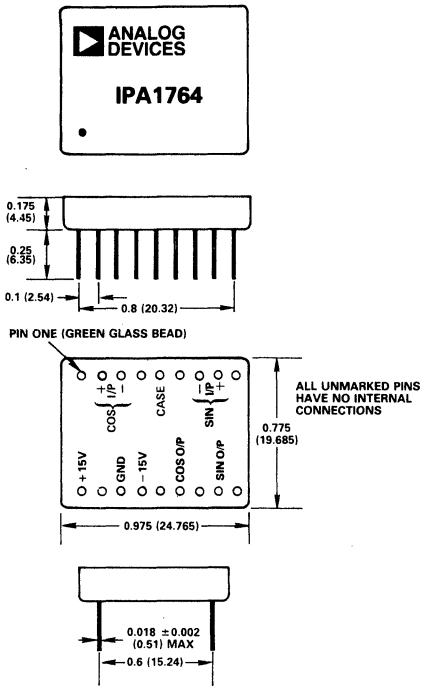
The preamplifier and oscillator have internal high frequency decoupling capacitors on the supply lines, however, it is recommended that electrolytic decoupling capacitors are connected close to the hybrid pins.

*Inductosyn is a registered trademark of Farrand Industries, Inc.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ORDERING INFORMATION

IPA1764 X 60 B

- B — High Reliability Processing
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range

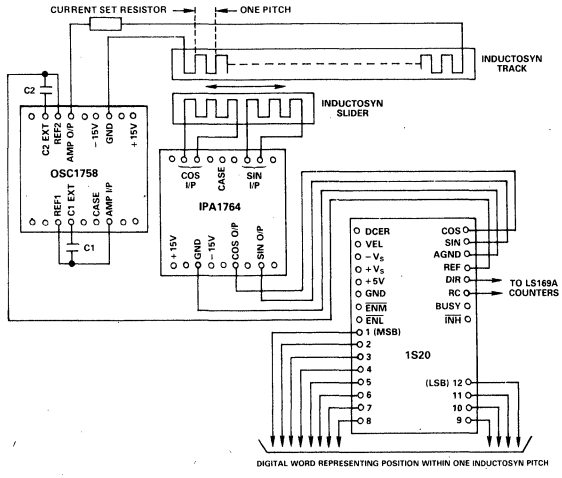
SPECIFICATIONS (typical @ +25°C over full range of power supply inputs unless otherwise noted)

Model	IPA1764/560	IPA1764/460
GAIN	1250 ± 5%	*
GAIN MISMATCH Channel to Channel Over Full Temperature Range	± 0.15% (equivalent to 2.5 arc mins)	± 0.3%
PHASE SHIFT	<5°	*
PHASE MISMATCH Channel to Channel	<1°	*
CROSSTALK	<0.1%	*
OPERATING FREQUENCY	10kHz	*
INPUT RESISTANCE	5kΩ ± 10%	*
OUTPUT RESISTANCE	<5Ω	*
MAX LOAD CAPACITY	10,000pF	*
MAX SIGNAL OUTPUT LEVEL	3V rms	*
POWER SUPPLIES Voltage Current	± 12V to ± 15V 50mA max	* *
TEMPERATURE RANGE Operating	0 to + 70°C	− 55°C to + 125°C
SIZE	0.775" × 0.975" × 0.175" (19.7mm × 24.8mm × 4.5mm)	*
WEIGHT	0.25 ozs (7 grams)	*

NOTES
*Specification same as IPA1764/560.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM VALUES WITH RESPECT TO SUPPLY GROUND

Sin and Cos I/P . . . . . +V
+V Pin . . . . . +17V
−V Pin . . . . . −17V
Sin and Cos O/P 1k Load . . . . . +10V
Indefinite Short Circuit Proof



Use of 1S20 with Inductosyn Preamplifier IPA1764, Hybrid Power Oscillator OSC1758

ANALOG DEVICES

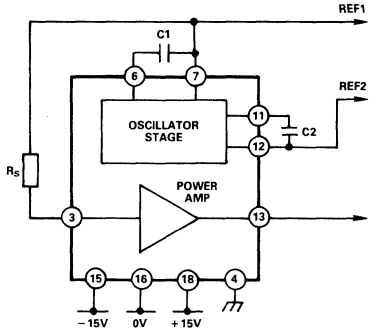
Hybrid Power Oscillator

OSC1758

FEATURES
Full Military Temperature Range
Hybrid Construction
18-Pin DIL Package
0-10kHz Frequency Range
In-Phase and Quadrature Outputs

APPLICATIONS
Synchro Resolver, and Inductosyn® Excitation
LVDT Drive

OSC1758 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The OSC1758 is a hybrid sine/cosine power oscillator which can provide a maximum power output of 1.5 watts, over 0 to 10kHz.

The device comprises two independent parts–an oscillator and a power amplifier.

The oscillator stage has two signal outputs, one 90° in phase advance with respect to the other.

The oscillator frequency is programmable in the range of 0 to 10kHz by two identical external capacitors.

The power amplifier stage is externally short circuit protected and has a gain of 2.8 ±1%. The maximum output current this stage can produce is 215mA rms (at 7V rms).

Connecting either of the oscillator stage outputs to the power amplifier input, using an external link, will give a nominal output of 7 volts rms. Lower voltages can be obtained by connecting an external resistor in series with the amplifier's inputs.

The OSC1758 is housed in an hermetically-sealed 18-pin DIL metal case, and operates over full military temperature range (−55°C to +125°C), as well as the industrial (0 to +70°C) temperature range.

MODELS AVAILABLE

The OSC1758 is available in both industrial and military temperature ranges. For details of how to specify the required part, see "Ordering Information".

CONNECTING THE OSC1758

The block diagram shows the output configuration, when using the power amplifier stage. If only the oscillator stage is required, the connection between pin 3 and pin 7 is not included.

The frequency of oscillation for the OSC1758 in the block diagram is determined by the two identical capacitors C1 and C2. For the frequency required, the value of C1 and C2 should be calculated using the following equation.

$$C_1 = C_2 = \frac{1}{F_{OSC} \times 10^5} \text{ Farads}$$

Where F_{OSC} = Frequency of oscillation in Hz.

For a reduced output a series resistor, R_S, must be added.

For the required output voltage R_S should be calculated as follows:

$$R_S = \frac{37.5 \times 10^3}{V_{OUT}\,(\text{rms})} - 5350 \text{ Ohms}$$

STABILITY

To ensure stability of both frequency and voltage level outputs it is essential that good quality external capacitors are used, e.g., Silver Mica or Polystyrene.

The tolerance quoted in the specification applies if high grade Silver Mica capacitors, with a temperature coefficient of less than 50ppm/° C, and a low loss factor, are used.

POWER DISSIPATION

The thermal dissipation characteristics for the OSC1758 are as follows:

θ junction – case = 15° C/W
θ junction – ambient = 40° C/W
θ j (max) = 150° C.

Total Power Dissipation =

$(V_{SUPPLY} \times I_{SUPPLY}) - (V_{OUT} \times I_{OUT} \times \text{cosine } \phi)$

where ϕ = load phase angle

NOTE: Although the power amplifier stage has internal short circuit protection, a heat sink should be employed for protection against continuous short circuit conditions.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

Inductosyn® is a registered trademark of Farrand Industries, Inc.

SPECIFICATIONS (typical @ +25°C with ±15V power supplies unless otherwise noted)

Model	OSC1758/500	OSC1758/400
FREQUENCY RANGE	0-10kHz	*
FREQUENCY STABILITY[1,2]	±5%	*
REFERENCE 1 OUTPUT[1]	2.5V rms ±5% @ 3mA rms	*
REFERENCE 2 OUTPUT[1]	2.5V rms ±5% @ 3mA rms 90° Phase Advanced with Respect to Ref. 1 Output	*
AMPLIFIER OUTPUT[3]	7V rms @ 215mA max	*
CAPACITIVE LOAD	10nF (max)	*
AMPLIFIER GAIN[1]	2.8 ±1%	*
AMPLIFIER INPUT RESISTANCE	5.35kΩ ±1%	*
POWER DISSIPATION	4.0 Watts (max)	*
POWER SUPPLY[4]	±15V 60mA (max) No Load 160mA (max) Full Load	* *
TEMPERATURE RANGE Operating Storage	 0 to +70°C −65°C to +150°C	 −55°C to +125°C *
SIZE	0.975" × 0.775" × 0.175" (24.8mm × 19.7mm × 4.5mm)	*
WEIGHT	0.25 ozs. 7 grams	*

NOTES
[1]Over full operating temperature range.
[2]See section on "Stability".
[3]Derated to 5V rms @ 215mA if using ±12 volt power supply.
[4]Will operate with ±12 volt power supply with derated output voltage.
*Specifications same as OSC1758/500
Specifications subject to change without notice.

ABSOLUTE MAXIMUM VALUES WITH RESPECT TO SUPPLY GROUND

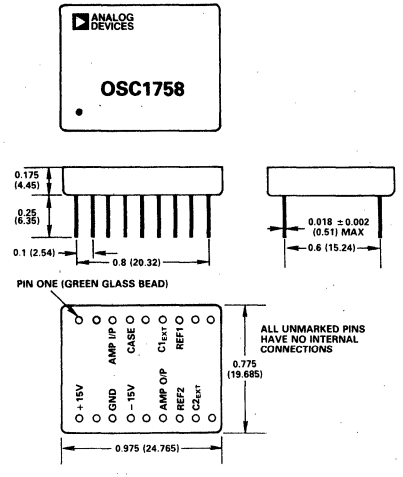
$+V_S$ . . . . . −0.3V to +18V
$-V_S$ . . . . . +0.3V to −18V

ORDERING INFORMATION

OSC1758 X 00 B
- B — High Reliability Processing
- X = 5 — 0 to +70°C Operating Temperature Range
- X = 4 — −55°C to +125°C Operating Temperature Range

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)



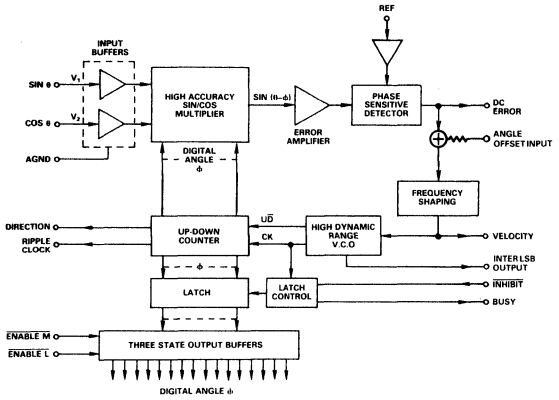
Tachogenerator Output, Hybrid, Resolver-to-Digital Converter

1S14, 1S24, 1S44 and 1S64

FEATURES
40-Pin Hybrid
Tachogenerator Velocity Output
DC Error Output
Sub LSB Output
Angle Offset Input
Reference Frequency of 2kHz to 10kHz
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Feed Forward Velocity Stabilizing Loops
Robotics
Closed Loop Motor Drives
Brushless Tachometry
Single Board Controllers

1S14, 1S24, 1S44 and 1S64 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1SN4* are hybrid devices that convert standard resolver inputs to digital position and analog velocity outputs. All the essential features for multiturn or multipitch operation are included for numerically controlled machine tool and velocity feedback applications.

Typically the input signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1SN4 ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway.

A unique feature of the converter is its internally generated tachogenerator velocity output offering a linear voltage-speed relationship. Only one external resistor is required to scale the velocity output to the users chosen volts/rpm relationship.

Repeatability is 1LSB under constant temperature conditions.

Four resolutions are available all operating over a frequency range of 2kHz to 10kHz.

1S14 is 10-bit up to 40,800 revolutions per minute.
1S24 is 12-bit up to 10,200 revolutions per minute.
1S44 is 14-bit up to 2,550 revolutions per minute.
1S64 is 16-bit up to 630 revolutions per minute.

*N is 1, 2, 4 or 6 depending upon resolution of model.

APPLICATIONS

The 1SN4 has been specifically designed for motor position control for the numerically controlled machine and robot industry, using the type 2 servo loop tracking principle that ideally suits these converters to the electrically noisy environment found in these industrial applications.

USER BENEFITS

Allows both velocity and position measurement from a single, low cost, standard, brushless resolver.

80dB dynamic range of velocity output.

0.5% ripple on velocity signal.

0.1% linearity of velocity signal.

Cost effective tachogenerator replacement.

Tracks at 5 to 10 times the rate of equivalent resolution encoders.

Analog output for interpolation between digital codes.

Direction and Ripple Clock (Datum) outputs facilitate revolution counting.

Hybrid construction offering small size and MTBF of >200 years at 50°C GB.

SPECIFICATIONS (typical for both commercial (5Y0) and extended (4Y0) temperature range options @ 25°C and ±15V or ±12V power supplies, unless otherwise noted)

Models / Parameters		1S14	1S24	1S44	1S64	Units
RESOLVER INPUTS						
Signal Voltage		2.0 ± 5%	*	*	*	V rms
Reference Voltage		2.0 + 50%/ − 20%	*	*	*	V rms
Signal & Reference Frequency		2k–10k	*	*	*	Hz
Signal Input Impedance		10(min)	*	*	*	MΩ
Reference Input Impedance		125	*	*	*	kΩ
Allowable Phase Shift (Signal to Reference)		±10	*	*	*	Degrees
POSITION OUTPUT						
Resolution		10	12	14	16	Bits
1LSB		0.35	0.088	0.022	0.0055	Degrees
Accuracy (max error over temp. range)	5Y0	±25.0(0.42)	±8.5(0.14)	±5.3(0.09)	±4.0(0.07)	Arc-mins (degrees)
		±0.12	±0.04	±0.025	±0.019	% F.S.
	4Y0	±25.0(0.42)	±8.5(0.14)	±5.3(0.09)	±2.6(0.04)	Arc-mins (degrees)
		±0.012	±0.04	±0.025	±0.012	% F.S.
Digital Position Output Format		Parallel natural binary	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Monotonicity		Guaranteed	*	*	*	
Repeatability		1	*	*	*	LSB
DATA TRANSFER						
Busy Output		Logic "Hi" when Busy	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Busy Width		380 (min) 530 (max)	*	*	*	ns
$\overline{\text{ENABLE}}$ Inputs		Logic "Lo" to Enable	*	*	*	
Load		1	*	*	*	LSTTL
Enable & Disable Times		250 (max)	*	*	*	ns
$\overline{\text{INHIBIT}}$ Input		Logic "Lo" to Inhibit	*	*	*	
Load		1	*	*	*	LSTTL
Direction Output (DIR)		Logic "Hi" when counting up, Logic "Lo" when counting down.	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Ripple Clock (RC)		Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.	*	*	*	
Load		6 (max)	*	*	*	LSTTL
Width		1μ(max) 850n(min)	*	*	*	Secs
DYNAMIC CHARACTERISTICS						
Tracking Rate (min)						
with ±15V supplies		40,800	10,200	2,550	630	rpm
with ±12V supplies		34,680	8,670	2,168	536	rpm
Acceleration Constant Ka		220,000	*	*	*	Sec^{-2}
Settling time (179° step input)		25 (max)	35 (max)	60 (max)	120 (max)	ms
Bandwidth		230	*	*	*	Hz
VELOCITY OUTPUT						
Polarity		Positive for increasing angle	*	*	*	
Tachogenerator Voltage Scaling		0.25	1	4	16	V/K rpm
Scale Factor Accuracy		±1 (max)	*	*	*	% of output
Scale Factor Tempco		200 (max)	*	*	*	ppm/°C
Reversion Error		±0.2 (max)	*	*	*	%
Reversion Error Tempco		50 (max)	*	*	*	ppm/°C
Linearity		0.1	*	*	*	% of output
Over full temp range		0.25 (max)	*	*	*	% of output
Ripple and Noise						
Steady State @10kHz (200Hz b/w)		100	150	300	1300	μV rms
Dynamic Ripple (av-pk)		0.5 (max)	*	*	*	% of output
Zero Offset		±500	*	*	*	μV
Zero Offset Tempco		50 (max)	*	*	*	μV/°C
Output Load		5 (min)	*	*	*	kΩ

Models Parameters	1S14	1S24	1S44	1S64	Units
SPECIAL FUNCTIONS					
DC Error Output Voltage	450	*	*	*	mV/degree
Inter LSB Output	±1 (±20%)	*	*	*	V/LSB
Load	1 (min)	*	*	*	kΩ
Angle Offset Input (over operating temperature range)	320 (±10%)	*	*	*	nA/LSB
Maximum Input	32	*	*	*	LSB
POWER REQUIREMENTS					
Power Supplies					
$\pm V_S$	±15 (±5%) or ±12 (±5%)	*	*	*	V dc
+5V	+4.75 to +5.25	*	*	*	V dc
Power Supply Consumption					
$\pm V_S$	30 (max)	*	*	*	mA
+5V	125 (max)	*	*	*	mA
Power Dissipation	1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating 5Y0 option	0 to +70	*	*	*	°C
4Y0 option	−55 to +125	*	*	*	°C
Storage 5Y0 option	−55 to +125	*	*	*	°C
4Y0 option	−60 to +150	*	*	*	°C
DIMENSIONS					
5Y0 option	2.1″ × 1.1″ × 0.195 (5.3 × 28 × 4.95)	*	*	*	Inches (mm)
4Y0 option	2.14″ × 1.14″ × 0.18 (54.4 × 29 × 4.6)	*	*	*	Inches (mm)
WEIGHT	1 (28)	*	*	*	oz. (grms)

NOTES
*Specifications same as 1S14.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1] . . . . . 0V to +17V dc
$-V_S$[1] . . . . . 0V to −17V dc
+5V[2] . . . . . 0V to +6.0V dc
Reference . . . . . ±17V dc
Sine . . . . . ±17V dc
Cosine . . . . . ±17V dc
Any Logical Input . . . . . −0.4V to +5.5V dc

CAUTION:
1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

OPERATION OF THE CONVERTER

The 1SN4 are tracking converters, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the resolution option. No convert command is necessary as the conversion is initiated by each LSB increment for the input. Each LSB increment of the converter initiates a BUSY pulse.

POSITION OUTPUT

The resolver shaft position is represented at the converter output by a natural binary parallel digital word.

The static angular accuracy quoted for each converter type is the worst case error that can occur over the full operating temperature range with the following input conditions:

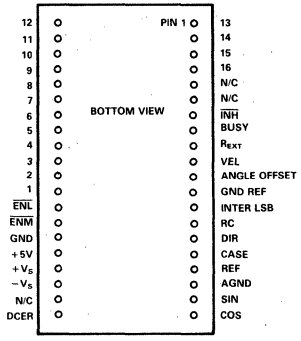
a) Signal input amplitudes within 5% of the nominal values.
b) Signal and reference frequency within the specified operating range.
c) Phase shift between signal and reference less than 10 degrees.
d) Signal and reference waveform harmonic distortion less than 10 percent.

These test conditions are selected primarily to establish a repeatable acceptance test procedure which can be traced to national standards. In practice the converters can be used well outside these operating conditions providing the following points are observed:

Signal Amplitude (Sine and Cosine Inputs)
The amplitude of the signal inputs should be maintained within 5% of the nominal values if full performance is required from the analog outputs and inputs of the converter such as velocity, inter LSB position and angle offset.

The digital position output is relatively insensitive to amplitude variation. Increasing the input signal levels by more than 10% will result in a dramatic loss in accuracy due to internal overload. Reducing level will result in a steady decline in accuracy. With the signal levels at 50% of the correct value, the angular error will increase to an amount equivalent to 1.3LSB. At this level the repeatability will also degrade to 2LSB and the dynamic response will also change, since the factor Ka is proportional to signal level.

PIN CONNECTIONS



NOTES
1. "R_{EXT}" SHOULD BE CONNECTED TO "VEL" WHEN NO SCALING REQUIRED.
2. CASE PIN CONNECTED ON 460 OPTION ONLY.

Signal and Reference Frequency
Any frequency within the specified range of the converter may be used. It should be noted that the same frequency must be used on both inputs.

Reference Voltage Level
The amplitude of the reference signal applied to the converter's input is very uncritical, however it is essential that the zero crossing points are maintained in the correct place to drive the converter's phase sensitive detector.

Harmonic Distortion
The amount of harmonic distortion allowable on the signal and reference lines mainly depends on the type of transducer being used.

Square and triangle waveforms can be used but the input levels should be adjusted so that the average value after rectification is 1.9 volts. (For example – a square wave should be 1.9V peak).

Note: The figure specified of 10% harmonic distortion is for calibration convenience only.

Phase Shift (Between Signal and Reference)
See Section on "Dynamic Accuracy vs. Resolver Phase Shift".

DATA TRANSFER

BUSY Output:
The validity of the output data is indicated by the state of the BUSY output. When the input to the converter is changing, the signal appearing on the BUSY output is a series of pulses of TTL levels. A BUSY pulse is initiated each time the input moves by the analog equivalent of an LSB and the internal counter is incremented or decremented.

$\overline{\text{INHIBIT}}$ Input:
The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore, does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

Note: With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

$\overline{\text{ENABLE}}$ Inputs:
Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the most significant 8-bits and $\overline{\text{ENABLE L}}$ for the least significant remainder. These $\overline{\text{ENABLES}}$ determine the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins. The operation of these $\overline{\text{ENABLES}}$ has no effect on the conversion process.

Two methods are available for transferring data, by using the inputs and outputs described.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

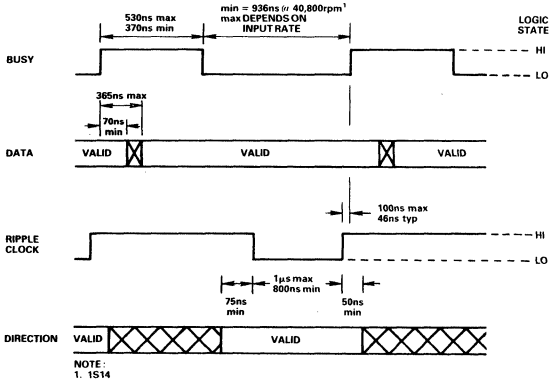


Figure 1. Timing Diagram

RIPPLE CLOCK (RC) and DIRECTION (DIR) Outputs:
As the digital output of the converter passes through the major carry, i.e. all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The DIRECTION (DIR) logic output indicates the direction of input rotation and this data is always valid in advance of the

RIPPLE CLOCK pulse, and stays valid until the direction changes (see Timing Diagram – Figure 1).

These two logic outputs are provided so that the user can count the input revolutions or pitches. An external extension counter is required. Figure 7 shows the application circuit which should be used to perform this counting function.

Note: CMOS external counters can be used (see Figure 2) but it is not advisable as great care must be taken to keep stray capacitances low because of the high tracking rate of the converter.

VELOCITY OUTPUT
The tracking conversion technique produces an internal signal at the input to the voltage controlled oscillator (VCO) that is proportional to the rate of the input angle. In the 1SN4 series additional circuitry is included to linearize this signal, which is closely characterized, producing a high quality tachogenerator

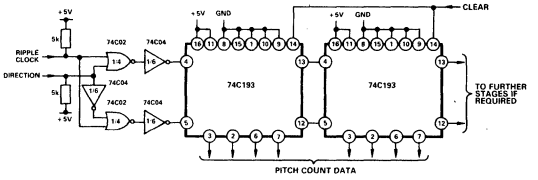


Figure 2. CMOS External Counter

velocity output at the VELOCITY (VEL) pin.

This analog tachogenerator velocity output is resistively scaled internally to give a full scale output of ±10V dc at the specified tracking rate for the converter.

However, a full scale output of ±10V dc can be obtained for lower speeds by changing the gain of the internal scaling amplifier using only one external resistor. The external resistor, R_{EXT}, should be connected between "R_{EXT}" pin and the GND REF pin, and calculated using the following equation.

$$R_{EXT} = \frac{10 \times A}{B - A}\ k\Omega$$

Where A = required rps to be represented by ±10V FS
and B = specified rps for the converter.

Note: A cannot be greater than B and for unity gain "VEL" and "R_{EXT}" pins should be linked (no external resistor required).

When the external resistor facility is used to provide large magnifications there is an additional velocity output offset generated due to the inevitable common ground impedance inherent with a single ground connection point. While these offsets will still be in spec, they can be code dependent. They can be minimized by taking the external scaling resistor from "R_{EXT}" to GND REF instead of "GND". This means that the velocity output will be unaffected by the varying current drawn from the +5V supply as the digital output changes.

Ripple and noise on the velocity signal consists of two components – steady state noise and dynamic noise.

Steady state noise – this is internally generated noise produced by the converter's circuitry and is the only noise signal present under static input conditions.

Dynamic noise – this is the noise produced, in addition to steady state noise, under dynamic operating conditions.

The two main components of the dynamic noise signal are due to the "non-zero" angular error of the resolver/converter combination. The figures given in the specification are typical for a size 11, 7 arc-minutes, brushless resolver.

It should be noted that when operating at low tracking rates it is critical to maintain the signal input voltage at its nominal value in order to keep the noise level on the velocity signal to an absolute minimum. The effect of variation in signal voltage at low tracking rates is to produce low energy spikes on the velocity output on the rising edge of the BUSY pulse. The amplitude of these spikes will be in the region of 30µV per percent variation in signal input voltage level.

Note: The velocity signal output and max tracking rate derates by 15% (max) for operation with ±12 volt power supplies.

SPECIAL FUNCTIONS

DC Error: The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converters are a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason. It is therefore an indication that the input has exceeded the maximum tracking rate of the converter, or, due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

INTER LSB Output: In order to overcome the "free play" inherent in a servo system using digitized position feedback, an analog output voltage is available representing the resolver shaft position within the least significant bit of the digital angle output.

The output is therefore proportional to the inter LSB resolved position with a maximum output representing 1LSB.

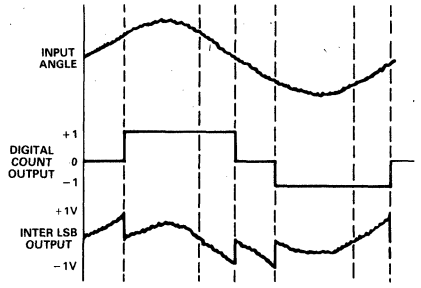


Figure 3

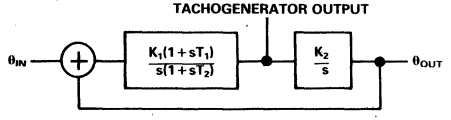
Figure 3 illustrates how the INTER LSB output compensates for the instances where, due to hysteresis, there is no change in the digital count output for 1LSB change in input angle. The sum of the digital count output and INTER LSB output equals the actual input angle.

ANGLE OFFSET Input: A unique feature of the 1SN4 series of converter is their angle offset input which allows the user to electrically "rotate" the input shaft of the resolver.

Injecting a current of 320nA into the angle offset input pin will offset the digital output of the converter by 1LSB relative to the angle defined by the resolver inputs. It is recommended that an offset equivalent to no greater than 30LSB's be applied to this input.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Positional Transfer Function:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_1K_2}{s^2} \cdot \frac{1 + sT_1}{1 + sT_2} \text{ Open Loop}$$

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + sT_1}{1 + sT_1 + \frac{s^2}{K_1K_2} + \frac{s^3T_2}{K_1K_2}} \text{ Closed Loop}$$

where $K_1K_2 = K_a$

Tachogenerator Transfer Function:

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{K_1(1 + sT_1)}{s(1 + sT_2)} \text{ Open Loop}$$

$$\frac{\text{Tachogenerator Output}}{\theta_{IN}} = \frac{s(1 + sT_1)}{K_2(1 + sT_1) + \frac{s^2}{K_1} + \frac{s^3T_2}{K_1}}$$

Closed Loop

Where: $K_1 = 3.23$
$K_2 = 68.2 \times 10^3$
$K_a = 220 \times 10^3$
$T_1 = 4.46\text{ms}$
$T_2 = 0.21\text{ms}$

Refer: Figures 4 and 5

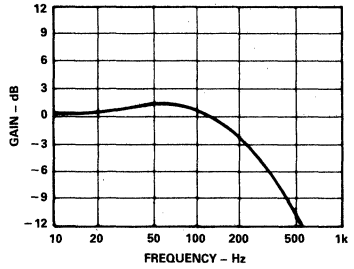


Figure 4. Gain Plot

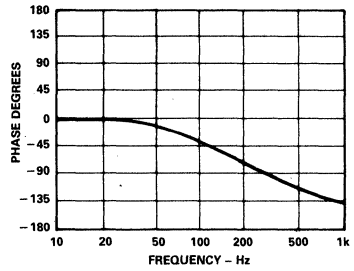


Figure 5. Phase Plot

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Under static operating conditions phase shift between signal and reference lines theoretically does not effect the converter's static accuracy.

However, when rotating, most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

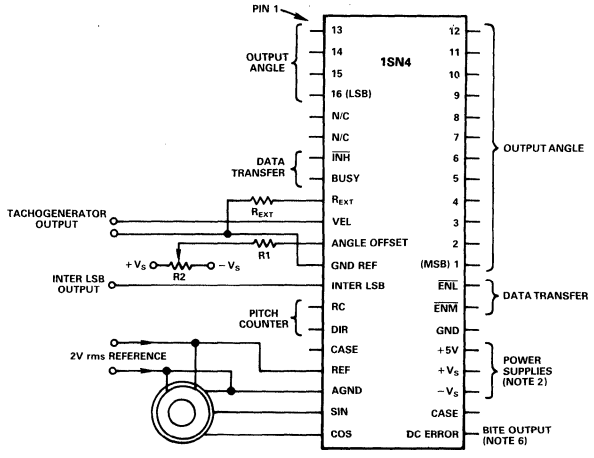
$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

Note: Capacitive and inductive crosstalk in the signal and reference leads and wiring can cause similar problems.



NOTES
1. GND, GND REF AND AGND ARE INTERNALLY CONNECTED.
2. EACH SUPPLY SHOULD BE DECOUPLED WITH 100nF CERAMIC CAPACITOR IN PARALLEL WITH A 6μF TANTALLUM CAPACITOR.
3. REXT IS EXTERNAL TACHOGENERATOR SENSITIVITY SCALING RESISTOR (IF REQUIRED) – SEE TEXT UNDER HEADING "VELOCITY OUTPUT".
4. R1 AND R2 ARE ANGLE OFFSET INPUT SCALING RESISTORS (IF REQUIRED) – SEE TEXT.
5. CASE PIN CONNECTED ON 460 OPTION ONLY.
6. POSSIBLE USE AS BUILT-IN TEST EQUIPMENT. (SEE HEADING "SPECIAL FUNCTIONS".)

Figure 6. Electrical Connections

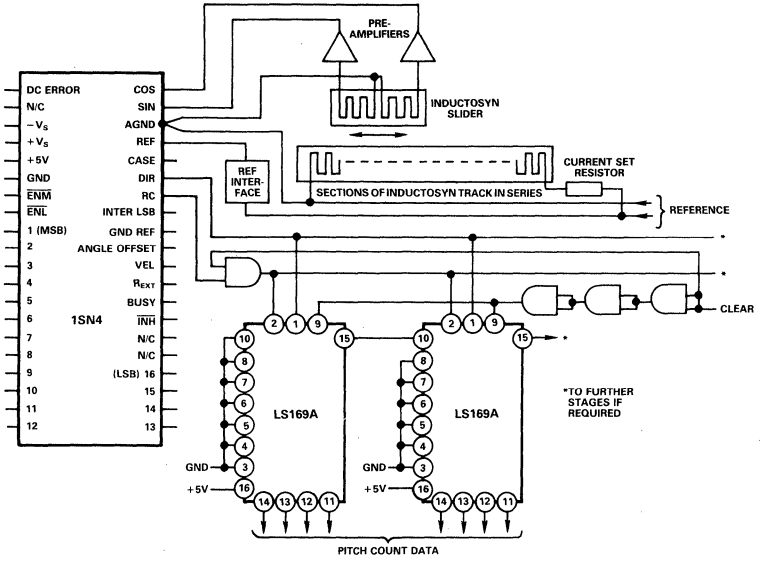


Figure 7. Connections for Use with Inductosyn/"LS" External Counters

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be $\pm 12V$ to $\pm 15V$ but must not be reversed. The $+5V$ supply connects to the $+5V$ pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors are connected in parallel between the power lines ($+V_S$, $-V_S$ and $+5V$) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 6).

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

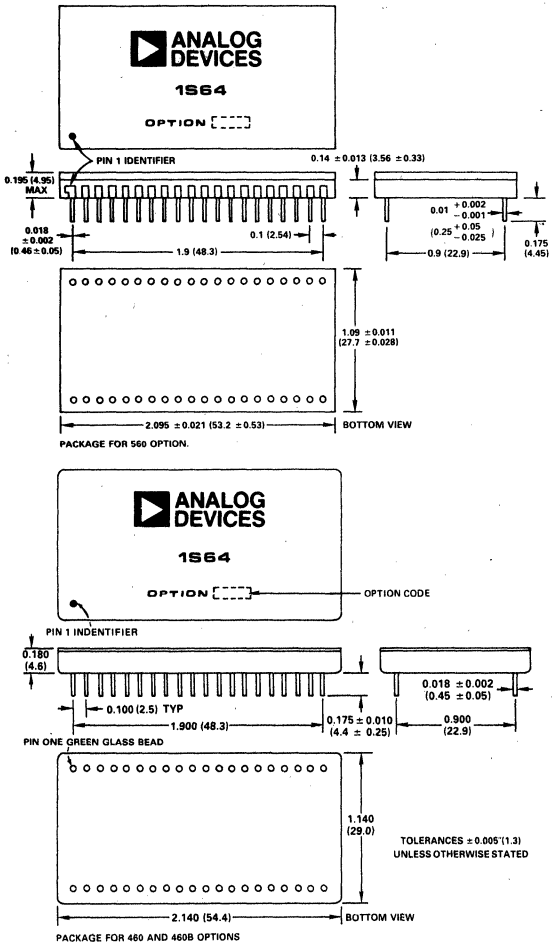
HIGH REL PROCESSING

All models ordered to high reliability requirements will be identified with a B suffix, and will have received the following processing:

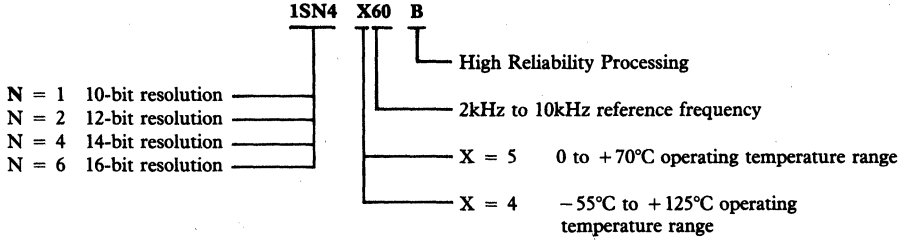
1. Internal visual inspection
2. Stabilization bake, 24 hours at 150°C
3. Temperature cycling, −65°C to +150°C
4. Constant acceleration, 5000g
5. Powered burn-in, 160 hours at 125°C
6. Final electrical test at T_{MIN} and T_{MAX}
7. Seal test, fine and gross
8. External visual inspection

OUTLINE DIMENSIONS
PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm).



ORDERING INFORMATION



Tachogenerator Output, Variable Resolution, Hybrid, Resolver-to-Digital Converter

1S74

FEATURES
40-Pin Hybrid
Tachogenerator Velocity Output
User Selectable Resolution
DC Error Output
Sub LSB Output
Angle Offset Input
Reference Frequency of 2kHz to 10kHz
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Feed Forward Velocity Stabilizing Loops
Robotics
Closed Loop Motor Drives
Brushless Tachometry
Single Board Controllers

GENERAL DESCRIPTION

The 1S74 is a hybrid device that converts standard resolver inputs to digital position and analog velocity outputs. All the essential features of multiturn or multipitch operation are included for numerically controlled machine tool and velocity feedback applications.

Typically, the input signal would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S74 ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway.

A unique feature of the converter is its internally generated tachogenerator velocity output offering a linear voltage-speed relationship. Only one external resistor is required to scale the velocity output to the user's chosen volts/rpm relationship.

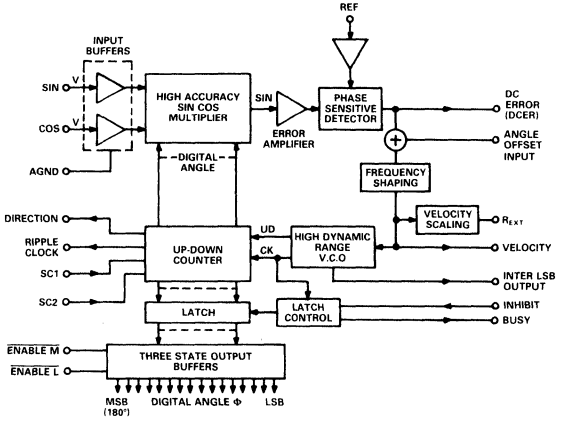
Repeatability is 1LSB under constant temperature conditions.

The resolution of the 1S74 converter is user selectable by means of applying a specific binary code to two of the converter's pins.

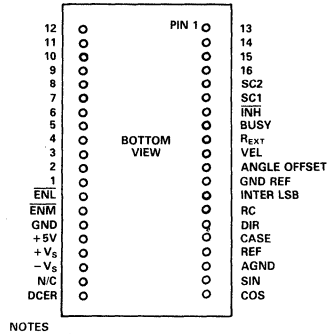
Four resolutions can be selected, all operating over a frequency range of 2kHz to 10kHz.

10 bit up to 40,800 revolutions per minute.
12 bit up to 10,200 revolutions per minute.
14 bit up to 2,550 revolutions per minute.
16 bit up to 630 revolutions per minute.

1S74 FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



NOTES
1. "R_{EXT}" SHOULD BE CONNECTED TO "VEL" FOR UNITY GAIN.
2. CASE PIN CONNECTED ON 460 OPTION ONLY

ORDERING INFORMATION

1S74 X60 B

- B — High Reliability Processing
- 60 — 2kHz to 10kHz reference frequency
- X = 5 0 to +70°C operating temperature range
- X = 4 −55°C to +125°C operating temperature range.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical for both commercial (5Y0) and extended (4Y0) temperature range options @ 25°C and ±15V or ±12V power supplies, unless otherwise noted)

Resolution	10 Bits	12 Bits	14 Bits	16 Bits
ALL SPECIFICATIONS				
560 Option	Same as 1S14 560 Option	Same as 1S24 560 Option	Same as 1S44 560 Option	Same as 1S64 560 Option
460 Option	Same as 1S14 460 Option	Same as 1S24 460 Option	Same as 1S44 460 Option	Same as 1S64 460 Option

For full specification details please refer to the 1S14/24/44/64 data sheet on pages 3-400 and 3-401.

RESOLUTION PROGRAMMING

The 1S74 converter can be programmed for resolutions of 10, 12, 14, and 16 bit by applying a binary code to the pins "SC1" and "SC2".

The dc error output and maximum revolutions per minute for full scale are scaled internally according to the particular resolution selected.

Table I gives the binary code, dc error output and maximum tracking rate for the resolutions available.

Resolution	Binary Code SC1	SC2	DC Error (mV/Bit)	Tracking Rate for FS (±10V) rpm
10 Bit	0	0	160	40,800
12 Bit	0	1	40	10,200
14 Bit	1	0	10	2,550
16 Bit	1	1	2.5	630

Table I.

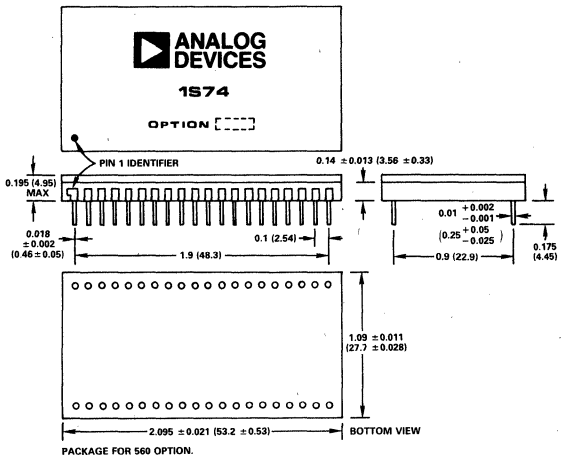
NOTE: When changing resolution under dynamic conditions, a period of uncertainty will exist before position and velocity data is valid.

For more information ask for the relevant application note.

OUTLINE DIMENSIONS

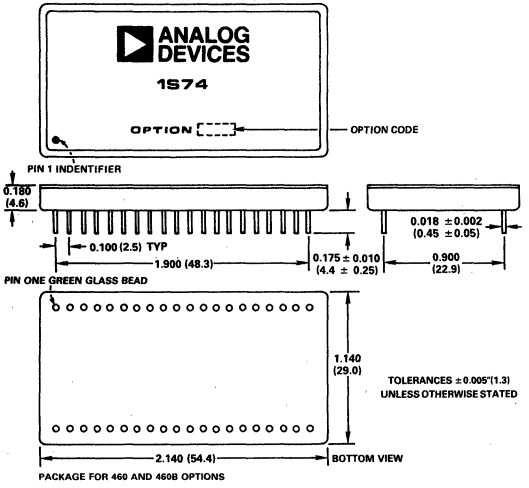
Dimensions Shown in inches and (mm).

PACKAGE FOR 560 OPTION



PACKAGE FOR 560 OPTION.

PACKAGE FOR 460 AND 460B OPTIONS



PACKAGE FOR 460 AND 460B OPTIONS

ANALOG DEVICES

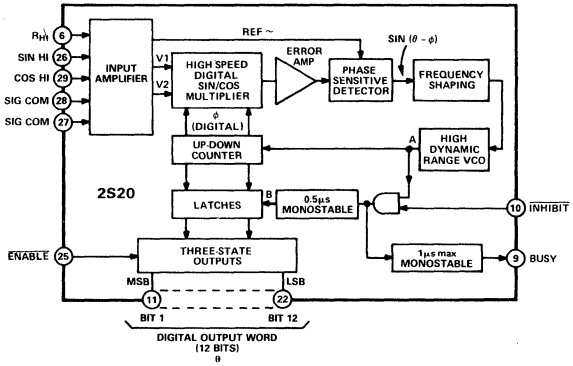
Low Cost, Hybrid, 12-Bit, Resolver-to-Digital Converters

2S20

FEATURES
Converts Brushless Resolver Outputs to Digital Angles
Low-Cost Digital Shaft Angle Measurement
High Tracking Rate (6000 rpm)
Uses Applications Specific LSI Integrated Circuit
Hybrid Construction
Three-State Digital Output
Operates Over 1kHz to 10kHz Frequency Range

APPLICATIONS
Robotics
Machine Tool Control
Factory Automation
Industrial Control

2S20 FUNCTIONAL BLOCK DIAGRAM



3

GENERAL DESCRIPTION

The 2S20 converts the output of a brushless resolver into a 12-bit parallel digital word representing the resolver's shaft angle. The combination of resolver and 2S20 can be regarded as a high reliability, low-cost absolute shaft encoder.

The converter is of the continuous tracking type and can follow the resolver's shaft at speeds of up to 100 revs per sec (6000 rpm) without additional error.

The converter operates over the reference frequency range of 1kHz to 10kHz and the unit accepts signal inputs of 2.5 volts rms and reference inputs of 2.5 to 10 volts rms.

The low cost has been achieved by the use of an Applications Specific Integrated Circuit which performs 90% of the total converter function and ensures extremely high reliability.

The 2S20 is housed in a 32-pin, triple DIP ceramic package and operates over the temperature range 0 to +70°C.

USER BENEFITS

Unlike some other resolver-to-digital conversion techniques, the 2S20 uses only the ratio of the sine and cosine stator signals for the conversion and consequently is extremely insensitive to reference voltage, frequency and waveform variations.

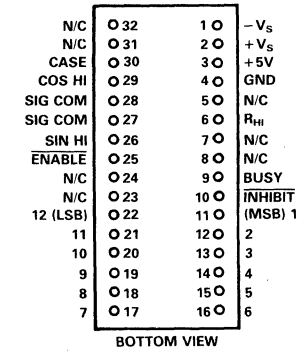
The ratiometric amplitude measurement technique and the internal phase sensitive detector provide very high input noise rejection by attenuating signals which are not phase and frequency coherent with the reference signal.

Data is transmitted from the resolver to the 2S20 in analog format thus allowing noise immune data transmission over long distances. Furthermore only 6 wires are required to transmit the angular data.

MODELS AVAILABLE

Only one model of the 2S20 is available operating over the frequency range 1kHz to 10kHz and 0 to +70°C.

PIN CONFIGURATION



BOTTOM VIEW

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
+5V[2]	0V to +5.5V
R_{HI} to GND	±20V dc
Sin Hi/Cos Hi	±20V dc
Case to	±20V dc
Any Logical Input	−0.4V to +5.5V dc

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

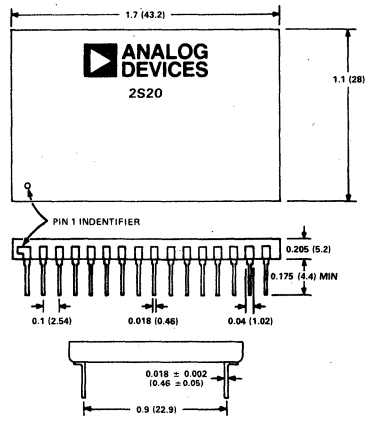
SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Model	2S20
RESOLUTION	12 Bits (Natural Binary)
ACCURACY[1]	± 11 arc mins
ACCURACY TEMPERATURE COEFFICIENT	0.12 arc mins/°C
DIGITAL OUTPUT	Parallel 1LS TTL Load MSB = 180°
SIGNAL & REFERENCE FREQUENCY	2kHz to 10kHz
SIGNAL VOLTAGE	2.5V rms
SIGNAL INPUT IMPEDANCE	50kΩ ± 2%
REFERENCE VOLTAGE	2.5V to 10V rms
ALLOWABLE PHASE SHIFT (SIGNAL TO REFERENCE)	± 20° Will Give No Additional Static Error
TRACKING RATE	100 Revolutions Per Second Minimum (6000 rpm)
SETTLING TIME (179° Step)	20ms max
ACCELERATION CONSTANT (K_a)	650,000/sec/sec
BUSY OUTPUT	Logic "Hi" When BUSY 1μs max 1LS TTL Load
INHIBIT INPUT	Logic "Lo" to INHIBIT 1LS TTL Load
POWER SUPPLIES	
$+V_S$	+12V to +15V @ 10mA
$-V_S$	−12V to −15V @ 10mA
+5V	+4.75V to +5.25V @ 3mA
POWER DISSIPATION	0.320 Watts
TEMPERATURE RANGE	0 to +70°C Operating −60°C to +150°C Storage
DIMENSIONS	1.72" × 1.1" × 0.205" (43.5 × 28.0 × 5.2mm)
WEIGHT	1 oz (28 grams)

NOTES
[1]Accuracy applies at 25°C and for ± 10% signal and reference voltage and frequency variation. ± 5% power supply variation.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply −12V dc to −15V dc.
$+V_S$	Main positive power supply +12V dc to +15V dc.
+5V	Logic voltage.
GND	Power supply ground. Digital ground. Reference voltage low.
Bit 1-12	Parallel output data bits 1MSB = 180°.
Sin Hi Cos Hi	Input analog signals.
R_{HI}	Reference voltage input HI. Reference low connects to GND.
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the the output latches are being updated. Data should not be transferred from the converter output while BUSY is "Hi".
$\overline{\text{ENABLE}}$	The output data bits are set to a low impedance state by application of a logic "lo".
CASE	This should normally be grounded. Case can be be taken to any voltage with a low impedance up ± 20V.
N/C	Pins designated N/C not connected internally.
SIG COM	Internally connected to GND.

ANALOG DEVICES

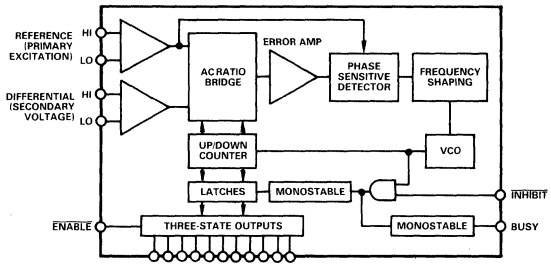
LVDT-to-Digital Converter

2S50

FEATURES
Internal Signal Conditioning
Direct Conversion to Digits
Reference Frequency 400Hz or 1kHz to 10kHz
High MTBF
No External Trims
Absolute Encoding

APPLICATIONS
Industrial Measurement and Gauging
Numerical Control
Avionic Control Systems
Valves and Actuators
Limit Sensing

2S50 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 2S50 series converters translate the outputs from LVDT and RVDT transducers into digits directly. No signal conditioning, trims, preamplifiers, demodulators or filters are required. The 2S50 series can also be used as general purpose ratiometric A-to-D converters; very compatible with load cells, strain gauge bridges, some pressure transducers and interferometers.

The 2S50 linearly converts ac signals into an 11-bit parallel digital word. The digital output is an offset binary word which is the ratio of the signal and reference inputs. When used with LVDT and RVDT transducers, the digital output represents the linear or rotary displacements of the transducer. The converter is a continuous tracking type using a type 2 servo loop.

PRINCIPLE OF OPERATION

The 2S50 is a tracking converter. This means that the output automatically follows the input without the necessity of a convert command.

A conversion is initiated by a change of input signal equivalent to 1LSB of the output.

Each LSB increment of the output is indicated by a "Busy" pulse.

With an LVDT connected to give a null at center position, the output will track the input from digital "1 + all zeroes" to digital "all ones" for plus full scale, and digital "1 + all zeroes" to digital "all zeroes" for negative full scale.

The 2S50 operates only on the ratio of the two inputs for the conversion process. As such the whole system, consisting of excitation oscillator, LVDT and converter, is insensitive to change in excitation voltage, amplitude, frequency and waveshape.

Since a phase sensitive demodulator is included with the conversion loop of the 2S50, the system has a high rejection to signals that are not phase and frequency coherent with the excitation voltage. This feature, combined with ratiometric conversion gives a very high standard of integrity to digitized LVDT and RVDT systems.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

PIN FUNCTION DESCRIPTION

$-V_S$	Main negative power supply -15V dc.
$+V_S$	Main positive power supply $+15$V dc.
$+5$V	Logic supply.
GND	Power supply ground. Digital ground. Reference voltage low.
Bit 1-11	Parallel output data bits.
Ref Hi	Analog reference input (Hi).
Diff Hi	Analog difference input (Hi).
Ref Lo	Analog reference input (Lo).
Diff Lo	Analog difference input (Lo).
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "Lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the output latches are being updated. Data should not be transferred from the converter while BUSY is "Hi".
$\overline{\text{ENABLE}}$	The output data bits are set to a low impedance state by application of a logic "Lo".
CASE	This should normally be grounded. Case can be taken to any voltage with a low impedance up to ± 20V.
N/C	Pins designated N/C not connected internally.

ORDERING INFORMATION

2S50/ X Y 0 B

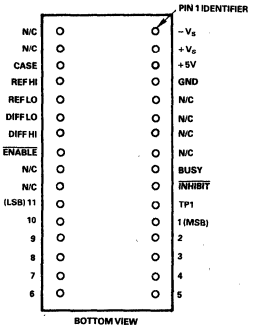
- B — High Reliability Processing
- Y = 1 400Hz reference frequency
- Y = 6 1kHz to 10kHz reference frequency
- X = 4 −55°C to +125°C operating temperature range (Metal Package)
- X = 5 0 to +70°C operating temperature range (Ceramic Package)

SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models	2S50/510	2S50/560	2S50/410	2S50/460
RESOLUTION	11 Bits	*	*	*
ACCURACY[1]	0.1% (Full Scale)	0.1%	0.2%	0.2%
LINEARITY	±1/2LSB	*	*	*
REFERENCE FREQUENCY	400Hz	1kHz–10kHz	400Hz	1kHz–10kHz
SIGNAL INPUTS[2]	2.5V rms	*	*	*
INPUT IMPEDANCE	5MΩ (min)	*	*	*
SLEW RATE (Min)	200LSB/ms	400LSB/ms	200LSB/ms	400LSB/ms
SETTLING TIME (99% FS Step)	50ms	25ms	50ms	25ms
ACCELERATION CONSTANT (k_a)	70,000	650,000	70,000	650,000
BUSY PULSE	1μs (max) 1 LS TTL Load	* *	* *	* *
INHIBIT INPUT	Logic "Lo" to Inhibit 1 LS TTL Load	* *	* *	* *
POWER DISSIPATION	550mW	*	*	*
POWER SUPPLIES[3]	−15V @ 18mA (typ) 25mA (max) +15V @ 18mA (typ) 25mA (max) +5V @ 3mA (max)	* * *	* * *	* * *
TEMPERATURE RANGE				
Operating	0 to +70°C	*	−55°C to +125°C	**
Storage	−60°C to +150°C	*	*	*
DIMENSIONS	1.72" × 1.1" × 0.205" (43.5 × 28.0 × 5.2mm)	* *	1.74" × 1.14" × 0.28" (44.2 × 28.9 × 7.1mm)	** **
WEIGHT	1 oz. (28g)	*	*	*

NOTES
[1]Accuracy applies over ±20% signal voltage, ±20% excitation frequency and full temperature range, and for not greater than 3° phase error between reference and difference inputs.
[2]This is a nominal value.
[3]±12 volts to ±17 volts.
*Specifications same as 2S50/510.
**Specifications same as 2S50/410.
Specifications subject to change without notice.

PIN CONFIGURATION

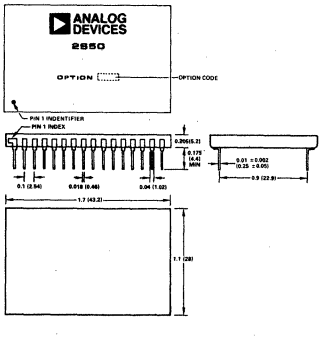


ABSOLUTE MAXIMUM INPUTS (with respect to GND)

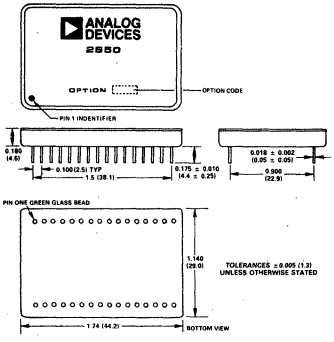
$+V_S$	0V to +17V dc
$-V_S$	0V to −17V dc
+5V	0V to +5.5V dc
Ref, Hi to Lo	±20V dc
Diff, Hi to Lo	±20V dc
Case to GND	±20V dc
Any Logical Input	−0.4V to +5.5V dc

OUTLINE DIMENSIONS
PACKAGING SPECIFICATION

Dimensions shown in inches and (mm).



2S50/510 and 560 Options, 0 to +70°C (Ceramic Package)



2S50/410 and 460 Options, −55°C to +125°C (Metal Package)

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Microprocessor Based Autoranging RTD/Thermistor Meter

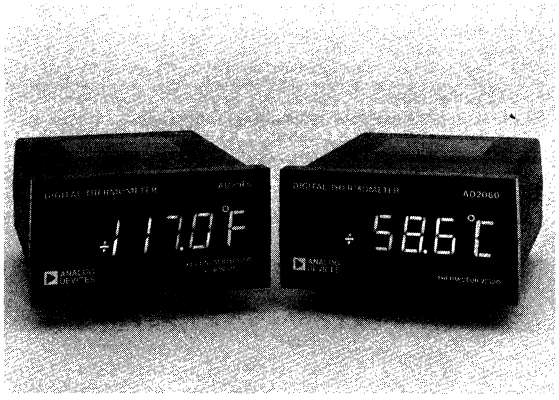
AD2060/AD2061

FEATURES

Temperature Ranges: −328°F to +1562°F
−200°C to +850°C
Autoranging: 0.1° from −199.9° to +199.9°; 1°≥200°
Sensor Selection (AD2060): RTD 100Ω Platinum
α = 0.00385, 0.00390, 0.00392 or 2252Ω Thermistor
Universal Meter (AD2061) Sensor User Programmable
Switch Selectable Sensor Configuration: 2, 3 or 4-wire
7-Bit ASCII Character Serial Data Output
Automatic Self-Calibration for Gain, Offset, Excitation and Sensor Linearization
Optional Linearized Analog Voltage Output: 1mV/degree
Optional Isolated 20mA ASCII Loop/TTL Serial Outputs

APPLICATIONS

Temperature Monitoring in Laboratory, Manufacturing and Quality Control Environments
Process Control Temperature Measurements
Remote Data Logging



4

GENERAL DESCRIPTION

The AD2060/AD2061 are high performance single channel 3½ digit RTD/Thermistor meters that can measure temperature accurately between −328°F and +1562°F (−200°C and +850°C). Both meters offer autoranging from 0.1°C/F to 1°C/F. The AD2060 is supplied factory programmed for one of four sensor types: 100Ω Platinum RTDs: α = 0.00385, 0.00390, 0.00392 or a 2252Ω Thermistor. The AD2061 is a universal meter in which the user selects one of the four sensor types via switch programming. The microprocessor based AD2060/AD2061 provides gain, offset and excitation error correction, linearization and °C/°F scaling in firmware. The AD2060/AD2061 display temperature information on large 0.56"(14.3mm) high LEDs. Digital information is provided in 7-bit standard ASCII character serial format with baud rate selection for easy interface to printers, terminals and other peripherals. For remote data acquisition applications, an optional isolated 2-wire 20mA ASCII serial loop/TTL compatible interface is available. For driving recorders or other analog instruments, an optional linearized analog voltage output of 1mV/degree is available. Selection of °C or °F scaling is accessed by removing the front panel lens and setting the selector switch to its proper position.

The AD2060/AD2061 can be ordered in one of the following power versions: 120V ac, 240V ac or +7.5V dc to +28.0V dc. Input voltage protection of 180V peak (RTD short to ac line), common-mode voltage to 1400V peak (ac version) with overrange and open sensor detection is provided. These meters are rated for operation over the 0 to +40°C temperature range. Each AD2060/AD2061 is burned-in for 168 hours @ 50°C with on/off power cycles for increased reliability.The AD2060/AD2061 are supplied in rugged molded plastic cases that meet UL94V-0 and DIN/NEMA standard dimensions.

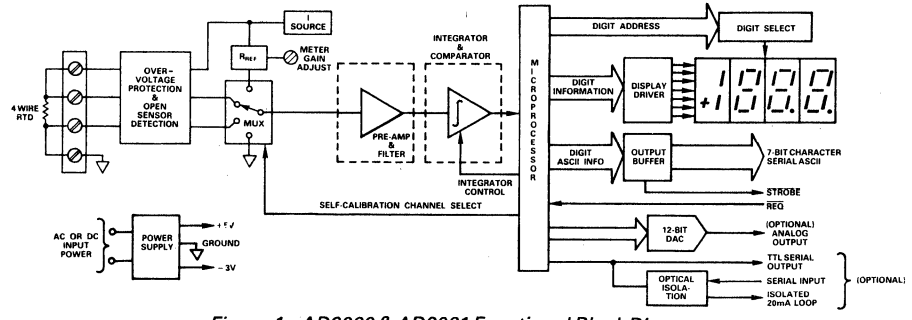


Figure 1. AD2060 & AD2061 Functional Block Diagram

SPECIFICATIONS (typical @ +25°C and rated supply voltages unless otherwise specified)

RTD INPUTS
- RTD Types: 100Ω Platinum
  α = 0.00385 (Per DIN 43760)
  α = 0.00390
  α = 0.00392
- Configuration: 2, 3 or 4 Wire
- Excitation Current: 0.25mA nominal
- External Lead
  Resistance Effect: Automatically Compensated for 3 & 4 wire configurations
- Lead Resistance: 50Ω/Lead max; RTD + Lead Resistance must be less than 400Ω
- 3 Wire Error: 2.8°C/Ω of impedance imbalance
- Open Sensor: DISPLAY +EEE
- RTD Short to ac Line: Internal protection provided to 180V peak (130V rms)
- Maximum Common-Mode Voltage: 1400V peak (ac or dc) between input and power line ground (ac version)
- Common-Mode Rejection Ratio: 100dB ac power to RTD input
- Normal Mode Rejection: 60dB @ 50/60Hz

THERMISTOR INPUTS
- Thermistor Type: Series 400 R = 2252Ω
- Configuration: 2 Wire
- Open Sensor: DISPLAY -EEE

ACCURACY
- Temperature Resolution: Autoranging (0.1° from −199.9° to +199.9°, 1°≥200°)
- All Ranges Guaranteed Monotonic
- Range Temperature Coefficient: 20ppm/°C typ, 30ppm/°C max
- Readout Accuracy* @ +25°C

Sensor	Range	Accuracy
100Ω RTD α = 0.00385	−200°C to +850°C	±0.3°C ± 1/2LSD
	−328°F to +1562°F	±0.6°F ± 1/2LSD
100Ω RTD α = 0.00392	−200°C to +640°C	±0.3°C ± 1/2LSD
	−328°F to +1184°F	±0.6°F ± 1/2LSD
100Ω RTD α = 0.00390	−200°C to +640°C	±0.3°C ± 1/2LSD
	−328°F to +1184°F	±0.6°F ± 1/2LSD
Thermistor R = 2252Ω	−30°C to +100°C	±0.4°C ± 1/2LSD
	−22°F to +212°F	±0.8°F ± 1/2LSD

*Readout Accuracy: Includes Gain and Offset Errors. Recommended Recalibration Interval 15-MONTHS.

DIGITAL OUTPUTS
- Character Serial ASCII
  Data: Eleven transmitted characters, (each 7 bits plus strobe)
  Drive Capability: 2TTL loads, CMOS/TTL compatible
  Strobe: Negative transition determines when character serial data is valid. CMOS/TTL compatible.
  Character Rate: Selectable on P1 (Pin 32)
  Grounded: 25 characters/sec. (SLOW)
  Open: 100 characters/sec. (FAST)
- Isolated Serial Output (Optional)
  Data: Asynchronous ASCII 20mA current loop (Optically isolated to ±600V peak)
  Baud Rate: Selectable on P1 (Pin 32)
  Grounded: 300 baud (SLOW)
  Open: 1200 baud (FAST)
  Distance: 10,000 ft. max
- Nonisolated Serial Output (Optional)
  Data: Serial ASCII
  Drive Capability: 2TTL Loads, CMOS/TTL compatible
  Baud Rate: (same as Isolated Serial Output)
- Overrange: ±EEE.E
- Minimum Time Between New Data Update: 150ms

DIGITAL INPUTS
- REQ: Low-Level Triggered: Must go low at any time other than during data transmission to be recognized. REQ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by REQ.
- SERIAL INPUT (Optional): Edge Triggered, Current On to Current Off: Must be triggered at any time other than during data transmission to be recognized. Serial Input triggered during data transmission will not be acknowledged and the 20mA isolated/TTL compatible serial output transmission will not occur. Display readings are not effected by Serial Input.

ANALOG OUTPUT (OPTIONAL)
- Voltage: 1mV/degree, linearized
- Current: ±2mA max drive
- CMV: 1400V peak (ac or dc) between Analog Output Ground & ac Power Line Ground
- Overrange: +2.048V, −0.512V
- Accuracy: ±2mV from Display Reading

ANALOG TO DIGITAL CONVERSION
- Technique: Offset Dual Slope with Gain and Offset Error Correction
- Rate: 2.5 Conversions/Second Typical
- Input Integration Period: 100ms for 50/60Hz Noise Rejection

POWER REQUIREMENTS (Choice of Three Supply Ranges)
- ac: 90V ac to 132V ac @ 25mA (47Hz to 500Hz)
  198V ac to 264V ac @ 12.5mA (47Hz to 500Hz)
- dc: +7.5V to +28V dc @ 200mA (Protected Against Supply Reversals)

DISPLAY
- Type: Seven Segment Orange LED 0.56" (14.3mm) high
- Polarity Indication: "+" or "−" displayed
- Overrange Indication: ±EEE
- Display Test: At Power Turn-On, 3 Second Display of "+188.8." Tests all Segments of Display

ENVIRONMENTAL
- Rated Temperature Range: 0 to +40°C
- Operating Temperature Range: −10°C to +50°C
- Storage Temperature Range: −40°C to +85°C
- Relative Humidity: Meets MIL-STD-202E, Method 103B (0 to 90%, Noncondensing)

DIMENSIONS
- Case: 3.78" × 1.89" × 5.13" (96.8mm × 48.9mm × 131.3mm), rugged molded plastic case. Meets UL94V-0 and DIN/NUMA Standard dimensions
- Weight: 15.2 oz (431 grams) max, ac powered
  12.0 oz (341 grams) max, dc powered.

RELIABILITY
- MTBF: >55,000 hours calculated
- Burn In: 168 Hours at +50°C with Power ON/OFF Cycles.
- Calibration: NBS Traceable
- Recalibration: Recommended 15-Month Intervals
- Warranty: 12 months

CONNECTOR
One 44 pin 0.1" (2.54mm) spacing card edge connector Viking 3VH22/1 JN5 or equivalent
Optional: Order AC2630

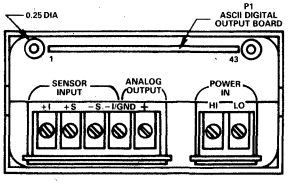


Figure 2. Rear Panel View

ORDERING GUIDE

AD2061 /__/__/__
AD2060 /__/__/__/__

SENSOR TYPE*
(385) 100Ω Platinum RTD α = 0.00385
(390) 100Ω Platinum RTD α = 0.00390
(392) 100Ω Platinum RTD α = 0.00392
(2252) Thermistor R = 2252Ω
} ENTER

POWER OPTION*
(1) 120V ac
(2) 240V ac
(3) +7.5V dc to +28V dc
} ENTER

ANALOG OUTPUT OPTION
(A) Contains Analog Output
(Blank) Does Not Contain Analog Output
} ENTER

SERIAL OUTPUT OPTION
(S) Contains Serial Output
(Blank) Does Not Contain Serial Output
} ENTER

*Only one option can be ordered. The sensor type does not need to be specified when ordering the AD2061 since it is user programmable.

Specifications subject to change without notice.

Microprocessor Based Autoranging Thermocouple Meters

AD2070/AD2071

FEATURES

- **Autoranging (0.1° – 1°)**
- **4 1/2 Digit Resolution**
- **Automatic Self-Calibration for Gain, Offset, Cold Junction Compensation and Thermocouple Linearization**
- **J, K, T, E, R, S, C, B, J DIN, and T DIN Thermocouple Selection**
- **Universal Meter (AD2071), User Programmable for all Thermocouple Types**
- **Four Port Isolation: Input, Power, Digital Output and Analog Output**
- **Optional Isolated and Linearized Analog Voltage Output 1mV/Degree**
- **Optional Isolated 20mA Loop/TTL Serial Data Output**
- **Optional Isolated RS-232/TTL Serial Data Output**
- **Heavy Gauge Rugged Metal Case**

4

GENERAL DESCRIPTION

The AD2070/AD2071 are high performance, microprocessor based, autoranging, single channel thermocouple meters that can measure temperature accurately from −328°F to +4200°F (−200°C to +2315°C). The AD2070 is supplied factory programmed for any of the following ten thermocouple types: J, K, T, E, R, S, C, B, J DIN, and T DIN. The AD2071 is a universal meter in which the user selects one of the ten thermocouple types via switch programming. Both meters offer autoranging from 0.1°C/°F to 1°C/°F. The microprocessor based AD2070/AD2071 provides gain and offset error correction, cold junction compensation, thermocouple linearization and °C/°F scaling in firmware.

The AD2070/AD2071 display temperature information on large 0.56″ (14.3mm) high LEDs. Digital information is provided in standard ASCII character serial format with rate selection for easy interface to printers. For remote data acquisition applications, an optional isolated 20mA serial loop or RS-232 compatible interface is available. For driving recorders or other analog instruments, an optional isolated and linearized analog voltage output of 1mV/degree is available. Selection of °C or °F scaling is accessed by removing the front panel lens and setting a selector switch.

The AD2070/AD2071 can be ordered in one of the following power versions: 120V ac, 240V ac or +7.5V dc to +28.0V dc. Input overvoltage protection rating is 300V peak (thermocouple to ac line shorts). The common-mode voltage rating is 1400V peak. Overrange and open thermocouple detection are provided in all models. Analog output and digital outputs are isolated to 500V peak from power, input and output sections. Each meter is burned-in for 168 hours at 50°C with on/off power cycles for increased reliability. These meters are rated for operation over a +10°C to +40°C range. The AD2070/AD2071 are supplied in a heavy gauge, rugged metal case that meets DIN/NEMA standard dimensions.

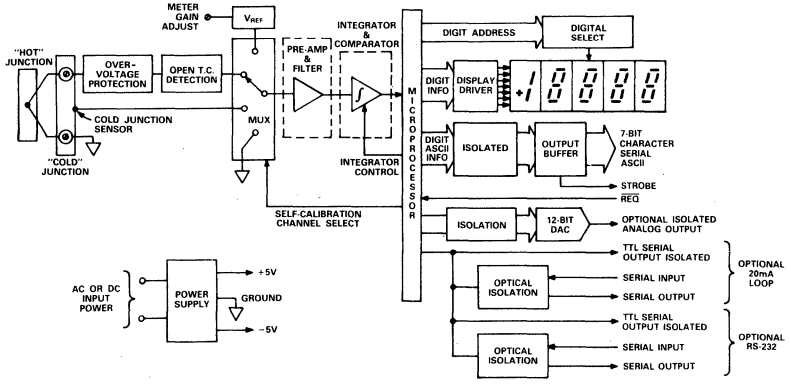


Figure 1. AD2070/AD2071 Functional Block Diagram

SPECIFICATIONS (typical @ +25°C and rated supply voltages unless otherwise specified)

THERMOCOUPLE INPUTS

THERMOCOUPLE TYPES:
J, K, T, E, R, S, B, C, J DIN and T DIN
INPUT IMPEDANCE:
100MΩ
EXTERNAL LEAD RESISTANCE EFFECT:
<20μV per 350Ω of Lead resistance
COLD JUNCTION COMPENSATION ERROR:
±0.3°C max (+10°C to +40°C)
OPEN THERMOCOUPLE:
+EEEE Display; +EEEE.E ASCII DIGITAL OUTPUT: +3.500V ANALOG OUTPUT
THERMOCOUPLE SHORT TO AC LINE:
Internal Protection Provided to 300V peak, (200V ac rms)
COMMON-MODE VOLTAGE:
1400V peak (dc or ac), Between Input and Power Line Ground
COMMON-MODE REJECTION RATIO:
>130dB with 250Ω Source Imbalance (dc to 60Hz)
NORMAL-MODE REJECTION RATIO:
>80dB @ 50/60Hz

DIGITAL OUTPUTS

ISOLATED CHARACTER SERIAL ASCII (Standard)
DATA:
Eleven transmitted characters, each 7 bits plus strobe
DRIVE CAPABILITY:
2TTL Loads, CMOS/TTL compatible
OVERRANGE: ±EEEE.E
STROBE:
Positive transition determines when character serial data is valid. CMOS/TTL compatible.
ISOLATION:
500V Between Input, Analog Output and Power Input
CHARACTER RATE:
Selectable on P1 (Pin 20)
Grounded: 25 Characters/sec. (SLOW)
Open: 100 Characters/sec. (FAST)

ISOLATED SERIAL OUTPUT (Optional)
DATA:
Asynchronous ASCII 20mA current loop or RS-232
BAUD RATE:
Selectable on P1 (Pin 20)
Grounded: 300 baud (SLOW)
Open: 1200 baud (FAST)
OVERRANGE:
±EEEE.E
DISTANCE:
50 ft. (RS-232), 10,000 ft. (20mA loop)
ISOLATION:
500V Between Input, Analog Output and Power Input

ISOLATED SERIAL OUTPUT
DATA:
Serial ASCII TTL
DRIVE CAPABILITY:
2TTL Loads, CMOS/TTL Compatible
BAUD RATE:
(same as above)
OVERRANGE:
±EEEE.E
ISOLATION:
500V Between Input, Analog Output and Power Input
MINIMUM TIME BETWEEN NEW DATA UPDATE:
100ms

DIGITAL INPUTS

$\overline{\text{REQ}}$: LOW-LEVEL TRIGGERED:
Must go low at any time other than during data transmission to be recognized. $\overline{\text{REQ}}$ line taken low during data transmission will not be acknowledged and the ASCII digital output transmission will not occur. Display readings are not effected by $\overline{\text{REQ}}$.

$\overline{\text{SERIAL INPUT}}$: EDGE TRIGGERED, CURRENT ON TO CURRENT OFF
Must be triggered at any time other than during data transmission to be recognized. $\overline{\text{Serial Input}}$ triggered during data transmission will not be acknowledged and the isolated 20mA loop/TTL or isolated RS-232/TTL compatible serial output transmission will not occur. Display readings are not effected by $\overline{\text{Serial Input}}$.

ISOLATED ANALOG OUTPUT (OPTIONAL)

VOLTAGE:
1mV/degree, Fahrenheit or Celsius linearized
CURRENT:
±2mA max
OVERRANGE:
+3.500V, −0.328V
ACCURACY:
±2mV from Display Reading
ISOLATION:
500V Between Input, Digital Output and Power Input

ACCURACY

TEMPERATURE RESOLUTION:
Autoranging 0.1°C/°F – 1°C/°F (see Sensor Ranges)
RANGE TEMPERATURE COEFFICIENT:
20ppm/°C typ, ±40ppm/°C max (of Reading)
All Ranges are Guaranteed Monotonic.

Sensor Type	Range	Readout Accuracy @ +25°C[1]	
J	−200.0°C to +760.0°C	±0.4°C	±1/2 LSD
J	−328.0°F to +1400.0°F	±0.8°F	±1/2 LSD
J DIN	−200.0°C to +760.0°C	±0.4°C	±1/2 LSD
J DIN	−328.0°F to +1400.0°F	±0.8°F	±1/2 LSD
K	−200.0°C to +1250.0°C	±0.4°C	±1/2 LSD
K	−328.0°F to +1999.9°F	±0.8°F	±1/2 LSD
K	+2000°F to +2282°F	±0.8°F	±1/2 LSD
T	−200.0°C to +400.0°C	±0.4°C	±1/2 LSD
T	−328.0°F to +752.0°F	±0.8°F	±1/2 LSD
T DIN	−200.0°C to +400.0°C	±0.4°C	±1/2 LSD
T DIN	−328.0°F to +752.0°F	±0.8°F	±1/2 LSD
E	−200.0°C to +1000.0°C	±0.4°C	±1/2 LSD
E	−328.0°F to +1832.0°F	±0.8°F	±1/2 LSD
R	0°C to +299°C	±2°C	±1/2 LSD
R	+300°C to +1768°C	±1°C	±1/2 LSD
R	+32°F to +570°F	±4°F	±1/2 LSD
R	+571°F to +3214°F	±2°F	±1/2 LSD
S	0°C to +299°C	±2°C	±1/2 LSD
S	+300°C to +1768°C	±1°C	±1/2LSD
S	+32°F to +570°F	±4°F	±1/2 LSD
S	+571°F to +3214°F	±2°F	±1/2 LSD
B	+300°C to +400°C	±3°C	±1/2 LSD
B	+401°C to +1820°C	±1°C	±1/2LSD
B	+572°F to +752°F	±6°F	±1/2 LSD
B	+753°F to +3308°F	±2°F	±1/2 LSD
C	0°C to +400°C	±3°C	±1/2 LSD
C	+401°C to +2315°C	±1°C	±1/2 LSD
C	+32°F to +752°F	±6°F	±1/2 LSD
C	+753°F to +4200°F	±2°F	±1/2 LSD

NOTE
[1]Readout Accuracy includes all Conformity Errors, CJC Errors, Gain and Offset errors. Recommended recalibration interval 15-months. Warm-up time 10 minutes.

ANALOG TO DIGITAL CONVERSION

TECHNIQUE:
Offset Dual Slope with Gain and Offset Error Correction
RATE:
2.5 Conversions/Second (Typical)
INPUT INTEGRATION PERIOD:
100 Milliseconds for 50/60Hz Noise Rejection

POWER REQUIREMENTS (Choice of Three Supply Ranges)

ac:
90V ac to 132V ac @ 25mA (dc to 1kHz)
198V ac to 264V ac @ 12.5mA (dc to 1kHz)
dc:
+7.5V to +28V dc @ 600mA (Protected Against Supply Reversals)

DISPLAY

TYPE:
Seven Segment Orange LED 0.56" (14.3mm) high
POLARITY INDICATION:
"+" or "−" displayed
OVERRANGE INDICATION:
±EEEE
DISPLAY TEST:
At Power Turn-On, 3 Second Display of "+1888.8." Tests All Segments of Display

ENVIRONMENTAL

RATED TEMPERATURE RANGE:
+10°C to +40°C
OPERATING TEMPERATURE RANGE:
−10°C to +50°C
STORAGE TEMPERATURE RANGE:
−40°C to +85°C
RELATIVE HUMIDITY:
Meets MIL-STD-202E, Method 103B
(0 to 90%, Noncondensing)

RELIABILITY

MTBF:
> 200,000 hours calculated
BURN IN:
168 Hours at +50°C with Power On/Off Cycles

CALIBRATION:
NBS Traceable
RECALIBRATION:
Recommended 15-Month Intervals
WARRANTY:
12 months

DIMENSIONS

CASE:
3.78" × 1.89" × 6.75" (96.8mm × 48.0mm × 171.0mm), rugged aluminum case. DIN/NEMA Standard.
PANEL CUT OUT: $3.622^{+0.031}_{-0.000}$" ($92^{+,8}_{-,0}$)mm × $1.771^{+0.024}_{-0.000}$ ($45^{+,6}_{-,0}$)mm
PANEL THICKNESS:
1/16" (1.5mm) to 3/16" (4.8mm)
WEIGHT:
23 oz. (650 grams) typ

Specifications subject to change without notice.

GENERAL THERMOCOUPLE OPERATION

A thermocouple is a device that measures temperature by converting thermal energy to electrical energy. In order for this conversion process to take place, two phenomena must occur: (1) Two dissimilar metals must be bound together at one end to form the "HOT" or measuring junction with the free end attached to the instrument constituting the "COLD" or reference junction (shown in Figure 2) and (2) the "HOT" and "COLD" junction must be maintained at different temperatures (ΔT). The magnitude of voltage (V_1) developed at the "COLD" junction is directly proportional to temperature differential developed between the two junctions.

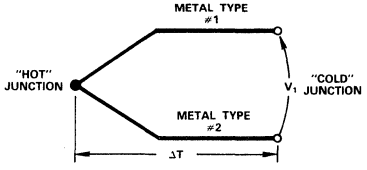


Figure 2. Typical Thermocouple

In order for an accurate temperature measurement to be made of the "HOT" junction point, the "COLD" junction temperature must be known. Currently, there are two approaches in which this can be accomplished:

1) By setting the "COLD" junction temperature to a fixed value, or (2) by measuring the ambient temperature at the "COLD" junction termination.

One common convention for setting the "COLD" junction temperature to a fixed value is to place that junction into an ice bath which is set at the melting temperature of ice. 32°F/0°C.

The AD2070/AD2071 use the second approach. By physically placing a "COLD" junction temperature sensor near the thermocouple input terminal block, the most accurate measurement of the ambient "COLD" junction temperature is made.

THERMOCOUPLE TYPE

Thermocouples come in many forms depending upon the two dissimilar metals used, temperature range, and the application required. Because any two dissimilar metals that are bonded together can theoretically form a thermocouple, the National Bureau of Standards (NBS) sets standards and establishes calibration tables for each thermocouple temperature vs. output voltage. Shown in Table I are the thermocouple types, metallic composition, and environmental applications that can be interfaced with the AD2070/AD2071.

Each thermocouple type is designated by an alphabetic letter that is accepted by the American National Standards Institute (ANSI). Shown in Figure 3 are the thermocouple types, that can interface with the AD2070/AD2071, displaying each NBS calibrated range and the corresponding specified operating range of the meter.

ANSI Designated Thermocouple Type	Metallic Composition	Environmental Applications
E	Chromel-Constantan	Vacuum or inert, mildly oxidizing or reducing atmosphere. Not subject to corrosion at sub-zero temperatures.
J	Iron-Constantan	Reducing atmospheres
K	Chromel-Alumel	Clean Oxidizing Atmosphere
S	Platinum-Platinum 10% Rhodium	High resistance to oxidation and corrosion.
T	Copper-Constantan	Mildly oxidizing and reducing atmospheres where moisture is present, high temperatures up to +750°F.
R	Platinum-Platinum 13% Rhodium	High resistance to oxidation and corrosion.
B	Platinum 6% Rhodium-Platinum 30% Rhodium	Oxidizing or inert atmosphere.
C*	Tungsten 5% Rhenium-Tungsten 26% Rhenium	Vacuum, inert or Hydrogen Atmosphere
*Not ANSI Symbol		
DIN Designated Type		
J	Iron-Constantan	Reducing atmosphere
T	Copper-Constantan	Mildly oxidizing and reducing atmospheres where moisture is present, high temperatures up to +750°F.

Table I. Thermocouple Types, Metallic Composition, and Environmental Applications

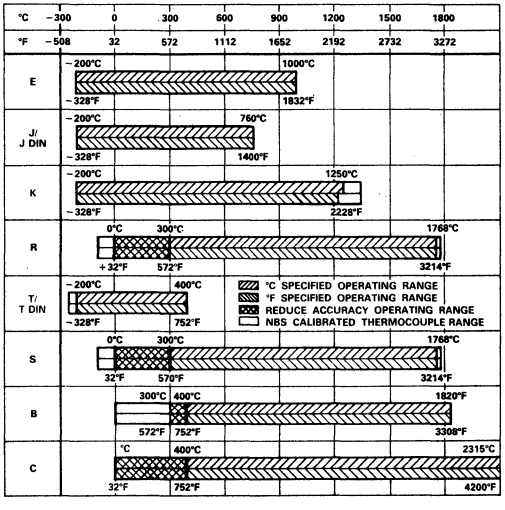


Figure 3. Thermocouple Temperature Range & AD2070/AD2071 Specified Operating Ranges

COLD JUNCTION COMPENSATION AND LINEARIZATION

Cold junction compensation is provided by measuring the temperature of the thermocouple screw terminals. The AD2070/AD2071 places an accurate temperature sensor in the terminal block to obtain the best possible thermal contact. The screw terminal temperature is measured periodically and stored in memory. The microprocessor uses this information to mathematically reference the thermocouple to 0°C before linearization is performed. Thermocouple linearization, for the AD2070/AD2071 is accomplished in firmware using the multisegment piecewise linear approximation technique. Here, the thermocouple span is broken up into about seventy linear segments that were computer selected to provide the least squared error to segment conformity (see Figure 4). This multisegment information is stored digitally in look-up tables and used for each thermocouple measurement. Since linearization is provided digitally, all conformity errors due to time and temperature are eliminated.

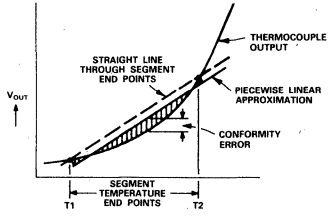


Figure 4. Linearization and Conformity Error

POWER SUPPLY

The AD2070/AD2071 are configured in three input power versions: 120V ac, 240V ac and +7.5V dc to +28V dc. The AD2070/AD2071 are designed using an off-line high frequency switching power supply circuit. Using this technique, the input voltage is rectified to a high voltage, switched through a high frequency transformer and then rectified and filtered. Using this technique small size and isolated voltages between all sections of the meter is obtained.

> WARNING HIGH VOLTAGE:
> The internal power supply circuit generates lethal voltages as high as 700V. Service to this meter should be performed by qualified personnel only.

The AD2070/AD2071 provides protection against high common-mode voltages as high as 1400V peak, that may be present between the thermocouple input and power supply ground (shown in Figure 5). The CMV figure applies for both ac, and dc powered meters. The AD2070/AD2071 also provides protection up to 300V peak across the thermocouple inputs in case one side is accidentally shorted to a 240V ac rms power line.

Additionally, Digital Output, Analog Output and Input sections of the AD2070/AD2071 are isolated from each other by up to 500V peak.

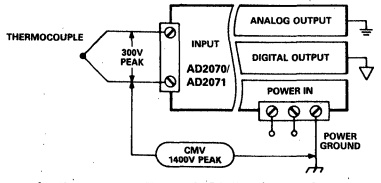


Figure 5. Rated CMV Specifications

ISOLATED ANALOG OUTPUT (Optional)

Shown in Figure 6 is the simplified block diagram of the optional analog output. It consists of a 12-bit digital-to-analog converter followed by an amplifier that provides a 1mV per degree output voltage for either the Fahrenheit or Celsius temperature scales. This output voltage is also compensated for cold junction effects and thermocouple linearization. The Analog Output is isolated to 500V peak between Input and Digital Output.

The two potentiometers for analog output gain and offset adjustments are located behind the lens.

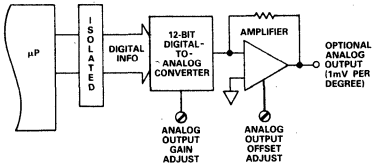


Figure 6. Optional Isolated Analog Output

ASCII DIGITAL OUTPUTS

The AD2070/AD2071 provides its 4 1/2 digit plus sign information in an ASCII character serial format. A 7-bit Digital ASCII output, request ($\overline{REQ}$), STROBE and CHARACTER/BAUD RATE lines are shown in Figure 1. Optional isolated 20mA Loop/TTL and Isolated RS-232/TTL serial output are provided in serial ASCII format, with $\overline{SERIAL\ INPUT}$ and CHARACTER/BAUD RATE control for remote data acquisition applications.

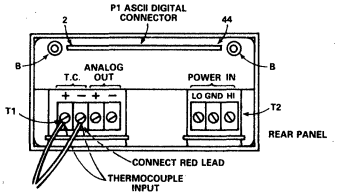


Figure 7. Rear Panel View

ORDERING GUIDE

THERMOCOUPLE TYPE*
J
K
T
E
R
S
C
B
JDIN
TDIN

AD2071 /——/——/——/——
AD2070 /——/——/——/——/——
ENTER

POWER OPTION*
(1) 120V ac
(2) 240V ac
(3) +7.5V dc to +28V dc
ENTER

ANALOG OUTPUT OPTION
(A) Contains Analog Ouput
(BLANK) Does Not Contain Analog Output
ENTER

SERIAL OUTPUT OPTION*
(S1) Contains RS-232 Serial Output
(S2) Contains 20mA Loop Serial Output
(BLANK) Does Not Contain Serial Output
ENTER

Example Order Number: AD2070/J/1/A/S1 = AD2070 for J Thermocouple Type, 120V ac Power, Analog Voltage Output and RS-232 Serial Output.

*Only one option can be ordered. The thermocouple type does not need to be specified when ordering the AD2071 since it is user programmable.

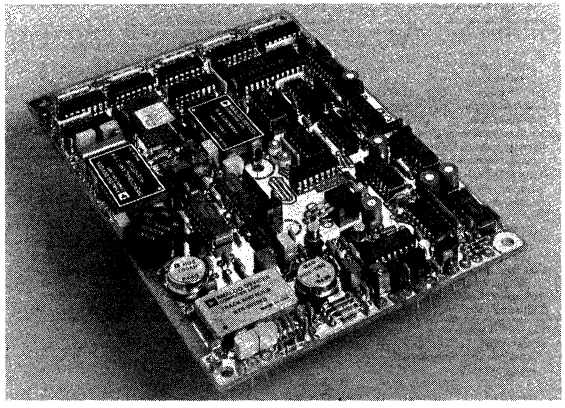
ANALOG DEVICES

10-Bit Video Analog-to-Digital Converter

CAV-1040

FEATURES
10-Bit Resolution
40MHz Word Rate
Single 35-In^2 PC Board
ECL Compatible
No External Circuits Required

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Transient Analysis



4

GENERAL DESCRIPTION

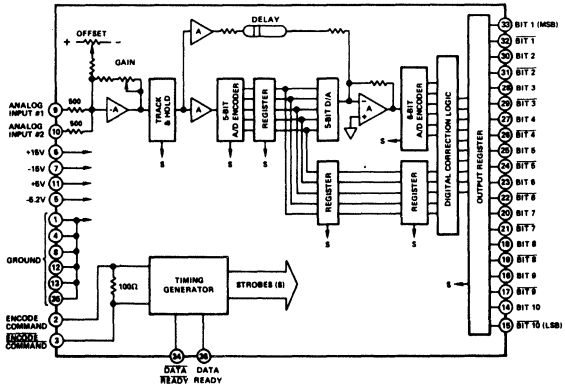
The Analog Devices Model CAV-1040 A/D converter is a "system solution" which combines 10-bit resolution, 40MHz word rates, and small size to solve high-speed digitizing problems. Its design is based on proven concepts introduced in the MOD-1020 and MOD-1205 A/D Converters and takes advantage of recent advances in technology to achieve a new level of performance in high-resolution converters.

It is pin-for-pin compatible with the industry's first 10-bit, 20MHz A/D, the MOD-1020. But it *doubles* the word rate of its predecessor, making it possible for system designers to upgrade their systems without new layouts.

This remarkable converter is a complete answer to the question of digitizing radar, video, and/or other high-frequency inputs; it includes a track-and-hold, along with encoding and timing circuits. The CAV-1040 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high-speed A/D conversion.

For applications requiring maximum analog bandwidth, the CAV-1040A is the choice. In this version, the input operational amplifier and its associated offset and gain controls have been eliminated; this effectively doubles the analog input bandwidth.

All inputs and outputs are ECL compatible. Analog input impedance is 250 ohms on 1V range; 500 ohms on 2V range. The A/D requires only an encode command and external power supplies for operation. The CAV-1040 is repairable and backed by Analog Devices' limited one-year warranty.



CAV-1040 Block Diagram

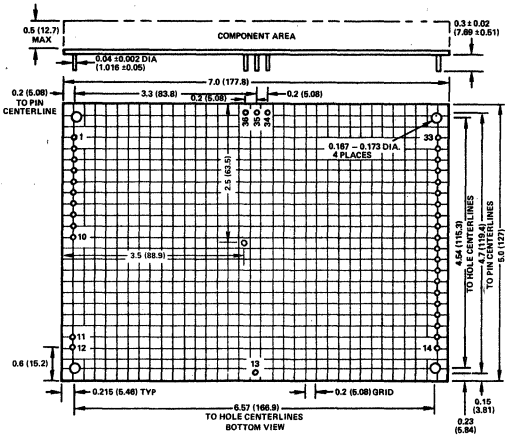
This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical at +25°C with nominal power supplies unless otherwise noted)

Model	Units	CAV-1040	CAV-1040A
RESOLUTION (FS = Full Scale)	Bits	10	*
	%FS	0.1	*
LSB WEIGHT			
1V p-p FS	mV	1	N/A
2V p-p FS	mV	2	*
ACCURACY			
(Including Linearity) @ dc	% FS ± 1/2LSB	0.05	*
Monotonicity		Guaranteed	
Nonlinearity Vs. Temperature	ppm/°C	10	*
Offset vs. Temperature	ppm/°C (max)	200 (300)	*
Gain vs. Temperature	ppm/°C (max)	50 (100)	*
DYNAMIC CHARACTERISTICS			
In-Band Harmonics[1]			
500kHz input	dB below FS, min	65	*
2.3MHz input	dB below FS, min	55	*
9.3MHz input	dB below FS, min	48	*
Conversion Time[2]	ns	100 + 1 clock period	*
Conversion Rate	MHz, max	40	*
Aperture Uncertainty (Jitter)	ps, rms max	20	*
Effective Aperture Delay Time (± 2ns tolerance unit-to-unit)	ns	−2	8
Signal to Noise Ratio (SNR)[3]	dB, min	56	*
Noise Power Ratio (NPR)[4]	dB (min)	50 (47)	*
Transient Response[5]	ns	50	*
Overvoltage Recovery[6]	ns	50	*
Input Bandwidth			
Small Signal, 3dB[7]	MHz	30	60
Large Signal, 3dB[8]	MHz	20	40
Two-Tone Linearity (@Input Frequencies)[9] (360kHz; 390kHz)	dB below FS, min	67	*
Differential Phase[10]	°	0.5	*
Differential Gain[10]	%	1	*
ANALOG INPUT			
Voltage Range			
Input Pins 9 & 10 Connected	V, p-p FS	1	N/A
Input Pin 9 or 10	V, p-p FS	2	N/A
	V, max	±4	*
Input Pin 9	V, p-p FS	N/A	2 ± 2%
Input Type		Either Unipolar or Bipolar	Bipolar only
Impedance			
1V Input Range	Ohms	250	N/A
2V Input Range	Ohms	500	*
Offset	mV	Adjustable to Zero with On-Card Potentiometer	±4 (Not adjustable)
vs. Temperature	ppm/°C (max)	200 (300)	*
ENCODE COMMAND INPUT[11]			
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Input)	V	"1" = −0.9	*
Impedance (Line-to-Line)	Ohms, max	100	*
Rise and Fall Times	ns, max	5	*
Width			
Min	ns	10	*
Max		70% of Encode Command period	*
Frequency[12]	MHz	dc to 40	*
DIGITAL OUTPUT			
Format	Bits	10 Parallel; NRZ	*
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Output)	V	"1" = −0.9	*
Drive (Line-to-Line)	Ohms, min	75	*
Time Skew	ns, max	5	*
Coding		Binary (BIN); 2's Complement (2SC)	Compl. Binary (CBIN) Compl. 2's Compl. (C2SC)
DATA READY OUTPUT			
Logic Levels, ECL-Compatible	V	"0" = −1.7	*
(Balanced Output)	V	"1" = −0.9	*
Drive (Line-to-Line)	Ohms, min	75	*
Rise and Fall Times	ns, max	5	*
Duration	ns (max)	10 (±2)	*
POWER REQUIREMENTS[13]			
+15V ±5%	mA, max	375	*
−15V ±5%	mA, max	200	*
+5V ±5%	mA, max	25	*
−5.2V ±5%	A, max	2.5	*
Power Consumption	W (max)	20 (22)	*
TEMPERATURE RANGE			
Operating	°C	0 to +70	*
Storage	°C	−55 to +85	*
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500	*
CONSTRUCTION			
Single Printed Circuit Card	Inches	7.0 × 5.0 × 0.5	*
MEAN TIME BETWEEN FAILURES[14]	Hours		3.22×10^4

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	19	BIT 8
2	ENCODE COMMAND	20	BIT 7
3	ENCODE COMMAND	21	BIT 7
4	GROUND	22	BIT 6
5	-5.2V	23	BIT 6
6	+15V	24	BIT 5
7	-15V	25	BIT 5
8	GROUND	26	BIT 4
9	ANALOG INPUT #1	27	BIT 4
10	ANALOG INPUT #2	28	BIT 3
11	+5V	29	BIT 3
12	GROUND	30	BIT 2
13	GROUND	31	BIT 2
14	BIT 10	32	BIT 1
15	BIT 10	33	BIT 1
16	BIT 9	34	DATA READY
17	BIT 9	35	GROUND
18	BIT 8	36	DATA READY

ALL GROUND PINS ARE CONNECTED TOGETHER WITHIN THE ADC.

NOTES

[1]In-Band Harmonics expressed in terms of spurious in-band signals and related harmonics generated at 40MHz encode rate.

[2]Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits.

[3]Rms signal to rms noise ratio with 500kHz analog input.

[4]Dc to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz, and encode rate of 40MHz.

[5]For full-scale step input, 10-bit accuracy attained in specified time.

[6]Recovers to 10-bit accuracy in specified time after 2 × FS input overvoltage.

[7]With analog input 40dB below FS.

[8]With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 8MHz on CAV-1040; dc to 20MHz on CAV-1040A.)

[9]Each input frequency applied at level 7dB below full scale.

[10]Differential phase and differential gain measured with 20-IRE unit reference.

[11]Transition from digital "0" to digital "1" initiates encoding.

[12]For operation at word rates below 500kHz, consult factory.

[13]±15V must be equal and opposite within 200mV and track over temperature.

[14]Calculated using MIL HNBK-217; +25°C Ambient; Ground Fixed; 500 LFPM Air Flow.

*Specifications same as CAV-1040.

Specifications subject to change without notice.

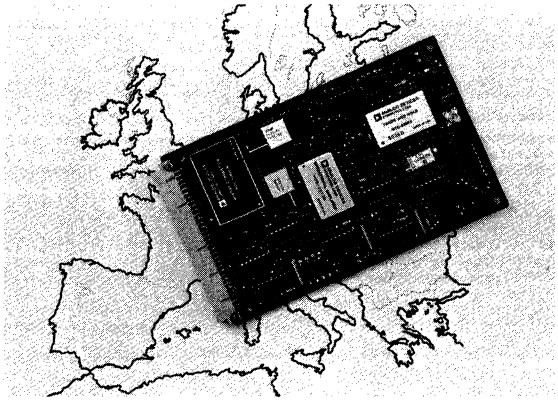
ANALOG DEVICES

12-Bit Eurocard Analog-to-Digital Converter

CAV-1202

FEATURES
12-Bit Resolution
2MHz Word Rate
Single Eurocard Size
TTL Compatible
No External Support Circuits

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Transient Analysis



GENERAL DESCRIPTION

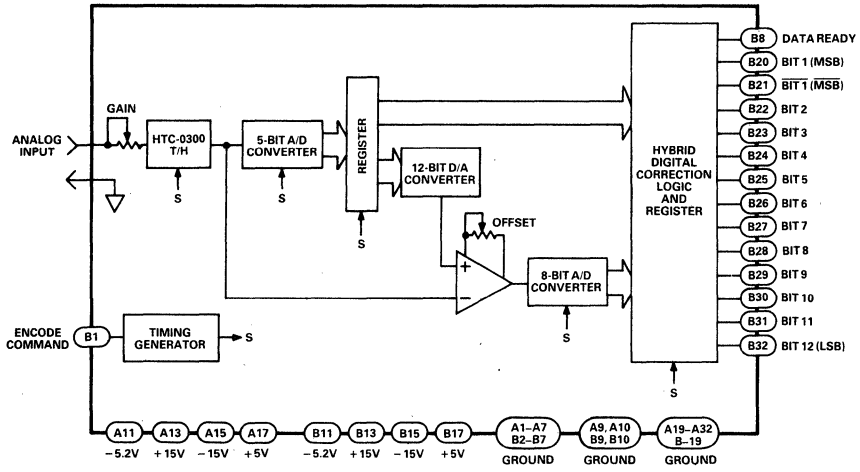
The Analog Devices Model CAV-1202 A/D Converter is a unique combination of 12-bit resolution, 2MHz word rates, and small size capable of being applied in a multitude of high-speed digitizing applications.

This remarkable, complete converter includes a track-and-hold along with encoding and timing circuits in a single "Eurocard" format. The unit requires only an encode command and external power supplies; no external support circuits are needed.

Increasingly, large scale electronic devices and systems are designed in modular form. This approach for combining complex circuits and subsystems is best served if all components of the systems share a common, standard geometry. When they do, it becomes possible to combine modules of various functions and manufacturers in one common subrack.

In Europe and many other parts of the world, Europa and double Europa-size printed circuit boards are used extensively as the basis of a standardized 19" system. The four levels of this system have evolved into a standard arrangement of dimensions which make it possible to combine components in one level and insert them into the components of the next higher level.

The design of the CAV-1202 is based on the Level 2 requirements for printed circuit board subunits and meets the standards established by DIN 41494, IEC 48D (sec) 12.



CAV-1202 Block Diagram

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	CAV-1202
RESOLUTION (FS = Full Scale)	Bits (% FS)	12 (0.024)
LSB WEIGHT	mV	1.0
ACCURACY		
(Including Linearity) @ dc	% FS ± 1/2LSB	0.0122
Monotonicity		Guaranteed Over Temperature
Diff. Nonlinearity vs. Temperature	ppm/°C (max)	2 (4)
Offset vs. Temperature	ppm/°C (max)	50 (100)
Gain vs. Temperature	ppm/°C (max)	75 (150)
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
dc to 500kHz Input	dB Below FS (min)	74 (70)
500kHz to 1MHz Input	dB Below FS (min)	67 (60)
Conversion Time[2]	ns (max)	400 (± 25) + 2 Clock Periods
Conversion Rate[3]	MHz (max)	dc to 2 (2.2)
Aperture Uncertainty (Jitter)	ps, rms, max	30
Effective Aperture Delay Time	ns (max)	− 19 (± 5)
Signal to Noise Ratio (SNR)[4]		
360kHz Input	dB (min)	66 (65)
Transient Response[5]	ns	500
Overvoltage Recovery[6]	ns	1000
Input Bandwidth (3dB)[7]	MHz	5
Two-Tone Linearity (@ Input Frequencies)[8]		
(500kHz; 540kHz)	dB Below FS	65
ANALOG INPUT		
Voltage Range[9]		
Operating	V, FS	± 2.048
Maximum Without Damage	V, max	± 4
Input Type		Bipolar
Impedance	Ω	95
Offset[10]		
Initial	mV	± 2
ENCODE COMMAND INPUT[11]		
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.4
	V	"1" = + 2.5 to + 5.0
Impedance	Ω, min	100k
Rise and Fall Times	ns, max	10
Width		
Min	ns	20
Max	70% of Encode Command Period	
Frequency	MHz	dc to 2
DIGITAL OUTPUT		
Format	Data Bits	12 Parallel, Plus $\overline{\text{MSB}}$; NRZ
	Data Ready	1; RZ
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.5
		"1" = + 2.5 to + 4.0
Drive	LS Loads	10
Time Skew	ns, max	10
Coding		Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, TTL-Compatible	V	"0" = 0 to + 0.5
		"1" = + 2.5 to + 4.0
Drive	LS Loads	10
Rise and Fall Times	ns, max	10
Duration	ns (max)	50 (± 10)
POWER REQUREMENTS[12]		
+ 15V ± 5%	mA (max)	105 (120)
− 15V ± 5%	mA (max)	70 (80)
+ 5V ± 5%	mA (max)	530 (550)
− 5.2V ± 5%	A (max)	1.0 (1.2)
Power Consumption	W (max)	10.5 (12)
TEMPERATURE RANGE		
Operating	°C	0 to + 70
Storage	°C	− 55 to + 85
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500
CONSTRUCTION		
Single Printed Circuit Card		
Including Connectors	Millimeters	167.3 × 100 × 13.13
	Inches	6.59 × 3.93 × 0.517
Board Only	Millimeters	160 × 100 × 1.57
	Inches	6.3 × 3.93 × 0.062

NOTES

[1] In-Band Harmonics expressed in terms of spurious in-band signals and related harmonics generated at 2MHz encode rate. Minimums shown guaranteed over operating temperature range of 0°C to + 70°C.

[2] Measured leading edge Encode Command to trailing edge of associated Data Ready; use trailing edge to strobe output data into external circuits.

[3] For word rates below 100kHz, consult factory.

[4] Rms signal to rms noise ratio with full scale 540kHz analog input; minimums guaranteed over operating temperature range of 0°C to + 70°C.

[5] For full-scale step input, 12-bit accuracy attained in specified time.

[6] Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage.

[7] Input bandwidth flat within 0.2dB, dc to 1MHz.

[8] Each input frequency applied at level 7dB below full scale.

[9] Standard bipolar input is adjustable ± 5% with on-card potentiometer.

[10] Adjustable ± 15mV without performance degradation.

[11] Transition from digital "0" to digital "1" initiates encoding.

[12] ± 15V must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.

PIN DESIGNATIONS

ROW A		ROW B	
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	1	ENCODE COMMAND
2	GROUND	2	GROUND
3	GROUND	3	GROUND
4	GROUND	4	GROUND
5	GROUND	5	GROUND
6	GROUND	6	GROUND
7	GROUND	7	GROUND
8	NO CONNECTION	8	DATA READY
9	GROUND	9	GROUND
10	GROUND	10	GROUND
11	− 5.2V	11	− 5.2V
12	− 5.2V SENSE	12	− 5.2V RETURN*
13	+ 15V	13	+ 15V
14	+ 15V SENSE	14	+ 15V RETURN*
15	− 15V	15	− 15V
16	− 15V SENSE	16	− 15V RETURN*
17	+ 5V	17	+ 5V
18	+ 5V SENSE	18	+ 5V RETURN*
19	GROUND	19	GROUND
20	GROUND	20	BIT 1 (MSB)
21	GROUND	21	$\overline{\text{BIT 1 (MSB)}}$
22	GROUND	22	BIT 2
23	GROUND	23	BIT 3
24	GROUND	24	BIT 4
25	GROUND	25	BIT 5
26	GROUND	26	BIT 6
27	GROUND	27	BIT 7
28	GROUND	28	BIT 8
29	GROUND	29	BIT 9
30	GROUND	30	BIT 10
31	GROUND	31	BIT 11
32	GROUND	32	BIT 12 (LSB)

***CONNECTED INTERNALLY TO GROUND PINS**
ANALOG INPUT IS SMA CONNECTOR LABELED J2

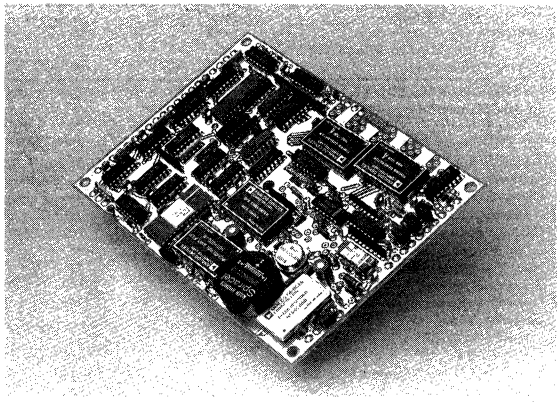
ANALOG DEVICES

12-Bit Video Analog-to-Digital Converter

CAV-1220

FEATURES
12-Bit Resolution
20MHz Word Rate
Single 35-In^2 PC Board
ECL Compatible
No External Support Circuits

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Signal Processing
Spectrum Analysis
Transient Analysis



GENERAL DESCRIPTION

The Analog Devices model CAV-1220 A/D converter is an outstanding combination of 12-bit resolution, 20MHz word rates, and small size. The unit is capable of solving a multitude of high-speed digitizing problems. Its design is based on concepts pioneered in the MOD-1020 and MOD-1205 A/D converters; and taken to an even higher level of achievement in the CAV-1210.

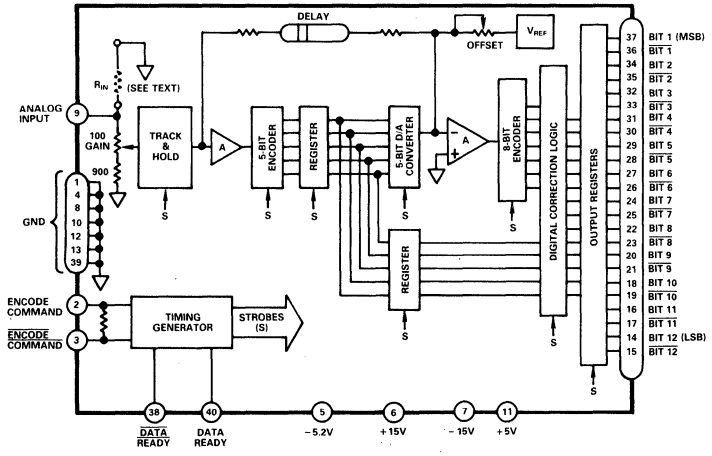
It is pin-for-pin compatible with the other units in the MOD and CAV series of A/D converters. But it *doubles* the word rate of its predecessor CAV-1210, making it possible for system designers to offer options or upgrade their high-resolution systems without new layouts.

This remarkable converter includes a track-and-hold, along with encoding and timing circuits. The CAV-1220 is an ideal choice for the designer who needs state-of-the-art performance in high-resolution, ultra-high speed A/D conversion.

For radar applications, 12-bits of resolution increase the dynamic range of the converter, making it possible to detect weaker signals than would be possible with lower resolution characteristics. The high-word rates enhance ranging resolution, thereby increasing system effectiveness.

In imaging applications, the CAV-1220 increases the contrast and/or color resolution of systems in which it is used. Its high-word rates increase spatial resolution; and this combination of high resolution and high speed can materially improve system performance.

All digital inputs and outputs are ECL compatible; optimum analog input impedance can be selected by the user. The unit requires only an encode command and external power supplies for operation. The CAV-1220 is repairable and backed by Analog Devices' limited one-year warranty.



CAV-1220 Block Diagram

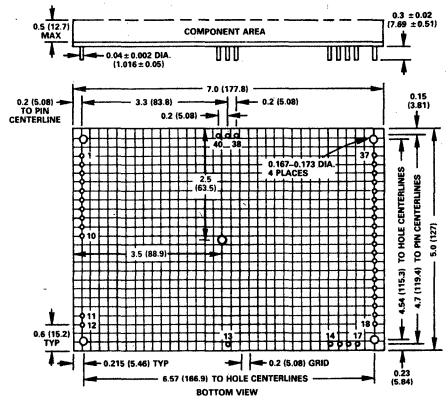
This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	CAV-1220
RESOLUTION (FS = Full Scale)	Bits (% FS)	12 (0.024)
LSB WEIGHT		
2.048V p-p FS	mV	0.5
ACCURACY		
(Including Linearity) @ dc	% FS ± 1/2LSB	0.0125
Monotonicity		Guaranteed
Nonlinearity vs. Temperature	ppm/°C (max)	10 (15)
Offset vs. Temperature	ppm/°C (max)	220 (250)
Gain Error	% FS	2
Adjustable to Zero with On-Card Potentiometer		
Gain vs. Temperature	ppm/°C, max	150
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
540kHz Input	dB Below FS, min	70
2.3MHz Input	dB Below FS, min	65
9.3MHz Input	dB Below FS, min	50
Conversion Time[2]	ns (max)	1 Clock Period + 155ns (± 10)
Conversion Rate	MHz, max	20
Aperture Uncertainty (Jitter)	ps, rms max	25
Effective Aperture Delay Time	ns (max)	2.5 (± 2.5)
Signal to Noise Ratio (SNR)[3]	dB, (min)	66 (65)
Noise Power Ratio (NPR)[4]	dB	52
Transient Response[5]	ns	100
Overvoltage Recovery[6]	ns	200
Input Bandwidth		
Small Signal, 3dB[7]	MHz	40
Large Signal, 3dB[8]	MHz	35
Two-Tone Linearity (@ Input Frequencies)[9]		
(60kHz; 62kHz)	dB Below FS	70
(2.496MHz; 2.498MHz)	dB below FS	65
(4.996MHz; 4.998MHz)	dB below FS	60
ANALOG INPUT		
Voltage Range[10]		
Operating	V, FS	± 1.024
Maximum Without Damage	V, max	± 2
Input Type		Bipolar
Impedance	Ω	1000
Offset[11]	mV	Adjustable to Zero with On-Card Potentiometer
ENCODE COMMAND INPUT[12]		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Input)	V	"1" = −0.9
Impedance	Ω, max	100
Rise and Fall Times	ns, max	5
Width		
Min	ns	10
Max	70% of Encode Command Period	
Frequency[13]	MHz	dc to 20
DIGITAL OUTPUT		
Format	Data Bits	12 Parallel; NRZ
	Data Ready and Data Ready	2; RZ
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)	V	"1" = −0.9
Drive (Line-to-Line)	Ω, min	75
Time Skew	ns, max	5
Coding		Binary (BIN); 2's Complement (2SC)
DATA READY OUTPUT		
Logic Levels, ECL-Compatible	V	"0" = −1.7
(Balanced Output)		"1" = −0.9
Drive (Line-to-Line)	Ω, min	75
Rise and Fall Time	ns, max	5
Duration	ns (max)	22 (± 3)
POWER REQUIREMENTS[14]		
+15V ± 5%	mA (max)	174 (192)
−15V ± 5%	mA (max)	157 (173)
+5V ± 5%	mA (max)	174 (192)
−5.2V ± 5%	A (max)	2.78 (3.06)
Power Consumption	W (max)	20.3 (22.3)
TEMPERATURE RANGE		
Operating	°C	0 to +70
Storage	°C	−55 to +85
Cooling Air Requirements	LFPM (Linear Feet Per Minute)	500
CONSTRUCTION		
Single Printed Circuit Card	Inches	7.0 × 5.0 × 0.5

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	40	DATA READY
2	ENCODE COMMAND	39	GROUND
3	$\overline{\text{ENCODE COMMAND}}$	38	$\overline{\text{DATA READY}}$
4	GROUND	37	BIT 1 (MSB)
5	−5.2V	36	$\overline{\text{BIT 1 (MSB)}}$
6	+15V	35	$\overline{\text{BIT 2}}$
7	−15V	34	BIT 2
8	GROUND	33	$\overline{\text{BIT 3}}$
9	ANALOG INPUT	32	BIT 3
10	GROUND	31	BIT 4
11	+5V	30	$\overline{\text{BIT 4}}$
12	GROUND	29	BIT 5
13	GROUND	28	$\overline{\text{BIT 5}}$
14	BIT 12 (LSB)	27	BIT 6
15	$\overline{\text{BIT 12 (LSB)}}$	26	$\overline{\text{BIT 6}}$
16	BIT 11	25	$\overline{\text{BIT 7}}$
17	$\overline{\text{BIT 11}}$	24	BIT 7
18	BIT 10	23	$\overline{\text{BIT 8}}$
19	$\overline{\text{BIT 10}}$	22	BIT 8
20	BIT 9	21	$\overline{\text{BIT 9}}$

NOTES

[1]In-Band Harmonics expressed in terms of spurious in-band signals and harmonics generated at 20MHz encode rate.

[2]Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits.

[3]Rms signal to rms noise ratio with full-scale 540kHz analog input.

[4]Dc to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz; and encode rate of 20MHz.

[5]For full-scale step input, 12-bit accuracy attained in specified time.

[6]Recovers to 12-bit accuracy in specified time after 2 × FS input overvoltage.

[7]With analog input 40dB below FS.

[8]With FS analog input. (Large-signal bandwidth flat within 0.2dB, dc to 10MHz).

[9]Both frequencies applied at level 7dB below full scale.

[10]Standard bipolar input is adjustable ± 5% with on-card potentiometer. Unipolar 0 to +2V input range is available on special order; consult factory for details.

[11]Adjustable ± 15mV without performance degradation.

[12]Digital "0" to digital "1" transition initiates encoding.

[13]Encode rate specified by customer. Units operated outside ± 10% of ± specified frequency (up to maximum 20MHz) must be returned to factory for recalibration. For operation at word rates below 500kHz, consult factory.

[14]± 15V must be equal and opposite within 200mV and track over temperature.

Specifications subject to change without notice.

For Applications Help, Call Computer Labs Division @ (919) 668-9511.

Low Power 14-Bit, 15-Bit & 16-Bit Sampling Analog-to-Digital Converters

DAS1157/DAS1158/DAS1159

FEATURES

- **Complete with High Accuracy Sample/Hold and A/D Converter**
- **Low Power Consumption: 650mW max, V_S = ±15V**
- **Rated Performance: −25°C to +85°C**
- **Low Nonlinearity (DAS1158 and DAS1159)**
  - **Differential: ±0.0015% FSR max**
  - **Integral: ±0.003% FSR max**
  - **Differential T.C.: ±1ppm/°C max**
- **High Throughput Rate: 18kHz min**
- **Byte-Selectable Tri-State Buffered Outputs**
- **Internal Gain & Offset Potentiometers**
- **All Hermetically-Sealed Semiconductors**
- **Improved Second Source to A/D/A/M-834 and A/D/A/M-835 Modules**

APPLICATIONS

- **Seismic Data Acquisition**
- **Portable Field Instrumentation**
- **Automated Test Equipment**
- **Process Control Data Acquisition**
- **Medical Instrumentation**

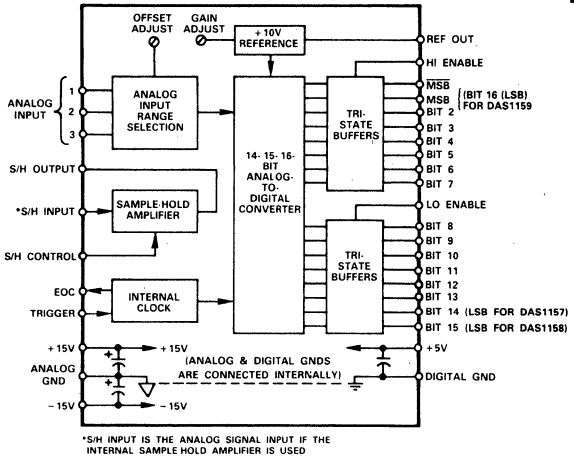


Figure 1. DAS1157/DAS1158/DAS1159 Block Diagram

GENERAL DESCRIPTION

The DAS1157/DAS1158/DAS1159 are 14-/15-/16-bit sampling analog-to-digital converters. They are ideally suited for use in portable and remote data acquisition equipment where low power consumption (650mW maximum) and wide temperature range (−25°C to +85°C rated performance) are required.

DAS1157/DAS1158/DAS1159 provide guaranteed high accuracy and high stability system performance essential to medical, analytical and process control equipment: differential nonlinearity of ±0.0015% max and integral nonlinearity of ±0.003% max (DAS1158 and DAS1159); no missing codes guaranteed; gain T.C. of ±8ppm/°C max, zero T.C. of ±80μV/°C max and differential nonlinearity T.C. of ±1ppm/°C max.

The wide dynamic range will enhance the performance of critical measurements in gas and liquid chromatography, blood analyzers, distributed data acquisition in factory automation and power generating equipment, and in automatic test equipment.

The DAS1157/DAS1158/DAS1159 make use of Analog Devices' proprietary CMOS technology to achieve low power operation, while utilizing the latest integrated circuit and thin-film components to achieve the highest level of performance and reliability. All hermetically-sealed semiconductor components are used to insure added reliability over a wide range of operating conditions.

As shown in Figure 1, each device contains a precision sample/hold amplifier, high accuracy 14-/15-/16-bit analog-to-digital converter, precision reference, CMOS tri-state output buffers (for direct 8-bit or 16-bit bus interface), user accessible gain and offset adjust potentiometers, and power supply bypass capacitors, all in a compact low profile 2″ × 4″ × 0.375″ metal case package. No additional components are required for operation.

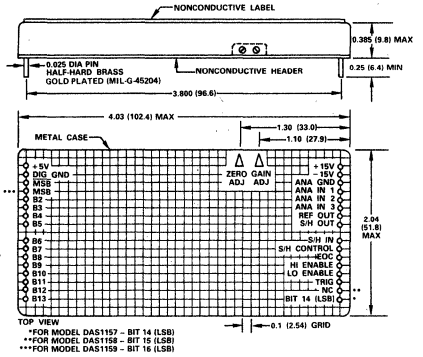
SPECIFICATIONS (typical @ +25°C, $V_S = \pm 15V$, $V_D = +5V$ unless otherwise specified)

MODEL	DAS1157	DAS1158	DAS1159
RESOLUTION	14 Bits	15 Bits	16 Bits
DYNAMIC PERFORMANCE			
Throughput Rate	18kHz min	*	*
Conversion Time	50µs max	*	*
S/H Acquisition Time	5µs max	*	*
S/H Aperture Delay	250ns	*	*
S/H Aperture Uncertainty	1ns	*	*
Feedthrough Rejection[1]	−90dB min	*	*
Droop Rate	0.05µV/µs, 0.1µV/µs max	*	*
Dielectric Absorption Error	±0.005% of Input Voltage Change	*	*
ACCURACY			
Integral Nonlinearity[2]	±0.005% FSR[3] max	±0.003% FSR[3] max	**
Differential Nonlinearity[4]	±0.003% FSR[3] max	±0.0015% FSR[3] max	**
No Missing Codes	Guaranteed	*	*
±3σ Noise (S/H plus A/D)	0.0022% p-p (75µV rms)	*	*
±3σ Noise (A/D)	0.0015% p-p (50µV rms)	*	*
STABILITY			
Differential Nonlinearity T.C.	±2ppm/°C max	±1ppm/°C max	**
Gain T.C.	±8ppm/°C max	*	*
Zero T.C.	±30µV/°C typ, ±80µV/°C max	*	*
Conversion Time T.C.	±0.05%/°C	*	*
Power Supply Sensitivity	±0.001% FSR[3]/% V_S	*	*
Warm-Up Time	Less than 1 Minute	*	*
ANALOG INPUT			
Voltage Range			
Bipolar	±5V, ±10V	*	*
Unipolar[4]	0 to +5V, 0 to +10V	*	*
ADC Input Impedance 0 to +5V	2.5kΩ	*	*
0 to +10V, ±5V	5kΩ	*	*
±10V	10kΩ	*	*
S/H Input Impedance	100MΩ‖5pF	*	*
DIGITAL INPUTS			
A/D Trigger[5]	Positive Pulse, Neg. Edge Triggered	*	*
Logic Levels	5V CMOS Compatible	*	*
S/H Control	SAMPLE = Logic 1, TTL Compatible	*	*
Low Enable, High Enable[6]	ENABLE = Logic 0, CMOS/TTL Compatible	*	*
DIGITAL OUTPUTS			
Parallel Data Outputs			
Unipolar	Binary	*	See Note 7
Bipolar	Offset Binary, 2's Complement	*	See Note 7
Output Drive	2TTL Loads	*	*
End of Conversion	Logic "1" During Conversion	*	*
Output Drive	2TTL Loads	*	*
INTERNAL REFERENCE VOLTAGE	+10V, ±0.3%	*	*
External Load Current (Rated Performance)	2mA max	*	*
POWER REQUIREMENTS			
Rated Voltages	±15V (±3%), +5V (±5%)	*	*
Operating Voltages[8,9]	±12V to ±17V, +4.75V to +5.25V	*	*
Supply Current Drain ±15V	±15mA	*	*
+5V	10mA	*	*
Total Power Consumption, $V_S = \pm 15V$	500mW typ, 650mW max	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−25°C to +85°C	*	*
Storage	−40°C to +100°C	*	*
Relative Humidity	Meets MIL-STD-202E, Method 103B	*	*
Shielding	Electrostatic (RFI) 6 Sides	*	*
	Electromagnetic (EMI) 5 Sides	*	*
SIZE	2" × 4" × 0.375" Metal Package	*	*

NOTES
*Specifications same as DAS1157
**Specifications same as DAS1158
[1]Measured in hold mode, input 20V pk-pk @ 10kHz.
[2]Worst-case summation of S/H and A/D nonlinearity errors.
[3]FSR means Full Scale Range.
[4]Differential Nonlinearity in the 0 to +5V input range is specified as ±0.003% typical for the DAS1157, DAS1158 and DAS1159.
[5]When connecting the Trigger and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy (5µs min). If the A/D converter only is used, the Trigger pulse width should be 1µs min (see Figure 3).
[6]Low Byte Enable pin connections are Bits 8 through 15; High Byte Enable pin connections are MSB, MSB or Bit 16 and Bits 2 through 7.
[7]DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only. The MSB must be inverted for binary and offset binary codes.
[8]When the S/H section is required, $-V_S$ must be at least 5 volts more negative than the most negative analog input voltage (example: $V_S = \pm 12V$ dc, therefore, maximum analog input is +10 and −7V).
[9]Recommended Power Supply: Analog Devices Model 923.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

OPERATION

For operation, the only connections necessary to the DAS1157/DAS1158/DAS1159 are the ±15V and +5V power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

Input voltage ranges are selectable via user pin programming: 0 to +5V, 0 to +10V, ±5V and ±10V. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement (DAS1157 and DAS1158). DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter. When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

Analog Voltage Input Range	Connect V_{IN} or S/H Out To	Connect Analog Common To	Connect Ref Out To
0 to +5V	ANA IN 1, ANA IN 2, ANA IN 3	Ground	NC*
0 to +10V	ANA IN 2 ANA IN 3	Ground ANA IN 1	NC*
±5V	ANA IN 1	Ground, ANA IN 3	ANA IN 2
±10V	ANA IN 3	Ground, ANA IN 1	ANA IN 2

*No Connection

Table I. Analog Input Pin Programming

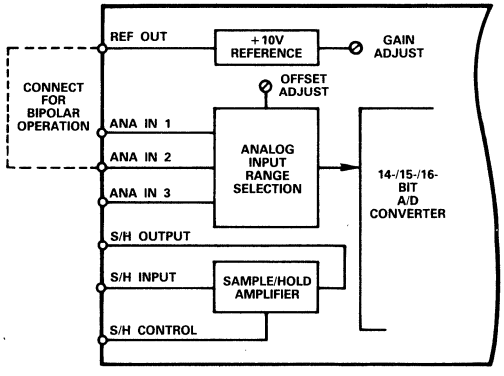


Figure 2. Analog Input Block Diagram

Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feedthrough rejection is provided for either single-channel or multichannel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

TIMING DIAGRAM

The timing diagram for the DAS1157/DAS1158/DAS1159 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of 5μs to insure accuracy. If the sample/hold amplifier is not used, the trigger pulse needs to be 1μs (minimum) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, all internal logic is reset and the A/D conversion begins. The conversion process can be retriggered at any time, including during conversion.

With this negative edge of the trigger pulse, the MSB is set high with the remaining digital outputs set to logic low state, and the end of conversion is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched high at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-/16-bit conversion taking 50μs maximum. At this time, the end of conversion line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.

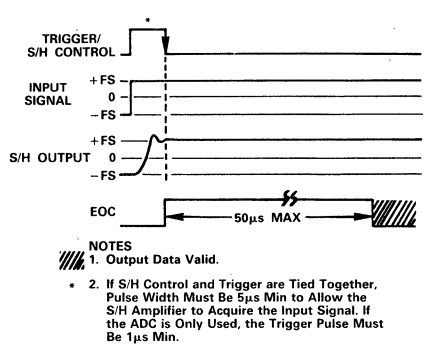


Figure 3. DAS1157/DAS1158/DAS1159 Timing Diagram

GAIN AND OFFSET ADJUSTMENT

The DAS1157/DAS1158/DAS1159 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Offset calibration is not affected by changes in gain calibration, and should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within ±1/10LSB of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a 0 to +5V unipolar range, set the input to +153μV for the DAS1157, +76μV for the DAS1158 and +38μV for the DAS1159. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001 (DAS1157/DAS1158) or from 100.....000 to 100.....001 (DAS1159).

For the ±5V bipolar range, set the input voltage precisely to +305μV for the DAS1157, +153μV for the DAS1158 and +76μV for the DAS1159. For a ±10V bipolar range, set the input voltage precisely to +610μV for the DAS1157, +305μV for the DAS1158 and +153μV for the DAS1159. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1157)/+9.99954V (DAS1158)/+9.99977V (DAS1159) for the 0 to +10V units, +4.99954V (DAS1157)/+4.99977V (DAS1158)/+4.99989V (DAS1159) for 0 to +5V units, +9.99817V (DAS1157)/+9.99909V (DAS1158)/+9.99954V (DAS1159) for ±10V units, or +4.99909V (DAS1157)/+4.99954V (DAS1158)/+4.99977V (DAS1159) for ±5V units. Note that these values are 1 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 or modified binary and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1157/DAS1158/DAS1159 INPUT/OUTPUT RELATIONSHIPS

The DAS1157/DAS1158 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while ($\overline{\text{MSB}}$) is used to obtain two's complement coding. The DAS1159 produces a modified binary coded output when configured as a unipolar device. Configured as a bipolar device it can only produce two's complement output codes. The DAS1159 uses $\overline{\text{MSB}}$ to obtain the modified binary and two's complement output codes; the DAS1159 does not have an MSB output. Table II shows the DAS1157/DAS1158/DAS1159 unipolar analog input/digital output relationships. Table III shows the DAS1157/DAS1158/DAS1159 bipolar analog input/digital output relationships.

Input Voltage – Output Code Relationships

Unipolar Input Voltages

Analog Input		Digital Output
0 to +5V Range	**0 to +10V Range**	
DAS1157		Binary Code
+4.99969V	+9.99939V	11 1111 1111 1111
+0.00000V	+0.00000V	00 0000 0000 0000
DAS1158		Binary Code
+4.99985V	+9.99969V	111 1111 1111 1111
+0.00000V	+0.00000V	000 0000 0000 0000
DAS1159		Modified Binary Code
+4.99992V	+9.99985V	0111 1111 1111 1111
+0.00000V	+0.00000V	1000 0000 0000 0000

Table II. Unipolar Input-Output Relationships

Bipolar Input Voltages

Analog Input		Digital Output	
±5V Range	**±10V Range**	**Offset Binary Code**	**Two's Complement Code**
DAS1157			
+4.99939V	+9.99878V	11 1111 1111 1111	01 1111 1111 1111
+0.00000V	+0.00000V	10 0000 0000 0000	00 0000 0000 0000
−5.00000V	−10.00000V	00 0000 0000 0000	10 0000 0000 0000
DAS1158			
+4.99969V	+9.99939V	111 1111 1111 1111	011 1111 1111 1111
+0.00000V	+0.00000V	100 0000 0000 0000	000 0000 0000 0000
−5.00000V	−10.00000V	000 0000 0000 0000	100 0000 0000 0000
DAS1159			
+4.99985V	+9.99969V		0111 1111 1111 1111
+0.00000V	+0.00000V		0000 0000 0000 0000
−5.00000V	−10.00000V		1000 0000 0000 0000

Table III. Bipolar Input-Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

No power supply decoupling is required since the DAS1157/DAS1158/DAS1159 contain high quality tantalum capacitors on each of the power supply inputs to ground.

The analog and digital grounds are internally connected in the DAS1157/DAS1158/DAS1159. But in many applications, an external connection between the digital ground pin and analog ground pin is advisable for optimum performance.

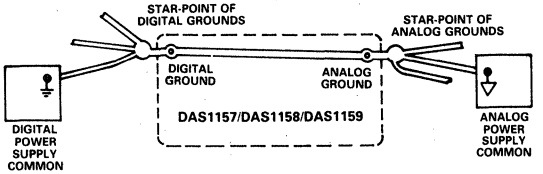


Figure 4. Typical Ground Layout for DAS1157/DAS1158/DAS1159

ANALOG DEVICES

Industrial Workstation

MACSYM 120

FEATURES

- **Ruggedized Packaging Designed to Address the Higher Temperatures, Vibration and Particulate Contaminants Found in Plant Floor Environments**
- **Color Graphics, 5 1/4" Diskette Drive, 10 MB Fixed Disk, Parallel and Serial Communication Ports, 256 KB RAM and Battery Backed-Up Clock**
- **An Industry Standard Real-Time Operating System, Concurrent CP/M-86* from Digital Research, to Serve as a Powerful Foundation for Application Software Development**
- **ADI's Measurement and Control BASIC, MACBASIC™, is Real Time, Multitasking, With Integral I/O Keywords and High Speed Graphics, to Optimize Monitoring, Test and Control Applications**
- **Supports the MACSYM® Family of Application Software Tools Including High Level Language, Menu Driven Application Software Programming Utilities and Assembly Language**
- **Compatibility with PC DOS** Files Allows Data Gathered in Real Time Using MACBASIC to be Stored in PC DOS Format and Manipulated, Analyzed and Presented by Standard Third-Party Software, Such as Lotus 1-2-3***, Wordstar†, and dBase††**
- **A Family of Measurement and Control I/O Cards that Install in the System Unit for Workstation Based Measurement and Control Configurations**
- **Integrated System Support for the Analog Devices Family of μMAC™ and MACSYM Measurement Control Units**
- **Expandable System Architecture Which Permits the Addition of Up to 640KB of Memory, Additional Communication Ports and Many Standard Products Designed for Use With the IBM PC/XT****
- **A Family of Peripherals Including Printers, Plotter, and Monitors**

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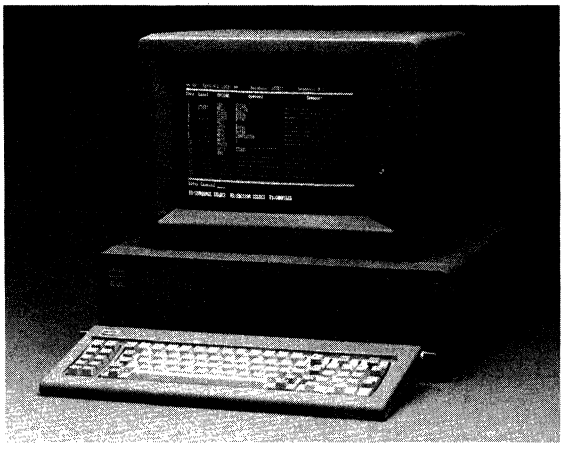
This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.



OVERVIEW

The MACSYM 120 is a version of the IBM PC/XT manufactured by IBM for Analog Devices and designed for use in plant floor environments. The system hardware supports all of the functions of Analog Devices hardware and software products as well as the IBM PC/XT. The MACSYM 121 is comprised of the standard MACSYM 120 system unit configured to support the MACSYM 200 family of products.

The base MACSYM 120 consists of a system unit and a keyboard. The system unit contains a 10MB fixed disk drive, dual sided 5 1/4" diskette drive, color/graphics monitor card, a multifunction combination card, 256KB of RAM and four system expansion slots. A door over the disk/diskette drive area protects the drives from particulate contaminants. A cooling fan with removable filter protects the system internals from suspended and settleable particulates. A retainer bar inside the system unit secures each of the installed cards against vibration. The multifunction combination card provides an asynchronous communication port, a parallel printer port, battery backed-up calendar-clock and a thermal sensor interface to monitor temperature inside the system unit.

The keyboard attaches to the rear of the system unit via a coiled cable. The keypad area is comprised of three sections: typewriter keys, numeric/editing keypad, and programmable function keys.

Various options are available for use with the base system such as a color monitor, more system memory, serial/parallel communication ports, peripheral devices, measurement and control I/O cards and subsystems.

THE STANDARD SYSTEM UNIT

The standard MACSYM 120 system unit has the following features:

- System Board With Intel 8088 Microprocessor and 8087 Math Coprocessor
- Power Supply
- 83 Key Sealed Membrane Keyboard With Typewriter Keyboard, Numeric/Editing Keypad, Buffered Input and Ten Function Keys
- 10 MB Fixed Disk and Adapter Card
- 5 1/4" Floppy Diskette Drive and Adapter Card
- Color/Graphics Display Adapter Card
- Combination Adapter Card With One Asynchronous Communication Port, One Parallel Interface Port, Battery Backed-Up Clock and Thermal Warning System
- Four System Expansion Slots for Option Boards such as Additional Memory, Communication Ports or Measurement and Control IO

The Macsym 120 is supported by two levels of diagnostics. A power-on self test is executed to verify that base system elements are working properly. It will report on problems that could prevent the system from booting. Additionally, each system is shipped with a diagnostic diskette. These tests can be used to verify proper operation of the system board, keyboard, memory, adaptor and option cards. Each of these units is customer replaceable.

System Board

The heart of the system unit is the System Board. It consists of five functional areas: the Microprocessor Subsystem and its support elements; the Read-Only-Memory (ROM) subsystem; the Random Access Memory (RAM) subsystem; I/O bus and adapter card interface circuitry. Eight IBM PC/XT compatible 62-pin card edge sockets are mounted on the board for system I/O. The I/O signals are bussed across these eight slots for use by the standard adapter cards and optional expansion products.

The MACSYM 120's processing power is based on the Intel 8088 Microprocessor. It is an 8-bit external bus version of Intel's 16-bit 8086 Microprocessor, and is software compatible with the 8086. Thus the 8088 supports 16-bit operations.

The 8088 operates in maximum mode so that an Intel 8087 math coprocessor can be used. The coprocessor enables the system to perform high speed arithmetic, logarithmic functions, and trigonometric operations with exceptional speed and accuracy. The coprocessor works in parallel with the 8088. The parallel operation allows the coprocessor to do mathematical calculations while the 8088 microprocessor continues to do other functions. This performance is important when performing real-time analysis or calculating control algorithms.

An eight position dual-in-line switch mounted on the system board provides system programs with information about installed options via the operating system.

The System Board also contains the circuitry for the serial interface to the keyboard. These circuits generate an interrupt to the system unit's 8088 microprocessor when a keyboard scan complete code is received. The interface logic can also request execution of a diagnostic test in the keyboard.

Power Supply

The power supply is an integral part of the system unit chassis. It supplies the power and power OK reset signal necessary for the operation of the system board, installed options, and the keyboard. It also provides two separate connectors for power to the 5 1/4" diskette drive and the 10MB fixed disk drive. It is designed for continuous operation at 130 watts and has a fused 120V ac input. The power supply is designed to operate in plant power environments. It provides system unit power through power line transients and input fluctuations from 104V ac to 127V ac, 57Hz to 63Hz. When the power supply is turned on after it has been off for 5 seconds, it generates a power good system reset signal that indicates adequate power is available for processing.

Keyboard

The keyboard has a permanently attached cable that connects to a DIN connector at the rear of the system unit. The keyboard assembly incorporates a microprocessor to perform the keyboard scan function and a power-on self test. It is a typewriter styled keyboard with full screen editing and cursor control keys. There are ten user definable function keys and a numeric keypad. The keypad assembly can be adjusted to a 5 or 15 degree tilt for operator comfort.

Fixed Disk Drive

The 10MB Fixed Disk drive is a random access storage device that uses two non-removable 5 1/4" disks for storage. It interfaces to the system board via the fixed disk drive adapter which is factory installed in one long slot on the system board. The total formatted capacity is 10M bytes (17 sectors per track with 512 bytes per sector and a total of 1224 tracks).

An impact-resistant enclosure provides mechanical and contamination protection for the heads, actuator and disks. A self contained air recirculating system, which consists of an internal filter and a breather filter, maintains a clean air environment. Thermal isolation of the stepper and spindle motor assemblies from the disk enclosure results in a very low temperature rise within the enclosure. This isolation provides a greater off track margin and the ability to perform read and write operations immediately after power-up with no thermal stabilization delay.

Floppy Diskette Drive

The 5 1/4" Diskette Drive utilizes double-sided double density soft-sectored diskettes with 40 tracks per side. The diskette drive itself is a self-contained unit consisting of a spindle drive system, a head-positioning system and a read/write/erase system. The diskette drive uses Modified Frequency Modulation (MFM) to read and write digital data. It interfaces to the system board via the diskette drive adapter card which is factory installed in one of the long system slots located on the system board.

Color/Graphics Display Adapter

The Color/Graphics Display Adapter Card is designed to interface the system unit with the MACSYM 120's Industrial Color Display. It is capable of operating with monochrome or color displays and provides three video interfaces: a composite-video port, a direct drive port (RGB), and a connection interface for driving a user supplied RF modulator. The adapter has two basic modes of operation: alpha-numeric (A/N) and all-points-addressable (APA) graphics.

In the A/N mode, the display is operated under CCP/M-86 in an 80 column by 25 row format for use with high resolution monitors.

In the APA mode, there are two resolutions available: a medium resolution color graphics mode (320 × 200) and a high resolution monochrome graphics mode (640 × 200). In the medium-resolution mode each pixel takes on one of four colors. The background color is fixed as black. The remaining three colors come from one of the two program selectable color palletes.

The color/graphics adapter card is factory installed in a long slot on the system board. The direct drive video port is a 9-pin, D shell female connector. The composite video port is a standard female phono jack.

Combination Adapter Card

The Combination Adapter Card is factory installed in a short system slot. It has the following four functions:

- Serial Asynchronous Communication
- Parallel Printer Port
- Battery Backed-Up Real Time Clock
- Thermal Warning System

The Serial Asynchronous Communication port is fully programmable and supports asynchronous communications. The hardware will add and remove start, stop and parity bits. A programmable baud rate generator settable by a CCP/M-86 operating system utility, allows operation from 50 to 9600 baud. The operating system also controls transmit, receive, modem control, and error conditions via interrupts. Diagnostic capabilities accessible from assembly language provide loop-back functions of transmit/receive and input/output signals. The following modem control signals are supported by the implementation of the operating system: CTS, RTS, DSR and DTR.

The parallel printer port is specifically designed to attach printers with a parallel port interface, but it can also be used as a general output port for any device that matches its capabilities.

When this port is used to attach a printer, data or printer commands are loaded into an 8-bit latched output port, and the strobe line is activated writing data to the printer. The operating system automatically checks printer status indicating when the next character can be written.

The thermal warning system monitors internal system temperature as a means of notifying the operator of a clogged filter, failed fan or excessive operating temperature. The operating system automatically displays the warning condition on line 25 of the system monitor. A status bit representing the same information is also accessible from a user program on a polled basis.

The real-time clock is a 24-hour battery backed-up calendar clock. It is also supported by the system software which can be set to read day, date and time.

Below is a system block diagram of the MACSYM 120 Industrial Workstation System Unit.

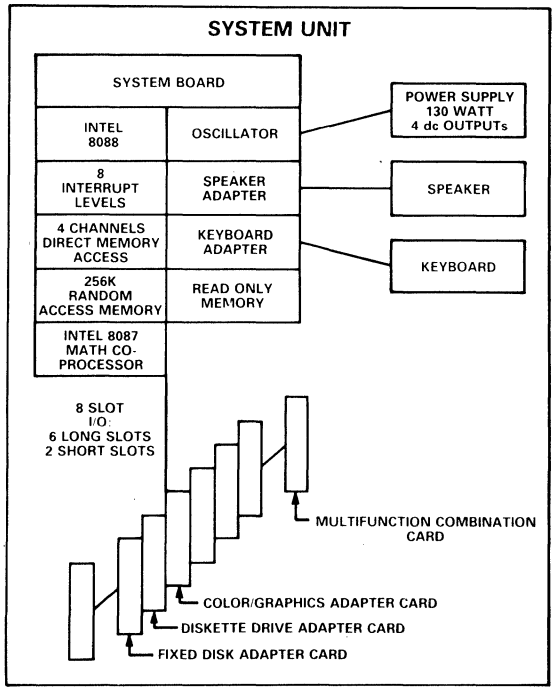


Figure 1.

SYSTEM EXPANSION OPTIONS

The MACSYM 120 Workstation can be expanded by adding a number of options. A family of peripherals including printers, a color plotter and monitor are available. Installation of the Series 120 measurement and control I/O products makes the MACSYM 120 a workstation based measurement and control system. System I/O options such as memory and communications hardware may also be installed based on your application requirements.

The MACSYM 120 can also be expanded to work with the μMAC and MACSYM family of I/O interface and programmable measurement and control units. The MACSYM 121 configuration of the workstation incorporates support for high speed communications to the MACSYM 200 family of measurement and control units. MCComm products allow the MACSYM 120 to be utilized with all of the Analog Devices measurement and control unit products as well as communicate easily with other popular computers.

SYSTEM OPTION RESOURCE REQUIREMENTS

Product	Card Size	DMA Channel Req'd	Interrupt Req'd	Comments
MIO120: analog and digital I/O	Long	Optional	Optional	Interrupt and DMA required to utilize SCAN, or COLLECT statements
AOT120: analog output	Long	NO	NO	
DIO120 digital I/O	Short	NO	Optional	Interrupt required if using ACT ON EVENT statement.
MEM120-010, 1, 2: RAM exp.	Short	NO	NO	
MEM120-020,1,2: RAM and comm. exp.	Long	NO	YES	Serial port must use one interrupt; parallel port does not use interrupt.

Table III.

MACSYM 120 TECHNICAL DATA

Standard System Unit

- Intel 8088 microprocessor, 4.77MHz clock speed
- Intel 8087 math coprocessor
- 256KB RAM with memory parity checking
- 250ns memory access time, 410ns memory cycle time
- Operating system:
  - Digital Research CCP/M-86 with additions to support Analog Devices measurement and control I/O products and graphics
  - Support for 4 virtual consoles with windows.
  - Occupies 145KB of RAM
  - File Compatibility with PC DOS
- Measurement and control language:
  - Analog Devices MACBASIC
  - Real time
  - Multitasking
  - Integral I/O keywords
  - High speed, high resolution graphics
- 130 watt power supply
- Cooling fan with replaceable filter
- Dual sided 5 1/4" diskette drive and adapter card, 48tpi, 40 tracks per side, 360K bytes formatted storage, 6 millisecond track-to-track access.
- 10MB Winchester disk drive and adapter card with 11-bit burst error detection and correction in the form of 32-bit error checking and correction.
- Combination adapter card with thermal sensor input, 10-year battery-backed calendar clock, serial asynchronous communication port with RS232C/20mA current loop, and parallel interface port
- Color/graphics display adapter
  - Medium Resolution: 320 × 200, 4 colors
  - High Resolution: 640 × 200, monochrome
  - Text Mode: 80 columns × 25 rows
- System unit dimensions:
  - Width 19.5" (496mm)
  - Depth 17.9" (455mm)
  - Height 6" (152mm)
- System unit weight:
  Approximately 39 pounds (17.7kg) without keyboard
- Electrical:
  - AC operating voltages: 104 minimum to 127 maximum, 57Hz to 63Hz
  - Transients: ±2500 volts maximum with 16 microsecond nominal pulse width
- Temperature:
  - Operating: 39.2 degrees to 115 degrees F (4 degrees to 46.1 degrees C)
  - Storage: 39.2 degrees to 125 degrees F (4 degrees to 51.7 degrees C)
- Particulate contaminants:
  - Suspended particulates: 500 micrograms per cubic meter
  - Benzene soluble organics: 30 micrograms per cubic meter
  - Settleable particulates: 1500 micrograms per square centimeter
- Shock:
  - 0.5G at 10 millisecond interval
- Vibration:
  - 5Hz to 17Hz at 0.005 inches double amplitude displacement
  - 17Hz to 200Hz at 0.07G peak
  - 200Hz to 500Hz at 0.036G peak
- Keyboard: 83 keys, 182.88cm (6 ft.) coiled cable, 5 and 15 degree tilt positions, standard typewriter keyboard layout, 10 function keys, 15 key numeric/screen editing keypad, 6.5 pounds (2.9kg)

MACSYM 120 WORKSTATION PERIPHERAL OPTIONS

- 13" diagonal, 16 color industrial display:
  - Protective screen cover
  - Direct drive connects to color/graphics monitor adapter card
  - Cooling fan with replaceable filter
  - Height: 297mm (11.7 in)
  - Length: 392mm (15.4 in)
  - Depth: 407mm (15.6 in)
  - Weight: 12.3kg (27 lb)
  - Heat output: 240 BTU/HR
  - Power cable: 1.83m (6 ft.)
  - Signal cable: 1.5m (5 ft.)
- 80/132 column dot matrix printers
- Interactive X-Y plotter, 8 colors

Measurement and Control I/O Options (see the Series 120 Data Sheet for detailed specifications)

- MIO120: Multifunction measurement and control I/O
  - 32 single ended/16 differential 12-bit analog inputs
  - 2, 12-bit analog outputs
  - 8 digital inputs, 8 digital outputs
  - Installs in one long slot
- AOT120: Analog output card
  - 4 or 8 analog output channels
  - 12-bit resolution
  - 4 selectable output ranges
  - Installs in one long slot
- DIO120: digital input and output card
  - 24 channels selectable in 8 channel groups as input or output
  - Integral change of state detection for activating a system interrupt
  - Installs in a long or short slot

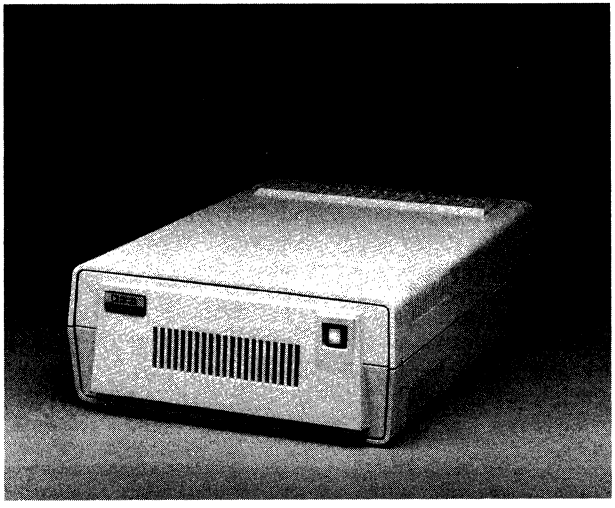
System I/O Options

- MEM120-010,011,012: Memory expansion card for expanding system memory to the 640KB maximum
  - Adds up to 384KB to the 256KB in the standard system unit
  - Installs in a short or long slot
- MEM120-020,021,022: Multifunction memory/communications expansion card
  - Adds up to 384KB to the 256KB in the standard system unit
  - One parallel printer port
  - One serial asynchronous communications port, RS-232-C; same features as the Combination Adapter Card
  - Installs in one long slot

ANALOG DEVICES

Programmable Measurement and Control Unit

MACSYM 250



4

FEATURES

Used with a MACSYM® Workstation, or IBM PC
16 Slots for ADIO Cards for up to:
- **512 Single Ended Analog Inputs, or**
- **256 Differential Analog Inputs, or**
- **256 Digital I/O Points, or**
- **64 Analog Outputs**

Versatile Data Acquisition:
- **33,000 12-Bit Samples/Second COLLECT**
- **7,000 Samples/Second SCAN**
- **Noise Immune 16-bit Sampling**
- **220 Samples/Second from Multiple Relay Cards**
- **AVeraGe and Frequency INput Commands**

MACBASIC™ – A Real-Time Multitasking BASIC which is both Interactive and Compiled for Ease of Program Development and Fast Execution
Local Limit Checking, Data Analysis and Statistical Report Generation to Offload Workstation Processor
Local Process Control Without Additional Host Communication
8088/8087 Math Co-Processor Architecture for High Speed Floating Point Operations
Up to 512K Bytes RAM with Parity Checking
Communication to Workstation at 307K baud
RS-232 Port for Local Printer, Terminal, or Local Operator Terminal
Watchdog Timer to Monitor Unit Operation

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

GENERAL DESCRIPTION

The MACSYM 250 is a Programmable Measurement and Control Unit used with the MACSYM 121 or 150 Workstations or the IBM Personal Computer with an ADI Compatibility Kit. It provides 16 slots for ADIO (Analog/Digital Input/Output) cards. The MACSYM 250 features 12-bit high speed or 16-bit high resolution data acquisition, automatic self-calibration, and up to 512K bytes of RAM.

MACBASIC, a compiled, real-time multitasking BASIC, is the programming language for both the MACSYM 250 and Workstation. Thus the MACSYM 250 can implement measurement and control strategies locally. Used with a Workstation, this provides distributed processing. The MACSYM 250 acquires data, checks limits, analyzes data, develops control outputs, generates statistics, and reports results to the workstation. The workstation provides operator interface, manages disk storage, generates screen graphics, and runs other programs under Concurrent CP/M-86*.

The MACSYM 250 is optimized for measurement and control. For high speed floating point operations, it has 8088/8087 microprocessor/math co-processor architecture. Its RAM supports the multitasking scheduler, MACBASIC, the application program, and variable data space.

Real-world data is acquired and control outputs are sent through ADIO cards which are plugged into the 16 slots of the MACSYM 250. The ADIO bus carries signals to and from the cards and the I/O Interface. The I/O Interface converts analog data to

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MACBASIC is a trademark of Analog Devices, Inc.
***CP/M-86 is a registered trademark of Digital Research, Inc.**

SPECIFICATIONS (Typical at 25°C unless otherwise specified)

COMPUTER	
CPU	8088/8087 Processor/Math Co-Processor
Clock Rate	5MHz
RAM Memory	256K Byte Standard (512K Byte Optional)
System Memory Requirement	110K Bytes
Diagnostic and Boot-Up PROM	16K Byte (Not User Accessible)
Communications	
Port 0	RS-422 Serial Synchronous at 307.2K Baud to Work Station (Up to 3.8 Volts Common-Mode Differential)
Port 1	RS-232 Serial Asynchronous 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 or 19,200 Baud (Switch Selectable)
Local Operator Terminal Power	5 Volts at 500mA
Watchdog Timeout Period	3 Seconds
A/D CONVERTER FUNCTION	
12-Bit Successive Approximation Mode	
Accuracy[1]	±0.024%
Resolution	0.024%
Speed	33,000 Samples/Sec Burst Mode
16-Bit Resolution Integrating Mode	
Accuracy[1]	±0.024%
Resolution	0.0015%
Normal Mode Rejection	50dB additive to ADIO card
Speed	16.6ms/Conversion (60Hz Systems) 20.0ms/Conversion (50Hz Systems)
CALIBRATION	Self-Calibration Minimizes Errors Over Changing Environmental Conditions
TEMPERATURE COEFFICIENTS[1,2]	
Offset TC	±15μV/°C
Gain TC	±3ppm/°C

PHYSICAL SPECIFICATIONS	
Size	8.0H × 17.5W × 25.5D Inch (20H × 45W × 65D CM)
Weight	50 lbs. (23kg) with 16
Shipping Weight	60 lbs. (27kg) ADIO cards
I/O Slots	16-Slots for ADIO Cards
Environmental	
Operating Temperature	32°F-122°F; 0-50°C
Relative Humidity	5-95% Noncondensing
POWER AVAILABLE FOR ADIO CARDS	
+5 Volts	10 Amps
+15Volts	2.4 Amps
−15 Volts	2.4 Amps
INPUT POWER	
Voltage	100/120 or 220/240 VAC
Voltage Tolerance	−20% to +10%
Frequency	47Hz to 63Hz
Power Consumption	150 Watts without ADIO 400 Watts max

NOTES
[1]Does not include ADIO Card Specifications.
[2]Assumes periodic auto calibration.
Specifications subject to change without notice.

digital form, delivers data to and receives it from the microprocessor bus. Acquired data may be used immediately in a running program, or accumulated for future use.

High-speed data and program communication is provided to MACSYM Workstations over a 307k baud link. A second communication port is available for a local terminal, printer, or other RS-232 device.

MACBASIC

Both the workstation and MACSYM 250 are programmed in MACBASIC. Each has the capability to run up to 18 tasks concurrently. As a result, the MACSYM 250 can effectively execute many tasks at once, providing real-time measurement and control.

The MACBASIC commands implemented in the MACSYM 250 support ADIO activity, computation, and communication. Since mass storage, screen graphics, and IEEE-488 communications are performed through the Workstation, those supporting MACBASIC commands appear only there. The MACSYM 250 can access a disk file and display tabular data on the screen through a cooperating Workstation program.

PROGRAM SEGMENT EXAMPLE

A small segment from a MACBASIC application program illustrates the distributed control achieved with a Workstation and MACSYM 250. This program scans 256 real world points and compares them to a pre-set limit value. Values higher than the limit will be sent to the Workstation for future processing, minimizing communication and freeing the Workstation for higher level functions.

MACSYM 250 PROGRAM	DESCRIPTION
10 TASK 3,100 ACT 3	
100 OPENW: 2" $BOX:0,5"	Prepare to send data through software channel 2 to the workstation (box 0), active task 5
110 SCAN (SPEC' (1), 256) INTO DATA (1)	Acquire data from all 256 Analog Input points
120 FOR INDEX = 1 TO 256	For all points
130 IF DATA (INDEX) ≤ LIMIT GO TO 150	Check to see if their value is greater than a limit, if so, report to Workstation
140 PRINT: 2 INDEX, DATA (INDEX)	
150 NEXT INDEX	
160 CLOSE:2	Complete this segment

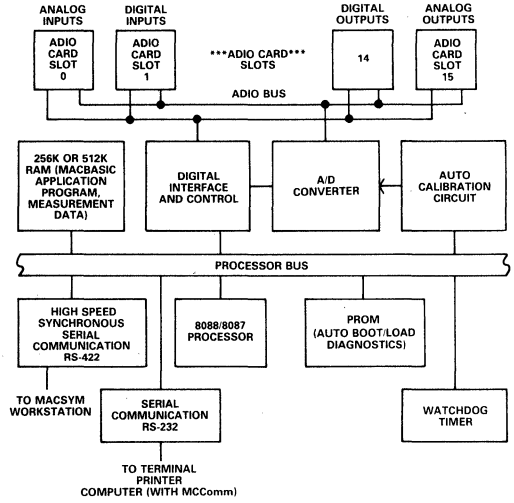
WORKSTATION PROGRAM	DESCRIPTION
30 TASK 5, 510 ACT 5	
510 OPENR: 4" $BOX: 1,3"	Prepare to receive data through software channel 4 from Box 1, task 3
520 INPUT: 4 SAMPLE, VALUE	The task looks for data from the MACSYM 250. If there is none, it suspends.
530 GOSUB 1000 REM EXCEPTION HANDLER	Processes and develops displays
540 GO TO 520	Return to await more data

Enhancements to this program are easily added to check both high and low limits. Each point can be checked against limits specific to that point by defining arrays of limits.

MULTITASKING SCHEDULER

The MACSYM 250 has an executive which performs the operating system functions required by the MACSYM 250, while remaining transparent to the user. It keeps track of all the things to be done, and arranges for them to happen in an orderly fashion. This multitasking scheduler has been optimized for efficiency in the MACSYM 250 environment. It activates and suspends MACBASIC tasks based upon the function performed by the task, as well as other tasks waiting to be processed. It also supervises input/output functions.

MACSYM 250 BLOCK DIAGRAM



ADIO CARDS

Real-world signal interfacing is accomplished through the ADIO family of over 30 (Analog/Digital Input/Output) cards. They provide all the signal conditioning necessary for connection directly to voltages, currents, frequencies, thermocouples, strain gages, flow meters, relays, tachometers, valves, alarms, controllers, and other devices. Calibrated excitations, input protection, isolation, multiplexing, amplification, and other required preconditioning are supplied by the ADIO cards. Sensors and actuators are connected to ADIO cards with convenient screw terminals on a separate panel.

The ADIO library includes solid state and relay multiplexer cards for analog inputs. Cards specifically for thermocouples, RTDs and strain gages are also available. Analog output cards have both voltage and current loop drive capability. Digital inputs and outputs are available on several cards, with either solid state or relay switching. Other cards include a calendar/clock, frequency measurement, pulse counting, and generation of priority interrupts. The dual loop PID control card functions independently of other system activity. Refer to the ADIO data sheets for additional details.

MACSYM 250 ARCHITECTURE

Tracing a typical analog input signal flow into the MACSYM 250 is one way to gain an appreciation for the strength of its design. An ADIO card is chosen for the particular measurement or control activity. Then the signal is multiplexed onto the ADIO bus. Shielding on the ADIO bus separates these signals from high speed digital signals and other noise sources within the MACSYM 250. The ADIO bus carries these signals to the central analog I/O Interface of the CPU board. Here a multiplexer selects the input signal from the card of interest. Final amplification through a programmable gain amplifier scales the signal into a ±10 volt range. Then a sample and hold amplifier captures the signal for conversion by the analog to digital converter. This digital representation is stored in memory.

The 8088 and 8087 work together to achieve rapid program execution with high accuracy. Program logic steps are executed by the 8088, while arithmetic (+, −, /, ×) and transcendental operations (sine, cosine, log) are performed by the 8087. The computational power available is illustrated by the rapid execution speed of some representative MACBASIC operations. A 32-bit floating point multiply or divide (X = A * B or X = A/B) is completed in less than 290 microseconds.

DUAL MODE A/D CONVERTER

Two modes of analog-to-digital conversion are selectable under program control in the MACSYM 250. High speed 12-bit conversions use the successive approximation technique. In addition, a statistical integration process may be used with the AIN command to achieve 16-bit resolution. High levels of noise immunity, and line frequency normal mode rejection result from this process.

AUTO CALIBRATION

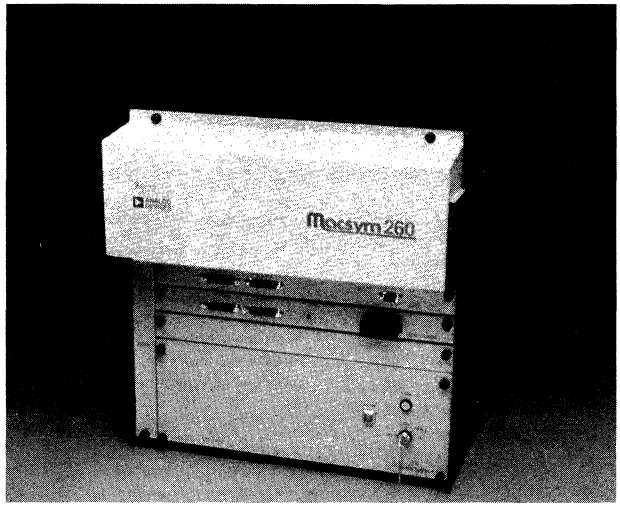
The MACSYM 250 automatically calibrates its data acquisition section when it is powered up, and after an initial temperature stablization period of 15 minutes. Subsequent calibrations may be initiated at any time, under program control. Accurate system performance over long periods of time and changing environmental conditions is ensured by the calibration process employed in the MACSYM 250.

Calibration is accomplished by applying known, accurate reference voltages to the A/D converter's analog input. A/D conversions are performed, and each result is compared with the expected value for that particular input. Automatic adjustments are made until the A/D conversion results match expected values. When this occurs, calibration is complete.

ANALOG DEVICES

Programmable Measurement and Control Unit

MACSYM 260



FEATURES

16-Slots for ADIO Cards–for Up to
512 Single Ended Analog Inputs or
256 Differential Analog Inputs or
256 Digital I/O Points or
64 Analog Outputs
Versatile, High Performance Data Acquisition
33,000 12-Bit Samples Per Second (Single Channel Burst)
7000 Samples per Second (Multiple Channels)
Noise Immune 16-Bit Sampling
Up to 220 Samples/Second from Multiple Relay Cards
SCAN, COLLECT, AVG and Frequency Input Commands
MACBASIC™ – A Real-Time Multitasking BASIC Which is Both Interactive and Compiled for Ease of Program Development and Fast Execution
8088/8087 Math Co-Processor Architecture for High Speed Floating Point Operations
Local Limit Checking, Data Analysis, and Statistical Report Generation to Offload Workstation
Program Development with a MACSYM® Workstation or Uses Programs Developed on a MACSYM 250
Up to 512K Bytes RAM with Parity Checking, for Large Data Handling Capacity
Runs Programs from PROM for Nonvolatile Program Storage and Automatic Operation on Power Up
Up to 384K Bytes PROM for System and Application Programs
Rugged Metal Construction for Industrial Environments
60°C Operating Temperature
All Assemblies Accessible from the Front
Diagnostic Indicator Lights
Stand-Alone or Distributed Control
Three RS-232 Ports for Local Printers, Terminals, Communication with Non-ADI Computer, or Other Control Units
Isolated 20mA Communications on 2 Ports
System Monitor to Verify Unit Operation
Monitors Internal Supply Voltages and Temperature to Facilitate Maintenance
Automatic Power-Up Diagnostics
Keylock Security

This six-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

GENERAL DESCRIPTION

The MACSYM 260 is an industrial Programmable Measurement and Control Unit which may be used as a stand-alone controller; with a MACSYM Workstation; IBM* Personal Computer with an ADI compatibility kit; or any popular computer. It provides 16 slots for ADIO (Analog/Digital Input/Output) cards. These accommodate up to 512 single ended or 256 differential analog inputs; or 256 digital I/O points; or up to 64 analog outputs. The MACSYM 260 features 12-bit high speed or 16-bit high resolution data acquisition, automatic self-calibration, up to 384K of PROM, and up to 512K bytes of RAM.

MACBASIC is a trademark of Analog Devices, Inc.
MACSYM is a registered trademark of Analog Devices, Inc.
***IBM is a trademark of International Business Machines Corporation.**

SPECIFICATIONS (Typical at 25°C unless otherwise specified)

COMPUTER	
CPU	8088/8087 Processor/Math Co-Processor
Clock Rate	5MHz
RAM Memory	256K Byte Standard (512K Byte Optional)
PROM	12 Sockets for 32K × 8 Chips (384K) or 16K × 8 Chips (192K)
System Memory Requirement	150K Bytes
Diagnostic and Boot-Up PROM	16K Bytes (Not User Accessible)
Communications	
Port 0	RS-422 at 307.2K Baud to Workstation (Nonisolated, for Program Development only)
Port 1	RS-232 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19,200 Baud (Switch Selectable)
Local Operator Terminal Power	5 Volts at 500mA min
Port 2 & 3	RS-232 Serial Asynchronous ASCII or Isolated 20mA Current Loop 150, 300, 600, 1200, 2400, 4800, 9600 or 19,200 Baud (Switch Selectable)
Watchdog Timeout Period	3 Seconds
A/D CONVERTER FUNCTION	
12-Bit Successive Approximation Mode	
Accuracy[1]	±0.024%
Resolution	0.024%
Speed	33,000 Samples/Sec Burst Mode
16-Bit Resolution Integrating Mode	
Accuracy[1]	±0.024%
Resolution	0.0015%
Normal Mode Rejection	50dB Additive to ADIO Card
Speed	16.6 µs Conversion (60Hz Systems) 20.0µs Conversion (50Hz Systems)
CALIBRATION	Self-Calibration Minimizes Errors Over Changing Environmental Conditions
TEMPERATURE COEFFICIENTS[1,2]	
Offset TC	±15µV/°C
Gain TC	3ppm/°C

PHYSICAL SPECIFICATIONS	
Size	20H × 18W × 16D Inch 51H × 45W × 41D CM
Weight	65 lbs. (30kg) with 16
Shipping Weight	80 lbs. (36kg) ADIO CARDS
I/O Slots	16-Slots for ADIO Cards
ENVIRONMENTAL	
Operating Temperature	0-60°C 32°F-140°F
Relative Humidity	5%-95% Noncondensing
INPUT POWER	
Voltage	100/120 or 220/240V ac
Voltage Tolerance	−20% to +10%
Frequency	47Hz to 63Hz
Power Consumption	150 Watts without ADIO 450 Watts max

NOTES
[1]Does not include ADIO Card Specifications.
[2]Assumes periodic auto calibration.
Specifications subject to change without notice.

Distributed processing can be implemented with another computer. Either RS-232 or isolated 20mA current loop communication can be used. Protocols may be defined by MCComm, or custom communications protocols may be developed.

In a typical distributed application, the MACSYM 260 acquires data, checks limits, analyzes data, develops control outputs, generates statistics, and may report results to another computer. That computer manages mass storage, and may send supervisory control messages, or parameter changes to the MACSYM 260. Operator interface is accomplished through a Workstation, video display terminal, or other local terminal device.

In stand-alone control applications, MACSYM 260 programs are stored in nonvolatile PROM. Operators may interact with the unit through a local terminal. Reports can be sent to a printer through a local serial port.

The MACSYM 260 is optimized for measurement and control. For high speed floating point math operations it has 8088/8087 microprocessor/math coprocessor architecture. Up to 512K bytes of RAM is available. The multitasking scheduler and MACBASIC require about 150K bytes. Alternatively, the scheduler and MACBASIC can be programmed in PROM, for nonvolatile storage. For stand-alone operation, a debugged application program can also be programmed into PROM and installed in the MACSYM 260. This frees over 100K bytes of RAM for additional variable data space.

Real-world data is acquired, and control outputs are sent through ADIO cards which are plugged into the 16 slots of the MACSYM 260. The ADIO bus carries signals to and from the cards and the I/O Interface. This I/O Interface converts analog data to digital form, and passes data to and from the processor bus. Acquired data can be used immediately in a running program, or accumulated for future use.

Communication for program development is provided to and from Workstations over a 307K baud RS-422 link. Three additional communication ports for local printers, terminals, and communication to another computer are included on the MACSYM 260. Both RS-232 and 20mA current loop capability are provided.

MACBASIC

The MACSYM 260 is programmed in MACBASIC. It has the capability to run up to 18 tasks concurrently. As a result, the MACSYM 260 can effectively execute many tasks at once, providing real time measurement and control.

The subset of MACBASIC which is implemented in the MACSYM 260 includes commands for ADIO activity, computation and communication, such as ACTIVATE ON EVENT, ALERT, SUSPEND, CHATR, POLY, and OPEN for Read or Write. MACBASIC in the MACSYM 260 works together with MACBASIC on the Workstation, where screen graphics and mass storage commands appear. Software developed for the MACSYM 250 can be executed on the MACSYM 260. The two units use the same commands, except that directed I/O to ports 2 and 3, and return of a high internal temperature indication are not supported by MACSYM 250.

PROGRAM SEGMENT EXAMPLE

A small segment from a MACBASIC application program will illustrate the power it brings to measurement and control problems. As a position sensor moves across a surface, its location is registered. Points out of specification are displayed on a terminal, and the mean of the sampled data is calculated and displayed.

MACSYM 260 PROGRAM	DESCRIPTION
310 OPENW:3 "$QTO:1"	Open port #1 for communication with a local operator interface terminal.
320 COLLECT (7, 1, 1, 1000) INTO DATA (1)	Collect 1000 data points from slot #7, channel #1, at a gain of 1, into an array with index starting at 1.
330 SUM = 0	Initialize the variable SUM to 0.
340 FOR INDEX = 1 to 1000	Over all points COLLECTED.
350 SUM = SUM + DATA (INDEX)	Add up their values.
360 IF DATA (INDEX) ≤ LIMIT GO TO 380	Check for those above a limit.
370 PRINT:3 "POINT #"; INDEX; "VALUE"; DATA (INDEX)	Display the measurement number and data value of any data point greater than the limit.
380 NEXT INDEX	
390 MEAN = SUM/1000.0	Calculate the mean value of all sampled points.
400 PRINT:3 "MEAN IS"; MEAN	Display the value of the mean.

Enhancements to this program could easily be added to check both high and low limits. Each measurement could be checked against limits specific to that point by defining arrays of limits.

MULTITASKING SCHEDULER

The MACSYM 260 has an executive which performs the operating system functions required by the MACSYM 260. This multitasking scheduler has been optimized for efficiency in the MACSYM 260 environment. It activates and suspends up to 18 MACBASIC tasks based upon the function performed by the task, as well as other tasks waiting to be processed. Input/output functions are also supervised by the multitasking scheduler.

PROM BASED SYSTEMS

The standard MACSYM 260 is shipped with 256K RAM and 12 socketed ROM locations to accommodate up to 384K of PROM in 32K × 8-bit chips. 16K × 8 chips can be used for up to 192K bytes. When a MACBASIC program has been developed and debugged, it may be burned into PROM with commercially available programmers, and installed in the MACSYM 260. From that time onward, the MACSYM 260 can operate in a stand-alone mode. When stand-alone operation is desired, applying line power to the MACSYM 260 will initiate program operation.

ADIO CARDS

Real-world signal interfacing is accomplished through the ADIO family of over 30 (Analog/Digital Input/Output) cards. They provide all the signal conditioning necessary for connection directly to voltages, currents, frequencies, thermocouples, strain gages, flow meters, relays, tachometers, valves, alarms, controllers, and other devices. Calibrated excitations, input protection, isolation, multiplexing, amplification, and other required preconditioning are supplied by ADIO cards. Sensors and actuators are connected to ADIO Cards with convenient screw terminals on a separate panel.

The ADIO library includes solid state and relay multiplexer cards for analog inputs. Cards specifically for thermocouples, RTDs and strain gages are also available. Analog output cards have both voltage and current loop drive capability. Digital inputs and outputs are available on several cards, with either solid state or relay switching. Other cards include a calendar clock function, frequency measurement, pulse counting and generation of priority interrupts. The dual loop PID control card functions independently of other system activity. Refer to the ADIO data sheets for additional details.

MACSYM 260 ARCHITECTURE

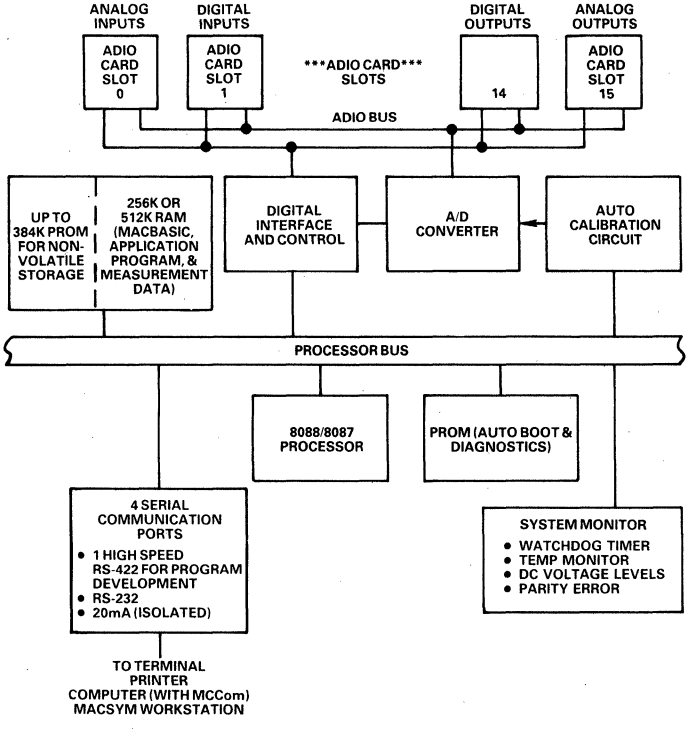
Tracing a typical analog input signal flow into the MACSYM 260 is one way to gain an appreciation for the strength of its design. An ADIO card is chosen to provide the necessary signal conditioning for the particular measurement. Then the signal is multiplexed onto the ADIO bus. Shielding on the ADIO bus separates these signals from high speed digital signals and other noise sources within the MACSYM 260. The ADIO bus carries these signals to and from the central analog I/O Interface of the CPU board. Here a multiplexer selects the input signal from the card of interest. Final amplification through a programmable gain amplifier scales the signal into a ±10 volt range. Then a sample and hold amplifier captures the signal for conversion by the analog to digital converter. This digital representation is now available to the processor bus.

The 8088 and 8087 work together to achieve rapid program execution with high accuracy. Program logic steps are executed by the 8088, while arithmetic (+, −, /, ×) and transcendental operations (sine, cosine, log) are performed by the 8087. The computational power available is illustrated by the rapid execution time of some representative MACBASIC operations. A 32-bit floating point multiply or divide (X = A * B or X = A/B) is completed in less than 290 microseconds.

DUAL MODE A/D CONVERTER

Two modes of analog to digital conversion are selectable under program control in the MACSYM 260. High speed 12-bit conversions use the successive approximation technique. In addition, a statistical integration process may be used with the AIN command to achieve 16-bit resolution. High levels of noise immunity, and line frequency normal mode rejection result from this process.

MACSYM 260 BLOCK DIAGRAM



AUTO CALIBRATION

Accurate system performance over long periods of time and changing environmental conditions is ensured by the calibration process employed in the MACSYM 260. The MACSYM 260 automatically calibrates its data acquisition section when it is powered up, and after an initial temperature stablization period of 15 minutes. Subsequent calibrations may be initiated at any time, under program control.

Calibration is accomplished by applying known, accurate reference voltages to the A/D converter's analog input. A/D conversions are performed, and each result is compared with the expected value for that particular input. Automatic adjustments are made until the A/D conversion results match expected values. When this occurs, calibration is complete.

ANALOG DATA ACQUISITION

Several modes of data acquisition are available in the MACSYM 260. COLLECT takes multiple readings from a single channel at a selected frequency. SCAN performs an analog input from selected channels and slots, with all gains and the order of sampling set up in advance. AIN returns a single analog input value of a single channel. While many additional modes are available, discussing these three modes gives information representative of MACSYM 260 performance.

A program in the MACSYM 260 may COLLECT measurements from a single channel at a rate of 33,000 samples per second, and load them into memory. Sampling multiple solid state channels is accomplished with a SCAN command, which can acquire an array of up to 16,000 data elements from one to 256 differential channels at a rate up to 7000 samples per second.

Individual analog inputs may be acquired with a command of the form "X = AIN (Slot, Channel, Gain). Response from solid state cards such as AIM03 and TIC01 is very rapid, so that when multiple AIN's are performed, data is loaded into memory at a rate above 800 samples per second.

Relay-based cards such as AIM02-XX1 and TIC02-XX1 have a slower response time, to allow for such things as contact bounce. The typical throughput speed from an individual mercury wetted relay card is 75 samples per second.

The multitasking capability of the MACSYM 260 allows a significant speed increase when several relay cards are in use. An AIN command in one task is used to initiate sampling from the first card. Without waiting for data to be returned, an AIN in the next task initiates data acquisition from the second card. After all the cards have been started, the first one is revisited to complete data acquisition from that card. Thus separate tasks are used in parallel to perform data acquisition from several slots at once. By setting up 8 two-slot mercury wetted relay cards in a fully loaded MACSYM 260, and then retrieving all 8 values, approximately 220 samples per second is achieved. Since these cards may connect to 240 to 256 individual real world points, the revisitation rate is just under once per second.

4

COMMUNICATIONS

For program development, port 0 of the MACSYM 260 communicates to the Workstation through a synchronous RS-422 port running an ADI proprietary protocol at 307.2K baud. The high speed communication link has built in error detection and recovery capability. Cyclical Redundancy Checking (CRC) error detection is performed on each message. If a bit error is detected, a retry is initiated. Should the retry fail, an error message is given, so the programmer may initiate an alternative recovery technique.

At run time, either RS-232 or 20mA isolated current loop communication may be used. Port 1 uses RS-232 to communicate with a terminal, printer, or other RS232 instrumentation. In addition, it supplies +5 volt power for a portable field terminal. Ports 2 and 3 support either RS-232 or isolated 20mA current loop connections. Rates from 50 to 19.2K baud are switch selectable.

These ports can be applied to several uses. Because some instrumentation provides an RS-232 data output, a port could bring measurement data into the MACSYM 260. Data, reports and statistics could be communicated out of one of these ports to a printer, local terminal, or another computer. A port could accept parameter changes which would modify the behavior of a program, or cause a new recipe to be run. In addition, MACBASIC programs can be edited through one of these ports when a configuration switch is set to "field terminal mode."

MCComm™

Analog Devices MCComm communication software products facilitate the use of ports 1, 2 and 3 of the MACSYM 260 when those ports are to be used to exchange data with non-ADI computers or Analog Devices Programmable Measurement and Control Units. Either RS-232 or isolated 20mA current loop hardware can be used. MCComm provides run-time support with high level language calls added to MACBASIC. MCComm defines a standard host and media independent protocol for all communicating devices. Its error checking and retry strategy makes the communication reliable. Point to point as well as multidrop configurations are supported.

MCComm also facilitates use of the MACSYM 260 with the MACSYM 120, the MACSYM 150 with DSI100/101, or IBM Personal Computers without a compatability kit. In these cases MACBASIC and an application program must be in PROM, installed in the MACSYM 260. That is because either RS-232 or isolated 20mA current loop communication is used at run time and those communication modes do not support downloading of MACBASIC from Workstation mass memory. Interaction with the Workstation is similar to interaction with any other computer in this configuration.

MCComm is a trademark of Analog Devices, Inc.

PROGRAM DEVELOPMENT

Program development for the MACSYM 260 is accomplished through a Workstation, which may be either a MACSYM 121, MACSYM 150, or IBM Computer equipped with an ADI compatability kit. The kit includes MACBASIC and necessary communication and processing hardware to interact with the MACSYM 260 over the high speed link. Refer to compatibility kit data sheets for details.

When programs are being developed, lines of MACBASIC are entered through the Workstation keyboard, used in a virtual terminal mode. Virtual terminal capability allows the Workstation screen and keyboard to service either the Workstation processor, or the MACSYM 260. Switching from one virtual terminal to another is accomplished instantly, with two keystrokes. When connected to the MACSYM 260, lines of MACBASIC are incrementally compiled by the MACSYM 260 as they are entered at the keyboard. Relevant messages are displayed on the screen. In this mode, the behavior is similar to a physical terminal directly connected to the MACSYM 260.

Debugging programs is facilitated with virtual terminal operation. Full screen editing is supported, so a few characters in a long program line can be easily changed. The virtual terminal may be instantly switched between the Workstation and MACSYM 260 to monitor the interactions between two programs running simultaneously.

Through cooperating Workstation programs, the MACSYM 260 has access to the Workstation's peripherals. Programs stored in the mass memory of the Workstation can be downloaded into the MACSYM 260. Programs developed in the MACSYM 260 can be sent to the Workstation, and stored on disk. The MACSYM 260 can also print programs or data through a printer connected to the Workstation.

In addition, the MACSYM 260 is software compatible with the MACSYM 250. Programs may be developed, and debugged on a MACSYM 250, perhaps in a laboratory or pilot plant. Then, when the approach is finalized, the program can be burned into PROM, and installed in the MACSYM 260 for production use.

UNATTENDED OPERATION

When a program has been developed and loaded into PROM, the MACSYM 260 supports stand-alone unattended operation. When power is applied, program execution begins. A keylock prevents an unauthorized reset or shutdown from the front panel.

Distributed unattended operation is also supported. RS232 or isolated 20mA communication ports can be used to send reports and receive changes in program parameters. Unit status can be indicated at a remote location utilizing the system monitor relay.

INDUSTRIAL PACKAGING

The MACSYM 260 is built with rugged, heavy gage aluminum so it will stand up to the vibration, shock, and handling found in many industrial installations.

Reliable operation is ensured in many ways. Airflow patterns were studied to minimize internal hot spots, which are frequently an underlying determinant of electronic reliability. Careful attention has also been given to reliable cabling and connections. Positive retention of field wiring cable connectors ensures continuity to ADIO cards. Provisions for cable dressing and strain relief are extensive.

Serviceability considerations are evident throughout the MACSYM 260. Diagnostic indicators aid troubleshooting. All assemblies are accessible from the front. Each major component can be removed separately, without disturbing adjacent parts of the system. For example, a cable trough routes ADIO field wiring cables up above the cards so the cable from one board does not interfere with extraction of the next.

Many human factors aspects of the MACSYM 260 have been considered. Fully assembled, the center of gravity is directly below the lifting handles for stability. Alternatively, heavy components such as the power supply are easily removed to facilitate mounting. Filters are easily accessible. Keylock of the on/off/reset switch prevents unauthorized use.

MOUNTING

The MACSYM 260 can be mounted in several ways. Lugs are provided at the rear for wall mounting. Mounting in a NEMA enclosure is facilitated because all electronic assemblies are accessible from the front. A rack mount kit, which provides a recessed front panel for cable dressing, is also available.

FAILURE DETECTION

The MACSYM 260 employs several modes of failure detection to ensure reliable operation, and provide clear indications of internal status. When initially powered up, diagnostics are run to verify microprocessor functions, and memory integrity. Parity bit error detection is employed when memory is accessed during run time. Internal voltage levels are monitored to detect line power outages or power supply problems. An improper dc level will hold the system reset until proper power is restored, when a power-up will occur. Overall operation is monitored with a watchdog timer which is periodically updated by the multitasking scheduler. Internal Unit temperature is monitored, and made available to MACBASIC programs to notify users that an air filter needs cleaning.

External indication of internal status is provided. A green lamp indicates that ac power is connected. A green LED shows that internal dc power levels are proper. Overall Unit operation is indicated with a system monitor light. Should internal temperature rise too high, a red "high temp" LED is illuminated.

Major failures, such as a parity error, or watchdog timeout will cause one of three preselected responses. The Unit can reset the ADIO cards, setting outputs of all cards except AOC07 and PID01 to zero, and halt; or halt without a reset, not affecting output values; or reset and restart the program. In each case, a major failure will cause the monitor relay (form C) to change state. This can be used with an annunciator to alert the operator, or to transfer control to a manual back-up system.

ANALOG DEVICES

Measurement and Control Communications Software

MCComm

FEATURES
Run-Time Data Exchange Between Devices
Multidrop Support (Up to 255 Devices)
Host and Media Independent
Accessible Using High Level Language Calls
ASCII Based Protocol
Reliable Serial Communications

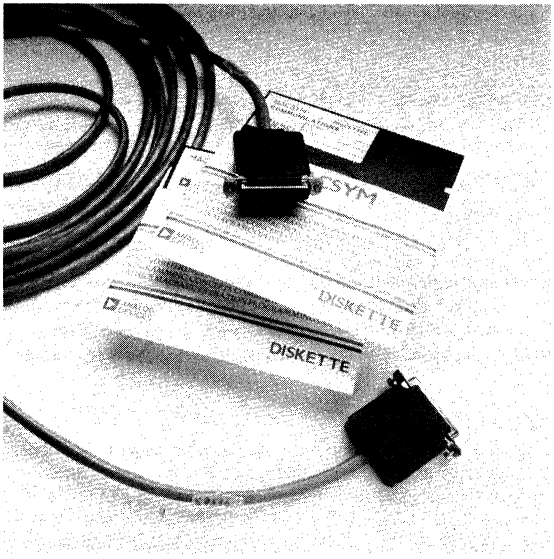
BENEFITS
Easy to Use
Master/Slave Relationship
Tutorial Documentation
Reduces Costs
Saves on Software Development Time
No Specialized Communications Hardware Required
Flexible
Supports Standard 20mA, RS-232C, Modem Communications
Compatible with New ADI System Products
Reliable
Proven and Tested
Data Integrity Met with Checksum and Time-Out Routines

APPLICATIONS
Distributed Systems – Data Transfer Between Host Computer/MACSYM® Workstations and ADI's Measurement and Control Units

Data Logging – On-Line Monitoring of Process Data in Slaves

Supervisory Control – Transmit Set Points, Loop Parameters and Function Commands to Slave Monitor Alarm and Status of Slave

Product Test – Transfer Setup Parameters to Slave Transfer Test Results to Host



DESCRIPTION

MCComm™ is a series of run-time data communication software packages which allow ADI workstations (MACSYM 120, MACSYM 150) or other host computers, such as an IBM personal computer, to communicate with measurement and control units such as the MACSYM 260 and the μMAC-5000 in a master/slave relationship. Capabilites of MCComm include on-line transmission of process parameters to host, sending of set points and alarm limits to slave, status monitoring. The software uses a simple ASCII protocol with a series of callable subroutines to pass data between the host and up to 255 slave devices. MCComm acts as a communications handler and does not effect the operation of the application program. Data in the form of reals, integers and strings are passed between devices using global arrays. Data integrity is maintained though a checksum routine, character parity, automatic retry and time-outs. It is distributed in floppy disk or PROM form, depending on the target device.

SOFTWARE OVERVIEW

MCComm software is composed of two separate packages: the MCComm Master and MCComm Slave. These packages provide the necessary run-time data communications between computers/workstations (acting as a master) and ADI's Distributed Measurement and Control Units (acting as slaves). The packages consist of a series of high level callable routines accessed by the user's application program (such as MACBASIC™ and μMACBASIC) and convert the host computer into a master and the distributed units into slaves. The following figure illustrates how MCComm MACBASIC master and the users application program are used. In the Master, the application program calls the MCComm routines which supports all communications and returns the status and data to the applications program. In the Slave, the communication software runs as a background routine independent of the application program, responding to the Master's requests for status and data. Data stored in arrays is passed between the application program and the MCComm software routine.

MACSYM is a registered trademark of Analog Devices, Inc.
MCComm and MACBASIC are trademarks of Analog Devices, Inc.

This four-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

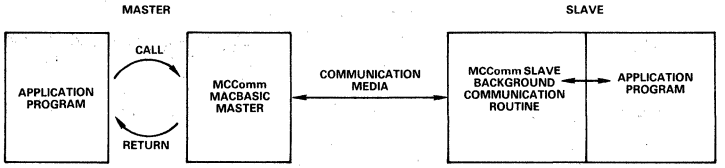


Figure 1. MCComm Master/Slave Communication Scheme

With the MCComm Master package, the host computer becomes a master. It initiates all communication to the slave devices. The master may be used to read data from or write data to any of the slaves. The master may be used to read on-line measurement and control data and write new set points and configurations to the slave(s). It may also be used to simply monitor the status of the slave devices.

With the MCComm Slave package, data passed between the master and slave is stored in arrays in the memory of the slave. These arrays or tables can be used by the application program that is running on the slave. The host (or master) is able to access the same data through communications calls. Single elements, as well as groups of data, can be read from or written to data arrays which are resident in the slave device. The data arrays within the slave are in the form of integers, reals, and strings.

MCComm OPERATION

MCComm performs communications between a master and one or more slave devices by providing software communications routines that transfer data over a serial link using a predefined protocol. Data transfer is transparent to the user because it is done through MCComm routines which are called from the user's application program running in the master. The software routines, in turn, use the MCComm communications protocol to actually transfer the data. Communication takes place in a command/response format with the host *always* initiating the communications action.

Data transfer rates vary depending on the host computer used and the baud rate selected.

In Figure 2, we see a typical command/response with the data exchange called a packet. In this example, three data values are returned to the host in the slave response. When using a host running MACBASIC, up to 3 packets of up to 5 data values can be exchanged every second. This means that a master can exchange data with up to 3 slaves every second. The number of slaves which can be polled is dependent on the size of these packets. If only one slave is polled, a packet of 20 data values consisting of integer or real values can be transferred in one second.

MCComm COMMANDS

The MCComm commands determine the type of data that is transferred between the master and the slave devices. The MCComm Master routine provides six commands to read and write the data stored within the slave device as well as a dedicated command to read the slave status. These commands allow individual data items, as well as groups of data items, to be accessed in a single communication exchange. Included below is a listing of these commands:

COMMAND CODE	COMMAND FUNCTION
1	Write Integer Data to Slave Array
2	Write Real Data to Slave Array
3	Write String Data to Slave Array
4	Read Integer Data from Slave Array
5	Read Real Data from Slave Array
6	Read String Data from Slave Array
7	Read Status of Slave (see section on Slave Status)

When the MCComm communication routine is called from the user's application program, data is transferred according to the command selected. The following steps are required in the Master application program to perform this data transfer.

1. Initialize the sizes of the integer, real, and string data variables.
2. Select the appropriate COMMAND (1 to 7) for data transfer.
3. Set up additional parameters (e.g., slave address) in the master.
4. Call the MCComm communications routine.

When the communication routine is called, data is transferred according to the standards of the MCComm communication protocol.

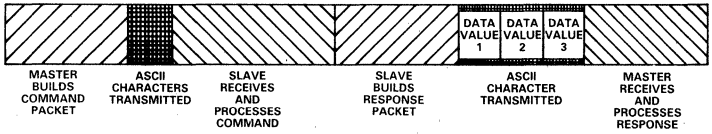


Figure 2. MCComm Data Exchange

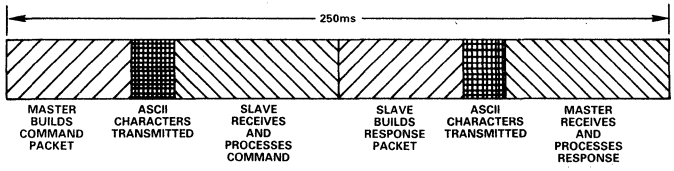


Figure 3. MCComm Status Checking Routing

SLAVE STATUS

A variable in the slave stores a user-defined integer value that is sent back to the master as part of any slave response. This parameter is only used by the user application program and is not tested by the communication routine. This status value can be used to flag events in the slave devices that need immediate attention by the master.

In the following example, we are using MACBASIC and have predefined the variable SLAVESTAT' as follows:

SLAVESTAT' = 0 when the slave is OK.
SLAVESTAT' = 1 if the temperature measured by the slave is below a limit.
SLAVESTAT' = 2 if the temperature measured by the slave is above a limit.

Using the following routine in the MCComm Master application program, the slave status value is tested and appropriate action taken.

STATUS EXAMPLE

```
900     REM SUBROUTINE TO TEST AND OPERATE ON
            SLAVESTAT'
910     IF SLAVESTAT' = 0 THEN RETURN  REM
        EVERYTHING OK
920     IF SLAVESTAT' = 1 THEN GO TO 1000  REM
        TEMP LO
930     IF SLAVESTAT' = 2 THEN GO TO 2000  REM
        TEMP HI
940     RETURN REM IF SLAVESTAT'
                <>  0,1,OR 2
                .
                .
                .
1000    REM ROUTINE TO SERVICE LOW TEMP
            ALARM CONDITION
1999    RETURN
2000    REM ROUTINE TO SERVICE HI TEMP
            ALARM CONDITION
                .
                .
                .
2999    RETURN
```

Status checks of the slaves can be performed at a rate of 4 per second. The structure of a status checking routine is shown in Figure 3.

HOST/SLAVE CONNECTION

MCComm supports a multidrop/distributed configuration of a master connected to slave devices such as the ones shown in Figure 4. Unlike many data highways, no special communications hardware is required since we use a simple asynchronous ASCII-based serial link to connect the devices. This eliminates the need to purchase expensive interface boxes and specialized test equipment. The master/slave communication link can be configured in either point-to-point or multidrop (party line) configurations. Various hardware interface media such as RS-232C, 20mA, and modems can be used with the MCComm packages. You can also easily mix different devices since all slaves running MCComm look the same. The protocol can support up to 255 slaves on the same communications link in a modem configuration. In a multidrop configuration, up to 16 slaves can be connected on the same 20mA link.

COMMUNICATIONS PROTOCOL

MCComm protocol establishes a set of rules that are followed when transmitting data between different devices. MCComm is a command/response, packet-oriented protocol with all the communication requests originating from the host. The relationship between host and remote devices is that of a master and slaves. Address recognition is provided in the slave package to enable a series of multidrop slaves to share a single communication line with the master. Reliable data transmission is provided using check sum and character parity error detection. The MCComm master packages also contain time-out detection to prevent system hangup in the event that a slave fails to respond or a communication link failure occurs. If an error is detected by the master, it automatically tries again to communicate with the slave. If, after retrying, it still cannot achieve error-free communication to a slave device, the master communication package reports an error to the applications program.

RUN-TIME COMMUNICATIONS

The MCComm Master and MCComm Slave communications packages provide support for run-time data communications between devices. Run-time means that both sides (master and slave) of the communications process must have a running applications program in order for data to be transferred. This data transfer is transparent to the user since it is done through MCComm software routines which are called from the user's application program.

Data, in the form of integer, real, and strings, are passed between the host and slave as an accessible data arrays. They are accessed from the application program using high level command calls.

HOST INDEPENDENT

MCComm provides host and media independent communications to the user. The simple ASCII-based protocol has been designed in such a way that nearly any host not supported by ADI can be tied into a MCComm communication if it has a RS-232C or 20mA serial port. The user's guide clearly defines the master/slave protocol which gives the systems programmer the ability to develop a master communication routine for other computers.

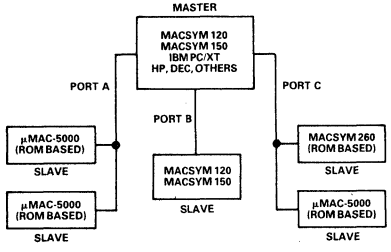


Figure 4. Hierarchical Serial Data Link Configuration Supported by MCComm

DOCUMENTATION

MCComm is furnished with full tutorial documentation to allow a user with little or no data communications experience to feel comfortable installing, using, and maintaining this communications system. Documentation for MCComm includes a general MCComm Guide, the MCComm Master User's Guide and the MCComm Slave User's Guide. The MCComm Guide answers communications questions that the user may have, whether it be on recommended communications media or the nature of communications principles in general. The guide includes a discussion on ASCII asynchronous serial communications, media selection, hardware configurations and communications media installation as well as providing information on the communications protocol. The MCComm Master and Slave User's Guides detail the software structure and describe how to write application programs using MCComm software.

DISTRIBUTION OF MCComm

There are two types of MCComm software modules, one for the host and one for the slave. They are installed by the user and supplied in floppy disk or PROM form.

SUMMARY

MCComm is ideal for users of Analog Devices' μMAC and MACSYM products who want to have a simple but efficient method of implementing communication without having to write communications software. MCComm provides quick and easy startups since it uses high level subroutine calls to interface with your program. Data integrity is maintained with error detection and automatic retry facilities which are built into the package. A simple protocol makes troubleshooting straightforward. MCComm's open architecture and straightforward design makes it easy to port to other hosts. The software can operate over virtually any media, ranging from shielded twisted pair, to telephone lines, to radio links, to broadband coaxial cable systems. And, finally, the protocol allows up to 255 devices on one communications line.

ORDERING INFORMATION

To use MCComm, both a master and a slave package must be selected that runs on the appropriate unit.

SOFTWARE PRODUCTS

P/N	USED ON	OPERATING SYSTEM	MEDIA	DESCRIPTION
MCCOMM-M120	MACSYM 120 IBM PC/XT* MACSYM 260[1]	CCP/M	Floppy Disk	MACBASIC Master Software MACBASIC Master User's Guide MCComm User's Guide
MCCOMM-M150	MACSYM 150 MACSYM 260[1]	MP/M or CCP/M	Floppy Disk	MACBASIC MASTER Software MACBASIC Master User's Guide MCComm User's Guide
MCCOMM-S120	MACSYM 120 IBM PC/XT MACSYM 260[1]	CCP/M	Floppy Disk	MACBASIC SLAVE Software MACBASIC SLAVE User's Guide MCComm User's Guide
MCCOMM-S150	MACSYM 150 MACSYM 260[1]	MP/M or CCP/M	Floppy Disk	MACBASIC SLAVE Software MACBASIC SLAVE User's Guide MCComm User's Guide
MCCOMM-S5000	μMAC-5000	REV1.3 or later	ROM	μMACBASIC SLAVE Software μMACBASIC SLAVE User's Guide MCComm User's Guide

NOTE

[1]Attn. MACSYM 260 Users – To install MCComm communications and develop application programs, you must have either a MACSYM 121, MACSYM 150 or IBM PC/XT with a compatibility kit. The MCComm Software is ordered for the workstation. Programs are then downloaded to MACSYM 260's or burned into EPROMs.

*IBM PC/XT is a trademark of International Business Machines Corporation.

ANALOG DEVICES

Two Channel Isolated Analog Output Module

QMXAO

FEATURES
Two Independent Analog Output Channels
12-Bit Resolution, ±0.05% Accuracy
Simultaneous Voltage and Current Outputs per Channel
High CMV Isolation: ±1000V Peak
Plugs into Sockets on the μMAC-5000 or μMAC-4010

APPLICATIONS
Excitation Source (Strain Gage and Potentiometers)
Proportional Control
Current-to-Position Converter
Low-Cost Multiloop Controller
Furnace and Oven Control

4

GENERAL DESCRIPTION

The QMXAO is a two channel, analog output module that plugs into any QMX socket on the μMAC-5000 Master Board or μMAC-4010 Expander Board. It allows a user to add analog output capability to a μMAC-5000 Master Board without the need for an analog output expander board (μMAC-4030).

Each analog channel has two tracking outputs; a 0 to +10V or ±10V voltage output and a 4-to-20mA or 0-to-20mA current loop output. In addition to the 12-bit resolution and ±0.05% accuracy, each channel is isolated to ±1000V peak from each other and also from system ground.

The drive capability in the voltage output mode is ±4mA minimum at full scale range (±15mA for ranges up to ±5V) and is protected against shorts to ground. Loop power is internally provided for the current loop output and is capable of driving resistive loads of 0 to 500Ω.

The QMXAO is a low cost solution to adding analog output capability to a μMAC-5000 system. The QMXAO can be ordered separately and installed by the user in an existing μMAC-5000 system or ordered configuration on a μMAC-5000 or μMAC-4010 board. Up to three QMXAO modules can be installed on a board. It can be mixed with any combination of QMX input modules.

APPLICATIONS

Analog outputs are required to drive actuators, position valves or operate set point controllers in control applications, or to drive recorders or indicators in monitoring applications. The voltage output mode can also be used as an excitation source for sensors such as strain gages and load cells. For example, a 350Ω strain gage can be excited by setting the voltage output to +5V (thereby drawing less than 15mA). To optimize accuracy, trimpots allow optional adjustment of the excitation source.

Figure 1 shows a μMAC-5000 configured with a single QMX03 input module and two QMXAO output modules implementing four PID control loops. The QMX modules provide total isolation on both analog inputs and outputs. The simultaneous output on the QMXAO is driving a recorder which is monitoring the output drive level.

Another potential application could be the μMAC-5000 operating in a supervisory mode (performing monitoring or control functions and communicating to a host computer), where the QMXAO output is controlling the set point of a dedicated process controller.

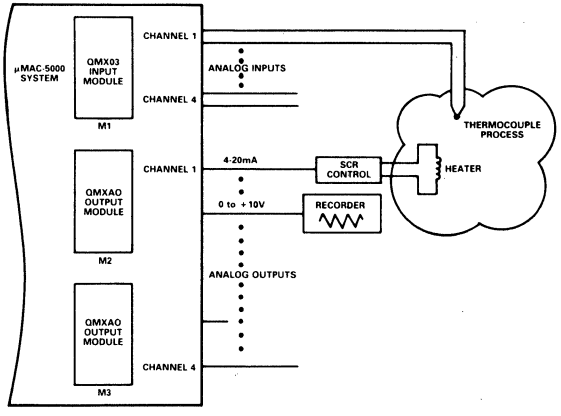


Figure 1. μMAC-5000 Single Board 4-Loop PID Controller

SPECIFICATIONS (typical +25°C and nominal power supply voltage)

Number of Channels		2
Output Types per Channel		Isolated Voltage and Current
Voltage Output		
Output Range[1]	Resolution	Accuracy (% Span)[1]
0 to +10V[2]	2.68mV	±0.05
±10V[2]	5.4mV	±0.1%
Current Drive	0 to ±5V: ±15mA ±5 to ±10V: Derated to +4mA ±10V to ±11V: ±1.8mA	
Monotonicity		Guaranteed, 0 to +60°C
Offset TC		±0.001% of Span °C
Span TC		±0.003% of Span °C
Settling Time		
Full Scale Step Change		600µs
Output Resistance		0.1Ω
Output Protection[3]		2 Minutes Short to Ground
Common-Mode Rejection @ 50/60Hz		106dB
Current Output[1]		
Output Range[4,5]	Resolution	Accuracy (% Span)
0-to-20mA	5.4µA	±0.05
4-to-20mA	5.4µA	±0.05
Monotonicity		Guaranteed, 0 to +60°C
Offset TC		±0.002% of Span°C
Span TC		±0.004% of Span/°C
Settling Time		
Full Scale Step Change		600µs
Common-Mode Rejection		
50/60Hz, R_L = 250Ω		104dB
Load Resistance Range[6]		0 to 500Ω max
Isolated Loop Power		Internally Provided
Output Protection		130V rms continuous
CMV Isolation		
Channel-to-Channel, Input-to-Output		±1000V peak Continuous
µMAC Board Compatibility		µMAC-4010[7] and µMAC-5000
Number of QMXAO per Board		Up to 3
AOTX Execution Time		25ms
µMACBASIC Software Requirement		Rev 1.4 or higher[8]

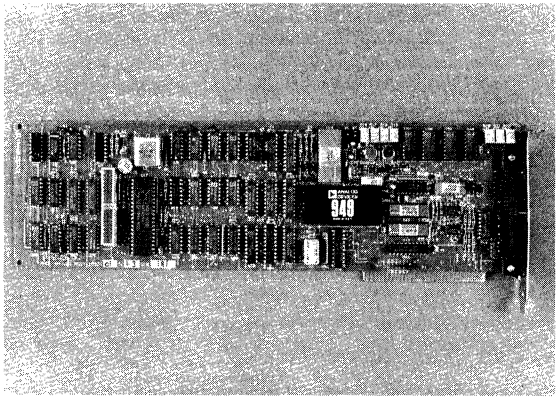
NOTES
[1] +10% overrange capability in software.
[2] Factory-calibrated system accuracy. Can be user-trimmed to higher accuracy if voltage output currents do not exceed 5mA and current outputs are not used.
[3] One channel only.
[4] If voltage output is configured for ±10V (bipolar), the current output accuracy on the same channel degrades to 2.5% which cannot be trimmed for higher accuracy.
[5] ±0.5mA maximum load current available on voltage output when using current output operation.
[6] User must provide loop power (up to +30V) for higher load resistance ranges.
[7] QMXAO can be used on µMAC-4010 only when in a µMAC-5000 system.
[8] The QMXAO can be used with earlier releases of software by using a µMACBASIC procedure included with the module.

Specifications subject to change without notice.

ANALOG DEVICES

IBM PC/XT/AT Compatible Multifunction Analog and Digital Board

RTI-800/815



FEATURES

RTI-800 Analog Input and Digital I/O Board
- 16 Analog Input Channels (Expandable to 32)
- Software Programmable Gain 1, 10, 100 and 500
- 12-Bit 25μs A/D (Optional 8 and 12μs Versions)
- Throughputs up to 71,000 Sample/Second
- Three A/D Trigger Modes Including External Trigger
- 8 Digital Input and 8 Digital Output Channels
- 3 Counter/Timer Channels

RTI-815 Multifunction Analog Input/Output and Digital I/O Board
- (Same Features as RTI-800 and Includes)
  - 2 Analog Output Channels
  - 12-Bit Resolution

GENERAL
- Supports DMA, Polled Status and Interrupt Operation
- Compatible to IBM PC/XT/AT* or Equivalent
- Optional Screw Termination Panels

SOFTWARE
- Callable Machine Language Routines for Analog and Digital I/O
- High-Level Language Support
  - BASIC, PASCAL, C, FORTRAN and TURBO PASCAL Running under PC-DOS
- Calibration Routines

TYPICAL APPLICATIONS
- Electronic Test
- Quality Assurance
- Data Logging
- Machine Control
- Analytical Data Acquisition
- Process Control
- Robotics
- Imaging
- Instrumentation

GENERAL DESCRIPTION

The RTI-800 and RTI-815, IBM-compatible members of the RTI® Interface family, are multifunction analog and digital I/O boards that plug into one of the expansion slots in the IBM PC/XT/AT. Their functions include analog input, analog output (RTI-815 only) digital I/O and time related functions.

The boards provide data acquisition for 16 single-ended or 8 differential channels with optional expansion to 32 single ended or 16 differential channels. The instrumentation amplifier is software selectable for gains of 1, 10, 100 and 500 which increases the dynamic input range for a variety of input signals. Combining this with a sample-hold circuit and a 12-bit A/D converter, the data acquisition section features ±0.02% accuracy and 12-bit resolution with conversion times of either 8, 12 or 25μs (depending on option). The RTI-815 provides two analog output channels consisting of two 12-bit D/A converters.

RTI is a registered trademark of Analog Devices, Inc.

***IBM PC/XT/AT is a trademark of International Business Machines Corporation**

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

The digital I/O is brought out on a separate connector and contains 8 digital inputs and 8 digital outputs. A counter/timer device is used to generate a pacer clock for A/D triggers and can be set up for event counting, frequency measurements, time proportional outputs, or single pulse outputs. This provides two channels of frequency measurements to 100kHz or three channels for event counting or pulse train outputs.

There are six interrupt lines (jumper selectable) to select from which are used by the PC to indicate an end of conversion. Several modes of A/D operation are possible, since the RTI-800/815 contains the hardware necessary to support Direct Memory Access (DMA), Polled Status, or Interrupt Operation.

The RTI-800/815 maps into the I/O channel address structure as 16 consecutive bytes, addressable in any unoccupied 16-byte boundary via a DIP switch. The board contains a dc/dc converter and is powered from the PC's +5V supply. It installs in one of the long slots in the PC expansion bus.

FUNCTIONAL DESCRIPTION

The RTI-800/815 is a multifunction analog/digital input/output board that plugs into one of the available long expansion slots in the IBM PC, PC/XT, PC/AT, or equivalent personal computer. The RTI-800 board has capabilities for analog input, digital input and output, and time-related digital I/O functions (through the AM9513A Counter/Timer chip). The RTI-815 board has the same capabilities as the RTI-800, along with two analog output channels.

SPECIFICATIONS (typical @ 25°C with nominal power supply voltage unless otherwise noted)

ANALOG INPUT	
Number of Input Channels[1]	16 Single-Ended, 16 Pseudo-Differential, or 8 Differential Inputs Expandable to 32 Single-Ended, 32 Pseudo-Differential, or 16 Differential Input Channels Using the Multiplexer Expansion Kit (ADI Part Number OA10)
Analog Resolution	12 Bits (4096 Counts)
A/D Ranges[1]	0 to 10V; ± 5V; ± 10V
Analog Input Codes[1]	Binary, Two's Complement
Instrumentation Amplifier Gain Ranges	1, 10, 100, 500V/V (Software Selectable)
A/D Conversion Time (Converter Only)[2]	
RTI-800 and RTI-815	25μs
RTI-800-A and RTI-815-A	12μs
RTI-800-F and RTI-815-F	8μs
System Throughput[3]	
RTI-800 and RTI-815	32.2kHz
RTI-800-A and RTI-815-A	55.5kHz
RTI-800-F and RTI-815-F	71.4kHz
Measurement Accuracy	± 0.02% of Full-Scale Range (10V) ± 0.03% of Full-Scale Range (1V) ± 0.12% of Full-Scale Range (100mV) ± 0.25% of Full-Scale Range (20mV)
Input Overvoltage Protection	± 35V (Powered), ± 20V (Unpowered)
Input Impedance	$>10^8\Omega$
Input Bias Current	± 20nA
Common Mode Voltage (CMV)	± 10V min
Common Mode Rejection (CMR)	80dB
Linearity	± 1/2LSB
Differential Nonlinearity	± 1LSB max
Temperature Coefficients	
Gains	± 30ppm/°C of Full-Scale Range (10V) ± 100ppm/°C of Full-Scale Range (20mV)
Offset	± 10ppm/°C of Full-Scale Range (10V) ± 100ppm/°C of Full-Scale Range (20mV)
ANALOG OUTPUT (RTI-815 ONLY)	
Number of Output Channels	2
Output Voltage Ranges[1]	0 to + 10V, ± 10V @2mA
D/A Resolution	12 Bits (4096 Counts)
Analog Output Accuracy	± 0.02%
D/A Input Codes[1]	Binary, Two's Complement
Differential Nonlinearity[4]	± 1LSB max
Output Settling Time (Converter Only)	20μs (to ± 1/2LSB, 10V Step)
Monotonicity	Guaranteed Over Operating Temperature
Temperature Coefficients	
Gains	± 15ppm/°C of Full-Scale Range
Offset	± 25μV/°C
Output Protection	Short-to-Ground, Continuous
DIGITAL I/O	
Digital I/O	8-Bit Digital Input Port and 8-Bit Digital Output Port, Polarity Inverted for Solid-State Relay Subsystem Compatibility (Active Low)
Input/Output Configuration	TTL Compatible
TIME-RELATED DIGITAL I/O	
Number of Counter/Timer Channels[5]	3
Modes of Operation	Event Counting, Frequency Measurement, Pulse Output, Time Proportional Outputs
SYSTEM CONFIGURATION	
Bus Resource Utilization	Occupies One Long Slot in the IBM Expansion Bus
Address	Switch-Selectable I/O Location (16 Consecutive Bytes in 512-Byte Block)
Data Acquisition Modes	High Speed Scan and Collect A/D Conversions Require Availability of DMA and Interrupt. Polled Status Does Not Require This Source
Compatibility	IBM, Compaq, or Other IBM-Compatible Backplane
PHYSICAL/ENVIRONMENTAL	
I/O Connector	
Analog I/O (J2)	50-Pin Male Ribbon Connector
Digital I/O (J1)	34-Pin Male Ribbon Connector
Dimensions (Including Connector)	4.2" (10.6cm) × 13.1" (33.2cm) × 1" (2.54cm)
Operating Temperature Range	0 to + 70°C
Storage Temperature Range	− 25°C to + 85°C
Relative Humidity	Up to 90% (Noncondensing)
POWER	
Power Consumption	+ 5V @ 1.1A

NOTES
[1]Jumper selectable.
[2]The A/D conversion must be initiated through the software convert command, an external convert pulse, or the pacer output of the AM9513A Counter/Timer chip. If using an external convert command pulse, it must be an LSTTL input signal, falling edge sensitive, with a minimum pulse width of 200ns.
[3]System throughput calculated for multiple channel scan at a gain of 1. The throughput will be less for higher gain settings. Note that throughput includes the 5μs time required for each DMA data transfer (two transfers per A/D conversion). Throughput = A/D conversion time + data transfer time.
[4]Monotonic over operating temperature range.
[5]The AM9513A Counter/Timer chip is used to provide the time-related functions. In addition, there is a dedicated 4-bit frequency output channel. Extensive assembly language programming is required to use these functions.

Specifications subject to change without notice.

ANALOG DEVICES

IBM PC/XT/AT Compatible Analog Output Board

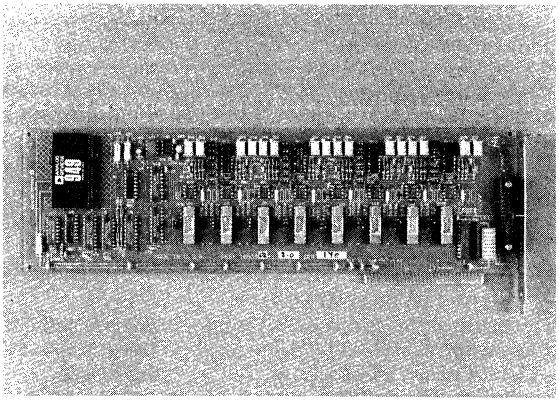
RTI-802

FEATURES
4 or 8 Analog Input Channels
12-Bit Resolution
0 to +10V or ±10V Output Range

GENERAL
Compatible to IBM PC/XT/AT* or Equivalent
Optional Screw Termination Panels

SOFTWARE
Callable Machine Language Routines for Digital I/O
High Level Language Support
BASIC, PASCAL, C, FORTRAN and TURBO PASCAL running under PC-DOS
Calibration Routines

APPLICATIONS
Precision Voltage Outputs
Position and Motion Control
Generate Set-Point Values for Loop Controllers



4

GENERAL DESCRIPTION

The RTI-802 analog output board, an IBM-compatible member of the RTI® Interface family, comes in two versions: a 4-channel (RTI-802-4 board) and an 8-channel board (RTI-802-8) for high-channel capacity applications. The analog outputs are user selectable for 0 to 10V or ±10V and are protected from shorts to ground. There is one 12-bit D/A converter per channel for maximum update rates.

The RTI-802 maps into the I/O channel structure as 4 consecutive bytes, addressable to any unoccupied 4-byte boundary via a DIP switch. The board contains a dc/dc converter and is powered from a PC's +5V supply. It installs in one of the long slots in the IBM PC/XT/AT.

Typical applications for the RTI-802 include direct control valve positioning or as a stimuli in test applications, utilizing a variable voltage output. The board can also be used for analog control in a process or laboratory application where material transfer rates, fluid flow, power consumption, motor speed, temperature levels, etc., are to be controlled. In a supervisory control applications, the generated analog outputs are used to provide set points to analog loop controllers.

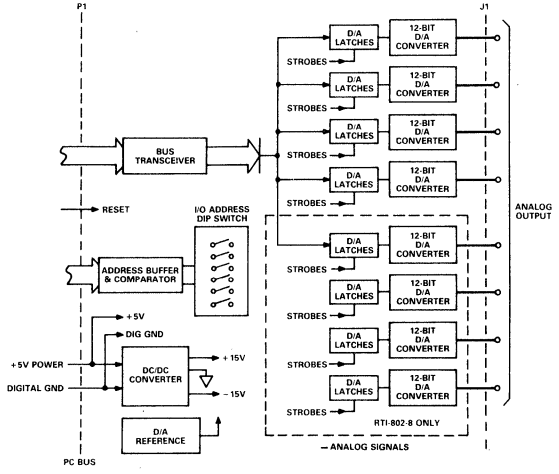


Figure 1. RTI-802 Block Diagram

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***IBM PC/XT/AT is a trademark of International Business Machines Corporation.**

SPECIFICATIONS (typical @ 25°C with nominal supply voltage unless otherwise noted)

ELECTRICAL	
Number of Analog Output Channels	
RTI-802-4	4
RTI-802-8	8
Analog Voltage Ranges[1]	0 to +10V, ±10V @2mA
D/A Resolution	12 Bits (4096 Counts)
Analog Output Accuracy	±0.02%
D/A Input Codes[1]	Binary, Two's Complement
Differential Nonlinearity	±1LSB max
Output Settling Time (Converter Only)	20μs (to ±1/2LSB, 10V Step)
Temperature Coefficients	
Gain	±15ppm/°C of Full-Scale Range
Offset	±25μV/°C
Output Protection	Short-to-Ground, Continuous
SYSTEM CONFIGURATION	
Bus Resource Utilization	Occupies One Long Slot in the IBM Expansion Bus
Address	Switch Selectable I/O Location (4 Bytes in 512 Byte Block)
Compatiblity	IBM, Compaq, or Other IBM-Compatible Backplanes
PHYSICAL/ENVIRONMENTAL	
I/O Connector	26-Pin Male Ribbon Cable
Dimensions	13.8" (35cm) × 5" (12.72cm) × 1" (2.54cm)
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−25°C to +85°C
Relative Humidity	Up to 90% (Noncondensing)
POWER	
Power Consumption	+5V dc @ 0.5 amp

NOTES
[1]Jumper selectable.
Specifications subject to change without notice.

ANALOG DEVICES

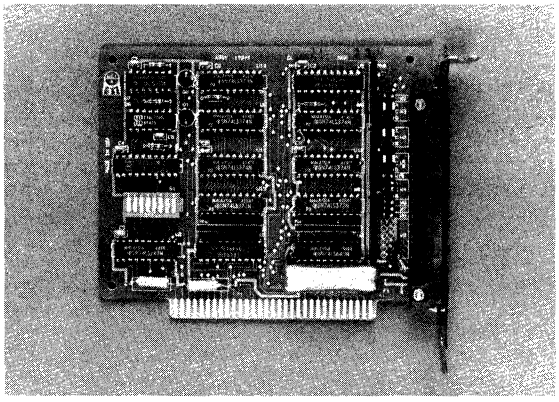
IBM PC/XT/AT Compatible Digital Input/Output Board

RTI-817

FEATURES
24 Channels of Digital Input/Output
Three 8-Bit Groups Independently Selectable for I/O
Interrupt Generation on Change of State
Compatible to 16 and 24 Position Solid-State Relay Subsystems

GENERAL
Compatible to IBM PC/XT/AT* or Equivalent
Optional Screw Termination Panels

APPLICATIONS
Parallel Data Transfer to PC
Digital I/O Control
AC or DC Monitoring and Control of Voltages
Relay Control



4

GENERAL DESCRIPTION

An IBM-compatible member of the RTI® Interface family, the RTI-817 is a 24-channel (bit) input and output board that plugs into one of the expansion slots in the IBM PC/XT/AT. The board can be used with TTL low-level input/output circuitry or with solid-state relay subsystems (16- or 24-channel versions) to provide 2500V isolation for interfacing with high-level ac and dc signals.

The 24-channel capability of the RTI-817 is divided into three ports (or groups) with 8 bits per group. These eight bit ports can be configured for either a digital input or output function.

There are two unique features associated with the RTI-817: an eight-bit latching capability and an interrupt on change of state. The latching capability is software or hardware selectable. It stores the state of eight digital input lines in a register which can then be read from the PC data bus. Interrupt generation occurs when one of the eight digital input channels changes state in a single port. This feature frees up the PC to do other activities since there is no need to poll the digital input port for an event to occur.

The RTI-817 can be installed in either a long or short slot in the IBM PC/XT/AT. The board maps into the I/O channel address structure as 4 consecutive bytes, addressable in an unoccupied 4-byte boundary using a DIP switch. The board operates from the bus +5V power source.

Typical applications of the RTI-817 include sensing and control of high-level signals, sensing low-level (TTL) switches or signals, driving indicator lights or controlling recorders, and parallel data transfer (via software) to computers or panel meters.

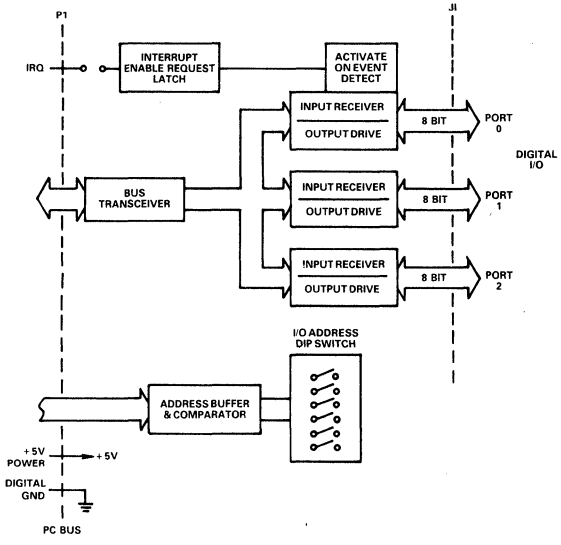


Figure 1. RTI-817 Block Diagram

RTI is a registered trademark of Analog Devices, Inc.
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SPECIFICATIONS (typically at +25°C and nominal power supply voltage unless otherwise specified)

DIGITAL INPUT AND OUTPUT	
NUMBER OF CHANNELS	24, Selectable in 8-Bit Groups or Ports Inputs or Outputs
I/O CONFIGURATION[1]	TTL Compatible
INPUT SPECIFICATION	V_{IH} = 2.0V min V_{IL} = 0.8V max I_{IL} = 1.5mA max I_{IH} = 20μA max
OUTPUT SPECIFICATIONS	V_{OH} = 2.4V min V_{OL} = 0.5V max I_{OL} = 23mA I_{OH} = 3.6mA max
MAXIMUM APPLIED VOLTAGE	7V dc
ISOLATION VOLTAGE	N/A
SYSTEM CONFIGURATION SPECIFICATIONS	
Bus Resource Utilization	Occupies One Short or Long Slot in IBM Expansion Bus. Use of Interrupt Channel is Optional
Address	Switch Selectable I/O Locations (4 Consecutive Bytes in 512 Byte Block)
Digital Input Monitoring Modes	Interrupt Line Required for Use as System Priority Interrupt
Compatibility	IBM, Compaq, or Other IBM-Compatible Backplane
PHYSICAL/ENVIRONMENTAL SPECIFICATIONS	
I/O Connector	50-Pin Male Ribbon Connector
Dimensions	5 7/8 in. (14.4 cm.) × 5 in. (17.2 cm.) × 1 in. (2.54 cm.)
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−25°C to +85°C
Relative Humidity	Up to 90% (Non-Condensing)
POWER	
Power Consumption	+5V dc @ 0.5A max

NOTES
[1]Polarity inverted for solid-state relay compatibility (active low) such as OPTO-22 or equivalent.
Specifications are subject to change without notice.

ANALOG DEVICES

CMOS STD Compatible Analog and Digital I/O Cards

RTI-1280 Series

FEATURES

RTI-1280 Analog Input Card
- **16SE/8D Analog Input Channels**
- **Jumper Selectable Gains of 1, 10, 100 and 500**
- **12-Bit A/D Resolution**

RTI-1281 Analog Input/Output Card
- **(Same Features as RTI-1280 and Includes)**
- **2 Analog Output Channels**
- **12-Bit Resolution**

RTI-1282 Analog Output Card
- **4 or 8 Analog Outputs**
- **12-Bit Resolution**
- **4-20mA Current Loop Outputs (optional)**

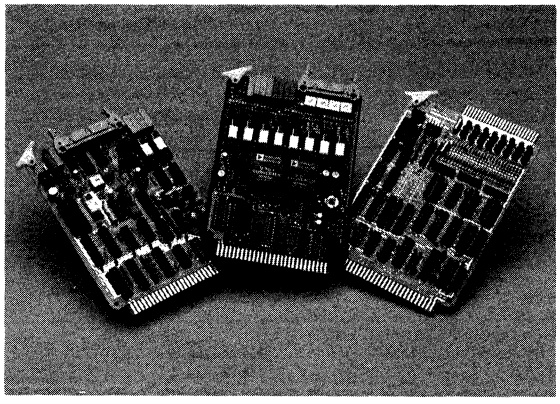
RTI-1287 Digital Input/Output Card
- **24 Digital Input/Output Channels**
- **Three 8-Bit Read/Write Ports Control 24 Bidirectional Lines**
- **Compatible to Industry Standard I/O Relay Rack (OPTO-22, Gordos)**

GENERAL
- **Low Power CMOS Design**
- **Compatible to all CMOS STD CPU Cards**
- **Memory or Port I/O Configurable**
- **Single +5V Power Requirement**
- **−25°C to +85°C Temperature Range**

SERIES DESCRIPTION

A CMOS STD-compatible family of the RTI® Interface product line, the RTI-1280 Series products are analog and digital input/output cards. Designed with high-speed, low-power CMOS technology, these products provide low-power, high noise immunity, and extended temperature ranges operation. They are cost effective and provide a convenient means of interfacing your CMOS STD bus microcomputer to the real (i.e., analog and digital) world.

The series consists of an analog input card (RTI-1280), an analog I/O card (RTI-1281), an analog output card (RTI-1282) and a digital I/O card (RTI-1287): each of which interfaces to the CMOS STD bus as either memory mapped or I/O port addressed peripherals through user-selectable jumpers.



APPLICATIONS

This family of CMOS STD BUS I/O cards from Analog Devices solves the problem of interfacing real-world signals to the μC bus. Using new high-speed analog and digital CMOS technology, these cards offer low power, high noise immunity and extended operating temperature ranges. Described in this technical document are analog and digital interface cards designed for use in harsh environments, remote sites, and battery-backed applications. Applications for these products include:

Well Site Supervision
Pipeline Monitoring
Meterological Data Acquisition
Process Control
Medical Electronics
Battery-Powered Instrumentation
SCADA Systems
Energy Management

Card Type	Model Number	Channel Capacity Input	Output
Analog Input	RTI-1280	16SE/8D	–
Analog Input/Output	RTI-1281	16SE/8D	2
Analog Output	RTI-1282-4	–	4
Analog Output	RTI-1282-8	–	8
Digital Input/Output	RTI-1287	24 I/O	

Table I. RTI-1280 Series Functional Chart

RTI is a registered trademark of Analog Devices, Inc.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

SPECIFICATIONS (typical @ 25°C with nominal supply voltage unless otherwise noted)

ANALOG INPUTS RTI-1280/1281	
Number of Input Channels	16 Single-Ended, 16 Pseudo-Differential or 8 Differential (Jumper Selectable)
Input Overvoltage Protection[1]	± 35V (Dielectrically Isolated)
Input Impedance	$>10^8\Omega$
Input Bias Current	± 50nA
Common-Mode Voltage (CMV)	± 10V min
Instrumentation Amplifier Gain Ranges[2]	1, 10, 100, 500 (Jumper Selectable) (Provisions for a Resistor Programmable Gain Up to 1000)
Common-Mode Rejection Ratio (CMRR)	86dB
A/D Ranges	0 to + 10V, ± 10V (Jumper Selectable)
A/D Resolution	12 Bits
A/D Conversion Time	55µs
Throughput (Multiple Channels)	12,000 Channels/sec (Gain = 1, 10) 10,000 Channels/sec (Gain = 100) 7,500 Channels/sec (Gain = 500)
(Single Channel)	16,000 Channels/sec (Gain = 1, 10, 100)
Temperature Coefficients	
Gain	± 30ppm/°C of FSR (Gain = 1) ± 100ppm/°C of FSR (Gain = 500)
Offset	± 30ppm/°C of FSR (Gain = 1) ± 100ppm/°C of FSR (Gain = 500)
Differential Nonlinearity	± 1/2LSB
Total System Errors	± 0.02% of FSR (G = 1) ± 0.05% of FSR (G = 10) ± 0.07% of FSR (G = 100) ± 0.1% of FSR (G = 500)

ANALOG OUTPUT RTI-1281/1282	
Number of Output Channels	2 (RTI-1281) 4 (RTI-1282-4) 8 (RTI-1282-8)
D/A Input Codes	Binary, Offset Binary (Jumper Selectable)
Output Voltage Ranges	0 to + 5V, 0 to + 10V, ± 5V, ± 10V @2mA (Jumper Selectable)
Output Current Range	4 to 20mA Using V/I Converters' Option (RTI-1282 Only)
Differential Nonlinearity	± 1/2LSB
Nonlinearity	± 0.01% of FSR
Gain Error (Adjustable to Zero)	± 0.01%[6]
Offset Error (Adjustable to Zero)	± 0.01%[6]
Output Settling Time	200µs (to ± 1/2LSB) for Full Scale Step Change
Temperature Coefficient	
Gain[3]	± 35ppm/°C of FSR
Offset	± 15ppm/°C of FSR

DIGITAL INPUT/OUTPUT RTI-1287

MNEM		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Voltage (I_{OL} = 20mA)		0.2	0.4	V
I_{OL}	Low Level Current (V_{OL} = + .4V)	20	25		mA
V_{OH}	High Level Voltage (I_{OH} = − 0.118mA)		2.4		V
I_{OH}	High Level Current (V_{OH} = + 2.4V)	− .118			mA
V_{EXT}	Supply Voltage to Module Rack	+ 4.5		+ 30.0	V
I_{EXT}	Supply Current to module rack			500	mA
I_{CC}	Supply Current (V_{CC} = + 5.0V ± 10%)				
	All Outputs ON		40	50	mA
	All Outputs OFF		6	9	mA

I/O CONNECTION	
RTI-1280/1281	3M #3494, 34-Pin IDE
RTI-1282	3M #3429, 26-Pin IDE
RTI-1287	50-Pin, Edge Connector, 0.1" Spacing

INTERFACE PARAMETERS	
Compatibility	STD CMOS Bus (Processor Independent)
Implementation	Memory or I/O Port Mapped
Expansion Option	MEMEX and IOEXP Fully Supported via Jumper Options
Address Selection	Jumper Selectable

POWER REQUIREMENTS[4]	
RTI-1280	
Sleep Mode	270mW typ, 380mW max
Multiple Conversion Mode	440mW typ, 580mW max
RTI-1281	
Sleep Mode	270mW typ, 380mW max
Multiple Conversion Mode	500mW typ, 740mW max
RTI-1282-4	350mW typ, 650mW max[5]
RTI-1282-8	550mW typ, 1.1W max[5]
RTI-1287	30mW (All Outputs OFF) 275mW max (All Outputs ON, V_{CC} = + 5.5V)
Voltage	+ 5V ± 10% (On-Board dc/dc Converter Generates ± 15V to Power Analog Circuit)

ENVIRONMENTAL	
Operating Temperature	− 25°C to + 85°C (− 40°C to + 85°C on RTI-1287)
Storage Temperature	− 55°C to + 85°C
Relative Humidity, Noncondensing	0 to 95%

NOTES
[1]Specified for a single channel with power applied, ± 20V with power off.
[2]Gain ranges above 500 (through user-installed resistor) may be subject to higher differential nonlinearity errors.
[3] ± 25ppm/°C of FSR from 0 to + 85°C.
[4]Maximum power specified at V_{CC} = + 5.5V, output current of 2mA where applicable.
[5]Does not include optional V/I converter (OA08) at 50mW each.
[6]Accuracy at factory calibrated range of ± 10V. Error at 0 to + 5V is ± 0.09 typ which is adjustable to zero.

FSR = Full Scale Range.

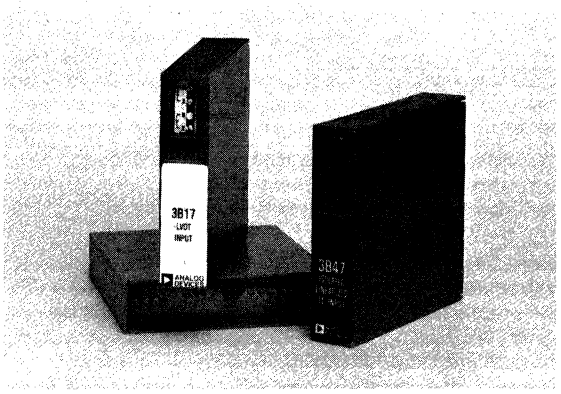
Specifications subject to change without notice.

ANALOG DEVICES

The Complete Signal Conditioning I/O Subsystem

3B Series Update

INPUT MODULE FEATURES
Wide Variety of Sensor Inputs
Thermocouples, RTDs, Strain Gages, AD590/AC2626, LVDTs
Dual High-Level Outputs
Voltage: 0 to +10V or ±10V
Current: 4-20mA/0-20mA (except 3B47)
Mix and Match Capability
Sensor Signals, mV, V, 4-20mA/0-20mA, Frequency
High Accuracy: ±0.1%
Low Drift: ±1μV/°C
Reliable Transformer Isolation:
±1500V CMV, CMR=160dB
Meets IEEE-STD-472: Transient Protection (SWC)
Input Protection: 130V or 220V rms Continuous
Low Cost Per Channel



4

GENERAL DESCRIPTION

The 3B Series Signal Conditioning I/O Subsystem, described on the following page, is continually evolving to meet new and changing signal conditioning needs. Its capabilities have been extended with the introduction of two new input modules: the 3B47 Linearized Thermocouple Conditioner and the 3B17 LVDT Signal Conditioner.

Each input module is a single-channel signal conditioner that plugs into sockets on the backplane and accepts its signal from the input screw terminals. All input modules provide input protection, amplification and filtering of the signal, accuracy of ±0.1%, low drift of 1μV/°C (low-level input modules), and feature two high-level analog outputs that are compatible with most process instrumentation (the 3B47 has only voltage out). The isolated input modules also provide ±1500V isolation.

The choice of a specific module depends on the type of input signal and also whether an isolated or nonisolated interface is required. Input modules are available to accept millivolt, volt, process current, thermocouple, RTD, strain gage, LVDT, and AD590 inputs. The voltage output of each module is available from the voltage I/O connector while the current output (except 3B47) is available on the output screw terminals.

LINEARIZED THERMOCOUPLE INPUT MODULE

The 3B47 accepts its signal from type J, K, T, E, R, S, and B thermocouples and, unlike other 3B modules, provides only a 0 to +10V output. The input signal is internally linearized to provide an output which is linear with temperature. This isolated thermocouple module incorporates cold junction compensation circuitry which provides an accuracy of ±0.5°C over the +5°C to +45°C ambient temperature range. Open thermocouple detection (upscale) is also provided.

LVDT INPUT MODULE

Model 3B17 is a nonisolated, wideband input module that accepts signals from 4-, 5-, or 6-wire LVDT or RVDT transducers. Unlike other 3B modules, all zero and span calibration is accomplished by screwdriver adjustments. Gain can be adjusted on a 256:1 range with a combination of a rotary switch and a potentiometer. Zero suppression is output referred and can provide a ±5V adjustment. The 3B17 provides an ac excitation of 1-5V rms at frequencies ranging from 1kHz to 10kHz.

INPUT MODULE SPECIFICATIONS

Input Types
Thermocouples: J, K, T, E, R, S, B
RTDs: 100Ω Platinum (linearized)
Strain Gage Transducers:
±30mV and ±100mV spans
Solid State Temperature Transducers:
AD590 or AC2626
DC Voltage: ±10mV, ±50mV, ±100mV
±1V, ±5V, ±10V
DC Current: 4 to 20mA, 0 to 20mA

Outputs (Simultaneous)
0 to +10V or ±10V and
4 to 20mA or 0 to 20mA*

Performance
Accuracy: ±0.1% of span
Nonlinearity: ±0.01% of span
Bandwidth: 3Hz (−3dB)

Isolated Modules
Common Mode Voltage,
Input to Output: ±1500V pk continuous
Transient Protection: Meets IEEE-Std 472 (SWC)
Normal Mode Input Protection: 220V rms continuous
Current Output Protection: 130V rms continuous
Common Mode Rejection @ 50Hz or 60Hz: 160dB
Normal Mode Rejection @ 50Hz or 60Hz: 60dB

Nonisolated Modules
Common Mode Voltage: ±6.5V
Normal Mode Input Protection: 130V rms continuous
Current Output Protection: 130V rms continuous
Common Mode Rejection @ 50Hz or 60Hz: 90dB
Normal Mode Rejection @ 50Hz or 60Hz: 60dB

*3B47, 0 to +10V only.
Specifications subject to change without notice.

This two-page data summary contains key specifications to speed your selection of the proper solution for your application. Additional information on this product can be obtained from your local sales office.

3B SERIES SUBSYSTEM FEATURES

Low Cost, Completely Integrated 16-Channel Modular Signal Conditioning Subsystem
Wide Selection of Functionally Complete Input and Output Plug-In Modules,
Rugged Industrial Chassis, Rack or Surface Mounted On-Board Power Supplies Available

Analog Input Modules Available for Direct Interface to a Wide Variety of Signal Sources
Thermocouples, RTDs, Strain Gages, LVDTs
Millivolt and Voltage Sources,
4-20mA/0-20mA Process Current Inputs

Current Output Modules
4-20mA/0-20mA Outputs

Complete Signal Conditioning Function
Input Protection, Filtering, Amplification,
Galvanic Isolation to ±1500V,
Wide-Range Zero Suppression,
High Noise Rejection and RFI/EMI Immunity,
Simultaneous Voltage and Current Outputs

GENERAL DESCRIPTION

The 3B Series Signal Conditioning I/O Subsystem provides a low cost, versatile method of interconnecting real world analog signals to a data acquisition, monitoring or control system. It is designed to interface directly to analog signals such as thermocouple, RTD, Strain Gage, LVDT, or AD590/AC2626 solid state temperature sensor outputs or millivolt or process current signals and convert the inputs to standardized analog outputs compatible with high level analog I/O subsystems.

The 3B Series Subsystem consists of a 19″ relay rack compatible universal mounting backplane and a family of plug in (up to 16 per rack) input and output signal conditioning modules. Eight and four channel backplanes are also available. Each backplane incorporates screw terminals for sensor inputs and current outputs and a connector for high level single ended outputs to the user's equipment.

The input and output modules are offered in both isolated (±1500V peak) and nonisolated versions. The input modules feature complete signal conditioning circuitry optimized for specific sensors or analog signals and provide high level analog outputs. Each input module provides two simultaneous outputs: 0 to 10V (or ±10V) and 4-20mA (or 0-20mA) (the 3B47 has no current output). Output modules accept high level single ended signals and provide an isolated or nonisolated 4-20mA (or 0-20mA) process signal. All modules feature a universal pin-out and may be readily "mixed and matched" and interchanged without disrupting field wiring.

Each backplane contains the provision for a subsystem power supply. The 3B Series Subsystem can operate from a dc/dc converter or ac power supply mounted on each backplane or from externally provided dc power. Two LEDs are used to indicate that power is being applied.

APPLICATIONS

The Analog Devices 3B Series Signal Conditioning Subsystem is designed to provide an easy and convenient solution to signal conditioning problems in measurement and control applications. Some typical uses are in mini- and microcomputer based systems, standard data acquisition systems, programmable controllers, analog recorders, dedicated control systems, and any other applications where monitoring and control of temperature, pressure, flow, and analog signals are required. Since each input module (except the 3B47) features two simultaneous outputs, the voltage output can be used to provide an input to a microprocessor based data acquisition or control system while the current output can be used for analog transmission, operator interface, or an analog backup system.

DESIGN FEATURES AND USER BENEFITS

Ease of Use: Direct sensor interface via screw terminals, standardized high level outputs, factory precalibration of each unit and the modular design make the 3B Series Subsystem extremely easy to use. The subsystem features rugged packaging for the industrial environment and can be easily installed and maintained.

High Protection and Reliability: All field wired terminations offer 130V or 220V rms normal mode protection. To assure connection reliability, gold plated pin and socket connections are used throughout the system. The isolated modules offer protection against high common mode voltages and are designed to meet the IEEE Standard for Transient Voltage Protection (472–1974: SWC).

High Performance: The high quality signal conditioning features ±0.1% calibration accuracy and chopper-based amplification which assures low drift (±1μV/°C) and excellent long term stability. For thermocouple applications, high accuracy cold junction sensing is provided in the backplane on each channel. Low drift sensor excitation is provided for RTD, strain gage, and LVDT models. For RTD models, the input signal is linearized to provide an output which is linear with temperature.

3B SERIES SUBSYSTEM SPECIFICATIONS

OUTPUT MODULES

Input
0 to +10V or ±10V

Output
4 to 20mA or 0 to 20mA

Performance
Accuracy: ±0.1% of span
Nonlinearity: ±0.01% of span

Isolated Module
Common Mode Voltage,
Input to Output: ±1500V pk continuous
Current Output Protection
Transient: Meets IEEE-Std 472 (SWC)
Continuous: 220V rms

Nonisolated Module
Current Output Protection: 130V rms continuous

BACKPLANES

Channel Capacity
3B01: 16 channels
3B02: 8 channels
3B03: 4 channels

POWER SUPPLIES

Backplane Mounted:
100, 115, 220, 240V ac, 50/60Hz
or +24V dc
External Power Option
±15V dc and +24V dc

MECHANICAL

Input or Output Modules:
3.150″ × 0.775″ × 3.395″
(80.0mm × 19.7mm × 86.2mm)
Backplanes:
3B01: 17.40″ × 5.20″ × 4.37″
(442.0mm × 132.1mm × 111.1mm)
3B02: 11.00″ × 5.20″ × 4.37″
(279.4mm × 132.1mm × 111.1mm)
3B03: 7.80″ × 5.20″ × 4.37″
(198.1mm × 132.1mm × 111.1mm)

ENVIRONMENTAL

Temperature Range, Rated Performance:
−25°C to +85°C
Storage Temperature Range:
−55°C to +85°C
Relative Humidity: Conforms to MIL-STD 202, Method 103
RFI Susceptibility: ±0.5% span error, 5W @ 400MHz @ 3 ft.

Specifications subject to change without notice.

Product Families Not in This Databook (But Still Available)

The information published in this Databook is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs or in designs for which they are uniquely suitable. Data sheets on these products are available upon request.

AD108/208/308	ADC1105	RTI-1202	184
AD108A/208A/308A	ADC1109	RTI-1230	230
AD111/211/311	ADC1111	RTI-1231	232
AD351	ADC1133	RTI-1232	233
AD370/371	ADG200	RTI-1240	260
AD502	ADG201	RTI-1241	261
AD511	BDM1615/1616/1617	RTI-1242	272
AD512	DAC-M	RTI-1243	273
AD514	DAC-QG	RTI-1250	275
AD520	DAC-QM	RTI-1251	276
AD523	DAC-QS	RTI-1252	285
AD528	DAC-QZ	SCM1677	288
AD530	DAC-10DF	SDC1604	310
AD531	DAC-10Z	SHA-1A	311
AD540	DAC1009	SHA-2A	424
AD559	DAC1106	SHA-3	426
AD801	DAC1108	SHA-4	428
AD2003	DAC1118	SHA-5	432
AD2008	DAC1125	SHA-1114	433
AD2009	DAC1132	SHA-1134	434
AD2020	DAC1420	THC-0750	435
AD2022	DAC1422	THC-1500	436
AD2023	DAC1423	THS-0060	440
AD2033	DAS1150	THS-0225	441
AD7513	DAS1151	40	450
AD7519	MAS-0801	42	452
AD7527	MAS-1001	43	454
AD7544	MDA-10Z	44	456
AD7555	MDH-0870	45	605
AD7570	MDH-1001	46	606
AD7583	MDH-1202	48	610
ADC-QM	MDS-0815	52	751
ADC-QU	MDS-0815E	105	752
ADC-8S	MDS-1020	118	756
ADC-10Z	MDS-1020E	119	934
ADC-12QZ	MDS-1240	141	942
ADC-14I/17I	MDSL-0825	146	944
ADC-16Q	MDSL-1035	148	946
ADC1100	MDSL-1250	165	947
ADC1102	RTI-1200	180	956
ADC1103	RTI-1201	183	

Substitution Guide for Product Families No Longer Available

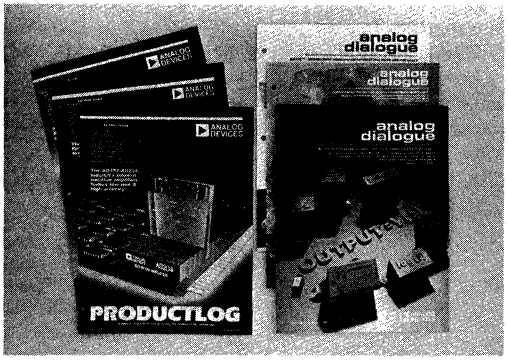
The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but–as a rule–they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, get in touch with Analog Devices.

Model	Closest Recommended Equivalent
AD501	AD511
AD505	AD509
AD508	AD517
AD513	AD503
AD516	AD506
AD550	None
AD551	None
AD553	None
AD555	AD7519
AD810-813	None
AD814-816	None
AD818	None
AD820-822	None
AD830-833	None
AD835-839	None
AD840-842	None
AD5010/6020	AD9000
AD7516	AD7510DI
ADC1121	AD7550
ADM501	ADM501/506
ADP501	ADP511
CAV-1020	MOD-1020
DAC-10H	DAC-10Z
DAC1112	DAC12QS
DAC1122	AD7541
IDC1703	IRDC1730/1731
MDA-LB	None
MDA-LD	None
MDA-UB	None
MDA-UD	None
MDA-8H	MDA-10Z
MDA-10H	MDA-10Z
MDA-11MF	AD7521
MDS-0830	HDS-0820
MDS-0850	HDS-0820
MDS-1040	HDS-1025
MDS-1080	HDS-1025
MDSL-0802	HDS-0820
MDSL-1002	HDS-1025
MDSL-1201	HDS-1250
SERDEX	μMAC-5000
SHA-6	SHA1144
TSDC1608-1611	TSL1612
2N3954	None
2N5900	None
41	AD515
47	48
101 (module)	45
102	48
106	118
107	118
108	52
110	48
111	AD308
114	119
115	43
120	50
142	48
143	52
149	50
153	AD517
161	165
163	165
170	171
220	234
231	233
274J	284J
279	286J
280	281
282J	292A
283J	292A
301 (module)	52
302	310 (module)
350	None
427	424
602J10	AD524
602J100	AD524
602K100	AD524
603	AD524
901	904
907	921
908	921
909	921
931	None
932	None
933	None
935	None
948	947
971	921
AD612	AD524
AD614	AD524

Technical Publications

TECHNICAL PUBLICATIONS

Analog Devices provides a wide array of FREE technical publications. These include Data Sheets for all products; Catalogs; Application Notes and Guides; and four serial publications: *Analog Productlog*, a digest of new-product information, *MCDigest*, a quarterly digest of measurement-and-control system applications, feedback, and information for (and from) system users; *Analog Briefings*, current information about products for military/avionics and the status of reliability at ADI; and *Analog Dialogue*, our technical magazine, with in-depth discussions of products, technologies, and applications.

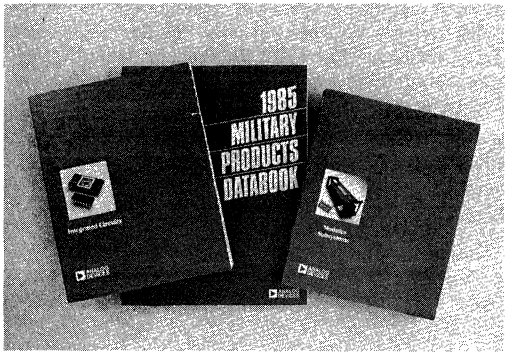


In addition to the free publications, three technical Handbooks, and *Synchro & Resolver Conversion*, are available at reasonable cost. System and subsystem products are supported with hardware, software, and user documentation, at prices related to content.

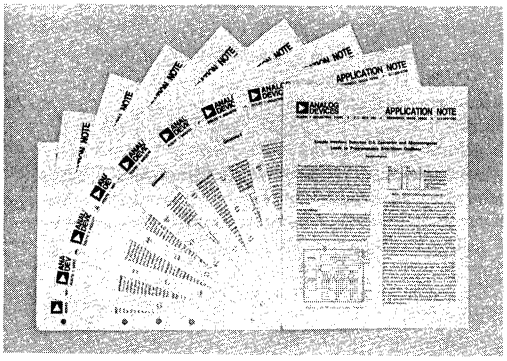
Brief descriptions of typical publications appear below. For copies of any items, to subscribe to any of our free serials, or to request any other publications, please get in touch with Analog Devices or the nearest sales office.

CATALOGS

1984 DATA-ACQUISITION PRODUCTS DATABOOK. Two volumes of data sheets for all Analog Devices ICs, hybrids, modules, and subsystem components recommended for new designs. It alternates with new-product supplement: *1986 UPDATE AND SELECTION GUIDE* (this book).



1985 MILITARY PRODUCTS DATABOOK. 480 pages of information and data on products processed in accordance with MIL-STD-883C Class B.



APPLICATION NOTES AND GUIDES

Application Notes. If a page number is given for an Application Note, it can be found in 1984 Databook, Volume 1. All others are available individually upon request.

	Page
A/D Converters:	
"AD670 8-Bit A/D Converter Applications."	*
"Exploring the AD667 12-Bit Analog Output Port."	*
"The AD7574 Analog-to-Microprocessor Interface."	20-59
"Temperature Measurement System with 10-Bit Resolution Using the AD7571 10-Bit ADC and AD594/595 Thermocouple Amplifiers."	*
Amplifiers:	
"An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change."	20-13
"Applications of High-Performance BIFET Op Amps."	20-73
"A User's Guide to IC Instrumentation Amplifiers."	20-21
"How to Select Operational Amplifiers."	20- 3
"How to Test Basic Operational-Amplifier Parameters."	20- 9
"Low-Cost, Two-Chip Voltage-Controlled Amplifier and Video Switch."	*
D/A Converters:	
"AD7528 Dual 8-Bit CMOS DAC."	20-59
"CMOS D/A Converter Circuits for Single +5-Volt Supplies."	20-69
"CMOS DACs in the Voltage-Switching Mode Can Work from a Single Supply, Including Output Op Amp, for Fast Response, No Offset-Induced Nonlinearity."	20-41
"Gain Error and Tempco of CMOS Multiplying DACs."	20-37
"Interfacing the AD558 DACPORT™ to Microprocessors".	20-31
"Interfacing the AD7549 Dual 12-Bit DAC to the MCS-48 and MCS-51 Microcomputer Families."	*
"Methods for Generating Complex Waveforms and Vectors Using Multiplying D/A Converters."	20-43
"Simple Interface Between D/A Converter and Microcomputer Leads to Programmable Sine-Wave Oscillator."	*

*Available upon request.

(continued)

"The AD7224 DAC Provides Programmable Voltages over Varying Ranges." *
"Three-Phase Sine-Wave Generation Using the AD7226 Quad DAC." *
"Understanding LOGDACs™." 20-65
Good Practice:
"Shielding and Guarding." 20-85
"Understanding Interference-Type Noise." 20-81
Resolver-to-Digital Conversion:
"Dynamic Resolution-Switching on the 1S74 Resolver-to-Digital Converter." *
"Resolver-to-Digital Conversion—A Simple and Cost-Effective Alternative to Optical Shaft Encoders." *
"Why the Velocity Output of the 1S74 and 1S64 Series R/D Converters is Continuous and Step-Free Down to Zero Speed." *
Sample-Holds:
"Applying IC Sample-Hold Amplifiers." *
Switches:
"Behind the Switch Symbol; Use CMOS Analog Switches More Effectively when You Consider Them as Circuits." 20-49
"Generate 4 Channels of Analog Output Using AD7542 12-Bit D/A Converters and Control It All with Only Two Wires." *
V/F Converters:
"Operation and Applications of the AD654 IC V-to-F Converter." *

*Available upon request.

Application Guides Available upon Request

CMOS DAC Application Guide by Phil Burton (1984 – 64 pages). Introduction to CMOS DACs, Inside CMOS DACs, Basic Application Circuits in Current-Steering Mode, Single-Supply Operation Using Voltage-Switching Mode, The Logic Interface, Applications.

RMS-to-DC Conversion Application Guide by Charles Kitchin and Lew Counts (1983 – 46 pages). RMS-DC Conversion: Theory, Basic Design Considerations; RMS Application Circuits; Testing Critical Parameters; Input Buffer Amplifier Requirements; Programs for Computing Errors, Ripple, and Settling Time.

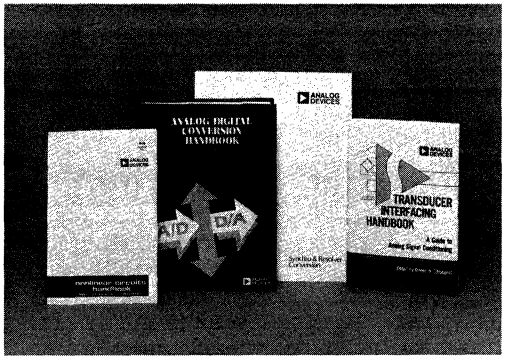
Angular and Linear Data Conversion—A 12-page short-form guide to analog-digital conversion products for synchros, resolvers, and Inductosyns*, in forms ranging from hybrid ICs to instruments and systems.

Applications Guide for Isolation Amplifiers and Signal Conditioners—A 20-page guide to specifications and applications of galvanically isolated amplifiers and signal conditioners for industrial, instrumentation, and medical applications.

A Cookbook to Digital Filtering and Other DSP Applications—A collection of reprints of papers that originally appeared in EDN Magazine during 1983. Topics include: FIR filtering, temporal averaging, multiband filters, IIR filtering, and implementing modern control theory with digital signal processing.

High-Speed Data Conversion—A 12-page short-form guide to video and other high-speed a/d and d/a converters and accessories, in forms ranging from monolithic ICs to card-level products.

*Inductosyn is a registered trademark of Farrand Industries, Inc.



BOOKS—Can be purchased from Analog Devices, Inc.; send check for indicated amount to P.O. Box 796, Norwood MA 02062-0007.

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice-Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices. 325 illustrations. $5.95

SYNCHRO & RESOLVER CONVERSION, edited by Geoff Boyes. Norwood MA: Analog Devices, Inc. (1980). Principles and practice of interfacing synchros, resolvers, and Inductosyns™ to digital and analog circuitry. $11.50

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

Worldwide Service Directory

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For features and comparative specifications of Analog Devices components and subsystems, see Selection Guides and spec tables in Section 2.

For technical data on all new products—introduced since publication of Volumes I and II of the 1984 Databook—see Section 3 of this volume for ICs and Section 4 for Modules & Subsystems.

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