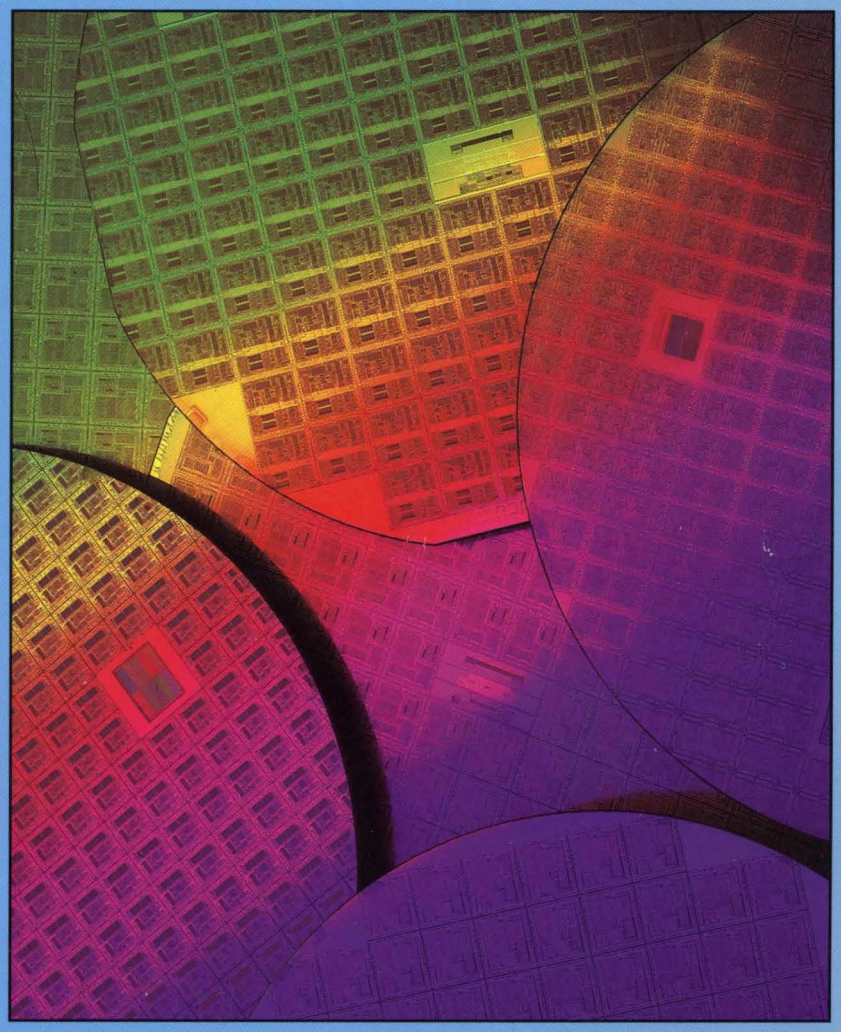
ZILOG

SUPERINTEGRATION

SHORTFORM CATALOG 1992



A complete guide to Zilog's Superintegration™ technology and Support Product solutions

ZILOG

SHORTFORM CATALOG 1992

ZILOG COMPONENTS SHORTFORM

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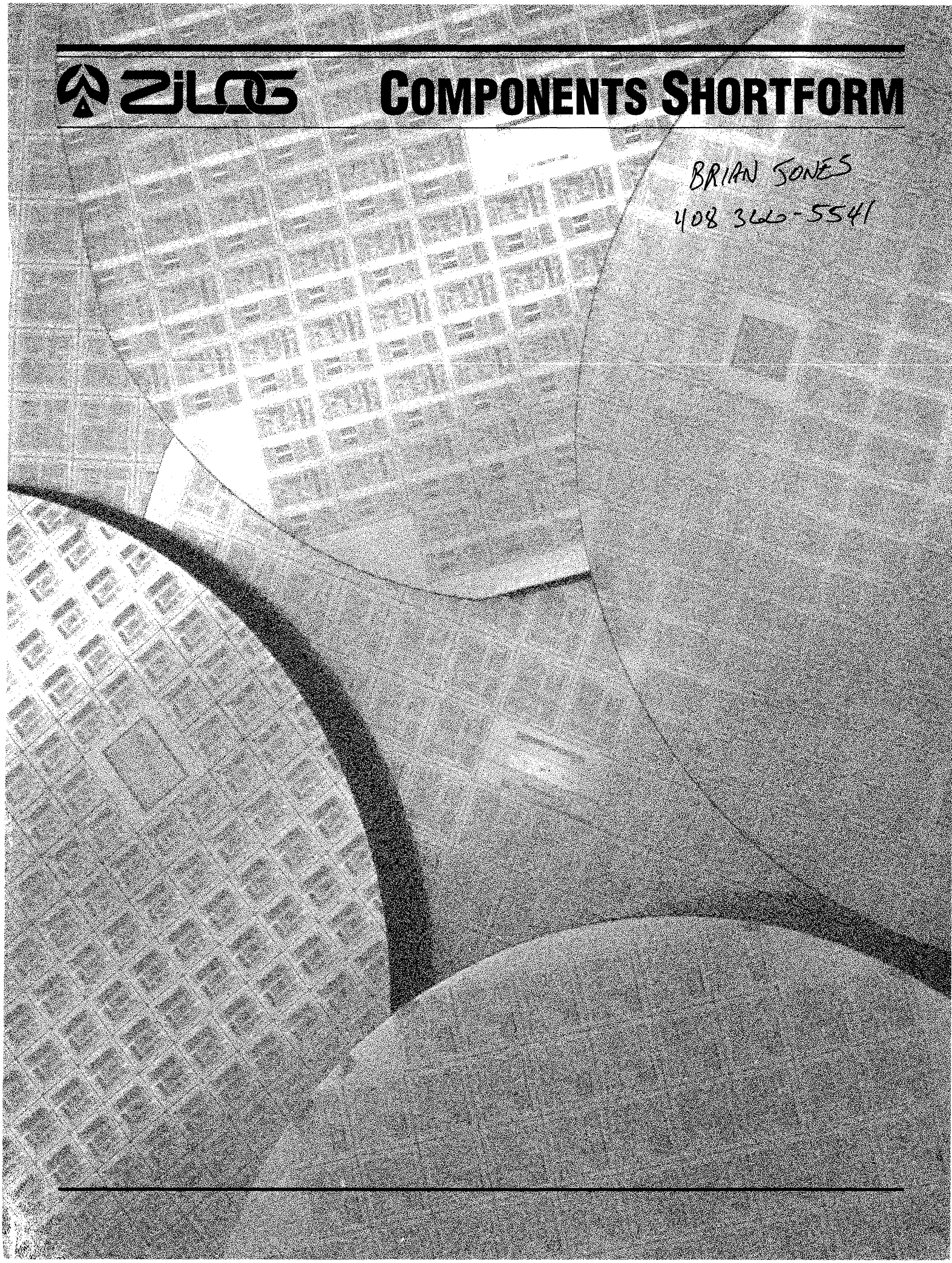
408 370-5541



ZiLOG COMPONENTS SHORTFORM

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Z8® Product Family (Continued)

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ZiLOG COMPONENTS SHORTFORM

Introduction

A pioneer in microprocessor development, Zilog is today a worldwide leader in the development, design and manufacture of Application Specific Standard Products (ASSPs) for datacommunications, computer peripherals, and consumer electronics products. The company's unique building-block design strategy, its in-depth grasp of the customers' industries and needs, and its advanced design and manufacturing capabilities all contribute to creating products with superior reliability, performance and value.

Superintegration™ - The Best of Both Worlds

ASSPs combine the advantages of custom IC design with the affordability and proven performance of "generic" components. Using an extensive library of well-characterized cores and cells as the starting point, Zilog works closely with the customer to gain a thorough understanding of that customer's industry, technology, and specific application requirements. A specialized solution is then created by integrating proven components from the core library. This trademarked process — Superintegration™ — results in a shorter, more efficient design cycle and high product reliability. Customization through software rather than hardware further reduces both short and long-term costs to the customer.

Key Product Families

Zilog's first product offering, the Z80® 8-bit microprocessor, enjoyed widespread use during the 1970s and 80s as a primary component of personal computers. Subsequent products included the Z8® 8-bit microcontroller and the Z8000® 16-bit microprocessor. Today, advanced versions of these standard products form the cornerstone of many Superintegration designs, bringing Zilog's expertise to both established and emerging technologies.

The Datacommunications/Networking arena, where Zilog's serial controllers hold a leadership position, is a key business area for the company. The industry-standard SCC (Serial Communications Controller) and the recently introduced USC™ (Universal Serial Controller) product families offer features which include on-chip DMA, DPLL, deeper FIFOs, and Time Slot Assigners. Zilog is also setting a new standard in high-performance LAN and WAN markets with data throughput of 20 Mbits/sec and a bus bandwidth of 18 Mbytes/sec.

Zilog products for Computer Peripherals include disk drive controllers and digital signal processors, and are used by major manufacturers of disk drives, keyboards, mice and modems. The company's Z86C95 and Z86018 chipset provides the industry's most optimal price-vs.-performance tradeoff, particularly for small form factor drives.

Consumer Electronics, particularly in the entertainment and communications areas, is another rapid growth market for Zilog. The company's closed-captioning controllers for television receivers (a component which will be required in virtually all U.S.-market sets by mid-1993) are the first to be approved for home use by the FCC, and initial production orders for several major manufacturers are now underway. Similarly, Zilog's controllers and digital signal processors for telephone answering machines/devices (TADs) dramatically reduce the costs of these instruments and set the stage for making voice-mail features available to a consumer audience at a minimal cost. Automotive, security and video applications are also areas which have benefitted from Zilog's high-performance solutions.

Quality, Support and Service

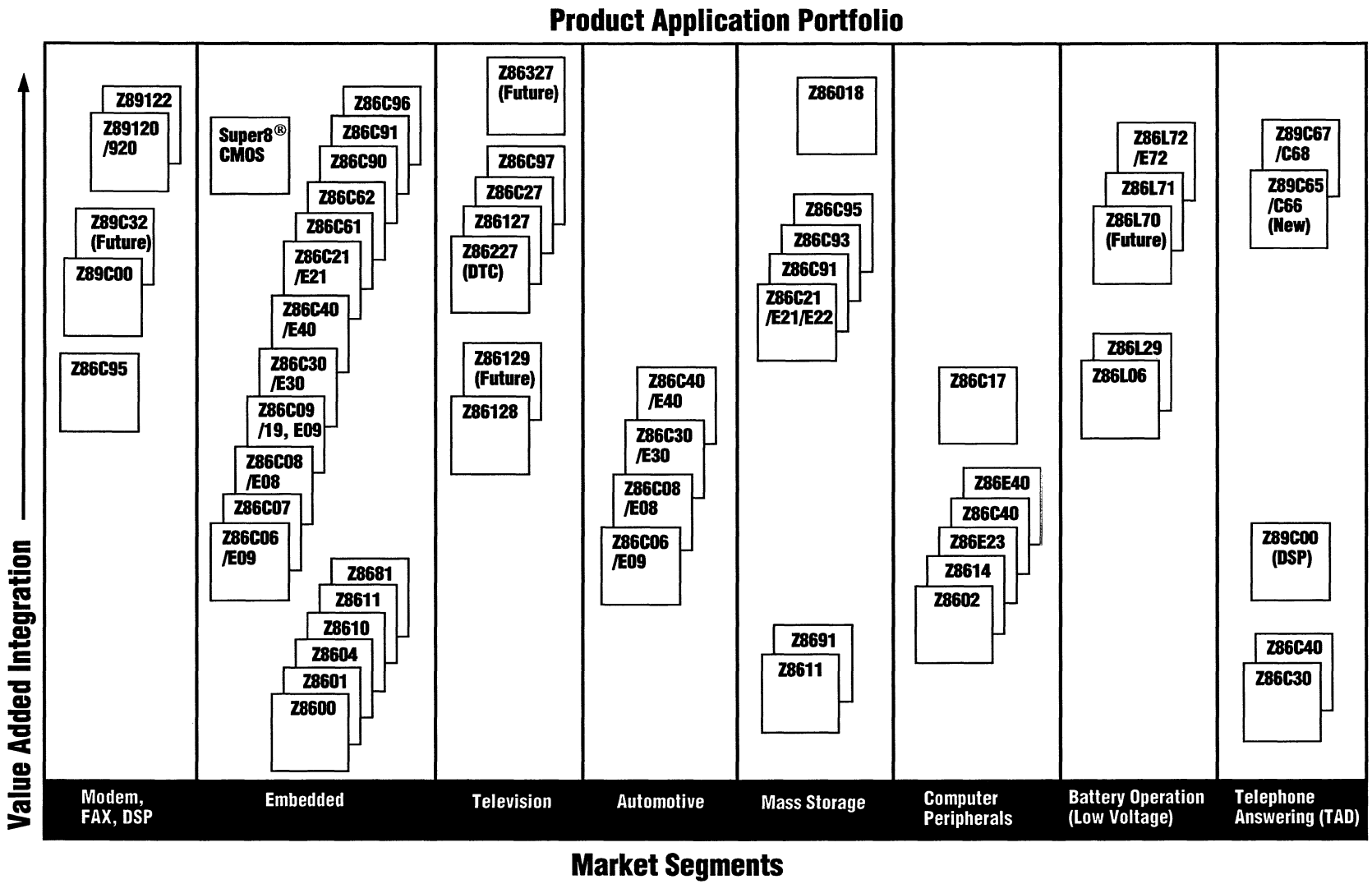
In contrast to many commodity IC sources, Zilog's support and service begin — not end — with the completed ASSP device. Zilog maintains a proactive relationship with the customer throughout the prototype phase, in many cases providing lab facilities for prototype systems. Technical centers throughout the U.S. are available for ongoing product support, as is a complete technical customer service staff based at Zilog headquarters in Campbell, California. And the company's twice-yearly "Quality and Reliability Report," publicly distributed to customers and industry analysts alike, exhaustively documents the latest test results of all Zilog devices and showcases the Zilog commitment to producing the highest quality products possible.

Rapid advances in technology mean that on-time deliveries are more critical than ever. Zilog's pledge of timely follow-through on orders is backed by the firm's state-of-the-art manufacturing facilities in Nampa, Idaho; Manila, the Philippines; Bangkok, Thailand; and Batam, Indonesia. Worldwide sales offices and distributors supplement these resources on a local basis, and actively work to ensure not just prompt delivery, but the best possible service before, during and after the order.

Intelligent design, customer partnership, and a dedication to quality and service: all part of "Doing it Right" at Zilog.

Z8® MICROCONTROLLER PRODUCT FAMILY

COMPONENTS SHORTFORM



MICROCONTROLLERS REFERENCE CHART COMPONENTS SHORTFORM

Product	Pin Count	ROM (Kbyte)	I/O	Interrupts	UARTS	Comparators	CTCs	WDT	Package Type	Speed (MHz)	Temp	Low Noise
CMOS												
Z86C00 MCU	28	2	22	3	-	-	2	-	DIP	8,12	S,E	-
Z86C06 MCU	18	1	14	6	-	2	2	X	DIP,SOIC†1	4*,12	S,E	X
Z86L06	18	1	14	6	-	2	2	X	DIP,SOIC†1	8	S	-
Z86C07	18	8	14	6	-	2	2	X	DIP	8,12	S	X
Z86C08 MCU	18	2	14	6	-	2	2	X	DIP,SOIC†1	4*,12	S,E	X
Z86E08 MCU	18	2 (OTP)	14	6	-	2	2	X	DIP	4*,12	S	X
Z86C09/19	18	2/4	14	6	-	2	2	X	DIP,SOIC†1	4*,12	S,E	-
Z86C10 MCU	28	4	22	3	-	-	2	-	DIP	8,12	S,E	-
Z86C11 MCU	40,44	4	32	6	1	-	2	-	QFP,DIP,PLCC	12,16	S,E	-
Z86C12 ICE	84	-	16	6	1	-	2	-	PGA	16	S	-
Z86C17	18	2	14	6	1	2	2	1	DIP,SOIC	4	5	X
Z86E09 MCU†1	18	2 (OTP)	14	6	-	2	2	X	DIP	12	S	X
Z86L29	18	6	14	6	-	2	2	X	DIP,SOIC†1	8	S	-
Z86C20 MCU	28	8	22	3	-	-	2	-	DIP	12	S	X
Z86C21 MCU	40,44	8	32	6	1	-	2	-	QFP,DIP,PLCC	4*,12,16	S,E	X
Z86E21/E22* MCU	40,44	8 (OTP)	32	6	1	-	2	-	QFP,DIP,PLCC	4*,12,16	S,E	X
Z86E23	40	4	32	6	1	-	2	-	DIP	4*	S	X*
Z86C91 MCU	40,44	-	16	6	1	-	2	-	QFP,DIP,PLCC	12,16,20	S,E	-
Z86C30 MCU	28	4	24	6	-	2	2	X	DIP	4*,12	S,E	X
Z86E30 MCU	28	4 (OTP)	24	6	-	2	2	X	DIP	12	S	X
Z86C40 MCU	40,44	4	32	6	-	2	2	X	QFP,DIP,PLCC	4*,12	S,E	X
Z86E40 MCU	40,44	4 (OTP)	32	6	-	2	2	X	QFP,DIP,PLCC	12	S	X
Z86C50 ICE	124	-	16	6	-	2	2	X	PGA	20	S	-
Z86C61 MCU†1	40,44	16	32	6	1	-	2	-	QFP,DIP,PLCC	16	S,E,	-
Z86C62 MCU†1	64,68	16	52	6	1	-	2	-	DIP,PLCC	16	S,E	-
Z86C89*†3/90 MCU	40,44	-	16	6	-	2	2	X	QFP,DIP,PLCC	4*,8,12	S,E	X
Z86C27 TV Controller	64	8	43	6	-	-	2	X	DIP	4	S	X
Z86127	64	8	35	6	-	-	2	X	DIP	4*	S	X
Z86227	40	6	24	6	-	-	2	X	DIP	4*	S	X
Z86C93 MCU	40,44	-	16	6	1	-	3	-	QFP,PLCC,DIP	20	S,E	-
Z86C95	80,89,100	ROMless	16	6	1	2	3	-	VQFP.QFP,PLCC	24	S	-
Z86C96 MCU†1	64,68	-	44	6	1	-	2	-	DIP,PLCC	20	S,E	-
Z86C97 TV Controller	64	-	16	6	-	-	2	X	DIP	4	S	X

Product	Pin Count	ROM (Kbyte)	I/O	Interrupts	UARTS	Comparators	CTCs	WDT	Package Type	Speed (MHz)	Temp	Low Noise
CMOS (Continued)												
Z88C00 Super8†1	48,68	-	24	27	1	-	2	-	DIP,PLCC	25	S	-
Z89C00	68	4KWord	16	3	-	-	-	-	PLCC	10	S	-
Z89C65	68	24	47	6	-	2	2	X	PLCC	20	S	-
Z89C66	68	ROMless	31	6	-	2	2	X	PLCC	20	S	-
Z89C67	84	24	43	6	-	2	2	X	PLCC	20	S	-
Z86C68	84	ROMless	27	6	-	2	2	X	PLCC	20	S	-
Z89120	68	24	47	6	-	2	2	X	PLCC	20	S	-
Z89920	68	ROMless	31	6	-	2	2	X	PLCC	20	S	-
NMOS												
Z8600 MCU	28	2	22	3	-	-	2	-	DIP	8	S,E	-
Z8601 MCU	40,44	2	32	6	1	-	2	-	DIP,PLCC	8	S,E	-
Z8602 MCU	40	2	32	6	-	-	2	-	DIP	4	S,E	X
Z8603 PROTOPACK	40	2	32	6	1	-	2	-	DIP	8,12	S	-
Z8604 MCU	18	1	14	5	-	-	2	X	DIP	8	S	-
Z8610 MCU	28	4	22	3	-	-	2	-	DIP	8,12	S,E	-
Z8611 MCU†2	40,44	4	32	6	1	-	2	-	DIP,PLCC	8,12.5	S,E,M	-
Z8681 MCU†2	40,44	-	16	6	1	-	2	-	DIP,PLCC	8,12	S,E,M	-
Z8691 MCU	40,44	-	16	6	1	-	2	-	DIP,PLCC	8,12	S,E	-
Z8612 ICE	64,68	4	32	6	1	-	2	-	PLCC,Ceramic	12	S	-
Z8613 PROTOPACK	40	4	32	6	1	-	2	-	DIP	8,12	S	-
Z8614	40	4	32	6	1	-	2	-	DIP,PLCC	4*	S	X*

Notes:
* Low EMI version
†1 Estimate Release Q4/92
†2 Available in Military version
†3 RC Oscillator Option
X = Yes, feature available.

Temperature Range:
S = Standard 0°C to +70°C
E = Extended -40°C to +105°C
M = Military -55°C to +125°C

COMPONENTS SHORTFORM

APPLICATIONS BOARDS
TOOL BOX Family

EMULATORS
ICEBOX™ Family

Part Number	Application Kits					Adapter Kits												C Series		S Series	
	Z08600ZCO	Z08600ZDP	Z08602ZCO	Z86C0800ZCO	Z86C1900ZCO	Z08602ZDP	Z86C0800ZDP	Z86E0600ZDP	Z86E2100ZDP	Z86E2100ZDV	Z86E2100ZDF	Z86E2101ZDV	Z86E2101ZDF	Z86E2300ZDP	Z86E2301ZDP	Z86E2300ZDV	Z86E2301ZDV	Z86C0800ZEM	Z86C1900ZEM	Z86C1200ZEM	Z86C5000ZEM	Z86C1200ZPD▲	Z86C5000ZPD▲
Z08600	●	●																●[1]		●[1]	
Z08601	●																	●[1]		●[1]	
Z08602			●			●												●[1]		●[1]	
Z08604							●[3]										●[3]	●[1]		●[1]	
Z08611	●																	●[1]		●[1]	
Z08614			●			●												●[1]		●[1]	
Z86C06/L06							●												●		●[3]
Z86C07/C08				●			●										●	●		●[2]	
Z06E08				●			●										●	●		●[2]	
Z86C09					●		●										●		●		●
Z86C19/L29					●		●										●		●		●
Z86C21	●																	●		●	
Z86E21/E22	●							●	●	●	●	●						●		●	
Z86E23			●										●	●	●	●		●[1]		●[1]	
Z86C00/10/20	●	●																●		●	
Z86C11	●																	●		●	

Notes:
1 Functional Emulation
2 Z86C0800ZDP Required
3 Excluding SPI
▲ Z86C0000ZUSP Required

COMPONENTS SHORTFORM

APPLICATIONS BOARDS
TOOL BOX Family

EMULATORS
ICE BOX™ Family

Part Number	Application Kits								Adapter Kits				C Series										S Series			
	Z08600002CO	Z86C2700ZCO	Z86C9500ZCO	Z89C0000ZCO	Z86E3000ZDP	Z86E4000ZDP	Z86E4000ZDV	Z86E4000ZDF	Z86E4001ZDV	Z86E4001ZDF	Z86C1900ZEM	Z86C1200ZEM	Z86C5000ZEM	Z86C9300ZEM	Z86C2700ZEM	Z86C2700ZDB	Z86C2702ZEM	Z86C6200ZEM	Z89C0000ZEM	Z89C6500ZEM	Z89C6700ZEM	Z89C6500ZDB	Z89C6700ZDB	Z86C1200ZPD▲	Z86C5000ZPD▲	Z86C9300ZPD▲	Z86C9500ZPD*
Z86C27		●												●	●	●											
Z86127		●												●	●	●											
Z86227		●												●	●	●											
Z86C96																	●										
Z86C97		●												●	●	●											
Z86C30/E30					●								●											●			
Z86C40/E40						●	●	●	●	●			●											●			
Z86C61	●[1]											●					●						●				
Z86C62																	●										
Z86C89										●			●[1]											●[1]			
Z86C90										●			●											●			
Z86C91	●											●											●				
Z86C93	●													●											●		
Z86C95			●																							●	
Z89C00				●														●									
Z89C65																			●		●						
Z89C66																			●		●						
Z89C67																				●		●					
Z89C68																				●		●					
Z89120																			●								
Z89920																			●								

Notes:
1 Functional Emulation
* Z89C9500ZUSP Required
▲ Z86C0000ZUSP Required

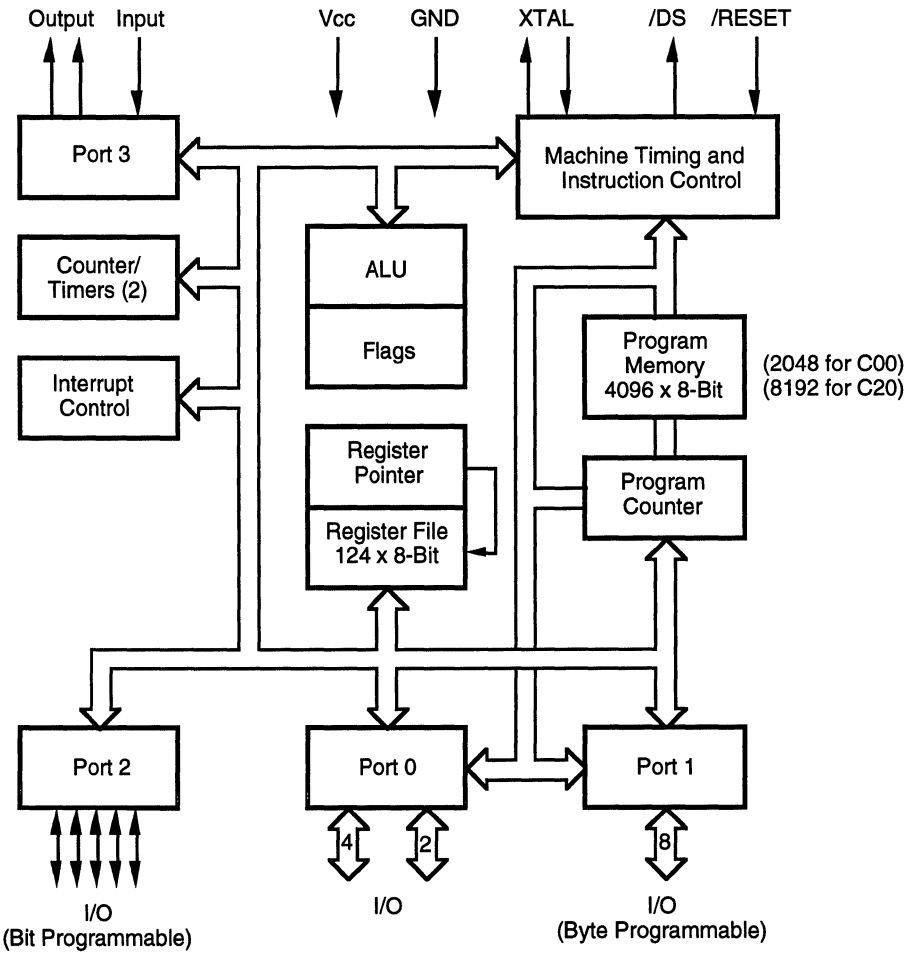
Z8® CMOS MICROCONTROLLERS

GENERAL DESCRIPTION

Z86C00/C10/C20 microcontrollers introduce a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcontrollers, the 86C10/C20 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output, bit manipulation capabilities, and easier system expansion.

FEATURES

- *Complete Microcontroller, 2K (86C00), 4K (86C10), or 8K (86C20), Bytes of ROM, and 22 I/O Lines in a 28-Pin DIP*
- *142-Byte (Z86C00, Z86C10) and 256-Byte (Z86C20) Register File, Including 124-Byte (Z86C00, Z86C10) and 236-Byte (Z86C20) General-Purpose Registers, Four I/O Port Registers, and 14 Status and Control Registers.*
- *Average Instruction Execution Time of 1.5 µs, Minimum of 1 µs*
- *Vectored, Priority Interrupts for I/O and Counter/Timers*
- *Two Programmable 8-Bit Counter/Timers, Each with a 6-bit Programmable Prescaler.*
- *Register Pointer So That Short, Fast Instructions Can Access Any of Nine Working-Register Groups in 1.0 µs.*
- *On-Chip Oscillator Which Accepts Crystal, Ceramic Resonator or External Clock Drive.*
- *Single +5V Power Supply, All Pins TTL Compatible*
- *Clock Speed 12 MHz*



Z86C06 CMOS Z8 CONSUMER CONTROLLER PROCESSOR

GENERAL DESCRIPTION

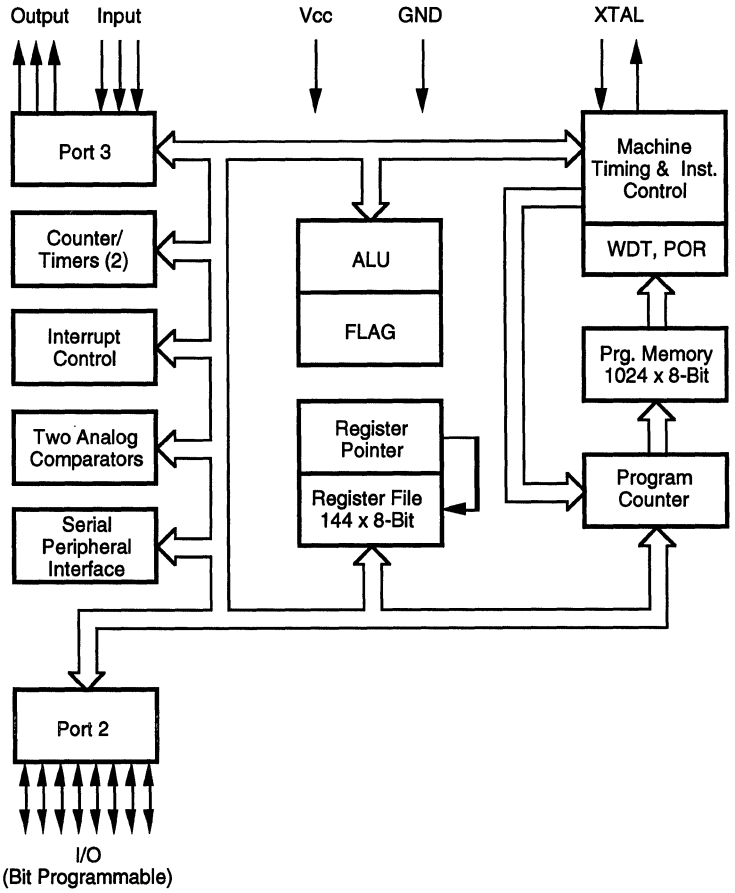
The Z86C06 is a member of the Z8® single-chip microcontroller family with 1 Kbytes of ROM and 124 bytes of RAM. The device is housed in an 18-pin DIP. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C06 architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many consumer, industrial, and automotive applications.

With powerful peripheral features such as on-board comparators, counter/timers, watch dog timer, and serial peripheral interface, the Z86C06 meets the needs of most sophisticated controller applications.

FEATURES

- *8-Bit CMOS Microcontroller, 18-Pin DIP; 18-Pin SOIC Available Q3/91.*
- *Low Cost*
- *3.0 to 5.5 Volt Operating Range*
- *Low Power Consumption*
- *Serial Peripheral Interface with Compare Feature*
- *Clock Speeds: 4 and 12 MHz*
- *"Brown-Out" Protection*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *Six Vectored, Priority Interrupts From Six Different Sources*
- *On-chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.*
- *14 Input/Output Lines*
- *Low EMI Noise Mode*
- *Schmitt-Triggered CMOS Inputs*
- *1K ROM*
- *124 Bytes of RAM*
- *Standby Modes: STOP and HALT*



GENERAL DESCRIPTION

The Z86L06 low voltage CCP™ (Consumer Controller Processor) is a member of the Z8® single-chip microcontroller family with 1 Kbyte of ROM, and 124 bytes of general-purpose RAM. The device is housed in an 18-pin DIP package, and is manufactured in low voltage CMOS technology. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. Now with the low voltage process this same processor may operate down to 2.0 volts.

The Z86L06 architecture is based on Zilog's 8-bit microcontroller core with the addition of an Expanded Register File which allows access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many consumer, industrial, and automotive applications.

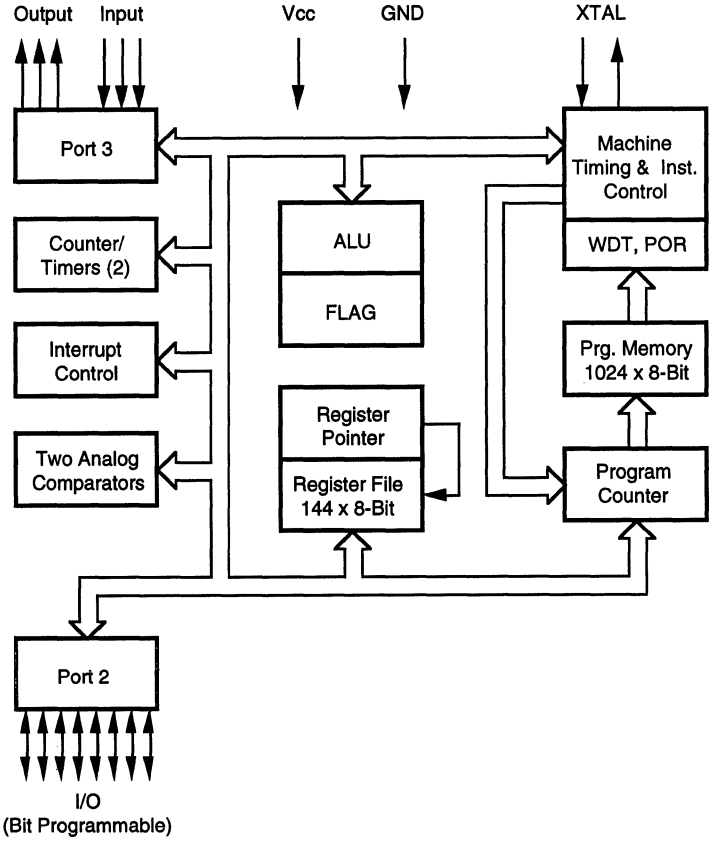
The device applications demand powerful I/O capabilities. The CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 124 bytes of general-purpose registers, two I/O port registers and fifteen control and status registers. The Expanded Register File consists of three control registers.

With powerful peripheral features such as on-board comparators, counter/timers, watch-dog timer, and serial peripheral interface, the Z86L06 meets the needs for most sophisticated controller applications.

FEATURES

- *8-Bit CMOS Microcontroller*
- *18-Pin DIP Package*
- *Low Cost*
- *2.0 to 3.6 Volt Operating Range*
- *Two Standby Modes - STOP and HALT*
- *14 Input/Output Lines (Two with Comparator Inputs)*
- *1 Kbyte of ROM*
- *124 Bytes of RAM*
- *Four Expanded Registers (File Control Registers)*
- *Two Programmable 8-Bit Counter/Timers*
- *High Current Output: (1)-7 ma Source at 2 Volts, (1)-10 ma Sink at 2 Volts.*
- *6-Bit Programmable Prescaler*
- *Six Vectored, Priority Interrupts From Five Different Sources*
- *Clock Speed: 8 MHz @ 2.0V*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.*
- *Low EMI Noise Mode*
- *From 0° C to +70° C Operation*
- *Brown-Out Protection*
- *Auto Latches*



Z86C07 CMOS Z8® MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C07 Microcontroller Unit (MCU) introduces a new level of sophistication to single-chip architecture. The Z86C07 is a member of the Z8 single-chip microcomputer family with 2 Kbytes of ROM and 124 bytes of general- purpose RAM. The device is housed in an 18-pin DIP, or an 18-pin SOIC, and is manufactured in CMOS technology. The Zilog Z86C07 offers all the outstanding features of the Z8 family architecture, and easy software/hardware system expansion along with low cost, low power consumption.

The Z86C07 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, industrial and automotive applications.

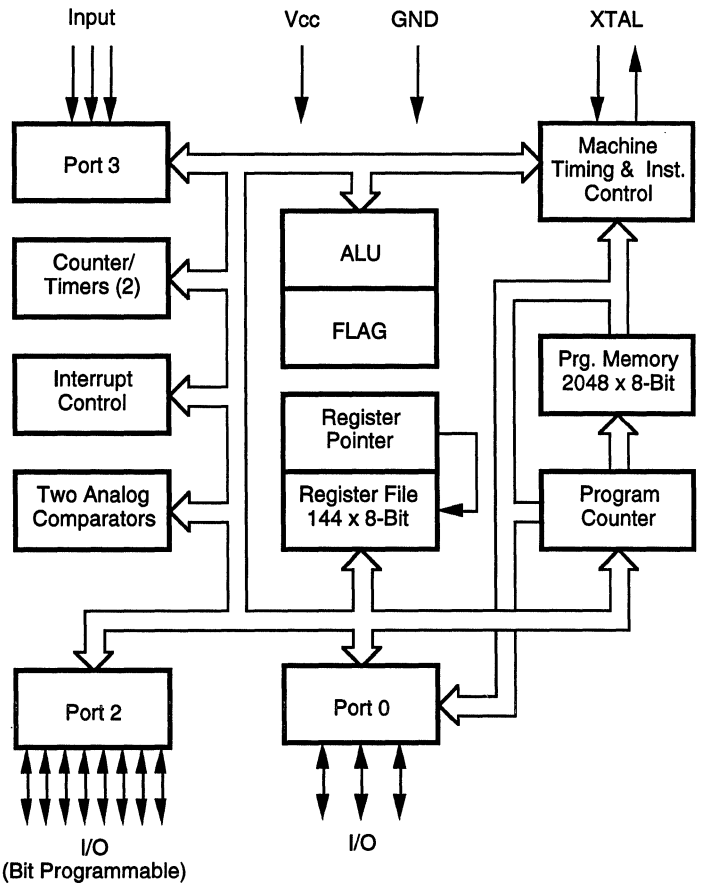
The device applications demand powerful I/O capabilities. The Z86C07 fulfills this with 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals. Please note that any inputs not being used must be connected to V_{CC} or GND.

There are two basic address spaces available to support this wide range of configurations, Program Memory, and 124 bytes of general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86C07 offers two on-chip counter/timers with a large number of user selectable modes. Also, there are two on-board comparators that can process analog signals with a common reference voltage.

FEATURES

- *8-Bit CMOS Microcomputer, 18-Pin DIP; 18-Pin SOIC Available Q3/91.*
- *Low EMI Noise Programmable*
- *3.0 to 5.5 Volts Operating Range*
- *Low Power Consumption - 50 mW (Typical)*
- *"Brown-Out" Protection*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Two Standby Modes - STOP and HALT*
- *Fourteen Input/Output Lines*
- *All Digital Inputs Are CMOS Levels and Schmitt Triggered*
- *2 Kbytes of ROM*
- *124 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers Each with a 6-bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts From Six Different Sources*
- *Clock Speed: 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *On-Chip Oscillator That Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.*



GENERAL DESCRIPTION

The Z86C08 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C08 is a member of the Z8® single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. The device is housed in a 18-pin DIP, and is manufactured in CMOS technology. The Zilog Z86C08 offers all the outstanding features of the Z8 family architecture, and easy software/hardware system expansions along with low cost, low power consumption.

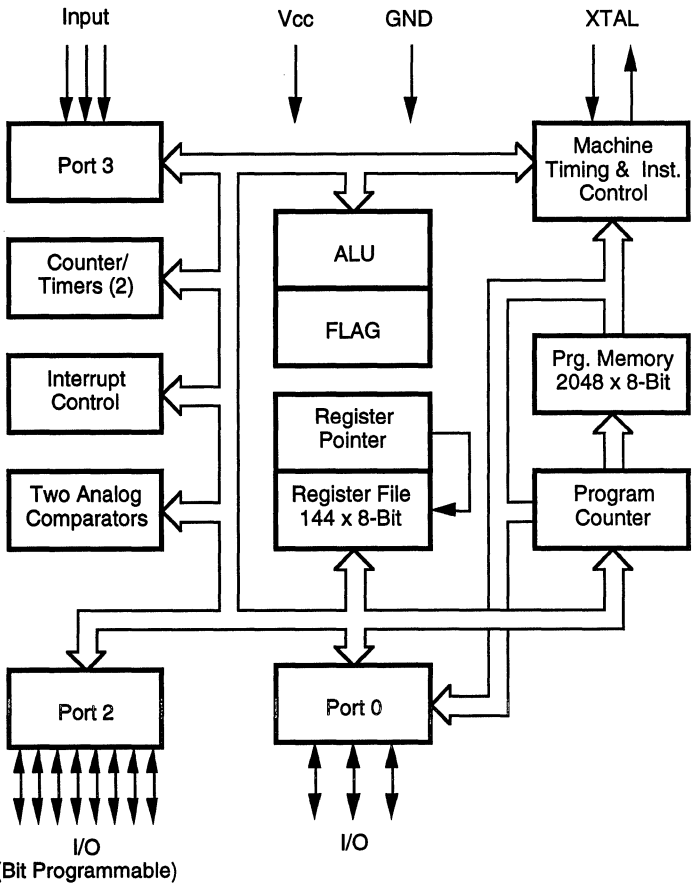
The Z86C08 has 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86C08 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators that can process analog signals with a common reference voltage.

For an OTP version of this device see the Z86E08.

FEATURES

- *8-Bit CMOS Microcomputer, 18-Pin DIP; 18-Pin SOIC Available Q3/91.*
- *Low EMI Noise Programmable*
- *3.0 to 5.5 Volts Operating Range*
- *Low Power Consumption - 50 mW (Typical)*
- *"Brown-Out" Protection*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Two Standby Modes - STOP and HALT*
- *Fourteen Input/Output Lines*
- *All Digital Inputs Are CMOS Levels and Schmitt Triggered with auto latches*
- *2 Kbytes of ROM*
- *124 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers Each with a 6-bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts From Six Different Sources*
- *Clock Speed: 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *On-Chip Oscillator That Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.*



Z86C09/Z86C19 CMOS Z8 CONSUMER CONTROLLER PROCESSOR

GENERAL DESCRIPTION

The Z86C09 and Z86C19 Consumer Controller Processors (CCP™) introduce a new level of sophistication to single-chip architecture. The Z86C09 and Z86C19 are members of the Z8® single-chip microcontroller family with 2 and 4 Kbytes of ROM, respectively, and 124 bytes of general purpose RAM. The devices are housed in a 18-pin DIP. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

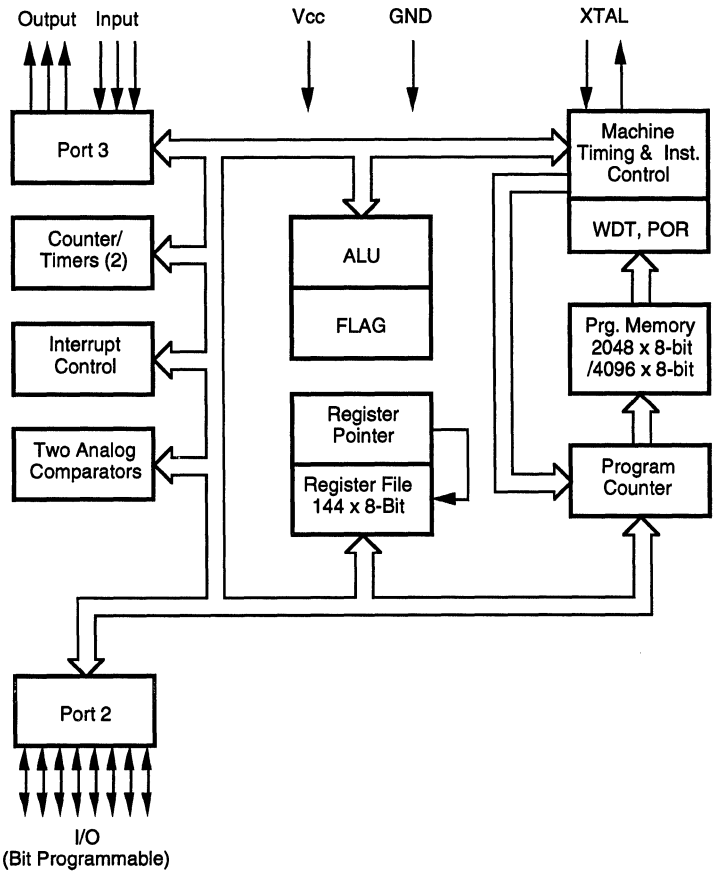
The CCP offers a flexible I/O architecture, and a number of ancillary features that are useful in many industrial, automotive, and consumer applications.

To unburden the program from coping with real-time problems such as counting/timing and input/output data communication, the Z86C09/C19 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators that can process analog signals with a common reference voltage.

Zilog's Z86E09 is the OTP version of these parts.

FEATURES

- *8-Bit CMOS Microcomputer, 18-Pin DIP; 18-Pin SOIC Available Q3/91.*
- *Low Cost*
- *3.0 to 5.5 Volt Operating Range*
- *Low Power Consumption - 50 mW (Typical)*
- *Fast Instruction Pointer, 1.0 µs at 12 MHz*
- *Standby Modes: STOP and HALT*
- *14 Input/Output Lines (2 with Comparator Inputs)*
- *All Digital Inputs Are CMOS Levels and Schmitt Triggered*
- *2K, 4 Kbytes of ROM, Z86C09, Z86C19, Respectively*
- *124 Bytes of RAM*
- *Two Expanded Register File Control Registers*
- *Two Programmable 8-Bit Counter/Timers*
- *6-Bit Programmable Prescaler*
- *Six Vectored, Priority Interrupts From Five Different Sources*
- *Clock Speed: 12 MHz*
- *Brown-Out Protection*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *On-chip Oscillator That Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.*



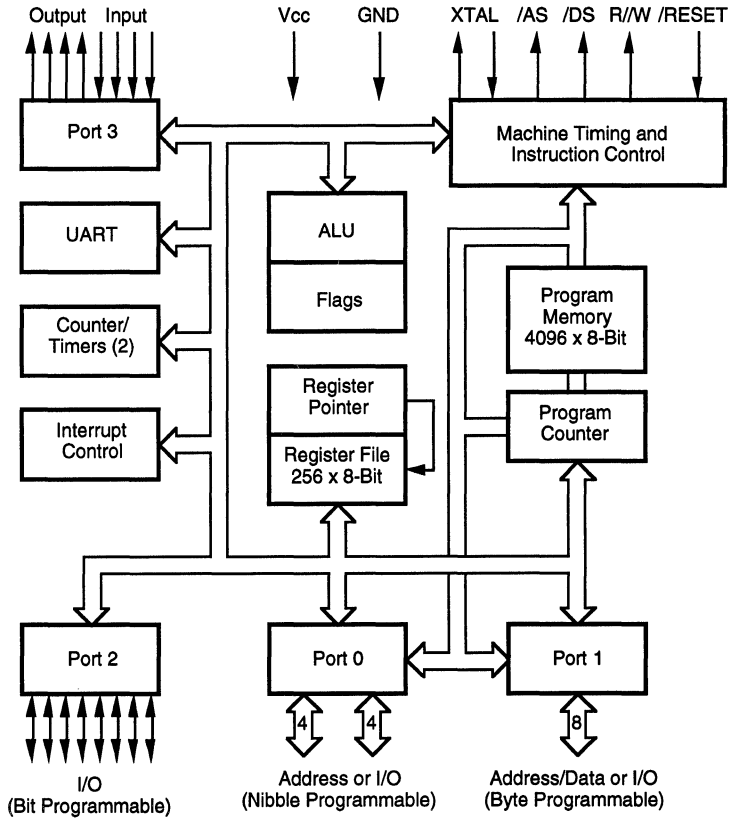
GENERAL DESCRIPTION

The Z86C11 microcontroller introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcontrollers, the Z86C11 offers faster execution, efficient use of memory, sophisticated interrupt, input/output, bit manipulation capabilities and easier system expansion.

Under program control, the Z86C11 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 4 Kbytes of internal ROM, a traditional microprocessor that manages up to 120 Kbytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-Bus®. In all configurations, a large number of pins remain available for I/O.

FEATURES

- *Complete Microcontroller, 4 KBytes of ROM, 236 Bytes of RAM, 32 I/O Lines, and Up to 60 Kbytes Addressable External Space Each For Program and Data Memory*
- *256-Byte Register File, Including 236 General-Purpose Registers, 4 I/O Port Registers, and 16 Status and Control Registers*
- *Vectored, Priority Interrupts For I/O, Counter/Timers, and UART*
- *Full-Duplex UART and Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler*
- *Register Pointer so that Short, Fast Instructions can Access any of 16 Working-Register Groups in 0.6 µs*
- *On-Chip Oscillator which Accepts Crystal or Ceramic Resonator, or External Clock Drive*
- *Standby Modes: HALT and STOP*
- *Single +5V Power Supply, all Pins TTL Compatible*
- *Clock Speeds: 12 and 16 MHz*



Z86C17 CMOS 2K MOUSE CONTROLLER

GENERAL DESCRIPTION

The Z86C17 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86C17 is a member of the Z8® single-chip microcontroller family with 2 Kbytes of ROM and 124 bytes of general-purpose RAM. The device is housed in an 18-pin DIP or SOIC package and is manufactured in CMOS technology. The Z86C17 offers all the outstanding features of Zilog's Z8 family architecture, and easy software/hardware system expansion along with low cost, low power consumption.

The Z86C17 is characterized by a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that make it ideal for use in computer mice and other consumer applications.

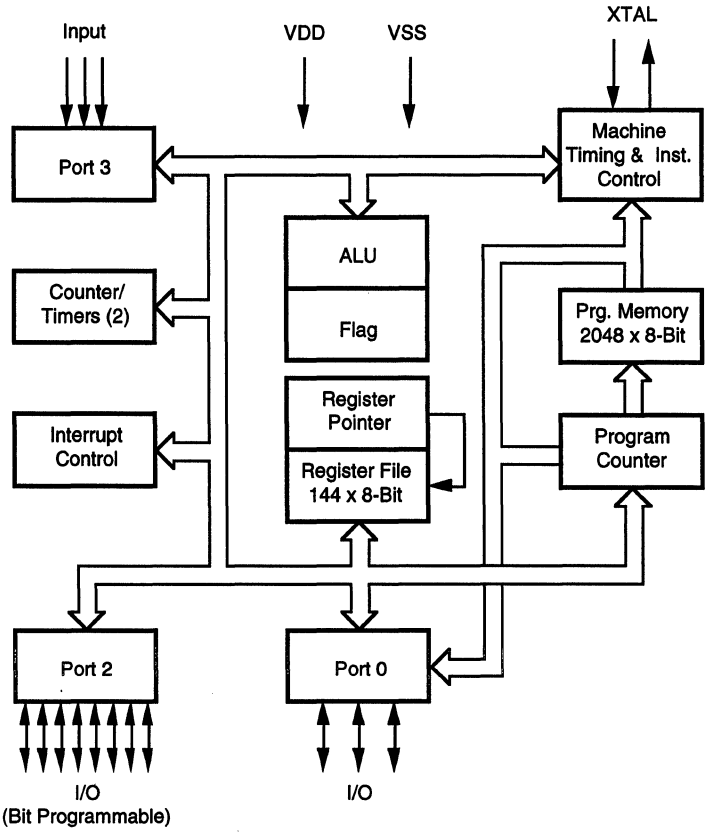
The device applications demand powerful I/O capabilities. The Z86C17 fulfills this with 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing, and status signals.

There are two basic address spaces available to support this wide range of configurations, Program Memory, and 124 bytes of general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86C17 offers two on-chip counter/timers with a large number of user selectable modes.

FEATURES

- *8-Bit CMOS Microcontroller*
- *18-Pin DIP and SOIC Package*
- *Low Cost*
- *3.0 to 5.5 Volt V_{DD} Range*
- *Low Power Consumption; 33 mW (max.)*
- *Brown-Out Protection*
- *Fast Instruction Pointer; 1.5 µs at 4 MHz*
- *Two Standby Modes - STOP and HALT*
- *14 Input/Output Lines*
- *Digital Inputs at CMOS Levels; Schmitt-Triggered*
- *2 Kbytes of ROM*
- *124 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers Each with a 6-bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Five Different Sources*
- *Clock Speed 4 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Less Than 2 mA Consumed During HALT Mode*
- *On-Chip Oscillator That Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.*
- *Low EMI Emission.*
- *Two User Selectable Mask Options.*



GENERAL DESCRIPTION

The Z86C21 is a single chip microcontroller with 8 Kbytes of ROM. It offers all the outstanding features of the Z8® family architecture.

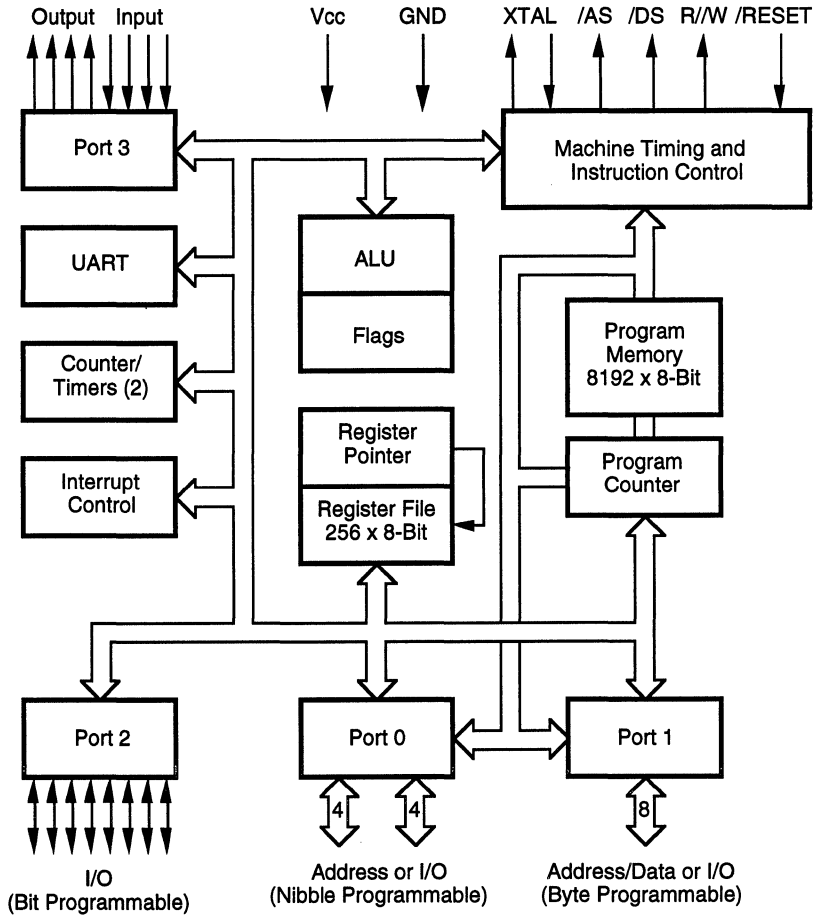
Z86C21 offers a low noise version which results in a 10 dB lower emitted radiation than the standard part.

The Z86C21 architecture is based on Zilog's 8-bit microcontroller core. The device has instruction compatibility with the entire Z8 family for easy software/hardware system expansion.

Two OTP versions are available for the Z86E21. The Z86E21 is form, fit and function equivalent to the Z86C21, while the Z86E22 is the low noise version of the Z86E21.

FEATURES

- *Complete Microcontroller with 40-pin DIP, or 44-Pin QFP, 32 I/O Lines and 8 Kbytes of On-Chip ROM.*
- *The Register File is Composed of 236 General-Purpose Registers, Four I/O Port Registers and 16 Control and Status Registers.*
- *Full Duplex UART and Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator which Accepts Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *RAM/ROM Protect Option*
- *Low Noise Option*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Standby Modes: STOP and HALT*
- *Clock Speeds: 12, 16 and 20 MHz*
- *CMOS Process*
- *4.5 to 5.5 Volts Operating Range*
- *Six Vectored, Priority Interrupts from Eight Different Sources*
- *All Pins TTL Compatible*



Z86C27/C97 CMOS Z8 DIGITAL TELEVISION CONTROLLER

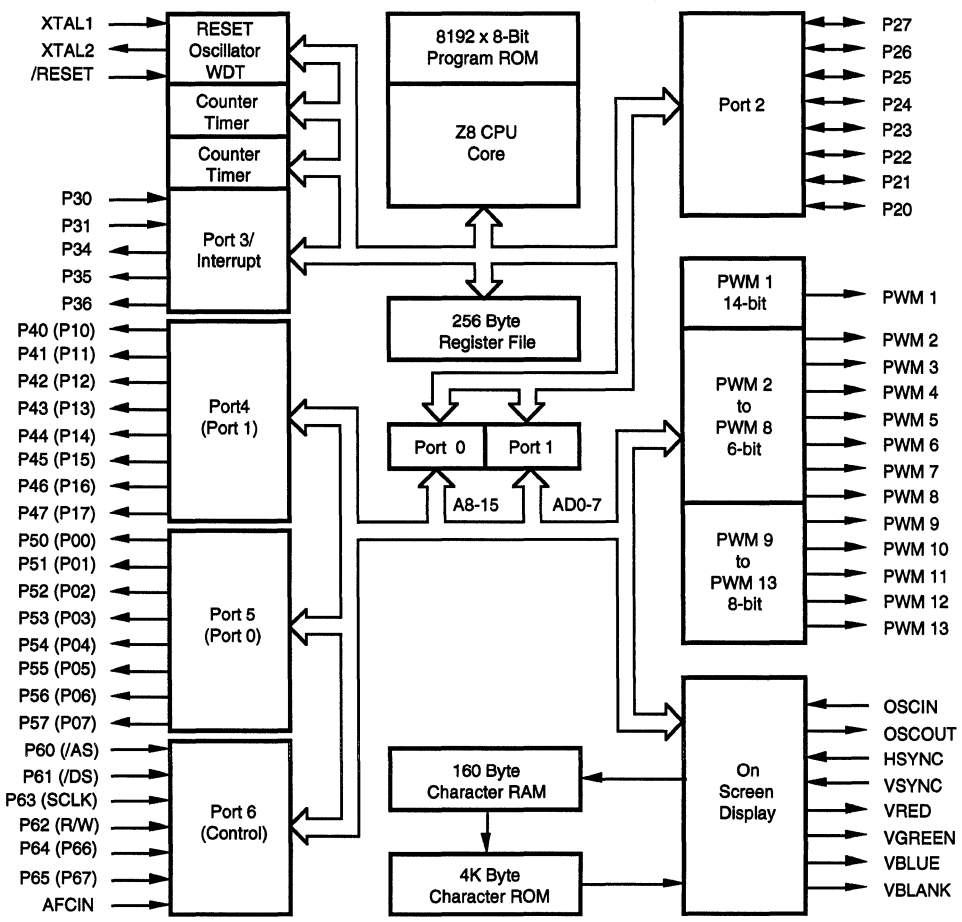
GENERAL DESCRIPTION

The Z86C27 and Z86C97 are CMOS Application Specific Standard Product microcontrollers that integrate specialized peripheral functions (normally provided by external components) for the control of color television, or CRT display related products. Utilizing Zilog's advanced Superintegration™ design methodology, these devices provide an ideal cost, performance solution for consumer and industrial CRT display applications.

The devices have an 8-bit internal data path controlled by a Z8® microcontroller core with 256 bytes of register space. On-chip peripherals include a two channel Counter/Timer, an On-Screen Display video controller, a 13 channel Digital-to-Analog converter and comprehensive Input/Output ports. The Z86C27 is the mask-ROM high volume production device embedded with a custom (customer supplied) program of up to 8K bytes in size. The Z86C97 is the ROM-less version for prototyping and low volume production.

FEATURES

- *Z8 Core-Based CMOS 64-Pin SDIP Controller for CRT Display Applications.*
- *8K ROM, 236-byte RAM, 43 I/O Lines*
- *Internal Reset/Low Voltage Detection*
- *Port 5 (8-Bit LED Drive Output) and Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports.*
- *On-Screen Display*
- *Programmable Row Character Color, Row Background Color, Row Fringe Color, Frame Background Color, Frame Position and Character Size.*
- *12 Volt Open-Drain Drivers for 13 PWM Outputs*
- *128 character set displayed as 8 rows by 20 columns, capable of supporting Roman, Chinese, Korean and Japanese high resolution characters.*
- *160 x 7-bit video RAM*
- *4K x 6-bit character generator ROM*
- *5 to 7 MHz on-chip L-C oscillator for character dot clock*
- *1 Pulse Width Modulator (14-bit resolution) for voltage synthesis tuner control.*
- *Five pulse width modulators (8-bit resolution) for picture control.*
- *Seven pulse width modulators (6-bit resolution) for audio control.*



GENERAL DESCRIPTION

The Z86L29 (ZIRC™) is a low voltage Consumer Controller Processor (CCP™) ideal for IR Remote applications which introduces a new level of sophistication to single-chip architecture. The Z86L29 is a member of the Z8® single-chip microcontroller family with 6 Kbytes of ROM, and 124 bytes of RAM. The device is housed in an 18-pin DIP package, and is CMOS compatible. Zilog's Z86L29 CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86L29 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, and a number of ancillary features that are useful in many industrial, automotive, hand held, battery operated and advanced scientific applications.

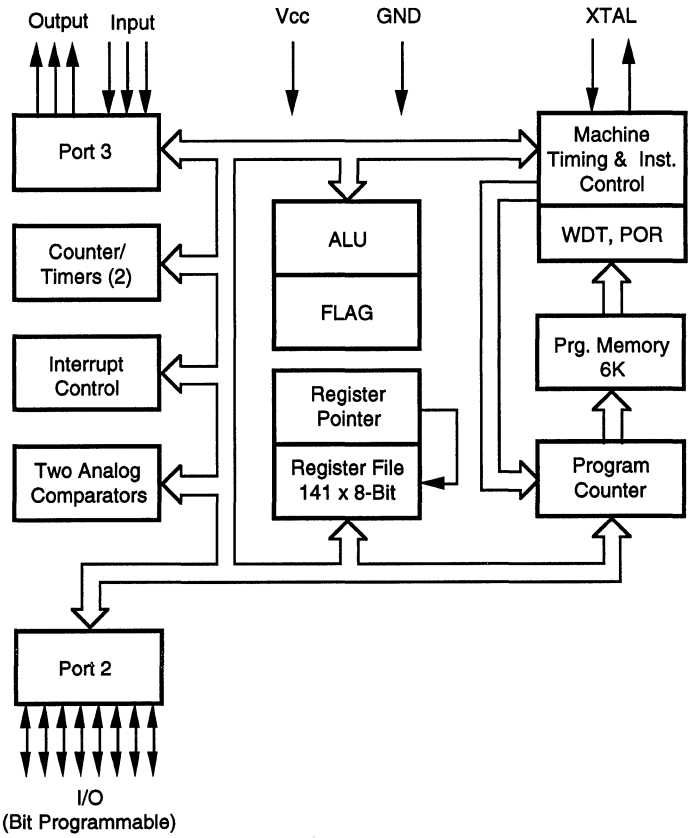
For device applications that demand powerful I/O capabilities, the CCP fulfills this with 14 pins dedicated to input and output. These lines are grouped into two ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

Three basic address spaces are available to support this wide range of configurations; Program Memory, Register File, and Expanded Register File. The Register File is composed of 125 bytes of general-purpose registers, two I/O Port registers and 14 Control and Status registers. The Expanded Register File consists of three control registers.

To unburden the program from coping with real-time problems such as counting/timing and input/output data communication, the Z86L29 offers two on-chip counter/timers with a large number of user selectable modes, and two on-board comparators that can process analog signals with a common reference voltage.

FEATURES

- *8-Bit CMOS Microcontroller, 18-Pin DIP Package*
- *Low Cost*
- *2.0 to 3.6 Volt Operating Range*
- *Low Power Consumption - 18 mW (Typical)*
- *Four High-Current Outputs at 2 Volts*
  - *7 ma Source (1)*
  - *10 ma Sink (3)*
- *Two Standby Modes - STOP and HALT*
- *14 Input/Output Lines (2 with Comparator Inputs)*
- *All Digital Inputs are CMOS Level*
- *6 Kbytes of ROM*
- *125 Bytes of RAM*
- *Three Expanded Register File Control Registers*
- *Two Programmable 8-Bit Counter/Timers*
- *6-Bit Programmable Prescaler*
- *Six Vectored, Priority Interrupts from Five Different Sources*
- *Clock Speed: 8 MHz*
- *Brown-Out Protection*
- *Watch-Dog Timer, Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.*



Z86C30 CMOS Z8 CONSUMER CONTROLLER PROCESSOR

GENERAL DESCRIPTION

The Z86C30 is a single chip microcontroller with 4 Kbytes of ROM. It offers all the outstanding features of the Z8® family architecture in a low power, 28-pin format.

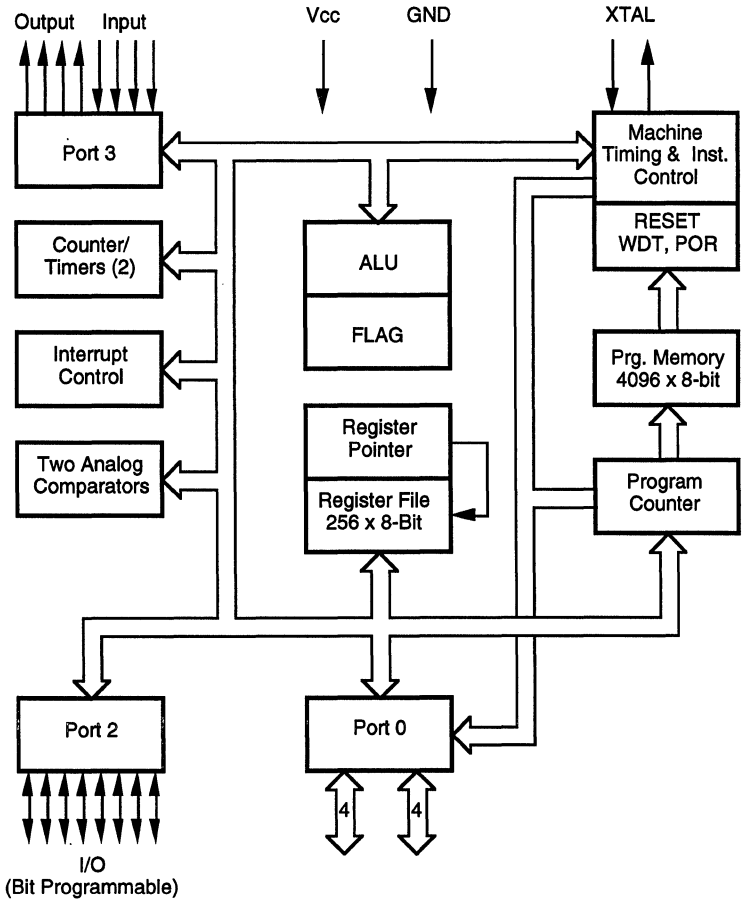
The Z86C30 architecture is based on Zilog's 8-bit microcontroller core with an expanded register file to allow access to register mapped peripheral and I/O circuits.

The Z86C30 has instruction compatibility with the entire Z8 family for easy software/hardware system expansion. The powerful feature set allows minimization of peripheral components.

The Z86E30 is a form, fit and function OTP/EPROM equivalent of the Z86C30.

FEATURES

- *Complete CMOS Microcontroller with 24 I/O Lines and 4 Kbytes of On-Chip ROM in a 28-Pin DIP Package.*
- *The Register File is Composed of 236 Bytes of General-Purpose Registers, Three I/O Port Registers and 15 Control and Status Registers.*
- *Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC, RC or External Clock Drive.*
- *"Brown-Out" Protection*
- *Two Comparators with Programmable Interrupt Polarity*
- *Fast Instruction Pointer, 1 µs at 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Standby Modes: STOP and HALT*
- *Clock Speeds: 12 and 16 MHz*
- *3.0 to 5.5 Volts Operating Range for 12 MHz*
- *4.5 to 5.5 Volts Operating Range for 16 MHz*
- *All Digital Inputs are CMOS Levels and Schmitt Triggered.*
- *Six Vectored, Priority Interrupts from Six Different Sources.*



GENERAL DESCRIPTION

The Z86C40 is a single chip microcontroller with 4 Kbytes of ROM. It offers all the outstanding features of the Z8® family architecture and is housed in a DIP, PLCC or QFP package.

The Z86C40 architecture is based on Zilog's 8-bit microcontroller core with an expanded register file to allow access to register mapped peripheral and I/O circuits.

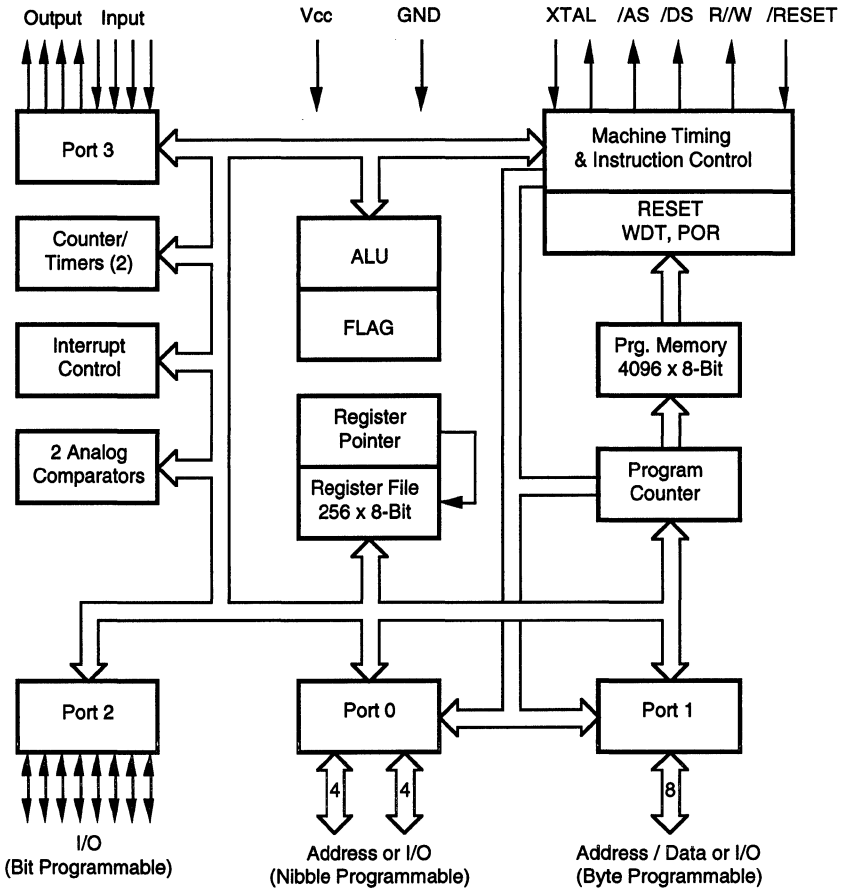
The Z86C40 has instruction compatibility with the entire Z8 family for easy software/hardware system expansion.

The Z86C89 is the ROMless version that can be used with a RC or LC circuit as the source for the on-chip oscillator.

The Z86E40 is a form, fit and function OTP equivalent of the Z86C40.

FEATURES

- *Complete Microcontroller with 32 I/O Lines and 4 Kbytes of On-Chip ROM.*
- *The Register File is Composed of 236 Bytes of General-Purpose Registers, Four I/O Port Registers and 15 Control and Status Registers*
- *Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC and RC or External Clock Drive.*
- *"Brown-Out" protection*
- *Low Noise Programmable*
- *Two comparators with programmable interrupt polarity*
- *Fast instruction pointer - 1 microsecond at 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Standby modes: STOP and HALT*
- *Power Management*
- *Clock speeds: 8, 12 and 16 MHz*
- *3.0 to 5.5 Volts Operating Range (up to 12 MHz)*
- *Six vectored, priority interrupts from six different sources*
- *Available in 40- or 44-pin package, DIP, PLCC or QFP*



Z86C61 CMOS Z8 MICROCONTROLLER

GENERAL DESCRIPTION

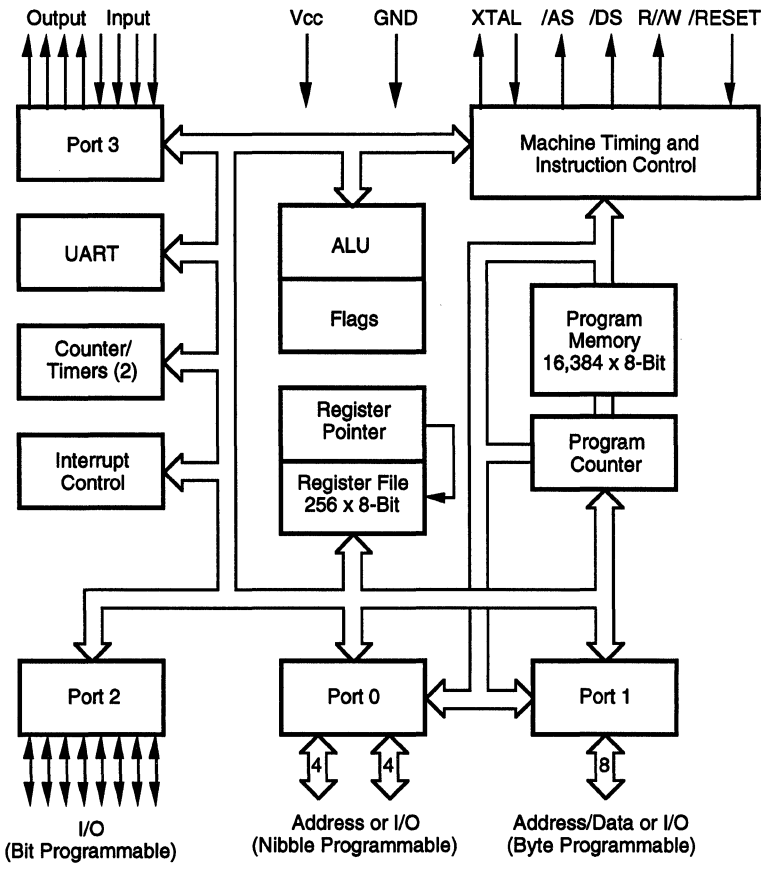
The Z86C61 is a member of the Z8® single-chip microcontroller family. It is pin compatible with the Z86C21 but has twice the on-board memory with 16 Kbytes of ROM. The device is housed in a 40-pin DIP, 44-pin PLCC, or a 44-pin QFP package. It offers all the outstanding features of the Z8 family architecture.

The Z86C61 provides up to 16 output address lines permitting an address space of up to 48 Kbytes of external program and data memory each. The 256-byte Register File consists of 236 general purpose registers, four I/O port registers, and 16 status and control registers.

The Z86C61 architecture is based on Zilog's 8-bit microcontroller core. The device has instruction compatibility with the entire Z8 family for easy software/hardware system expansion.

FEATURES

- *Complete Microntroller with 40-Pin DIP, 44-Pin PLCC, or 44-Pin QFP, 32 I/O Lines and 16 Kbytes of On-Chip ROM.*
- *The Register File is Composed of 236 General Purpose Registers, Four I/O Port Registers and 16 Control and Status Registers.*
- *Full Duplex UART and Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator which Accepts Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *RAM/ROM Protect Option*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Standby Modes: STOP and HALT*
- *1.2 Micron CMOS Technology*
- *Clock Speeds: 12 and 16 MHz*
- *3.0 to 5.5 Volts Operating Range for 12 MHz*
- *4.5 to 5.5 Volts Operating Range for 16 MHz*
- *Six Vectored, Priority Interrupts from Eight Different Sources*



GENERAL DESCRIPTION

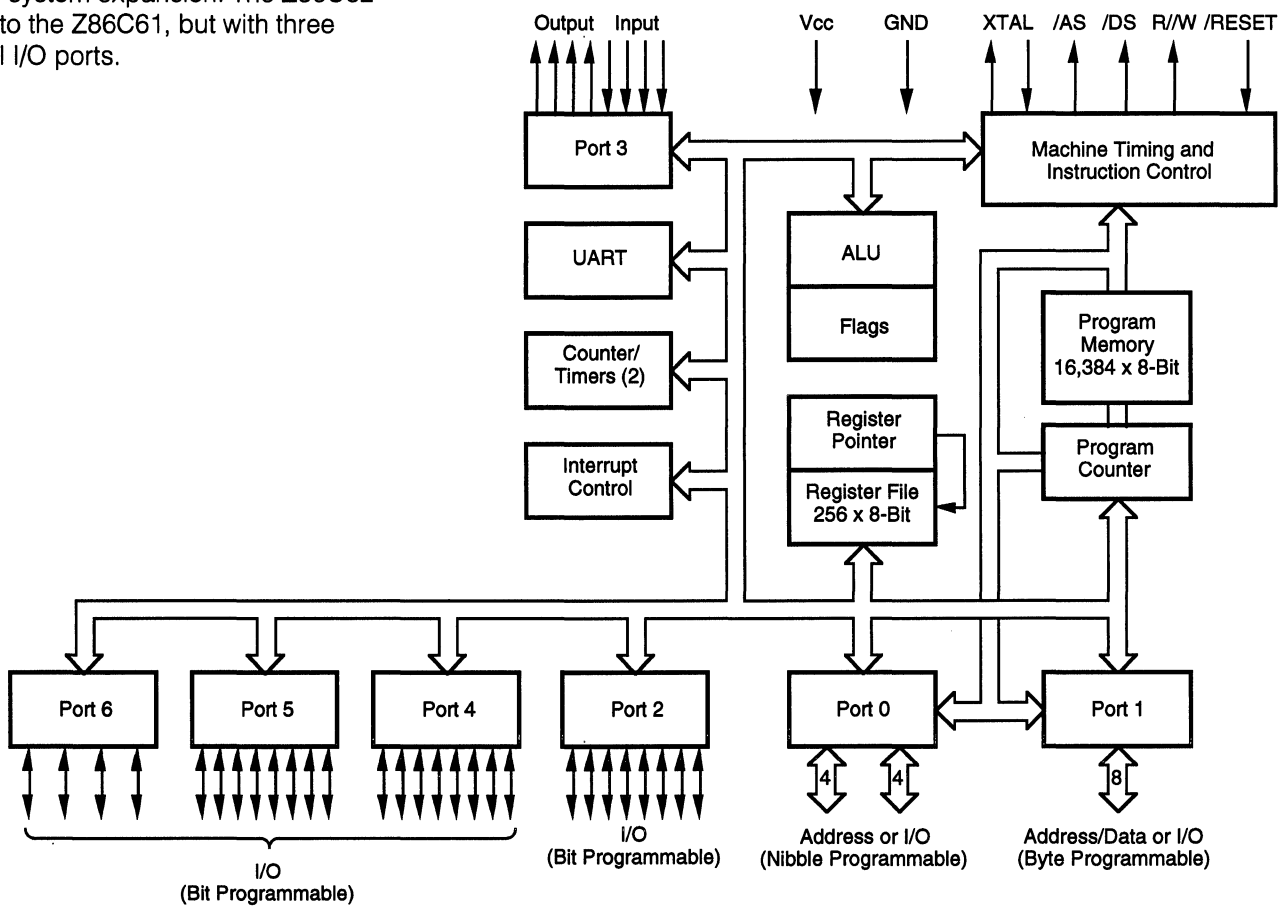
The Z86C62 is a member of the Z8® single-chip microcontroller family with 16 Kbytes of ROM. The device is housed in a 64-pin DIP or a 68-pin PLCC. It offers all the outstanding features of the Z8 family architecture.

The Z86C62 provides up to 16 output address lines permitting an address space of up to 48 Kbytes of external program and data memory each. The 256-byte Register File consists of 236 general-purpose registers, four I/O port registers, and 16 status and control registers. Three additional I/O port registers and five status and control registers reside in the Expanded Register File.

The Z86C62 architecture is based on Zilog's 8-bit microcontroller core. The device has instruction compatibility with the entire Z8 family for easy software/hardware system expansion. The Z86C62 is similar to the Z86C61, but with three additional I/O ports.

FEATURES

- *Complete Microcontroller with 68-Pin PLCC, or 64-Pin DIP, 56 I/O Lines and 16 Kbytes of On-Chip ROM.*
- *The Register File is Composed of 236 General-Purpose Registers, Four I/O Port Registers and 16 Control and Status Registers.*
- *Three Expanded Register File I/O Port Registers and Five Control Registers.*
- *Full Duplex UART and Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator which Accepts Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *Six Vectored, Priority Interrupts from Eight Different Sources*
- *RAM/ROM Protect Option*
- *Standby Modes: STOP and HALT*
- *1.2 Micron CMOS Technology*
- *Clock Speeds: 12 and 16 MHz*
- *3.0 to 5.5 Volts Operating Range for 12 MHz*
- *4.5 to 5.5 Volts Operating Range for 16 MHz*
- *All Pins TTL Compatible*



GENERAL DESCRIPTION

The Z86127 Low-Cost Digital Television Controller (LDTC) introduces a new level of sophistication to single-chip architecture. The Z86127 is a member of the Z8® single-chip microcontroller family with 8 Kbytes of ROM and 236 bytes of RAM. The device is housed in a 64-pin DIP package, in which only 52 are active, and are CMOS compatible. The LDTC offers mask programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program).

Zilog's LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86127 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The devices have an 8-bit internal data path controlled by a Z8 microcontroller, and On Screen Display (OSD) logic circuits/Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Ports 2 and Port 3), Interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support eight rows by 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5x7 dot pattern) or high resolution (11x15 dot pattern) characters. The Z86C97 currently supports high resolution characters only.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal level. Five 8-bit PWM ports are used to vary picture levels.

The LDTC applications demand powerful I/O capabilities. The Z86127 fulfills this with 27 I/O pins dedicated to input and output. These lines are grouped into four ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File .The Register File is composed of 236 bytes of general purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

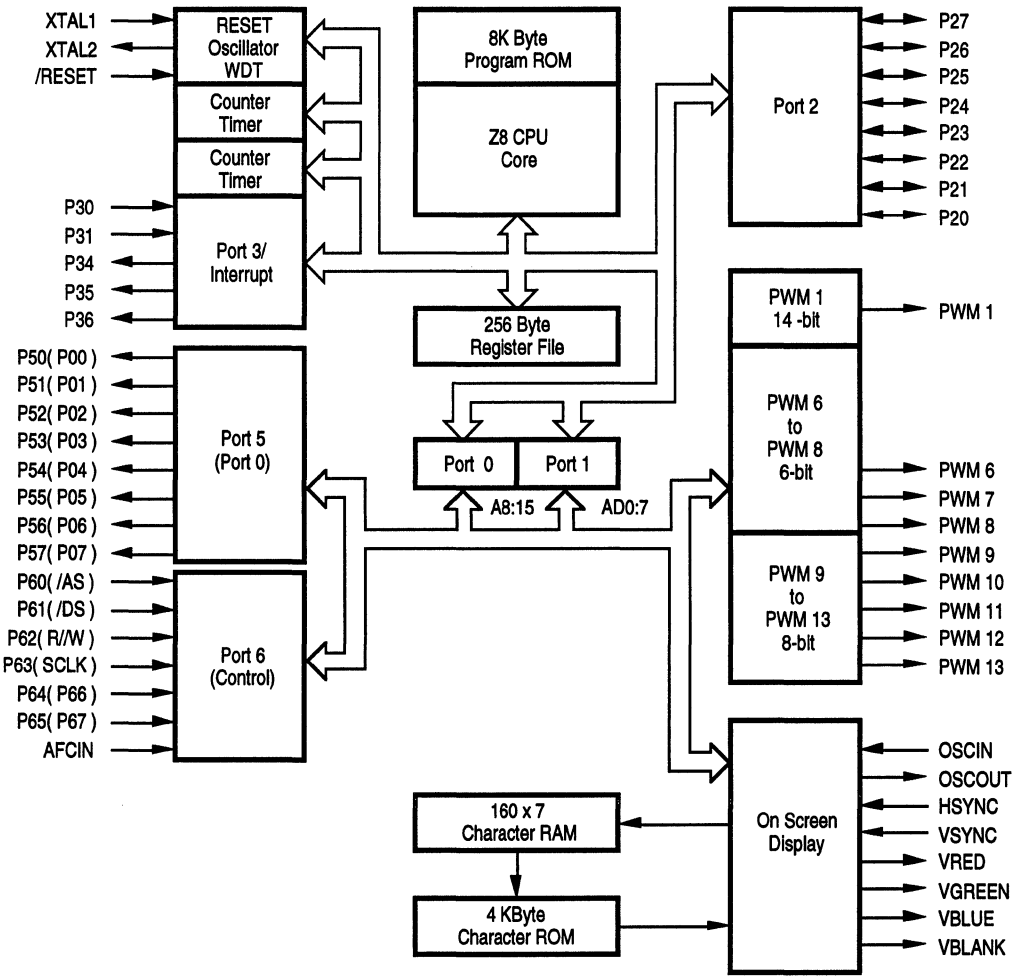
To unburden the program from coping with the real-time problems such as counting/timing and data communication, the LDTC's offers two on-chip counter/timers with a large number of user selectable modes.

FEATURES

- *8-Bit CMOS Low Cost Microcontroller for Consumer Television Applications, 64-Pin DIP Package.*
- *Low Power Consumption*
- *Fast Instruction Pointer -1.5 µs @ 4 MHz*
- *Two Standby Modes - STOP and HALT*
- *Low Voltage Detection/Voltage Sensitive Reset*
- *35 Input/Output Lines*
- *Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports.*
- *Port 5 (8-Bit LED Drive Output) and Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports.*
- *All Digital CMOS Levels Schmitt Triggered*
- *8 Kbytes of ROM*
- *236 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Six Different Sources*
- *Clock Speeds up to 4 MHz*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *Watch-Dog Timer and Power-On Reset*

On Screen Display Controller

- *4K x 6-Bit Character Generator ROM*
- *160 x 7-Bit Video RAM*
- *Mask Programmable 128 Character Set Displayed in an 8-Row by 20-Column Format, 12 by 15 Pixel Character Cell, Capable of Supporting English, Korean, Chinese and Japanese High Resolution Characters.*
- *Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character size.*
- *Programmable Display Position and Character Size Control.*
- *One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control.*
- *Five Pulse Width Modulators (8-Bit Resolution) for Picture Control.*
- *Three Pulse Width Modulators (6-Bit Resolution) for Audio Control.*



Z86128 L21C™ LINE 21 CLOSED CAPTION CONTROLLER

GENERAL DESCRIPTION

The Z86128 Line 21 Closed-Caption Controller is a single I.C. designed to conform to FCC Line 21 Closed-Caption Specifications of 12 April 1991. This Superintegration™ VLSI device is completely self contained requiring only composite video, a horizontal timing signal as input and an "external keyer", i.e., video switch between TV video and Closed-Caption video to produce captioned video. The Z86128 uses a wired logic approach to perform the functions selected through its input control signals. It is fabricated using standard CMOS technology and designed to achieve the lowest possible cost.

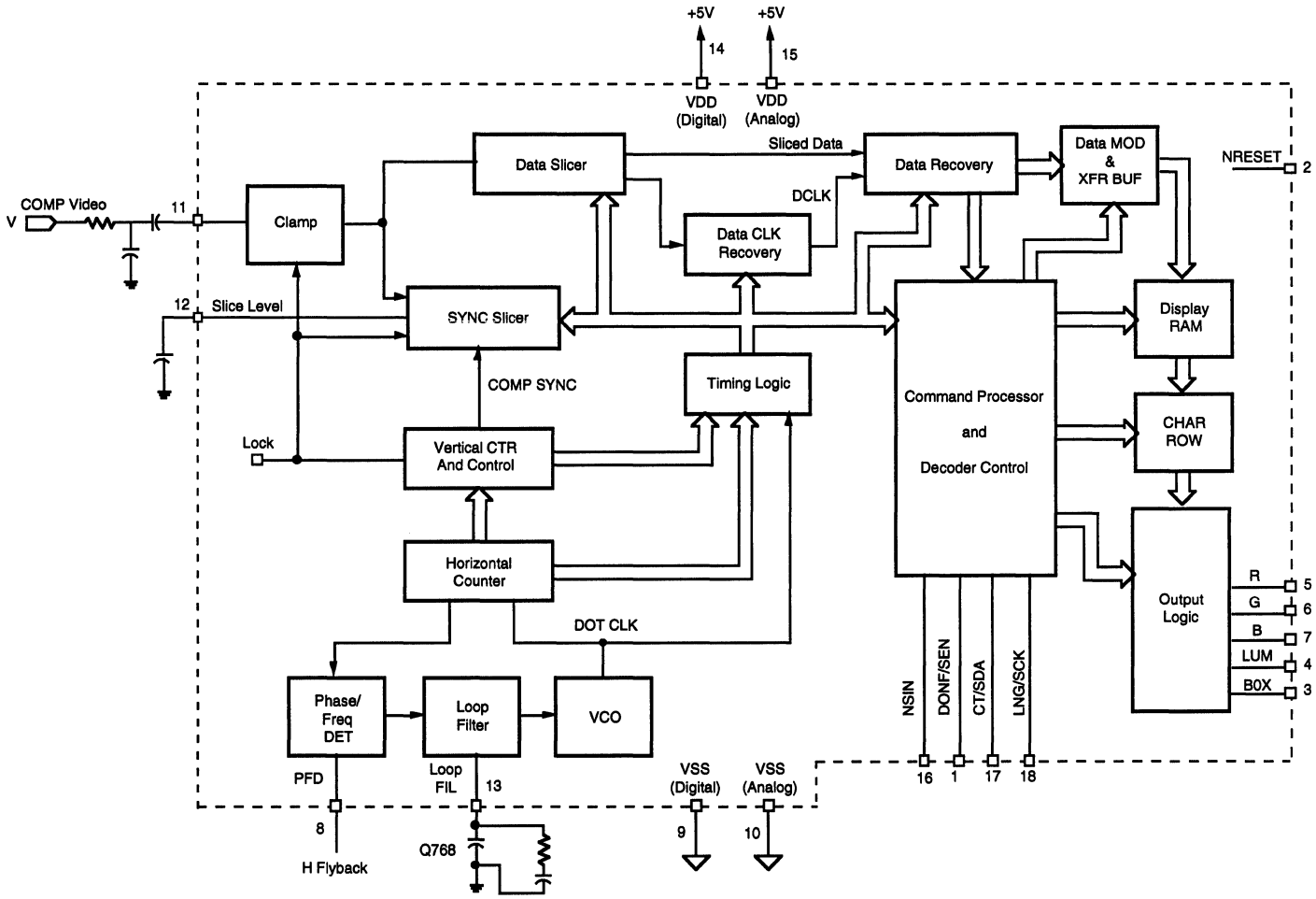
The Z86128 is intended for use in a set-top decoder or in any television receiver conforming to the NTSC standard. It is capable of processing and displaying all standard L21C format transmissions including the codes specified by the FCC "Report and Order" on GEN Docket No. 91-1, dated 12 April 1991. If and when PAL and SECAM TV standards define a protocol using the Line 21 format, this design will be readily convertible to that standard.

The Line 21 Closed Captioning System

The L21C system provides for the transmission of CAPTION information and other TEXT material as an encoded composite data signal. This is during the unblanked portion of Line 21, field 1, of the standard NTSC video signal. In addition, a framing code is transmitted during the first half of Line 21, field 2. The encoded composite video signal for Line 21, field 1 and 2 conforms to the Standard Synchronizing Waveform for Color Transmission given in Sub-part E, Part 73 of the FCC Rules and Regulations.

FEATURES

- *Complete Standalone Line 21 Closed-Caption Controller that Conforms to FCC Line 21 Closed-Caption Specifications of 4/12/91*
- *Simple System Interface*
- *Optional Serial Interface for Mode*
- *Requires only Two Inputs to Operate:*
  - *Composite Video*
  - *Any Horizontal Timing Pulse*
- *On-Board Analog Sync and Data Slicer - No External Analog Required*
- *CMOS VLSI Design for Low Power and Low Cost*
- *On-Board Display RAM*
- *Odd or Even Field Selectable in Serial Control Mode*
- *On-Board Character Font ROM - 12x18 Character in 16x26 Cell*
- *Visual Attributes:*
  - *Color*
  - *Underline*
  - *Italic*
  - *Blink*
- *Smooth Scrolling*
- *Valid Line 21 Input Detection*
- *Automatic Screen Blanking after 1.5 Seconds with no Valid Input (Auto Blanking)*
- *Automatic Caption Display RAM Erase after 16 Seconds with no Valid Input*
- *18-Pin DIP Package*
- *Automatic Erase on Channel Change*


+5V
+5V
14
15
VDD (Digital)
VDD (Analog)
COMP Video
V
11
Clamp
Data Slicer
Sliced Data
Data Recovery
Data MOD & XFR BUF
NRESET
2
DCLK
Data CLK Recovery
12
Slice Level
SYNC Slicer
Display RAM
COMP SYNC
Timing Logic
Command Processor and Decoder Control
Lock
Vertical CTR And Control
CHAR ROW
Horizontal Counter
Output Logic
R
G
B
LUM
BOX
5
6
7
4
3
DOT CLK
NSIN
DONF/SEN
CT/SDA
LNG/SCK
Phase/ Freq DET
Loop Filter
VCO
PFD
Loop FIL
13
VSS (Digital)
VSS (Analog)
16
1
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18
8
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10
H Flyback
Q768

Z86227 40-PIN LOW-COST DIGITAL TELEVISION CONTROLLER

GENERAL DESCRIPTION

The Z86227 40-pin Low-Cost Digital Television Controller (4LDTC) introduces a new level of sophistication to single-chip architecture. The Z86227 is a member of the Z8® single-chip microcontroller family with 6 Kbytes of ROM and 236 bytes of RAM. The device is offered in a 40-pin package and is CMOS compatible. The 4LDTC offers mask programmed ROM which enables the Z8 microcontroller to be used in a high volume production application device embedded with a custom program (customer supplied program) and combines together with the Z86C27 (DTC) and Z86127 (LDTC) to provide support for high-end, mid-range and low-end TV applications.

Zilog's 4LDTC offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption. The device provides an ideal performance and reliability solution for consumer and industrial television applications.

The Z86227 architecture is characterized by utilizing Zilog's advanced Superintegration™ design methodology. The device has an 8-bit internal data path controlled by a Z8 microcontroller and On-Screen Display (OSD) logic circuits and Pulse Width Modulators (PWM). On-chip peripherals include two register mapped I/O ports (Port 2 and Port 3), interrupt control logic (one software, two external and three internal interrupts) and a standby mode recovery input port (Port 3, P30).

The OSD control circuits support six rows by 20 columns of characters. The character color is specified by row. One of the eight rows is assigned to show two kinds of colors for bar type displays such as volume control. The OSD is capable of displaying either low resolution (5x7 dot pattern) or high resolution (11x15 dot pattern) characters.

A 14-bit PWM port provides enough voltage resolution for a voltage synthesizer tuning system. Three 6-bit PWM ports are used for controlling audio signal levels. Three 8-bit PWM ports used to vary picture levels.

The 4LDTC applications demand powerful I/O capabilities. The Z86227 fulfills this with 24 I/O pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide timing, status signals, parallel I/O and an address/data bus for interfacing to external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Video RAM, and Register File. The Register File is composed of 236 bytes of general purpose registers, two I/O Port registers, 15 control and status registers and three reserved registers.

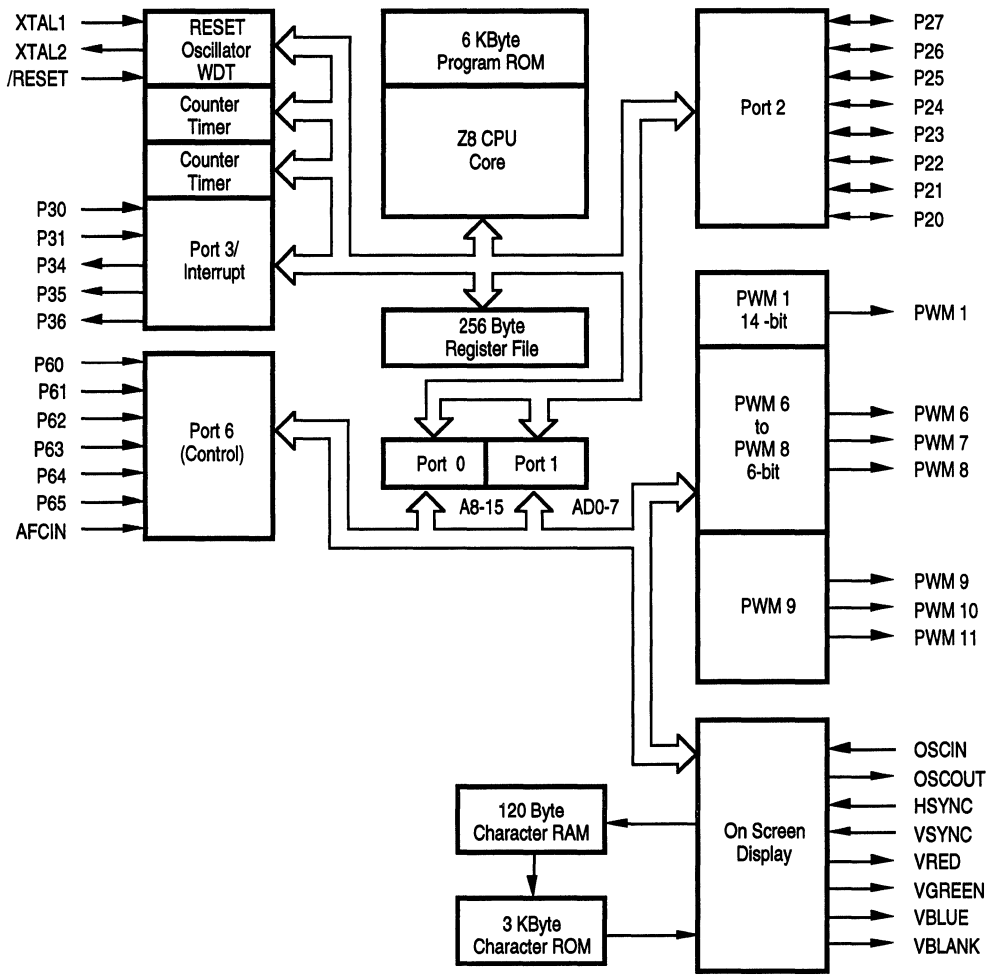
To unburden the program from coping with the real-time problems such as counting/timing and data communication, the 4LDTC offers two on-chip counter/timers with a large number of user selectable modes.

FEATURES

- *8-Bit CMOS Microcontroller for Consumer Television, Cable and Satellite Receiver Applications.*
- *40-Pin DIP Package*
- *Lowest Cost DTC Family Member*
- *Low Power Consumption*
- *Fast Instruction Pointer - 1.5 µs @ 4 MHz*
- *Two Standby Modes - STOP and HALT*
- *Low Voltage Detection/Voltage Sensitive Reset*
- *24 Input/Output Lines*
- *Port 2 (8-Bit Programmable I/O) and Port 3 (2-Bit Input, 3-Bit Output) Register Mapped Ports.*
- *Port 6 (6-Bit Input and Tri-State Comparator AFC Input) Memory Mapped I/O Ports.*
- *All Digital CMOS Levels Schmitt Triggered*
- *6 Kbytes of ROM*
- *236 Bytes of RAM*
- *Two Programmable 8-Bit Counter/ Timers each with 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Six Different Sources*
- *Clock Speeds up to 4 MHz*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *Watch-Dog Timer/Power-On Reset*

On Screen Display Controller

- *3K x 6-Bit Character Generator ROM*
- *120 x 7-Bit Video RAM*
- *Mask Programmable 96-Character Set Displayed in an 6-Row by 20-Column Format, 12 by 15 Pixel Character Cell, Capable of Supporting English, Korean, Chinese and Japanese High Resolution Characters.*
- *Fully Programmable Color Attributes Including Row Character, Row Background/Fringes, Frame Background/Position, Bar Graph Color Change, and Character Size.*
- *Programmable Display Position and Character Size Control.*
- *One Pulse Width Modulator (14-Bit Resolution) for Voltage Synthesis Tuner Control.*
- *Three Pulse Width Modulator (8-Bit Resolution) for Picture Control.*
- *Three Pulse Width Modulators (6-Bit Resolution) for Audio Control.*



Z86C89/C90 CMOS ROMLESS Z8 MICROCONTROLLER

GENERAL DESCRIPTION

The Z86C89/C90, are single chip ROMless microcontrollers. They offer all the outstanding features of the Z8 family architecture and is housed in a DIP, PLCC or QFP package.

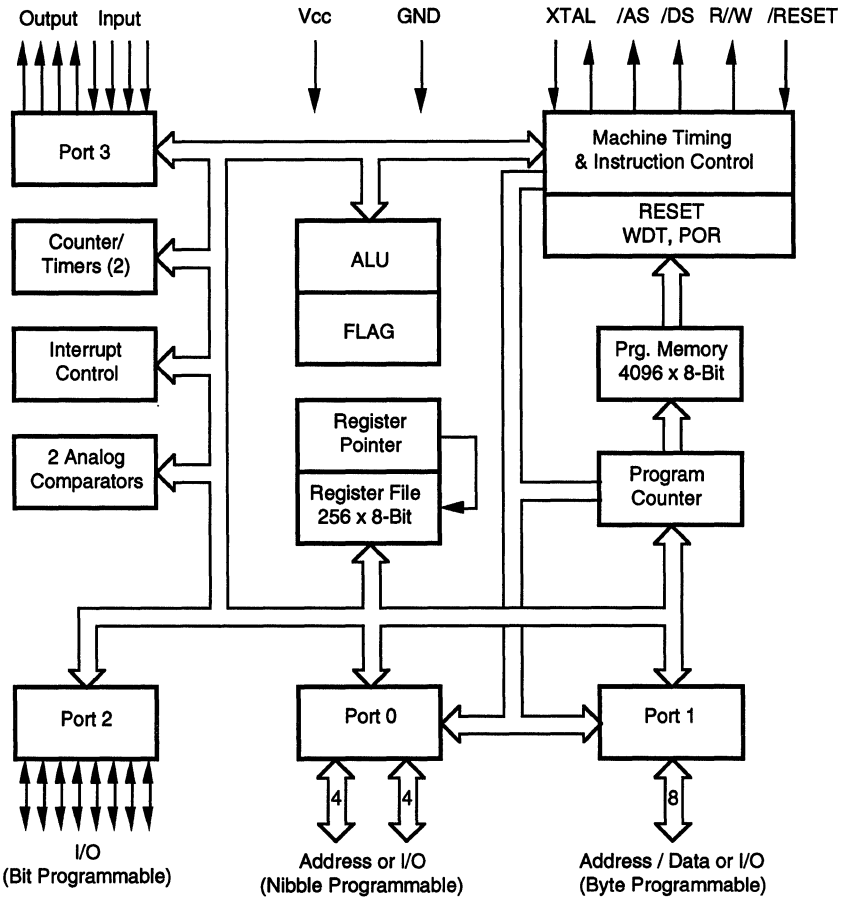
The Z86C89/C90 architecture is based on Zilog's 8-bit microcontroller core with an expanded register file to allow access to register mapped peripheral and I/O circuits.

The Z86C89/C90 have instruction compatibility with the entire Z8 family for easy software/hardware system expansion.

The Z86C89 is the ROMless version that can be used with a RC or LC circuit as the source for the on-chip oscillator.

FEATURES

- *Complete microcontroller with 32 I/O lines and 4 Kbytes of on-chip ROM or ROMless (Z86C90/C89), selectively*
- *The register file is composed of 236 bytes of general purpose registers, 4 I/O port registers and 15 control and status registers*
- *Two programmable 8-bit counter/ timers, each with a 6-bit programmable prescaler*
- *On-chip oscillator that accepts a crystal, ceramic resonator, or external clock drive. The C40/C89 versions also accept LC and RC.*
- *"Brown-Out" protection*
- *Two comparators with programmable interrupt polarity*
- *Fast instruction pointer - 1 microsecond at 12 MHz*
- *Watch Dog/Power-On Reset timer*
- *Standby modes: STOP and HALT*
- *Clock speeds: 8, 12, 16 and 20 MHz (8 MHz for Z86C89)*
- *3.0 to 5.5 Volts operating range*
- *Six vectored, priority interrupts from six different sources*
- *Available in 40- or 44-pin DIP, PLCC or QFP packages*



GENERAL DESCRIPTION

The Z86C91 is a CMOS ROMless version of the Z8® single-chip microcontroller. It offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microntroller to be used in applications where code flexibility is required.

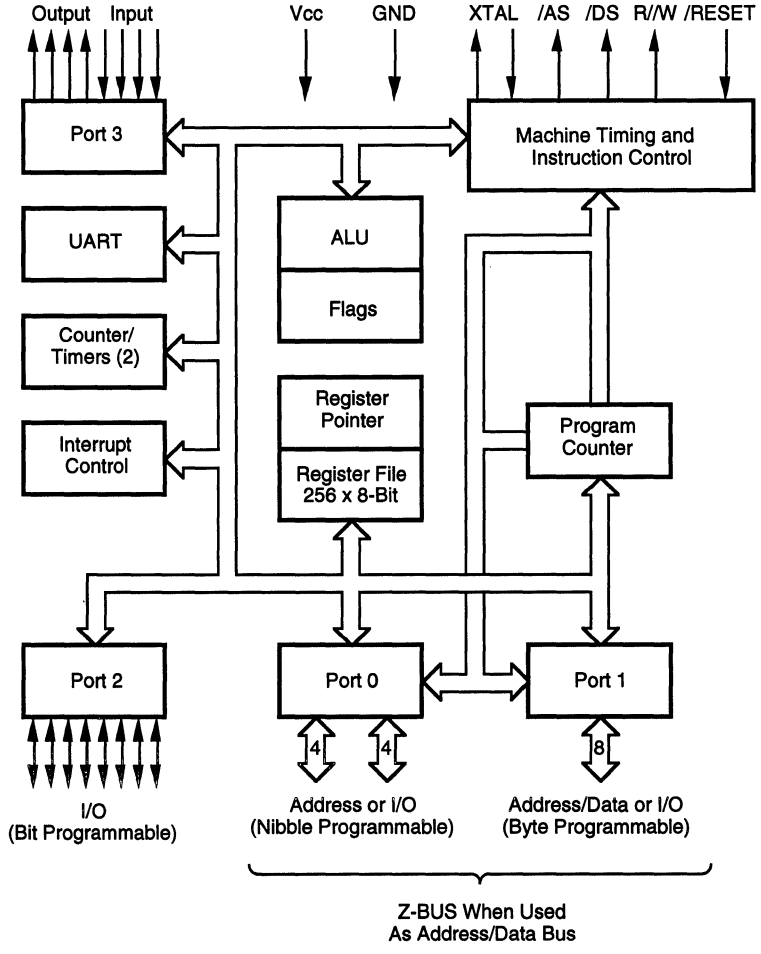
The Z86C91 can provide up to 16 output address lines, thus permitting an address space of up to 64 Kbytes of data or program memory. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

There are 256 registers located on-chip organized as 236 general purpose registers, 16 control and status registers, and three I/O port registers. Register file can be divided into sixteen groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

The Z86C91 is the ROMless version of the Z86C21.

FEATURES

- *Complete Microcontroller, 24 I/O Lines, and up to 64 Kbytes of Addressable External Space Each for Program and Data Memory.*
- *256-Byte Register File, Including 236 General-Purpose Registers, Three I/O Port Registers, and 16 Status and Control Registers.*
- *Vectored, Priority Interrupts for I/O, Counter/Timers, and UART.*
- *On-Chip Oscillator that Accepts Crystal or External Clock Drive.*
- *Full-Duplex UART and Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler.*
- *Register Pointer so that Short, Fast Instructions Can Access Any One of the Sixteen Working-Register Groups.*
- *Single +5V Power Supply, all I/O Pins TTL Compatible*
- *Clock Speeds: 16 and 20 MHz*
- *CMOS Process*
- *Two Low-Power Standby Modes, STOP and HALT*



Z86C93 CMOS Z8 ROMLESS MICROCONTROLLER

GENERAL DESCRIPTION

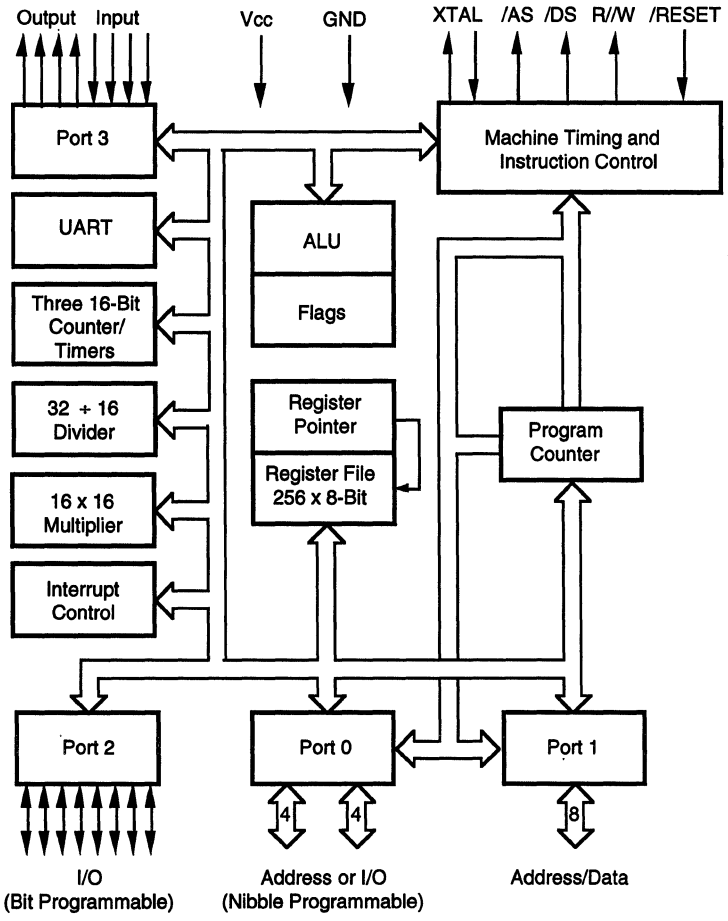
The Z86C93 is a CMOS ROMless Z8® microcontroller enhanced with a hardwired 16-bit x 16-bit multiplier, 32-bit/16-bit divider, and three 16-bit counter timers. It is fabricated using 1.2 micron CMOS technology. It is offered in 44-pin Leaded Chip Carrier and 44-pin Plastic Quad Flat Pack. The Z86C93 is fully pin compatible with the Z86C91, yet it offers a much more powerful mathematical capability.

The Z86C93 provides up to 16 output address lines permitting an address space of up to 64K bytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A8-A15.

There are 256 registers located on-chip; 236 general purpose registers, 16 control and status registers, and three I/O port registers. Register file can be divided into sixteen groups of 16 working registers each. Configuring the registers in this manner allows the use of short format instructions; any of the individual registers can be accessed directly.

FEATURES

- *Complete Microcontroller, 24 I/O Lines, and up to 64 Kbytes of Addressable External Space each for Program and Data Memory.*
- *16-Bit by 16-Bit Hardwired Multiplier with 32-Bit Result in 17 Clock Cycles; 32-Bit by 16-Bit Hardwired Divider with 16-Bit Quotient, and 16-Bit Remainder in 20 Clock Cycles.*
- *256-Byte Register File, Including 236 General-Purpose Registers, Three I/O Port Registers and 16 Status and Control Registers.*
- *Vectored, Priority Interrupts for I/O, Counter/Timers and UART.*
- *On-Chip Oscillator that Accepts Crystal or External Clock Drive.*
- *Full-Duplex UART and Three 16-Bit Counter/Timers. Two of the Counter/Timers have 6-Bit Prescalers. The Third has a 4-Bit Prescaler, One Capture Register and a Fast Decrement Mode.*
- *Register Pointer so that Short, Fast Instructions can Access any One of the Sixteen Working Register Groups.*
- *Single +5V Power Supply, all I/O Pins TTL Compatible.*
- *1.2 Micron CMOS Technology*
- *Clock Speeds: 20 and 25 MHz*
- *Two Low Power Standby Modes: STOP and HALT*



GENERAL DESCRIPTION

The Z86C96 is a CMOS ROMless version of the Z8™ single-chip microcontroller. It offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcontroller to be used in applications where code flexibility is required.

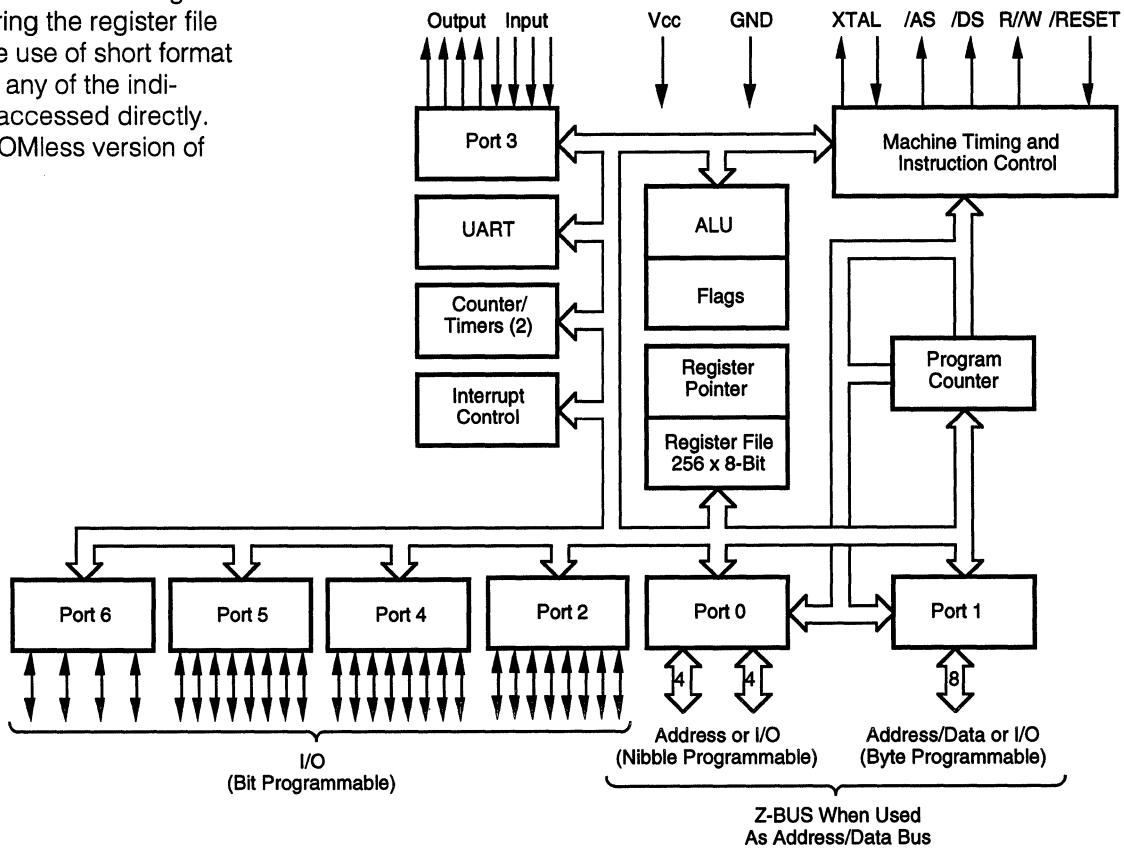
The Z86C96 can provide up to 16 output address lines, thus permitting an address space of up to 64 Kbytes of data or program memory. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

There are 256 registers located on-chip organized as 236 general-purpose registers, 16 control and status registers, and six I/O port registers. The register file can be divided into 16 groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

The Z86C96 is the ROMless version of the Z86C62.

FEATURES

- *Complete Microcontroller, 56 I/O Lines, and up to 64 Kbytes of Addressable External Space each for Program and Data Memory.*
- *256-Byte Register File, Including 236 General-Purpose Registers, Six I/O Port Registers, and 16 Status and Control Registers.*
- *Three Expanded Register File I/O Port Registers and Five Control Registers*
- *Vectored, Priority Interrupts for I/O, Counter/Timers, and UART.*
- *On-Chip Oscillator that Accepts Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *Full-Duplex UART and two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *Register Pointer so that Short, Fast Instructions can Access any One of the Sixteen Working-Register Groups.*
- *3.0 to 5.5 Volts Operating Range for 12 MHz*
- *4.5 to 5.5 Volts Operating Range for 20 MHz*
- *Clock Speeds: 12 and 20 MHz*
- *1.2 Micron CMOS Technology*
- *Two Low-Power Standby Modes, STOP and HALT*



Z88C00 CMOS SUPER8® MICROCONTROLLER

GENERAL DESCRIPTION

The CMOS Super8® offers new flexibility and sophistication in 8-bit microcontrollers.The Super8 offers all the features necessary for industrial, consumer, and automotive applications with an enhanced feature set and CMOS technology. At the same time, the CMOS Super8 retains full pin-for-pin compatibility with the NMOS Super8. Available in 48-pin plastic DIP and 68-pin plastic leaded chip carrier (PLCC), the CMOS Super8 is the last word in general-purpose controllers.

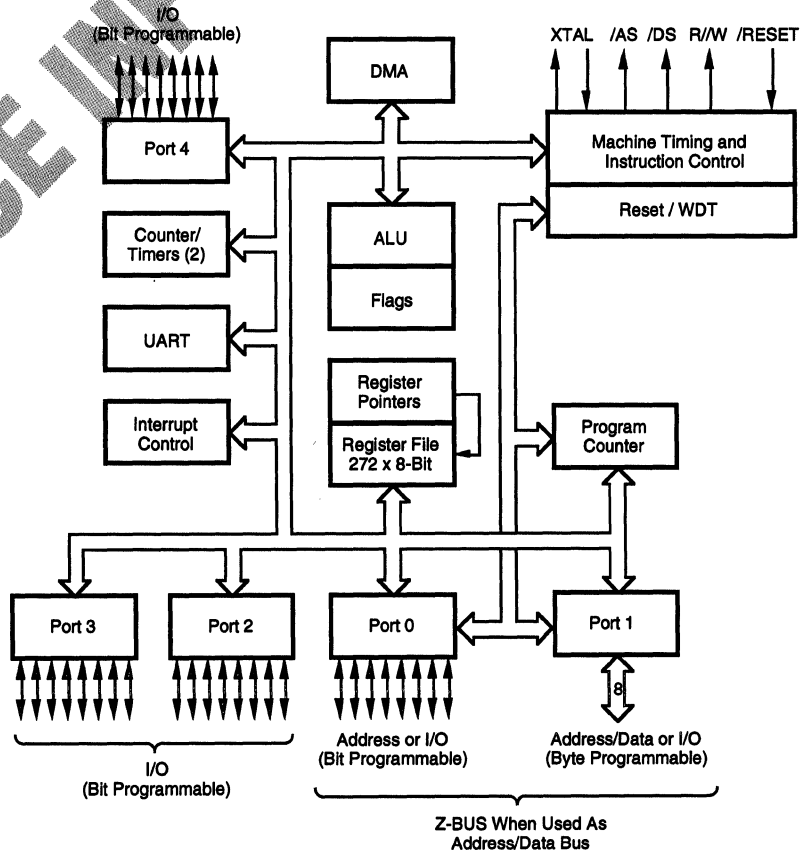
The Super8 features a full-duplex universal asynchronous receiver/transmitter (UART) with on-chip baud rate generator, on-chip oscillator, two 16-bit counter/timers each wtih an 8-bit prescaler, a direct memory access (DMA) controller, watch dog timer (WDT), and STOP mode.

Incorporated in the new CMOS Super8 is also a bonding option for a de-multiplexed external memory interface bus. In de-muxed mode, PORTs 0 and 4 will function as address PORTs, with PORT 1 as data bus. PORT 4 will drive the lower address bits and PORT 0 will drive the upper address bits when both PORTs are configured as external memory interface. This gives the user more addressing flexibility.

Finally, by adding the enhanced features of WDT, STOP and HALT modes, and more versatile counter/timers, the CMOS Super8 can fit easily into more complex function applications where a general purpose microcontroller is a necessity.

FEATURES

- *Full Super8 Instruction Set*
- *CMOS technology*
- *Multiply and Divide instructions, Boolean and BCD operations.*
- *329 byte registers, including 272 general purpose registers, and 57 mode and control registers.*
- *128K bytes of memory*
- *Two register pointers allow 600 nsec access time*
- *Direct Memory Access (DMA)*
- *Two 16-bit counter/timers with 8-bit prescalers*
- *Up to 32 bit-programmable and byte-programmable I/O lines, with two handshake channels.*
- *Interrupt structure supports:*
  - *27 interrupt sources*
  - *16 interrupt vectors*
  - *8 interrupt levels*
  - *Servicing capabilities in 600 nsec*
- *Full-duplex UART with special features*
- *On-chip oscillator*
- *Clock speed: 25 MHz*
- *STOP mode*
- *HALT mode with use of WFI instruction*
- *TEST word feature*
- *Low CMOS power consumption*
- *Full pin-for-pin compatibility with NMOS Super8*



Z8® NMOS MICROCONTROLLERS

Z8600 NMOS Z8 MICROCONTROLLER

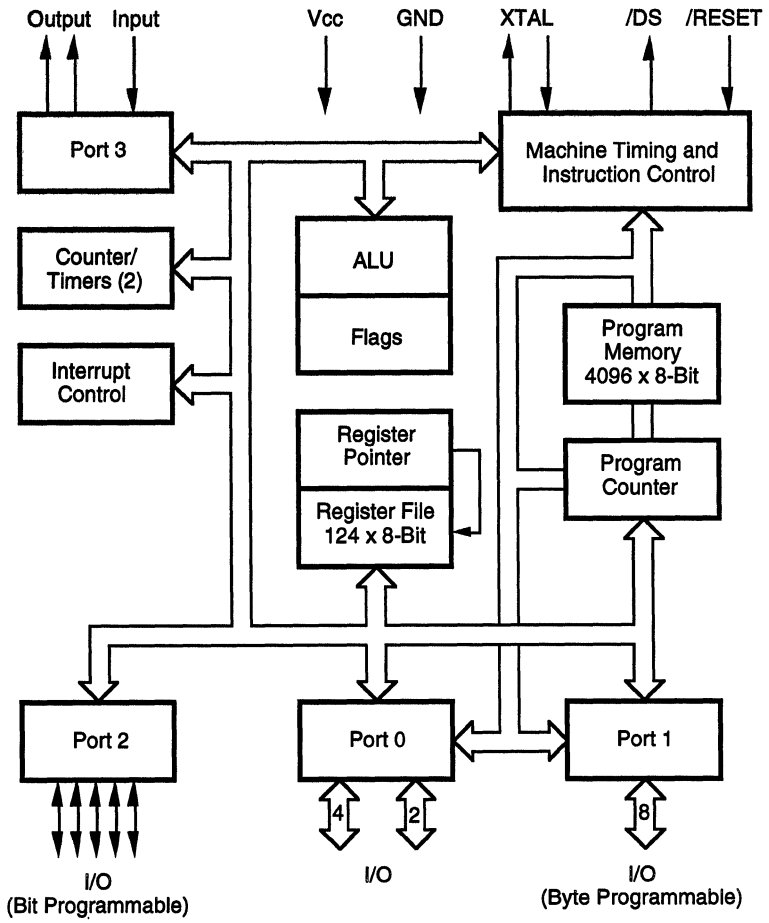
GENERAL DESCRIPTION

The Z8600 microcontroller introduces a new level of sophistication to single-chip microcontrollers. The Z8600 offers fast execution, efficient use of memory, sophisticated interrupt and bit manipulation capabilities, and easy system expansion.

Under program control, the MCU can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 2 Kbytes of internal ROM. In all configurations, a large number of pins remain available for I/O. The MCU is offered in a 28-pin DIP package.

FEATURES

- *Complete Microcontroller, 2 Kbytes of ROM, 124 Bytes of RAM, and 22 I/O Lines.*
- *142-Byte Register File, Including 124 General-Purpose Registers, Four I/O Port Registers, and 14 Status and Control Registers.*
- *Vectored, Priority Interrupts for I/O and Counter/Timers*
- *Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *Register Pointer so that Short, Fast Instructions can Access any One of the Nine Working Register Groups.*
- *On-Chip Oscillator that Accepts Crystal or External Clock Drive*
- *Clock Speed: 8 MHz*
- *Single +5V Power Supply, all Pins TTL-Compatible*
- *28-Pin DIP Package*



GENERAL DESCRIPTION

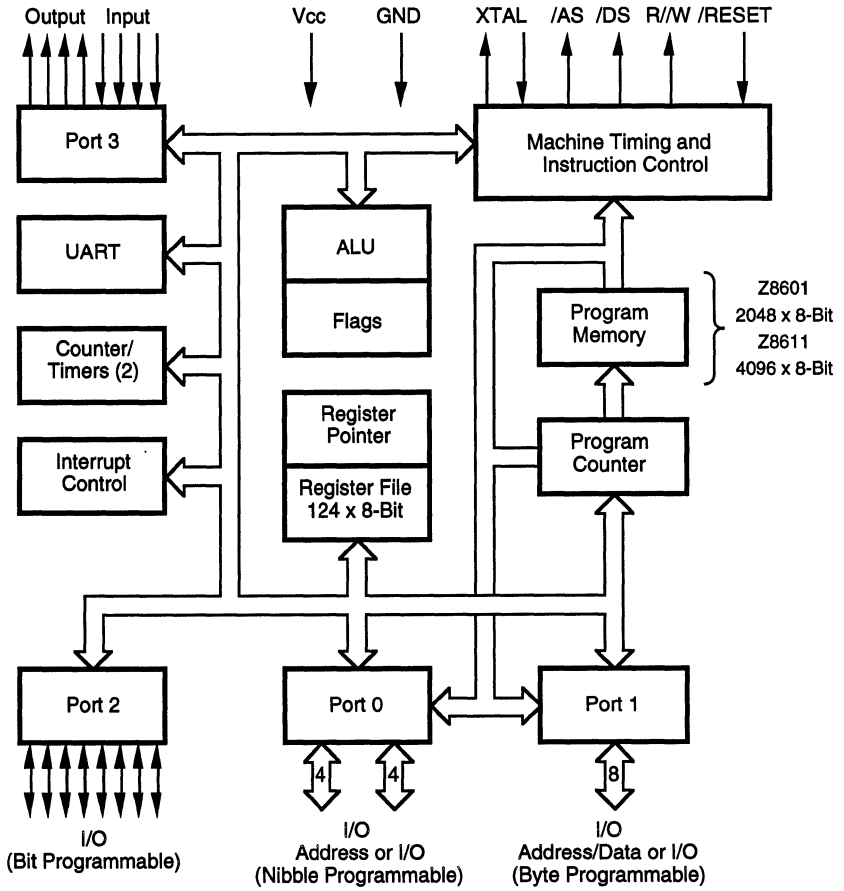
The Z8® microcontroller introduces a new level of sophistication to single-chip architecture. Compared to earlier single-chip microcontrollers, the Z8 offers faster execution, more efficient use of memory, more sophisticated interrupt, input/output, bit-manipulation capabilities, and easier system expansion.

Under program control, the Z8 can be tailored to the needs of its user. It can be configured as a stand-alone microcontroller with 2 or 4 Kbytes of internal ROM, a traditional microprocessor that manages up to 124 Kbytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-Bus®. In all configurations, a large number of pins remain available for I/O.

The Z8603 and Z8613 protopacks are used for prototype development and production of mask-programmed applications. The protopacks are ROMless versions of the Z8601 (Z8603) and Z8611 (Z8613) housed in a pin compatible 40-pin piggyback package.

FEATURES

- *Complete Microcontroller, 2K (8601) or 4K (8611) Bytes of ROM, 124 Bytes of RAM, 32 I/O Lines, and up to 62 (8601) or 60 (8611) Kbytes Addressable External Space each for Program and Data Memory.*
- *144-Byte Register File, Including 124 General-Purpose Registers, Four I/O Port Registers, and 16 Status and Control Registers.*
- *Vectored, Priority Interrupts for I/O, Counter/Timers, and UART*
- *Full-Duplex UART and Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *Register Pointer so that Short, Fast Instructions can Access Any of Nine Working Register Groups in 1 µs.*
- *On-Chip Oscillator Which Accepts Crystal or External Clock Drive.*
- *Single +5V Power Supply, all Pins TTL Compatible*
- *Clock Speeds: 8 and 12 MHz*



Z8602 NMOS 2K KEYBOARD CONTROLLER

GENERAL DESCRIPTION

The Z8602 Keyboard Controller (KBC) introduces a new level of sophistication to single-chip architecture. The Z8602 is a member of the Z8® single-chip microcontroller family with 2 Kbytes of ROM.

The Z8602 KBC is housed in a 40-pin DIP package, and is manufactured in NMOS technology. It offers fast execution, more efficient use of memory, more sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

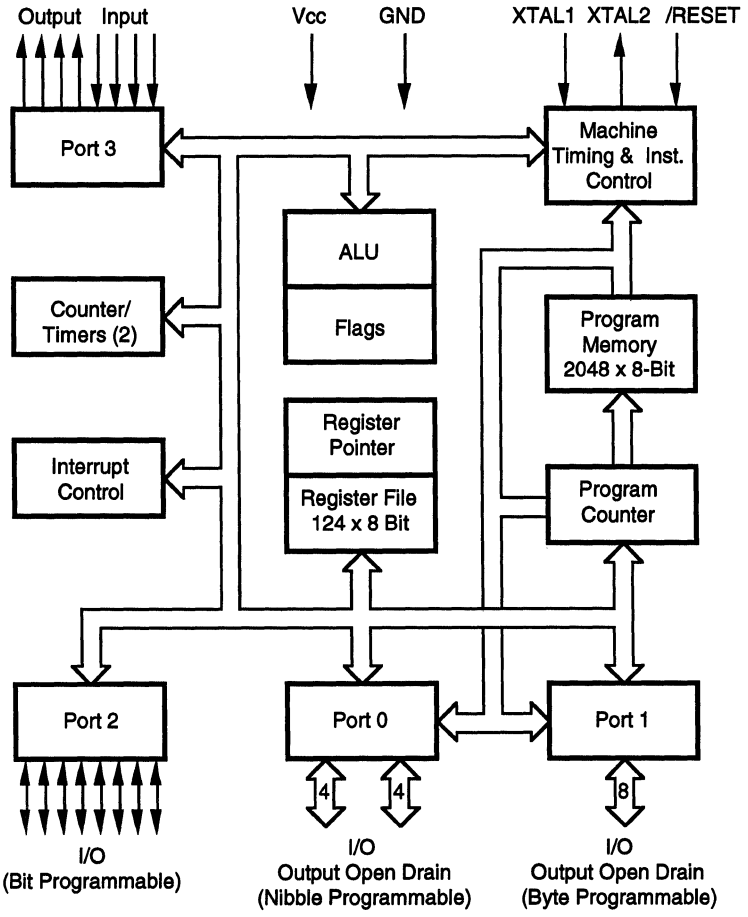
The KBC architecture is characterized by a flexible I/O feature, an efficient register I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The Z8602 offers low EMI emission achieved by means of several modifications in the output drivers and clock circuitry of the device.

The device is optimized for keyboard control and scan functions. Software is available under license from Zilog to perform keyboard control functions. See Zilog Application Note DC-2521-01: "Z8602 Controls a 101/102 PC/Keyboard."

FEATURES

- *8-Bit Microcontroller, 40-Pin DIP Package*
- *Low Cost*
- *+4.75 to +5.25 V_{cc} Range*
- *Low Power Consumption - 750 mW*
- *Fast Instruction Pointer - 1.5 µs at 4 MHz*
- *32 Input/Output Lines*
- *All Digital Inputs NMOS Levels*
- *2 Kbytes ROM*
- *124 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Eight Different Sources*
- *Clock Speeds up to 4 MHz*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator or External Clock Drive*
- *Low EMI Emission*



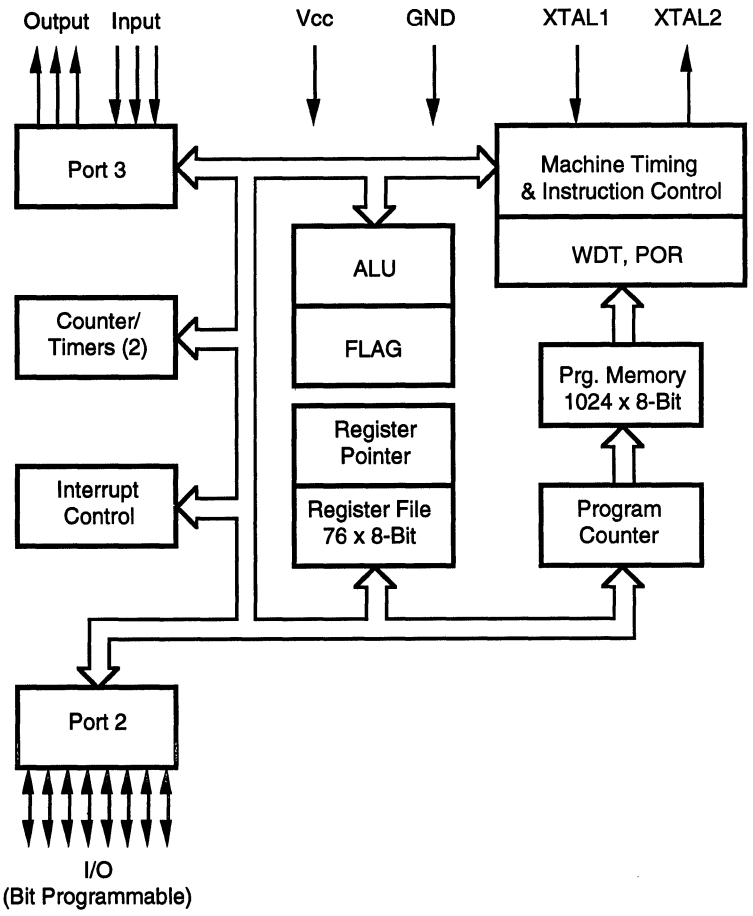
GENERAL DESCRIPTION

The Z8604 is a single chip microcontroller with 1 Kbytes of ROM. It offers all the outstanding features of the Z8® family architecture in a low cost, 18-pin plastic DIP for price and size sensitive designs.

The Z8604 architecture employs the powerful Z8 microcontroller core. The device has instruction compatibility with the entire Z8 family for easy software/hardware system expansion. The device is ideal for cost sensitive consumer applications. It can operate with low cost RC type oscillators as well as ceramic/crystal oscillators.

FEATURES

- *Complete NMOS microcomputer with 14 I/O lines and 1K bytes of on-chip ROM.*
- *The register file is composed of 76 general purpose registers, 2 I/O port registers and 4 control and status registers.*
- *Two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.*
- *On-chip oscillator that accepts a crystal, ceramic resonator, RC, or external clock drive.*
- *All inputs are TTL compatible and Schmitt triggered*
- *Watch Dog/Power-On Reset timer*
- *Fast instruction pointer, 1.5 microseconds at 8 MHz*
- *Clock speeds up to 8 MHz*
- *4.50 to 5.50 volts operating range*
- *Six vectored, priority interrupts from five different sources*
- *18-pin DIP package*
- *Pin compatible with Z86C06 18-pin CMOS MCU.*



Z8614 NMOS 4K KEYBOARD CONTROLLER

GENERAL DESCRIPTION

The Z8614 Keyboard Controller (KBC) introduces a new level of sophistication to single-chip architecture. The Z8614 is a member of the Z8® single-chip microcontroller family with 4 Kbytes of ROM.

The Z8614 KBC is housed in a 40-pin DIP package, and is manufactured in NMOS technology. It offers fast execution, more efficient use of memory, more sophisticated interrupt, input/output bit-manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

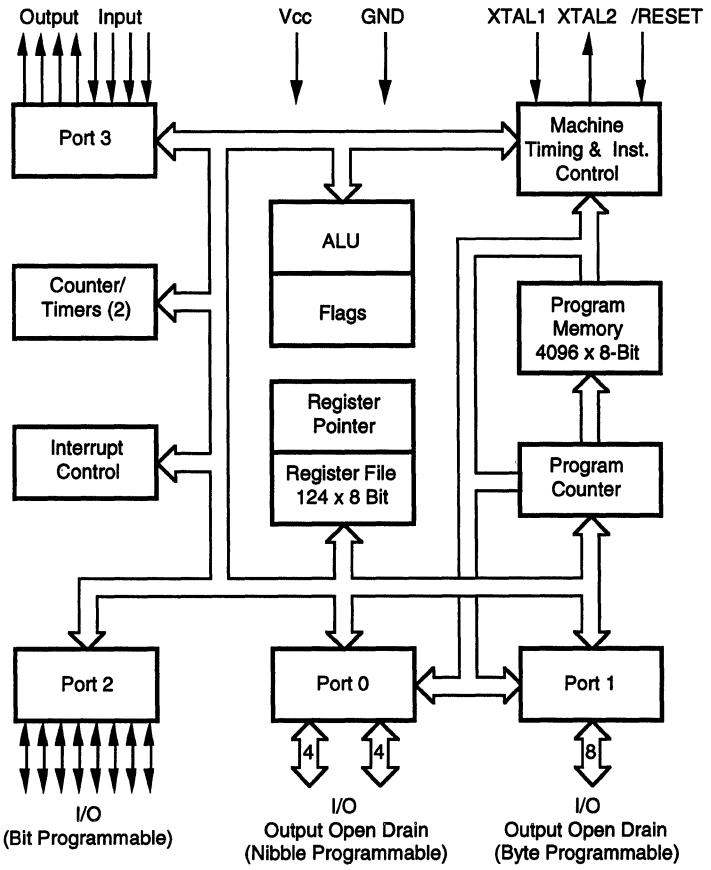
The KBC architecture is characterized by a flexible I/O feature, an efficient register I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

The Z8614 offers low EMI emission achieved by means of several modifications in the output drivers and clock circuitry of the device.

The device is optimized for keyboard control and scan functions. Software is available under license from Zilog to perform keyboard control functions. See Zilog Application Note DC-2521-01: "Z8602 Controls a 101/102 PC/Keyboard."

FEATURES

- *8-Bit Microcontroller, 40-Pin DIP Package*
- *Low Cost*
- *+4.75 to +5.25 V_{cc} Range*
- *Low Power Consumption - 750 mW*
- *Fast Instruction Pointer - 1.5 µs at 4 MHz*
- *32 Input/Output Lines*
- *All Digital Inputs NMOS Levels*
- *4 Kbytes ROM*
- *124 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers each with 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Eight Different Sources*
- *Clock Speeds up to 4 MHz*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator or External Clock Drive*
- *Low EMI Emission*



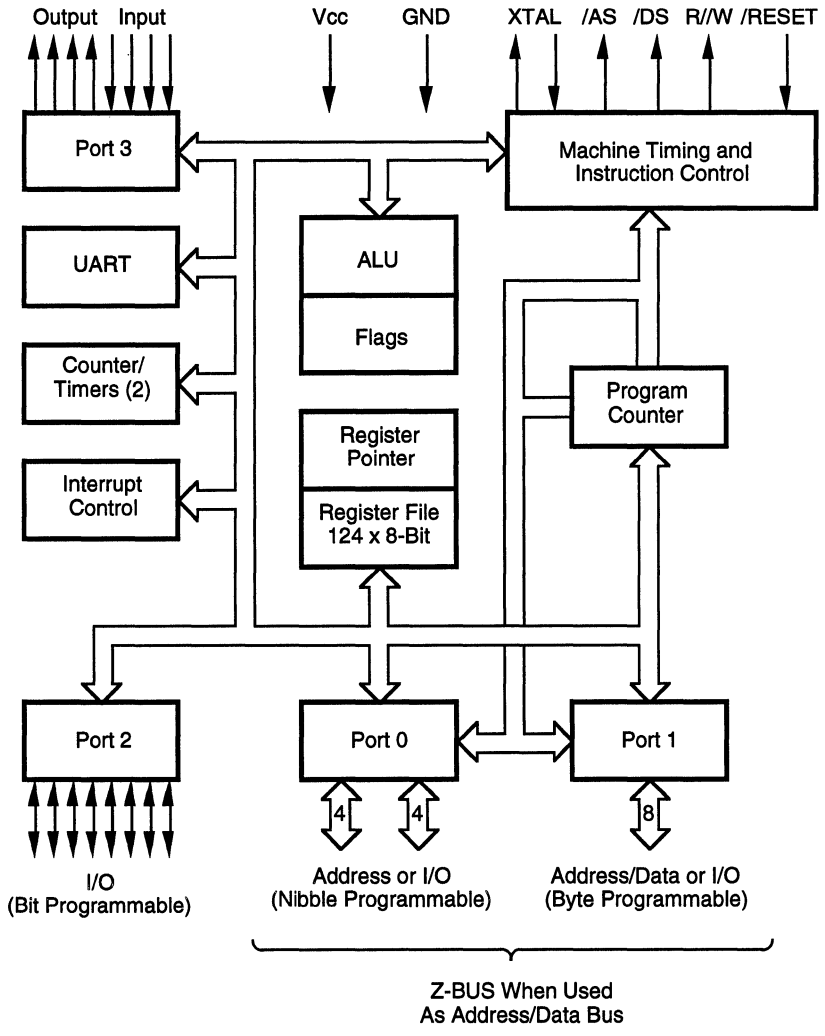
GENERAL DESCRIPTION

The Z8681 is a ROMless versions of the Z8 single-chip microcomputer. It can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

There are 143 registers located on-chip organized as 124 general purpose registers, 16 control and status registers, and three I/O registers. Register file can be divided into nine groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

FEATURES

- *Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.*
- *143-byte register file, including 124 general purpose registers, three I/O port registers, and 16 status and control registers.*
- *Vectored, priority interrupts for I/O, counter/timers, and UART*
- *On-chip oscillator that accepts crystal or external clock drive*
- *Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.*
- *Register Pointer so that short, fast instructions can access any one of the nine working-register groups.*
- *Single +5V power supply; all I/O pins TTL compatible*
- *Clock speeds: 8 MHz and 12 MHz*
- *Military version available*



Z8691 NMOS Z8 ROMLESS MICROCONTROLLER

GENERAL DESCRIPTION

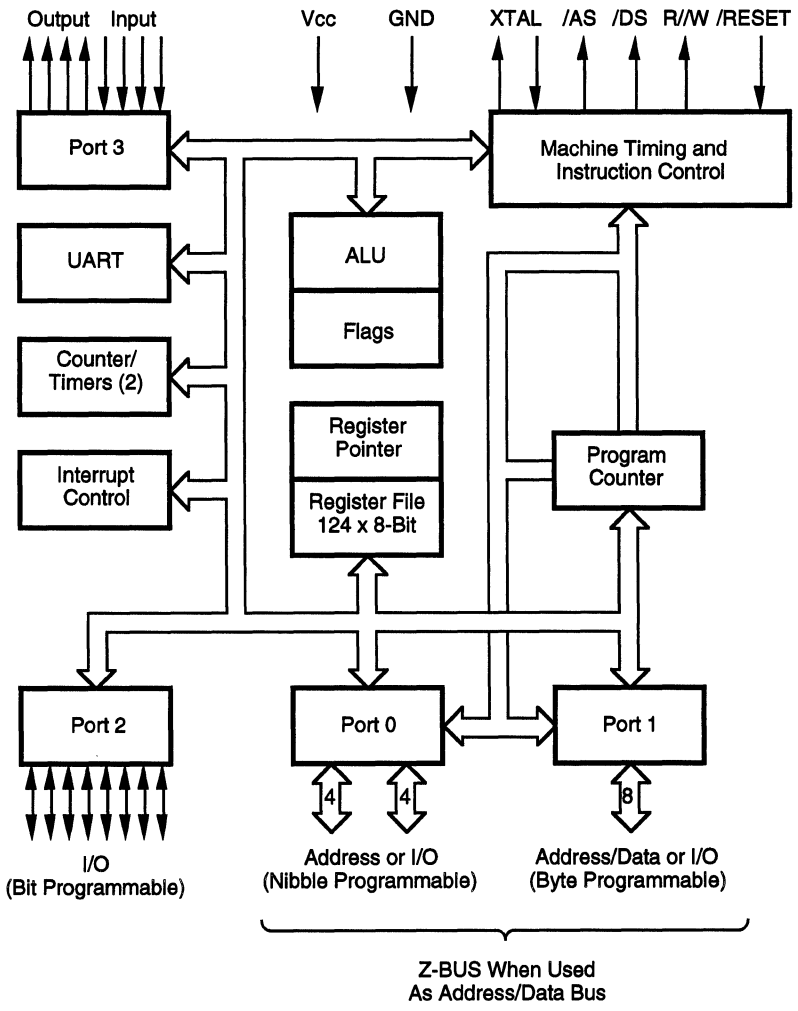
The Z8691 is a ROMless version of the Z8 single-chip microcomputer. The Z8691 offers all the outstanding features of the Z8 family architecture except an on-chip program ROM. Use of external memory rather than a preprogrammed ROM enables this Z8 microcomputer to be used in low volume applications or where code flexibility is required.

The Z8691 can provide up to 16 output address lines, thus permitting an address space of up to 64K bytes of data or program memory. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits can be provided by the software configuration of Port 0 to output address bits A15-A8.

There are 143 registers located on-chip organized as 124 general purpose registers, 16 control and status registers, and 3 I/O port registers. Register file can be divided into 9 groups of 16 working registers each. Configuring the register file in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly.

FEATURES

- *Complete microcomputer, 24 I/O lines, and up to 64K bytes of addressable external space each for program and data memory.*
- *143-byte register file, including 124 general purpose registers, three I/O port registers, and 16 status and control registers.*
- *Vectored, priority interrupts for I/O, counter/timers, and UART.*
- *On-chip oscillator that accepts crystal or external clock drive*
- *Full-duplex UART and two programmable 8-bit counter/timers, each with a 6-bit programmable prescaler.*
- *Register Pointer so that short, fast instructions can access any one of the nine working-register groups.*
- *Single +5V power supply, all I/O pins TTL compatible*
- *Clock speeds: 8 MHz and 12 MHz*



DIGITAL SIGNAL PROCESSORS

Z86C95 CMOS Z8 DIGITAL SIGNAL PROCESSOR

GENERAL DESCRIPTION

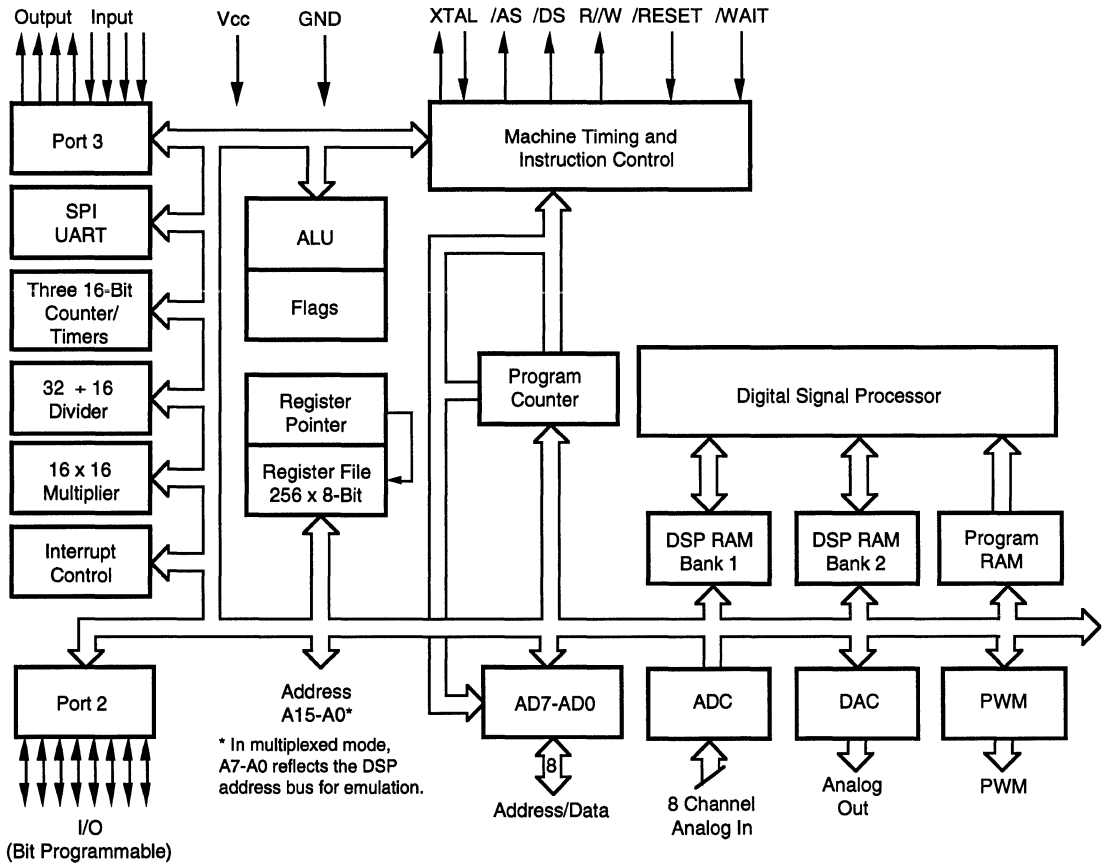
The Z86C95 MCU introduces a new level of sophistication for Superintegration™ ICs. The Z86C95 is a member of the Z8 single-chip microcontroller family incorporating a CMOS ROMless Z8 microcontroller with an embedded DSP processor for digital servo control. The DSP slave processor can perform 16-bit by 16-bit multiply and accumulate in one clock cycle. Additionally, the Z86C95 is further enhanced with a hardwired 16-bit by 16-bit multiplier and 32-bit/16-bit divider, three 16-bit counter timers with capture and compare registers, a half flash 8-bit A/D converter with a 2 µsec conversion time, an 8-bit DAC with 1/4 programmable gain stage, UART, serial peripheral interface, and a PWM output channel. It is fabricated using 1.2 micron CMOS technology and offered in an 80-pin QFP, 84-pin PLCC package, or a 100-pin VQFP.

The Z86C95 provides up to 16 output address lines. This permits an address space of up to 64 Kbytes of data and program memory each. Eight address outputs (AD7-AD0) are provided by a multiplexed, 8-bit, Address/Data bus. The remaining 8 bits are provided via output address bits A15-A8.

There are 256 registers located on chip and organized as 236 general-purpose registers, 16 control and status registers, and four I/O port registers. The register file can be divided into sixteen groups of 16 working registers each. Configuration of the registers in this manner allows the use of short format instructions; in addition, any of the individual registers can be accessed directly. The Z86C95 contains 512 bytes of DSP Program RAM and 256 bytes of DSP data RAM.

FEATURES

- *Complete Microcontroller, 16 I/O Lines, and up to 64 Kbytes of Addressable External Space each for Program and Data Memory.*
- *Embedded Reduced Instruction set DSP (Digital Signal Processor) for Digital Servo Control, with 16-Bit by 16-Bit Multiply and Accumulate in One Clock Cycle.*
- *8-Channel, 8-Bit A/D Converter with Track and Hold and Minimum Single Conversion Time of 2 µsec.*
- *8-Bit D/A Converter with 1/4 Programmable Gain Stage and a Maximum Settling Time of 3 µsec.*
- *Single Channel 40/80 kHz Pulse Width Modulator*
- *256-Byte Register File, Including 236 General-Purpose Registers, Four I/O Port Registers and 16 Status and Control Registers.*
- *16-Bit by 16-Bit Hardwired Multiply and 32-Bit by 16-Bit Divide, Exclusive of DSP.*
- *Four External Vectored Priority Interrupts for I/O, Counter/Timers and UART.*
- *On-Chip Oscillator that Accepts Crystal or External Clock Drive.*
- *Full-Duplex UART*
- *16-Bit Counter/Timers with Capture and Compare Registers.*
- *Register Pointer for Short, Fast Instructions to any One of the Sixteen Working Register Groups.*
- *Serial Peripheral Interface*
- *Multiplexed and Demultiplexed Address/Data Bus*
- *Single +5V Power Supply, all I/O Pins TTL Compatible*
- *1.2 Micron CMOS Technology*
- *Clock Speeds - 20 and 24 MHz*
- *Three Low-Power Standby Modes; STOP, HALT and PAUSE*
- *Flash EPROM Write Support*


Output
Input
Vcc
GND
XTAL
/AS
/DS
R/W
/RESET
/WAIT
Port 3
SPI
UART
Three 16-Bit
Counter/
Timers
32 ÷ 16
Divider
16 x 16
Multiplier
Interrupt
Control
Machine Timing and
Instruction Control
ALU
Flags
Register
Pointer
Register File
256 x 8-Bit
Program
Counter
Digital Signal Processor
DSP RAM
Bank 1
DSP RAM
Bank 2
Program
RAM
Port 2
I/O
(Bit Programmable)
Address
A15-A0*
* In multiplexed mode,
A7-A0 reflects the DSP
address bus for emulation.
AD7-AD0
8
Address/Data
ADC
8 Channel
Analog In
DAC
Analog
Out
PWM
PWM

Z89C00 CMOS 16-BIT DIGITAL SIGNAL PROCESSOR

GENERAL DESCRIPTION

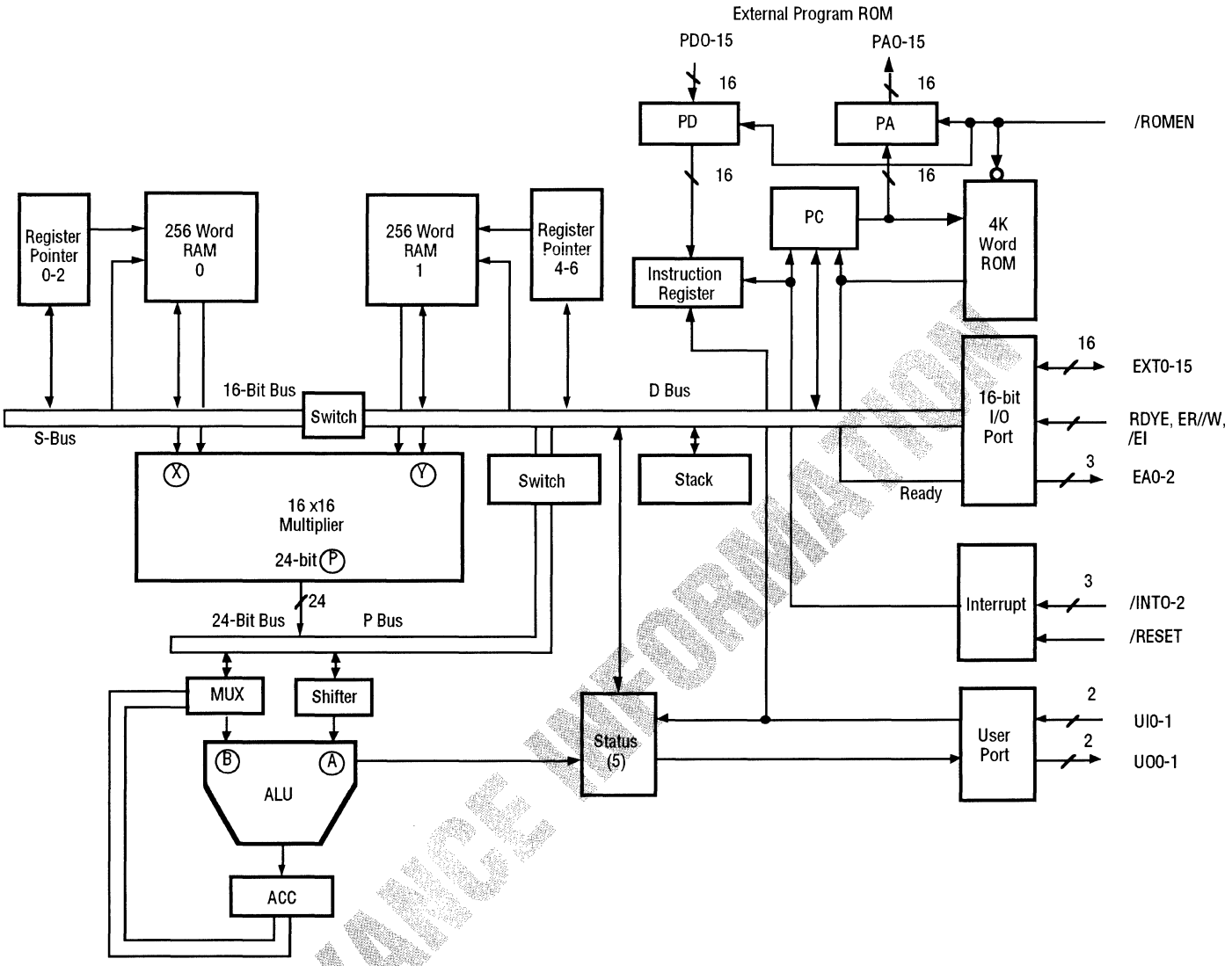
The Z89C00 is a second generation, 16-bit, fractional, two's complement CMOS Digital Signal Processor (DSP). Most instructions, including multiply and accumulate, are accomplished in a single clock cycle. The processor contains 1Kbyte on-chip data RAM (two blocks of 256 16-bit words), a 4 Kword program ROM and a 64 Kword program memory address space. Also, the processor features a 24-bit ALU, a 16x16 multiplier, a 24-bit Accumulator and a shifter. Additionally, the processor contains a six-level stack, three vectored interrupts and two inputs for conditional program jumps. Each RAM block contains a set of three pointers which may be incremented or decremented automatically to affect hardware looping without software overhead. The data RAMs can be simultaneously addressed and loaded to the multiplier for a true single cycle scalar multiply.

There is a 16-bit address and data bus for external program/data memory, and a 16-bit I/O bus for transferring data or for mapping peripherals into the processor address space. Additionally, there are two general purpose user inputs and two user outputs. Operation with slow peripherals is accomplished with a ready input pin.

Development tools for the IBM® PC include a relocatable assembler, a linker loader, and an ANSI-C compiler. Also, the development tools include a simulator/debugger, a cross assembler for the TMS320 family assembly code and a hardware emulator.

FEATURES

- *16-Bit Single Cycle Instructions*
- *Zero Overhead Hardware Looping*
- *16-Bit Data*
- *Ready Control for Slow Peripherals*
- *Single Cycle Multiply/Accumulate (100 ns)*
- *Six-Level Stack*
- *512 Words of On-Chip RAM*
- *16-Bit I/O Port*
- *4 Kwords of On-Chip Masked ROM*
- *Three Vectored Interrupts*
- *64K Words of External Address Space*
- *Two Conditional Branch Inputs/Two User Outputs*
- *24-Bit ALU, Accumulator and Shifter*
- *IBM® PC Development Tools*



Z89C65/C66 TELEPHONE ANSWERING DEVICE CONTROLLER

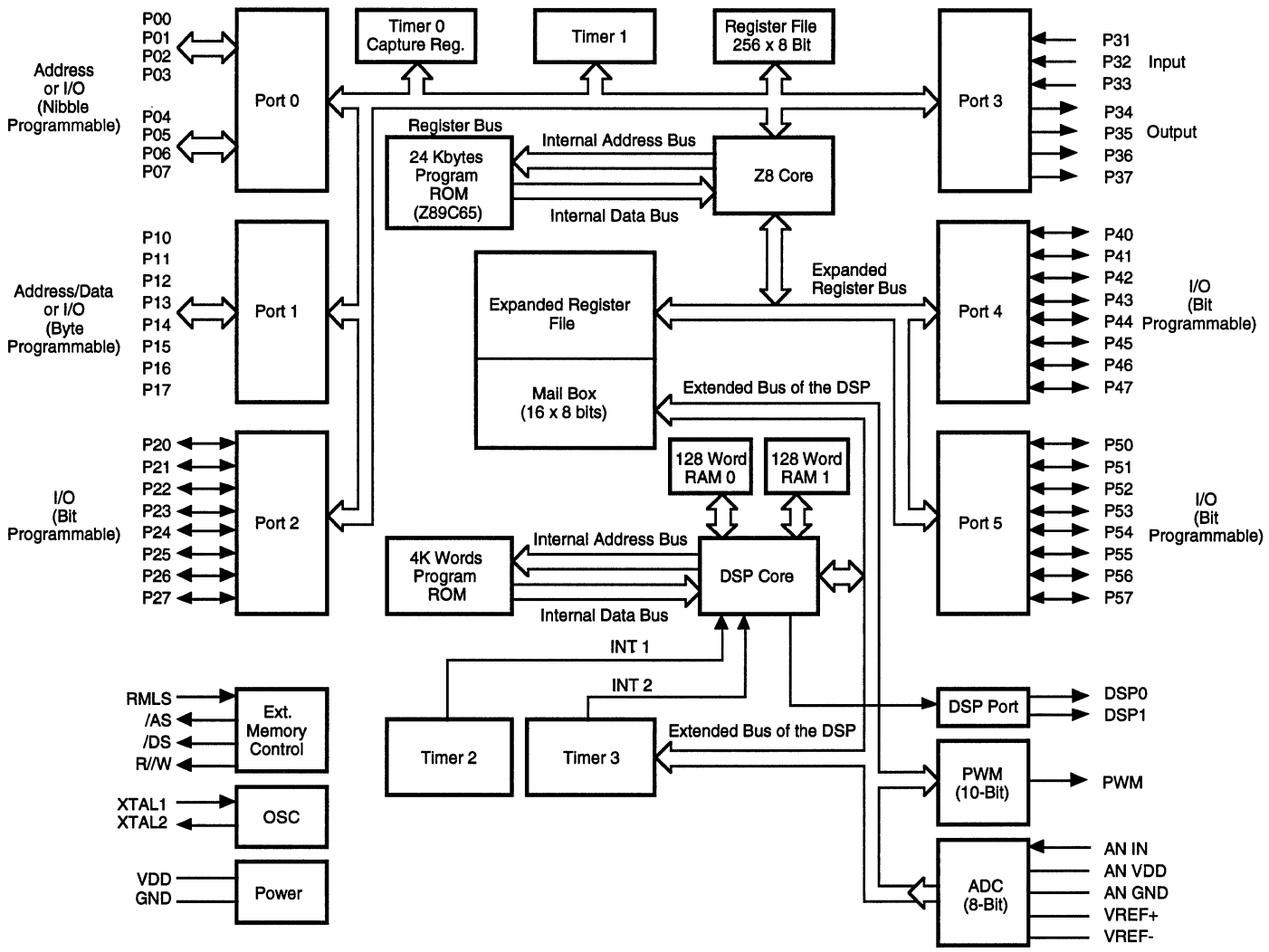
GENERAL DESCRIPTION

The Z89C65 and Z89C66 are fully integrated, dual processor controllers designed for telephone answering machines. The I/O control processor is a Z8® with 24 Kbytes of program memory (ROMless for the Z89C66), two 8-bit counter timers, and up to 47 I/O pins (31 I/O pins for the Z89C66). The DSP is a 16-bit processor with a 24-bit ALU and accumulator, 512 x 16 bits of RAM, single cycle instructions, and 4K word program ROM plus constants memory. The chip also contains a half-flash 8-bit A/D converter with up to 128 kHz sample rate and 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D may be extended by resampling the data at a lower rate in software.

The Z8 and DSP processors are loosely coupled by mailbox registers and an interrupt system. DSP or Z8 programs may be directed by events in each other's domain.

FEATURES

- *Z8® Microcontroller with 47 I/O Lines*
- *24 Kbytes of Z8 Program ROM (Z89C65)*
- *256 Bytes On-Chip Z8 RAM*
- *Watch-Dog Timer and Power-On Reset*
- *Low Power STOP Mode*
- *On-Chip Oscillator which Accepts a Crystal or External Clock Drive*
- *2x8-Bit Z8 Counter Timers with 6-Bit Prescaler*
- *Global Power-Down Mode*
- *Low-Power Consumption - 200 mW (Typical)*
- *Brown-Out Protection*
- *Two Comparators with Programmable Interrupt Priority*
- *Six Vectored, Priority Interrupts*
- *RAM and ROM Protect*
- *Clock Speed: 20.48 MHz*
- *Z89C00 Core 16-Bit Digital Signal Processor (DSP)*
- *4K word DSP Program ROM*
- *512 Words On-Chip DSP RAM*
- *8-Bit A/D Converter with up to 128 kHz Sample Rate*
- *10-Bit PWM D/A Converter (4 kHz to 64 kHz)*
- *Two DSP Timers to Support Different A/D and D/A Sampling Rates*
- *Hardware Modulo Addressing for Looping*
- *16-Bit Single Cycle DSP Instructions*
- *16-Bit Single Cycle DSP Multiply/Accumulate*
- *Six-Level DSP Stack*
- *24-Bit DSP ALU, Accumulator and Shifter*
- *Three Vectored DSP Interrupts*
- *Independent Z8 and DSP Operations*
- *IBM® PC-Based Development Tools*
- *Developer's Toolbox for T.A.M. Applications*


P00
P01
P02
P03
P04
P05
P06
P07
Address or I/O (Nibble Programmable)
Port 0
Timer 0 Capture Reg.
Timer 1
Register File 256 x 8 Bit
Port 3
P31
P32 Input
P33
P34
P35 Output
P36
P37
Register Bus
24 Kbytes Program ROM (Z89C65)
Internal Address Bus
Internal Data Bus
Z8 Core
P10
P11
P12
P13
P14
P15
P16
P17
Address/Data or I/O (Byte Programmable)
Port 1
Expanded Register File
Mail Box (16 x 8 bits)
Expanded Register Bus
Port 4
P40
P41
P42
P43
P44
P45
P46
P47
I/O (Bit Programmable)
Extended Bus of the DSP
P20
P21
P22
P23
P24
P25
P26
P27
I/O (Bit Programmable)
Port 2
128 Word RAM 0
128 Word RAM 1
Port 5
P50
P51
P52
P53
P54
P55
P56
P57
I/O (Bit Programmable)
4K Words Program ROM
Internal Address Bus
Internal Data Bus
DSP Core
INT 1
INT 2
RMLS
/AS
/DS
R/W
Ext. Memory Control
Timer 2
Timer 3
Extended Bus of the DSP
DSP Port
DSP0
DSP1
PWM (10-Bit)
PWM
XTAL1
XTAL2
OSC
ADC (8-Bit)
AN IN
AN VDD
AN GND
VREF+
VREF-
VDD
GND
Power

Z89C67/C68 TAPELESS TELEPHONE ANSWERING DEVICE CONTROLLER

GENERAL DESCRIPTION

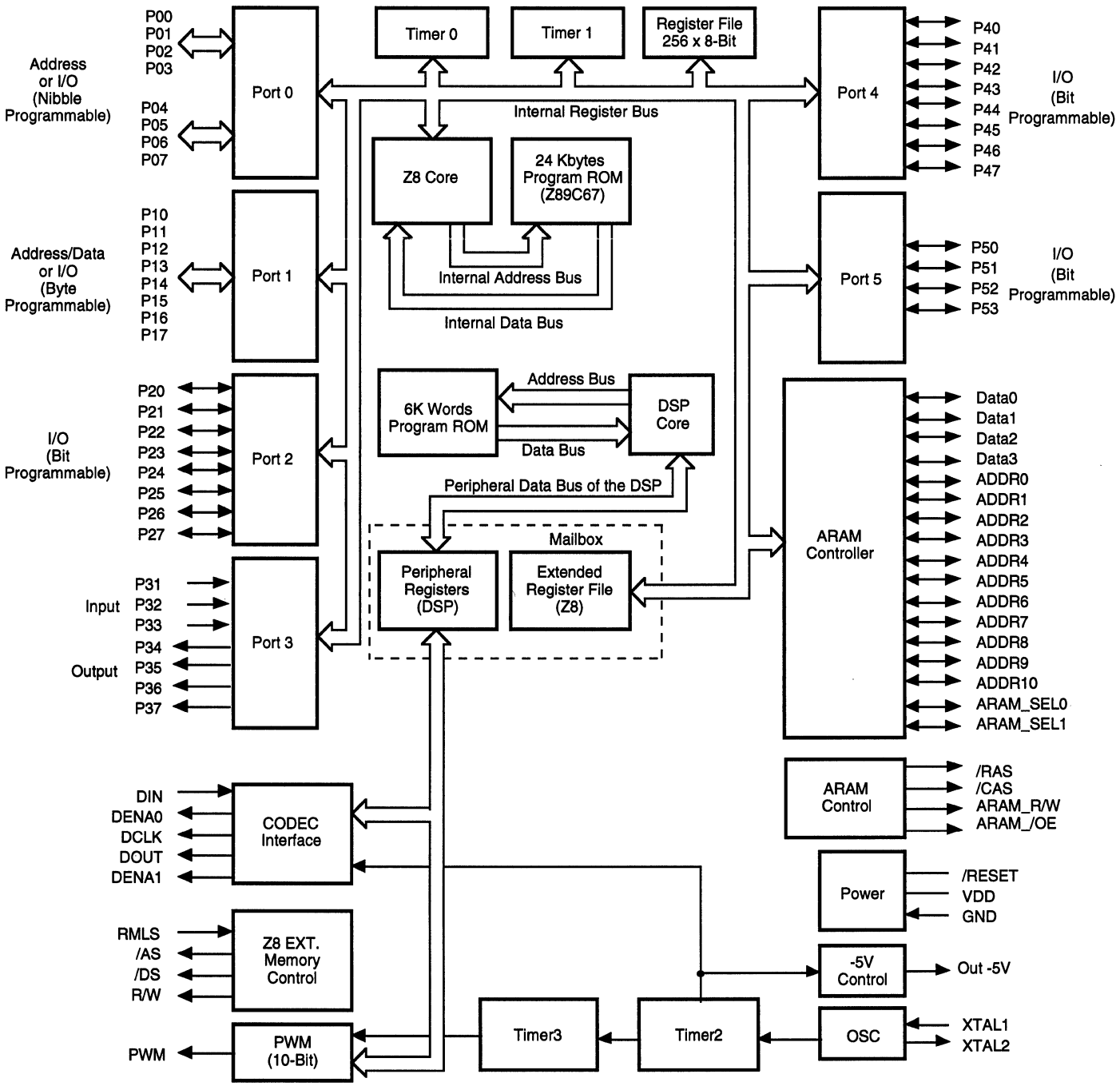
The Z89C67 and Z89C68 are fully integrated dual-processor controllers designed for Tapeless Telephone Answering Machine Applications (TTAM). The I/O control processor is a Z8® with 24 Kbytes of program memory (ROMless for the Z89C68), 256-byte register file, two 8-bit counter/timers with 6-bit prescalers, two analog comparators, 43 I/O pins (27 I/O pins for the Z89C68), low power stop mode, watch-dog timer, RAM and ROM protect, brown-out protection, six vectored interrupt with programmable priority interrupts, and on-chip oscillator that accepts 20.48 MHz crystal.

The DSP operates in parallel with the Z8. The inter-processor communication is achieved by mailbox registers and the Z8-DSP interrupt system.

For high-end TTAM applications, interface for CODECs, 48 Mbit ARAM/ DRAM interface with 4-bit wide data bus configuration, 10-bit Pulse Width Modulator for LPC speech synthesis and high quality tone generation are also found on-chip. IBM® PC-based development tools and developer's toolbox for TTAM applications are available.

FEATURES

- Z89C67 has 24 Kbytes of Program ROM while the Z89C68 is a ROMless Device.
- 84-Pin PLCC Package
- Masked ROM (Z89C67)
- Fully Static Low Power CMOS
- Dual-Processor Architecture with a Z8 Microcontroller and a DSP
- Low Power STOP Mode
- Watch-Dog Timer and Power-On Reset
- 256-Byte Register File
- 6K Word DSP ROM
- 43 I/O Pins (27 I/O Pins for the Z86C68)
- One Interface for Two Codecs with 8 kHz Sampling Rate and 2.048 MHz Clock
- 2x8-Bit Z8 Counter Timers with 6-Bit Prescalers
- 10-bit PWM with Sampling Frequency from 4 kHz up to 64 kHz for Speech Generation
- 43 Programmable I/O Pins
- ARAM Interface for up to 48 Mbit ARAM with 4-bit wide data bit.
- -5V Charge Pump Control Circuit
- Two DSP Timers to Support Different Sampling Rates for the Codecs and PWM
- 20.48 MHz Oscillator
- PC Based Development Tools
- Developer's software for tapeless T.A.D. Applications


Address or I/O (Nibble Programmable)
P00
P01
P02
P03
P04
P05
P06
P07
Port 0
Timer 0
Timer 1
Register File 256 x 8-Bit
Internal Register Bus
Z8 Core
24 Kbytes Program ROM (Z89C67)
Internal Address Bus
Internal Data Bus
Port 4
P40
P41
P42
P43
P44
P45
P46
P47
I/O (Bit Programmable)
Address/Data or I/O (Byte Programmable)
P10
P11
P12
P13
P14
P15
P16
P17
Port 1
Port 5
P50
P51
P52
P53
I/O (Bit Programmable)
I/O (Bit Programmable)
P20
P21
P22
P23
P24
P25
P26
P27
Port 2
6K Words Program ROM
Address Bus
Data Bus
DSP Core
Peripheral Data Bus of the DSP
Mailbox
Peripheral Registers (DSP)
Extended Register File (Z8)
ARAM Controller
Data0
Data1
Data2
Data3
ADDR0
ADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
ADDR7
ADDR8
ADDR9
ADDR10
ARAM_SEL0
ARAM_SEL1
Input
Output
P31
P32
P33
P34
P35
P36
P37
Port 3
ARAM Control
/RAS
/CAS
ARAM_R/W
ARAM_/OE
DIN
DENA0
DCLK
DOUT
DENA1
CODEC Interface
Power
/RESET
VDD
GND
RMLS
/AS
/DS
R/W
Z8 EXT. Memory Control
-5V Control
Out -5V
PWM
PWM (10-Bit)
Timer3
Timer2
OSC
XTAL1
XTAL2

Z89120 16-BIT MIXED SIGNAL PROCESSOR

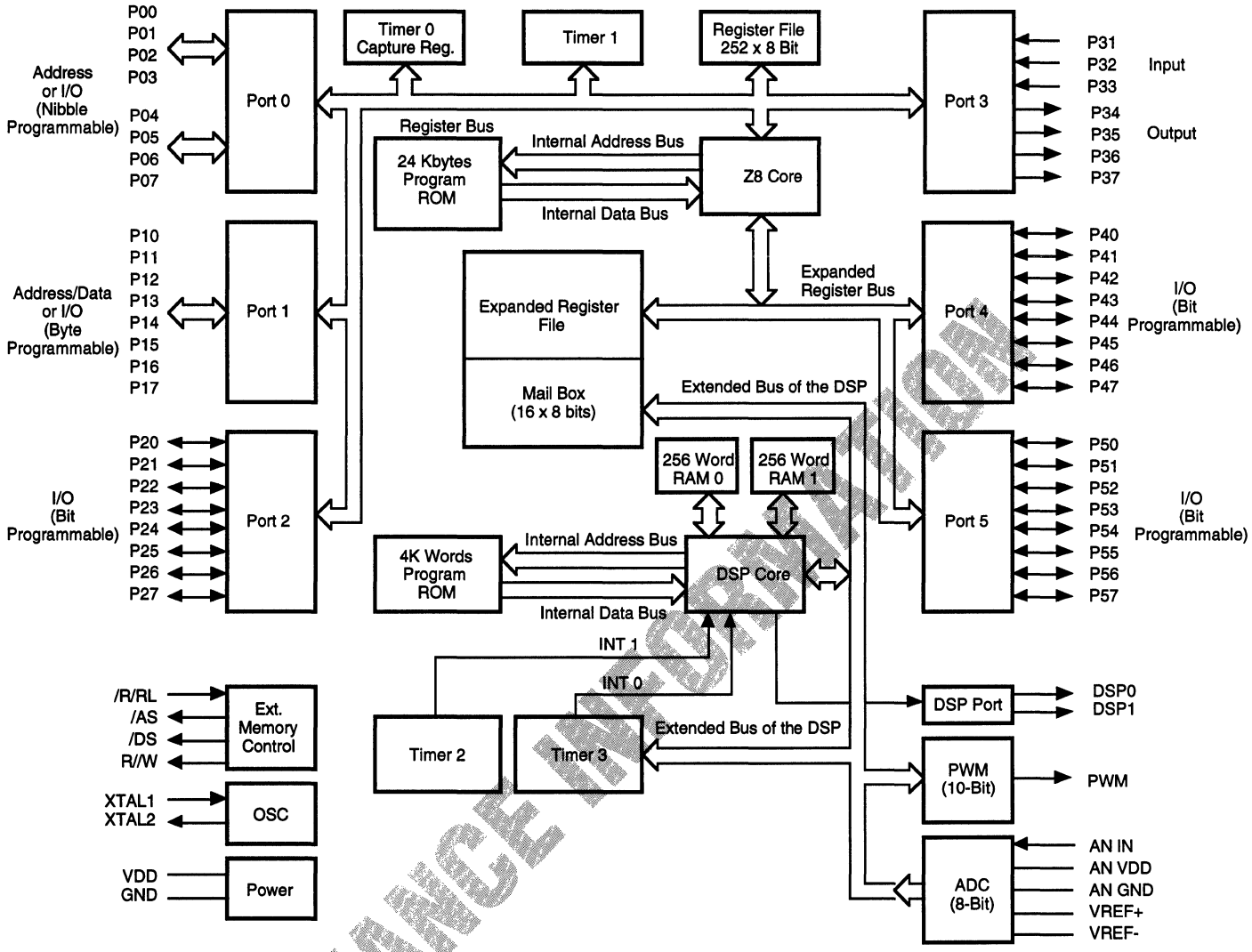
GENERAL DESCRIPTION

The Z89120/920 is a fully integrated, mixed signal, dual processor chip system designed for lower sample rates such as audio, telephone, security systems, modem, faxes, instrumentation, noise cancellation, and sonar. The I/O control processor is a Z8® with 24 Kbytes of program memory, two 8-bit counter timers, and up to 47 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and Accumulator, 512x16 bits of RAM, single cycle instructions, and 4K word program ROM plus constants memory. The chip also contains a half-flash 8-bit A/D converter with up to 128 kHz sample rate and 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D may be extended by resampling the data at a lower rate in software.

The Z8 and DSP processors are loosely coupled by mailbox registers and an interrupt system. DSP or Z8 programs may be directed by events in each other's domain.

FEATURES

- *Z8® Microcontroller with 47 I/O Lines*
- *24 Kbytes of Z8 Program ROM*
- *256 Bytes On-Chip Z8 RAM*
- *Watch-Dog Timer and Power-On Reset*
- *Low Power Stop Mode*
- *On-Chip Oscillator which Accepts a Crystal or External Clock Drive*
- *2x8 Bit Z8 Counter Timers with 6-Bit Prescaler*
- *Global Power-Down Mode*
- *Low-Power Consumption - 200 mW (typical)*
- *Brown-Out Protection*
- *Two Comparators with Programmable Interrupt Priority*
- *Six Vectored, Priority Interrupts*
- *RAM and ROM Protect*
- *Clock Speed of 20.48 MHz*
- *Z89C00 Core 16-Bit Digital Signal Processor (DSP)*
- *4 Kword DSP Program ROM*
- *512 words On-Chip DSP RAM*
- *8-Bit A/D Converter with up to 128 kHz Sample Rate*
- *10-Bit PWM D/A Converter (4 kHz to 64 kHz)*
- *Two DSP Timers to Support Different A/D and D/A Sampling Rates*
- *Zero Overhead Hardware Looping*
- *16-Bit Single Cycle DSP Instructions*
- *16-Bit Single Cycle DSP Multiply/Accumulate*
- *Six-Level DSP Stack*
- *24-Bit DSP ALU, Accumulator and Shifter*
- *Three Vectored DSP Interrupts*
- *Independent Z8 and DSP Operations*
- *IBM® PC-Based Development Tools*



Z89920 16-BIT MIXED SIGNAL PROCESSOR (ROMLESS)

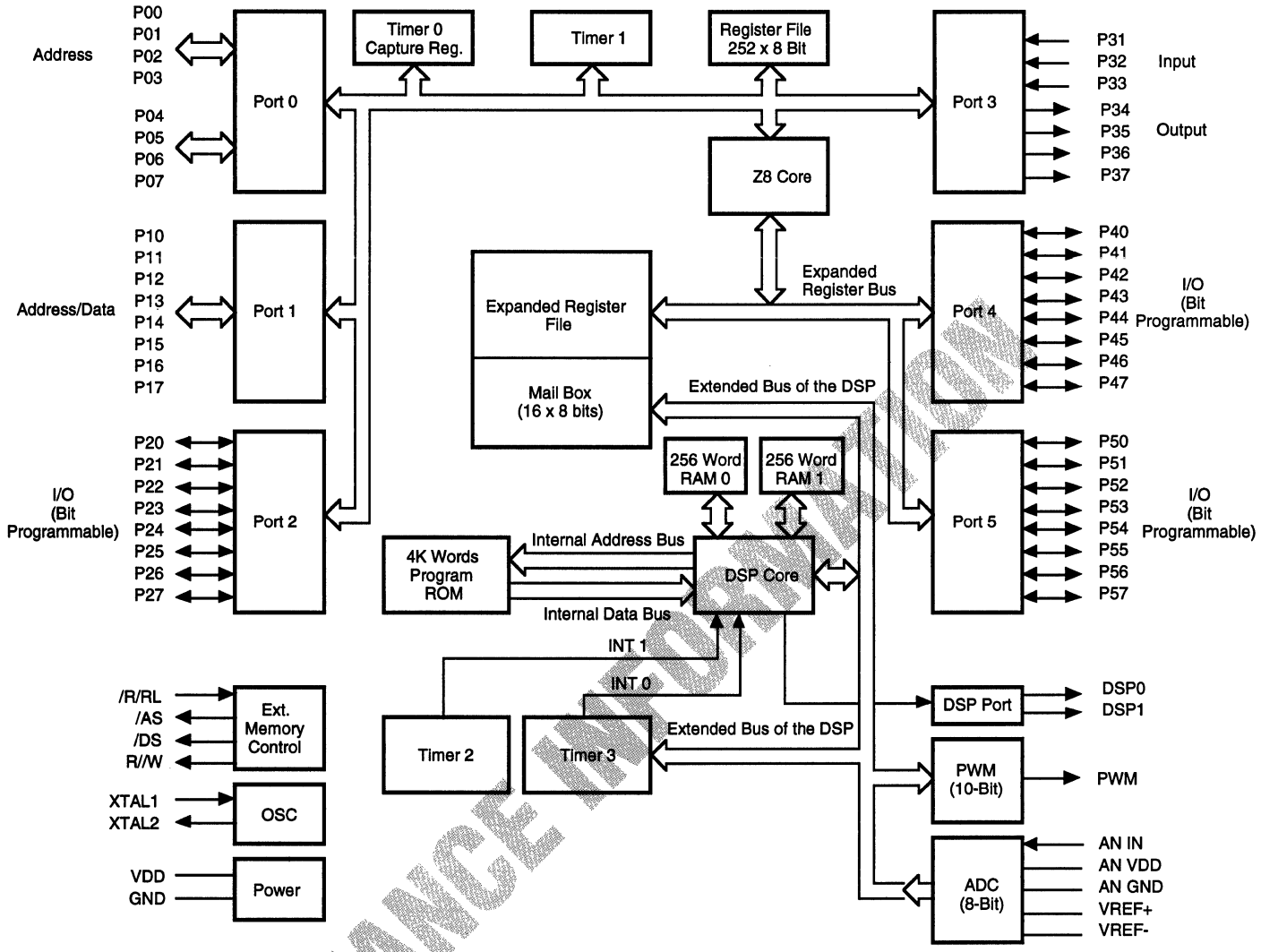
GENERAL DESCRIPTION

The Z89920 is a fully integrated, ROMless, mixed signal, dual processor chip system designed for lower sample rates such as audio, telephone, security systems, modem, faxes, instrumentation, noise cancellation, and sonar. The I/O control processor is a Z8® with two 8-bit counter timers, and up to 47 I/O pins. The DSP is a 16-bit processor with a 24-bit ALU and Accumulator, 512x16 bits of RAM, single cycle instructions, and 4 Kword program ROM plus constants memory. The chip also contains a half-flash 8-bit A/D converter with up to 128 kHz sample rate and 10-bit PWM D/A converter. The sampling rates for the converters are programmable. The precision of the 8-bit A/D may be extended by resampling the data at a lower rate in software.

The Z8 and DSP processors are loosely coupled by mailbox registers and an interrupt system. DSP or Z8 programs may be directed by events in each other's domain.

FEATURES

- *Z8® Microcontroller with 31 I/O Lines*
- *Up to 64 Kbytes of Addressable External Space*
- *256 Bytes On-Chip Z8 RAM*
- *Watch-Dog Timer and Power-On Reset*
- *Low Power Stop Mode*
- *On-Chip Oscillator which Accepts a Crystal or External Clock Drive*
- *2x8 Bit Z8 Counter Timers with 6-Bit Prescaler*
- *Global Power-Down Mode*
- *Low-Power Consumption - 200 mW (typical)*
- *Brown-Out Protection*
- *Two Comparators with Programmable Interrupt Priority*
- *Six Vectored, Priority Interrupts*
- *RAM and ROM Protect*
- *Clock Speed of 20.48 MHz*
- *Z89C00 Core 16-Bit Digital Signal Processor (DSP)*
- *4K word DSP Program ROM*
- *512 words On-Chip DSP RAM*
- *8-Bit A/D Converter with up to 128 kHz Sample Rate*
- *10-Bit PWM D/A Converter (4 kHz to 64 kHz)*
- *Two DSP Timers to Support Different A/D and D/A Sampling Rates*
- *Zero Overhead Hardware Looping*
- *16-Bit Single Cycle DSP Instructions*
- *16-Bit Single Cycle DSP Multiply/Accumulate*
- *Six-Level DSP Stack*
- *24-Bit DSP ALU, Accumulator and Shifter*
- *Three Vectored DSP Interrupts*
- *Independent Z8 and DSP Operations*
- *IBM® PC-Based Development Tools*



PROTOTYPE/EPROM/OTP MICROCONTROLLERS

GENERAL DESCRIPTION

The Z86C12 ICE (In-Circuit-Emulator) introduces a new level of sophistication to single-chip architecture. The ICE is housed in a 84-pin PGA package, and is manufactured in CMOS technology.

The ICE architecture is characterized by Zilog's 8-bit microcontroller core. The device offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, easy hardware/software system expansion, a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

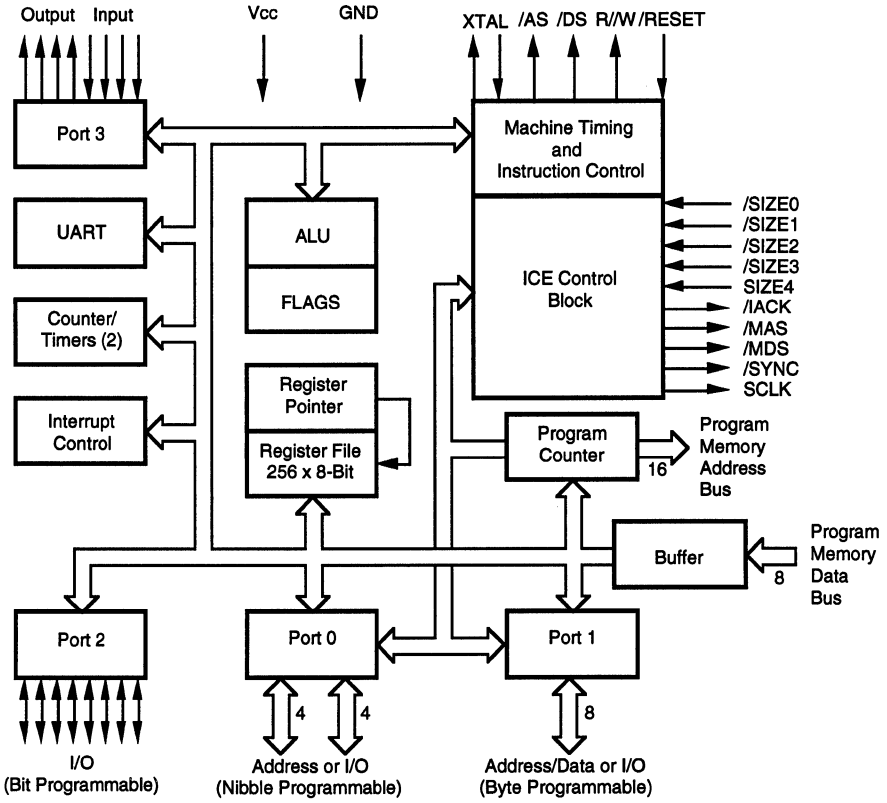
Industrial applications demand powerful I/O capabilities. The ICE fulfills this with 32-pins dedicated to input and output.

These lines are grouped into four ports. Each port consists of eight lines, and is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configuration: Program Memory, Data Memory, and 236 General Purpose Registers. To unburden the program from coping with real-time problems such as counting/timing and serial data communication, the ICE offers two on-chip counter/timers with a large number of user selectable modes, and an asynchronous receiver/transmitter.

FEATURES

- *8-Bit CMOS Microcontroller Emulator*
- *84-Pin PGA Package*
- *4.5 to 5.5 Volt Operating Range*
- *Low Power Consumption - 275 mW (max)*
- *Average Instruction Execution Time of 1 µs*
- *Fast Instruction Pointer - 0.6 µs @ 16 MHz*
- *Two Standby Modes - STOP and HALT*
- *32 Input/Output Lines*
- *Full-Duplex UART*
- *All Digital Inputs are TTL Levels*
- *Six Memory Emulation Modes*
- *256 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupt from Eight Different Sources*
- *Clock Speed: 16 MHz*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.*



Z86C50 CMOS Z8 ICE MICROCONTROLLER

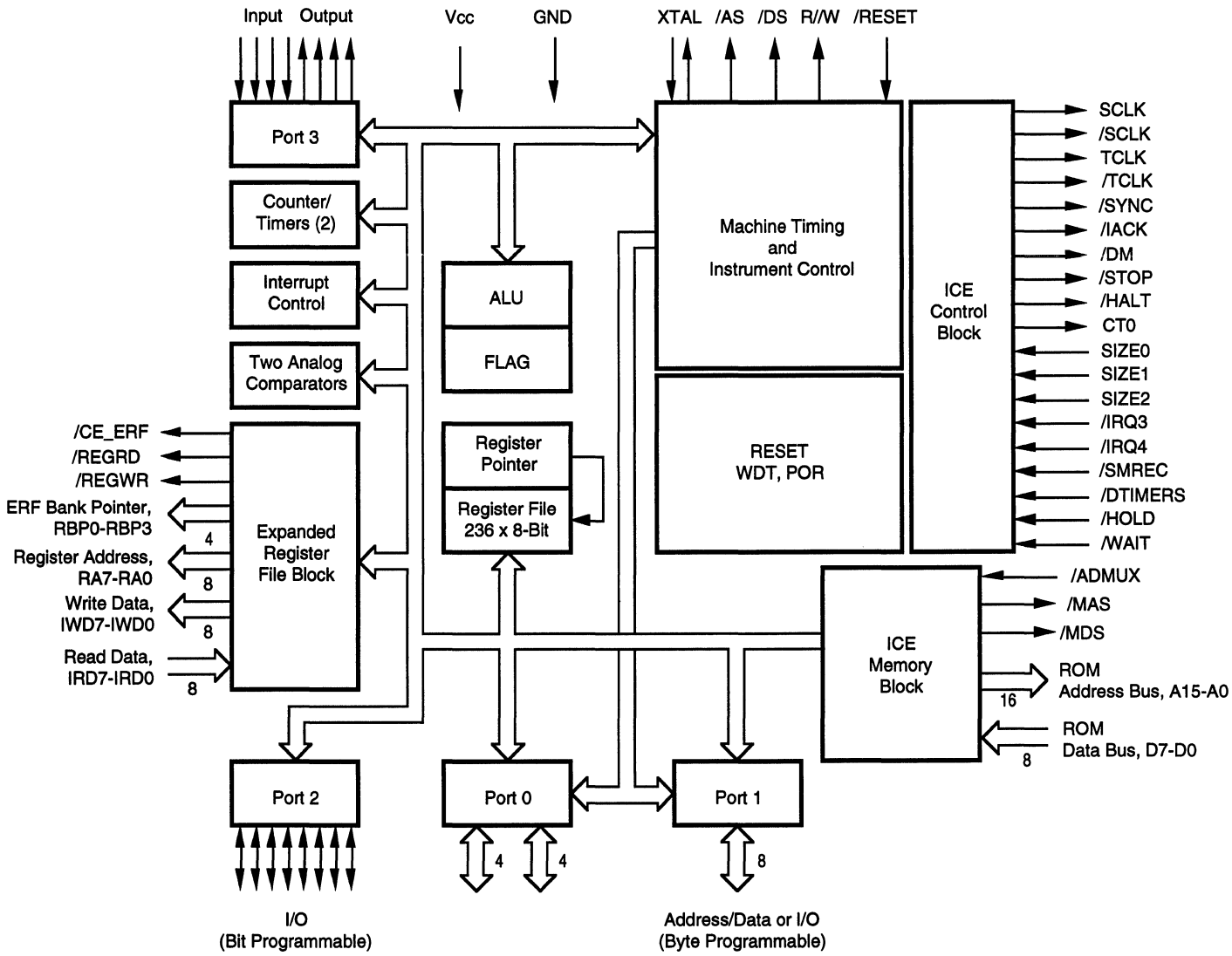
GENERAL DESCRIPTION

The Z86C50 CCP™ In-Circuit Emulation (ICE) chip introduces a new level of sophistication to ICE architecture. The Z86C50 not only provides all the control signal interfaces, but also the internal register bus interface. The Expanded Register File (ERF) can be external and interface with the internal register bus and ERF control signals.

The Z86C50 allows users to prototype a system with an actual hardware device and to develop the code. Also, this device is very useful in emulator applications.

FEATURES

- *8-bit CMOS Z8® CCP™ Base In-Circuit Emulation Chip*
- *124-Pin PGA Package*
- *Full Z8 CCP Family Instruction Set*
- *3.0 to 5.5 Volt Operation Range*
- *Clock Speed 20 MHz*
- *236-Byte General-Purpose Register*
- *Low EMI Mode Programmable*
- *Internal Register Read Bus and Write Bus Interface*
- *Register File Bank Pointer and Register File Address Bus Interface for Accessing the Expanded Register File (ERF) Externally.*
- *Expanded Register Control Signals (/REGRD, /REGWR and /CE_ERF) Interface*
- *All Internal Control Signals Interface (i.e., /SYNC, /IACK, /MAS, /MDS, etc.)*
- *Disable Timers Control Signal*
- *Hold Internal Clock Control Signal*
- *Wait Control Signal*
- *STOP and HALT Modes Signal Status Outputs*
- *Two On-Board Analog Comparators*
- *Two Programmable 8-bit Counter/Timers, Each with a 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Six Different Sources*
- *Internal Program Memory Size Select Interface*


Input
Output
Vcc
GND
XTAL
/AS
/DS
R/W
/RESET
Port 3
Counter/ Timers (2)
Interrupt Control
Two Analog Comparators
ALU
FLAG
Register Pointer
Register File 236 x 8-Bit
Machine Timing and Instrument Control
RESET WDT, POR
ICE Control Block
SCLK
/SCLK
TCLK
/TCLK
/SYNC
/IACK
/DM
/STOP
/HALT
CT0
SIZE0
SIZE1
SIZE2
/IRQ3
/IRQ4
/SMREC
/DTIMERS
/HOLD
/WAIT
/CE_ERF
/REGRD
/REGWR
ERF Bank Pointer, RBP0-RBP3
4
Register Address, RA7-RA0
8
Write Data, IWD7-IWD0
8
Read Data, IRD7-IRD0
8
Expanded Register File Block
ICE Memory Block
/ADMUX
/MAS
/MDS
ROM Address Bus, A15-A0
16
ROM Data Bus, D7-D0
8
Port 2
Port 0
Port 1
4
4
8
I/O (Bit Programmable)
Address/Data or I/O (Byte Programmable)

Z86E08 CMOS Z8 ONE-TIME-PROGRAMMABLE MICROCONTROLLER

GENERAL DESCRIPTION

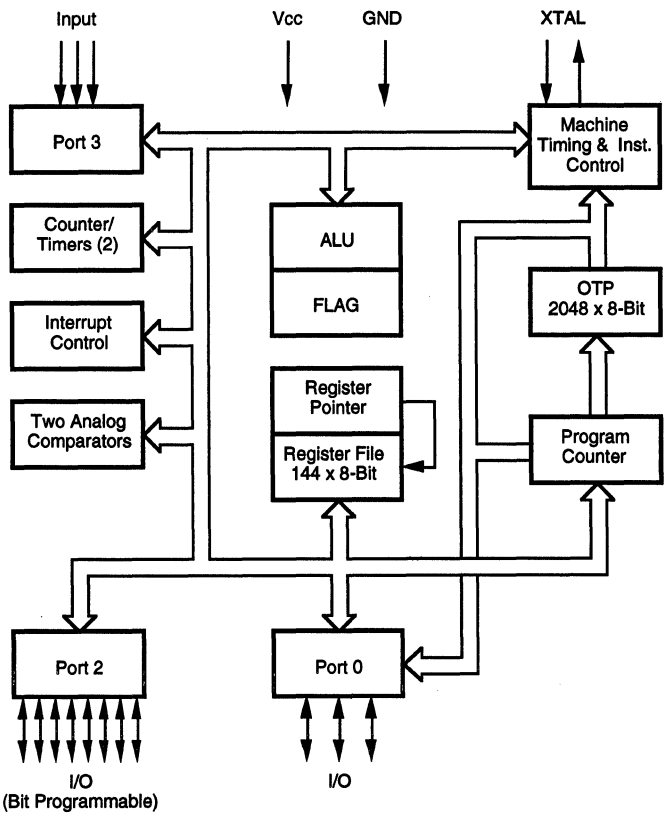
The Z86E08 microcontroller introduces a new level of sophistication to single-chip architecture. The Z86E08 is a member of the Z8® single-chip microcontroller family with 2 Kbytes of one-time-PROM. The device is housed in an 18-pin DIP, and is manufactured in CMOS technology. The device offers easy software development and debug, prototyping, and small production runs not economically desirable with a masked ROM version (Z86C08).

The Z86E08 has 14 pins dedicated to input and output. These lines are grouped into three ports, and are configurable under software control to provide I/O, timing and status signals.

To unburden the program from coping with real-time problems such as counting/timing and I/O data communications, the Z86E08 offers two on-chip counter/timers with a large number of user selectable modes. Included are two on-board comparators that can process analog signals with a common reference voltage.

FEATURES

- *8-Bit CMOS Microcomputer, 18-Pin DIP*
- *Low Noise Programmable*
- *Programmable ROM Protect*
- *4.5 to 5.5 Volt V_{CC} Range*
- *Low Power Consumption - 50 mW (Typical)*
- *Fast Interrupt Pointer - 1 µs at 12 MHz*
- *Standby Modes: STOP and HALT*
- *14 Input/Output Lines*
- *All Digital Inputs Are CMOS Levels and Schmitt-Triggered*
- *2 Kbytes of One-Time-PROM*
- *124 Bytes of RAM*
- *Two Programmable 8-Bit Counter/Timers Each with a 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts From Five Different Sources*
- *Clock Speeds 8 and 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators*
- *On-Chip Oscillator That Accepts a Crystal, Ceramic Resonator, LC, or External Clock Drive.*



GENERAL DESCRIPTION

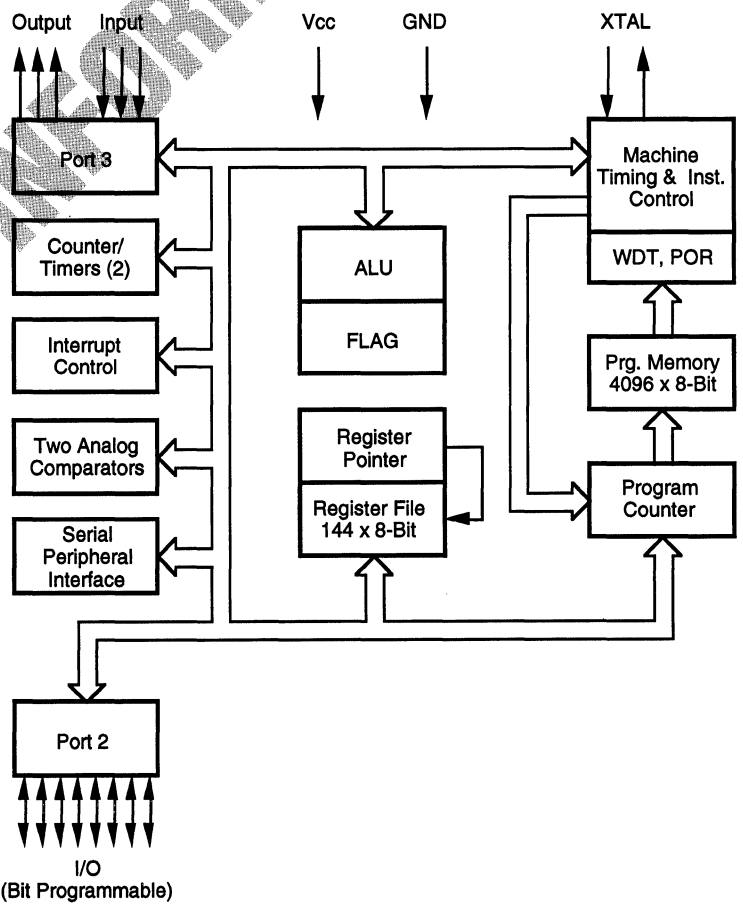
The Z86E09 is a member of the Z8® single-chip one-time-programmable microcontroller family. The device is housed in an18-pin DIP. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86E09 architecture is based on Zilog's 8-bit microcontroller core with an Expanded Register File to allow access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme and a number of ancillary features that are useful in many consumer, industrial and automotive applications.

With powerful peripheral features such as on-board comparators, counter/timers, watch dog timer, and serial peripheral interface, the Z86E09 meets the needs of most sophisticated controller applications.

FEATURES

- *8-Bit CMOS Microcontroller, 18-Pin DIP*
- *Emulates the Z86C06/09*
- *Serial Peripheral Interface with Compare Feature*
- *Clock Speed: 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Two Comparators with Programmable Interrupt Polarity*
- *Six Vectored, Priority Interrupts from Six Different Sources*
- *On-Chip Oscillator That Accepts a Crystal, Ceramic Resonator, LC, RC, or External Clock Drive.*
- *14 Input/Output Lines*
- *Low EMI Noise Mode*
- *Schmitt-Triggered CMOS Inputs*
- *4 Kbytes of OTP ROM*
- *124 Bytes of RAM*
- *Standby Modes: STOP and HALT*



Z86E21/E22 CMOS Z8 ONE-TIME-PROGRAMMABLE MICROCONTROLLER

GENERAL DESCRIPTION

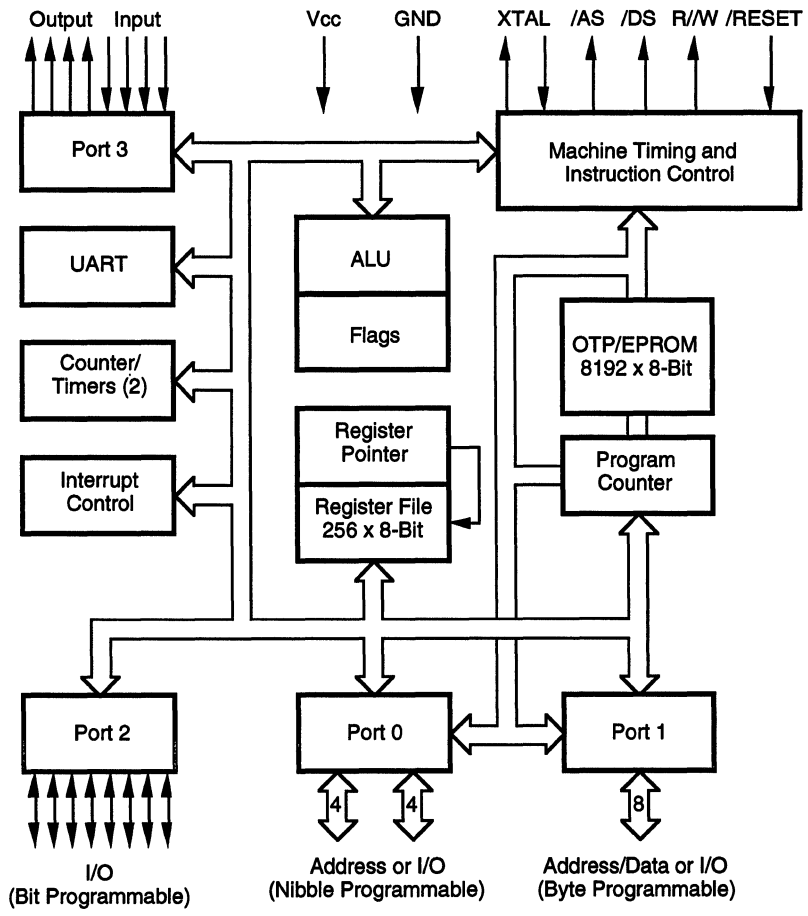
The Z86E21 and Z86E22 are single chip microcontrollers with 8 Kbytes of EPROM. They offer all the outstanding features of the Z8® family architecture.

The Z86E21/E22 can be tailored to the needs of its user. It can be configured as a stand-alone microcomputer with 8 Kbytes of internal ROM, a traditional microprocessor that manages up to 120 Kbytes of external memory, or a parallel-processing element in a system with other processors and peripheral controllers linked by the Z-Bus®. In all configurations, a large number of pins remain available for I/O.

These parts are available in EPROM and OTP versions.

FEATURES

- *Complete Microcontroller with 32 I/O Lines, and 8 Kbytes of On-Chip EPROM in a 40-Pin DIP, 44-Pin QFP, or 40-Pin Window DIP package.*
- *The Register File is Composed of 236 General-Purpose Registers, Four I/O Port Registers and 16 Status and Control Registers.*
- *Full Duplex UART and Two Programmable 8-Bit Counter/Timers, Each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *Low Noise - 86E22, Slower Rise/Fall Times of Output Drivers*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Standby Modes: STOP and HALT*
- *CMOS Process*
- *4.5 to 5.5 Volts Operating Range*
- *Six Vectored, Priority Interrupts from Eight Different Sources*
- *All Pins TTL Compatible*
- *Clock Speeds:*
  - *Z86E21 - 12 and 16 MHz*
  - *Z86E22 - 4 MHz*



GENERAL DESCRIPTION

The Z86E23 microcontroller introduces the next level of sophistication to single-chip architecture. The Z86E23 is a member of the Z8 single-chip microcontroller family with 8 Kbytes of EPROM and 236 bytes of general- purpose RAM.

The Z86E23 is a pin compatible, One-Time-Programmable (OTP) version of the Z8614 and Z8602 Keyboard Controller (KBC).

Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

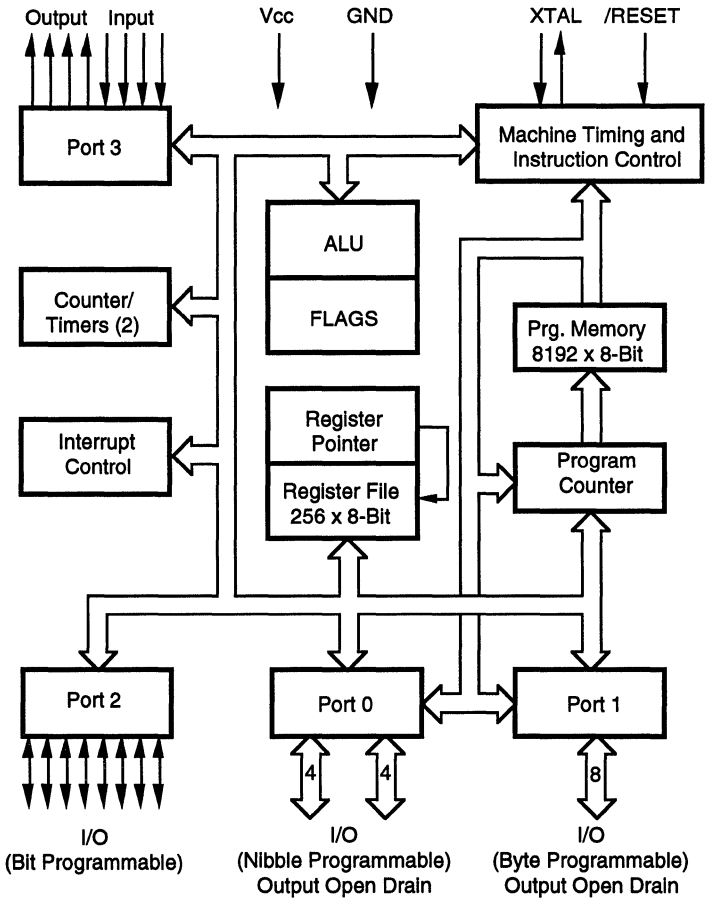
The Z86E23 architecture is based on Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

There are two basic address spaces available to support this wide range of configuration: program memory and 236 general-purpose registers.

To unburden the program from coping with real-time problems such as counting/timing, the Z86E23 offers two on-chip counter/timers with a large number of user selectable modes.

FEATURES

- *8-Bit CMOS Microcontroller*
- *40- or 44-Pin Package*
- *4.5 to 5.5 Voltage Operating Range*
- *Low Power Consumption - 165 mW (max.)*
- *Standby Modes: STOP and HALT*
- *32 Input/Output Lines*
- *All Digital Inputs are TTL Levels*
- *Auto Latches*
- *High Voltage Protection on High Voltage Inputs*
- *RAM and EPROM Protect*
- *8 Kbytes of EPROM*
- *256 Bytes of RAM (236 for General Purpose)*
- *Two Programmable 8-Bit Counter/Timers each with a 6-Bit Programmable Prescaler.*
- *Six Vectored, Priority Interrupts from Eight Different Sources.*
- *System Clock Speeds up to 4 MHz.*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, LC or External Clock Drive.*
- *Low EMI Emission*



Z86E30 CMOS Z8 ONE-TIME-PROGRAMMABLE CONSUMER CONTROLLER PROCESSOR

GENERAL DESCRIPTION

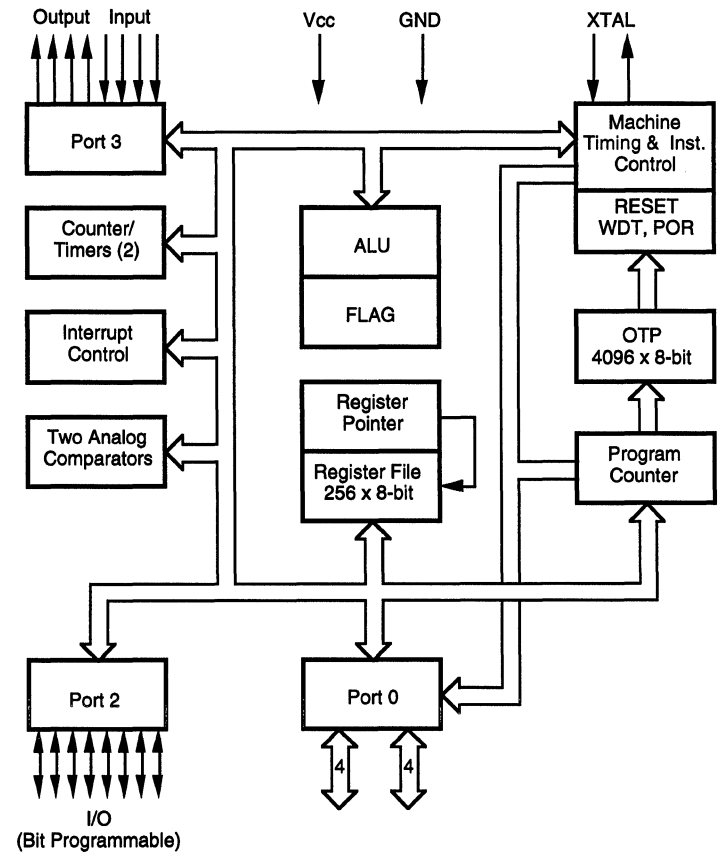
The Z86E30 is a single chip microcontroller with 4 Kbytes of OTP and is functionally compatible with the Z86C30 Mask ROM device. It offers all the outstanding features of the Z8® family architecture in a low power, 28-pin format.

The Z86E30 architecture is based on Zilog's 8-bit microcontroller core with an expanded register file to allow access to register mapped peripheral and I/O circuits.

The Z86E30 has instruction compatibility with the entire Z8 family for easy software/hardware systems expansion. The powerful feature set allows minimization of peripheral components.

FEATURES

- *Complete CMOS Microcontroller with 24 I/O Lines and 4 Kbytes of On-Chip OTP in a 28-Pin DIP, or Window DIP Package.*
- *The Register File is Composed of 236 Bytes of General-Purpose Registers, Three I/O Port Registers and 15 Control and Status Registers.*
- *Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator which Accepts Crystal or Ceramic Resonator, LC, RC or External Clock Drive.*
- *Two Comparators with Programmable Interrupt Polarity*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Standby Modes: STOP and HALT*
- *Clock Speeds: 12, 16 MHz*
- *4.5 to 5.5 Volts Operating Range*
- *All Digital Inputs are CMOS Levels and Schmitt-Triggered.*
- *Six Vectored, Priority Interrupts from Six Different Sources*
- *Programmable Low EMI mode*



GENERAL DESCRIPTION

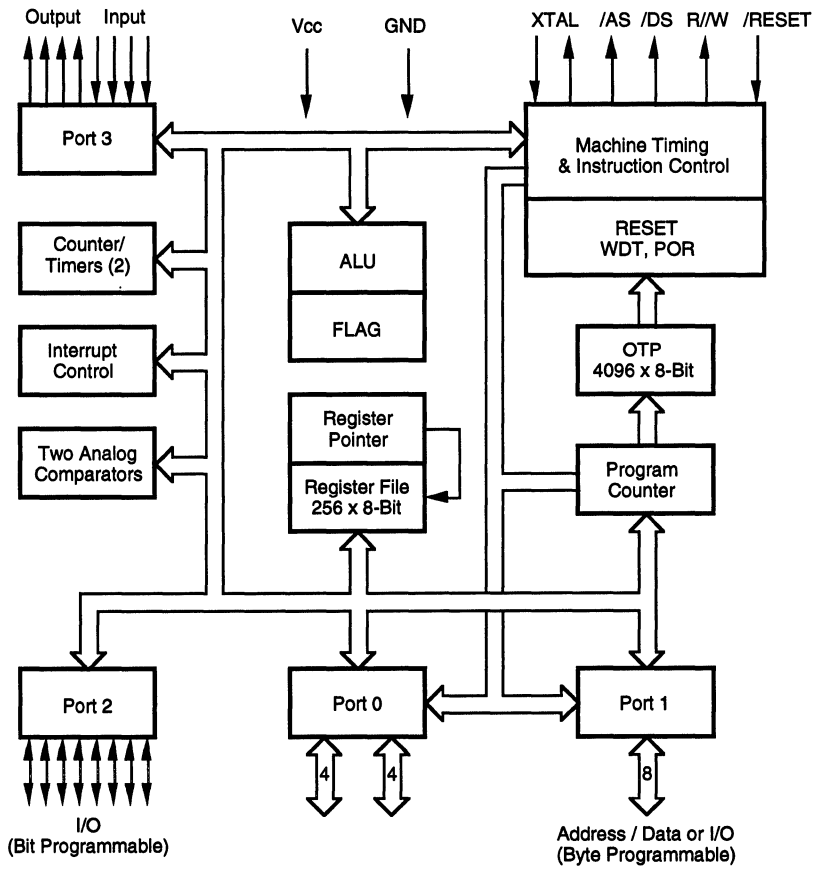
The Z86E40 is a single chip microcontroller with 4 Kbytes of OTP ROM and is functionally compatible with the Z86C40 Mask ROM device. It offers all the outstanding features of the Z8® family architecture and is housed in a DIP, PLCC or QFP package.

The Z86E40 architecture is based on Zilog's 8-bit microcontroller core with an expanded register file to allow access to register mapped peripheral and I/O circuits.

The Z86E40 has instruction compatibility with the entire Z8 family for easy software/hardware system expansion. It is available in both EPROM and OTP versions.

FEATURES

- *Complete Microontroller with 32 I/O Lines and 4 Kbytes of On-Chip OTP.*
- *The Register File is Composed of 236 Bytes of General-Purpose Registers, Four I/O Port Registers and 15 Control and Status Registers.*
- *Two Programmable 8-Bit Counter/Timers, each with a 6-Bit Programmable Prescaler.*
- *On-Chip Oscillator that Accepts a Crystal, Ceramic Resonator, RC, or External Clock Drive.*
- *Two Comparators with Programmable Interrupt Polarity*
- *Fast Instruction Pointer - 1 µs at 12 MHz*
- *Watch-Dog Timer and Power-On Reset*
- *Standby Modes: STOP and HALT*
- *Clock Speeds: 12, 16 MHz*
- *4.5 to 5.5 Volts Operating Range*
- *Programmable Low EMI Noise Mode*
- *Available in 40- or 44-Pin Package, DIP, PLCC or QFP*



MASS STORAGE DATA PATH CONTROLLERS

Z86018 DATA PATH CONTROLLER

GENERAL DESCRIPTION

The Z86018 single-chip data path controller is a high performance integrated device that combines the functions necessary to implement a variety of low-cost, high-performance Winchester® products. The five functions performed by this chip are: disk control and sequencing, host interface logic, local microcontroller interface, Reed-Solomon® ECC Correction, and sector buffer interface. Programmable power down modes are provided for battery operated applications.

The disk controller interface features a low overhead programmable sequencer that can be programmed to transfer a full track of data from disk to buffer with no firmware intervention. The sequencer can support all types of Winchester drives, but is especially well suited to low-power sampled, or embedded servo types of drives.

The 31x32 bit sequencer has the ability to be interrupted, save its state, execute a servo interrupt routine, and return to the interrupted instruction. The sequencer can fetch up to 1024 bytes of format specific data per track operation, to be used as format data, to load the servo interrupt counter, or as section numbers, allowing for full track reads with no firmware intervention.

Data rates of up to 34 Mbits/sec are supported through the use of high-speed, low cost CMOS technology. Data integrity through a hardware implementation of a widely used 88-bit Reed-Solomon ECC code is provided. 16-bit CRC is also supported in hardware for error detection on ID fields.

The microcontroller port provides for Intel, Motorola, National, NEC and Zilog microcontroller interfaces with no need for external chip select logic. Interrupt and status registers facilitate interrupt or polling operations. Direction microcontroller access to the buffer RAM is possible even during disk and Host data transfer.

The Z86018 provides automatic host interface control which allows for full track reads from disk to host with no microcontroller intervention. The ATA signals DRQ, BSY and IRQ14 are generated by the Z86018 in hardware allowing for the fastest possible transfers over the AT bus.

The buffer controller interface arbitrates between disk, host, Reed-Solomon ECC, microcontroller, and formatter data requests. The buffer interface directly drives up to 64K of SRAM, or 1 Mbyte of DRAM. To maximize buffer bandwidth page mode is used when accessing DRAMs. Parity generation and checking is also supported for data integrity. The buffer controller operates with an independent clock source to maximize its bandwidth.

FEATURES

- *Low Profile 100-Pin Plastic VQFP*
- *Programmable Power Down Mode*
- *Point and Go automatic disk and host control and transfers*

Microcontroller Port

- *Supports Intel, Motorola, and Zilog Multiplexed Interfaces*
- *Access to External Swtich Settings After Hardware Reset Through the Buffer RAM Data Bus*
- *Automatic Configuration for Microcontroller Type*
- *Direct, Transparent Access to all Buffer Memory, with up to 8 Kbytes of Buffer Reserved for Microcontroller Data*
- *Storage such as Cache and Defect Management*
- *Hardware Wait State Generation or Polled Mode for Microcontroller Buffer Accesses*
- *Programmable Chip Select Generation for the Firmware PROM and One Other Device.*

Drive Interface Port

- *Full Track Read, Write, or Format Capability with no Microcontroller Intervention.*
- *Programmable RAM Based Sequencer with Enhanced Branching Capability*
- *The Sequencer is Interruptible by Either the Internal Servo Counter, or External Input to Handle Servo Fields Within a Sector*
- *Sequencer Data can Come From the Internal RAM Based Sequencer, or From the Buffer Memory Allowing for Different Data Each Time a Sequencer Instruction is Executed*
- *Sequencer Can be Updated at Any Time*
- *Soft and Hard Sector Drive Support*
- *88-Bit Reed-Solomon with on the fly Hardware Correction of a Sector Within 1/2 Sector Time*
- *16-Bit CRC*
- *8-Byte Stack for Pushing Header Information*

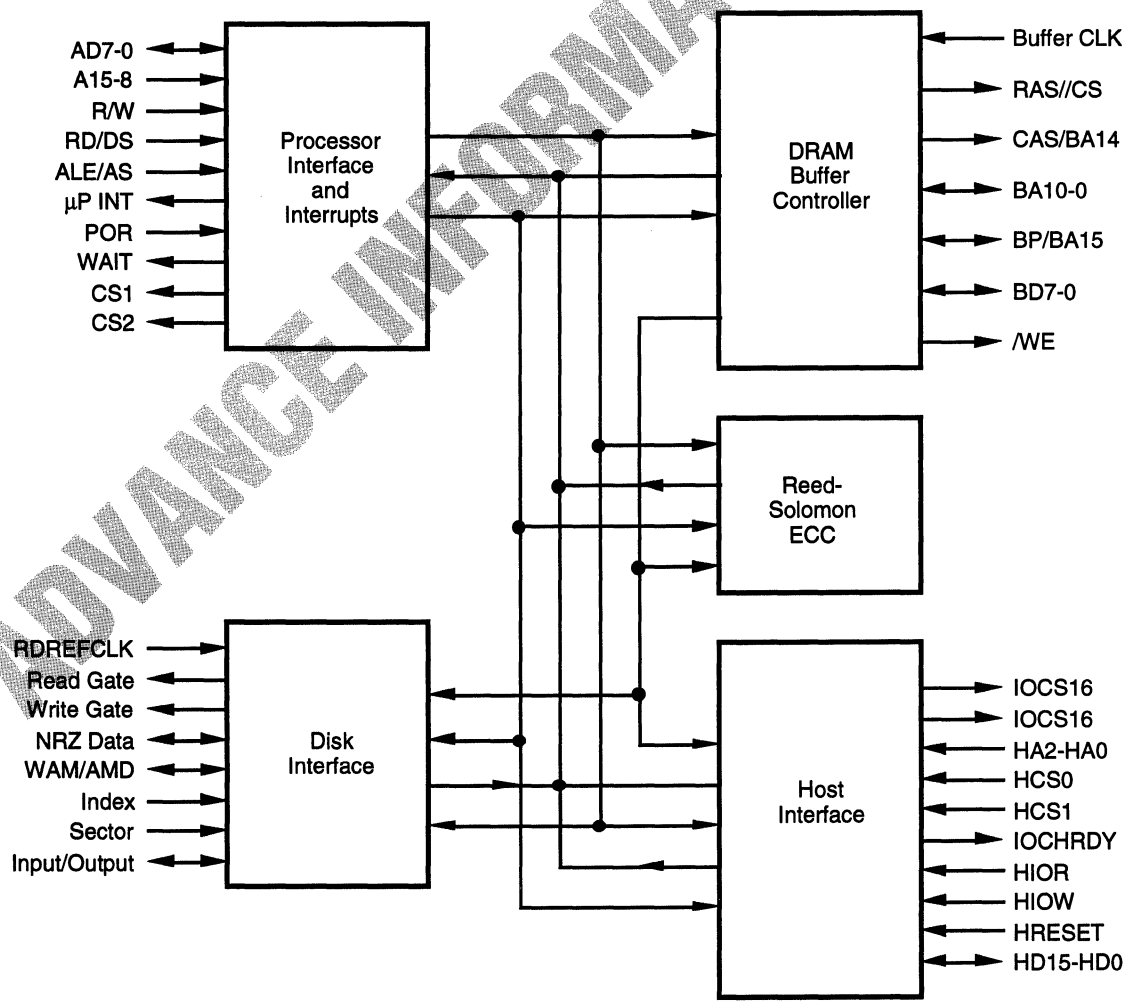
FEATURES (Continued)

Buffer Port

- *DRAM Support With up to 1 Mbyte Addressing Capability*
- *SRAM Support With up to 64 Kbyte Addressing Capability*
- *4.125 Mbytes/sec Disk Data Rate (33 MHz Read Reference Clock), and 7 Mbytes/sec Host Transfer Rate Using 100 ns Page Mode DRAMs or 70 ns SRAMs*
- *8-Bit Memory Data Bus with Parity Option for DRAM Mode*
- *Separate Microcontroller Channel into Memory for Scratch Pad Buffer*
- *6-Byte Host FIFO, 5-Byte Disk Data FIFO, and 4-Byte Formatter FIFO for Speed Matching with the Host, Disk, and Sequencer.*

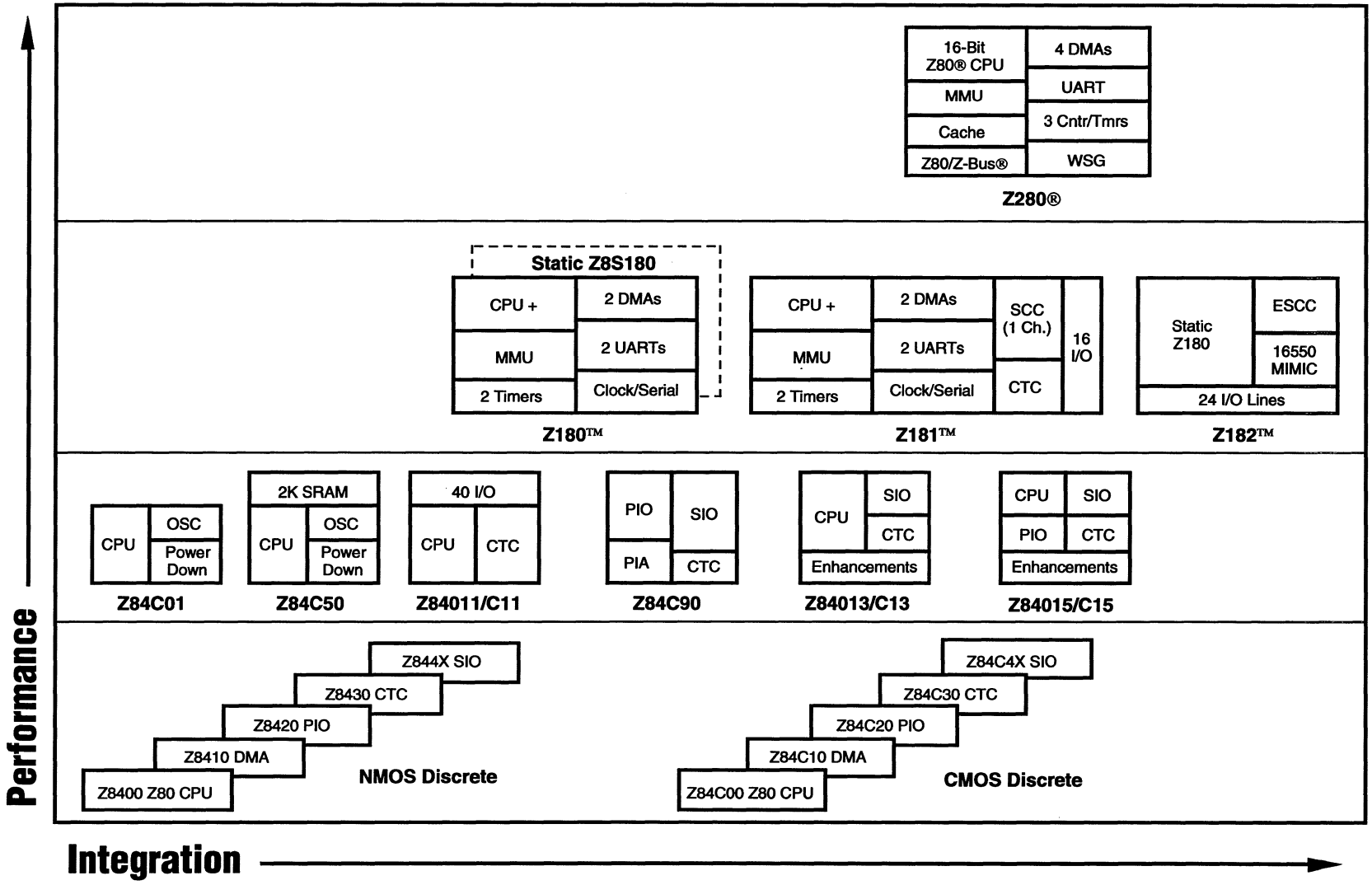
AT Port

- *True AT (IDE Connector) Interface with no Glue Logic Needed*
- *Direct Host Interface Through Programmable 24 mA Drives with Hysteresis Receivers*
- *On-Chip Registers to Emulate the Task Files for PC AT Task File*
- *Provides 8 and 16-Bit Data Transfer on the Host Bus*
- *Provides Flexible Timing Interface to the Host Through the Ability to Insert Wait States*
- *Provides the Logic to Daisy Chain Two Embedded Disk Controllers on the PC AT*



CLASSIC PRODUCT FAMILY

CLASSIC FAMILY PRODUCT PORTFOLIO **COMPONENTS SHORTFORM**



CLASSIC FAMILY REFERENCE CHART **COMPONENTS SHORTFORM**

Product	Pin Count	COMMERCIAL VQFP	QFP	DIP	PLCC	Cerdip	Speed	Temp	MILITARY DIP	PGA	Speed	883C	SMD	JAN
NMOS														
Z8400 CPU	40,44	-	-	X	X	X	4,6,8	S,M	X	-	2.5,4	X	-	X
Z8410 DMA	40,44	-	-	X	X	X	4	-	-	-	-	-	-	-
Z8420 PIO	40,44	-	-	X	X	X	4,6	S,M	X	-	2.5,4	X	X	-
Z8430 CTC	28,44	-	-	X	X	X	4,6	S,M	X	-	2.5,4	X	X	-
Z844X SIO	40,44	-	-	X	X	X	4,6	S,M	X	-	2.5,4	X	X	-
Z8470 DART	40,44	-	-	X	-	-	4,6	S	-	-	-		-	-
CMOS														
Z84C00 CPU	40,44	-	X	X	X	X	6,8,10,20	E,M	X	-	6	X	-	X
Z84C01 CPU	44	-	X	-	X	-	6,10	E	-	-	-	-	-	-
Z84C10 DMA	40,44	-	X	X	X	X	6,8	E	-	-	-	-	-	-
Z84C20 PIO	40,44	-	X	X	X	X	6,8,10	E,M	X	-	6	X	X	-
Z84C30 CTC	28,44	-	X	X	X	X	6,8,10	E,M	X	-	6	X	X	-
Z84C4X SIO	40,44	-	X	X	X	X	6,8,10	E,M	X	-	6	X	X	-
Z84C50 RAM80	40,44	-	X	X	X	-	10	E	-	-	-	-	-	-
Z84C90 KIO	84	-	X	-	X	-	8,10,12	E,S,M	-	X	8	X	-	-
Z84011/C11 PIC	100	-	X	-	-	-	6,10	E	-	-	-	-	-	-
Z84013/C13 IPC	84	-	-	X	-	-	6,10	E	-	-	-	-	-	-
Z84015/C15 IPC	100	X*	X	-	-	-	6,10,16*	E	-	-	-	-	-	-
Z80180 MPU	64,68,80	-	X	X	X	-	6,8,10	E,S,M	-	X	8	X	-	-
Z8S180	68,80	-	X	-	X	-	16,20	S	-	-	-	-	-	-
Z80181 SAC	100	-	X	-		-	10,12	E,S	-	-	-	-	-	-
Z80182 ZIP	100	X	X	-	-	-	16,20	S	-	-	-	-	-	-
Z80280 MPU	68	-	-	-	X	-	10,12	S	-	-	-	-	-	-

Temperature Range
S = Standard 0°C to +70°C
E = Extended -40°C to +100°C
M = Military -55°C to +125°C
***** Z84C15 only.

CLASSIC FAMILY REFERENCE CHART COMPONENTS SHORTFORM

Product	Pin Count	COMMERCIAL Plastic DIP	PLCC	QFP	PGA	Cerdip	Ceramic Dip	Speed	Temp	MILITARY Ceramic DIP	Ceramic LCC	Speed	SMD	JAN
Z8001 CPU	48	X	-	-	-	-	X	6,10	S,E,M	X	X	4,6,10	X	-
Z8002 CPU	40,44	X	X	-	-	X	-	6,10	S,E,M	X	X	4,6,10	X	X
Z8016 DTC	48	X	-	-	-	-	-	4,5,6	S	-	-	-	-	-
Z8036 CIO	40,44	X	X	-	-	X	-	6	S,E,M	X	X	4,6	X	-
Z8536 CIO	40,44	X	X	-	-	X	-	6	S,E,M	X	X	4,6	X	-
Z8038 FIO	40,44	X	X	-	-	X	-	6	S,E,M	X	X	6	-	-
Z8060 FBU	28	X	-	-	-	-	-	1 MB/sec	S	-	-	-	-	-
Z8068 DCP	40,44	X	X	-	-	-	-	4	-	-	-	-	-	-
Z8581 CGC	18	X	-	-	-	-	-	6,10	S,E,M	X	X	6,10	X	-
Z32H00	120,144	-	-	X	X	-	-	25	S,E	-	-	-	-	-

Temperature Range
S = Standard 0°C to +70°C
E = Extended -40°C to +100°C
M = Military -55°C to +125°C

Part-To-Kit Cross Reference Matrix

	Z8S18000ZCO	Z80181100ZCO	Z80181100ZDP	Z80181101ZCO*	Z84C1100ZCO	Z84C1500ZCO	Z84C5000ZCO	Z84C9000ZCO	ZEPMIP00001	ZEPMIP00002
Z8S180	●								●	
Z80181		●	●	●					●	
Z80182										●
Z84C01								●		
Z84C11					●					
Z84C15						●				
Z84C43					●					
Z84C50							●			
Z84C90							●	●		

* Includes LLAP software that can be licensed.

DISCRETE Z80® FAMILY

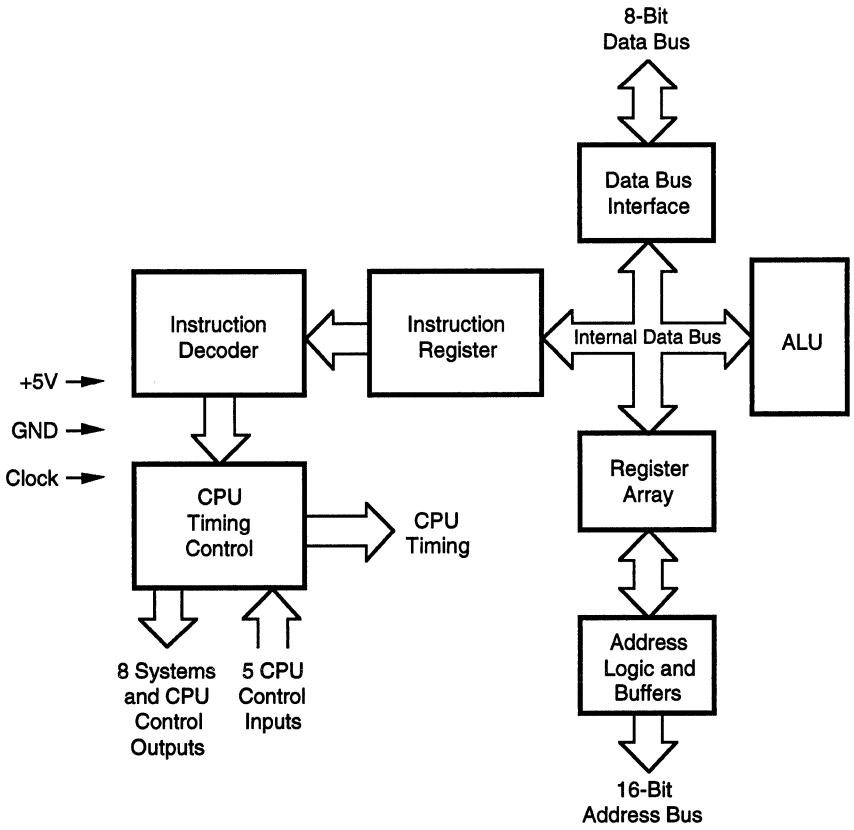
GENERAL DESCRIPTION

The Z8400/Z84C00 CPUs are fourth-generation enhanced microprocessors with exceptional computational power. They offer higher system throughput and more efficient memory utilization than comparable second- and third-generation microprocessors. The speed offerings from 6 - 20 MHz suit a wide range of applications which migrate software. The internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of "Exchange" instructions makes either set of main or alternate registers accessible to the programmer. The alternate set allows operation in foreground-background mode or it may be reserved for very fast interrupt response.

The CPU also contains a Stack Pointer, Program Counter, two index registers, a Refresh register (counter), and an Interrupt register. The CPU is easy to incorporate into a system since it requires only a single +5V power source. All output signals are fully decoded and timed to control standard memory or peripheral circuits; the CPU is supported by an extensive family of peripheral controllers.

FEATURES

- *The Extensive Instruction Set Contains 158 Instructions, Including the 8080A Instructions Set as a Subset.*
- *Single 5 Volt Power Supply*
- *NMOS Version for Low Cost, High Performance Solutions; CMOS Version for High Performance, Low Power Designs.*
- *NMOS Z084004 - 4 MHz*
  Z0840006 - 6.17 MHz
  Z084008 8 MHz
- *CMOS Z0840006 - DC to 6.17 MHz*
  Z84C0008 - DC to 8 MHz
  Z84C0010 - DC to 10 MHz
  Z84C0020 - DC to 20 MHz
- *6 MHz Version can be Operated at 6.144 MHz Clock*
- *The Z80 Microprocessors and Associated Family of Peripherals can be Linked by a Vectored Interrupt System. This System can be Daisy-Chained to Allow Implementation of a Priority Interrupt Scheme.*
- *Duplicate Set of Both General-Purpose and Flag Registers*
- *Two 16-Bit Index Registers*
- *Three Modes of Maskable Interrupts:*
  - *Mode 0 - 8080A Similar*
  - *Mode 1 - Non-Z80 Environment, Location 38H*
  - *Mode 2 - Z80 Family Peripherals, Vectored Interrupts*
- *On-Chip Dynamic Memory Refresh Counter*



Z8410/Z84C10 NMOS/CMOS Z80 DMA DIRECT MEMORY ACCESS CONTROLLER

GENERAL DESCRIPTION

The Z80 DMA (Direct Memory Access), is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control, with little or no external logic, in systems using an 8- or 16-bit data bus and a 16-bit address bus.

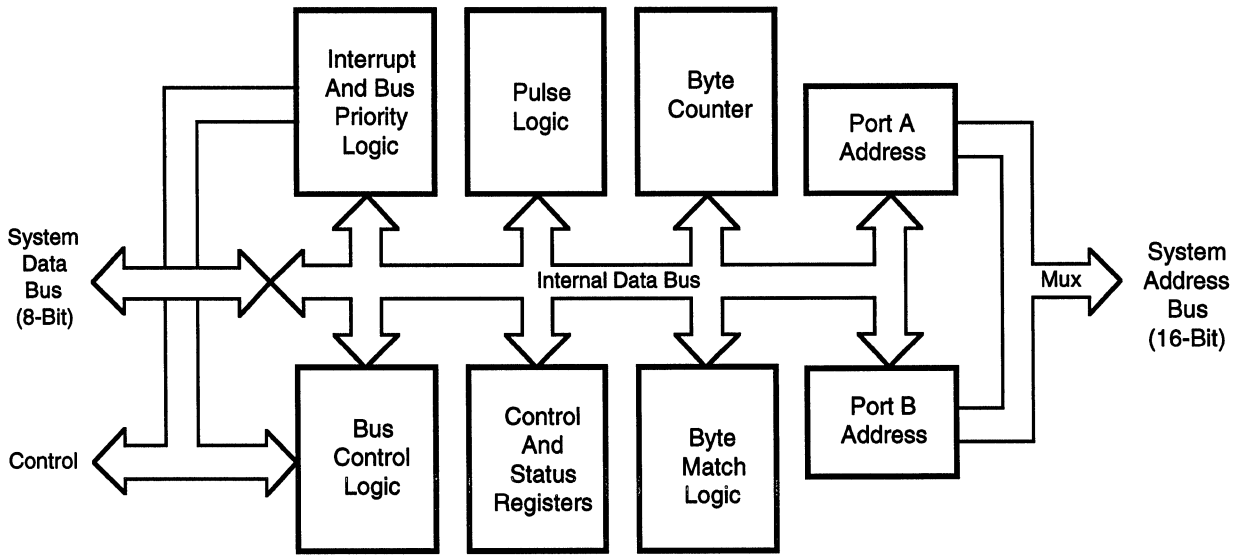
Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte searches are performed either concurrently with transfers or as an operation in itself.

The Z80 DMA contains direct interfacing to, and independent control of, system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart, minimize CPU software overhead. They are especially useful in adapting this special-purpose transfer processor to a broad variety of memory, I/O and CPU environments.

The Z80 DMA is packaged in a 40-pin plastic or ceramic DIP, or 44-pin PLCC. It uses a single +5V power supply and the standard Z80 Family single-phase clock.

FEATURES

- *Transfers, Searches, and Search/Transfers in Byte-at-a-Time, Burst, or Continuous Modes. Cycle Length and Edge Timing can be Programmed to Match the Speed of any Port.*
- *Dual-Port Addresses (Source and Destination) Generated for Memory-to-I/O, Memory-to-Memory, or I/O-to-I/O Operations. Addresses may be Fixed or Automatically Incremented/Decremented.*
- *Next-Operation Loading without Disturbing Current Operations via Buffered Starting-Address Registers. An Entire Previous Sequence can be Repeated Automatically.*
- *Extensive Programmability of Functions. CPU can read Complete Channel Status.*
- *NMOS Z08410 - 4 MHz*
- *NMOS Version for Cost Sensitive Performance Solutions*
- *CMOS Version for the Designs Requiring Low Power Consumption*
- *CMOS Z84C1006 - DC to 6.17 MHz, Z84C1008 - DC to 8 MHz*
- *6 MHz Version Supports 6.144 MHz CPU Clock Operation*
- *Standard Z80 Family Bus-Request and Prioritized Interrupt-Request Daisy-Chains Implemented without External Logic. Sophisticated, Internally Modifiable, Interrupt Vectoring.*
- *Direct Interfacing to System Buses without External Logic*



GENERAL DESCRIPTION

The Z80 PIO Parallel I/O Circuit (PIO) is a programmable, dual-port device that provides a TTL-compatible interface between peripheral devices and the Z80 CPU. Note the QFP package is only available in CMOS version. The CPU configures the Z80 PIO to interface with a wide range of peripheral devices that are compatible with the Z80 PIO including most keyboards, paper tape reads and punches, printers, and PROM programmers.

One characteristic of the Z80 peripheral controllers that separates them from other interface controllers is that all data transfers between the peripheral device and the CPU is accomplished under interrupt control. Thus, the interrupt logic of the PIO permits full use of the efficient interrupt capabilities of the Z80 CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO.

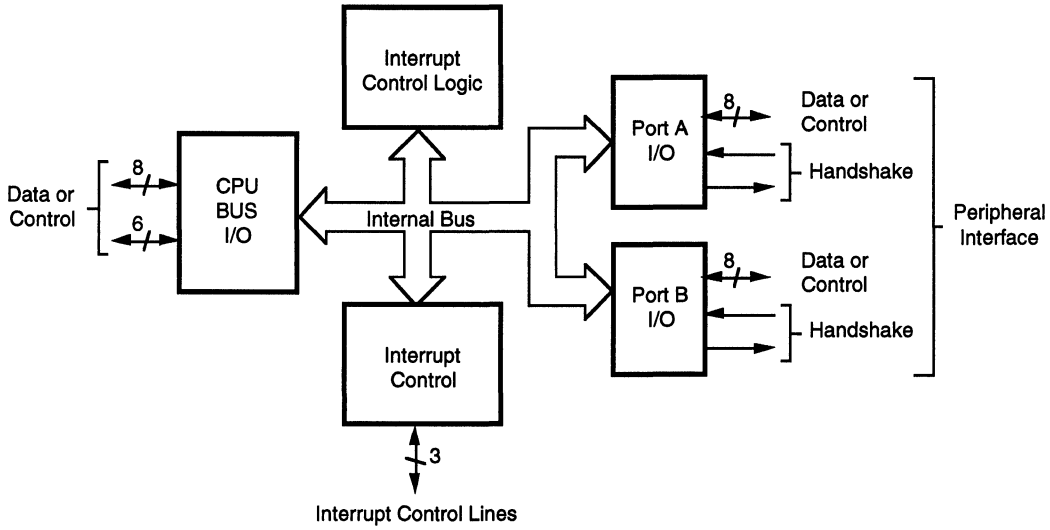
Another feature of the PIO is the ability to interrupt the CPU upon occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the time the processor must spend in polling peripheral status.

The Z80 PIO interfaces to peripherals via two independent general purpose I/O ports, designated Port A and Port B. Each port has eight data bits and two handshake signals, Ready and Strobe, which control data transfer. The Ready output indicates to the peripheral that the port is ready for a data transfer. Strobe is an input from the peripheral that indicates when a data transfer has occurred.

The Z80 PIO ports can be programmed to operate in four modes; Output (Mode 0), Input (Mode 1), Bi-directional (Mode 2) and Bit Control (Mode 3).

FEATURES

- *Two 8-Bit Ports with Handshake, and Four Programmable Operating Modes: Output, Input, Bi-directional (Port A only), and Bit Control.*
- *Programmable Interrupts on Peripheral Status Conditions*
- *NMOS Version for Cost Sensitive Applications. CMOS Version for Designs Requiring High Speed and Low Power Consumption.*
- *NMOS Z0842004 - 4 MHz*
  Z0842006 - 6.17 MHz
- *CMOS Z84C2006 - DC to 6.17 MHz*
  Z84C2008 - DC to 8 MHz
  Z84C2010 - DC to 10 MHz
- *Provides a Direct Interface Between Z80 Microcomputer Systems and Peripheral Devices.*
- *Standard Z80 Family Bus-Request and Prioritized Interrupt-Request Daisy-Chains Implemented without External Logic.*
- *The Eight Port B Outputs Can Drive Darlington Transistors (1.5 mA at 1.5 V).*
- *6 MHz Version Supports 6.144 MHz CPU Clock Operation.*



Z8430/Z84C30 NMOS/CMOS Z80 CTC COUNTER/TIMER CIRCUIT

GENERAL DESCRIPTION

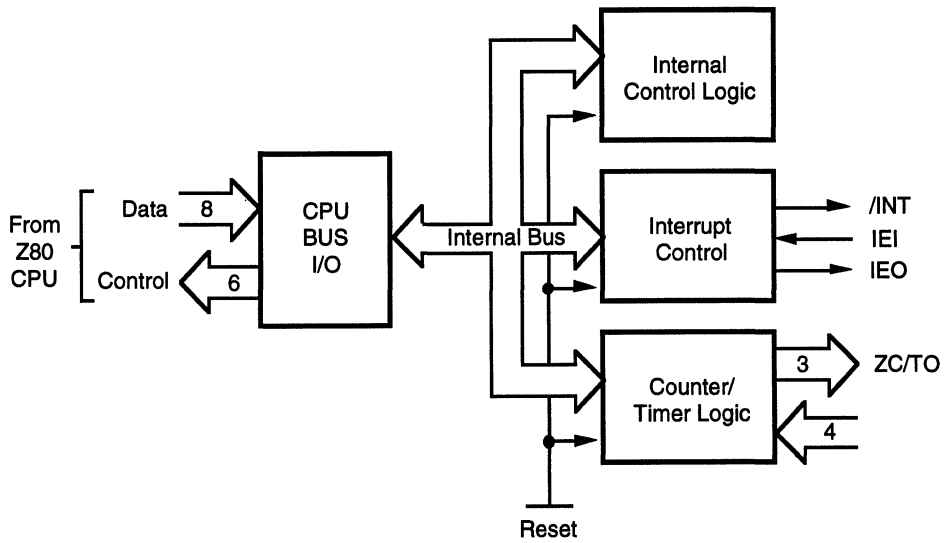
The Z80 Counter/Timer Circuit (CTC) can be programmed by system software for a broad range of counting and timing applications. The four independently programmable channels of the Z80 CTC satisfy common microcomputer system requirements for event counting, interrupt and interval timing, and general clock rate generation.

System design is simplified because the CTC connects directly to both the Z80 CPU and the Z80 SIO with no additional logic. In larger systems, address decoders and buffers may be required.

Programming the CTC is straight forward: each channel is programmed with two bytes; a third is necessary when interrupts are enabled. Once started, the CTC counts down, automatically reloads its time constant, and resumes counting. Software timing loops are completely eliminated. Interrupt processing is simplified because only one vector need be specified; the CTC internally generates a unique vector for each channel.

FEATURES

- *Four Independently Programmable Counter/Timer Channels, each with a Readable Downcounter and a Selectable 16 or 256 Prescaler. Downcounters are Reloaded Automatically at Zero Count.*
- *Selectable Positive or Negative Trigger Initiates Timer Operation*
- *NMOS Version for Cost Sensitive Performance Solutions. CMOS Version for Designs Requiring High Speed and Low Power Consumption*
- *NMOS Z0843004 - 4 MHz*
  Z0843006 - 6.17 MHz
- *CMOS Z84C3006 - DC to 6.17 MHz*
  Z84C3008 - DC to 8 MHz
  Z84C3010 - DC to 10 MHz
- *Interfaces Directly to the Z80 CPU, or for Baud Rate Generation to the Z80 SIO*
- *Three Channels have Zero Count/ Timeout Outputs Capable of Driving Darlington Transistors (1.5 mA at 1.5V).*
- *Standard Z80 Family Daisy-Chain Interrupt Structure Provides Fully Vectored, Prioritized Interrupts without External Logic. The CTC may also be used as an Interrupt Controller.*
- *6 MHz Version Supports 6.144 MHz CPU Clock Operation*



GENERAL DESCRIPTION

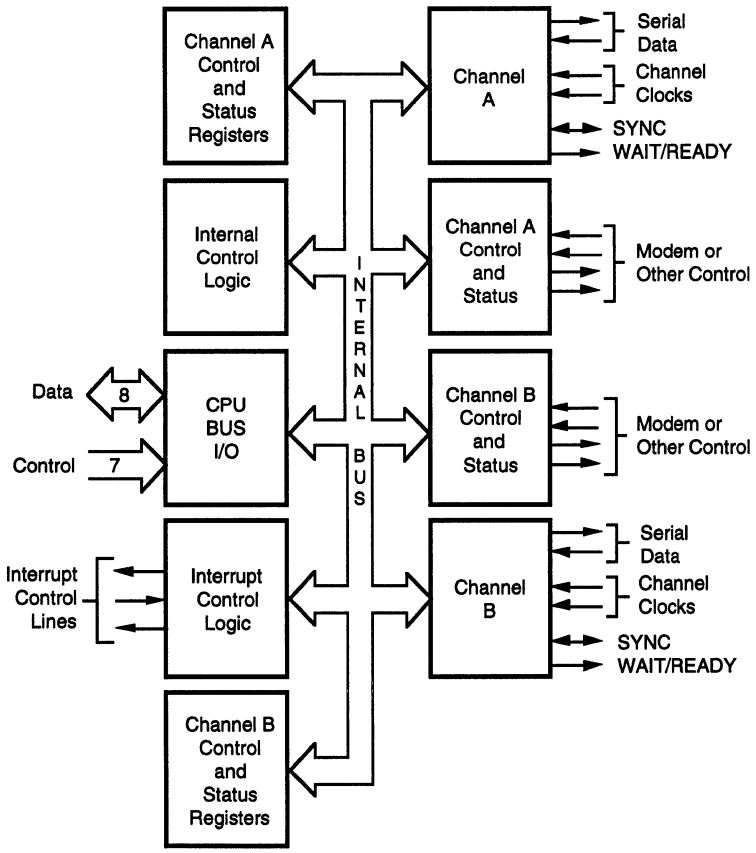
The Z80 Serial Input/Output Controller (SIO) is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs, and synchronous communication controllers combined. Also, it supports additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast, or slow, peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

FEATURES

- *Two Independent Full-Duplex Channels, with Separate Control and Status Lines for Modems or other Devices.*
- *Data Rate in the x1 Clock Mode or 0 to 1.6M Bits/Second with a 8.0 MHz Clock.*
- *NMOS Version for Cost Sensitive Performance Solutions; CMOS Version for the Designs Requires Low Power Consumption.*
- *NMOS Z0844x04 - 4 MHz*
  Z0844x06 - 6.17 MHz
  (Where x is the Designator for the Bonding Option; 0,1,2 or 4).
- *6 MHz Version Supports 6.144 MHz CPU Clock Operation*
- *CMOS Z84C4x06 - DC to 6.7 MHz,*
  Z84C4x08 - DC to 8 MHz,
  Z84C4x10 - DC to 10 MHz,
  Z84C4X10 - DCto 10 MHz
  (Where X is the Designator for the Bonding Option; 0,1,2 or 3,4).
- *Asynchronous Protocols: Everything Necessary for Complete Messages in 5, 6, 7 or 8 Bits/Character. Includes Variable Stop Bits and Several Clock-Rate Multipliers, Break Generation and Detection, Parity, Overrun and Framing Error Detection.*
- *Synchronous Protocols: Everything Necessary for Complete Bit- or Byte-Oriented Messages in 5,6,7 or 8 Bits/Character, Including IBM® Bisync, SDLC, HDLC, CCITT-X-25 and others. Automatic CRC Generation/Checking, Sync Character and Zero Insertion/Deletion, Abort Generation/Detection, and Flag Insertion.*
- *Receiver Data Registers Quadruply Buffered; Transmitter Registers Doubly Buffered.*
- *Highly Sophisticated and Flexible Daisy-Chain Interrupt Vectoring for Interrupts without External Logic.*



Z8470 Z80 DART DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER

GENERAL DESCRIPTION

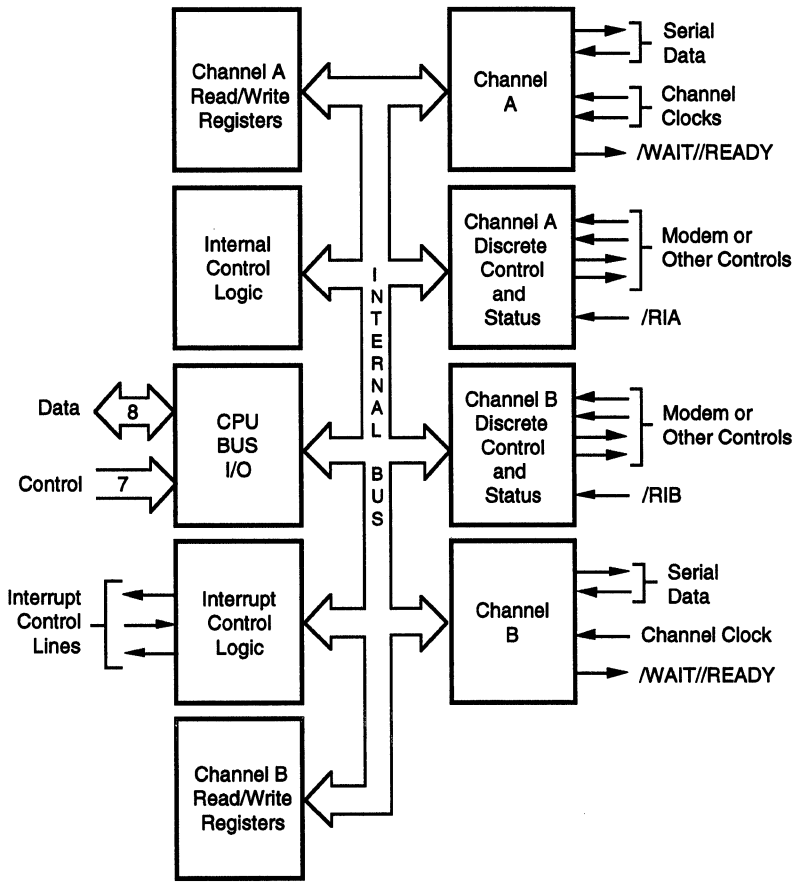
The Z80 DART (Dual-Channel Asynchronous Receiver/Transmitter) is a dual-channel multi-function peripheral component that satisfies a wide variety of asynchronous serial data communications requirements in microcomputer systems.

The Z80 DART is used as a serial-to-parallel, parallel-to-serial converter/controller with asynchronous appli-cations. In addition, the device also provides modem controls for both channels. In applications where modem controls are not needed, these lines can be used for general purpose I/O.

Zilog also offers the Z80 SIO, a more versatile device that provides synchronous (Bisync, HDLC, and SDLC) as well as asynchronous operation.

FEATURES

- *Two Independent Full-Duplex Channels with Separate Modem Controls. Modem Status can be Monitored.*
- *In x1 Clock Mode; Data Rates are 0 to 800K Bits/Second with a 4.0 MHz Clock or 0 to 12M Bits/Second with a 6.0 MHz Clock.*
- *Programmable Options Include 1, 1 1/2, or 2 Stop Bits; Even, Odd, or no Parity; and x1, x16, x32, and x64 Clock Modes.*
- *On-Chip Logic for Ring Indication and Carrier-Detect Status*
- *Receiver Data Registers are Quadruply Buffered; the Transmitter is Doubly Buffered.*
- *Break Generation and Detection as well as Parity-, Overrun-, and Framing-Error Detection are Available.*
- *Interrupt Features Include a Programmable Interrupt Vector, a "Status Affects Vector" Mode for Fast Interrupt Processing, and the Standard Z80 Peripheral Daisy-Chain Interrupt Structure that Provides Automatic Interrupt Vectoring with no External Logic.*
- *Available in 40-Pin Plastic or Ceramic DIP*



EMBEDDED CONTROLLERS

GENERAL DESCRIPTION

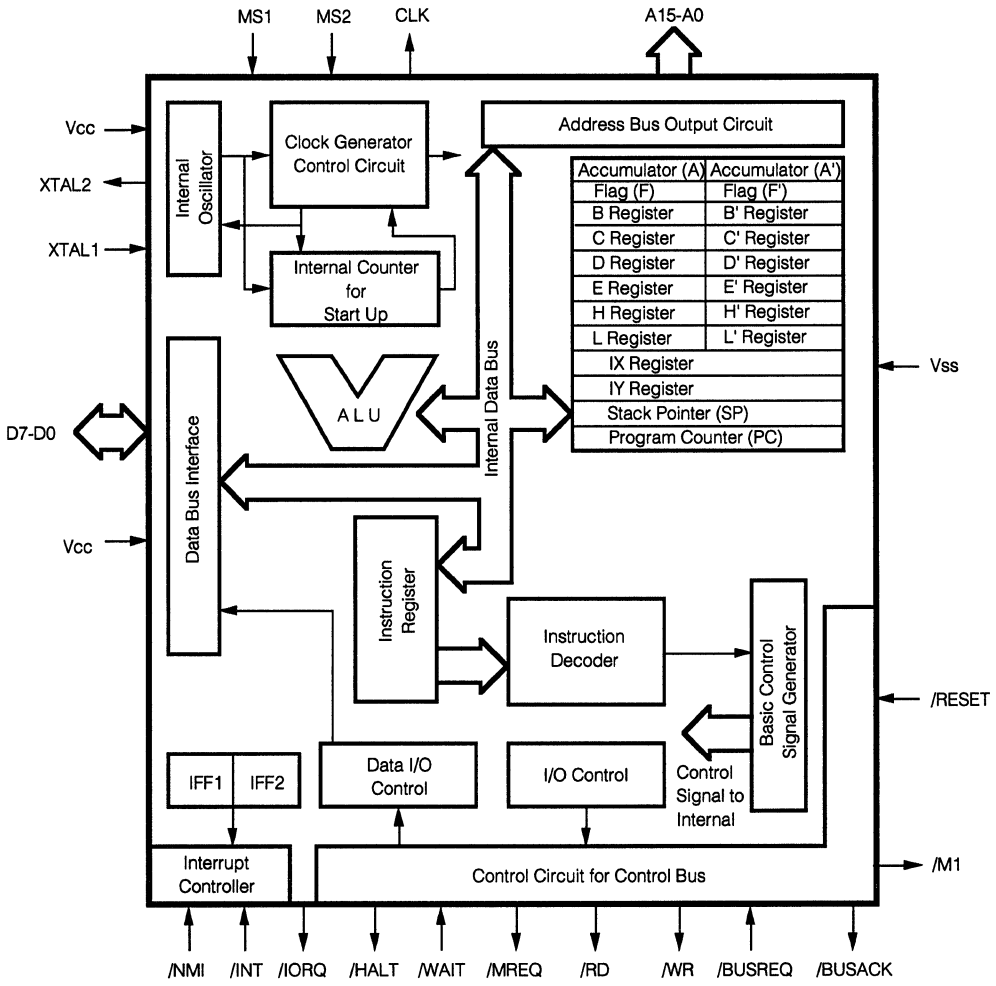
The Z84C01 is an 8-bit microprocessor with a built-in clock generator/controller, which provides low power operation and high performance.

Built into the Z84C01 is a control function and clock generator for the standby function. Included, are six paired general purpose registers, accumulator, flag registers, arithmetic/logic unit, bus control, and memory control/timing control circuits.

The Z84C01 is fabricated with Zilog CMOS technology and molded in a 44-pin PLCC or QFP package.

FEATURES

- *Commands Compatible with the Zilog Z80 MPU*
- *Low Power Consumption:*
  - *40 mA Typ (5V, 10 MHz Under RUN Mode)*
  - *2 mA Typ (5V, 10 MHz Under IDLE1 Mode)*
  - *10 mA Typ (5V, to 10 MHz Under IDLE2 Mode)*
  - *0.5 µA Typ (5V Under STOP Mode)*
- *DC to 6, 10 MHz Operation*
- *Single 5V Power Supply at 5V ±10%*
- *Operating Temperature: -40° C to 100° C*
- *On-Chip Clock Generator*
- *In the HALT State, the Following Four Modes are Selectable:*
  - *RUN Mode*
  - *IDLE1 Mode*
  - *IDLE 2 Mode*
  - *STOP Mode*
- *Powerful Set of 158 Instructions*
- *Powerful Interrupt Function:*
  - *Non-Maskable Interrupt Terminal (/NMI)*
  - *Maskable Interrupt Terminal (/INT)*
- *The Following Three Modes are Selectable:*
  - *8080 Compatible Interrupt Mode (Interrupt by Non-Z80 Family Peripheral LSI) (Mode 0)*
  - *Restart Interrupt (Mode 1)*
  - *Daisy-Chain Structure Interrupt Using Z80 Family Peripheral LSI (Mode 2)*
- *An Auxiliary Register Provided to Each of the General-Purpose Registers*
- *Two Index Registers*
- *10 Addressing Modes*
- *Built-In Refresh Circuit for Dynamic Memory*
- *44-Pin PLCC or QFP Package*



Z84C50 Z80 RAM80™ Z80 CPU / 2K SRAM

GENERAL DESCRIPTION

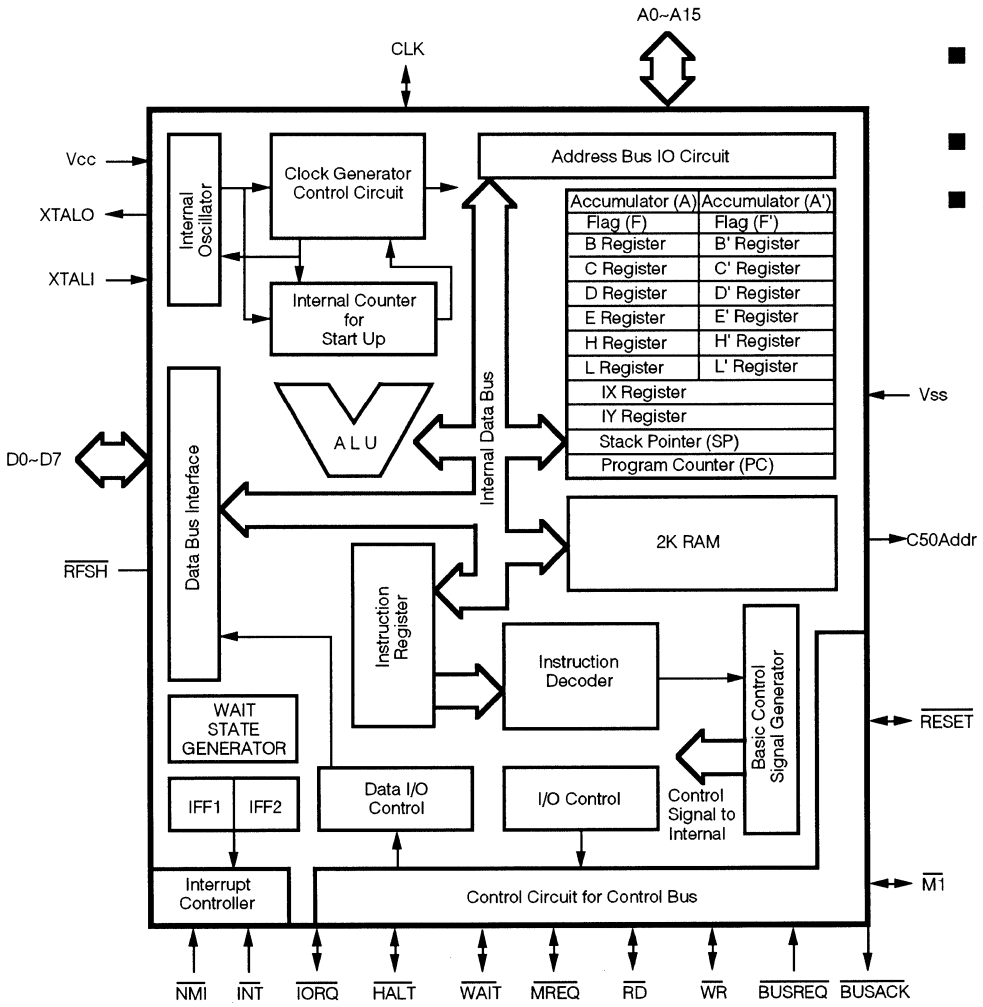
The Z84C50 is an 8-bit microprocessor integrated with 2 Kbytes of static memory and a clock generator/controller. The Z84C50 is targeted for a broad range of applications requiring a small amount of RAM. Additionally, the on-chip RAM can be accessed at a much higher rate than the external memory. This will significantly enhance performance, as the most commonly used and time critical software can be placed in on-chip memory.

Built into the Z84C50 is a control function and clock generator for the standby function in addition to: six paired general purpose registers, accumulator, flag registers, an arithmetic-and-logic unit, bus control, memory control and timing control circuits. Also, an on-chip wait state generator can be used for automatically inserting wait states for external memory access.

The Z84C50 is fabricated with Zilog CMOS technology and molded in 40-pin DIP, 44-pin PLCC, and 44-pin QFP packages.

FEATURES

- *Z80 CPU 2K Static RAM*
- *Wait State Generator for External Memory*
- *Low Power Consumption:*
  - *50 mA Typ (5V, 10 MHz Under RUN Mode)*
  - *4 mA Typ (5V, 10 MHz Under IDLE1 Mode)*
  - *10 mA Typ (5V, 10 MHz Under STOP Mode*
- *Z84C5006 - DC to 6 MHz, Z84C5010 - DC to 10 MHz*
- *Voltage Range 5V±10%*
- *In the HALT State, the Following Three Modes are Selectable:*
  - *RUN Mode*
  - *IDLE 1 Mode*
  - *STOP Mode*
- *The Following Three Modes are Selectable:*
  - *8080 Compatible Interrupt Mode (Interrupt by Non-Z80 Family Peripheral LSI-Mode 0).*
  - *Restart Interrupt (Mode 1).*
  - *Daisy-Chain Structure Interrupt Using Z80 Family Peripheral LSI (Mode 2)*
- *Power Interrupt Function:*
  - *Non-Maskable Interrupt Terminal (NMI)*
  - *Maskable Interrupt Terminal (INT)*
- *Built-In Refresh Circuit for Dynamic Memory*
- *On-Chip Clock Generator*
- *Available in 40-Pin DIP, 44-Pin PLCC, and 44-Pin QFP Packages*



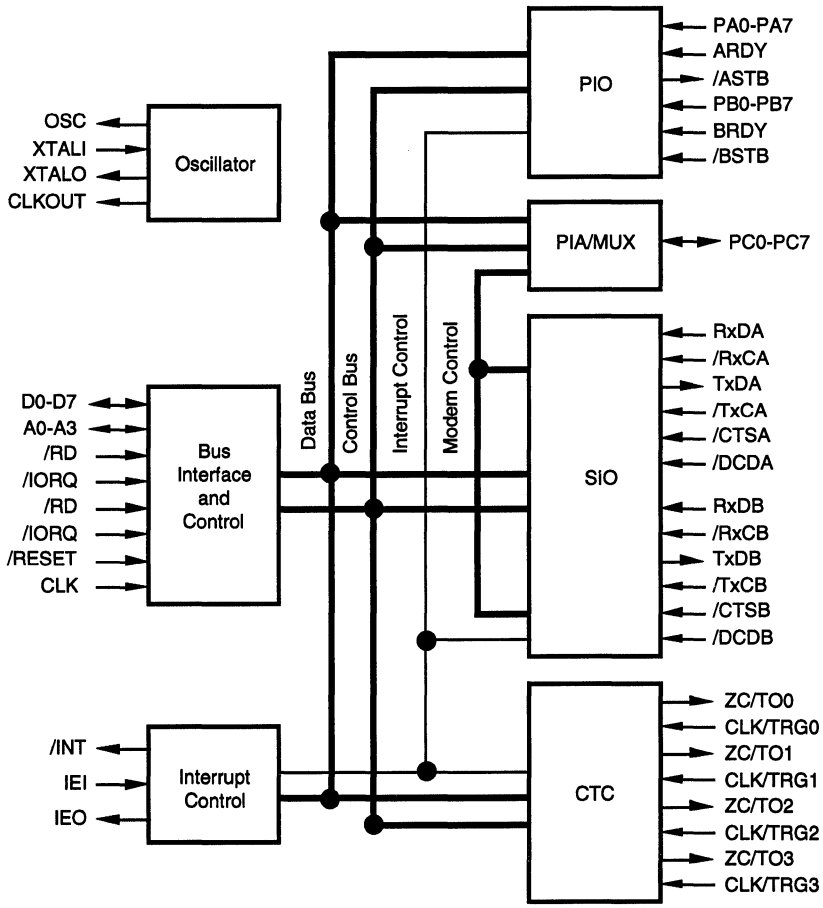
GENERAL DESCRIPTION

Zilog's Z84C90 Serial/Parallel I/O /Counter/Timer (KIO) is a multi-channel, multi-purpose I/O device designed to provide the end-user with a cost effective and powerful solution to meet the designers peripheral needs. The Z84C90 combines the features of one Z84C30 CTC, one Z84C4xSIO, one Z84C20 PIO, a byte-wide bit programmable I/O and a crystal oscillator in a single 84-pin package.

Utilizing fifteen internal registers for data and programming information, the KIO can easily be configured to any given system environment. Although the optimum performance is obtained with a Z84C00 CPU, the KIO can also be used with any other CPU.

FEATURES

- *Two Independent Synchronous/ Asynchronous Serial Channels*
- *Three 8-Bit Parallel Ports*
- *Four Independent Counter/Timer Channels*
- *On-Chip Clock Oscillator/Driver*
- *Software/Hardware Resets*
- *Designed in CMOS for Low Power Operation*
- *Supports Z80 Family Interrupt Daisy-Chain*
- *Programmable Interrupt Priorities*
- *8, 10 and 12.5 MHz Bus Clock Frequency*
- *Single +5V±10% Power Supply*
- *Available in an 84-Pin PLCC*



GENERAL DESCRIPTION

The Z84011 and Z84C11 Parallel I/O Controllers (PIC) are CMOS 8-bit microprocessors. They are integrated with the CTC and five 8-bit parallel ports into a single 100-pin QFP (Quad Flat Pack) package. The Z84C11 is an upward compatible version of the Z84011. Figure 1(a) shows the block diagram of Z84011, and Figure 1(b) shows the block diagram of the Z84C11. These high end superintegrated Parallel I/O Controllers are targeted for a broad range of applications from embedded controller to enhancement/cost reductions of existing hardware using Z80 based discrete peripherals.

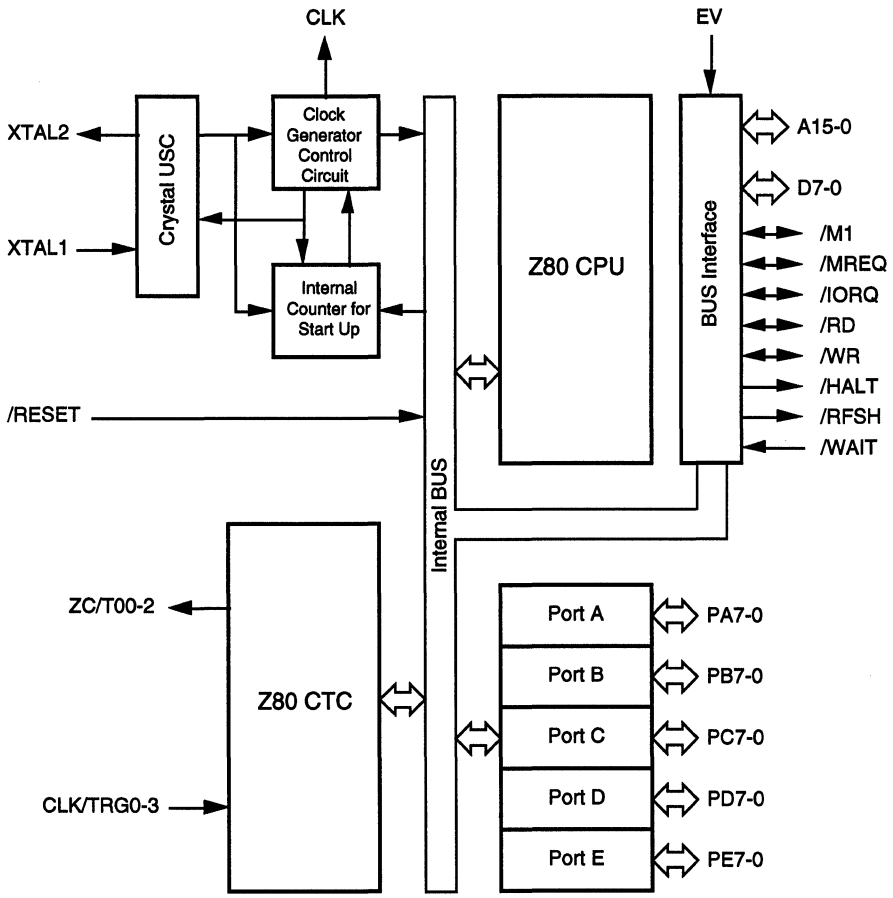


Figure 1a. Z84011 Block Diagram

FEATURES

- *Z84C00 Z80 CPU with CGC, Z84C30 Z80 CTC, Five 8-Bit Parallel Ports*
- *High Speed Operation 6/10 MHz*
- *Wide Operational Voltage Range 5V±10%*
- *TTL/CMOS Compatible*
- *Z84011 Features:*
  - *Z84C00 Z80 CPU*
  - *On-Chip Four Channel Counter Timer Controller(Z80 CTC)*
  - *Built-In Clock Generator Controller(CGC)*
  - *Five 8-Bit Parallel Ports*
  - *100-Pin QFP*
  - *Noise Package Filter to CLK/TRG nputs of the Z80 CTC*
- *Low Power Consumption in Four Operation Modes:*
  - *45 mA Typ. (Run Mode)*
  - *6 mA Typ. (Idle 1 Mode)*
  - *9 mA Typ. (Idle 2 Mode; Not applicable to Z84011)*
  - *1 µA Typ. (Stop Mode)*
- *Z84C11 Features:*
  - *All Z84011 Features*
  - *Support of Idle 2 Mode*
  - *Built-in Watch-Dog Timer (WDT)*
  - *Power-On Reset and Reset Extension*
  - *Wait State Generator*
  - *Simplified EV Mode Selection*
  - *Crystal Divide-by-One Option*
  - *External Clock Input Option*

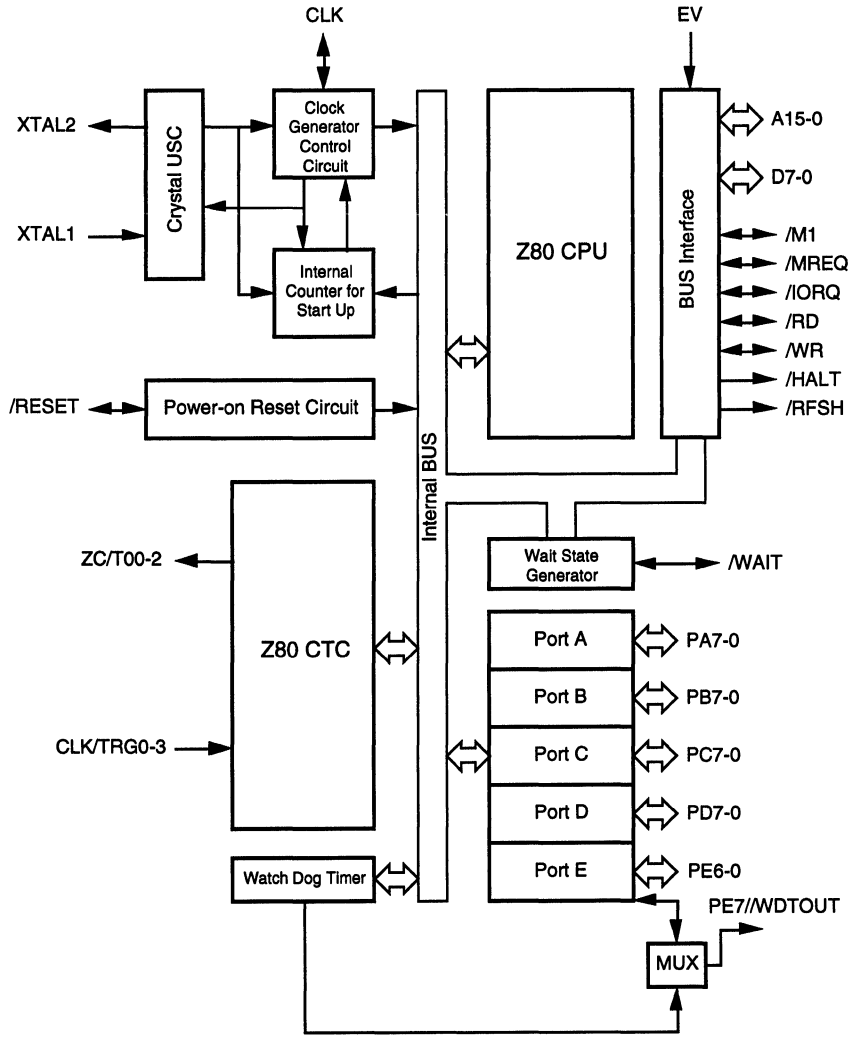
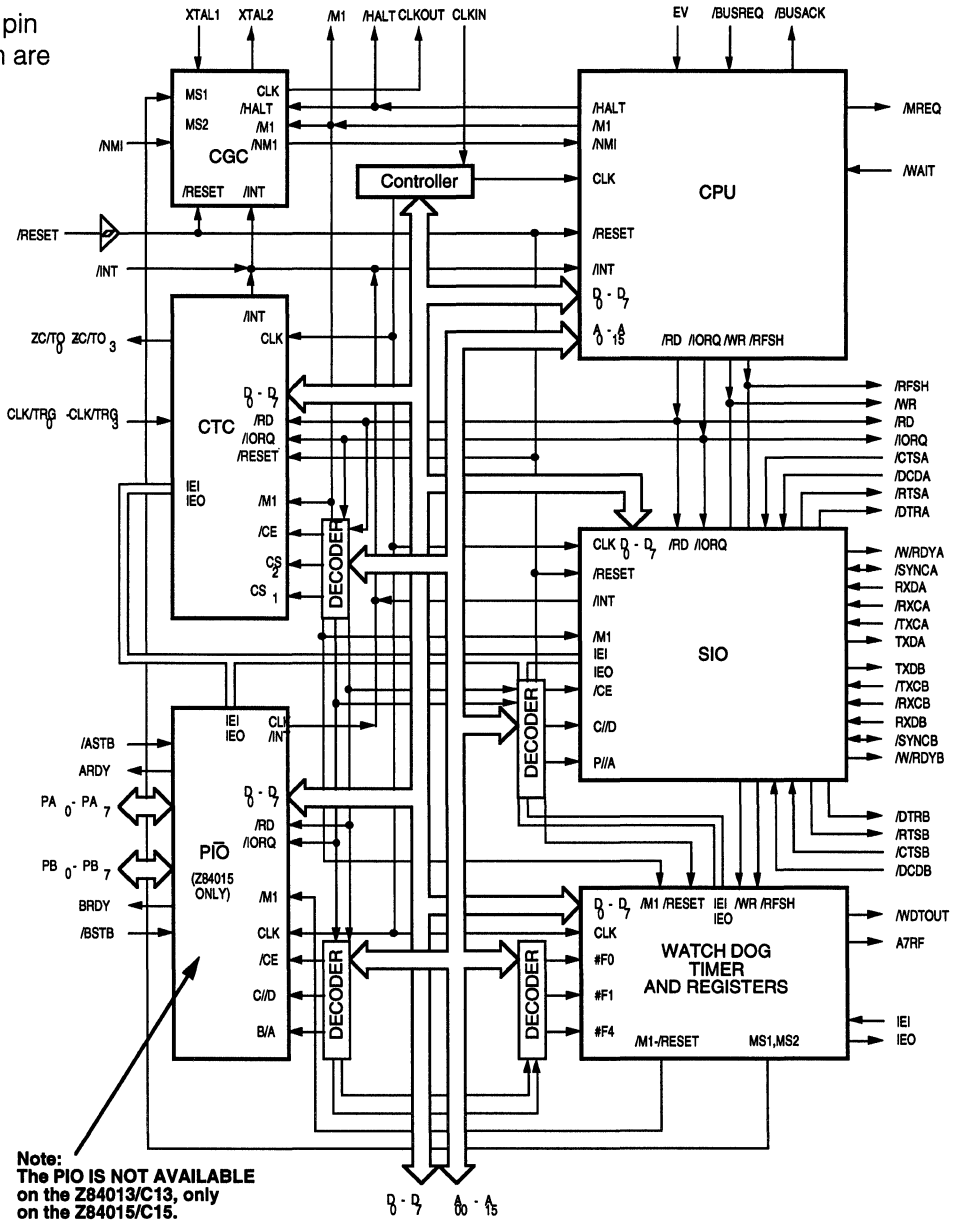


Figure 1b. Z84C11 Block Diagram

GENERAL DESCRIPTION

The Z84013 and Z84C13 are a series of Intelligent Peripheral Controllers (IPC) targeted for a broad range of applications from error correcting modems to enhancement/cost reduction of existing hardware using Z80 based discrete devices. The products are software and hardware compatible with discrete devices Z84C00, Z84C30 and Z84C40.

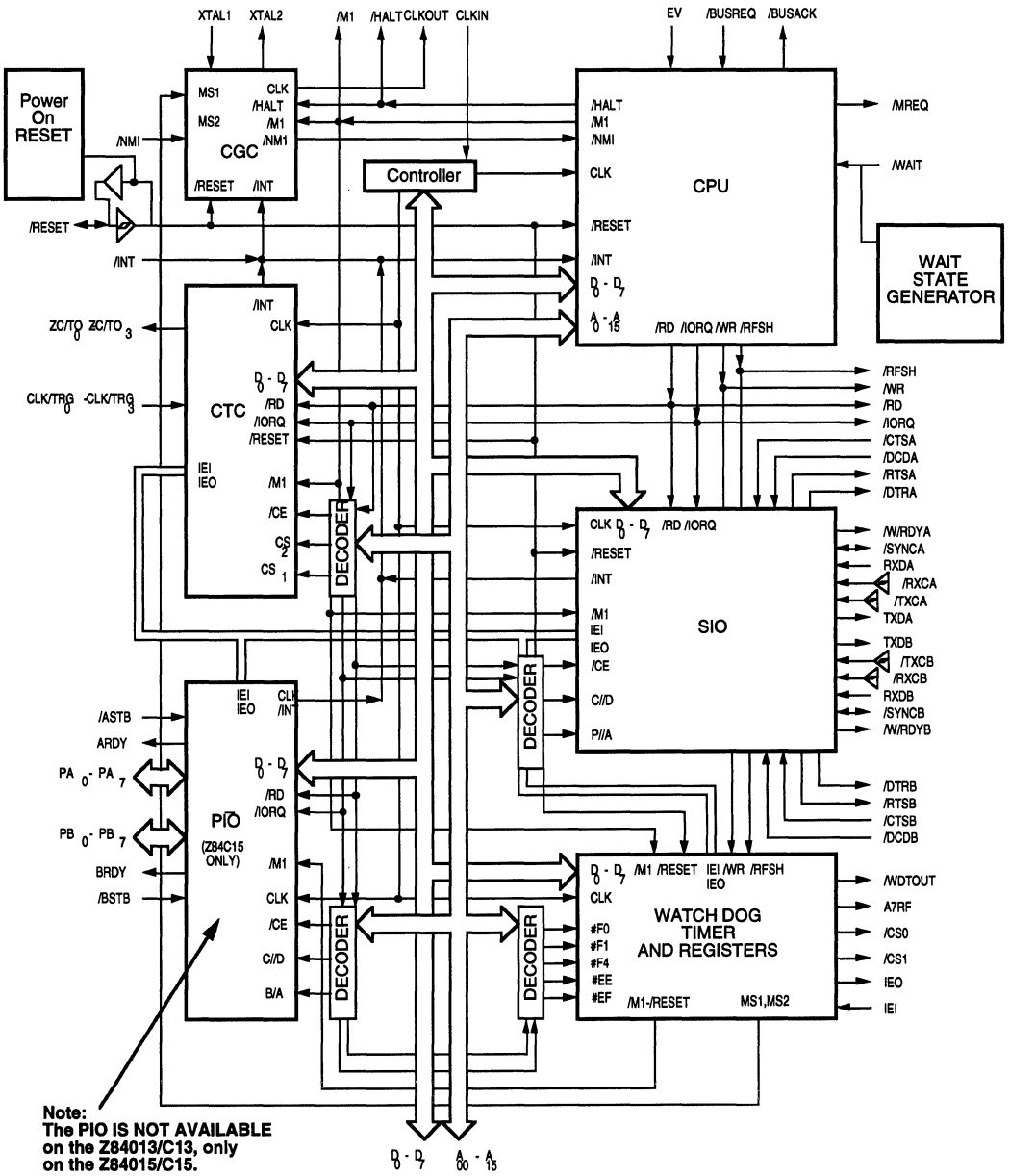
The enhanced version, Z84C13, is pin compatible with the Z84013 and both are housed in 84-pin PLCC packages.



Block Diagram for Z84013 IPC

FEATURES

- *Z84C13 Enhancements:*
  - *Power-On Reset*
  - *Two Additional Chip Selects*
  - *Wait State Generator*
  - *Simplified EV Mode*
  - *Schmitt Trigger I/O on Tx/Rx Clock*
  - *Crystal Divide-by-One Mode*
  - *32-Bit CRC Generation/Checking*
- *Z84C13 Features Z84013 and Above Enhancements*
- *6, 10 MHz Operation*
- *Low Power Consumption - Three Operating Modes*
- *Z84013 Features:*
  - *Z84C00 CPU*
  - *Z84C40 (SIO) - Two Serial Channels*
  - *Z84C30 (CTC) - 4x8 Bit C/T*
  - *Clock Generator Controller (CGC)*
  - *Watch-Dog Timer (WDT)*
- *Voltage Range 5V ±10%*
- *84-Pin PLCC Package*

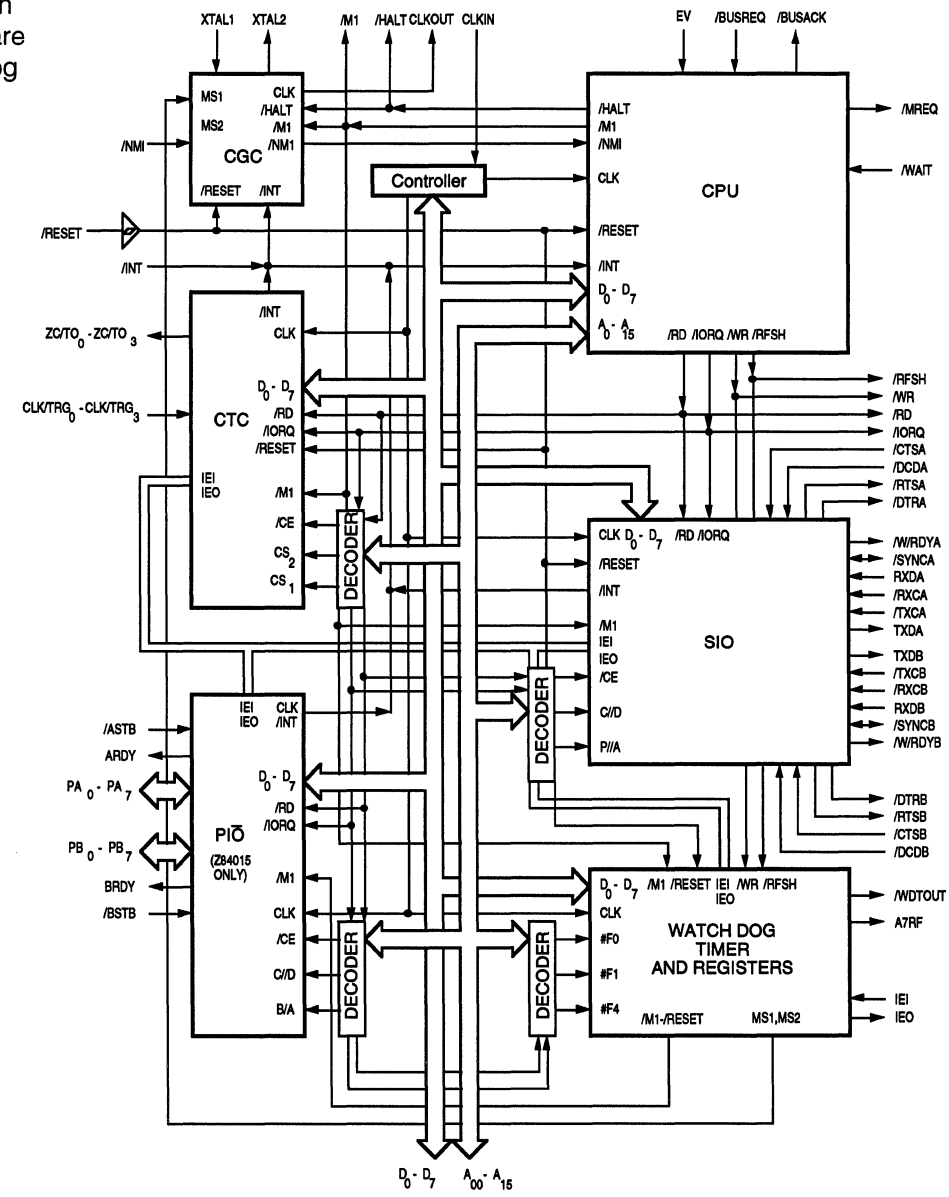


Block Diagram for Z84C13

GENERAL DESCRIPTION

The Z84015 and Z84C15 are a series of Intelligent Peripheral Controllers (IPC) targeted for a broad range of applications from error correction modems/faxes, to enhancement/cost reduction of existing Z80 hardware using Z80 based discrete devices. The products are software and hardware compatible with the discrete devices Z84C00, Z84C20, Z84C30 and Z84C40.

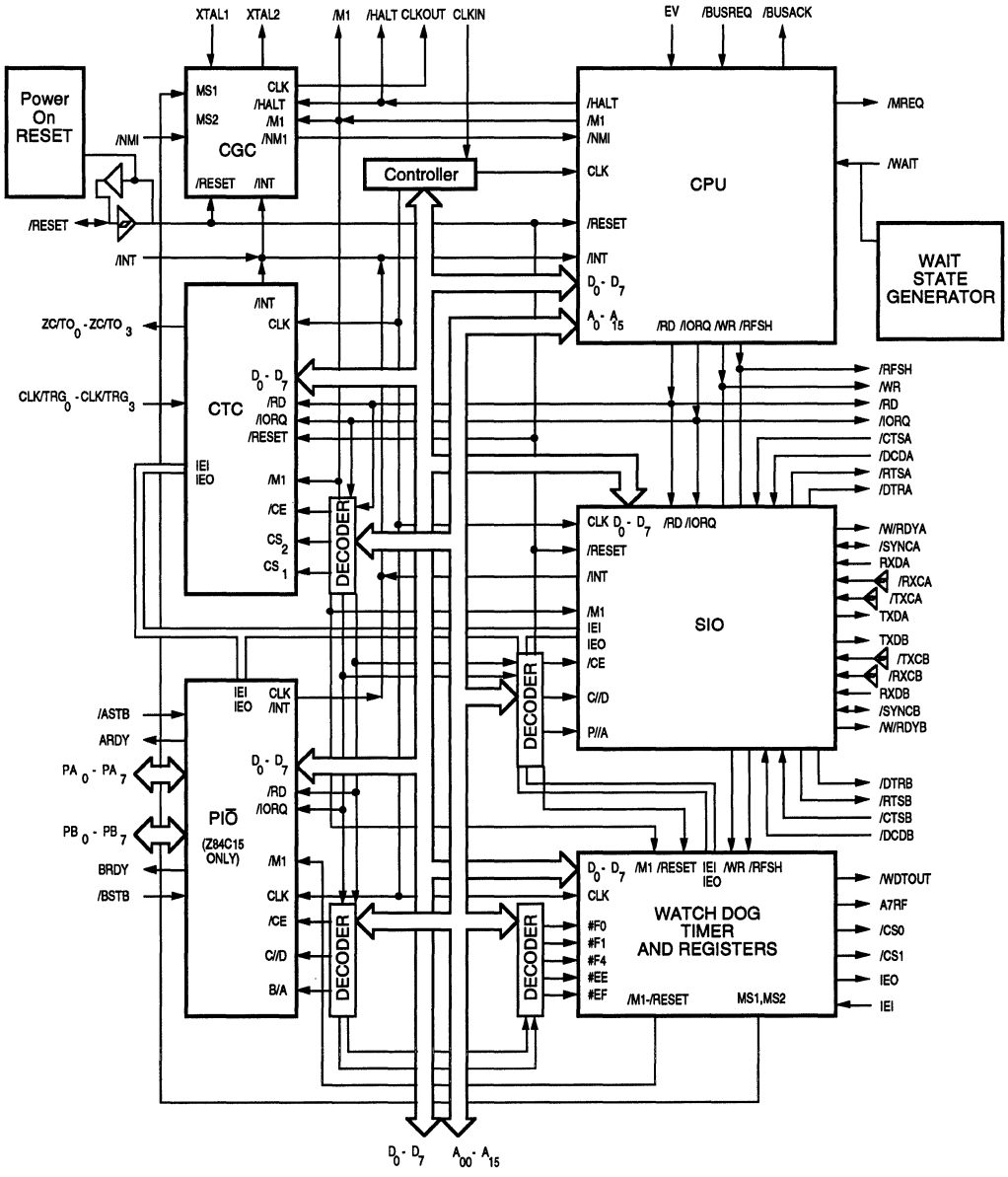
The enhanced version, Z84C15, is pin compatible with the Z84015 and both are housed in a 100-pin QFP package. Zilog also offers Z84C15 in a 100-pin VQFP package.



Block Diagram for Z84015 IPC

FEATURES

- *Z84C15 Enhancements:*
  - *Power-On Reset*
  - *Two Additional Chip Select Pins*
  - *32-Bit CRC for Channel A of SIO*
  - *Wait State Generator*
  - *Simplified EV Mode*
  - *Schmitt-Trigger I/O, No Tx/Rx Clock*
  - *Crystal Divide-by-One Mode*
- *Z84C15 Features the Z84015 and Above Enhancements*
- *Z84015 Features:*
  - *Z84C00 - CPU*
  - *Z84C40 - SIO - Two Serial Channels*
  - *Z84C30 - CTC - 4x8 bit C/T*
  - *Z84C20 - PIO*
  - *Watch-Dog Timer (WDT)*
  - *Clock Generator Controller (CGC)*
- *Low Power Consumption*
  Three Operating Modes
- *6, 10 MHz Operation*
- *16 MHz Operation for Z84C15 Only.*
- *Voltage Range 5V±10%*
- *100-Pin QFP Package*
- *100-Pin VQFP Package for Z84C15*



Block Diagram for Z84C15 IPC

Z80180 CMOS Z180™ MICROPROCESSOR

GENERAL DESCRIPTION

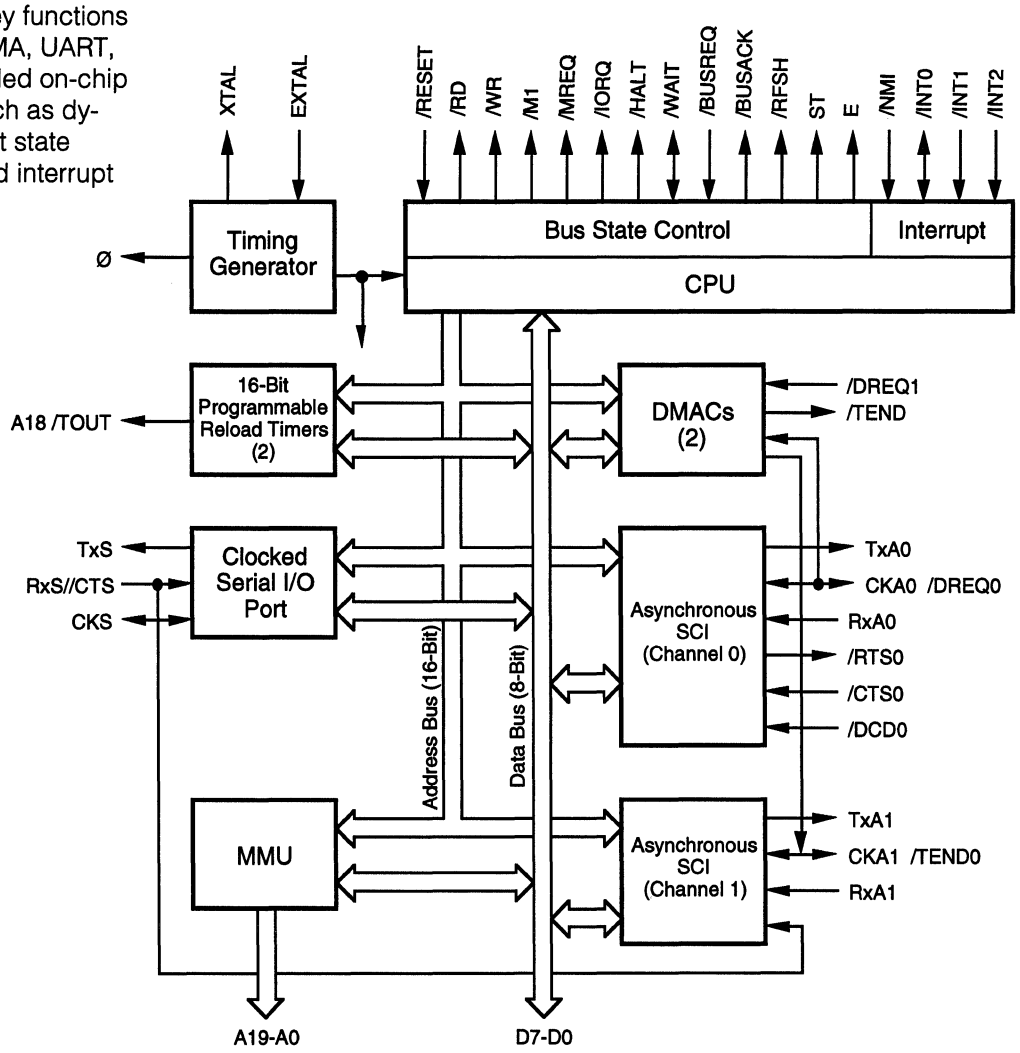
The Z80180 is an 8-bit MPU which provides the benefits of reduced system costs and low power operation while offering higher performance and maintaining compatibility with a large base of industry standard software written around the Zilog Z80 CPU.

Higher performance is obtained by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1 Mbyte of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several "glue" functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

FEATURES

- *Operating Frequency to 10 MHz*
- *6 MHz Version Supports 6.144 MHz CPU Clock*
- *On-Chip MMU Supports Extended Memory*
- *Two DMA Channels*
- *On-Chip Wait State Generators*
- *Two UART Channels*
- *Two 16-Bit Timer Channels*
- *On-Chip Interrupt Controller*
- *On-Chip Clock Oscillator/Generator*
- *Clocked Serial I/O Port*
- *Code Compatible with Zilog Z80 CPU*
- *Seven Additional Instructions*
- *Available in 64-Pin DIP, 68-Pin PLCC, and 80-Pin QFP*



GENERAL DESCRIPTION

The Z8S180 (static 180) is an 8-bit MPU which provides the benefits of reduced system costs and low power operation while offering higher performance and maintaining compatibility with a large base of industry standard software written around the Zilog Z80 CPU.

Higher performance is obtained by virtue of higher operating frequencies, reduced instruction execution times, an enhanced instruction set, and an on-chip memory management unit (MMU) with the capability of addressing up to 1 Mbyte of memory.

Reduced system costs are obtained by incorporating several key system functions on-chip with the CPU. These key functions include I/O devices such as DMA, UART, and timer channels. Also included on-chip are several "glue" functions such as dynamic RAM refresh control, wait state generators, clock oscillator, and interrupt controller.

Low power operation is obtained by incorporating several power-down operating modes. In addition to the two operating modes supported by the Z80180, the SLEEP mode and the SYSTEM STOP mode. The Z8S180 incorporates two additional power-saving modes: STANDBY and IDLE. The power-down modes supported by the Z8S180 are:

(a) SLEEP mode places the CPU into a "stopped" state.

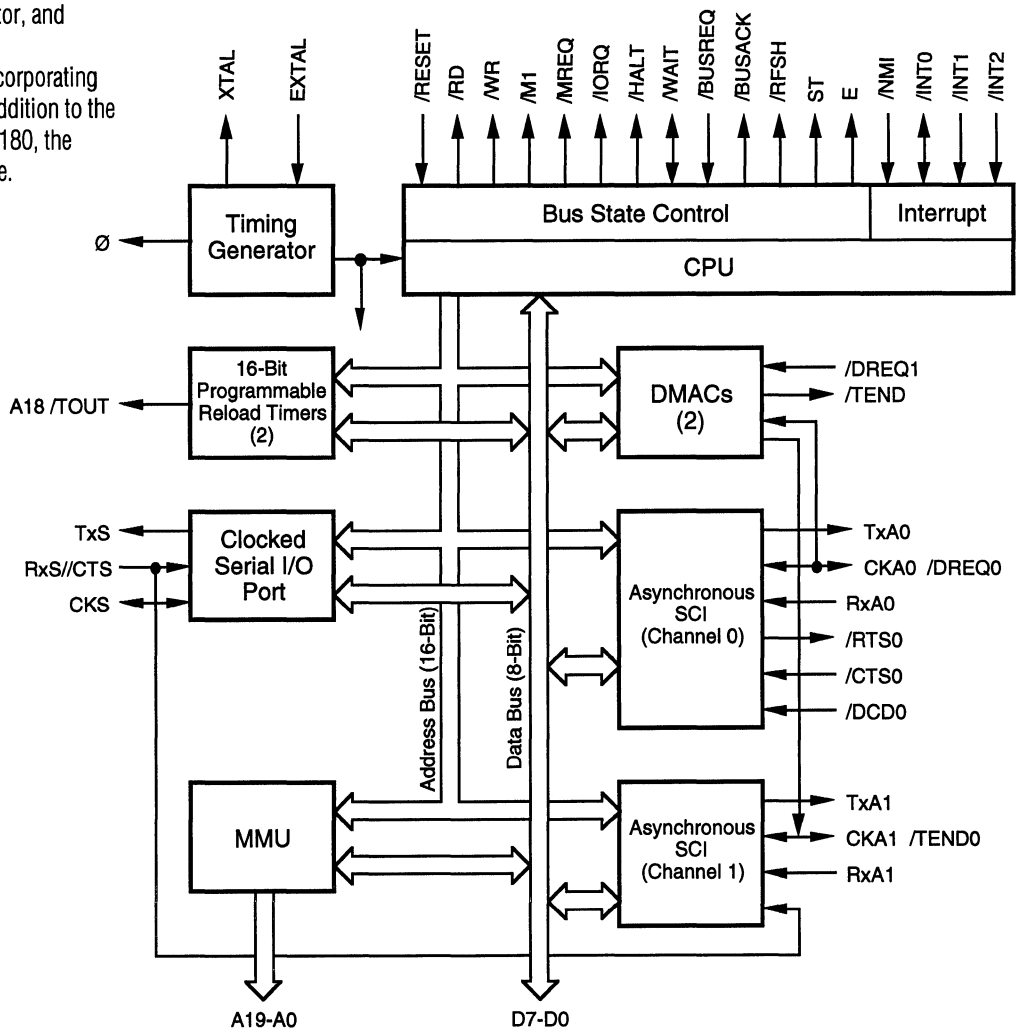
(b) SYSTEM STOP mode places both the CPU and on-chip peripherals into a "stopped" state.

(c) STANDBY mode places the CPU, on-chip peripherals, external clock and internal clock completely into a "stopped" state, thereby reducing power consumption to minimal.

(d) IDLE mode leaves the clock oscillator running while placing the CPU, on-chip peripherals and the clock for the rest of the internal circuit into a "stopped" state.

FEATURES

- *Operating Frequency to 16, 20 MHz*
- *Fully Static*
- *Standby Mode*
- *Low EMI Mode*
- *On-Chip MMU Supports Extended Memory*
- *Two DMA Channels*
- *On-Chip Wait State Generators*
- *Two UART Channels*
- *Two 16-Bit Timer Channels*
- *On-Chip Interrupt Controller*
- *On-Chip Clock Oscillator/Generator*
- *Clocked Serial I/O Port*
- *Code Compatible with Zilog Z80 CPU*
- *Seven Additional Instructions*
- *Available in 68-Pin PLCC, and 80-Pin QFP*



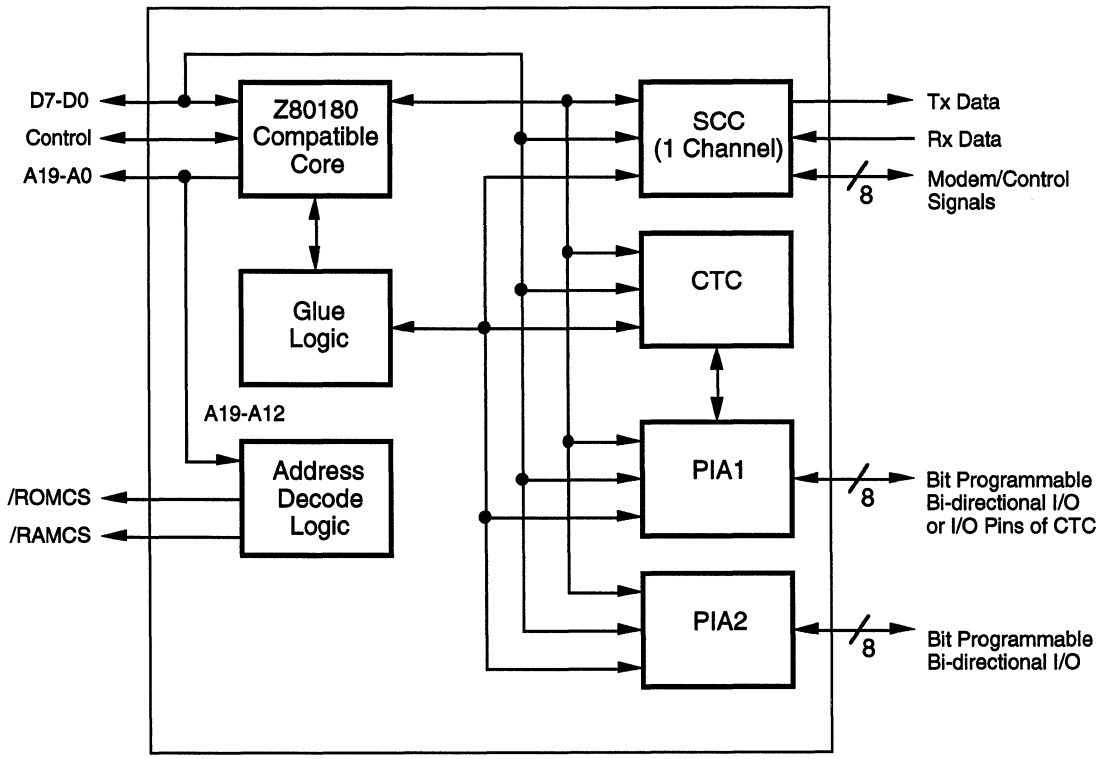
Z80181 CMOS ZIO™ ZILOG I/O CONTROLLER

GENERAL DESCRIPTION

Zilog's Z80181 I/O Controller (ZIO™) is a CMOS 8-bit microprocessor containing the Z180 compatible MPU (Z181 MPU), one channel of Z85C30 Serial Communication Controller (SCC), Z84C30 (CTC), two 8-bit general purpose parallel ports, and two chip select signals into a single 100-pin QFP (Quad Flat Pack) package. This high-end superinte-grated intelligent peripheral controller is targeted for a broad range of intelligent communication control applications, i.e., terminals, printers, modems, slave communication processors for 8-, 16- and 32- bit MPU based systems. The Z181 is also ideal for enhancement/cost reductions of existing hardware using Z80/Z180 with Z8530/ Z85C30 applications.

FEATURES

- *Z80180 Compatible MPU Core with One Channel of Z85C30 SCC, Z80 CTC, Two 8-Bit General-Purpose Parallel Ports, and Two Chip Select Signals.*
- *High Speed Operation (10/12.5 MHz)*
- *Low Power Consumption in Two Operating Modes:*
  (TBD) mA Typ. (Run Mode)
  (TBD) mA Typ. (STOP Mode)
- *Voltage Range 5V±10%*
- *TTL/CMOS Compatible*
- *Clock Generator*
- *Z84C30 CTC*
- *One Channel of Z85C30 Serial Communication Controller (SCC)*
- *Z180 Compatible MPU Core, which has:*
  - *Enhanced Z80 CPU Core*
  - *Memory Management Unit (MMU) Enables Access to 1MB of Memory*
  - *Two Asynchronous Channels*
  - *Two DMA Channels*
  - *Two 16-Bit Timers*
  - *Clocked Serial I/O Port*
- *Two 8-Bit General-Purpose Parallel Ports*
- *Memory Configurable RAM and ROM Chip Select Pins*
- *100-Pin QFP Package*



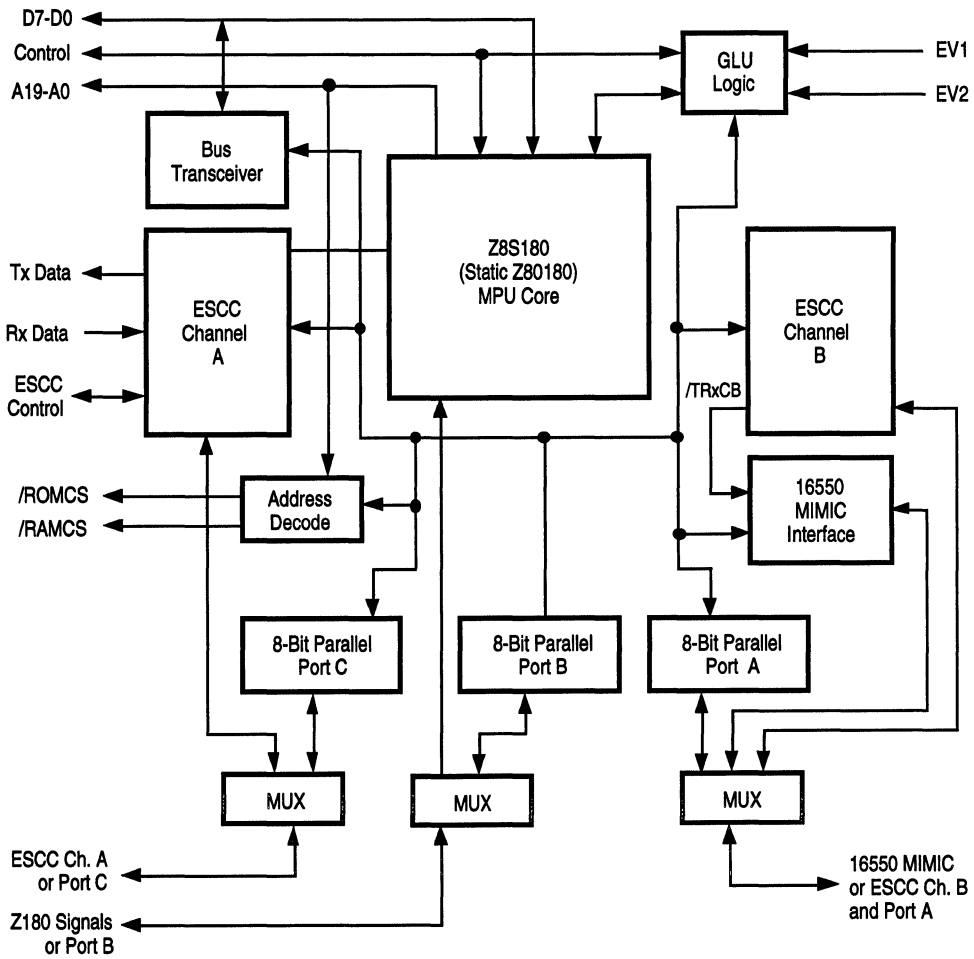
Z80181 = Z180 + SCC/2 + CTC + PIA

GENERAL DESCRIPTION

The Z80182 is the Zilog Intelligent Peripheral controller chip that can be used for modems, faxes, voice messaging and other communications applications. It uses the static Z80180 microprocessor (Z8S180 MPU core) linked with two channels of the industry standard Z85230 ESCC (Enhanced Serial Communications Controller), 24 bits of Parallel I/O, and a 16550 MIMIC for direct connection to the IBM PC, XT, AT, bus. Two different modes of operation allow complete flexibility for both internal PC and external applications. Also current PC modem software compatibility can be maintained with the Z80182's ability to MIMIC the 16550 UART chip. The Z80180 acts as an interface between the ESCC and 16550 MIMIC interface when used in internal applications and between the two ESCC channels in the external applications. This interface allows for data compression and error correction on outgoing and incoming data.

FEATURES

- *Z8S180 MPU (Static Version of Z180™)*
  - *Code Compatible with Zilog Z80® CPU*
  - *Additional Instructions*
  - *Operating Frequency DC to 16 MHz and 20 MHz*
  - *Two DMA Channels*
  - *On-Chip Wait State Generators*
  - *Two UART Channels*
  - *Two 16-Bit Timer Counters*
  - *On-Chip Interrupt Controller*
  - *On-Chip Clock Oscillator*
  - *Generator with Idle and Standby Modes of Operation*
  - *Clocked Serial I/O Port*
- *Two ESCC™ Channels*
- *Three 8-Bit Parallel I/O Ports*
- *16550 Compatible MIMIC Interface for Direct Connection to PC, XT, AT, PS2 PC and Microchannel Bus*
- *Package 100-Pin QFP (Quad Flat Package) or 100-Pin VQFP (Very Small Quad Flat Package)*
- *A Fully Static Device*



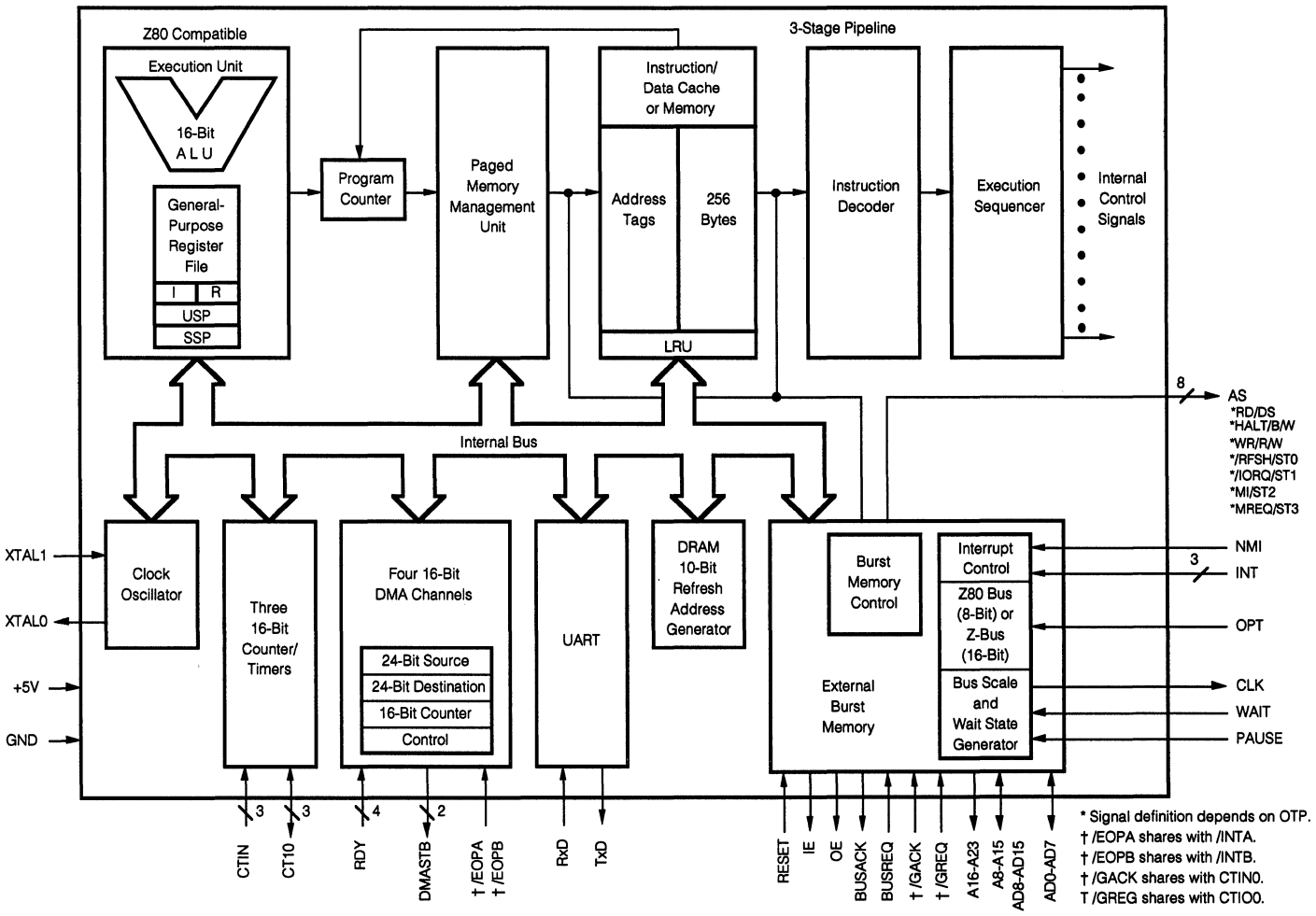
Z80280 Z280® MICROPROCESSOR

GENERAL DESCRIPTION

The Z80280 brings 16-bit CPU and sophisticated features required by complex, high performance applications to the Z80 architecture. The Z280 maintains complete object code compatibility with the Z80. One of the unique features of the Z280 is its bus size. By strapping a single pin on the chip, the designer can select 8- or 16-bit bus widths. Thus, to use existing designs, an 8-bit Z80 compatible bus can be used. Higher performance systems can be designed using the Z280's 16-bit mode, in which all memory references use true 16-bit accesses. A single processor can be used in both medium and high performance products, without changing the software. The Z280 includes a Memory Management Unit (MMU), which gives the processor access to 16 Mbytes of memory. Other features of the Z280 include on-chip instruction and cache memory, 3-stage pipeline, dual operating modes, four channel DMA Controller, three 16-bit counter-timers, programmable refresh and wait state generation, and a serial port with on-chip baud rate generation.

FEATURES

- *Designed in CMOS for Low Power Operations*
- *Enhanced Z80 CPU Instruction Set that Maintains Object-Code Compatibility with Z80 Microprocessor.*
- *Three-Stage Pipeline, 16-Bit CPU Architecture with User and System Modes.*
- *Direct Co-Processor and Multiprocessor Interface Support*
- *On-Chip Memory Management Unit (MMU) Addresses up to 16 Mbytes.*
- *20 and 25 MHz Oscillator Clock Frequency*
- *On-Chip 256-Byte Instruction and Data Associative Cache Memory with Burst Load.*
- *High Performance 16-Bit Z-BUS Interface or 8-Bit Z80 CPU Compatible Bus Interface.*
- *Three On-Chip 16-Bit Counter/Timers*
- *Four On-Chip DMA Channels*
- *On-Chip Full Duplex UART*
- *Refresh Controller for Dynamic RAMs*
- *On-Chip Oscillator of Direct Input Clock Options*
- *68-Pin PLCC Package*



GENERAL DESCRIPTION

Zilog's low voltage devices operate from 2.7 Volts up to 5.5 Volts. The specifications for each device consists of two sets; one set is for V_{CC} at 5V ±10% and the other is for 3V ±10%. For the voltage range between 3.3-4.5V, the 3V specification applies.

The set for 5V is identical to the existing product specifications. The set for 3V has unique DC specifications. For the AC specification, refer to the following individual specification sections. In general, speed at 3V is half of the speed at 5V operation.

Operating temperature is an extended temperature range (-40°C to +100°C) at 5V operation and standard temperature range (0 to +70°C) at 3V operation.

This document has the preliminary specifications for eight of Zilog's Low Voltage Component versions listed below.

DC Parameter Specifications

There are two sets of DC specifications defined for each device; one for 5V ± 10% and the other is 3V ± 10%. The 3V specification set is listed by the device type; for the DC specification of V_{CC}=5V ± 10%, refer to the particular device specification for 5V products.

AC Parameter Specifications

AC specification of each device are identical to the discrete components AC characteristics given for 5V ±10%.

Operating Speeds for 3V/5V Ranges

Product	Speed MHz 3V ± 10%	5V ± 10%
Z84L00 Low Voltage Z80® CPU	10	20
Z84L15 Low Voltage Z84C15 EPIC	6	16
Z84L90 Low Voltage Z84C90 Z80® KIO™	6	12.5
Z8L180 Low Voltage Z180™ MPU	10	20
Z8L181 Low Voltage Z181™ ZIO™	6	12.5
Z85L30 Low Voltage CMOS SCC	8.5	16.5
Z8L230 Low Voltage ESCC™	10	20
Z8L233 Low Voltage EMSCC™	10	20

Z8000®
PRODUCT FAMILY

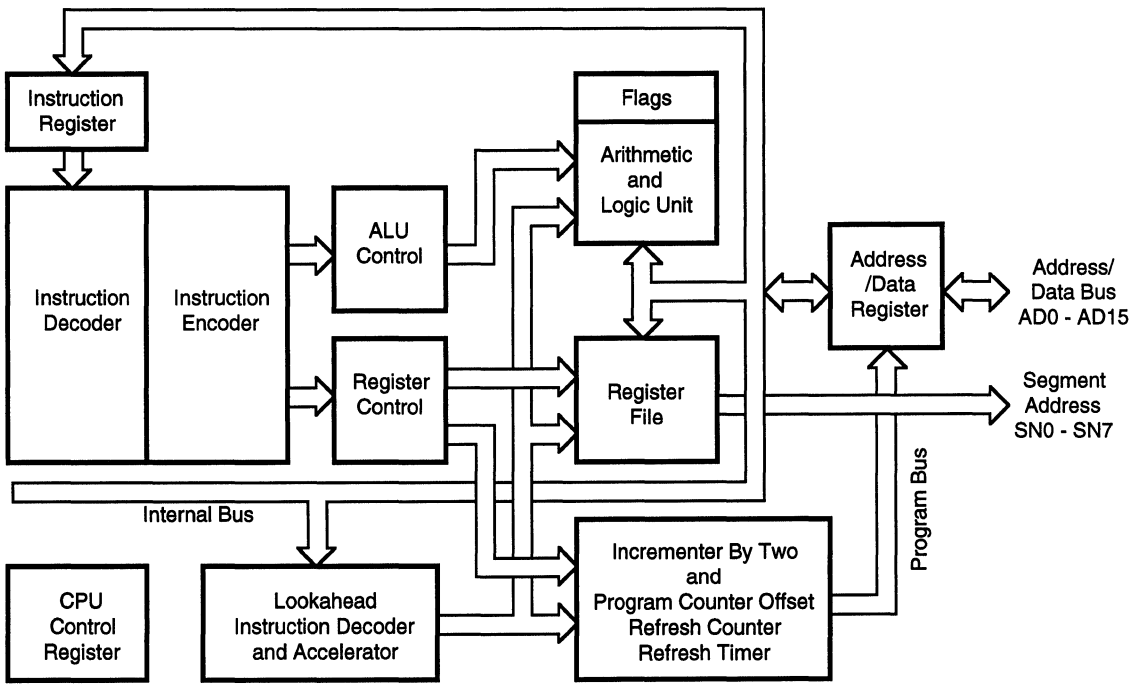
GENERAL DESCRIPTION

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; abundant resources on register, data types, addressing modes and addressing range, and a regular architecture that enhances throughput by avoiding critical bottlenecks such as implied or dedicated registers.

The Z8000 CPU is offered in two versions: the Z8001 segmented CPU and the Z8002 nonsegmented CPU. The main difference is in addressing range. The Z8001 can directly address 8 megabytes of memory; the Z8002 directly addresses 64 kilobytes. The two operation modes - system and normal - and the distinction between code, data, and stack spaces within each mode, allows memory extension up to 48 megabytes for the Z8001 and 384 kilobytes for the Z8002.

FEATURES

- *Regular, Easy-to-Use Architecture.*
- *Instruction Set More Powerful Than Many Microcomputers.*
- *Directly Addresses 8 Mbytes.*
- *Eight User-Selectable Addressing Modes.*
- *Seven Data Types that Range from Bits to 32-Bit Long Words and Byte and Word Strings.*
- *System and Normal Operating Modes.*
- *Separate Code, Data, and Stack Spaces.*
- *Sophisticated Interrupt Structure.*
- *Resource-Shaping Capabilities for Multiprocessing Systems.*
- *Multi-Programming Support.*
- *"C" Compiler Support.*
- *32-Bit Operations, Including Signed Multiply and Divide.*
- *Z-BUS® Compatible.*
- *6 and 10 MHz Clock Rate.*



Z8016 DIRECT MEMORY ACCESS CONTROLLER

GENERAL DESCRIPTION

The Z8016 DMA Controller is a high performance data transfer device designed to match the power and addressing capability of the Z8000 CPUs. In addition to providing block data transfer capability between memory and peripherals, each of the two DMA channels can perform peripheral-to-peripheral and memory-to-memory transfers. A special Search mode of operation compares data read from memory or peripherals with the content of a pattern register. A search can be performed concurrently with transfers or as an operation in itself.

In all operations (Search, Transfer, and Transfer-and Search), the DMA can operate in either Flow-through or Fly-by transfer mode. In the Flow-through mode, data is stored temporarily within the DMA on its way from source to destination. In this mode, transfers can be made between a word-oriented memory and a byte-oriented peripheral through the bi-directional byte/word funneling option. In Fly-by mode, data is transferred in a single step (from source to destination), thus providing twice the throughput.

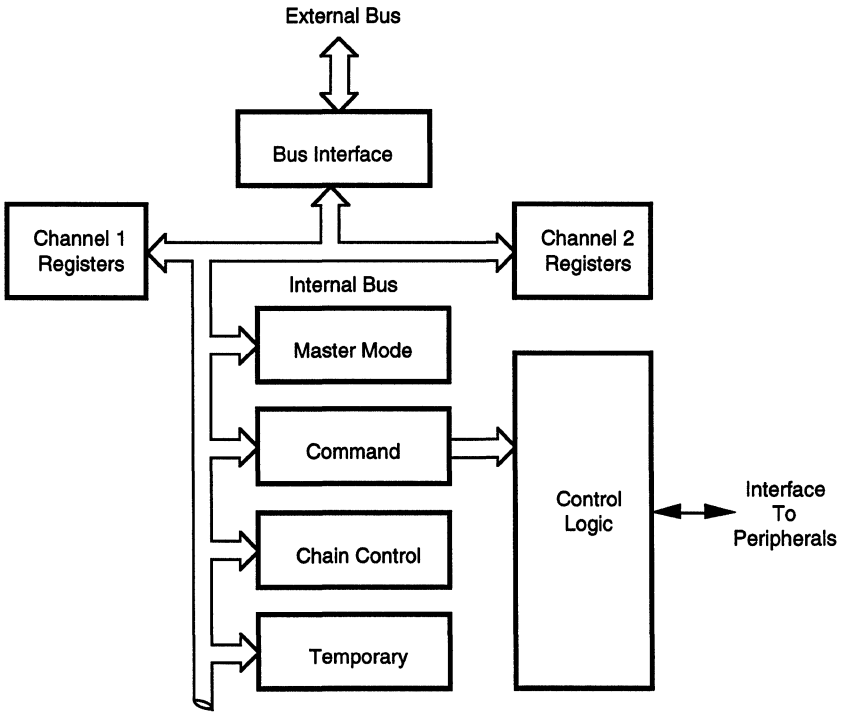
In addition to providing a hardware/WAIT input to accommodate different memory or peripheral speeds, the Z8016 DMA allows the user to program the automatic insertion of either zero, one, two, or four Wait states for either source or destination addresses. Alternately, the /WAIT input pin function can be disabled and these software-programmed Wait states are used exclusively.

The Z8016 minimizes CPU involvement by allowing each channel to load its control registers from memory automatically when a DMA operation is complete. By loading the address of the next block of control parameters as part of this operation, command chaining is accomplished. The only action required of the CPU is to load the address of the control parameter table into the channel's Chain Address register and then issue a Start Chain command.

The Demand Interleave operation allows the DMA to surrender the bus to the external system, or to alternate between internal channels. This capability allows for parallel operations between dual channels or between a DMA channel and the CPU.

FEATURES

- *Memory-to-peripheral transfers up to 4M bytes per second at 6 MHz.*
- *Memory-to-memory transfers up to 2M bytes per second at 6 MHz.*
- *Two fully independent, multi-function channels*
- *Masked data pattern matching for Search and Transfer-and-Search operations.*
- *Funneling Option that Permits Mixing of Byte and Word Data During Transfer Operations.*
- *Can Operate in Logical Address Space with Zilog Memory Management Units, Providing an 8 Mbyte Logical Addressing Range and 16 Mbyte Physical Addressing Range.*
- *Programmable Chaining Operation Provides Automatic Loading of Control Parameters from Memory into Each Channel.*
- *Software- or Hardware-Controlled Wait State Insertion.*
- *Z-BUS® Daisy-Chain Interrupt Hierarchy and Bus-Request Structure.*



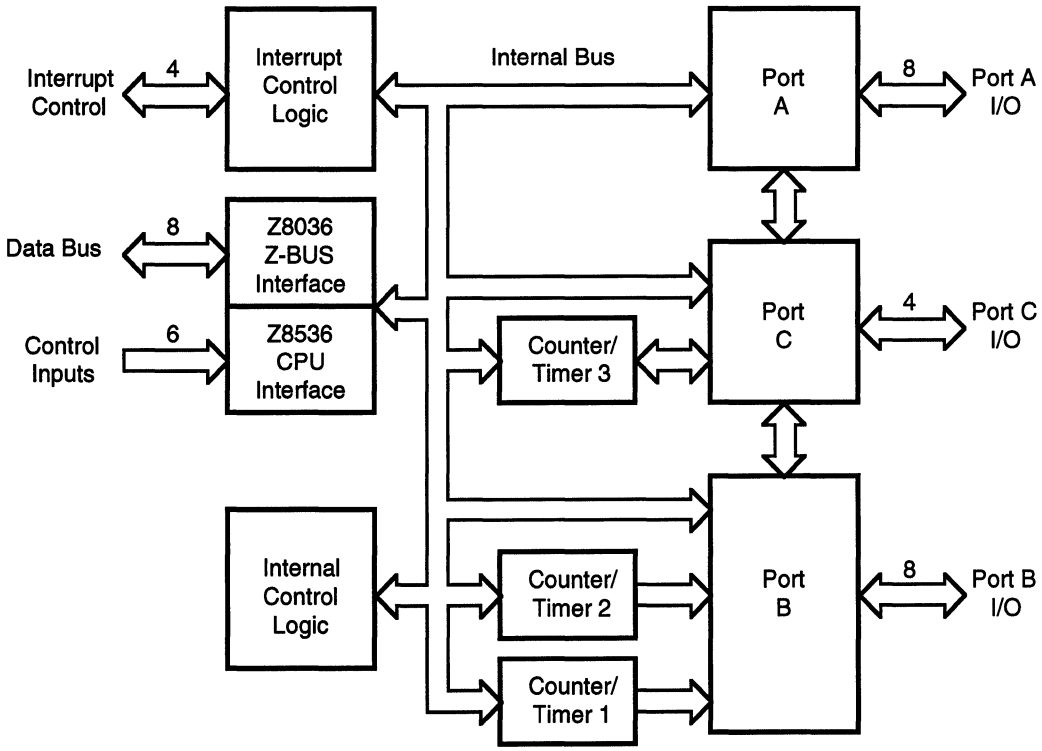
GENERAL DESCRIPTION

The Z8036/Z8536 CIO Counter/Timer and Parallel I/O devices are general purpose peripheral circuits, satisfying most counter/timer and parallel I/O needs encountered in system designs. These versatile devices contain three I/O ports and three counter/timers. Many programmable options tailor their configuration to specific applications.

The use of these devices is simplified by making all internal registers (command, status, and data) readable and (except for status bits) writable. In addition, each register is given its own unique address so that it can be accessed directly - no special sequential operations are required. The CIO is directly Z-BUS® compatible.

FEATURES

- *Two Independent 8-Bit, Double-Buffered, Bi-Directional I/O Ports, Plus a 4-Bit Special Purpose I/O Port. I/O Ports Feature Programmable Polarity, Programmable Direction (Bit Mode), "Pulse Catchers", and Programmable Open-Drain Outputs.*
- *Four Handshake Modes, Including 3-Wire IEEE-488 Mode*
- *Flexible Pattern-Recognition Logic, Programmable as a 16-Vector Interrupt Controller.*
- *REQUEST//WAIT Signal for High-Speed Data Transfer*
- *Three Independent 16-Bit Counter/Timers with up to Four External Access Lines per Counter/Timer (Count Input, Output, Gate, and Trigger), and Three Output Duty Cycles (Pulsed, One-Shot, and Square-Wave), Programmable as Retriggerable or Non-Retriggerable.*
- *Easy to use Since all Registers are Read/Write and Directly Addressable*
- *6 MHz Operation*



Z8038 FIO FIFO INPUT/OUTPUT INTERFACE UNIT

GENERAL DESCRIPTION

The Z8038 FIO (FIFO Input/Output Interface Unit) provides an asynchronous 128-byte FIFO buffer between two CPUs or between a CPU and a peripheral device. This buffer interface expands to a 16-bit or wider data path and expands in depth to add as many Z8060 FIFOs as are needed.

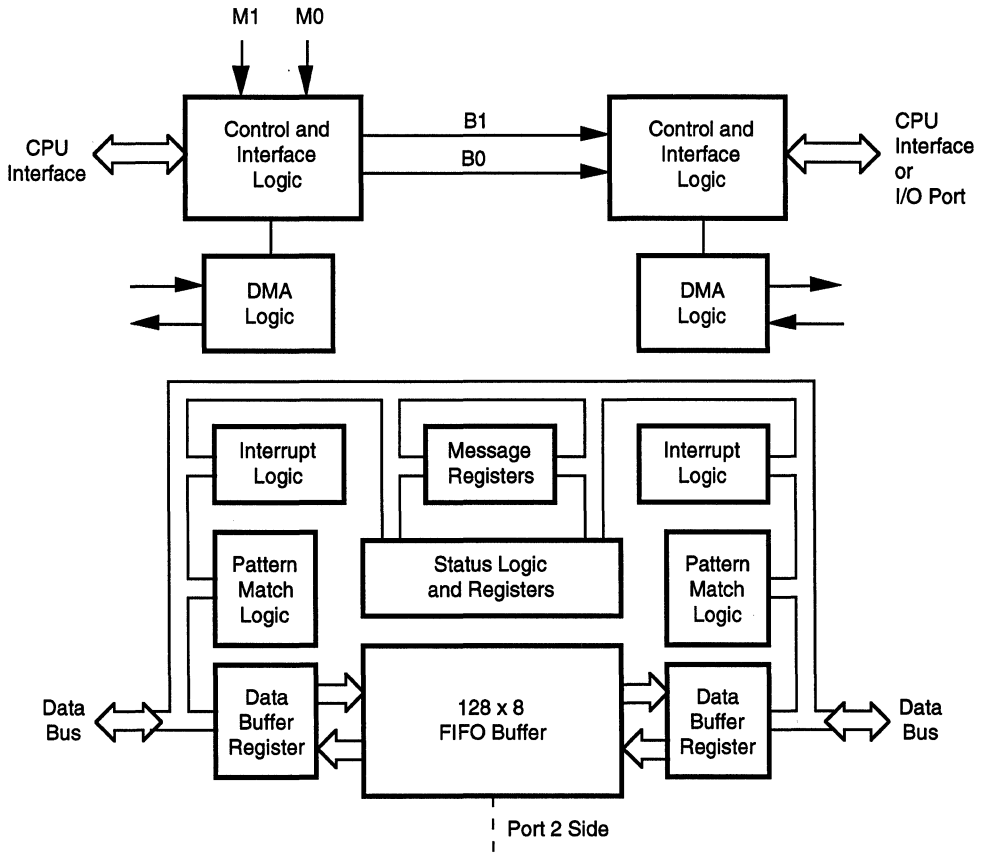
The Z8038 manages data transfers by assuming Z-BUS® microprocessor (a generalized microprocessor interface), Interlocked 2-Wire Handshake, and 3-Wire Handshake operating modes. These modes interface dissimilar CPUs or CPUs and peripherals running under differing speeds or protocols, allowing asynchronous data transactions and improving I/O overhead by as much as two orders of magnitude.

The Z8038 supports the Z-BUS interrupt protocols, generating seven sources of interrupts upon any of the following events: a write to a message register, change in data direction, pattern match, status match, over/underflow error, buffer full and buffer empty status. Each interrupt source can be enabled or disabled, and can also place an interrupt vector on the port address/data lines.

The data transfer logic of the Z8038 has been specially designed to work with DMA (Direct Memory Access) devices for high-speed transfers. It provides for data transfers to or from memory each machine cycle, while the DMA device generates memory address and control signals. The Z8038 also supports the variable sized block length, improving system throughput when multiple variable length messages are transferred amongst several sources.

FEATURES

- *128-Byte FIFO Buffer Provides Asynchronous Bi-Directional CPU/CPU or CPU/Peripheral Interface, Expandable to any Width in Byte Increments by use of Multiple Z8038s.*
- *Interlocked 2-Wire or 3-Wire Handshake Logic Port Mode; Z-BUS® interface.*
- *Pattern Recognition Logic Stops DMA Transfers and/or Interrupts CPU; Preset Byte Count can Initiate Variable-Length DMA Transfers.*
- *Seven Sources of Vectored/Nonvectored Interrupt which Include Pattern-Match, Byte Count, Empty for Full Buffer Status; a Dedicated "Mailbox" Register with Interrupt Capability Provides CPU/CPU Communication.*
- */REQUEST/WAIT Lines Control High-Speed Data Transfers.*
- *All Functions are Software Controlled via Directly Addressable Read/Write Registers.*
- *6 MHz Operation*



GENERAL DESCRIPTION

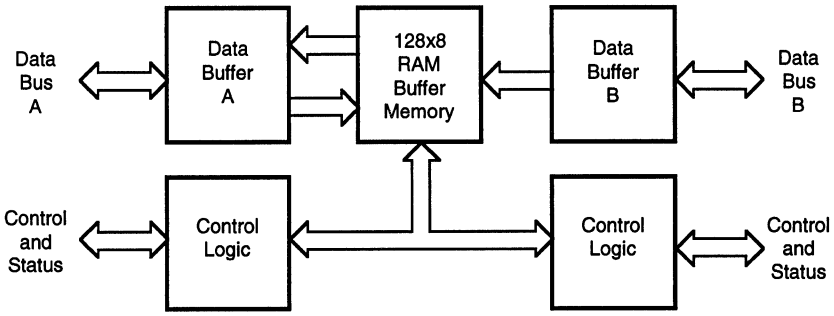
The Z8060 First-In First-Out (FIFO) Buffer Unit consists of a 128-bit-by-8-bit memory, bi-directional data transfer and handshake logic. The structure of the FIFO unit is similar to that of other available buffer units. The FBU is a general purpose unit; its handshake logic is compatible with that of other members of Zilog's Z8 and Z8000 Families.

Several Z8060's can be cascaded end-to-end without limit to form a parallel 8-bit buffer of any desired length (in 128-byte increments). Any number of single or multiple unit FIFO serial buffers can be connected in parallel to form buffers of any desired width (in 8-bit increments).

The FIFO Buffer Units are available in 28-pin packages.

FEATURES

- *Bi-Directional, Asynchronous Data Transfer Capability*
- *Large 128-Bit-by-8-Bit Buffer Memory*
- *2-Wire, Interlocked Handshake Protocol*
- *Tri-State Data Outputs*
- *Direct Connection of Empty and Full Outputs for Sensing of Multiple-Unit Buffers.*
- *Any Number of FIFOs May be Connected in Parallel or in Series to Form a Buffer of any Desired Length or Width.*
- *1 MByte/Second Transfer Rate*



Z8068 DATA CIPHERING PROCESSOR

GENERAL DESCRIPTION

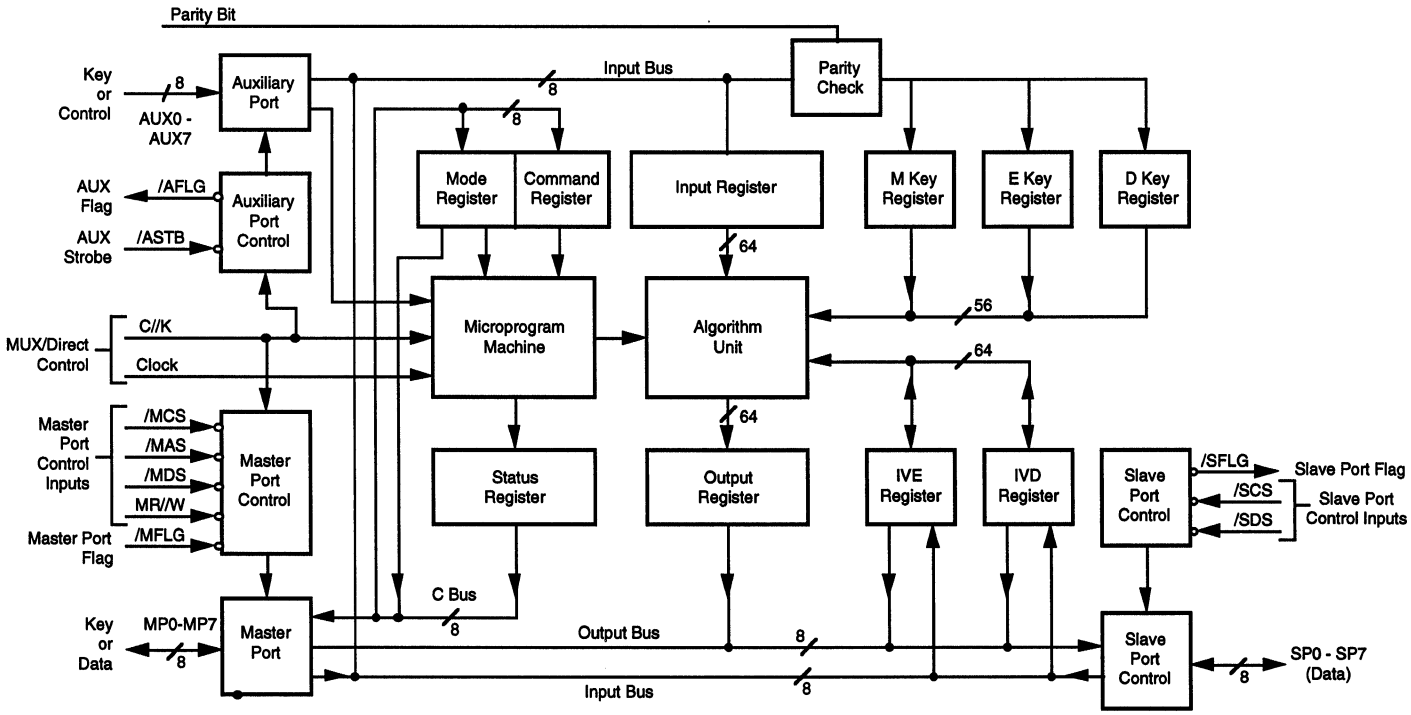
The Z8068 Data Ciphering Processor (DCP) is an LSI device which contains the circuitry to encrypt and decrypt data using National Bureau of Standards encryption algorithms. It is designed to be used in a variety of environments, including dedicated controllers, communication concentrators, terminals, and peripheral task processors in general processor systems.

The DCP provides a high throughput rate using Cipher Feedback, Electronic code book, or Cipher Block Chain operation modes. The provisions of separate ports for key input, clear data, and enciphered data enhances security.

The host system communicates with the DCP using commands entered in the master port or through auxiliary control lines. Once set up, data can flow through the DCP at high speeds because input, output and ciphering activities can be performed concurrently. External DMA control can easily be used to enhance throughput in some system configurations.

FEATURES

- *Encrypts and Decrypts Data using the National Bureau of Standards Encryption Algorithm.*
- *Data Rates Greater than 1 Mbytes per Second can be Handled.*
- *Three Separate Registers for Encryption, Decryption, and Master Keys Improve System Security and Throughput by Eliminating Frequent Reloading of Keys.*
- *Supports Three Standard Ciphering Modes: Electronic Code Book, Chain Block and Cipher Feedback.*
- *Three Separate Programmable Ports (Master, Slave, and Key Data) Provide Hardware Separation of Encrypted Data, Clear Data, and Keys.*
- *Key Parity Check*



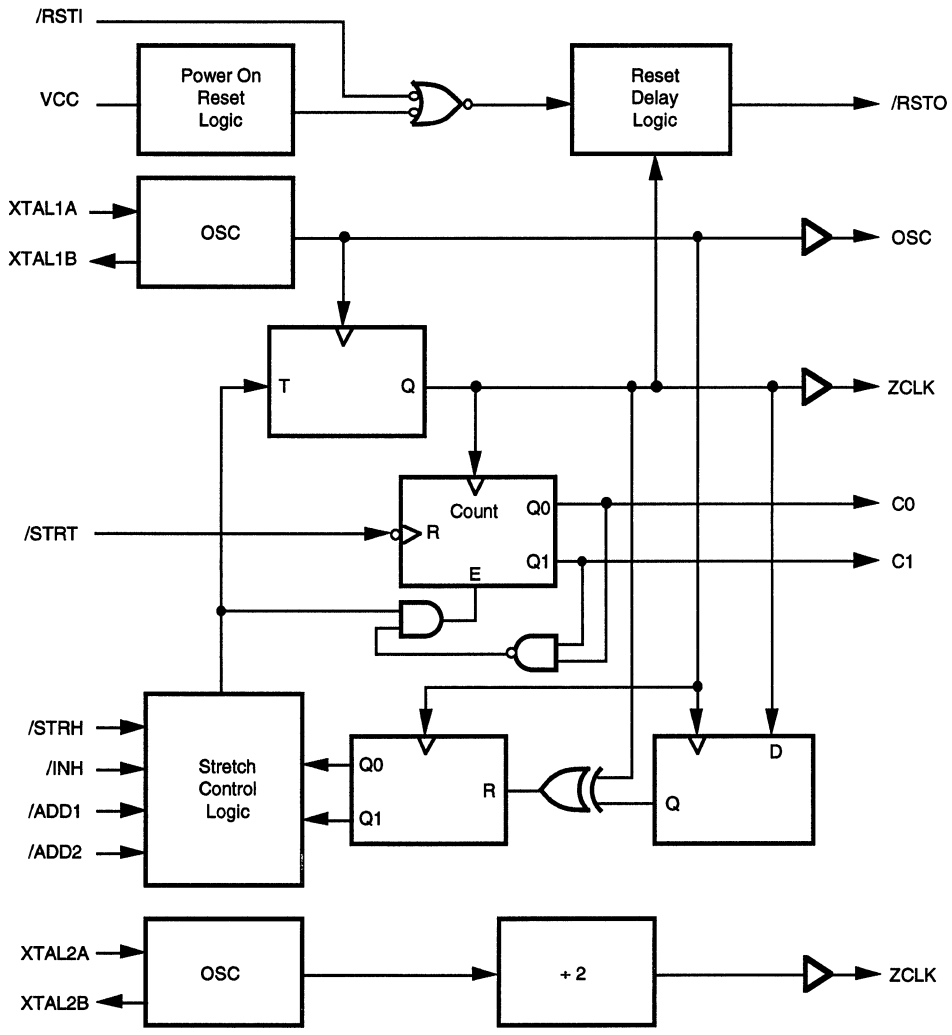
GENERAL DESCRIPTION

The Z8581 Clock Generator and Controller (CGC) is a versatile addition to Zilog's family of universal microprocessor components. The selective clock-stretching capabilities and variety of timing outputs produced by this device allow it to easily meet the timing design requirements of systems with microprocessors and LSI peripherals. The clock output drivers of the Z8581 also meet the non-TTL voltage requirements for driving NMOS clock inputs with no additional external components. The Z8581 provides an elegant, single-chip solution to the design of system clocks for microprocessor-based products.

The Z8581 oscillators are referenced as the system clock oscillator and the general purpose clock oscillator. Both oscillators are driven by external crystals or other frequency sources.

FEATURES

- *Two Independent 20 MHz Oscillators Generate Two 10 MHz Clock Outputs and One 20 MHz Clock Output.*
- *Oscillator Input Frequency Sources can be either Crystals or External Oscillators.*
- *Can be used as a General-Purpose Clock Generator.*
- *Outputs Directly Drive the Z80, Z8000, 8086, 8088, and 68000 Microprocessor Clock Inputs.*
- *18-Pin DIP, Single 5V ±5% Power Supply Required*
- *Provides Ability to Stretch High and/or Low Phase of Clock Signal Under External Control:*
  - *On-Chip 2-Bit Counter can be Used to Selectively Stretch Clock Cycles.*
- *On-Chip Reset Logic:*
  - *Reset Output is Synchronized with System Clock Output.*
  - *Power-Up Reset Period is Maintained for a Minimum of 30 ns.*
  - *External Input Initiates System Reset.*



Z32H00 HYPERSTONE (E1) 32-BIT RISC CPU

GENERAL DESCRIPTION

Z32H00 Hyperstone has a powerful set of instructions of 16, 32 or 48 bits in length. A typical program with the Z32H00 consists mainly of 16-bit instructions. Programs for Z32H00 therefore require less than half of the memory space needed by most RISC processors and are even more compact than the programs of many CISC processors.

As a result of the variable format you can specify 16- and 32-bit constants as well as all addresses as immediate operands: elaborate pre-instructions for the generations of longer constants and addresses are not necessary.

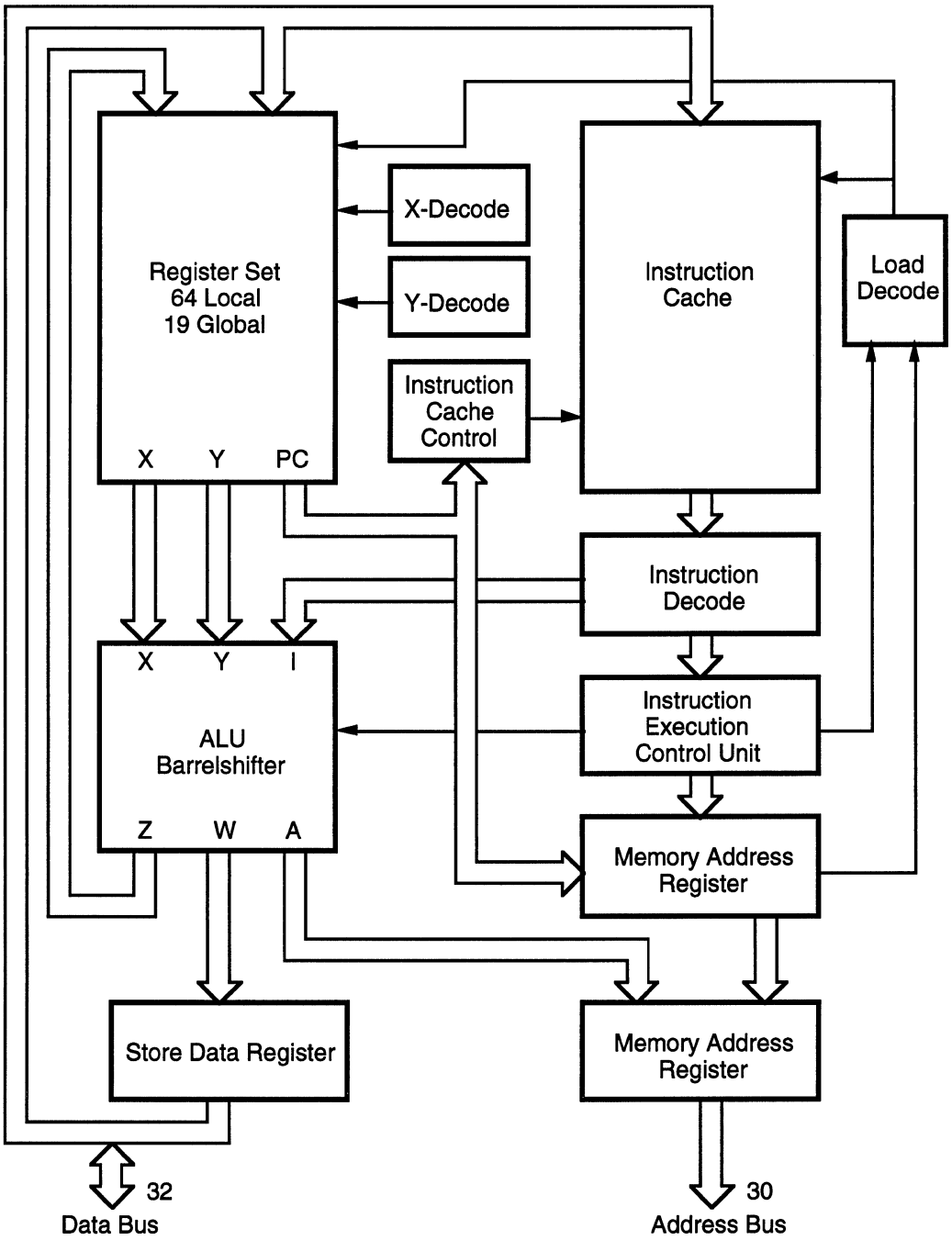
The compact instruction code also reduces the bandwidth required for loading instructions from the memory; more of the total bandwidth is available for data transfer. Most instructions are executed in one cycle: the result is then already available in the next cycle.

The powerful instruction set facilitates programming. It contains multiplication and division as well as double-word instructions. The management of stack frames during subprogram instructions is effected automatically. A variety of address modes are available for memory instructions.

FEATURES

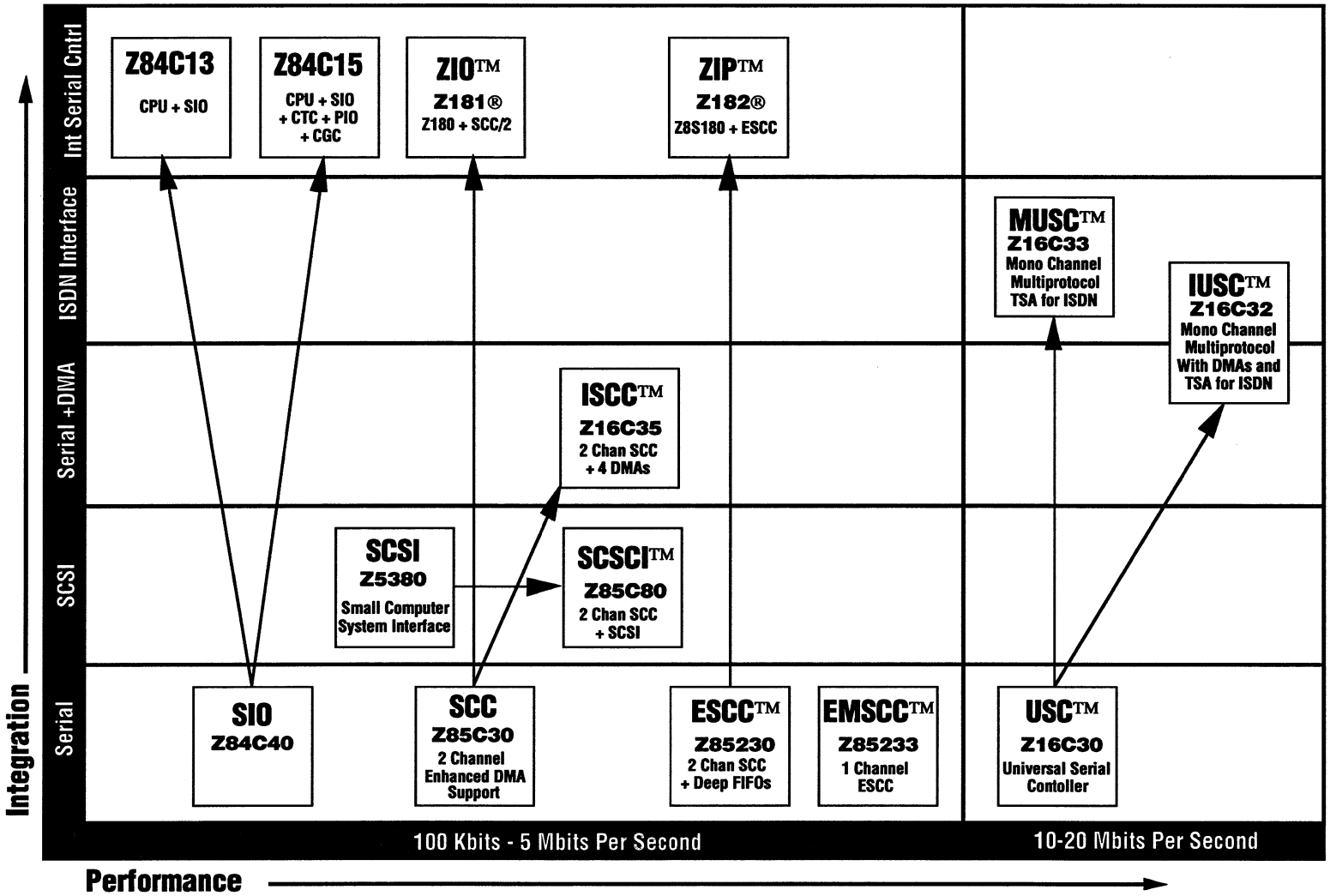
- *Registers*
  - *19 Global and 64 Local Registers of 32 Bits Each*
  - *Directly Addressable are 16 Global and up to 16 Local Registers*
- *Flags*
  - *Zero(Z), Negative(N), Carry(C), and Overflow(V) Flag*
  - *Interrupt-Lock, Trace-Mode, Trace-Pending, Supervisor State, Cache-Mode and High Global Flag*
- *Register Data Types*
  - *Unsigned Integer, Signed Integer, Bitstring. IEEE-754 Floating-Point, Each Either 32 or 64 Bits.*
- *Speeds*
  - *25 MHz Operation with Low-Cost 100 ns DRAMs Operated in Page Mode.*
  - *25 MIPS with Standard DRAMs*
- *Memory*
  - *Address Space of 4 Gbytes*
  - *Separate I/O Address Space*
  - *Load/Store Architecture*
  - *Pipelined Memory and I/O Accesses*
  - *High-Order Data Located at Lower Address*
  - *Virtual Memory by Demand Paging Via a Page Fault Signal from External MMU*
  - *Fault-Causing Memory Instructions can Easily be Identified and Repeated*
  - *Instructions and Double-Word Data May Cross Page Boundaries*
- *Memory Data Types*
  - *Unsigned and Signed Byte (8-Bit)*
  - *Unsigned and Signed Halfword (16-Bit), Located on Halfword Boundary*
  - *Undedicated Word (32-Bit), Located on Word Boundary*
  - *Undedicated Double-Word (64 Bits), Located on Word Boundary*
- *Runtime Stack*
  - *Runtime Stack is Subdivided into Memory Part and Register Part*
  - *Register Part is Implemented by the 64 Local Registers Holding the Most Recent Stack Frame(s)*
  - *Current Stack Frame (Maximum 16 Registers) is Always Kept in Register Part of the Stack*
  - *Data Transfer Between Memory and Register Part of the Stack is Automatic*
  - *Upper Stack Bound is Guarded*
- *Instruction Cache*
  - *An Instruction Cache of 128 Bytes Reduces Instruction Memory Accesses Substantially*
- *Exceptions*
  - *Pointer, Privilege, Frame, and Range Error. Data and Instruction Page Fault, Interrupt and Trace mode exception*
  - *Error- and Fault-Causing Instructions can be Identified by Backtracking, Allowing a Very Detailed Error Analysis*
- *Bus Interface*
  - *Separate Address and Data Bus of 30 and 32 Bit Respectively*
  - *Fast Bus Switching on DMA*
  - *DRAM-Controller with RAS-CAS-Multiplexer, Refresh Logic, Parity Generation and Test and a Programmable Bus-Controller Fully Integrated.*
- *Packaging:*
  - *144-Pin PGA*
  - *120-Pin QFP*

■ *General Instructions*
- *Variable-Length Instructions of 16, 32 or 48 Bits Halve Required Memory Bandwidth*
- *Pipeline Depth of Only Two Stages Assures Immediate Refill After Branches*
- *Register Instructions of type ,,source operator destination →destination" or ,,source operator immediate→destination"*
- *All 32 or 64 Bits Participate in an Operation*
- *Immediate Operands of 5, 16, and 32 Bits, Zero- or Signed-Expanded*
- *Two Sets of Signed Arithmetical Instructions: Instructions Either Set Only the Overflow Flag on Overflow or Trap Additionally to a Range Error Routine.*



DATACOM PRODUCT FAMILY

DATACOM PRODUCTS COMPONENTS SHORTFORM



DATACOM REFERENCE CHART **COMPONENTS SHORTFORM**

Product	Pin Count	COMMERCIAL Plastic DIP	QFP	PGA	Ceramic PLCC	CERDIP	DIP	Speed	Temp	MILITARY Ceramic DIP	Ceramic LCC	Speed	SMD	JAN
Z5380 SCSI	40,44	-	X	X	-	-	-	1.5 MB/sec	S	-	-	-	-	-
Z53C80 SCSI	40,44	-	X	X	-	-	-	3.0 MB/sec	S	-	-	-	-	-
Z8030 SCC	40,44	X	-	-	X	X	-	6,8	S,E,M	X	X	4,6	X	-
Z8530 SCC	40,44	X	-	-	X	X	-	4,6,8	S,E,M	X	X	4,6	X	-
Z80C30 SCC	40,44	X	-	-	X	-	-	8,10	S,E,M	X	X	6,8	-	-
Z85C30 SCC	40,44	X	-	-	X	-	X	8,10,16	S,E,M	X	X	6,8	X	X
Z80230 ESCC	40,44	X	-	-	X	-	-	10,16	S,E	-	-	-	-	-
Z85230 ESCC	40,44	X	-	-	X	-	-	8,10,16,20	S,E,M	X	X	10,16	-	-
Z85233 EMSCC	44	-	X	-	X	-	-	10,16,20	S	-	-	-	-	-
Z85C80 SCSCI	68	-	-	-	X	-	-	10,16	S	-	-	-	-	-
Z16C30 USC	68	-	-	-	X	-	-	10,20	S,E,M	-	PGA	10	-	-
Z16C32 IUSC	68	-	-	-	X	-	-	16,20	S,E	-	-	-	-	-
Z16C33 MUSC	68	-	-	-	X	-	-	10	S,E	-	-	-	-	-
Z16C35 ISCC	68	-	-	-	X	-	-	10,16	S,E	-	-	-	-	-

Temperature Range
S = Standard 0°C to +70°C
E = Extended -40°C to +100°C
M = Military -55°C to +125°C

Part-To-Kit Cross Reference Matrix

	Z8S18000ZCO	Z80181000ZCO	Z80181010ZCO*	Z8523000ZCO	Z16C3001ZCO	Z8018600ZCO	ZEPMDC00001	ZEPMDC00002
Z8030						●		●
Z8530				●		●		●
Z80C30						●		●
Z85C30		●	●	●		●		●
Z80230						●		●
Z85230	●			●		●		●
Z85233				●†		●		●
Z16C30					●	●	●	
Z16C32						●	●	
Z16C33					●	●	●	
Z16C35						●		

* Includes LLAP software that can be licensed.
† Software modifications needed.

SERIAL COMMUNICATIONS CONTROLLERS

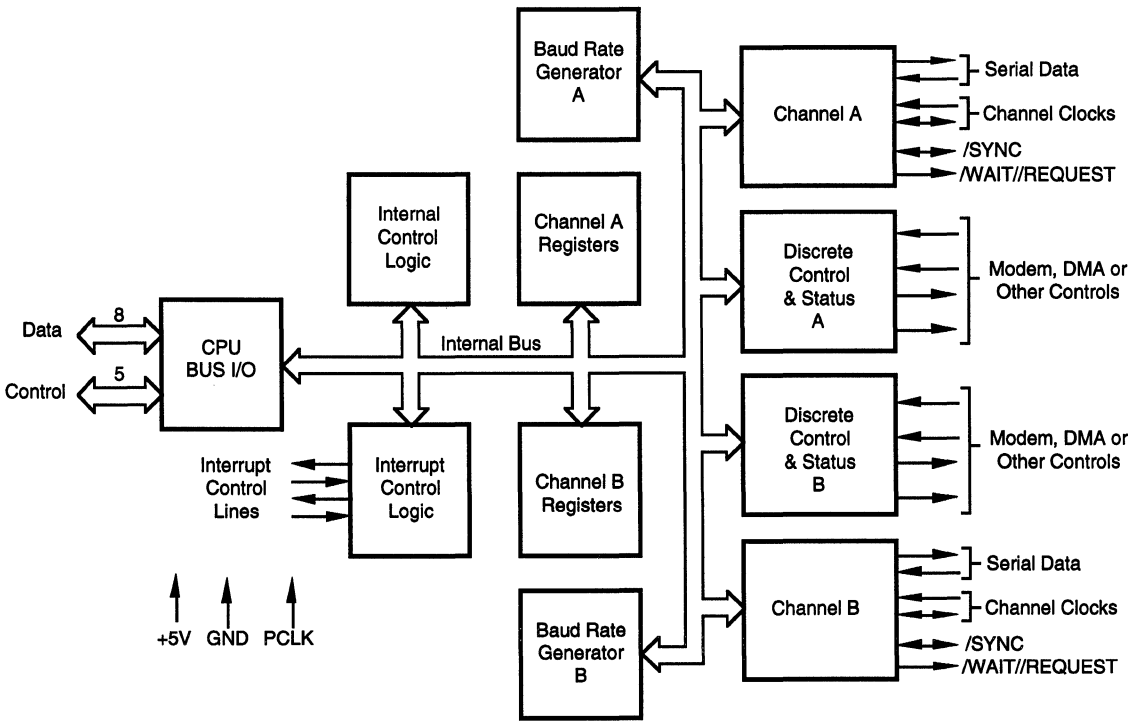
Z8030/Z8530 Z-BUS® SCC/SCC SERIAL COMMUNICATIONS CONTROLLER

GENERAL DESCRIPTION

The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with conventional non-multiplexed buses and the Zilog Z-Bus®. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators that dramatically reduce the need for external logic.

FEATURES

- *Two Independent, 0 to 2M Bit/Second, Full Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop for Clock Recovery.*
- *Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.*
- *Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.*
- *Supports T1 Digital Trunk.*
- *Clock Speeds: 4, 6 and 8 MHz.*
- *Local Loopback and Auto Echo Modes.*
- *Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1s or 0s.*
- *SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.*
- *Available in 40-Pin PDIP and 44-Pin PLCC Package Types.*



GENERAL DESCRIPTION

The Z80C30/Z85C30 CMOS SCC Serial Communications Controller is a CMOS version of the industry standard NMOS SCC. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPUs with either multiplexed or non-multiplexed address/data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allows the SCC to be configured to satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase-locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10x19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.).

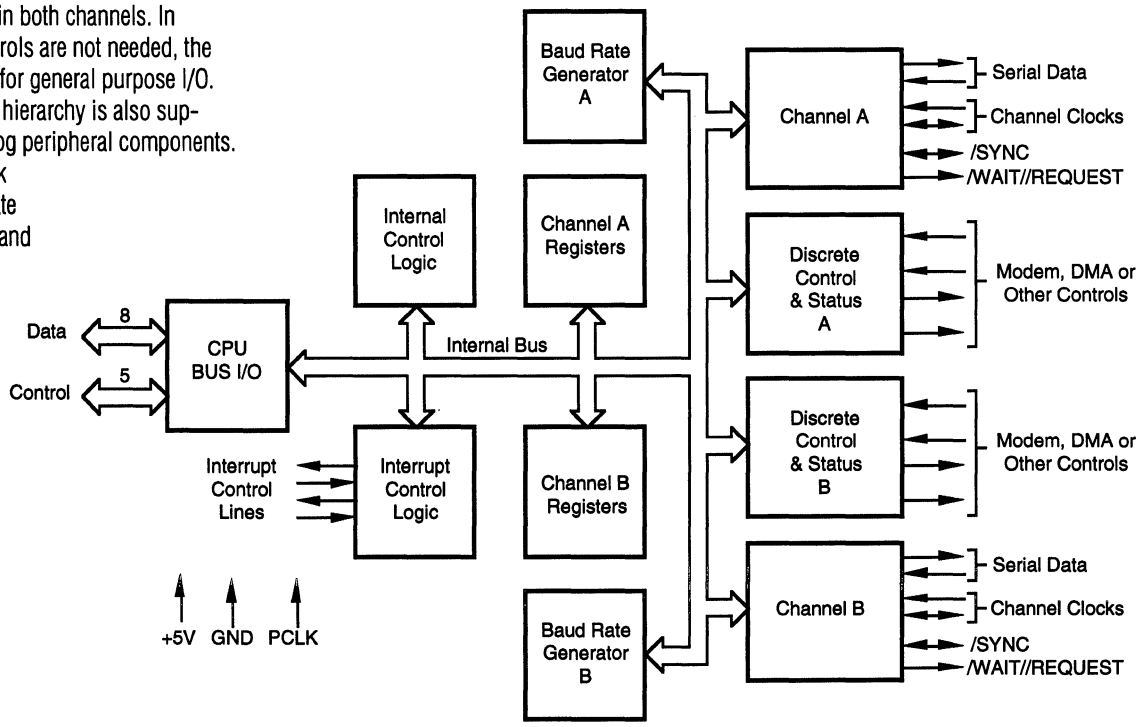
The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general purpose I/O.

The daisy-chain interrupt hierarchy is also supported and is standard for Zilog peripheral components.

The SCC provides a Block Transfer mode to accommodate CPU block transfer functions and DMA controllers.

FEATURES

- *Low Power CMOS*
- *Pin Compatible to NMOS Version*
- *Two Independent, 0 to 4.0 Mbit/sec, Full-Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop for Clock Recovery.*
- *Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.*
- *Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.*
- *Supports T1 Digital Trunk*
- *Clock Speeds: 8, 10 and 16 MHz*
- *Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1s or 0s.*
- *SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, SDLC Loop Mode Operation.*
- *Local Loopback and Auto Echo Modes*
- *Enhanced DMA Support:*
  - *10 x 19-Bit Status FIFO*
  - *14-Bit Byte Counter*
- *Available in 40-Pin PDIP and 44-Pin PLCC Packages.*



Z80230/85230 CMOS ESCC™ ENHANCED SERIAL COMMUNICATIONS CONTROLLER

GENERAL DESCRIPTION

The Zilog Enhanced Serial Communications Controller Z85230 (ESCC), is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. The ESCC is a dual-channel, full-duplex data communications controller capable of supporting a wide range of popular protocols. The ESCC is built from Zilog's industry standard SCC core and is compatible with designs using Zilog's SCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitters and receivers.

The ESCC also has many features that improve packet handling in SDLC mode. The ESCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin high at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO.

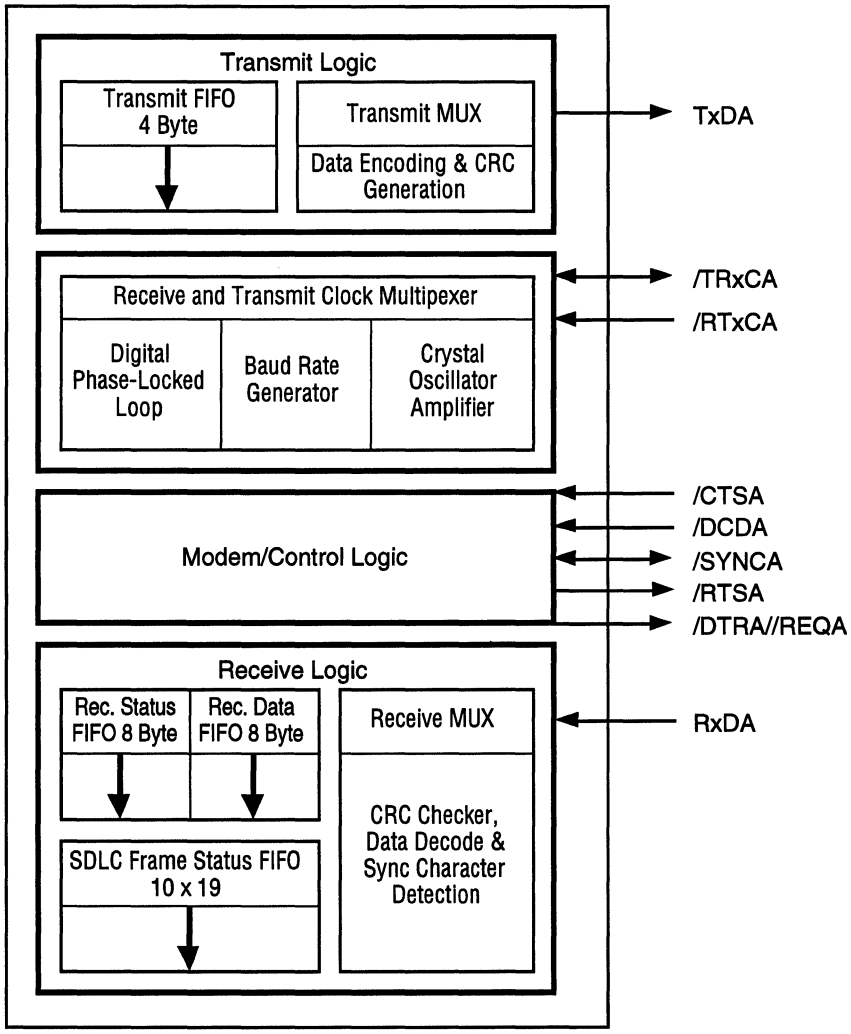
The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the ESCC is improved over the SCC with faster response of the /INT and /DTR//REQ pins.

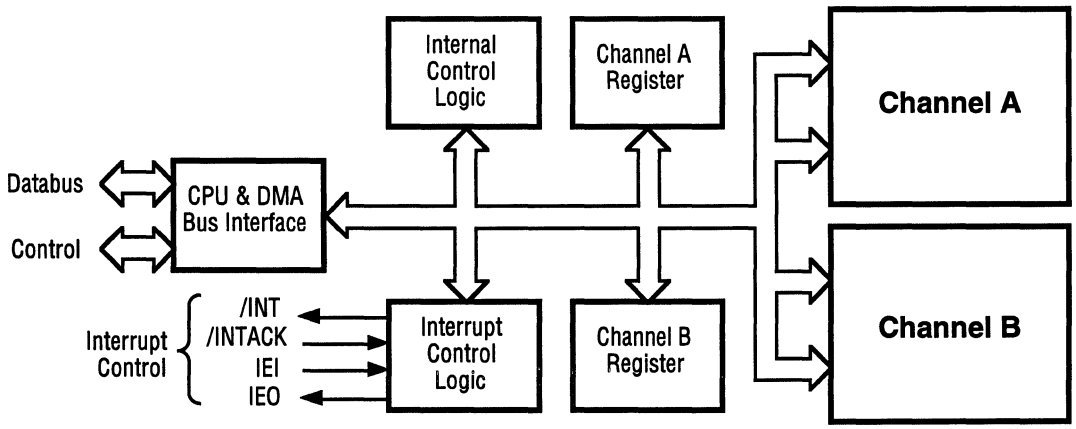
The many enhancements added to the ESCC permits a system design that increases overall system performance with better data handling and less interface logic.

FEATURES

- *Deeper Data FIFOs*
  - *4-Byte Transmit FIFO*
  - *8-Byte Receive FIFO*
- *Programmable Interrupt and DMA Request Levels*
- *Pin and Function Compatible to CMOS and NMOS Z85C30 SCC*
- *Available in 40-Pin PDIP and 44-Pin PLCC Packages*
- *Many Improvements to Support SDLC/HDLC Transfers:*
  - *Deactivation of /RTS Pin After Closing Flag*
  - *Automatic Transmission of the Opening Flag*
  - *Automatic Reset of Tx Underrun/ EOM Latch*
  - *Complete CRC Reception*
  - *TxD Pin Automatically Forced High with NRZI Encoding When Using Mark Idle.*
  - *Receive FIFO Automatically Unlocked for Special Receive Interrupts When Using the SDLC Status FIFO.*
- *Easier Interface to Popular CPUs*
- *Fast Speeds:*
  - *8.5 MHz for Data Rates Up to 2.1 Mbit/sec*
  - *10.0 MHz for Data Rates Up to 2.5 Mbit/sec*
  - *16.384 MHz for Data Rates Up to 4.096 Mbit/sec*
  - *20.0 MHz for Data Rates Up to 5.0 Mbit/sec*
- *Improved SDLC Frame Status FIFO*
- *Read Register 0 Latched During Access*
- *Low Power CMOS*
- *New Programmable Features Added with Write Register 7'*
- *Write Registers: WR3, WR4, WR5, and WR10 are now Readable*
- *Software Interrupt Acknowledge Mode*
- *DPLL Counter Output Available as Jitter-Free Clock Source*
- */DTR//REQ Pin Deactivation Time Reduced*
- *Two Independent Full-Duplex Channels, each with a Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop.*
- *Multi-Protocol Operation Under Program Control*
- *Asynchronous Mode with Five to Eight Bits, and One, One and One-Half, or Two Stop Bits Per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.*
- *Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters. CRC Generation and Checking with Programmable CRC Preset Values.*
- *Available in 40-Pin DIP and 44-Pin PLCC Package types.*

Channel A
Exploded View





Z85233 EMSCC™ ENHANCED MONO SERIAL COMMUNICATION CONTROLLER

GENERAL DESCRIPTION

The Zilog Enhanced Mono Serial Communication Controller, Z85233 EMSCC, is a software compatible CMOS member of the SCC family introduced by Zilog in 1981. The EMSCC is a full-duplex datacommunications controller capable of supporting a wide range of popular protocols. The Z85233 EMSCC is a single channel version (Channel A) of Zilog's Z85230 ESCC. Based on Zilog's unique Superintegration™ Technology, the EMSCC is compatible with designs using Zilog's SCC and ESCC to receive and transmit data. It has many improvements that significantly reduce CPU overhead. The addition of a 4-byte transmit FIFO and an 8-byte receive FIFO significantly reduces the overhead required to provide data to, and get data from, the transmitter and receiver.

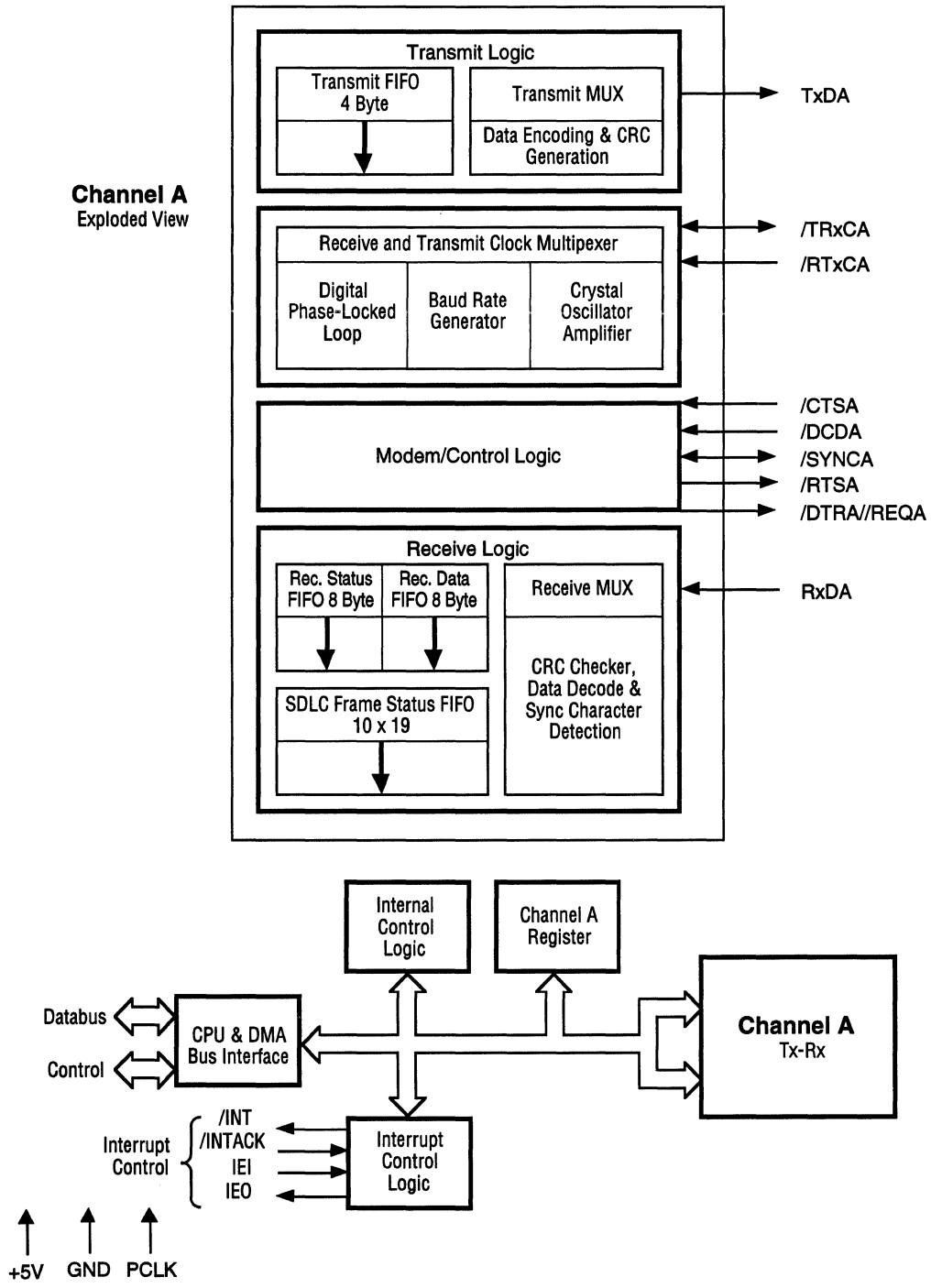
The EMSCC also has many features that improve packet handling in SDLC mode. The EMSCC will automatically: transmit a flag before the data, reset the Tx Underrun/EOM latch, force the TxD pin High at the appropriate time when using NRZI encoding, deassert the /RTS pin after the closing flag, and better handle ABORTed frames when using the 10x19 status FIFO. The combination of these features along with the deeper data FIFOs significantly simplifies SDLC driver software.

The CPU hardware interface has been simplified by relieving the databus setup time requirement and supporting the software generation of the interrupt acknowledge signal (/INTACK). These changes allow an interface with less external logic to many microprocessor families while maintaining compatibility with existing designs. I/O handling of the EMSCC is improved over the SCC with faster response of the /DTR//REQ pin.

The many enhancements added to the EMSCC permits a system design that increases overall system performance with better data handling and less interface logic.

FEATURES

- *Hardware and software compatible with Zilog's SCC/ESCC™*
- *Deeper Data FIFOs*
  - *4-Byte Transmit FIFO*
  - *8-Byte Receive FIFO*
- *Programmable FIFO Interrupt Levels Provide Flexible Interrupt Response*
- *Many Improvements to Support SDLC/HDLC Transfers:*
  - *Deactivation of /RTS Pin after Closing Flag*
  - *Automatic Transmission of the Opening Flag*
  - *Automatic Reset of Tx Underrun/EOM Latch*
  - *Complete CRC Reception*
  - *TxD pin Automatically Forced High with NRZI Encoding when Using Mark Idle.*
  - *Receive FIFO Automatically Unlocked for Special Receive Interrupts when Using the SDLC Status FIFO.*
  - *Back-to-Back Frame Transmission Simplified*
- *Easier Interface to Popular CPUs*
- *Fast Speeds:*
  - *10.0 MHz for Data Rates up to 2.5 Mbit/Sec.*
  - *16.384 MHz for Data Rates up to 4.096 Mbit/Sec.*
  - *20.0 MHz for Data Rates up to 5.0 Mbit/Sec.*
- *Improved SDLC Frame Status FIFO*
- *Low Power CMOS*
- *New Programmable Features Added with Write Register 7'*
- *Write registers: WR3, WR4, WR5, and WR10 are Now Readable*
- *Read Register 0 Latched During Access*
- *Software Interrupt Acknowledge Mode*
- *DPLL Counter Output Available as Jitter-Free Clock Source*
- */DTR//REQ Pin Deactivation Time Reduced*
- *A Full-Duplex Channel with a Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop.*
- *Multi-Protocol Operation Under Program Control*
- *Asynchronous Mode/Synchronous Mode*


Channel A
Exploded View
Transmit Logic
Transmit FIFO
4 Byte
Transmit MUX
Data Encoding & CRC
Generation
TxDA
Receive and Transmit Clock Multipexer
Digital
Phase-Locked
Loop
Baud Rate
Generator
Crystal
Oscillator
Amplifier
/TRxCA
/RTxCA
Modem/Control Logic
/CTSA
/DCDA
/SYNCA
/RTSA
/DTRA//REQA
Receive Logic
Rec. Status
FIFO 8 Byte
Rec. Data
FIFO 8 Byte
Receive MUX
RxDA
SDLC Frame Status FIFO
10 x 19
CRC Checker,
Data Decode &
Sync Character
Detection
Internal
Control
Logic
Channel A
Register
Databus
Control
CPU & DMA
Bus Interface
Channel A
Tx-Rx
Interrupt
Control
/INT
/INTACK
IEI
IEO
Interrupt
Control
Logic
+5V
GND
PCLK

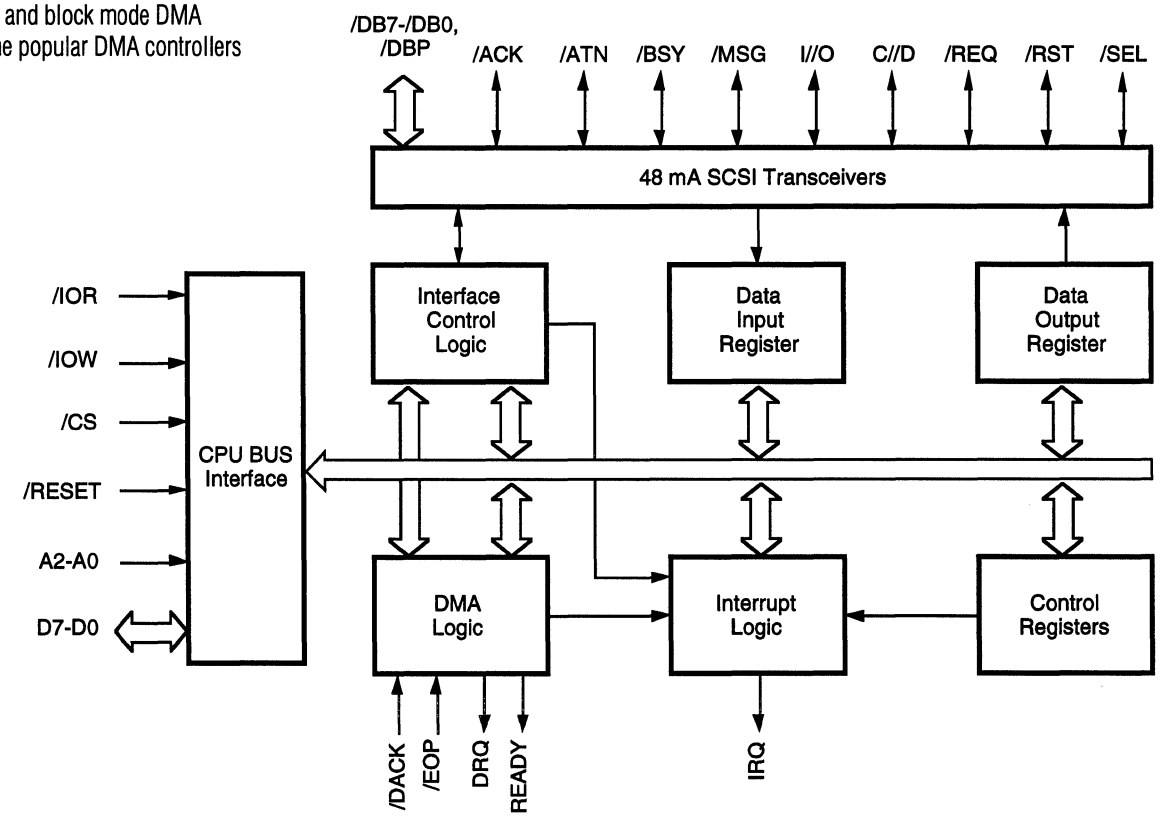
Z5380 SCSI™ SMALL COMPUTER SYSTEM INTERFACE CONTROLLER

GENERAL DESCRIPTION

Zilog's Z5380 SCSI (Small Computer System Interface) controller, is a 40-pin DIP or 44-pin PLCC CMOS device. It was designed to implement the SCSI protocol as defined by the ANSI X3T9.2 Committee, and is a plug-in replacement of the industry standard; the NMOS 5380. The Z5380 is capable of operating both as a Target and an Initiator. This enables the Z5380 to find its use in Bus Host Adapters, Formatters, and Host Port designs. Special high-current open-drain outputs enable it to directly interface to, and drive, the SCSI bus. These drivers are capable of sinking 48 mA at 0.5V. The Z5380 has the necessary interface hook-ups so the system CPU can communicate with it, like with any other peripheral device. The CPU can read from, or write to the SCSI registers which may be addressed as standard or memory-mapped I/O's. The Z5380 increases system performance by minimizing the CPU intervention in DMA operations which the Z5380 controls. The CPU is interrupted by the Z5380 when it detects a bus condition that requires attention. It also supports arbitration and reselection. The Z5380 has the proper handshake signals to support normal and block mode DMA operations with most of the popular DMA controllers available.

FEATURES

- *Compatible 5380 pin-out*
- *CMOS - Typical I_{cc} 2.5 mA*
- *Asynchronous Interface, supports 1.5M bytes/sec*
- *Direct SCSI Bus Interface with On-Board 48 mA*
- *Supports Target and Initiator Roles*
- *Arbitration Support*
- *DMA or Programmed I/O Data Transfers*
- *Supports Normal or Block Mode DMA*
- *Memory or I/O Mapped CPU Interface*



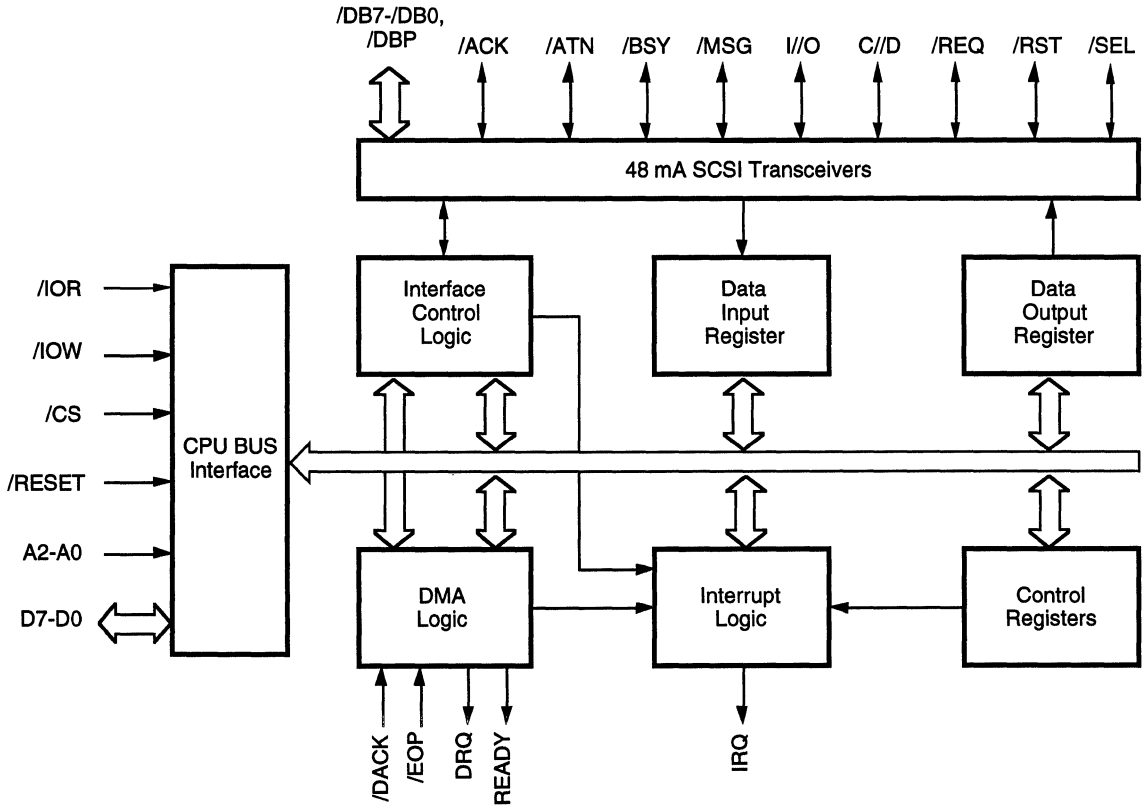
GENERAL DESCRIPTION

The Z53C80 SCSI (Small Computer System Interface)) controller is a 44-pin PLCC, or 48-pin DIP CMOS device. It is designed to implement the SCSI protocol as defined by the ANSI X3. 131-1986 standard, and is fully compatible with the industry standard 53C80. It is capable of operating both as a Target and as an Initiator. Special high-current open-drain outputs enable it to directly interface to the SCSI bus. The Z53C80 has the necessary interface hookups so the system CPU can communicate with it like with any other peripheral device. The CPU can read from, or write to, the SCSI registers which are addressed as standard or memory-mapped I/Os.

The Z53C80 increases the system performance by minimizing the CPU intervention in DMA operations which the SCSI controls. The CPU is interrupted by the SCSI when it detects a bus condition that requires attention. It also supports arbitration and reselection. The Z53C80 has the proper hand-shake signals to support normal and block mode DMA operations with most DMA controllers available.

FEATURES

- *Compatible 53C80 pin-out*
- *Low power CMOS*
- *Asynchronous Interface, supports 3.0M bytes/sec*
- *Direct SCSI Bus Interface with On-Board 48 mA drivers*
- *Supports Target and Initiator Roles*
- *Arbitration Support*
- *DMA or Programmed I/O Data Transfers*
- *Supports Normal or Block Mode DMA*
- *Memory or I/O Mapped CPU Interface*



Z85C80 CMOS SCSCI™ SERIAL COMMUNICATION AND SMALL COMPUTER INTERFACE

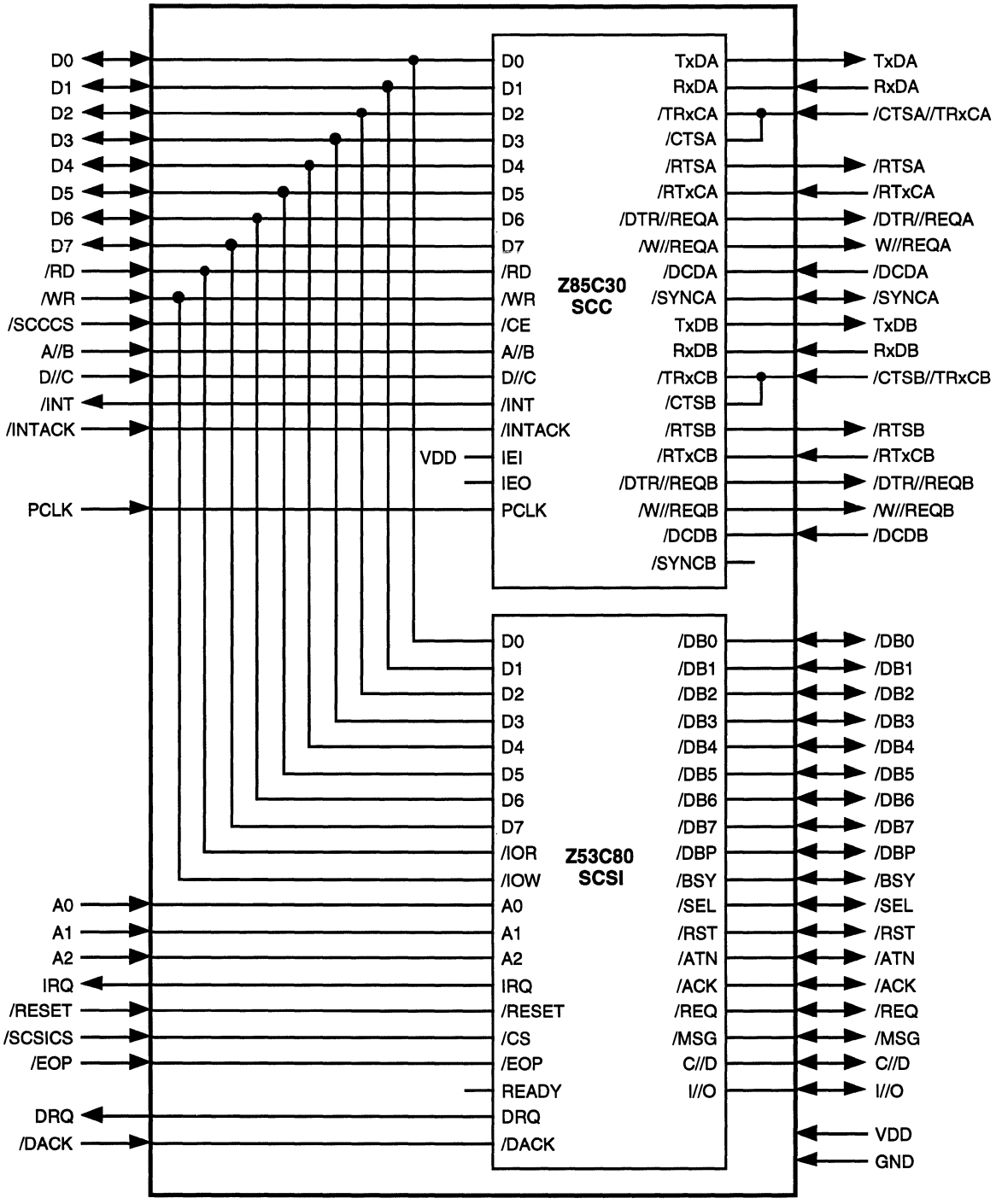
GENERAL DESCRIPTION

The Z85C80 CMOS SCSCI is an industry standard 85C30 dual channel Serial Communication Controller (SCC) and an industry standard 53C80 Small Computer System Interface (SCSI) integrated into one monolithic Integrated Circuit. The internal SCC and SCSI share the 8-bit data bus (D7 through D0) and read and write inputs (/RD and /WR).

The Z85C80 is offered in a 68-pin PLCC package. With a few exceptions, all of the internal SCC and SCSI signals are connected to the outside pins.

FEATURES

- *Low Power CMOS*
- *Two Independent, 0 to 2.5 Mbit/sec, Full-Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop for Clock Recovery.*
- *Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.*
- *Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character, Programmable Clock Factor, Break Detection and Generation; Parity, Overrun, and Framing Error Detection.*
- *Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1s or 0s.*
- *SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.*
- *Local Loopback and Auto Echo Modes*
- *Supports T1 Digital Trunk.*
- *Enhanced DMA Support:*
  - *10 X 19-Bit Status FIFO*
  - *14-Bit Byte Counter*
- *Supports SCSI ANSI-X3.131-1986 Standard.*
- *Arbitration Support*
- *DMA or Programmed I/O Data Transfers*
- *Supports Normal DMA*
- *Memory or I/O Mapped CPU Interface*
- *Asynchronous Interface Supports 3 Mbytes/sec*
- *Direct SCSI Bus Interface with On-Board 48 mA Drivers*
- *Supports Target and Initiator Roles*
- *Available in 68-pin PLCC, 10 MHz and 16 MHz*


D0
D1
D2
D3
D4
D5
D6
D7
/RD
/WR
/SCCCS
A//B
D//C
/INT
/INTACK
PCLK
Z85C30
SCC
/CE
IEI
IEO
TxDA
RxDA
/TRxCA
/CTSA
/RTSA
/RTxCA
/DTR//REQA
/W//REQA
/DCDA
/SYNCA
TxDB
RxDB
/TRxCB
/CTSB
/RTSB
/RTxCB
/DTR//REQB
/W//REQB
/DCDB
/SYNCB
/CTSA//TRxCA
/CTSB//TRxCB
Z53C80
SCSI
/IOR
/IOW
/DB0
/DB1
/DB2
/DB3
/DB4
/DB5
/DB6
/DB7
/DBP
/BSY
/SEL
/RST
/ATN
/ACK
/REQ
/MSG
C//D
I//O
A0
A1
A2
IRQ
/RESET
/SCSICS
/EOP
READY
DRQ
/DACK
/CS
VDD
GND

Z16C30 CMOS USC™ UNIVERSAL SERIAL CONTROLLER

GENERAL DESCRIPTION

The USC Universal Serial Controller is a dual-channel multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The USC functions as a serial-to-parallel, parallel-to-serial converter/controller and may be software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including two baud rate generators per channel, a digital phase-locked loop per channel, character counters for both receive and transmit in each channel, and 32-byte data FIFOs for each receiver and transmitter.

The USC handles asynchronous formats, synchronous byte-oriented formats such as BISYNC, and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O. The same is true for most of the other pins in each channel.

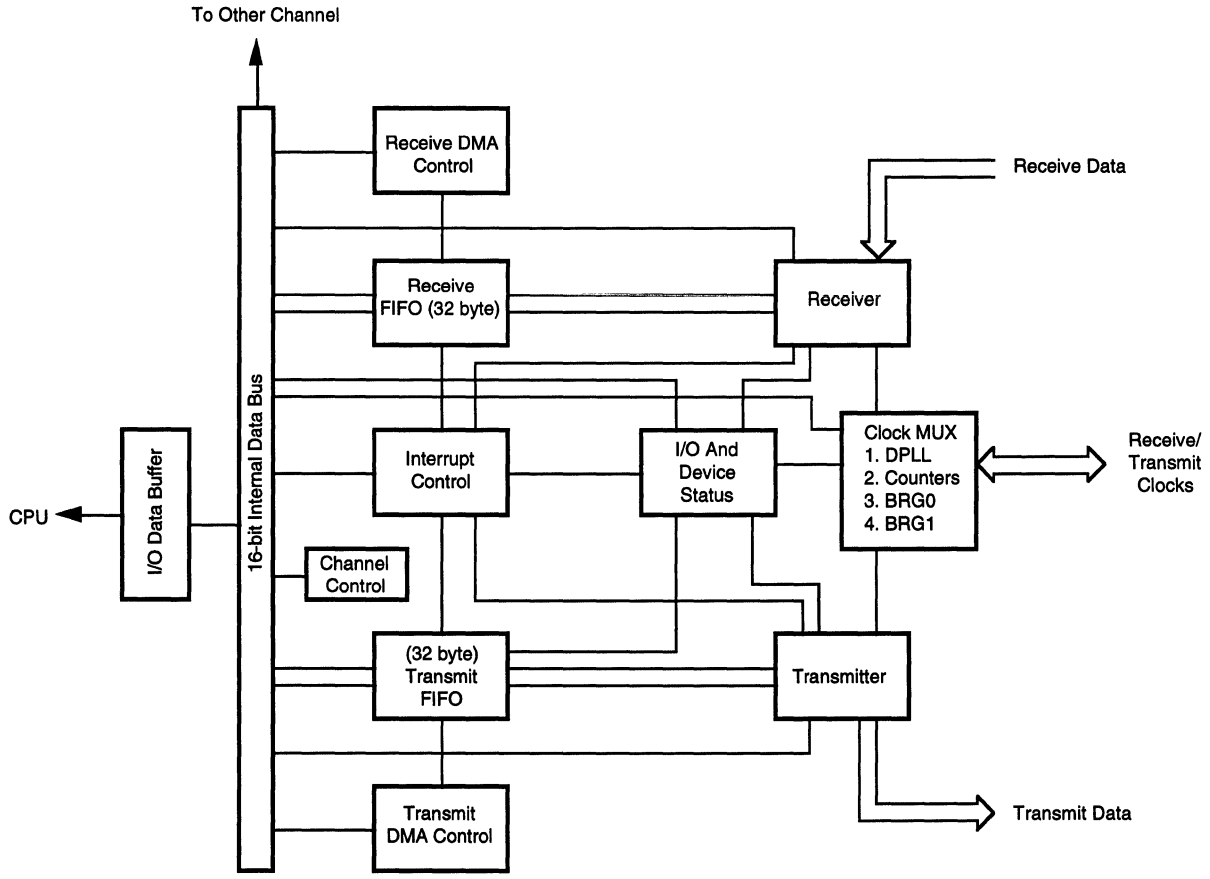
Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers via DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer via DMA and allows device initialization under DMA control.

To aid the designer in efficiently programming the USC, additional literature is available. The Technical Manual describes in detail all features presented in this product specification and gives programming sequence hints. The Electronic Programmer's Manual is an MS-DOS disk based programming initialization tool to be used in conjunction with the Technical Manual. There are also available assorted application notes and development boards to assist the designer in the hardware/software development.

FEATURES

- *Two Independent, 0 to 10 Mbit/sec, Full Duplex Channels, Each with Two Baud Rate Generators and One Digital Phase-Locked Loop for Clock Recovery.*
- *32-Byte Data FIFOs for Each Receiver and Transmitter*
- *12.5 Mbyte/sec (16-Bit) Data Bus Bandwidth*
- *Multi-Protocol Operation Under Program Control with Independent Mode Selection for Receiver and Transmitter.*
- *Async Mode with One to Eight Bits/Character, 1/16 to 2 Stop Bits/Character in 1/16 Bit Increments; Programmable Clock Factor; Break Detect and Generation; Odd, Even, Mark, Space or no Parity and Framing Error Detection. Supports One Address/Data Bit and MIL STD 1553B Protocols.*
- *Byte Oriented Synchronous Mode with One to Eight Bits/Character; Programmable Idle Line Condition; Optional Receive Sync Stripping; Optional Preamble Transmission; 16- or 32-Bit CRC and Transmit-to-Receive Slaving (for X.21).*
- *Low Power CMOS*
- *68-Pin PLCC Package*
- *Bisync Mode with 2- to 16-Bit Programmable Sync Character; Programmable Idle Line Condition; Optional Receive Sync Stripping; Optional Preamble Transmission; 16- or 32-Bit CRC.*
- *Transparent Bisync Mode with EBCDIC or ASCII Character Code; Automatic CRC Handling; Programmable Idle Line Condition; Optional Preamble Transmission; Automatic Recognition of DLE, SYN, SOH, ITX, ETX, ETB, EOT, ENQ and ITB.*
- *External Character Sync Mode for Receive*
- *HDLC/SDLC Mode with 8-Bit Address Compare; Extended Address Field Option; 16- or 32-Bit CRC; Programmable Idle Line Condition; Optional Preamble Transmission and Loop Mode.*
- *DMA Interface with Separate Request and Acknowledge for each Receiver and Transmitter.*
- *Flexible Bus Interface for Direct Connection to most Microprocessors; user Programmable for 8- or 16-Bits Wide. Directly Supports 680X0 Family or 8X86 Family Bus Interfaces.*
- *Channel Load Command for DMA Controlled Initialization*


To Other Channel
Receive DMA Control
Receive Data
Receive FIFO (32 byte)
Receiver
16-bit Internal Data Bus
Clock MUX
1. DPLL
2. Counters
3. BRG0
4. BRG1
Receive/ Transmit Clocks
Interrupt Control
I/O And Device Status
CPU
I/O Data Buffer
Channel Control
(32 byte) Transmit FIFO
Transmitter
Transmit DMA Control
Transmit Data

Z16C32 CMOS IUSC™ INTEGRATED UNIVERSAL SERIAL CONTROLLER

GENERAL DESCRIPTION

The IUSC (Integrated Universal Serial Controller) is a single-channel multiple protocol data communications device with on-chip dual-channel DMA. The integration of a high speed serial communications channel with a high performance DMA facilitates higher data throughput than is possible with discrete serial/DMA chip combinations. The buffer chaining capabilities combined with features like character counters, frame status block and buffer termination at the end of the frame facilitate sophisticated buffer management that can significantly reduce CPU overhead.

The IUSC is software configurable to satisfy a wide variety of serial communications applications. The 10Mbit per second data rate and multiple protocol support make it ideal for applications in todays dynamic environment of changing specifications and ever increasing speed. The many programmable features allow the user to tune the device response to meet system requirements and adapt to future changes with software instead of redesigning hardware.

The on-chip DMA channels allow high-speed data transfers for both the receiver and the transmitter. The device supports automatic status transfer via DMA and allows device initialization under DMA control. Each DMA channel can transfer data words in as little as three 50 ns clock cycles and can generate addresses compatible with 32-, 24- or 16-bit memory ranges. The DMA channels may operate in any of four modes: single buffer, pipelined, array-chained, or linked-list. The array-chained and linked-list modes reduce the problems with segmentation and re-assembly of messages in systems. To prevent the DMA from holding bus mastership too long, mastership time may be limited by counting the absolute number of clock cycles, the number of bus transactions, or both.

The CPU bus interface is designed for use with any conventional multiplexed or non-multiplexed bus. The device contains a variety of sophisticated internal functions including two baud rate generators, a digital phase-locked loop, character counters, and 32-byte FIFOs for both the receiver and transmitter.

The IUSC handles asynchronous formats, synchronous byte-oriented formats (e.g., BISYNC), and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The IUSC can generate, and check CRC in any synchronous mode and is programmed to check data integrity in various modes. Access to the CRC value allows system software to resend or manipulate it as needed in various applications. The IUSC also has facilities for modem controls. In applications where these controls are not needed, the modem controls can be used for general purpose I/O.

Interrupts are supported by a daisy-chain hierarchy within the serial channel and between the serial channel and the DMA.

FEATURES

- *0 to 20 Mb/s, Full-Duplex Channel, with Two Baud Rate Generators and a Digital Phase-Locked Loop for Clock Recovery.*
- *Dual 20 MHz 32-Bit On-Board DMA Controllers*
- *Four Modes of DMA Operations:*
  - *Single Buffered*
  - *Pipelined*
  - *Array-chained*
  - *Linked List*
- *32-Byte Data FIFOs for Receive and Transmit*
- *18 Mbyte/s (16-Bit) Data Bus Bandwidth*
- *8-Bit General-Purpose Port with Transmission Detection*
- *ISDN Time Slot Assigner*
- *Multi-Protocol Operation Under Program Control with Independent Mode Selection for Receiver and Transmitter.*
- *Async Mode with One to Eight Bits/Character, 1/16 to 2 Stop Bits/Character in 1/16 Bit Increments; Programmable Clock Factor; Break Detect and Generation; Odd, Even, Mark, Space or no Parity and Framing Error Detection.*
- *HDLC/SDLC Mode with 8-Bit Address Compare; Extended Address Field Option; 16- or 32-Bit CRC; Programmable Idle Line Condition; Optional Preamble Transmission and Loop Mode.*
- *Byte Oriented Synchronous Mode with One to Eight Bits/Character; Programmable Idle Line Condition; Optional Receive Sync Stripping; Optional Preamble Transmission; 16- or 32-Bit CRC and Transmit-to-Receive Slaving (for X.21).*
- *Bisync Mode with 2- to 16-Bit Programmable Sync Character; Programmable Idle Line Condition; Optional Receive Sync Stripping; Optional Preamble Transmission; 16- or 32-Bit CRC.*
- *External Character Sync Mode for Receive*
- *Transparent Bisync Mode with EBCDIC or ASCII Character Code; Automatic CRC Handling; Programmable Idle Line Condition; Optional Preamble Transmission; Automatic Recognition of DLE, SYN, SOH, ITX, ETX, ETB, EOT, ENQ, and ITB.*
- *Flexible Transmit and Receive Clock Control is Supported with Multiple Clock Inputs, 2 Baud Rate Generators, 2 Counters, and a DPLL. All of these Options are Independent of the DMA Clock.*
- *Encodes and Decodes NRZ, NRZI, NRZB, NRZI-Mark, NRZI-Space, Biphase-Mark (FM1), Biphase-Space (FM0), Biphase-Level (Manchester), and Differential Biphase-Level Data Formats.*
- *DMA Interface with Separate Request and Acknowledge for the Receiver and Transmitter.*
- *Channel Load Command for DMA Controlled Initialization.*
- *Flexible Bus Interface for Direct Connection to Most Microprocessors; User Programmable for 8 or 16 Bits wide. Directly Supports 680X0 Family or 80X86 Family Bus Interfaces.*
- *Daisy-Chain Hierarchy Interrupts*
- *Low Power CMOS*
- *68-Pin PLCC*

APPLICATIONS

Wide Area Networks

Exceeds the data rate of T1/E1 WAN applications. Many features support the frame format of the HDLC/SDLC protocol to meet the changing requirements of todays networks. This includes supporting the frame format of X.25, LAPB, LAPD and Frame Relay. ISDN D-channel applications are supported with a time slot assigner. The buffer chaining features of the DMA minimize CPU intervention to maximize throughput. Termination of memory buffers on End Of Frame allows data from different frames to be separated in memory.

Local Area Networks

Supports a variety of local area network framing and formatting protocols including LocalTalk™ LLAP, proprietary HDLC/SDLC based protocols, and Ethernet. The 32-byte data FIFOs can be programmed to DMA request at any level allowing the response to meet system latency requirements.

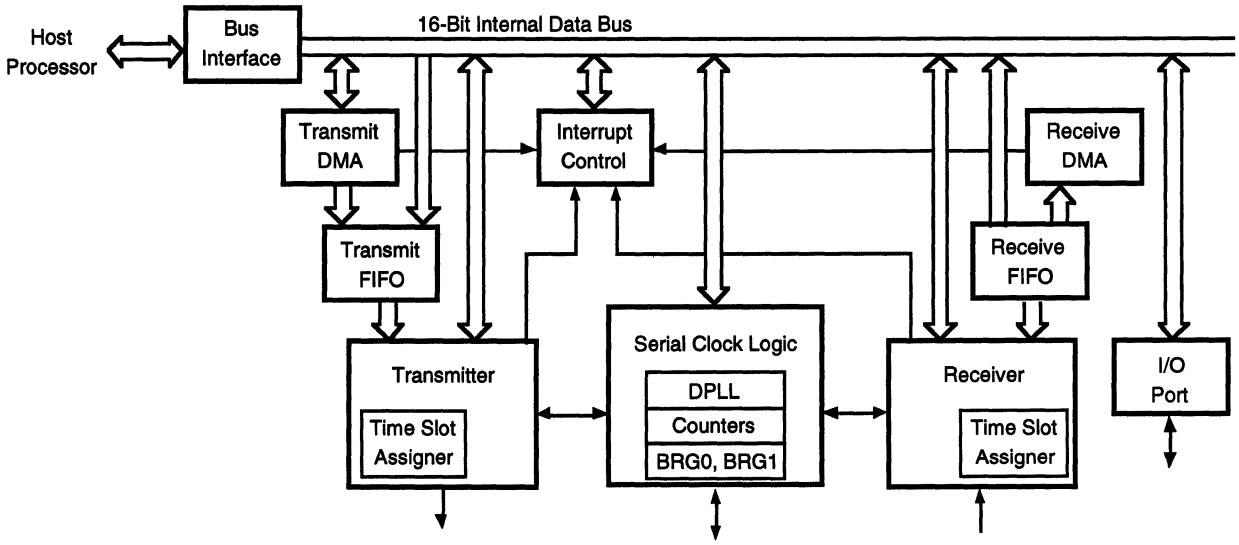
Bridges & Routers

The fast 150 ns per word data transfers and the ability to automatically store frame information in memory allow the IUSC to keep up with high speed networks. Queueing delays are minimized by efficient handling of reading and writing to and from memory in array chained and linked list modes of the DMA. The ability to receive and transmit in different protocols is well suited to bridge applications.

Test Equipment

The IUSC's multiple protocol support with a high degree of flexibility makes it ideal for test equipment and line monitors. This allows the IUSC to be able to adjust to the many variations of protocols in use today.

LocalTalk is a registered trademark of Apple Computer Inc.



Z16C33 CMOS MUSC™ MONO UNIVERSAL SERIAL CONTROLLER

GENERAL DESCRIPTION

The MUSC (Mono Universal Serial Controller) is a single-channel multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The MUSC functions as a serial-to-parallel, parallel-to-serial converter/controller and is software configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including two baud rate generators, a digital phase-locked loop, character counters for both receive and transmit, and 32-byte data FIFOs for both the receiver and transmitter.

The MUSC handles asynchronous formats, synchronous byte-oriented formats (e.g., BISYNC), and synchronous, bit-oriented formats like HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and is programmed to check data integrity in various modes. The MUSC also has facilities for modem controls. In applications where these controls are not needed, the modem controls are used for general-purpose I/O. The same is true for most of the other pins.

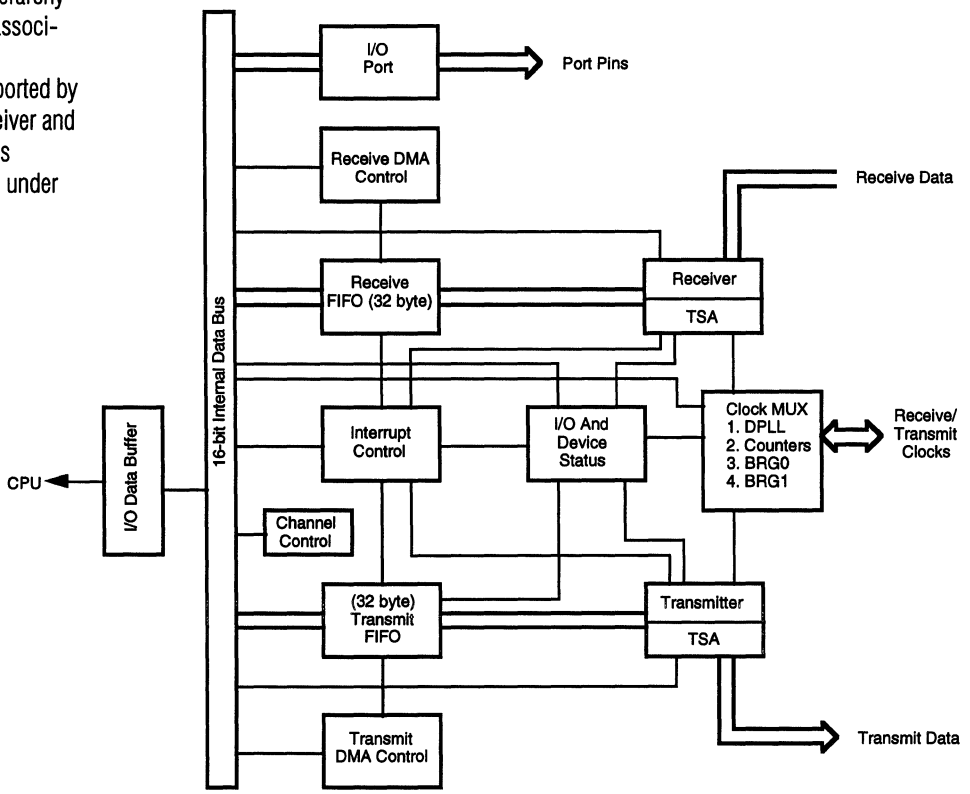
Interrupts are supported by a daisy-chain hierarchy with the serial channel. There are no interrupts associated with the 8-bit port.

High-speed data transfers via DMA are supported by a Request/Acknowledge signal pair for both receiver and transmitter. The device supports automatic status transfer via DMA and allows device initialization under DMA control.

Literature is available to aid the designer in efficiently programming the MUSC. The Technical Manual describes in detail all features presented in this product specification and gives programming sequence hints. Also, there are assorted application notes and development boards to assist the designer in hardware/software development.

FEATURES

- *0 to 10 Mbit/sec, Full-Duplex Channel, with Two Baud Rate Generators and One Digital Phase-Locked Loop for Clock Recovery.*
- *32-Byte Data FIFOs for Receiver and Transmitter*
- *12.5 MByte/sec (16-Bit) Data Bus Bandwidth*
- *ISDN Time Slot Assigner*
- *Multi-Protocol Operation Under Program Control with Independent Mode Selection for Receiver and Transmitter.*
- *Async Mode with One to Eight Bits/Character, 1/16 to 2 Stop Bits/Character in 1/16 Bit Increments; Programmable Clock Factor; Break Detect and Generation; Odd, Even, Mark, Space or no Parity and Framing Error Detection. Supports One Address/Data Bit and MIL STD 1553B Protocols.*
- *Low Power CMOS*
- *External Character Sync Mode for Receive*
- *HDLC/SDLC Mode with Eight Bit Address Compare; Extended Address Field Option; 16- or 32-Bit CRC; Programmable Idle Line Condition; Optional Preamble Transmission and Loop Mode.*
- *DMA Interface with Separate Request and Acknowledge for the Receiver and Transmitter.*
- *Channel Load Command for DMA Controlled Initialization*
- *Flexible Bus Interface for Direct Connection to Most Microprocessors; User Programmable for 8 or 16 Bits Wide. Directly Supports 680X0 Family or 8X86 Family Bus Interfaces.*
- *8-Bit General-Purpose Port with Transition Detection*
- *68-Pin PLCC Package*



GENERAL DESCRIPTION

The Z16C35 ISCC™ is a CMOS Superintegrated device with a flexible Bus Interface Unit (BIU) connecting a built-in Direct Memory Access (DMA) cell to the CMOS Serial Communications Control (SCC) cell.

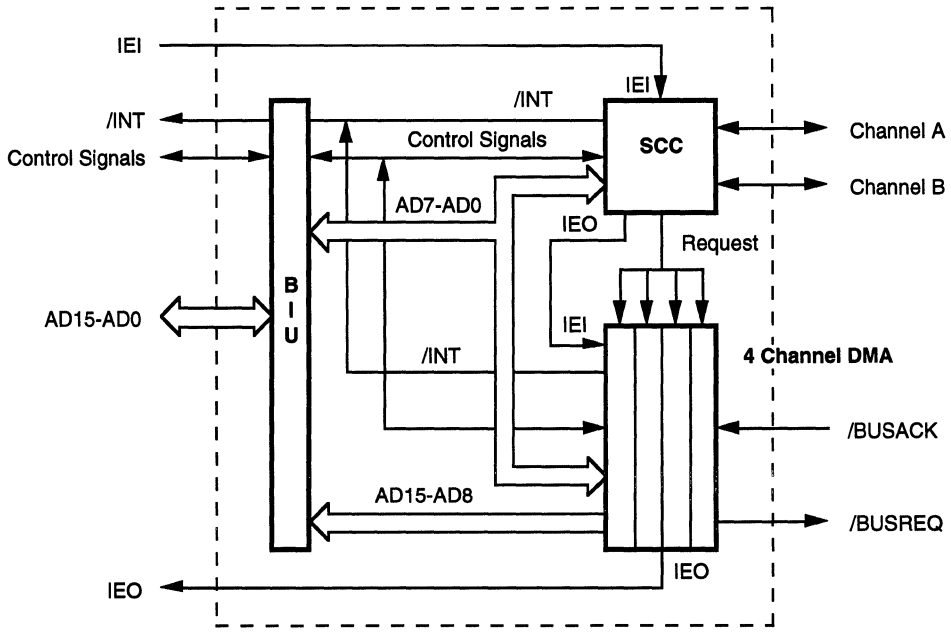
The ISCC is a dual-channel, multi-protocol data communications peripheral which easily interfaces to CPUs with either multiplexed or non-multiplexed address and data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allow the ISCC to be configured for a wide variety of serial communications applications. The many on-chip features such as, streamlined bus interface, four channel DMA, baud rate generators, digital phase-locked loops, and crystal oscillators dramatically reduce the need for external logic.

The ISCC can address up to 4 gigabytes per DMA channel by using the /UAS and /AS signals to strobe out 32-bit multiplexed addresses.

The ISCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC.

FEATURES

- *Low Power CMOS Technology*
- *Two General-Purpose SCC Channels, Four DMA Channels; and Universal Bus Interface Unit.*
- *Software Compatible to the Zilog CMOS SCC*
- *Four DMA Channels; Two Transmit and Two Receive Channels to and from the SCC*
- *Four Gigabyte Address Range per DMA Channel*
- *Fly-by DMA Transfer Mode*
- *Programmable DMA Channel Priorities*
- *Independent DMA Register Set*
- *A Universal Bus Interface Unit Providing Simple Interface to Most CPUs Multiplexed or Non-Multiplexed Bus; Compatible with 680x0 and 8x86 CPUs.*
- *32-Bit Addresses Multiplexed to 16-Pin Address/Data Lines*
- *68-Pin PLCC*
- *Supports all Zilog CMOS SCC Features.*
- *Two Independent, 0 to 4.0 Mbit/sec, Full-Duplex Channels, each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop Circuit for Clock Recovery.*
- *Multi-Protocol Operation Under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.*
- *Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.*
- *Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to Either 1's or 0's.*
- *SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.*
- *Full CMOS SCC Register Set*
- *10 and 16 MHz Speeds Suitable for T1 Full Duplex Operation*



Support Products Summary

Foreword

Zilog recognizes the customer's need to successfully design and develop new systems or applications quickly with maximum reliability and performance. The company has developed new design/architectural support products to enhance the growing portfolio of new products in the datacommunication, intelligent peripheral control and microcontroller markets. The Support Products Summary features the latest component support tools for accomplishing these goals.

New Products

Zilog has continued to introduce many new Superintegration™ CMOS components to fit multiple niche market designs. The company's proven core and cell library, one of the largest in the industry, is used to create Application Specific Standard Products (ASSPs) to meet the needs of specific market designs.

Zilog's support technology also allows customers to automate software design with innovative support tools such as the EPM™ (Electronic Programmer's Manual). The EPM Manual provides a turnkey modular approach to creating device driver software in "C" code. This approach provides an easy, flexible integration of datacommunication products into new system designs.

Choosing the right microprocessor/microcontroller architecture is key to successful product development and development support. Zilog backs its customers with years of experience in engineering assistance, advanced integrated development tools, electronic interactive programs, training, documentation and much more.

Z8® Microcontrollers

The Z8 family of microcontrollers offers optimum system cost/performance in specific markets such as mass storage, automotive, computer peripherals, speech processing and general purpose embedded control. Zilog's expertise has helped customers follow their product designs from inception through to completion. Time to market and maximum cost/performance are just a few of the important areas served by these support tools.

The new ICEBOX™ in-circuit emulation tools provide real-time diagnostic/test emulations and OTP programming support for Zilog's Z8 microcontrollers. The emulator provides all the essential MCU timing and I/O circuitry to simplify user emulation of the prototype hardware/software products.

Z80® Intelligent Peripherals

The Z80 family of intelligent peripheral controllers offers on-board intelligence for faxes, cellular phones, Local Area Network (LAN) network controllers, wireless controllers, printers, terminals, modems and general-purpose embedded control. To support the IPC line, Zilog offers evaluation kits that contain an assembled circuit board with supporting software documentation. These kits assist software and hardware development of customer designs.

The IPC family provides a software migration path for accelerating the customer design application from the lab through production assembly.

Z8000® Datacommunications

The Z8000 datacommunications family has many innovative intelligent, multi-protocol components for the high bit-rate, serial datacommunications markets. These products provide customers with a tremendous selection and the most flexibility in protocols, system interfaces and data transfer rates in the industry. Zilog datacom controllers ensure quick, easy and flexible interconnection of hosts and peripherals in applications such as local area networks, metropolitan area networks, bridges, routers, gateways and wide area networks.

The innovative EPM is among the support tools offered for Zilog's datacommunications controllers.

To find out more about Zilog's growing family of Superintegration products and support tools, contact your local Zilog sales office or authorized distributor today.

Microcontrollers

PART-TO-KIT CROSS REFERENCE MATRIX

APPLICATIONS BOARDS
TOOL BOX Family

EMULATORS
ICEBOX™ Family

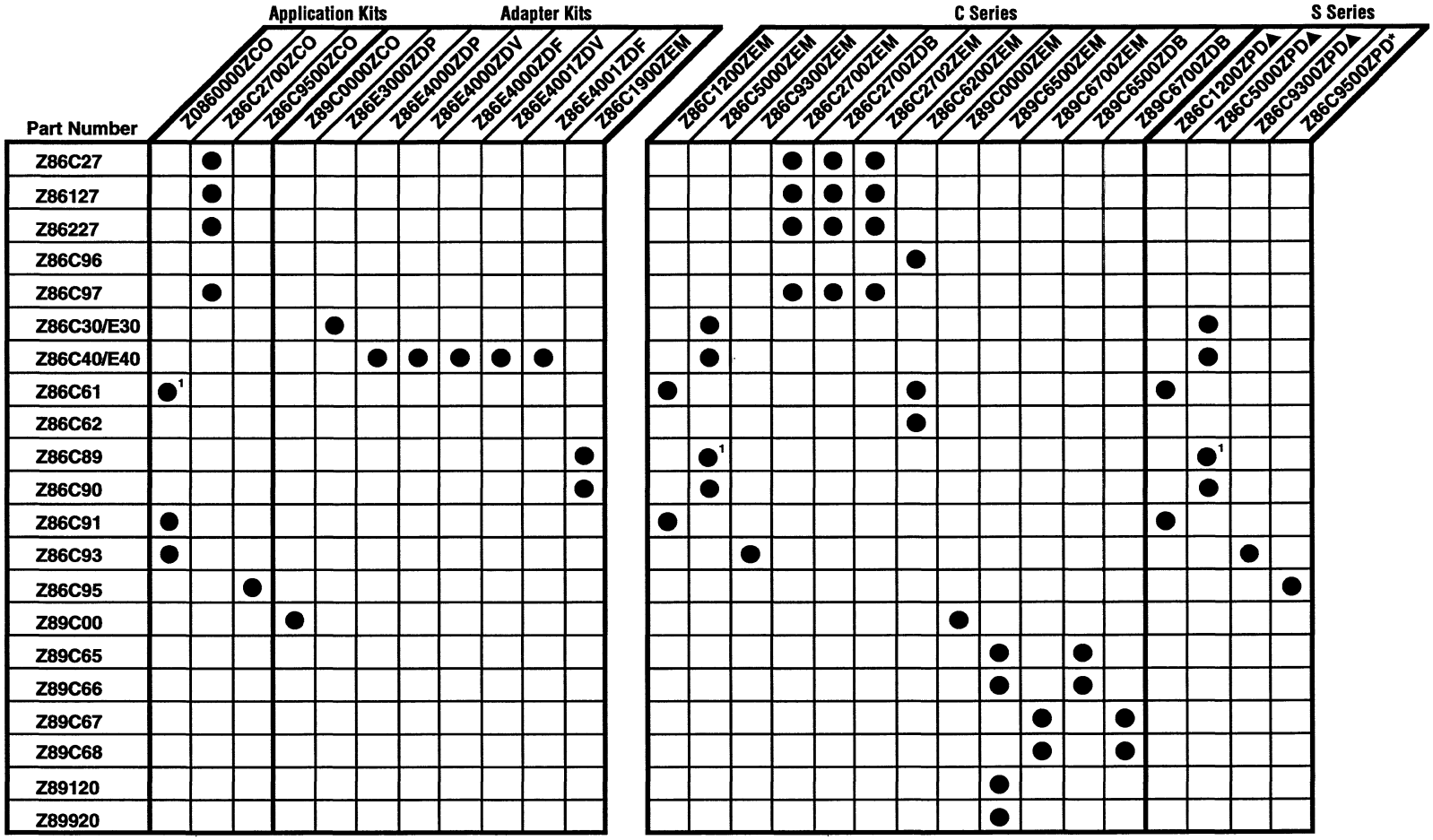
Part Number	Application Kits					Adapter Kits													C Series		S Series	
	Z08600ZCO	Z08600ZDP	Z08602ZCO	Z86C0800ZCO	Z86C1900ZCO	Z08602ZDP	Z86C0800ZDP	Z86E0600ZDP	Z86E2100ZDP	Z86E2100ZDV	Z86E2100ZDF	Z86E2101ZDV	Z86E2101ZDF	Z86E2300ZDP	Z86E2301ZDP	Z86E2300ZDV	Z86E2301ZDV	Z86C0800ZEM	Z86C1900ZEM	Z86C1200ZEM	Z86C5000ZEM	Z86C1200ZPD▲	Z86C5000ZPD▲
Z08600	●	●																		●[1]		●[1]	
Z08601	●																			●[1]		●[1]	
Z08602			●			●														●[1]		●[1]	
Z08604							●[3]												●[3]	●[1]		●[1]	
Z08611	●																			●[1]		●[1]	
Z08614			●			●														●[1]		●[1]	
Z86C06/L06							●														●		●[3]
Z86C07/C08				●			●											●		●		●[2]	
Z06E08				●			●											●		●		●[2]	
Z86C09					●		●												●		●		●
Z86C19/L29					●		●												●		●		●
Z86C21	●																			●		●	
Z86E21/E22	●							●	●	●	●	●								●		●	
Z86E23			●										●	●	●	●				●[1]		●[1]	
Z86C00/10/20	●	●																		●		●	
Z86C11	●																			●		●	

Notes:
1 Functional Emulation
2 Z86C0800ZDP Required
3 Excluding SPI
▲ Z86C0000ZUSP Required

PART-TO-KIT CROSS REFERENCE MATRIX

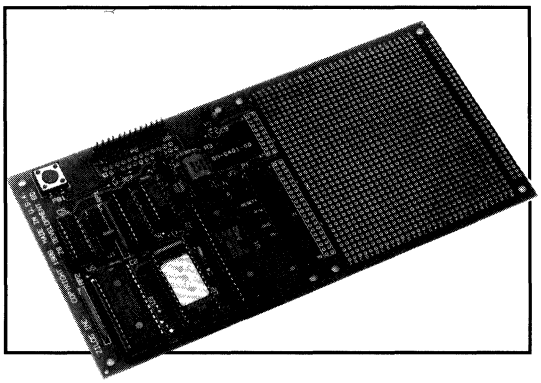
APPLICATIONS BOARDS
TOOL BOX Family

EMULATORS
ICE BOX™ Family



Notes:
1 Functional Emulation
* Z89C9500ZUSP Required
▲ Z86C0000ZUSP Required

Z0860000ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8600, Z8601, Z8611, Z86C21, Z86C61, Z86C91, Z86C93

DESCRIPTION
The Z8® Development Kit can be used for several purposes. As an evaluation tool, one can learn the Z8 instruction set plus the manipulation of the Z8 MCU's interrupt vectors and register set. Secondly, the Z8 Development Kit is designed to aid the user in constructing specific applications using the Z8 microcontroller.

SPECIFICATIONS
Power Requirements
+5 Vdc @ 50 mA

Dimensions
Width: 4.0 in. (10.2 cm)
Length: 8.0 in. (20.3 cm)

Serial Interface
RS-232C @ 9600 baud

KIT CONTENTS
Z8 Development Board
CMOS Z86C91 MPU
12 MHz Crystal
(32K)/8K x 8 EPROM
(32K)/8K x 8 Static RAM
RS-232C PC Interface
Z86C91 Expansion Header

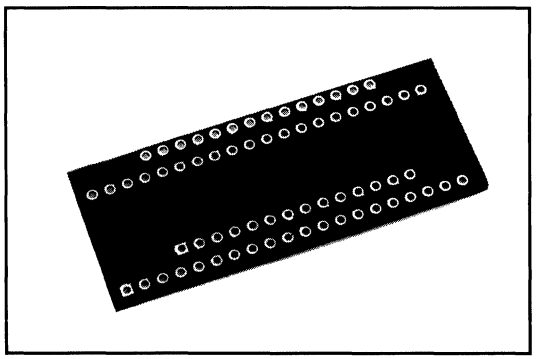
Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8/Super8™ Assembler and Utilities
Host Communication Package
Monitor Instructions
Tutorial
Sample Z86C91 Application Software

Documentation
Microcontrollers Data Book
Z8 Development Kit User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z0860000ZCO

Z0860000ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8600, Z8610, Z86C00, Z86C10, Z86C20, Z86C60

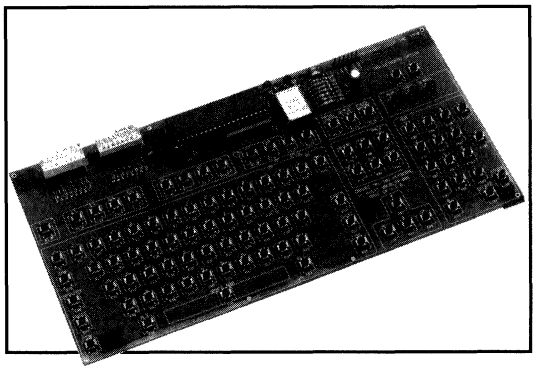
DESCRIPTION
The Z8600 Adapter Kit allows a standard Z8® emulator to emulate a Z8600 microcontroller converting a 40-pin Z8 pin out MCU to a 28-pin Z8 pin out MCU.

SPECIFICATIONS
Dimensions
Width: 0.9 in. (2.3 cm)
Length: 2.2 in. (5.4 cm)

KIT CONTENTS
Z8600 Adapter Board
PC Board

ORDERING INFORMATION
Part No: Z0860000ZDP

Z0860200ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z08602, Z08614, Z86E23

DESCRIPTION
The kit contains an assembled circuit board, Z08602 with keyboard, ROM-code, and documentation to help the user become familiar with the features of the Z08602 keyboard controller.

The Z08602 microcontroller is designed into a 101/102 PC keyboard circuit to control all scan codes, line status modes, scan timing and communication between the keyboard and PC.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .2 A (supplied by PC)

Dimensions
Width: 4.6 in. (11.7 cm)
Length: 9.3 in. (23.6 cm)

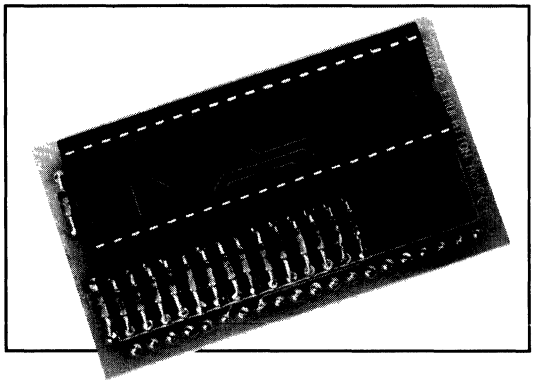
KIT CONTENTS
Z08602 101/102 Keyboard
NMOS Z08602 MPU
2 MHz Crystal
101/102 Keyboard Option
3 LEDs
Two 8-Position Dip Switches
6-Pin Communication Header

Software (IBM® PC Platform)
Contact Zilog for Licensing of Keyboard Source Code

Documentation
Z8602 Application Note
Z8602 Product Specification

ORDERING INFORMATION
Part No: Z0860200ZCO

Z0860200ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z08602

DESCRIPTION
The Z08602 adapter board is a tool used to adapt a standard Z8601 type device or emulation system to a Z8602 target socket.

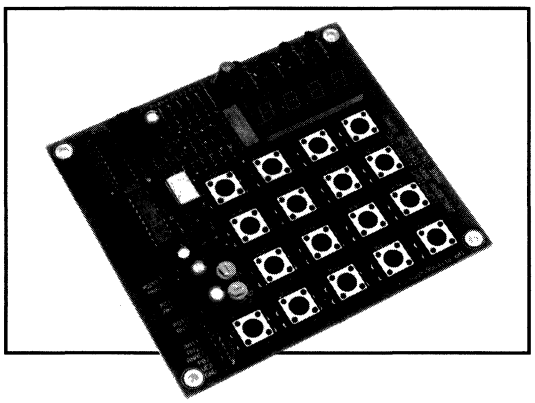
SPECIFICATIONS
Dimensions
Width: 1.3 in. (3.3 cm)
Length: 2.3 in. (5.8 cm)

KIT CONTENTS
Z08602 Adapter Board
40-Pin Z08601/Z08611 MPU Socket
40-Pin Z08602 Connecter

Documentation
Z08602 Adapter Kit User Guide

ORDERING INFORMATION
Part No: Z0860200ZDP

Z86C0800ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86C08

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to help the user become familiar with the features of the Z86C08 microcontroller.

The Applications Board is used to demonstrate the advantages and versatility of the 18-pin Z8 device. Included is simple hardware and software that demonstrates the implementation of WDT, HALT, and STOP mode, low cost D to A and A to D conversion techniques.

SPECIFICATIONS
Power Requirements
+5 Vdc @ 50 mA

Dimensions
Width: 4.4 in. (11.2 cm)
Length: 4.8 in. (12.2 cm)

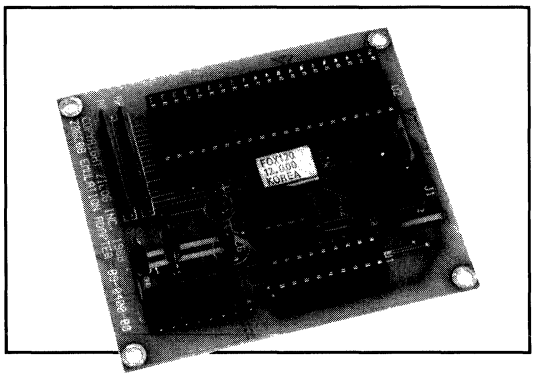
KIT CONTENTS
Z86C08 Application Board
CMOS Z86C08 MPU
4 MHz Crystal
Four 7-segment LED Displays
17-Key Keypad

Software (IBM® PC Platform)
Application Source Code
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader

Documentation
Microcontrollers Data Book
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Z86C08 Application Kit User Guide

ORDERING INFORMATION
Part No: Z86C0800ZCO

Z86C0800ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86C08

DESCRIPTION
The Z86C08 adapter board converts the Z8® MCU from a 40-pin pin out to an 18-pin pin out. This adapter board allows a standard Z8 emulation device to emulate the Z86C08. The Z86C08 Adapter Board is placed between the Z8 emulator and the user's target socket. The board does not emulate the watchdog timer function.

SPECIFICATIONS
Dimensions
Width: 2.5 in. (6.4 cm)
Length: 2.9 in. (7.4 cm)

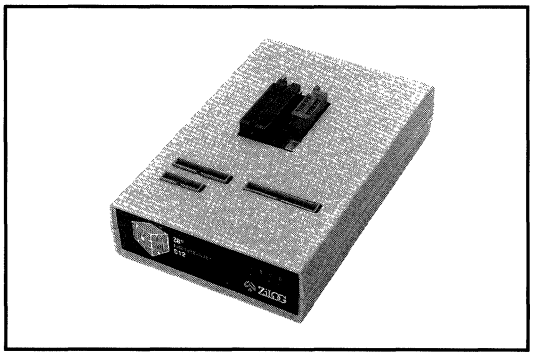
KIT CONTENTS
Z86C08 Adapter Board
40-Pin Z8 MPU Socket
18-Pin Z86C08 Socket
12 MHz Crystal

Cables
18-Pin Z86C08 Emulation Cable

Documentation
Z86C08 Adapter Kit User Guide

ORDERING INFORMATION
Part No: Z86C0800ZDP

Z86C1200ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86C08, Z86E08, Z86C00, Z86C10, Z86C11 Z86C20, Z86C21, Z86E21, Z86C61, Z86C91

DESCRIPTION
The Z86C1200ZEM is a member of Zilog's ICEBOX product family of in-circuit emulators. The ICEBOX -C12 provides emulation and OTP programming support for Zilog's Z8® microcontroller. The Emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM XT, AT compatible).

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed 16 MHz

Power Requirements
+5 Vdc @ 1.0 A

Dimensions
Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface
RS-232C @ 19200 baud

KIT CONTENTS
Z86C12 Emulator
Z8 Emulation Base Board
- CMOS Z86C9120PSC
- 8K x 8 EPROM
  (Programmed with Debug Monitor)
- EPM5128 EPLD
- 32K x 8 Static RAM
- 3 64K x 4 Static RAM
- RS-232C Interface
- Reset Switch

Z86C12 Emulation Daughter Board
- EPM5032 EPLD
- 16 MHz CMOS Z86C1216GSE ICE Chip
- 40-,18-Pin ZIF OTP Sockets
- 80-, 60-, 40-Pin Target Connectors

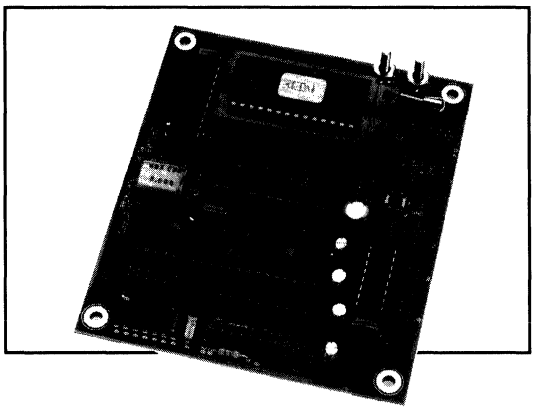
Cables
12" 40-Pin DIP Emulation Pod
12" 28-Pin DIP Emulation Pod
12" 18-Pin DIP Emulation Pod
48" Power Cable
15" Power Cable with Banana Plugs
60" DB 25 RS-232C Cable

Software (IBM® PC Platform)
Z8/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Host Package
Windowss Host Interface (GUI)

Documentation
ICEBOX™ User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Registration Card
Windows Host Interface User Guide (GUI)

ORDERING INFORMATION
Part No: Z86C1200ZEM

Z86C1900ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8604, Z86C09, Z86C19, Z86C90

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the maskROM Z86C09/19 and ROMless Z86C90 devices.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows object code to be down-loaded and subsequently debugged.

Code targeted for the Z86C09/19 device may be verified in the target application before submitting to Zilog for production masking.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .5 A

Dimensions
Width: 3.5 in. (8.9 cm)
Length: 4.0 in. (10.2 cm)

Serial Interface
RS-232C @ 9600 baud

KIT CONTENTS
Z86C19 Evaluation Board
CMOS Z86C90 MPU
8 MHz Crystal
(32K)/8K x 8 ZIF Socket (supplied with Debug Monitor EPROM)
(32K)/8K x 8 Static RAM
RS-232C PC Interface
Z86C90 Expansion Header
Z86C09/19 Emulation Header

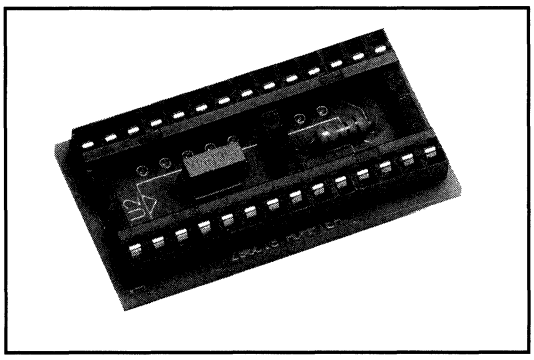
Cables
25-Pin RS-232 Cable
18-Pin Z86C19 Emulation Cable

Software (IBM® PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code
Z86C09 Example Software

Documentation
Microcontrollers Data Book
Z86C09/19 Product Specification
Z86C30/40/90 Product Specification
Z86C19ZEM Kit User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z86C1900ZEM

Z86E0600ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86E06/09/19

DESCRIPTION
The Z86E06 Program Conversion Board is a simple adapter which converts the 28-pin footprint of the Zilog Z86E30 OTP chip to the 18-pin DIP configuration of the Z86E06/09/19 OTP chip. The board supports all the functions of the Z86E06/09/19 except for SPI function.

SPECIFICATIONS
Dimensions
Width: 0.8 in. (2.0 cm)
Length: 1.5 in. (3.8 cm)

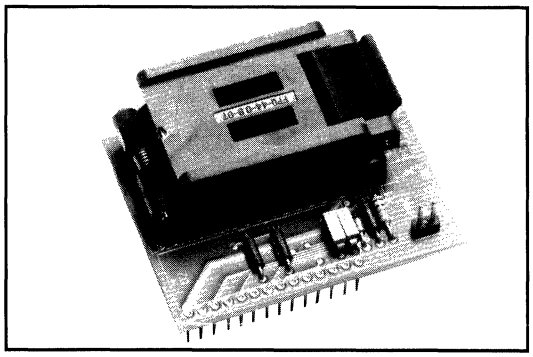
KIT CONTENTS
Z86E06 Program Conversion Board
28-Pin Z86E30 MCU Socket
18-Pin Z86E06/09/19 Connector

Cables
25-Pin RS-232 Cable
18-Pin Z86C19 Emulation Cable

Documentation
Z86E06 OTP Conversion Kit User Guide

ORDERING INFORMATION
Part No: Z86E0600ZDP

Z86E2100ZDF
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E21

DESCRIPTION
The Z86E21 QFP OTP Program Adapter Kit allows the 2764A standard EPROM programmer to program the Z86E21 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

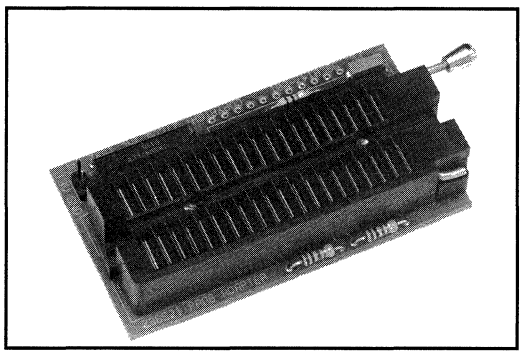
Dimensions
Width: 1.75 in. (4.4 cm)
Length: 2.20 in. (5.6 cm)

KIT CONTENTS
Z86E21 QFP OTP Program Adapter Board
44-Pin QFP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E2100ZDF

Z86E2100ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E21

DESCRIPTION
The Z86E21 DIP OTP Program Adapter Kit allows the 2764A standard EPROM programmer to program the Z86E21 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

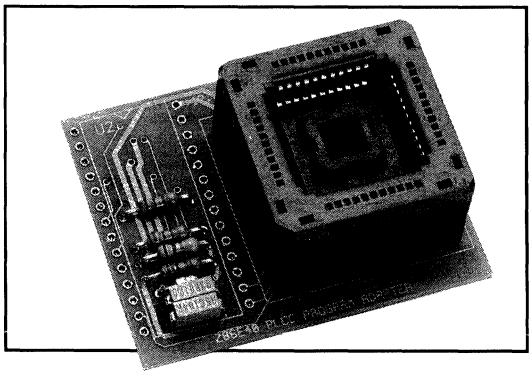
Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E21 OTP Program Adapter Board
40-Pin DIP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E2100ZDP

Z86E2100ZDV
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E21

DESCRIPTION
The Z86E21 PLCC OTP Program Adapter Kit allows the 2764A standard EPROM programmer to program the Z86E21 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

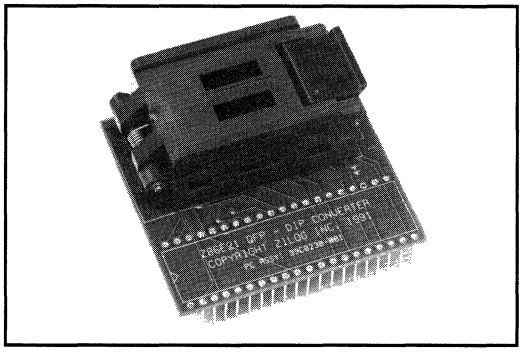
Dimensions
Width: 1.75 in. (4.4 cm)
Length: 2.20 in. (5.6 cm)

KIT CONTENTS
Z86E21 PLCC OTP Program Adapter Board
44-Pin PLCC ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E2100ZDV

Z86E2101ZDF
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E21

DESCRIPTION
The Z86E21 OTP Program Conversion Kit converts a 44-pin QFP package to a 40-pin DIP package, which allows the C12 ICEBOX™ to program the 44-pin QFP Z86E21 OTP microcontroller.

SPECIFICATIONS
Power Requirements
Not applicable.

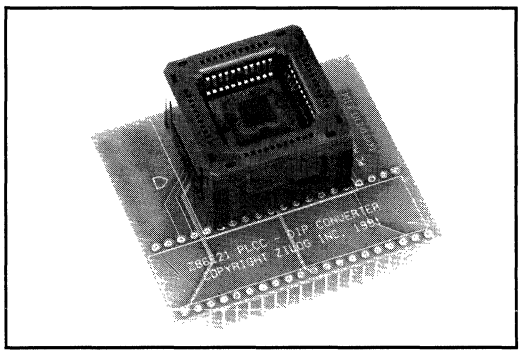
Dimensions
Width: 2.0 in. (5.1 cm)
Length: 2.1 in. (5.3 cm)

KIT CONTENTS
Z86E21 OTP Program Conversion Board
44-Pin QFP ZIF Socket
40-Pin Connector

Documentation
Not applicable.

ORDERING INFORMATION
Part No: Z86E2101ZDF

Z86E2101ZDV
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E21

DESCRIPTION
The Z86E21 OTP Program Conversion Kit converts a 44-pin PLCC package to a 40-pin DIP package, which allows the C12 ICEBOX™ to program the 44-pin PLCC Z86E21 OTP microcontroller.

SPECIFICATIONS
Power Requirements
Not applicable.

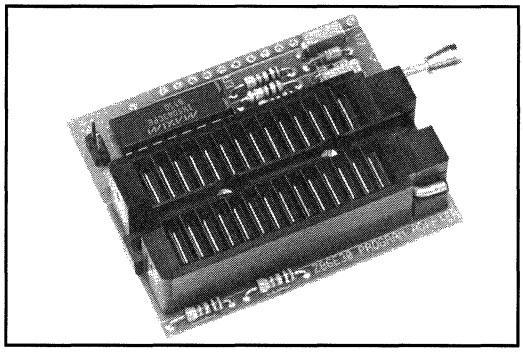
Dimensions
Width: 1.8 in. (4.6 cm)
Length: 2.1 in. (5.3 cm)

KIT CONTENTS
Z86E21 OTP Program Conversion Board
44-Pin PLCC ZIF Socket
40-Pin Connector

Documentation
Not applicable.

ORDERING INFORMATION
Part No: Z86E2101ZDV

Z86E2300ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E23

DESCRIPTION
The Z86E23 OTP Program Adapter Kit allows a Z86E21 OTP programmer to program the 40-pin DIP Z86E23 One-Time-Programmable microcontroller.

SPECIFICATONS
Power Requirements
Not applicable

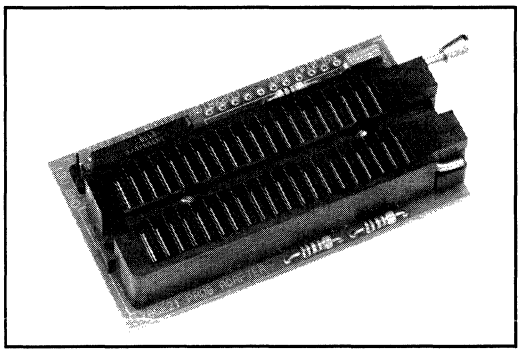
Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E23 OTP Program Adapter Board
40-Pin ZIF Socket
40-Pin Connector

DOCUMENTION
Z86E23ZDP Adapter User Guide

ORDERING INFORMATION
Part No: Z86E2300ZDP

Z86E2301ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E23

DESCRIPTION
The Z86E23 DIP OTP Program Adapter Kit provides the addition of hardware to program the 40-pin DIP Z86E23 OTP microcontroller on the C12 ICEBOX™.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

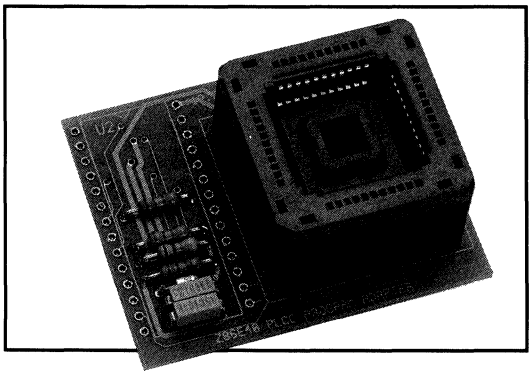
Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E23 OTP Program Adapter Board
40-Pin DIP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E2301ZDP

Z86E2300ZDV
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E23

DESCRIPTION
The Z86E23 PLCC OTP Program Adapter Kit allows the 2764A standard EPROM programmer to program the Z86E23 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

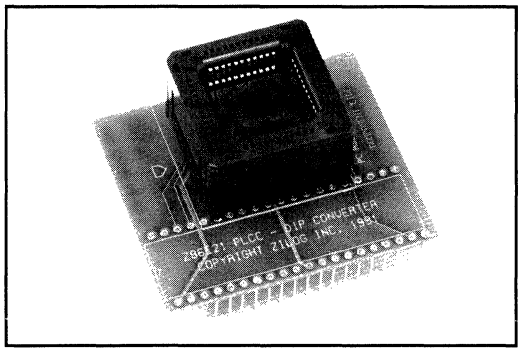
Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E23 PLCC OTP Program Adapter Board
40-Pin PLCC ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E2300ZDV

Z86E2301ZDV
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E23

DESCRIPTION
The Z86E23 OTP Program Conversion Kit converts a 44-pin PLCC package to a 40-pin PLCC package, which allows the C12 ICEBOX™ to program the 44-pin PLCC Z86E23 OTP microcontroller.

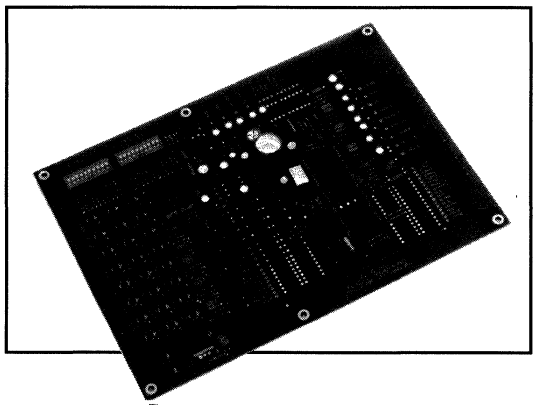
SPECIFICATIONS
Power Requirements
Not applicable.

Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E23 OTP Program Conversion Board
44-Pin PLCC ZIF Socket
40-Pin Connector

ORDERING INFORMATION
Part No: Z86E2301ZDV

Z86C2700ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86C27, Z86C97

DESCRIPTION
The Z86C2700ZCO Application Kit is specifically designed for users to evaluate the hardware and software of Zilog's Z86C27 Digital Television Controller (DTC™).

SPECIFICATIONS
Power Requirements
Supplied by Television Set

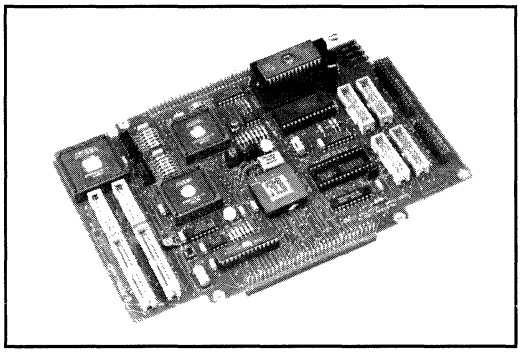
Dimensions
Width: 6.2 in. (15.7 cm)
Length: 8.6 in. (21.8 cm)

KIT CONTENTS
Z86C27 Application Board
CMOS Z86C27 MPU Socket
4 MHz Crystal
24 Key Multiplexed Keypad
Two 7-segment LED Displays
8 LEDs
13 PWMs
Low Pass Filter Interface
PLL Interface

Documentation
Microcontrollers Data Book
Z86C27 Application Kit User Guide

ORDERING INFORMATION
Part No: Z86C2700ZCO

Z86C2700ZDB
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86C27, Z86127, Z86C97, Z86227

DESCRIPTION
The Z86C2700ZDB Emulation Daughter Board provides emulation support for Zilog's DTC™ Family of ICs. The emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. An EPROM ZIF socket is provided for character ROM (CGROM) verification

An EPROM socket is provided for applying the application software. In addition, it can be used in conjunction with an Orion Unilab™ 8620 Emulator to generate program code and provide a simple connector interconnection for this purpose.

SPECIFICATIONS
Emulation Specification
Maximum emulation speed 16 MHz

Power Requirements
+5 Vdc @ 1.0 A

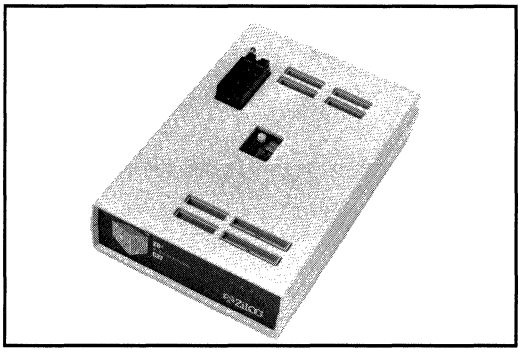
KIT CONTENTS
Z86C27 Emulation Daughter Board
16 MHz CMOS Z86C1216GSE ICE Chip
8K x 8 Static RAM
28-Pin ZIF Socket
6 HP-16500A Logic Analysis System Interface Connectors
60/60 Pin Target Connectors

Cables
12" Z86C27 64-Pin DIP Emulation Pod
12" Z86227 40-Pin DIP Emulation Pod
15" Power Cable with Banana Plugs
60" DB 25 RS-232C Cable

Documentation
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Registration Card

ORDERING INFORMATION
Part No: Z86C2700ZDB

Z86C2702ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86C27, Z86127, Z86C97, Z86227

DESCRIPTION
The Z86C2702ZEM In-Circuit-Emulator (ICEBOX™) provides emulation support for Zilog's DTC™ Family of ICs. The emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT compatible). An EPROM ZIF socket is provided for character ROM (CGROM) verification.

The Z86C2700ZDB daughter board can also be used in a standalone mode. An EPROM socket is provided for applying the application software. In Addition, it can be used in conjunction with an Orion Unilab™ 8620 Emulator to generate program code and provide a simple connector interconnection for this purpose.

SPECIFICATIONS
Emulation Specification
Maximum emulation speed 16 MHz

Power Requirements
+5 Vdc @ 1.0 A

Dimensions
Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

KIT CONTENTS
Z86C27 Emulator
Z8 Emulation Base Board
- CMOS Z86C9120PSC
- 8K x 8 EPROM (Programmed with Debug Monitor)
- 32K x 8 Static RAM
- 3 64K x 4 Static RAM
- RS-232C Interface
- Reset Switch

Z86C27 Emulation Daughter Board
- 16 MHz CMOS Z86C1216GSE ICE Chip
- 8K x 8 Static RAM
- 28-Pin ZIF Socket
- 6 HP-16500A Logic Analysis System Interface Connectors
- 60/60 Pin Target Connectors

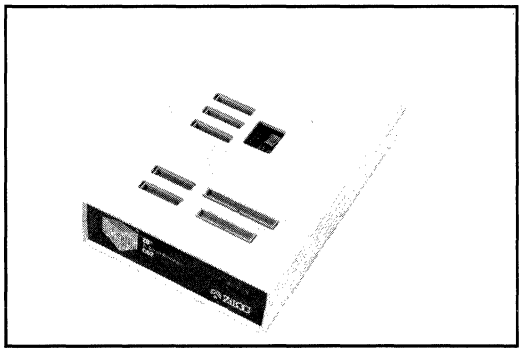
Cables
12" Z86C27 64-Pin DIP Emulation Pod
12" Z86227 40-Pin DIP Emulation Pod
15" Power Cable with Banana Plugs
60" DB 25 RS-232C Cable

Software (IBM PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Host Package
Windows Host Interface (GUI)

Documentation
ICEBOX™ User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Registration Card
Windows Host Interface User Guide (GUI)

ORDERING INFORMATION
Part No: Z86C2702ZEM

Z86C6200ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86C62, Z86C96

DESCRIPTION
The Z86C6200ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The ICEBOX C62 provides emulation for Zilog's Z86C62 (ROM device) and Z86C96 (ROMless device) micro-controllers. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT, 386, 486 compatible).

SPECIFICATIONS
Emulation Specification
Maximum emulation speed 16 MHz

Power Requirements
+5 Vdc @ .5 A

Dimensions
Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface
RS-232C @ 19200 baud

KIT CONTENTS
Z86C62 Emulator
Z8® Emulation Base Board
- CMOS Z86C9120PSC
- 8K x 8 EPROM (Programmed with Debug Monitor)
- 32K x 8 Static RAM
- 3 64K x 4 Static RAM
- RS-232C Interface
- Reset Switch

Z86C62 Emulation Daughter Board
- 20 MHz CMOS Z86C9620VSC ICE Chip
- 5 HP-16500A Logic Analysis System Interface Connectors
- 80/60 Pin Target Connector

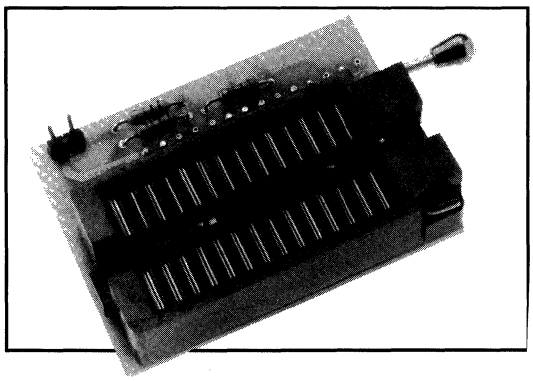
Cables
12", Z86C96 68-Pin PLCC Emulation Pod
12", Z86C62 64-Pin DIP Emulation Pod
48" Power Cable
15" Power Cable with Banana Plugs
60" DB 25 RS-232C Cable

Software (IBM PC Platform)
Z8/Z80®/Z8000® Cross Assembler
Windows Host Interface (GUI)
MOBJ Link/Loader
Host Package

Documentation
ICEBOX™ User Guide
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Windows Host Interface User Guide (GUI)
Registration Card

ORDERING INFORMATION
Part No: Z86C6200ZEM

Z86E3000ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E30

DESCRIPTION
The Z86E30 DIP OTP Program Adapter Kit allows a standard EPROM programmer to program the Z86E30 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5A

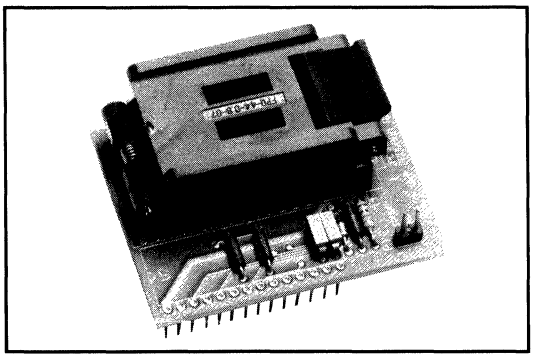
Dimensions
Width: 1.45 in. (3.68 cm)
Length: 2.0 in. (5.08 cm)

KIT CONTENTS
Z86E30 OTP Program Adapter Board
28-Pin DIP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E3000ZDP

Z86E4000ZDF
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E40

DESCRIPTION
The Z86E40 QFP OTP Program Adapter Kit allows a standard EPROM programmer to program the Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

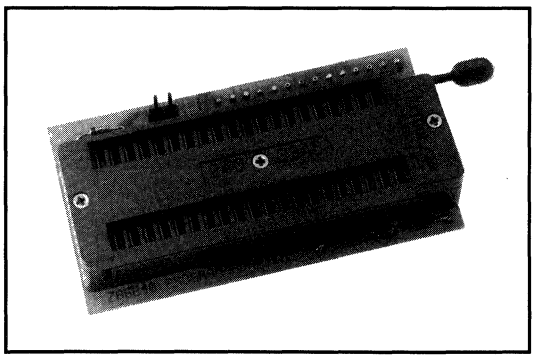
Dimensions
Width: 1.75 in. (4.4 cm)
Length: 2.20 in. (5.6 cm)

KIT CONTENTS
Z86E40 QFP OTP Program Adapter Board
44-Pin QFP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E4000ZDF

Z86E4000ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E40

DESCRIPTION
The Z86E40 DIP OTP Program Adapter Kit allows a standard EPROM programmer to program the Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

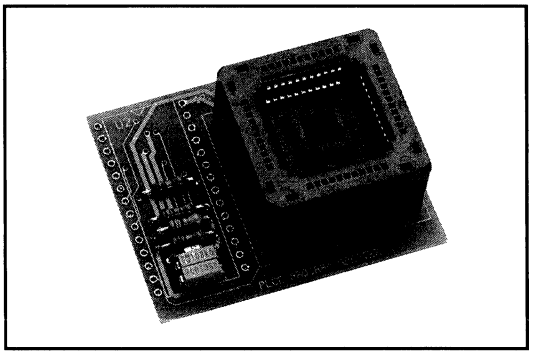
Dimensions
Width: 1.4 in. (3.6 cm)
Length: 2.6 in. (6.6 cm)

KIT CONTENTS
Z86E40 DIP OTP Program Adapter Board
40-Pin DIP ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E4000ZDP

Z86E4000ZDV
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E40

DESCRIPTION
The Z86E40 PLCC DIP OTP Program Adapter Kit allows a standard EPROM programmer to program the Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
+12.5 Vdc @ .5 A

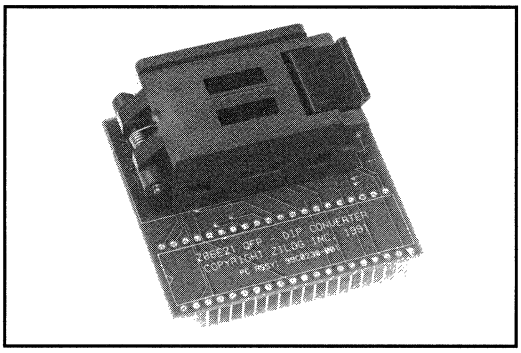
Dimensions
Width: 1.6 in. (4.1 cm)
Length: 2.0 in. (5.1 cm)

KIT CONTENTS
Z86E40 PLCC OTP Program Adapter Board
40-Pin ZIF Socket
28-Pin Connector

Documentation
OTP Program Adapter User Guide

ORDERING INFORMATION
Part No: Z86E4000ZDV

Z86E4001ZDF
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E40

DESCRIPTION
The Z86E40 OTP Program Conversion Kit converts a 44-pin QFP package to a 40-pin DIP package, which allows the C50 ICEBOX™ to program the 44-pin QFP Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
Not applicable.

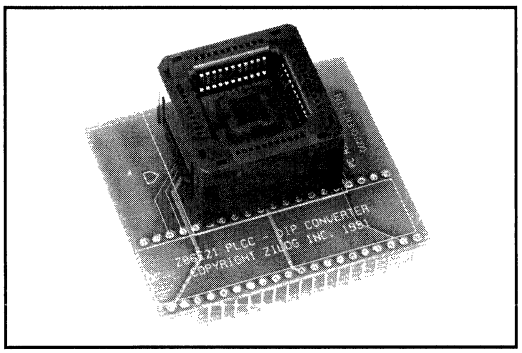
Dimensions
Width: 2.05 in. (5.2 cm)
Length: 2.10 in. (5.3 cm)

KIT CONTENTS
Z86E40 OTP Program Conversion Board
44-Pin QFP ZIF Socket
40-Pin Connector

Documentation
Not applicable.

ORDERING INFORMATION
Part No: Z86E4001ZDF

Z86E4001ZDV
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86E40

DESCRIPTION
The Z86E40 OTP Program Conversion Kit converts a 44-pin PLCC package to a 40-pin DIP package, which allows the C50 ICEBOX™ to program the 44-pin PLCC Z86E40 OTP microcontroller.

SPECIFICATIONS
Power Requirements
Not applicable.

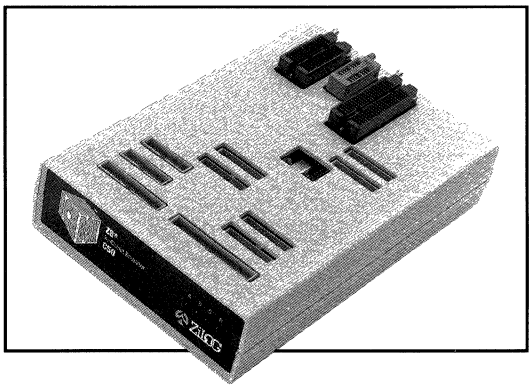
Dimensions
Width: 1.8 in. (4.6 cm)
Length: 2.1 in. (5.3 cm)

KIT CONTENTS
Z86E40 OTP Program Conversion Board
40-Pin PLCC ZIF Socket
40-Pin Connector

Documentation
Not applicable.

ORDERING INFORMATION
Part No: Z86E4001ZDV

Z86C5000ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z86C06, Z86C09/19, Z86E09, Z86C30, Z86E30, Z86C40, Z86E40, Z86C89, Z86C90

DESCRIPTION
The Z86C5000ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The ICEBOX -C50 provides emulation and OTP programming support for Zilog's CCP™ (Consumer Controller Processor) microcontroller. The Emulator provides all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/software product. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT compatible).

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed 16 MHz

Power Requirements
+5 Vdc @ 1.0 A

Dimensions
Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface
RS-232C @ 19200 baud

KIT CONTENTS
Z86C50 Emulator
Z8® Emulation Base Board
- CMOS Z86C9120PSC
- 8K x 8 EPROM (Programmed with Debug Monitor)
- 32K x 8 Static RAM
- 3 64K x 4 Static RAMs
- RS-232C Interface
- Reset Switch

Z86C50 Emulation Daughter Board
- 20 MHz CMOS Z86C5020GSE ICE Chip
- 2K x 8 Static RAM
- 40/28/18 Pin ZIF OTP Sockets
- 6 HP-16500A Logic Analysis System Interface Connectors
- 80-, 60-, 40-Pin Target Connectors

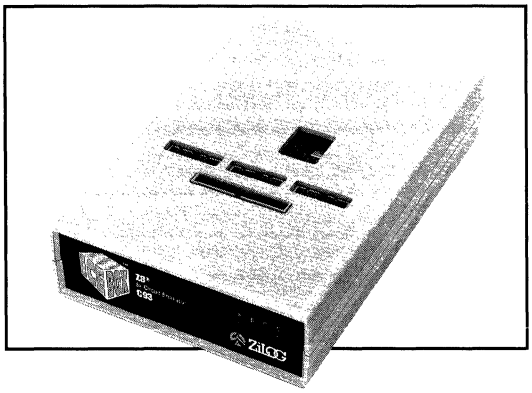
Cables
12" 40-Pin DIP Emulation Cable
12" 28-Pin DIP Emulation Cable
12" 18-Pin DIP Emulation Cable
15" Power Cable with Banana Plugs
48" Power Cable
60" DB 25 RS-232C Cable

Software (IBM PC Platform)
Z8/Z80®/Z8000® Cross Assembler
Windows Host Interface (GUI)
MOBJ Link/Loader
Host Package

Documentation
ICEBOX™ User Guide
Z8 Cross Assembler User Guide
Windows Host Interface User Guide (GUI)
MOBJ Link/Loader User Guide
Registration Card

ORDERING INFORMATION
Part No: Z86C5000ZEM

Z86C9300ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86C93

DESCRIPTION
The Z86C9300ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The ICEBOX -C93 provides emulation for Zilog's Z86C93 microcontroller. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware/ software product. The Emulator can be connected to a serial port COM 1 or COM 2 of the host computer (IBM® XT, AT, 386, 486 compatible).

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed 16 MHz

Power Requirements
+5 Vdc @ .5A

Dimensions
Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface
RS-232C @ 19200 baud

KIT CONTENTS
Z86C93 Emulator
Z8® Emulation Base Board
- CMOS Z86C9120PSC
- 8K x 8 EPROM (Programmed with Debug Monitor)
- 32K x 8 Static RAM
- 3 64K x 4 Static RAMs
- RS-232C Interface
- Reset Switch

Z86C93 Emulation Daughter Board
- 20 MHz CMOS Z86C9320GSE ICE Chip
- 3 HP-16500A Logic Analysis System Interface Connectors
- 80-Pin Target Connector

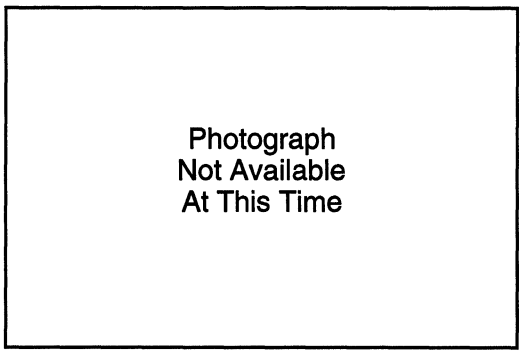
Cables
12" Z86C93 44-Pin PLCC Emulation Pod
15" Power Cable with Banana Plugs
48" Power Cable
60" DB 25 RS-232C Cable

Software (IBM PC Platform)
Z8/Z80®/Z8000® Cross Assembler
Windows Host Interface (GUI)
MOBJ Link/Loader
Host Package

Documentation
ICEBOX™ User Guide
Z8 Cross Assembler User Guide
Windows Host Interface User Guide (GUI)
MOBJ Link/Loader User Guide
Registration Card

ORDERING INFORMATION
Part No: Z86C9300ZEM

Z86C9500ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z86C95

DESCRIPTION
The Z86C9500ZCO Evaluation Board contains an assembled circuit board, software and documentation for use in evaluating the Z86C95 Z8®/DSP microcontroller. The board comes equipped with a monitor program which provides access to all the Z86C95 registers and on-board memory and assists in using the Z86C95.

SPECIFICATIONS
Power Requirements
$+3 < V_{cc} < +5$ Vdc

Serial Interface
RS-232C @ 9600 baud

Dimensions
Width: 5.2 in. (13.2 cm)
Length: 5.0 in. (12.7 cm)

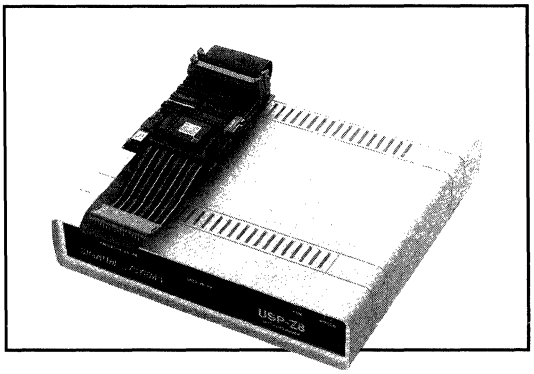
KIT CONTENTS
Z86C95 Evaluation Board
Z86C95 CMOS Microcontroller Z8®/DSP Unit
8Kx8 EPROM with Monitor Program
32Kx8 SRAM
RS232-C Port
Sockets for external DAC80 and ADC0820 12 LEDs
Headers for access to all signals
Pin-out Header
RS232-C Connector
Power Connector

Software (IBM-PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader

Documentation
Z8 Cross Assembler User Guide
MOBJ Link/Loader User Guide
Z86C95 Product Specification
Z86C95 Evaluation Kit User's Guide

ORDERING INFORMATION
Part No: Z86C9500ZCO

Z8 S Series Emulators
BASE UNITS AND PODS



DESCRIPTION
The system comprises three base unit options, (64K, 128K, or 256K of emulation program ROM), and four pod options which allow the emulation of various Z8 microcontrollers. Features include real-time trans-parent emulation up to 20 MHz, in-line symbolic assembler and disassembler, real-time hardware breakpoints, eight channel user logic analyser, external trigger input and outputs, trace display and memory display/edit during execution, and window or command driven user interface.

SPECIFICATIONS
Microcontrollers Emulated:

Z86C1200ZPD	Z86C00, Z86C10, Z86C20, Z86C11, Z86C21, Z86E21, Z86C91, Z86C61
Z86C5000ZPD	Z86C09, Z86C19, Z86C30, Z86C40, Z86C90
Z86C9300ZPD	Z86C93
Z86C9500ZPD	Z86C95

Maximum Emulation Speed:
Up to 30 MHz (microcontroller dependent)

Size:
260 mm wide, 260 mm deep, 64 mm high

Operating Temperature:
0°C to +40°C

Storage Temperature:
-10°C to +65°C

Operating Humidity:
0 to 90%

Maximum Emulation Program Memory:
64 Kbytes with Z86C0000ZUSP064
128 Kbytes with Z86C0000ZUSSP128
256 Kbytes with Z86C0000ZUSP256

Maximum Emulation Data Memory:
64 Kbytes

Program Memory Mapping:
1K blocks

Pass Counters:
Two, 16-bit each

Trace Buffer:
32K - 80 bits

Sequencer:
Hardware, 8 levels

User Probe:
Eight channel logic input
One trigger input
Seven trigger outputs (Events, Pass Counters, Sequencer)

Host Interface:
Asynchronous RS-232C
9600/115 KBaud
XON/XOFF support

File Upward/Downward Format:
Zilog MUFOM (EEE 695-1985)
Intel® HEX
Intel AOMF
2500AD® Software

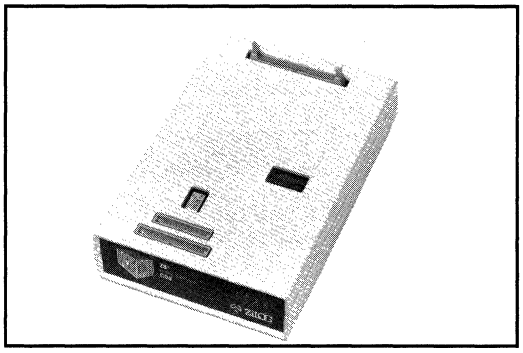
MINIMUM HOST REQUIREMENTS
- IBM® compatible PC/XT/AT/386 or PS-2
- 640 Kbyte memory
- 20 Mbyte hard disk
- RS-232 serial port (COM 1 or COM 2)
- Mouse (serial or bus)
- MDA, CGA, EGA, or VGA video adaptor

MINIMUM EMULATION SUPPORT
- One base unit
- One emulation pod

ORDERING INFORMATION:

Base Unit	Emulation Pod
Z86C0000ZUSP064	Z86C9300ZPD
Z86C0000ZUSP128	Z86C1200ZPD
Z86C0000ZUSP256	Z86C5000ZPD
Z86C9500ZUSP064	Z86C9500ZPD

Z89C0000ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z89C00

DESCRIPTION
The Z89C0000ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The ICEBOX -C00 provides emulation for Zilog's Z89C00 DSP core. This includes all the essential DSP timing and I/O circuitry which simplifies user emulation of the prototype hardware/ software product. The ICEBOX can be connected to a serial port COM 1 through COM 4 of the host computer (IBM® 386, 486, or compatible).

The ICEBOX provides basic support of a emulator (program execution, single step, jump, halt, breakpoint, download/upload program code, etc.). In addition, 64 K x 16 program memory in steps of 4K, 8K, 16K, 32K, and 64K (software selectable), 64K breakpoint support, maximum internal clock frequency of up to 16 MHz.

The host software runs under both MS Windows 3.0 and 3.1, it creates the Graphical User Interface (GUI) for the C00 ICEBOX. The software trace and symbolic debugging features give a big advantage for user code debugging.

SPECIFICATIONS
Power Requirements
+5 Vdc @ 1.5A

Dimensions
Width: 6.0 in. (15.2 cm)
Length: 8.8 in. (22.4 cm)

Serial Interface
RS-232C @ 19200 baud

Emulation Specification
Maximum Emulation Speed: 16 MHz

KIT CONTENTS
Z89C00 Emulator
Z8 Emulation Base Board
CMOS Z86C9120PSC
8K x 8 EPROM (Programmed with Debug Monitor)
32K x 8 Static RAM
RS-232C Interface
Three 64K x 4 Static RAM

Z89C00 Emulation Daughter Board
Z89C00 DSP ICE Chip
Five 64K x 4 Static RAM
80/60 Pin Target Connectors
100-Pin HP-16500 Interface Board Connector

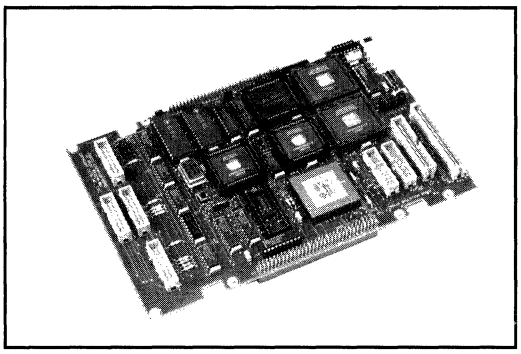
Cables
12" 68-Pin PLCC Emulation Cable
15" Power Cable with Banana Plugs
60" DP25 RS-232C Cable

Software (IBM PC platform)
ICEBOX GUI Host Package

Documentation
Z8 ICEBOX User Manual
Z8 ICEBOX GUI User Manual
Registration Card

ORDERING INFORMATION
Part No: Z89C0000ZEM

Z89C6500ZDB
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z89C65, Z89C66

DESCRIPTION
The Z89C6500ZDB is a daughter board that provides emulation support for Zilog's Z89C65 and Z89C66 microcontrollers. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware and/or software. The internal mask ROMs of Z89C65 and Z89C66 are emulated by external EPROMs on the board.

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed: 20.48 MHz

Power Requirements
+5 Vdc @ 1.4A

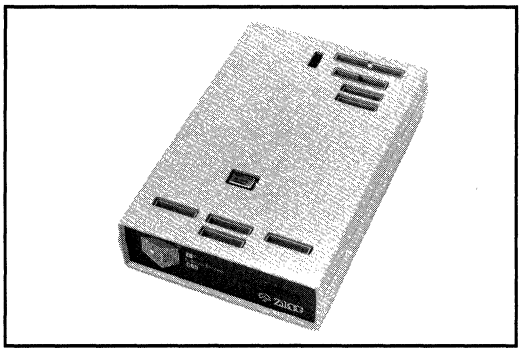
KIT CONTENTS
Z89C65 Emulation Daughter Board
Z86C5020GSE ICE Chip
Clarkspur CD2400
Three EPM5128 EPLD
Three EPM5192 EPLD
64K x 8 Static RAM
Six HP-16500A Logic Analysis System Interface Connectors
80/80 Pin Target Connectors

Cables
12" 84-Pin PLCC Emulation Cable
15" Power Cable with Banana Plugs
48" Power Cable

Documentation
Z89C65 User's Manual Supplement
Registration Card

ORDERING INFORMATION
Part No: Z89C6500ZDB

Z89C6500ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z89C65, Z89C66

DESCRIPTION
The Z89C6500ZEM is a member of Zilog's ICEBOX™ product family of in-circuit emulators. The emulator provides emulation support for Zilog's Z89C65 and Z89C66 microcontrollers. This includes all essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware and/or software.

Data entering and program debugging are performed by the monitor ROM and the Host Package which communicates via a RS-232C serial interface with a fixed 19200 baud rate. The user program can be downloaded directly from the host computer via the RS-232C connector and may then be executed using various debugging commands in the monitor. The ICEBOX can be connected to a serial port COM1 or COM2 of the host computer (IBM® XT, AT, 286, 386 or 486 compatible).

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed: 20.48 MHz

Power Requirements
+5 Vdc @ 1.4A

Dimensions
Width: 6.25 in.
Length: 9.50 in.
Height: 2.50 in.

Serial Interface
RS-232C @ 19200 baud

KIT CONTENTS
Z89C65 Emulator
Z8® Emulation Base Board
CMOS Z86C91120PSC
8K x 8 EPROM (Programmed with Debug Monitor)
EPM5128 EPLD
32K x 8 Static RAM
Three 64 x 4 Statoc RAM
RS-232C Interface
Reset Switch

Z89C65 Emulation Daughter Board
Z86C5020GSE ICE Chip
Clarkspur CD2400
Three EPM5128 EPLD
Three EPM5192 EPLD
64K x 8 Static RAM
Six HP-16500A Logic Analysis System Interface Connectors
80/80 Pin Target Connectors

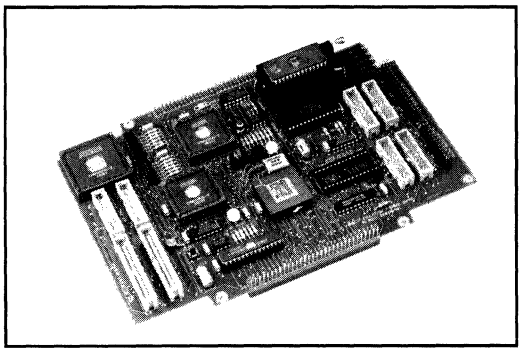
Cables
12" 68-Pin PLCC Emulation Cable
15" Power Cable with Banana Plugs
48" Power Cable
60" DP25 RS232C Cable

Software (IBM PC platform)
Z80®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Host Package
Windows Host Interface (GUI)

Documentation
Z8 ICEBOX™ User's Manual
Z89C65 User's Manual Supplement
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User's Guide
Windows Host Interface (GUI) User's Guide
Registration Card

ORDERING INFORMATION
Part No: Z89C6500ZEM

Z89C6700ZDB
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z89C67, Z89C68

DESCRIPTION
The Z89C6700ZBD is a daughter board that provides emulation support for Zilog's Z89C67 and Z89C68 microcontrollers. This includes all essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware and/or software. The internal mask ROMs of Z89C67 and Z89C68 are emulated by external EPROMs on the daughter board.

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed: 20.48 MHz

Power Requirements
+5Vdc @ 1.4A

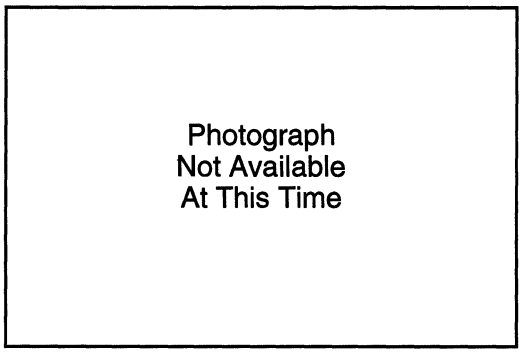
KIT CONTENTS
Z89C67 Emulation Daughter Board
Z86C5020GSE ICE Chip
Z89C00 DSP ICE Chip
Three EPM5128 EPLD
Three EPM5192 EPLD
64K x 8 Static RAM
Two 100-Pin HP-16500
Interface Board Connectors
80/80 Pin Target Connectors

Cables
12" 84-Pin PLCC Emulation Cable
15" Power Cable with Banana Plugs

Documentation
Z89C67 User's Manual Supplement
Registration Card

ORDERING INFORMATION
Part No: Z89C6700ZDB

Z89C6700ZEM
PRODUCT SPECIFICATION



SUPPORTED DEVICE
Z89C67, Z89C68

DESCRIPTION
The Z89C6700ZEM is a member of Zilog's ICEBOX™ product family of in circuit emulators. The emulator provides emulation support for Zilog's Z89C67 microcontroller. This includes all the essential MCU timing and I/O circuitry which simplifies user emulation of the prototype hardware and/or software.

Data entering and program debugging are performed by the monitor ROM and the Host Package which communicates via a RS-232C serial interface with a fixed 19200 baud rate. The user program can be downloaded directly from the host computer via the RS-232C connector and may then be executed using various debugging commands in the monitor. The ICEBOX can be connected to a serial port COM1 or COM2 of the host computer (IBM® XT, AT, 286, 386 or 486 compatible).

SPECIFICATIONS
Emulation Specification
Maximum Emulation Speed: 20.48 MHz

Power Requirements
+5Vdc @ 1.4A

Dimensions
Width: 6.25 in.
Length: 9.50 in.
Height: 2.50 in.

Serial Interface
RS-232 @ 19200 baud

KIT CONTENTS
Z89C67 Emulator
Z8® Emulation Base Board
CMOS Z86C91120PSC
8K x 8 EPROM (Programmed with Debug Monitor)
EPM5128 EPLD
32K x 8 Static RAM
Three 64 x 4 Static RAM
RS-232C Interface
Reset Switch

Z89C67 Emulation Daughter Board
Z86C5020GSE ICE Chip
Z89C00 DSP ICE Chip
Three EPM5128 EPLD
Three EPM5192 EPLD
64K x 8 Static RAM
Two 100-Pin HP-16500
Interface Board Connectors
80/80 Pin Target Connectors

Cables
12" 84-Pin PLCC Emulation Cable
15" Power Cable with Banana Plugs
60" DP25 RS-232C Cable

Software (IBM PC platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Host Package
Windows Host Interface (GUI)

Documentation
Z8 ICEBOX™ User Manual
Z89C67 User Manual Supplement
Z8 Cross Assembler User's Guide
MOBJ Link/Loader User Guide
Windows Host Interface User's Guide (GUI)
Registration Card

ORDERING INFORMATION
Part No: Z89C6700ZEM

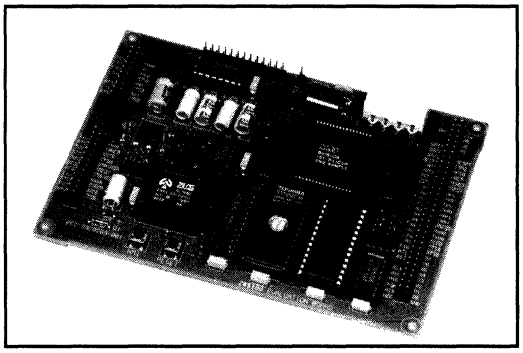
Classic

Part-To-Kit Cross Reference Matrix

	Z8S18000ZCO	Z80181100ZCO	Z80181100ZDP	Z80181101ZCO*	Z84C1100ZCO	Z84C1500ZCO	Z84C5000ZCO	Z84C9000ZCO	ZEPMIP00001	ZEPMIP00002
Z8S180	●								●	
Z80181		●	●	●					●	
Z80182										●
Z84C01								●		
Z84C11					●					
Z84C15						●				
Z84C43					●					
Z84C50							●			
Z84C90							●	●		

* Includes LLAP software that can be licensed.

Z8S18000ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8S180, Z85230

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z8S180 and Z85230 system at 18.432 MHz.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

The board comes with sample code to illustrate the use of Zilog's Z8S180 and Z85230 in a variety of communication applications.

SPECIFICATIONS
Power Requirements
+5Vdc @ 5A

Dimensions
Width: 5.65 in.
Length: 4.0 in.

Serial Interface
RS-232 @ 9600 baud

KIT CONTENTS
Z8S180/ESCC Evaluation Board
CMOS Z8S180 MPU
18.432 MHz Crystal
Socketed 64K/(8K) x 8 EPROM
(Programmed with Debug Monitor and Device Driver Demonstration Software)
Socketed 32K/(8K) x 8 Static RAM
RS-232C PC Interface
Z8S180 Expansion Header
Z85230 Expansion Header
Reset Switch
NMI Switch

Cables
25-pin RS-232 Cable

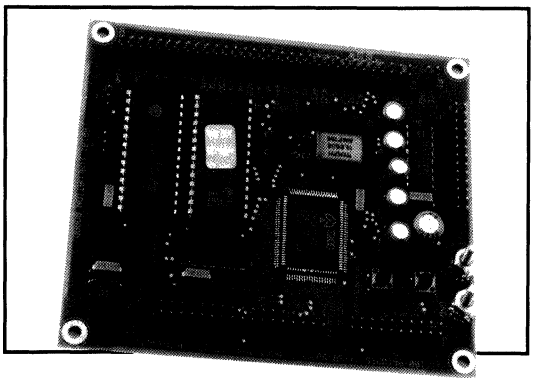
Software (IBM® PC Platform)
ASM800 Z800 Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor and Device Drivers Demonstration Software Source Code
Z8S180 Example Software
(a) In ASM800 Assembly
(b) In Microtec MCC80 C and Microtec ASM80 Assembly

Note: Zilog is not responsible for support and maintenance of the above software.

Documentation
Z8S180/ESCC Kit User Guide
Z80180/Z8S180 Product Specification
Z80180/Z180 Technical Manual
Z85230 Product Specification
Z85230/Z80230 Technical Manual
ASM800 Z800 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z8S18000ZCO

Z8018100ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z80181

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z80181 device.

The supplied cross assembler and link/loader package allows full assembly language support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .65 A

Dimensions
Width: 3.65 in. (9.27 cm)
Length: 4.20 in. (10.67 cm)

Serial Interface
RS-232C @ 9600 bits/sec.

KIT CONTENTS
Z180181 Evaluation Board
CMOS Z80181 MPU
19.6608 MHz Crystal
Socketed (32K) /8K x 8 EPROM
(Programmed with Debug Monitor)
Socketed (32K) /8K x 8 Static RAM
RS-232C Interface
Z80181 MPU Expansion Header
Z80181 Peripheral Signal
Expansion Header
Reset switch
Nmi switch

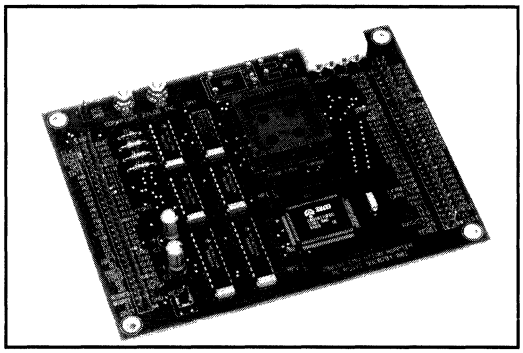
Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code
Z80181 Example Software

Documentation
Z80181 Kit User Guide
Z80181 Product Specification
Z8030/8530 Technical Manual
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z8018100ZCO

Z8018100ZDP
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z80181

DESCRIPTION
The Z80181 Emulator Adapter enables development and debugging of user target systems which utilize the Z80181 chip plus the use of a Z80180 In-Circuit Emulator that provides a 68-pin PLCC probe. It serves as a bridge between a Z80180 In-Circuit Emulator and a user target system.

SPECIFICATIONS
Power Requirements
V_{CC}= 5.0V

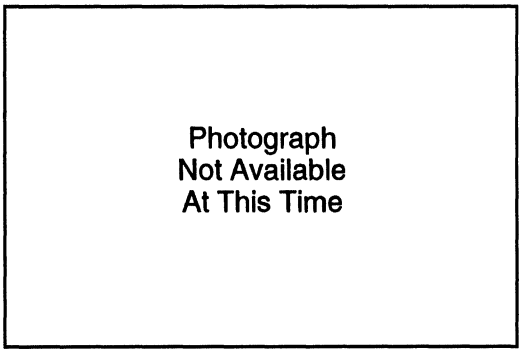
Dimensions
Width: 4.10 in.
Length: 5.40 in.

KIT CONTENTS
Z80181 Adapter Board
68-Pin PLCC Z180™ socket
Power Supply cable

Documentation
Z80181 Emulator Adapter Kit User Guide

ORDERING INFORMATION
Part No: Z8018100ZDP

Z8018101ZA6
PRODUCT SPECIFICATION



DESCRIPTION

The kit contains software and documentation to support AppleTalk® LocalTalk™ Link Access Protocol (LLAP) on Zilog's Z181™ (Z80181).

The Z8018101ZA6 LLAP driver requires a software licensing agreement. The driver is written in ANSI Microtec C and partly in Z181 Assembler, all contained in diskettes to be executed using an IBM® PC and a Microtec C compiler. The driver is composed of a series of C function calls that allows the Z181 (in conjunction with proper LLAP hardware interface, e.g., Z8018101ZCO) to transmit and receive LLAP packets. The lower level transmission and reception routines are finely tuned using Z181 assembler codes. Interface of Zilog's LLAP driver to AppleTalk®'s upper layer is left for the user.

Two examples using the Z181 LLAP driver are included. "Demo.c" tests the RTS and CTS handshake between two Z8018101ZCO boards by transmitting data between them. This demo requires two terminals interfaced via the RS-232C ports to the Z8018101ZCO boards. "Mainecho.c" allows two Z8018101ZCO boards to transmit and receive LLAP packets. The user can then observe the transactions with his LLAP network analyzer. Although this example application program does not execute the higher layers of the AppleTalk stack, its inclusion demonstrates that the LLAP packets adhere to LLAP specifications. The example application programs also provide the user with models on which to base his own application program. Source codes and documentations are included in the kit.

Z80181 LLAP Driver Description

The kit contains source code and documentation (User Guide, LLAP Driver for the Z181 and Design, LLAP Driver for the Z181) for the Z181 LocalTalk Link Access Protocol Driver. The User Guide, LLAP Driver for the Z80181 describes the Zilog-provided driver for the Z181 and explains how the driver is to be used. The Design, LLAP Driver for the Z181 explains how the driver works.

The kit is intended for users who wish to interface an AppleTalk node to a LocalTalk network using the Z181. Interface to the upper layers of the AppleTalk stack varies from user to user and is not addressed in the documentation. The documentation does provide a general overview of the ways the Z181 LLAP driver is intended to fit in a larger software system.

In general, the Z181 LLAP Driver implements the LLAP protocol described in Inside AppleTalk by Sidhu et.al. In particular, the driver performs the following functions:

- It establishes its own node address by transmitting ENQ frames as required.
- It responds to a received ENQ frame with an appropriate ACK frame.
- It responds to a received RTS frame with an appropriate CTS frame.
- It receives any data frames addressed to the node or to the broadcast address and routes them according to given instructions.
- It transmits an RTS frame before sending a broadcast data frame.
- It transmits an RTS frame and waits for a CTS frame in response before sending a non-broadcast data frame. It retries as necessary.
- It handles all of the hardware interactions necessary to send and receive frames.
- It deals with all of the timeouts and timings required by the LLAP protocol.

Z80181 LLAP Driver Resource Usage And Hardware Requirements

- Approximately 4.5 Kbytes of program memory (ROM or RAM) written partly in Z181 assembler and in ANSI C (Microtec).
- Approxiamtely 128 bytes of data memory (RAM).
- TxD and RxD of the Z181's SCC are connected to the RS-422 differential drivers.
- The /REQ pin from the Z181's SCC is connected to the Z181 DMA's /DREQ1.
- A 3.6864 MHz crystal is attached to the RTxC and SYNC pins for LLAP clocking.
- The Z181 uses a 10.0 MHz clock
- Memory access requires no added wait states.

KIT CONTENTS

Software

Z181 LLAP Driver Source Code Diskette
(licensing agreement required)

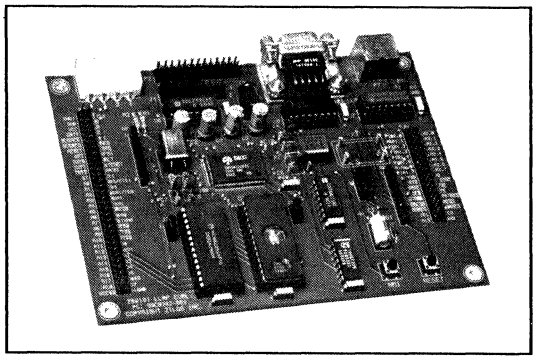
Documentation

User Guide, LLAP Driver for the Z181
Design, LLAP Driver for the Z181

ORDERING INFORMATION

Part No: Z8018101ZA6

Z8018101ZCO
PRODUCT SPECIFICATION



DESCRIPTION

The kit contains assembled circuit boards support hardware, and documentation to support AppleTalk®'s LocalTalk™ Link Access Protocol (LLAP) on Zilog's Z181™ (Z80181) .

The purpose of the Z181 LLAP Evaluation Board is to demonstrate one possible hardware configuration when implementing LLAP on the Z181 (Z8018101ZA6)and to provide a platform from which to execute example LLAP application programs. A diagnostic program (demo.c) is included with the kit. This program tests the RTS and CTS hand shake between two Z8018101ZCO boards by transmitting data between them. This demo requires two terminals interfaced via the RS-232C ports to the Z8018001ZCO boards.

A second example LLAP application program (mainecho.c) allows the board to transmit and receive LLAP packets to another board. The user can then observe the transactions with his LLAP network analyzer. Although the example application program does not execute the higher layers of the AppleTalk stack, its inclusion in the kit does demonstrate that the LLAP packets adhere to LLAP specifications. The example application program also provides the user with a model on which to base the user's own application program.

Power Requirements
+5 Vdc @ 0.50A

Dimensions
Width: 4.4 in.
Length: 5.8 in.

Serial Interfaces
RS-232C
RS-422 LocalTalk DIN-8 and DB-9 interface

Z80181 LLAP Driver Resource Usage And Hardware Requirements

- Approximately 4.5 Kbytes of program memory (ROM or RAM) written partly in Z181 assembler and in ANSI C (Microtec).
- Approxiamtely 128 bytes of data memory (RAM).
- TxD and RxD of the Z181's SCC are connected to the RS-422 differential drivers.
- The /REQ pin from the Z181's SCC is connected to the Z181 DMA's /DREQ1.
- A 3.6864 MHz crystal is attached to the RTxC and SYNC pins for LLAP clocking.
- The Z181 uses a 10.0 MHz clock
- Memory access requires no added wait states.

KIT CONTENTS

Two Z8018101ZCO LLAP Evaluation Boards, each has:
- CMOS Z181 MPU @ 10MHz
- 20 MHz Crystal (for MPU)
- 3.6864 MHz Crystal (for LLAP)
- Socketed 32K x 8 EPROM (containing demo.c)
- Socketed 32K x 8 Static RAM
- RS-232C Interface
- RS-422 Interface for LocalTalk DIN-8 or DB-9 connection
- Z181 MPU Expansion Header
- Z181 Peripheral Expansion Header
- Reset switch
- NMI switch

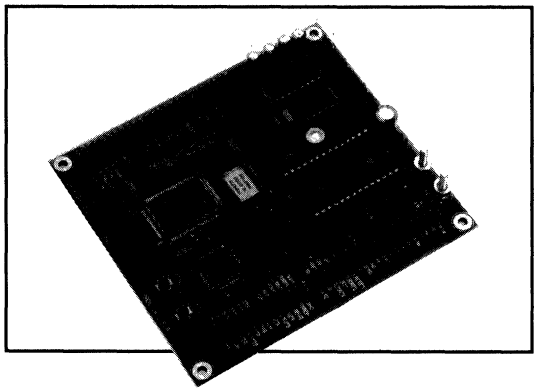
Hardware
Two unsocketed 32K X 8 EPROMs containing mainecho.c
Two LocalTalk DB-9 connection modules
Two power supply cables
Two DB-25 connectors

Documentation
User Guide, LLAP Driver for the Z181
Design, LLAP Driver for the Z181
Z181 Product Specification
Z85C30 Product Specification

ORDERING INFORMATION

Part No: Z8018101ZCO

Z84C1100ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z84C11, Z84C43

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z84C11 and Z84C43 devices.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .36 A

Dimensions
Width: 4.5 in. (8.9 cm)
Length: 4.0 in. (10.2 cm)

Serial Interface
RS-232C @ 9600 baud

KIT CONTENTS
Z84C11 Evaluation Board
CMOS Z84C11 MPU
CMOS Z84C43 SIO
19.6608 Mhz Crystal
Socketed (32K)/8K x 8 EPROM
(supplied with Debug Monitor EPROM)
Socketed (32K)/8K x 8 Static RAM
RS-232C PC Interface
Z80 signal Expansion Header
Z84C11 I/O signal Expansion Header
Reset switch
Nmi switch

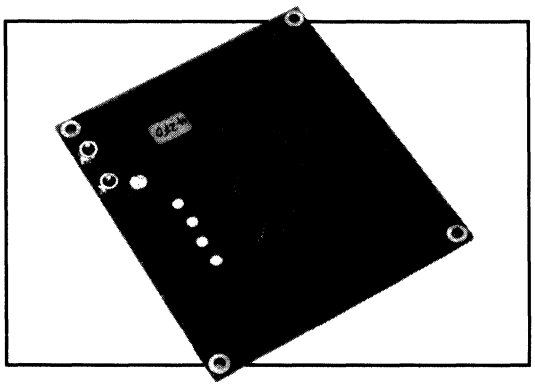
Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code

Documentation
Z84C11 Kit User Guide
Z84C11 Product Specification
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z84C1100ZCO

Z84C1500ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z84C15

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z84C15 device.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .39 A

Dimensions
Width: 3.9 in. (8.9 cm)
Length: 3.5 in. (10.2 cm)

Serial Interface
RS-232C @ 9600 baud

KIT CONTENTS
Z84C15 Evaluation Board
CMOS Z84C15 MPU
19.6608 MHz Crystal
Socketed (32K)/8K x 8 EPROM
(programmed with Debug Monitor)
Socketed (32K)/8K x 8 Static RAM
RS-232C PC Interface
Z80® MPU Signal Expansion Header
Z84C15 I/O Expansion Header
Reset switch
Nmi switch

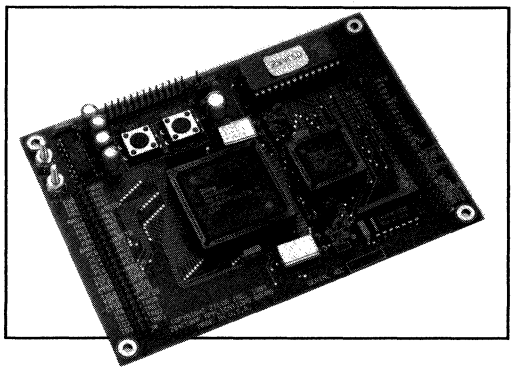
Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8®/Z80/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code

Documentation
Z84C15 Kit User Guide
Z84C15 Product Specification
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z84C1500ZCO

Z84C5000ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z84C50, Z84C90

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z84C50 and Z84C90 devices.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .47 A

Dimensions
Width: 5.5 in. (8.9 cm)
Length: 4.0 in. (10.2 cm)

Serial Interface
RS-232C @ 9600 baud

KIT CONTENTS
Z84C50 Evaluation Board
CMOS Z84C50 MPU
CMOS Z84C90 KIO™ IC
8 MHz Crystal
(32K)/8K x 8 EPROM
(programmed with Debug Monitor)
RS-232C PC Interface
Z84C90 Signal Expansion Header
Z84C50 Signal Expansion Header
Reset switch
Nmi switch

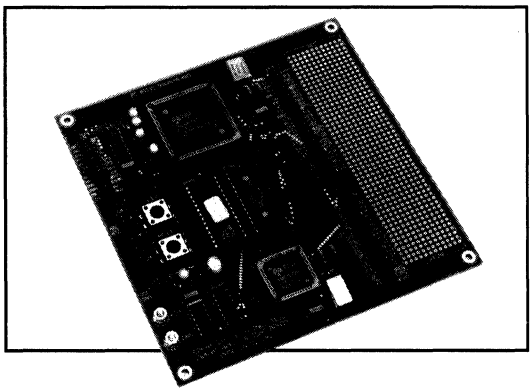
Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code
Example Software

Documentation
Z84C50 Kit User Guide
Z84C50 Product Specification
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z84C5000ZCO

Z84C9000ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z84C01, Z84C90

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z84C01 MPU and Z84C90 KIO™ devices.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

Code targeted for the Z84C01 and/or Z84C90 device may be verified for the target application before prototype build.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .45 A

Dimensions
Width: 6.0 in. (8.9 cm)
Length: 6.0 in. (10.2 cm)

Serial Interface
RS-232C @ 9600 baud

KIT CONTENTS
Z84C90 Evaluation Board
CMOS Z84C01 MPU
CMOS Z84C90 KIO™ IC
8 MHz Crystal
Sockted (32K)/8K x 8 EPROM
(programmed with Debug Monitor)
Socketed (32K)/8K x 8 Static RAM
RS-232C PC Interface
Z84C90 Signal Expansion Header
Z84C01 Signal Expansion Header
Bread Board Area
Reset switch
Nmi switch

Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code
Example Software

Documentation
Z84C90 Kit User Guide
Intelligent Peripheral Controllers Data Book
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z4C9000ZC0

ZEPMIP00001
PRODUCT SPECIFICATION

SUPPORTED DEVICES
Z8S180/Z180, Z80181/Z181

DESCRIPTION
The EPM™ Electronic Programmer's Manual provides on-line documentation on Zilog's Microprocessor Unit Z8S180/Static Z180™ and Z80181/Z181™ register sets and device operation. Its code generation features make it a most valuable tool for the pro-grammer. The EPM Manual helps you set the registers to ensure that the device operates with your specified settings. Once you have selected the field values as a series of C function calls, or as an assembler table, you can include this output in any software that utilizes the device.

SPECIFICATIONS
Minimum Hardware Requirements
IBM® PC/AT with available 512K RAM
5.25 inch, high density, or 3.5 inch,
high density floppy disk drive
Hard disk drive
Color monitor

Minimum Operating System
MS-DOS, version 3.0 or later

KIT CONTENTS
Software (IBM® PC Platform)
2 EPM Floppy Diskettes: 5.25 inch,
high density and 3.5 inch, high density

Documentation
EPM User's Guide
Z80180/Z180 Technical Manual
Z80181/Z181 Preliminary Product Spec.
Z8030/Z8530 SCC Technical Manual
EPM Registration Reply Card

ORDERING INFORMATION
Part No: ZEPMIP00001

ZEPMIP00002
PRODUCT SPECIFICATION

SUPPORTED DEVICES
Z80182

DESCRIPTION
The EPM™ Electronic Programmer's Manual provides on-line documentation on Zilog's Microprocessor Unit Z80182 register sets and device operation. Its code generation features make it a most valuable tool for the programmer. The EPM Manual helps you set the registers to ensure that the device operates with your specified settings. Once you have selected the field values as a series of C function calls, or as an assembler table, you can include this output in any software that utilizes the device.

SPECIFICATIONS
Minimum Hardware Requirements
IBM® PC/AT with available 512K RAM
3.5 inch or 5.25 inch, high density floppy disk drive
Hard disk drive
Color monitor

Minimum Operating System
MS-DOS, version 3.0 or later

KIT CONTENTS
Software (IBM® PC Platform)
2 EPM Floppy Diskettes: high density 3.5" and 5.25" inch

Documentation
EPM User's Guide
Z80180/Z180 Technical Manual
Z80182 Preliminary Product Spec.
Z8030/Z8530 SCC Technical Manual
EPM Registration Reply Card

ORDERING INFORMATION
Part No: ZEPMIP00002

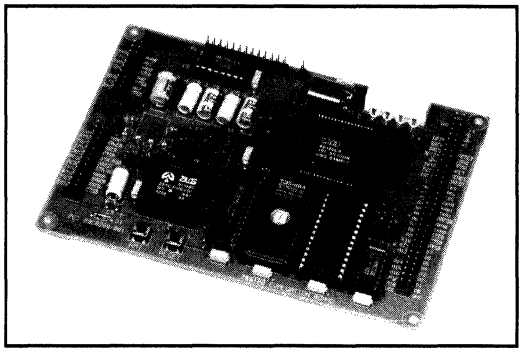
Datacom

Part-To-Kit Cross Reference Matrix

	Z8S18000ZCO	Z80181OOZCO	Z80181O1ZCO*	Z8523000ZCO	Z16C3001ZCO	Z8018600ZCO	ZEPMDC00001	ZEPMDC00002
Z8030						●		●
Z8530				●		●		●
Z80C30						●		●
Z85C30		●	●	●		●		●
Z80230						●		●
Z85230	●			●		●		●
Z85233				●†		●		●
Z16C30					●	●	●	
Z16C32						●	●	
Z16C33					●	●	●	
Z16C35						●		

* Includes LLAP software that can be licensed.
† Software modifications needed.

Z8S18000ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8S180, Z85230

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z8S180 and Z85230 system at 18.432 MHz.

The supplied cross assembler and link/loader package allows full assembly language programming support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

The board comes with sample code to illustrate the use of Zilog's Z8S180 and Z85230 in a variety of communication applications.

SPECIFICATIONS
Power Requirements
+5Vdc @ 5A

Dimensions
Width: 5.65 in.
Length: 4.0 in.

Serial Interface
RS-232 @ 9600 baud

KIT CONTENTS
Z8S180/ESCC Evaluation Board
CMOS Z8S180 MPU
18.432 MHz Crystal
Socketed 64K/(8K) x 8 EPROM
(Programmed with Debug Monitor and Device Driver Demonstration Software)
Socketed 32K/(8K) x 8 Static RAM
RS-232C PC Interface
Z8S180 Expansion Header
Z85230 Expansion Header
Reset Switch
NMI Switch

Cables
25-pin RS-232 Cable

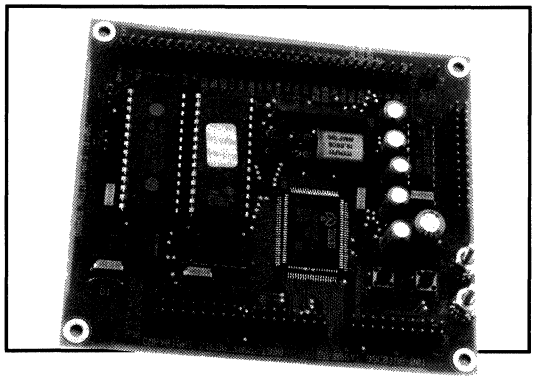
Software (IBM® PC Platform)
ASM800 Z800 Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor and
Device Drivers Demonstration
Software Source Code
Z8S180 Example Software
(a) In ASM800 Assembly
(b) In Microtec MCC80 C and
Microtec ASM80 Assembly

Note: Zilog is not responsible for support and maintenance of the above software.

Documentation
Z8S180/ESCC Kit User Guide
Z80180/Z8S180 Product Specification
Z80180/Z180 Technical Manual
Z85230 Product Specification
Z85230/Z80230 Technical Manual
ASM800 Z800 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z8S18000ZCO

Z8018100ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z80181

DESCRIPTION
The kit contains an assembled circuit board, software and documentation to support software and hardware development for the Z80181 device.

The supplied cross assembler and link/loader package allows full assembly language support. A board resident debug monitor program allows executable code to be down-loaded and subsequently debugged.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .65 A

Dimensions
Width: 3.65 in. (9.27 cm)
Length: 4.20 in. (10.67 cm)

Serial Interface
RS-232C @ 9600 bits/sec.

KIT CONTENTS
Z180181 Evaluation Board
CMOS Z80181 MPU
19.6608 MHz Crystal
Socketed (32K) /8K x 8 EPROM
(Programmed with Debug Monitor)
Socketed (32K) /8K x 8 Static RAM
RS-232C Interface
Z80181 MPU Expansion Header
Z80181 Peripheral Signal
Expansion Header
Reset switch
Nmi switch

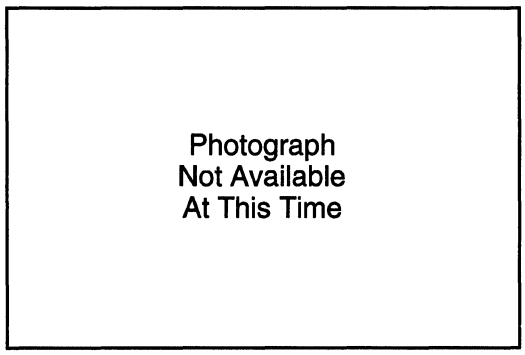
Cables
25-Pin RS-232 Cable

Software (IBM® PC Platform)
Z8®/Z80®/Z8000® Cross Assembler
MOBJ Link/Loader
Resident Debug Monitor Source Code
Z80181 Example Software

Documentation
Z80181 Kit User Guide
Z80181 Product Specification
Z8030/8530 Technical Manual
Z80 Cross Assembler User Guide
MOBJ Link/Loader User Guide

ORDERING INFORMATION
Part No: Z8018100ZCO

Z8018101ZA6
PRODUCT SPECIFICATION



DESCRIPTION

The kit contains software and documentation to support AppleTalk® LocalTalk™ Link Access Protocol (LLAP) on Zilog's Z181™ (Z80181).

The Z8018101ZA6 LLAP driver requires a software licensing agreement. The driver is written in ANSI Microtec C and partly in Z181 Assembler, all contained in diskettes to be executed using an IBM® PC and a Microtec C compiler. The driver is composed of a series of C function calls that allows the Z181 (in conjunction with proper LLAP hardware interface, e.g., Z8018101ZCO) to transmit and receive LLAP packets. The lower level transmission and reception routines are finely tuned using Z181 assembler codes. Interface of Zilog's LLAP driver to AppleTalk®'s upper layer is left for the user.

Two examples using the Z181 LLAP driver are included. "Demo.c" tests the RTS and CTS handshake between two Z8018101ZCO boards by transmitting data between them. This demo requires two terminals interfaced via the RS-232C ports to the Z8018101ZCO boards. "Mainecho.c" allows two Z8018101ZCO boards to transmit and receive LLAP packets. The user can then observe the transactions with his LLAP network analyzer. Although this example application program does not execute the higher layers of the AppleTalk stack, its inclusion demonstrates that the LLAP packets adhere to LLAP specifications. The example application programs also provide the user with models on which to base his own application program. Source codes and documentations are included in the kit.

Z80181 LLAP Driver Description

The kit contains source code and documentation (User Guide, LLAP Driver for the Z181 and Design, LLAP Driver for the Z181) for the Z181 LocalTalk Link Access Protocol Driver. The User Guide, LLAP Driver for the Z80181 describes the Zilog-provided driver for the Z181 and explains how the driver is to be used. The Design, LLAP Driver for the Z181 explains how the driver works.

The kit is intended for users who wish to interface an AppleTalk node to a LocalTalk network using the Z181. Interface to the upper layers of the AppleTalk stack varies from user to user and is not addressed in the documentation. The documentation does provide a general overview of the ways the Z181 LLAP driver is intended to fit in a larger software system.

In general, the Z181 LLAP Driver implements the LLAP protocol described in Inside AppleTalk by Sidhu et.al. In particular, the driver performs the following functions:

- It establishes its own node address by transmitting ENQ frames as required.
- It responds to a received ENQ frame with an appropriate ACK frame.
- It responds to a received RTS frame with an appropriate CTS frame.
- It receives any data frames addressed to the node or to the broadcast address and routes them according to given instructions.
- It transmits an RTS frame before sending a broadcast data frame.
- It transmits an RTS frame and waits for a CTS frame in response before sending a non-broadcast data frame. It retries as necessary.
- It handles all of the hardware interactions necessary to send and receive frames.
- It deals with all of the timeouts and timings required by the LLAP protocol.

Z80181 LLAP Driver Resource Usage And Hardware Requirements

- Approximately 4.5 Kbytes of program memory (ROM or RAM) written partly in Z181 assembler and in ANSI C (Microtec).
- Approxiamtely 128 bytes of data memory (RAM).
- TxD and RxD of the Z181's SCC are connected to the RS-422 differential drivers.
- The /REQ pin from the Z181's SCC is connected to the Z181 DMA's /DREQ1.
- A 3.6864 MHz crystal is attached to the RTxC and SYNC pins for LLAP clocking.
- The Z181 uses a 10.0 MHz clock
- Memory access requires no added wait states.

KIT CONTENTS

Software

Z181 LLAP Driver Source Code Diskette
(licensing agreement required)

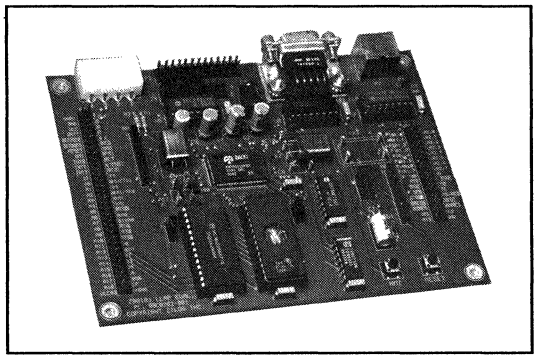
Documentation

User Guide, LLAP Driver for the Z181
Design, LLAP Driver for the Z181

ORDERING INFORMATION

Part No: Z8018101ZA6

Z8018101ZCO
PRODUCT SPECIFICATION



DESCRIPTION

The kit contains assembled circuit boards support hardware, and documentation to support AppleTalk®'s LocalTalk™ Link Access Protocol (LLAP) on Zilog's Z181™ (Z80181) .

The purpose of the Z181 LLAP Evaluation Board is to demonstrate one possible hardware configuration when implementing LLAP on the Z181 (Z8018101ZA6)and to provide a platform from which to execute example LLAP application programs. A diagnostic program (demo.c) is included with the kit. This program tests the RTS and CTS hand shake between two Z8018101ZCO boards by transmitting data between them. This demo requires two terminals interfaced via the RS-232C ports to the Z8018001ZCO boards.

A second example LLAP application program (mainecho.c) allows the board to transmit and receive LLAP packets to another board. The user can then observe the transactions with his LLAP network analyzer. Although the example application program does not execute the higher layers of the AppleTalk stack, its inclusion in the kit does demonstrate that the LLAP packets adhere to LLAP specifications. The example application program also provides the user with a model on which to base the user's own application program.

Power Requirements

+5 Vdc @ 0.50A

Dimensions

Width: 4.4 in.
Length: 5.8 in.

Serial Interfaces

RS-232C
RS-422 LocalTalk DIN-8 and DB-9 interface

Z80181 LLAP Driver Resource Usage And Hardware Requirements

- Approximately 4.5 Kbytes of program memory (ROM or RAM) written partly in Z181 assembler and in ANSI C (Microtec).
- Approxiamtely 128 bytes of data memory (RAM).
- TxD and RxD of the Z181's SCC are connected to the RS-422 differential drivers.
- The /REQ pin from the Z181's SCC is connected to the Z181 DMA's /DREQ1.
- A 3.6864 MHz crystal is attached to the RTxC and SYNC pins for LLAP clocking.
- The Z181 uses a 10.0 MHz clock
- Memory access requires no added wait states.

KIT CONTENTS

Two Z8018101ZCO LLAP Evaluation Boards, each has:
- CMOS Z181 MPU @ 10MHz
- 20 MHz Crystal (for MPU)
- 3.6864 MHz Crystal (for LLAP)
- Socketed 32K x 8 EPROM (containing demo.c)
- Socketed 32K x 8 Static RAM
- RS-232C Interface
- RS-422 Interface for LocalTalk DIN-8 or DB-9 connection
- Z181 MPU Expansion Header
- Z181 Peripheral Expansion Header
- Reset switch
- NMI switch

Hardware

Two unsocketed 32K X 8 EPROMs containing mainecho.c
Two LocalTalk DB-9 connection modules
Two power supply cables
Two DB-25 connectors

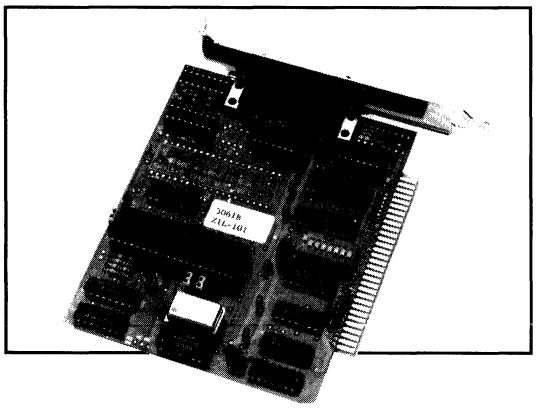
Documentation

User Guide, LLAP Driver for the Z181
Design, LLAP Driver for the Z181
Z181 Product Specification
Z85C30 Product Specification

ORDERING INFORMATION

Part No: Z8018101ZCO

Z8523000ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8530, Z85C30, Z85230

DESCRIPTION
The kit contains an assembled PC/XT/AT circuit board with one high speed serial port, selectively driven by RS-232C or RS-422 line drivers. The kit also contains software and documentation to support software and hardware development for Zilog's ESCC™ device.

The board illustrates the use of Zilog's ESCC in a variety of communication applications such as SDLC/HDLC, and high speed ASYNC.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .5 A

Dimensions
Width: 4 in. (10.16 cm)
Length: 5 in. (12.70 cm)

Serial Interface
A DB25 port selectively driven by RS-232C or RS-422 at selectable baud rates.

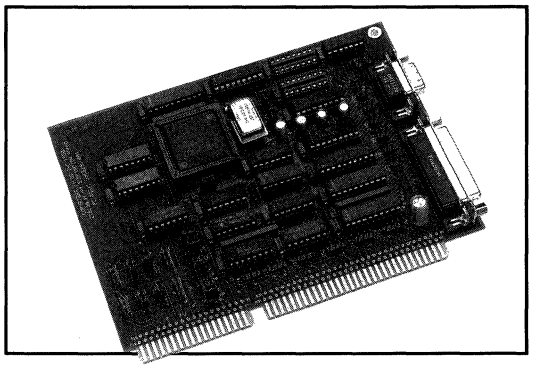
KIT CONTENTS
Z85230 Evaluation Board
CMOS Z85230 ESCC
RS-232C and RS-422 line drivers
DB25 connector

Software (IBM® PC Platform)
Source and executable codes to run the ESCC in SDLC/HDLC and ASYNC modes using DMA, Interrupt and polling methods. All codes are written in C and compiled using the Microsoft® Quick C compiler.

Documentation
Z85230 Product Specifications
Z85230 Technical Manuals
Z8523000ZCO User Guide
Sealevel™ User's Manual

ORDERING INFORMATION
Part No: Z8523000ZCO

Z16C3001ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z16C30, Z16C33

DESCRIPTION
The kit contains an assembled PC/XT/AT circuit board with two high-speed serial connections, DB9 and DB25 connectors selectively driven by RS-232 or RS-422 line drivers. The kit also contains software and documentation to support software and hardware development for Zilog's USC™ and MUSC™ devices.

The board illustrates the use of Zilog's USC and MUSC devices in a variety of communication applications such as ASYNC, SDLC/HDLC and high-speed ASYNC.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .5 A

Dimensions
Width: 4.5 in. (11.43 cm)
Length: 6.5 in. (16.51 cm)

Serial Interface
DB9 and DB25 connectors selectively driven by RS-232C or RS-422 at
selectable baud rates.

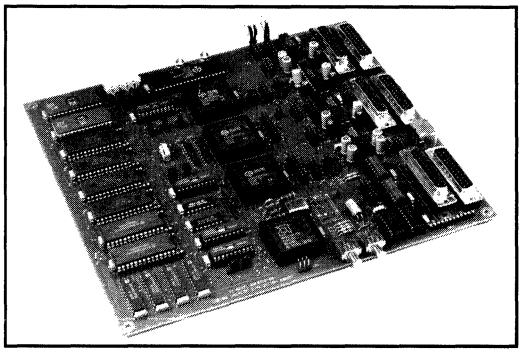
KIT CONTENTS
Z16C30/Z16C33 Evaluation Board
CMOS Z16C30 USC and Z16C33 MUSC
RS-232C and RS-422 line drivers
DB9 and DB25 Interfaces

Software (IBM® PC Platform)
Source and executable codes to run the USC or MUSC in SDLC/HDLC or ASYNC mode. All codes are written and compiled using Microsoft® Quick C 2.5.

Documentation
Z16C30 and Z16C33 Product Specifications
Z16C30/Z16C33 Technical Manual
Z16C3001ZCO Kit User Guide

ORDERING INFORMATION
Part No: Z16C3001ZCO

Z8018600ZCO
PRODUCT SPECIFICATION



SUPPORTED DEVICES
Z8X30, Z85230, Z85233, Z16C32, Z8XC30, Z16C33, Z16C30

DESCRIPTION
The kit contains an assembled circuit board, software, and documentation to support the evaluation and development of code for Zilog's Z85C30 SCC, Z85230 ESCC™, Z85233 EMSCC™, Z16C30 USC™, Z16C32 IUSC™, Z16C33 MUSC™, and the Z16C35 ISCC™. The purpose of the board is to illustrate how the datacom family interfaces and communicates with the 80186 CPU. This will help potential customers evaluate Zilog's data com-munication controllers in an Intel® environment. A board-resident monitor program allows code to be downloaded and executed.

SPECIFICATIONS
Power Requirements
+5 Vdc @ .50A

Dimensions
Width: 8.4 in. (21.34 cm)
Length: 9.3 in. (23.62 cm)

Serial Interfaces
RS-232C, RS-422

KIT CONTENTS
Z8018600ZCO Evaluation Board
Intel 80186 Integrated 16-bit MPU @ 16 MHz
CMOS Z85230 ESCC
CMOS Z16C30 USC
CMOS Z16C32 IUSC
CMOS Z16C35 ISCC
2 (64K) 8Kx8 EPROMs
6 (256K) 32Kx8 SRAMs
RS-232C, RS-422, and Apple® LocalTalk™ line drivers
DB9, DB25, and DIN 8 Interfaces

Cables
1 25-pin RS-232C Cable
14 Jumper Wires

Software (IBM® PC Platform)
Resident Monitor for download and execution (80186 Assembler source code)
PC-board terminal emulator
Z85230, Z16C30/33, Z16C32, and Z16C35 Examples Software (All codes written in "C" and compiled using the Microtec® C compiler.)

Documentation
Z85230 ESCC Product Specification and Technical Manual
Z16C30/33 (M)USC Product Specification and Technical Manual
Z16C32 IUSC Product Specification and Technical Manual
Z16C35 ISCC Product Specification and Technical Manual
Datacom Evaluation Board Application Note

ORDERING INFORMATION
Part No: Z8018600ZCO

ZEPMDC00001
PRODUCT SPECIFICATION

SUPPORTED DEVICES
Z16C30, Z16C32, Z16C33

DESCRIPTION
The EPM™ Electronic Programmer's Manual provides on-line documentation on Zilog's USC™ Universal Serial Communicatons Controller (Z16C30), MUSC™ Mono-Universal Serial Controller (Z16C33), and the IUSC™ Integrated Universal Serial Controller (Z16C32) register sets and device operation. Its code generation features make it a most valuable tool for the programmer. The EPM helps you set the registers to ensure that the device operates with your specified settings. Once you have selected the field values as a series of C function calls, or as an assembler table, you can include this output in any software that utilizes the device.

SPECIFICATIONS
Minimum Hardware Requirements
IBM PC/AT with available 512K RAM
5.25 inch, high density, or 3.5 inch,
high density floppy disk drive
Hard disk drive
Color monitor

Minimum Operating System
MS-DOS, version 3.0 or later

KIT CONTENTS
Software (IBM® PC Platform)
2 EPM Floppy Diskettes: 5.25 inch,
high density and 3.5 inch, high density

Documentation
EPM User's Guide
USC/MUSC Technical Manual
IUSC Technical Manual
EPM Registration Reply Card

ORDERING INFORMATION
Part No: ZEPMDC00001

ZEPMDC00002
PRODUCT SPECIFICATION

SUPPORTED DEVICES
Z8X30, Z8XC30, Z8X230, Z16C35

DESCRIPTION
The EPM™ Electronic Programmer's Manual provides on-line documentation on Zilog's Serial Communicatons Controller family of devices (Z08X30 NMOS SCC, Z8XC30 CMOS SCC, Z8X230 ESCC, Z16C35 ISCC™ controller): register set and operation of the device. Its code generation features make it a most valuable tool for the programmer. The EPM Manual helps you set the registers to ensure that the device operates with your specified settings. Once you have selected values for the registers, the EPM Manual lets you save the field values as a series of C function calls or as an assembler table. You can include this output in any software that utilizes the device.

SPECIFICATIONS
Minimum Hardware Requirements
IBM® PC/AT with available 512K RAM
5.25 inch, high density, or 3.5 inch,
high density floppy disk drive
Hard disk drive
Color monitor

Minimum Operating System
MS-DOS, version 3.0 or later

KIT CONTENTS
Software (IBM® PC Platform)
2 EPM Floppy Diskette: 5.25 inch,
high density and 3.5 inch, high density

Documentation
EPM User's Guide
SCC Technical Manual
ESCC Technical Manual
ISCC Technical Manual
EPM Registration Reply Card

ORDERING INFORMATION
Part No: ZEPMDC00002

Zilog's Quality and Reliability Program

Introduction

Zilog Inc. has an excellent reputation for the quality and reliability of its products.

Zilog's Quality and Reliability Program is based on careful study of the principles laid down by such pioneers as W.E. Deming and J.M. Juran, but even more importantly, the observation and practical implementation of those principles as practiced in Japanese, European and American manufacturing facilities.

The Zilog program begins with employee involvement. Whether the judgement of our performance is based on perfection with incoming inspection, trouble-free service in the field, or timely and accurate customer service, we recognize that our employees ultimately control these factors. Hence, our Quality Program is broadly shared throughout the organization.

1. Harmony Between Design and Process

High product quality and reliability in VLSI products are possible only if there is structural harmony between product design and manufacturing. Great care is taken to ensure that the statistical process control limits observed within the manufacturing plants properly guardband the design technology used to configure the circuit and layout in Zilog's automated design methodology.

Through use of a technique which we call Process Templating, the technology file in the automated design system is periodically updated to ensure that product design parameters fall within the statistical control limits with which the process is actually operated. In simple terms, the Process Template is the profile displayed by the process evaluation parameters which are automatically recorded from the test patterns on wafers as they proceed through the production line. These parameters are translated into the design technology file attributes so every product design technology file attributes bears a key and lock relationship to the process.

2. Training

The integrity of our product design and manufacturing process depends on the skills of our employees. Zilog training emphasizes the fundamentals involved in product design and processing for quality and reliability.

Customer Service, an important aspect of Zilog's quality performance as a vendor, also depends upon our people clearly understanding their jobs, and our obligations to our customers. This too is part of the training curriculum administered by Zilog.

3. Order Acknowledgement Policy

One definition of vendor quality performance is that the vendor "does what he promises or acknowledges." Reliability and quality warranties are met only if Zilog and the customer are in agreement on product and delivery specifications. Zilog makes an extra effort to ensure that the customer is fully informed by providing documents with its purchase order acknowledgements that clearly state what Zilog understands the specifications to be.

4. Test Guardbanding

No physical attribute is absolute. Customers' test methods may differ from Zilog's due to variations in test equipment, temperature or specification interpretation. To ensure that every Zilog product performs to full customer expectations, Zilog uses a "waterfall" methodology in its testing. The first electrical tests made on the circuit, at the wafer probe operation, are guardbanded to the final test specifications. The final test specifications, in turn, are guardbanded to the quality control outgoing sample. The quality control outgoing sample is guardbanded to the customer procurement or data sheet specifications. This technique of "waterfall" guardbanding ensures that circuits which may be marginal to the customer's expectations are eliminated in the manufacturing process long before they get to the shipping container.

5. Probe at Temperature

Semiconductor devices tend to exhibit their most limited performance at the highest operating temperature. Therefore, it is Zilog's policy that all chips are tested at high temperature the very first time they are electrically screened, at the wafer probe station. The circuits are tested again at their upper operating temperature limit in the 100% final test operation.

6. Process Characterization

Before release to production, every process is thoroughly characterized by an exhaustive series of pilot production runs and tests which identify the statistical, electrical, and mechanical limits of which that particular process regime is capable. This documentation, which fills a large loose-leaf binder for each process, is maintained as the historical record or "footprint" for that particular regime.

Process recharacterization is done any time there is a major process or manufacturing site change, and the resulting documentation is then added to the characterization history. Once the process is fully characterized, the frequent test site evaluation and process template data demonstrate that the process remains in specification.

7. Product Characterization

Every Zilog product design is evaluated over extremes of operating temperature, supply voltage and clock frequencies, prior to production release. This information permits the proper guardbanding of the test program waterfall and identification of any marginal "corners" in design tolerances.

A product characterization report, which summarizes the more important tolerances identified in the process of this exhaustive product design evaluation, is available to Zilog's customers.

8. Process Qualification

Zilog also qualifies every process prior to production by an exhaustive stress sequence performed on test chips and on representative products. Once a process regime is qualified, a process requalification is performed any time there is a major process change, or whenever the process template statistical quality limits are significantly exceeded or adjusted.

9. Product Qualification

In addition to characterization, every new Zilog product design is fully qualified by a comprehensive series of life, electrical, and environmental tests before release to production. Again, a qualification report is available to our customers which summarizes certain key life and environmental data taken in the course of these evaluations. Whenever possible, industry standard environmental and life tests are employed.

10. PPM Measurement, Direct and Indirect

It is frequently said that if you want to improve something, you need to put a measure on it. Therefore, Zilog measures its outgoing quality "parts per million" by the maintenance of careful records on the statistical sampling of production lots prepared for shipment. This information is then translated by our statisticians to a statement of our parts per million (or parts per billion) outgoing quality performance.

Of course, it is one thing for Zilog to think it is doing a good job in outgoing product quality and it is another for a customer to agree. Therefore, we ask certain key customers to provide us with their incoming inspection data which helps us calibrate our outgoing performance in terms of the actual results in the field. The fact that Zilog has been awarded "ship to stock" status by many customers testifies to our success in this area.

11. FIT Measurement Direct and Indirect

Just as Zilog records its outgoing quality in terms of parts per million, it also measures its outgoing product reliability in terms of "FITS" or failures per billion device hours, using the results of weekly operating life test measurements on the circuits, performed in accordance with standard specifications.

12. Field Quality Engineers

It is frequently said that the customer is always right. If the customer has an application quality or reliability problem while using a Zilog product, whether it is Zilog's responsibility or not, we believe that we have a responsibility to resolve it. Therefore, Zilog maintains a force of skilled Applications Engineers who are also trained as field quality engineers and are available on immediate call to consult at the customer's locations on any problems they may be experiencing with Zilog product performance.

13. Product Analysis

As noted earlier, we feel that a customer problem is a Zilog problem. Accordingly, Product Analysis facilities, staffed by experienced professionals, exist at each Zilog site to provide rapid evaluation of in-process and in-field rejects to determine the cause and provide corrective action through a feedback loop into the production, design, and applications process. Zilog is pleased to share product analysis reports on specific products with the customer upon request.

14. Test Site Step-Stress

The process evaluation test sites on the wafer are packaged and subjected to step-stress testing. Any drift in parameters under severe conditions of stress outside the norm is taken as an indication of possible process contamination or variation.

15. Statistical Process Control

Zilog employs Statistical Process Control at all critical process steps. Deviations from norms must be evaluated by a Q/R review board.

16. Perfection Plus Program

Zilog employees actively participate in meetings where methods are proposed, reviewed, and adopted and which enable a department to do its job in more of a precise and accurate manner. Employees who have made suggestions proudly wear the Zilog Perfection Plus pin.

17. Zilog Vendor of the Year Award

Zilog is proud of the many quality and performance awards it has received from its customers. In turn, Zilog makes an annual award to the vendor who has done the best overall job for Zilog.

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Arrow Electronics ..... (918)252-7537
Hall-Mark Electronics ..... (918)254-6110

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Anthem Electronics ..... (503)643-1114
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Nordqvist & Berg AB 010-46-87646710

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Dietikon
EBV Elektronik GMBH 41-1-7401090
Regensdorf
Moor AG 41-1-8433111

Z8®/SUPER8™ MICROCONTROLLER FAMILY

Databook	Part No	Unit Cost
Z8 Microcontrollers Databook (includes the following documents)	DC-8275-04	5.00

Z8 CMOS Microcontrollers

Z86C00/C10/C20 MCU OTP Product Specification
Z86C06 Z8 CCP™ Preliminary Product Specification
Z86C08 8-Bit MCU Product Specification
Z86E08 Z8 OTP MCU Product Specification
Z86C09/19 Z8 CCP Product Specification
Z86E19 Z8 OTP MCU Advance Information Specification
Z86C11 Z8 MCU Product Specification
Z86C12 Z8 ICE Product Specification
Z86C21 Z8 MCU Product Specification
Z86E21/Z86E22 OTP Product Specification
Z86C30 Z8 CCP Product Specification
Z86E30 Z8 OTP CCP Product Specification
Z86C40 Z8 CCP Product Specification
Z86E40 Z8 OTP CCP Product Specification
Z86C27/97 Z8 DTC™ Product Specification
Z86127 Low-Cost Digital Television Controller Adv. Info. Spec.
Z86C50 Z8 CCP ICE Advance Information Specification
Z86C61 Z8 MCU Advance Information Specification
Z86C62 Z8 MCU Advance Information Specification
Z86C89/C90 CMOS Z8 CCP Product Specification
Z86C91 Z8 ROMless MCU Product Specification
Z86C93 Z8 ROMless MCU Preliminary Product Specification
Z86C94 Z8 ROMless MCU Product Specification
Z86C96 Z8 ROMless MCU Advance Information Specification
Z88C00 CMOS Super8 MCU Advance Information Specification

Z8 NMOS Microcontrollers

Z8600 Z8 MCU Product Specification
Z8601/03/11/13 Z8 MCU Product Specification
Z8602 8-Bit Keyboard Controller Preliminary Product Spec.
Z8604 8-Bit MCU Product Specification
Z8612 Z8 ICE Product Specification
Z8671 Z8 MCU With BASIC/Debug Interpreter Product Spec.
Z8681/82 Z8 MCU ROMless Product Specification
Z8691 Z8 MCU ROMless Product Specification
Z8800/01/20/22 Super8 ROMless/ROM Product Specification

Peripheral Products

Z86128 Closed-Captioned Controller Adv. Info. Specification
Z765A Floppy Disk Controller Product Specification
Z5380 SCSI Product Specification
Z53C80 SCSI Advance Information Specification

Z8 Application Notes and Technical Articles

Zilog Family On-Chip Oscillator Design
Z86E21 Z8 Low Cost Thermal Printer
Z8 Applications for I/O Port Expansions
Z86C09/19 Low Cost Z8 MCU Emulator
Z8602 Controls A 101/102 PC/Keyboard
The Z8 MCU Dual Analog Comparator
The Z8 MCU In Telephone Answering Systems
Z8 Subroutine Library
A Comparison of MCU Units
Z86xx Interrupt Request Registers
Z8 Family Framing
A Programmer's Guide to the Z8 MCU
Memory Space and Register Organization

Super8 Application Notes and Technical Articles

Getting Started with the Zilog Super8
Polled Async Serial Operations with the Super8
Using the Super8 Interrupt Driven Communications
Using the Super8 Serial Port with DMA
Generating Sine Waves with Super8
Generating DTMF Tones with Super8
A Simple Serial Parallel Converter Using the Super8

Additional Information

Z8 Support Products
Zilog Quality and Reliability Report
Literature List
Package Information
Ordering Information

Z8®/SUPER8™ MICROCONTROLLER FAMILY (Continued)

Z8 Product Specifications, Technical Manuals and Users Guides	Part No	Unit Cost
Z86C06 CMOS Z8 CCP Preliminary Product Specification	DC-2563-00	N/C
Z86C08 CMOS Z8 8-Bit Microcontroller Product Specification and Addendum	DC-2527-02	N/C
Z86E08 CMOS Z8 8-Bit Microcontroller Product Specification and Addendum	DC-2542-01	N/C
Z86C09/C19 CMOS Z8 8-Bit Microcontroller Product Specification	DC-2506-02	N/C
Z86C11 CMOS Z8 Microcontroller Product Specification	DC-2572-01	N/C
Z86C12 Z8 ICE Product Specification	DC-2553-01	N/C
Z86C17 CMOS Z8 Microcontroller Preliminary Specification	DC-2597-00	N/C
Z86C21 CMOS Z8 Microcontroller Product Specification	DC-2568-01	N/C
Z86E21 CMOS OTP Microcontroller Product Specification	DC-2514-01	N/C
Z86E23 CMOS Z8 OTP Microcontroller Preliminary Product Specification	DC-2598-00	N/C
Z86C27/97 Z8 DTC™ Product Specification	DC-2561-01	N/C
Z86127 Low-Cost Digital Television Controller Preliminary Product Specification	DC-2574-00	N/C
Z86227 40-Pin Low-Cost Digital Television Controller Preliminary Product Specification	DC-3002-00	N/C
Z86C30 CMOS Z8 8-Bit Microcontroller Product Specification	DC-2509-03	N/C
Z86E30 CMOS Z8 OTP CCP Product Specification	DC-2573-01	N/C
Z86C40 CMOS CCP Product Specification	DC-2550-01	N/C
Z86E40 CMOS OTP CCP Product Specification	DC-2571-01	N/C
Z86C50 CMOS Z8 CCP ICE Advance Information Specification	DC-2559-0A	N/C
Z86C61/62/96 CMOS Z8 Microcontroller Preliminary Product Specification	DC-2587-00	N/C
Z86C90/C89 ROMless CMOS Z8 8-Bit Microcontroller Product Specification	DC-2506-01	N/C
Z86C91 Z8 CMOS ROMless Microcontroller Product Specification	DC-2566-01	N/C
Z86C93 CMOS Z8 ROMless Microcontroller Product Specification	DC-2508-02	N/C
Z86C95 CMOS Z8 Digital Signal Processor Advanced Information Specification	DC-3000-00	N/C
Z88C00 CMOS Super8 ROMless Microcontroller Preliminary Product Specification	DC-2551-00	N/C
Z89C00 4-Bit Digital Signal Processor (DSP) Preliminary Product Speficication	DC-2585-01	N/C
Z89120 ROM, Z89920 ROMless 16-Bit Mixed Signal Processor Preliminary Product Specification	DC-2615-00	N/C
Z8602 NMOS Z8 8-Bit Microcomputer Keyboard Controller Preliminary Product Specification	DC-2525-01	N/C
Z8604 NMOS Z8 8-Bit Microcontroller Preliminary Product Specification	DC-2524-03	N/C
Z8614 NMOS Z8 8-Bit MCU Keyboard Controller Preliminary Product Specification	DC-2576-00	N/C
Z86128 Closed-Captioned Controller Preliminary Product Specification	DC-2570-01	N/C
Z86L06 Low Voltage CMOS Preliminary Product Specification	DC-2564-01	N/C
Z86L29 6K Infrared (IR) Remote (ZIRC) Controller Advanced Information Specification	DC-2602-0A	N/C
Z8 OTP CMOS One-Time-Programmable Microcontrollers Addendum	DC-2614-AA	N/C
asm S8 Super8/Z8 Cross Assembler User's Guide	DC-8267-05	3.00
Z8 Microcontrollers Technical Manual	DC-8291-01	5.00

Z8 Application Notes	Part No	Unit Cost
The Z8 MCU In Telephone Answering Systems	DC-2514-01	N/C
Z8602 Controls A 101/102 PC/Keyboard	DC-2601-01	N/C
The Z8 MCU Dual Analog Comparator	DC-2516-01	N/C
Z86C09/19 Low Cost Z8 MCU Emulator	DC-2537-01	N/C
Z8 Applications for I/O Port Expansions	DC-2539-01	N/C
Z86E21 Z8 Low Cost Thermal Printer	DC-2541-01	N/C
Zilog Family On-Chip Oscillator Design	DC-2496-01	N/C
Using the Zilog Z86C06 SPI Bus	DC-2584-01	N/C
Interfacing LCDs to the Z8	DC-2592-01	N/C
X-10 Compatible Infrared (IR) Remote Control	DC-2591-01	N/C
Z86C17 In-Mouse Applications	DC-3001-01	N/C
Z86C40/E40 MCU Applications Evaluation Board	DC-2604-01	N/C
Z86C08/C17 Controls A Scrolling LED Message Display	DC-2605-01	N/C

Z80®/Z8000® CLASSIC FAMILY OF PRODUCTS

Z80®/Z180™/Z280®/Z8000® and Datacom Family	Part No	Unit Cost
Volume I Databook Microprocessors and Peripherals	DC-2610-01	5.00

Discrete Z80® Family

Z8400/C00 NMOS/CMOS Z80® CPU Product Specification
Z8410/C10 NMOS/CMOS Z80 DMA Product Specification
Z8420/C20 NMOS/CMOS Z80 PIO Product Specification
Z8430/C30 NMOS/CMOS Z80 CTC Product Specification
Z8440/Z84C40 NMOS/CMOS Z80 SIO Product Specification

Embedded Controllers

Z84C01 Z80 CPU with CGC Product Specification
Z84C50 RAM80™ Preliminary Product Specification
Z8470 Z80 DART Product Specification
Z84C90 CMOS Z80 KIO™ Product Specification
Z84011/C11 PIO Parallel I/O Product Specification
Z84013/015 Z84C13/C15 IPC/EIPC™ Product Specification
Z80180/Z8S180 Z180 MPU Product Specification
Z80181 ZIO™ Controller Product Specification
Z280™ MPU Preliminary Product Specification

Serial Communications Controllers

Z8030/Z8530 Z-BUS® SCC Product Specification
Z80C30/Z85C30 SCC Product Specification
Z85230 ESCC™ Product Specification
Z80230 Z-BUS ESCC Product Specification
Z16C35 ISCC™ Product Specification
Z5380 SCSI Product Specification
Z53C80 SCSI Product Specification
Z85C80 SCSI/SCC Product Specification
Z16C30 USC™ Product Specification
Z16C32 IUSC™ Product Specification
Z16C33 MUSC™ Product Specification
Z16C50 DDPLL™ Product Specification

Technical Articles

Z80 Questions and Answers
Z180 Questions and Answers
SCC Questions and Answers
ESCC Questions and Answers
ISCC Questions and Answers

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Z80®/Z8000® CLASSIC FAMILY OF PRODUCTS (Continued)

Z80/Z180/Z280 Product Specifications, Technical Manuals and Users Guides	Part No	Unit Cost
Z80 CPU Central Processing Unit Technical Manual	DC-0029-04	3.00
Z80 Family Programmer's Reference Guide	DC-0012-04	3.00
Z80 DMA Direct Memory Access Technical Manual	DC-2013-A0	3.00
Z80 PIO Parallel Input/Output Technical Manual	DC-0008-03	3.00
Z80 CTC Counter/Timer Circuit Technical Manual	DC-0036-03	3.00
Z80 SIO Serial I/O Technical Manual	DC-3033-01	3.00
Z80180 Z180 MPU Microprocessor Unit Technical Manual	DC-8276-03	3.00
Z280 MPU Microprocessor Unit Technical Manual	DC-8224-03	3.00
Z80181 Z181 ZIO™ Zilog I/O Controller Preliminary Product Specification	DC-2519-03	N/C
Z84013/15, Z84C13/C15 CMOS IPC™ Intelligent Peripheral Controller Product Specification	DC-2507-04	N/C
Z84011/C11 PIO Parallel I/O Controller Product Specification	DC-2526-02	N/C
Z84C00 20 MHz Z80 CPU Central Processing Unit Preliminary Product Specification	DC-2523-02	N/C
Z84C50 Z80 RAM80 Z80 CPU/2K SRAM Preliminary Product Specification	DC-2498-01	N/C
Z80180/Z8S180 Z180 Microprocessor Product Specification	DC-2609-00	N/C
Z80182 Zilog Intelligent Peripheral (ZIP™)	DC-2616-00	N/C
Low Voltage Devices	DC-2618-00	N/C

Z80/Z180/Z280 Application Notes	Part No	Unit Cost
Z180/SCC™ Serial Communications Controller Interface at 10 MHz	DC-2521-02	N/C
Z80 Using the 84C11/C13/C15 in place of the 84011/013/015	DC-2499-02	N/C
LocalTalk Link Access Protocol Using the Z80181	DC-2589-01	N/C
A Fast Z80 Embedded Controller	DC-2578-01	N/C

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Z8000 Product Specifications, Technical Manuals and Users Guides	Part No	Unit Cost
Z8000 CPU Central Processing Unit Technical Manual	DC-2010-06	3.00
SCC Serial Communication Controller Technical Manual	DC-8293-01	3.00
Z8036 Z-CIO/Z8536 CIO Counter/Timer and Parallel Input/Output Technical Manual	DC-2091-02	3.00
Z8038 Z8000 Z-FIO FIFO Input/Output Interface Technical Manual	DC-2051-01	3.00
Z8000 CPU Central Processing Unit Programmer's Pocket Guide	DC-0122-03	3.00
Z5380 SCSI Small Computer System Interface Preliminary Product Specification	DC-2477-01	N/C
Z80C30/Z85C30 CMOS SCC Serial Communication Controller Product Specification	DC-2442-05	N/C
Z85230 ESCC™ Enhanced Serial Communication Controller Product Specification	DC-2596-01	N/C
Z85233 EMSCC Enhanced Mono Serial Communication Controller Preliminary Product Specification	DC-2590-00	N/C
Z85C80 SCSCI™ Serial Communication and Small Computer Interface Preliminary Product Specification	DC-2534-02	N/C
Z16C30 CMOS USC™ Universal Serial Controller Preliminary Product Specification	DC-2492-03	N/C
Z16C30 USC Universal Serial Controller Preliminary Technical Manual	DC-8280-02	3.00
Z16C30/Z16C33 CMOS USC/MUSC™ Universal Serial Controller Technical Manual	DC-8285-01	3.00
Z16C30/Z16C33 CMOS USC/MUSC Universal Serial Controller Addendum	DC-8285-01A	N/C
Z16C32 IUSC™ Integrated Universal Serial Controller Product Specification	DC-2600-00	N/C
Z16C32 IUSC™ Integrated Universal Serial Controller Product Specification Addendum	DC-2600-00A	N/C
Z16C32 IUSC™ Integrated Universal Serial Controller Technical Manual	DC-8292-02	3.00
Z16C33 CMOS MUSC Mono-Universal Serial Controller Preliminary Product Specification	DC-2517-03	N/C
Z16C35 CMOS ISCC™ Integrated Serial Communication Controller Product Specification	DC-2515-03	N/C
Z16C35 ISCC Integrated Serial Communication Controller Technical Manual	DC-8286-01	3.00
Z16C35 ISCC Integrated Serial Communication Controller Addendum	DC-8286-01A	N/C
Z53C80 Small Computer System Interface (SCSI) Product Specification	DC-2575-01	N/C
Z80230 Z-Bus® ESCC Enhanced Serial Communication Controller Preliminary Product Specification	DC-2603-01	N/C
Z85233 EMSCC™ Enhanced Mono Serial Communication Controller Preliminary Product Specification	DC-2590-00	N/C

Z8000 Application Notes	Part No	Unit Cost
Z16C30 Using the USC in Military Applications	DC-2536-01	N/C
Datacom IUSC/MUSC Time Slot Assigner	DC-2497-02	N/C
Datacom Evaluation Board Using The Zilog Family With The 80186 CPU	DC-2560-03	N/C
ESCC Enhancements Over The SCC	DC-2555-01	N/C
Z16C30 USC - Design a Serial Board for Multiple Protocols	DC-2554-01	N/C
Integrating Serial Data and SCSI Peripheral Control on one Chip	DC-2594-01	N/C
Using a SCSI Port for Generalized I/O	DC-2608-01	N/C

MILITARY COMPONENTS FAMILY

Military Specifications	Part No	Unit Cost
Z8681 ROMless Microcomputer Military Product Specification	DC-2392-02	N/C
Z8001/8002 Military Z8000 CPU Central Processing Unit Military Product Specification	DC-2342-03	N/C
Z8581 Military CGC Clock Generator and Controller Military Product Specification	DC-2346-01	N/C
Z8030 Military Z8000 Z-SCC Serial Communications Controller Military Product Specification	DC-2388-02	N/C
Z8530 Military SCC Serial Communications Controller Military Product Specification	DC-2397-02	N/C
Z8036 Military Z8000 Z-CIO Counter/Timer Controller and Parallel I/O Military Electrical Specification	DC-2389-01	N/C
Z8038/8538 Military FIO FIFO Input/Output Interface Unit Military Product Specification	DC-2463-02	N/C
Z8536 Military CIO Counter/Timer Controller and Parallel I/O Military Electrical Specification	DC-2396-01	N/C
Z8400 Military Z80 CPU Central Processing Unit Military Electrical Specification	DC-2351-02	N/C
Z8420 Military PIO Parallel Input/Output Controller Military Product Specification	DC-2384-02	N/C
Z8430 Military CTC Counter/Timer Circuit Military Electrical Specification	DC-2385-01	N/C
Z8440/1/2/4 Z80 SIO Serial Input/Output Controller Military Product Specification	DC-2386-02	N/C
Z80C30/85C30 Military CMOS SCC Serial Communications Controller Military Product Specification	DC-2478-02	N/C
Z84C00 CMOS Z80 CPU Central Processing Unit Military Product Specification	DC-2441-02	N/C
Z84C20 CMOS Z80 PIO Parallel Input/Output Military Product Specification	DC-2384-02	N/C
Z84C30 CMOS Z80 CTC Counter/Timer Circuit Military Product Specification	DC-2481-01	N/C
Z84C40/1/2/4 CMOS Z80 SIO Serial Input/Output Military Product Specification	DC-2482-01	N/C
Z16C30 CMOS USC Universal Serial Controller Military Preliminary Product Specification	DC-2531-01	N/C
Z80180 Z180 MPU Microprocessor Unit Military Product Specification	DC-2538-01	N/C
Z84C90 CMOS KIO Serial/Parallel/Counter Timer Preliminary Military Product Specification	DC-2502-00	N/C
Z85230 ESCC Enhanced Serial Communication Controller Military Product Specification	DC-2595-00	N/C

GENERAL LITERATURE

Catalogs, Handbooks and Users Guides	Part No	Unit Cost
Superintegration Short Form Catalog 1992	DC-5472-09	N/C
Quality and Reliability Report	DC-2475-09	N/C
Superintegration Products Guide	DC-5499-06	N/C
The Handling and Storage of Surface Mount Devices User's Guide	DC-5500-02	N/C
Support Products Summary	DC-2545-03	N/C
Universal Object File Utilities User's Guide	DC-8236-04	3.00
Zilog 1991 Annual Report	DC-1991-AR	N/C
Microcontroller Quick Reference Folder	DC-5508-01	N/C

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