ISL71090SEH50

Radiation Hardened Ultra Low Noise, Precision Voltage Reference

FN8588
Rev 4.0
May 14, 2021

The ISL71090SEH50 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 7V to 30V. The ISL71090SEH50 uses the Advanced Bipolar technology to achieve 1.1µV_{P-P} noise at 0.1Hz with an accuracy over-temperature of 0.15%.

The ISL71090SEH50 offers a 5.0V output voltage with 10ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld Flatpack package.

The ISL71090SEH50 is ideal for high-end instrumentation, data acquisition and applications requiring high DC precision where low noise performance is critical.

Applications

- RH voltage regulators precision outputs
- Precision voltage sources for data acquisition system for space applications
- Strain and pressure gauge for space applications

Features

- **Reference output voltage . . . . . 5.0V ±0.05%**
- **Accuracy over temperature . . . . . ±0.15%**
- **Output voltage noise . . . . . 1.1µV_{P-P} typical (0.1Hz to 10Hz)**
- **Supply current . . . . . 930µA (typical)**
- Tempco (box method) . . . . . 10ppm/°C maximum
- Output current capability 20mA
- Line regulation 8ppm/V
- Load regulation 10ppm/mA
- Operating temperature range. . . . . -55°C to +125°C
- **Radiation environment**
  - **High dose rate (50-300rad(Si)/s) . . . . . 100krad(Si)**
  - **Low dose rate (0.01rad(Si)/s) . . . . . 50krad(Si)***
  - **SET/SEL/SEB . . . . . 86MeV•cm²/mg**

*Product capability established by initial characterization.

- Electrically screened to SMD 5962-13211

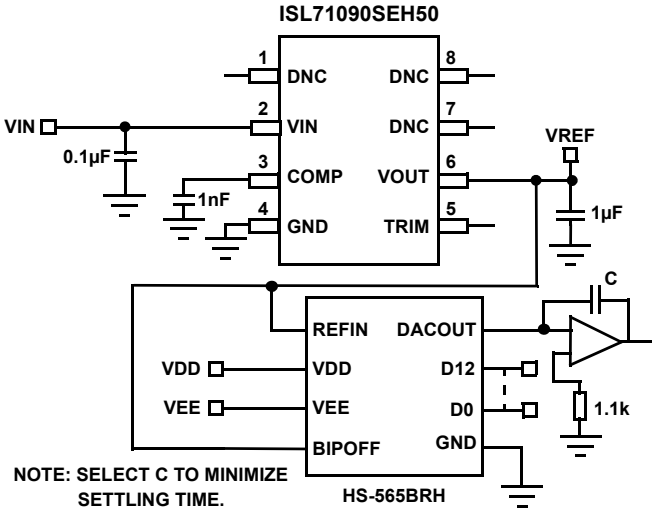


FIGURE 1. ISL71090SEH50 TYPICAL APPLICATION DIAGRAM

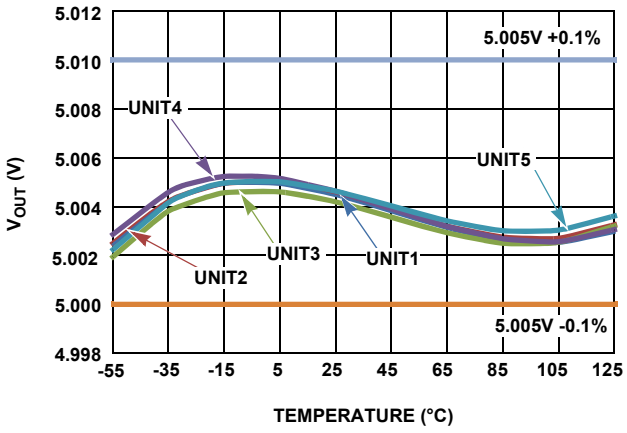


FIGURE 2. V_{OUT} vs TEMPERATURE

Ordering Information

SMD ORDERING NUMBER (Note 2)	PART NUMBER (Note 1)	V_{OUT} OPTION (V)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE	TEMP RANGE
5962R1321103VXC	ISL71090SEHVF50	5.0	HDR to 100krad(Si), LDR to 50krad(Si)	8 Ld Flatpack	K8.A	Tray	-55 to +125°C
N/A	ISL71090SEHF50/PROTO Note 4		N/A				
5962R1321103V9A	ISL71090SEHVX50 Note 3		HDR to 100krad(Si), LDR to 50krad(Si)	Die	-	-	
N/A	ISL71090SEHX50SAMPLE Notes 3, 4		N/A				
N/A	ISL71090SEH50EV1Z Note 5	Evaluation Board					

NOTES:

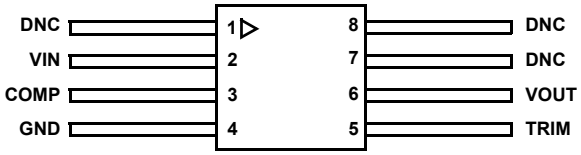
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications for Die" on page 6.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	V_{OUT} (V)	TEMPCO (ppm/°C)	OUTPUT VOLTAGE NOISE (μV_{P-P})	LOAD REGULATION (ppm/mA)
ISL71090SEH12	1.25	10	1	35
ISL71090SEH25	2.5	10	2	2.5
ISL71090SEH50	5.0	10	1.1	10
ISL71090SEH75	7.5	10	1	10

Pin Configuration

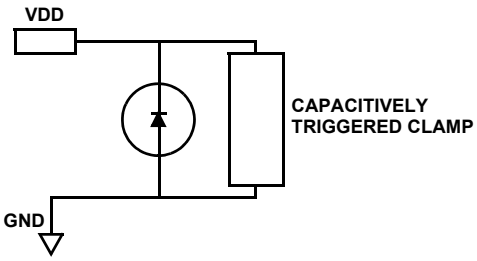
ISL71090SEH50
(8 LD FLATPACK)
TOP VIEW



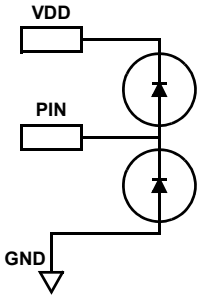
NOTE: The ESD triangular mark is indicative of pin #1. It is a part of the device marking and is placed on the lid in the quadrant where pin #1 is located.

Pin Descriptions

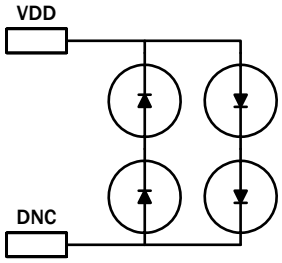
PIN NUMBER	PIN NAME	ESD CIRCUIT	DESCRIPTION
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection
3	COMP	2	Compensation and noise reduction capacitor
4	GND	1	Ground connection. Also connected to the lid.
5	TRIM	2	Voltage reference trim input
6	VOUT	2	Voltage reference output



ESD CIRCUIT 1



ESD CIRCUIT 2



ESD CIRCUIT 3

Functional Block Diagram

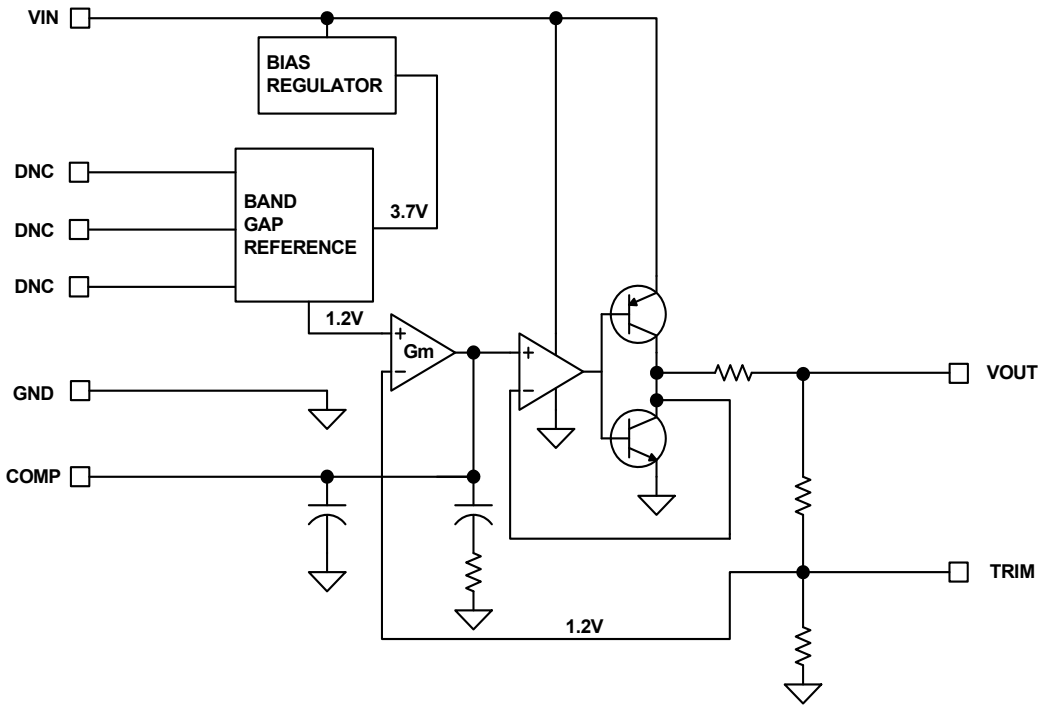


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

Maximum Voltage
- V_{IN} to GND ..... -0.5V to +40V
- V_{IN} to GND at an LET = 86MeV • cm^2/mg ..... -0.5V to +36V
- V_{OUT} to GND (10s) ..... -0.5V to V_{OUT} + 0.5V
- Voltage on any Pin to Ground ..... -0.5V to +V_{OUT} + 0.5V
- Voltage on DNC Pins ..... No connections permitted to these pins

ESD Ratings
- Human Body Model (Tested per MIL-PRF-883 3015.7) 2kV
- Machine Model (Tested per JESD22-A115-A) 200V
- Charged Device Model (Tested per JESD22-C101D)) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 6, 7)	140	15

Storage Temperature Range ..... -65°C to +150°C

Maximum Junction Temperature (T_{JMAX}) ..... +150°C

Recommended Operating Conditions

V_{IN} ..... 7.0V to +30V

Temperature Range ..... -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions CAN adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
7. For θ_{JC}, the case temperature location is the center of the ceramic on the package underside.
8. Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.
9. The output capacitance used for SEE testing is C_{IN} = 0.1µF and C_{OUT} = 1µF.

Electrical Specifications for Flatpack

V_{IN} = 10V, I_{OUT} = 0mA, C_L = 0.1µF and C_C = 1nF unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
V_{OUT}	Output Voltage			5.005		V
V_{OA}	V_{OUT} Accuracy at T_A = +25°C	V_{OUT} = 5.005V, (Note 13)	-0.05		+0.05	%
	V_{OUT} Accuracy at T_A = -55°C to +125°C	V_{OUT} = 5.005V, (Note 13)	**-0.15**		**+0.15**	%
	V_{OUT} Accuracy at T_A = +25°C, Post Radiation	V_{OUT} = 5.005V, (Note 13)	-0.3		+0.3	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 11)				**10**	ppm/°C
V_{IN}	Input Voltage Range		**7.0**		**30**	V
I_{IN}	Supply Current			0.930	**1.500**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 7.0V to 30V		8	**20**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		10	**20**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		21	**40**	ppm/mA
V_D	Dropout Voltage (Note 12)	I_{OUT} = 10mA		1.5	**1.7**	V
I_{SC+}	Short-Circuit Current	T_A = +25°C, V_{OUT} tied to GND		53		mA
I_{SC-}	Short-Circuit Current	T_A = +25°C, V_{OUT} tied to V_{IN}		-63		mA
t_R	Turn-On Settling Time	90% of final value, C_L = 1.0µF, C_C = open		250		µs
PSRR	Ripple Rejection	f = 120Hz		90		dB
e_N	Output Voltage Noise	0.1Hz ≤ f ≤ 10Hz		1.1		μV_{P-P}
V_N	Broadband Voltage Noise	10Hz ≤ f ≤ 1kHz		2.2		μV_{RMS}
	Noise Density	f = 1kHz, V_{IN} = 7.1V		68		nV/√Hz
$\Delta V_{OUT}/\Delta t$	Long Term Drift	T_A = 125°C, 1000hrs		15		ppm

Electrical Specifications for Die

V_{IN} = 10V, I_{OUT} = 0mA, C_L = 0.1µF and C_C = 1nF unless otherwise specified. **Boldface limits apply after radiation at 25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. Specifications over temperature are guaranteed but not production tested on die.**

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
V_{OUT}	Output Voltage			5.005		V
V_{OA}	V_{OUT} Accuracy at T_A = +25°C	V_{OUT} = 5.005V (Note 14)	-0.05		+0.05	%
	V_{OUT} Accuracy at T_A = -55°C to +125°C	V_{OUT} = 5.005V (Note 14)	**-0.15**		**+0.15**	%
	V_{OUT} Accuracy at T_A = +25°C Post Radiation	V_{OUT} = 5.005V, (Note 14)	-0.3		+0.3	%
TC V_{OUT}	Output Voltage Temperature Coefficient (Note 11)				**10**	ppm/°C
V_{IN}	Input Voltage Range		**7.0**		**30**	V
I_{IN}	Supply Current			0.930	**1.500**	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{IN} = 7.0V to 30V		8	**20**	ppm/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	Sourcing: 0mA ≤ I_{OUT} ≤ 20mA		10	**20**	ppm/mA
		Sinking: -10mA ≤ I_{OUT} ≤ 0mA		21	**40**	ppm/mA
V_D	Dropout Voltage (Note 12)	I_{OUT} = 10mA		1.5	**1.7**	V

NOTES:

10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
11. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in $V_{OUT(max)}$ - $V_{OUT(min)}$ is divided by the temperature range; in this case, -55°C to +125°C = +180°C.
12. Dropout Voltage is the minimum V_{IN} - V_{OUT} differential voltage measured at the point where V_{OUT} drops 1mV from V_{IN} = nominal at T_A = +25°C.
13. Post-reflow drift for the ISL71090SEH50 devices can be 100µV typical based on experimental results with devices on FR4 double sided boards. The engineer must take this into account when considering the reference voltage after assembly.
14. The V_{OUT} accuracy is based on die mount with Silver Glass die attach material such as “QMI 2569" or equivalent in a package with an Alumina ceramic substrate.

Typical Performance Curves

V_{OUT} = 5.005V, T_A = +25°C, C_{OUT} = 1µF, COMP = 1nF unless otherwise specified.

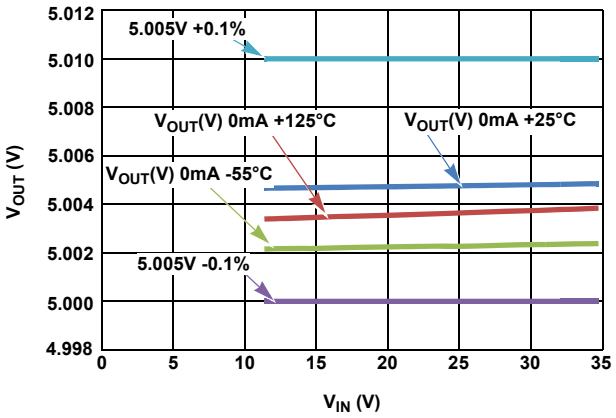


FIGURE 4. V_{OUT} ACCURACY OVER TEMPERATURE

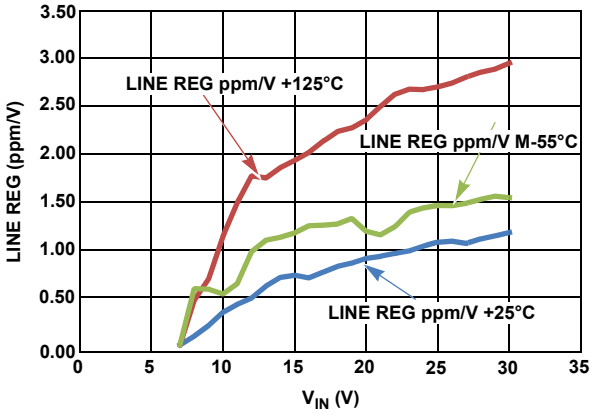


FIGURE 5. LINE REGULATION OVER TEMPERATURE

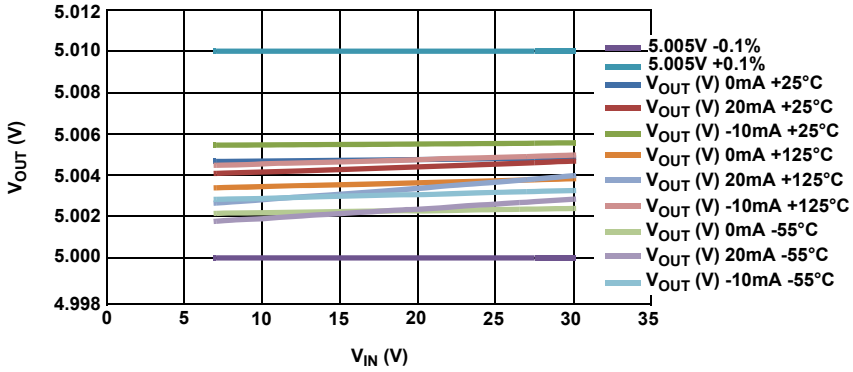


FIGURE 6. V_{OUT} vs V_{IN} AT 0mA, 20mA AND -10mA

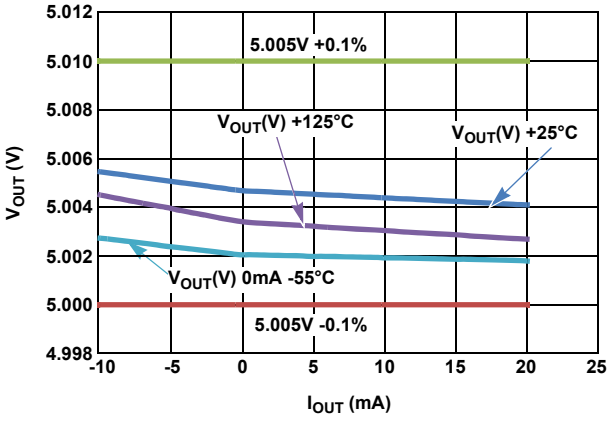


FIGURE 7. LOAD REGULATION OVER TEMPERATURE AT V_{IN} = 7V (V)

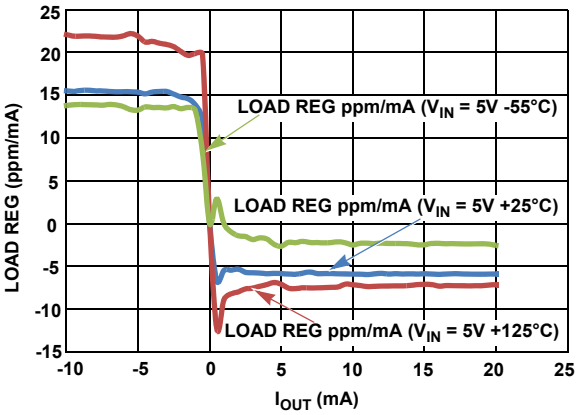


FIGURE 8. LOAD REGULATION OVER TEMPERATURE AT V_{IN} = 7V (ppm/mA)

Typical Performance Curves

V_{OUT} = 5.005V, T_A = +25°C, C_{OUT} = 1µF, COMP = 1nF unless otherwise specified.

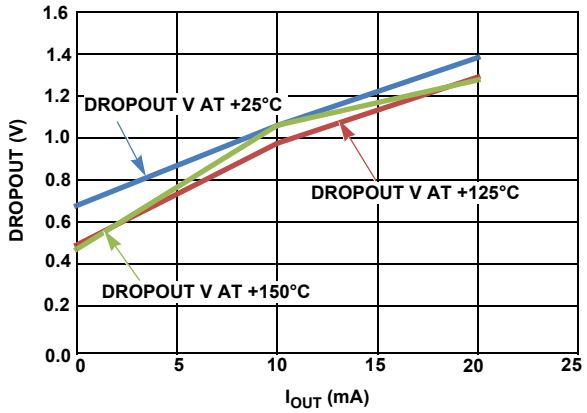


FIGURE 9. DROPOUT VOLTAGE FOR 5.005V

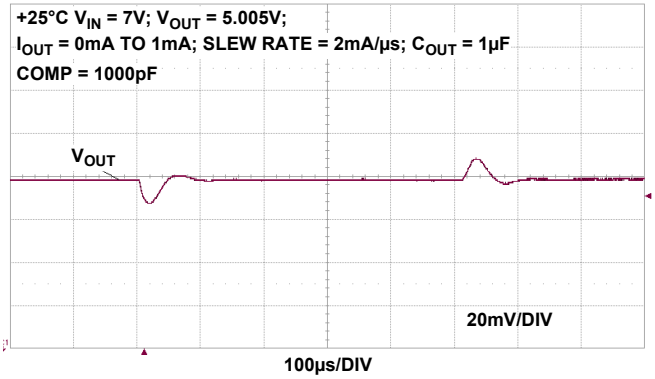


FIGURE 10. LOAD TRANSIENT (0mA TO 1mA)

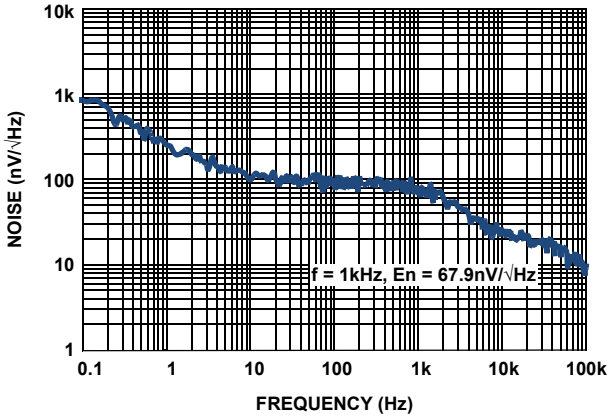


FIGURE 11. NOISE DENSITY vs FREQUENCY (V_{IN} = 7.1V, I_{OUT} = 0mA, C_{IN} = 0.1µF, C_{OUT} = 1µF, COMP = 1nF)

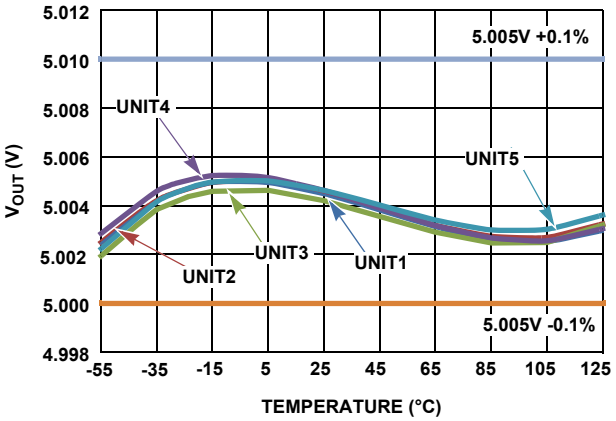


FIGURE 12. 5.005V V_{OUT} LIMITS PLOT

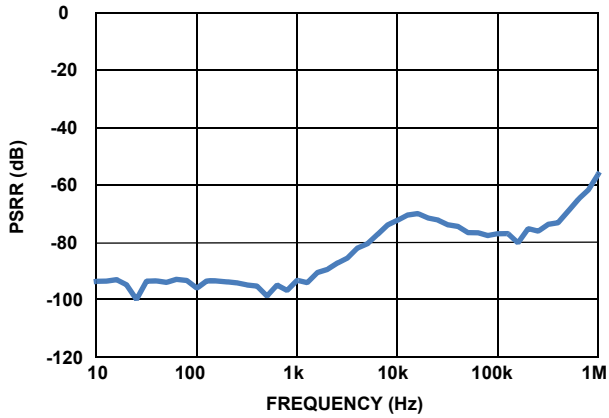


FIGURE 13. PSRR (+25°C, V_{IN} = 7V, V_{OUT} = 5.005V, I_{OUT} = 0mA, C_{IN} = 0.1µF, C_{OUT} = 1.0µF, COMP = 1nF, V_{SIG} = 300mV_{P-P})

Device Operation

Bandgap Precision Reference

The ISL71090SEH50 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

Applications Information

Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally, mild stresses to the die when the Printed Circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of typically 100µV can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

Noise Performance and Reduction

The output noise voltage over the 0.1Hz to 10Hz bandwidth is typically 1.1µV_{P-P} (V_{OUT} = 5.0V). The noise measurement is made with a 9.9Hz bandpass filter. Noise in the 10Hz to 1kHz bandwidth is approximately 2.2µV_{RMS}, with 1µF capacitance on the output. This noise measurement is made with a bandpass filter of 990Hz. Load capacitance up to 10µF (with COMP capacitor from Table 2) can be added but will result in only marginal improvements in output noise and transient response.

Turn-On Time

Normal turn-on time is typically 250µs, the circuit designer must take this into account when looking at power-up delays or sequencing.

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, which provide for the maximum voltage deviation and take the total variation, (V_{HIGH} - V_{LOW}), this is then divided by the temperature extremes of measurement (T_{HIGH} – T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the “Box” method for specifying temperature coefficient.

Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The voltage at the trim pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference. The suggested method to adjust the output is to connect a 1MΩ external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100kΩ resistance and whose outer terminals connect to V_{OUT} and ground. If a 1MΩ resistor is connected to trim, the output adjust range will be ±6.3mV. The TRIM pin should not have any capacitor tied to its output, also it is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal, to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

Output Stage

The output stage of the device has a push pull configuration with an high side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 20mA.

Use of COMP Capacitors

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from COMP pin to GND. See Table 2 for recommended values of the COMP capacitor.

TABLE 2.

C_{OUT} (µF)	C_{COMP} (nF)
0.1	1
1	1
10	10

SEE Testing

The SET result is based on the ISL71090SEH25. The ISL71090SEH25 and ISL71090SEH50 share the same active circuitry consisting of a precision bandgap ckt and a trimmable amplifier to set the output reference with only a resistor change to scale the output. The SET test was done under an ion beam having an LET of 86MeV•cm^2/mg. The device did not latch-up or burnout to a VDD of 36V and at +125°C. Single Event transients were observed and are summarized in the Table 3:

TABLE 3.

V_{IN} (V)	I_{OUT} (mA)	C_{OUT} (µF)	SET (% V_{OUT})
4	5	1	-4.6
30	5	1	-4.4
30	5	10	-1.0

DNC Pins

These pins are for trimming purpose and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

Package Characteristics

Weight of Packaged Device

0. 31 Grams (typical)

Lid Characteristics

Finish: Gold
Potential: Connected to lead #4 (GND)
Case Isolation to Any Lead: 20 x 10^9 Ω (minimum)

Die Characteristics

Die Dimensions

1464µm x 1744µm (58 mils x 69 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Floating

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

<2 x 10^5 A/cm^2

TRANSISTOR COUNT

182

PROCESS

Dielectrically Isolated Advanced Bipolar Technology- PR40 SOI

Metallization Mask Layout

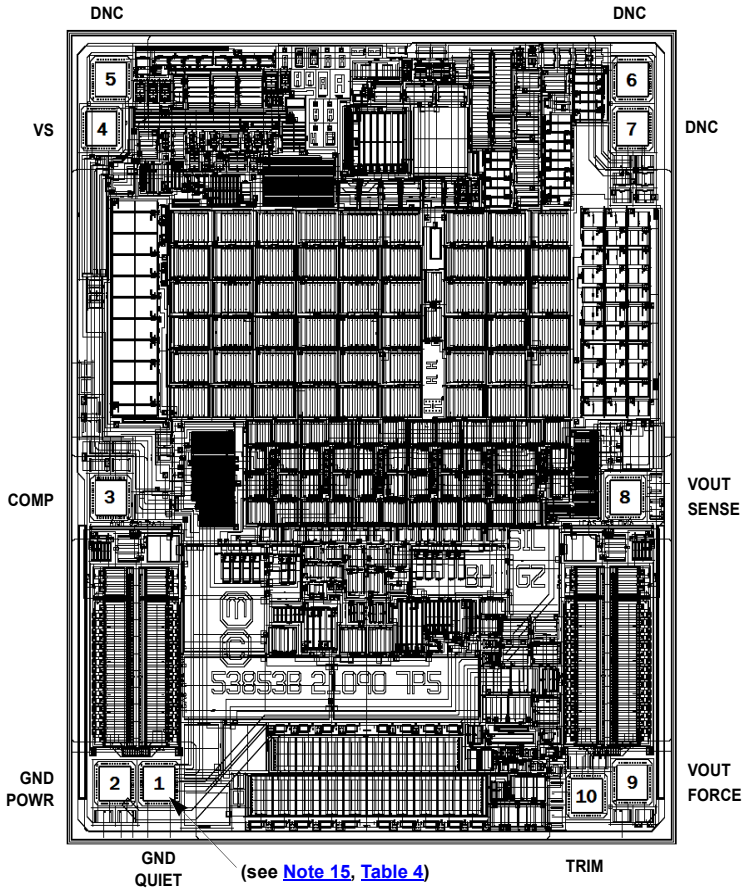


TABLE 4. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	BOND WIRES PER PAD
GND PWR	2	-104	0	1
GND QUIET	1	0	0	1
COMP	3	-108	589	1
VS	4	-125	1350	1
DNC	5	-108	1452	1
DNC	6	1089	1452	1
DNC	7	1089	1350	1
VOUT SENSE	8	1072	598	1
VOUT FORCE	9	1088	1	1
TRIM	10	985	-25	1

NOTES:

15. Origin of coordinates is the centroid of GND QUIET.
16. Bond wire size is 1.0 mil.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
May 14, 2021	4.0	Updated the Radiation Features bullet. Updated Ordering Information table formatting and added Notes 3, 4, and 5. Added the Transistor Count to the Assembly Related Information. Removed Related Literature and About Intersil sections.
March 15, 2016	3.0	-Updated Related Literature document titles to match titles on the actual documents. -Corrected the Evaluation board part number in the Ordering Information table on page 2. -Added Table 1 on page 2. -On page 5: Changed Electrical Specification for Flatpack note from: “Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.” To: “Boldface limits apply after radiation at 25°C or across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified.” For parameter V_{OA} (row 4) in Electrical Specifications for Flatpack table changed the description from: “V_{OUT} Accuracy, Post Rad”, to: “V_{OUT} Accuracy at TA = +25°C, Post Radiation”. For parameters V_{OA} (rows 2, 3, 4) in Electrical Specifications for Flatpack table added “Note 10" to Conditions column. Removed reference to TB493 as this is not applicable to hermetic packages. -On page 6: Changed Electrical Specification for Die note from: “Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation.” To: “Boldface limits apply after radiation at 25°C or across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. For parameter V_{OA} (row 4) in Electrical Specifications for Die table changed the description from: “V_{OUT} Accuracy, Post Rad”, to: “V_{OUT} Accuracy at TA = +25°C, Post Radiation”. For parameters V_{OA} for Post Rad (row 4) in Electrical Specifications for Die table added “Note 11” to Conditions column. -Updated POD K8.A to the latest revision changes are as follows: Modified Note 2 by adding the words “...in addition to or instead of...”
Dec 2, 2013	2.0	Electrical spec table on page 5 (Flatpack) and page 6 (Die): V_{OUT} Accuracy Post Rad section, changed the value for Min from -0.2 to -0.3 and Max from +0.2 to +0.3
Oct9, 2013	1.0	Initial Release.

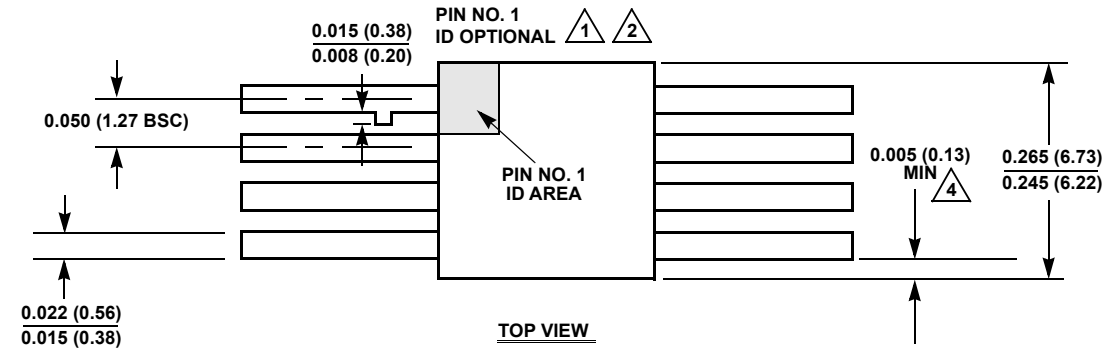
Package Outline Drawing

For the most recent package outline drawing, see K8.A.

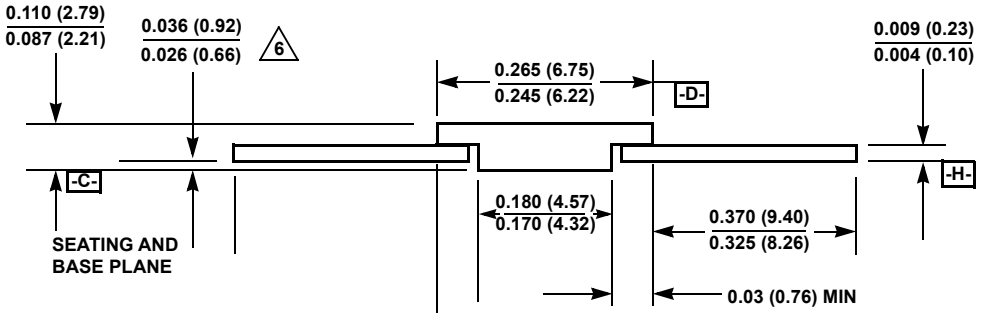
K8.A

8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

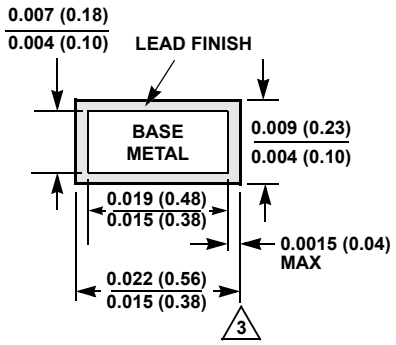
Rev 4, 12/14



TOP VIEW



SIDE VIEW



SECTION A-A

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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