Development Tools for i.MX Applications Processors

APF-CON-T0679

Rui Yang

May 2013

freescale™ 飞思卡尔

Agenda

- **Introduction**
  - Processor Overview
  - Multimedia (IPU/VPU/GPU)
  - System Boot
- **Operating System**
  - Release Version Control
  - Linux (LTIB/Yocto)
  - Android
  - WinCE/QNX
- **Hardware Platform**
  - SABRE SD
  - SABRE AI
- **Develop Tools**
  - ARM Debug
  - Clock Configuration
  - IOMUX
  - DDR Stress Test
  - OBDS/PLATLIB
  - MFG
- **Freescale Support**
  - IMXCommunity
- **Summary and QA**

Introduction

Processor Overview

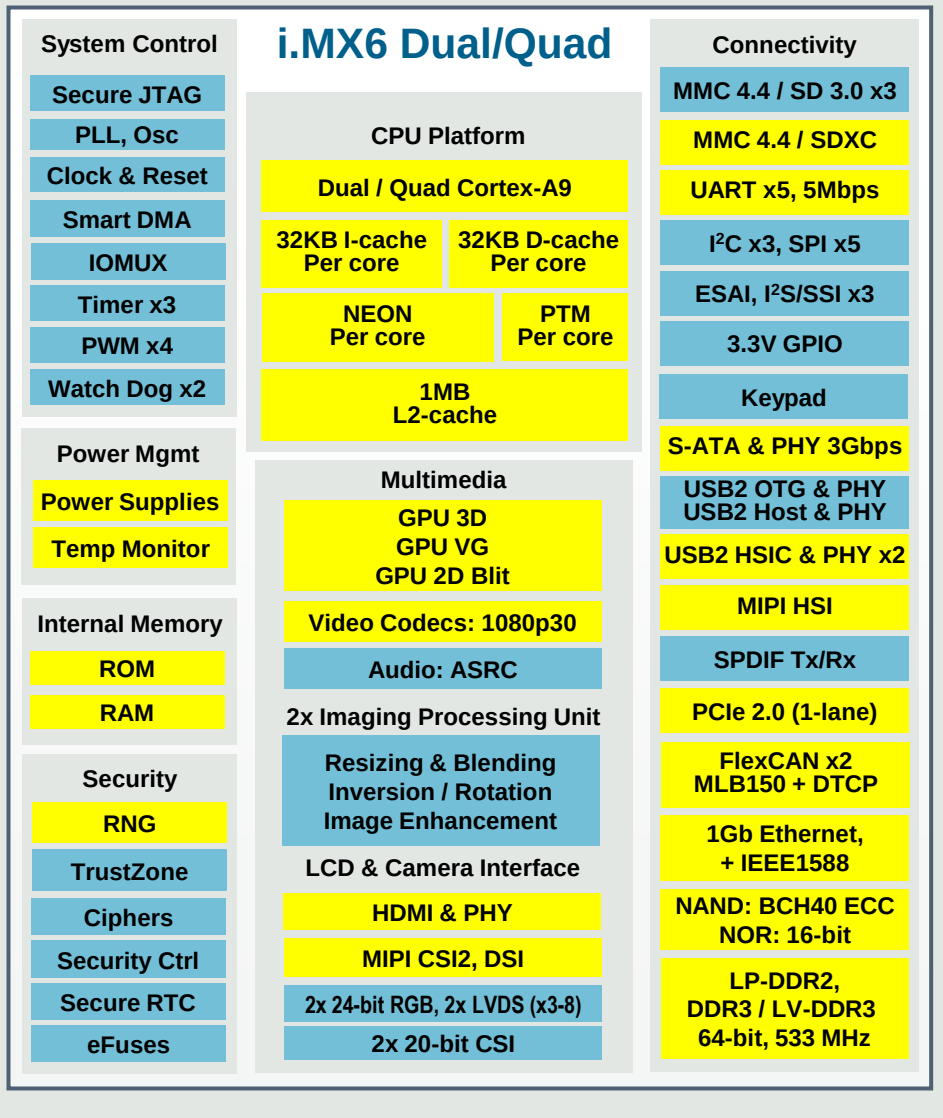
i.MX 6Dual/6Quad Applications Processor

Specifications

- **CPU:** i.MX 6Quad 4x Cortex-A9 @1.2 GHz, 12000 DMIPS
  i.MX 6Dual 2x Cortex-A9 @1.2 GHz, 6000 DMIPS
- **Process:** 40nm
- **Core Voltage:** 1.1V
- **Package:** 21x21 0.8mm Flip-chip BGA
  12x12 PoP (LP-DDR2 dual channel – standard JEDEC POP)

Key Features and Advantages

- Multi-core architecture for high performance, 1MB L2 cache
- 64-bit dual channel LP-DDR2, 64bit DDR3 and raw / managed NAND
- S-ATA 3Gbps interface (SSD / HDD)
- Delivers rich graphics and UI in HW
  - OpenGL/ES 2.x 3D accelerator with OpenCL EP support and OpenVG 1.1 acceleration
- Drives high resolution video in HW
  - Multi-format HD1080 video decode and encode
  - 1080p60 decode, 720p60 encode
  - High quality video processing (resizing, de-interlacing, etc.)
- Flexible display support
  - Four simultaneous: 2x Parallel, 2x LVDS, MIPI-DSI, or HDMI
  - Dual display up to WUXGA (1920x1200) and HD1080
- MIPI-CSI2, DSI and HSI
- Increased analog integration simplifies system design and reduces BOM
  - DC-DC converters and linear regulators supply cores and all internal logic
  - Temperature monitor for smart performance control
- Expansion port support via PCIe 2.0
- Car network: 2xCAN, MLB150 with DTCP, 1Gb Ethernet with IEEE1588



Updated from i.MX53

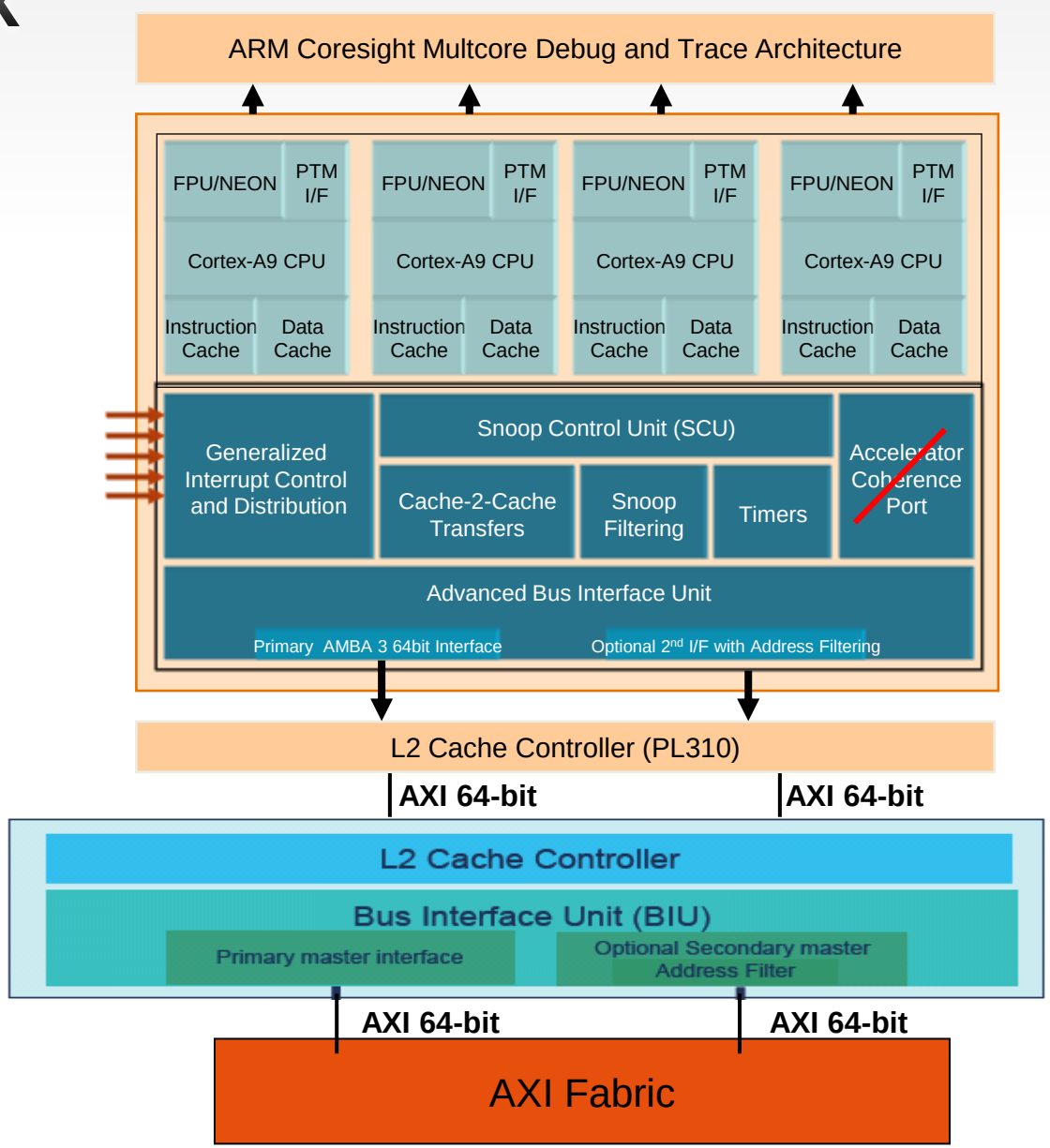
freescale™ 飞思卡尔

5

ore Complex – i.MX 6Dual/Quad

HW Components:

- System:
  - 2x/4x Cores in i.MX 6 Dual/Quad
  - 32 KB L1 (I and D)
  - 1MB L2 Cache
  - 128 Interrupts
  - Using 2x 64-bit AXI to L2C
- Per core
  - 32 KB I and 32KB D L1 Cache
  - Neon, FPU, Jazelle, Trustzone



freescale 飞思卡尔

6

freescale™
飞思卡尔

Introduction

Multimedia(IPU/VPU/GPU)

Intelligent Integration of Multi-Media

i.MX 6Dual/6Quad VPU

-H.264 MVC 1080p60 decode
-H.264 MVC 720p60 encode
- 350mW power consumption for single video!

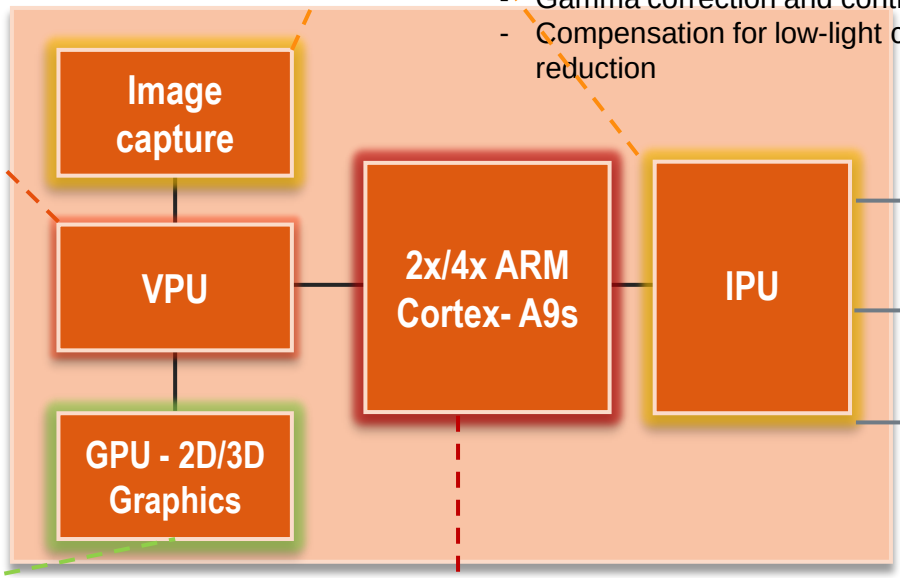
i.MX 6Dual/6Quad IPU

- Four Display support (2x MIPI-DSI, Parallel, HDMI v1.4a)
- Stereoscopic camera input
- Color adjustments and gamut mapping
- Gamma correction and contrast stretching
- Compensation for low-light conditions & backlight reduction

Recording Video

Movie Content

Game Content



3D LCD

3D Television

i.MX 6Dual/6Quad Triple-Play Graphics

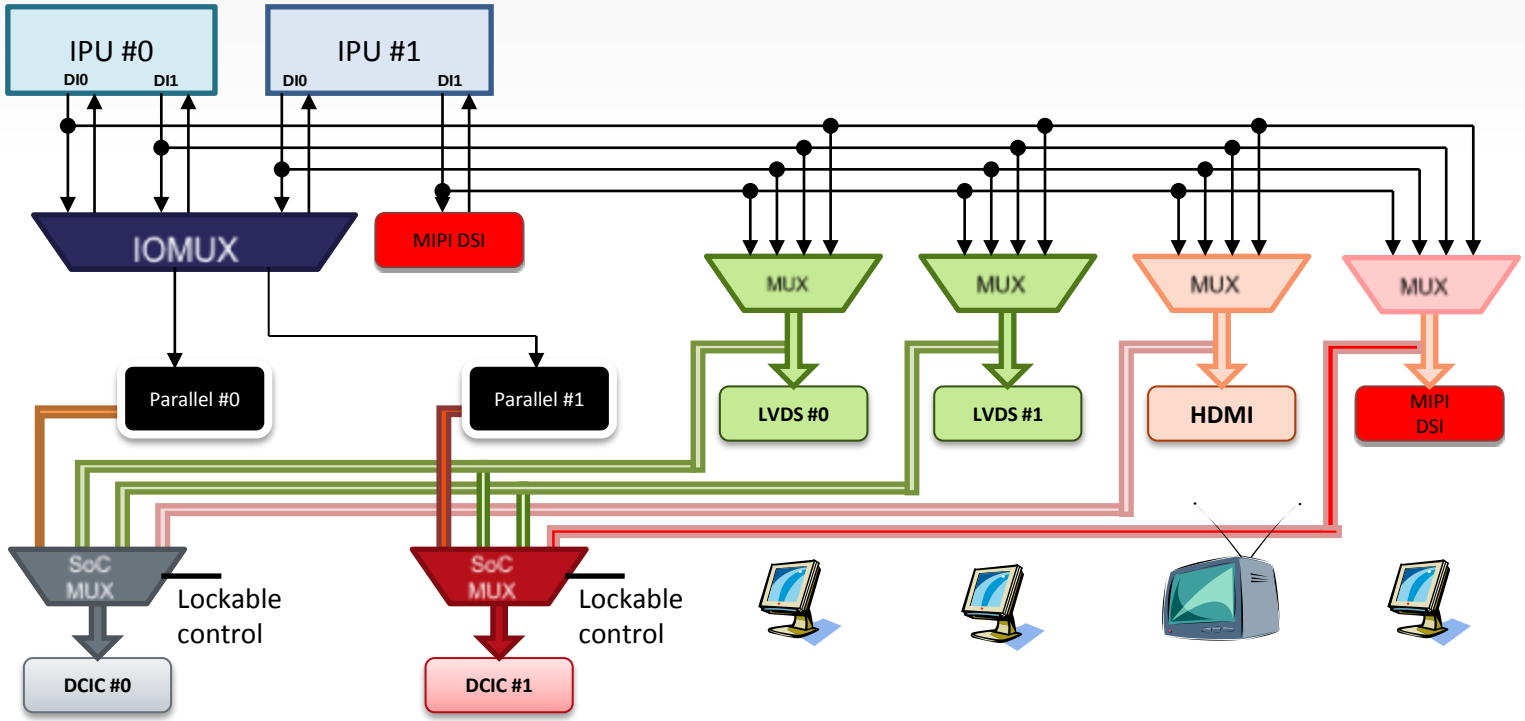
- 3 engines: 3D, OpenVG and BLT
- 200 MT/s, 4 shaders, 3 separate engines
- High quality 3D games optimized for mobile
- Augmented reality views (real world + 3D objects)
- Advanced 3D video formats (source/depth format)

i.MX 6Dual/6Quad– 2x/4x cores

- Create, transform, enhance, & publish multimedia fast!
- Intuitive User Interfaces for content viewing
- Scalability for 'the next big use case'

freescale™ 飞思卡尔

Display Ports Muxing – i.MX 6Dual/Quad



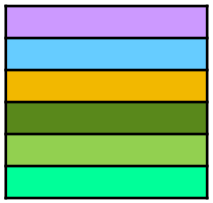
- **Six ports**
  - Two parallel - driven directly by the IPU
  - Two LVDS channels - driven by the LVDS bridge
  - One HDMI – driven by the HDMI transmitter
  - One MIPI-DSI – driven by the MIPI-DSI transmitter
- **Four simultaneous outputs**
  - Each IPU has two display ports (DI0 and DI1)
  - Therefore, up to four external ports can be active at any given time.
  - Additional asynchronous data flows can be sent through the parallel ports and the MIPI-DSI port
- **Display Content Integrity Check (DCIC)**
  - For parallel interfaces: probes the I/O loopback (essentially equivalent to probing the external wires)
  - For other integrated interfaces (e.g. LVDS): probes the IPU output (essentially equivalent to the inputs to the serializers)

freescale™ 飞思卡尔

VPU HD Video – i.MX53 vs i.MX 6Dual/Quad

- Embeds a flexible, powerful and low power hardware acceleration for HD video decoding in Blue-ray disk quality
- Note: in all cases, the HW CODEC meets or exceeds the bit-rate requirements specified in the standards

Feature	Format	Profile	i.MX53	i.MX6 Quad/Dual
Low-Power Audio Decode			SW	SW
Low-Power Video Decode	MPEG-2	Main-High	HW	HW
	H.264	BP/MP/HP	HW	HW
	VC1	SP/MP/AP	HW	HW
	RV10	8/9/10	HW	HW*
	MPEG4/Xvid	SP/ASP	HW	HW
	DivX	3/4/5/6	HW	HW
	H.263	P0/P3	HW	HW*
	Sorenson H.263	N/A	HW	HW*
	AVS	Jizhun	SW	HW
	On2 VP6/8	N/A	SW	HW* (for VP8)
	SVC	HP	SW	SW
	MVC	N/A	SW/HW	HW*
	MJPEG	Baseline	HW, 40MP/sec	HW, 120MP/sec
Low-Power Video Encode	H.264	Baseline	HW	HW*
	H.263	P0/P3	HW	HW*
	MPEG4	Simple	HW	HW*
	MJPEG	Baseline	HW, 80MP/sec	HW, 160MP/sec
Video Telephony (SiP, H323) – H.264 BP			HW	HW
Transcode (DLNA) – (M)DMS/(M)DMP			HW	HW
Video de-interlacing			HW	HW
Further Video Processing (deblocking, resizing, CSC)			HW	HW



1080i/p30+D1
1080i/p30 (* - p only)
720p30 or 720p60
720p20
WVGA
D1 (PAL/NTSC)

freescale™ 飞思卡尔

..iple-Play Graphics Solution - i.MX 6 Series

VIVANTE GC355

Vector Graphics

- GPU-VG @ 500MHz
- 350M pixels / sec raw performance
- Native OpenVG™ 1.1 Khronos conformance with hardware tessellation

VIVANTE GC2000

3D + GPGPU

- GPUv4 @ 533MHz
- 200M triangles / sec
- 4 Shader Cores: 30 GFLOPS
- Halti support

VIVANTE GC320

2D-Composition

- GPU-2Dv1 @500Mhz
- Up to 1G pixels / sec raw performance

OpenGL|ES OpenVG OpenCL DirectX® DirectFB

freescale™ 飞思卡尔

freescale™
飞思卡尔

Introduction

System Boot

Boot Modes and Boot Sources

- Flash Devices
  - NOR flash (using WEIM)
  - OneNand (using WEIM)
  - NAND flash (using NFC)
- Serial ATA (using SATA)
  - Only for 6Quad / 6Dual
- Expansion Devices
  - SD/eSD/SDXC/MMC/eMMC (using USDHC1 / USDHC2 / USDHC3 / USDHC4)
  - I2C (using I2C1 / I2C2 / I2C3)
  - SPI (using eCSPI1 / eCSPI2 / eCSPI3/eCSPI4/eCSPI5)
- Serial Downloader
  - USB (using USB OTG)
- Plug-in Mode
  - For custom / user-defined boot

- Boot modes are set via eFuses
- For development purposes, there is an option to set boot modes via external pins

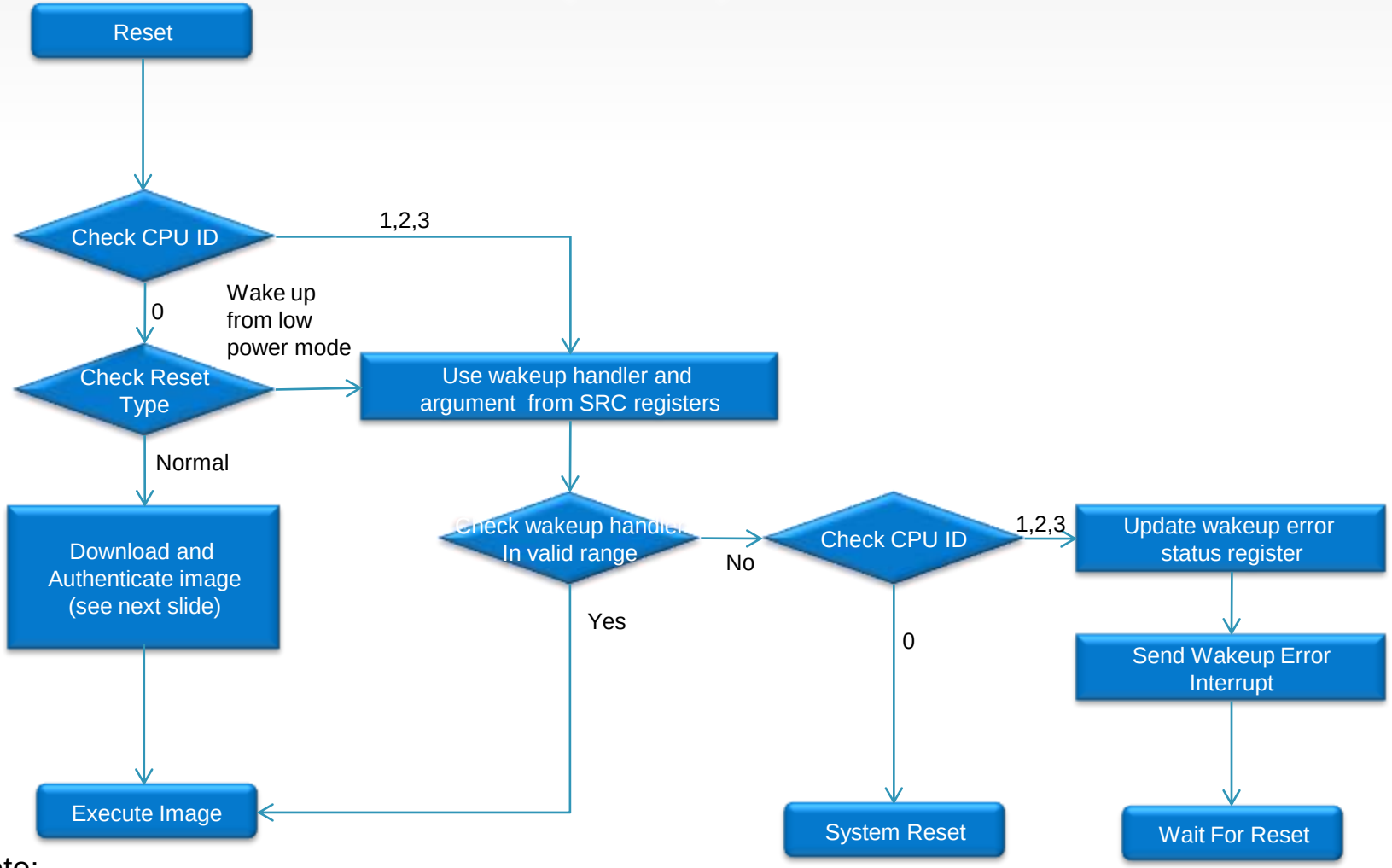
freescale™ 飞思卡尔

Boot Modes

BOOT_MODE[1:0]	Mode	Description
00	Internal Boot (Production)	BT_FUSE_SEL = 0: Boot via USB serial loader, on un-configured parts, indicated by unburned BT_FUSE_SEL fuse. BT_FUSE_SEL = 1: Boot according to fuse values BOOT_CFG, from either of the following sources: • NOR Flash (via WEIM) • OneNAND • SPI (serial flash) / I2C • NAND Flash, MLC NAND 2KB/4KB/8KB page (8-bit). 4-40-bit ECC. • SD3.0/eMMC4.4.1 (support high capacity)/MoviNAND boot (through MMC interface) • SATA (Hard disk or SSD) On error or exception in one of these modes: fallback to USB boot.
01	Serial Downloader	Load and execute code, via USB (HID driver)
10	Internal Boot (Development)	Executing ROM code, which handles booting from various sources (see mode '00' above). BT_FUSE_SEL=0: Boot source is selected by GPIO boot pins (overwrite BOOT_CFG fuses). BT_FUSE_SEL=1: Boot source is selected by BOOT_CFG fuses. GPIO boot pins are ignored On error or exception in one of these modes: fallback to USB boot.
11	FSL Test Mode	Freescale Test Mode, special mode reserved for device testing.

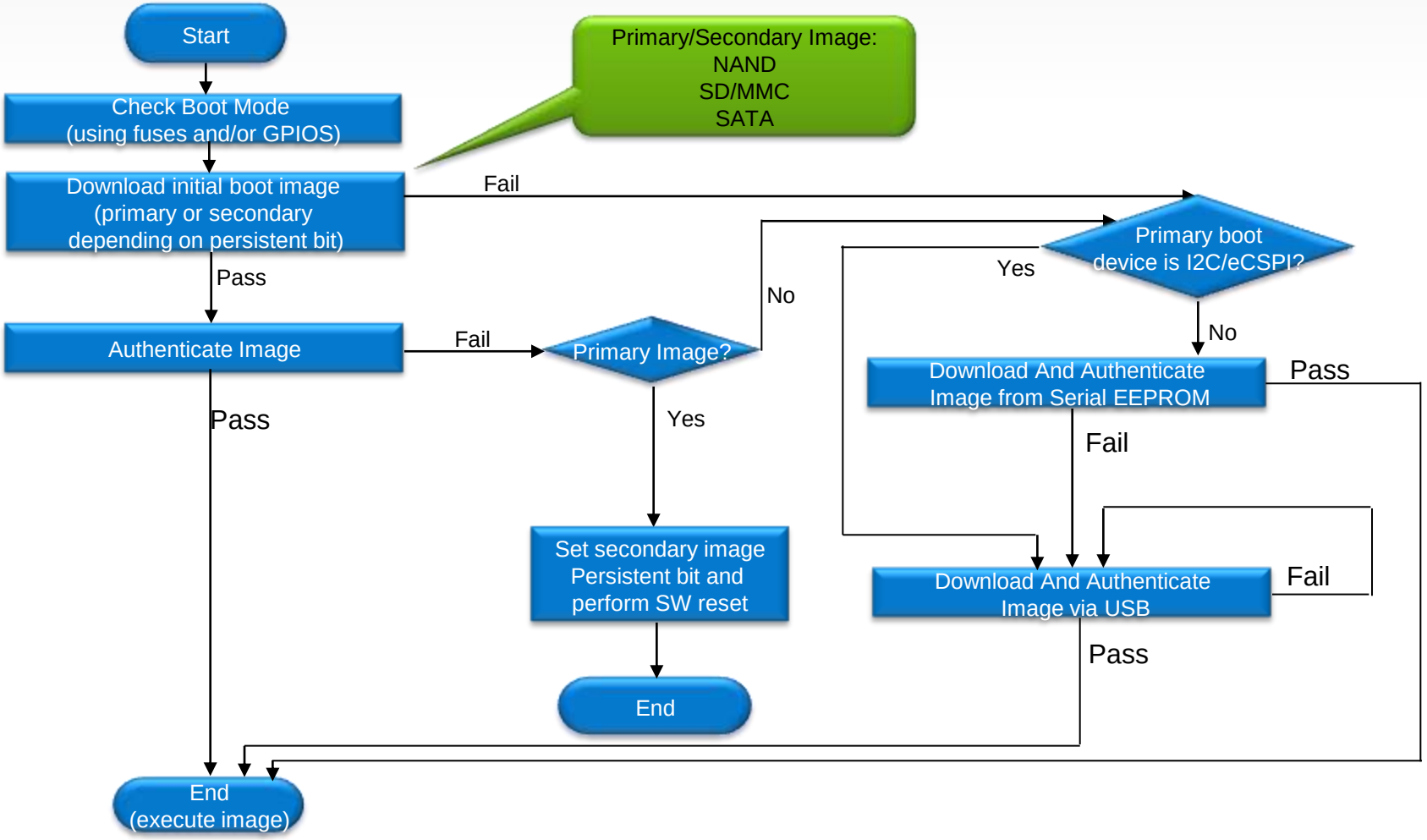
freescale™ 飞思卡尔

Multicore Boot Flow (ROM)



Note:
On reset only CPU0 starts running. Other CPUs clock are gated.
CPU0 is responsible on enabling clocks of other CPUs.

Boot Flow



freescale™
飞思卡尔

Operating System

Release Version Control

...ajor Release Type Definition

Release	Support	Definition	Entry Criteria	Exit Criteria
Alpha Release	**No**	• Not expected to be feature or functionally complete • Customers may start designs, but should not plan to take an Alpha Release into formal integration • Validation executes only BAT • Copyright and License Review (CLR) is required • Very basic Out Of Box Test (OOBT) • Core Team/Marketing approves Release to Customers • Documentation (RN, User Guide) is also Alpha quality	• Features are fully defined • Internal repository mainlined • Unit level test plan reviewed, entry criteria for next phase approved • Basic UC (use case) unit test passes • System test plan reviewed and signed off • Documentation requirements reviewed and signed off	• Core Team/Marketing Approval of unit and BAT issues. • Documentation is updated to reflect the current state of the product
Beta Release	**No**	• Feature and functional complete, may have major bugs or gaps • Release supersedes all previous releases • Qualified by Validation Team • No customer support • Customer issues tracked via CQ (escalated SRs) tickets, reviewed and commitment provided when applicable	• Features included are functional but not necessarily hardened • API finalized • System Test Cases reviewed and signed off • No S1 issues from *unit test*	• No S1 issues • S2 issues require approval by the staff, release and core teams • External Release passes OOBT • Draft publication of release documents reviewed and approved • The SW runs on all supported products and configurations
General Availability Release (GA)	**Full**	• Release supersedes all previous releases • Release is ready for customer integration and production • Long term customer support expected • Internal Release is fully qualified by the validation team at the system level on Freescale board(s) • External Release is fully qualified by the OOBT Team • May include alpha or beta level features but they are not advertised as supported from this release	• Features included are fully functional and hardened • API hardened • No S1/S2 issues during *unit level* testing by Platform • S3 *unit level* testing issues are reviewed by project management, Platform and Validation • Draft publications updated	• No open S1 or S2 issues • S3 issues require approval by the staff and release teams • External Release passes Out Of Box Test (OOBT) • Release documentation reviewed and approved

freescale™ 飞思卡尔

Demo, Patch & Minor Release Definition

Release	Definition	Entry Criteria	Exit Criteria
Demo Release	• Specific feature(s) pre-alpha demo • Not validated, only tagged • First silicon or new major/targeted feature/upgrade - may not be committed • Only images are available, no source code distribution • Code may not necessarily be in Git mainline	• Feature demonstrable	• Requestor/marketing approval • S1/S2 issues likely to be present
Patch Release	• Legacy Support, bug fix only • Fixes for one or more specific issues usually reported by the customer • Fix is tested in the customer HW when applicable • Limited Regression testing in FSL HW	• Code Complete • Test plan reviewed and approved • Draft Patch Release Notes Document • RM changes logged into CQ for next release if necessary	• Passes in customer HW (when applicable) • No new S1/S2 issues from regression testing • Patch Release Document reviewed and approved
Minor Release	• Legacy Support, includes new functionality and all patches to-date • Periodic Release for legacy products past mass production • Supersede all previous releases • Process is similar to that of a GA release • Internal Release is functionally qualified by the validation team at the system level • External Release is fully qualified by the Out Of Box Test (OOBT) Team	• Predefined periodic schedule: – Quarterly for 'new devices' – Biyearly for 'recent devices' – Yearly for 'mature devices' • OR when a critical patch affecting all customers is found	• No open S1 or S2 issues • S3 issues require approval by the staff and release teams • External Release passes Sanity Testing • Release documentation reviewed, tested and approved

freescale™ 飞思卡尔

Generic Release Versioning (Semantic)

X.Y.Z-[alpha | beta].n-[rcm]
1.0.0-[alpha | beta].n-[rcm]

Possible Release Sequence:

1.0.0-alpha – External Release
- *1.0.0-alpha-rc1 – not releasable*
- *1.0.0-alpha-rc2 – not releasable*

1.0.0-beta – External Release
- *1.0.0-beta-rc1 – not releasable*
- *1.0.0-beta-rc2 – not releasable*

1.0.0-beta.1 – Allows for more than 1 beta or alpha release

1.0.0
- *1.0.0-rc1 – not releasable – 1st GA RC*
- *1.0.0-rc2 – not releasable – 2nd GA RC*

1.0.1
1.0.2
1.1.0
1.1.1
2.0.0

X Major
Backwards Incompatible Changes

Y Minor
Backwards Compatible
* New Functionality
* Deprecated Functionality
* Substantial Improvement (ie support new board)

Z Patch
Backwards Compatible Bug Fixes

freescale™ 飞思卡尔

Linux Release Version

Linux Release Name:	LVersion_X.Y.Z
	L3.0.35_2.0.0
Linux Release Pkg:	LVersion_X.Y.Z_yyyymmdd.tar.gz
	L3.0.35_2.0.0_20121106.tar.gz

L3.0.35_12.09.01_GA MX 6DQ :Exception already delivered (L3.0.35_1.0.0)
L3.0.35_12.10.02_GA MX 6SL :Exception about to be delivered (L3.0.35_2.0.0)

L3.0.35_1.1.0	MX 6DQ	:New functionality (current Post GA)
L3.0.35_1.1.1	MX 6DQ	:Example patch release (bug fix)
L3.0.35_2.1.0	MX 6SL	:Post GA Minor Release (example)
L3.0.35_3.0.0	MX6 DLS	:Current L3.0.35_12.11.01_GA
L3.0.35_4.0.0	MX6 DQ & DL/S	:Unified release (example)
L3.0.49_1.2.0	MX6DQ	:Compatible kernel upgrade (example)
L3.0.49_3.1.0	MX6DL/S	:Compatible kernel upgrade (example)
L3.5.7_1.0.0	MX 6DQ	:Incompatible Kernel Upgrade (Reset Major to 1)

freescale™ 飞思卡尔

Android Release Version

Android Release Name: CodeNameVersion_X.Y.Z

JB4.1.2_1.0.0

Android Release Pkg: Android_CodeNameVersion_X.Y.Z_yyyymmdd.tar.gz

Android_JB4.1.2_1.0.0_20130114.tar.gz

13.4.1	ICS 6 DQ, DL/S	:Exception, 13.4 already released
13.5.0	ICS 6 SL	:Exception 13.5 Beta already released
14.0.0	ICS 53	:Exception, early release in March 2012
JB4.1.2_1.0.0		:First JB release, reset major to 1 (current 15.0.0)
JB4.1.2_1.1.0		:Post GA (new functionality)
JB4.1.2_2.0.0		:Same JB version, upgrade kernel version
JB4.2_1.0.0		:New JB version (customers may not want to upgrade)
KLPx.y.z_1.0.0-beta		:Beta release of first Key Lime Pie, reset Major to 1
KLPx.y.z_1.0.0		:First GA Key Lime Pie release, 1.0.0

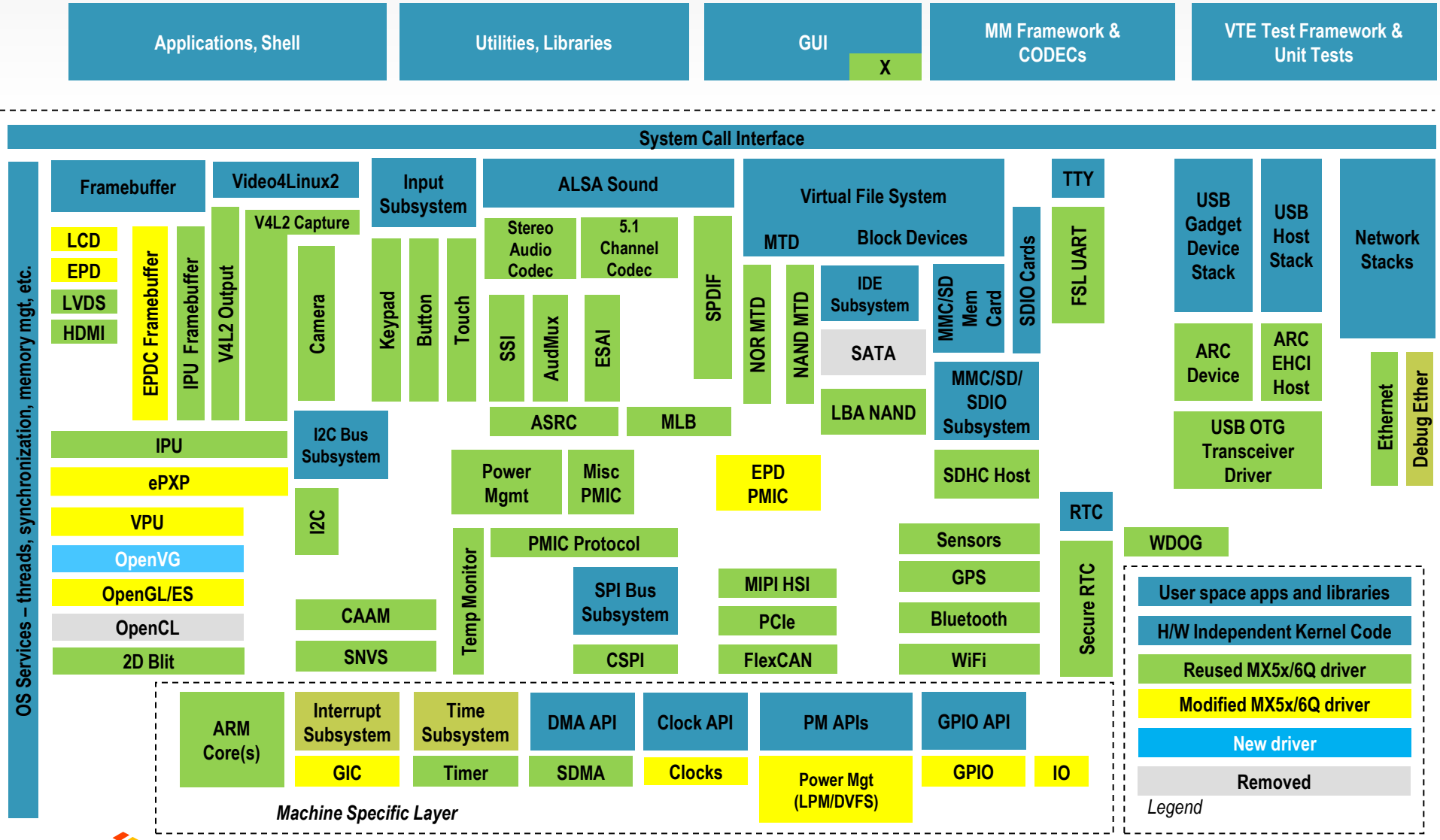
freescale™ 飞思卡尔

Operating System

Linux (LTIB & Yocto)

nux Driver Similarity

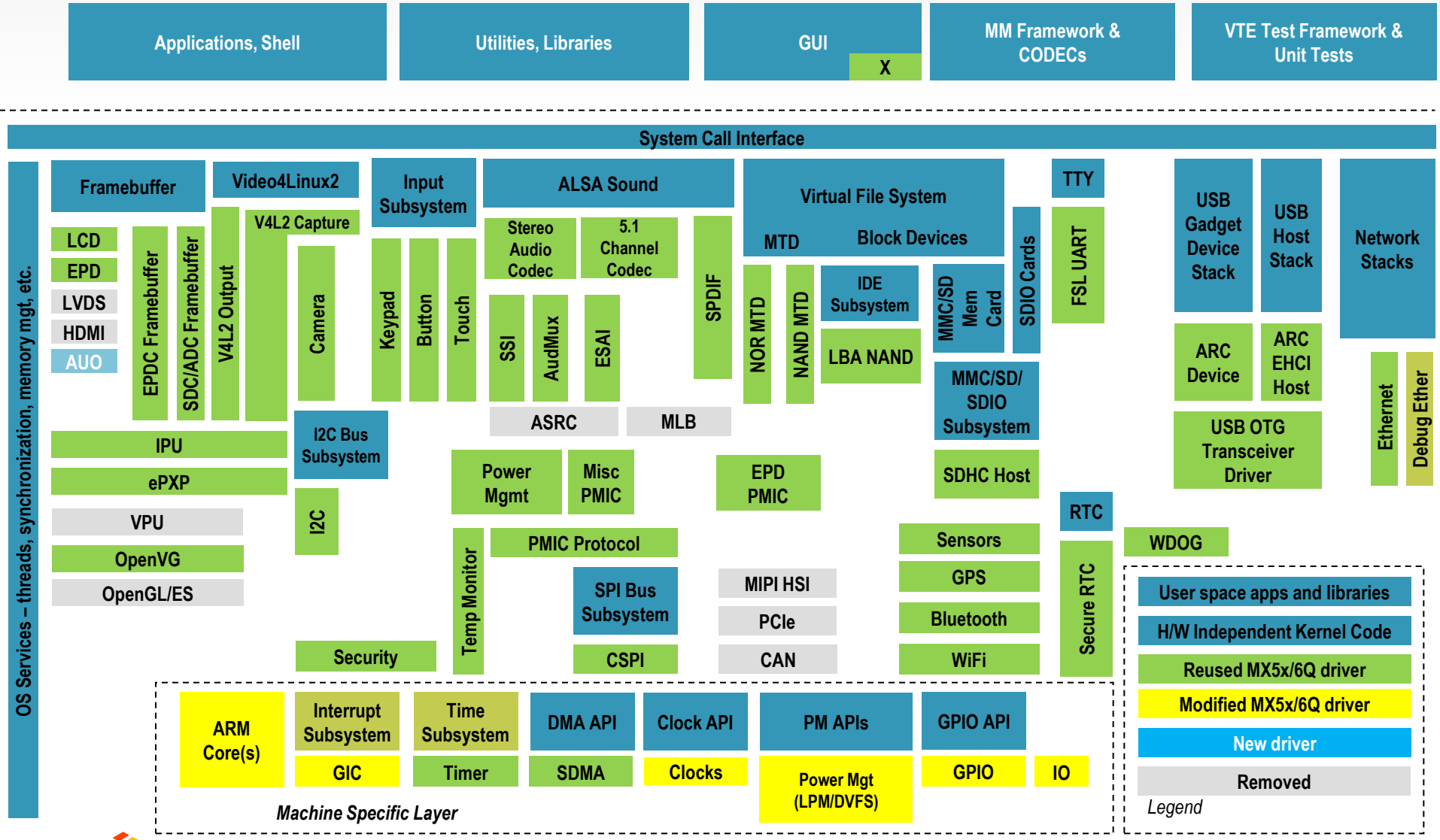
i.MX 6DualLite/Solo Compared to i.MX 6Quad/Dual Linux BSP Drivers



freescale™ 飞思卡尔

nux Driver Similarity

i.MX 6SoloLite Compared to i.MX 6Solo Linux BSP Drivers



Software Completeness

Ecosystem

Applications/ HMI

UI | Games | Apps | Browser | Launcher

Partners

Segment Specific

Auto infotainment
- Fast boot
- Connectivity
- MARS, GenIVI

eReaders
- EPD optimizations
- Adobe PDF Reader

Tablets
- Flash AIR
- Skype
- Player tuning

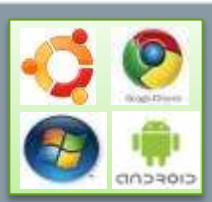
Middleware Layer

- Optimized OpenGL/ES
- Codec parsers
- Power management hooks
- Flash10

Graphics Libraries | Media Framework | Power Management | Security / DRM

OS Layer

- Optimized drivers
- Codec bundle
- Common code base
- Latest kernels



Drivers | Accelerated Codecs | Bootloader | Kernel

Hardware

i.MX PLATFORM

Freescale focus

What is LTIB?

- Linux Target Image Builder (LTIB) is a tool created by Freescale that is used to build Linux target images, composed of a set of packages
  - A mechanism to deliver Linux board support packages (BSPs)
  - A wrapper around tool chains and standard Linux commands (cp, make, objcopy, tar, gcc, …)
- Provides:
  - A known working configuration for a target board
  - Functionality to configure and build Linux system components (kernel, bootloader, application packages, …)

Typical LTIB Cycle

1. Download packages from the network/Internet/local repository
2. Build kernel, boot loader, and application packages from source
3. Deploy built packages to a root file system (RFS) tree
4. Prepare appropriate kernel or RFS image files ready for network or flash-based use on the embedded target board
5. Capture source modifications into patches and auto update the .spec files

LTIB Build Host Setup

- LTIB is very picky and will likely not work unless the build environment is correct. Known to work with
  - Ubuntu 9.04 (Jaunty) Desktop
  - Ubuntu 10.04 (Lucid) Desktop
  - Both the 32 Bit and the 64 Bit install from the Desktop CD are supported
  - Other versions of Ubuntu are not supported and may have build issues
- Follow instructions listed in the document “Setting_up_LTIB_Host_L3.0.35_1.1.0.pdf” included in the BSP documentation package

Installing and Building LTIB

- Remove all previously-installed packages in /opt/freescale/pkgs/.
- Install the LTIB package, not as root, in a location such as /home/user/.

  tar zxvf L3.0.35_1.1.0_121218_source.tar.gz

  ./L3.0.35_1.1.0_121218_source/install
- Config the LTIB

  cd <LTIB directory>

  ./ltib -m config
- Select platform to Freescale iMX reference boards and exit, saving the changes.
- To build U-Boot for target board, select “Choose your board for U-Boot” such as “mx6q_sabreauto”.
- Close the configuration screen saving the changes.
- Run the following command to build LTIB.

  ./ltib
- When this procedure is completed, the kernel image and the U-Boot images are located at: rootfs/boot/.

freescale™ 飞思卡尔

Useful LTIB Commands

- ./ltib -m selectype

  Change the profile after the first selection.

  Min profile, FSL gnome release packages, and mfg firmware profile

- ./ltib –help

- ./ltib –m listpkgs

  List the packages in LTIB

- ./ltib -m prep -p <package name>

  Get the source code of one package. The source code will be extracted to <ltib folder>/rpm/BUILD

- ./ltib -m scbuild -p <package name>

  This command is used to build the source code of <package name>. If you modify the source code, you can rebuild the source code by this command

- ./ltib -m scdeploy -p <package name>

  Install one package to rootfs

freescale™ 飞思卡尔

What is Yocto?

- The Yocto Project™ is an open source collaboration project that provides templates, tools and methods to help you create custom Linux-based systems for embedded products regardless of the hardware architecture.

- It consist of several separate projects to achieve the above goals

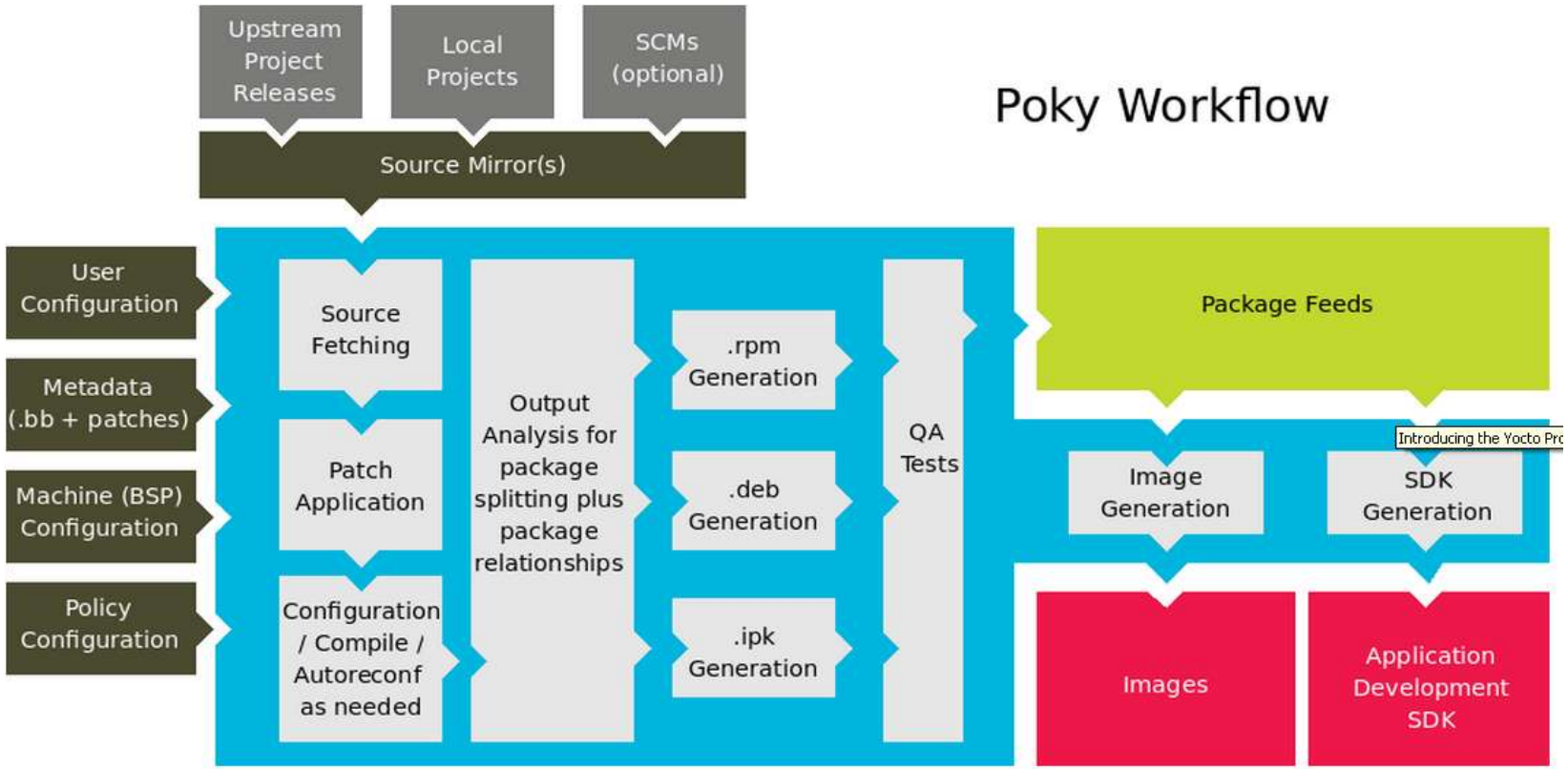
- In principal it is a typical open source project such as Linux or u-boot and consist of many individual contributors as well as companies making contributions (e.g. Intel, TI, Wind River, Mentor, etc)

Yocto projects

- Bitbake
  - Parses metadata to run tasks
- OpenEmbedded Core
  - Core metadata and build information to build baseline embedded system
- Poky
  - Yocto example distribution which integrates all the required pieces and makes an official release
- HOB
  - GUI tool to select packages to build and easily create custom image
- Others: cross-prelink, eclipse IDE plugin, pseudo, and more…

Poky Workflow

Fully supports a wide range of hardware and device emulation through the QEMU Emulator



The Yocto Project Development Environment

Build with Yocto

- Yocto Build Host Setup

  http://www.yoctoproject.org/docs/1.0/yocto-quick-start/yocto-project-qs.html

- Getting Yocto build framework

  git clone git://git.yoctoproject.org/poky.git

- Getting Freescale meta layer

  git clone git://github.com/Freescale/meta-fsl-arm.git

  git clone ssh://sw-git.freescale.net/git/sw_git/repos/meta-fsl-mx.git

- Initializing the build environment

  source oe-init-build-env

- Configure Yocto build for target board

conf/local.conf	User local config file
conf/bblayers.conf	Enables multiple meta layers

- Build the minimal image

  bitbake core-image-minimal

- Build specific packages

  bitbake gst-meta-base -c compile –f

  bitbake gst-meta-base -c clean

- Run the image on emulator

  poky/scripts/runqemu core-image-minimal qemux86

freescale™ 飞思卡尔

freescale™
飞思卡尔

Operating System

Android

Android – Software Stack on Mobile Device

Apps (Java) – Everyone can create his/her own application based on "Open" Android API

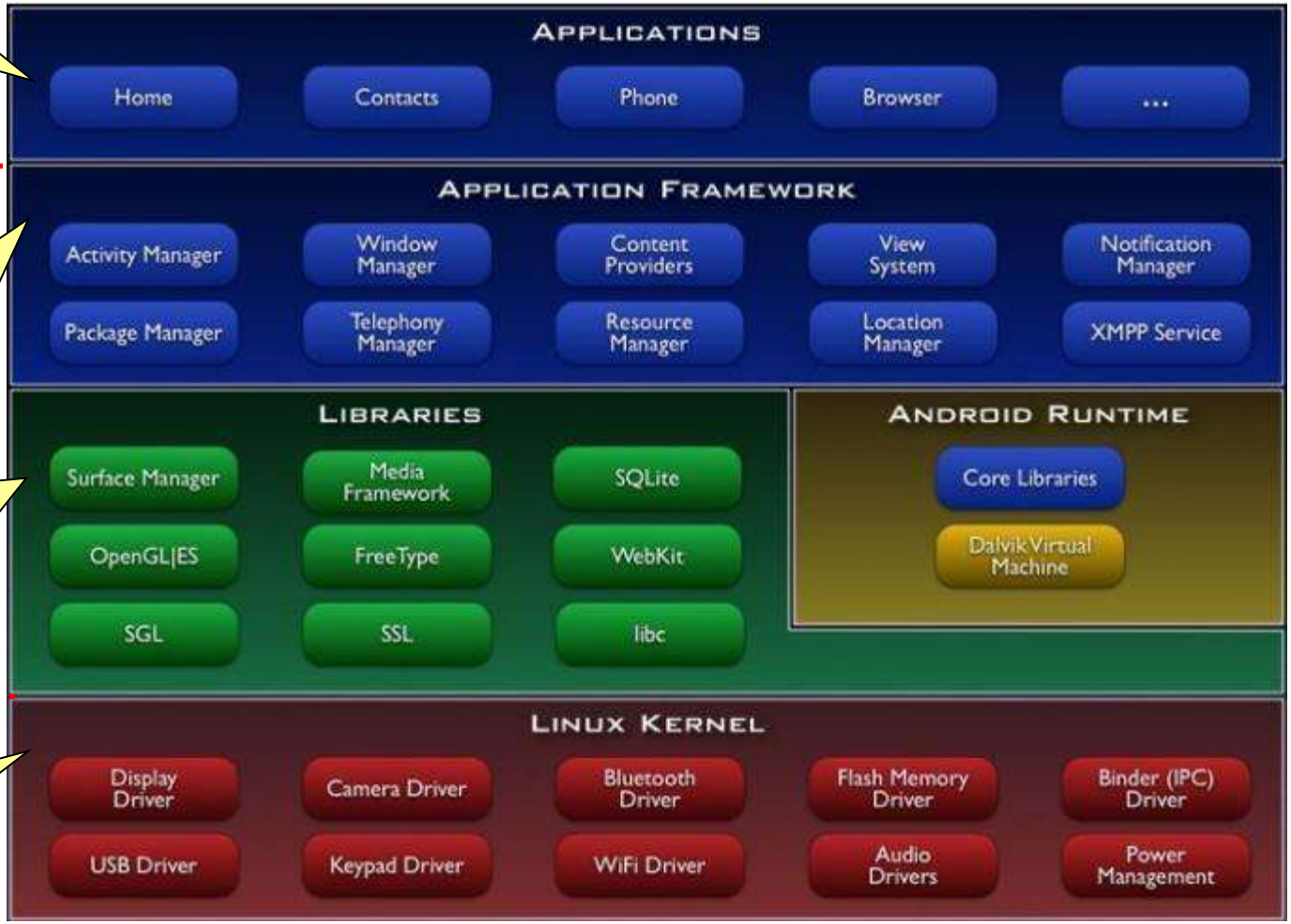
Android "Program" API

Middleware (Java) – App framework including window/focus management, inter-app communication, event notification, etc

Middleware (C/C++) – system libraries for media, graphic, database, font, web engine, etc

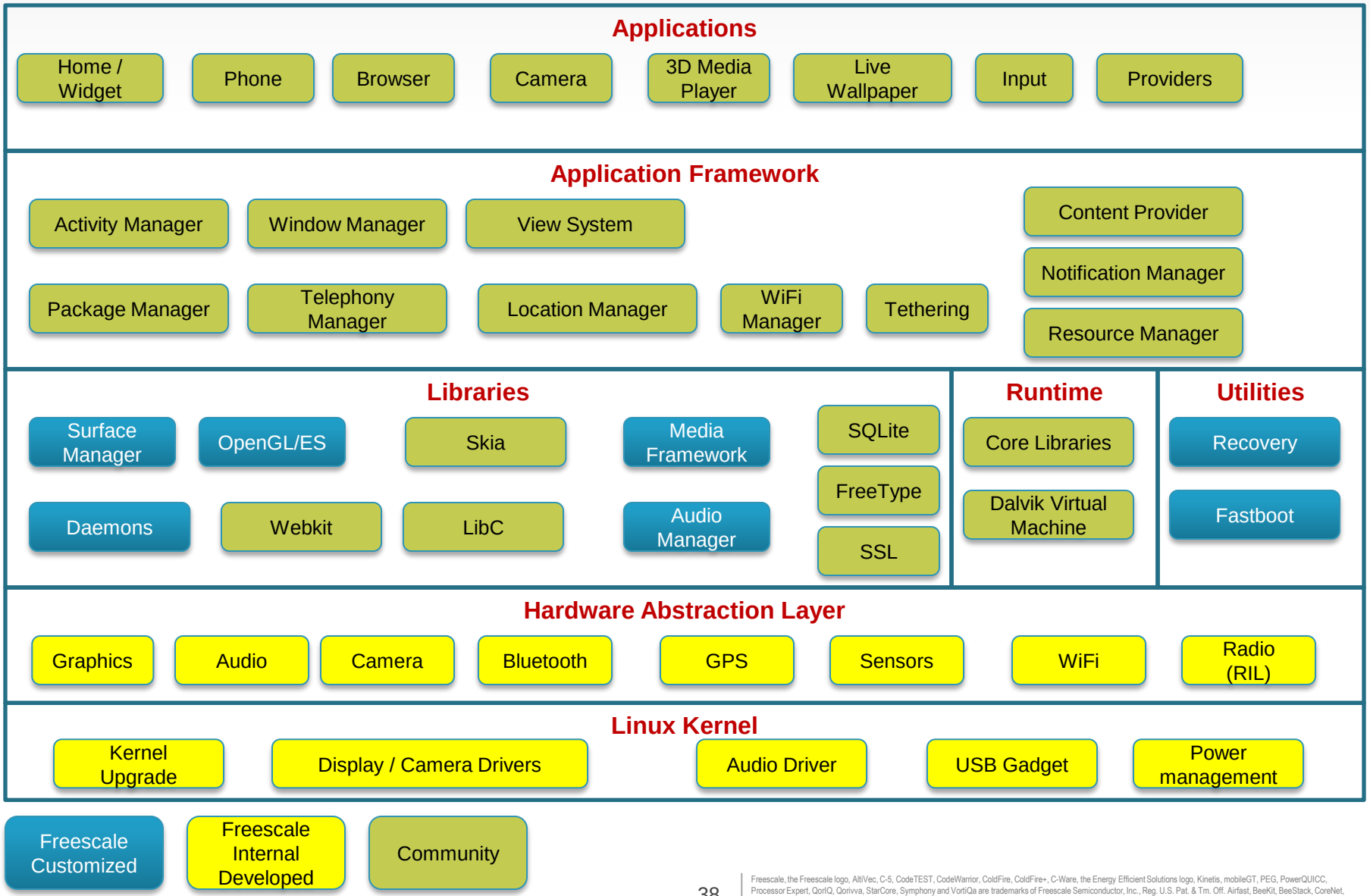
Android "Porting" I/F

Linux kernel with Android patch. "Open Source" already



freescale™ 飞思卡尔

Origin of Android Components



Freescale Android Core Competencies

- **Porting**
  - Variety of FSL and 3rd party drivers integrated into single platform
  - Kernel level and component level optimizations

- **Enhancements**
  - Video and Graphics
  - Software updates, recovery and fastboot
  - 3G modem runtime detection, touch screen calibration

- **Extensions**
  - Flash 10.x / 11.x
  - Media formats
  - Multiple external storage
  - Dual display with auto detection
  - eInk optimizations
  - Complete multimedia framework implementation

Examples of FSL Specific Android Porting

- Kernel
- Tuning HAL with i.MX Kernel
- 3G Modem & Telephony
- Multi-touch
- Bluetooth
- WIFI
- Display devices
- Camera
- G-sensor

freescale™ 飞思卡尔

Examples of FSL Specific Android Enhancements

- Hardware accelerated video decoder/encoder
- Hardware accelerated CSC/Resize/Combining for rendering (especially for video frame rendering)
- Two video/camera rendering acceleration simultaneously
- GPU-based OpenGL/ES implementation
- GPU-based HW copyblt for display surface composition
- GPU-based HW acceleration for surface composition and display
- Software update and factory reset
- 3G modem runtime detection
- Touch screen calibration service
- Freescale optimized software audio decoders/encoders

How To Use FSL Android Release

- **PC Setup**

  Refer to "Setting up your machine" on the Android web site http://source.android.com/source/initializing.html.

- **Unpack i.MX Android Release Package**

  $ cd /opt (or any other directory you like)

  $ tar xzvf imx-android-r13.4-ga.tar.gz

  $ cd imx-android-r13.4-ga/code

  $ tar xzvf r13.4-ga.tar.gz

- **Unpack Google Android release Package**

  $ tar xzvf myandroid_google_20120816.tar.gz

- **Patch Code for i.MX**

  $cd ~/myandroid

  $. /opt/imx-android-r13.4-ga/code/r13.4-ga/and_patch.sh

  $ help

  Now you should see "c_patch" function is available for you

  $ c_patch /opt/imx-android-r13.4-ga/code/r13.4-ga imx_r13.4-ga

freescale™ 飞思卡尔

Build Android Image

- **Build the uboot, kernel, and Android image**

  $ cd ~/myandroid

  $ source build/envsetup.sh

  $ lunch sabresd_6dq-user

  $ make

  "sabresd_6dq" is the product name

  (see ~/myandroid/device/fsl/product)

  After build, check build_*_android.log to make sure no build error.

- **Build out images**

  under myandroid/out/target/product/sabresd_6dq

  boot.img(uImage,ramdisk,boot parameters)

  system.img recovery.img

freescale™
飞思卡尔

Operating System

WinCE & QNX

WinCE/QNX

- **WEC6.0**
  - i.MX2x, i.MX3x, i.MX50, i.MX51 (FSL)
- **WEC7.0**
  - i.MX51, i.MX53 (FSL)
  - i.MX6x (3rd party)
- **QNX**
  - i.MX6x (3rd party)

freescale™ 飞思卡尔

freescale™
飞思卡尔

Hardware Platform

SABRE SD

SABRE Board for Smart Devices (SDB)

i.MX 6Quad 1Ghz Cortex-A9 Processor
- Can be configured as i.MX 6Dual
- Freescale MMPF0100 PMIC
- 1 GB DDR3 memory (non terminated)
- 3” x 7” 8-layer PCB

Display connectors
- 2x LVDS connectors
- Connector for 24 bit 4.3” 800x480 WVGA with 4-wire touch screen
- HDMI Connector

Audio
- Wolfson Audio Codec
- Microphone and headphone jacks

Expansion Connector
- Camera CSI port signals
- I2C, SSI, SPI signals

Part Numbers: MCIMX6Q-SDB ($399)

Display (9.7”): MCIMX-LVDS1 ($499)
Display (4.3”): MCIMX28LCD ($199)

Tools Support
- Lauterbach, ARM (DS-5), Macraigor debug/IDE tool chain

Connectivity
- 2x Full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector

Debug
- JTAG connector
- Serial to USB connector

Additional Features
- 3-axis Freescale accel
- eCompass
- Power supply
- No battery charger

OS Support
- Linux and Android IceCream Sandwich from Freescale;
- Others: support by 3rd parties

freescale™ 飞思卡尔

SABRE Platform for Smart Devices (SDP)

i.MX 6Quad 1GHz Cortex-A9 Processor
i.MX 6DualLite 1GHz Cortex-A9 Processor
- Freescale MMPF0100 PMIC
- 1 GB DDR3 memory (non terminated)
- 3” x 7” 8-layer PCB

Part Numbers: MCIMX6Q-SDP ($999)
MCIMX6DL-SDP ($999)

Display (4.3”): MCIMX28LCD ($199)
WiFi: Silex WiFi module

Display connectors
- Native 1024x768 LVDS display (comes with kit)
- 2nd LVDS connector
- Connector for 24 bit 4.3” 800x480 WVGA with 4-wire touch screen
- HDMI Connector
- MIPI DSI connector

Audio
- Wolfson Audio Codec
- Microphone and headphone jacks
- Dual 1W Speakers

Expansion Connector
- Enables parallel LCD or HDMI output
- Camera CSI port signals
- I2C, SSI, SPI signals

Tools Support
- Lauterbach, ARM (DS-5), Macraigor debug/IDE tool chain

Connectivity
- 2x Full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector

Debug
- JTAG connector
- Serial to USB connector

Additional Features
- 3-axis Freescale accel
- GPS receiver
- Ambient Light Sensor
- eCompass
- Dual 5MP Cameras
- Power supply
- Battery Charger
- Battery connectors

OS Support
- Linux and Android IceCream Sandwich from Freescale;
- Others: support by 3rd parties

freescale™ 飞思卡尔

freescale™
飞思卡尔

Hardware Platform

SABRE AI

SABRE Platform for Automotive Infotainment (AI)

CPU Card Details

- **Power and Memory**
- Freescale MMPF0100 PMIC
- 2 GB DDR3 memory (i.MX 6Dual/Quad)
- 1GB DDR3 memory (i.MX 6Solo)
- 32GB Parallel NOR Flash
- NAND Socket

Display
- LVDS connector
  - compatible with MCIMX-LVDS1
- Parallel RGB display interface
- HDMI output connector

Debug
- JTAG connector
- Debug UART connector

Connectivity and Expansion
- SD Card Slot
- High Speed USB OTG
- Ethernet
- SATA
- MIPI CSI
- PCIe
- MLB150 INIC connector
- 281-pin MXM card edge connector for main board expansion

Part Numbers

Base Board: MCIMXABASEV1 ($699)
CPU Cards: MCIMX6SAICPU1 ($799)
MCIMX6QAICPU1 ($799)
Display: MCIMX-LVDS1 ($499)

Base Board Details

Can be reused from i.MX53 SABRE AI

Connectivity and Expansion
- SD card slot (WiFi module or SD)
- Bluetooth or Bluetooth+WiFi header
- AM/FM tuner header
- Sirius XM Module header (de-pop"d)
- GPS (UART) module connector
- 2x CAN
- Dual High Speed USB Host connectors
- MLB 25/50 INIC connector
- SPI NOR flash

Display I/O
- LVDS connector
  - compatible with MCIMX-LVDS1
- Analog Video Input
- LVDS Input

Audio
- Cirrus multichannel audio codec
  - Up to 8 outputs
  - Dual microphone inputs
  - Stereo Line Level Input
- SPDIF receiver

OS Support
- Linux
- Others: future support by 3rd parties

freescale™ 飞思卡尔

freescale™
飞思卡尔

Develop Tools

ARM Debug

Platform Debug System

The i.MX 6D/6Q debug and trace architecture is designed around the following:

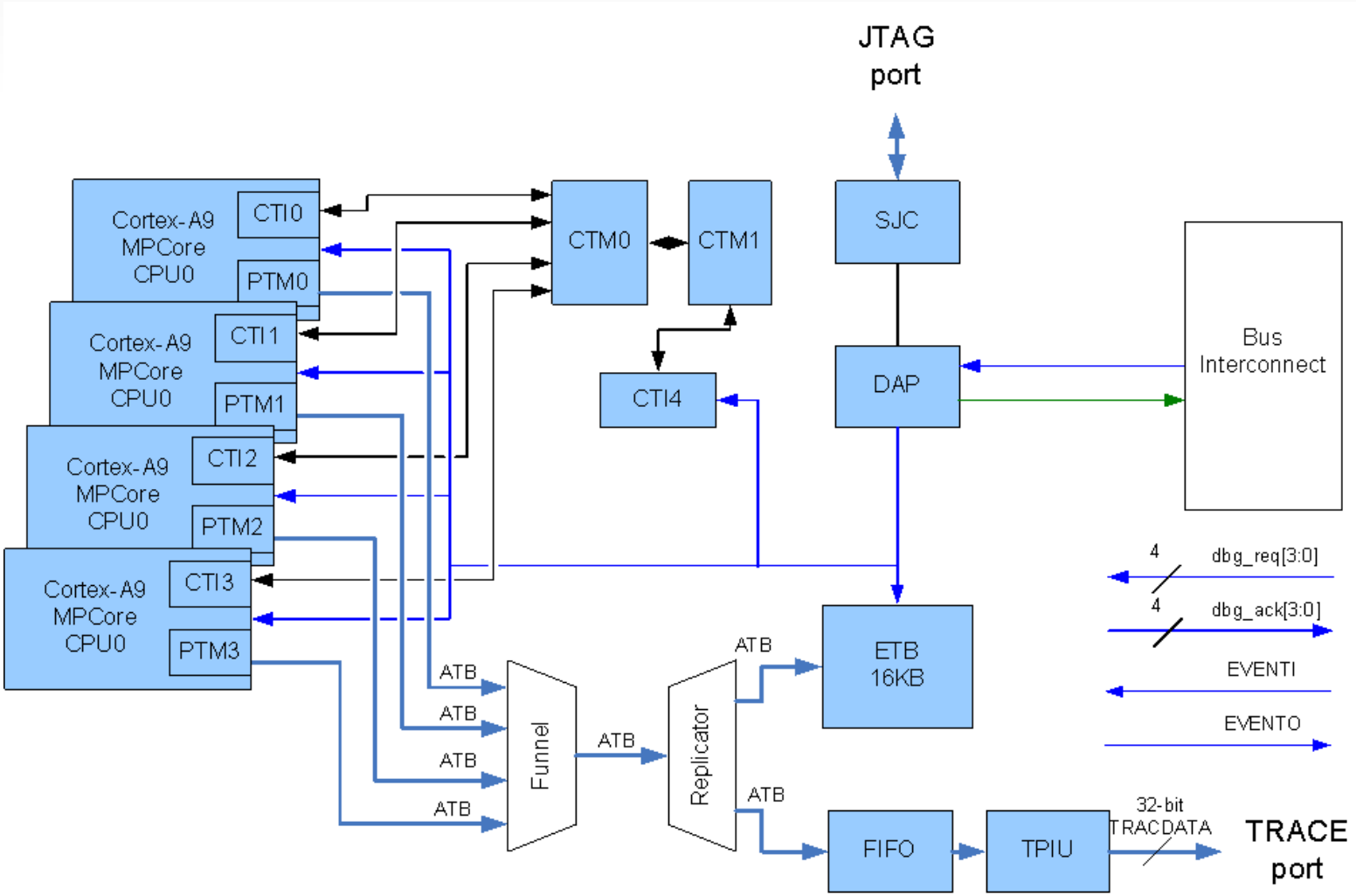
- ARM's CoreSight architecture, adapted to i.MX 6D/6Q SoC (for 2x and 4x core debug).
- JTAG port used to interact with cores under debug, via the System JTAG controller (SJC) port.
- Various SoC system resources, such as signal visibility and debug features built into i.MX 6D/6Q IP's.

CoreSight Components:

- 4x PTM (One per core) – Program Trace Macrocell – For real-time program flow trace, uses TPIU port, for extracting trace data. (Require added Trace-Box HW, to capture and proccess the traces). The PTM is a replacement of ETM, used with A8 core system.
- Embedded Trace Buffer (ETB) - 16 Kbyte RAM array to be used for on-chip capture of trace data output from the PTM
- ATB Replicator to connect the trace data to TPIU (Trace Port Interface) and ETB (Embedded Trace Buffer).
- TPIU – Trace Port Interface, used for routing internal busses, to "Trace Port" signals.
- ATB Funnel - for capturing trace data from the either two or four cores.
- Cross Triggering logic, for event routing, including CTI's and CTM's.

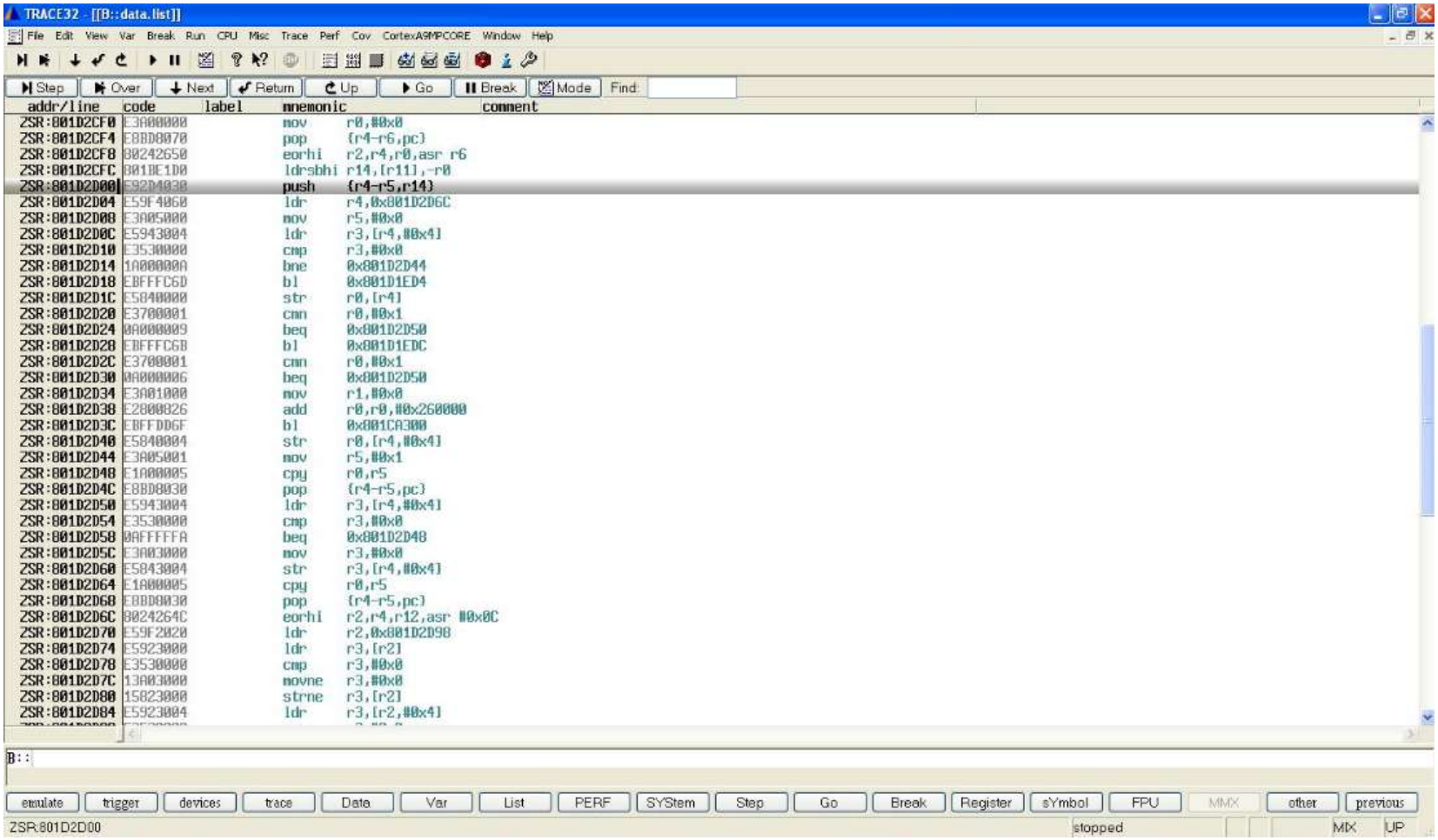
freescale™ 飞思卡尔

Debug Scheme



Debug Scheme

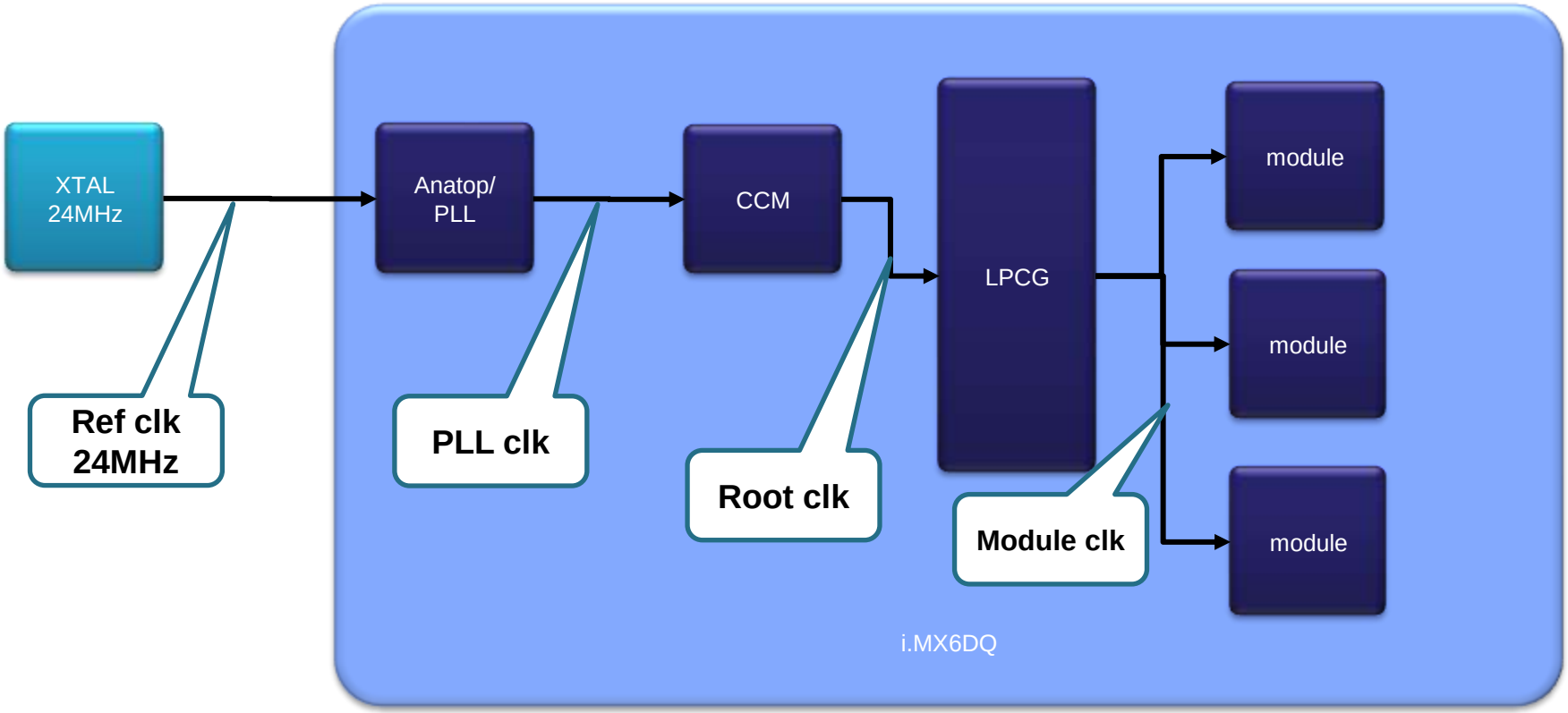
Lauterbach:



freescale™ 飞思卡尔

Clock Generation Scheme

- Clock generation scheme is generally preserved from i.MX37/i.MX51 designs.



Clock Generation Scheme *cont.*

- PLLs now are located in “anatop” module. Anatop module also includes PLL configuration registers.

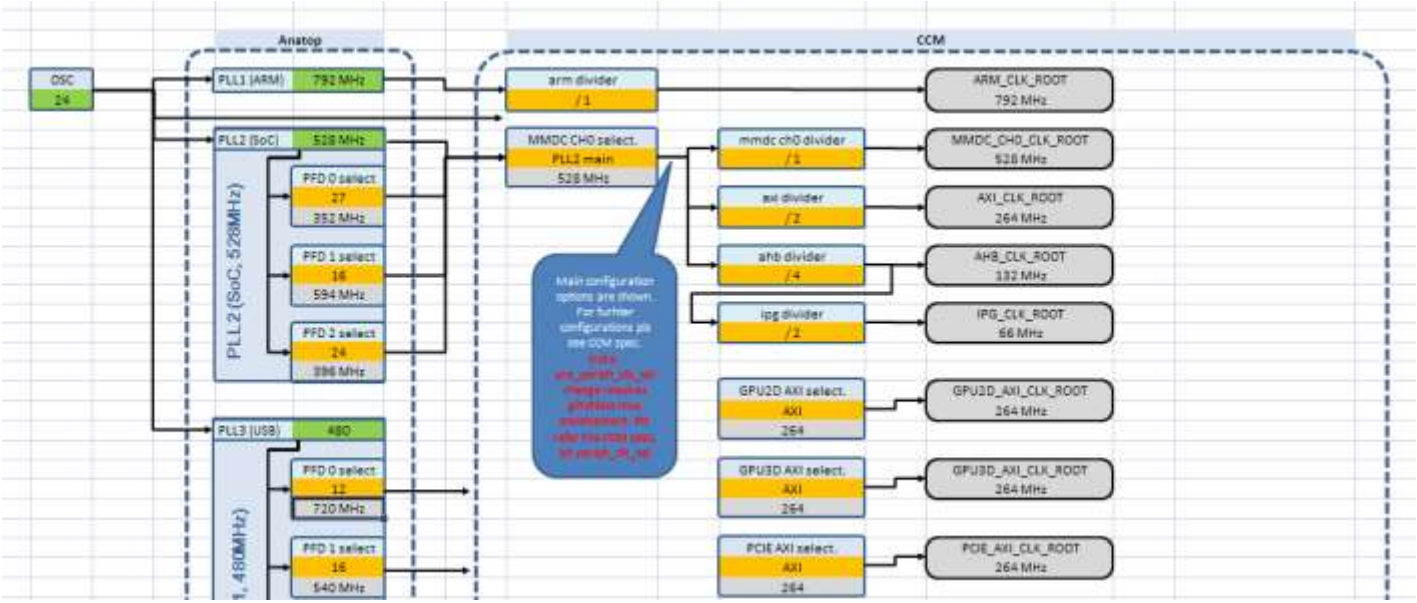
- PLLs have additional output clock named PFD (phase fractional dividers)

  PFD clock depends on the main PLL clock and calculated by Freq(PFD)=Freq(PLL)*18/N where N can range from12-35.

  - Clocks of 5 PLLs are going from anatop through CCM:
    - ARM PLL aka System PLL – PLL1
    - Bus PLL aka 528M PLL – PLL2
    - USB1 PLL aka 480M PLL – PLL3
    - High definition Audio PLL – PLL4
    - High definition Video PLL – PLL5
  - Clocks of 3 PLLs are going from anatop directly to the modules:
    - ENET PLL – PLL6
    - USB2 PLL – PLL7
    - MLB PLL – PLL8

Clock configuration

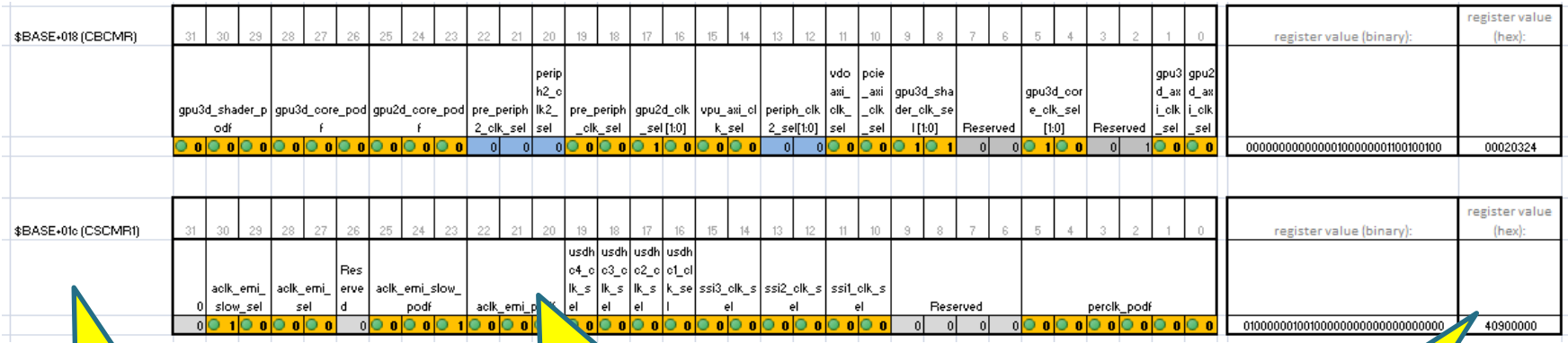
- Since clock configuration raises a lot of questions, a user-friendly tool was generated



- Excel-based tool provides visual configuration w/ drop-down options, while all selected clock frequencies are specified.
- This tool covers clock generation part from XTAL→PLL→CCM.

Clock configuration *cont.*

- Once the clock select is completed on the visual part of the tool, all related PLL(anatop) and CCM's registers values can be seen in the "register value" sheets of the same tool: Link



$BASE+018 (CBCMR)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	register value (binary):	register value (hex):
	gpu3d_shader_podf			gpu3d_core_podf			gpu2d_core_podf			pre_periph2_clk_sel		periph2_clk2_sel	pre_periph_clk_sel		gpu2d_clk_sel [1:0]		vpu_axi_clk_sel		periph_clk2_sel[1:0]		vdoaxi_clk_sel	pcie_axi_clk_sel	gpu3d_shader_clk_sel [1:0]		Reserved		gpu3d_core_clk_sel [1:0]		Reserved		gpu3d_axi_clk_sel	gpu2d_axi_clk_sel	00000000000001000000100100100	00020324
	0	0	0	0	0	0	0	0	0	0		0	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	0	0	1	0	0		

$BASE+01c (CSCMR1)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	register value (binary):	register value (hex):
	0	aclk_emi_slow_sel		aclk_emi_sel		Reserved	aclk_emi_slow_podf			aclk_emi_p			usdhc4_clk_sel	usdhc3_clk_sel	usdhc2_clk_sel	usdhc1_clk_sel	ssi3_clk_sel		ssi2_clk_sel		ssi1_clk_sel		Reserved				perclk_podf								01000000100100000000000000000000	40900000
	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Register name and address offset

Per-field bits values and fields descriptions, following spec.

32bits binary and hex values for each register

freescale™ 飞思卡尔

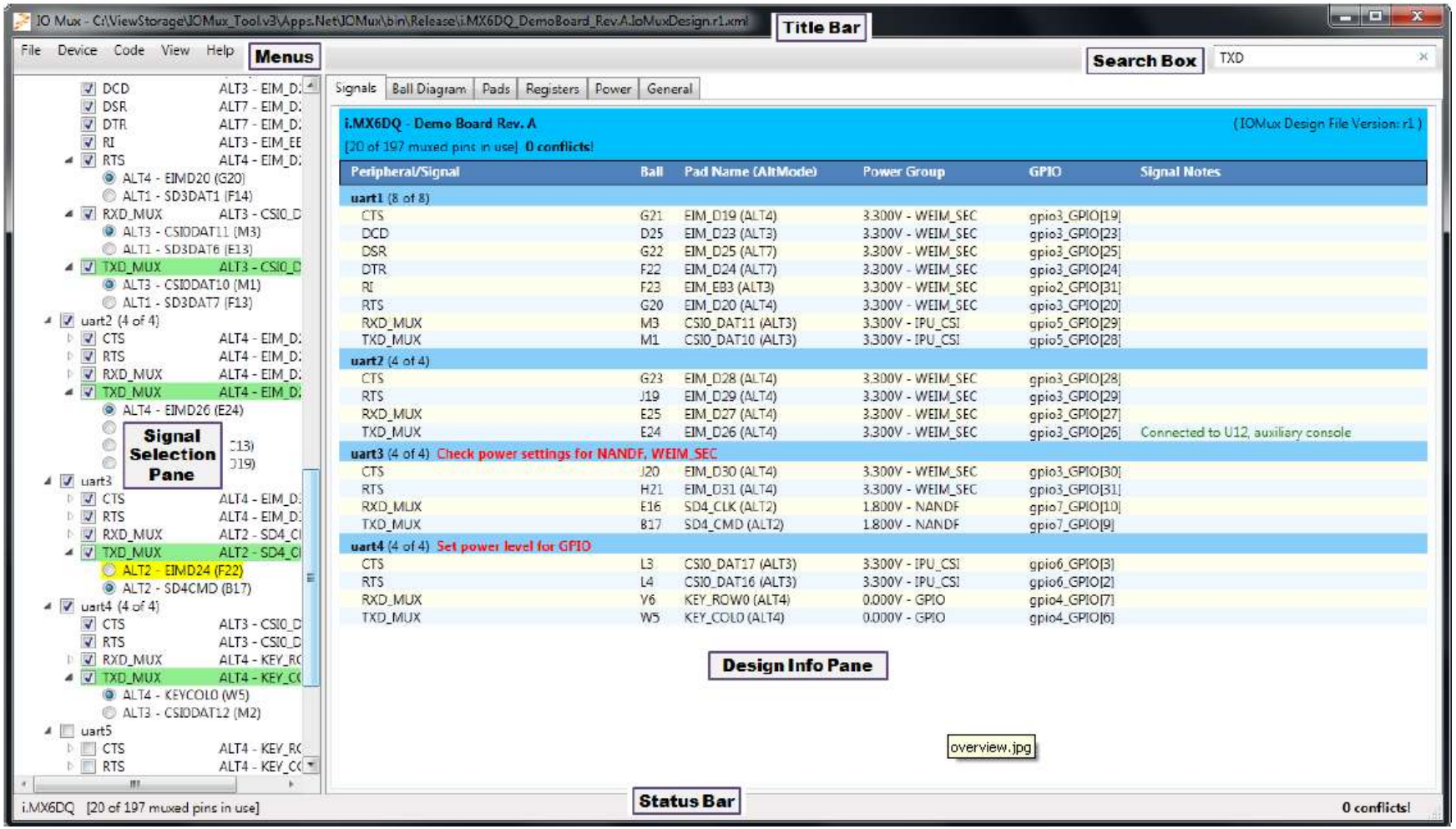
freescale™
飞思卡尔

Develop Tools

IOMUX

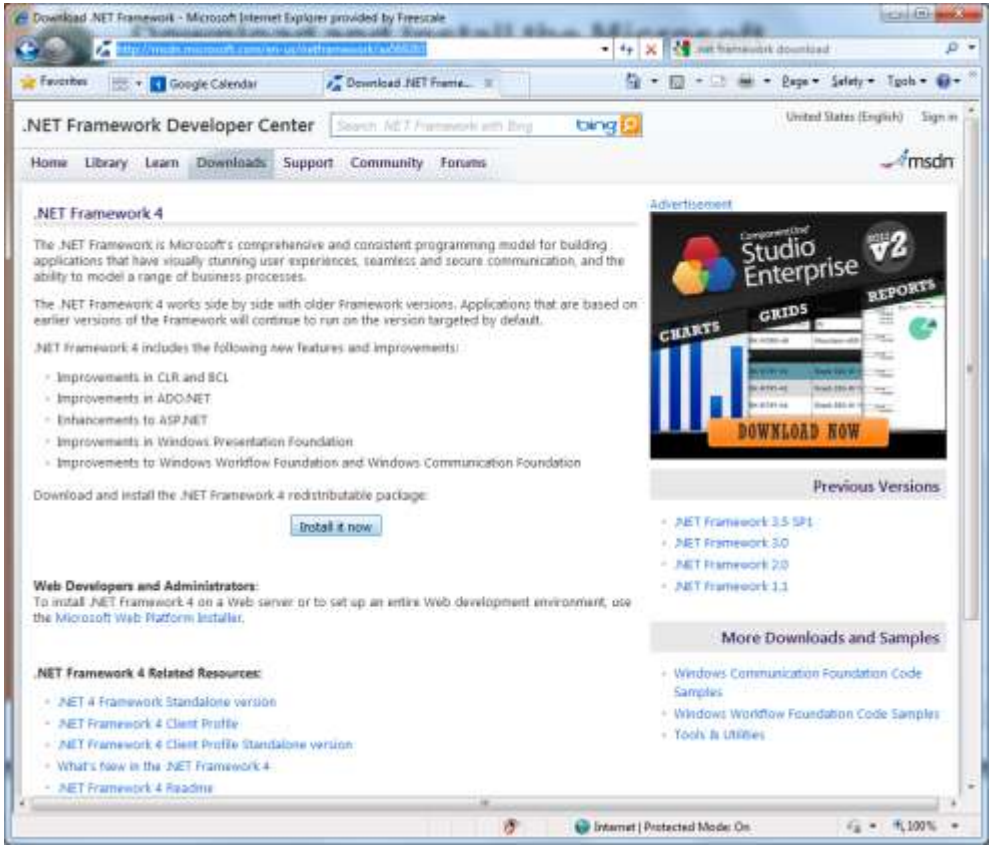
IOMUX Tool

- Application Window Overview



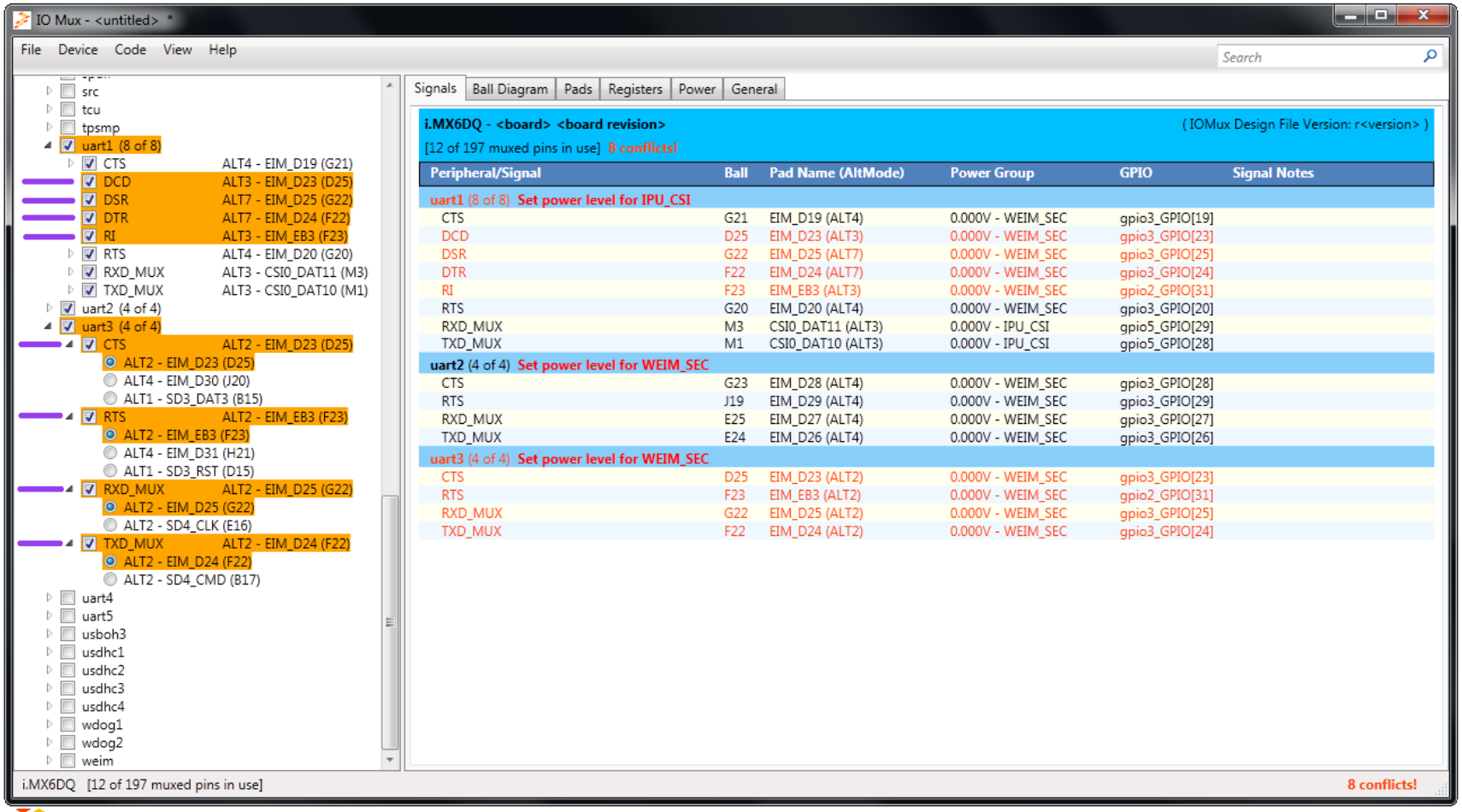
Download and Install the Microsoft .NET Framework 4.0

- http://msdn.microsoft.com/en-us/netframework/aa569263

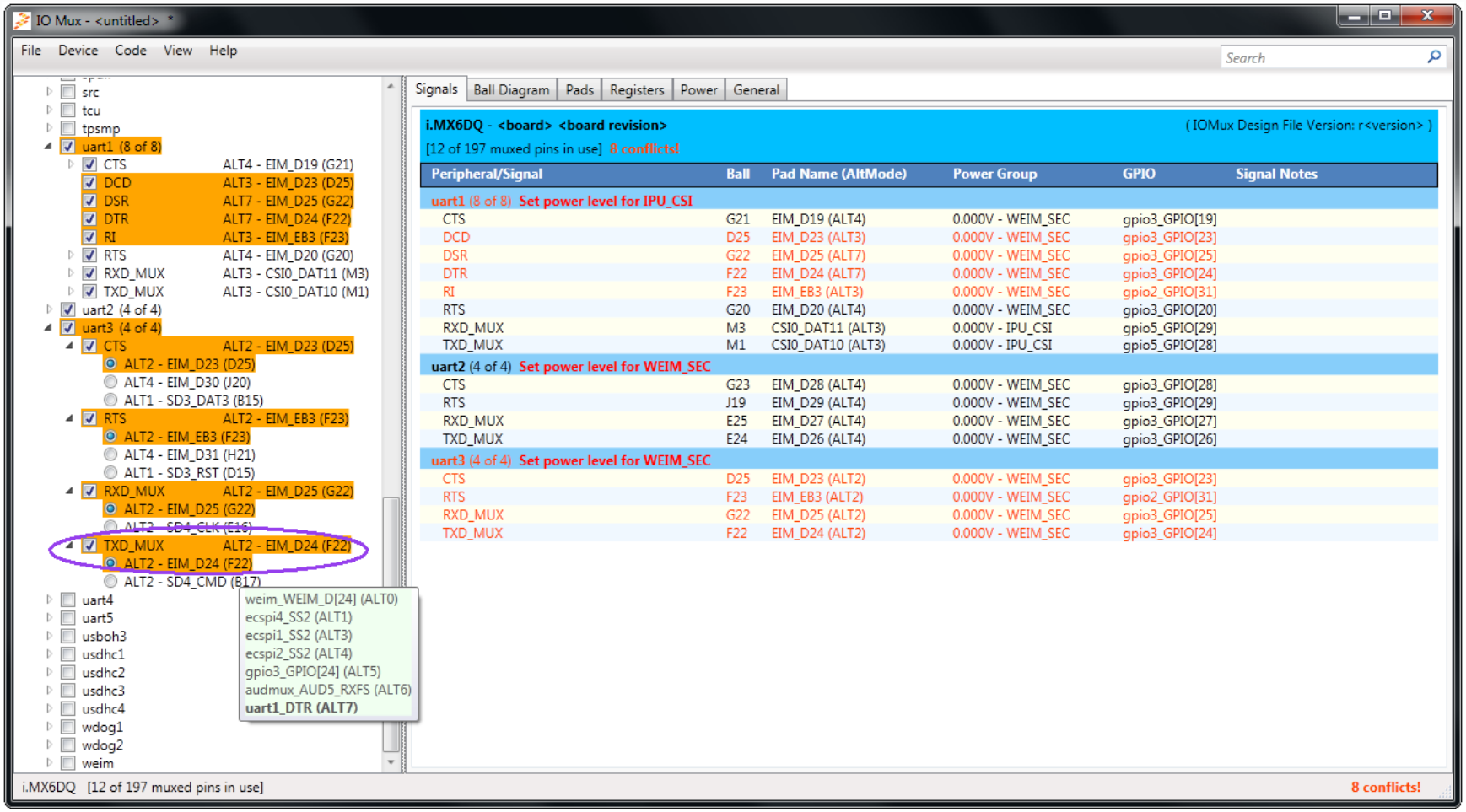


Select Modules and Signals for Board

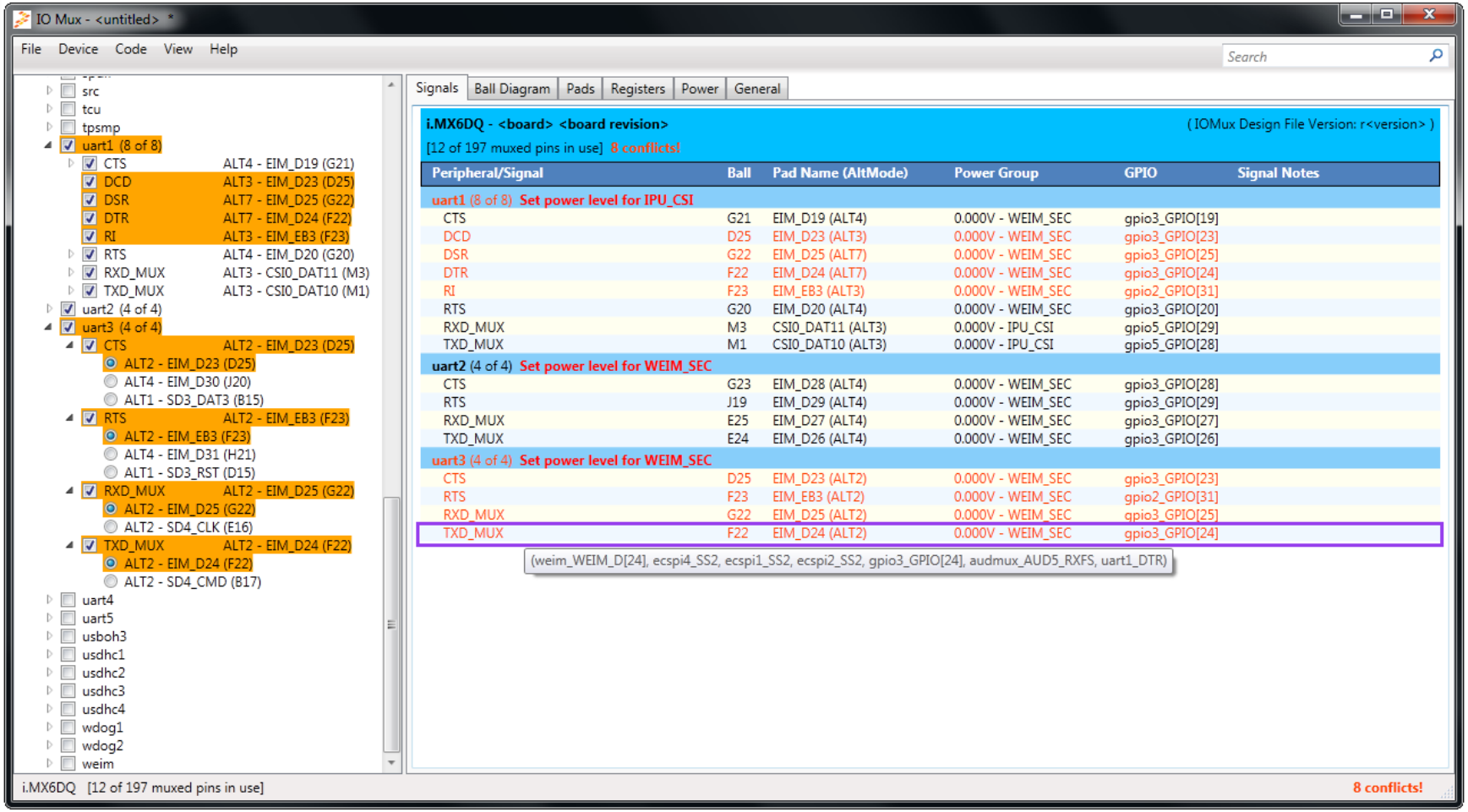
- Check the UARTS: UART1, UART2 and UART3.
- Expand all signals under UART3.



Accessing Muxed-Signal Info



Accessing Muxed-Signal Info



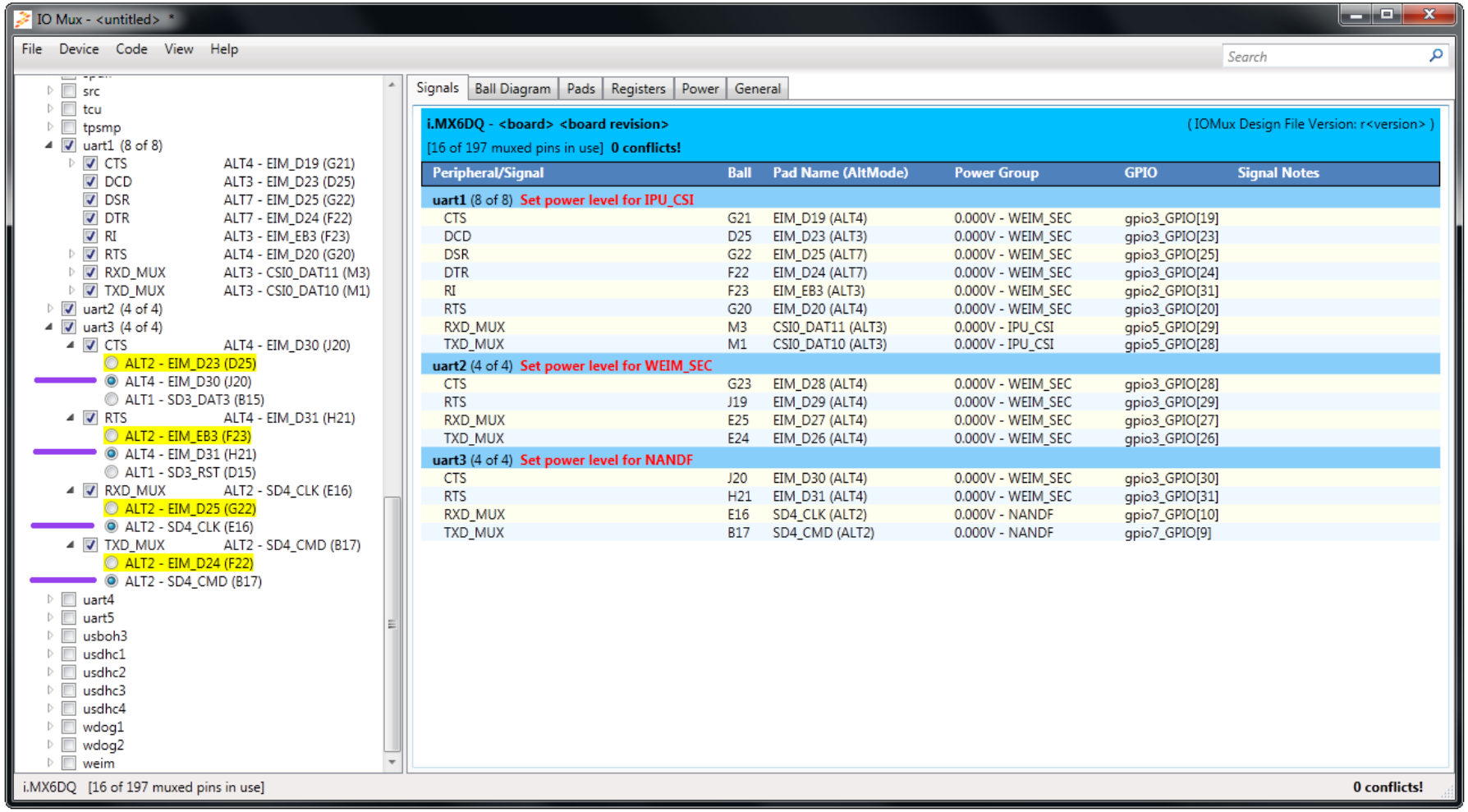
Resolve Conflicting Signals

Select ALT4 – EIM_D30(J20) for UART3/CTS.

Select ALT4 – EIM_D31(H21) for UART3/RTS.

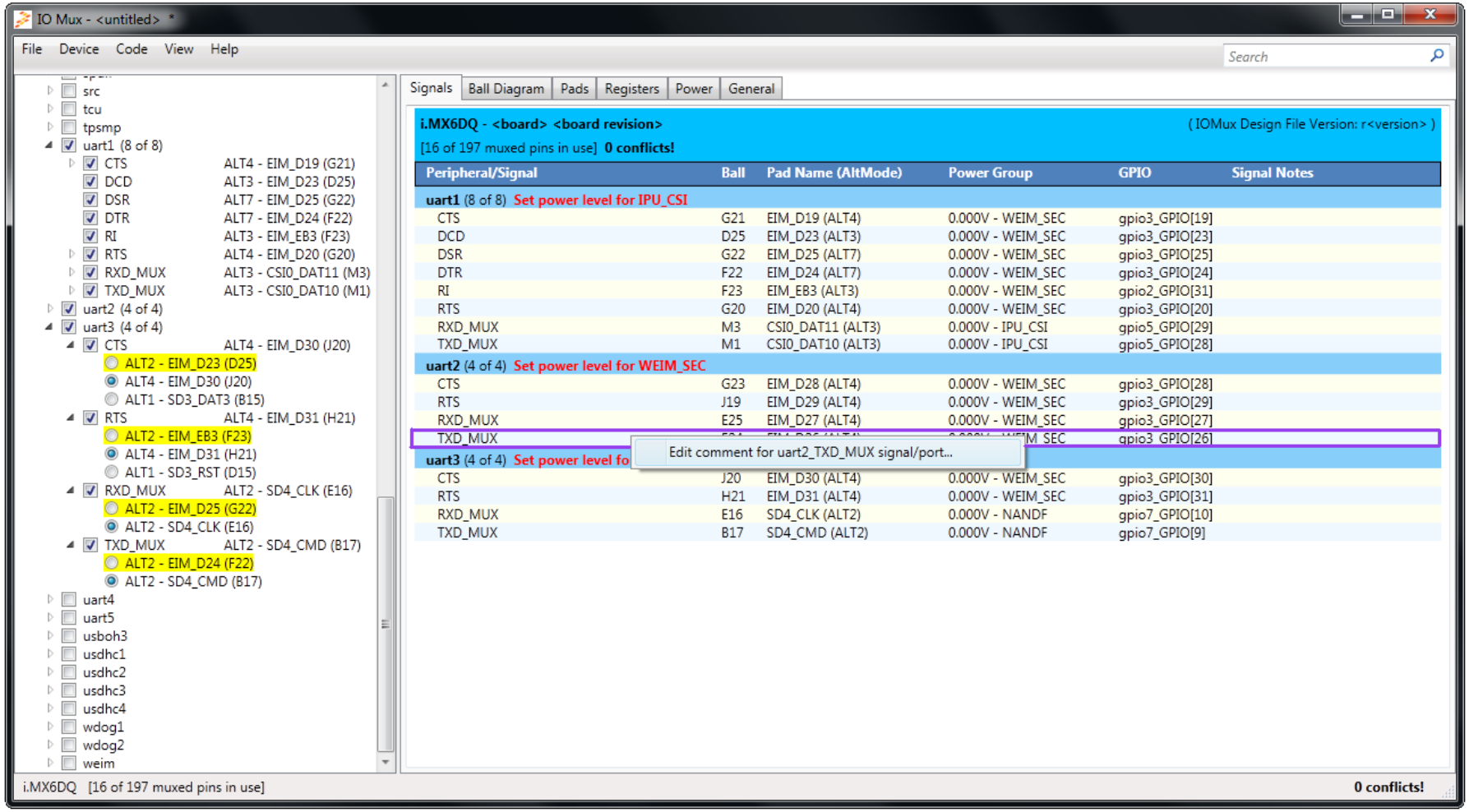
Select ALT2 – SD4_CLK(E16) for UART3/RXD_MUX.

Select ALT2 – SD4_CMD(B17) for UART3/TXD_MUX.

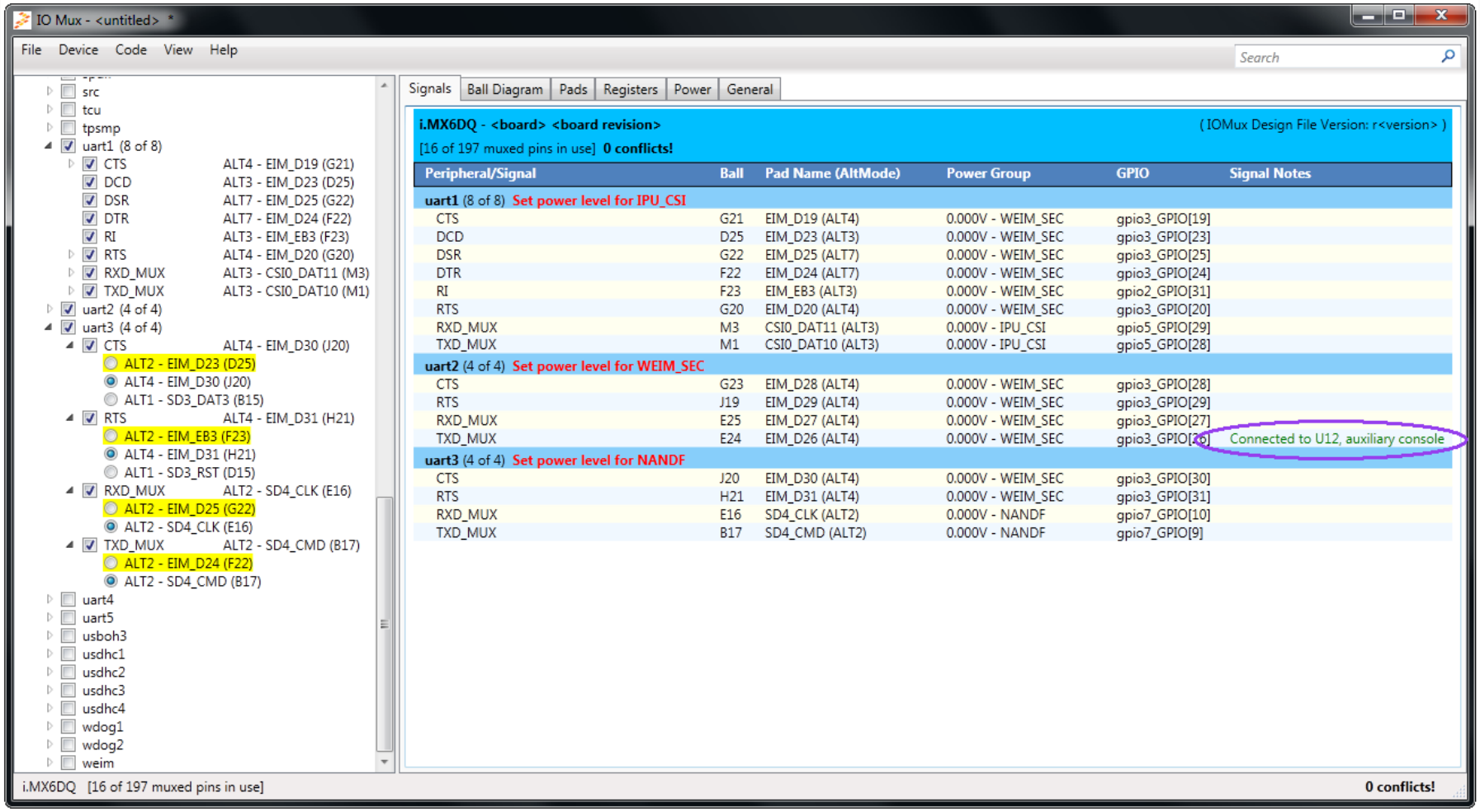


Adding Comments for Clarity

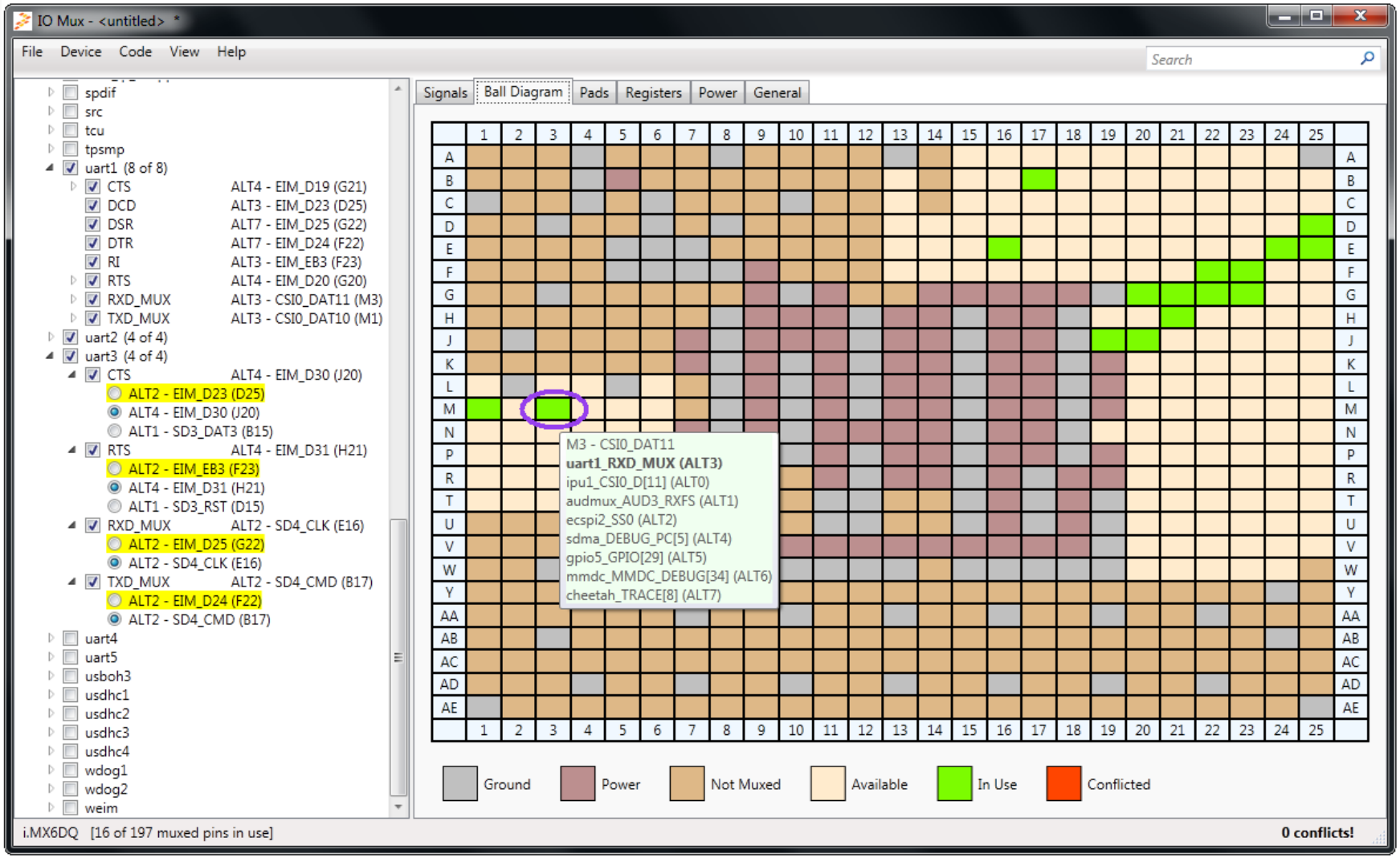
- Right-click the UART2/TXD_MUX row in the Signals tab to bring up the context menu.
- Clicking on the menu will bring up a text entry field where the user may enter text.



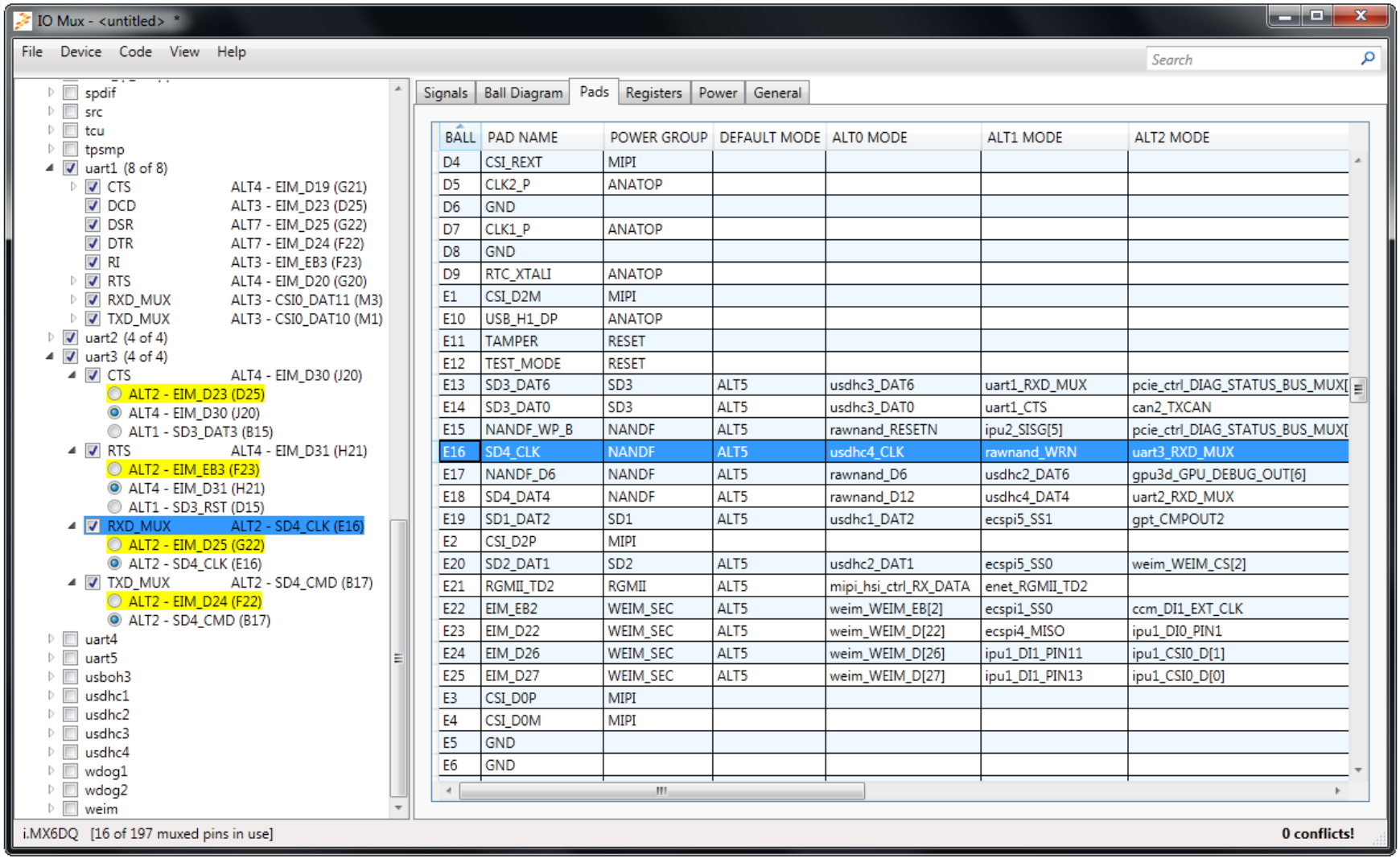
Adding Comments for Clarity



Ball Diagram View

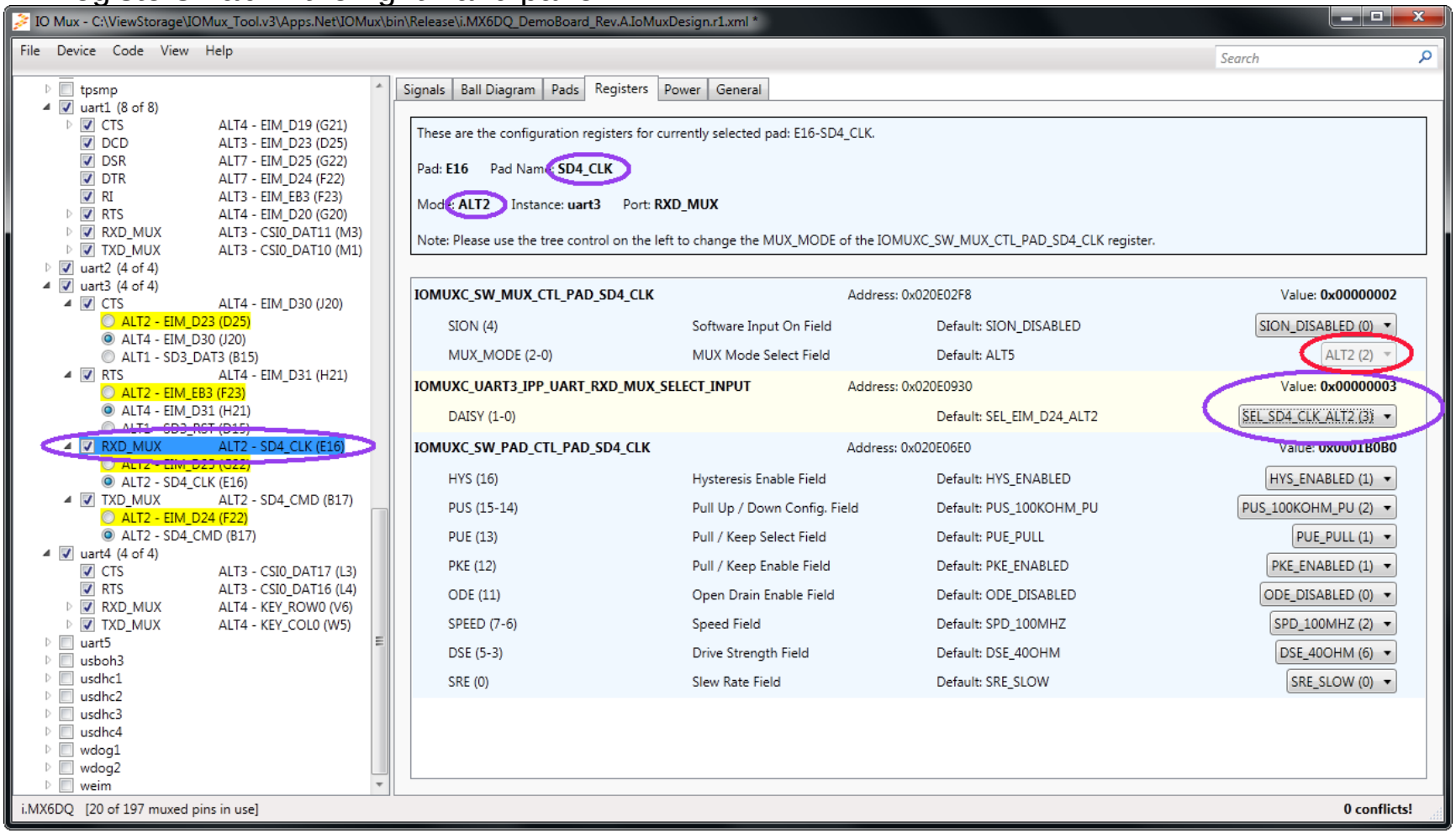


Pads “Spreadsheet” View

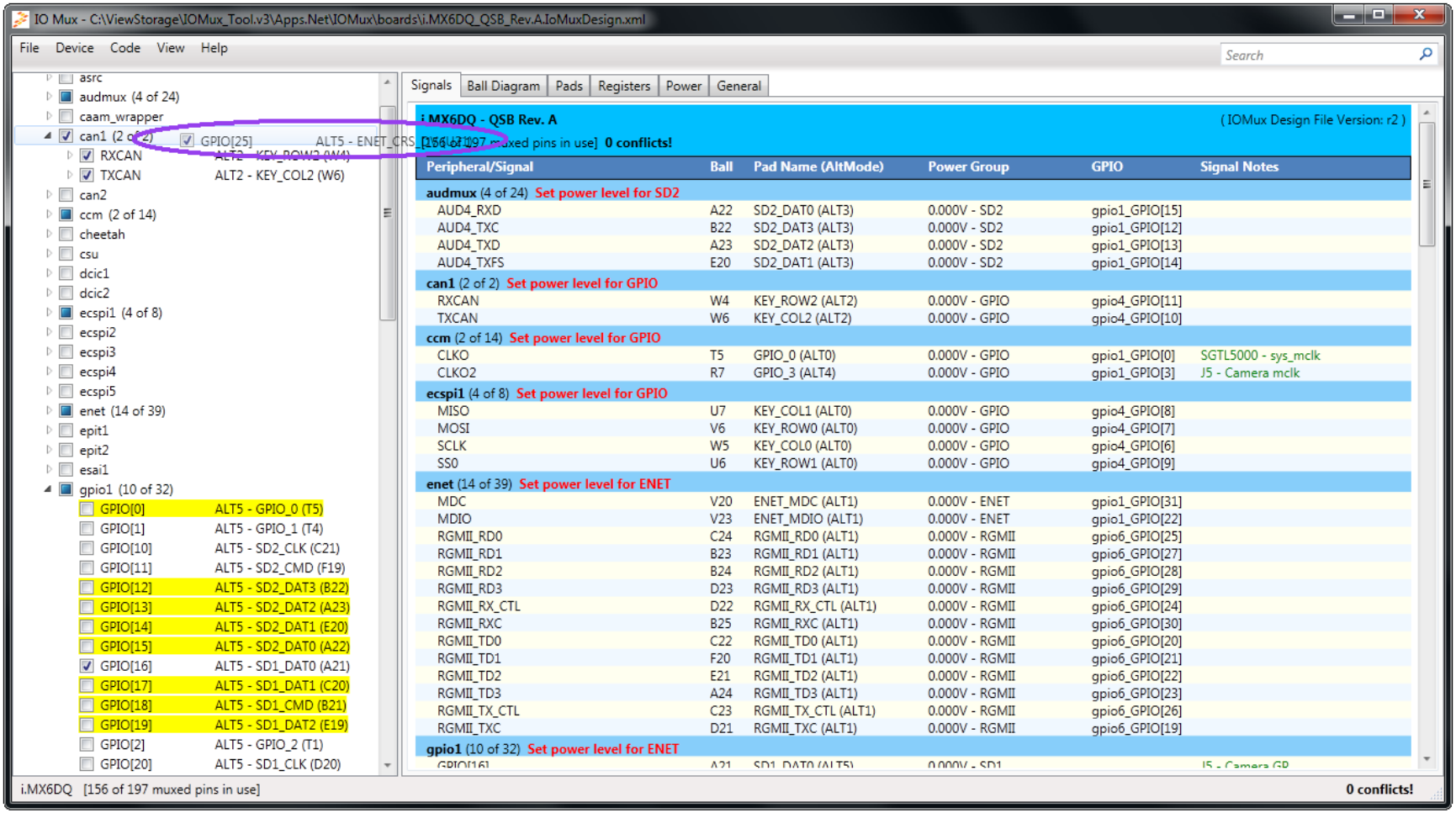


Configuring IOMUXC Registers

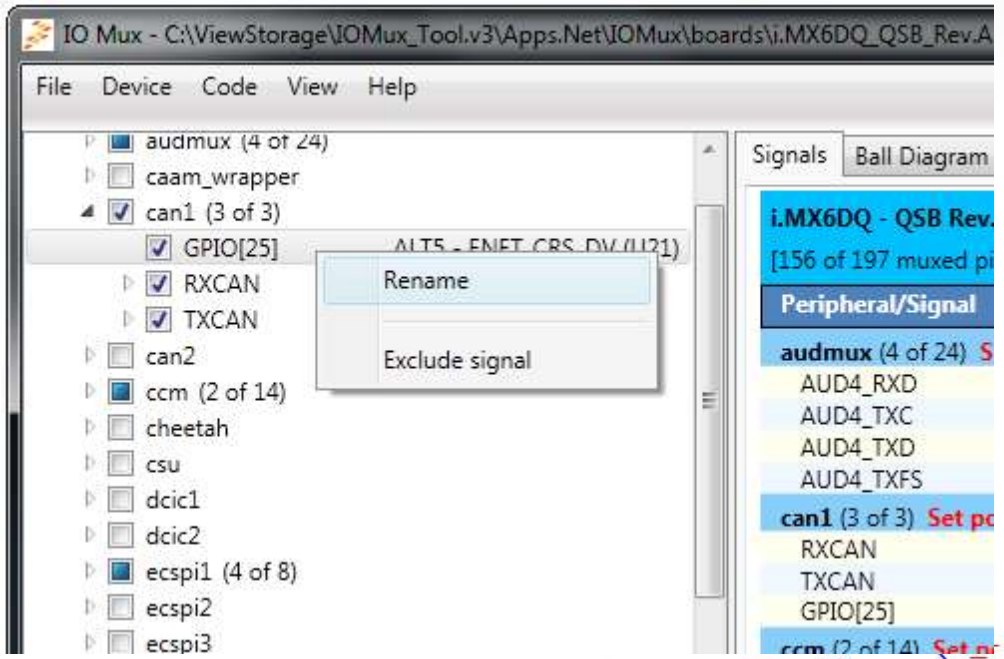
- Select UART3/RXD_MUX in the left-hand pane.
- All of the IOMUXC Registers associated with the AD4_CLK(E16) pad are shown on the Registers Tab in the right-hand pane.

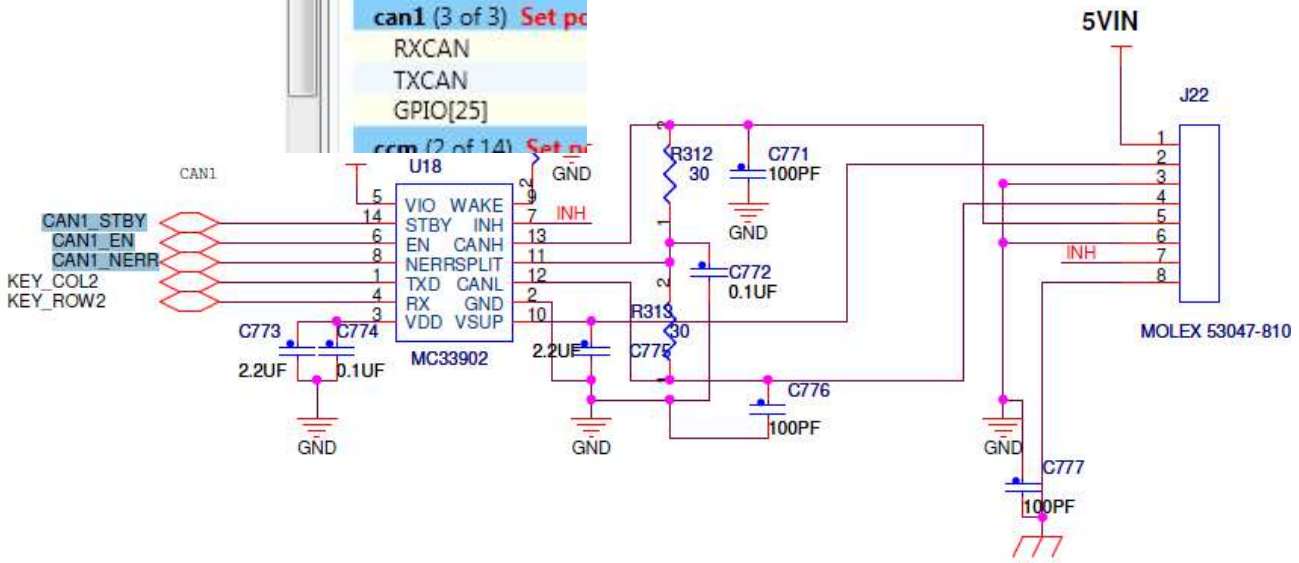


Drag a Signal to another Module



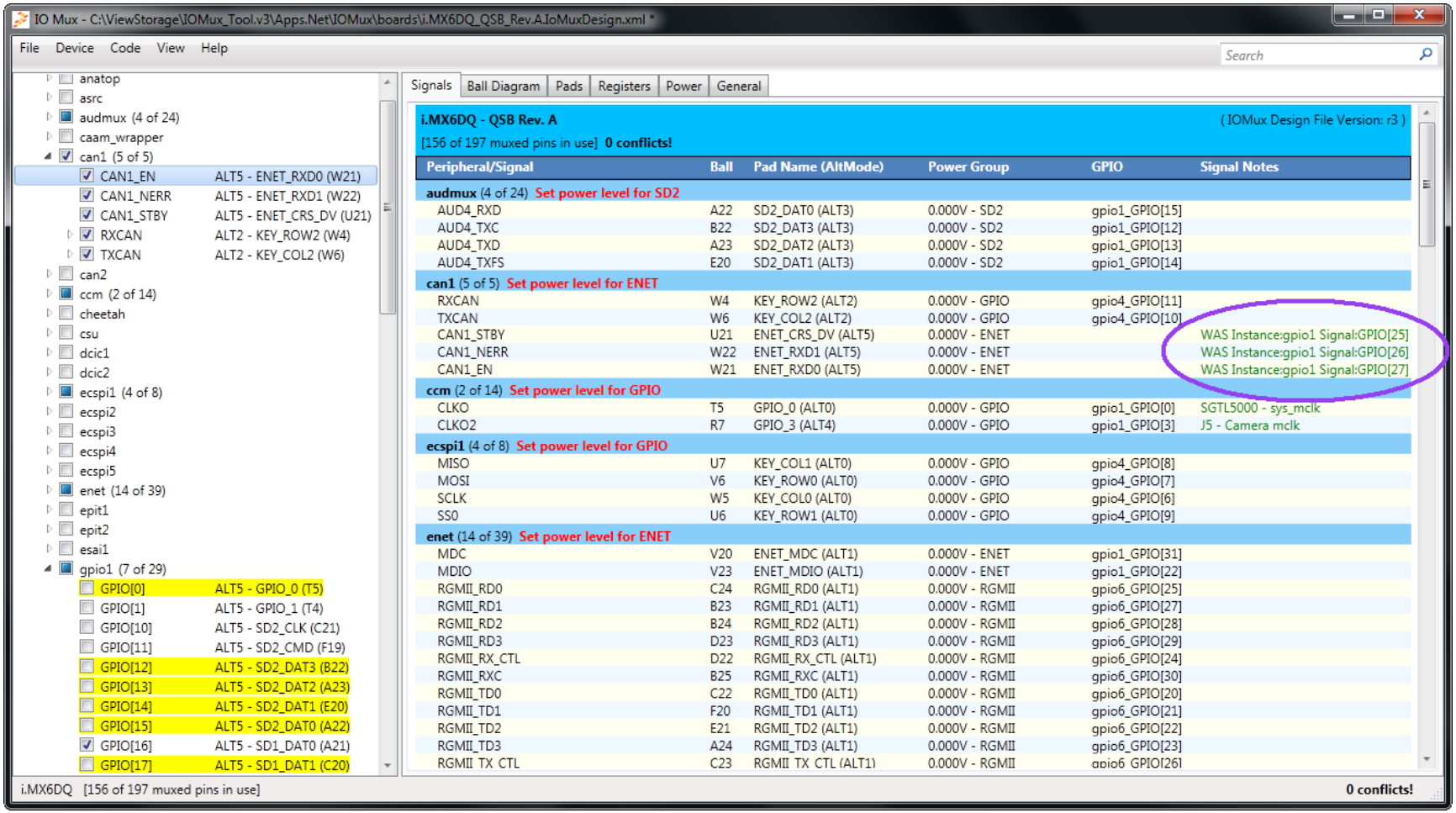
Rename Signal to Match Schematics





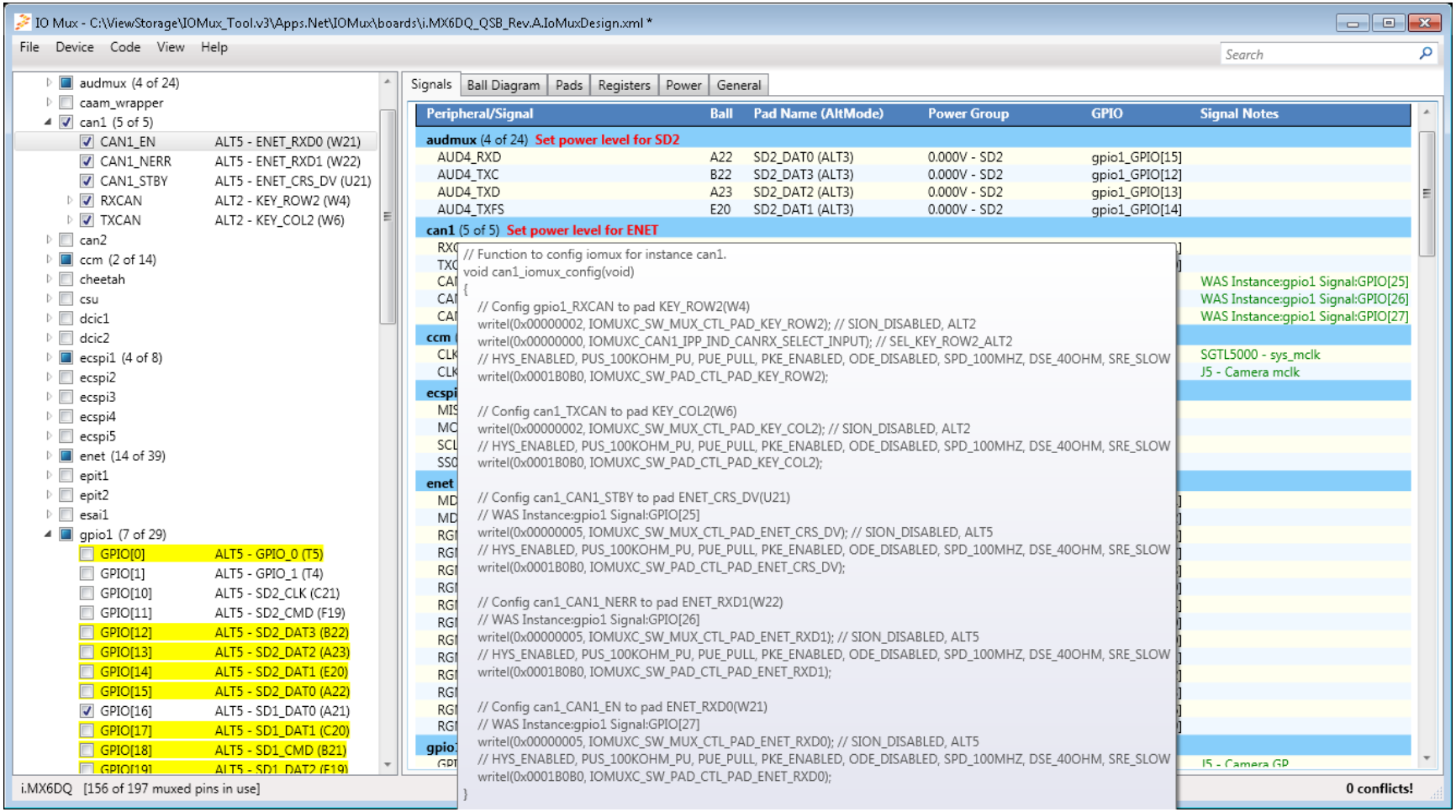
CAN1 Module with All Signals

- Comments auto-generated to denote original Module/Signal.



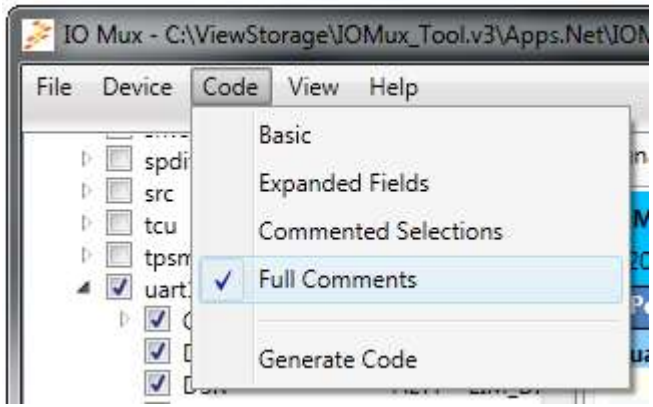
Code Reflects Added Signals

- Basic Code Style as a Tooltip.

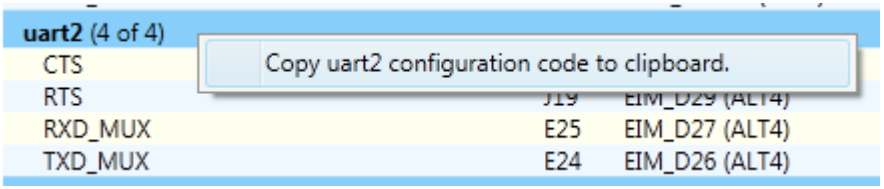


Generate Configuration Code

- Several Code-Styles available in the Code Menu.
- Examples are shown in the User's Guide.
- Click "Generate Code" to create the files for the current design.



Try it



freescale™ 飞思卡尔

freescale™
飞思卡尔

Develop Tools

DDR Stress Test

DDR Stress Test Tool

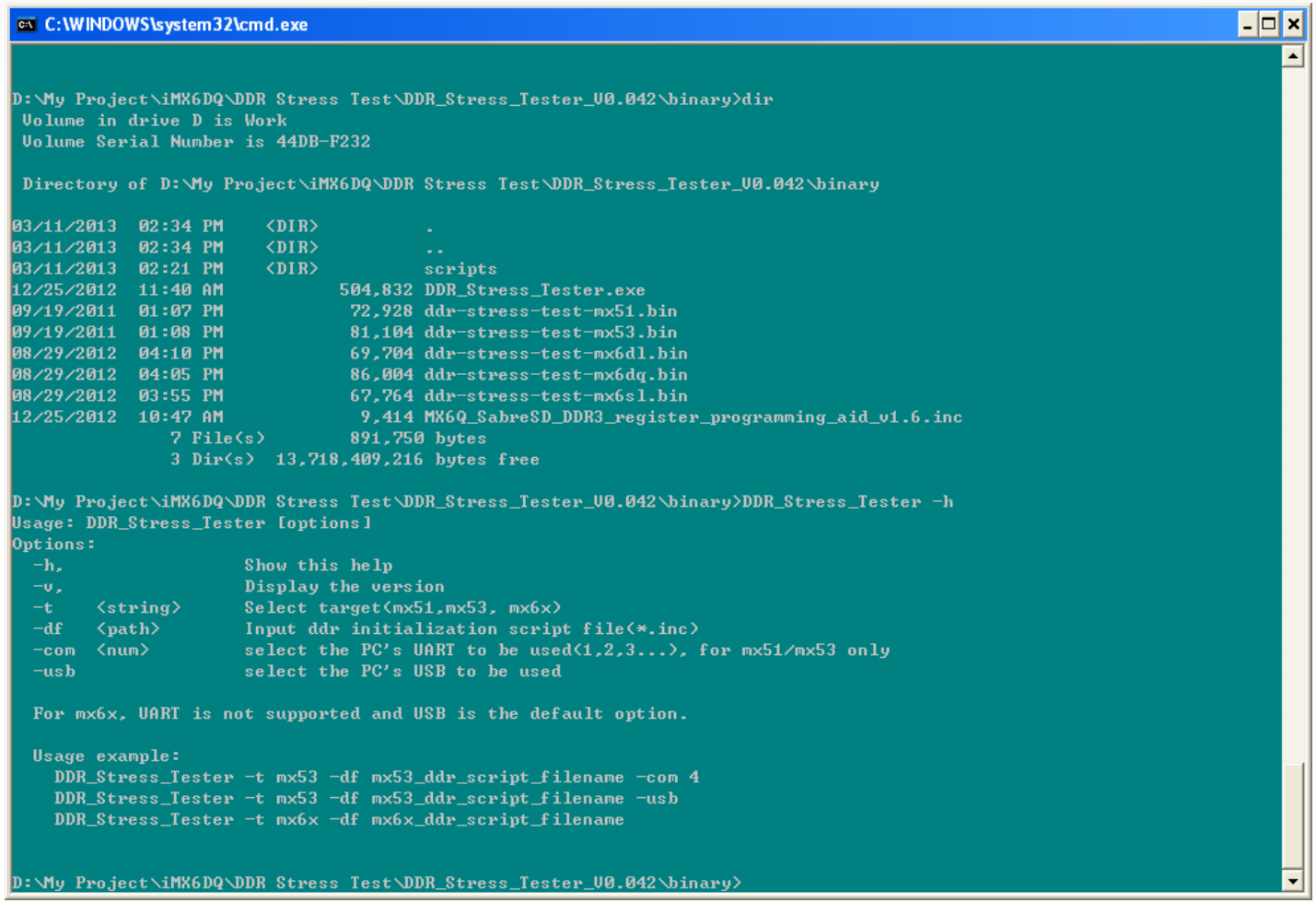
- **What is DDR Stress Tester kit?**

  It is downloadable test application architecture. A program running on PC (DDR_Stress_Tester.exe, which running on Command Prompt window) will download the test image to target board's IRAM with the help of UART/USB connection. The test image will do the DDR stress test and the result will be sent to PC through UART/USB and be printed on the Command Prompt window.

- **For mx6dq, mx6dl or mx6sl, UART is not supported.**
- **Support mx53, mx51, mx6dq, mx6dl and mx6sl.**

freescale™ 飞思卡尔

DDR Stress Test Tool *cont.*



Test Log Link

freescale™
飞思卡尔

Develop Tools

OBDS & PLATLIB

OBDS and PLATLIB

- **What is OBDS ?**
  - The On Board Diagnostics Suite (OBDS) is a suite of tests designed to ensure the hardware connectivity between the SoC and on board peripherals to help ensure working and bug-free board systems.

- **What is PLATLIB ?**
  - Example low-level driver code that enables all main features of a peripheral without the need for an operating system.
  - Provides example usage of each driver which demonstrates the main features.
  - Provides a solid and simple environment for quick board bring-up.
  - Similar to OBDS except that more module functionality is supported in addition to providing a firmware guide.

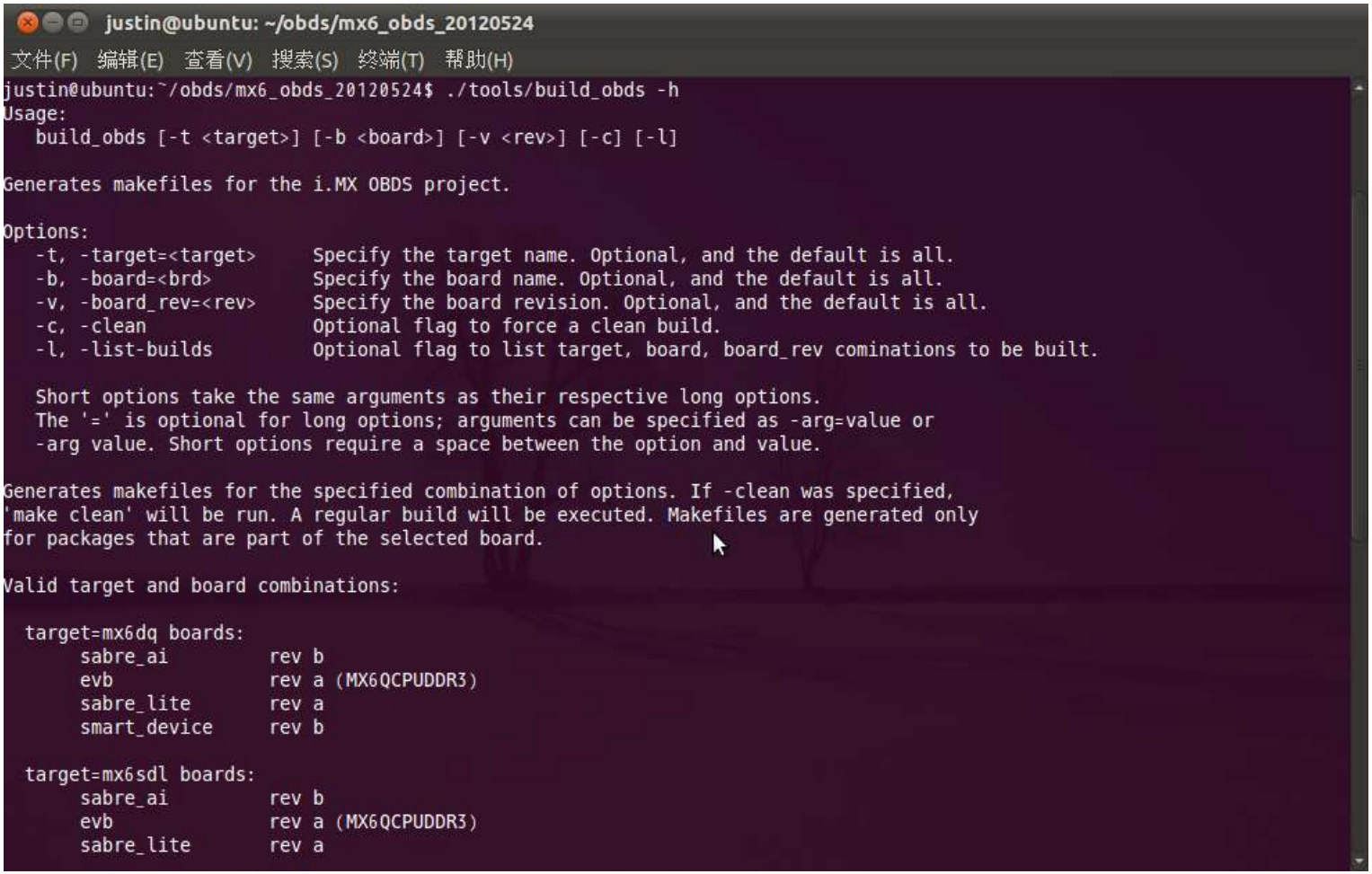
Setting up the Tool Chain

- **Obtained the GNU Toolchain for ARM processors**
  - Go to http://compass.freescale.net/go/217844329
  - Download the Linux version:
    arm-2008q3-66-arm-none-eabi-i686-pc-linux-gnu.tar.bz2
  - Or search: “Sourcery G++ Lite 2008q3-66”

- **Setting up the OBDS GCC Build Environment under Linux**
  - Under /opt directory
    tar xjvf -2008q3-66-arm-none-eabi-i686-pc-linux-gnu.tar.bz2
  - Add /opt/tools/bin and /opt/arm-2008q3/bin to your environment
    PATH variable.

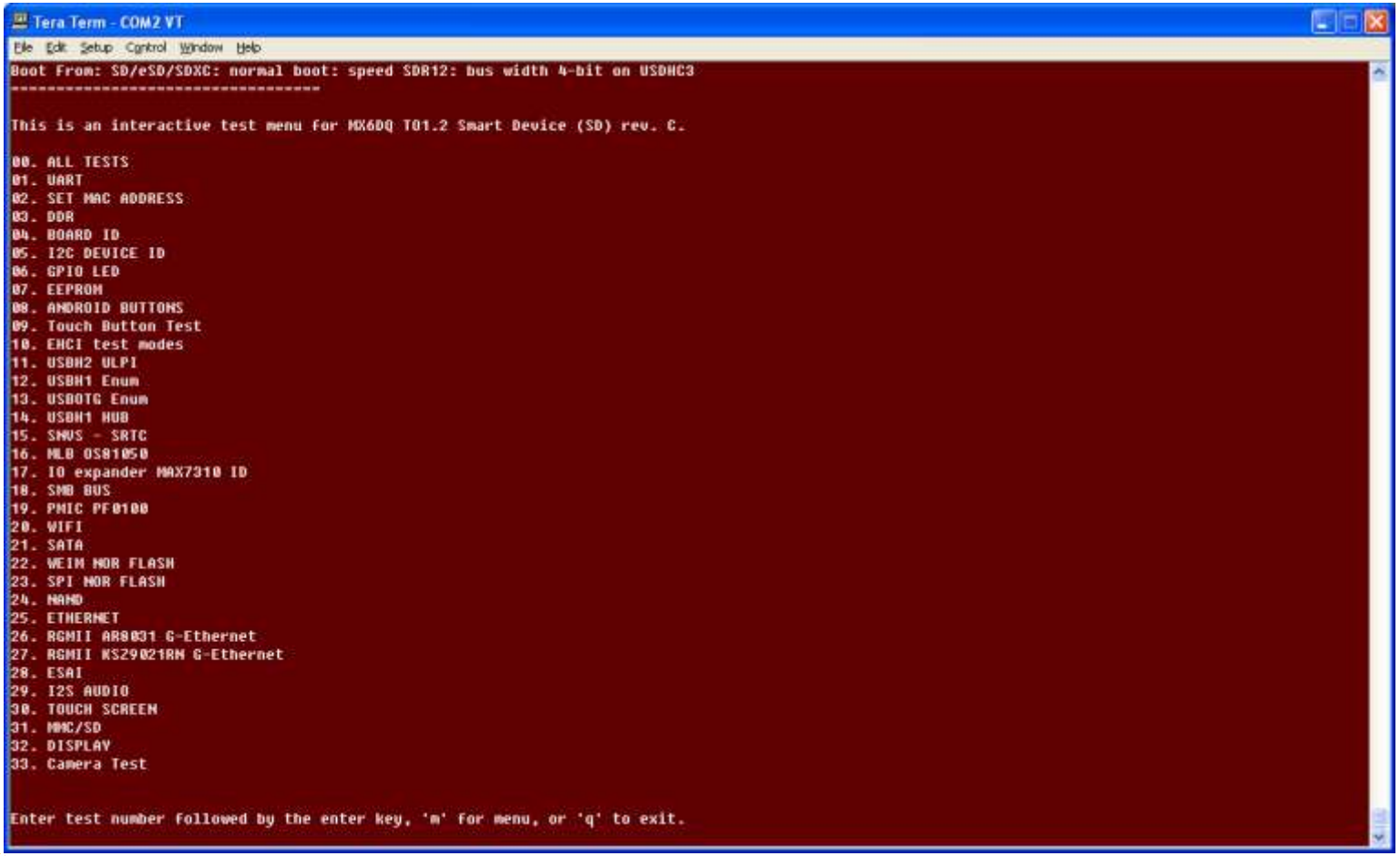
Build the OBDS Binary

- Build command: ./tools/build_obds -t mx6dq -b sabre_ai -v b –clean



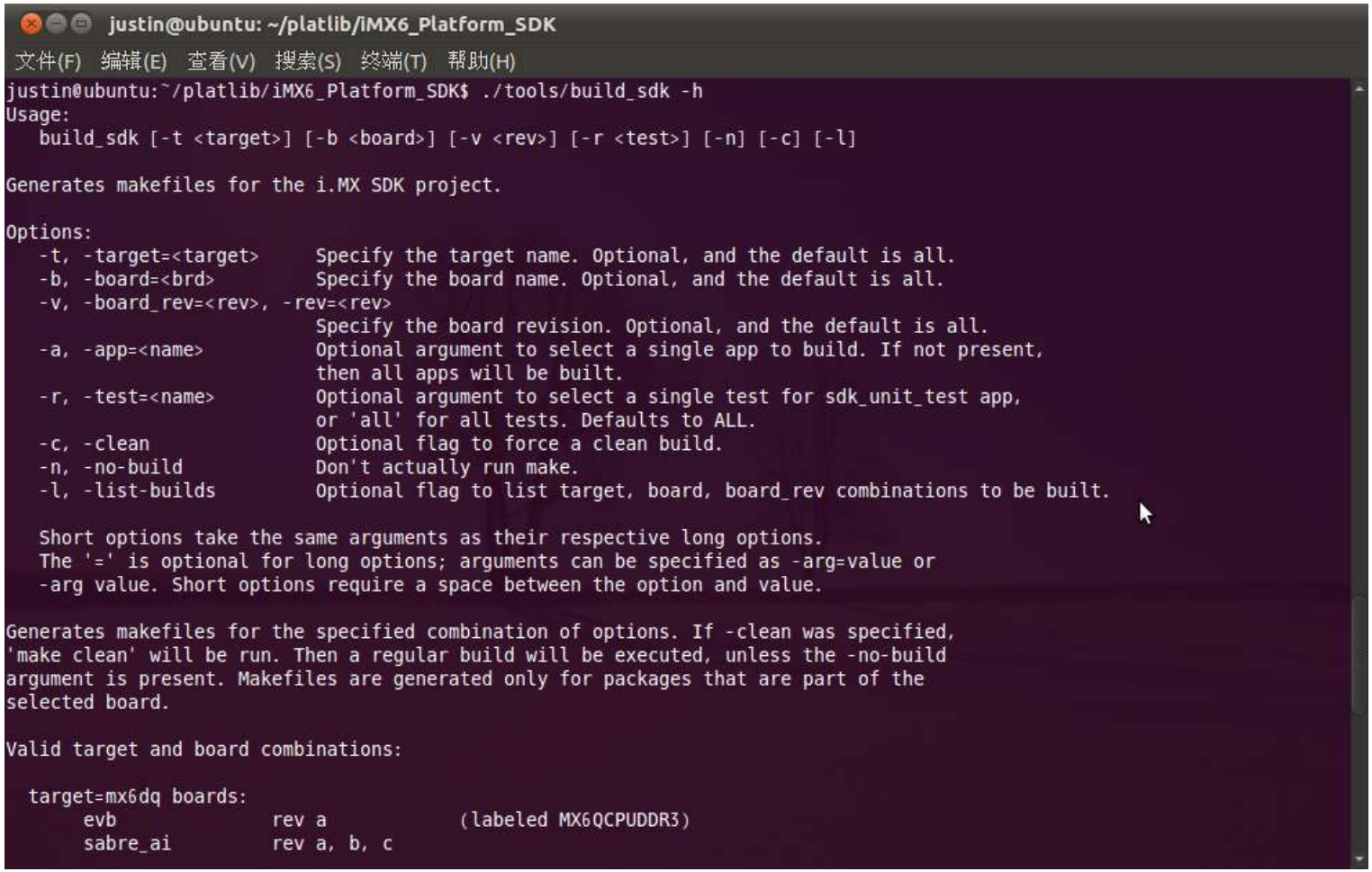
Deploy the OBDS Binary

- cd ./output/mx6dq/smart_device_rev_b/bin/
- dd if=mx6dq-smart_device-revb-obds.bin of=/dev/sdb skip=2 seek=2 && sync



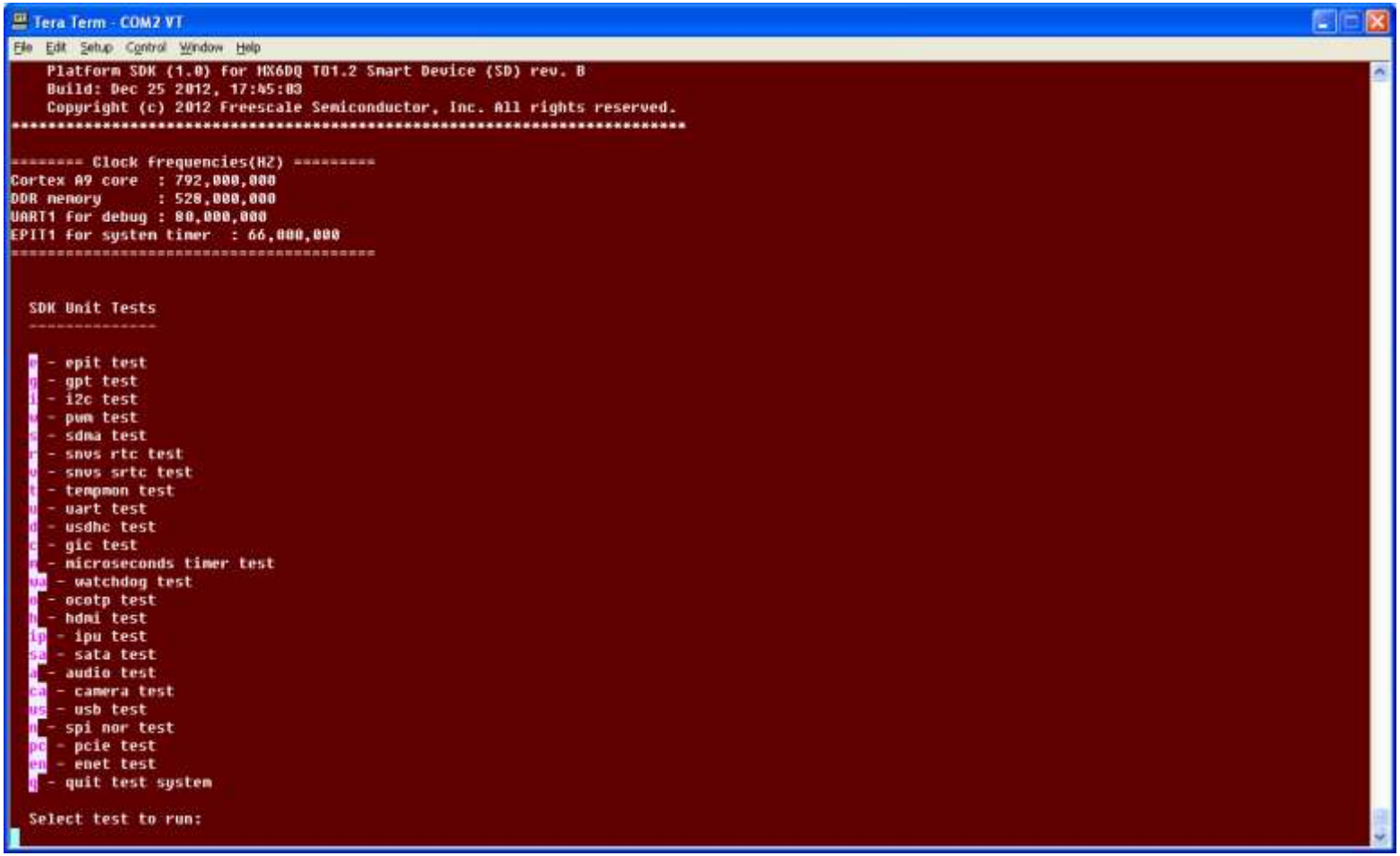
Build the PLATLIB Binary

- Build command: ./tools/build_sdk -t mx6dq -b sabre_ai -v b -clean



Deploy the PLATLIB Binary

- cd ./output/mx6dq/sdk_unit_test/sabre_ai_rev_b/
- dd if=sdk_unit_test_ALL.bin of=/dev/sdb skip=2 seek=2 && sync



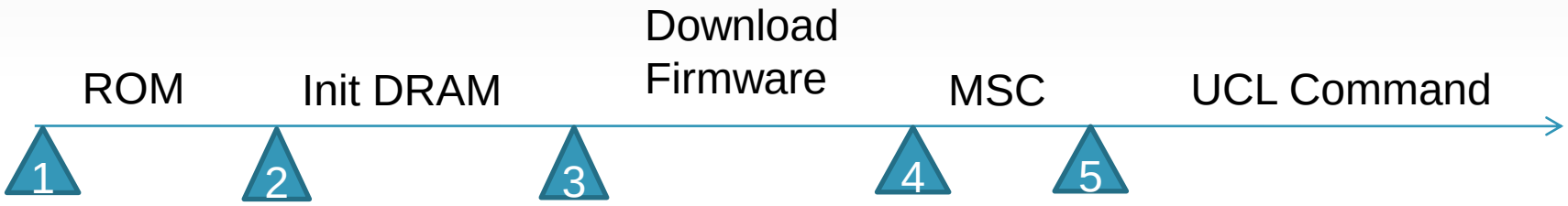
freescale™ 飞思卡尔

freescale™
飞思卡尔

Develop Tools

MFG

Manufacturing (MFG) Tool V2



- How the tool works - Steps
  1. After a board is powered up, it has nothing to run but ROM. ROM initializes USB and enumerates it as a dedicated device like HID device(MX23,MX28, MX50, MX6) or Bulk-IO device(MX3x, MX25, MX51, MX53).
  2. Once a host detects the device, it will setup the connection with the device. Now the first task for host is to initialize RAM memory. It extract memory initialization code or data from an image (like u-boot) to do the task. It is also possible to use a memory initialization script to get initialization data.
  3. After RAM is initialized, the host sends a kernel and mini RAM filesystem to RAM. The host then sends a command to ROM to jump into the kernel.
  4. The kernel runs and enumerate USB as a MSC device. Now the device is ready for high speed data transfer.
  5. The host runs commands in UCL script one by one.

Manufacturing Tool Usage

- Configure Files
  - UICfg.ini

    [UICfg]

    PortMgrDlg=1
  - Cfg.ini

    [profiles]

     chip = MX6Q Linux Update

    [platform]

      board = SabreSD

    [LIST]

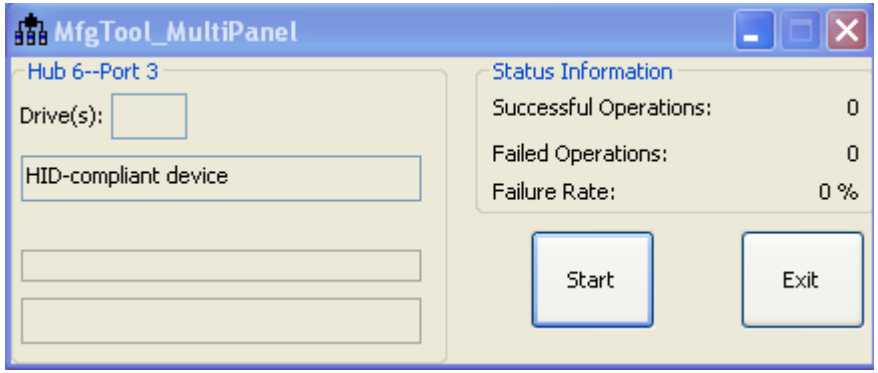
      name = MX6Q-Sabreauto-NAND
  - Ucl2.xml

    Located: Profiles\MX6Q Linux Update\OS Firmware

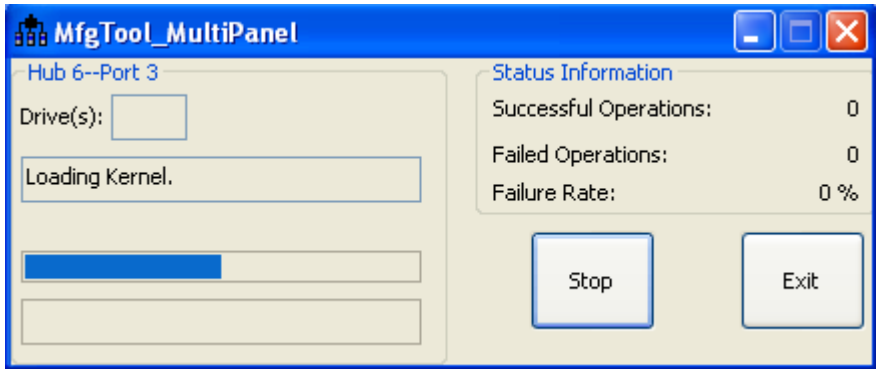
    Download script file , customer can change it.

Manufacturing Tool Usage *Cont.*

- Power on board and enter serial download mode
- Connect Board to PC with USB cable
- Start the MfgTool



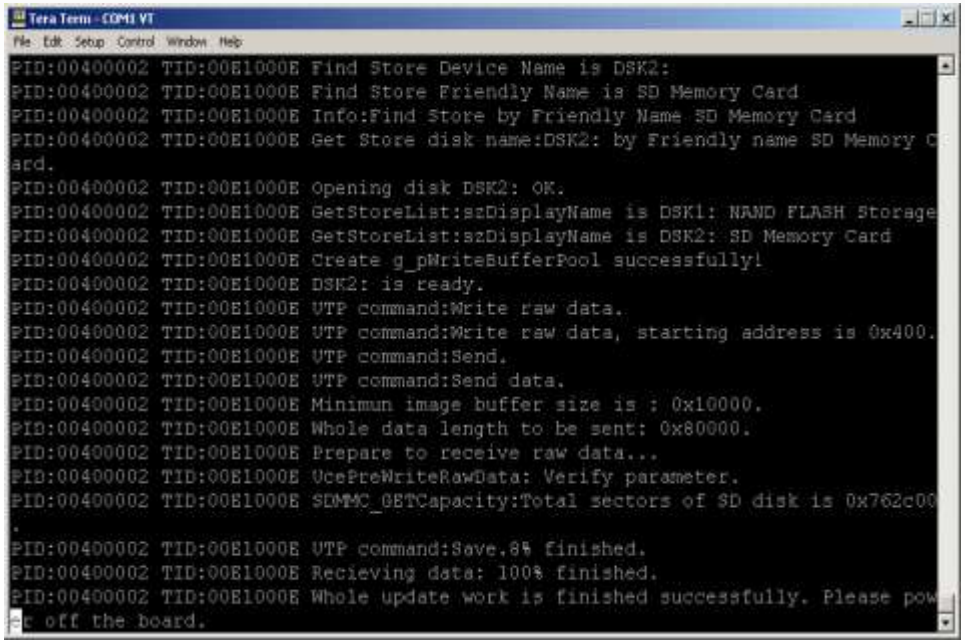
- Click Start button



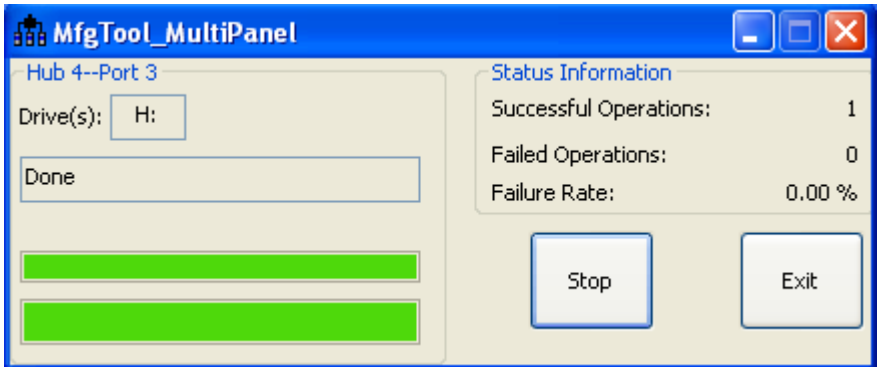
freescale™ 飞思卡尔

Manufacturing Tool Usage *Cont.*

You can find information from the terminal



It is done. Click “Stop” to finish, and Click “Exit” to terminate the application



Manufacturing Tool Usage *Cont.*

- How to Program a Fuse

  MfgTool V2 supports writing the specified value into the fuse.

  The OTP fuse can be written through the following commands:

<CMD state="Updater" type="push" body="$ ls /sys/fsl_otp ">Showing HW_OCOTP fuse bank</CMD>

<CMD state="Updater" type="push" body="$ echo 0x11223344 > /sys/fsl_otp/HW_OCOTP_MAC0">write 0x11223344 to HW_OCOTP_MAC0 fuse bank</CMD>

<CMD state="Updater" type="push" body="$ cat /sys/fsl_otp/HW_OCOTP_MAC0">Read value from HW_OCOTP_MAC0 fuse bank</CMD>

The fuse bank name (ex: HW_OCOTP_MAC0) should be changed according as needed.

freescale™
飞思卡尔

Freescale Support

IMXCommunity

www.imxcommunity.org

A Freescale supported open web community of developers sharing common interest in transforming i.MX applications processors into practically anything imaginable.

Community Facts at a Glance

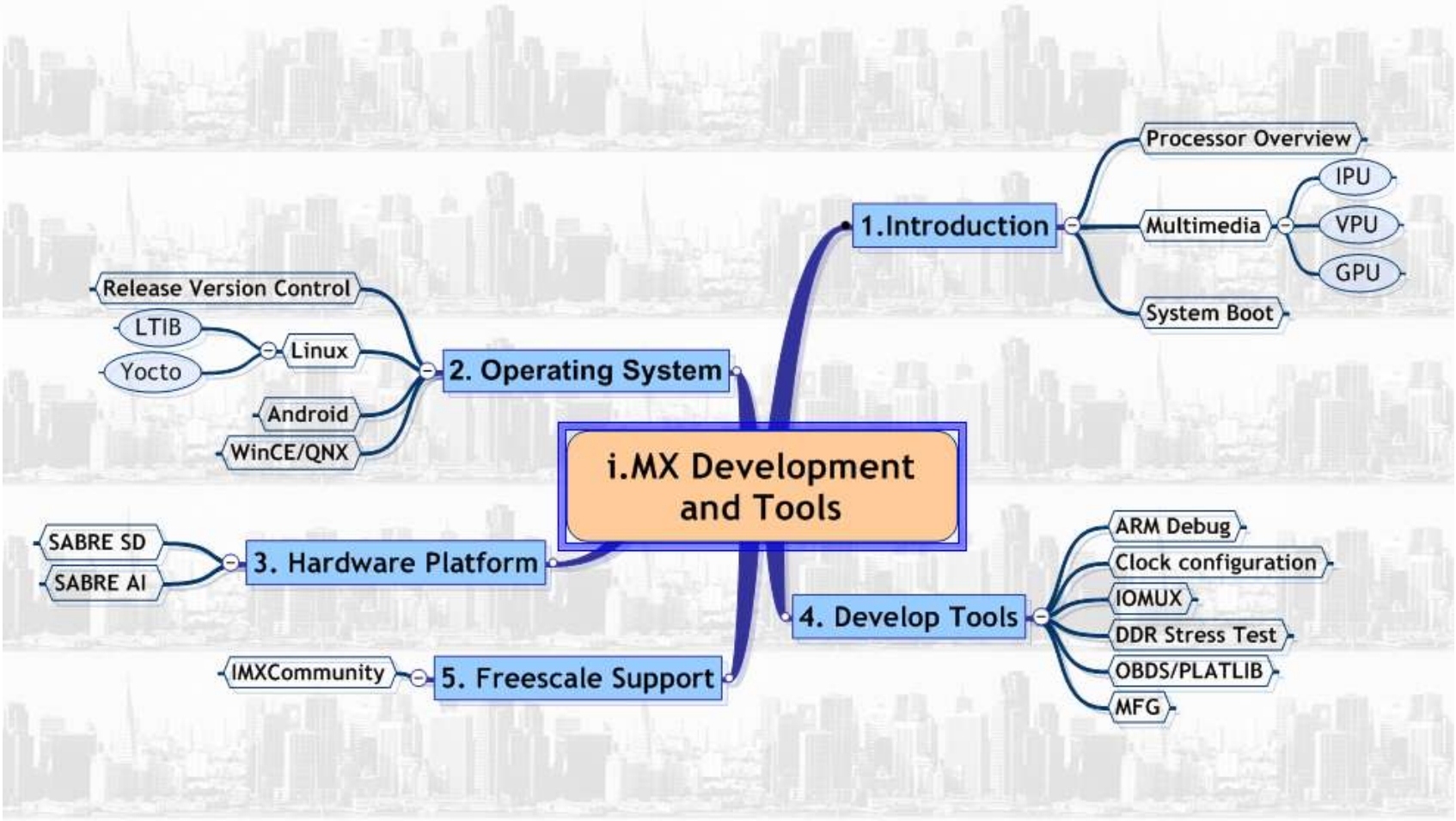
- Over 3,800 members and over 200 Freescale engineers and marketers interacting with you
- Support and enablement for i.MX processors and software
- Forums, Groups and Blogs Posts
- News, Photos and Videos
- Training, Events and Promotions

freescale™ 飞思卡尔

freescale™
飞思卡尔

Summary

MindMap



freescale™
飞思卡尔

Q&A


freescale
飞思卡尔