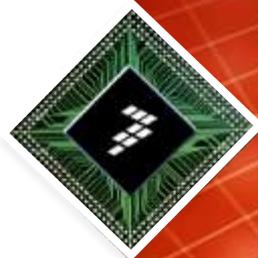




# Development Tools for i.MX Applications Processors APF-CON-T0679

Rui Yang



May 2013

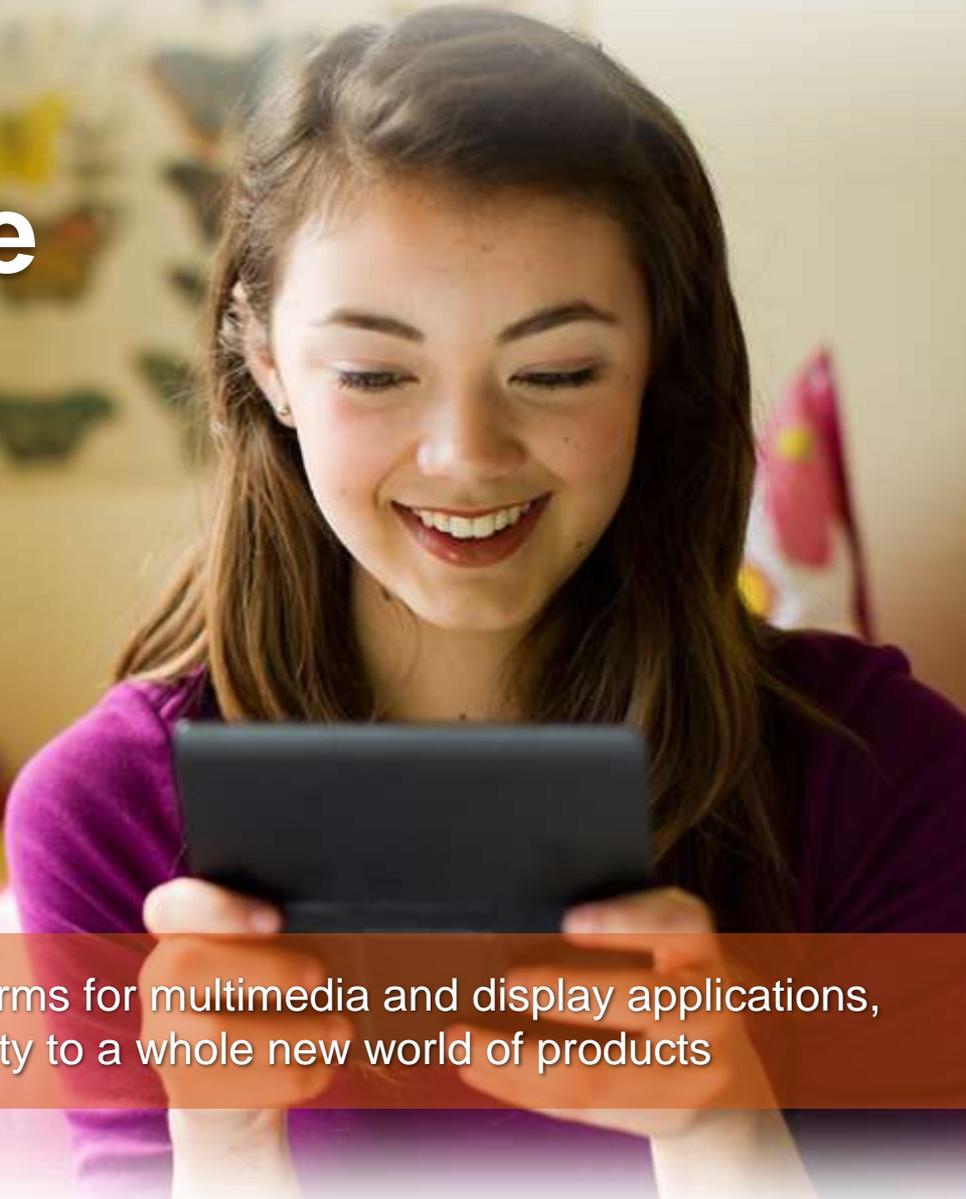
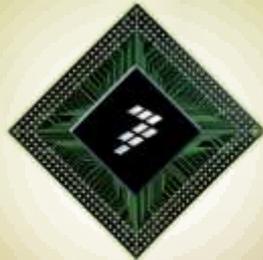
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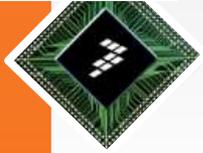


i.MX

# Your Interface to the World



i.MX families offer the most versatile platforms for multimedia and display applications, bringing personality and interactivity to a whole new world of products



# Agenda

- **Introduction**
  - Processor Overview
  - Multimedia (IPU/VPU/GPU)
  - System Boot
- **Operating System**
  - Release Version Control
  - Linux (LTIB/Yocto)
  - Android
  - WinCE/QNX
- **Hardware Platform**
  - SABRE SD
  - SABRE AI
- **Develop Tools**
  - ARM Debug
  - Clock Configuration
  - IOMUX
  - DDR Stress Test
  - OBDS/PLATLIB
  - MFG
- **Freescale Support**
  - IMXCommunity
- **Summary and QA**



# Introduction

## Processor Overview



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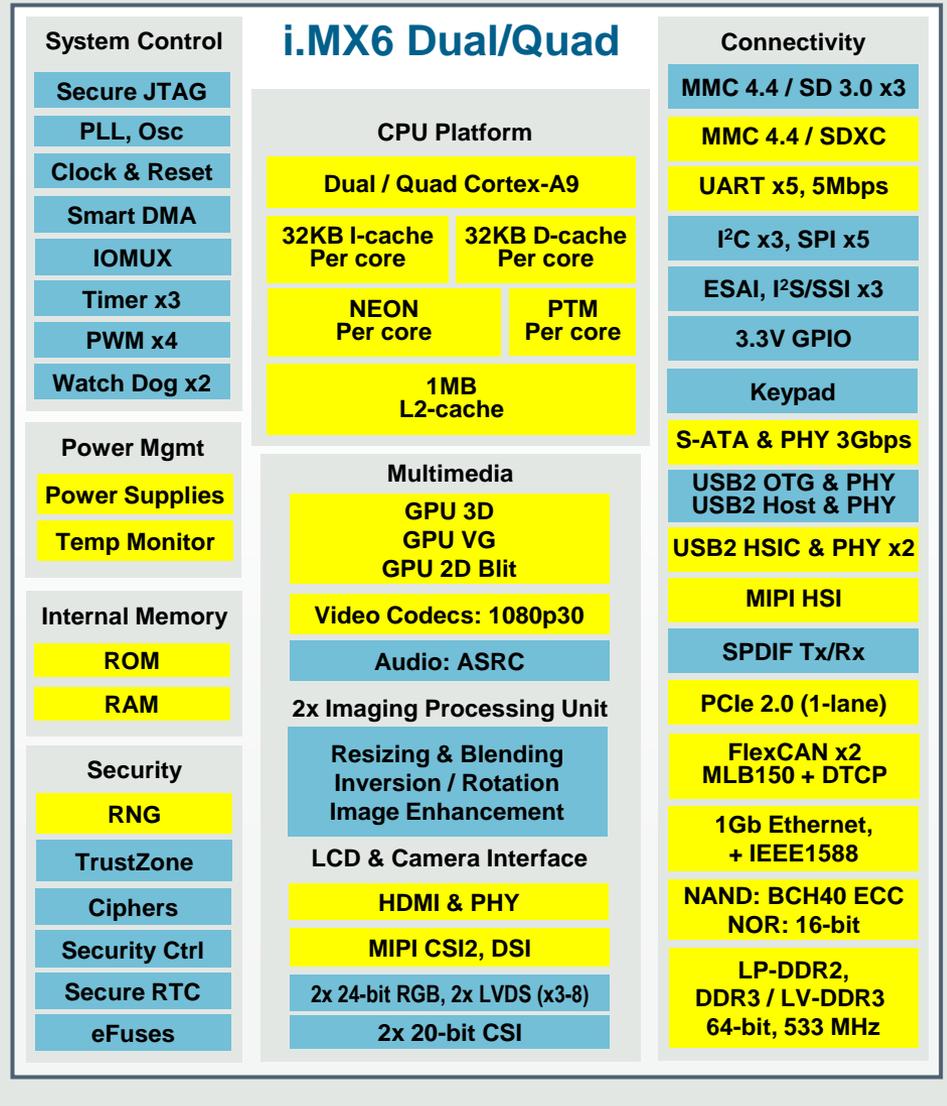
# i.MX 6Dual/6Quad Applications Processor

## Specifications

- **CPU:** i.MX 6Quad 4x Cortex-A9 @1.2 GHz, 12000 DMIPS  
i.MX 6Dual 2x Cortex-A9 @1.2 GHz, 6000 DMIPS
- **Process:** 40nm
- **Core Voltage:** 1.1V
- **Package:** 21x21 0.8mm Flip-chip BGA  
12x12 PoP (LP-DDR2 dual channel – standard JEDEC POP)

## Key Features and Advantages

- Multi-core architecture for high performance, 1MB L2 cache
- 64-bit dual channel LP-DDR2, 64bit DDR3 and raw / managed NAND
- S-ATA 3Gbps interface (SSD / HDD)
- Delivers rich graphics and UI in HW
  - OpenGL/ES 2.x 3D accelerator with OpenCL EP support and OpenVG 1.1 acceleration
- Drives high resolution video in HW
  - Multi-format HD1080 video decode and encode
  - 1080p60 decode, 720p60 encode
  - High quality video processing (resizing, de-interlacing, etc.)
- Flexible display support
  - Four simultaneous: 2x Parallel, 2x LVDS, MIPI-DSI, or HDMI
  - Dual display up to WUXGA (1920x1200) and HD1080
- MIPI-CSI2, DSI and HSI
- Increased analog integration simplifies system design and reduces BOM
  - DC-DC converters and linear regulators supply cores and all internal logic
  - Temperature monitor for smart performance control
- Expansion port support via PCIe 2.0
- Car network: 2xCAN, MLB150 with DTCP, 1Gb Ethernet with IEEE1588

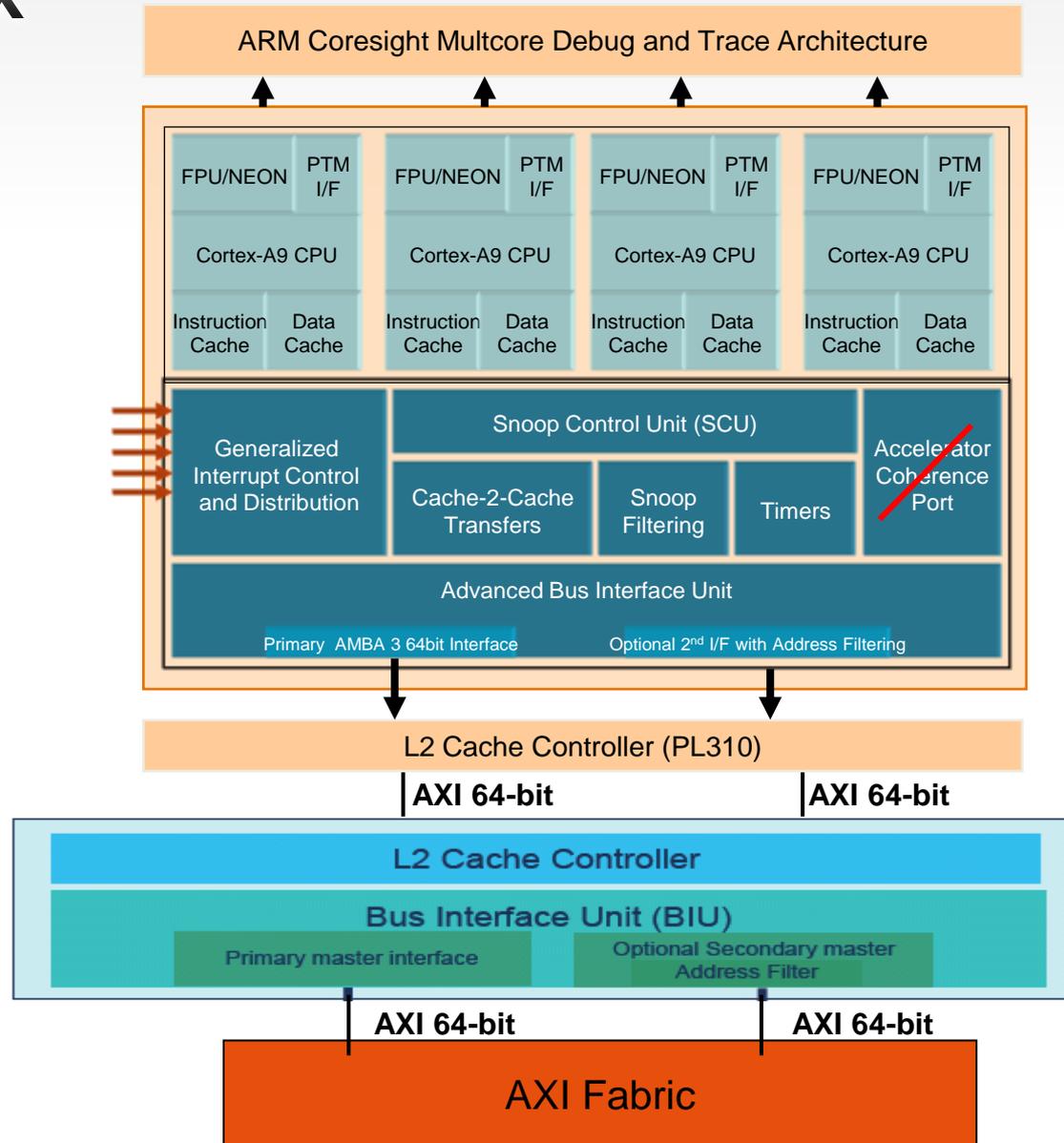


Updated from i.MX53

# Core Complex – i.MX 6Dual/Quad

## HW Components:

- System:
  - 2x/4x Cores in i.MX 6 Dual/Quad
  - 32 KB L1 (I and D)
  - 1MB L2 Cache
  - 128 Interrupts
  - Using 2x 64-bit AXI to L2C
- Per core
  - 32 KB I and 32KB D L1 Cache
  - Neon, FPU, Jazelle, Trustzone





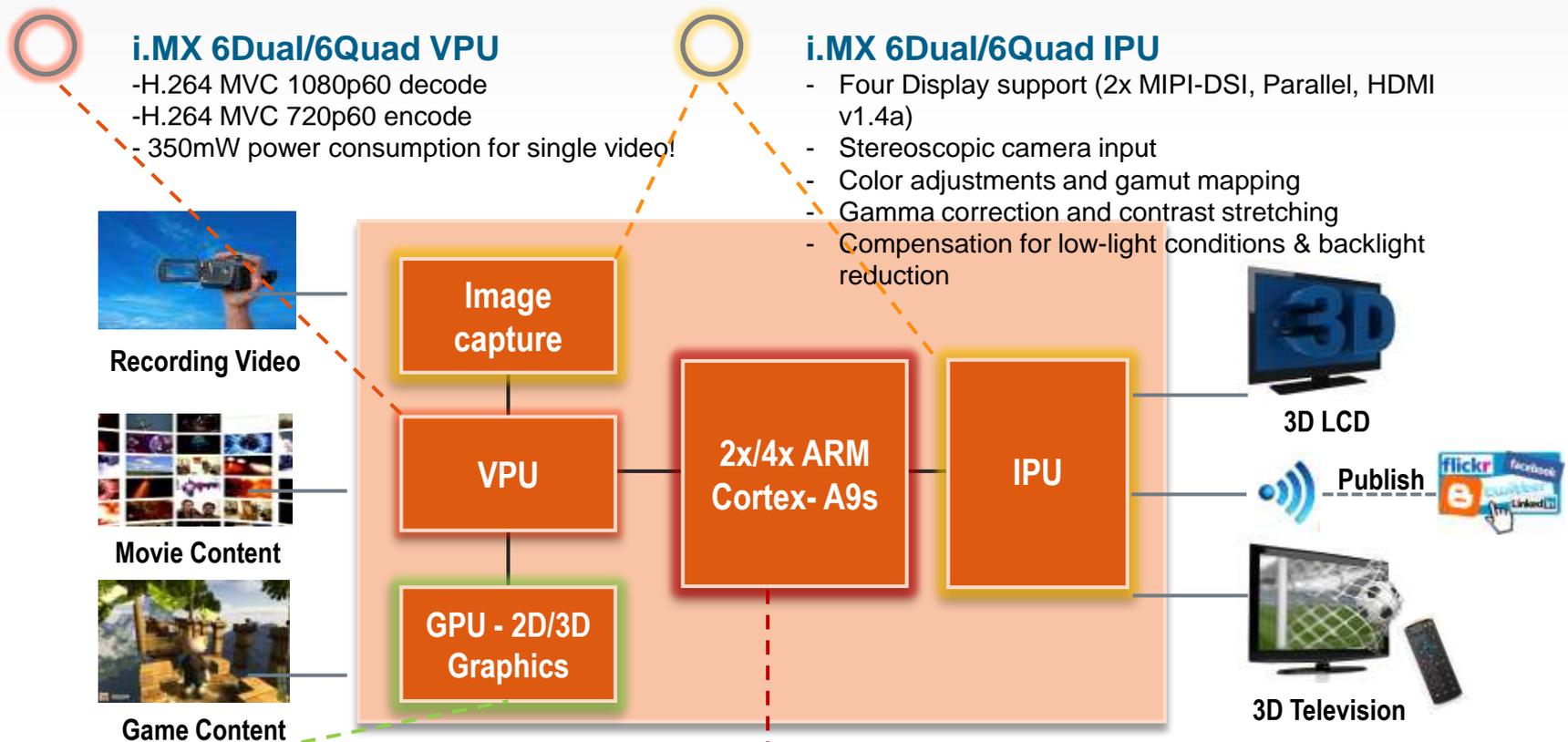
# Introduction

## Multimedia(IPU/VPU/GPU)



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# Intelligent Integration of Multi-Media



## i.MX 6Dual/6Quad VPU

- H.264 MVC 1080p60 decode
- H.264 MVC 720p60 encode
- 350mW power consumption for single video!

## i.MX 6Dual/6Quad IPU

- Four Display support (2x MIPI-DSI, Parallel, HDMI v1.4a)
- Stereoscopic camera input
- Color adjustments and gamut mapping
- Gamma correction and contrast stretching
- Compensation for low-light conditions & backlight reduction

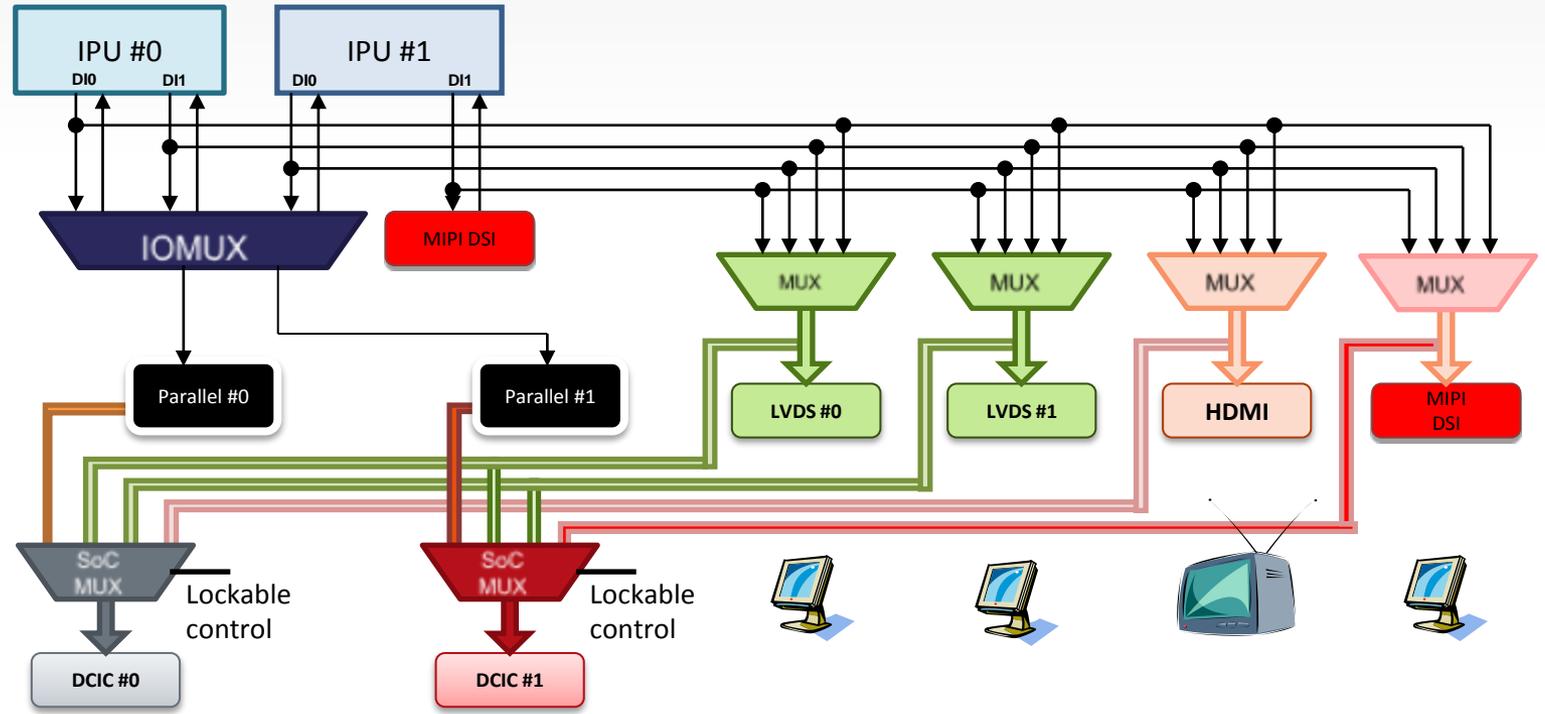
## i.MX 6Dual/6Quad Triple-Play Graphics

- 3 engines: 3D, OpenVG and BLT
- 200 MT/s, 4 shaders, 3 separate engines
- High quality 3D games optimized for mobile
- Augmented reality views (real world + 3D objects)
- Advanced 3D video formats (source/depth format)

## i.MX 6Dual/6Quad– 2x/4x cores

- Create, transform, enhance, & publish multimedia fast!
- Intuitive User Interfaces for content viewing
- Scalability for 'the next big use case'

# Display Ports Muxing – i.MX 6Dual/Quad



- **Six ports**
  - Two parallel - driven directly by the IPU
  - Two LVDS channels - driven by the LVDS bridge
  - One HDMI – driven by the HDMI transmitter
  - One MIPI-DSI – driven by the MIPI-DSI transmitter
- **Four simultaneous outputs**
  - Each IPU has two display ports (DI0 and DI1)
  - Therefore, up to four external ports can be active at any given time.
  - Additional asynchronous data flows can be sent through the parallel ports and the MIPI-DSI port
- **Display Content Integrity Check (DCIC)**
  - For parallel interfaces: probes the I/O loopback (essentially equivalent to probing the external wires)
  - For other integrated interfaces (e.g. LVDS): probes the IPU output (essentially equivalent to the inputs to the serializers)

# VPU HD Video – i.MX53 vs i.MX 6Dual/Quad

- Embeds a flexible, powerful and low power hardware acceleration for HD video decoding in Blue-ray disk quality
- Note: in all cases, the HW CODEC meets or exceeds the bit-rate requirements specified in the standards

1080i/p30+D1  
 1080i/p30 (\* - p only)  
 720p30 or 720p60  
 720p20  
 WVGA  
 D1 (PAL/NTSC)

Feature	Format	Profile	i.MX53	i.MX6 Quad/Dual
Low-Power Audio Decode			SW	SW
Low-Power Video Decode	MPEG-2	Main-High	HW	HW
	H.264	BP/MP/HP	HW	HW
	VC1	SP/MP/AP	HW	HW
	RV10	8/9/10	HW	HW*
	MPEG4/Xvid	SP/ASP	HW	HW
	DivX	3/4/5/6	HW	HW
	H.263	P0/P3	HW	HW*
	Sorenson H.263	N/A	HW	HW*
	AVS	Jizhun	SW	HW
	On2 VP6/8	N/A	SW	HW* (for VP8)
	SVC	HP	SW	SW
	MVC	N/A	SW/HW	HW*
	MJPEG	Baseline	HW, 40MP/sec	HW, 120MP/sec
Low-Power Video Encode	H.264	Baseline	HW	HW*
	H.263	P0/P3	HW	HW*
	MPEG4	Simple	HW	HW*
	MJPEG	Baseline	HW, 80MP/sec	HW, 160MP/sec
Video Telephony (SiP, H323) – H.264 BP			HW	HW
Transcode (DLNA) – (M)DMS/(M)DMP			HW	HW
Video de-interlacing			HW	HW
Further Video Processing (deblocking, resizing, CSC)			HW	HW

# Multiple-Play Graphics Solution - i.MX 6 Series



i.MX 6



## Vector Graphics

- GPU-VG @ 500MHz
- 350M pixels / sec raw performance
- Native OpenVG™ 1.1 Khronos conformance with hardware tessellation



## 3D + GPGPU

- GPUv4 @ 533MHz
- 200M triangles / sec
- 4 Shader Cores: 30 GFLOPS
- Halti support



## 2D-Composition

- GPU-2Dv1 @500Mhz
- Up to 1G pixels / sec raw performance





# Introduction

## System Boot



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# Boot Modes and Boot Sources

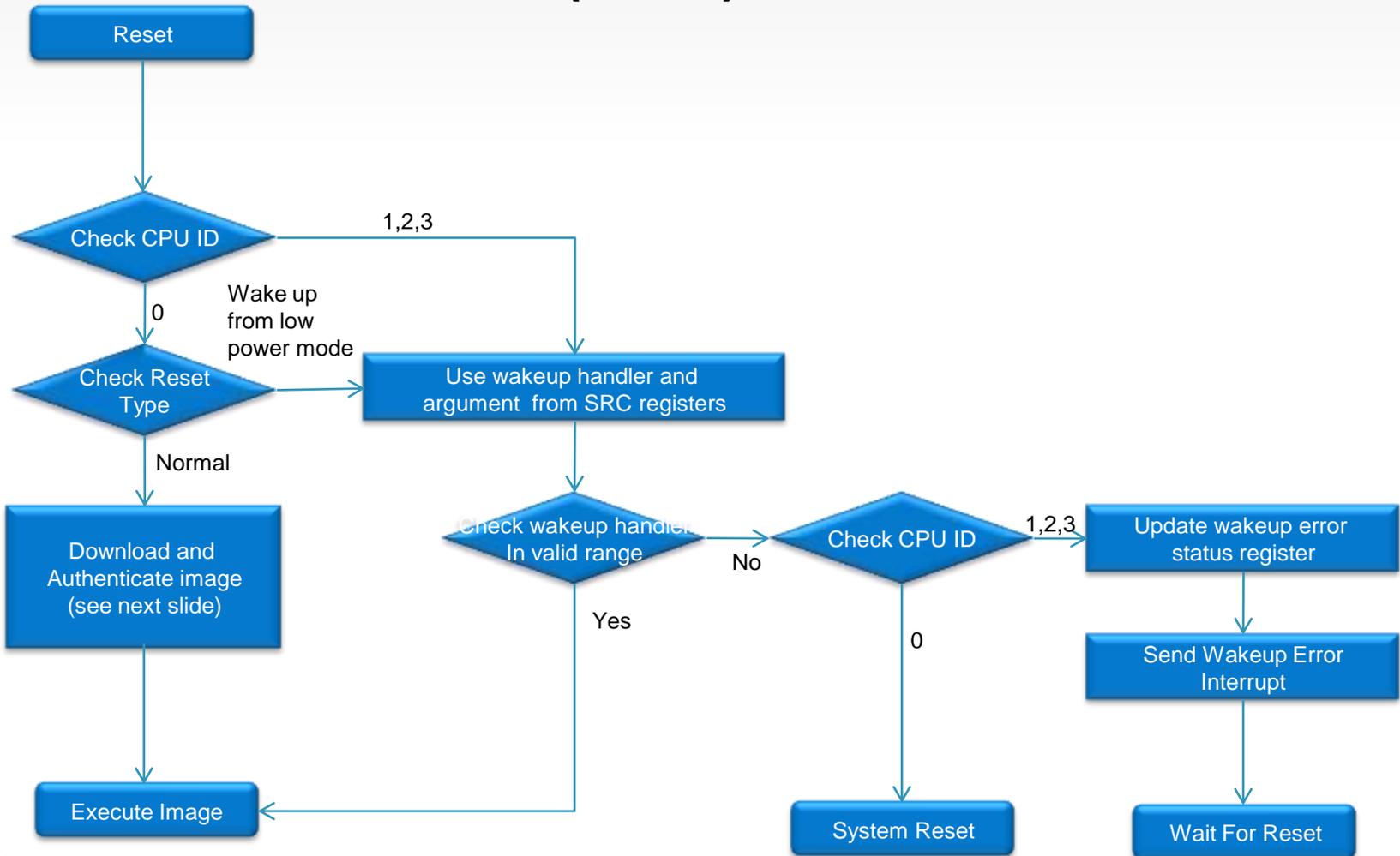
- Flash Devices
  - NOR flash (using WEIM)
  - OneNand (using WEIM)
  - NAND flash (using NFC)
- Serial ATA (using SATA)
  - Only for 6Quad / 6Dual
- Expansion Devices
  - SD/eSD/SDXC/MMC/eMMC (using USDHC1 / USDHC2 / USDHC3 / USDHC4)
  - I2C (using I2C1 / I2C2 / I2C3)
  - SPI (using eCSPI1 / eCSPI2 / eCSPI3/eCSPI4/eCSPI5)
- Serial Downloader
  - USB (using USB OTG)
- Plug-in Mode
  - For custom / user-defined boot

- Boot modes are set via eFuses
- For development purposes, there is an option to set boot modes via external pins

# Boot Modes

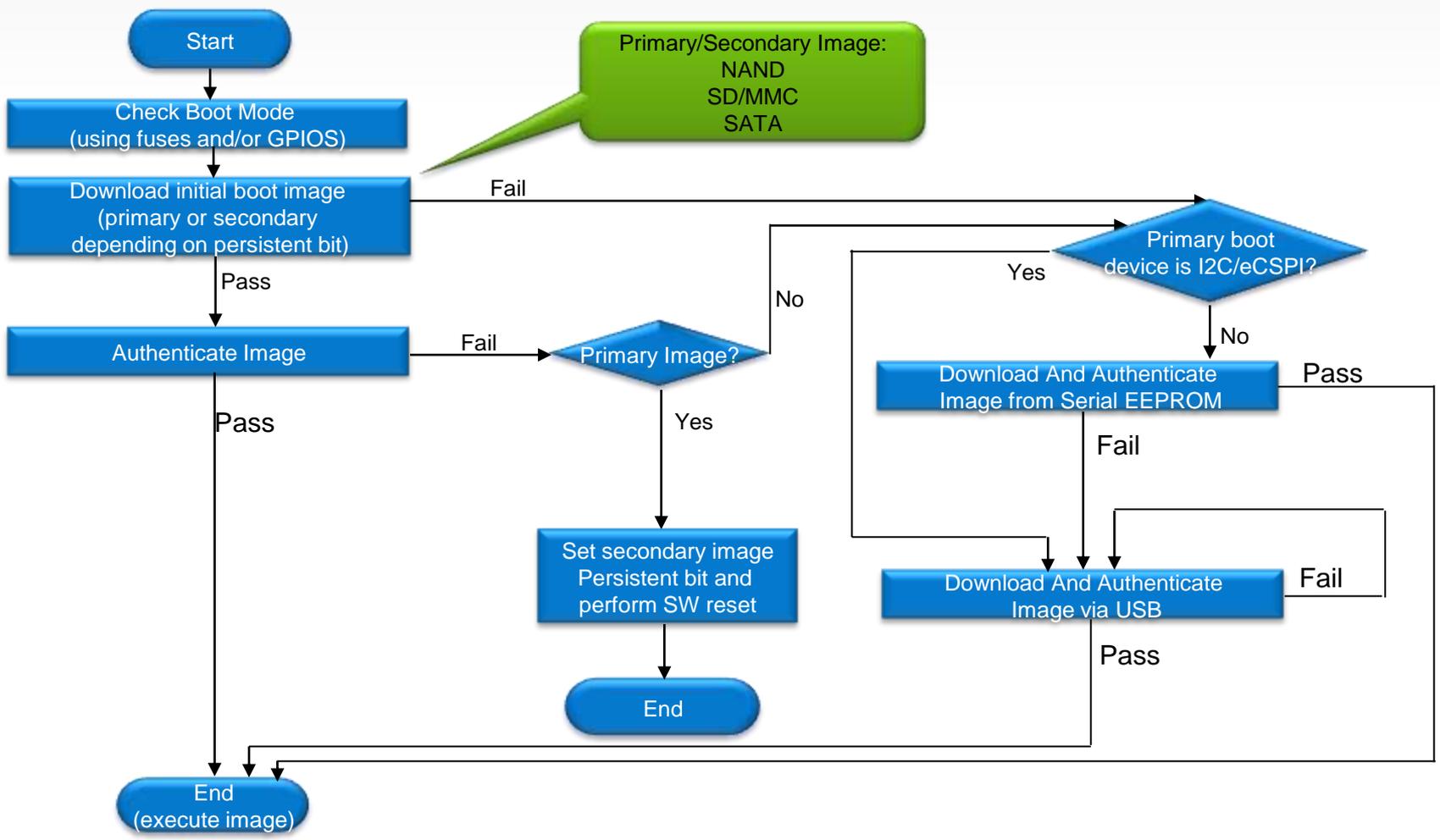
BOOT_MODE[1:0]	Mode	Description
00	Internal Boot (Production)	<p>BT_FUSE_SEL = 0: Boot via USB serial loader, on un-configured parts, indicated by unburned BT_FUSE_SEL fuse.</p> <p>BT_FUSE_SEL = 1: Boot according to fuse values BOOT_CFG, from either of the following sources:</p> <ul style="list-style-type: none"> <li>NOR Flash (via WEIM)</li> <li>OneNAND</li> <li>SPI (serial flash) / I2C</li> <li>NAND Flash, MLC NAND 2KB/4KB/8KB page (8-bit). 4-40-bit ECC.</li> <li>SD3.0/eMMC4.4.1 (support high capacity)/MoviNAND boot (through MMC interface)</li> <li>SATA (Hard disk or SSD)</li> </ul> <p>On error or exception in one of these modes: fallback to USB boot.</p>
01	Serial Downloader	Load and execute code, via USB (HID driver)
10	Internal Boot (Development)	<p>Executing ROM code, which handles booting from various sources (see mode '00' above).</p> <p>BT_FUSE_SEL=0: Boot source is selected by GPIO boot pins (overwrite BOOT_CFG fuses ).</p> <p>BT_FUSE_SEL=1: Boot source is selected by BOOT_CFG fuses. GPIO boot pins are ignored</p> <p>On error or exception in one of these modes: fallback to USB boot.</p>
11	FSL Test Mode	Freescale Test Mode, special mode reserved for device testing.

# Multicore Boot Flow (ROM)



**Note:**  
 On reset only CPU0 starts running. Other CPUs clock are gated.  
 CPU0 is responsible on enabling clocks of other CPUs.

# Boot Flow





# Operating System Release Version Control



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# Major Release Type Definition

Release	Support	Definition	Entry Criteria	Exit Criteria
<b>Alpha Release</b>	<b>No</b>	<ul style="list-style-type: none"> <li>Not expected to be feature or functionally complete</li> <li>Customers may start designs, but should not plan to take an Alpha Release into formal integration</li> <li>Validation executes only BAT</li> <li>Copyright and License Review (CLR) is required</li> <li>Very basic Out Of Box Test (OOBT)</li> <li>Core Team/Marketing approves Release to Customers</li> <li>Documentation (RN, User Guide) is also Alpha quality</li> </ul>	<ul style="list-style-type: none"> <li>Features are fully defined</li> <li>Internal repository mainlined</li> <li>Unit level test plan reviewed, entry criteria for next phase approved</li> <li>Basic UC (use case) unit test passes</li> <li>System test plan reviewed and signed off</li> <li>Documentation requirements reviewed and signed off</li> </ul>	<ul style="list-style-type: none"> <li>Core Team/Marketing Approval of unit and BAT issues.</li> <li>Documentation is updated to reflect the current state of the product</li> </ul>
<b>Beta Release</b>	<b>No</b>	<ul style="list-style-type: none"> <li>Feature and functional complete, may have major bugs or gaps</li> <li>Release supersedes all previous releases</li> <li>Qualified by Validation Team</li> <li>No customer support</li> <li>Customer issues tracked via CQ (escalated SRs) tickets, reviewed and commitment provided when applicable</li> </ul>	<ul style="list-style-type: none"> <li>Features included are functional but not necessarily hardened</li> <li>API finalized</li> <li>System Test Cases reviewed and signed off</li> <li>No S1 issues from <i>unit test</i></li> </ul>	<ul style="list-style-type: none"> <li>No S1 issues</li> <li>S2 issues require approval by the staff, release and core teams</li> <li>External Release passes OOBT</li> <li>Draft publication of release documents reviewed and approved</li> <li>The SW runs on all supported products and configurations</li> </ul>
<b>General Availability Release (GA)</b>	<b>Full</b>	<ul style="list-style-type: none"> <li>Release supersedes all previous releases</li> <li>Release is ready for customer integration and production</li> <li>Long term customer support expected</li> <li>Internal Release is fully qualified by the validation team at the system level on Freescale board(s)</li> <li>External Release is fully qualified by the OOBT Team</li> <li>May include alpha or beta level features but they are not advertised as supported from this release</li> </ul>	<ul style="list-style-type: none"> <li>Features included are fully functional and hardened</li> <li>API hardened</li> <li>No S1/S2 issues during <i>unit level</i> testing by Platform</li> <li>S3 <i>unit level</i> testing issues are reviewed by project management, Platform and Validation</li> <li>Draft publications updated</li> </ul>	<ul style="list-style-type: none"> <li>No open S1 or S2 issues</li> <li>S3 issues require approval by the staff and release teams</li> <li>External Release passes Out Of Box Test (OOBT)</li> <li>Release documentation reviewed and approved</li> </ul>

# Demo, Patch & Minor Release Definition

Release	Definition	Entry Criteria	Exit Criteria
<b>Demo Release</b>	<ul style="list-style-type: none"> <li>• Specific feature(s) pre-alpha demo</li> <li>• Not validated, only tagged</li> <li>• First silicon or new major/targeted feature/upgrade - may not be committed</li> <li>• Only images are available, no source code distribution</li> <li>• Code may not necessarily be in Git mainline</li> </ul>	<ul style="list-style-type: none"> <li>• Feature demonstrable</li> </ul>	<ul style="list-style-type: none"> <li>• Requestor/marketing approval</li> <li>• S1/S2 issues likely to be present</li> </ul>
<b>Patch Release</b>	<ul style="list-style-type: none"> <li>• Legacy Support, bug fix only</li> <li>• Fixes for one or more specific issues usually reported by the customer</li> <li>• Fix is tested in the customer HW when applicable</li> <li>• Limited Regression testing in FSL HW</li> </ul>	<ul style="list-style-type: none"> <li>• Code Complete</li> <li>• Test plan reviewed and approved</li> <li>• Draft Patch Release Notes Document</li> <li>• RM changes logged into CQ for next release if necessary</li> </ul>	<ul style="list-style-type: none"> <li>• Passes in customer HW (when applicable)</li> <li>• No new S1/S2 issues from regression testing</li> <li>• Patch Release Document reviewed and approved</li> </ul>
<b>Minor Release</b>	<ul style="list-style-type: none"> <li>• Legacy Support, includes new functionality and all patches to-date</li> <li>• Periodic Release for legacy products past mass production</li> <li>• Supersede all previous releases</li> <li>• Process is similar to that of a GA release</li> <li>• Internal Release is functionally qualified by the validation team at the system level</li> <li>• External Release is fully qualified by the Out Of Box Test (OOBT) Team</li> </ul>	<ul style="list-style-type: none"> <li>• Predefined periodic schedule:               <ul style="list-style-type: none"> <li>– Quarterly for 'new devices'</li> <li>– Biyearly for 'recent devices'</li> <li>– Yearly for 'mature devices'</li> </ul> </li> <li>• OR when a critical patch affecting all customers is found</li> </ul>	<ul style="list-style-type: none"> <li>• No open S1 or S2 issues</li> <li>• S3 issues require approval by the staff and release teams</li> <li>• External Release passes Sanity Testing</li> <li>• Release documentation reviewed, tested and approved</li> </ul>

# Generic Release Versioning (Semantic)

X.Y.Z-[alpha | beta].n-[rcm]  
 1.0.0-[alpha | beta].n-[rcm]

**Possible Release Sequence:**

**1.0.0-alpha – External Release**  
*1.0.0-alpha-rc1 – not releasable*  
*1.0.0-alpha-rc2 – not releasable*

**1.0.0-beta – External Release**  
*1.0.0-beta-rc1 – not releasable*  
*1.0.0-beta-rc2 – not releasable*

**1.0.0-beta.1 – Allows for more than 1 beta or alpha release**

**1.0.0**  
*1.0.0-rc1 – not releasable – 1<sup>st</sup> GA RC*  
*1.0.0-rc2 – not releasable – 2<sup>nd</sup> GA RC*

**1.0.1**  
**1.0.2**  
**1.1.0**  
**1.1.1**  
**2.0.0**

**X Major**  
 Backwards Incompatible Changes

**Y Minor**  
 Backwards Compatible  
 \* New Functionality  
 \* Deprecated Functionality  
 \* Substantial Improvement (ie support new board)

**Z Patch**  
 Backwards Compatible Bug Fixes



# Linux Release Version

Linux Release Name: LVersion\_X.Y.Z  
 L3.0.35\_2.0.0

Linux Release Pkg: LVersion\_X.Y.Z\_yyyymmdd.tar.gz  
 L3.0.35\_2.0.0\_20121106.tar.gz

L3.0.35_12.09.01_GA	MX 6DQ	:Exception already delivered (L3.0.35_1.0.0)
L3.0.35_12.10.02_GA	MX 6SL	:Exception about to be delivered (L3.0.35_2.0.0)
L3.0.35_1.1.0	MX 6DQ	:New functionality (current Post GA)
L3.0.35_1.1.1	MX 6DQ	:Example patch release (bug fix)
L3.0.35_2.1.0	MX 6SL	:Post GA Minor Release (example)
L3.0.35_3.0.0	MX6 DLS	:Current L3.0.35_12.11.01_GA
L3.0.35_4.0.0	MX6 DQ & DL/S	:Unified release (example)
L3.0.49_1.2.0	MX6DQ	:Compatible kernel upgrade (example)
L3.0.49_3.1.0	MX6DL/S	:Compatible kernel upgrade (example)
L3.5.7_1.0.0	MX 6DQ	:Incompatible Kernel Upgrade (Reset Major to 1)



# Android Release Version

Android Release Name: CodeNameVersion\_ **X.Y.Z**

JB4.1.2\_ **1.0.0**

Android Release Pkg: Android\_CodeNameVersion\_ **X.Y.Z** \_yyyymmdd.tar.gz

Android\_ JB4.1.2\_ **1.0.0** \_20130114.tar.gz

13.4.1 ICS 6 DQ, DL/S :Exception, 13.4 already released

13.5.0 ICS 6 SL :Exception 13.5 Beta already released

14.0.0 ICS 53 :Exception, early release in March 2012

JB4.1.2\_ **1.0.0** :First JB release, reset major to 1 (current 15.0.0)

JB4.1.2\_ **1.1.0** :Post GA (new functionality)

JB4.1.2\_ **2.0.0** :Same JB version, upgrade kernel version

JB4.2\_ **1.0.0** :New JB version (customers may not want to upgrade)

KLPx.y.z\_ **1.0.0-beta** :Beta release of first Key Lime Pie, reset Major to 1

KLPx.y.z\_ **1.0.0** :First GA Key Lime Pie release, 1.0.0



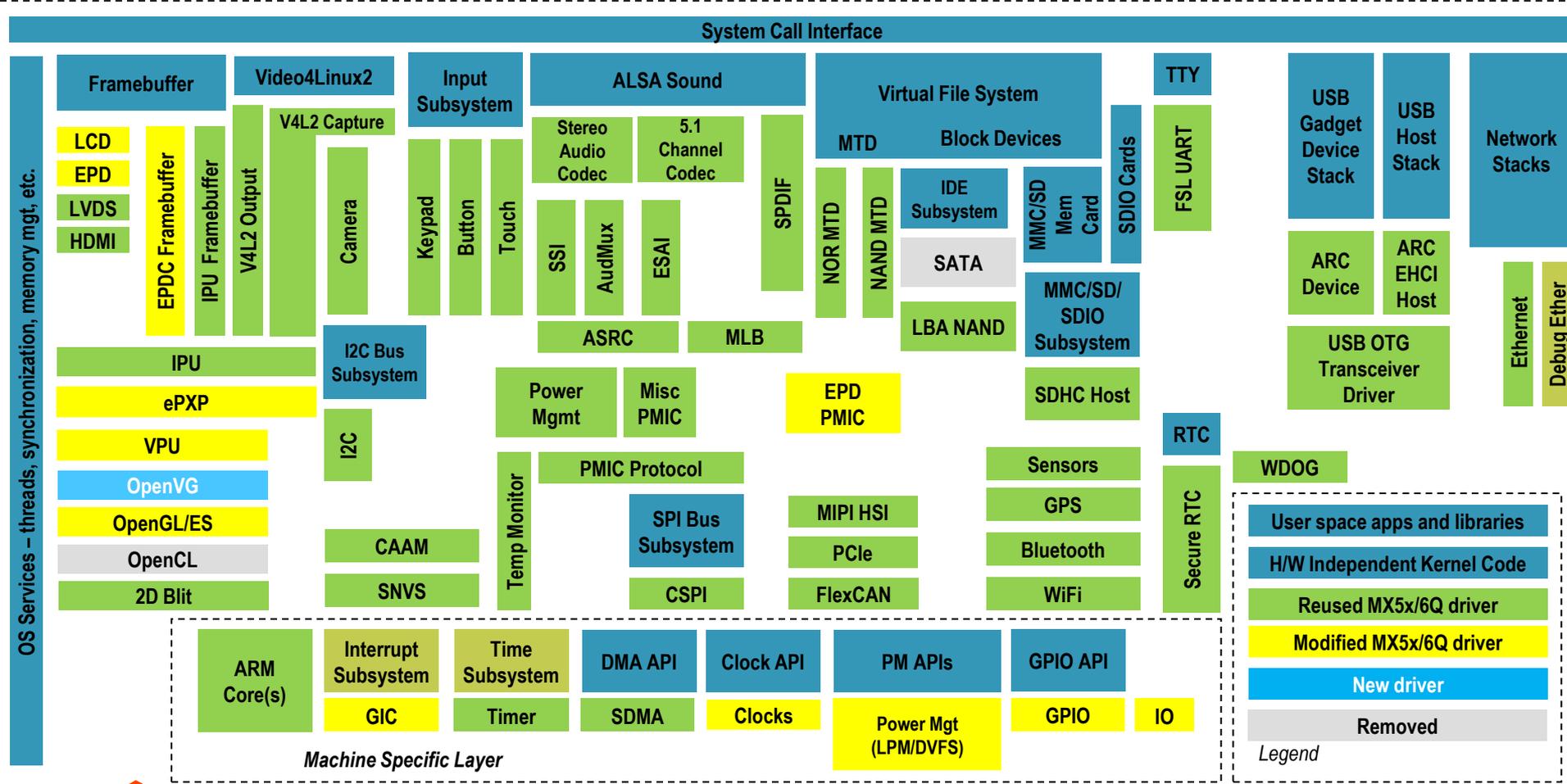
# Operating System Linux (LTIB & Yocto)



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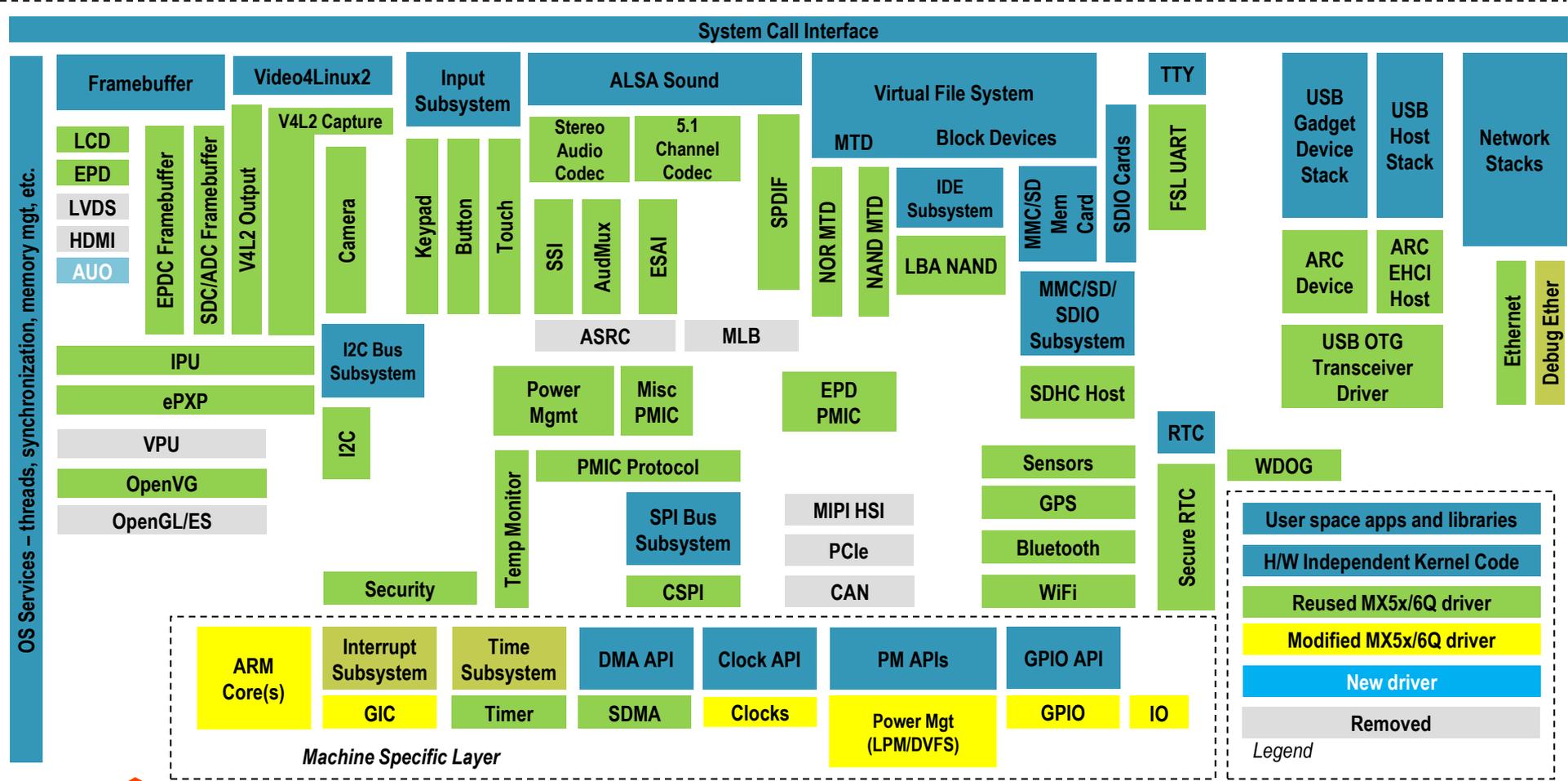
# NXP Linux Driver Similarity

## i.MX 6DualLite/Solo Compared to i.MX 6Quad/Dual Linux BSP Drivers

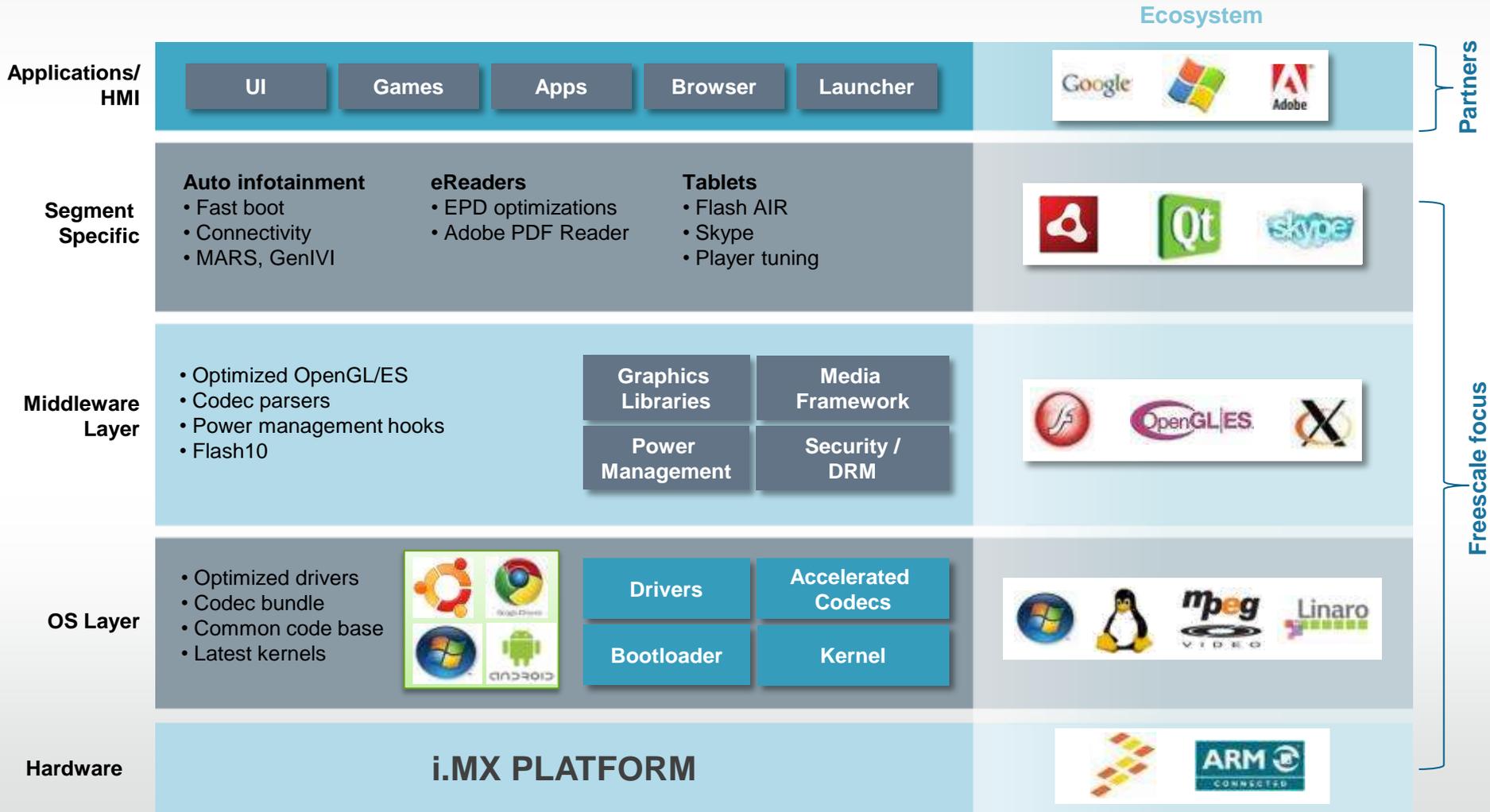


# NXP Linux Driver Similarity

## i.MX 6SoloLite Compared to i.MX 6Solo Linux BSP Drivers



# Software Completeness



# What is LTIB?

- Linux Target Image Builder (LTIB) is a tool created by Freescale that is used to build Linux target images, composed of a set of packages
  - A mechanism to deliver Linux board support packages (BSPs)
  - A wrapper around tool chains and standard Linux commands (cp, make, objcopy, tar, gcc, ...)
- Provides:
  - A known working configuration for a target board
  - Functionality to configure and build Linux system components (kernel, bootloader, application packages, ...)

# Typical LTIB Cycle

1. Download packages from the network/Internet/local repository
2. Build kernel, boot loader, and application packages from source
3. Deploy built packages to a root file system (RFS) tree
4. Prepare appropriate kernel or RFS image files ready for network or flash-based use on the embedded target board
5. Capture source modifications into patches and auto update the .spec files

# LTIB Build Host Setup

- LTIB is very picky and will likely not work unless the build environment is correct. Known to work with
  - Ubuntu 9.04 (Jaunty) Desktop
  - Ubuntu 10.04 (Lucid) Desktop
  - Both the 32 Bit and the 64 Bit install from the Desktop CD are supported
  - Other versions of Ubuntu are not supported and may have build issues
- Follow instructions listed in the document “Setting\_up\_LTIB\_Host\_L3.0.35\_1.1.0.pdf” included in the BSP documentation package

# Installing and Building LTIB

- Remove all previously-installed packages in /opt/freescale/pkg/.
- Install the LTIB package, not as root, in a location such as /home/user/.

```
tar zxvf L3.0.35_1.1.0_121218_source.tar.gz
./L3.0.35_1.1.0_121218_source/install
```

- Config the LTIB

```
cd <LTIB directory>
./ltib -m config
```

- Select platform to Freescale iMX reference boards and exit, saving the changes.
- To build U-Boot for target board, select “Choose your board for U-Boot” such as “mx6q\_sabreauto”.
- Close the configuration screen saving the changes.
- Run the following command to build LTIB.

```
./ltib
```

- When this procedure is completed, the kernel image and the U-Boot images are located at: rootfs/boot/.

# Useful LTIB Commands

- `./ltib -m selectype`  
Change the profile after the first selection.  
Min profile, FSL gnome release packages, and mfg firmware profile
- `./ltib -help`
- `./ltib -m listpkgs`  
List the packages in LTIB
- `./ltib -m prep -p <package name>`  
Get the source code of one package. The source code will be extracted to `<ltib folder>/rpm/BUILD`
- `./ltib -m scbuild -p <package name>`  
This command is used to build the source code of `<package name>`. If you modify the source code, you can rebuild the source code by this command
- `./ltib -m scdeploy -p <package name>`  
Install one package to rootfs

# What is Yocto?

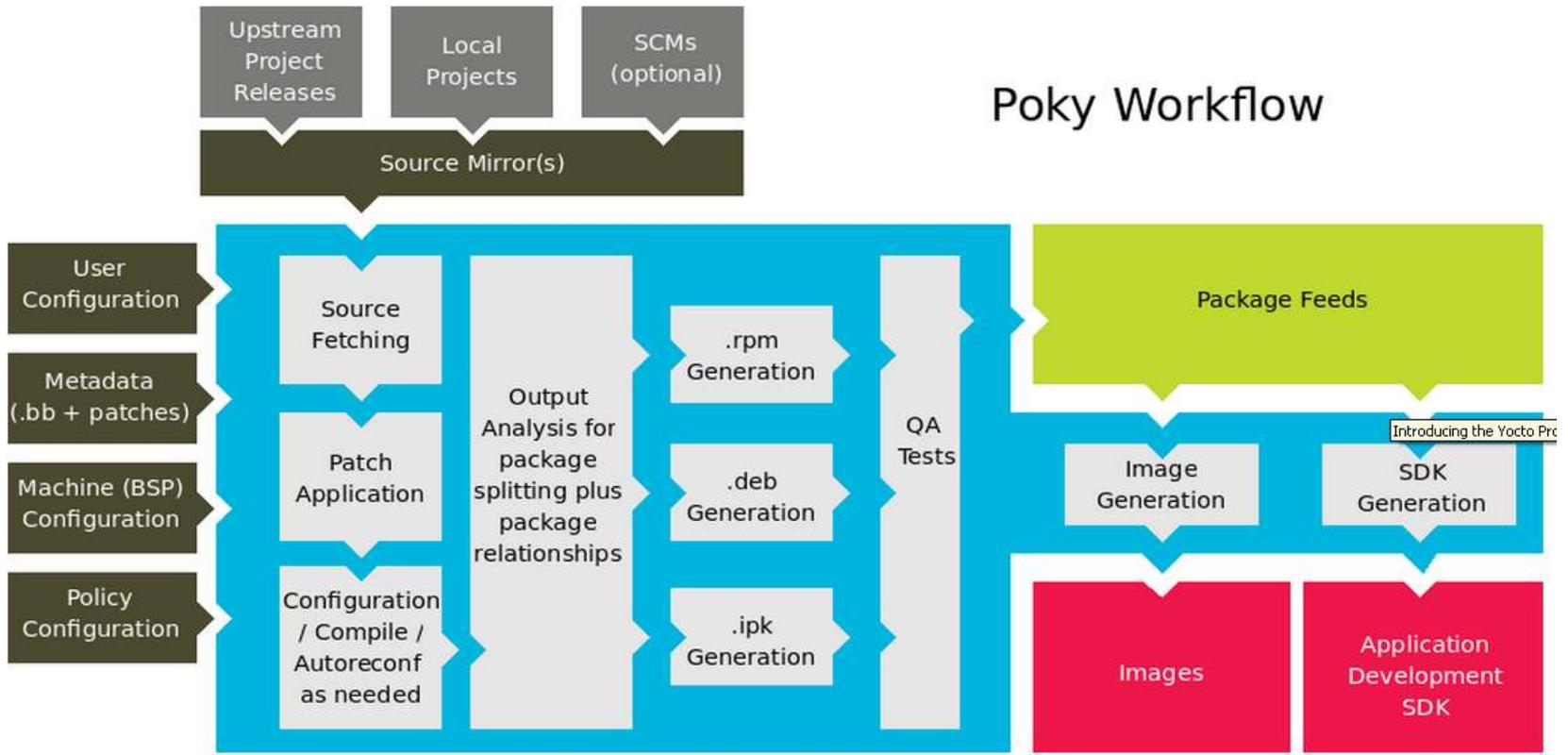
- The Yocto Project™ is an open source collaboration project that provides templates, tools and methods to help you create custom Linux-based systems for embedded products regardless of the hardware architecture.
- It consist of several separate projects to achieve the above goals
- In principal it is a typical open source project such as Linux or u-boot and consist of many individual contributors as well as companies making contributions (e.g. Intel, TI, Wind River, Mentor, etc)

# Yocto projects

- Bitbake
  - Parses metadata to run tasks
- OpenEmbedded Core
  - Core metadata and build information to build baseline embedded system
- Poky
  - Yocto example distribution which integrates all the required pieces and makes an official release
- HOB
  - GUI tool to select packages to build and easily create custom image
- Others: cross-prelink, eclipse IDE plugin, pseudo, and more...

# Poky Workflow

Fully supports a wide range of hardware and device emulation through the QEMU Emulator



The Yocto Project Development Environment

# Build with Yocto

- Yocto Build Host Setup

<http://www.yoctoproject.org/docs/1.0/yocto-quick-start/yocto-project-qs.html>

- Getting Yocto build framework

```
git clone git://git.yoctoproject.org/poky.git
```

- Getting Freescale meta layer

```
git clone git://github.com/Freescale/meta-fsl-arm.git
```

```
git clone ssh://sw-git.freescale.net/git/sw_git/repos/meta-fsl-mx.git
```

- Initializing the build environment

```
source oe-init-build-env
```

- Configure Yocto build for target board

```
conf/local.conf          User local config file
```

```
conf/bblayers.conf      Enables multiple meta layers
```

- Build the minimal image

```
bitbake core-image-minimal
```

- Build specific packages

```
bitbake gst-meta-base -c compile -f
```

```
bitbake gst-meta-base -c clean
```

- Run the image on emulator

```
poky/scripts/runqemu core-image-minimal qemux86
```



# Operating System Android



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# Android – Software Stack on Mobile Device

Apps (Java) – Everyone can create his/her own application based on “Open” Android API

## Android “Program” API

Middleware (Java) – App framework including window/focus management, inter-app communication, event notification, etc

Middleware (C/C++) – system libraries for media, graphic, database, font, web engine, etc

## Android “Porting” I/F

Linux kernel with Android patch. “Open Source” already



# Origin of Android Components

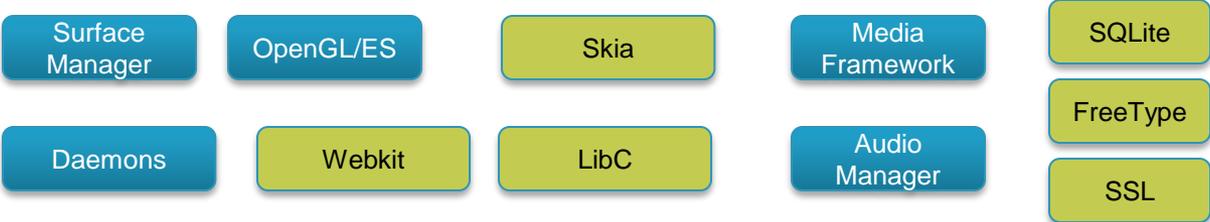
## Applications



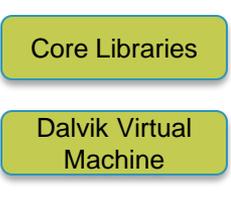
## Application Framework



## Libraries



## Runtime



## Utilities



## Hardware Abstraction Layer



## Linux Kernel



# Freescale Android Core Competencies

- **Porting**
  - Variety of FSL and 3<sup>rd</sup> party drivers integrated into single platform
  - Kernel level and component level optimizations
  
- **Enhancements**
  - Video and Graphics
  - Software updates, recovery and fastboot
  - 3G modem runtime detection, touch screen calibration
  
- **Extensions**
  - Flash 10.x / 11.x
  - Media formats
  - Multiple external storage
  - Dual display with auto detection
  - eInk optimizations
  - Complete multimedia framework implementation

# Examples of FSL Specific Android Porting

- Kernel
- Tuning HAL with i.MX Kernel
- 3G Modem & Telephony
- Multi-touch
- Bluetooth
- WIFI
- Display devices
- Camera
- G-sensor

# Examples of FSL Specific Android Enhancements

- Hardware accelerated video decoder/encoder
- Hardware accelerated CSC/Resize/Combining for rendering (especially for video frame rendering)
- Two video/camera rendering acceleration simultaneously
- GPU-based OpenGL/ES implementation
- GPU-based HW copyblt for display surface composition
- GPU-based HW acceleration for surface composition and display
- Software update and factory reset
- 3G modem runtime detection
- Touch screen calibration service
- Freescale optimized software audio decoders/encoders

# How To Use FSL Android Release

- **PC Setup**

Refer to "Setting up your machine" on the Android web site  
<http://source.android.com/source/initializing.html>.

- **Unpack i.MX Android Release Package**

```
$ cd /opt (or any other directory you like)
$ tar xzvf imx-android-r13.4-ga.tar.gz
$ cd imx-android-r13.4-ga/code
$ tar xzvf r13.4-ga.tar.gz
```

- **Unpack Google Android release Package**

```
$ tar xzvf myandroid_google_20120816.tar.gz
```

- **Patch Code for i.MX**

```
$ cd ~/myandroid
$ . /opt/imx-android-r13.4-ga/code/r13.4-ga/and_patch.sh
$ help
```

Now you should see "c\_patch" function is available for you

```
$ c_patch /opt/imx-android-r13.4-ga/code/r13.4-ga imx_r13.4-ga
```

# Build Android Image

- **Build the uboot, kernel, and Android image**

```
$ cd ~/myandroid
```

```
$ source build/envsetup.sh
```

```
$ lunch sabresd_6dq-user
```

```
$ make
```

"sabresd\_6dq" is the product name

(see ~/myandroid/device/fsl/product)

After build, check build\_\*\_android.log to make sure no build error.

- **Build out images**

under myandroid/out/target/product/sabresd\_6dq

boot.img(ulmage,ramdisk,boot parameters)

system.img recovery.img



# Operating System

## WinCE & QNX



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# WinCE/QNX

- **WEC6.0**
  - i.MX2x, i.MX3x, i.MX50, i.MX51 (FSL)
- **WEC7.0**
  - i.MX51, i.MX53 (FSL)
  - i.MX6x (3<sup>rd</sup> party)
- **QNX**
  - i.MX6x (3<sup>rd</sup> party)



# Hardware Platform SABRE SD



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# SABRE Board for Smart Devices (SDB)

## i.MX 6Quad 1Ghz Cortex-A9 Processor

- Can be configured as i.MX 6Dual
- Freescale MMPF0100 PMIC
- 1 GB DDR3 memory (non terminated)
- 3" x 7" 8-layer PCB

## Display connectors

- 2x LVDS connectors
- Connector for 24 bit 4.3" 800x480 WVGA with 4-wire touch screen
- HDMI Connector

## Audio

- Wolfson Audio Codec
- Microphone and headphone jacks

## Expansion Connector

- Camera CSI port signals
- I2C, SSI, SPI signals

**Part Numbers:** MCIMX6Q-SDB (\$399)

**Display (9.7"):** MCIMX-LVDS1 (\$499)

**Display (4.3"):** MCIMX28LCD (\$199)



## Tools Support

- Lauterbach, ARM (DS-5), Macraigor debug/IDE tool chain

## Connectivity

- 2x Full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector

## Debug

- JTAG connector
- Serial to USB connector

## Additional Features

- 3-axis Freescale accel
- eCompass
- Power supply
- No battery charger

## OS Support

- Linux and Android IceCream Sandwich from Freescale;
- Others: support by 3<sup>rd</sup> parties

# SABRE Platform for Smart Devices (SDP)

## i.MX 6Quad 1GHz Cortex-A9 Processor i.MX 6DualLite 1GHz Cortex-A9 Processor

- Freescale MMPF0100 PMIC
- 1 GB DDR3 memory (non terminated)
- 3" x 7" 8-layer PCB

### Part Numbers:

MCIMX6Q-SDP (\$999)  
MCIMX6DL-SDP (\$999)

### Display (4.3"): WiFi:

MCIMX28LCD (\$199)  
Silex WiFi module

### Connectivity

- 2x Full-size SD/MMC card slot
- 22-pin SATA connector
- 10/100/1000 Ethernet port
- 1x high-speed USB OTG port
- mPCI-e connector

### Display connectors

- Native 1024x768 LVDS display (comes with kit)
- 2<sup>nd</sup> LVDS connector
- Connector for 24 bit 4.3" 800x480 WVGA with 4-wire touch screen
- HDMI Connector
- MIPI DSI connector

### Audio

- Wolfson Audio Codec
- Microphone and headphone jacks
- Dual 1W Speakers

### Expansion Connector

- Enables parallel LCD or HDMI output
- Camera CSI port signals
- I2C, SSI, SPI signals

### Tools Support

- Lauterbach, ARM (DS-5), Macraigor debug/IDE tool chain



### Debug

- JTAG connector
- Serial to USB connector

### Additional Features

- 3-axis Freescale accel
- GPS receiver
- Ambient Light Sensor
- eCompass
- Dual 5MP Cameras
- Power supply
- Battery Charger
- Battery connectors

### OS Support

- Linux and Android IceCream Sandwich from Freescale;
- Others: support by 3<sup>rd</sup> parties



# Hardware Platform SABRE AI



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# SABRE Platform for Automotive Infotainment (AI)

## CPU Card Details

### Power and Memory

- Freescale MMPF0100 PMIC
- 2 GB DDR3 memory (i.MX 6Dual/Quad)
- 1GB DDR3 memory (i.MX 6Solo)
- 32GB Parallel NOR Flash
- NAND Socket

### Display

- LVDS connector
  - compatible with MCIMX-LVDS1
- Parallel RGB display interface
- HDMI output connector

### Debug

- JTAG connector
- Debug UART connector

### Connectivity and Expansion

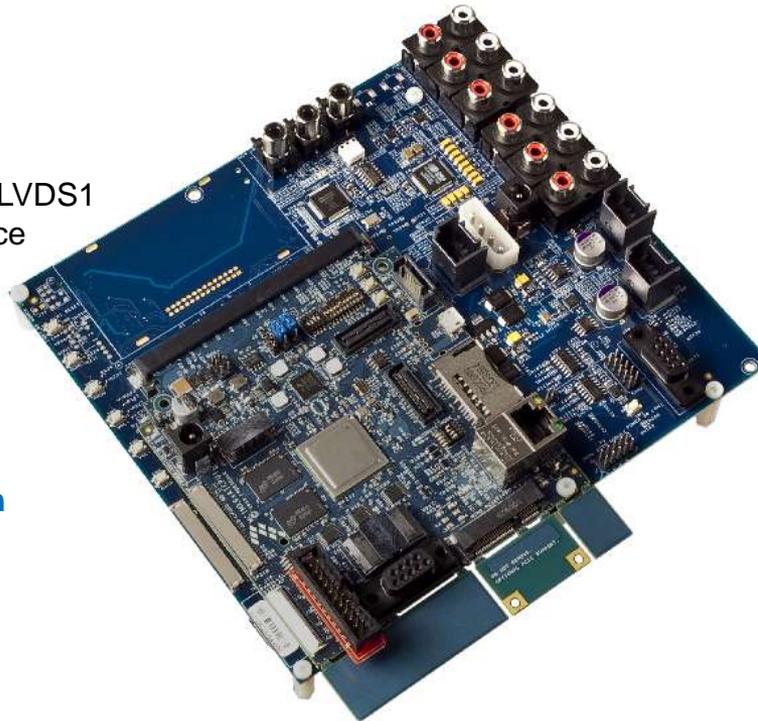
- SD Card Slot
- High Speed USB OTG
- Ethernet
- SATA
- MIPI CSI
- PCIe
- MLB150 INIC connector
- 281-pin MXM card edge connector for main board expansion

## Part Numbers

**Base Board:** MCIMXABASEV1 (\$699)

**CPU Cards:** MCIMX6SAICPU1 (\$799)  
MCIMX6QAICPU1 (\$799)

**Display:** MCIMX-LVDS1 (\$499)



## Base Board Details

### Can be reused from i.MX53 SABRE AI Connectivity and Expansion

- SD card slot (WiFi module or SD)
- Bluetooth or Bluetooth+WiFi header
- AM/FM tuner header
- Sirius XM Module header (de-pop'd)
- GPS (UART) module connector
- 2x CAN
- Dual High Speed USB Host connectors
- MLB 25/50 INIC connector
- SPI NOR flash

### Display I/O

- LVDS connector
  - compatible with MCIMX-LVDS1
- Analog Video Input
- LVDS Input

### Audio

- Cirrus multichannel audio codec
  - Up to 8 outputs
  - Dual microphone inputs
  - Stereo Line Level Input
- SPDIF receiver

### OS Support

- Linux
- Others: future support by 3<sup>rd</sup> parties



# Develop Tools

## ARM Debug



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# Platform Debug System

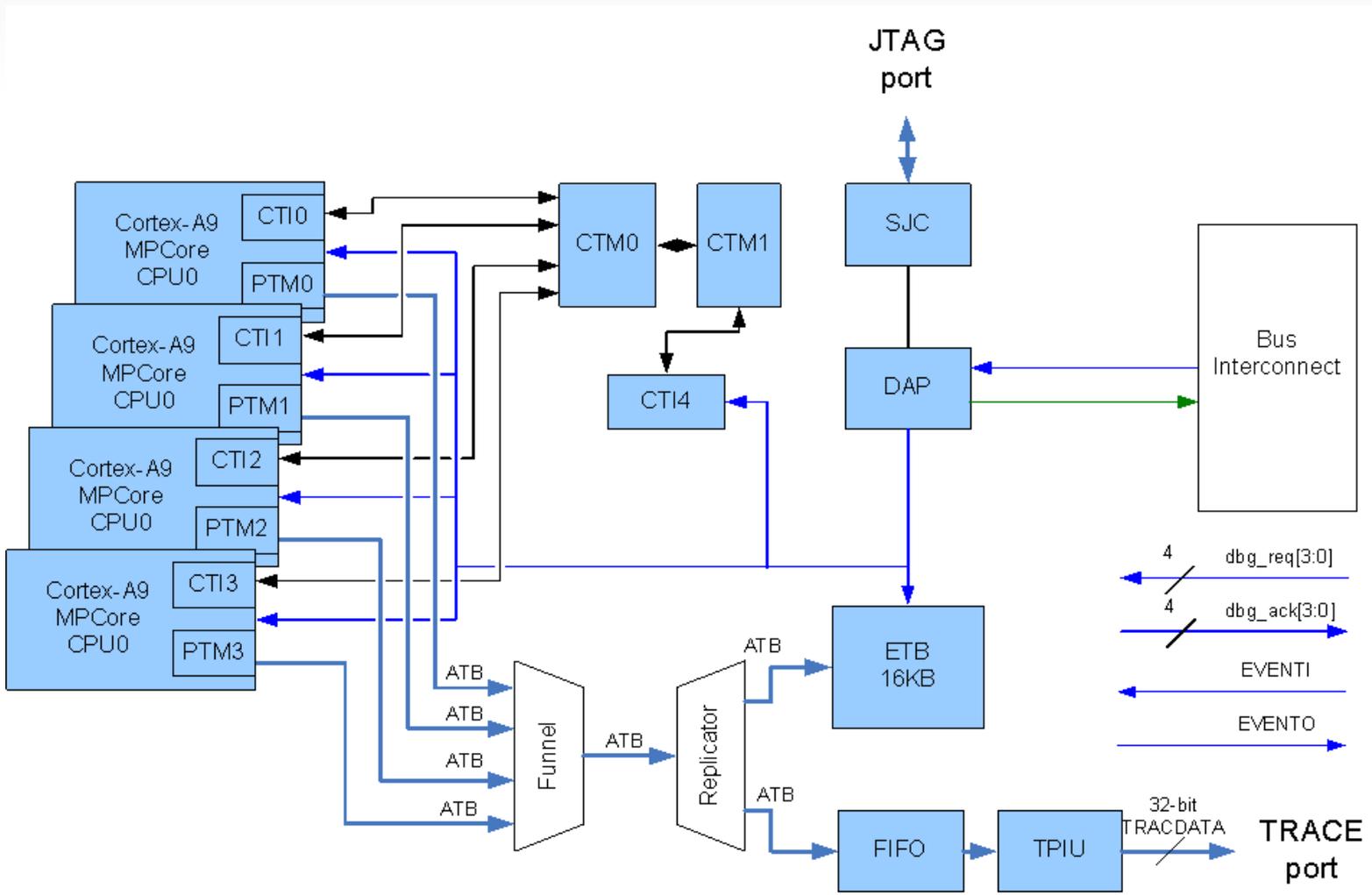
**The i.MX 6D/6Q debug and trace architecture is designed around the following:**

- ARM's CoreSight architecture, adapted to i.MX 6D/6Q SoC (for 2x and 4x core debug).
- JTAG port used to interact with cores under debug, via the System JTAG controller (SJC) port.
- Various SoC system resources, such as signal visibility and debug features built into i.MX 6D/6Q IP's.

## **CoreSight Components:**

- 4x PTM (One per core) – Program Trace Macrocell – For real-time program flow trace, uses TPIU port, for extracting trace data. (Require added Trace-Box HW, to capture and process the traces). The PTM is a replacement of ETM, used with A8 core system.
- Embedded Trace Buffer (ETB) - 16 Kbyte RAM array to be used for on-chip capture of trace data output from the PTM
- ATB Replicator to connect the trace data to TPIU (Trace Port Interface) and ETB (Embedded Trace Buffer).
- TPIU – Trace Port Interface, used for routing internal busses, to “Trace Port” signals.
- ATB Funnel - for capturing trace data from the either two or four cores.
- Cross Triggering logic, for event routing, including CTI's and CTM's.

# Debug Scheme



# Debug Scheme

Lauterbach:

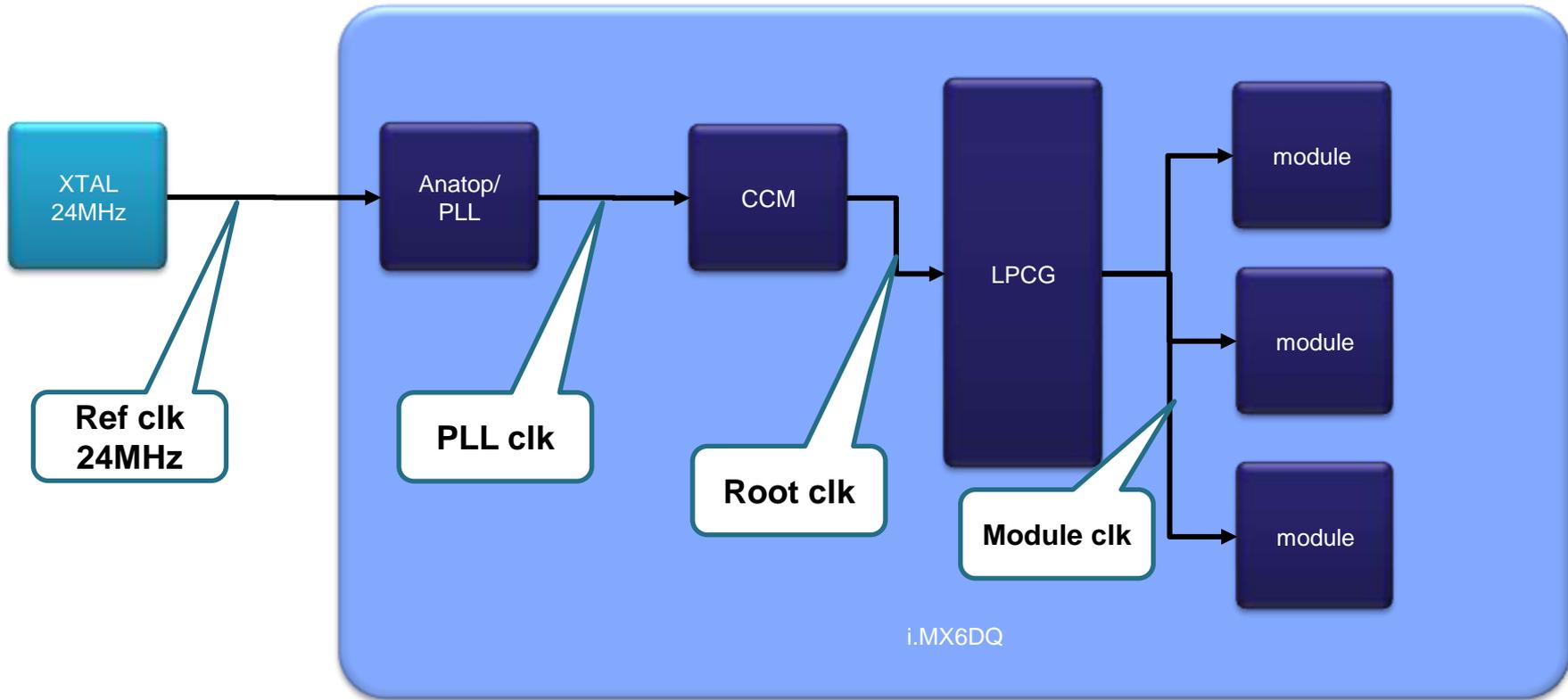
The screenshot shows the TRACE32 debugger interface. The main window displays assembly code with columns for address/line, code, label, mnemonic, and comment. The current instruction is highlighted in grey.

addr/line	code	label	mnemonic	comment
ZSR:001D2CF0	E3A00000		mov	r0,#0x0
ZSR:001D2CF4	E8BD0070		pop	{r4-r6,pc}
ZSR:001D2CF8	00242650		eorhi	r2,r4,r0,asr r6
ZSR:001D2CFC	0010C1D0		ldrsbhi	r14,[r11],-r0
ZSR:001D2D00	E92D4030		push	{r4-r5,r14}
ZSR:001D2D04	E59F4060		ldr	r4,0x001D2D6C
ZSR:001D2D08	E3A05000		mov	r5,#0x0
ZSR:001D2D0C	E5943004		ldr	r3,[r4,#0x4]
ZSR:001D2D10	E3530000		cmp	r3,#0x0
ZSR:001D2D14	1A000000		bne	0x001D2D44
ZSR:001D2D18	EBFFFC6D		bl	0x001D1ED4
ZSR:001D2D1C	E5040000		str	r0,[r4]
ZSR:001D2D20	E3700001		cmn	r0,#0x1
ZSR:001D2D24	0A000009		beq	0x001D2D50
ZSR:001D2D28	EBFFFC6B		bl	0x001D1EDC
ZSR:001D2D2C	E3700001		cmn	r0,#0x1
ZSR:001D2D30	0A000006		beq	0x001D2D50
ZSR:001D2D34	E3001000		mov	r1,#0x0
ZSR:001D2D38	E2800026		add	r0,r0,#0x260000
ZSR:001D2D3C	EBFFD06F		bl	0x001CA300
ZSR:001D2D40	E5040004		str	r0,[r4,#0x4]
ZSR:001D2D44	E3A05001		mov	r5,#0x1
ZSR:001D2D48	E1A00005		cpy	r0,r5
ZSR:001D2D4C	E8BD0030		pop	{r4-r5,pc}
ZSR:001D2D50	E5943004		ldr	r3,[r4,#0x4]
ZSR:001D2D54	E3530000		cmp	r3,#0x0
ZSR:001D2D58	0AFFFFFA		beq	0x001D2D48
ZSR:001D2D5C	E3A03000		mov	r3,#0x0
ZSR:001D2D60	E5043004		str	r3,[r4,#0x4]
ZSR:001D2D64	E1A00005		cpy	r0,r5
ZSR:001D2D68	E8BD0030		pop	{r4-r5,pc}
ZSR:001D2D6C	0024264C		eorhi	r2,r4,r12,asr #0x0C
ZSR:001D2D70	E59F2020		ldr	r2,0x001D2D98
ZSR:001D2D74	E5923000		ldr	r3,[r2]
ZSR:001D2D78	E3530000		cmp	r3,#0x0
ZSR:001D2D7C	13A03000		movne	r3,#0x0
ZSR:001D2D80	15023000		strne	r3,[r2]
ZSR:001D2D84	E5923004		ldr	r3,[r2,#0x4]

At the bottom, there is a control bar with buttons for emulate, trigger, devices, trace, Data, Var, List, PERF, SYStem, Step, Go, Break, Register, sYmbol, FPU, MMX, other, and previous. The status bar shows 'stopped' and 'MX UP'.

# Clock Generation Scheme

- Clock generation scheme is generally preserved from i.MX37/i.MX51 designs.

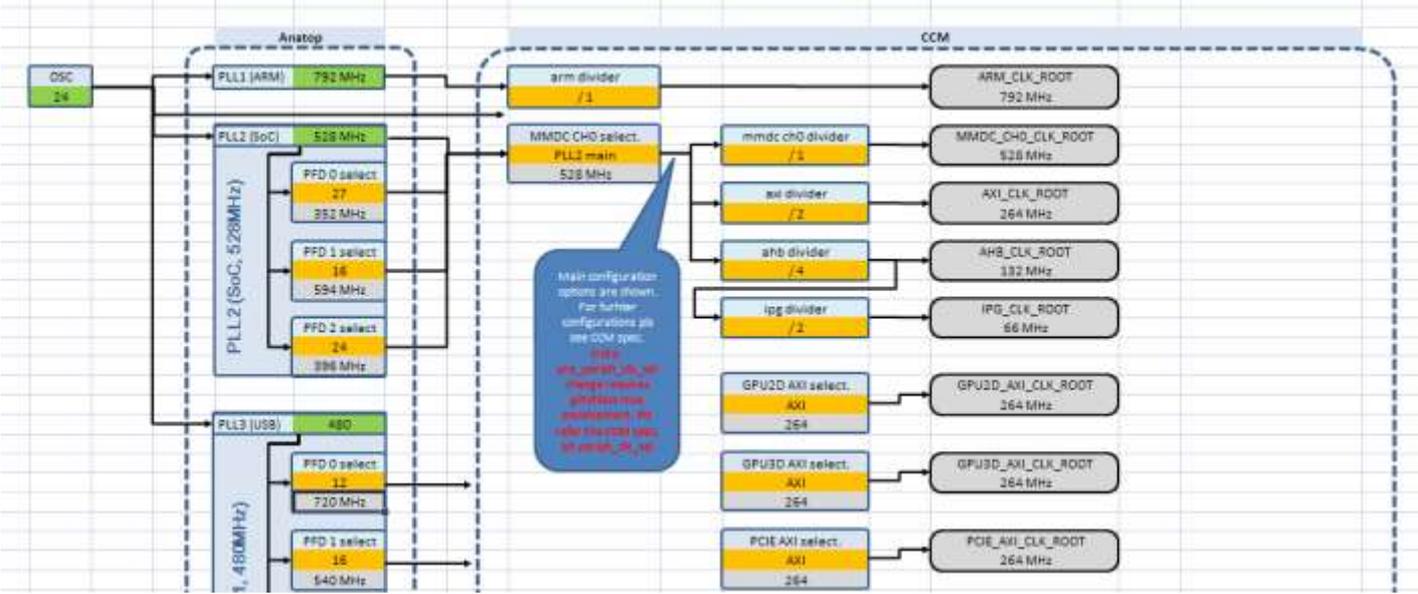


# Clock Generation Scheme *cont.*

- PLLs now are located in “anatotop” module. Anatotop module also includes PLL configuration registers.
- PLLs have additional output clock named PFD (phase fractional dividers)  
PFD clock depends on the main PLL clock and calculated by  $\text{Freq(PFD)} = \text{Freq(PLL)} * 18/N$  where N can range from 12-35.
  - Clocks of 5 PLLs are going from anatotop through CCM:
    - ARM PLL aka System PLL – PLL1
    - Bus PLL aka 528M PLL – PLL2
    - USB1 PLL aka 480M PLL – PLL3
    - High definition Audio PLL – PLL4
    - High definition Video PLL – PLL5
  - Clocks of 3 PLLs are going from anatotop directly to the modules:
    - ENET PLL – PLL6
    - USB2 PLL – PLL7
    - MLB PLL – PLL8

# Clock configuration

- Since clock configuration raises a lot of questions, a user-friendly tool was generated



- Excel-based tool provides visual configuration w/ drop-down options, while all selected clock frequencies are specified.
- This tool covers clock generation part from XTAL→PLL→CCM.





# Develop Tools IOMUX



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# IOMUX Tool

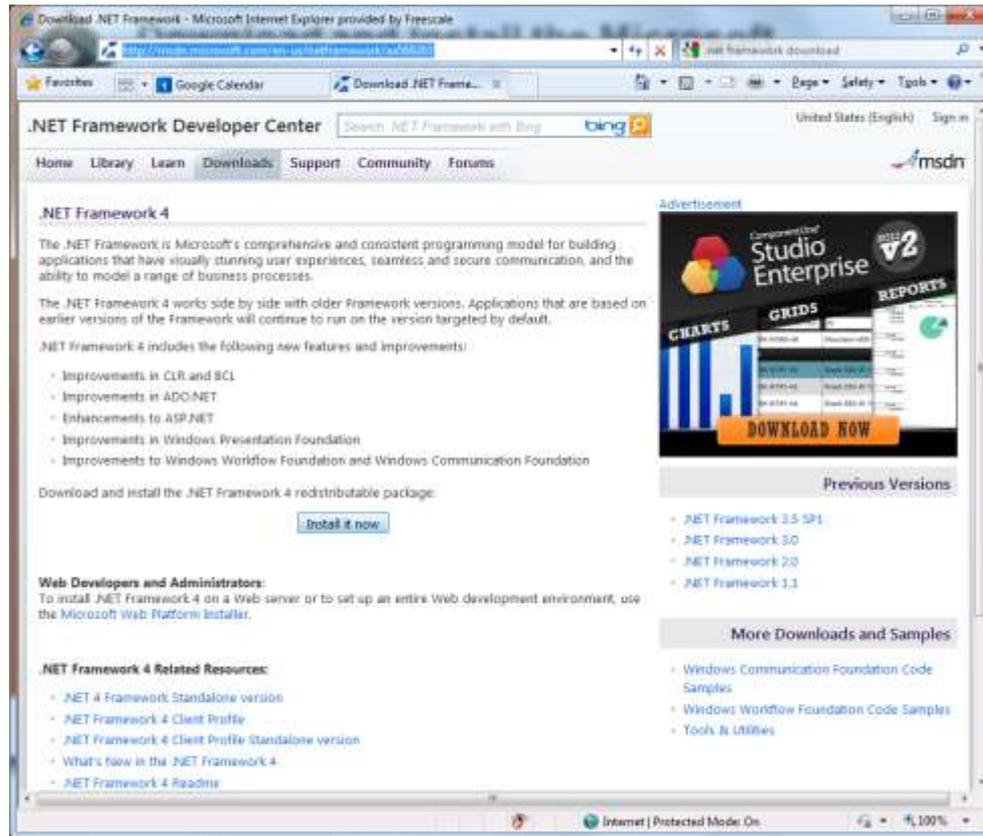
- Application Window Overview

The screenshot shows the IOMUX Tool interface for the i.MX6DQ - Demo Board Rev. A. The left pane displays a tree view of IOMUX configurations, with 'TXD\_MUX' selected under 'uart2'. A 'Signal Selection Pane' is overlaid on this tree, showing 'ALT2 - EIMD24 (F22)' selected. The main pane displays a table of peripheral signals with columns for Peripheral/Signal, Ball, Pad Name (AltMode), Power Group, GPIO, and Signal Notes. The table lists signals for uart1, uart2, uart3, and uart4. A 'Design Info Pane' is overlaid on the table, showing 'overview.jpg'. The status bar at the bottom indicates '0 conflicts!'.

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8)</b>					
CTS	G21	EIM_D19 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	3.300V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	3.300V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	3.300V - WEIM_SEC	gpio3_GPIO[24]	
RT	F23	EIM_EB3 (ALT3)	3.300V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	3.300V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	3.300V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4)</b>					
CTS	G23	EIM_D28 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[25]	Connected to U12, auxiliary console
<b>uart3 (4 of 4) Check power settings for NANDF, WEIM_SEC</b>					
CTS	J20	EIM_D30 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	3.300V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	F16	SD4_CLK (ALT2)	1.800V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	1.800V - NANDF	gpio7_GPIO[9]	
<b>uart4 (4 of 4) Set power level for GPIO</b>					
CTS	L3	CSIO_DAT17 (ALT3)	3.300V - IPU_CSI	gpio6_GPIO[3]	
RTS	L4	CSIO_DAT16 (ALT3)	3.300V - IPU_CSI	gpio6_GPIO[2]	
RXD_MUX	Y6	KEY_ROW0 (ALT4)	0.000V - GPIO	gpio4_GPIO[7]	
TXD_MUX	W5	KEY_COL0 (ALT4)	0.000V - GPIO	gpio4_GPIO[6]	

# Download and Install the Microsoft .NET Framework 4.0

- <http://msdn.microsoft.com/en-us/netframework/aa569263>



# Select Modules and Signals for Board

- Check the UARTS: UART1, UART2 and UART3.
- Expand all signals under UART3.

The screenshot shows the IO Mux configuration window for i.MX6DQ. On the left, a tree view shows the selection of UART1, UART2, and UART3 modules. Under UART3, all signals (CTS, RTS, RXD\_MUX, TXD\_MUX) are expanded. The right pane shows a table of selected signals with their corresponding ball numbers, pad names, power groups, and GPIO pins.

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8) Set power level for IPU_CSI</b>					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
<b>uart3 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	D25	EIM_D23 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
RTS	F23	EIM_EB3 (ALT2)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RXD_MUX	G22	EIM_D25 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
TXD_MUX	F22	EIM_D24 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[24]	

# Accessing Muxed-Signal Info

**IO Mux - <untitled> \***

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**i.MX6DQ - <board> <board revision>** (IOMux Design File Version: r<version> )

[12 of 197 muxed pins in use] **8 conflicts!**

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8) Set power level for IPU_CSI</b>					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
<b>uart3 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	D25	EIM_D23 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
RTS	F23	EIM_EB3 (ALT2)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RXD_MUX	G22	EIM_D25 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
TXD_MUX	F22	EIM_D24 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[24]	

i.MX6DQ [12 of 197 muxed pins in use] **8 conflicts!**

# Accessing Muxed-Signal Info

**IO Mux - <untitled> \***

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[12 of 197 muxed pins in use] **8 conflicts!**

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8) Set power level for IPU_CSI</b>					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
<b>uart3 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	D25	EIM_D23 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
RTS	F23	EIM_EB3 (ALT2)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RXD_MUX	G22	EIM_D25 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
TXD_MUX	F22	EIM_D24 (ALT2)	0.000V - WEIM_SEC	gpio3_GPIO[24]	

(weim\_WEIM\_D[24], ecspi4\_SS2, ecspi1\_SS2, ecspi2\_SS2, gpio3\_GPIO[24], audmux\_AUD5\_RXFS, uart1\_DTR)

i.MX6DQ [12 of 197 muxed pins in use] **8 conflicts!**

# Resolve Conflicting Signals

Select ALT4 – EIM\_D30(J20) for UART3/CTS.  
 Select ALT4 – EIM\_D31(H21) for UART3/RTS.

Select ALT2 – SD4\_CLK(E16) for UART3/RXD\_MUX.  
 Select ALT2 – SD4\_CMD(B17) for UART3/TXD\_MUX.

**IO Mux - <untitled>**

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**i.MX6DQ - <board> <board revision>** (IOMux Design File Version: r<version> )

[16 of 197 muxed pins in use] **0 conflicts!**

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8) Set power level for IPU_CSI</b>					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
<b>uart3 (4 of 4) Set power level for NANDF</b>					
CTS	J20	EIM_D30 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	E16	SD4_CLK (ALT2)	0.000V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	0.000V - NANDF	gpio7_GPIO[9]	

i.MX6DQ [16 of 197 muxed pins in use] **0 conflicts!**

# Adding Comments for Clarity

- Right-click the UART2/TXD\_MUX row in the Signals tab to bring up the context menu.
- Clicking on the menu will bring up a text entry field where the user may enter text.

The screenshot shows the IO Mux application interface. On the left is a tree view of components, including uart1, uart2, and uart3. The main area displays a table of signals for i.MX6DQ. The table has columns for Peripheral/Signal, Ball, Pad Name (AltMode), Power Group, GPIO, and Signal Notes. A context menu is open over the TXD\_MUX row of the uart2 group, showing the option 'Edit comment for uart2\_TXD\_MUX signal/port...'. The status bar at the bottom indicates '0 conflicts!'.

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8) Set power level for IPU_CSI</b>					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	
<b>uart3 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	J20	EIM_D30 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	E16	SD4_CLK (ALT2)	0.000V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	0.000V - NANDF	gpio7_GPIO[9]	

# Adding Comments for Clarity

IO Mux - <untitled> \*

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i.MX6DQ - <board> <board revision> (IOMux Design File Version: r<version> )

[16 of 197 muxed pins in use] 0 conflicts!

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>uart1 (8 of 8) Set power level for IPU_CSI</b>					
CTS	G21	EIM_D19 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[19]	
DCD	D25	EIM_D23 (ALT3)	0.000V - WEIM_SEC	gpio3_GPIO[23]	
DSR	G22	EIM_D25 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[25]	
DTR	F22	EIM_D24 (ALT7)	0.000V - WEIM_SEC	gpio3_GPIO[24]	
RI	F23	EIM_EB3 (ALT3)	0.000V - WEIM_SEC	gpio2_GPIO[31]	
RTS	G20	EIM_D20 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[20]	
RXD_MUX	M3	CSIO_DAT11 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[29]	
TXD_MUX	M1	CSIO_DAT10 (ALT3)	0.000V - IPU_CSI	gpio5_GPIO[28]	
<b>uart2 (4 of 4) Set power level for WEIM_SEC</b>					
CTS	G23	EIM_D28 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[28]	
RTS	J19	EIM_D29 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[29]	
RXD_MUX	E25	EIM_D27 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[27]	
TXD_MUX	E24	EIM_D26 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[26]	Connected to U12, auxiliary console
<b>uart3 (4 of 4) Set power level for NANDF</b>					
CTS	J20	EIM_D30 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[30]	
RTS	H21	EIM_D31 (ALT4)	0.000V - WEIM_SEC	gpio3_GPIO[31]	
RXD_MUX	E16	SD4_CLK (ALT2)	0.000V - NANDF	gpio7_GPIO[10]	
TXD_MUX	B17	SD4_CMD (ALT2)	0.000V - NANDF	gpio7_GPIO[9]	

i.MX6DQ [16 of 197 muxed pins in use] 0 conflicts!

# Ball Diagram View

**IO Mux - <untitled> \***

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Tree View:

- ▶ spdif
- ▶ src
- ▶ tcu
- ▶ tpsmp
- ▶  uart1 (8 of 8)
  - ▶  CTS ALT4 - EIM\_D19 (G21)
  - DCD ALT3 - EIM\_D23 (D25)
  - DSR ALT7 - EIM\_D25 (G22)
  - DTR ALT7 - EIM\_D24 (F22)
  - RI ALT3 - EIM\_EB3 (F23)
  - ▶  RTS ALT4 - EIM\_D20 (G20)
  - ▶  RXD\_MUX ALT3 - CSIO\_DAT11 (M3)
  - ▶  TXD\_MUX ALT3 - CSIO\_DAT10 (M1)
- ▶  uart2 (4 of 4)
- ▶  uart3 (4 of 4)
  - ▶  CTS ALT4 - EIM\_D30 (J20)
    - ALT2 - EIM\_D23 (D25)
    - ALT4 - EIM\_D30 (J20)
    - ALT1 - SD3\_DAT3 (B15)
  - ▶  RTS ALT4 - EIM\_D31 (H21)
    - ALT2 - EIM\_EB3 (F23)
    - ALT4 - EIM\_D31 (H21)
    - ALT1 - SD3\_RST (D15)
  - ▶  RXD\_MUX ALT2 - SD4\_CLK (E16)
    - ALT2 - EIM\_D25 (G22)
    - ALT2 - SD4\_CLK (E16)
  - ▶  TXD\_MUX ALT2 - SD4\_CMD (B17)
    - ALT2 - EIM\_D24 (F22)
    - ALT2 - SD4\_CMD (B17)
- ▶  uart4
- ▶  uart5
- ▶  usboh3
- ▶  usdhc1
- ▶  usdhc2
- ▶  usdhc3
- ▶  usdhc4
- ▶  wdog1
- ▶  wdog2
- ▶  weim

Ball Diagram Grid (Pin A-AE, 1-25):

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	A
B	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	In Use	Not Muxed	B							
C	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	C
D	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	In Use	In Use	D
E	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	In Use	Not Muxed	In Use	In Use	In Use	E					
F	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	In Use	In Use	In Use	In Use	F
G	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	G
H	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	In Use	In Use	In Use	In Use	H
J	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	J
K	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	K
L	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	L
M	In Use	Not Muxed	<b>In Use</b>	Not Muxed	M																					
N	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	N
P	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	P
R	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	R
T	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	T
U	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	U
V	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	V
W	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	W
Y	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Y
AA	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	AA
AB	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	AB
AC	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	AC
AD	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	AD
AE	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	Not Muxed	AE

Legend:

- Ground (Grey)
- Power (Red)
- Not Muxed (Brown)
- Available (Light Yellow)
- In Use (Green)
- Conflicted (Red)

i.MX6DQ [16 of 197 muxed pins in use] **0 conflicts!**



# Pads "Spreadsheet" View

IO Mux - <untitled> \*

File Device Code View Help

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Signals Ball Diagram Pads Registers Power General

spdif  
 src  
 tcu  
 tpsmp  
 uart1 (8 of 8)  
    CTS ALT4 - EIM\_D19 (G21)  
    DCD ALT3 - EIM\_D23 (D25)  
    DSR ALT7 - EIM\_D25 (G22)  
    DTR ALT7 - EIM\_D24 (F22)  
    RI ALT3 - EIM\_EB3 (F23)  
    RTS ALT4 - EIM\_D20 (G20)  
    RXD\_MUX ALT3 - CSIO\_DAT11 (M3)  
    TXD\_MUX ALT3 - CSIO\_DAT10 (M1)  
 uart2 (4 of 4)  
 uart3 (4 of 4)  
    CTS ALT4 - EIM\_D30 (J20)  
      ALT2 - EIM\_D23 (D25)  
      ALT4 - EIM\_D30 (J20)  
      ALT1 - SD3\_DAT3 (B15)  
    RTS ALT4 - EIM\_D31 (H21)  
      ALT2 - EIM\_EB3 (F23)  
      ALT4 - EIM\_D31 (H21)  
      ALT1 - SD3\_RST (D15)  
    RXD\_MUX ALT2 - SD4\_CLK (E16)  
      ALT2 - EIM\_D25 (G22)  
      ALT2 - SD4\_CLK (E16)  
    TXD\_MUX ALT2 - SD4\_CMD (B17)  
      ALT2 - EIM\_D24 (F22)  
      ALT2 - SD4\_CMD (B17)  
 uart4  
 uart5  
 usboh3  
 usdhc1  
 usdhc2  
 usdhc3  
 usdhc4  
 wdog1  
 wdog2  
 weim

BALL	PAD NAME	POWER GROUP	DEFAULT MODE	ALT0 MODE	ALT1 MODE	ALT2 MODE
D4	CSL_REXT	MIPI				
D5	CLK2_P	ANATOP				
D6	GND					
D7	CLK1_P	ANATOP				
D8	GND					
D9	RTC_XTALI	ANATOP				
E1	CSL_D2M	MIPI				
E10	USB_H1_DP	ANATOP				
E11	TAMPER	RESET				
E12	TEST_MODE	RESET				
E13	SD3_DAT6	SD3	ALT5	usdhc3_DAT6	uart1_RXD_MUX	pcie_ctrl_DIAG_STATUS_BUS_MUX[E
E14	SD3_DAT0	SD3	ALT5	usdhc3_DAT0	uart1_CTS	can2_TXCAN
E15	NANDF_WP_B	NANDF	ALT5	rawnand_RESETN	ipu2_SISG[5]	pcie_ctrl_DIAG_STATUS_BUS_MUX[
E16	SD4_CLK	NANDF	ALT5	usdhc4_CLK	rawnand_WRN	uart3_RXD_MUX
E17	NANDF_D6	NANDF	ALT5	rawnand_D6	usdhc2_DAT6	gpu3d_GPU_DEBUG_OUT[6]
E18	SD4_DAT4	NANDF	ALT5	rawnand_D12	usdhc4_DAT4	uart2_RXD_MUX
E19	SD1_DAT2	SD1	ALT5	usdhc1_DAT2	ecspi5_SS1	gpt_CMPOUT2
E2	CSL_D2P	MIPI				
E20	SD2_DAT1	SD2	ALT5	usdhc2_DAT1	ecspi5_SS0	weim_WEIM_CS[2]
E21	RGMII_TD2	RGMII	ALT5	mipi_hsi_ctrl_RX_DATA	enet_RGMII_TD2	
E22	EIM_EB2	WEIM_SEC	ALT5	weim_WEIM_EB[2]	ecspi1_SS0	ccm_DI1_EXT_CLK
E23	EIM_D22	WEIM_SEC	ALT5	weim_WEIM_D[22]	ecspi4_MISO	ipu1_DIO_PIN1
E24	EIM_D26	WEIM_SEC	ALT5	weim_WEIM_D[26]	ipu1_D11_PIN11	ipu1_CSI0_D[1]
E25	EIM_D27	WEIM_SEC	ALT5	weim_WEIM_D[27]	ipu1_D11_PIN13	ipu1_CSI0_D[0]
E3	CSL_D0P	MIPI				
E4	CSL_D0M	MIPI				
E5	GND					
E6	GND					

i.MX6DQ [16 of 197 muxed pins in use] 0 conflicts!



# Configuring IOMUXC Registers

- Select UART3/RXD\_MUX in the left-hand pane.
- All of the IOMUXC Registers associated with the AD4\_CLK(E16) pad are shown on the Registers Tab in the right-hand pane.

The screenshot shows the IOMUXC configuration tool interface. On the left, a tree view lists various pins and their associated ALTs. The 'RXD\_MUX ALT2 - SD4\_CLK (E16)' pin is selected and highlighted with a blue oval. The right pane displays the configuration registers for this pad. The 'Pad Name' is 'SD4\_CLK' and the 'Mode' is 'ALT2'. The 'Registers' tab is active, showing three registers:

Register Name	Address	Value
IOMUXC_SW_MUX_CTL_PAD_SD4_CLK	0x020E02F8	0x00000002
IOMUXC_UART3_IPP_UART_RXD_MUX_SELECT_INPUT	0x020E0930	0x00000003
IOMUXC_SW_PAD_CTL_PAD_SD4_CLK	0x020E06E0	0x0001B0B0

The 'MUX\_MODE (2-0)' field in the first register is set to 'ALT2 (2)'. The 'DAISY (1-0)' field in the second register is set to 'SEL\_SD4\_CLK\_ALT2(3)'. The status bar at the bottom indicates '0 conflicts!'.



# Drag a Signal to another Module

IO Mux - C:\ViewStorage\IOMux\_Tool.v3\Apps.Net\IOMux\boards\i.MX6DQ\_QSB\_Rev.A\IoMuxDesign.xml

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Signals Ball Diagram Pads Registers Power General

i.MX6DQ - QSB Rev. A (IOMux Design File Version: r2)

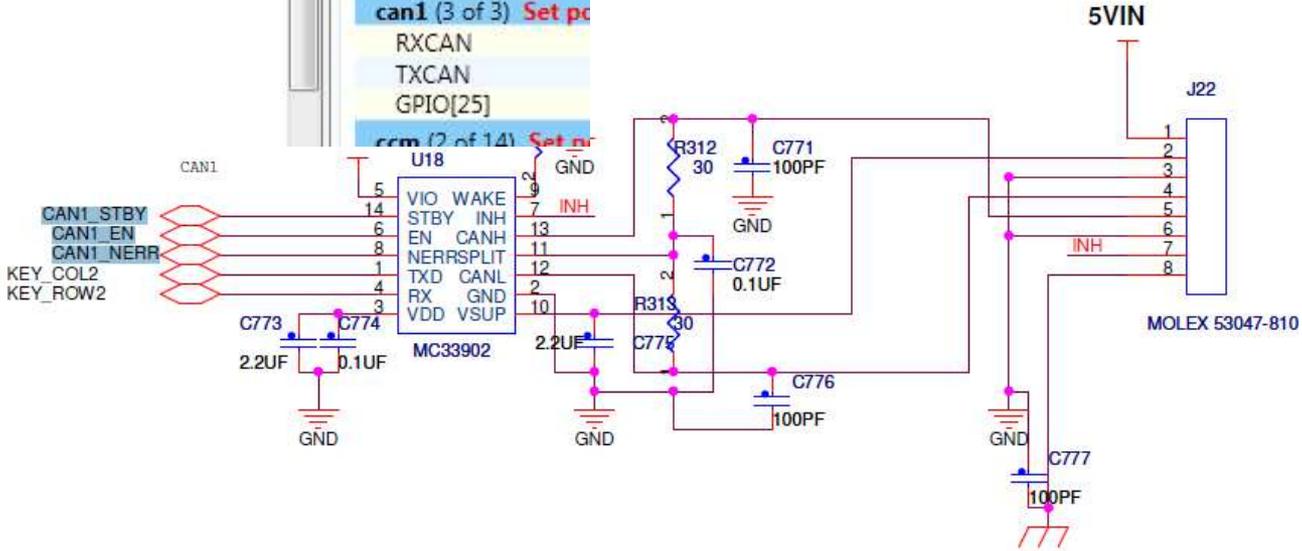
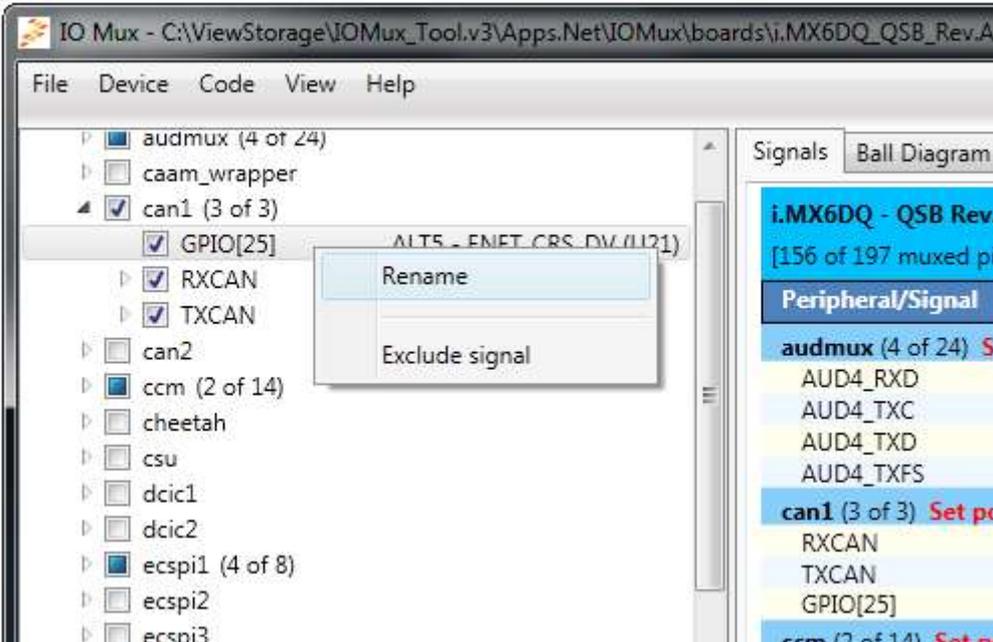
156 of 197 muxed pins in use | 0 conflicts!

Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>audmux (4 of 24) Set power level for SD2</b>					
AUD4_RXD	A22	SD2_DAT0 (ALT3)	0.000V - SD2	gpio1_GPIO[15]	
AUD4_TXC	B22	SD2_DAT3 (ALT3)	0.000V - SD2	gpio1_GPIO[12]	
AUD4_TXD	A23	SD2_DAT2 (ALT3)	0.000V - SD2	gpio1_GPIO[13]	
AUD4_TXFS	E20	SD2_DAT1 (ALT3)	0.000V - SD2	gpio1_GPIO[14]	
<b>can1 (2 of 2) Set power level for GPIO</b>					
RXCAN	W4	KEY_ROW2 (ALT2)	0.000V - GPIO	gpio4_GPIO[11]	
TXCAN	W6	KEY_COL2 (ALT2)	0.000V - GPIO	gpio4_GPIO[10]	
<b>ccm (2 of 14) Set power level for GPIO</b>					
CLKO	T5	GPIO_0 (ALT0)	0.000V - GPIO	gpio1_GPIO[0]	SGTL5000 - sys_mclk
CLKO2	R7	GPIO_3 (ALT4)	0.000V - GPIO	gpio1_GPIO[3]	J5 - Camera mclk
<b>ecspi1 (4 of 8) Set power level for GPIO</b>					
MISO	U7	KEY_COL1 (ALT0)	0.000V - GPIO	gpio4_GPIO[8]	
MOSI	V6	KEY_ROW0 (ALT0)	0.000V - GPIO	gpio4_GPIO[7]	
SCLK	W5	KEY_COL0 (ALT0)	0.000V - GPIO	gpio4_GPIO[6]	
SS0	U6	KEY_ROW1 (ALT0)	0.000V - GPIO	gpio4_GPIO[9]	
<b>enet (14 of 39) Set power level for ENET</b>					
MDC	V20	ENET_MDC (ALT1)	0.000V - ENET	gpio1_GPIO[31]	
MDIO	V23	ENET_MDIO (ALT1)	0.000V - ENET	gpio1_GPIO[22]	
RGMIIR_RD0	C24	RGMIIR_RD0 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[25]	
RGMIIR_RD1	B23	RGMIIR_RD1 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[27]	
RGMIIR_RD2	B24	RGMIIR_RD2 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[28]	
RGMIIR_RD3	D23	RGMIIR_RD3 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[29]	
RGMIIR_RX_CTL	D22	RGMIIR_RX_CTL (ALT1)	0.000V - RGMIIR	gpio6_GPIO[24]	
RGMIIR_RXC	B25	RGMIIR_RXC (ALT1)	0.000V - RGMIIR	gpio6_GPIO[30]	
RGMIIR_TD0	C22	RGMIIR_TD0 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[20]	
RGMIIR_TD1	F20	RGMIIR_TD1 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[21]	
RGMIIR_TD2	E21	RGMIIR_TD2 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[22]	
RGMIIR_TD3	A24	RGMIIR_TD3 (ALT1)	0.000V - RGMIIR	gpio6_GPIO[23]	
RGMIIR_TX_CTL	C23	RGMIIR_TX_CTL (ALT1)	0.000V - RGMIIR	gpio6_GPIO[26]	
RGMIIR_TXC	D21	RGMIIR_TXC (ALT1)	0.000V - RGMIIR	gpio6_GPIO[19]	
<b>gpio1 (10 of 32) Set power level for ENET</b>					
GPIO[16]	A21	SD1_DAT0 (ALT5)	0.000V - SD1		J5 - Camera GP

i.MX6DQ [156 of 197 muxed pins in use] 0 conflicts!



# Rename Signal to Match Schematics



# CAN1 Module with All Signals

- Comments auto-generated to denote original Module/Signal.

IO Mux - C:\ViewStorage\IOmux\_Tool.v3\Apps.Net\IOmux\boards\i.MX6DQ\_QSB\_Rev.A\IoMuxDesign.xml

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Signals Ball Diagram Pads Registers Power General

i.MX6DQ - QSB Rev. A (IOmux Design File Version: r3)

[156 of 197 muxed pins in use] 0 conflicts!

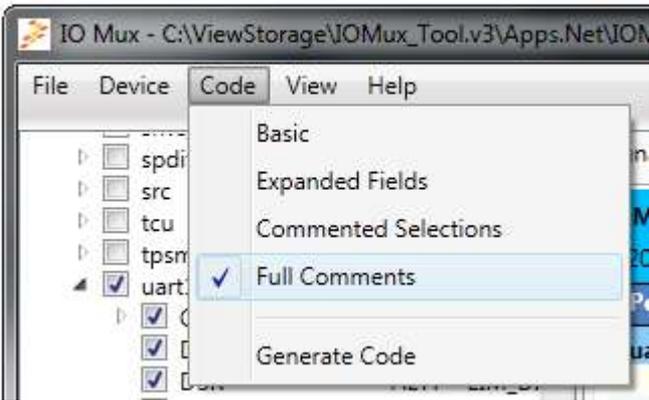
Peripheral/Signal	Ball	Pad Name (AltMode)	Power Group	GPIO	Signal Notes
<b>audmux (4 of 24) Set power level for SD2</b>					
AUD4_RXD	A22	SD2_DAT0 (ALT3)	0.000V - SD2	gpio1_GPIO[15]	
AUD4_TXC	B22	SD2_DAT3 (ALT3)	0.000V - SD2	gpio1_GPIO[12]	
AUD4_TXD	A23	SD2_DAT2 (ALT3)	0.000V - SD2	gpio1_GPIO[13]	
AUD4_TXFS	E20	SD2_DAT1 (ALT3)	0.000V - SD2	gpio1_GPIO[14]	
<b>can1 (5 of 5) Set power level for ENET</b>					
RXCAN	W4	KEY_ROW2 (ALT2)	0.000V - GPIO	gpio4_GPIO[11]	
TXCAN	W6	KEY_COL2 (ALT2)	0.000V - GPIO	gpio4_GPIO[10]	
CAN1_STBY	U21	ENET_CRSDV (ALT5)	0.000V - ENET		
CAN1_NERR	W22	ENET_RXD1 (ALT5)	0.000V - ENET		WAS Instance:gpio1 Signal:GPIO[26]
CAN1_EN	W21	ENET_RXD0 (ALT5)	0.000V - ENET		WAS Instance:gpio1 Signal:GPIO[27]
<b>ccm (2 of 14) Set power level for GPIO</b>					
CLKO	T5	GPIO_0 (ALT0)	0.000V - GPIO	gpio1_GPIO[0]	SGTL5000 - sys_mclk
CLKO2	R7	GPIO_3 (ALT4)	0.000V - GPIO	gpio1_GPIO[3]	J5 - Camera mclk
<b>ecspi1 (4 of 8) Set power level for GPIO</b>					
MISO	U7	KEY_COL1 (ALT0)	0.000V - GPIO	gpio4_GPIO[8]	
MOSI	V6	KEY_ROW0 (ALT0)	0.000V - GPIO	gpio4_GPIO[7]	
SCLK	W5	KEY_COL0 (ALT0)	0.000V - GPIO	gpio4_GPIO[6]	
SS0	U6	KEY_ROW1 (ALT0)	0.000V - GPIO	gpio4_GPIO[9]	
<b>enet (14 of 39) Set power level for ENET</b>					
MDC	V20	ENET_MDC (ALT1)	0.000V - ENET	gpio1_GPIO[31]	
MDIO	V23	ENET_MDIO (ALT1)	0.000V - ENET	gpio1_GPIO[22]	
RGMIIRD0	C24	RGMIIRD0 (ALT1)	0.000V - RGMII	gpio6_GPIO[25]	
RGMIIRD1	B23	RGMIIRD1 (ALT1)	0.000V - RGMII	gpio6_GPIO[27]	
RGMIIRD2	B24	RGMIIRD2 (ALT1)	0.000V - RGMII	gpio6_GPIO[28]	
RGMIIRD3	D23	RGMIIRD3 (ALT1)	0.000V - RGMII	gpio6_GPIO[29]	
RGMIIRD3_CTL	D22	RGMIIRD3_CTL (ALT1)	0.000V - RGMII	gpio6_GPIO[24]	
RGMIIRD4	B25	RGMIIRD4 (ALT1)	0.000V - RGMII	gpio6_GPIO[30]	
RGMIIRD5	C22	RGMIIRD5 (ALT1)	0.000V - RGMII	gpio6_GPIO[20]	
RGMIIRD6	F20	RGMIIRD6 (ALT1)	0.000V - RGMII	gpio6_GPIO[21]	
RGMIIRD7	E21	RGMIIRD7 (ALT1)	0.000V - RGMII	gpio6_GPIO[22]	
RGMIIRD8	A24	RGMIIRD8 (ALT1)	0.000V - RGMII	gpio6_GPIO[23]	
RGMIIRD9	C23	RGMIIRD9 (ALT1)	0.000V - RGMII	gpio6_GPIO[26]	

i.MX6DQ [156 of 197 muxed pins in use] 0 conflicts!



# Generate Configuration Code

- Several Code-Styles available in the Code Menu.
- Examples are shown in the User’s Guide.
- Click “Generate Code” to create the files for the current design.



Try it

uart2 (4 of 4)			
CTS			
RTS	J19	EIM_D29 (ALT4)	
RXD_MUX	E25	EIM_D27 (ALT4)	
TXD_MUX	E24	EIM_D26 (ALT4)	

Copy uart2 configuration code to clipboard.



# Develop Tools DDR Stress Test



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# DDR Stress Test Tool

- **What is DDR Stress Tester kit?**

It is downloadable test application architecture. A program running on PC (DDR\_Stress\_Tester.exe, which running on Command Prompt window) will download the test image to target board's IRAM with the help of UART/USB connection. The test image will do the DDR stress test and the result will be sent to PC through UART/USB and be printed on the Command Prompt window.

- **For mx6dq, mx6dl or mx6sl, UART is not supported.**
- **Support mx53, mx51, mx6dq, mx6dl and mx6sl.**

# DDR Stress Test Tool cont.

```

C:\WINDOWS\system32\cmd.exe

D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary>dir
Volume in drive D is Work
Volume Serial Number is 44DB-F232

Directory of D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary

03/11/2013  02:34 PM  <DIR>          .
03/11/2013  02:34 PM  <DIR>          ..
03/11/2013  02:21 PM  <DIR>          scripts
12/25/2012  11:40 AM             504,832 DDR_Stress_Tester.exe
09/19/2011  01:07 PM             72,928 ddr-stress-test-mx51.bin
09/19/2011  01:08 PM             81,104 ddr-stress-test-mx53.bin
08/29/2012  04:10 PM             69,704 ddr-stress-test-mx6dl.bin
08/29/2012  04:05 PM             86,004 ddr-stress-test-mx6dq.bin
08/29/2012  03:55 PM             67,764 ddr-stress-test-mx6sl.bin
12/25/2012  10:47 AM             9,414 MX6Q_SabreSD_DDR3_register_programming_aid_v1.6.inc
              7 File(s)          891,750 bytes
              3 Dir(s)    13,718,409,216 bytes free

D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary>DDR_Stress_Tester -h
Usage: DDR_Stress_Tester [options]
Options:
  -h,                Show this help
  -v,                Display the version
  -t <string>        Select target(mx51,mx53, mx6x)
  -df <path>         Input ddr initialization script file(*.inc)
  -com <num>         select the PC's UART to be used(1,2,3...), for mx51/mx53 only
  -usb               select the PC's USB to be used

For mx6x, UART is not supported and USB is the default option.

Usage example:
  DDR_Stress_Tester -t mx53 -df mx53_ddr_script_filename -com 4
  DDR_Stress_Tester -t mx53 -df mx53_ddr_script_filename -usb
  DDR_Stress_Tester -t mx6x -df mx6x_ddr_script_filename

D:\My Project\iMX6DQ\DDR Stress Test\DDR_Stress_Tester_U0.042\binary>

```

Test Log [Link](#)



# Develop Tools OBDS & PLATLIB



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# OBDS and PLATLIB

- **What is OBDS ?**

- The On Board Diagnostics Suite (OBDS) is a suite of tests designed to ensure the hardware connectivity between the SoC and on board peripherals to help ensure working and bug-free board systems.

- **What is PLATLIB ?**

- Example low-level driver code that enables all main features of a peripheral without the need for an operating system.
- Provides example usage of each driver which demonstrates the main features.
- Provides a solid and simple environment for quick board bring-up.
- Similar to OBDS except that more module functionality is supported in addition to providing a firmware guide.

# Setting up the Tool Chain

- **Obtained the GNU Toolchain for ARM processors**
  - Go to <http://compass.freescale.net/go/217844329>
  - Download the Linux version:  
arm-2008q3-66-arm-none-eabi-i686-pc-linux-gnu.tar.bz2
  - Or search: “Sourcery G++ Lite 2008q3-66”
  
- **Setting up the OBDS GCC Build Environment under Linux**
  - Under /opt directory  
tar xjvf -2008q3-66-arm-none-eabi-i686-pc-linux-gnu.tar.bz2
  - Add /opt/tools/bin and /opt/arm-2008q3/bin to your environment PATH variable.

# Build the OBDS Binary

- Build command: `./tools/build_obds -t mx6dq -b sabre_ai -v b -clean`

```

justin@ubuntu: ~/obds/mx6_obds_20120524
文件(F) 编辑(E) 查看(V) 搜索(S) 终端(T) 帮助(H)
justin@ubuntu:~/obds/mx6_obds_20120524$ ./tools/build_obds -h
Usage:
  build_obds [-t <target>] [-b <board>] [-v <rev>] [-c] [-l]

Generates makefiles for the i.MX OBDS project.

Options:
  -t, -target=<target>    Specify the target name. Optional, and the default is all.
  -b, -board=<brd>       Specify the board name. Optional, and the default is all.
  -v, -board_rev=<rev>   Specify the board revision. Optional, and the default is all.
  -c, -clean              Optional flag to force a clean build.
  -l, -list-builds       Optional flag to list target, board, board_rev combinations to be built.

Short options take the same arguments as their respective long options.
The '=' is optional for long options; arguments can be specified as -arg=value or
-arg value. Short options require a space between the option and value.

Generates makefiles for the specified combination of options. If -clean was specified,
'make clean' will be run. A regular build will be executed. Makefiles are generated only
for packages that are part of the selected board.

Valid target and board combinations:

target=mx6dq boards:
  sabre_ai      rev b
  evb           rev a (MX6QCPUDDR3)
  sabre_lite    rev a
  smart_device  rev b

target=mx6sdl boards:
  sabre_ai      rev b
  evb           rev a (MX6QCPUDDR3)
  sabre_lite    rev a
  
```

# Deploy the OBDS Binary

- `cd ./output/mx6dq/smart_device_rev_b/bin/`
- `dd if=mx6dq-smart_device-revb-obds.bin of=/dev/sdb skip=2 seek=2 && sync`

```

Tera Term - COM2 VT
File Edit Setup Control Window Help
Boot From: SD/eSD/SDXC: normal boot: speed SDR12: bus width 4-bit on USDHCC3
-----
This is an interactive test menu for MX60Q T01.2 Smart Device (SD) rev. C.

00. ALL TESTS
01. UART
02. SET MAC ADDRESS
03. DDR
04. BOARD ID
05. I2C DEVICE ID
06. GPIO LED
07. EEPROM
08. ANDROID BUTTONS
09. Touch Button Test
10. EHCI test modes
11. USBH2 ULP1
12. USBH1 Enum
13. USBOTG Enum
14. USBH1 HUB
15. SNVS - SRTC
16. MIB OS01050
17. IO expander MAX7310 ID
18. SMB BUS
19. PMIC PF0100
20. WIFI
21. SATA
22. WEIM NOR FLASH
23. SPI NOR FLASH
24. NAND
25. ETHERNET
26. RMII AR8031 G-Ethernet
27. RMII KS29021RN G-Ethernet
28. ESAI
29. I2S AUDIO
30. TOUCH SCREEN
31. MMC/SD
32. DISPLAY
33. Camera Test

Enter test number followed by the enter key, 'm' for menu, or 'q' to exit.
  
```

# Build the PLATLIB Binary

- Build command: `./tools/build_sdk -t mx6dq -b sabre_ai -v b -clean`

```

justin@ubuntu: ~/platlib/IMX6_Platform_SDK
文件(F) 编辑(E) 查看(V) 搜索(S) 终端(T) 帮助(H)
justin@ubuntu:~/platlib/iMX6_Platform_SDK$ ./tools/build_sdk -h
Usage:
  build_sdk [-t <target>] [-b <board>] [-v <rev>] [-r <test>] [-n] [-c] [-l]

Generates makefiles for the i.MX SDK project.

Options:
  -t, -target=<target>      Specify the target name. Optional, and the default is all.
  -b, -board=<brd>         Specify the board name. Optional, and the default is all.
  -v, -board_rev=<rev>, -rev=<rev>
                           Specify the board revision. Optional, and the default is all.
  -a, -app=<name>          Optional argument to select a single app to build. If not present,
                           then all apps will be built.
  -r, -test=<name>         Optional argument to select a single test for sdk_unit_test app,
                           or 'all' for all tests. Defaults to ALL.
  -c, -clean               Optional flag to force a clean build.
  -n, -no-build            Don't actually run make.
  -l, -list-builds        Optional flag to list target, board, board_rev combinations to be built.

Short options take the same arguments as their respective long options.
The '=' is optional for long options; arguments can be specified as -arg=value or
-arg value. Short options require a space between the option and value.

Generates makefiles for the specified combination of options. If -clean was specified,
'make clean' will be run. Then a regular build will be executed, unless the -no-build
argument is present. Makefiles are generated only for packages that are part of the
selected board.

Valid target and board combinations:

target=mx6dq boards:
  evb          rev a          (labeled MX6QCPUDDR3)
  sabre_ai     rev a, b, c
  
```

# Deploy the PLATLIB Binary

- `cd ./output/mx6dq/sdk_unit_test/sabre_ai_rev_b/`
- `dd if=sdk_unit_test_ALL.bin of=/dev/sdb skip=2 seek=2 && sync`

```

Tera Term - COM2 VT
File Edit Setup Control Window Help
Platform SDK (1.0) for iMX6DQ T01.2 Smart Device (SD) rev. B
Build: Dec 25 2012, 17:45:03
Copyright (c) 2012 Freescale Semiconductor, Inc. All rights reserved.
*****

----- Clock frequencies(HZ) -----
Cortex A9 core : 792,000,000
DDR memory : 528,000,000
UART1 for debug : 80,000,000
EPIT1 for system timer : 66,000,000
-----

SDK Unit Tests
-----
0 - epit test
0 - gpt test
0 - i2c test
0 - pmu test
0 - sdma test
0 - snvs rtc test
0 - snvs srtc test
0 - tempmon test
0 - uart test
0 - usdhc test
0 - gic test
0 - microseconds timer test
00 - watchdog test
0 - ocatp test
0 - hdmi test
00 - ipu test
00 - sata test
00 - audio test
00 - camera test
00 - usb test
00 - spi nor test
00 - pcie test
00 - enet test
0 - quit test system

Select test to run:
  
```

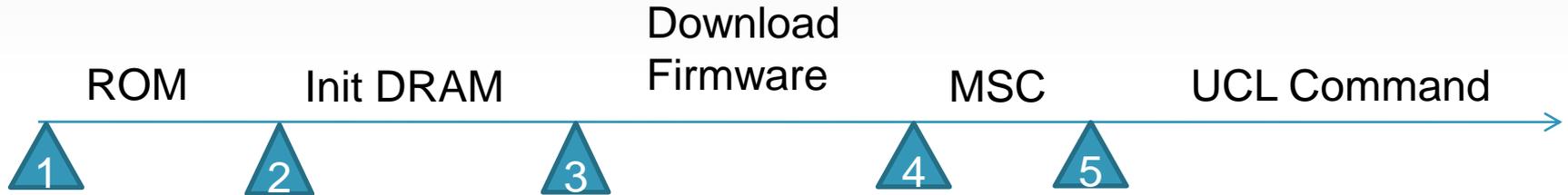


# Develop Tools MFG



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# Manufacturing (MFG) Tool V2



- How the tool works - Steps

1. After a board is powered up, it has nothing to run but ROM. ROM initializes USB and enumerates it as a dedicated device like HID device(MX23, MX28, MX50, MX6) or Bulk-IO device(MX3x, MX25, MX51, MX53).
2. Once a host detects the device, it will setup the connection with the device. Now the first task for host is to initialize RAM memory. It extract memory initialization code or data from an image (like u-boot) to do the task. It is also possible to use a memory initialization script to get initialization data.
3. After RAM is initialized, the host sends a kernel and mini RAM filesystem to RAM. The host then sends a command to ROM to jump into the kernel.
4. The kernel runs and enumerate USB as a MSC device. Now the device is ready for high speed data transfer.
5. The host runs commands in UCL script one by one.

# Manufacturing Tool Usage

- Configure Files

- UICfg.ini

- [UICfg]

- PortMgrDlg=1

- Cfg.ini

- [profiles]

- chip = MX6Q Linux Update

- [platform]

- board = SabreSD

- [LIST]

- name = MX6Q-Sabreauto-NAND

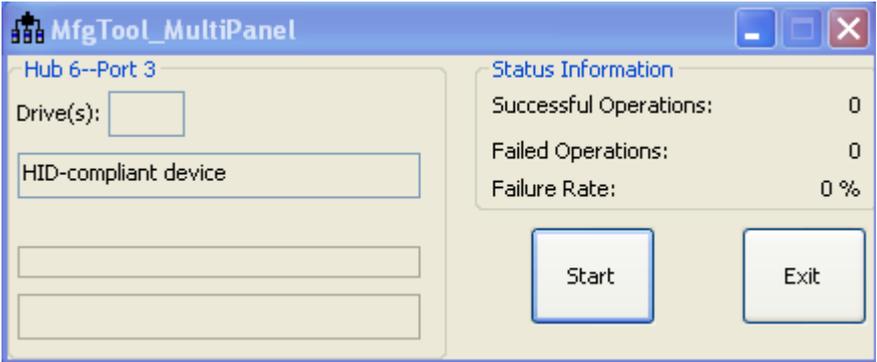
- Ucl2.xml

- Located: Profiles\MX6Q Linux Update\OS Firmware

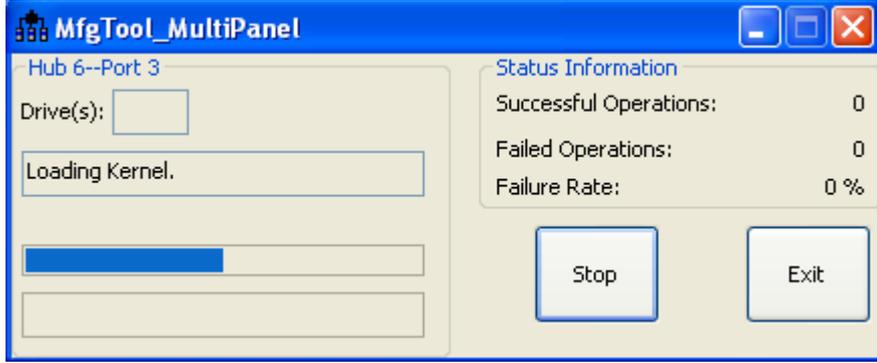
- Download script file , customer can change it.

# Manufacturing Tool Usage *Cont.*

- Power on board and enter serial download mode
- Connect Board to PC with USB cable
- Start the MfgTool

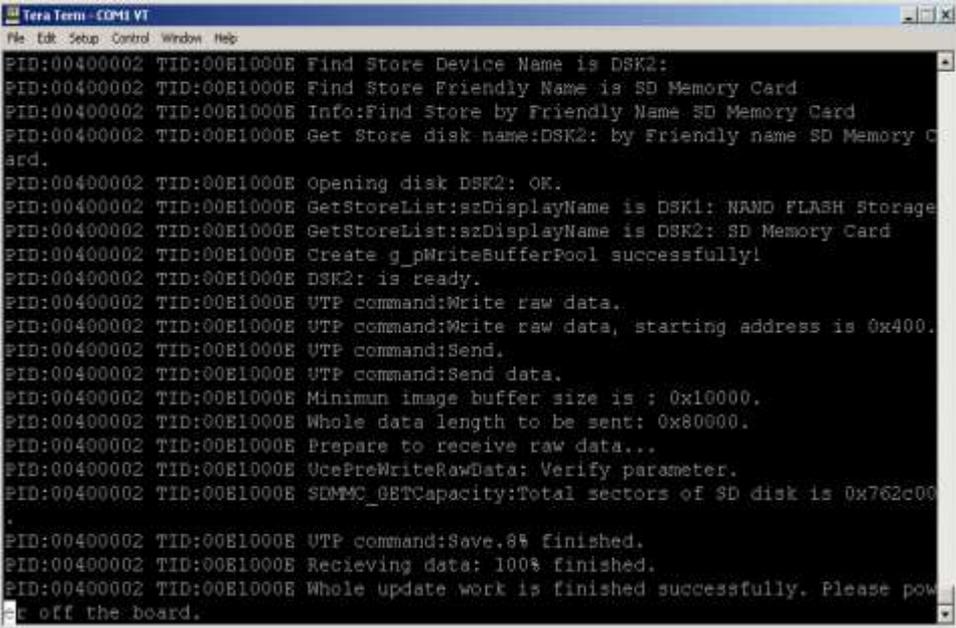


- Click Start button

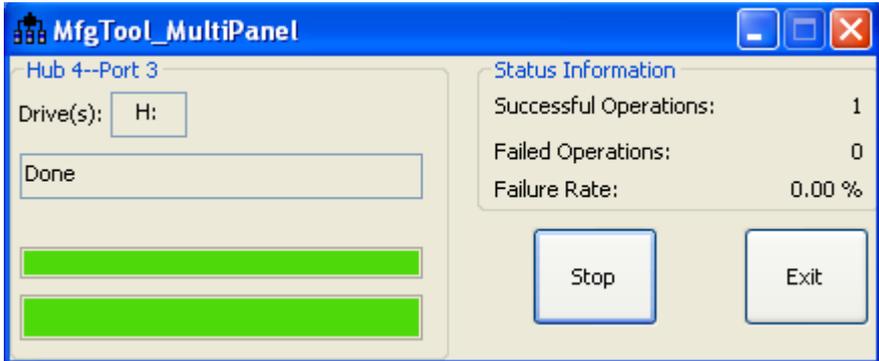


# Manufacturing Tool Usage Cont.

You can find information from the terminal



It is done. Click “Stop” to finish, and Click “Exit” to terminate the application



# Manufacturing Tool Usage *Cont.*

- How to Program a Fuse

MfgTool V2 supports writing the specified value into the fuse.

The OTP fuse can be written through the following commands:

```
<CMD state="Updater" type="push" body="$ ls /sys/fsl_otp ">Showing HW_OCOTP fuse bank</CMD>
```

```
<CMD state="Updater" type="push" body="$ echo 0x11223344 >
/sys/fsl_otp/HW_OCOTP_MAC0">write 0x11223344 to HW_OCOTP_MAC0 fuse bank</CMD>
```

```
<CMD state="Updater" type="push" body="$ cat /sys/fsl_otp/HW_OCOTP_MAC0">Read value from
HW_OCOTP_MAC0 fuse bank</CMD>
```

The fuse bank name (ex: HW\_OCOTP\_MAC0) should be changed according as needed.



# Freescale Support IMXCommunity



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[www.imxcommunity.org](http://www.imxcommunity.org)

A Freescale supported open web community of developers sharing common interest in transforming i.MX applications processors into practically anything imaginable.

## Community Facts at a Glance

- Over 3,800 members and over 200 Freescale engineers and marketers interacting with you
- Support and enablement for i.MX processors and software
- Forums, Groups and Blogs Posts
- News, Photos and Videos
- Training, Events and Promotions

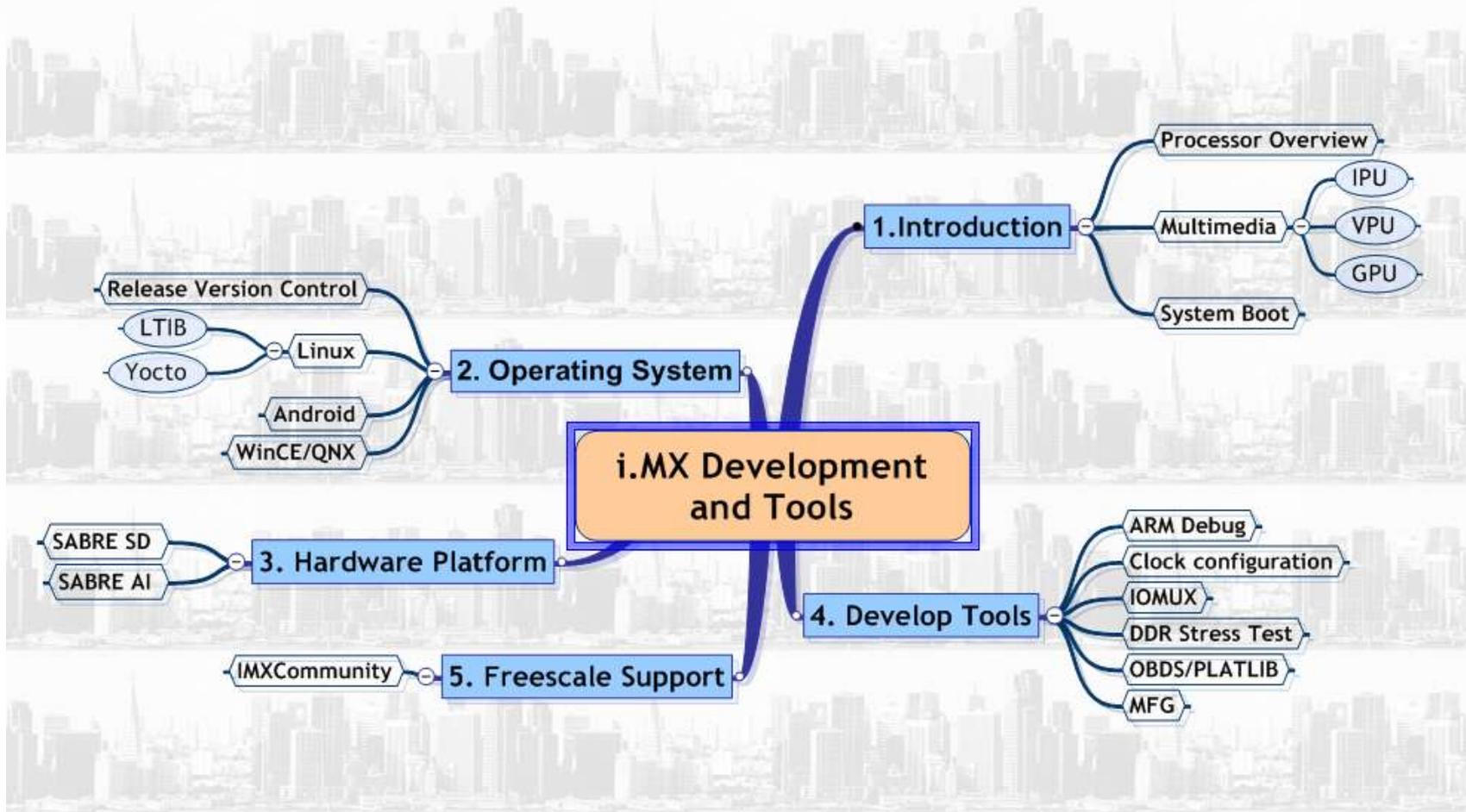


# Summary



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# MindMap





# Q&A



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