Freescale Semiconductor
Application Note

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Migrating from the MPC862 to the MPC866 PowerQUICC™ Processor

This application note lists some of the design considerations that a customer must make when migrating from the MPC862/857 CDR2 family to the MPC866/859 HiP6W family. The following topics are covered:

Contents

1 Overview

This application note describes the hardware and software design considerations when migrating from the MPC862/MPC857 family to the MPC866/MPC859 family. The MPC866/MPC859 family is the latest development of the MPC8xx family of products. The MPC862 and the MPC866 are Power Architecture™ derivatives of Freescale's MPC8xx PowerPC™ Quad Integrated Communications Controller (PowerQUICC™). The MPC866/MPC859 processors use the HIP6W (0.18µm) technology to achieve higher performance with system frequencies up to 133 MHz.

The MPC866/MPC859 keeps the same functionality as the MPC862/MPC857, including any micro-code implementation. Although the MPC866 is pin-compatible with the MPC862, a number of small but significant programming changes must be made to accommodate differences between the controllers.

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The MPC859P/859T/MPC859DSL is a low-cost derivative of the MPC866 that includes the same basic feature set with the exception that only one serial communication controller (SCC) is available to the user. Before selecting the MPC859/MPC859T/MPC859DSL as the host processor, carefully consider whether one SCC is capable of providing enough performance for the target application.

NOTE

This application note refers to the *MPC862 PowerQUICC™ Family User's Manual* and the *MPC866 PowerQUICC™ Family User's Manual*.

The MPC866/MPC859 PLL circuitry received a major design overhaul (that is, hardware and software must be modified when changing over from an MPC862/857-based design to support the high CPU frequency). Therefore, Section 10, "Clocks and Power Control," talks about the clocks and the DPLL operation.

2 System and External Bus Frequency Operation

The MPC866/859 family operates at a maximum system frequency of 133 MHz and an external bus frequency of 66 MHz. Table 1 shows the maximum operating frequency operation and external bus frequency for the MPC862/857 and MPC866/859.

Table 1. Maximum Operating Frequency in MHz

	MPC862/857T		MPC866/859		MPC859DSL	
	1:1 Mode	2:1 Mode	1:1 Mode	2:1 Mode	1:1 Mode	2:1 Mode
Maximum system frequency operation	66	80	66	133	66	66
Maximum external bus frequency operation	66	40	66	66	66	33

To achieve the best performance, minimize the capacitive loading for the MPC866/859 external bus as much as possible. Connect the SDRAM directly to the external bus while isolating and buffering slow access devices such as FLASH and DRAM on the external bus. Use devices such as data transceivers to help remove the extra capacitance on the bus.

NOTE

New system frequencies are supported in the MPC866. Be careful when reusing previous MPC862 drivers that use baud generator clocks (BRGCs). BRG clock dividers should be readjusted to generate the desired baud when operating at frequencies higher than 80 MHz.

3 New PLL Implementation

The MPC866/859 implements a new digital phase lock loop (DPLL) block that eliminates the need for an XFC capacitor. The XFC pin is a no connect (NC) on the MPC866/859. The XFC pin is not connected internally. Table 2 lists the related pins for the PLL and clock block.

Table 2. DPLL Considerations

Pin Name	MPC862/857	MPC866/859
XFC	XFC capacitor	N/C
EXTCLK	EXTCLK	EXTCLK
XTAL	XTAL	XTAL
EXTAL	EXTAL	EXTAL
CLKOUT	CLKOUT	CLKOUT

The following list includes major changes in the clock and DPLL implementation:

- Input clock can be a 10-MHz crystal at EXTAL/XTAL and 10 MHz and above only at EXTCLK.
- Power-on reset DPLL configuration default value has changed.
- The low-power and reset control register (PLPRCR) is used to control the system frequency. This register now has several different fields (MFN, MFD, MFI, and PDF) for the frequency factor calculation. This register is not backward compatible with the MPC862/857.

For further details on the clock and DPLL programming module, refer to Section 10.3, "Clock and Power Control Registers."

4 Power Voltage Structure

The MPC866 has two voltage levels for the power supply connection. The internal logic and the DPLL block are fed by 1.8 V (V_{DDL} and V_{DDSYNC}, respectively), while the I/O buffers are supplied by 3.3 V (V_{DDH}).

The keep alive power (KAPWR) power pin is not available now on the MPC866/859 and is replaced as an additional V_{DDL} power pin. Table 3 highlights the power supply voltage levels for each of the power pins.

Table 3. Power Supply Connection

Pin Name	MPC862/857	MPC866/859
VDDH	3.3	3.3
VDDL	3.3	1.8
VDDSYN	3.3	1.8
KAPWR	KAPWR	1.8
VSS	Ground	Ground
VSSSYN1	Ground	Ground
VSSSYN2	Ground	Ground

The organization of the power rails is shown in Figure 1. Note that the clock control and DPLL blocks are now powered by V_{DDL} on the MPC866/859, instead of V_{DDH} on the MPC862/857.

NOTE

The low-power (sleep, doze, and power-down) modes are not supported.

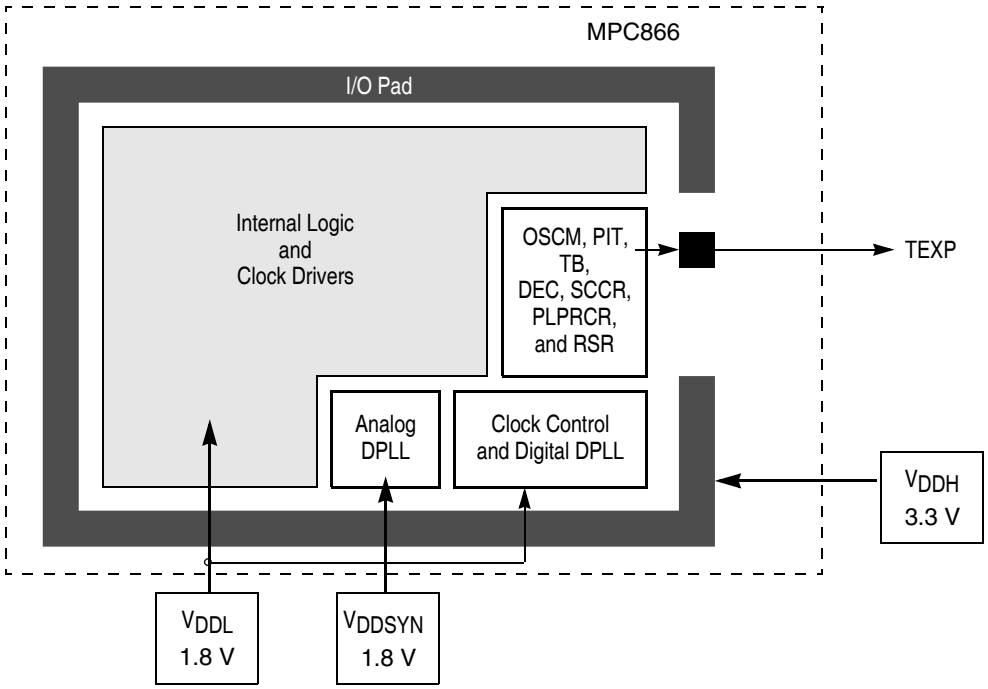


Figure 1. Organization of the Power Rails

5 Five-Volt Tolerant Pins

With the exception of the EXTAL and EXTCLK pins, the MPC862/857 pins are all 5-V tolerant. The MPC866/859 differs from the MPC862/857 with regard to pins that are 5-V tolerant. Table 4 lists all the pins on the MPC862/857 and MPC866/859 and shows whether the pins are 5-V tolerant.

Table 4. List of 5-V Tolerant Pins on MPC862/857 and MPC866/859

Pin Name	MPC862/857 5-V Tolerant	MPC866/859 5-V Tolerant
XTAL	No	No
EXTAL	No	No
EXTCLK	No	No
PB[14:31]	Yes	Yes
PA[0:15]	Yes	Yes
PC[4:15]	Yes	Yes
PD[3:15]	Yes	Yes
TDI	Yes	Yes
TDO	Yes	Yes
TCK	Yes	Yes
$\overline{\text{TRST}}$	Yes	Yes

Table 4. List of 5-V Tolerant Pins on MPC862/857 and MPC866/859 (continued)

Pin Name	MPC862/857 5-V Tolerant	MPC866/859 5-V Tolerant
TMS	Yes	Yes
MII_MDIO	Yes	Yes
MII_TXEN	Yes	Yes
Rest of the 862/866 pins	Yes	No

6 Pinout Description

Figure 2 shows the MPC866/859 pinout. Table 5 shows the changes made from MPC862/857 to MPC866/859. The following list notes the changes:

- All V_{DDL} pins and V_{DDSYNC} (shown in blue in Figure 2) were changed to 1.8-V pins on the MPC866/859.
- All V_{DDH} pins (shown in green in Figure 2) are still 3.3-V pins on the MPC866/859.
- Pin T2 (shown and labeled in red in Figure 2) was changed from XFC on the MPC862/857 to NC on the MPC866/859 (see Table 5).
- Pin R1 (labeled in magenta in Figure 2) was changed from KAPWR on the MPC862/857 to V_{DDL} on the MPC866/859 (see Table 5).

Table 5. Pin Changes from MPC862/857 Moving to MPC866/859

Pin Name	Pin No.	MPC862/857	MPC866/859
XFC	T2	XFC	NC
KAPWR	R1	KAPWR	V_{DDL}

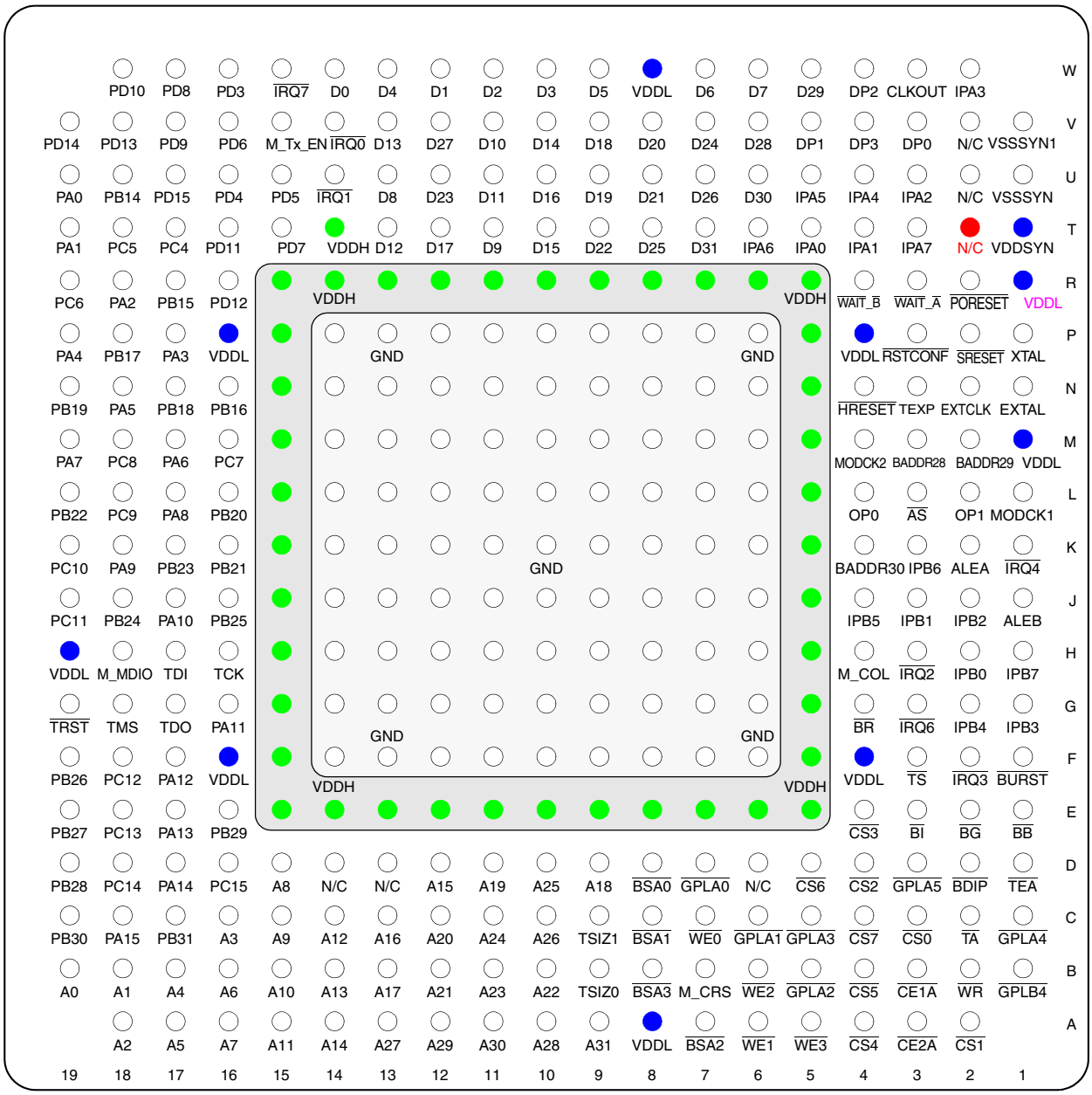


Figure 2. MPC866 Pinout

7 Microcode Status

Table 6 lists all the available protocols that can be implemented on the CPM ROM/RAM microcodes for the MPC862/857 and MPC866/859 families. The table also shows the availability of the patch as a RAM patch, or whether it is included in the ROM.

Table 6. MPC862/857 and MPC866/859 ROM-Based Microcodes

		MPC862/857	MPC866/859
	Mask (MOO No.)	2K26A	3L90H
	Silicon revision	B	0.3
	Part No. IMMR[16:23]	0x07	0x08
	MSKNUM IMMR[24:31]	0x00	0x00
	ROM microcode revision no.	0x0003	0x0001
	Max microcode DPRAM space	8k	8k
SCC	Appletalk/Localtalk	Yes	
	Asynchronous HDLA/IrdA	Yes	
	AAL2	Yes	
	ATM AAL0 & AAL5	Yes	
	BISYNC	Yes	
	Dynamic CLP and CNG marking	Yes	
	Enhanced UBR	TBD	
	Ethernet / IEEE 802.3	Yes	
	HDLC	Yes	
	Multi sub-channel [MSC]	TBD	
	Port-to-port switching	Yes	
	SS7	TBD	
	Transparent	Yes	
	UART	Yes	
	RTP accelerator	TBD	
SMC	GCI (ISDN)	Yes	
	Transparent	Yes	
	UART	Yes	

8 Register Lock Mechanism

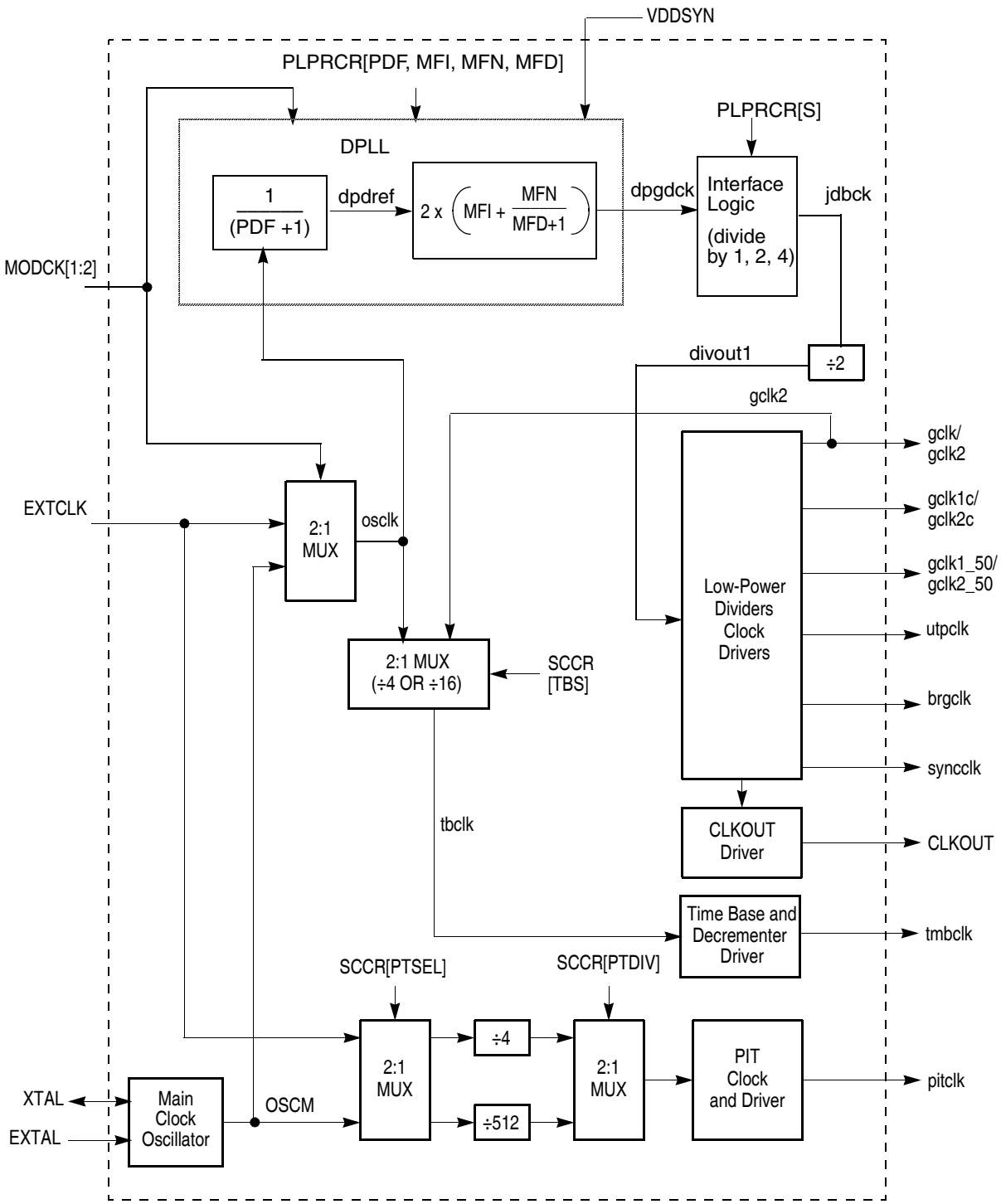
Except for the omission of the power-down feature, the operation of the register lock mechanism is unchanged.

9 Development Boards

Freescale has developed an ADS board that accommodates MPC8xx processors, including the MPC866/859 (see the Freescale website listed on the backpage of this document for more information).

10 Clocks and Power Control

The MPC866 clock system provides many different clocking options for all on-chip and external devices. For its clock sources, the MPC866 contains PLL and crystal oscillator support circuitry. The PLL circuitry can be used to provide a high-frequency system clock from a low-frequency external source. Furthermore, to enable flexible power control, the MPC866 provides frequency divider options. Figure 3 illustrates internal clock source and distribution that includes the DPLL and interface, clock dividers, drivers, and crystal oscillator.



Note that only CLKOUT is an actual external output; all other outputs are internal signals. The real-time clock is not supported.

Figure 3. Clock Source and Distribution

10.1 Clock Module

The clock module consists of two external reference sources and a PPL loop, arranged as shown in Figure 4.

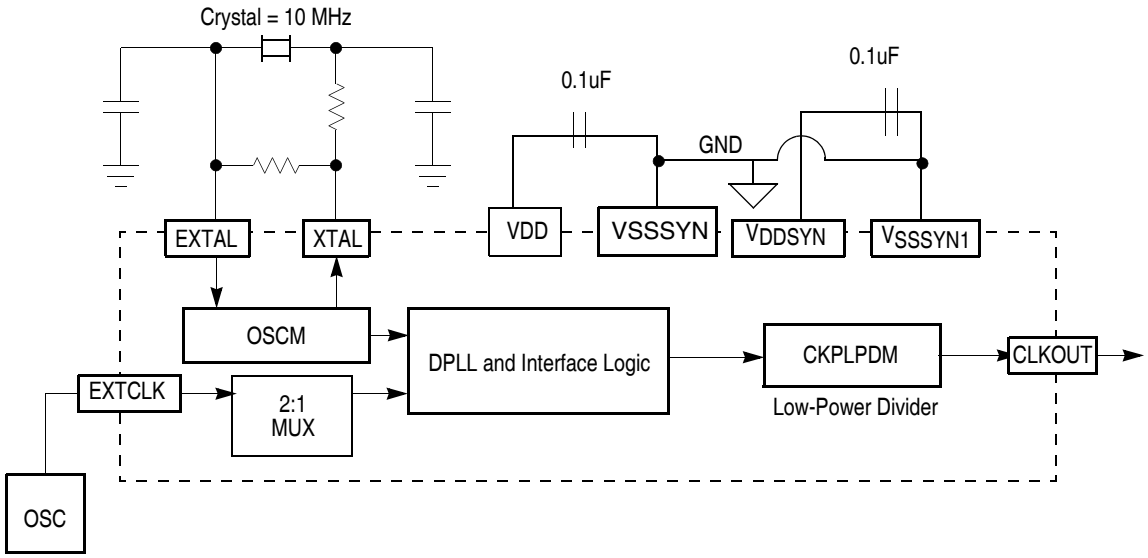


Figure 4. Clock Module Components

10.2 External Reference Clocks

The MPC866 has two input clock sources, which are either provided at the EXTCLK pin or at the EXTAL and XTAL pins. These two clock sources can select to drive three internal clock signals, referred to as OSCLK, PITCLK, and TMBCLK. OSCLK provides the input clock to the PLL. PITCLK and TMBCLK provide dedicated clocks for special system timer circuitry, which includes the periodic interrupt timer (PIT), timebase (TB), and decrementer (DEC) in the SIU. These separate clock sources for the PIT, TB, and DEC enable these modules to continue to count at a fixed, user-defined rate regardless of system frequency.

The clock sources for OSCLK, PITCLK, and TMBCLK are selected at reset. The sources for PITCLK and TMBCLK can also be selected in the software by manipulating the SCCR. See Section 10.3.1, “System Clock and Reset Control Register (SCCR). For more information, see Section 10.2.2, “DPLL Reset Configuration,” and the *MPC866 PowerQUICC™ Family User’s Manual*, Section 14.3.2, “PIT Clock (PITCLK)” and Section 14.3.3, “Time Base and Decrementer Clock (TMBCLK).”

NOTE

It is possible to use both clock sources in a system, so that each provides reference for different functions. If neither reference source is used, inputs should be grounded. Do not select the crystal oscillator circuit as OSCLK while also driving a high-frequency clock source on EXTCLK; noise from the EXTCLK clock source couples into the crystal oscillator circuit and might not allow the DPLL to lock. The converse, however, is allowable; EXTCLK can be selected as OSCLK while the crystal oscillator circuit supplies a separate frequency reference.

A typical configuration uses a canned oscillator with the EXTCLK input selected as OSCLK and a 10-MHz crystal at EXTAL and XTAL to provide PITCLK.

Four different PLL modes that the MODCK pins define at reset determine the initial value of the PLPRCR register. Three of these modes require a 10-MHz input frequency, while the fourth mode can accept from 45 to 66 MHz. After reset, the PLPRCR can be programmed to achieve a different general system clock if the following requirements are met:

- OSCM is 10 MHz only (MODCK = 00 or 01)
- EXTCLK is 10 MHz (MODCK = 11)
- EXTCLK is 45 to 66 MHz (MODCK = 10)

The input frequency requirements at reset are shown in Table 7.

Table 7. Input Frequency Requirements

MODCK[1-2]	Frequency In	PDF	MFI, MFN, MFD for DPGDCK
00, 01	OSCM = 10 MHz	0	160 MHz < OSCLK * 2 * (MFI + (MFN / (MFD+1))) < 320 MHz
11	EXTCLK = 10 MHz	0	160 MHz < OSCLK * 2 * (MFI + (MFN / (MFD+1))) < 320 MHz
10	45 MHz ≤ EXTCLK ≤ 66 MHz	10 MHz ≤ EXTCLK / (PDF + 1) ≤ 32 MHz	160 MHz < OSCLK * 2 * (MFI + (MFN / (MFD +1))) / (PDF+1) < 320 MHz

10.2.1 DPLL and Interface

The programmable DPLL in the MPC866 generates the overall system operating frequency in integer and non-multiples of the input clock frequency. CLKOUT synchronization is not guaranteed for non-integer multiples of OSCLK. If CLKOUT is an integer multiple of OSCLK/EXTCLK, the rising edge of EXTCLK is aligned (locked/synchronized) with the rising edge of CLKOUT. For a non-integer multiple of EXTCLK, this synchronization is lost, and the rising edges of EXTCLK and CLKOUT have a continuously varying phase skew.

Digital implementation of frequency control and loop filtering functions in the design of the DPLL allows the following new features:

- Eliminating an on-board loop filter capacitor, minimization of internal capacitor value
- Selection of frequency and phase/frequency operation modes
- Improved noise immunity, eliminating additional supply and ground pins

- High frequency resolution with a reduced lock time
- Reduced sensitivity to parameter variations caused by temperature and process

The main purpose of the DPLL is to generate a stable reference frequency by multiplying the frequency and eliminating the clock skew. The DPLL allows the processor to operate at a high internal clock frequency using a low-frequency clock input, providing two advantages. First, lower frequency clock input reduces the overall electromagnetic interference the system generates. Second, the programmability of the oscillator enables the system to operate at a variety of frequencies with only a single external clock source.

The DPLL reference clock (OSCLK) can be generated from either of the external clock sources described in Section 10.2, "External Reference Clocks."

Inside the DPLL, the OSCLK is divided by the predivision factor (PDF+1) to generate the DPDREF clock. The frequency range of the DPDREF is 10 to 32 MHz. This DPDREF clock is used inside the DPLL for generating the output clock of the DPLL, that is, DPGDCK (see Figure 3). The frequency range of DPGDCK is 160 to 320 MHz. These frequency ranges must be maintained by both the reset configuration settings of the DPLL and interface and the final operating frequency of the DPLL and interface.

The interface logic works in three modes, depending on divider selection input PLPRCR[S]. The formula for the output frequency of the DPLL, and interface logic for each mode is given according to the following formula:

$$\text{jdbck} = 2 * \left(\frac{\text{MFI} + (\text{MFN}/(\text{MFD}+1))}{\text{PDF} + 1} \right) * \text{OSCLK} / 2^{S}$$

for S = 0, 1, or 2

NOTE

For synchronization between EXTCLK to CLKOUT, the total value by which the EXTCLK is multiplied must be an integer.

The total MF factor [MFI + (MFN/(MFD+1))] is an integer as a prerequisite.

Table 8 shows the DPLL parameters for some typical system frequencies during normal operation. The frequency after power on reset is shown in Table 9. The multiplication factors (MF) shown are for the integer part (MFI), numerator part (MFN), denominator part minus 1(MFD), and predivision factor minus 1 (PDF) with their ranges listed in Table 8. The total MF value, MFI+(MFN/(MFD+1)), must be between 5 and 15.

Table 8. Typical System Frequency Generation

Input Frequency in MHz (f_{ref})	PDF	MFI	MFN [1]	MFD	dpgdck	PLPRCRS [10:11]	JDBCK	General System Frequency [GCLK2] [2] (MHz)
10	0	8	0	0	160	1	80	40
10	0	9	6	9	192	1	96	48
10	0	10	4	9	208	1	104	52

Table 8. Typical System Frequency Generation (continued)

Input Frequency in MHz (f_{ref})	PDF	MFI	MFN [1]	MFD	dpgdck	PLPRCRS [10:11]	JDBCK	General System Frequency [GCLK2] [2] (MHz)
10	0	13	2	9	264	1	132	66
10	0	15	0	0	300	1	150	75
10	0	10	0	0	200	0	200	100
10	0	13	3	9	266	0	266	133
45	3	8	0	0	180	1	90	45
45	2	8	1	2	250	0	250	125
50	2	9	0	0	300	1	150	75
50	1	5	2	6	264	0	264	132
66	2	6	0	1	264	1	132	66
66	2	6	0	1	264	0	264	132

1 For MFN = 0, EXTCLK will be synchronized to CLKOUT.

2 Assuming DFNH = 0 and CSR = 0.

The OSCLK can be supplied by either a crystal or an external clock oscillator. Crystals are typically much cheaper than clock oscillators; however, a clock oscillator has significant design advantages over a crystal circuit in that clock oscillators are easier to work with, resulting in faster design, debugging, and production.

10.2.2 DPLL Reset Configuration

While $\overline{\text{PORESET}}$ is asserted, the reset configuration of the DPLL is sampled on the MODCK[1-2] pins. The DPLL immediately begins to use the multiplication factor and pre-division factor values and external clock source for OSCLK determined by the sampled MODCK[1-2] pin and attempts to achieve lock; therefore, the MODCK[1-2] signals should be maintained steadily throughout $\overline{\text{PORESET}}$ assertion. The mode selection field and various factors are set as Table 9 shows. After $\overline{\text{PORESET}}$ is negated, the MODCK[1-2] values are internally latched, and the signals applied to MODCK[1-2] can be changed.

Table 9. Power-On Reset DPLL Configuration

MODCK[1-2]	Default at Power-On Reset		OSCLK (DPLL and Interface Input)	General System Frequency (GCLK2)
	MFI[12-15]	PDF[27-30]		
00	8	0000	OSCM	40 MHz (for OSCLK freq = 10 MHz)
01	15	0000	OSCM	75MHz (for OSCLK freq = 10 MHz)
10 [1]	6	0010	EXTCLK	1:1 mode (allowable frequencies on EXTCLK are 45 to 66 MHz)

Table 9. Power-On Reset DPLL Configuration (continued)

MODCK[1-2]	Default at Power-On Reset		OSCLK (DPLL and Interface Input)	General System Frequency (GCLK2)
11	15	0000	EXTCLK	75 MHz (for EXTCLK freq = 10 MHz)
Note: sS = 1, MFN = 0, MFD = 1 for all of the reset configurations.The general system clock[GCLK2] is jdbck divided by 2. divout1 is jdbck divided by 2.				

1 For Revision 0.x of the MPC866, MFI = 8 and PDF = 0011 binary.

NOTE

Under no condition should the voltage on MODCK1 and MODCK2 exceed the power supply voltage V_{DDH} applied to the part.

At power-on reset, before the PLL achieves lock, no internal or external clocks are generated by the MPC866, which may cause higher than normal static current during the short period of stabilization.

10.3 Clock and Power Control Registers

The following sections describe the clock and power control registers.

10.3.1 System Clock and Reset Control Register (SCCR)

The DPLL has a 32-bit control register, the system clock and reset control register (SCCR), shown in Figure 5, which is memory-mapped into the MPC866 SIU's register map.

	0	1 2	3 5	6	7	8	9	10	11 12	13 14	15
Field	—	COM	—	TBS	PTDIV	PTSEL	CRQEN	–	—	EBDF	—
HRESET	—	#	0	#	#	#	0	0	0	†	0
POR	0	0	0	0	*	*	0	0	0	†	0
R/W	R/W										
Addr	(IMMR&0XFFFF0000) + 280										

	16	17 18	19 20	21 23	24 26	27 29	30 31
Field	—	DFSYNC	DFBRG	DFNL	DFNH	DFUTP	DFAUTP
HRESET	0						
POR	0						
R/W	R/W						
Addr	(IMMR&0XFFFF0000) + 282						

Note: HRESET is hard reset and POR is power-on reset.

The field is undefined
—The field is unaffected.
* PTDIV depends on the combination of MODCK1 and MODCK2. PTSEL depends on MODCK1. See Table 10 for more information.
† This field is set according to the default of the hard reset configuration word.

Figure 5. System Clock and Reset Control Register (SCCR)

This register is affected by HRESET but is not affected by SRESET. Table 10 describes the SCCR fields.

Table 10. SCCR Field Descriptions

Bits	Name	Description
0	—	Reserved, should be cleared
1–2	COM	Clock output module. This field controls the output buffer of the CLKOUT pin. When both bits are set, the CLKOUT pin is held in the high state. These bits can be dynamically changed without generating spikes on the CLKOUT pin. If the CLKOUT pin is not connected to external circuits, clock output should be disabled to minimize noise and power dissipation. The COM field is cleared by hard reset. 00 Clock output enabled full-strength buffer 01 Reserved 10 Reserved 11 Clock output disabled
3–5	—	Reserved, should be cleared
6	TBS	Timebase source. Determines the clock source that drives the timebase and decrementer. 0 Timebase frequency source is the OSCLK divided by 4 or 16 . 1 Timebase frequency source is GCLK2 divided by 16.
7	PTDIV	Periodic interrupt timer clock divide. Determines if the clock, the crystal oscillator, or main clock oscillator to the periodic interrupt timer is divided by 4 or 512. At power-on reset this bit is cleared if the MODCK1 and MODCK2 signals are low. 0 The clock is divided by 4. 1 The clock is divided by 512.

Table 10. SCCR Field Descriptions (continued)

Bits	Name	Description
8	PTSEL	Periodic interrupt timer select. Selects the crystal oscillator or main clock oscillator as the input source to PITCLK. At power-on reset, it reflects the value of MODCK1. 0 OSCM (crystal oscillator) is selected. 1 EXTCLK is selected.
9	CRQEN	CPM request enable. Cleared by power-on or hard reset. In low-power modes, specifies if the general system clock returns to high frequency while the CP is active. 0 System remains in low frequency even if the communication processor module is active. 1 System switches to high frequency when the communication processor module is active.
10	–	Reserved, should be cleared
11–12	—	Reserved, should be cleared
13–14	EBDF	External bus division factor. This field defines the frequency division factor between GCLKx and GCLKx_50. CLKOUT is similar to GCLK2_50. The GCLKx_50 is used by the bus interface and memory controller to interface with an external system. This field is initialized during hard reset using the hard reset configuration word in the *MPC866 PowerQUICC™ Family User's Manual,* Section 11.3.1.1, "Hard Reset Configuration Word." 00 CLKOUT is GCLK2 divided by 1. 01 CLKOUT is GCLK2 divided by 2. 10 Reserved 11 Reserved
15–16	—	Reserved, should be cleared
17–18	DFSYNC	Division factor for the SYNCCLK. This field sets the divout1, where divout1 is equivalent to JDBCK divide by 2, frequency division factor for the SYNCCLK signal. Changing the value of this field does not result in a loss-of-lock condition. This field is cleared by a power-on or hard reset. 00 Divide by 1 (normal operation). 01 Divide by 4. 10 Divide by 16. 11 Divide by 64.
19–20	DFBRG	Division factor of the BRGCLK. This field sets the divout1, where divout1 is equivalent to JDBCK divide by 2, frequency division factor for the BRGCLK signal. Changing the value of this field does not result in a loss-of-lock condition. This field is cleared by a power-on or hard reset. 00 Divide by 1 (normal operation). 01 Divide by 4. 10 Divide by 16. 11 Divide by 64.
21–23	DFNL	Division factor low frequency. Sets the divout1, where divout1 is equivalent to JDBCK divided by 2, frequency division factor for general system clocks to be used in low-power mode. In low-power mode, the MPC866 automatically switches to the DFNL frequency. To select the DFNL frequency, load this field with the divide value and set the CSRC bit. A loss-of-lock condition will not occur when changing the value of this field. This field is cleared by a power-on or hard reset. 000 Divide by 2. 001 Divide by 4. 010 Divide by 8. 011 Divide by 16. 100 Divide by 32. 101 Divide by 64. 110 Reserved 111 Divide by 256.

Table 10. SCCR Field Descriptions (continued)

Bits	Name	Description
24–26	DFNH	Division factor high frequency. Sets the divout1, where divout1 is equivalent to JDBCK divided by 2, frequency division factor for general system clocks to be used in normal mode. In normal mode, the MPC866 automatically switches to the DFNH frequency. To select the DFNH frequency, load this field with the divide value and clear CSRC. A loss-of-lock condition does not occur when this field is changed. This field is cleared by a power-on or hard reset. 000 Divide by 1. 001 Divide by 2. 010 Divide by 4. 011 Divide by 8. 100 Divide by 16. 101 Divide by 32. 110 Divide by 64. 111 Reserved
27–29	DFUTP	UTOPIA clock dividers; see the *MPC866 PowerQUICC™ Family User's Manual*, Section 41.2, "UTOPIA Mode Registers."
30–31	DFAUTP	

10.3.2 PLL and Reset Control Register (PLPRCR)

The 32-bit system PLL and reset control register (PLPRCR), shown in Figure 6, controls the system frequency and low-power mode operation.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	MFN					MFD					S		MFI			
HRESET	—					—					—	—	—			
POR	0000					00001					0	1	*			
R/W	R/W															
Addr	(IMMR&0xFFFF0000) + 284															

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	—	TEXPS	—	–	—	CSRC	–		CSR	—	FIOPD	PDF				DBRMO
HRESET	—	1	0	0	0	0	0		—	—	—	0000				0
POR	0	1	0	0	0	0	0		0	0	0	*				0
R/W	R/W															
Addr	(IMMR&0xFFFF0000) + 286															

Notes: HRESET is hard reset and POR is power-on reset. * POR depends on the combination of MODCK1 and MODCK2. See Table 11 for more information.

Figure 6. PLL and Reset Control Register (PLPRCR)

HRESET and SRESET affect this register. Table 11 describes the PLPRCR fields.

Table 11. PLPRCR Field Descriptions

Bits	Name	Description
0–4	MFN	Numerator of the fractional part of the multiplication factor in the formula for the output frequency of the DPLL and Interface. The range of values for the MFN is 0-31. The numerator of the fractional part of the multiplication factor (MFN) must be less than the denominator of the fractional part of the multiplication factor (MFD+1). [1] If the numerator is larger than the denominator, the output clock frequency differs from the desired frequency. If the numerator is 0, the circuit for fractional division is disabled to save power. Refer to Section 10.2.1, “DPLL and Interface”
5–9	MFD	Denominator minus 1 of the fractional part of the multiplication factor in the formula for the output frequency of the DPLL and interface.The range of values for the MFD is 1-31. The denominator of the fractional part of the multiplication factor(MFD+1) must be greater than the numerator of the fractional part of the multiplication factor MFN. [1] If the numerator is larger than the denominator, the output clock frequency differs from the desired frequency. If the numerator is 0, the circuit for fractional division is disabled to save power. Refer to Section 10.2.1, “DPLL and Interface.”
10–11	S	Selection bits for the divider after the double clock (fdck) 00 Divide by 1. 01 Divide by 2. 10 Divide by 4. 11 = Reserved Refer to Section 10.2.1, “DPLL and Interface”
12–15	MFI	Integer part of the multiplication factor in the formula for the output frequency of the DPLL and interface. The range of values for the MFI is 5-15. [1] If the MFI is less than 5, the DPLL uses 5. Refer to Section 10.2.1, “DPLL and Interface.”
16	—	Reserved
17	TEXPS	Timer expired status. Internal status bit set when the periodic timer expires, the timebase clock alarm sets, the decrementer interrupt occurs, or the system resets. This bit is cleared by writing a 1; writing 0 has no effect. 0 TEXP is negated. 1 TEXP is asserted.
18	—	Reserved, should be cleared
19	—	Reserved, should be cleared
20	—	Reserved, should be cleared
21	CSRC	Clock source. Specifies whether DFNH or DFNL generates the general system clock. Cleared by hard reset. 0 The general system clock is generated by the DFNH field. 1 The general system clock is generated by the DFNL field.
22–23	–	Reserved, should be cleared
24	CSR	Checkstop reset enable. Enables an automatic reset when the processor enters checkstop mode. If the processor enters debug mode at reset, then reset is not generated automatically; refer to Table 12. See the *MPC866 PowerQUICC™ Family User’s Manual*, Section 45.5.2.2, “Debug Enable Register (DER).”
25	—	Reserved, should be cleared

Table 11. PLPRCR Field Descriptions (continued)

Bits	Name	Description
27-30	PDF	Predivision factor minus 1 in the formula for the output frequency of the DPLL and Interface. The range of values for the PDF is 0 to 15. Refer to Section 10.2.1, "DPLL and Interface."
31	DBRMO	DPLL BRM Order bit 0 First Order (should be used when fractional part, MFN/MFD, in undivisible form is greater than 1/10) 1 Second Order (should be used when fractional part, MFN/MFD, in undivisible form is less than 1/10) This bit is ignored if the MFN is zero.

[1] The total multiplication factor, including both the integer and fractional parts, must be between 5 to 15.

Table 12 describes PLPRCR[CSR] and DER[CHSTPE] bit combinations.

Table 12. PLPRCR[CSR] and DER[CHSTPE] Bit Combinations

PLPRCR[CSR]	DER[CHSTPE]	Checkstop Mode	Result
0	0	No	—
0	0	Yes	—
0	1	No	—
0	1	Yes	Enter debug mode
1	0	No	—
1	0	Yes	Automatic reset
1	1	No	—
1	1	Yes	Enter debug mode

11 Programming Considerations

To take advantage of the new features on the 866 device, consider several significant programming considerations:

- SCC Parameter RAM. Page 4 of this memory area contains all of the necessary connection tables, buffer descriptors and data buffers required for 866 operation. This section of memory **MUST** be cleared during the initialization sequence before any 866 operation; otherwise the 866 could operate unpredictably.
- ALL ESAR bits must be cleared through the ESAR register set to reduce the complexity of the internal microcode. Clear all the ESAR bits in the SRSTATE, STSTATE, APCST registers. Similarly, if 866 ESAR functionality is required, set these bits in all of these registers.
- The 866 ESAR device allows programming or modification of any memory location on the fly without conflicting with the current CPM process. Only the WRITE_TO_MEMORY command can be used to do this modification. Attempting to modify any memory location without using this

command causes system CPM failure. (Adding or removing internal channels and modifying the APC period can also be changed on-the-fly in both 866 SAR and 866 ESAR modes.)

- Avoid writing non-zero values to the 32-bit location IMMR+0x3CB8 on the 866, even for non-ATM applications, unless Freescale specifically requires that writing. The 866 reserves this location for internal CPM usage.

12 Document Revision History

Table 13 shows the history of revisions and changes to this application note.

Table 13. Revision History

Revision Number	Date	Changes
1	11/05/2006	• Document template update.
0.2	09/29/2003	• Minimum Extclk frequency is now 45 MHz • In Table 8, changed the two rows that say 40 MHz to 45 MHz and updated the parameters • Nontechnical changes
0.1	08/22/2003	• Updates incorporated in document • Nontechnical reformatting changes
0.0	07/25/2003	Initial release

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