MARCH 1977

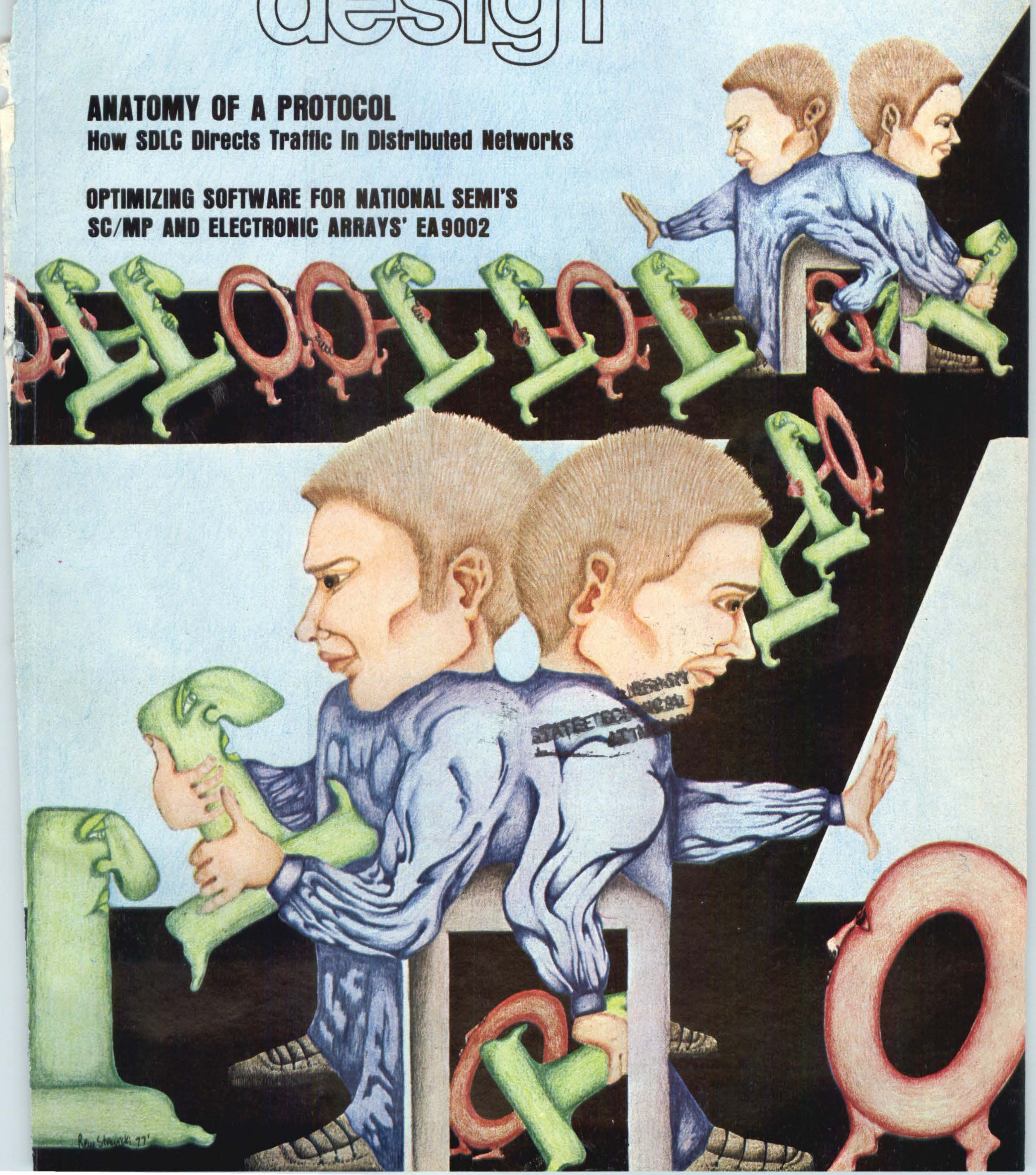
digital design

the magazine of digital systems

ANATOMY OF A PROTOCOL

How SDLC Directs Traffic In Distributed Networks

OPTIMIZING SOFTWARE FOR NATIONAL SEMI'S SC/MP AND ELECTRONIC ARRAYS' EA9002



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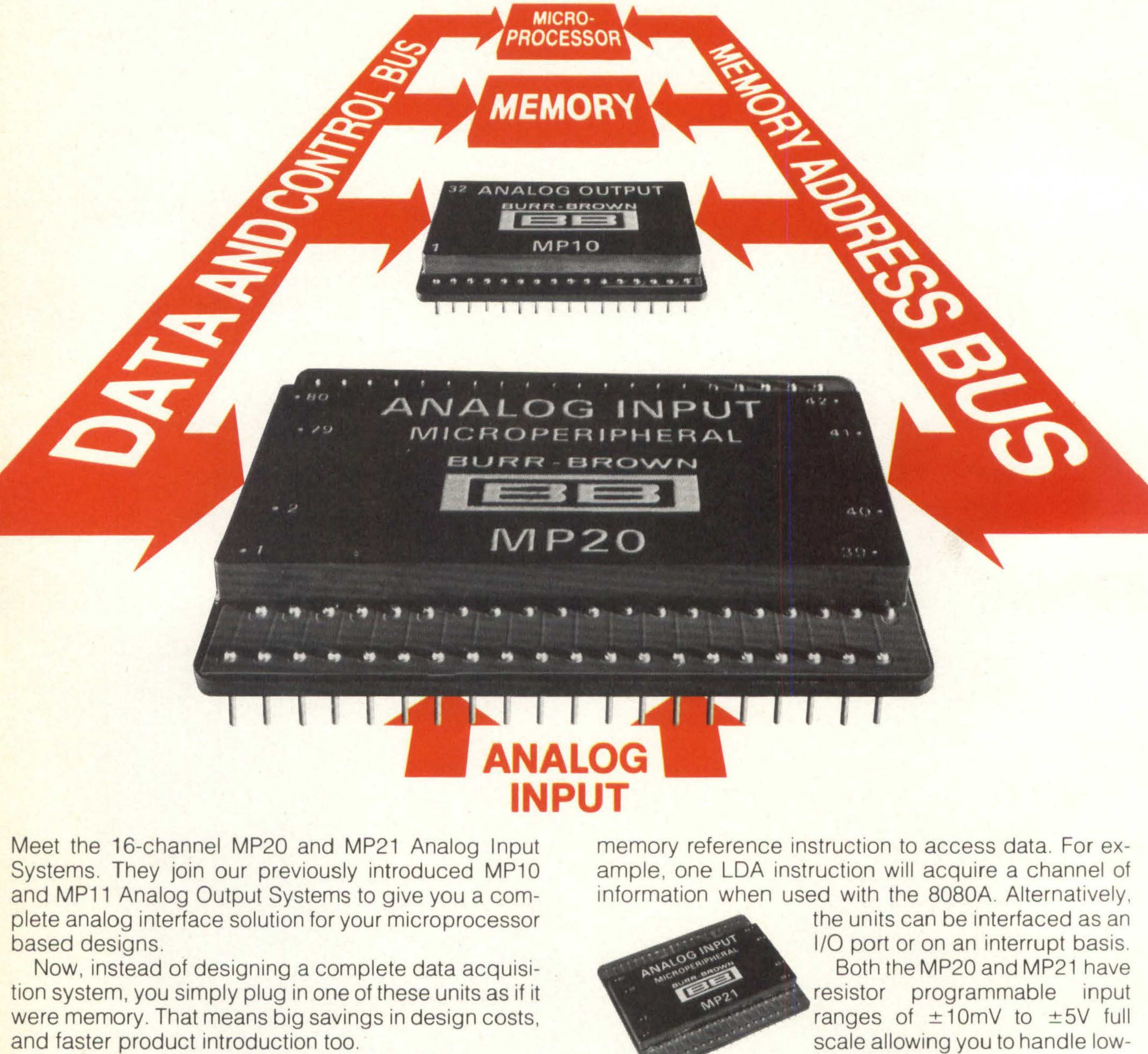

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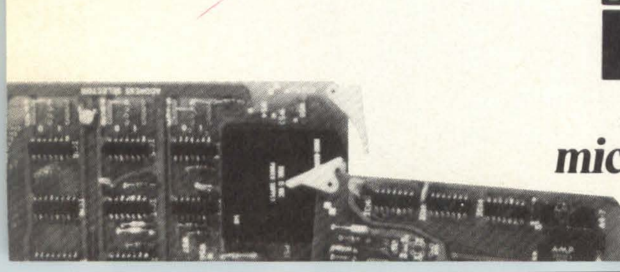

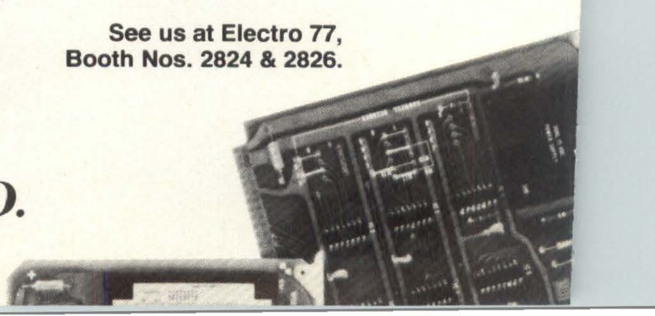

CIRCLE 1

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CIRCLE 4

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DM77


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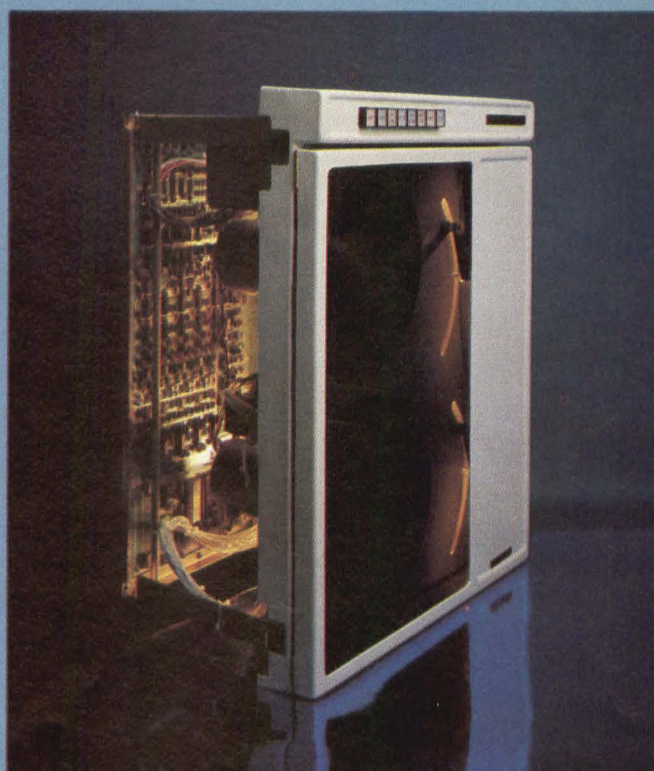

Mr. Peter A. Gilbody, Vice President, Tandberg Data Inc.
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CIRCLE 5

digital design

Volume 7 Number 3 March 1977

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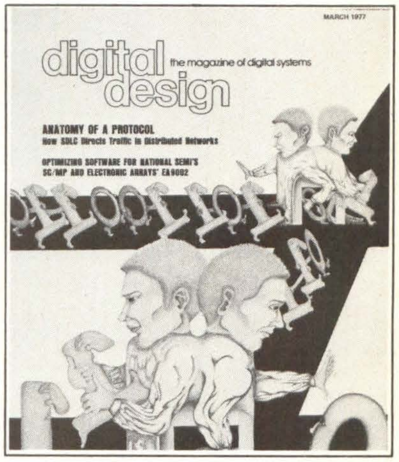

Synchronous Data Link Control can channel data communications in distributed computer networks with a minimum amount of extra hardware and software. To find out how, turn to page 60. Cover illustration by Irene Stawicki.

DEPARTMENTS

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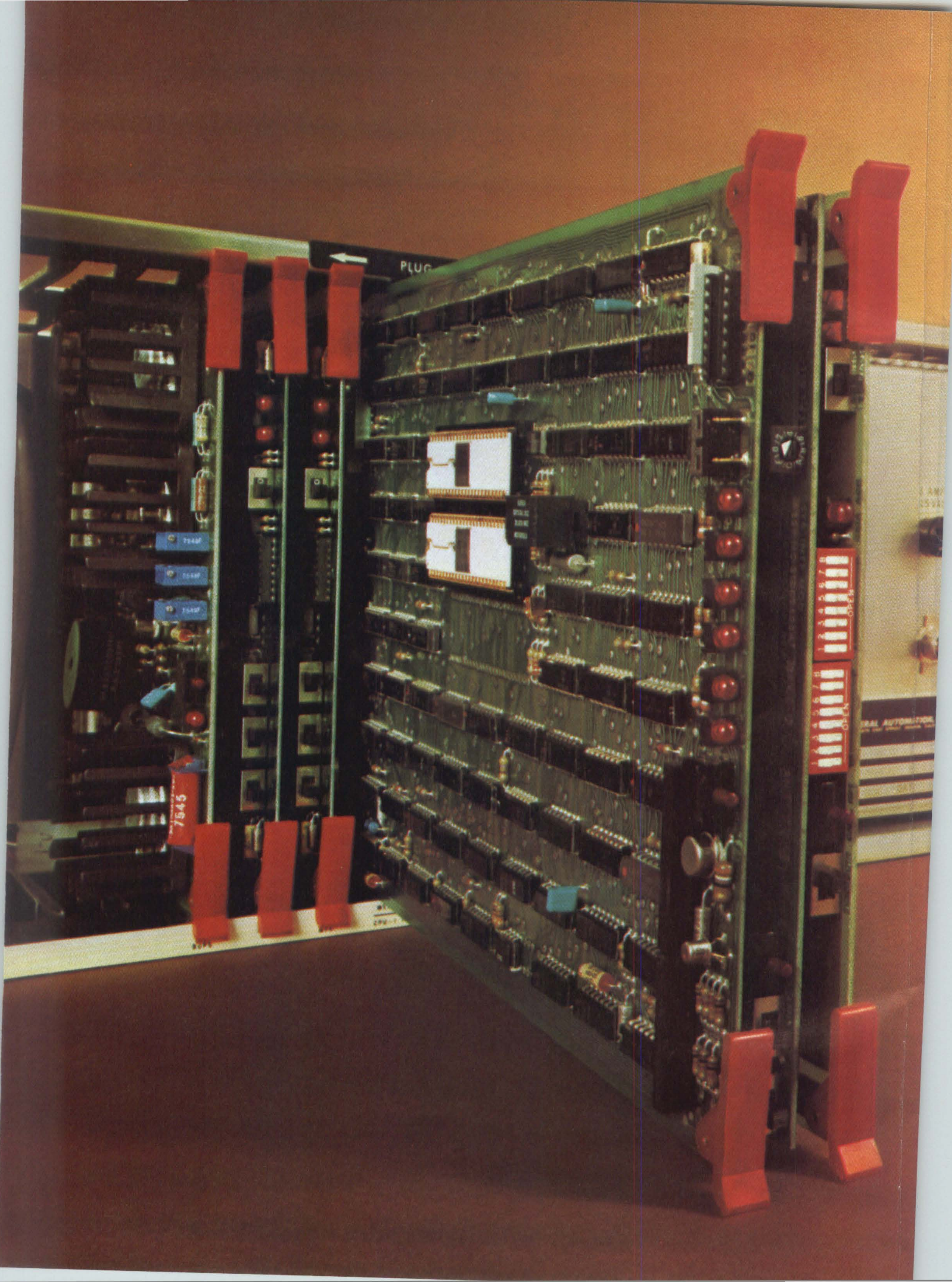
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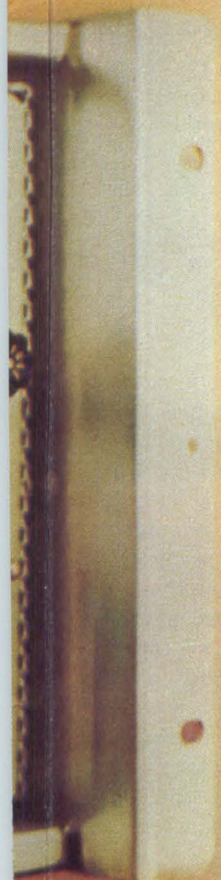

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CIRCLE 9

letters

CRT omission

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Our computer graphics system, Picture System 2, presents dynamically moving pictures of two- or three-dimensional objects . . .

TED NAANES
Marketing Support Specialist
Evans & Sutherland Computer Corp.
Salt Lake City, UT

dangerous advice?

• Although it is nice to see some assembly-language coding techniques in print ("How to Optimize Timing and Memory Usage," November) I found much of the advice given to be rather dangerous in the light of modern programming practice. Many of the tips involve saving a single byte here and there, when in fact long experience has shown that it is far better to buy a little extra program memory and to code in a straightforward and obvious way. I would venture to say this is even true for very small microprocessor systems, expecially as programming (and debugging) costs continue to increase and memory costs decline.

A particularly striking example appeared in the 6800 SWI dispatch routine (page 67), in which the restriction was made that a subroutine call must not be just below a page boundary. Because the location of a subroutine is not usually exactly known until after assembly, how is one to enforce this restriction? By manually blocking the code into pages (a giant step into the stone age)? By checking the assembly by hand and adding NOPs if needed? By a conditionally assembled NOP before each call (if your assembler has this capability)? How long before an error slips by? And all this to avoid a mere 4 bytes of code in a single-copy routine, and to save typically 4 microseconds in a routine that already takes 56 (counting the SWI). Even if you get it right the first time, the booby trap has been planted for future pro-

Up until now, a thermal printer that printed 30 cps was considered fast. No more. Now there's the EM-T7.

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CIRCLE 11

grammers who augment or modify the code.

If the last decade of programming experience has taught us anything, it has certainly taught us to avoid this kind of cute trick to save a few bytes. The extra ROM you buy will pay for itself many times over in the long run.

LAWRENCE J. KRAKAUER
Senior Member Technical Staff
Codex Corp.
Newton, MA

• *Terry Dollhoff replies: I agree with Mr. Krakauer in principle, but alas not in practical application. First, the series is intended to include something for all micro programmers; its three highlights are algorithms, timesaving techniques and memory-saving techniques. His comment that programming experience has taught us to avoid time and memory optimization and to buy extra memory is wrong. For example, at Acuity we have developed a complicated laser signal processing device that uses the TI 9900. We use almost 100 percent of the processing capability of the machine, and without many of the timesaving tricks indicated in this series we could not have built the device. Currently, our processor has only one or two percent of its capability left; if we ignored timesaving tricks we would have gone into the red.*

Saving memory is easier to justify. In 1980, a major auto manufacturer will include a microprocessor under the hood of one of its models. An extra memory at $5 would mean millions of dollars in total cost increase. But the added cost isn't the only problem. There are many microprocessor applications that require minimum power consumption because they must operate for long periods on battery power. An extra ROM means extra power – maybe a 30 percent increase for small systems.

As I said, I agree in principle, but the need for programming tricks still exists. But don't use them unless you need them. The golden rule is: if you don't need it, don't save it. In the laser application we do not use any tricks to save memory because we have plenty available. We don't have time, so we save it.

kudos for μP software article

• Dollhoff's "μP Software" article (November) was excellent!

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Design Engineer
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Meeting the diversified demands of an ever-increasing microprocessor market requires flexibility: not just hardware flexibility but software flexibility as well. MITS software including the innovative Altair BASIC language, allows the full potential of the Altair 8800b computer to be realized.

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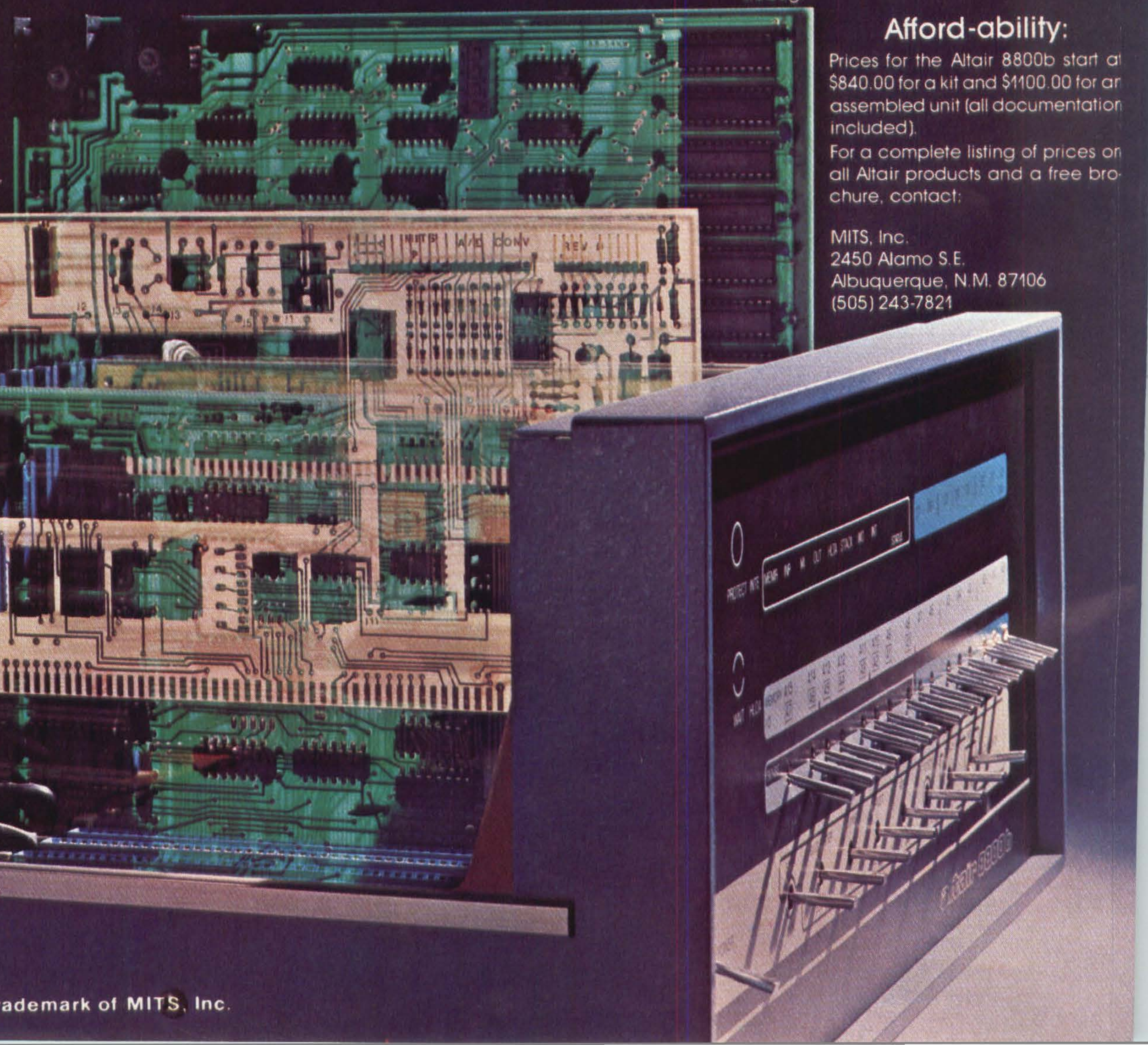


NOTE: Altair is a trademark of MITS, Inc.

Microprocessor based voice synthesizer puts speech at its user's fingertips

At the touch of its verbally handicapped master's fingers, a recently introduced artificial voice system outputs statements formed from a stored vocabulary of over 400 words, phrases, letters, prefixes and suffixes. Intended for use by persons with perceptual difficulties as well as by mentally retarded and other handicapped individuals, the microprocessor based system can interface with several types of control devices.

Termed Handi-Voice, the unit incorporates speech-synthesizer circuitry developed for its manufacturer's other artificial-voice systems. But Trez Wigfall, new-product development consultant at the Federal Screw Works' Vocal Interface Div., Troy, MI, explains that unlike the firm's basic Votrax synthesizer, the self-contained Handi-Voice constructs statements from pre-stored words and phrases.

Rather than construct speech from phonemes, Handi-Voice strings together words recalled from ROM by user-generated numeric codes.

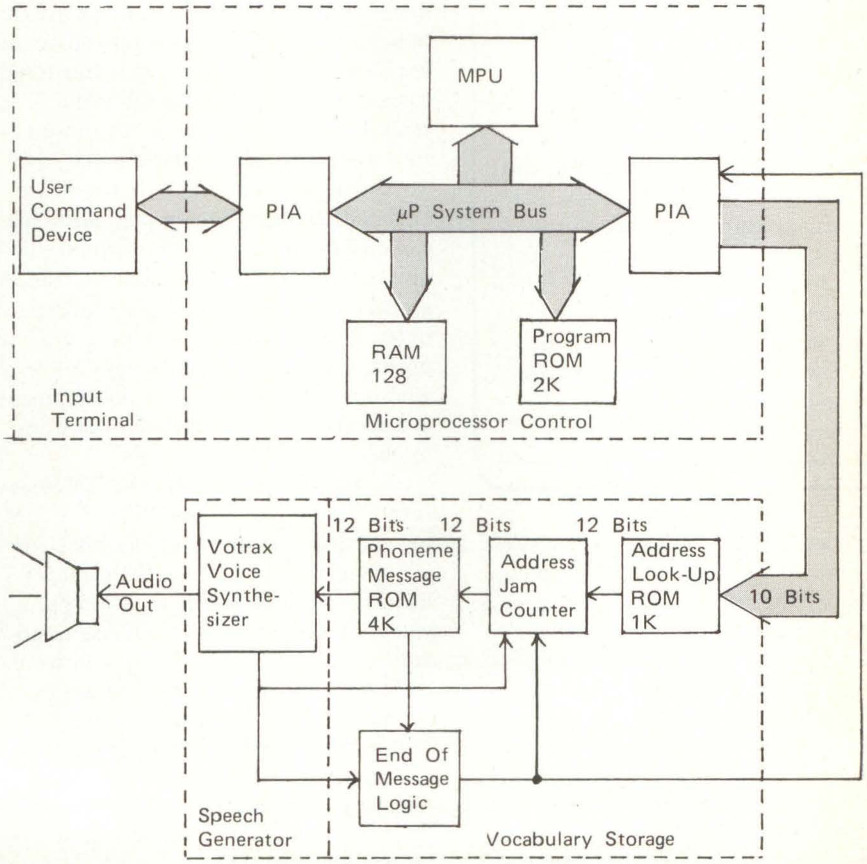
By contrast, Votrax functions as a computer peripheral; it creates statements by stringing together phonemes – basic units of speech.

Numeric phrase list. To trigger a specific word, a user keys-in its corresponding 3-digit numeric code on a calculator-type keyboard; a 3-digit LED display on the keyboard provides visual feedback. The user can modify a standard vocabulary word by keying-in appropriate prefix and suffix codes; if a desired word isn't stored in the system's vocabulary ROM, the user can spell it out.

The system also incorporates a memory that the user can load with frequently spoken sentences. One code entry then recalls one of these sentences.

Besides generating speech in response to numeric codes, the system can also operate more actively. In this mode, used by persons with severe physical handicaps, the system sequentially scrolls through all the numbers (0 through 9) for a given digit in its visual display. When it reaches a desired number, the user can stop it by activating a palm switch, a blow switch or some other type of specialized actuator. The system then repeats the process for the

Artificial voice system stores 400 words, letters or phrases, which a verbally handicapped user can call up by entering an appropriate 3-digit code on the system's calculator-type keyboard.



Microprocessor in the artificial voice system, an MOS Technology 6502, provides handshake and recognition of two terminal types, controls the terminals' displays, captures data, provides message buffer and lookup control, oversees keyboard operation, provides multiple mode control and distinguishes between a terminal's keyboard and other optional sensors.

two subsequent digits in the display until the user has chosen the proper numeric code, explains Wigfall.

For users unable to deal at all with numeric codes, the system can also interface with a terminal whose keyboard is labeled with symbols that represent frequently used words and phrases. This direct-selection keyboard serves mentally retarded persons and patients suffering from various forms of aphasia (the inability to articulate ideas), says Wigfall.

Talking Back

Systems like Handi-Voice utilize digital technology to generate speech; designers have also developed systems by which speech can directly generate computer commands. One recent application of such voice data-entry capability occurs on the Chicago Mercantile Exchange, where systems manufactured by Threshold Technology, Delran, NJ, help update price changes in commodity- and stock-trading operations.

Stationed in the Exchange's trading pit, a price reporter wearing a wireless microphone states, for each trade that involves a price change, the month of the contract traded and the trade's new price. A Model 500 voice data-entry terminal translates this spoken information into a visual display, which the reporter then verifies.

Verified and transmitted to the Exchange's price reporting system by the reporter's "enter" statement, the new price information updates national wire service reports on the Exchange's trading.

μP a data handler. The speech system incorporates an MOS Technology 6502 microprocessor, used primarily as a data handler, according to the consultant. Its functions include supervising I/O between the numeric keyboard and the synthesizer unit, handling ROM-lookup of the synthesizer's speech codes and overseeing handshake with the various terminals used by the system.

The microprocessor also supervises the system's operating modes, which include, for example, a "talk repeat" function whereby the system can continuously repeat an emergency message until shut off.

Tape speed is up, but most systems need slow units

Minicomputer throughput rates have increased in the last five years, and tape-drive speed and throughput have kept pace. But throughput limitations in many minicomputer systems still require OEM systems designers to specify tape drives at the low end of the performance spectrum for most minicomputer applications.

So says Darell Meyer, tape product manager for the Pertec Div. of Pertec Computer Corp., Costa Mesa, CA. Many minicomputers now provide 200- to 750-kbyte/sec throughput rates, compared with 10 to 30 kbytes/sec five years ago, he claims. But system throughput limitations still mandate tape speeds in the 25- to 50-ips range for "the bulk" of minicomputer applications.

For applications that can ulitize higher-speed tape drives, however, such units – which utilize group code recording techniques and run at 125 ips – will become available.

7-track declining. While 7-track tape drives still find use, they now represent only about 3% of the total tape-drive market, claims Meyer, adding that this trend toward 9-track recording will make 7-track units more expensive for those future users who will require them.

New tape drives primarily use phase encoded recording techniques, although some of the most recently introduced units offer combination phase encoded/group code capabilities. This dual capability allows designers to achieve simplified system architecture, says Meyer, who reported on tape-drive developments at a recent Invitational Computer Conference.

½" tape on way out? Meyer foresees future tape drives, with 6250-bpi recording density, trading off higher price for increased throughput and the greater reliability that group code recording provides. All 6250-bpi units will accommodate existing 1600-bpi formats, however.

Eventually, a new tape medium – probably 2.5"-wide tape comparable to IBM's 3850 – could replace ½" tape, claims Meyer. But while industry is moving away from ½" tape as a primary backup storage medium, ½" tape's demise lies far in the future.

Future transfer rates and format of the new tape medium will be equivalent to and interchangeable with disk storage, according to Meyer.

The unique demands of microprocessor-based systems and their increasing popularity has resulted in the development of a special breed of low-cost power supply.

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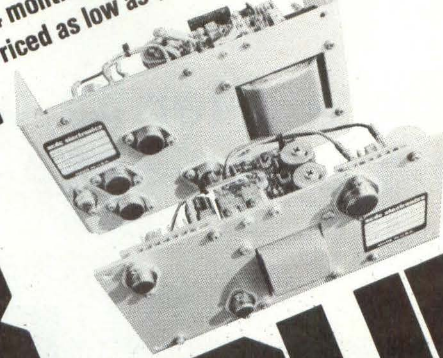

INPUT: 105-125/210-250 VAC at 47-63 Hz. Derate 10% at 50 Hz.

OUTPUT

Model	Nominal Voltage	Adj. Output Range ±V	40°C	55°C	70°C
			Ratings (Amps) Maximum Current		
MP 301	+5	0.25	3.0	2.25	1.50
	+12	0.5	0.5	0.38	0.25
	−5	0.25	0.85	0.50	0.43
MP 401	+5	0.25	6.00	4.50	3.00
	+12	0.5	1.00	0.75	0.50
	−5	0.25	1.00	0.75	0.50

All outputs are isolated from line and ground.

REGULATION	0.1% +5mV NL-FL; ±0.1% ±5mV for a ±10% input change.
RIPPLE	2mV RMS max, 20mV P-P max.
STABILITY	Typically 10mV for eight-hour period after initial warm-up.
TRANSIENT RESPONSE	Output voltage returns to within regulation limits within 50 microseconds in response to a 50% load step.
OUTPUT IMPEDANCE	DC-1KHz: 0.005 ohm max. 1KHz-100KHz: 0.5 ohm max.
TEMPERATURE COEFFICIENT	0.02%/°C max.
REMOTE SENSING	Terminals are provided to maintain regulation at the load, compensating for up to 0.25 Volt loss in the load cable.
AMBIENT TEMPERATURE	Operating: 0 to 70°C Storage: −55 to 85°C
OVERLOAD PROTECTION	Inherently protected against overload and short circuit by a foldback type characteristic. Recovery is automatic.
OVERVOLTAGE PROTECTION	The unit can be furnished with overvoltage protection on any or all of the outputs. The output will be crowbarred in the event of a rise in the voltage of between 1 to 2 Volts or 10 to 20% (whichever is larger) above maximum adjustable output voltage. This protection circuit is completely independent of the supply and is adjustable. The addition of overvoltage protection does not add to the outline dimensions of the supply.
CONSTRUCTION	Integral aluminum chassis and heatsink. Sides are open to allow unobstructed ventilation, easy inspection and accessibility.

DIMENSIONS (Shown as $\frac{inches}{mm}$)

	Wide	High	Long
MP 301	4.03 / 102.36	2.70 / 68.58	8.03 / 203.96
MP 401	3.20 / 81.28	4.88 / 123.95	9.00 / 228.6

PRICES

MP301	$ 79.00 (1-9); $72.00 (25-49); $71.00 (100-249); $65.00 (250 and up)
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CIRCLE 15

Week late for its debut, μP-based system will oversee Rose Parade float next year

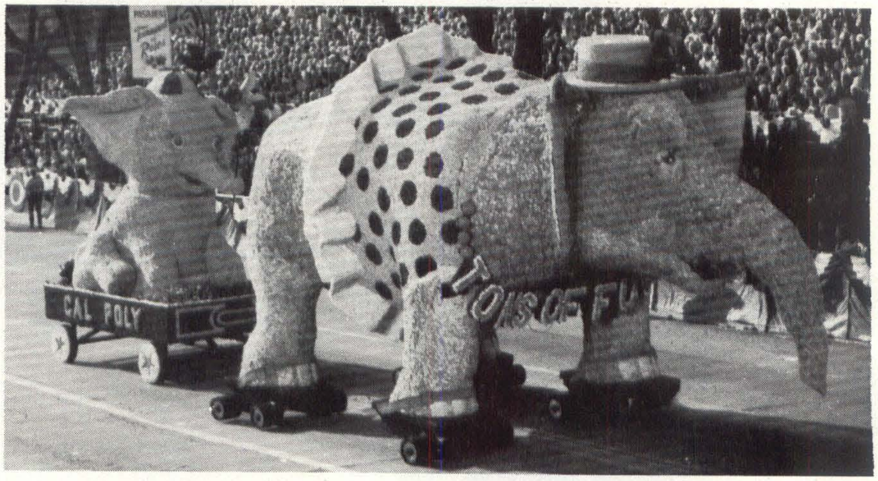
Though it wasn't quite completed in time for use in this year's Rose Parade on New Year's Day, a microprocessor based control system will oversee the operation of a float in next year's event. The system will replace a programmable controller that this year operated "Tons of Fun," a 17 ft-high animated mother elephant on roller skates that lurched along the Rose Parade route at 3-5 mph with an animated mouse on her hat and her rambunctious baby in tow in a wagon.

Entered by California State Polytechnic University, Pomona and San Luis Obispo, the award-winning float measured 16 ft wide and 45 ft long and weighed 25,000 lbs. According to Doug Dubrall, recent Cal Poly graduate and electronics chairman of the school's 1976-77 float committee, students in 1976 began designing the microprocessor based controller to replace the plugboard-programmed Master Animation Controller (MAC) that he and a friend had designed in 1975 and that ran "Tons of Fun" in the 1977 Rose Parade.

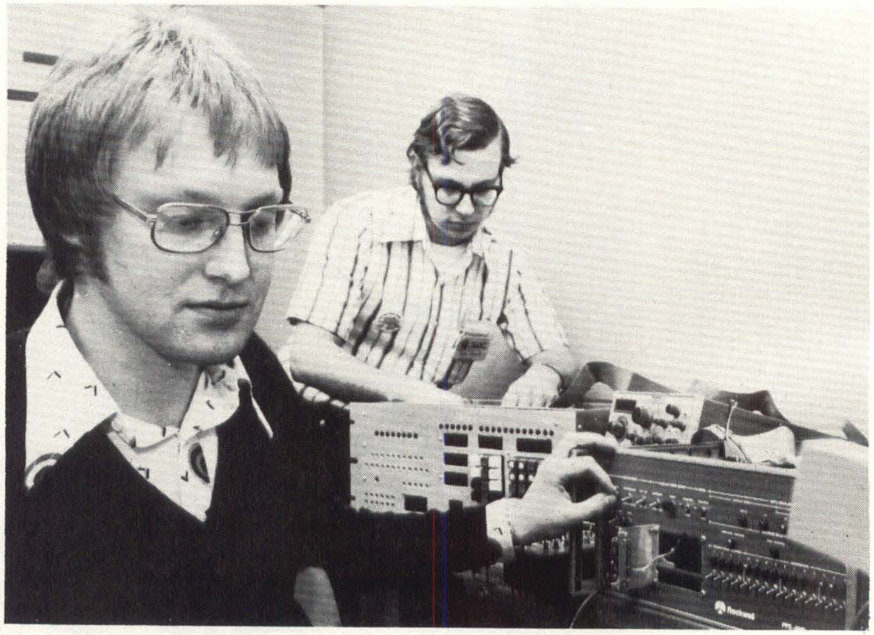
Reusable system required. As configured by Dubrall and Rick Regan, the MAC met two design goals; it formed a reusable system that students could reconfigure for subsequent floats, and it provided automatic animation – it could sequence through a float's motions without intervention by the float's operators.

Designed around a group of Signetics 5 x 5 timer chips, the MAC triggers those chips sequentially to run relay drivers that in turn drive a float's hydraulic solenoids, electric motors and other actuators. When an animation sequence reaches its programmed destination, a limit-switch actuation signals the MAC, which resets the sequence's timer chip and triggers the next timer in line.

Aboard "Tons of Fun " a 351-cu.in.



Dubbed "Tons of Fun," California State Polytechnic University's float in the 1977 Rose Parade measured 17 ft high, 16 ft wide and 45 ft long and weighed 25,000 lbs. It "walked" in response to signals sent by a plugboard-programmable controller to hydraulic actuators in the mother elephant's rear legs; the controller also monitored the operation of the rest of the float's animation. Next year, a microprocessor based system will provide greater control and decision-making capability for Cal Poly's float; with one additional week of tests the μP system could have supervised this year's entry.



Cal Poly student Dan Klukovich (foreground) programs the μP-based control system with the aid of a Rockwell Assemulator as Doug Dubrall, electronics chairman of the school's 1976-77 Rose Parade float committee, assembles a controller subsystem.

CIRCLE 16▶

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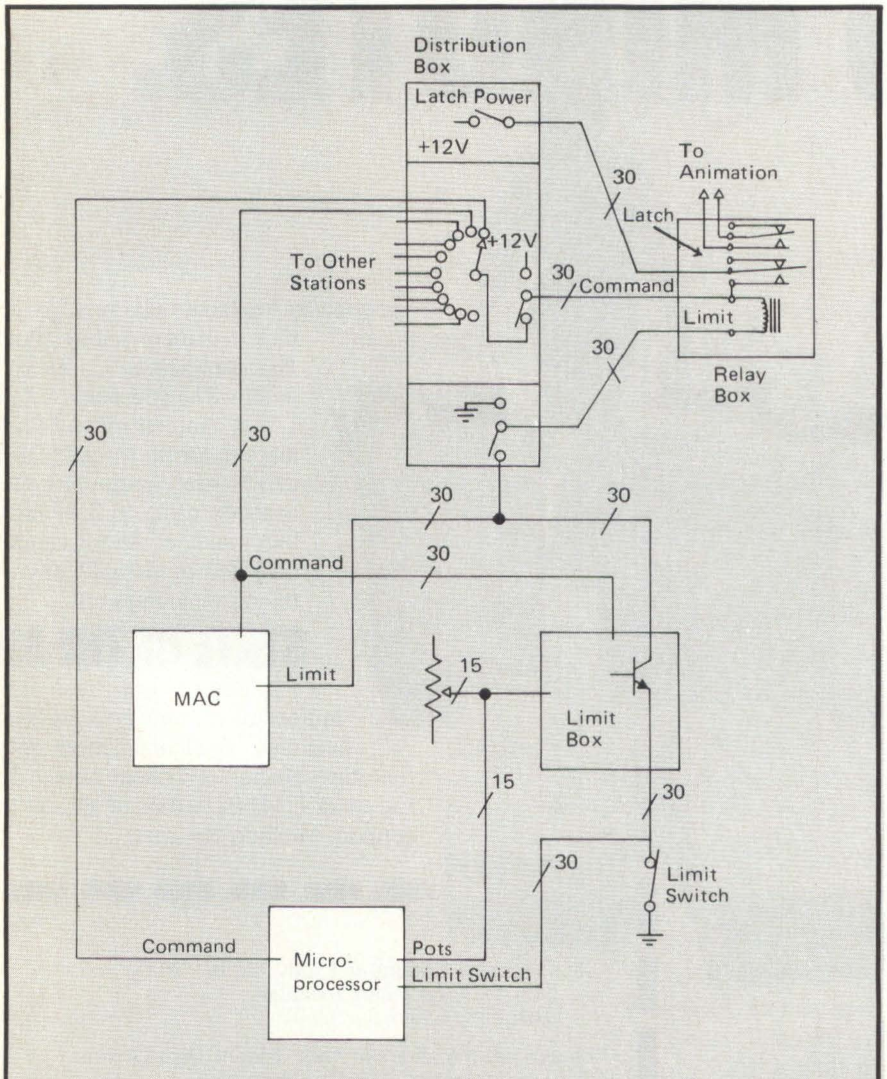
gasoline engine drove hydraulic pumps, which in turn drove hydraulic motors mounted on the mother elephant's two rear legs. The MAC sequenced these motors' operation and thus caused the elephant to "walk." The controller also sequenced the operations of the windshield-wiper motors that operated the mother's and baby's eyelids and hydraulic systems that controlled other elements of the float's animation, such as the baby elephant's beanie. Operators maneuvered the float from inside by turning the mother elephant's front legs, which mounted on a pair of Northrup F5 landing gear whose steering mechanisms were linked together.

The MAC exhibits one drawback, says Dubrall – it can't make decisions if something goes wrong; it can only signal that part of a float's animation has ceased functioning. During the 1977 parade, such animation failures occurred; Dubrall had to correct them by shorting out each affected limit switch, thereby fooling the MAC into thinking the switch was enabled. The controller then "timed out" each affected animation feature before resetting that feature's timer chip.

Enter micro. Reasoning that a microprocessor based control system would provide greater flexibility in dealing with such problems, Dubrall and others began last fall to design one. They chose Rockwell International's PPS/4 microprocessor because such units were readily available; Professor Art Arellanes at the school serves as a Rockwell consultant and provided advice on the microprocessor's operation, and the school also owns several Assemulator development systems.

Dubrall also "kind of liked the idea of the bus design system on (the PPS/4), where you can just hang more and more things on the bus." The microprocessor exhibits a "party-line" bus structure, he explains; its address, data and read/write buses connect to all peripheral chips in a system.

As designed by Dubrall, who also constructed some of its subsystems, the microprocessor based controller incorporates a system clock, the CPU, a general-purpose I/0 board, a printer (GPKD) module, a multiplexer board, a general purpose I/0 board, a printer controller, 4K each of PROM and RAM, an interval-timer board, a bus analyzer board, relay-driver boards and a cassette programming system. Dan Klukovich, now a Cal Poly senior, supervised construction of the processor system and developed its software with help from Arellanes and Andy Dannelley, another student. Among other functions, this software replaces the MAC's timer chips.



The μP-based control system incorporates a Rockwell PPS/4 CPU, whose buses support a system clock, a general-purpose keyboard-display module, a multiplexer board, a general-purpose I/0 board, a printer controller, 4K each of PROM and RAM, an interval-timer board, a bus analyzer board, relay-driver boards and a cassette programming system. The printer controller, interval-timer board and bus analyzer board weren't completed in time for use in the 1977 Rose Parade; an earlier, less flexible plugboard-programmable master animation controller (MAC) subbed for the microprocessor system in that parade.

The μP-based system will replace a plugboard-programmable controller used in this year's float.

One more week. The system's printer controller, interval timer board (an animation-status backup system) and bus analyzer board (a debug device) weren't completed in time for the parade. The team needed about one more week to get the remainder of the system working, says Dubrall; all of the other multiplexing and I/0 subsystems had been completed but were untested.

The GPKD module handles the control system's LED displays as well as its keyboard and pushbuttons, all of which were to have mounted inside the mother elephant. Dubrall initially used the wrong type of drivers for the LEDs in the display but quickly corrected this problem.

The controller's multiplexer board accepts 40 limit-switch inputs and reduces them down to two lines. It can also supervise 20 analog potentiometers, whose outputs were to have further described the position of each animation element during the parade. Not completed in time for use in the parade, the 10-turn potentio-

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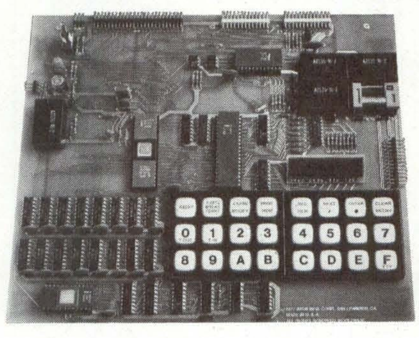

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meters would have been attached through string and return springs to each animation element. The multiplexer board would have reduced the pots' 20 outputs down to one line, attached to a Burr-Brown ADC82 8-bit A/D converter. By outputting an address (0-19) that specifies one set of limit switches and a potentiometer, the controller's CPU would have acquired from the multiplexer board a 4-bit word representing the sensors' status.

Chips on the system's general-purpose I/0 board, explains Dubrall, control the relays that in turn supervise a float's hydraulic solenoids. Designing this board was "straightforward;" preconstructed by Rockwell, it only required the addition of relay-driver circuitry already used in the MAC.

The system's memory boards were also preconstructed; the designers programmed the PROM boards with a Rockwell Assumulator and transferred the programming to Intel 1702 UV-erasable units. The RAM board, which stores the "operating system" of specific system data for a float, is backed up by the cassette system. Dubrall notes that using magnetic tape for this backup was easier than relying on paper tape, which wouldn't stand up to a float's internal environment.

Gap narrows between µPs and custom LSI as micro specialization grows

As in most other fields of endeavor, specialization has arrived in the world of microprocessors. And such specialization—the design of microprocessor families that work best when used in narrowly defined application areas—will continue, until someday engineers may find it difficult to "define the dividing line between microprocessors and custom LSI."

The µP's evolution from universal to specialized processor was probably inevitable.

Surveying developments in microprocessor architectures, Peter Verhofstadt of Fairchild Camera and Instrument has reached this conclusion and has also concluded that the trend to specialized microprocessors was probably inevitable. "After all," he points out, "there are 34 types of TTL 4-bit shift registers available on the market today, and who would have predicted the need for that years ago?"

Improved classification. Reporting to the 7th International Conference on Microelectronics, held concurrently with Electronica 76 in Munich last fall, Verhofstadt noted that computer experts usually classify microprocessors according to such architectural parameters as number of data bits, address bits, accumulators, general-purpose registers, I/O ports and instructions; type of arithmetic used; availability of hardware stack and DMA; and time for one basic instruction cycle.

Such classifications mean little from an applications point of view, he said, urging that they be replaced by a broader, applications oriented scheme with four classes:

★ "Low-end" units for simple control applications and replacement of electromechanical devices;

★ Intermediate units to replace hardwired logic or custom LSI in more complex industrial controllers as well as in peripheral, communications and other equipment;

★ "High-end" units with minicomputer-like structures for use in such applications as data processing, real-time con-

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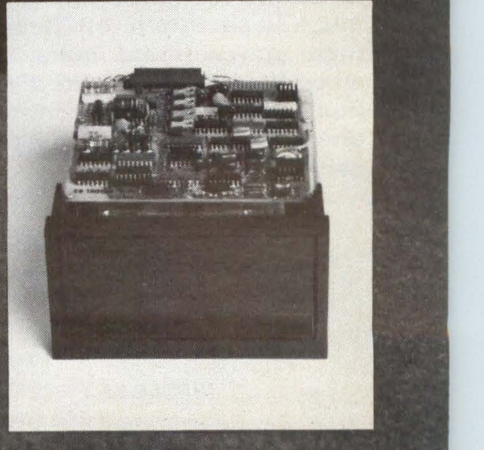

CIRCLE 22

trol and stand-alone terminals;
★ Bit-slice units for very-high-performance applications.

Difficult questions. Assesing possible future developments in microprocessor architecture, Verhofstadt predicted continued specialization within and between these four classes. Faced with this specialization, designers will have to answer:

★ Will "hybridized microprocessors"—LSI products programmable within an applications class but tailored to that class—appear?
★ Should specialized, one-chip programmable controllers incorporate semi-analog I/O as well as CPU and memory?
★ How completely will microprocessor based architectures replace current mini- or maxicomputer architectures?
★ How soon and how completely will networks of microprogrammable microprocessors replace larger computers?

Hardware and services

Cosmac evaluation kit. Designated CDP18S020, this kit contains a PC board, byte input and output ports, a terminal interface, a 512-byte ROM that stores a utility program of commonly required functions, and 256 bytes of RAM for user program storage. Con-

trol logic and built-in displays provide facilities for program debugging; you must provide a terminal and a power supply. The kit's CPU is the CDP1802 Cosmac microprocessor, a single-chip 8-bit CMOS unit. A 6" x 4" area of the board is free for user-added I/O devices. Price: $249 in singles. RCA Solid State Div., Somerville, NJ 08876. (201) 685-6423 **Circle 145**

I/0 modules. For interfacing machines, instruments, computers and other devices to the manufacturer's Series 180 microcomputers, these I/O modules include the PCS 1804, an ac/dc unit that accepts up to eight ac inputs, eight high-level digital inputs, eight ac outputs and eight high-level digital outputs. A multifunction module, designated the PCS 1820, accepts up to 32 digital inputs and 16 digital outputs under the control of a PCS 1806 or 1810 microcomputer. It also accepts up to eight priority interrupt inputs, three software programmable 16-bit counters and a programmable time base generator. A TTL module, designated the PCS 1823, accepts up to 64 TTL digital inputs and 64 TTL digital outputs under the control of a PCS 1806 or 1810. Finally, a 16-channel A/D module, designated the PCS 1850, consumes 1.5W. Prices: $335 for the 1804, $375 for the 1820, $285 for the 1823 and $805 for the 1850. Process Computer Systems, 5467 Hill 23 Dr., Flint, MI 48507. (313) 767-8920 **Circle 146**

$325 computer system board. The 2650 Computer System incorporates a Signetics 2650 CPU and includes an 80-character, 16-line video generator; a keyboard interface; a 300-baud cassette interface; 768 bytes of user RAM and a supervisor program. It comes completely assembled and tested and requires a 5V, 3A power supply. An assembler/editor package is available, and a Basic interpreter will be available shortly. The available supervisor program allows alteration or display of memory, execution of user programs, setting and clearing of breakpoints, inspection and alteration of the CPU's registers, dumping to and loading from tape, and verification of a tape's contents. The assembler/editor and Basic packages cost $20, which includes a cassette tape and a listing. Central Data Co., P.O. Box 2484, Station A. Champaign, IL 61820. **Circle 147**

Bipolar bit-slice additions. These six devices expand the manufacturer's 2900 family of bipolar μP components and include the Am2902, which provides look-ahead carries across a group of four Am2901 microprocessor ALUs with a typical propagation delay of 6 μs. Three additional devices—the Am2905, 2906 and 2907— are quad bus transceivers; the 24-pin 2905 and 2906 offer dual-driver inputs while the 20-pin 2907 has only single-driver inputs. The Am2911 microprogram sequencer provides eight pins for direct inputs and register inputs. Finally, the Am2918 quad D register provides four standard totem-pole outputs and four three-state outputs. Prices: $3.31 for the Am2902, $7.80 for the Am2905/6/7, $9.31 for the Am2911 and $3.56 for the Am2918,

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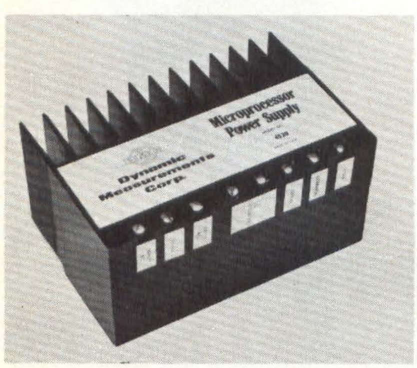
CIRCLE 24

all for commercial versions; military versions also available. Raytheon Semiconductor, 350 Ellis St., Mountain View, CA 94040. (415) 968-9211 **Circle 148**

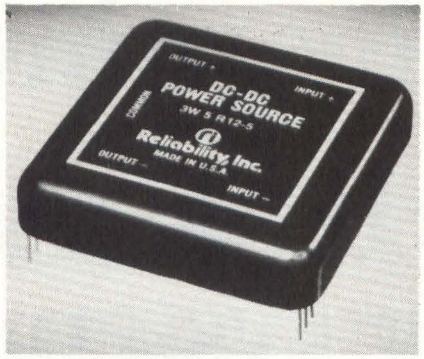
µP analog output circuits. The MP10 and MP11 are 32-pin, triple-wide DIP units and are compatible with the 8008, 8080A, 6800 and other microprocessors with regard to voltage level, loading, timing, logic and software. Each unit provides two channels with ±10V output, and throughput accuracy measures better than ±0.4% of full scale range. Both units contain two internally trimmed 8-bit D/A converters plus all necessary interface, timing and address decoding logic. The MP10 is bus compatible with both the 8008 and 8080 and requires no external components when used with those devices. You can also use it with SC/MP by adding pull-up resistors to the address bus and with the F8 and Z-80 by changing some timing parameters. The MP11 is compatible with 6800, 650X and 9002-type microprocessors. Price: $125 in 25-99 quantities. Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734. (602) 294-1431 **Circle 143**

Encapsulated µP power supplies. Encapsulated in epoxy, these 30W power supplies measure 6.1" x 4.25" x 3". The MPS line includes single, dual and triple output models. Total (line plus load) regulation lies within 0.03% for 5 V outputs, and within 0.01% for 9, 10, 12 and 15 V outputs. Positive and negative outputs track within 100ppm/°C, and maximum output voltage error



measures between minus zero and plus one percent. 5V outputs are current limited and all others fold back to 20mA. Price (single quantity): $130 for single output, $140 for dual and $155 for triple outputs. Dynamic Measurements Corp., 6 Lowell Ave., Winchester, MA 01890. (800) 225-1151 **Circle 153**

DC/DC power source. Model 3W 5 R12-5 provides +12V @ 200mA and -5 V @ 100mA from a 5 Vdc input. The outputs are fully short-circuit protected and free of damaging turn-on and turn-off overshoots. Ripple and noise measure 1 mV rms, and line and



load regulation equal 0.02%. Input to output isolation equals 300 V, and operating temperature ranges from -25°C to +70°C. The unit measures 2.0" x 2.0" x 0.40" and comes encapsulated in a black finished copper case. Reliability, Inc., 5325 Glenmont, Houston, TX 77036. (713) 666-3261 **Circle 155**

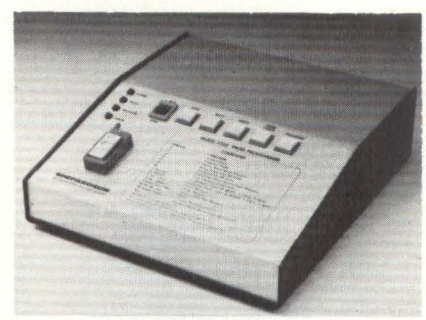
8080 DOS program source. This program source for an 8080-based disk operating system includes listing and documentation for: DOS for 3740-format compatible diskettes, sector allocation/de-allocation software, eight character file names and three character extensions, sequential and random-access files, binary file storage and loading, and other operating-system functions. Offered to single users on a non-resale, licensing basis, the package costs $500 plus shipping and COD. Intelligent Computer Systems, 777 Middlefield Rd., Suite 40, Mountain View, CA 94043. (415) 961-8941 or (408) 244-5511 **Circle 156**

Analog I/O for Pro-Log µCs. These single-board analog I/O systems, designated the 4216 (16-channel input board) and 4102 (2-channel output board), are electrically and mechanically compatible with Pro-Log microcomputers. A CPU can treat the boards as memory – each channel requires one 8-bit memory location, and the address block occupied by each board is strap selectable. Alternatively, the systems can be treated as I/O. Intended primarily for industrial control or test-equipment applications, each input board is a 16-channel system. Unit prices: $295 for the 4216. $195 for the 4102. In 100s: $180 and $120.

Burr-Brown, international Airport Industrial Park, Tucson, AZ 85734. (602) 294-1431 **Circle 161**

Bipolar µP evaluation kit. For evaluating the manufacturer's 8X300 bipolar microprocessor, this single-board kit includes the 250-ns CPU, four I/O ports and 256 bytes of working data storage. Additionally, preprogrammed PROMs contain control logic, RAM control and RAM diagnostic programs. Designated 8X300KT100SK, the kit provides access to the microprocessor's address, instruction and IV buses as well as all controls and signals. Controls for diagnostic and instructional purposes include a Wait mode to single-step through a program; one-shot instruction jamming for control of program start location, changes of program flow, changing or examination of internal registers, or testing of simple sequences; and repeated instruction jamming to examine I/O bus and control lines without software changes. Price: $299 in singles. Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. (404) 739-7700 **Circle 144**

PROM programmer. Model 2708 incorporates 20 mA and RS 232 interfaces and provides full editing capability that lets you store, move and alter data in its buffer memory. It can adapt



to any terminal data rate up to 600 baud and accepts data from paper tape in BNPF, BHLF, binary or ASCII hexadecimal formats. The device programs any manufacturer's 2704- or 2708-type PROMs. Shepardson Microsystems, 20823 Stevens Creek Blvd., Bldg. C4-H, Cupertino, CA 95014. (408) 257-9900 **Circle 149**

SC/MP-II Samples. An NMOS version of the manufacturer's SC/MP 8-bit microprocessor, SC/MP-II consumes 200mW, about one-fourth as much as the PMOS unit. It requires one +5V source, compared with +5V and -7V for the earlier model, and requires 1 µs to complete a microcycle and 5 µs to execute a typical instruction—half as much as SC/MP. Pin-, code- and soft-

Con't p. 31

Scanner's μcomputer constructs images of patients' innards

To achieve accuracy and performance not possible in an analog control system, the developers of an ultrasonic scanner designed it around a microcomputer that keeps track of the scanner's transducer coordinates, converts echo data into images and maintains the system's CRT display. The manager of G.D. Searle's ultrasound program claims the microcomputer offers cost, size and expansion advantages not possible with other types of controllers.

Dr. Albert Waxman explains that Searle's Pho/Sonic SM sells for about the same price as an analog ultrasonic scanner – about half the price of a conventional X-ray machine and about one-tenth the price of a computer-axial tomography (three-dimensional X-ray) unit. It creates a digital image of a cross-section of a patient's body by processing low-energy sound waves reflected from the body into a special transducer.

Speeding software development. The scanner's designers "never seriously considered" using a minicomputer as the system's controller, according to Waxman. The microcomputer they chose, an LSI-11 manufactured by

The scanner's designers "never seriously considered" using a minicomputer as a controller.

Digital Equipment Corp., Maynard, MA, has a 400-instruction set that allowed them to develop the system's software quickly – "exceptionally important for a small operation," he says.

Actual software development occurred on a DEC PDP-11/35 mini. The system's applications programming allows incorporation of such scanner options as an electronic caliper, scanning and power tilt, and a multi-imaging camera. It also will allow future expansions with minimum additional hardware, claims Waxman.

Fifty-percent resolution improvement. The ultrasonic scanner can distinguish between various kinds of tissues, diagnose conditions resulting from pregnancy and visualize such conditions as tumors, lesions of the eye and liver abnormalities. Physicians also use it – usually to complement X-ray and computer-axial tomography studies – in heart studies and to visualize gall-bladder lesions, especially gallstones. It can resolve a one-mm-square area – a resolution 50% better than analog ultrasonic scanners', according to DEC.

Accessing 4K x 16 bits of core memory and interfaced with the scanning circuitry through DEC's DVL11 serial line unit, the LSI-11 acquires transducer coordinates and direction, converts reflected sound into CRT images and automatically annotates the scanner's display with patient identification, scale factors and other information.

The microcomputer's control chip provides microinstruction sequences, and its data chip incorporates paths, registers and logic for the microinstructions. Two microcontrol ROMs store DEC's PDP-11/35 and 11/40 instruction sets, as well as debugging firmware and ASCII/console routines. A third microcontrol ROM provides fixed and floating point arithmetic.

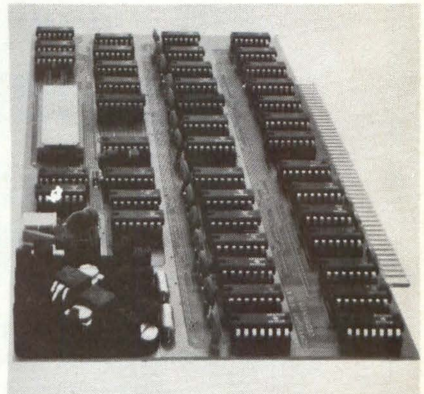
The microcomputer must perform large numbers of trigonometric calculations to determine the absolute coordinates and direction of the scanner's transducer; the scanner's overall accuracy measures better than ±1.5 mm at 20 cm from the transducer face.

ware-compatible with the PMOS unit, SC/MP-II requires slight modifications to its crystal frequencies to achieve compatibility with all SC/MP support equipment. Its clock oscillator, located on the chip, uses tv-type 3.58- or 4-MHz crystals, and you can also drive its clock with a standard TTL timing system. Price for single samples: $17.76. National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. (408) 737-5000

M6800 support hardware. This support hardware includes chassis, 5- and 10-slot card cages and a power supply for the manufacturer's Micromodule products. Both card cages have mother boards, pin-compatible with the Micromodules and all of the maker's Exorciser modules. The cages can mount on five different axes. Power supply outputs measure 15A at +5 Vdc, 2.5A at +12 Vdc, 1.5A at -12 Vdc and 0.1A at 8 Vac. A remote voltage sensing capability for the 5 V output can compensate for as much as 0.5 Vdc drop along the connecting leads; the supply requires single-phase ac power over a 47 Hz to 420 Hz range. Two chassis models serve ten-card cage and five-card cage systems; both fit into a standard 19" Retma rack. Prices: $147 for the 10-card cage, $98 for the 5-card cage, $295 for the power supply, $660 for the 10-card chassis and $610 for the 5-card chassis. Technical Information Center, Motorola Semiconductor Products, Inc., P.O. Box 20294, Phoenix, AZ, 85036. (602) 244-6815 **Circle 154**

I/0 interface controllers. For use with the manufacturer's GA-16/220 and GA-16/330 16-bit microcomputers, these I/0 interface controllers serve floppy disks, moving-arm disks that store up to 300 Mbytes, head-per-track disks that store up to 2 Mbytes, magnetic tape drives, line printers that write up to 1250 lpm, card readers that scan up to 1000 cpm, Teletypes, character printers, paper-tape readers and punches, plotters, keyboards and CRTs. For data acquisition and process control, the firm offers optically isolated input and output controllers for TTL digital signals, variable threshold dc or ac signals, and a family of A/D and D/A converters and multiplexers for analog signals. The controllers plug into any I/0 slot in the microcomputers' chassis. General Automation, 1055 S. East St., Anaheim, CA 92805. (714) 778-4800 **Circle 152**

Z-80 CPU card. This CPU card incorporates a Zilog Z-80 with a 4-MHz clock rate and is plug-compatible with existing microcomputers. It uses the S-100 computer bus and can also work with 2-MHz systems. The card can jump to any 4K boundary in memory upon power turn-on and incorporates



jumper-wire-selectable wait states. It comes with a Z-80 monitor, complete documentation, source code and paper-tape object code. A Z-80 assembler and Basic interpreter are also available. Price: $295 in kit form or $395 assembled. Cromemco, 2432 Charleston Rd., Mountain View, CA 94043. (415) 964-7400 **Circle 151**

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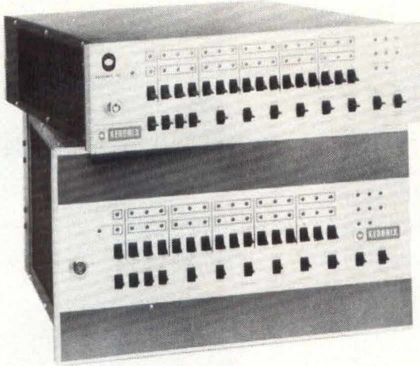

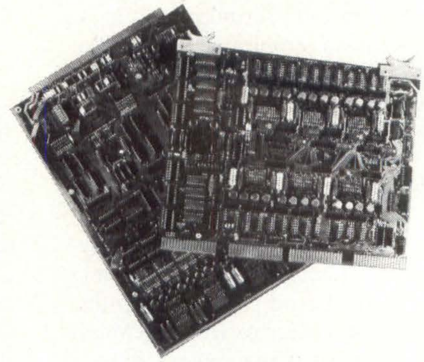

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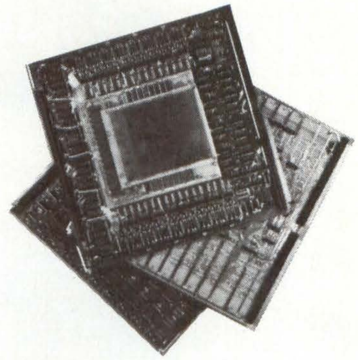

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LED THERE BE LIGHT

by Wayne Filichowski

LED photoelectrics: how they work, how to specify them and what they can do in computerized control systems

Computer networks have made it on the production floor. Like LEDs in photoelectric sensors, microprocessor chips in systems ranging from specialized hybrid machine controls to programmable controllers and minicomputers have made solid state control a reality.

While relay control circuits are still in use, computers should dominate by 1980 and will place interesting challenges on the pilot devices serving the systems they control. First, with the pressures on industry to increase productivity, entire processes will have to automated with consequent reductions in direct operator controls. This procedure will require more sophistication in the sensors used for positioning, sizing, color inspection, routing and other functions – functions previously provided by human operators. Second, the new sensors will have to interface directly with control computers' I/O circuitry, a task that requires direct compatibility with various power bus voltages, self-contained amplifiers to eliminate intermediate amplifier stages, light or dark signal availability and high-noise-immune logic outputs like those provided by open-collector power transistors.

Advances in solid state technology have provided a standardized line of computer hardware and software for control-system designers. But the reliability of the production-floor systems those designers create hinges for the most part on the systems' process inputs.

One class of such inputs comes from LED photoelectric scanners, which now replace incandescent-equipped photoelectrics in many applications. LED photoelectric devices for controlling motion – as opposed to optical code readers and photocells for light detection (street lighting) or light measurement (camera metering) can perform all of the functions of mechanical switches, including stop, start, detect, limit, count, inspect, sort, measure, position, sequence, protect, monitor, identify and control. LED photoelectrics can also do many things a mechanical switch or a machine operator cannot. They can react to printed marks, liquids, two-dimensional shapes and surfaces, smoke, turbidity, reflections and colors. Their sensing areas can be focused to almost a point, or fall anywhere along a light beam that extends many feet. Sensing can also extend around corners with the aid of mirrors or to deep within a machine with the help of fiber optics.

Among non-contact, non-destructive sensors, photoelectrics are superior in that they need not be intimately close to the sensed object, as most inductive, capacitive, rf, ultrasonic and magnetic-pickup-type proximity devices must. And the sensed object doesn't have to be a special material, nor must the system generally be delicately tuned to a physical property such as weight or speed. The only requirement is that the object be able to block, attenuate or reflect a light beam, or act as a detectable light source itself.

Photoelectric systems have evolved in both technology and equipment. Early photoelectric controls relied upon an incandescent lamp as the light source and a phototube as the detector, and such equipment tended to be bulky, inefficient, sensitive to shock and vibration, and relatively costly. The advent of photosensitive semiconductors in the early

Wayne Filichowski *is manager of market development at Warner Electric Brake & Clutch Co., Beloit, WI.*

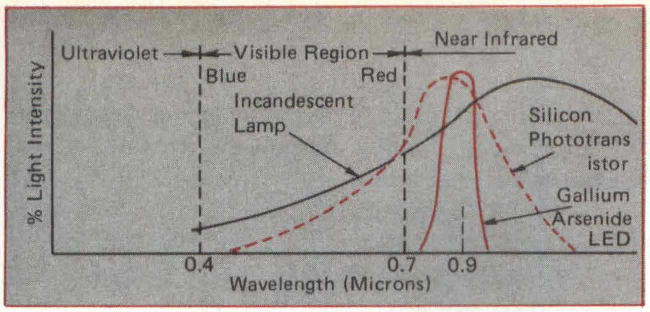

Fig 1 Intensity of the gallium arsenide LEDs used in most photoelectric control systems peaks at 0.9 nm – close to silicon phototransistors' peak sensitivity wavelength of 0.85 nm.

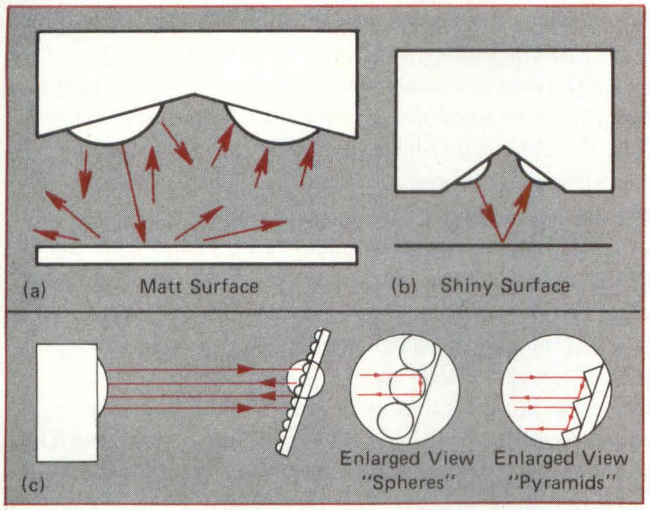

Fig 2 (a) Diffuse reflection system allows increased ranges between a sender/receiver and a target. (b) Specular reflection setup requires that a scanned object remain at a relatively constant distance from the sender/receiver. (c) Retroreflection system accepts light at any angle of incidence and returns it over the same path.

1960s had a major impact on photoelectrics, and most systems configured since then have incorporated phototransistors as light detectors. The phototransistor allowed smaller, more efficient and more reliable photoelectric controls. But in those controls, the inefficient incandescent lamp still supplied the light.

The LED now brings the light source up to date with the sensor, and it should supplant the incandescent bulb in the majority of future applications. Photoelectrics with phototransistors as their sensors and LEDs as their light sources are all-solid-state and carry all of the advantages and capabilities that such electronics can bring.

system components

Every photoelectric system consists of a light source, a light sensor, an amplifier and an output. These subsystems can be separately housed, or partially or completely combined into a single package. The light source provides a light beam, which is then broken or completed by an object the system must detect. The light sensor then picks up the light beam or the absence of it and transmits the information to the amplifier, which steps up and transmits the signal to the output. That subsystem provides the desired control, counting or notification function.

Light sources. Unlike visible incandescent sources, which have relatively short lifetimes and can fail if subjected to excessive vibration, the LEDs used in photoelectric controls output infrared light. They have lifetimes longer than 100,000 hrs and are relatively immune to vibration. The gallium arsenide LEDs most often used in photoelectric control systems are the most intense units available. Their 0.9-nm wavelength lies very close to the wavelength (Fig 1) to which the most-often-used sensor – the silicon phototransistor – is most sensitive (0.85 nm).

Invisibility may appear to be a disadvantage in aligning an LED photoelectric system, but it is an advantage for most applications once the system is in operation. Photoelectric controls become less noticeable and therefore are less prone to tampering – people don't wave their hands in a beam to see the reaction or defeat a control's purpose.

Unlike incandescent sources, a sample of LEDs is rated by how long it takes for half of them to reach a point where light emission intensity is only half its original value. Because an LED can operate at a variety of voltages, currents and temperatures, manufacturers can't quote a simple, single LED life value. But basically, the harder an LED is worked (in terms of output intensity), the shorter its life. An LED also loses its intensity non-uniformly – it dims fastest in the early stages of its life before settling down to a more gradual loss. Dimming to half intensity, therefore, does not signal that its life is necessarily half over.

Most photoelectric control systems pulse their LEDs to attain greater intensity. A fringe benefit of this type of operation lets a system simultaneously pulse its sensors to receive only the type of signal transmitted by the source. Thus external light sources don't register as legitimate signals, as is sometimes the case with other types of photoelectric systems.

Because LED-type photoelectrics are pulsed, their response time (2-5 ms) is somewhat lower than that of incandescent designs (50 μs), although the difference for most applications is immaterial. The delayed response results from the sensor's need to integrate – or count – 6-12 con-

Back To Basics

A light emitting diode (LED) is a semiconductor chip that emits light energy when stimulated by a low-voltage dc current. It is much more efficient than an incandescent bulb, because its light output is not created by a superheated filament (which consumes and dissipates large amounts of energy), but by electrons jumping from higher to lower energy states at the semiconductor's junction. Depending upon the LED's component elements, the color of its emitted light can range from ultraviolet, through the visible spectrum and into the infrared. The more efficient and intense types are those at the red end of the spectrum; thus most small calculator and digital watch LED displays are red.

One type of light source that has received considerable publicity lately is the more expensive laser design, which emits a very intense, narrow beam of coherent light. The LEDs used in current photoelectric controls are not lasers; their light must be focused with lenses in the same manner as light from an incandescent lamp.

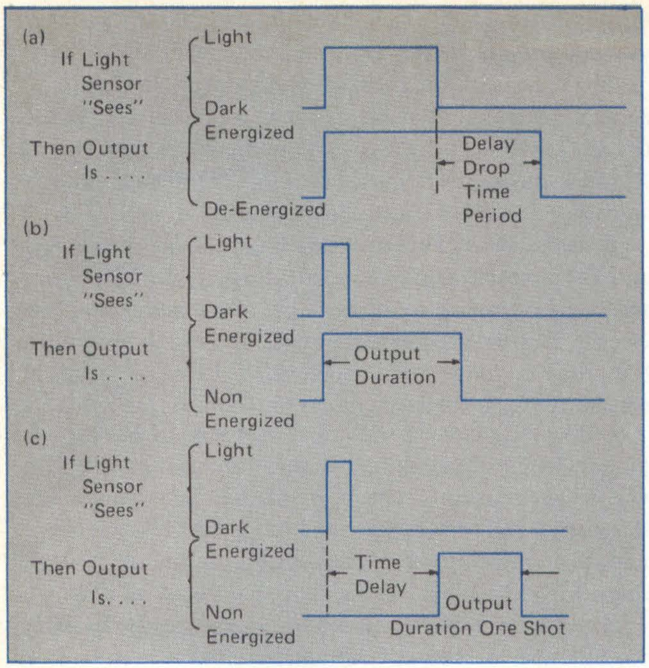

Fig 3 (a) Retriggerable time delay energizes an output when the light beam is completed but delays the output for a preset time when the light beam is broken. (b) One-shot timing function activates an output when the beam is completed and keeps the output activated for a preset time regardless of the light sensor's subsequent condition. (c) Delayed one-shot operates like a normal one-shot but waits for a preset time before activating its output.

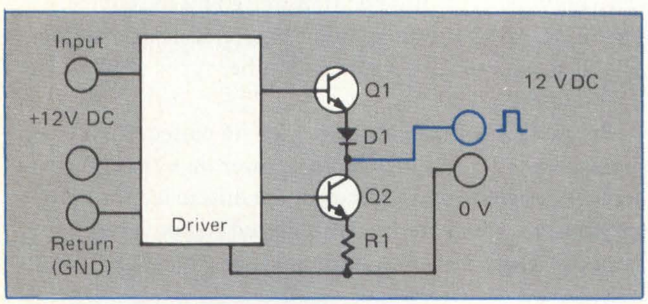

Fig 4 Logic output allows a photoelectric scanner to interface directly with most digital equipment. It pulses its 12-Vdc output when signalled by the scanner's amplifier.

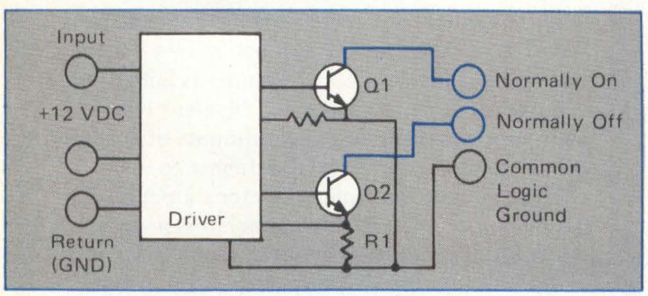

Fig 5 Switch-type logic output serves control systems that don't respond to 12-V pulses; it operates like a single-pole-double-throw relay and typically outputs 0.06 A @ 30 Vdc.

secutive pulses before reaching a threshold level that signals the output to perform some action. Because of the resulting delay, pulsed LED photoelectrics are generally not recommended for ultra-high speed applications in which the interval between operations (including dropout times) is shorter than 10 ms – that is, for applications of more than 600 operations/sec. But few object-detecting applications require responses anywhere near this level.

Light sensors. The simplest type of light sensor, the cadmium sulfide *photocell*, undergoes a change in its electrical characteristics when subjected to light. With a response time longer than that of other types of light sensors, it has color sensitivities that suit it to high-sensitivity applications. The solid state *photodiode* provides a much faster response than the photocell, although it is somewhat less sensitive to light. A compromise between these two devices, the *phototransistor* provides greater sensitivity to light than the photodiode but can detect very fast pulses of light.

Because photoelectric sensing systems require a surface or a mass to react to, you must understand the behavior of light when it strikes various media. In a *thru beam* or "two-part" system, a detected object must block most of the beam. Some manufacturers provide aperture attachments that reduce the beam size to narrow slits or cylinders of light for operation with small objects. In a *diffuse reflection* system (Fig 2a), using higher-intensity LEDs makes possible increased ranges between the sender/receiver combination and the target, the sending and receiving paths are generally separate. Distance from the target varies with original light signal strength, the surface properties of the target and the angle between the sender and receiver. In a *specular reflection* system (Fig 2b), a light beam strikes a shiny surface and reflects at an angle equal in magnitude to its angle of incidence. Scanners that utilize this method house the sender and receiver in one head, and the scanned object must lie at a relatively constant distance from the head for the light beam to reflect properly. This method can detect the presence or absence of glossy objects and can also detect contrasts between colors and surface qualities. Finally, in a *retroreflection* system (Fig 2c), a light beam strikes a reflector that directs it back the way it came, regardless of the angle of incidence. Retroreflective mirrors are usually plastic, with reflective surfaces formed from three-dimensional "pyramids" or "spheres."

Amplifiers. Most amplifiers in photoelectric scanning systems allow time-delay processing, by which amplifier output activation lags light-sensor activation. Various time delays allow a wide variety of applications. In conveyor-jam detection, for example, a system must determine when several units "jam up," or bunch together on a conveyor system. Under normal circumstances, the units pass through the light beam at a uniform rate, and with this action, the light beam is alternately broken and completed. When the units jam up, however, the light beam is broken and remains broken as long as the jam is present.

A *retriggerable time delay* (Fig 3a) can detect such a jam. When the light beam is completed, the output immediately energizes. When the light beam is broken, however, a delay occurs before the output follows the light sensor and drops out. Thus, when the light beam is completed, the output follows the light sensor and energizes. When the light beam is broken, the output remains energized for the pre-set period of the time delay. If at any time during this period the light beam is again completed, the timer resets, and the timing function cancels and begins again without de-energizing the output. As long as the light beam is again completed some time during the delay, the output remains energized. Otherwise, the output de-energizes and the timer "times out."

Cont'd p. 38

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CIRCLE 30

In conveyor-jam detection, when the conveyor starts, the light beam is completed, the timer starts and the output energizes. When an object passes through the light beam and interrupts it, the time delay begins, and the light sensor sees dark although the output device remains energized. When the object passes completely through the light beam, and the light sensor again sees light, the entire cycle is reset. If at any time, however, the objects jam up, the timer times out and the output de-energizes. The deactivated output can then activate an alarm or other function.

Sometimes an object passes very quickly through a light beam. Even though the light sensor can respond to it and the amplifier can process the resulting signal, that signal may occur too quickly to operate the output device. To register the swift action of the beam interruption, the system must have some means of expanding the normal on/off output. A *one-shot timing function* (Fig 3b) can perform this task. The one-shot output is a non-retriggerable pulse with variable duration. Like the delay drop timing function, the one-shot timer activates an output device immediately upon beam completion and begins its timing cycle. Unlike that function, however, the one-shot's output remains energized for the timer period, regardless of the condition and status of the light sensor. When the timing period expires, the output de-energizes and the light sensor can again trigger the amplifier when its light beam is completed. Whereas a delay drop timer can reset without changing the status of the output device, a one-shot timer can only reset by completing one timing cycle at a time.

This ability finds many applications. In a fast-counting situation, for example, a one-shot timer can extend the pulse as required for the counting device or other form of automation. Similarly, if a system must count slow-moving objects, a one-shot timer can shorten the output signal if its timing period measures less than the object's speed.

An amplifier can also perform other functions in addition to amplification and signal delay. It can activate an output

A delayed one-shot (Fig 3c) waits a preset period before it begins timing. In this mode of operation, the timer produces a non-retriggerable output pulse just like the one created by a one-shot timer but delayed by an adjustable time period. The entire timing function is non-retriggerable and finds uses in applications that require a delay between beam completion or interruption and output operation.

LIGHT TRANSMISSIBILITY	SURFACE QUALITY: SHINY	SMOOTH	DULL
TRANSPARENT	**Reflective** Two Part (Angle Mount) Target	**Reflective**	**Reflective**
T'LUCENT	**Reflective Best** Also Consider *Two Part or *Retro-Reflective	**Reflective** Also Consider *Two Part or *Retro-Reflective	**Use Reflective Scanner At Reduced Range** Also Two Part or Retro-Reflective
OPAQUE	**Reflective Or Two Part**	**Reflective, Two Part Or, Retro-Reflective**	**Two Part Or Retro-Reflective** Use Reflective Scanner At Reduced Range

*Adjustable amplifier sensitivity may greatly enhance operation

Fig 6 Extremely shiny surfaces can fool retroreflective scanners by acting as mirrors and generating false signals.

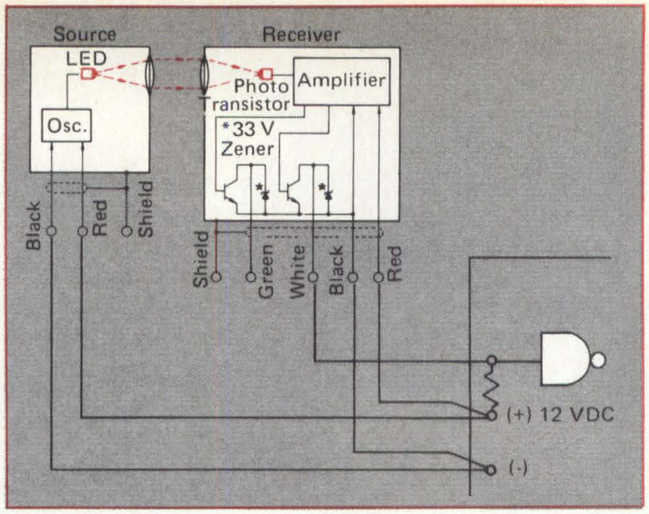

Fig 7 Warner's MCS-627 LED scanner interfaces with computers and eliminates the need for a conventional separate amplifier.

when the light sensor sees dark, rather than when it sees light – a feature useful in empty-conveyor detection. It can provide sensitivity control, which lets you specify the amount of light blockage required to register a "break" in the light beam – an ability useful in detecting translucent objects. Through an inhibit capability, it can prevent a photoelectric system from registering until an object is properly positioned. A latching capability lets it respond normally until an initial activation occurs, then keep an output energized regardless of the status of the light sensor. Finally, it can provide notification when an incandescent lamp burns out. No one amplifier has all of these features, but plug-in optional circuitry can often provide you with a system matched to your needs and application.

Outputs. While considered a separate subsystem, an output is almost always located within the amplifier. *Relays* can best handle heavy loads, but they have finite lives and respond slowly to signals – a typical unit requires 0.02 to 0.05 sec to complete a cycle. *Hybrid switches,* unlike relays, can only handle ac loads. A combination of a triac and a miniature reed relay or opto-isolator, a hybrid switch has a typical life of 10^8 operations, compared with 5×10^5 for the average relay. It can also switch faster than the relay, typically in 0.01 to 0.015 sec. But it cannot handle as heavy a current load, nor can it provide more than a single switch action.

Suited for use with computers, counters and other solid state systems, a *logic output* supplies its own low current, 12 Vdc internal power and requires no external voltages (Fig 4). Typically a "pulse output" device, a logic output usually generates a 12-V pulse when signalled by the amplifier. Because it is completely solid state, its operating life is virtually infinite. And its overall response time is approximately 5000 times faster than that of a hybrid switch, making considerations of amplifier and sensor response time necessary. Because not all electronic controls respond to a 12-V pulse, some systems require a switch-type logic output device, also termed an open collector unit (Fig 5). Rather than providing a voltage output, this unit provides a switching action similar to that of a single-pole-double-throw relay. Acting as a low-voltage, low-current switch (typically 0.06 A, 30 Vdc), this type of output device lets you switch your own voltages for electronic load devices. *Cont'd p. 40*


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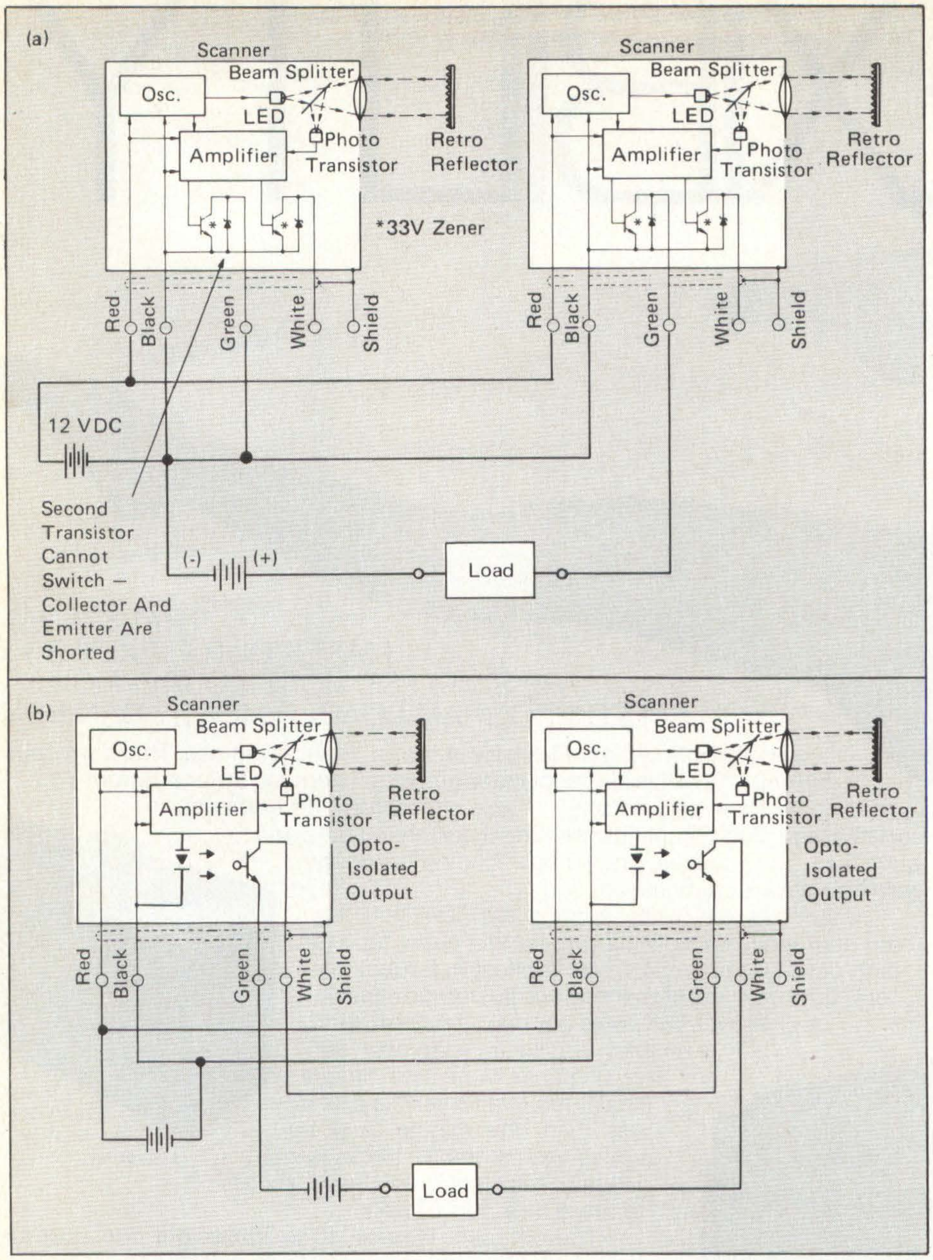

Fig 8 (a) Connected together for AND or OR operation, two scanners' output switching transistors remain unisolated. (b) Opto-isolated output for each scanner provides the required electrical isolation.

system considerations

When selecting a photoelectric scanner system, consider these key factors:

★ Target size. Does the target's size dictate a maximum allowable beam diameter or even the maximum dimensions of the scanner package itself? Counting cartons passing on a conveyor requires using the entire target. Orienting parts on an automatic assembly machine may be a matter of detecting a small hole in the correct position. In general, moving the target surface closer to the system's lens(es) allows a corresponding decrease in target size. And decreasing the system's amplifier sensitivity lets you scan smaller targets with retroreflective and two-part scanner configurations. The converse is true with reflective proximity and reflective fixed-focal-distance configurations. Surface reflectivity can also affect target sizes on all reflective scanners – a reflective scanner may react better to a shiny, smaller target than a dull, larger one.

★ Target speed. Assuming a target has sufficient size and/or reflectivity to significantly interfere with a beam, it must do this long enough for the scanner's amplifier to respond. For most applications this amplifier response time is unimportant, because the beam make or break period lasts more than one second. But applications like high-speed counting may have amplifier response as a limiting factor.

★ Target composition (Fig 6). Translucent targets can be detected by beam break methods if the sender/receiver package does not have too much penetration power or the amplifier has built-in adjustable sensitivity that you can reduce. With extremely shiny surfaces, exercise caution when using retroreflective scanners because the target itself may act as a mirror and produce false signals. For such surfaces a two-part system is more desirable than a retroreflective unit.

★ Sensing range. The simplest and most conservative method of assigning a distance rating to LED photoelectric controls is to specify the maximum distance recommended with relatively clean optics *and* a free air space, and with the units subjected to the worst case conditions of ambient temperature and voltage.

Additional important scanner-selection factors include ambient contaminants, ambient light conditions, light source life and wiring access.

Once you have selected a scanner, consider the type of logic, timing or output signals that must serve that scanner's load. We'll focus here on logic-level switching circuits, which have grown in use as computers and programmable controllers find more in-plant applications and pressures from public interest groups to reduce safety hazards increase. With such interface circuitry, a machine is controlled from one low-voltage (usually 12 Vdc) power supply. Fig 7 shows how Warner's MCS-627 scanner interfaces with a computer and eliminates the need for a conventional separate amplifier.

In solid state transistor logic circuits, the output switching transistor usually connects directly to an internal power supply and is thus not isolated. This characteristic can cause problems when two or more scanners are connected together for AND or OR operation (Fig 8a). A remedy for this problem involves using an isolated output for each scanner. Each output consists of an LED and a phototransistor. Light from the LED goes through a gap to the input of the phototransistor, and the separation between the two components provides electrical isolation. Fig 8b shows the resulting modified circuit. ♦

Who

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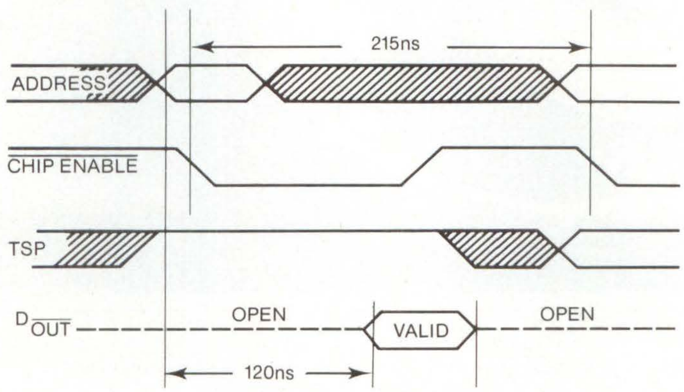

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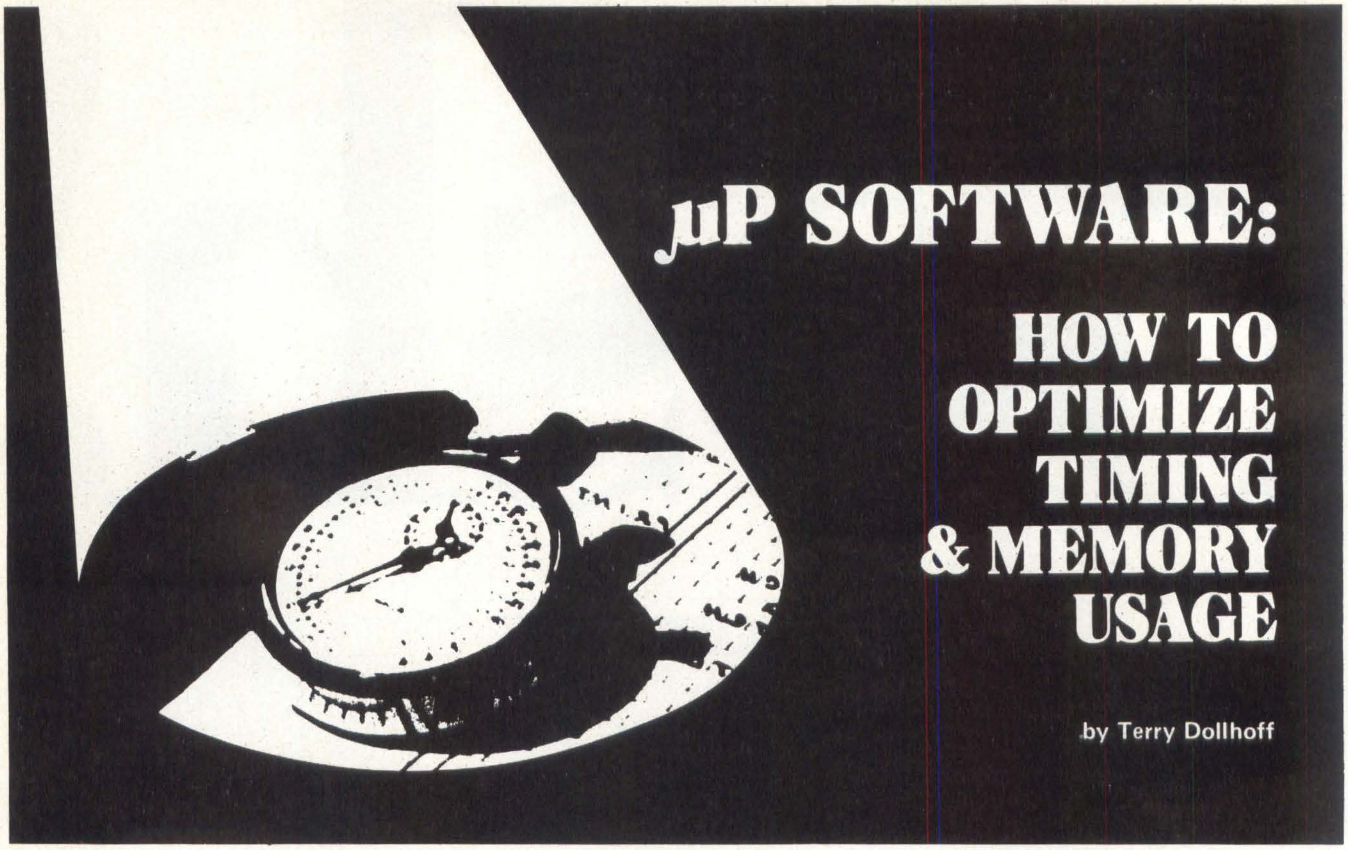
PART FIVE: TECHNIQUES FOR NSC'S SC/MP AND ELECTRONIC ARRAYS' EA9002



µP SOFTWARE: HOW TO OPTIMIZE TIMING & MEMORY USAGE

by Terry Dollhoff

This final series installment covers two typical low-end microprocessors: the National Semiconductor SC/MP and the newer Electronic Arrays EA9002. In most low-end, controller applications, the microprocessor rides herd on some piece of equipment, usually a very simple piece. For example, microprocessors now control point-of-sale terminals, gas pumps, microwave ovens, telephone PBXs and even a hi-fi record changer. What separates a controller from any other microprocessor? Cost – speed is not terribly important, but total system cost is crucial and minimization of parts cost is the prime goal.

The SC/MP and the EA9002 are simpler than any of the microprocessors I've discussed so far. For example, neither machine has any 3-byte instructions; all instructions are either one or two bytes long. For quite some time this low end of the market has been dominated by the 4-bit microprocessors, but I think that this dominance is ending. There are few, if any, applications where the total system cost for an 8-bit machine is not competitive with a 4-bit system's. Because a 4-bit machine is awkward to program and offers no significant advantage, why use it?

SC/MP system architecture

The SC/MP (Simple Cost-effective MicroProcessor) is a single-accumulator, 8-bit microprocessor (Fig 1). Its accumulator serves all arithmetic operations, and all memory data enters or leaves the processor through this register. In addition to the accumulator, the SC/MP has four 16-bit pointer registers and an accumulator extension, which serves as temporary storage for the accumulator and can be used as a source operand for arithmetic operations. One of the pointer registers serves as a program counter (PTR O); the others may be used by the program.

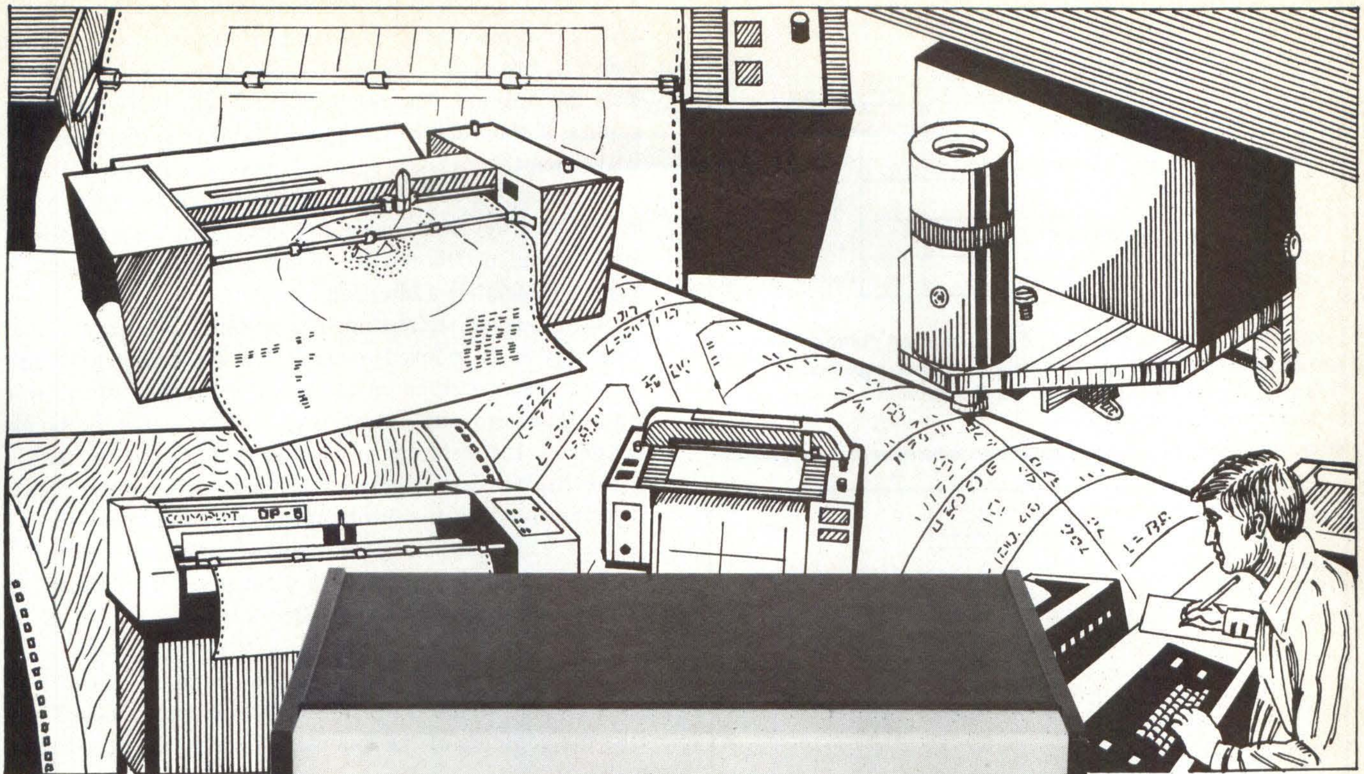
SC/MP is a page addressed machine; all addresses are specified within a page (Fig 2). If your system contains more than one page – many applications don't – you must be careful to address memory properly. Whenever the program counter is incremented to fetch the next instruction, only the lower 12 bits are affected; the page remains the same. Therefore, if you place a no-op in memory location OFFF (hexadecimal) and branch to that no-op, the instruction the machine executes after the no-op will be the one at address 0000 (not 1000 as you might logically expect). The manufacturer's documentation refers to this phenomenon as "wrap around" addressing and further says that it is provided for "maximum programming flexibility." It's difficult, if not impossible, to foresee any time that this capability would be desirable from a software viewpoint, but I can see how it simplifies the hardware design. The microprocessor's instruction set appears in Fig 3.

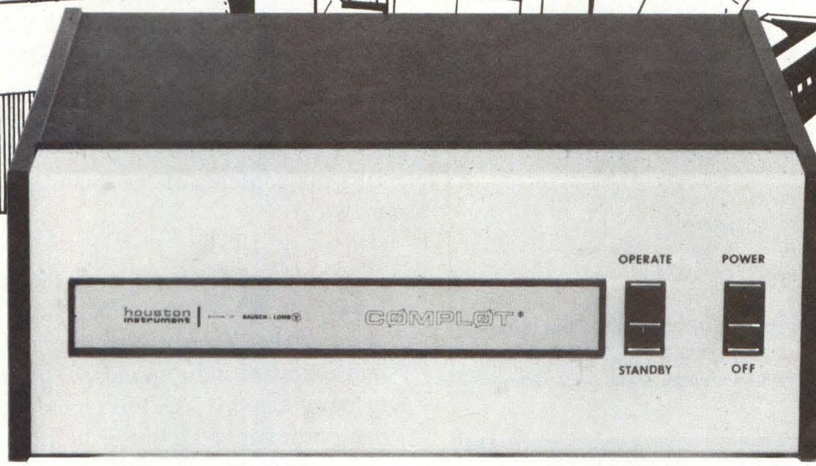
One of the SC/MP's features is its repertoire of simple yet flexible addressing modes:

★ Immediate addressing. The operand lies in the memory location following the instruction opcode. For example, this instruction will exclusive OR the accumulator with 35 (hexadecimal):

```
XRI   X'35          ; exclusive or acc with 35
```

Terry Dollhoff *is director of computer science at Acuity Systems, Inc., Reston, VA.*





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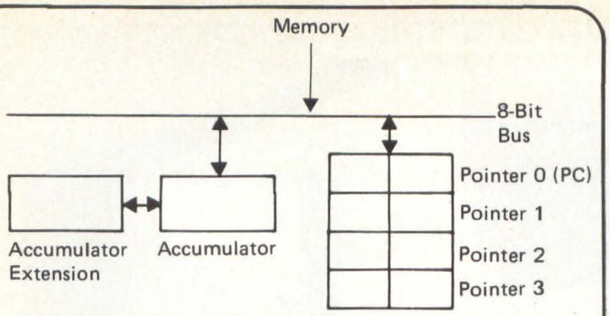


Fig 1 A single-accumulator, 8-bit processor, National Semiconductor's SC/MP has four 16-bit pointer registers and an accumulator extension, which can function as a source operand for arithmetic operations.

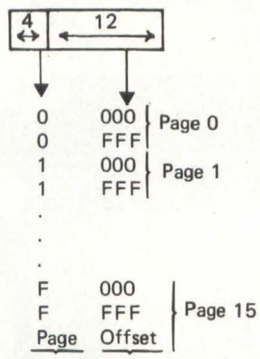


Fig 2 The SC/MP is a page addressed unit; when the microprocessor's program counter is incremented to fetch the next instruction, only the lower 12 bits change — the page remains the same.

★ Indexed addressing. The operand address results from adding a displacement (-128 to +127) to one of the pointer registers; this sum is termed the effective address and selects the operand. The restriction on page addressing still applies; if the pointer contains FFO and the displacement is 10, then the effective address is 000 (not 1000).

A special case of indexed addressing occurs when you use Pointer Register Zero (program counter). In this case, the displacement occurs relative to the program counter and is termed PC-relative addressing.

★ Auto indexed addressing. The operand is generated the same way as an indexed operand, but the designated pointer register is incremented or decremented. If the displacement is less than zero, the microprocessor decrements the pointer register by the displacement before fetching the operand. If the displacement is greater than zero, the pointer register is incremented by the displacement after the operand is fetched. This instruction loads the accumulator with the contents of the memory location addressed by Pointer One and then adds four to Pointer One:

```
LD    @4(P1)        ; A=M(P1), P1=P1+4
```

★ Extension register addressing. The operand is the contents of the extension register. This instruction logically ORs the contents of the extension register with the accumulator:

```
ORE                 ; A=A or E
```

A unique SC/MP feature is the microprocessor's special I/O capability. It handles normal I/O as external memory references; that is, external hardware detects a reference to certain addresses and responds with peripheral data. Termed memory mapped I/O, this technique is commonly used for microprocessor I/O. But in addition to it, the SC/MP pro-

Cont'd p. 50

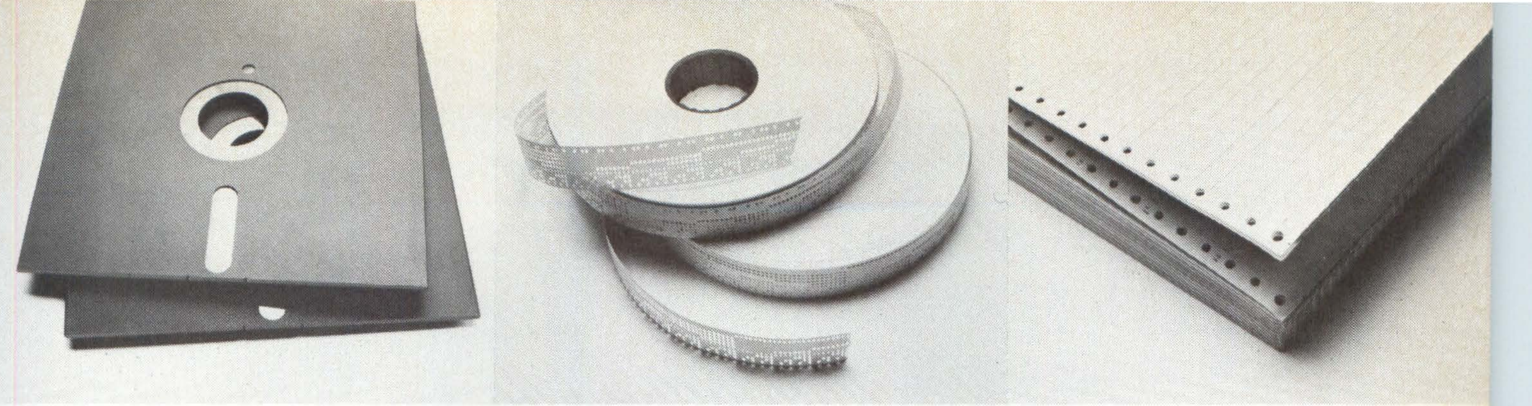
National Semiconductor SC/MP Instruction Set

	Immediate	Extension Register	Relative	Indexed/Auto Indexed PTR1	PTR2	PTR3	
ADD	F4	70	F0	F1/F5	F2/F6	F3/F7	add to accumulator (with CY)
AND	D4	50	D0	D1/D5	D2/D6	D3/D7	and with accumulator
CAD	FC	78	F8	F9/FD	FA/FE	FB/FF	complement & add to acc (with CY)
DAD	EC	68	E8	E9/ED	EA/EE	EB/EF	decimal add to acc (with CY)
DLD	—	—	B8	B9/—	BA/—	BB/—	dec & load acc (memory is dec)
ILD	—	—	A8	A9/—	AA/—	AB/—	inc & load acc (memory is inc)
JMP	—	—	90	91/—	92/—	93/—	jump to effective address
JNZ	—	—	9C	9D/—	9E/—	9F/—	jump if acc not zero
JP	—	—	94	95/—	96/—	97/—	jump if acc positive
JZ	—	—	98	99/—	9A/—	9B/—	jump if acc zero
LD	C4	40	C0	C1/C5	C2/C6	C3/C7	load accumulator
OR	DC	58	D8	D9/DD	DA/DE	DB/DF	or with accumulator
ST	—	—	C8	C9/CD	CA/CE	CB/CF	store accumulator
XOR	E4	60	E0	E1/E5	E2/E6	E3/E7	exclusive-or with accumulator

	PC	PTR1	PTR2	PTR3	
XPAL	30	31	32	33	exchange acc and lower byte of pointer
XPAH	34	35	36	37	exchange acc and higher byte of pointer
XPPC	—	3D	3E	3F	exchange pc(ptr0) with pointer

CAS	07	copy acc to status	NOP	08	no operation
CCL	02	clear carry	RR	1E	rotate right, zero fill
CSA	06	copy status to acc	RRL	1F	rotate right, CY fill
DLY	8F	delay 13+2*acc+514*disp.	SCL	03	set carry
DINT	04	disable interrupt	SIO	19	shift ext. right to I/O
HALT	00	halt	SR	1C	shift acc right, zero fill
IEN	05	enable interrupt	SRL	1D	shift acc right, CY fill
			XAE	01	exchange acc and ext

Fig 3 Clip and save this summary of the SC/MP instruction set.



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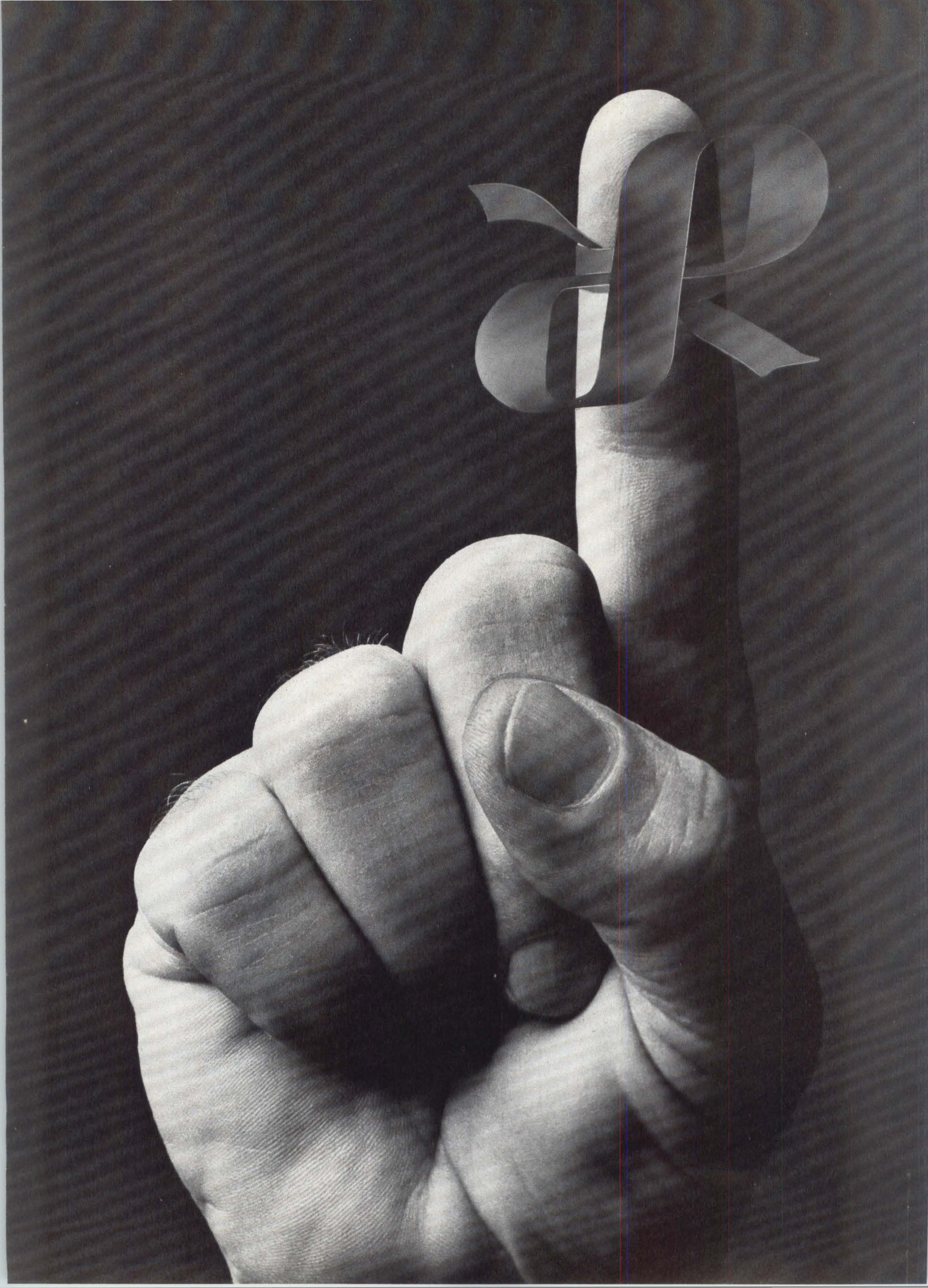

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CIRCLE 35

vides three other types of special I/O:

★ Flag bits. Three flag bits in the status register go to the outside world: the program places desired data in the status register bits that correspond to the flags and sets the external pins accordingly. These flags can be useful control lines.

★ Status bits. External hardware can set or clear two bits; their status appears in the status register. The first status line (Sense A) is also the interrupt line if interrupts are software-enabled.

★ Serial I/O. A serial input (SIN) and a serial output (SOUT) pin are controlled by the microprocessor's software; a special shift instruction controls these lines. This Shift I/O (SIO) instruction shifts the extension register right one position; then the vacated bit is filled by the current setting of SIN. The bit shifted out then goes to the SOUT line (Fig 4).

using the SC/MP I/O capability

SC/MP's special I/O is ideally suited to a serial asynchronous interface; SIN serves as the receive data line and SOUT as the send data line. A typical asynchronous communication (Fig 5) consists of a start bit, data bits and a stop bit. In full-duplex mode, any input must go back to the terminal to complete the communication; SIN and SOUT can implement this capability. All you need is a way to control the timing. The SC/MP's DLY instruction can create program delays and thereby control the I/O timing; it delays processing for a variable amount of time. The total instruction time comes from this formula:

DELAY=13+2*accumulator+514*displacement

If you want to determine the best values for the accumulator and displacement, use

Displacement = (DELAY-13)/514 (truncated to nearest integer)

Accumulator = (DELAY-13-514*displacement)/2

These equations produce a delay that measures within one microcycle of the desired value. The length of a microcycle depends on the system clock frequency, but $2\mu s$ is typical. The delays you'll need are determined by the baud rate; if the time between bits is B, you need a delay of B and B/2. Assume that the baud rate is 300. In this case, $B=1/300sec=3333\mu s$. If the clock cycle time is $2\mu s$, you must create a delay of 1666 and 833 μs. Using the formulas, you obtain

Displacement = (1666-13)/514 = 3

Accumulator = (1666-13-514*3)/2=55

and

Displacement = (833-13)/514 = 1

Accumulator = (833-13-514)/2 = 153

The routine in Listing 1 performs the terminal-handling chore. It saves the input character in P1 (lower) and uses P1 (upper) as a flag to indicate when all eight data bits have arrived. At the end of the routine, the character goes to the accumulator.

Listing 1 has several features you should note. First, it clears the carry before the add, because all additions occur with carry. Second, it uses the pointer as temporary storage. (Although the pointers often hold addresses, they can also hold temporary data – especially when the extension is busy.) Finally, the 1-bit delay is off. We calculated this delay properly but didn't take into account the time required to travel through the loop. To obtain a more accurate timing, subtract the time required for the loop (instructions LOOPS to LOOPE – it amounts to 125 cycles, or 7.5% of the delay. At higher baud rates (2400), this time would introduce a 30% error, and the routine wouldn't work. The correct computation for the second delay is

Displacement = (1666-13-125)/514 = 2

Accumulator = (1666-13-125-514*2)/2 = 250

SC/MP subroutine interface

The SC/MP has no special instructions for calling subroutines; you must load the routine address into one of the pointer registers and then branch to the subroutine. For example, this sequence calls subroutine XXX:

```
        LDI   H(RETN)        ; set P3=return
        XPAH 3
        LDI   L(RETN)
        XPAL 3
        JMP   XXX            ; call subroutine
XXX
```

The sequence has one drawback: XXX must lie within the same page as the call because a JMP relative is used. I'll examine ways around this limitation later. In any case, if subroutine XXX is called this way, control can return from the subroutine with

```
        XPPC  3              ; exchange PC and P3
```

If you want to make nested calls, this approach isn't very efficient. An alternate approach is to develop a general call-and-return subroutine. The first step is to assign two pointer registers:

P1 – address of a pushdown stack in RAM; contains the next usable location on the stack

P2 – address of subroutine call/return processor

The pushdown stack resembles the one in the 8080 or 6800. To push an entry on the stack, use

```
        ST    @1(P1)         ; push acc, increment stack
                             ; pointer
```

To pop an item off the stack, use

```
        LD    @-1(P1)        ; pop acc after stack pointer
                             ; decrement
```

In this increasing stack pointer, the stack builds upward in memory instead of downward (as in the 8080 or 6800). The advantage of building the stack upward is that P1 always points to the next usable location, so it can be used as a temporary storage. If you build the stack downward, P1 points to the top entry on the stack. Now to call a subroutine, code

```
        LDI   n              ; accumulator = subroutine
                             ; number
        XPPC  2              ; call the caller
```

The n signifies the subroutine number. Achieve the subroutine return by setting the accumulator to zero and again calling the call/return processor; the return is thus

```
        LDI   0              ; perform a return
        XPPC  2              ; call the returner
```

Because only the number of the subroutine appears, you must maintain a table of subroutine addresses. To simplify programming, use only even numbers to signify subroutines; in that case a typical subroutine table might appear as

```
TAB     .ADDR   RETN         ; routine RETN
        .ADDR   ROUT1        ; user routine (2)
        .ADDR   ROUT2        ; user routine (4)

        .ADDR   ROUTn        ; user routine (n)
```

The subroutine call processor appears in Listing 2.

Listing 1. Terminal-Handler Routine

```
WAIT    LDI  1        ; wait for start bit
        XAE           ; E=0000 0001
        SIO           ; E=i000 0000, SOUT=1
        LDE           ; A=E
        JNZ  WAIT     ; wait till E=O
        LDI  153      ; wait 1/2 bit time
        DLY  1
        LDI  9        ; P1 (H)=loop count
LOOPS   XPAH          ; update loop count
        SIO           ; echo last bit
        LDE           ; A (LSB)=next bit
        RRL           ; CY=bit
        XPAL 1        ; A=character
        RRL           ; put bit in character
        XPAL 1        ; put back character
        LDI  55       ; delay one bit
        DLY  3
        SIO           ; sample bit (put in right of E)
        SIO
        SIO
        SIO
        SIO
        SIO
        SIO
        XPAH 1        ; get flag
        CCL           ; clear carry
        ADI  -1       ; decrement count
LOOPE   JNZ  LOOPS    ; continue till no carry
        SIO           ; send stop bit
        XAPL 1        ; A=character
```

Whenever you enable an interrupt, the address of the interrupt processing subroutine must lie in P3, because an interrupt initiates this instruction:

```
XPPC 3            ; interrupt
```

At the start of the user interrupt routine, you must also save the status register if you wish to modify it. Using the stack I've developed, you can save it this way:

```
ST   @1(P1)       ; save A
CSA               ; A=status
ST   @1(P1)       ; save status
```

At the end of the interrupt routine, reset the status and accumulator this way:

```
LD   @-1(P1)      ; A=status
CAS               ; status = A
LD   @-1(P1)      ; reset A
XPPC 3            ; return to interrupted code
```

speeding table lookup

Last month I discussed the Z80, which has a unique set of instructions for finding data in tables, and I indicated that still faster ways exist to perform that function. This month I'll further investigate table lookup and offer some suggestions for speeding your table manipulations.

The basic problem is to find a certain item within a table. As a simple example, assume that you must convert a decimal digit into the appropriate code so you can display that digit on a 7-segment display. One approach is to create a table that contains the digit and 7-segment equivalent. To make the problem more interesting, assume you receive the digit in ASCII instead of binary. The table might appear as

```
TAB  '0',A0
     '1',A1
     .
     '9',A9
```

Assume that A0 to A9 are the appropriate constants that indicate the digit's 7-segment equivalent. A brute-force approach to the problem is to search the table until you locate the desired digit and then load the 7-segment data; the Z80 compare and increment instruction does just that. On the other hand, you can simply calculate the position within the the table; the first entry is ASCII '0' and the last is '9'. Because '0' to '9' are sequential in the coding sequence, this formula provides the location of the 7-segment equivalent:

TABLE LOCATION = TAB + (input - '0')*2 + 1

This SC/MP sequence performs the calculation:

```
CCL               ; clear carry
CAI  '0'          ; subtract ASCII zero
XAE               ; set A=E
LDE
ADE               ; A=A+E=2*A
ADI  L(TAB)+1     ; increment and add TAB
XPAL 3            ; put address in P3
LDI  H(TAB)
XPAL 3
LD   (P3)         ; A= translated value
```

You can make one obvious improvement on this program. Because you never reference the character in the table,

Listing 2. Subroutine Call Processor

```
CALL    CCL            ; clear carry
        JZ    RETN     ; if A=0, return
        XAE            ; save A in E
        XPAH  2        ; stack call address
        ST    @1(P1)
        XPAL  2
        ST    @1(P1)
        LDI   L(TAB)   ; set P2=table address
        ADE
        XPAL  2
        LDI   H(TAB)
        ADI   0        ; add in carry from lower byte
        XPAH  2
        LD    @1(P2)   ; set P3=routine address
        XPAH  3
        LD    (P2)
        XPAL  3
        JMP   GO       ; go to routine
RETN    ILD   @-1(P1)  ; get call address + 1
        XPAL  3
        LD    @-1(P1)
        XPAH  3
GO      XPAH  0        ; reset P2
        XPAH  2
        LDI   L(CALL)
        XPAL  2
        XPPC  3        ; call or return
```

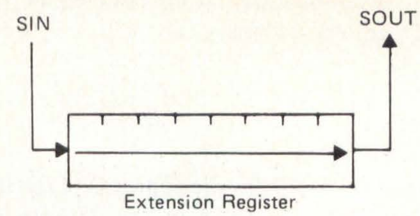


Fig 4 A Shift I/O instruction in the SC/MP controls the microprocessor's serial input (SIN) and serial output (SOUT) pins. The instruction shifts the extension register right one position; then the vacated bit is filled by the current setting of SIN. The bit shifted out goes to the SOUT line.

there's no reason to store it there; the table need only contain the 7-segment equivalents. Compute the table address by

TABLE LOCATION = TAB + input - '0'

The required sequence is

```
CCL             ; clear carry
CAI '0'         ; subtract zero
ADI L (TAB)     ; add table address
XPAL 3          ; put address in P3
LDI H (TAB)
XPAH 3
LD   (3)        ; load the translation
```

One last improvement remains. The second two instructions in the routine illustrate a common error in programming – they calculate a constant, an unnecessary operation because the assembler can do it for you (although you may have to indicate the value of '0' to some assemblers). You can thus replace the second two instructions by

```
ADI   L(TAB)-'0'     ; add offset
```

The technique I've just developed is termed a direct-access hash and is useful whenever you must translate codes or look up a limited number of uniquely coded items in a table. Indeed, the subroutine call-and-return processor uses a direct-access hash to store the addresses of the subroutines.

Unfortunately, the direct-access method isn't always feasible. Assume that you want to determine whether a specific SC/MP opcode is legal but doesn't belong to the general accumulator group (all opcodes in the first portion of Fig 3). Specifically, the relevant opcode list includes

07 02 06 8F, 04, 00, 05 08, 1E, 1F, 03, 19, 1C, 1D, 01, 30-33, 34-37, 3D-3F,

The input to the routine is, naturally, any possible 8-bit number. Therefore, a direct-access hash isn't possible, because the table would require 255 locations. Instead, you can compute a table location using the rightmost hex digit of the opcode. This location won't be unique because 02 and 32 are both entries in the table. Start by writing the first few entries (those that don't conflict):

0: 00	6: 06	B: –
1: 01	7: 07	C: 1C
2: 02	8: 08	D: 1D
3: 03	9: 19	E: 1E
4: 04	A: –	F: 8F
5: 05		

Now fill out the table by entering each of the remaining values in the first empty location following the one it conflicts with:

A: 1F	12: 33	16: 37
B: 30	13: 34	17: 3D
10: 31	14: 35	18: 3E
11: 32	15: 36	19: 3F

If you now look up an item in the table, you first examine the location selected by the rightmost digit of the opcode. If a match occurs, you're finished. If not, increment through the table one location at a time until you find the item or locate the end of the table. This technique, termed an open hash, can greatly speed a search program. Indeed, hash methods aren't proportional to table length; statistically you can locate an entry in a table of 10,000 items just as fast as you can locate the same entry in a table of 100 items – certainly not the case with a linear search.

I've only scratched the surface of the topic of table accessing algroithms, but I hope you can see the potential benefits. Because controllers often require table lookup procedures, these techniques deserve careful exploration if you're designing a controller.

EA9002 system architecture

A late entry in the 8-bit market, the Electronic Arrays EA9002 appeared in the third quarter of last year. It offers on-chip scratchpad and subroutine stack, so many applications will require no additional RAM – a feature that could further reduce system parts cost. Like the SC/MP, the EA9002 is a single-accumulator machine (Fig 6); its on-chip, 64-byte scratch memory holds intermediate results, and the subroutine stack holds return addresses. The general-purpose registers address memory or scratchpad; each scratchpad register has a data portion and a page address portion. The page address portion indicates what page contains the data, and the data address portion indicates the offset within the page. The EA9002 is the first microprocessor I've discussed that does not provide full 65K addressing. It has a 12-bit address bus, so addressing is restricted to 4K bytes of data. Because we're considering the machine as a potential controller, this memory should prove more than adequate.

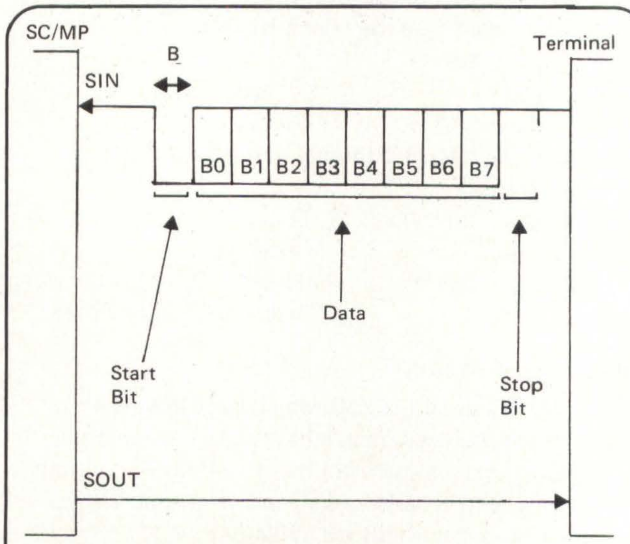


Fig 5 SC/MP's DLY instruction can create program delays and thereby control I/O timing in an asynchronous communication like this one.

The EA9002 offers these addressing modes:

★ Register. The operand lies in the general registers. If the instruction operates on the accumulator, the microprocessor uses only the lower byte of the register. Instructions that operate on the registers (e.g. decrement) manipulate all bits. An example is

```
ADD RO          ; A=A+RO(lower 8 bits)
```

which adds the lower eight bits of RO to the accumulator.

★ Register indirect. The operand lies in the memory location addressed by one of the general registers. This instruction loads the contents of the memory location addressed by R5 into the accumulator:

```
LRN R5          ; A=M(R5)
```

★ Scratchpad. The operand lies in the scratchpad memory location addressed by the lower bits of one of the general registers. This instruction adds the scratchpad memory location addressed by R7 to the accumulator:

```
ADS R7          ; A=A+MS(R7)
```

★ Page address. Most of the microprocessor's jumps determine the destination address this way. The second byte of the instruction replaces the lower eight bits of the program counter. If the following instruction lies in location 200(hex),

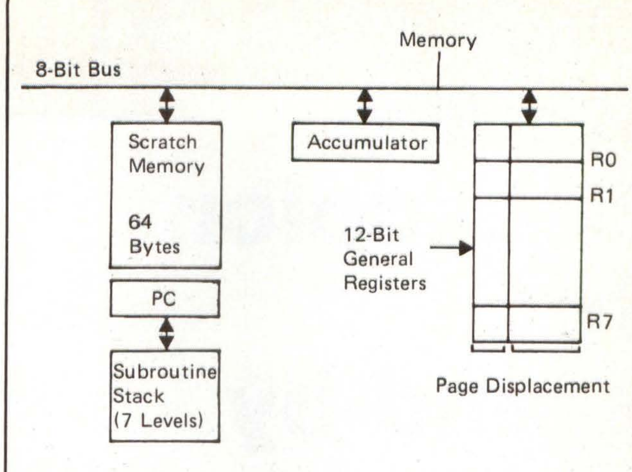


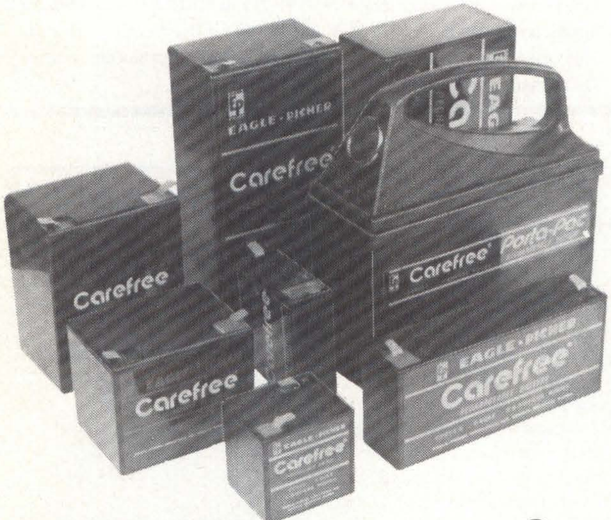
Fig 6 The 8-bit EA9002 from Electronic Arrays incorporates on-chip scratchpad and subroutine stack, features that could reduce system parts costs in many applications that require small amounts of RAM. It is the first unit discussed in this series that provides less than 65K bytes of addressing; you're restricted to 4K bytes of data.

Electronic Arrays EA90002 Instruction Set

	R0	R1	R2	R3	R4	R5	R6	R7	
ADD	80	81	82	83	84	85	86	87	add register to accumulator
ADS	C0	C1	C2	C3	C4	C5	C6	C7	add scratchpad addressed by register to accumulator
AND	90	91	92	93	94	95	96	97	and register with accumulator
CAP	48	49	4A	4B	4C	4D	4E	4F	load register (page portion) with accumulator
CAR	B0	B1	B2	B3	B4	B5	B6	B7	load register with accumulator
CMP	A8	A9	AA	AB	AC	AD	AE	AF	compare register with accumulator
CPA	08	09	0A	0B	0C	0D	0E	0F	load accumulator with register (page portion)
CRA	B8	B9	BA	BB	BC	BD	BE	BF	load accumulator with register
DCR	78	79	7A	7B	7C	7D	7E	7F	decrement register (all)
*DRJ	38	39	3A	3B	3C	3D	3E	3F	decrement register (all), jump if register (data portion) not zero
INP	50	51	52	53	54	55	56	57	load accumulator with memory specified by register
INR	70	71	72	73	74	75	76	77	increment register (all)
IOR	98	99	9A	9B	9C	9D	9E	9F	or register with accumulator
*IRJ	30	31	32	33	34	35	36	37	increment register (all), jump if register (data portion) not zero
JIN	68	69	6A	6B	6C	6D	6E	6F	jump to contents of register (all)
*LRI	60	61	62	63	64	65	66	67	load register immediate
LRN	E0	E1	E2	E3	E4	E5	E6	E7	load register with memory addressed by R0
OUT	58	59	5A	5B	5C	5D	5E	5F	store accumulator in memory specified by register
RDS	D0	D1	D2	D3	D4	D5	D6	D7	load accumulator with scratchpad addressed by register
SRN	E8	E9	EA	EB	EC	ED	EE	EF	store register in memory addressed by R0
SUB	88	89	8A	8B	8C	8D	8E	8F	subtract register from accumulator with borrow
SUS	C8	C9	CA	CB	CC	CD	CE	CF	subtract scratchpad addressed by register from acc with borrow
WRS	D8	D9	DA	DB	DC	DD	DE	DF	load scratchpad addressed by register with accumulator
XCH	40	41	42	43	44	45	46	47	exchange accumulator and register
XOR	A0	A1	A2	A3	A4	A5	A6	A7	exclusive-or register and accumulator

CLA	F6	clear accumulator	*JZE	06	jump if zero (equal)
CLB	F2	clear acc and carry	*JHC	04	jump in half carry
CLC	F0	clear carry	*JLE	07	jump if less or equal
CMA	F7	complement accumulator	*JSR	2x	jump to subroutine (x=page)
CMC	F3	complement carry	*JUN	1x	jump unconditional (x=page)
CSA	0C	load acc with status	*LAI	0D	load accumulator immediate
DAC	F5	decrement accumulator	NOP	FF	no operation
*DLY	00	no operation	RAL	F8	rotate acc left (set both carry)
DSI	0E	disable interrupts	RAR	F9	rotate acc right (set both carry)
ENI	0F	enable interrupts	RET	FE	return from subroutine
IAC	F4	increment accumulator	RLC	FA	rotate acc, carry left
*JCY	05	jump if carry (greater or equal)	RRC	RB	rotate acc, carry right
*JGT	03	jump if greater	SEB	FD	set binary mode (D=0)
*JNC	01	jump if no carry (less)	SEC	F1	set carry
*JNZ	02	jump if nonzero (not equal)	SED	FC	set decimal mode (D=1)

Fig 7 Clip and save this summary of the EA9002 instruction set. Asterisks (*) denote 2-byte instructions; the rest are 1-byte commands.



then control transfers to location 205 if the zero flag is set:

```
        JZE   5                ; jump to 5 within this page
```

★ Absolute. Two jumps (JSR and JUN) use absolute addressing. The second byte of the instruction contains the page displacement, and the lower four bits of the opcode indicate the page. These instructions allow direct access to all 4K locations in memory. This instruction calls subroutine XXX:

```
        JSR   XXX              ; call XXX, stack the return
```

The EA9002's entire instruction set appears in Fig 7. All 2-byte instructions are flagged by an *; this labeling highlights the number of single-byte instructions in the unit's repertoire.

parity computation with the EA9002

When a microprocessor computes parity, it counts the number of bits set in a byte. The most obvious method appears below; the byte to be tested lies in the accumulator (and may be destroyed), and the parity is placed in the register RO:

```
        LRI   R0,0             ; preset the parity
        LRI   R1,8             ; R1=loop counter
LOOP    RAL                    ; rotate A, next bit to carry
        JNC   CLR              ; skip the increment if no carry
        INR   RO               ; increment parity count
CLR     DRJ   LOOP             ; continue till all bits counted
```

At the end of this routine, RO contains the number of bits set in the word. To test the parity, move R0 to the accumulator and shift it into the carry. If carry is set, the byte has odd parity; if clear, it has even parity. This routine tests for odd parity:

```
        CRA   R0               ; A=parity
        RAR                    ; CY=rightmost bit
        JNC   ERR              ; jump if even parity
```

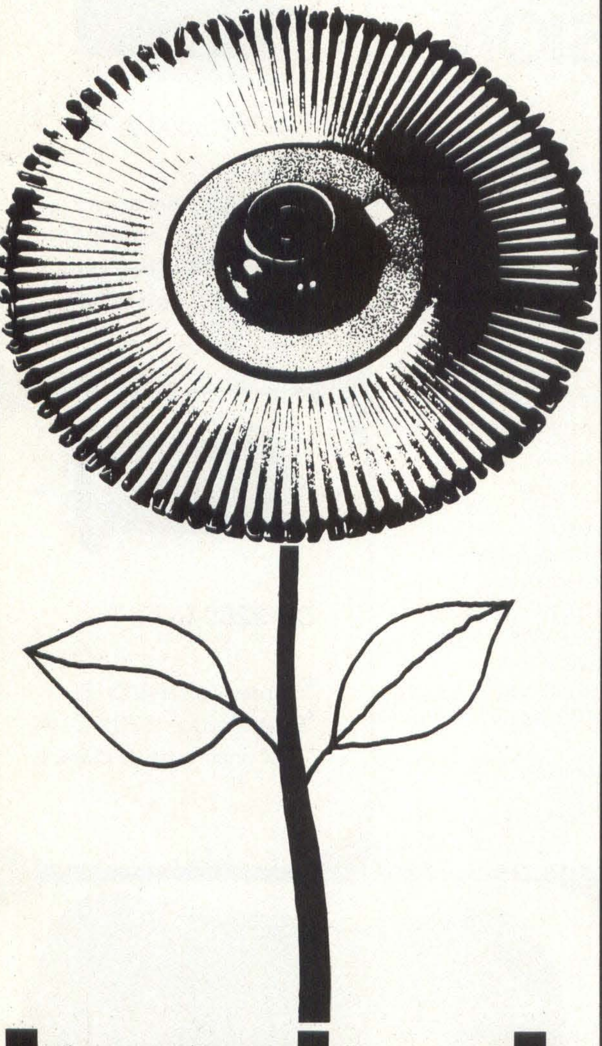
As I've stressed before, the obvious approach is not necessarily the best one. A more efficient algorithm for testing parity executes the loop only as many times as a one-bit is detected. That is, if the word is 1101 1011, the new algorithm executes the loop six times instead of eight. If the word is 0000 0010, the loop is executed one time. The key to this algorithm lies in recognizing what happens when -1 is added to the accumulator. If the accumulator's contents are nonzero and you add -1 to them, you'll create this situation:

```
   x x x .... 1 0 0 . . . 0
 + 1 1 1     1 1 1     1
 ------------------------
   x x x . . . 0 1 1 . . . 1
```

The key fact is that the rightmost one is translated into a zero, and all bits to the left of that one are left untouched. If you logically AND the result of this sum with the original number, you cancel the rightmost one and leave all other digits untouched. If the original number contains n one-digits, you can repeat this procedure n times to get a zero result. Thus, you have an algorithm for counting the number of one-bits that does not always require eight passes through the loop:

```
        LRI   R0,0             ; preset the bit count
        LRI   R1,-1            ; preset the mask
LOOP    AND   R1               ; A=A and mask
        JZE   FINI             ; if zero, finished
        INR   R0               ; count one more one
        CAR   R1               ; R1=A
        DAC                    ; A=A-1
```

Listing continues




```
JMP   LOOP          ; continue the procedure
FINI  .
      .
```

If the input to the routine is 0101 0011 it produces these results:

A	R0
0101 0011	0
0101 0010	1
0101 0000	2
0100 0000	3
0000 0000	4

BCD arithmetic in the EA9002

The EA9002 tackles BCD arithmetic uniquely; the processor has a flag – D – that determines the mode of operation for these instructions:

ADD, ADS, DAC, IAC, SUB, SUS, RAR

If the flag is set, these instructions perform decimal arithmetic (BCD). If the flag is clear, the processor performs normal binary operations. This capability is more flexible than that of any other microprocessor, but you must be careful to set the flag properly before executing any of these instructions. For example, this sequence adds register R0 to the accumulator using decimal arithmetic:

```
SED              ; set decimal mode
CLC              ; clear carry (always clear be-
                 ; fore first add)
ADD   R0         ; A=A+R0
```

Like SC/MP, the EA9002 performs all arithmetic with carry. Therefore, you must be certain that the carry flag is valid before executing any arithmetic statements.

To illustrate the BCD capability, consider this routine, which adds the contents of SM(0)-SM(3) to SM(4)-SM(7) – an 8-digit add:

```
ADD    LRI   R0,3     ; R0=index to number one
       LRI   R1,7     ; R1=index to number two
       SED            ; decimal mode
       CLC            ; clear the carry
ADDL   RDS   R1       ; get SM(R1)
       ADS   R0       ; add SM(R0)
       WRS   R1       ; SM(R1)=SM(R0)+SM(R1)
       DCR   R1       ; decrement pointers and
       DRJ   ADDL     ; continue till finished
```

In the past few months I've examined the architecture of a few of the more typical microprocessors. What I've done has by no means provided an exhaustive coverage of them. I've selected units that I feel offer something unique in their architecture; if you thoroughly understand these units you'll have little or no trouble learning to use a new one.

I'm always interested in new or unique algorithms for microprocessors. If you have a subroutine that you think is unique and would be valuable to others, drop me a line at Acuity Systems, 11413 Isaac Newton Square, Reston, VA 22090.

BIBLIOGRAPHY

Day, Colin A., "Full Table Quadratic Searching for Scatter Storage," *Communications of the ACM* 13,8 (August 1970), pp 481-482.

Dollhoff, T., "Making Hash With Tables," *BYTE*, January 1977. ♦

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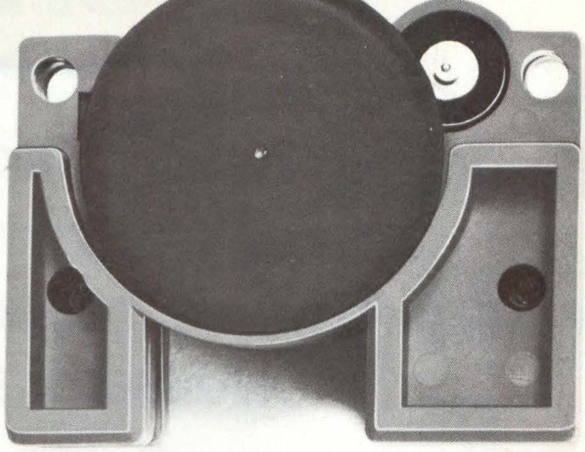

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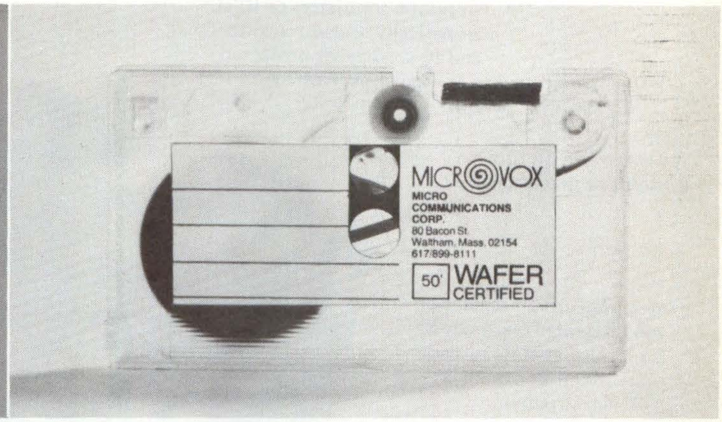

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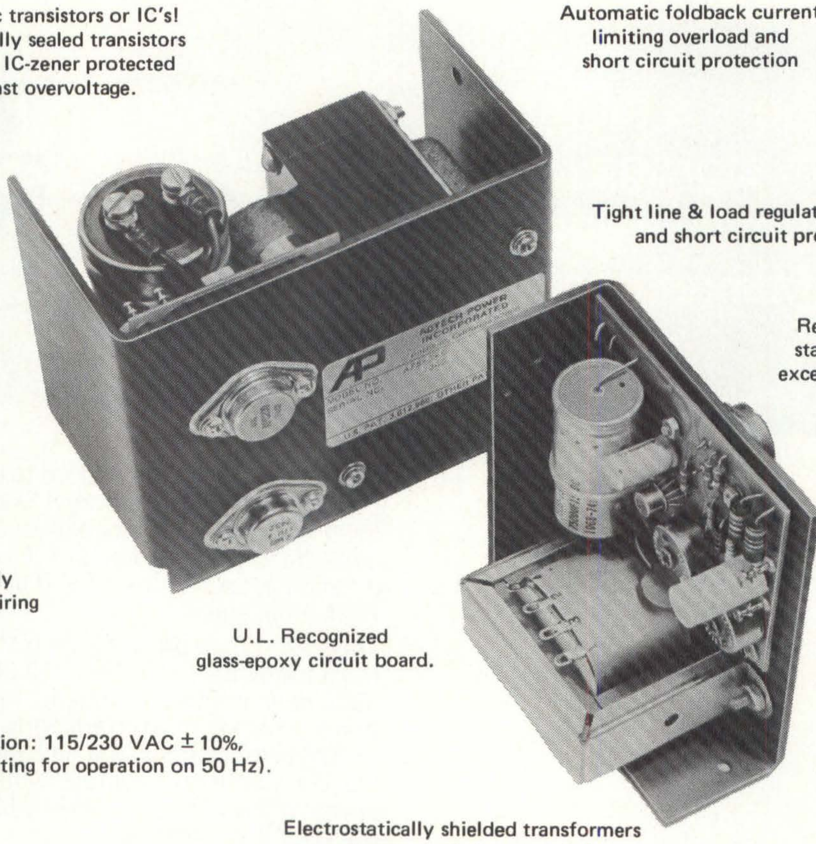

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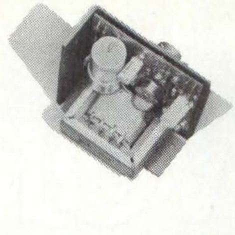

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APS 15–1.5	15	1.5	OV1–152
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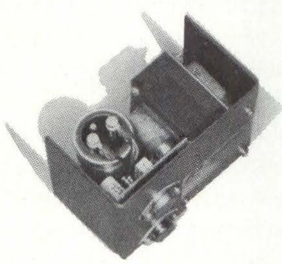

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APS 5–6	5	6	OV2–56
APS 6–5	6	5	OV2–65
APS 12–4	12	4	OV2–124
APS 15–3	15	3	OV2–153
APS 20–2.4	20	2.4	OV2–203
APS 24–2.2	24	2.2	OV2–245
APS 28–2	28	2	OV2–284

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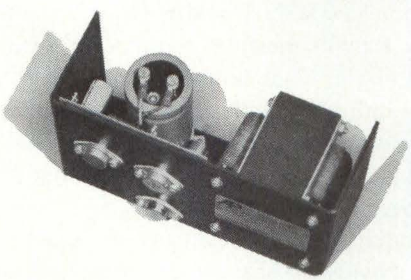

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	Volts	Amps	
APS 5-12	5	12	OV2-512
APS 5-10	5	10	OV2-510
APS 5-18	5	18	OV2-518
APS 12-7	12	7	OV2-127
APS 15-6	15	6	OV2-156
APS 24-5	24	5	OV2-245
APS 28-4	28	4	OV2-284

Power Supply Prices				OVP Prices	
Qty.	All Others	APS 5-12	APS 5-18	Qty.	Price
1-4	75.20	85.00	108.00	1-4	15.00
5-9	73.40	82.95	104.50	5-9	14.85
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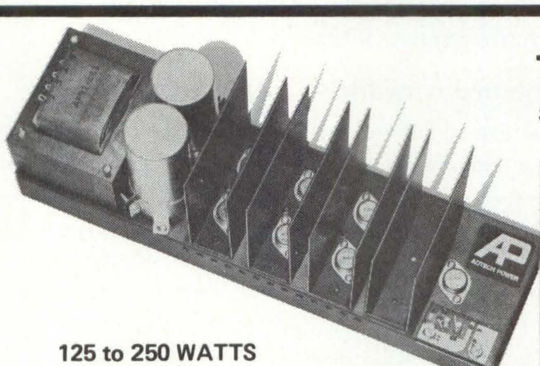

125 to 250 WATTS

Model Number	Rating		OVP Model No. Suffix
	Volts	Amps	
APS 5-30	5	30	OV3-530
APS 5-25	5	25	OV3-525
APS 6-22	6	22	OV3-622
APS 12-17	12	17	OV3-1217
APS 15-15	15	15	OV3-1515
APS 20-11	20	11	OV3-2011
APS 24-10	24	10	OV3-2410
APS 28-9	28	9	OV3-289

Power Supply Prices			OVP Prices	
Qty.	APS 5-30	All Others	Qty.	Prices
1-4	163.00	158.00	1-4	25.00
5-9	159.25	154.40	5-9	24.50
10-24	154.65	149.95	10-24	24.25
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CIRCLE 40

Implementing Networks

by Elton Sherman

How synchronous data link control lets distributed computers utilize existing communications capabilities and tie up minimal amounts of extra hardware and software.

With the advent of distributed network computing, many organizations can achieve broad-scale data-base consolidation while maintaining local availability and control of information. Particularly important in applications that require local data processing as well as access to central files, such capabilities prove especially useful to banks and other financial institutions with many branch offices, insurance companies that place a high degree of responsibility at the agent level, manufacturing concerns with multiple plant sites and distribution operations that maintain many regional warehouses.

The growing use of synchronous data link control (SDLC), a network communications protocol, allows the computers in such distributed networks to hook up over existing communication channels and places minimal burdens on the computers' hardware and software. The protocol also facilitates gradual network growth, because it allows network designers to interconnect terminals and processors at the most appropriate times and levels.

How have firms achieved data-base consolidation in the past? Many companies have extensive data-processing experience; they typically acquired such experience by installing large-scale centralized computers at headquarters locations. Then they met requirements for local data-base access by installing batch job-entry terminals at individual sites; these terminals generally communicate with a central system through a high-speed manual or automated dial-up telephone link activated at designated times. In newer systems, particularly where on-line inquiry response is more important than high-volume data exchanges, timesharing has replaced batch job entry. A third alternative, favored if local processing capability is the overriding concern, involves installing individual minicomputer systems at various sites; these systems then connect to the central EDP system in batch or timesharing modes or may use magnetic tape as their information-exchange medium.

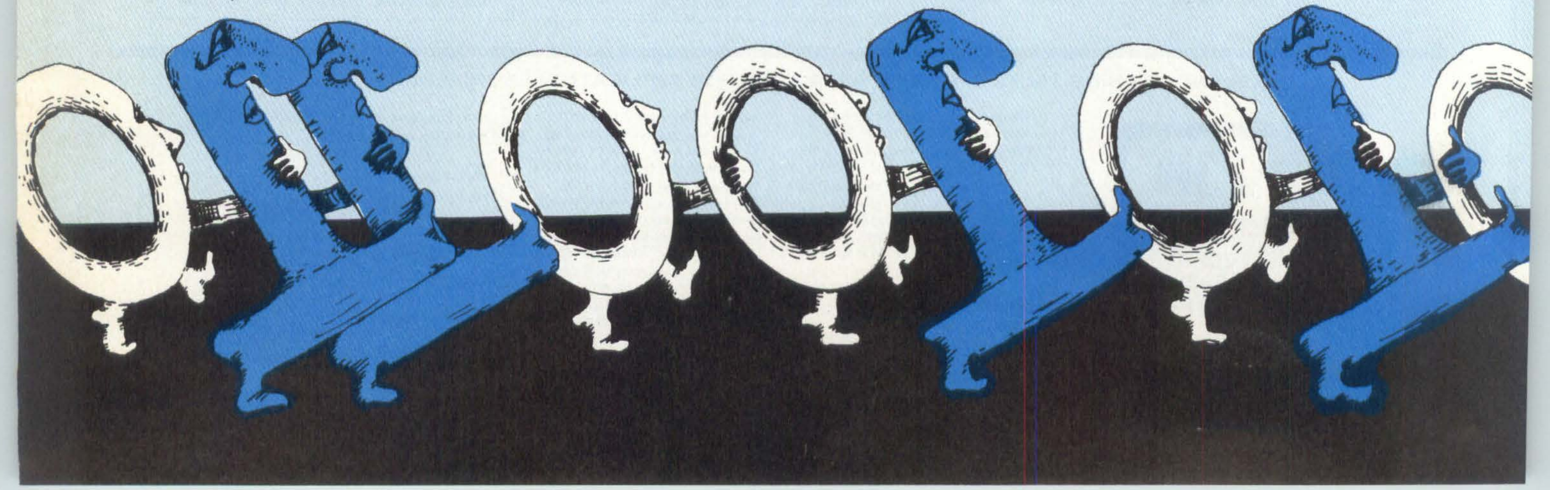
All of these traditional methods of broad-scale data-base consolidation have several fundamental shortcomings and limitations. Remote job-entry stations and local computers with batch or tape communication capabilities introduce long delays into file-updating procedures; they also can't support real-time inquiry-response transactions. Timesharing relieves these difficulties but places a large communications management burden on the central processor. Concentrating all network processing at one location also poses high risks; a hardware or software failure near the hub can shut down the entire system. And timesharing's total transaction capacity is limited, so expanding the number of terminals in a network can lead to unacceptably long interactive response times.

distributed networks — another alternative

In distributed network computing, a user segments a data base and manipulates its files in more than one processor

Elton Sherman *is manager of communication systems marketing at General Automation, Anaheim, CA.*

Illustration by Irene Stawicki



Distributed with SDLC

while exchanging data and commands freely among various computing nodes. The distributed processing can all occur at one or more central geographical locations, with little or no intelligence at remote terminals (Fig 1). Or the processing can occur at many remote locations (Fig 2). Such local computation offers good interactive response speed because of the small number of direct hands-on users at each machine. And such distributed machines can operate autonomously if the central office is unavailable.

Distributed network processing is feasible today because mini and microcomputers are cheaper and more reliable than ever; the development of high-speed, low-overhead communications disciplines for automated information-transfer management over data channels is another key factor in its growth. Such network disciplines permit the use of common-carrier or other low-cost communication paths to interconnect data-processing elements. They also provide uniform interfacing so that system components with different architectures can interact directly to share resources such as files or devices, and they avoid burdening file-oriented nodes with routine message-handling functions.

Effective communications in distributed processing networks requires that the procedures or protocols used must minimize the signalling and processing overheads required for each unit of information reliably transmitted. The methods must be open-ended to permit growth, and hardware and software must be compatible with large-scale EDP systems currently installed. Finally, network architecture must be hardware-intensive, so that design efforts are absorbed by the supplier rather than the individual user.

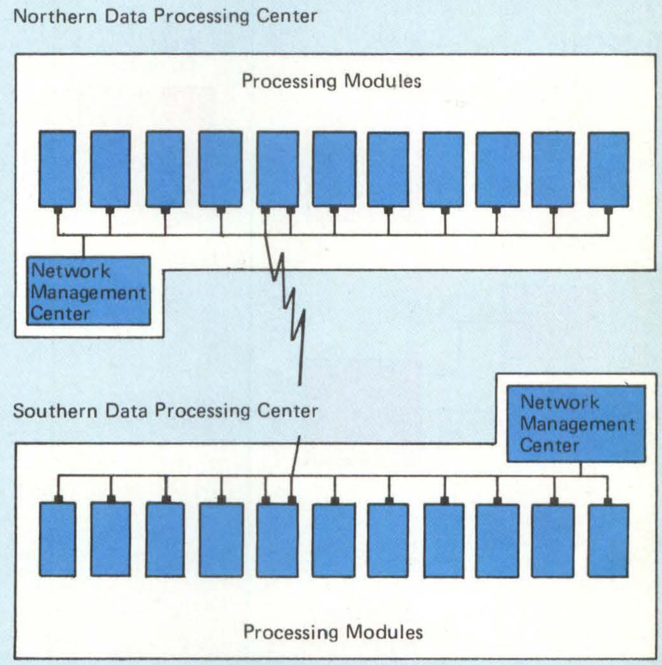


Fig 1 Processing network for a West Coast bank allows distributed data manipulation at two central locations; individual bank branches have terminals for data entry or retrieval only and perform no applications processing.

synchronous data link control

A data link includes a communication path plus all modulators, controllers and other equipment needed to achieve information transfer between designated points. Unless it's a dedicated, direct-wired connection, such a link must have the capability to establish message source and destination, operate transmission and reception equipment, detect and recover errors, supervise data-exchange procedures and perform functions related to such communication-path characteristics as point-to-point or multipoint connections and half- or full-duplex transmissions. The information needed to perform such tasks requires exchanges of signals in addition to those that carry the desired message; the signalling,

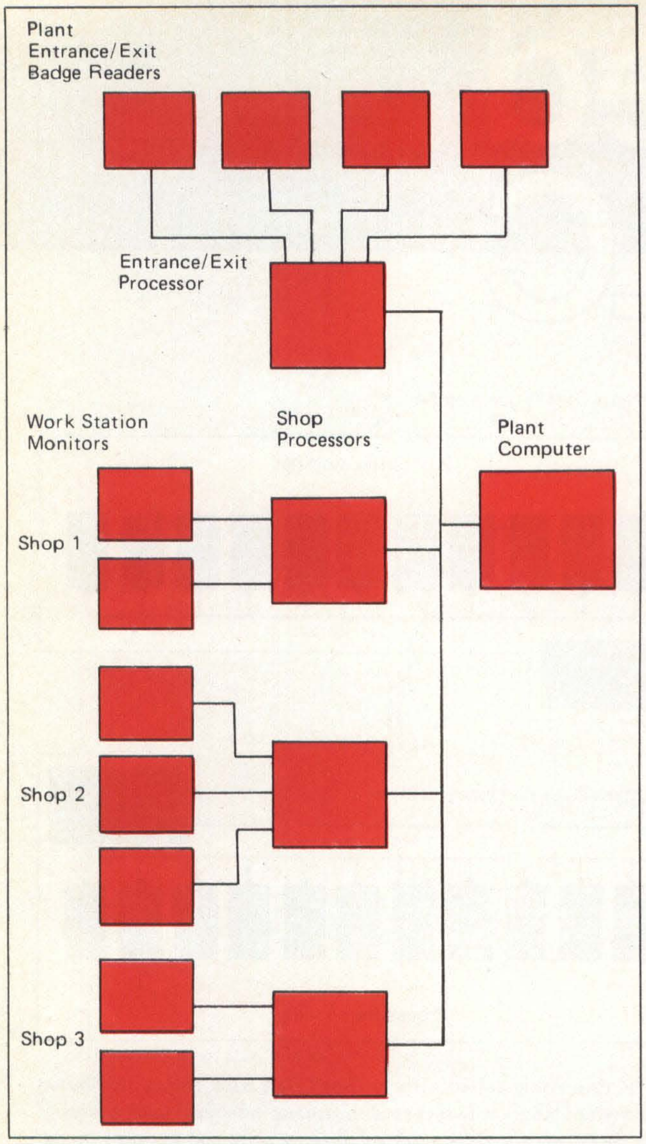


Fig 2 In this distributed processing network, processors at the plant gate and in each shop collect time information from badge readers and other terminals. Scheduling, absence reporting, productivity studies and other functions occur on-site; the plant computer provides coordination among shops.

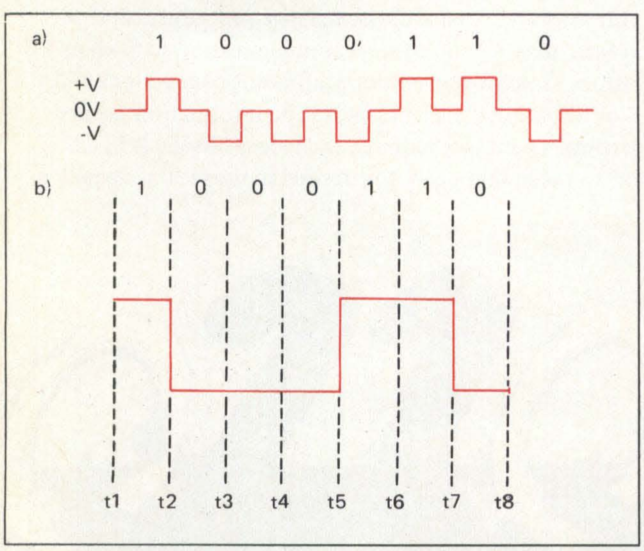


Fig 3 (a) Asynchronous transmission requires that signal level return to zero to mark the end of each bit cell. (b) Synchronous transmission establishes bit spacing by referencing a known time interval.

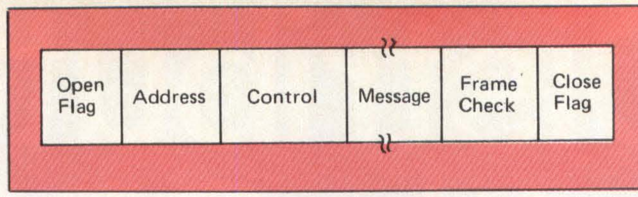


Fig 4 An SDLC frame can perform message-transmission, supervisory or management functions; the message field is absent in a supervisory frame and may provide link-oriented instructions in a management frame.

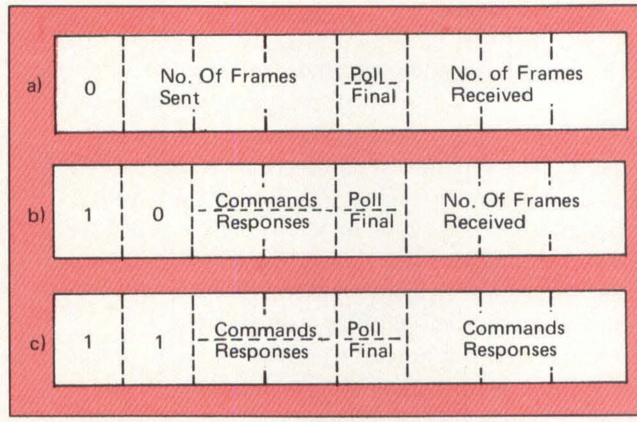


Fig 5 Control field bit patterns for (a) an information frame, (b) a supervisory frame and (c) a management frame.

switching and processing activities associated with such network communication constitute data link control.

If data communication is asynchronous, messages must incorporate some means of marking the beginning or end of each bit in a serial stream (Fig 3a). The advantage of such communication is that a message is self-contained; the chief limitation is the amount of signalling performed purely for identification purposes.

Synchronous data communication requires a predictable time relationship that defines bit durations or coordinates receiver and transmitter. A receiver can accordingly identify each bit space in a message once it has been referenced to the transmitter (Fig 3b). In the past few years users have shifted to such synchronous transmission, and network communications has accordingly moved toward synchronous data link control (SDLC) disciplines. IBM, General Automation and several other suppliers have already introduced hardware and software products to permit SDLC communication among a variety of processors; the American National Standards Institute (ANSI), Canadian Standards Association (CSA) and International Standards Organization (ISO) are all currently evaluating SDLC disciplines. Some of these organizations use "SDLC" as an identifying term for network procedures, but other terminology is also in use or proposed. All of these SDLC protocols are bit-oriented and involve similar concepts; differences occur principally in the coding of commands, so software analysis can provide compatibility.

In a generalized SDLC, one node in a link functions as a primary station and provides communication control; this primary node contacts one or more secondaries. Primaries have greater computational requirements than secondaries; a node with sufficient capability can act as a primary station in one link and a secondary in another. All transmissions occur to or from a primary station, but a primary or secondary station can initiate a call. Some applications, usually ones that involve well-defined processing functions and interactions, can be served by distributed networks whose stations all act as secondaries. The banking system diagrammed in Fig 1 is an example; its data link control functions are implemented by network hardware independently of individual processor modules.

All SDLC transmissions occur in well-defined frames. *Information frames* incorporate the transmitted message intelligence. *Supervisory frames* carry no data; they convey such signals as ready or busy indications, polls or acknowledgements and requests for retransmission after detecting errors. *Management frames* provide the data needed for such functions as activating, initializing and controlling the response mode of secondary stations and reporting errors in transmission procedures. Each message frame has six distinct fields (Fig 4); the standardized format minimizes the amount of signalling needed for data link control – by permitting multiple-frame transmission sequences that don't require an acknowledgement, for example.

Open flag field. This field is an 8-bit sequence generated at the transmitter. It indicates the beginning of a frame, provides a synchronizing reference for the position of subsequent fields and triggers a transmission-checking algorithm. All enabled stations monitor the network in an idle state and become active when they detect an open flag.

The usual open flag bit pattern is 01111110, unique because SDLC requires that a 0 be inserted after any five successive 1s within a frame – the pattern can't occur by chance in an error-free transaction.

Address field. This 8-bit field identifies one or more secondary stations in the link undergoing formation. Each secondary station normally has an individual and a group address; the latter is shared with other secondaries and finds use when messages must be accepted from or go to several points.

If the primary station is the receiver activated by a start flag, it recognizes any address as a valid transmitter and goes into synchronization to receive further bits. If a secondary station is the receiver, it only goes into synchronization if it recognizes its own individual or group address.

Control field. The 8-bit control field provides the signals needed to operate the data link; its bits accordingly identify frame type, sequence numbers and command or response commands.

In a typical SDLC implementation, if the leading bit in a frame's control field is a 0, the transmission constitutes an information frame (Fig 5a). One 3-bit value is a count stored at the transmitter; it designates the number of frames already sent in a sequence. A second 3-bit value, the total stored at the receiver, gives the number of error-free frames previously accepted in the sequence. The remaining bit in the control field acts as a send/receive indicator – it may either be a *poll* sent to a secondary station to require transmission or a *final* sent by a secondary station to mark end of transmission.

If the leading bit in the control field is a 1, the protocol examines the second bit to distinguish between a supervisory and a management frame. A supervisory frame (Fig 5b) initiates and controls subsequent message transfers; it has six additional bits – three for the receiver count, two for a command or response code and one for a poll/final indicator. A management frame (Fig 5c) provides means for operating communications devices; its six additional bits include 3- and 2-bit command/response codes and a 1-bit poll/final

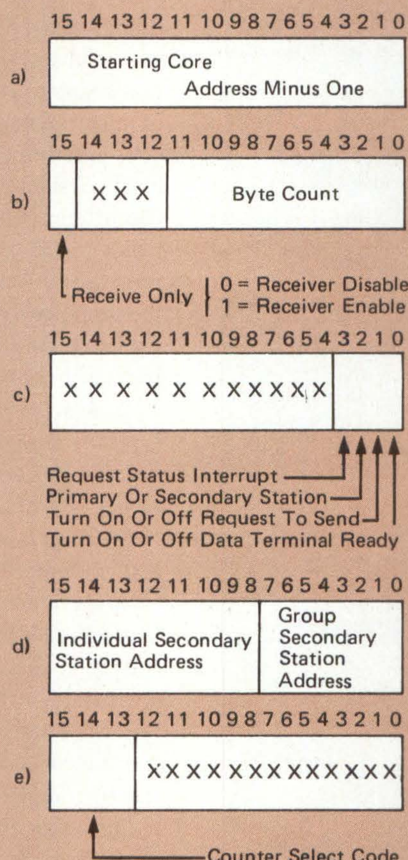


Fig 6 A "data transfer out from register or memory" instruction in a single-line DMA SDLC controller generates object words that provide (a) core address for receiver or transmitter, (b) byte count for receiver or transmitter, (c) line control bits, (d) secondary station and individual group addresses and (e) counter selection code.

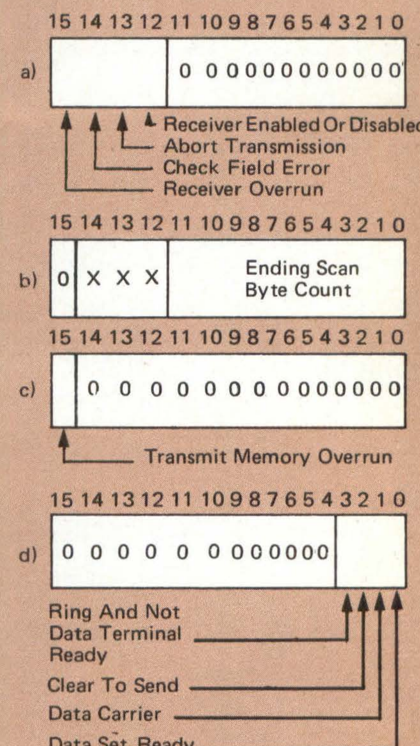


Fig 7 A "data transfer into register or memory" instruction in a single-line DMA SDLC controller generates object words that provide (a) receiver interrupt or error indicator, (b) byte count when no abort is required, (c) transmitter interrupt caused by memory overrun and (d) status interrupt.

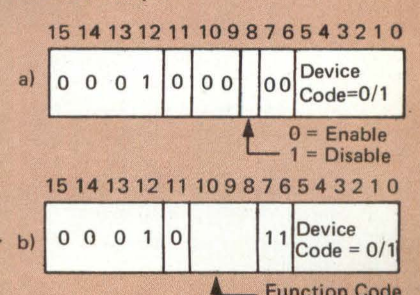


Fig 8 In a single-line DMA SDLC controller, control-interrupt instructions (a) and test instructions (b) each generate one object word.

Table 1. Command/Response Functions In Supervisory- And Management-Frame Control Fields

SUPERVISORY FRAMES

Ready to receive: command or response sent by either a primary or a secondary station to indicate availabilty of input buffers

Not ready to receive: command or response sent by either a primary or a secondary station to indicate availability of input buffers

Transmit or retransmit: command or response sent by either a primary or a secondary station to request a frame from another station on a link

MANAGEMENT FRAMES

Nonsequential information: command for or response to transmission of operating control data

Request for initialization: response by a secondary station asking for a reset of sequence counts

Set initialization mode: command by a primary station, resetting sequence counts

Set normal response mode: command by a primary station, establishing the subordination of a secondary station

Request on-line: response by a secondary station, telling that it is disconnected

Disconnect: command by a primary station, placing a secondary station off-line

Nonsequenced acknowledgement: affirmative response to commands that set normal response mode, disconnect or set initialization mode

Command reject: response by a secondary station in a normal response mode when it receives a nonvalid command

Exchange station identification: command by a primary asking for the address of the receiving secondary station; response to such a request by a secondary station, with the required address in the message field of the frame

Nonsequenced poll: command by a primary, requesting transmission from a secondary station; the request is an invitation when no poll bit is present and is a demand when the poll bit is set

Test: command by a primary station to check the bit pattern in the message field; response by a secondary station indicating the check

Table 2. SDLC Program-Driver Functions

* Select line register to be loaded
* Load selected register
* Set address and byte count to start input
* Deactivate output
* Start output transmission
* Set up line status control register
* Set up address
* Turn around half-duplex line for change to input or output
* Test line status
* Mediate conflicts among terminals attempting to transmit simultaneously

Table 3. SDLC Program-Handler Functions

* Initialize driver and handler tables, placing the controller in the ready state
* Close driver and handler tables, placing the controller in the ready state
* Place line in the continuous read condition and issue responses after information frames are received and processed
* Start transmissions and retransmissions
* Change addresses for switchovers to alternate processors
* Abort reads in progress

indicator. Table 1 summarizes the functions defined by the command/response bits in the supervisory and management frame control fields.

Message field. This field can be any integral multiple of eight bits long, up to the capacity limitations of buffers or other link or processor hardware. In an information frame, this field contains the message intelligence; it's absent in a supervisory frame and may be included in a management frame for link oriented instructions.

Frame check field. This 16-bit number, computed at the transmitter on the basis of the other bits in the frame, is compared with the result of a similar calculation performed at the receiver. If the values agree, the frame transmission is assumed to be error-free; a retransmission request automatically goes out if the check is negative.

Close flag field. This 8-bit field terminates the error check and indicates the end of a frame. Its bit pattern is identical to the open flag's.

network architecture for SDLC systems

Standardized SDLC implies commercially available hardware and software, used to interface different terminals and processors to common lines and to implement unified communication management functions. One SDLC controller configuration could serve all applications, but cost and overhead considerations suggest developing subsets of controllers for different classes of communications. For example, my firm's SDLC product line includes a multiplexer to tie a processor to several terminals or computers, a single-line programmed I/0 controller to interface a terminal to a controller and a single-line DMA controller for processor-to-processor connection.

A network's hardware comprises the SDLC controllers, typically designed as one or more cards for insertion in a processor or terminal communications rack. These controllers automatically detect opening and closing frame flags, insert and delete transparent zeros into bit streams and compute frame check sequences.

In its transmit mode, a processor typically enables its controller by loading a core location and byte count. The controller then automatically produces an open flag, an address and control bits and transmits data from core, starting at the designated location and ending when the byte count is exhausted. Next it generates check bits and a close flag to complete the frame and interrupts the processor to indicate that transmission is complete. Any required zeros are inserted during transmission.

In its receive mode, the processor enables the SDLC controller by loading a core location and byte count for storage of incoming messages. The controller then waits for activation by a start flag and checks for a valid address. If it finds one, it goes into synchronization and accepts control commands and information bits while deleting any required zeros. The controller also calculates check digits and performs the necessary comparisons, and generates a retransmission request if it senses an error. After generating the close flag, the controller interrupts the processor to indicate completion of reception.

SDLC hardware operates under the control of its associated processors' or terminals' software, but it also requires some additional communication software. That software

can be built around a program driver, which executes physical I/0 tasks and performs the line-dependent functions listed in Table 2. The software also requires a program handler to implement protocol and perform the device-dependent jobs outlined in Table 3.

The required programming tasks are relatively simple. For example, an I/0 driver for a typical single-line DMA SDLC controller has only four standard instructions – data transfer into (out from) register or memory, control interrupts and test commands. Writing the SDLC software involves specifying sequences of these instructions, accompanied by identification of memory or register locations for the object words where corresponding parameters are stored.

Each instruction generates object words that incorporate the parameters needed for specific link-control functions. Again referring to the single-line DMA SDLC controller, five 16-bit object words result from the "data transfer out from register or memory" instructions. For transmit and receive tasks, an entire word (Fig 6a) defines starting core location. Likewise, 12 bits of a second object word (Fig 6b) provide byte count; for the transmit function the remaining four bits are ignored, and for the receive function three are ignored and one provides an enable/disable flag. Four bits of another word (Fig 6c) establish line control; these bits indicate a request for a status interrupt, identify a primary or secondary station, turn on or off a request to send, and turn on or off a data-terminal-ready signal. For secondary stations, two 8-bit bytes designate the individual and group addresses (Fig 6d). Finally, a counter select word (Fig 6e) with a 3-bit code specifies the receive core address counter, receive control byte counter, transmit core address counter, transmit control byte counter, line control register or secondary address register.

Four object words result from "data transfer into register or memory" parameters. The receiver interrupt or error indicator (Fig 7a) operates during multi-frame transfers and includes bits that indicate receiver overrun, check sequence error, abort command and receiver enable or disable. A second object word (Fig 7b) incorporates a 12-bit ending scan byte count used when no abort is indicated. The transmitter interrupt word (Fig 7c) requires one bit to indicate memory overrun, and the status interrupt word (Fig 7d) uses four bits to indicate ring and not data terminal ready, clear to send, data carrier on or off and data set ready.

Only one object word results from control-interrupt instruction parameters (Fig 8a); it incorporates a 6-bit device code and a 1-bit enable/disable flag. Finally, one object word also results from the test instruction (Fig 8b); it incorporates a 6-bit device code, plus a 3-bit function code to designate controller ready, data set ready, data carrier detect, clear to send, single-line or multiplex controller identification, receive interrupt ready, transmit interrupt ready or status interrupt ready.

With a small set of such SDLC controllers and minimal communications software, a system designer can configure a wide variety of computer networks, which can both meet immediate needs and expand or change to match changing requirements. Each network requires data link control hardware at every node. ♦

designers' notebook

Dynamic shift register simplifies circuitry in display-equipped experimental telephone

With applications far removed from its initial use as a carrier of voice messages, the telephone now routinely functions as a transmitter of digital information between people and computers. And further evolution continues; telephone lines could someday routinely carry video information and also perform a host of other tasks.

To investigate the feasibility of some of these additional telephone functions, engineers at Bell-Northern Research, Ottawa, Canada, configured an experimental telephone that incorporates a 16-digit LED display. A user dials a number with the phone "on hook;" the number appears digit by digit on the display but isn't sent into the telephone network until the user lifts the handset and presses the telephone's octothorpe button (#). If the dialed number produces a busy signal, pressing the octothorpe again redials the number automatically. Pressing another key on the phone's pushbutton set displays the time of day on the LEDs; pressing that button again clears the display.

The work of Peter Luff, manager of new-products applications research, and Terry Thomas, manager of custom integrated-circuit design, the experimental display telephone could also, with suitable changes, provide such functions as credit-card verification or time countdown in coin-operated installations. Its buffer memory now stores only one number, but add-on modules could increase that capacity to ten.

As they designed the Displayphone, Luff and Thomas faced several problems, whose solutions they discuss in a recent issue of Bell-Northern's *Telesis.* First, they had to decide whether to implement the unit's dialing functions using dial pulses or pushbutton signals (audible tones). Second, they had to choose a display method and then configure the circuitry required to implement that method.

Most telephones now in use have rotary dials and use dial pulsing as their signaling method; each dialed digit corre-

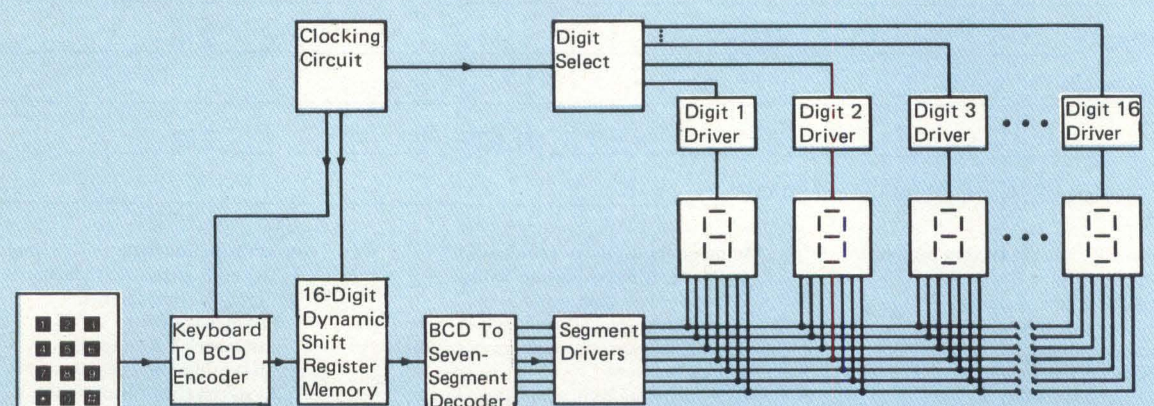


Fig 1 Display multiplexing chip for the experimental telephone incorporates seven leads that connect in parallel the corresponding segments of each of the display's 16 LED digits; each digit also has a ground connection. A 16-bit dynamic shift register stores the dialed digits and circulates them at a rate that suits display refresh. In addition to acting as a clocking circuit for this process, a 4-bit dynamic counter on command selects the digits one at a time from the register and conveys them to a dialer chip, which pulses them into the telephone network.

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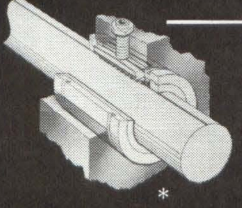

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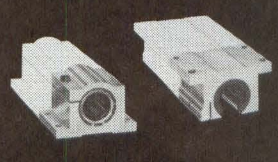

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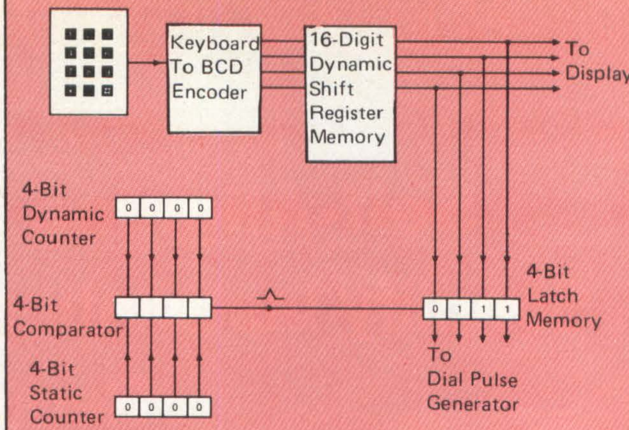


Fig 2 When the telephone's user presses the phone's octothorpe button (#), a 4-bit static counter on the telephone's dialer chip sets at 0000; the next time the 4-bit dynamic counter on the display multiplexer chip reaches 0000, it generates an output pulse from a comparator. That pulse reads the storage register's first digit into a latch memory and pulses the phone network accordingly. The chip then increments the static counter by one and repeats the process for the next dialed digit.

sponds to a fixed number of 48-V pulses that, transmitted at 10 Hz, operate the telephone network's switching machines. But newer pushbutton telephones speed up the dialing process by substituting tones of various frequencies for the voltage pulses; each frequency corresponds to a different digit.

Because both types of units currently find use in telephone networks, Luff and Thomas decided to implement the Displayphone with a pushbutton dialer that generates voltage pulses. Because a user can push the buttons in the unit at a rate greater than 10 Hz, they added a buffer memory that stores the dialed digits until all have been entered. This buffer provides the bonus function of single-number redial, and a converter can transform the entire dialer to a tone-signaling unit if the network it serves uses that signaling method.

Investigating display technologies, Luff and Thomas decided that liquid crystals exhibited "questionable" reliability; LCDs also make display multiplexing impractical. The designers thus chose LEDs, which require higher currents than LCDs – not a problem, however, because the telephone's display set uses standard 115 Vac current converted to 6 Vdc. They chose this alternative rather than rely on the telephone system's 48-V supply to achieve reliability with low power consumption at low voltages; operation at 6 Vdc also provides safety, and it simplified the design of the interface between the LEDs and their custom integrated driving circuits.

To fabricate those custom circuits – a 16-digit buffer memory chip, a display multiplexing chip and a dialer chip– Luff and Thomas chose CMOS technology because of its low power consumption, high noise immunity and low-voltage operation. Their lab also had CMOS fabrication and design facilities; in a commercial design, the three chips' functions would be implemented on one custom designed chip.

The two designers chose a 16-digit LED display because it can accommodate international, long-distance and tie-line dialing as well as such contemplated applications as credit-card verification. To reduce circuit size and cost, they decided to multiplex one set of display-driver circuits among all 16 digits.

Such multiplexing minimizes the amount of circuitry required to decode into 7-segment display format the BCD-formatted information produced when a user dials a number. It also reduces the number of connections the display requires, but it requires more complex circuitry than a static display system to steer information to the proper digit on the display. Additionally, multiplexing the 16 LEDs reduces the brightness of each of them by a factor of 16; Luff and Thomas solved this problem by adding 23 transistor amplifiers that boost the current through each LED by that same factor.

In the basic multiplexing arrangement (Fig 1), seven leads connect in parallel the corresponding LED segments of all 16 digits, and each digit also has one ground connection. (One transistor amplifier serves each of these 23 leads). When a user pushes a button on the telephone, the BCD signals it generates are decoded into 7-segment format, and without multiplexing circuitry, 16 identical digits would light up. But the circuitry selects and grounds the required digit, so when a button is pushed, only the digit it corresponds to turns on.

To multiplex the display and provide information storage for dial pulsing, Luff and Thomas chose a 16-digit dynamic circulating shift register; an identical unit on the memory chip serves as the buffer for pushbutton dialing. Termed the most "elegant" feature of the Displayphone design, this device reduces the amount of circuitry required to address the display, say the two designers. They could have used a RAM, but that device would have required an additional scanning/refresh circuit, plus addressing circuitry to provide data for dialing.

By contrast, the shift register merely circulates the display data at a rate that suits display refresh; its output is displayed and then recirculated back into its input in a closed loop. Time-division multiplexing apportions one digit's display circuitry among all 16; the multiplexing rate also allows the register's output, when properly clocked and identified, to select the correct digit for dialing. And, say Luff and Thomas, because the register is continuously clocked, the Displayphone can incorporate dynamic circuit elements, which further reduce its complexity.

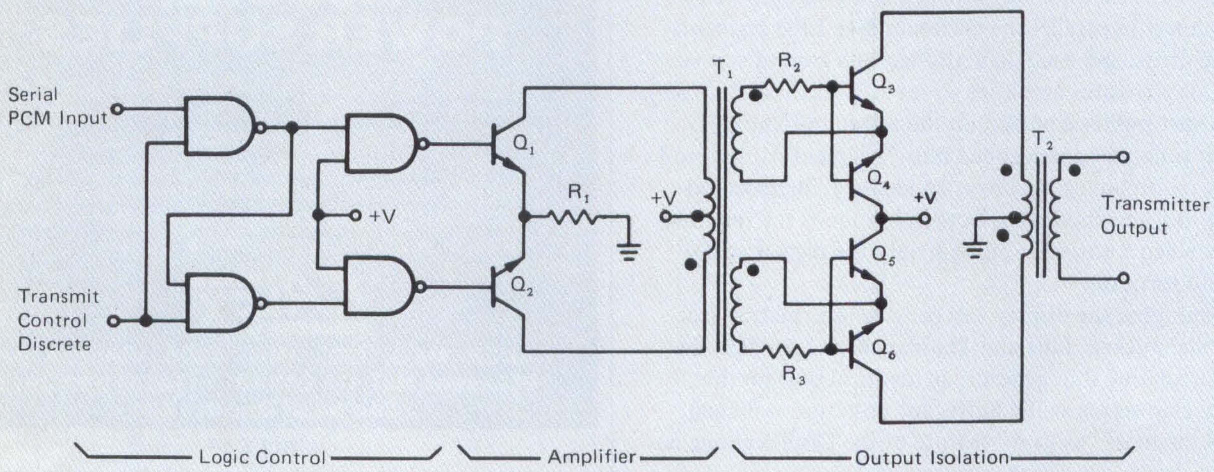
One of these dynamic elements, a 4-bit counter on the display multiplexing chip, functions as the Displayphone's clocking circuit. It cycles through 16 states, just enough to circulate the content's of the chip's 16-bit storage register once; each state corresponds to a digit and is treated as a time slot. To send a telephone number down the line once it is in the telephone and displayed there (Fig 2), a user pushes the octothorpe button, which sets a 4-bit static counter on the dialer chip to 0000. The next time the 4-bit dynamic counter reaches 0000, it generates an output pulse from a 4-bit comparator; that pulse opens a 4-bit latch memory, reads into it the BCD output pulse from the storage register's first time slot and sends the corresponding number of pulses down the line. The dialer then increments the static counter by one, and the process repeats until all digits in the required number have been dialed.

Circuit isolates transmitter output

Used to isolate the output of idle transmitters from data buses, high impedance couplings increase a transmitter's active input impedance, cutting power transfer efficiency. These couplings require complex circuits, often with high supply voltages. They also require both positive and negative supply voltages. And they provide inadequate isolation during power-off. To deal with some of the problems associated with output isolation, G. E. Proch of Lockheed Electronics devised a digital transmitter with an output isolation circuit. He claims the circuit provides dynamic impedance as a function of the amplifier output level.

them into their high-impedance cutoff state. In the forward biased state, the amplifier, controlled by the collector-emitter impedance, supplies current. Operating Q_3 in the inverted mode yields an effective current gain approximately equal to two. Limiting base current with R_2 restricts the maximum output current through Q_3, Q_4 to a value commensurate with the base current and inverted mode current gain. Thus, as the load impedance decreases, the output current increases proportionally until it reaches the current limit. Further decreases in load impedance lower output current only slightly.

Digital Transmitter for Data Bus Communications System



Designed for one Mbps Manchester-coded signals, the transmitter contains a logic control section, an amplifier and an output isolation section. Two series of transistor pairs – Q_3, Q_4 and Q_5, Q_6 – provide dynamic impedance. A positive signal level at resistor R_2 forward biases the base-emitter junctions of Q_3 and Q_4 and drives them into low-impedance conduction. Additionally, a negative signal level at R_2 reverse biases the base-emitter junctions and drives

The functions and operation of Q_5, Q_6 and R_3 resemble those of Q_3, Q_4 and R_2, says Proch. By driving Q_3, Q_4 into conduction and Q_5, Q_6 into cutoff and reversing drive polarity, the transmitter generates bilevel output signals that occur alternately at the collectors at Q_3 and Q_6. Hybrid transformer T_2 couples these signals to the load. The resultant transmitter output is a balanced differential signal, dc-isolated from the transmitter circuits.

Digital threshold receiver improves discrimination

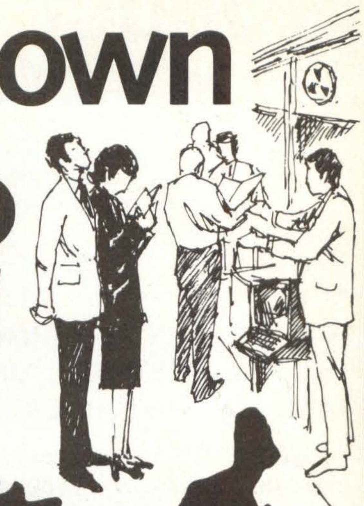
Using high-gain, saturating differential amplifiers with level-shifting circuits, common receiver designs convert transmission line signals to standard logic levels. In pulse-code modulated digital communication systems, these receivers also include auxiliary circuits which discriminate between information signals and noise. Often, however, the circuits mistake extraneous input for information, a failing that increases the likelihood of data errors and compounds the difficulty of extracting encoded information.

To improve a receiver's discrimination between true signals and noise, G. E. Proch of Lockheed Electronics has designed a receiver with a threshold circuit that converts filtered signals to standard logic levels. He claims the design also attenuates the received signal's baseline wander.

Eight resistors serve as source and termination for the two filters. In the absence of power supply voltages, the resistors prevent excessive mismatches in multi-terminal systems by placing a proper load across the transmission line. Limiting the high-frequency response of the communication channel, two band-limiting prefilters provide a standard waveform characteristic at the detector input. With cutoff frequencies 0.6 to 0.8 times the inverse of the minimum information waveform pulse width, RC-, LC- or RLC-type low-pass filter networks yield this filter characteristic.

The receiver's Schmitt trigger circuits consist of a differential amplifier, a NAND gate and a two-resistor feedback network, says Proch. Together, these components produce a hysteresis characteristic that provides threshold detection level stability. Bilevel outputs of the two trigger circuits combine in an RS-latch to provide a serial output stream.

How to get your own free ticket to



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These display terminals serve systems that use the Honeywell 7700 VIP, Univac-Uniscope and IBM 2265 and

3275 protocols. System 400 terminals operate synchronously over dial or dedicated networks at rates of up to 9600 bps and provide fully buffered communications. They also provide dual-intensity display, upper and lower case character sets, user defined program function keys and self diagnostics, which include a line monitor mode for system troubleshooting. You can obtain either 960-or-1920-character screens. International Communications Corp., 8600 N.W. 41st St., Miami, FL 33166. (305) 592-7654

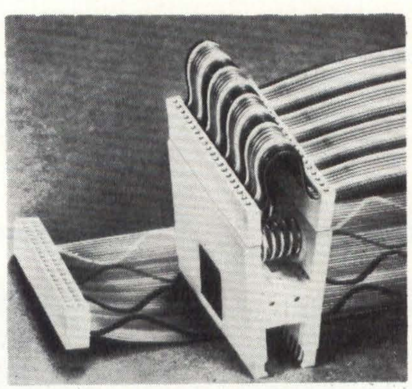
Circle 274

66-CPS PRINTER RUNS ON 12 VDC

For data processing terminals, communications, instrumentation and point-of-sale terminals, the 115DR character printer requires one 12 Vdc supply. It stands 100 mm high, weighs 3 kg and prints up to 40 char /line at 66 cps, using a 5x7 matrix printhead. The unit also achieves facsimile reproduction; you can set the line spacing so that continuous vertical lines are formed seven dots at a time with each passage of the the printer head. The unit comes with printer head and ribbon system, paper roller and feed mechanism and motor control electronics. Character generator and amplifier for the head solenoids aren't included. Philips, Elcoma Div., P.O. Box 523, Eindhoven, Netherlands.

CLIP ASSEMBLY MATES IC PACKAGE WITH RIBBON CABLE

Test Clip Jumper assembly marries a tandem pair of single-row, 20-contact female connectors to any of several 28 AWG stranded 40-conductor ribbon cables, at a customer-specified length, and terminated in any of several ways. Standard cable options include Electric Pink and double-encoded Rainbow (groups of ten color striped on the cable reverse). Standard remote end terminations include unterminated, double-row 0.100" matrix socket connectors, card-edge connectors, printed circuit board connectors, DIP plug connectors and daisy chained connectors.Price



for an assembly that connects to a 40-pin double-row socket connector through 12" of rainbow ribbon cable: $13.88 in tens. AP Products, Box 110, 72 Corwin Dr., Painesville, OH 44077. (216) 354-2101

Circle 278

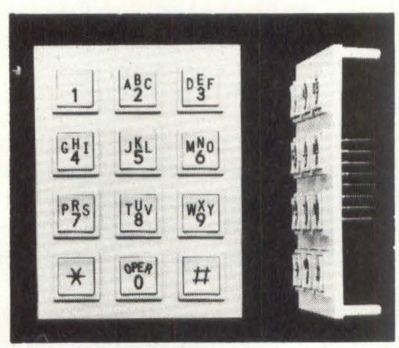
ANALOG I/O SYSTEM MATES WITH DEC LSI-11

One of four analog I/O systems that serve Digital Equipment's LSI-11 microcomputer, the DT 1761 incorporates a 16-channel 12-bit A/D converter, 2-channel 12-bit D/A converters with point plotting and options for programmable gain amplifier and DMA interface. It comes on one quad board. Price: $995. Data Translation, 23 Strathmore Rd., Natick, MA 01760. (617) 655-5300

Circle 272

KEYBOARD UNIT RESEMBLES TOUCH TONE

This keyboard resembles a Touch Tone unit but is simpler and less costly. Key travel on the ET measures 0.015" to 0.020" and operating temperature range equals -20° to 150° F. The unit operates with 10-12 oz. force and comes with both single-pole encoding (with a common contact



and a separate contact for each key) and three Touch Tone row/column matrix encodings (with zero, one or two common contacts per key). Termination (0.030" dia pins on 0.125" centers) occurs through cylindrical pins that accept a variety of connectors and can also be soldered. Contact resistance measures less than 20Ω, and capacitance is less than 20 pF. Chomerics, 77 Dragon Ct., Woburn, MA 01801. (617) 935-4850 **Circle 276**

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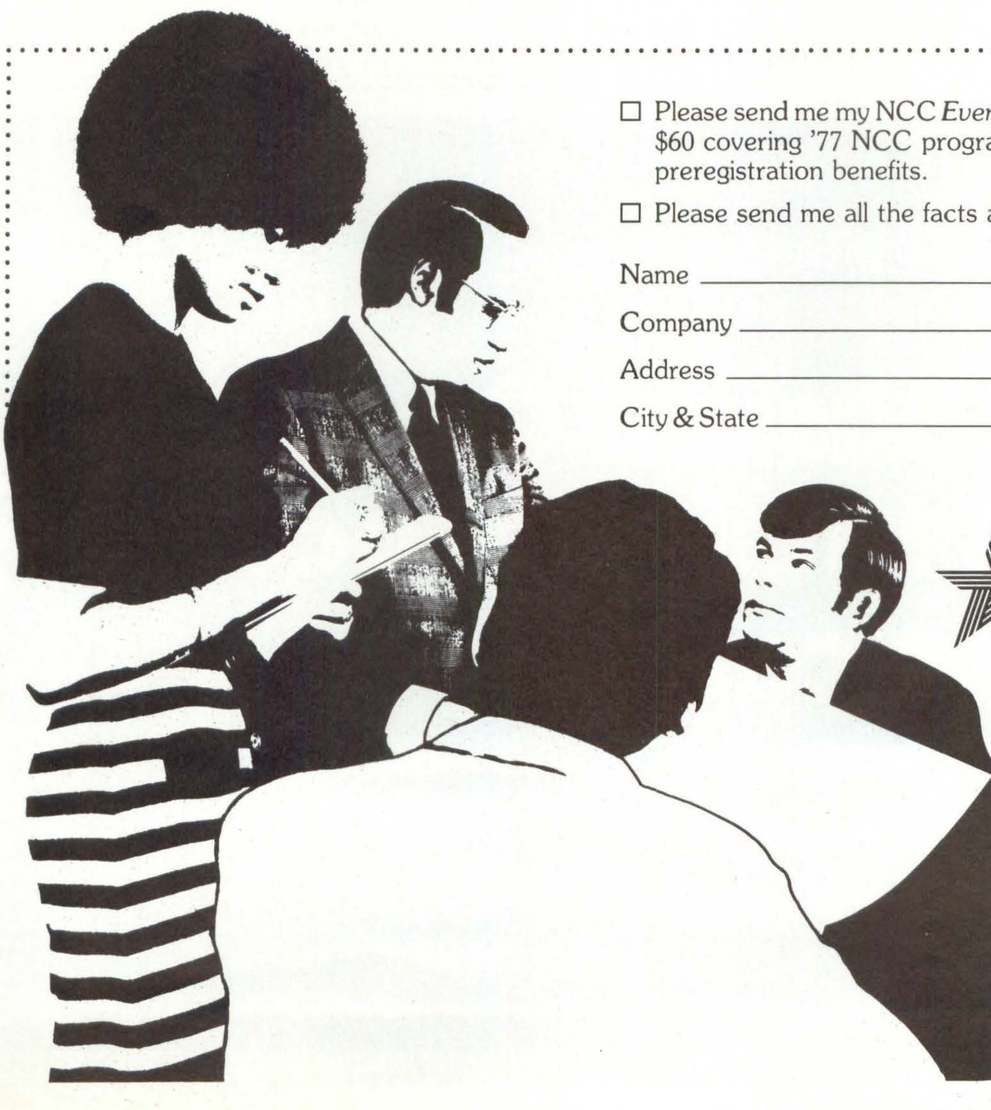

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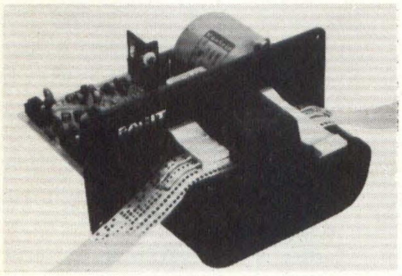

has one moving part and uses an LED as its light source; it can read tapes with up to 60% transmissivity. The unit comes either as a read head with control electronics or with power supply and parallel SP-1 interface. Facit-Addo, Inc., 66 Field Point Rd., Greenwich, CT 06830. **Circle 290**

CARD READER MOUNTS ON 2 PLANES

Model MKL magnetic card reader scans cards to ABA/ISO/IATA standards and can also code cards if required. Divided into transport and read/write modules, it can be assembled on two different planes. Four light sensors monitor card position and signal to the control electronics; a serrated belt provides transport. The unit accepts cards up to 1 mm thick and also processes embossed plastic cards. The standard model comes with one single-track head; you can also get units with two heads. Steinmetz-Krischke-Systemtechnik, 75 Karlsruhe 41, Maybachstr. 10, W. Germany.

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The Execuport 3000 provides 136-column printout and plots data with a 240 point/in^2 resolution (24 vertical x 10 horizontal). It can underscore, overscore, subscript and superscript and also provides 1/4-line stepping in both directions. The unit has a built-in acoustic coupler and accepts 80-or 136-column paper rolls in 100-ft. lengths. Other features include switchable mode options (line and local or isolate for separation of printer and modem), error control through operators (selected odd or even parity generation), and choice of keyboards (Teletype or multimode with a numeric cluster). Options include out-of-paper alarm, Bell decoder, 20 mA loop, 20-character response generator, 1-char-

acter ACK/NAK, out-of-service switch and data access connector. Computer Transceiver Systems, Inc., E. 66 Midland Ave., Paramus, NJ

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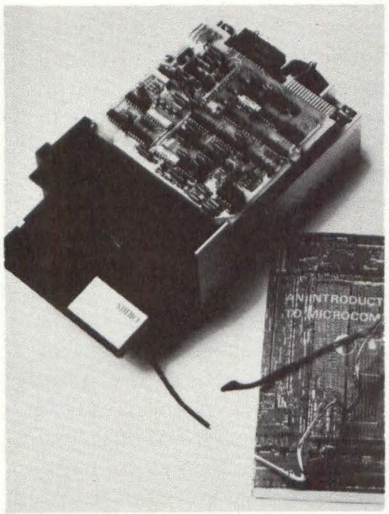


diskette. It suits applications in word processing systems, microcomputers, smart terminals, portable computers and program load/storage devices, and it accepts hard sectored diskettes (10 sectors/track) or a modified IBM-type soft sectored format (18 sectors/track, 128 bytes/sector). The unit's basic unformatted capacity equals 109.4K bytes on 35 tracks, and you can expand that capacity by choosing to address an additional 5 tracks on any diskette. Track-to-track access time measures 30 ms, and a random average seek measures 370 ms. The unit's rotational speed equals 300 rpm. Price: under $300 in large OEM quantities. Wangco, 5404 Jandy Pl., Los Angeles, CA 90066. (213) 390-8081 **Circle 288**

CRT TERMINAL SPORTS FULLY CONTROLLABLE CURSOR

Model 3841 CRT terminal measures 13.5" x 15.5" x 21" and weighs 48 lbs; it offers wide/narrow character display on 12" screen, plug-in ICs, RS 232 and current loop interfaces and upper/lower case ASCII character display. Its cursor is fully controllable from keyboard or computer by ESC codes A, B, C, D and H for up, down, right, left and home respectively. X-Y addressing also occurs through ESC sequences. All interface codes and choice of 15 speeds — 50 to 9600 baud — are set by DIP switches. The unit operates in scroll or page mode; offers erase to end of line, erase to end of page and page erase; and displays a blinking cursor. Options include columnar tab, video output, peripheral interface, numeric keypad, 15" CRT and upper case only. Price $1450.

Teleray Div. of Research, Inc., Box 24064, Minneapolis, MN 55424. (612) 941-3300 **Circle 291**

CIRCLE 53

product news

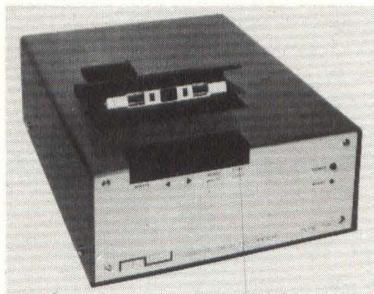
PACKAGING SYSTEM ACCEPTS INTERMIXED BOARDS

This packaging system lets you mix Wire Wrap panel sizes and IC densities; you can insert panels containing from 32 to 192 ICs and measuring from 4.5" x 6.0" to 14.9" x 8.0" into one panel assembly. Multiples of a two-piece Wire Wrap-to-Wire Wrap connector containing 108 I/O pins implement this interchangeability. The smallest panel contains 32 ICs and has 108 I/O pins; the largest, 192 ICs and 540 I/O pins. The panels plug into three independent backplanes, each of which can contain as many as three voltage distribution planes. Also part of the system, a data signal bus backplane handles the parallel signal requirements of memories or parallel data bus systems. Mupac Corp., 646 Summer St., Brockton, MA 02402. (617) 588-6110

Circle 287

CASSETTE RECORDER STORES MICRO DATA

This digital cassette recorder, designated Model 715, loads and dumps data for minicomputers and microcomputers and can also facilitate video-display-unit dumping and backup in Teletype operations. A modified version, Model 715R, incorporates a remote control



pause that suits it to long-term data logging operations. Using standard low-noise cassettes, the unit can operate at speeds up to 2.4 kbps with a reliability of $1/10^6$. At 1.2 kbps it loads a 4K 16-bit compiler or assembler program in less than 2 min. Standard available interfaces, selected by internal link-change, include V 24/RS 232B, current loop (20-60mA), EIA modem, and positive and negative TTL/DTL levels. M.S. Instruments, Ltd., Rowden Road, Beckenham, Kent BR3 4NA, England.

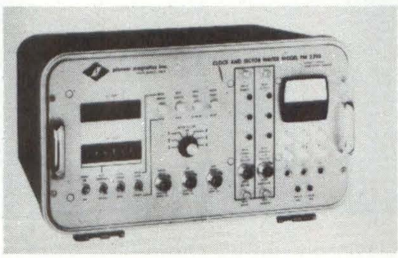
VOICE READOUT STORES 112 WORDS

Designated Model 1650, this programmable voice readout system stores data in PROMs and allows vocabulary expansion from one to 112 words in the standard half ATR rack. The system uses a male voice; each word has a 4-bit (16 combination) word address and a 3-bit (7 combination) board address. You can select any one of the 112 words by providing a correct 7-digit binary word/board address and an enable signal. At the end of a word, a pause pulse signals the system is ready for the next command. The dual circuit provides 8Ω at 250 mW for local monitoring in addition to a balanced 600Ω isolated transformer output. Master Specialties, 1640 Monrovia, Costa Mesa, CA 92627. (714) 642-2427

Circle 289

CLOCK/SECTOR WRITER AIDS ROTATING-MEMORY DESIGN

This portable high-speed clock and sector writer for rotating memories, designated PM 2390, records open or closed clock tracks at rates as high as 12 Mbps and measures frequency to 25 MHz. Used in the design of rotating memories, it allows for the measurement of amplitude and/or frequency modulation, area defects,



pinhole defects and track-following servo performance. Driven from a counter separate from the one used in recording the clock, a bit count can be verified on a six-decimal-digit display. Price: $9895. Pioneer Magnetics, Inc., 1745 Berkeley St., Santa Monica, CA 90404. (213) 829-3305 **Circle 286**

THUMBWHEEL SWITCHES SPORT INTEGRAL LOGIC

The SF/SR Series of thumbwheel switches provides direct conversion from dial settings to coded output. Decimal and BCD, with or without complement, are standard items, and logic options integrated in the 0.315"-wide switch assembly include digital comparators, counter/timer decoders, resistance and capacitance decades, seven-segment display drivers and Kelvin-Varley dividers. Other features and options include: Wire-Wrap or solder pin terminals (for PCB mount); repositionable switch rotation stops; half bodies to add decimal point to assembly and dust windows. International Microtronics Corp., 4016 E. Tennessee St., Tucson, AZ 85714. (602) 748-7900 **Circle 285**

0.6"-HIGH LEDS DRAW 10mA/SEGMENT

With 0.6"-high numerals, the Diode-Lite LED readout modules are readable from 35 to 40 ft. The 730 Series includes a 7-segment numeral readout module with decimal point (730-6001), a plus/minus module (730-6005), and a polarity/overflow module that incorporates a plus/minus symbol, the numeral one, and a decimal point (730-6006). Typical current consumption equals 10 mA/segment. Maximum ratings for the 730-6001 at 25°C ambient include -3V reverse voltage, 30 mA/segment continuous forward current and 600 mW/segment power dissipation. Typical operating characteristics per segment include 300 μcd luminous intensity at 10 mA forward current, 200 nm spectral bandwidth between half-power points, 2V static forward voltage at 10 mA and 10 μA static reverse current at 3V. Prices in 1000s: $2.55 ea for the 730-6001, $3.10 ea for the 730-6005 and $3.10 ea for the 730-6006. Dialight, 203 Harrison Pl., Brooklyn, NY 11237. **Circle 207**

48-COL. PRINTER OUTPUTS 144 CPS

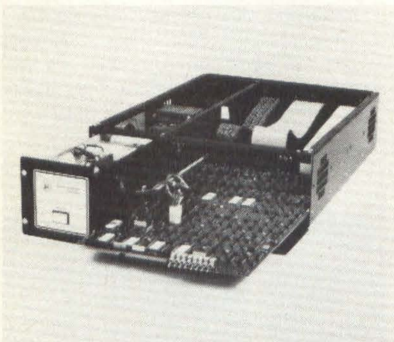
This electronic discharge printer, designated Model DC4004A, outputs 48-column lines and prints all the letters of the alphabet, digits 0 through 9 and several symbols at 3 lps (144 cps). Formed in either a 5 x 7 or 7 x 9 dot matrix, characters appear on a standard 4.75"-wide roll of aluminum-coated paper. Current in the printhead exposes the characters on a high-contrasting, permanent black undercoat. Mea-

suring 6.70" W x 5.90" Dx2.55" H and weighing 1.32 lbs, the unit serves microprocessor based systems, communications systems, miniterminals and systems that incorporate CRTs. Hycom, Inc., 16841 Armstrong Ave., Irvine, CA 92714. **Circle 214**

product news

DISK CONTROLLER SERVES PDP-11 SYSTEMS

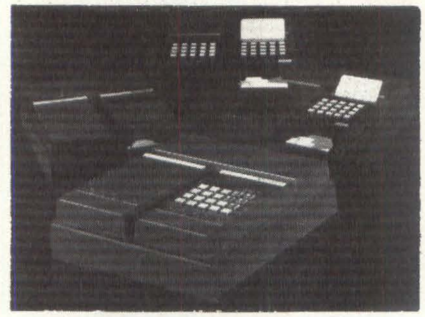
A microprocessor based controller that supports storage module devices with capacities from 25 to



300 Mbytes/spindle, the MSC-1000 handles from one to four (eight optional) drives of one type and capacity. Standard features include overlapped seeks, automatic track seek and verification, automatic head and cylinder switching, and multiple-sector transfer of adjacent sectors, tracks, and cylinders. The controller also contains a set of resident microdiagnostics. Options include extended maintenance microdiagnostics, a 32-bit polynomial error correction code that allows correction of single-error sector data bursts up to 11 bits long, an expander module for control of four more drives, expanded buffering for programmable transfer rates, and multiport operation. The unit responds to PDP-11 systems running under DEC's RSX-11D and can issue memory reference requests on the DEC Unibus. A software support package for RSX-11D includes a driver program and several RSX-11D replacement modules that let you generate a system whose system disk resides on an MSC 1000-controlled drive. Price for the controller/formatter and one host adapter: $7900. Microcomputer Systems Corp., 440 Oakmead Pkwy., Sunnyvale, CA 94086. (408) 733-4200 **Circle 218**

DATA COLLECTORS, COMM CONTROLLERS SERVE JOB-COST APPS.

This series of three programmable data collection terminals and two communications controllers include the Model 1647-1, an 8080 microprocessor based terminal that electro-optically reads punched badges, dis-



plays time of day and provides five LEDs for prompting. The 1647-2 terminal additionally reads 80-column ANSI cards and incorporates 20 user-defined keys for inputting variable data. The 1647-3 provides 40 user-defined keys and 10 LEDs. All three terminals can optionally receive data from magnetic striped badges like

credit cards, from bar codes and directly from key stations. Other options include additional 10-digit numeric displays, 32-character alphanumeric gas discharge displays, twisted pair line drivers, low-speed telephone system modem, serial asynchronous and serial synchronous communications ports and expandable ROM and RAM. The Model 1648-1 communications controller oversees up to 30 terminals on one party line, while the Model 1648-2 controller oversees up to 100 terminals on four separate party lines. Prices: $995 for the 1647-1, $1310 for the 1647-2, $1455 for the 1647-3, $1310 for the 1648-1. Epic Data Corp., c/o Kader/Brigham/Scully, 1122 S. Robertson, Suite 9, Los Angeles, CA 90035.
Circle 223

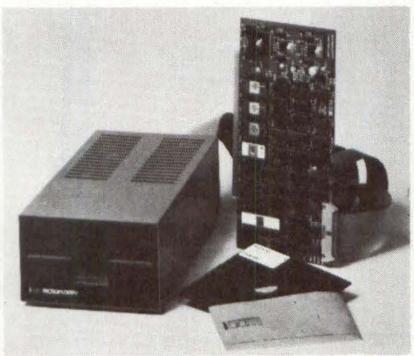
$971 CRT TERMINAL SPORTS BUFFERED PRINTER PORT

An asynchronous CRT terminal with a 12" viewing area, 24 x 80 display, upper-and lower-case characters and full cursor addressing and control, the Fox-1100 incorporates a Motorola 6800 microprocessor and provides selectable black-on-white or white-on-black display, a 9 x 12 dot matrix and a hooded screen. It is upward program-compatible with the ASR-33 Teletype and the Carousel 15, 30 and 35 printing terminals, and its Typamatic keyboard automatically repeats an entry at 15 cps if a key is held

down more than 0.5 sec. The unit also incorporates a fully buffered printer port. Price: $971 in quantities of 25. Perkin-Elmer Data Systems, Terminals Div., Rte. 10 and Emery Ave., Randolph, NJ 07801. (201) 366-5550 **Circle 229**

5¼"-FLOPPY SYSTEM MATES WITH ALTAIR-TYPE MICROCOMPUTER BUSES

With operating software and interface electronics that provide plug-compatibility with microcomputers that use the Altair bus, the Microfloppy uses 5-¼" diskettes and incorporates a Shugart Minifloppy flexible-disk drive, power supply, cabinet, controller/interface card, power cord, fuse and all cables. It also provides the manufacturer's FDOS-M software on diskette and, as an introductory offer, an 8K Basic software package. The system's controller/interface card contains an LSI chip that offers automatic track seek with verification, single or multiple record read/write with automatic sector search, entire track read and entire track write for diskette initialization. The



card also incorporates on-board ROM and RAM. The system's software includes a macro assembler, a string-oriented text editor and a diskette initializer; capabilities include named variable-length files, auto file create, open and close, and multiple-file merge and delete. iCom Div., Pertec, 6741 Variel Ave., Canoga Park, CA 91303. (213) 348-1391 **Circle 210**

DC/DC POWER SUPPLIES OUTPUT UP TO 300 V

These dc/dc proportional high-voltage power supplies, designated Series H, sport 4-12 Vdc input voltage, 3500 V input-to-output isolation, 60% typical efficiency and 100% encapsulation. You can mount them in two through holes, using PC pins as terminals. Price: $51 for 1-9. Wall Industries, Inc., 175 Middlesex Turnpike, Bedford, MA 01730. (617) 275-0708 **Circle 227**

CIRCLE 57 ▶

product news

150-CPS PRINTER OUTPUTS 6 COPIES

Model 810, a 150-cps printer, serves applications that include output printing for minicomputer and microprocessor systems, auxiliary forms printing for intelligent CRT terminals and remote office output printing in data communications systems. A 132-column, multicopy unit, the system provides microprocessor control of printing functions, programmable forms control and a 256-character buffered communications interface. The unit generates the standard 64 ASCII character set using a 9 x 7 dot pattern; other standard features include self-test, an adjustable tractor drive for form widths ranging from 3" to 14-7/8", line-spacing selection of six or eight lpi, the ability to feed continuous forms from the printer's rear or its bottom, and power selection of 100, 120, 220 or 240 Vac at 50-60 Hz. Options include full ASCII character set, compressed-character printing and either 11 form lengths for standard forms usage or vertical forms control with up to eight nonvolatile programs. Price: $2250 in singles. Texas Instruments, Digital Systems Div., P.O. Box 1444, M/S 784, Houston, TX 77001. (713) 494-5115, x 2124 **Circle 212**

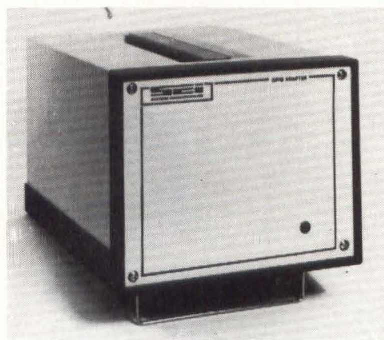
2-DRIVE FLOPPY SYSTEM SERVES PDP-8 MINIS

For PDP-8 systems, the 6200LP double-density diskette system incorporates a DMA-type interface

and an OS-8 Version 3 driver that lets it serve as a mini's system residence device. It provides 1.26 Mbytes of program or data storage on two drives; you can also obtain a four-drive system. Price: $3900 in singles for the 6200LP with DMA interface; $850 for the OS-8 driver. Quantity discounts up to 40% available. Advanced Electronics Design, 754 N. Pastoria, Sunnyvale, CA 94086. (408) 733-3555 **Circle 217**

INTERFACE ADAPTER LINKS RS 232 AND IEEE 488 SYSTEMS

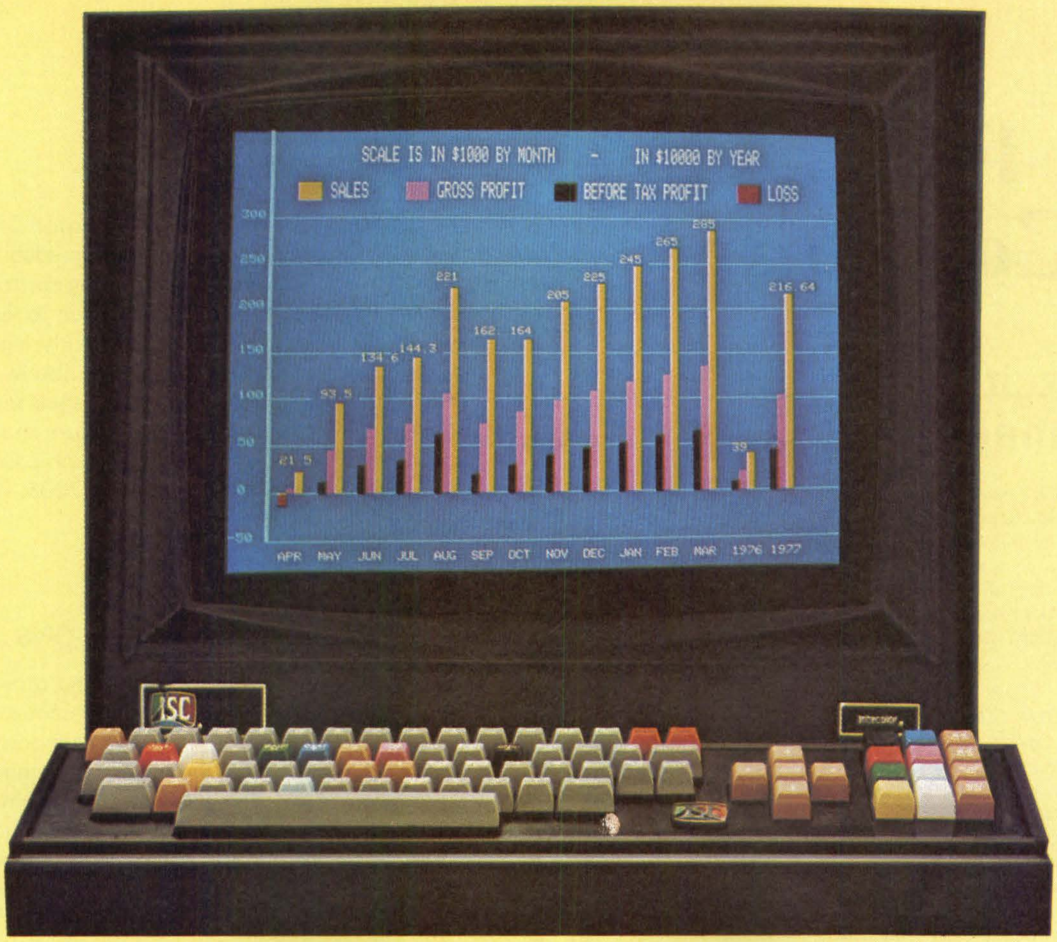
Model 111 adapter lets you interconnect the IEEE parallel GPIB (general-purpose interface bus) with RS 232C systems. It provides two-way transmission of data and can be used to adapt older instruments and terminals, designed to RS 232C



standards, to control and processing systems that use the newer GPIB parallel format. Systems Consultants, 410 Jericho Tpke., Jericho, NY 11753. (516) 822-5500 **Circle 209**

MASS-TERMINATION KIT AIDS BREADBOARDING

The DK-1 mass termination flat cable/connector kit provides engineering evaluation and prototype fabrication aid and contains an assortment of over 100 of the manufacturer's Blue Macs insulation displacing connectors, including DIP plugs, DIP sockets, PCB solder transition connectors, wrap post solder connectors, PCB solder tail and wrap post tail headers. You also get a 100-ft roll of 28 AWG stranded 50-conductor cable and a hand installation tool for crimping the connectors on the cable, as well as installation instructions and technical data. Price: $395. T&B/Ansley Corp., 3208 Humboldt St., Los Angeles, CA (213) 223-2331 **Circle 215**



Unretouched photograph of screen.

product news

ANTI-GLARE PANELS SHIELD CLINTON CRTS

Placed against the faceplate of a Clinton CRT, the Video/Filter improves the display's readability by eliminating reflections and increasing contrast. It reduces front-surface specular reflection to less than 1% and can accept printed-on custom grids, legends, reference lines and graticules. You can obtain the filter with a pressure-sensitive adhesive; panels serve all the Clinton CRT sizes and phosphor colors and most standard JEDEC tube sizes. Panelgraphic Corp., 10 Henderson Dr., West Caldwell, NJ 07006. (201) 227-1500 **Circle 201**

16-BIT MINICOMPUTER ADDRESSES UP TO 64 ADD-ONS

For use in small business systems and other applications, the Micro 16E minicomputer comes in either a 5¼"-high rack-mount unit or a table-mount cabinet. It can address up to 64 peripherals and incorporates such features as automatic bootstrap, memory partitioning, multilevel interrupts, real-time clock and DMA. Instruction time for the 16-bit processor equals 1 μs (minimum); it addresses 16K or 32K bytes of semiconductor memory, expandable to 128K bytes. Software includes assembler, Extended Basic compiler, Mathchat interpreter, multiprogramming executive and test and utility programs. Digico Ltd., Wedgwood Way, Stevenage, Hertfordshire SG1 4PY, England. (0438) 4381

MINIATURE SWITCHING SUPPLIES PROVIDE 4KV RMS ISOLATION

Designated Series MMG, these switching power supplies operate from 110/120 Vac or 220/240 Vac ±10%, 50 or 60 Hz, and use optical coupling to provide 4kV rms isolation (5.7kV peak) between input and output. You can adjust their output voltages by ±10% with a multi-turn potentiometer. Four models provide dc outputs of 5, 12, 15, or 24V at currents ranging from 1.4 to 5 A. The units' voltage regulation measures 0.1% max for the worst case combination of 0-100% load change and ±10% line change. Ripple remains below 10mV rms or 50mV peak-to-peak measured over a 30 MHz bandwidth. Transient response for a step-load change of 100% to 10% or 10% to 100% allows a typical voltage deviation of 300mV and a return to the regulation band in approximately 2 ms. With efficiencies ranging from 75% to 85%, the units weigh 1.2 lbs and measure 6.3" x 3.5" x 1.3". Price: $125 for 1-9. Gould, Inc., Power Supply Dept., 3631 Perkins Ave., Cleveland, OH 44114. (216) 361-3315
Circle 203

LIGHTED PUSHBUTTON SWITCH INCORPORATES INTERNAL WATER SEAL

The 419 Series lighted pushbutton switch incorporates an internal silicone rubber gasket that seals the switch's lamps and prevents water from entering its front panel. A 4-lamp, 4-pole, 0.750"-square unit, the switch has stationary lamps that you can replace from the front. Its cap has a retaining wire to prevent loss while relamping and a slide-off cap shell that facilitates legend change. The unit meets MIL-S-22885 requirements and could find uses in portable test equipment used outdoors. Korry Manufacturing Co., 223 8th Ave. North, Seattle, WA 98109. (206) 223-5400

Circle 202

CCD ANALOG SHIFT REGISTER STORES ONE VIDEO SIGNAL LINE

This solid state analog shift register can store the video information for one complete horizontal line of a standard U.S. broadcast television signal. Designated the CCD321, it utilizes CCD technology and consists of two independent 455-bit analog shift registers that you can combine for use as a 910-bit analog delay line. The delay of analog information from input to output depends exclusively on the applied external clock frequency; with a 14.318-MHz sampling and shifting clock frequency you can store one 63.5-μs tv line in 910 bits. Fixed clock frequency operation provides fixed delay of information with an input bandwidth greater than 5 MHz, a signal-to-noise ratio of 55dB and differential gain and phase of 3% and 3° respectively. The device's delay ranges from 25μs to 50 ms. Fairchild Camera and Instrument, MOS/CCD Products Div., 4001 Miranda Ave., Palo Alto, CA 94304. (415) 493-8001 **Circle 294**

1K CMOS RAMS ACCESS IN 250 NS

For μP-based POS systems, portable instruments and electronic cash registers, the MM54C920/MM74C920 and MM54C921/MM74C921 CMOS RAMs each store 256 x 4 words. The MM74C920 comes in a 22-pin package and has separate Data In and Data Out, while the MM74C921 is an 18-pin device with common I/O. Each device accesses in 250 ns (commerical version). Data output and input have the same polarity in both devices; address inputs, CES and data inputs are clocked into internal latches by the falling edge of STROBE. The true and complement address information goes to row and column decoders, which access the selected 4-bit memory word, which in turn goes to four sense amplifiers through the column decoders. Standard 54/74 TTL supplies power the units, and all inputs and outputs can interface directly with TTL. Price: $12.15 (100s) for the MM74C920 and MM74C921, and $20.10 (100s) for the military temperature range parts, MM54C920 and MM54C921. National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. (408) 737-5892

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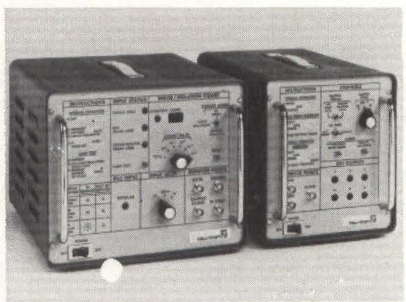
If writing is not your forte and you have something of interest for our readers, why not let us work with you in organizing your material for publication. Just drop a note to the Editor or call (617) 232-5470.

product news

TRANSMITTER/RECEIVER TESTS T3 LINKS

A field portable test set for T3 communications links, the S-5200C transmitter/receiver pair incorporates a crystal oscillator that operates at 44.736 MHz and generates a 32,767-bit pseudo-random code. The transmitter also includes a controller to generate the F, P, C and M housekeeping bits of the DS-3 format. Six data outputs provide B3ZS encoded bipolar data; three output levels provide 0.9V peak, 0.4V peak



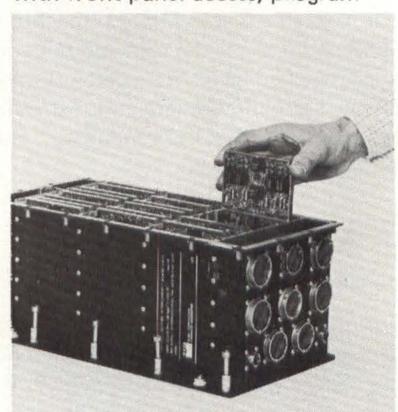
(simulation of 450 ft of 728A cable) and 0.2V peak. The transmitter also injects bit errors, code violations and parity violations. The receiver recovers clock and synchronizes on both the DS-3 framing bits and the pseudo-random data. After synchronization, it counts bit errors, bipolar violations or parity errors, totalized or calculated as an error rate ranging from 10^{-3} to 10^{-8}. Price: $6800. Tau-Tron, 11 Esquire Rd., N. Billerica, MA 01862. (617) 667-3874 **Circle 208**

MODEM ELIMINATOR OPERATES TO 19.2 KBPS

Model ME-1 modem eliminator permits direct terminal-to-terminal or terminal-to-computer connection and eliminates the need for two modems operating back-to-back. Signal regeneration permits extension of the 50-ft EIA RS 232 interface limitation between devices. The unit provides synchronous operation in half- or full-duplex modes with selectable data rates of 1800, 2000, 2400, 4800, 7200 and 9600 bps and 19.2 kbps. An internal crystal controlled clock provides transmit and receive timing elements; request-to-send can be continuous or terminal controlled, and the clear-to-send delay is selectable at 0, 8, 50 or 150 ms. Front-panel LEDs show status, and digital loopback permits fault isolation. Cooke Engineering Div., Dynatech Laboratories, Inc., 900 Slaters Lane, Alexandria, VA 22314. (703) 548-3889 **Circle 222**

DATA ACQUISITION SYSTEM EXPANDS TO 512 CHANNELS

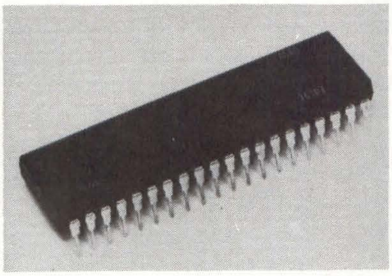
Model 7-201 data acquisition/signal conditioning system accepts high- or low-level input signals. You can specify channel capacity and enclosure size; the system expands in blocks of 16 or 32 channels to a maximum of 512 channels in one enclosure. The system incorporates a microprocessor based controller equipped with field programmable EPROMs; its output is a serial data stream that you can program for sample rate, work length and sample sequence. System features include programmable "gain" and "offset" with front panel access, program-



mable digital filters, 16 bit A/D capability and free running or addressable capability. Current applications include flight test monitoring, engine mounted multiplexing, vibration monitoring, wind tunnel data acquisition and aircraft maintenance systems. Specifications include 24 to 32 Vdc, 110V/60 Hz or 110V/400 Hz operation; one bps to one Mbps output rate; 4- to 20-bit word length; one- to 1000-sps channel sampling rate. Data and Control Group, Eldec Corp., 16700 - 13th Ave. W., Lynwood, WA 98036. (206) 743-1313 **Circle 221**

DUAL UP/DOWN COUNTER USES DC TO 350 KHZ

A synchronous, dual 3-decade or 6-decade up/down counter that outputs all BCD data in parallel, the LS-7040 operates from dc to 350 kHz, comes with output latches and provides a carry/borrow output for synchronous or asynchronous cascading

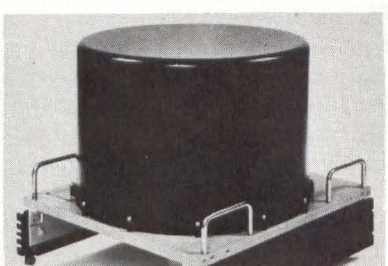


with another LS7040. All inputs are CMOS, TTL and DTL compatible at +5V operation and all I/O signals are CMOS compatible over the entire voltage range. Other features include separate low-current drain power supply, power-on-reset, reset and count enable inputs. The circuit can operate from either a single power supply that outputs between +5 and +15 Vdc, or from two supplies in battery standby mode. It comes on a 40-pin DIP. Price: $7.50 in 100s. LSI Computer Systems, Inc., 1235 Walt Whitman Rd., Melville, NY 11746. (516) 271-0400

Circle 228

FIXED-HEAD DISK FOR RUGGED COMPUTERS

This MIL-Spec fixed-head disk memory system serves the manufacturer's 1600 Series rugged computers. Model 3343 disk controller interfaces and controls Model 3344 and 3345 MIL-Spec disks, which access in 8.5 ms (min.). RDOS soft-



ware support provides multi-tasking in both foreground and background as well as program overlay and spooled I/O. It also provides such facilities as compilers (including 1664 Fortran), assemblers, editors, utilities, math libraries, file handling capability and data base management capability. Price: $7000 for the Model 3343 disk controller; $19,000 up for the Model 3344 and 3345 disk memory units. Rolm Corp., 18922 Forge Dr., Cupertino, CA 95014. (408) 257-6440 **Circle 211**

FLOPPY-DISK DRIVE SPORTS POWER-SAVER

Designated Model 550, this floppy-disk drive serves such OEM information processing applications as data entry, small business systems, computer terminals and mini/microcomputers. It records up to 800K bytes of unformatted data or 234K bytes in IBM 3740 format; with an appropriate controller, it can operate in double bit density mode without modification or additional electronics. A power-saver feature reduces head positioner power by 95% within 15 ms of the last stepping command. Options include a second index transducer to allow recording on the reverse side of a flipped-over disk, file-busy indicator, write protect, hard-sector separator and data/clock separator. Memorex Corp., San Tomas at Central Xway, Santa Clara, CA 95052. (408) 987-2203 **Circle 206**

PAPER-TAPE INTERFACE KIT SERVES LSI-11 MICROS

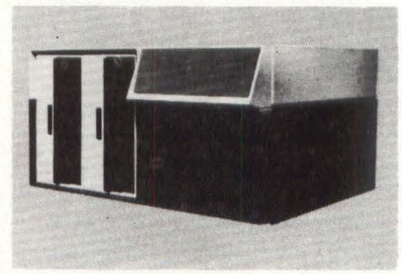
For interfacing DEC LSI-11 computers and the manufacturer's punched tape readers and reader/punches, this kit includes a circuit card, interconnecting 10-ft cables, test tape and instruction manual, which contains diagnostic programs. You can use existing software detailed in the PDP-11 handbook to program the interface to specific system applications. The circuit board plugs into the computer's backplane bus, and the interface's peripheral device address and interrupt vector are jumper selectable. Price for Kit E-9000-LSI-RP: $250 in singles. EECO, 1441 E. Chestnut Ave., Santa Ana, CA 92701. (714) 835-6000

Circle 225

product news

FLOPPY-DISK SYSTEM CONTROLS BUS

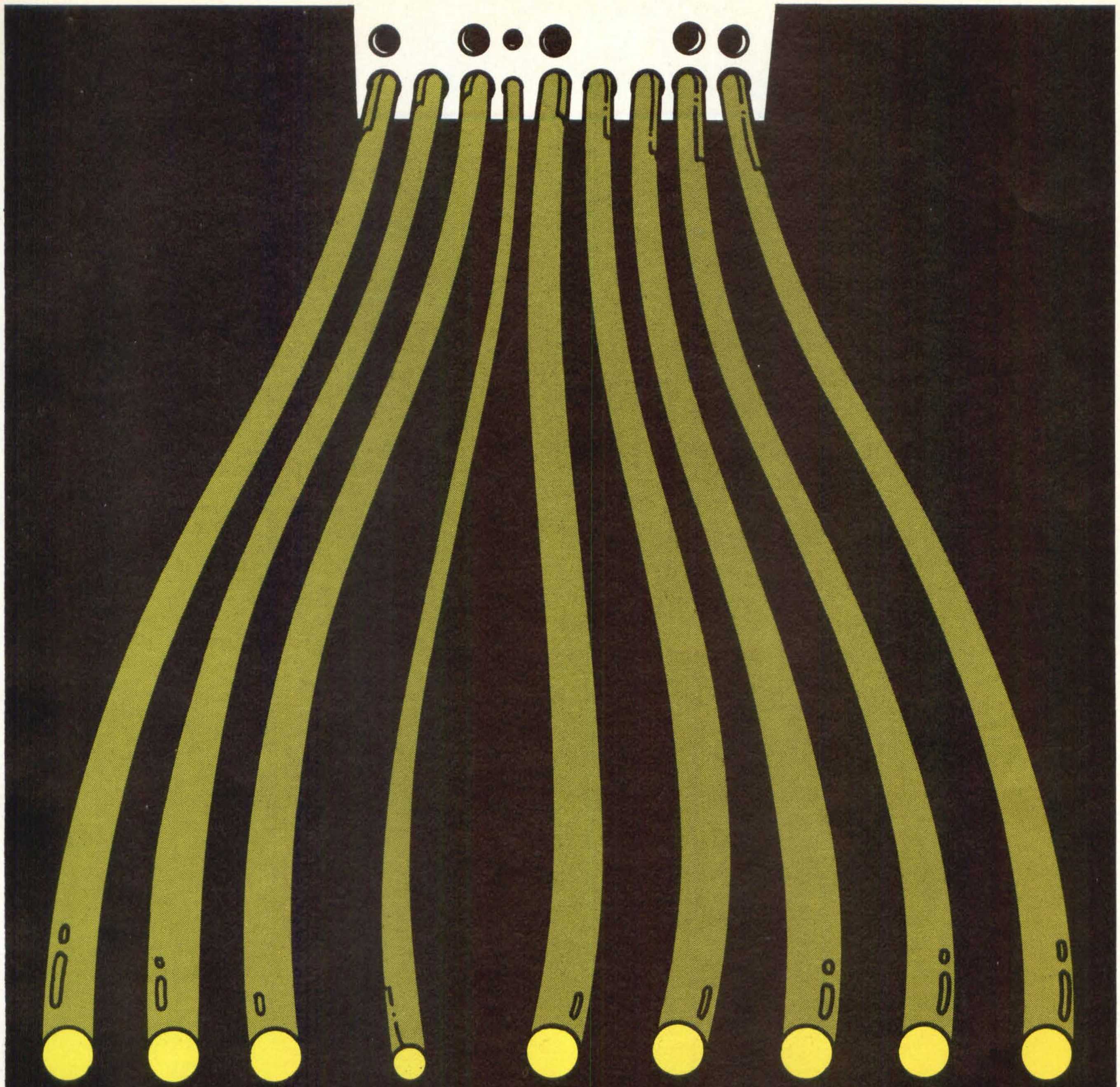
Model 3300 Dual Floppy Plus serves as a disk memory with file maintenance capability for the Tektronix 4051 graphic system and can also function as a dual-processing, disk-based system or a standalone, Basic-language GPIB/HPIB bus controller. It incorporates a Z-80 based processor with 4K bytes of ROM,



16K to 61K bytes of semiconductor workspace memory, two 308K byte floppy disks, an RS 232C interface, four 4051 bus interfaces and disk operating systems. It connects to the Tektronix 4051 to provide 608K bytes of disk memory with complete transparency to the 4051 tape and disk commands. Operating as a standalone system, it can hand control back and forth to another controller; an RS 232C port allows the connection of an operator's terminal. Price: $6950. Second Source Industries, 906 Treat Ave., San Francisco, CA 94110. (415) 282-1171 **Circle 220**

MULTIPLEXED LCDS FOR PORTABLE SYSTEMS

This multiplexed, 4-digit, liquid crystal instrument display, designated Model 3624, serves applications in portable and panel mounted digital displays. Each digit, electrically isolated with separate backplanes, allows sequential 7-segment driving. You can also obtain the 4LDD-7, a latch configuration of the same display with drive and display that requires only BCD or pulse counting input. Price for the 3624: $13 ea in 100s. UCE, Inc., 20 N. Main St., Norwalk, CT 06854. (203) 838-7509 **Circle 213**



COMING IN APRIL

"What's Ahead In CRT Terminals?"

"Improving CRT-Module Performance in Today's CRT Terminals"

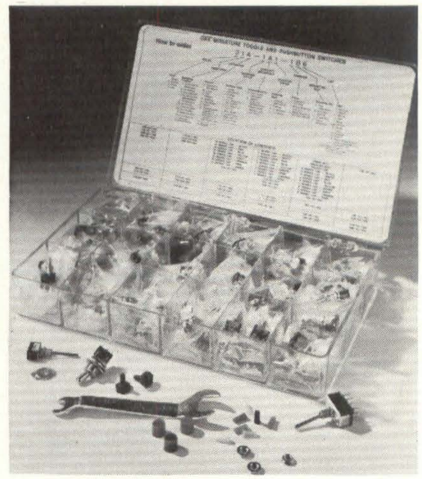
"CRT-Terminal Review: A Product Sampler"

"Balancing µP-Interface Tradeoffs"

product news

286-PIECE KIT SAMPLES SWITCHES

This 286-piece kit of miniature toggle and pushbutton switches with complementary caps, dress nuts and wrench comprises single, double, three and four-pole switches with several types of toggle and pushbutton actuators. The inside top cover of its transparent plastic case contains a chart that shows how to specify the type of pole configura-



tion, switching function, actuator and terminal style, contact material, bushing, finish, mounting nut and cap desired. All switches conduct 6 A @ 125 Vac and come with solid silver contacts standard; two other contact types are optional. Both U.L. and C.S.A. listings are available. Insert-molded or epoxy-sealed terminals eliminate solder flux contamination: three of the six terminal styles serve PC mounting. Price: $87.50. Oak Switch Div., Crystal Lake, IL 60014. (815) 459-5000

Circle 219

36"-WIDE PLOTTERS RESOLVE 200 DOTS/IN

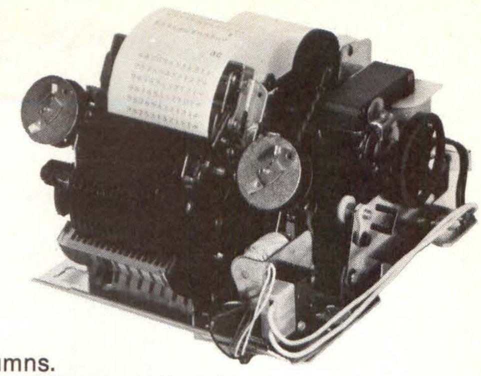
These two computer plotters produce 36"-wide E-size drawings electrostatically. Model 8136 plots at paper speeds of up to two ips; Model 8236 plots at 0.75 ips but offers twice the resolution — 200 dots/linear inch. Designed to replace or supplement pen plotters, the electrostatics plot a raster of data across 32.20" in one scan, can shade, tone or draw variable line widths with one command, and can produce continuous plots up to 500 ft long. Both models include self-diagnostics that let you test board-by-board without external test gear; integral self-diagnostics test write timing, input clock, data timing and shift registers. Both models measure 40" H x 63" W x 34" D; optional paper take-up winder adds 12" and extension table adds 48." Prices: $25,000 for Model 8136, $34,500 for Model 8236. Versatec, 2805 Bowers Ave., Santa Clara, CA 95051. (408) 988-2800 **Circle 226**

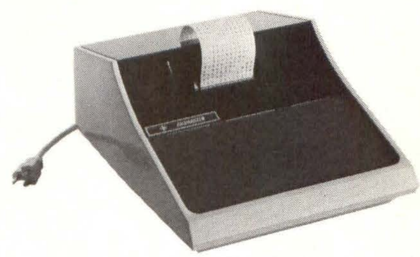
CMOS COUNTER/TIMER CLOCKS ON DC TO 1 MHZ

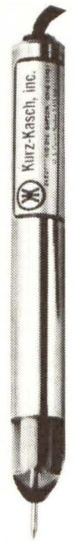
This CMOS 4-decade unit has five wire connections that supply power, input and output signals, and reset to form a complete up/down counter used for timing or length measurement. The counter can operate on clock frequencies ranging from dc to greater than one MHz; you program its count through a pushbutton digiswitch. The unit mounts on a front panel. Price: $65 ea in 100s. Adaptive Systems, P.O. Box 1481, Pompano Beach, FL 33061. (305) 942-4000 **Circle 216**

10 x 10 MEMORY KIT AIDS CONTROL-PROGRAM DEVELOPMENT

This 10 x 10 mini memory matrix allows manual programming for prototyping of solid state sequential control applications. In kit form, it comes with 10 diode holders, 10 shorting pins and 20 terminations. TTL and CMOS compatible, the matrix can also serve as a simplified memory device for use with microprocessors and other solid state controllers. You program binary information by inserting diode pins into the matrix board and producing a logic 1 or 0 at the output side of the board. Capacity equals ten 10-bit words; you can link additional matrices together for added memory capacity. You can also obtain custom matrices with 8, 16 or 32 bits. Programming Devices Div., Sealectro Corp., Mamaroneck, NY 10543. **Circle 224**







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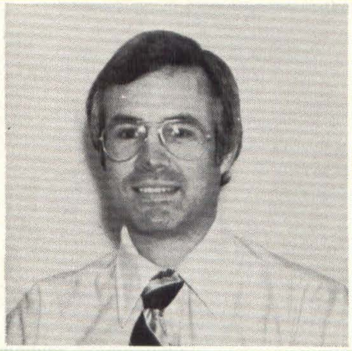
The μP Supermarket: Off-The-Shelf Buys or Customized Orders?



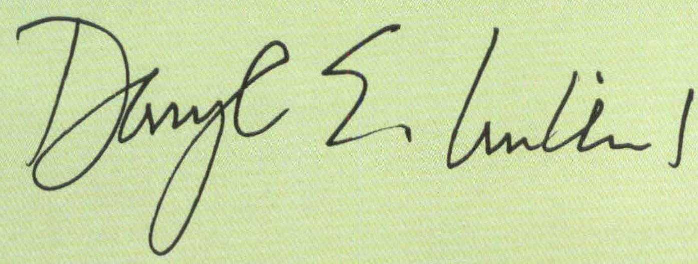
The pressure is on today's designers to add sophisticated features to their products with the aid of LSI circuitry. But in your haste to keep pace with market trends, don't blindly jump on the microprocessor bandwagon. You've heard this advice before, but it bears repeating. For even if you decide after careful study to rely on a microprocessor to update a product, you may still face difficult choices.

For example, should you choose a standard, off-the-shelf microprocessor set or design and build a custom unit? Complicating the answer to this question are two emerging trends: the growing catalog list of standard, general-purpose microprocessors, associated circuits and options; and the introduction of "specialized" microprocessors, also available off the shelf but designed for use in specific classes of applications.

One such specialized circuit, an "appliance" microcomputer, serves the white-goods industry. Another, a programmable, six-function watch circuit, offers seconds, minutes, hours, day, date and stop-watch modes, and time-zone features. Programming the on-board ROM of either circuit customizes the circuit for a particular set of features.

There's also a third option. Some designers want their own set of bells and whistles and can afford them because of their products' volume production. They can justify the development expense of a custom microprocessor and thereby obtain a cost-effective chip. Custom microprocessors provide maximum utilization of chip real estate and point to maximized capability, no overkill and no need for peripheral circuits.

The next two years will spotlight the continued development of circuits for special market segments and the subsequent broadening of product designers' options. So remember this lesson: Don't automatically latch onto the newest, "sexiest" and most widely publicized general-purpose microprocessor. It's not the only alternative. Standard, specialized and custom microprocessors each serve important market segments.



Daryl Mullins *is product marketing manager for automotive and appliance circuits at American Microsystems, Inc. (AMI), Santa Clara, CA. We will be pleased to provide space for opposing views.*

CIRCLE 2

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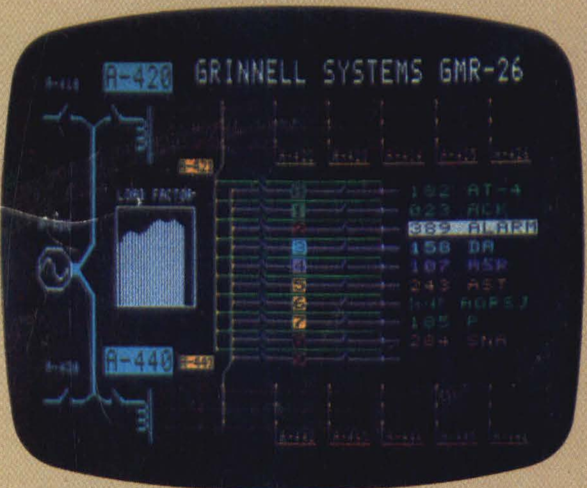

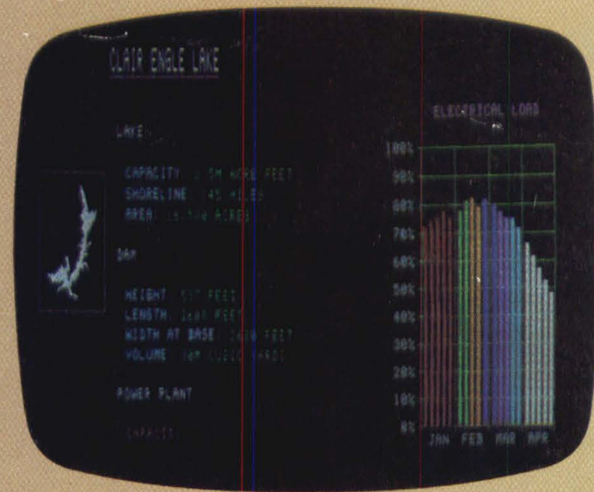

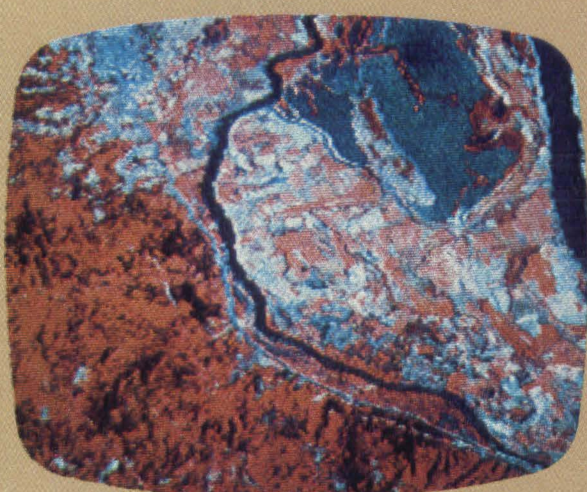

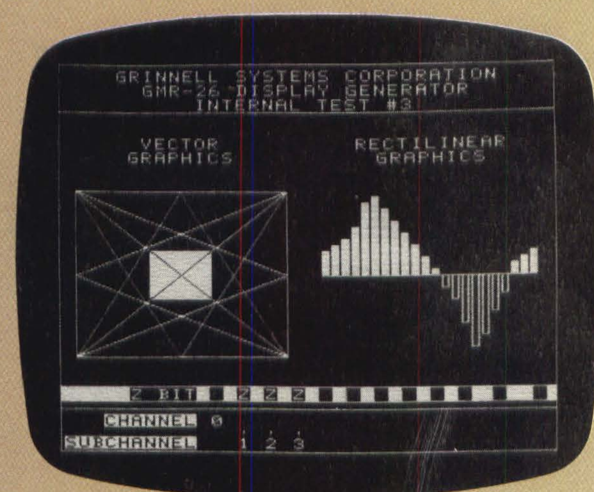

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