X20CM8281

1 General information

The module is a universal mixed module. On this module, digital I/O and analog I/O are combined. A current or voltage signal can be used for the analog I/O as desired. Counter functions on two of the digital inputs expand the range of use.

- Digital and analog channels
- Selectable current and voltage for AI and AO
- Counter functions

2 Order data

Model number	Short description	Figure
	Other functions	
X20CM8281	X20 universal mixed module, 4 digital inputs, 24 VDC, sink, 1-wire connections, 2 digital outputs, 0.5 A, source, 1-wire connections, 1 analog input, ±10 V or 0 to 20 mA / 4 to 20 mA, 12-bit converter resolution, 1 analog output, ±10 V / 0 to 20 mA, 12-bit converter resolution, 2 counters as event counters or gate measurement	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O supply continuous	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20CM8281 - Order data

3 Technical data

Model number	X20CM8281
Short description	
I/O module	4 digital inputs, 2 digital outputs, 1 analog input, 1 analog output, special functions
General information	
B&R ID code	0x24C3
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Analog inputs	Yes, using status LED and software
Digital outputs	Yes, using status LED and software (output error status)
Power consumption	
Bus	0.01 W
Internal I/O	1.75 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
Digital inputs	
Quantity	4
Nominal voltage	24 VDC
Input characteristics per EN 61131-2	Type 1
Input voltage	24 VDC -15 % / +20 %
Input current at 24 VDC	Typ. 3.3 mA
Input circuit	Sink
Input filter	
Hardware	≤2 µs
Software	Default 1 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Connection type	1-wire connections
Input resistance	Typ. 7.18 kΩ
Additional functions	20 kHz event counting, gate measurement
Switching threshold	
Low	<5 VDC
High	>15 VDC
Isolation voltage between channel and bus	500 V_{eff}
Event counters	
Quantity	2
Signal form	Square wave pulse
Evaluation	Each falling edge, cyclic counter
Input frequency	Max. 20 kHz
Counter 1	Input 1
Counter 2	Input 3
Counter frequency	Max. 20 kHz
Counter size	16-bit
Gate measurement	
Quantity	1
Signal form	Square wave pulse
Evaluation	Rising edge - falling edge
Counter frequency	
Internal	48 MHz, 24 MHz, 12 MHz, 6 MHz, 3 MHz, 1.5 MHz, 750 kHz, 375 kHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 4
Analog inputs	
Quantity	1

Table 2: X20CM8281 - Technical data

Model number	X20CM8281
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections
Input type	Single ended
Digital converter resolution	
Voltage	±12-bit
Current	12-bit
Conversion time	400 µs, conversion runs asynchronously to the X2X Link cycle
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Input impedance in signal range	
Voltage	>1 MΩ
Current	-
Load	
Voltage	-
Current	<300 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±15 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	Successive approximation
Input filter	2nd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% 1)
Offset	0.02% 2)
Current	
Gain	0 to 20 mA = 0.08 % / 4 to 20 mA = 0.1 % 1)
Offset	0 to 20 mA = 0.03 % / 4 to 20 mA = 0.16 % 3)
Max. gain drift	
Voltage	0.01 %/°C 1)
Current	0 to 20 mA = 0.009 %/°C 4 to 20 mA = 0.0113 %/°C 1)
Max. offset drift	
Voltage	0.002 %/°C 2)
Current	0 to 20 mA = 0.004 %/°C 4 to 20 mA = 0.005 %/°C 3)
Nonlinearity	
Voltage	<0.02% 2)
Current	<0.02% 3)
Isolation voltage between channel and bus	500 V_{eff}
Digital outputs	
Quantity	2
Variant	FET positive switching
Nominal voltage	24 VDC
Switching voltage	24 VDC -15 % / +20 %
Nominal output current	0.5 A
Total nominal current	1 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
$R_{DS(on)}$	105 mΩ
Peak short-circuit current	<14 A
Switch-on in the event of overload shutdown or short-circuit shutdown	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 → 1	<250 µs
1 → 0	<270 µs
Switching frequency	
Resistive load	Max. 100 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	Typ. 50 VDC
Isolation voltage between channel and bus	500 V_{eff}

Table 2: X20CM8281 - Technical data

Model number	X20CM8281
Analog outputs	
Quantity	1
Output	±10 V or 0 to 20 mA, via different terminal connections
Digital converter resolution	12-bit
Conversion time	300 µs, conversion runs asynchronously to the X2X Link cycle
Settling time for output changes over entire range	1 ms
Switch on/off behavior	Internal enable relay for booting and errors
Max. error at 25°C	
Voltage	
Gain	0.04% 4)
Offset	0.0225% 5)
Current	
Gain	0.05% 4)
Offset	0.125% 5)
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0010 = 4.882 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0010 = 9.766 µA
Load per channel	
Voltage	Max. ±10 mA, load ≥ 1 kΩ
Current	Max. load is 400 Ω
Max. gain drift	
Voltage	0.012 %/°C 4)
Current	0.014 %/°C 4)
Max. offset drift	
Voltage	0.0075 %/°C 5)
Current	0.03 %/°C 5)
Error caused by load change	
Voltage	Max. 0.02%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 400 Ω, resistive
Nonlinearity	<0.1% 6)
Isolation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Derating"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 2: X20CM8281 - Technical data

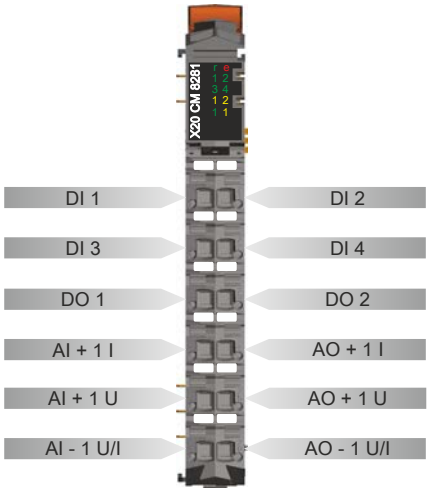
1) Based on the current measured value.
2) Based on the 20 V measurement range.
3) Based on the 20 mA measurement range.
4) Based on the current output value.
5) Based on the entire output range.
6) Based on the output range.

4 LED status indicators

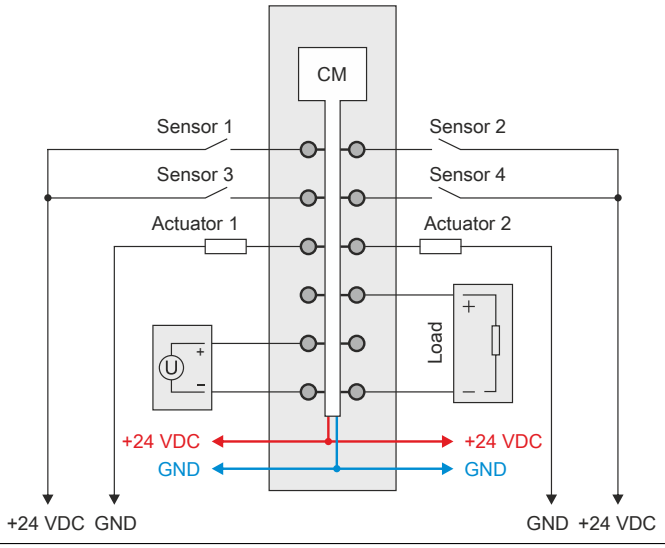
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" of the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green		Input state of the corresponding digital input
	1 - 2	Orange		Output status of the corresponding digital output
	1	Green	Off	Open line or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK
	1	Orange	Off	Value = 0
			On	Value ≠ 0

5 Pinout

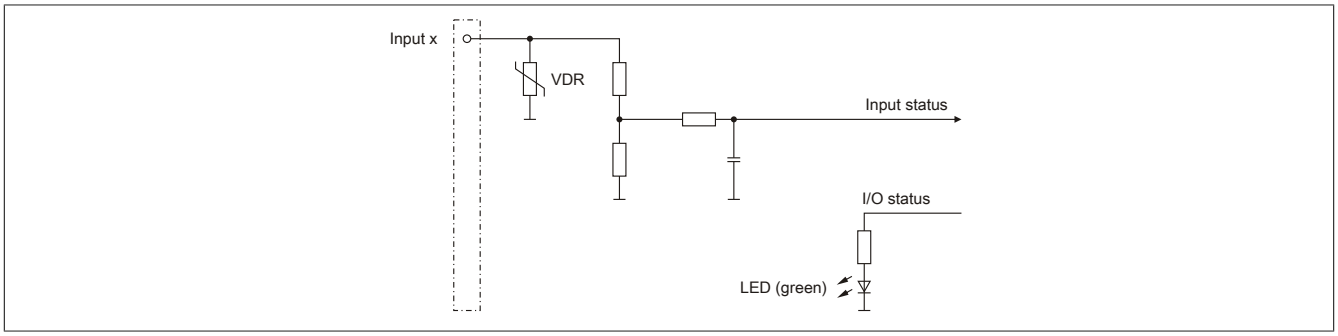


6 Connection example

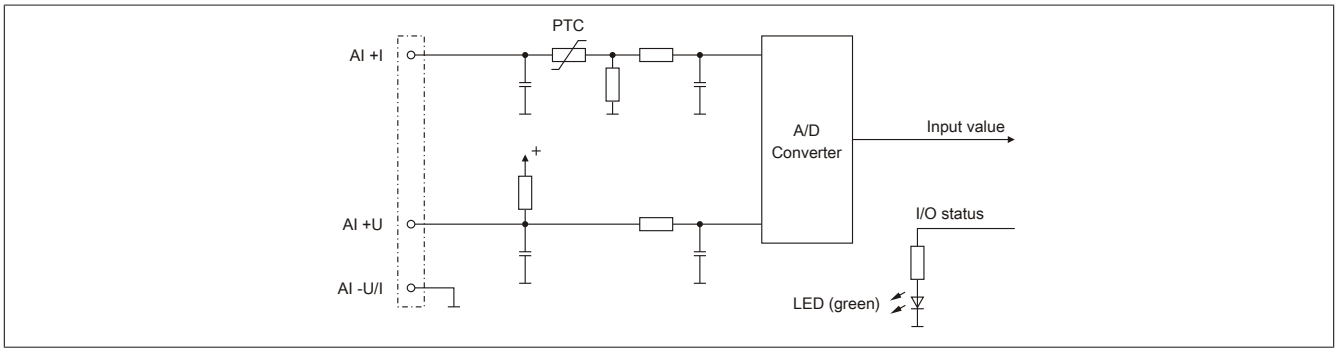


7 Input circuit diagram

Digital inputs

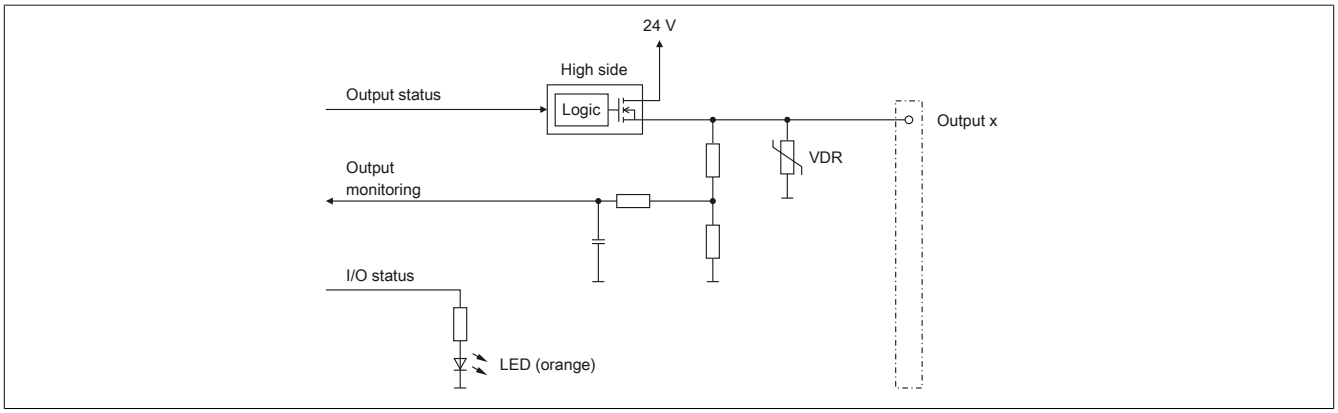


Analog inputs

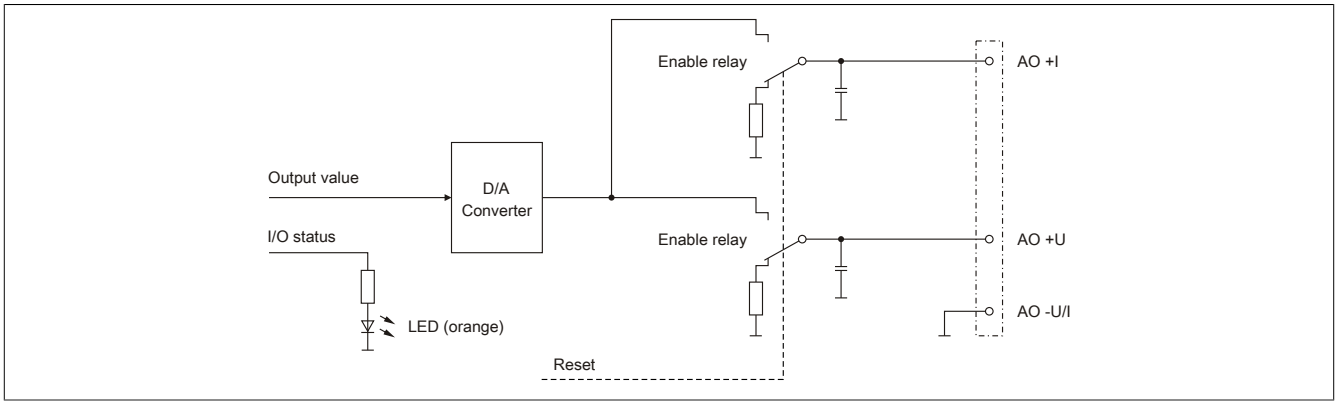


8 Output circuit diagram

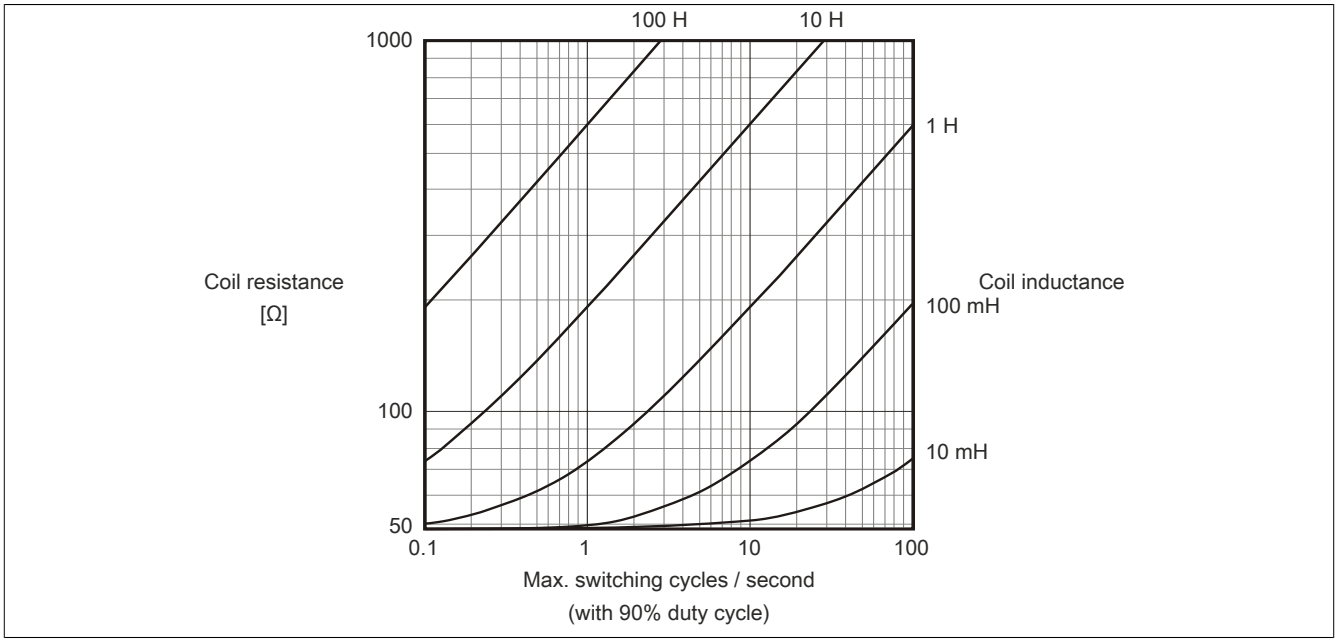
Digital outputs



Analog outputs



9 Switching inductive loads

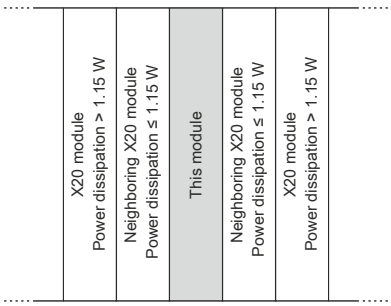


10 Derating

There is no derating when operated below 55°C.

During operation over 55°C, the power dissipation of the modules to the left and right of this module is not permitted to exceed 1.15 W!

For an example of calculating the power dissipation of I/O modules, see section "Mechanical and electrical configuration - Power dissipation of I/O modules" in the X20 user's manual.



11 Register description

11.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" of the X20 system user's manual.

11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
12	ConfigOutput01 (digital input filter)	USINT				•
14	ConfigOutput02 (counter configuration)	USINT				•
22	ConfigOutput03 (analog input filter)	USINT				•
24	ConfigOutput04 (configure analog input/output)	USINT				•
26	ConfigOutput05 (lower limit value)	INT				•
28	ConfigOutput06 (upper limit value)	INT				•
Communication						
Digital inputs						
0	Digital inputs	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput04	Bit 3				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
14	Reset counter	USINT			•	
	ResetCounter01	Bit 4				
	ResetCounter02	Bit 5				
16	Input state of digital latch inputs 1 - 4	DINT	•			
	DigitalInput01Latch	Bit 0				
	...	...				
	DigitalInput04Latch	Bit 3				
18	Acknowledge digital inputs	USINT			•	
	DigitalInput01LatchQuit	Bit 0				
	...	...				
	DigitalInput04LatchQuit	Bit 3				
Digital outputs						
0	Status of the digital outputs	USINT	•			
	StatusDigitalOutput01	Bit 4				
	StatusDigitalOutput02	Bit 5				
2	Switching state of digital outputs 1 to 2	USINT			•	
	DigitalOutput01	Bit 0				
	DigitalOutput02	Bit 1				
Analog input						
8	AnalogInput01	INT	•			
31	StatusInput01	USINT	•			
Analog output						
10	AnalogOutput01	INT			•	

11.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
12	-	ConfigOutput01 (digital input filter)	USINT				•
14	-	ConfigOutput02(counter configuration)	USINT				•
22	-	ConfigOutput03 (analog input filter)	USINT				•
24	-	ConfigOutput04 (configure analog input/output)	USINT				•
26	-	ConfigOutput05 (lower limit value)	INT				•
28	-	ConfigOutput06 (upper limit value)	INT				•
Communication							
Digital inputs							
0	0	Digital inputs	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput04	Bit 3				
4	2	Counter01	UINT	•			
6	4	Counter02	UINT	•			
14	-	Reset counter	USINT				•
		ResetCounter01	Bit 4				
		ResetCounter02	Bit 5				
16	-	Input state of digital latch inputs 1 - 4	DINT		•		
		DigitalInput01Latch	Bit 0				
		...	...				
		DigitalInput04Latch	Bit 3				
18	-	Acknowledge digital inputs	USINT				•
		DigitalInput01LatchQuit	Bit 0				
		...	...				
		DigitalInput04LatchQuit	Bit 3				
Digital outputs							
0	0	Status of the digital outputs	USINT	•			
		StatusDigitalOutput01	Bit 4				
		StatusDigitalOutput02	Bit 5				
2	0	Switching state of digital outputs 1 to 2	USINT			•	
		DigitalOutput01	Bit 0				
		DigitalOutput02	Bit 1				
Analog input							
8	6	AnalogInput01	INT	•			
31	-	StatusInput01	USINT		•		
Analog output							
10	2	AnalogOutput01	INT			•	

1) The offset specifies the position of the register within the CAN object.

11.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use additional registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" of the X20 user's manual (version 3.50 or later).

11.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

11.4 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

11.4.1 Digital inputs and status of the digital outputs

Name:
DigitalInput01 to DigitalInput04
StatusDigitalOutput01 to StatusDigitalOutput02

This register is used to indicate the input state of the digital inputs and the status of the digital outputs.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input state - Digital input 1
4	StatusDigitalOutput01	0	Digital output channel 1: No error
		1	Digital output channel 1: Short circuit or overload
5	StatusDigitalOutput02	0	Digital output channel 2: No error
		1	Digital output channel 2: Short circuit or overload
6 - 7	Reserved	-	

11.4.2 Digital input filter

Name:
ConfigOutput01

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter (bus controller default setting)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

11.4.3 Event or gate counter

Event counter operation

The rising (positive) edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF) and corrected with the adjustable prescaler.

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

11.4.3.1 Event or gate counter

Name:
Counter01 to Counter02

Counter01 is intended for event counter operation.

Event counter operation or gate measurement can be selected for Counter02:

Data type	Value
USINT	Counter value

11.4.3.2 Counter configuration

Name:
ConfigOutput02

This register can be used to configure and reset the individual counters.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Name	Value	Information
0 - 3	Counter02 (counter frequency, only with gate measurement)	0	48 MHz (bus controller default setting)
		1	3 MHz
		2	187.5 kHz
		3	24 MHz
		4	12 MHz
		5	6 MHz
		6	1.5 MHz
		7	750 kHz
		8	375 kHz
4	ResetCounter01	0	No influence on the counter
		1	Clear counter (at positive edge)
5	ResetCounter02	0	No influence on the counter
		1	Clear counter (at positive edge)
6 - 7	Counter02 (operating mode)	0	Event counter measurement (bus controller default setting)
		1	Gate measurement

This register also includes configuration data in addition to the cyclic data. If the register is used cyclically and in the init script, then the preset configuration only remains available when operated directly on the CPU. On the bus controller, the configuration is always overwritten with 0.

However, starting with upgrade version 1.0.2.1, the cyclic bit can be hidden in order to prevent the configuration from being overwritten.

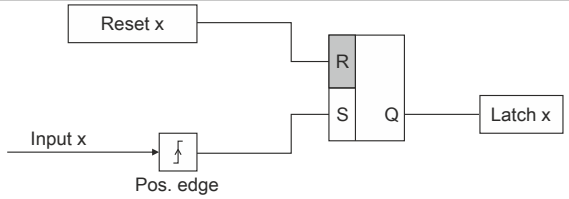
Information:

If the counter should be cleared, this must be done using a non-cyclic write command. When doing so, the configuration bit must be transferred together with the reset counter bit!

11.4.4 Rising edge input latch

Using this function, the rising edges of the input signal can be latched with a resolution of 200 µs. With the "Acknowledge - input latch" function, the input latch is either reset or prevented from latching.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	Status
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

11.4.4.1 Input state of digital latch inputs 1 - 4

Name:
DigitalInputLatch01 to DigitalInputLatch04

This register is used to indicate input state of digital inputs 1 to 4 after expiration of the input filter time.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInputLatch01	0 or 1	Input state of digital input 1 after expiration of the delay time
...		...	
3	DigitalInputLatch04	0 or 1	Input state of digital input 4 after expiration of the delay time
4 - 7	Reserved	-	

11.4.4.2 Acknowledge digital inputs

Name:
DigitalInput01LatchQuitt to DigitalInput04LatchQuitt

This register is used to reset the input latches channel by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
...		...	
3	DigitalInput04LatchQuitt	0	No influence on the latch status
		1	Resets the latch status
4 - 7	Reserved	-	

11.5 Digital outputs

The output status is transferred to the output channels with a fixed offset (<60 µs) based on the network cycle (SyncOut).

11.5.1 Switching state of digital outputs 1 to 2

Name:
DigitalOutput01 to DigitalOutput02

This register is used to store the switching state of digital outputs 1 to 2.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
1	DigitalOutput02	0	Digital output 02 reset
		1	Digital output 02 set

11.5.2 Digital inputs and status of the digital outputs

Name:
DigitalInput01 to DigitalInput04
StatusDigitalOutput01 to StatusDigitalOutput02

This register is used to indicate the input state of the digital inputs and the status of the digital outputs.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
3	DigitalInput04	0 or 1	Input state - Digital input 1
4	StatusDigitalOutput01	0	Digital output channel 1: No error
		1	Digital output channel 1: Short circuit or overload
5	StatusDigitalOutput02	0	Digital output channel 2: No error
		1	Digital output channel 2: Short circuit or overload
6 - 7	Reserved	-	

11.6 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

11.6.1 Analog input register

Name:
AnalogInput01

This register is used to indicate the analog input value depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	0 to 32767	Current signal 4 mA to 20 mA

11.6.2 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >400 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the channels are scanned in 1 ms cycles. Conversion is performed acyclically to the X2X cycle.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

11.6.2.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Adjustable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input jump and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

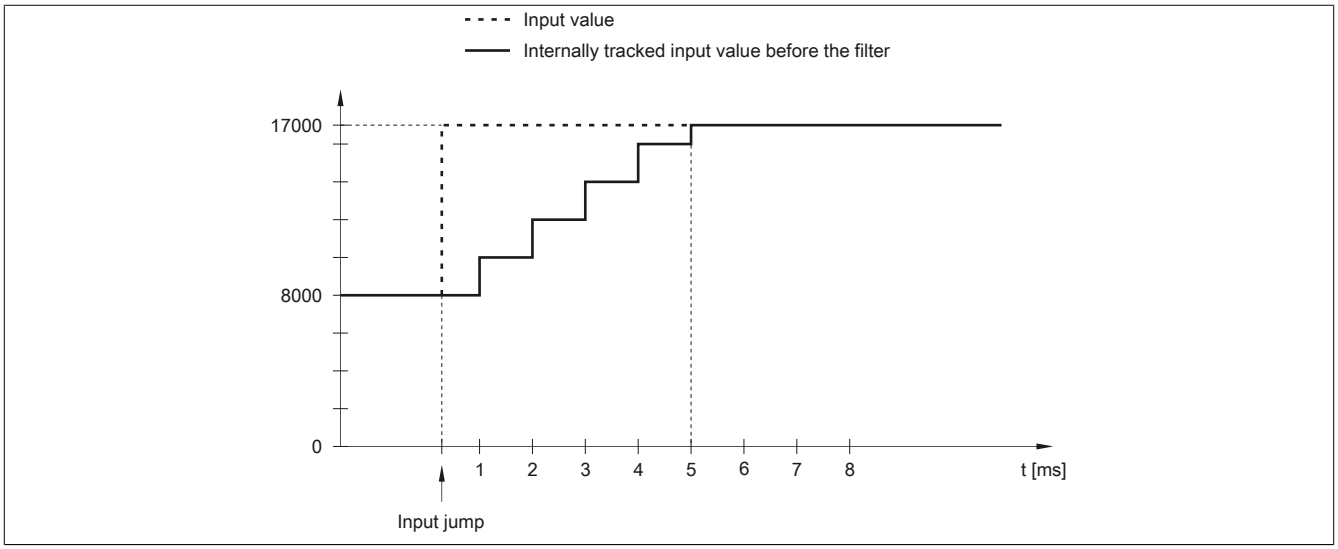


Figure 1: Tracked input value for input jump

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

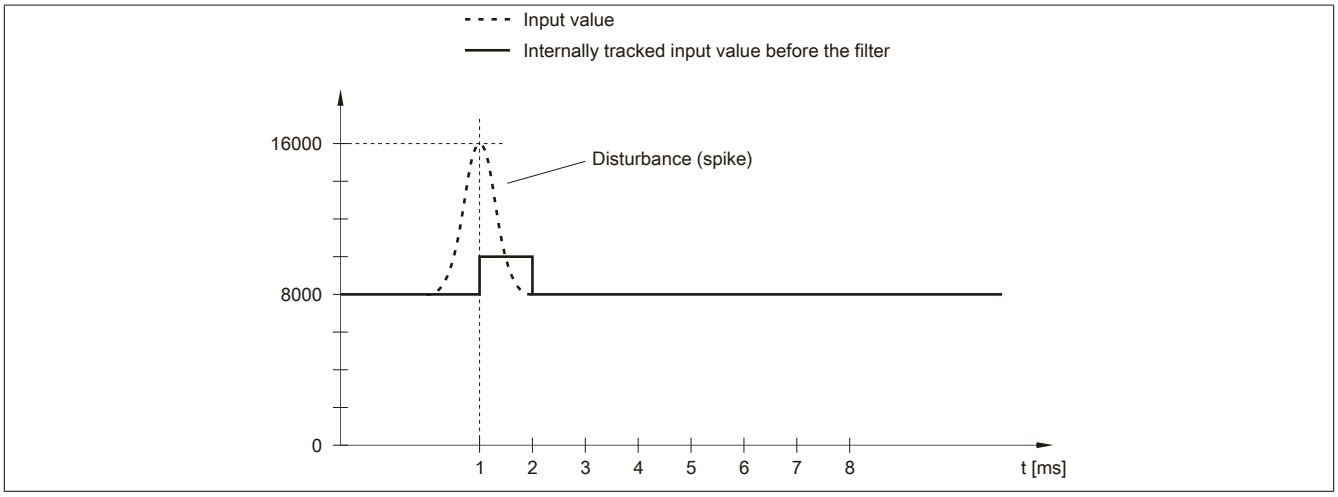


Figure 2: Adjusted input value for disturbance

11.6.2.2 Filter level

A filter can be defined to prevent large input jumps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after input ramp limitation.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show how filtering works in the event of an input jump or disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

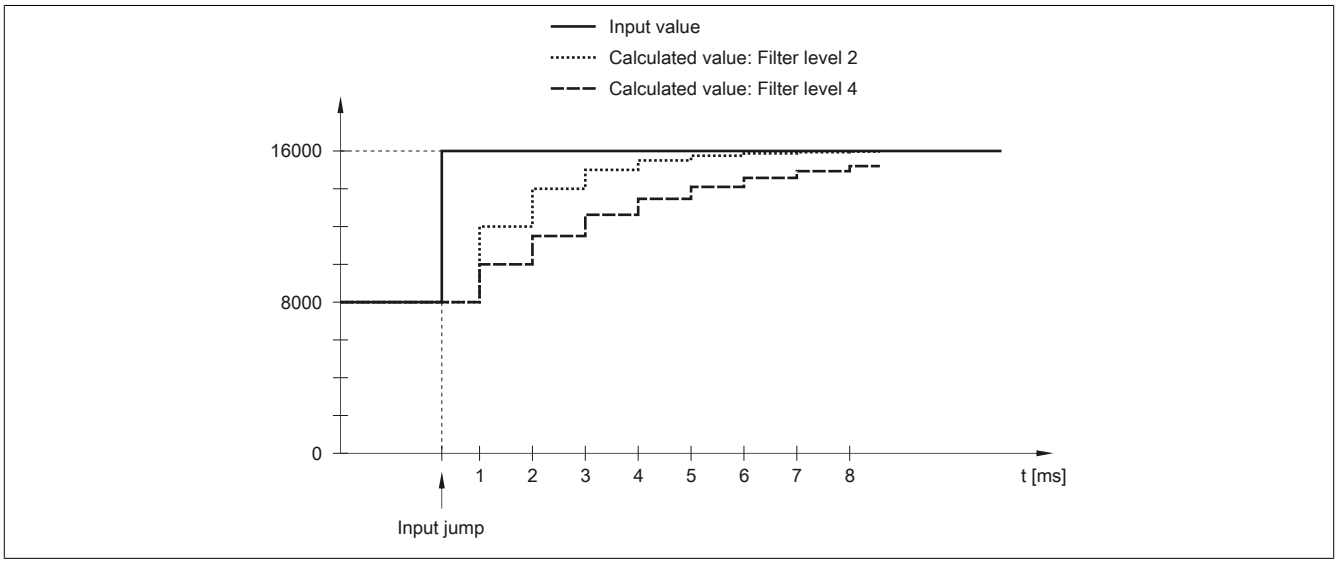


Figure 3: Calculated value during input jump

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

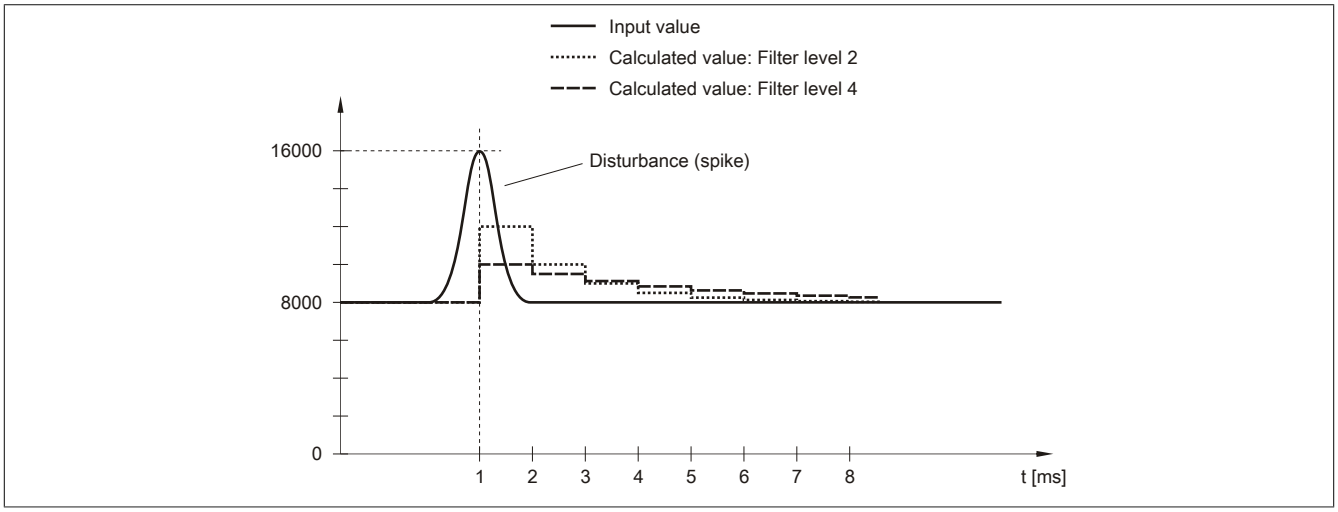


Figure 4: Calculated value during disturbance

11.6.3 Configuring the input filter

Name:
ConfigOutput03

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limit	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

11.6.4 Lower limit for the analog value

Name:
ConfigOutput05

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

Information:

- **The default value of -32768 corresponds to the minimum default value of -10 VDC.**
- **For current measurements, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

11.6.5 Upper limit for the analog value

Name:
ConfigOutput06

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

Information:

- **The default value of 32767 corresponds to the maximum default value of 20 mA or +10 VDC.**

11.6.6 Status of the analog input

Name:
StatusInput01

This register is used to monitor the analog input on the module. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line[1)]
2 - 7	Reserved	0	

1) Open-circuit detection does not occur during current signal measurement.

11.7 Analog output

The channel can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.

11.7.1 Analog output register

Name:
AnalogOutput01

This register is used to output the analog output value appears depending on the operating mode that is set.

Data type	Value	Information
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA

11.8 Configuration of the analog inputs and outputs

Name:
ConfigOutput04

This register can be used to define the type and range of signal measurement.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the terminal connections used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal.

Input signal:

- ±10 V voltage signal
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Output signal:

- ±10 V voltage signal
- 0 to 20 mA current signal

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 1	Analog input	00	Voltage signal -10 VDC to +10 VDC (bus controller default setting)
		01	Current signal 0 mA to 20 mA
		11	Current signal 4 mA to 20 mA
2 - 3	Reserved	0	
4	Analog output	0	Voltage signal -10 VDC to +10 VDC (bus controller default setting)
		1	Current signal 0 mA to 20 mA
5 - 7	Reserved	0	

11.9 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	100 µs
With filtering	150 µs

11.10 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time	
Digital without filtering	150 µs
Digital with filtering	200 µs
Analog without filtering	400 µs
Analog with filtering	1000 µs