COMPUTER DESIGN

THE MAGAZINE OF MODERN DIGITAL ELECTRONICS

APRIL 1967

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Tomorrow's Breed of I/C Computer . . .

. . . And They're Being Delivered Today!

I/C construction . . . 16-bit word . . . 960 nanosecond speeds . . . strong software support — unprecedented computer capability in a low cost compact. And these are only some of the features that put Honeywell, Computer Control Division's two new μ-***COMP*** machines in tomorrow's computer class today.

THE DDP-516, at $25,000, is the most advanced I/C 16-bit computer now available. Both hardware and software are already operational. Hardware includes high-speed multiply and divide (optional), a 4096-word memory (expandable to 32K), 960 nsec cycle time. The command repertoire includes 72 instructions with such capabilities as byte manipulation, skip-branch conditioning, and extensive memory reference and control.

250 field proven programs are available with every DDP-516 . . . including ASA FORTRAN IV compiler, selectable one- or two- pass assembler with a unique DESECTORIZING loader that lets you ignore memory restrictions. DDP-516 delivery: about 120-days depending on configuration.

THE DDP-416, at $16,900, was engineered for a price/performance ratio that can't be beat by any other on-line real-time computer. Hardware features include a 4096-word memory (expandable to 16K), 960 nsec cycle time, 1.92 μsecs add, with indirect addressing.

A 30-command repertoire, priority interrupt and power failure protection are standard. Both the DDP-516 and the DDP-416 may be mounted in standard 19″ racks. Best of all, if you decide to get the more powerful DDP-516 in the future, you can continue to use your DDP-416 programs because of direct compatibility. DDP-416 delivery: third quarter, 1967. Write today for information on both μ-***COMP*** computers. You can't go wrong with either one. Honeywell, Computer Control Division, Old Connecticut Path, Framingham, Massachusetts.

Honeywell

COMPUTER CONTROL DIVISION

SEE US AT SJCC

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PAT. PENDING

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OUR OMNI-COMB* DIP Connection (based on our universally-accepted Omni-Comb*) provides even greater density and more nimble application for single or double-sided card back-panel wiring. This should intrigue you. It costs a lot less. This should convince you.

OUR SERIES 8358 DIP SOCKET is a 14-contact connector with .025" square tails for wire wrap applications. Its contact noses will mate with every known dual in-line package presently available. This should excite you.

WHY NOT SHOW THEM? Because, unfortunately, one picture does not speak ten thousand words, and cannot reveal the "inside stories" these products' outside shells conceal. Such as detailed design, versatility, performance and reliability. However we will be delighted to send you complete technical data; and if you insist, photographs. This should invite you. Write?

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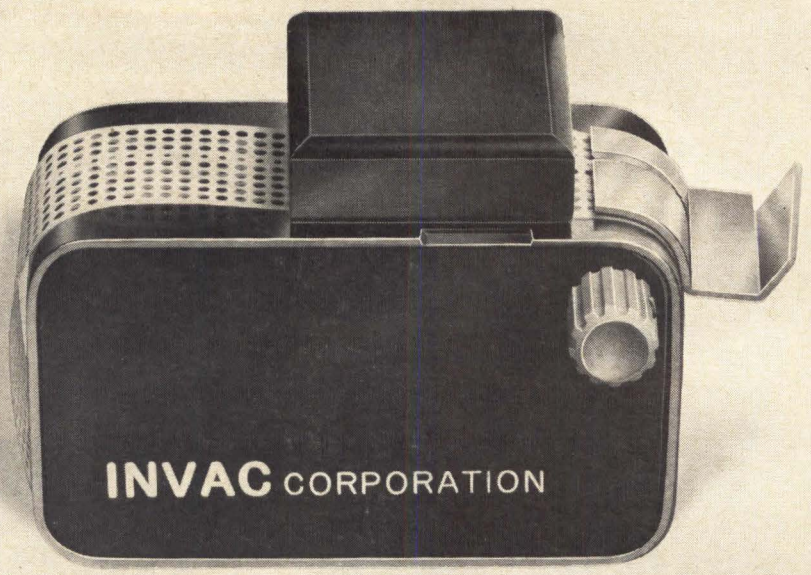
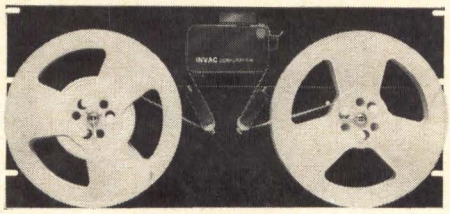


Breakthrough



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A sensing design breakthrough by Invac means Tape Readers are now available for only $195.00 (less standard discounts) with smaller size and inherent high reliability as extra bonuses. The Model R-360 utilizes a unique "reading" method, "Ball Sensing", and accommodates 5, 6, 7 or 8 channel tapes (paper, mylar and aluminized mylar) at speeds up to 60 characters per second.

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Write for the Model R-360 Technical Bulletin

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CIRCLE NO. 3 ON INQUIRY CARD

APRIL 1967 • VOLUME 6 • NUMBER 4

COMPUTER DESIGN

FOR ENGINEERING PERSONNEL RESPONSIBLE FOR THE DESIGN & APPLICATION OF DIGITAL CIRCUITS, EQUIPMENT, AND SYSTEMS IN COMPUTING, DATA PROCESSING, CONTROL AND COMMUNICATIONS.

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This article presents a new technique for either manual or mechanized conversion of any number from any base to any other base, using one simple set of rules. The technique, known as the Hartmann method, may well be the most significant contribution to number conversion since John Couleur's BIDEC in 1958.

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Introducing the Bryant Series 4000-2A real time mass memory system. It can store 3.8 billion bits. The largest single unit disc file capacity in the world. And by far the lowest costing random access system available today. All data is on-line, available within an average of 100 milliseconds. A basic cabinet offers modular growth to capacity. Environmental control reduces maintenance to a minimum. Dual access option offers increased throughput. The 2A joins 190 Series 4000 files operating all over the world. Deliveries begin in November, 1966. But don't wait till then. Call your nearby Bryant Application Engineer now or write: 850 Ladd Road, Walled Lake, Michigan 48088.

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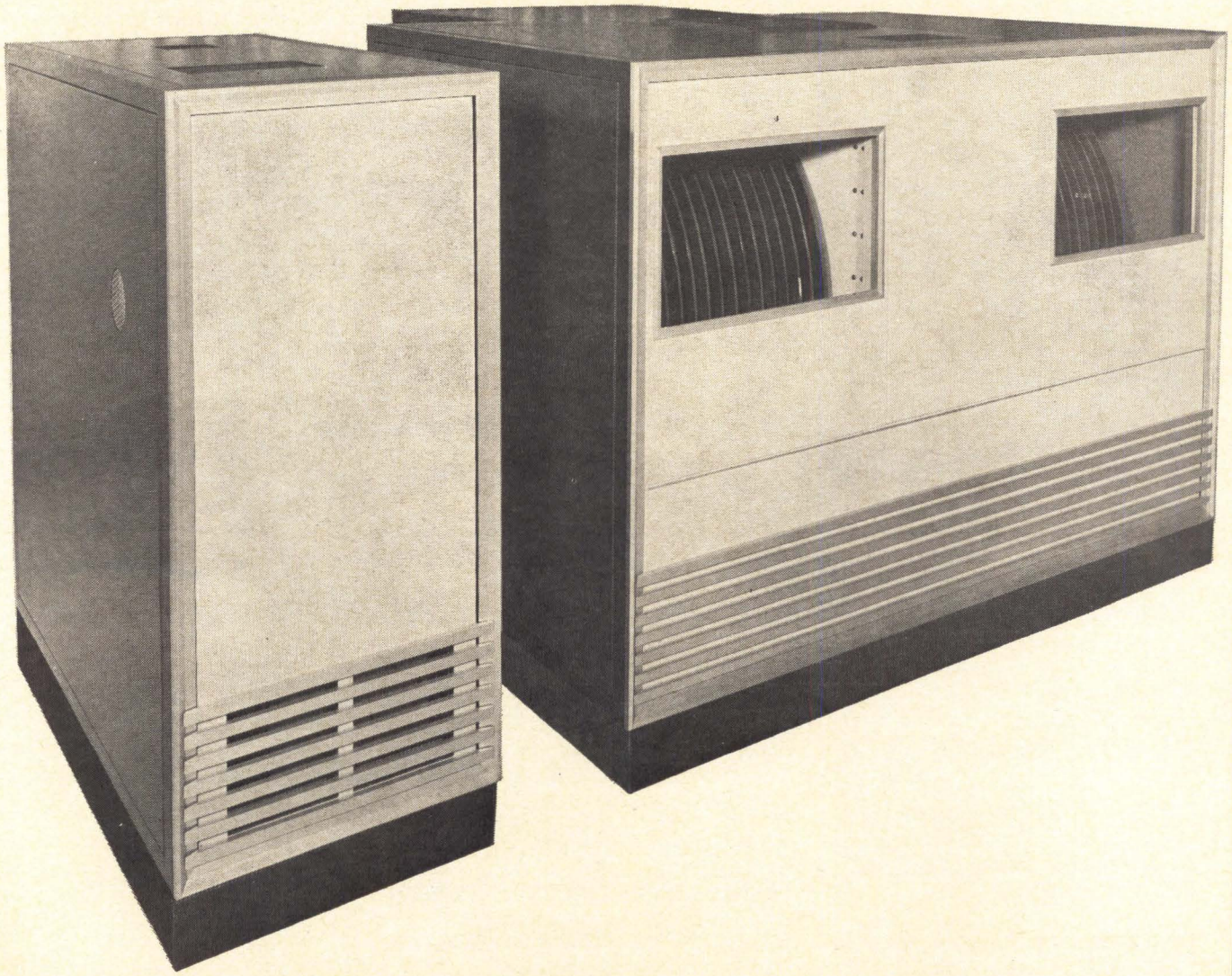


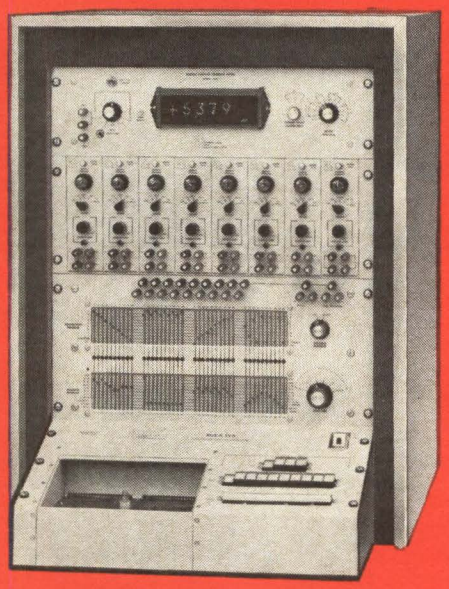
CIRCLE NO. 4 ON INQUIRY CARD

Circle No. 5 on Inquiry Card

NEW

semi-automatic integrated circuit analyzer

MICA 150



COMPUTER TEST CORPORATION

Now the integrated circuit user can get all the flexibility and performance of an expensive, large scale IC test system in an accurate and reliable DC bench top analyzer.

The new MICA-150 Modular Integrated Circuit Analyzer tests all IC configurations of up to 40 pins with unique programming, fast pushbutton sequencing and built-in DVM readout.

Fast, Versatile Programming Two independent 10x40 crossbar switches and rapid pushbutton sequencing provide up to 40 tests on a single device without re-programming. For example, it's now quick and easy to check a 10 pin device using four completely different test programs without resetting any switches to advance the test from pin-to-pin or program-to-program. Additional flexibility allows the built-in DVM to measure current on one pin of the device and voltage on another—all pre-programmed.

Universal Test Adapters Through use of universal test adapters, the MICA-150 is designed to check ICs according to the number of pins of a particular package, not device or circuit type. Adapters are available for diode, transistor, TO-5, flat-pack, dual in-line and other package configurations, and can also be provided for Kelvin connections.

Accurate Digital Readout Specifically designed for the MICA-150 analyzer, the built-in Digital Volt/Ammeter has a conservatively rated readout accuracy of 0.1% with a four digit display. Other features include automatic ranging and polarity selection, self-calibration, automatic voltage or current readout selection. Measures currents as low as 1 nanoamp, voltages to 1 mv.

Modular Design Modular construction allows users to select an economical, customized tester without obsolescence problems. Maximum capacity of eight function generators permits later expansion, including modules for AC and pulse testing, without additional modifications.

Variable Soak Time Marginal device operation can be easily detected through use of an adjustable test time control which provides a period for thermal stabilization prior to measurement. A continuous position on the control allows parameters to be varied while observing results.

Precision, Wide Range Power Supplies Highly precise supplies utilize multi-turn calibrated potentiometer controls with high resolution and repeatability. Constant current supplies are continuously variable from 0-100 ma with voltage compliance adjustable to 100v. Constant voltage supplies are variable from 0-100v with automatic current limiting to 100 ma to provide device protection.

QUICK ACTION REPLY

Detailed technical literature on the MICA-150 will be mailed immediately upon receipt of this request.

Attn.: A. Norman Into, Marketing Manager
Computer Test Corporation, Three Computer Drive
Cherry Hill, N.J. 08034 • Phone: (609) 424-2400

Name_____

Company_____

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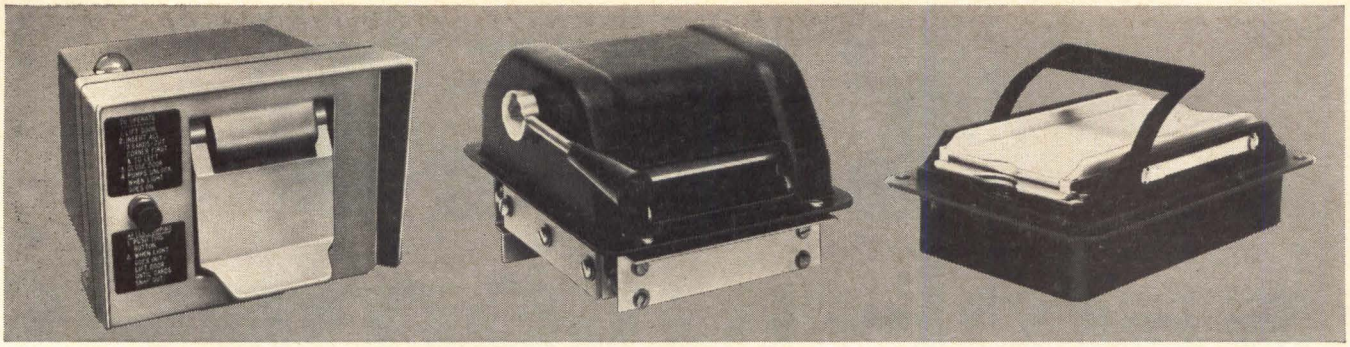
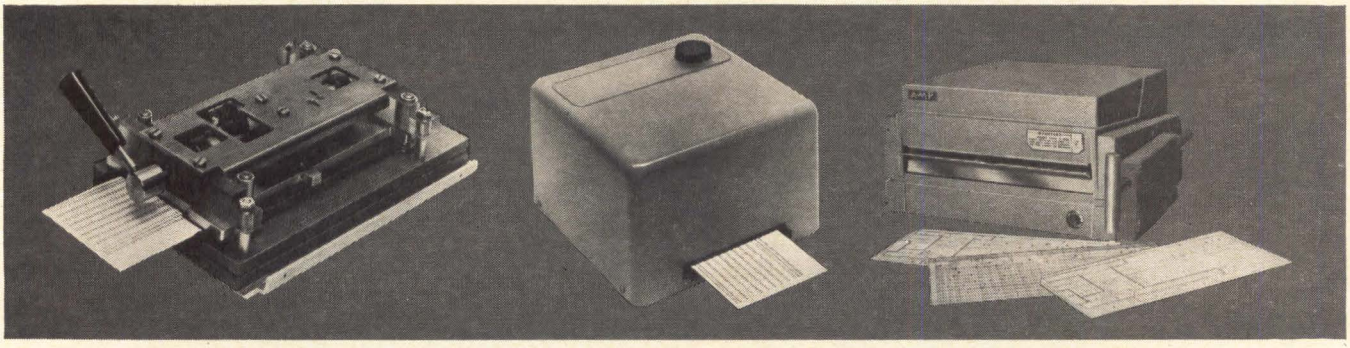
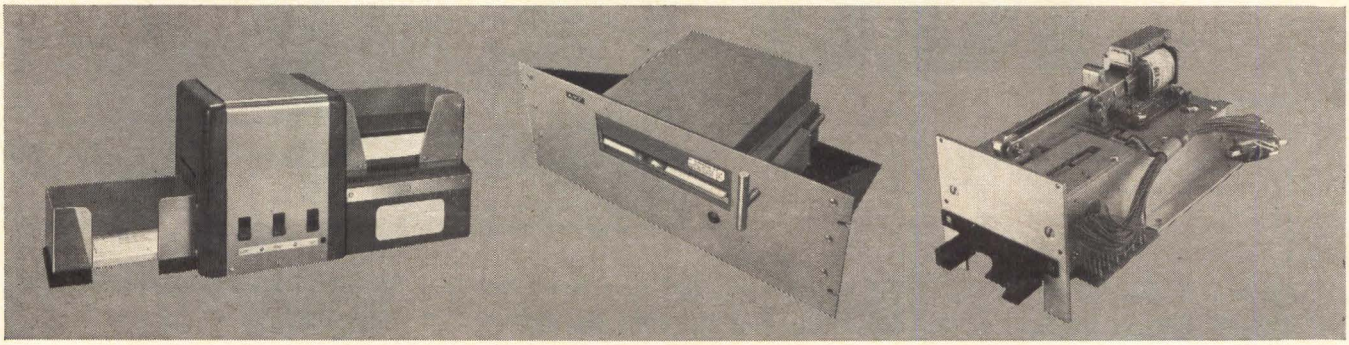


Are we handing you a line?



Yes. The biggest in the world...



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Circle No. 7 on Inquiry Card

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A FABRI-TEK OFFERS TODAY'S BROADEST MEMORY CAPABILITY Ω

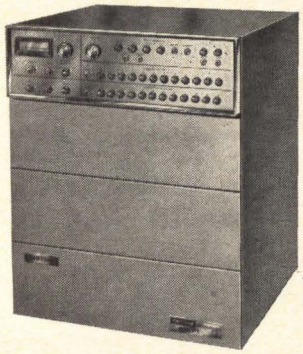
Fabri-Tek's business is electro-magnetic memories. Core stacks or systems, 2½D and 3D organization, thin film systems, low-cost systems with "off-the-shelf" delivery or special designs, Fabri-Tek does it all.

But offering the widest possible product range is only halfway to leadership in memory technology. Research and design capability is the rest of the way, and Fabri-Tek is advancing the state of the art.

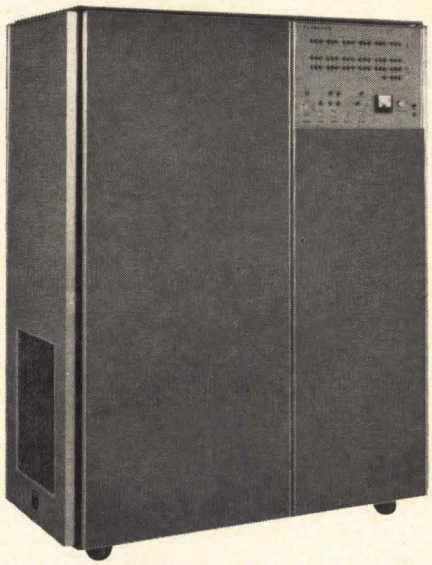
Symbolic of leadership is the fact that Fabri-Tek now is stringing cores at the rate of 40 per second or a billion per year. That's a lot of customer-confidence. By the way, an added benefit is price. Stringing that many cores that fast helps attain lowest possible cost per bit.

SEE US AT THE SJCC. AREA D.

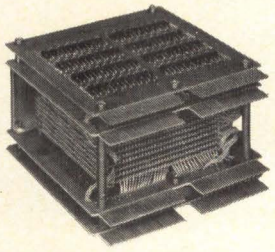
2½D STACKS: FABRI-TEK led the way with 2½D more than two years ago. Speeds to 650 nanoseconds. Unique low-noise design and manufacturing techniques.



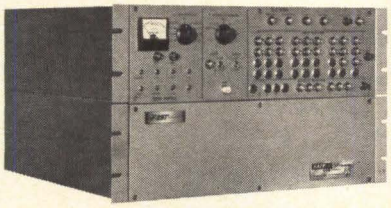
CORE MEMORY SYSTEMS: Speeds from 500 nanoseconds to 10 microseconds, 2½D and 3D organization. Use of integrated circuitry. Custom performance at "off-the-shelf" prices.



MASS CORE MEMORY: 2½D mass core storage at less than 2 cents per bit for 20,000,000 bits. Cycle times at computer speeds.



3D STACKS: FABRI-TEK is the world's major producer of 3D stacks. Get 1 microsecond or slower with everyday delivery. Now shipping 200 per week.



THIN FILM SYSTEMS: Scratchpad to main memory. FABRI-TEK has delivered many 300 nanosecond systems for commercial and military applications and is the only manufacturer supplying a large thin film system to a computer manufacturer for main memory.

FABRI-TEK LEADS IN MEMORY TECHNOLOGY

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For further information, write for BULLETIN 9056A, or contact Systems Engineering Laboratories, Inc., 6901 West Sunrise Blvd., Fort Lauderdale, Fla. 33310. Area Code 305-587-2900. Offices also in Washington, D.C.; Los Angeles, California; Boston, Massachusetts; San Francisco, California; Cleveland, Ohio; Houston, Texas; Huntsville, Alabama; and Orlando, Florida.

Systems Engineering Laboratories

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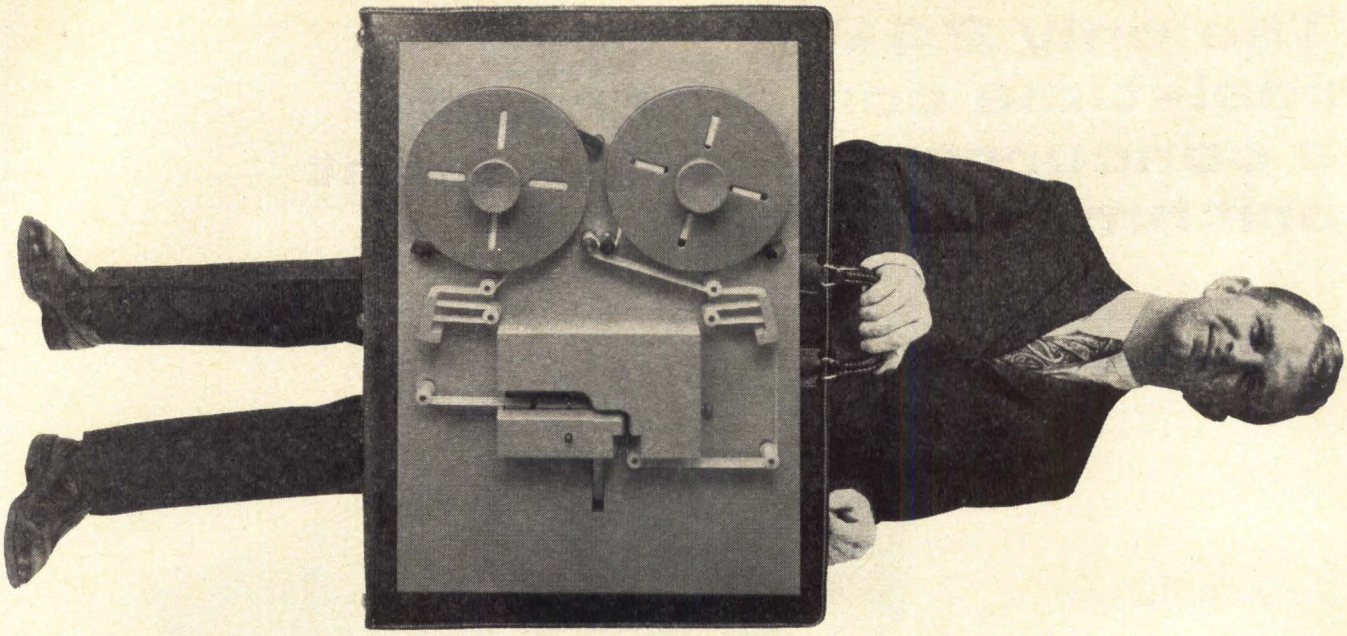

The Peripheral People announce a 200 cps perforator. It's fast (1) reliable (2) easy to maintain (3) modular (4) accurate (5) inexpensive (6) and available (7). Any questions? Speak, demand, we'll answer (8).

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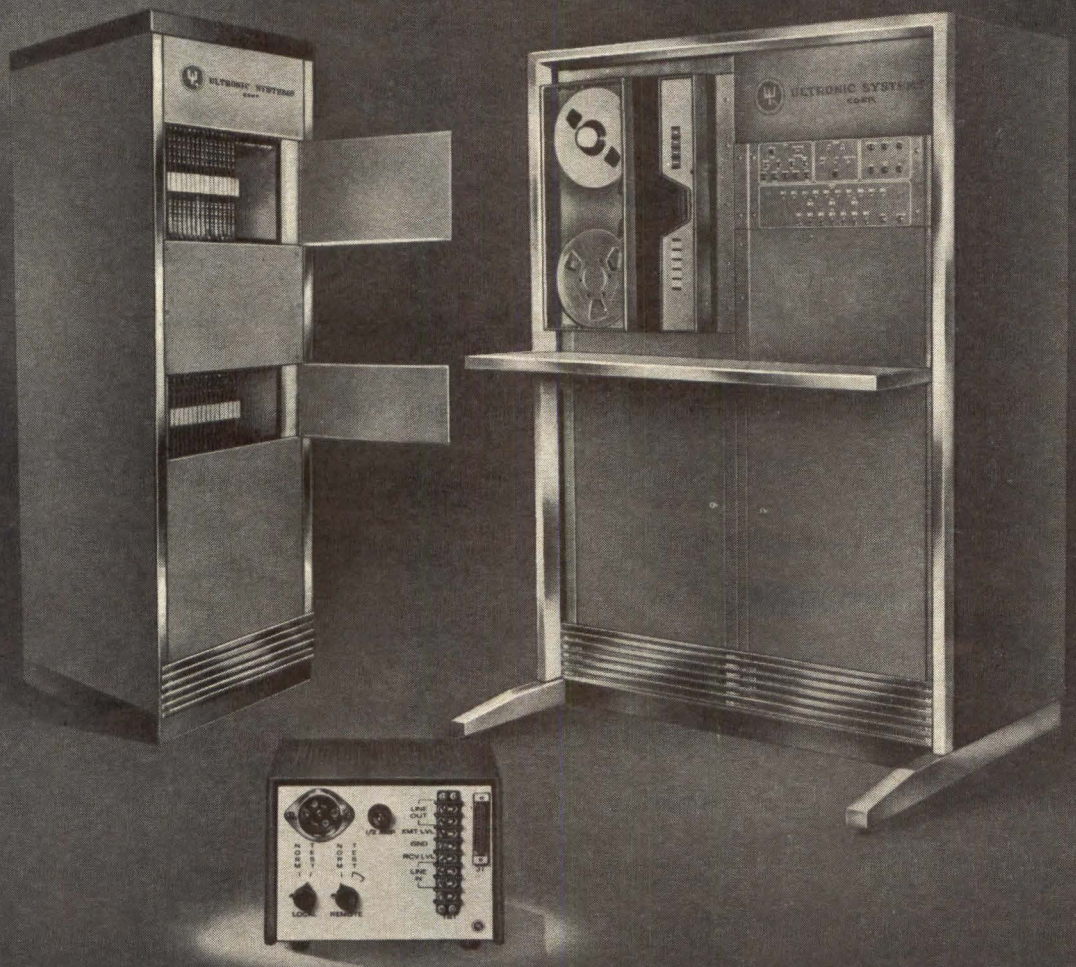

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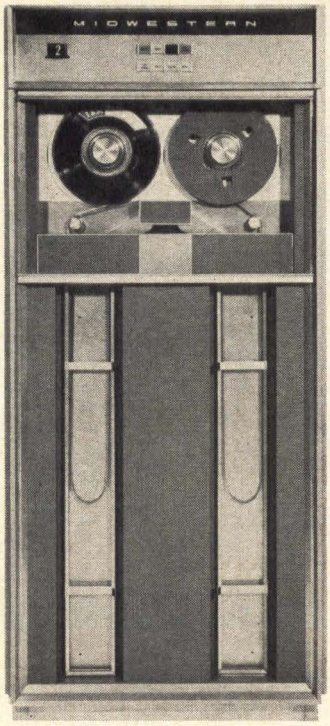

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APRIL 18, 19 & 20

End high leasing costs forever with Midwestern's M4700 series digital tape transports. Designed as **direct** replacements for primary leased transports, the M4700 is ready immediately to become a part of your on-line operation. No conversion is necessary. The I-0 connectors are exactly the same. So are the 3-phase power connectors. And the control electronics are completely compatible. Just slide it in place and plug it in. The M4700 is ready to start saving your company thousands of dollars per year.

You can own an M4700 outright for approximately the cost of 16 months' leasing. The M4700 is a refinement of Midwestern's M4000 that has earned acclaim for its compatibility and superior reliability throughout the O.E.M. market. Exclusive features include Midwestern's lightning-quick, but feather-light pneumatic tape drive and proven reliability at speeds to 150 ips.

For complete information on the M4700, (including names of companies who have made the change already) write or call Digital Tape Products Division, Tulsa, Okla. 74101. Our phone number is 918-627-1116.

MIDWESTERN INSTRUMENTS / **TELEX**

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THE MIDWESTERN
M4700

CIRCLE NO. 19 ON INQUIRY CARD

We'll stop at nothing to help you select the right memory system

...we'll even lend you one (with or without the applications engineer) for a free trial

We can help if you have no experience with core memories, but are designing industrial control systems that must handle and store data. To see how they can profit by the use of a low cost core memory, give us a call. We'll send an applications engineer around with the system best suited to your needs. He'll help you get it on line for evaluation.

We can help if you're familiar with core memories, but don't see how a standard off-the-shelf design could satisfy your requirements. Send us your block diagram. We'll study it and send you back a complete blueprint showing you how a general purpose core memory can be used as a versatile data-manipulating system capable of many more logic functions than storage. (We may even be able to eliminate some redundant functions required by less versatile storage techniques.)

We can help even if you're already using core storage, but aren't convinced that a mass produced memory can provide many of the control, access and operating mode functions formerly associated (usually one at a time) with custom design. Drop us a line. We'll lend you a small system for a 10-day free trial. See for yourself what it can do. If at the end of the trial period you can't bear to part with it, we'll work something out.

Our point—to prove that our line of catalog standards is broad enough to satisfy most data storage requirements and that we'll do almost anything to help you apply them to your system. Our FX-12 and FX-14 Series Systems are available in some 200 types. Sizes range from 128 words x 8 bits to 4K x 32, with cycle times from 4 to 8 microseconds. Prices start at $1,190. If you'd like to check details and specifications before we talk, write for Bulletins M6612 and M6614.

Ferroxcube
Systems Division Englewood, Colorado

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Systems Division
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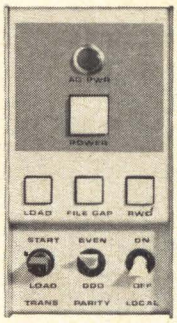
CIRCLE NO. 24 ON INQUIRY CARD

This New 3M Asynchronous Digital Recorder writes data at the rate of 0-2000 characters per second



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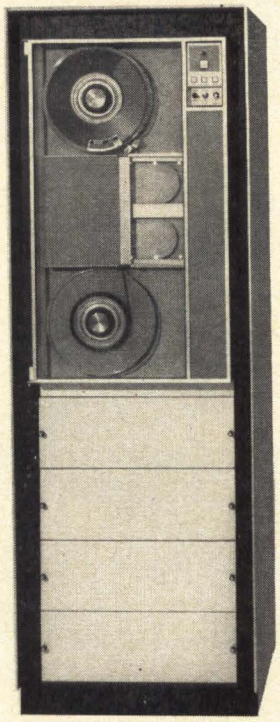

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25	0.082/4.7
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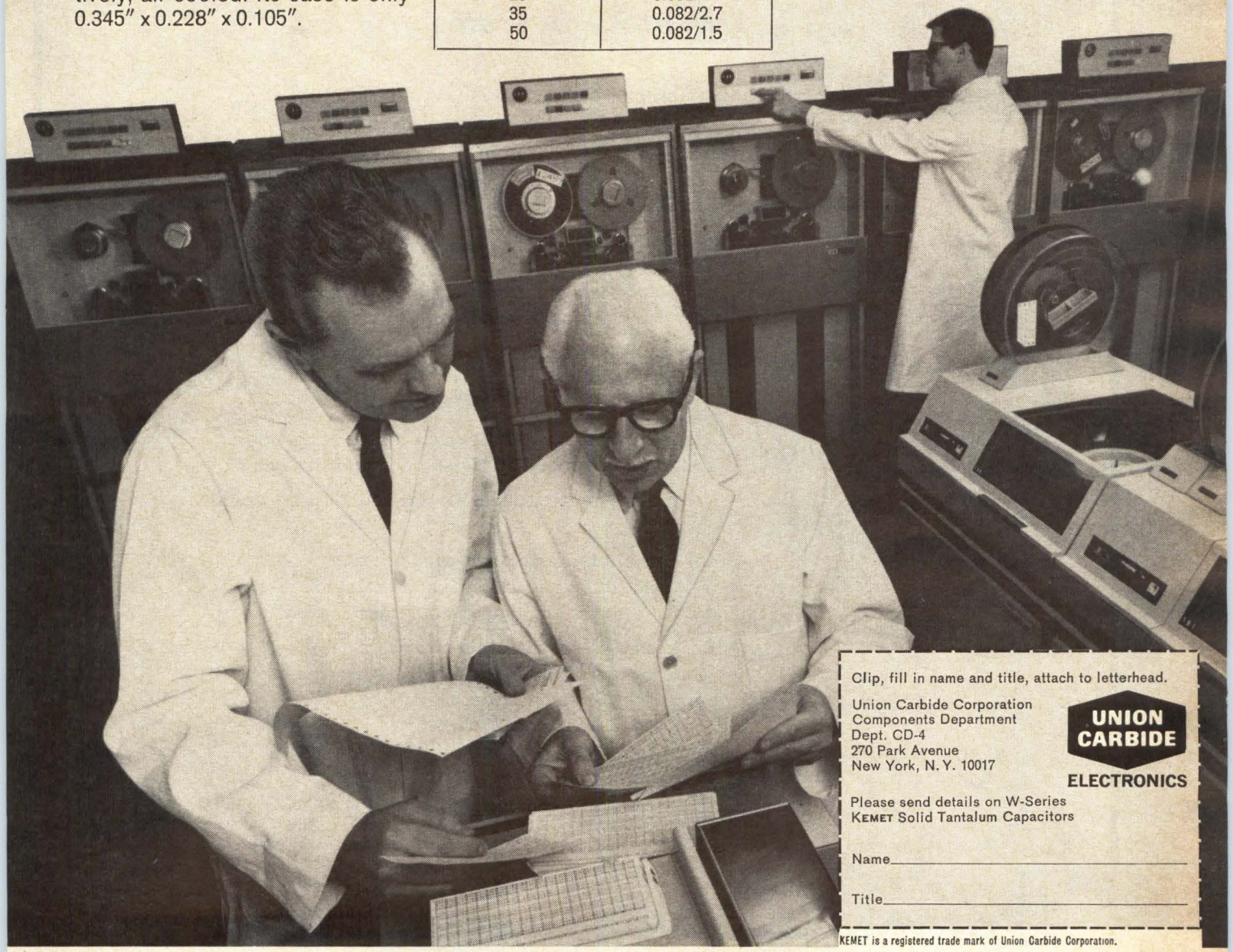

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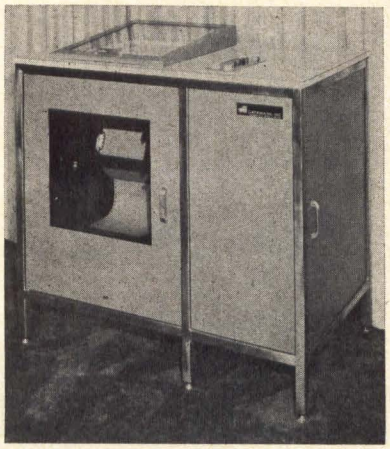

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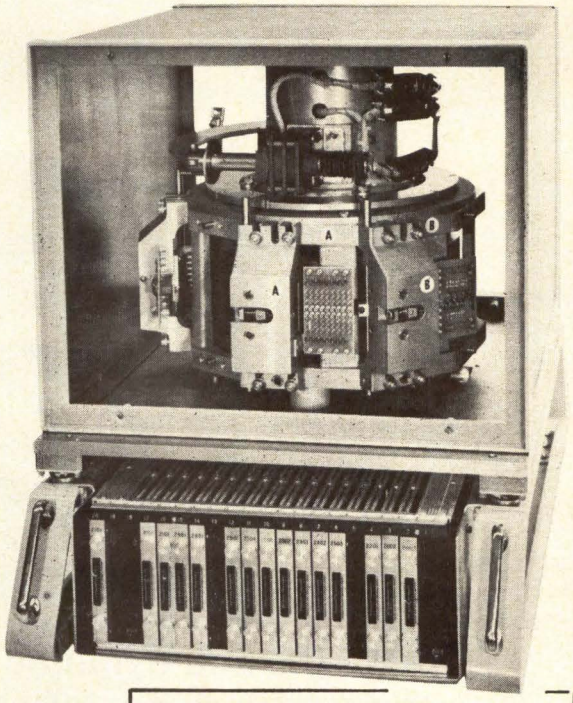

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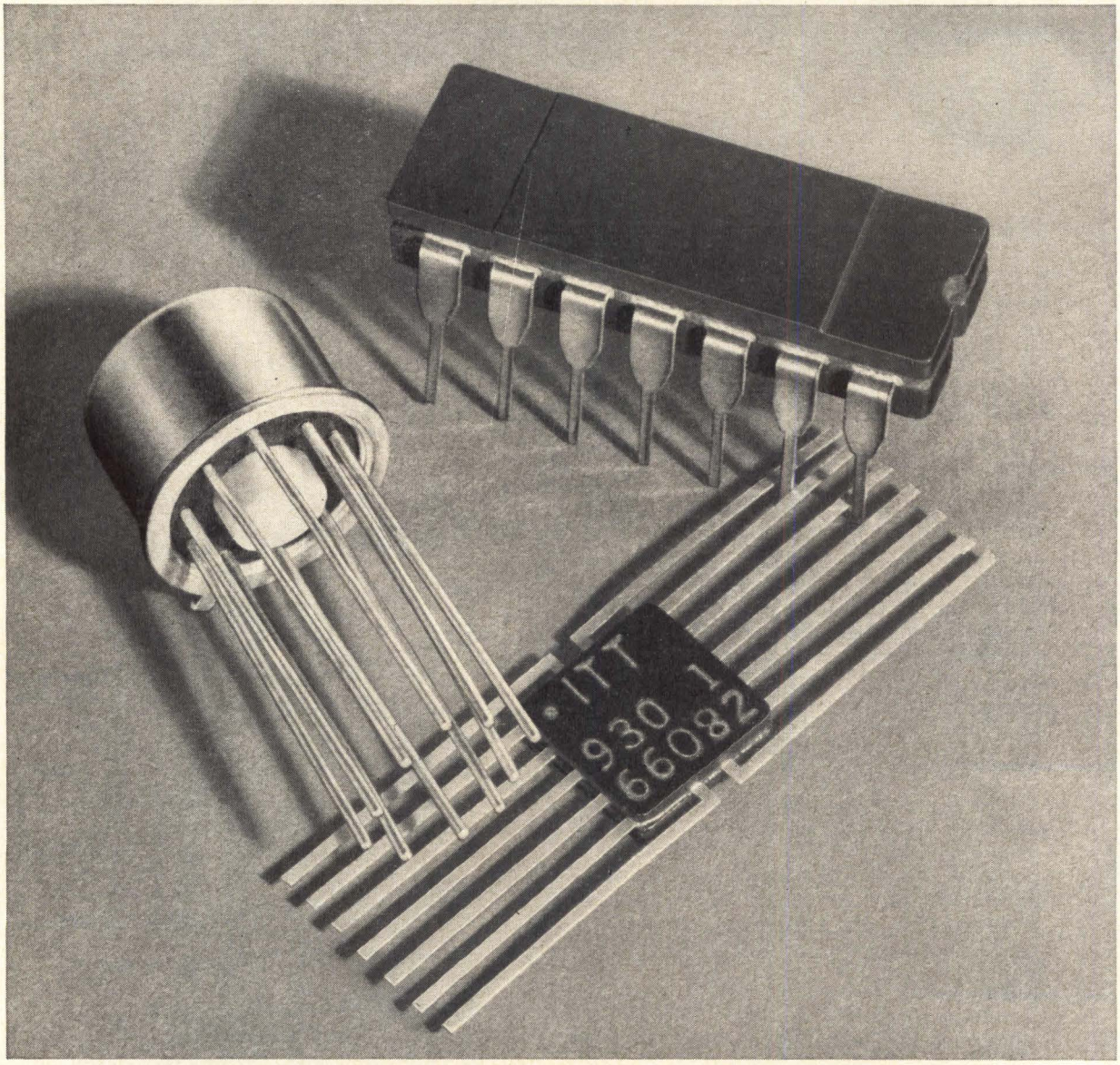

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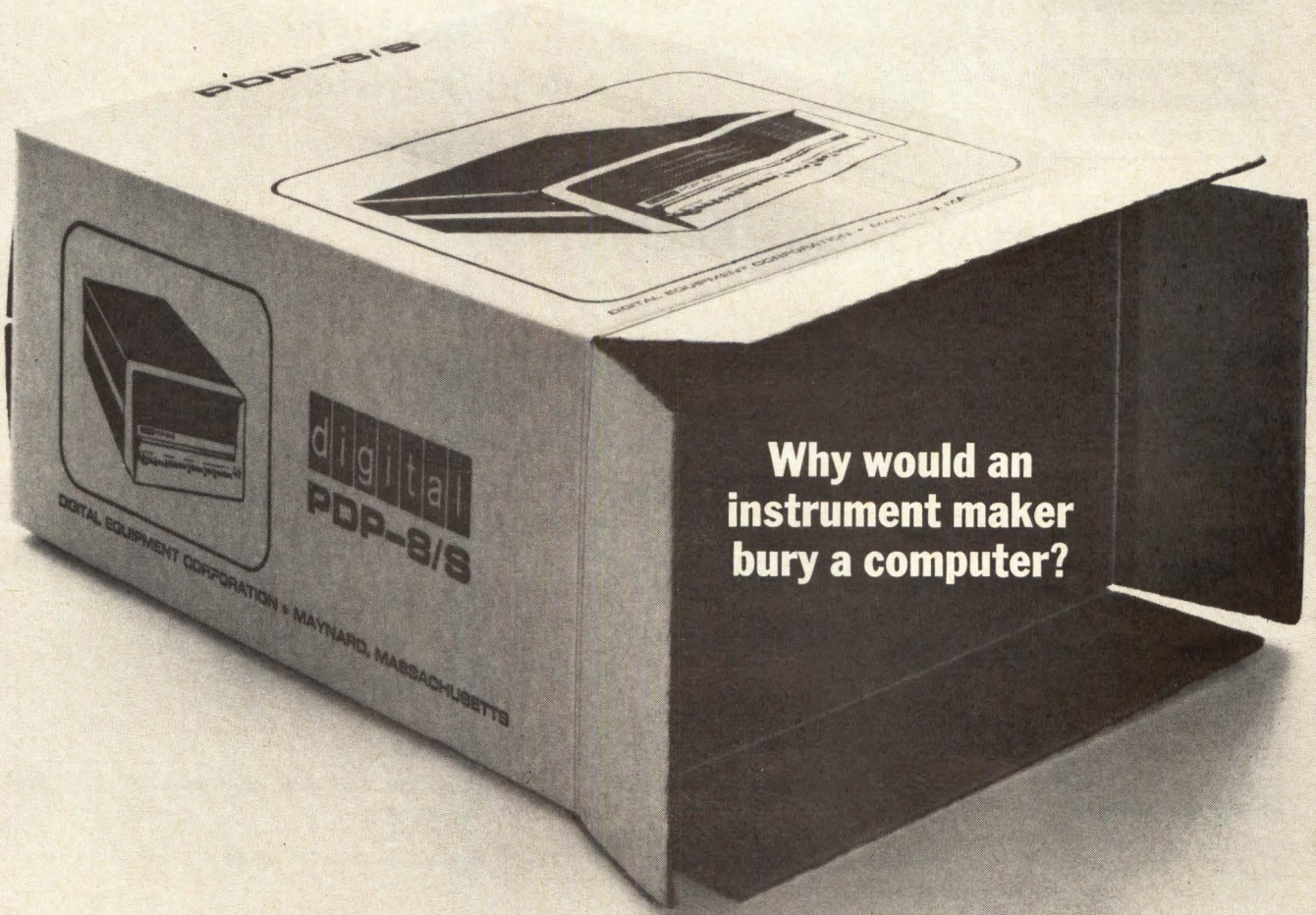

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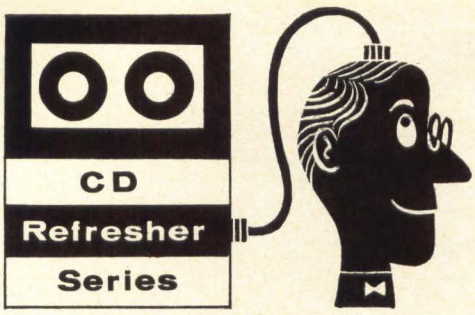

MATHEMATICS REVISITED:

Selected Topics In Probability And Statistics

DAN M. BOWERS, Contributing Editor

Part 9 – STATISTICAL PREDICTION

It is the function of Descriptive Statistics to gather, organize, and present data. The data may consist of stock prices, performance of a race-horse, lengths of brook trout caught in the Willowemoc, times-between-failures of a computer, or presidential preferences of a sampling of voters. The resulting statistical presentation may be of some historical interest, but the usual justification for the required expenditure of time and money is the expectation that, given past statistics on a phenomenon, we can predict future results and take appropriate action such as selling short, betting the long-shot in the feature at Aqueduct, doing our fishing in the Beaverkill, improving the design of the computer, or campaigning harder for our candidate. As always, we must keep in mind the admonitions of the first article of this series that we are dealing with "independent trials" of "random" events and that our predictions will at best be accurate only "in the long run." Therefore our statistical conclusions are not necessarily invalid if a particular stock doubles in value, the long-shot breaks his leg in the clubhouse turn, a 28" trout is lured from under a log in the Willowemoc, or serial number 47 of the computer runs two years without failure.

We might suspect a flaw in our procedure if "Truman" defeats "Dewey," since a national election certainly provides sufficient results to be in the "long run" category. This was shown to be the case when the defeat of Roosevelt by Landon in 1936 was predicted by the Literary Digest — which then experienced instant oblivion.

Index Numbers

A method of statistical presentation which lends itself well to predictive techniques is the **index number.** An index number is a binary comparison of two quantities; for example if the price of a loaf of bread was 10¢ in 1937 and is 29¢ now, the bread index now would be 290, i.e., bread prices have gone up 290%. This is a single-item index, which is useful in presenting data on a particular phenomenon. As another example, Table 1 lists the gross income of IBM Corp. for each of the last ten years, along with the associated index. The **base year** of this index is 1957, that is, the index for a given year is the ratio of the given year gross to the 1957 gross. Obviously all indices must have a base year (which in this case may be noted as 1957 = 100).

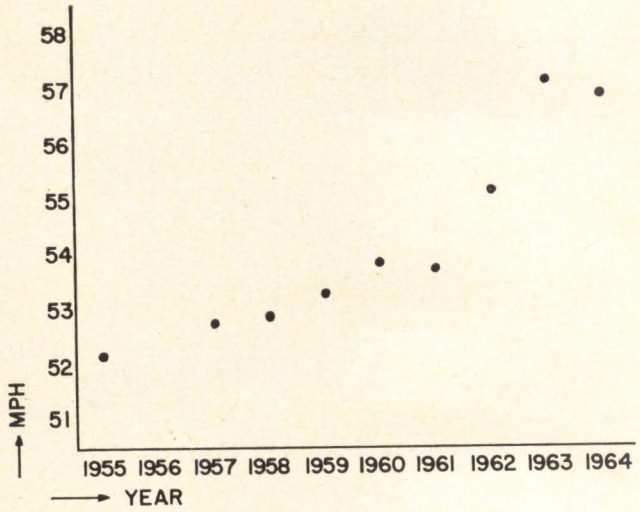

Fig. 1 Scatter diagram for speed of passenger cars

More typical than the single-item index, however, are such familiar indices as the Cost-of-Living Index (now known as the Consumer Price Index), the Dow-Jones "Average," and the New York Stock Exchange Index. These indices are intended to quantify, with one number, a vast quantity of data such as the cost of all consumer goods and services, or the price of all 1250 common stocks listed on the New York Stock Exchange. In addition to summarizing many bits of data, the usual index number assigns to each constituent a weighting factor which establishes the relative importance of each constituent within the index. For example, in a Consumer Price Index we should assign a higher weight to the price of bread than to the price of caviar, if we want to relate the index to an average consumer. The general form for an index number is:

$$I = \frac{\Sigma P_n \cdot W_i}{\Sigma P_o \cdot W_i}(100)$$

where P_n are the prices for the given year; P_o are the prices for the base year; and W_i are the weights assigned to the various constituents. The weights are sometimes assigned by using the quantity of that particular commodity sold during the given

TABLE 1

IBM Corp. Gross Income Index, 1957 = 100

Year	Gross Income in Billion $	Index
1957	1.20	100
1958	1.42	118
1959	1.61	134
1960	1.82	152
1961	2.20	183
1962	2.59	216
1963	2.86	238
1964	3.24	270
1965	3.57	297
1966	4.25	354

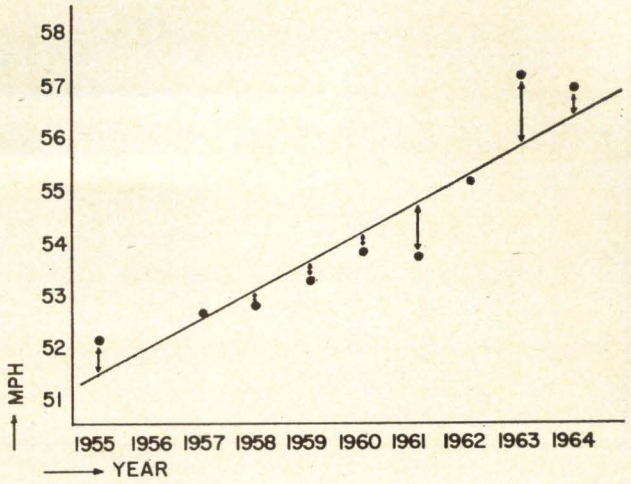

Fig. 3 Variance of best-fit line

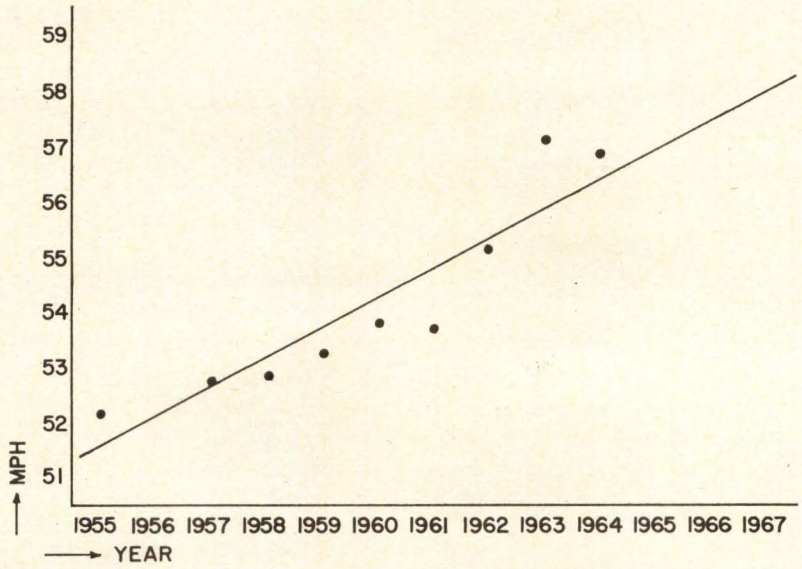

Fig. 2 Passenger car speed with best-fit line

year, the base year, or some benchmark year between.

As an example of the formulation of a weighted index, Table 2 lists hypothetical figures for the average wages and labor-hours expended in each of three categories for the computer industry, for the five years 1960-1964. From this we shall calculate a cost-of-labor index for the computer industry. Using a base year of 1960, the formula shown above, and given-year quantities as weights, we have:

$$I_{1961} = (100)\frac{(1.80)(470M) + (2.30)(193M) + (4.80)(208M)}{(1.73)(470M) + (2.25)(193M) + (4.65)(208M)} = 103$$

$$I_{1962} = (100)\frac{(1.92)(485M) + (2.48)(203M) + (4.82)(219M)}{(1.73)(485M) + (2.25)(203M) + (4.65)(219M)} = 108$$

$$I_{1963} = (100)\frac{(2.01)(510M) + (2.75)(205M) + (5.13)(225M)}{(1.73)(510M) + (2.25)(205M) + (4.65)(225M)} = 113$$

$$I_{1964} = (100)\frac{(2.15)(530M) + (2.87)(212M) + (5.35)(238M)}{(1.73)(530M) + (2.25)(212M) + (4.65)(238M)} = 120$$

Based on these figures, then, we would conclude that our cost-of-labor has risen through gradual steps by 20% since 1960.

The configuration of a particular index is a subject for study in its own right, and we shall do no more here than introduce the concept. The method of assignment of weights can give a high or low bias to the index. There is also a chain index, in which the base-year concept is discarded and each index number is based upon the period immediately preceding it: the Consumer Price Index, for example, is month-to-month chain index. The important fact to bear in mind about an index is that it is a human-invented statistical measure of a large number ("in the long run") of independent trials which, although not random, must be treated with the same caution we used in applying our probability calculations.

To conclude the discussion of index numbers, we shall illustrate the mechanism of the New York Stock Exchange Industrial Index, which was concocted in 1966 in an attempt to displace the well-known Dow-Jones Industrial "Average" as the major indicator of stock prices on the NYSE. In the years since its invention, the weighting of the Dow-

TABLE 2

Hypothetical Wage and Hour Figures for the Computer Industry

	Wireman		Technician		Engineer	
	Average wages	Total hours	Average wages	Total hours	Average wages	Total hours
1960	1.73	465M	2.25	188M	4.65	199M
1961	1.80	470M	2.30	193M	4.80	208M
1962	1.92	485M	2.48	203M	4.82	219M
1963	2.01	510M	2.75	205M	5.13	225M
1964	2.15	530M	2.87	212M	5.35	238M

Jones Index has become so affected by stock splits, "rights," stock dividends, acquisitions, etc. that there is virtually no relation between "points" on the Dow-Jones, and dollars in the marketplace. The NYSE Index is intended to provide a direct dollars-and-cents measurement of the variation in the average stock price by allowing continual variation of the constituents of the index. The base of the Index is (Dec. 31, 1965 = $50.00), and the Index is calculated by the formula:

$$I = \frac{\Sigma \text{ Current Market Value}}{\Sigma \text{ Base Market Value}} (50)$$

The current market value can be obtained by multiplying the number of shares listed (for each stock) by the price. Stock splits and dividends merely change the number of listed shares, and "rights" values are added if applicable. These adjustments are also made, proportionately, to each constituent of the base market value.

Prediction: Trends, Regression

The mechanisms of prediction involve the finding of those characteristics of past statistics which will enable us to deduce what the future statistics will be. The statistics of interest may be aggregative, such as index numbers, or specific, such as the price of a particular stock. In simple cases, we may be able to find a single mathematical curve which will fit the observed data. As an example, one of the invaluable bits of information in the 1966 Statistical Abstract of the United States is reproduced in Table 3: "The average speed of motor vehicles on tangent sections of main rural highway during off-peak hours." In Fig. 1 we have plotted the "passenger cars" portion of this table in a form known as a **scatter diagram**. This diagram appears to be amenable to the fitting of a straight-line curve of the form $y = ax + b$; the problem is to find the best-fitting line, on the theory that it will provide the best prediction. The most common means of accomplishing this is to use the **method of least squares,** which will provide a line for which the sum of the squares of the vertical distances from the plotted points to the line will be a minimum, i.e.

$$\Sigma(y_{io} - y_{ic})^2 = \min.$$

where y_{io} is the observed value and y_{ic} is calculated, given x_{io}, from the equation of our best-fitting line, $y - ax + b$. (This is called a **regression line** when it describes a set of means, as it does in our example.) Dispensing with the intermediate manipulations, we can find that the following constants provide the best fit through the method of least squares:

$$a = \frac{n \sum_{i=1}^{n} x_{io} y_{io} - \left(\sum_{i=1}^{n} x_{io}\right)\left(\sum_{i=1}^{n} y_{io}\right)}{n \sum_{i=1}^{n} x_{io}^2 - \left(\sum_{i=1}^{n} x_{io}\right)^2}$$

$$b = \frac{\sum_{i=1}^{n} y_{io} - a \sum_{i=1}^{n} x_{io}}{n}$$

TABLE 3

Speed of Motor Vehicles (MPH)

	1945	1950	1955	1957	1958	1959	1960	1961	1962	1963	1964
Buses	45.5	49.8	52.6	52.6	53.6	53.5	55.5	55.3	56.0	58.1	57.3
Pass. Cars	45.0	48.7	52.1	52.6	52.8	53.3	53.8	53.7	55.1	57.1	56.9
Trucks	39.8	43.0	45.8	47.0	47.3	47.3	48.2	48.2	49.4	51.3	50.9

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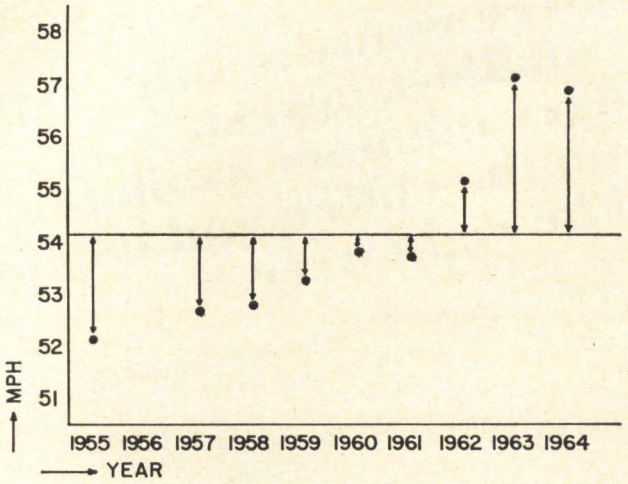

Fig. 4 Variance of $y = \bar{y}$

Performing these horrible calculations on the passenger car speed above, we find (letting 1954 = 0):

$a = 0.549$
$b = 50.9$

The best-fit line is shown in Fig. 2, and based on it we might predict that the average passenger car speed by 1970 will be about 60 mph. Since this is a mean, we will expect as many cars to be exceeding 60 as driving less than 60, which might point to either a raising of the highway speed limits or an increase in the workload of traffic courts.

There are many potential characteristics of statistical curves over a time base which should be taken into account when the black art of prediction is being practiced. Depending upon the needs of the prognosticator, these may be nuisances to be adjusted out, or they may be the result he is after. The three principle characteristics are:

- The long-term trend — sometimes called the **secular trend;** this is a supposedly smooth movement or gravitation over a relatively-long period of time.

- **Cyclic variations** — these reflect the effect (correlation) of other phenomena on the statistics at hand; for example, if we plot department store sales on a monthly basis, we will discover cyclic variations related to the time of the calendar year. Other statistics may vary with the supposed business cycle.

- **Transient variations** — these reflect the correlation of the statistics with some random factor such as war, the horsepower race in automobiles, presidential elections or assassinations, etc.

A statistical curve, then, can be crudely related to an electrical signal which is the superposition on a steady-state condition (the secular trend) of periodic ac components (the cyclic variations) and aperiodic transients (the transient variations). Prediction requires at least an adequate divining of the secular trend and cyclic variation, and one takes one's lumps on the transients.

Correlation

Techniques exist for the establishment of correlation between two sets of data, and we shall touch only briefly on one, the **coefficient of correlation.** Using the technique described above, we can create a best-fit relationship between any two events; the coefficient of correlation measures whether or not the linear relationship thus established is significant, or whether we have created a meaningless line. The coefficient of correlation is a comparison of the fit to the data of the least-squares line, with the fit of a line drawn through the mean of the y variable:

$$\rho = \sqrt{1 - \frac{\sum_{i=1}^{n} (y_{io} - y_{ic})^2}{\sum_{i=1}^{n} (y_{io} - y)^2}}$$

Since $\Sigma (y_{io} - \bar{y})^2$ cannot be less than $\Sigma (y_{io} - y_{ic})^2$ by the definition of the least-squares method, the ratio of the summation terms will vary from 1 in the uncorrelated case to 0 in a completely correlated case (i.e., all data points are on the least-squares line). Therefore ρ varies from 0 to 1, with $\rho = 0$ indicating no correlation, and $\rho = 1$ signifying perfect correlation. (Actually the range $-1 \leq \rho \leq +1$ is used, but this is unimportant for our nonrigorous interest.)

Since earlier we established a correlation between passenger car speeds and the passage of time, we shall now calculate the correlation coefficient to determine whether the apparently descriptive line we created really described a correlation strong enough to use for predictive purposes. Figs. 3 and 4 illustrate the mechanism of the correlation coefficient. We shall compare the sum of the squares of the distances of the data points from the best-fit line (Fig. 3) with the sum of the squares of their distances from the line $y = \bar{y} = 54.16$ (Fig. 4). We find that $\rho = 0.925$, indicating an excellent (strong) correlation between average speed with the passage of years.

One caution should always be observed. A strong correlation is often indicated between two unrelated events, simply because both events happen to be related to some third event, such as the passage of time. For example, we could establish strong correlation between the number of UFO sightings and the number of persons admitted to mental hospitals, simply because both are increasing with respect to time.

Next month we shall conclude this series of Selected Topics in Probability and Statistics with a discussion of statistical sampling, illustrating the methods by which one can predict "long run" events (such as presidential elections) through the intelligent gathering of limited samples. The confidence factor which can be associated with conclusions based on statistical evidence will also be presented.

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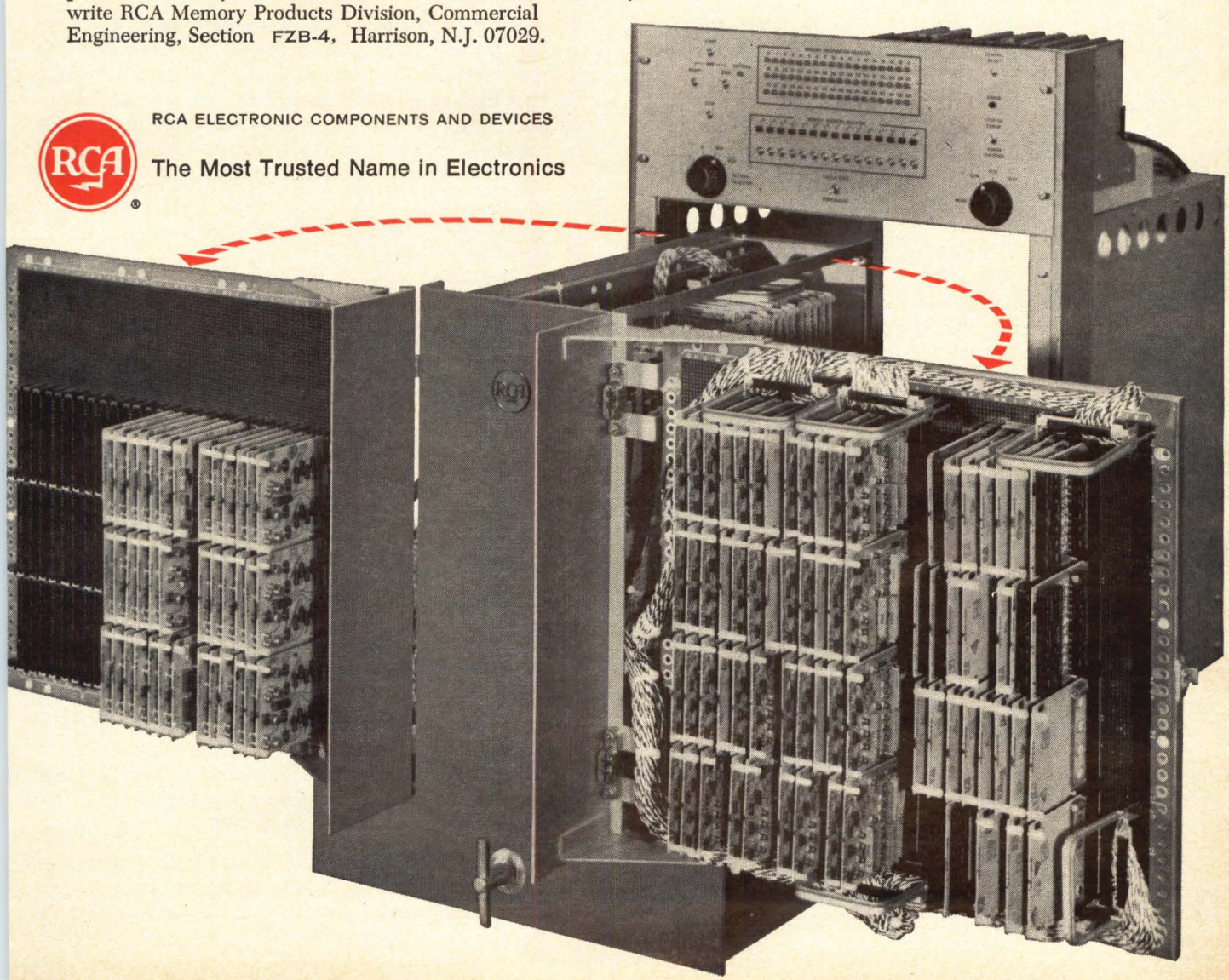

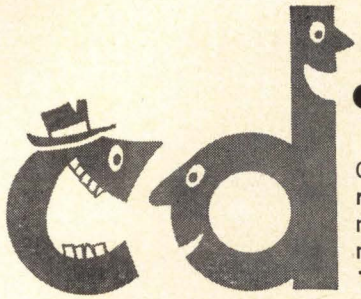

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

SMALL GENERAL-PURPOSE COMPUTERS ARE REPLACING SPECIAL-PURPOSE COMPUTERS

GEORGE F. MANAHAN and DAN C. DURAND

The advantage of flexibility in the application of general-purpose computers to digital control system configurations has been recognized as long as the industry has existed. Historically, however, the cost/performance ratio of general-purpose machines in the early days of the industry was prohibitively high to allow their economic integration as controllers within total system configurations. Special-purpose "wired-program" systems were therefore configured with digital building block modules to accomplish certain control functions within overall systems. These were later followed by patchboard systems having limited program flexibility. Stored-programmed controllers came next in the large control systems. These, however, were of a pseudo-general-purpose nature, since they were designed to fit a particular application, which made them either totally unacceptable or very inefficient for use in other application areas. Also, the software for these systems was generally written in machine language and therefore very expensive to produce, and incompatible with other processors.

Evolution of digital hardware and software technology has improved the cost/performance ratio by more than two orders of magnitude over the past fifteen years — to the point where the general-purpose processor now represents a small fraction of cost in most system configurations. A few application areas where "off-the-shelf" general-purpose processors have replaced special-purpose controllers of the three types mentioned above are:

- Information storage and retrieval
- Message switching
- Data concentration
- Process control
- Flight trainer control
- Data acquisition and data logging
- Machine tool control
- Data display
- Graphic arts control
- Off-line data conversion.

In considering the pros and cons of general-purpose versus special-purpose control, the system designer must weigh the following factors.

- Hardware design versus operation software design — These generally balance out but the software of the general-purpose machine is useful in future improvements or expansion of the total system and is much more amenable to such changes. Also, computer-independent software languages (exclusive of special input or output communications) provide upward compatibility within computer product lines, allowing easy exchange of the processor if problem scope grows.

- Recurring costs for identical system hardware — The general-purpose system is probably more expensive than the equivalent hard-wired system on

George F. Manahan is Communications Systems Engineer at the Computer Control Division of Honeywell. He is responsible for various aspects of electronic design, project control, and administration. Dan C. Durand is the Director of European Operations for the Computer Control Division of Honeywell. He is responsible for all systems operations and marketing in the United Kingdom and Europe.

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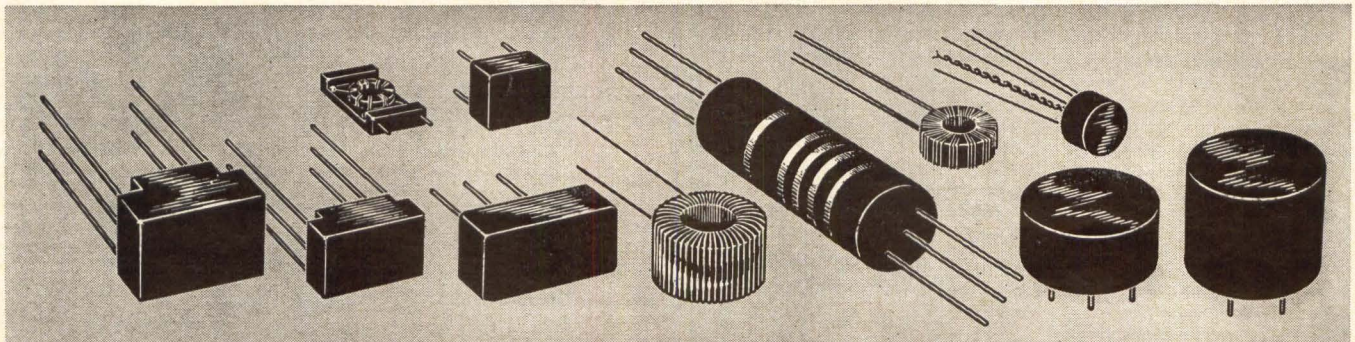

Here are commonly used packages for which tooling is available. Other configurations are always possible.

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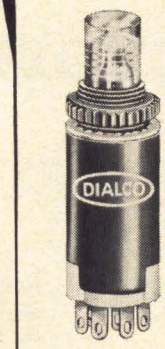

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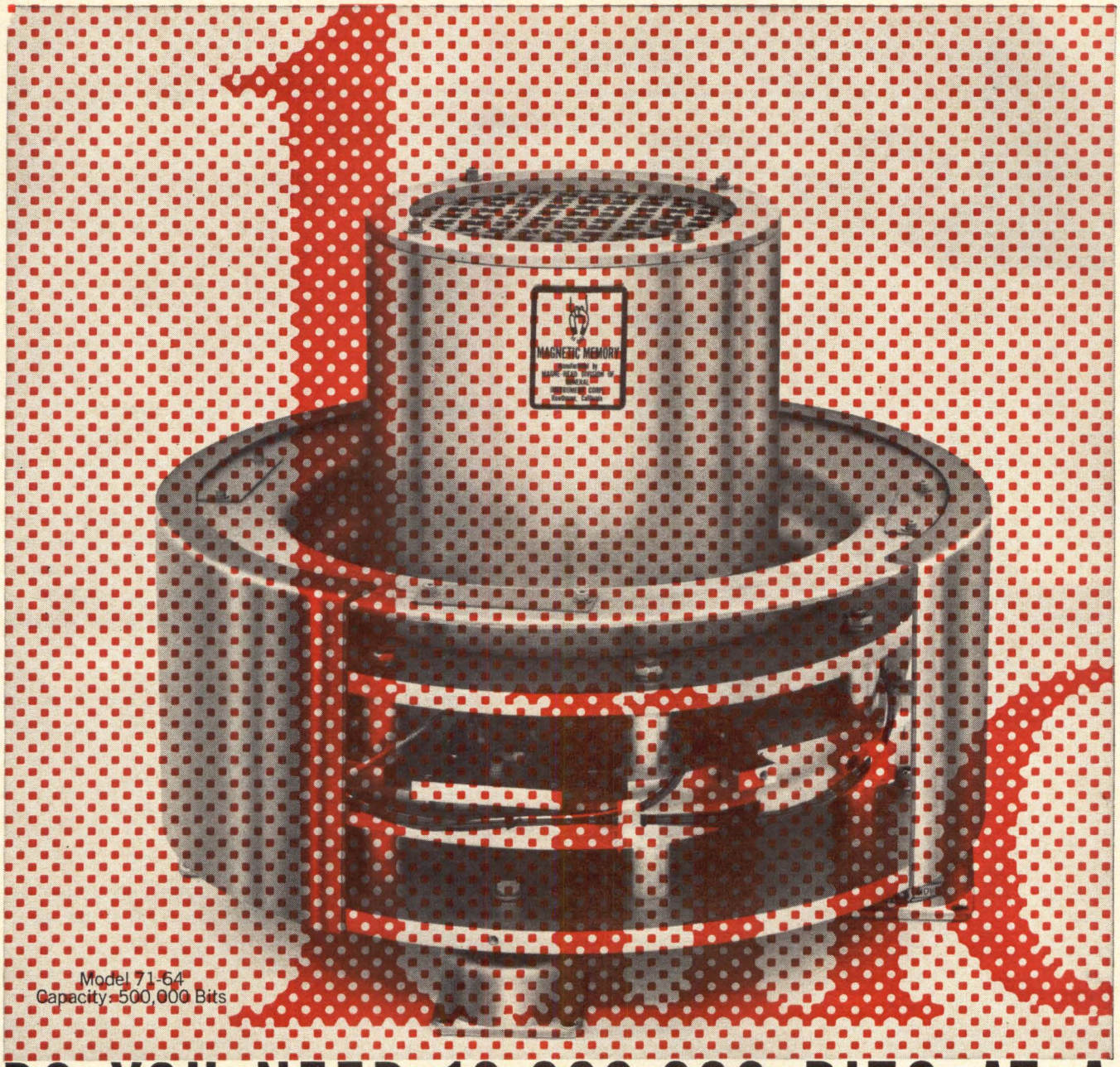
a repeat basis. Certain functions of the general-purpose controller may not be necessary for a particular application. For example, multiply-divide instructions are unnecessary in data switching applications. Logical instruction may not be necessary in certain machine tool control applications. There is also the probability that off-the-shelf processors contain more than the minimum core memory necessary for the operational program. However, these cost factors are generally balanced out by the compatibility of the general-purpose controllers across a complete line of products a manufacturer may be supplying to a particular market; i.e., the machine tool, graphic arts, or process control systems supplier may have several product lines of hardware all controlled with a single type of processor. This allows him the advantage of maximum standardization and lowest cost in purchasing the computers.

• Cost of "breadboarding" prototype hardware — Use of a general-purpose computer for this function offsets prototype development costs and minimizes the time required for development and experimental analysis. The computer is also available at the end of this period for other functions.

• Cost of programming each problem — Certain applications are identical from system to system, and the initial programming cost may be pro-rated. Other applications involve recurring programming cost to adapt to each new situation. Special input and output requirements (analog, digital, pulse, display, keyboard, etc.) contribute heavily to programming costs. No recognized standard software language for communicating with control type input-output signals has evolved to date. Consequently, control input-output programs must be implemented in machine language for the equipment in question (at a high programming cost). A combination of input-output hardware with pre-processing capability plus an accepted language of communication could reduce future recurring programming costs below the current levels.

There are other peripheral advantages that one secures with a general-purpose computer-based system: flexibility of modular hardware and software; relative ease of expandability of memory and addition of peripheral devices; and reliability designed into product-line hardware.

The day is rapidly approaching when there will be virtually no real-time environment, sophisticated electromechanical device, or data processing application that cannot be more economically controlled with a standard general-purpose machine of some type rather than a special-purpose controller.



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CIRCLE NO. 34 ON INQUIRY CARD

from our man in Washington

Congress has been asked to approve $2,723,000 for computer science and technology work at the Bureau of Standards in the 1968 budget. In Fiscal 1966, $1,141,000 was spent on this activity and an estimated $2,034,000 in Fiscal 1967. The increase would be used for the development of uniform Federal standards and for assistance to other Federal agencies in optimizing the effectiveness of their data processing installations. Another proposed 1968 appropriation is that of $10,000,000 which would represent the initial capital for the EDP fund authorized under legislation passed by Congress in October 1965 to provide for efficient use of EDP equipment by the Government.

.....

U. S. manufacturers of computers continued, in 1966, to export heavily despite the considerable expansion of U. S. production abroad, the Commerce Department reports. Sales of these machines went up by a third to meet rising foreign demand not only for EDP equipment, but also for industrial control apparatus to achieve greater reliability and uniformity in production and to insure closer tolerances on machine work. Accordingly, most of the increase went to the industrial countries, especially Canada, the United Kingdom, Germany, and France.

.....

Precise control of a laser's intense coherent light to position a beam to any of 131,072 points, within a space smaller than a match head and at speeds exceeding 100,000 selections-per-second, is under Army study for high-speed computer printouts. Now in exploratory development at the U. S. Army Electronics Command (ECOM), Fort Monmouth, N. J., the experimental equipment was produced under contract by IBM. Considering its potential to store data, provide printed readouts, and project images, ECOM scientists envision a system in which such inputs as typed material, charts, and line drawings could be fed into a computer. Relayed hundreds of miles by radio to another computer, they could be processed and reproduced instantly as printed pages or as greatly-enlarged screen displays.

A computer-equipped system which provides instant information on procurement actions throughout the Army Materiel Command (AMC) has been inaugurated at the Army Electronics Command, Fort Monmouth, N. J. When in full operation, the system, called Standard Work Ordering and Reporting Data System (SWORDS), will establish a data bank of contractual information at every AMC installation involved in providing or using work ordering service. Another function of the system provides instant communication between all AMC elements and the Defense Contract Administration Services on daily procurement actions. Information on the actions can be fed into one installation's computer by magnetic tape or punch cards and be immediately available at the others.

.....

The Internal Revenue Service reports that in January alone it refunded $6.6 million to 51,000 taxpayers thanks to the help of EDP. This is the first year every individual and business Federal tax return is being processed with IRS's EDP system. Under the system, returns are routed to seven IRS service centers where magnetic tapes are prepared and forwarded to the National Computer Center at Martinsburg, W. Va. Here the information is processed against master files for all taxpayers and the tapes authorizing refunds are sent to the Treasury's Disbursing Offices for issuing refund checks.

.....

Senator Warren G. Magnuson (D. Wash.), Chairman of the Senate Commerce Committee, has introduced a bill to make critically-evaluated reference data readily available to scientists and engineers. The bill, requested by the Commerce Department, would authorize the Secretary of Commerce to arrange for the collection, compilation, critical evaluation, publication, and dissemination of standard reference data. Authority also would be provided the Commerce Secretary to utilize, with their consent, the reference data services and facilities of other government agencies, federal, state and local, and to prescribe and publish

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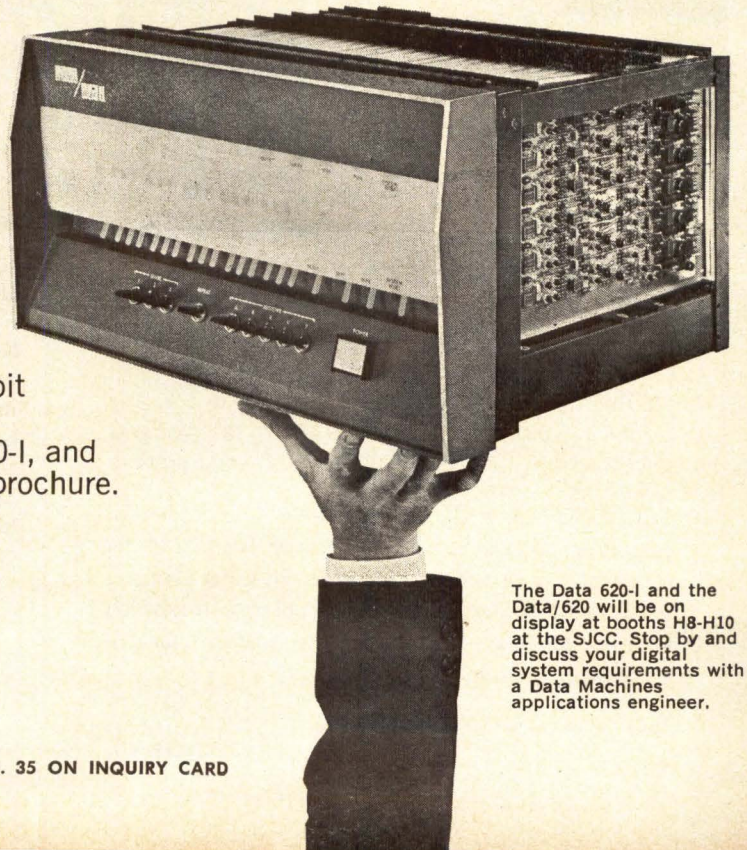

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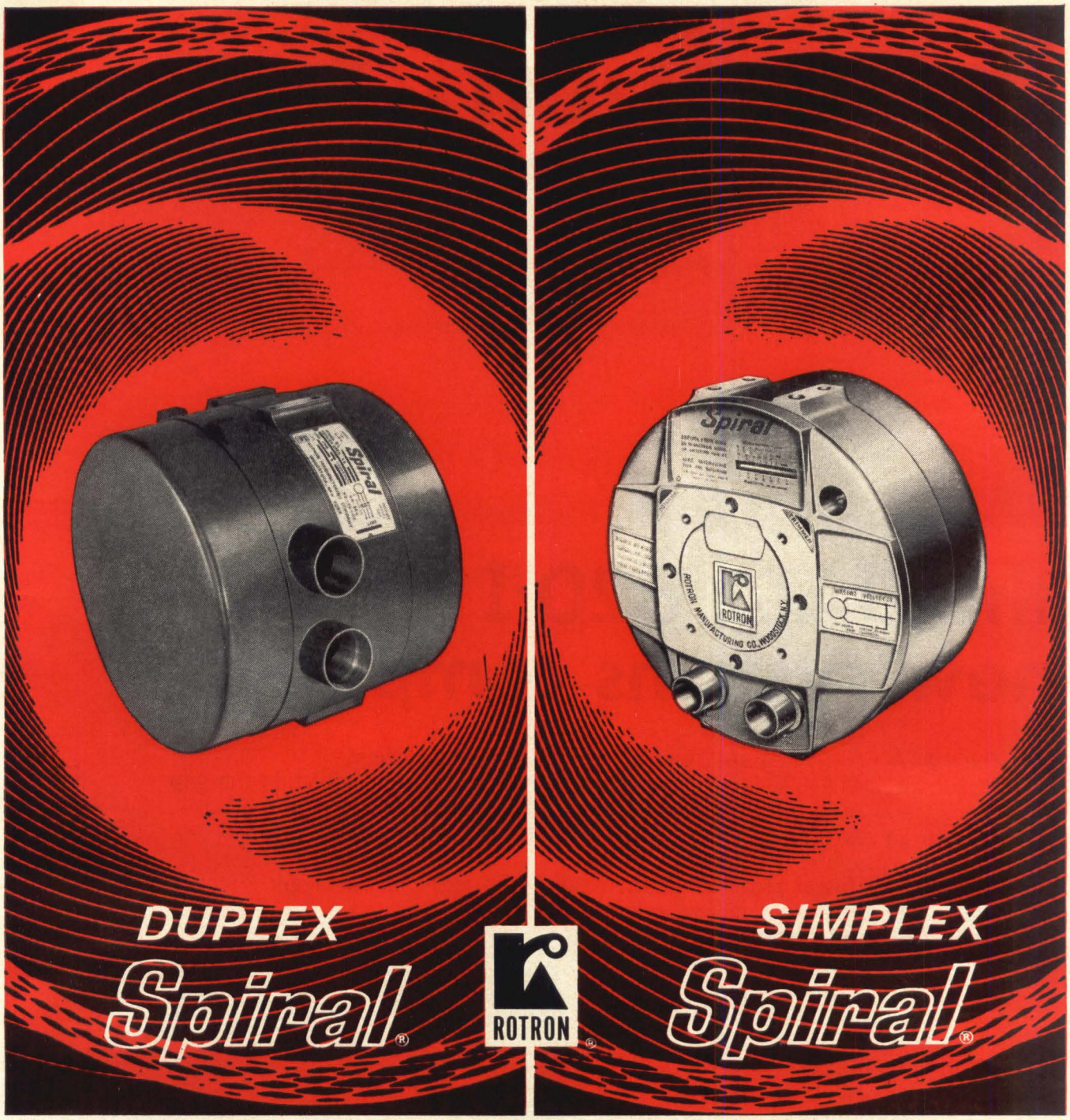

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in the Federal Register such standard reference data as may be necessary to carry out the Act.

Recent Government Contract

NASA has awarded contracts for the major subsystems for the two-spacecraft Mariner mission to Mars in 1969. The central computer and sequencer and command subsystems will be produced by the Military Electronics Division of Motorola, Scottsdale, Ariz. Litton Industries, Guidance and Control Systems division, Woodland, Cal., will do the data automation system.

GOVERNMENT REPORTS ★★

COMPUTER WORD RECOGNITION

A recent MIT report on the scope of automatic speech recognition, technological aims, and other aspects of this complex problem states that talking to computers appears to be the most promising application of a word recognizer. In the work described, recordings were made of 10 male speakers, each of whom read the same list of 54 computer-oriented words. All processed words were passed through the word-recognition program and the results of the measurements were tabulated. The main function of the program was to segment the word, make 15 measurements after segmentation, and file these measurements for each of the 540 spoken words. The tabulation of all measurements was printed and after inspection of the data, a decision algorithm was devised. All words were then passed through this algorithm and the results tabulated and printed. Out of the 540 words 74 were incorrectly classified by the program. The report describes in detail the computer facility, segmentation, the measurements, and the decision algorithm, and discusses the results that were obtained.

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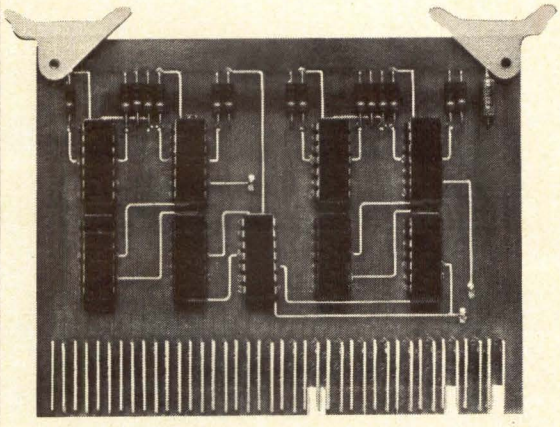

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What do you think?

This department is devoted to a continuous interchange of ideas, comments, and opinions on significant problems facing the industry. What do you think about the impact of a computer-automated world and the engineer/scientist's role in it? What do you think about engineering unions — professional societies — industry conferences? Or any significant facet of your professional life. COMPUTER DESIGN will print your views here. Write to: CD Readers' Forum, Computer Design, Baker Ave., West Concord, Mass. 01781.

CD READERS' FORUM

CHARACTER STRUCTURE AND CHARACTER PARITY SENSE FOR PARALLEL-BY-BIT DATA COMMUNICATION IN ASCII — A Proposed USA Standard

EDITOR'S NOTE: *This month we continue our presentation of the current activities of the USASI, with extracts from a currently proposed standard. "This Proposed USA Standard has been approved by Subcommittee X3.3 and has been accepted for publication by the USA Standards Institute Committee X3, Computers and Information Processing. In order that the final version of the proposed standard reflect the largest public consensus, X3 has authorized publication of this document to elicit comment, criticism, and general public reaction with the understanding that such a working document is an intermediate result in the standardization process and is subject to change, modification, or withdrawal in part or in whole." All comments which are sent to CD Readers' Forum will be forwarded to the USASI.*

PROPOSED AMERICAN STANDARD

Scope

• This standard specifies the character structure and sense of character parity for parallel-by-bit, serial-by-character, data communication in the American Standard Code for Information Interchange (ASCII).

• This standard applies to general information interchange at the interface between Data Processing Terminal Equipment (such as data processors, data media input-output devices, office machines) and Data Communication Equipment (such as data sets, modems).

Standard Character Structure

The character structure shall consist of eight bits, i.e., seven ASCII bits plus one character parity bit.

Standard Bit-to-Channel Relationship

The seven ASCII bits (b_1 through b_7) plus the character parity bit (P) shall be assigned to an ordered series of channel designators as follows: b_1 to the lowest designator, and in ascending order, with P to the highest designator.

ASCII Bit:	b_1	b_2	b_3	b_4	b_5	b_6	b_7	P
Channel:	1	2	3	4	5	6	7	8

Standard Sense of Character Parity

The sense of character parity shall be ODD over the eight bits, i.e., an odd number of "1" (marking) bits per character.

Qualifications

This standard does not specify the character synchronizing technique, the character rate, nor does it apply to serial-by-bit, serial-by-character data communication.

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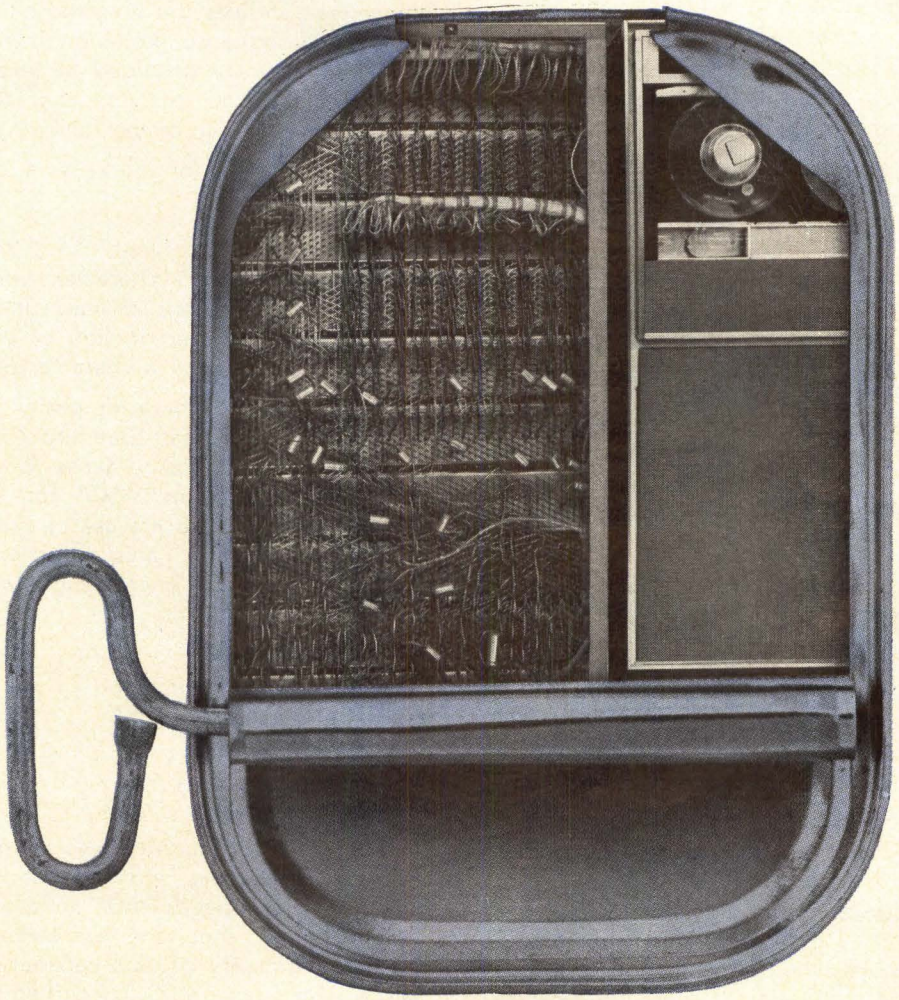

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The character rate is specified in the proposed Standard X3.3.6/2 Parallel Signalling Speeds for Parallel-by-Bit Data Transmission in the ASCII.

APPENDIX "A" CRITERIA

• This Appendix contains the criteria upon which the character structure, bit-to-channel relationship and the character parity sense were based. Not all criteria have been entirely satisfied. Some of these criteria conflict with others, and the character structure and the character parity sense specified represent compromises among these divergent criteria.

• Criteria were drawn from communication aspects of information interchange as well as processing and media recording aspects of information interchange.

• One hundred twenty-eight characters should be uniquely specified.

• A single character structure should be specified regardless of the transmission facility, speed, or modulation technique.

• No ASCII character should require special treatment.

• The character structure for parallel-by-bit communication should be consistent with that for serial-by-bit communication.

• Each character should contain a single character parity bit.

• The character structure and character parity sense should cause minimum confusion to maintenance and operating personnel.

• The character structure should be independent of the existence of a timing channel.

• There should be no restrictions on sequences of characters, e.g., successive Null, Sync, Space, Zero, or Delete characters.

• Maximum compatibility should be provided with the parity sense requirements of the various media.

• The character structure and sense of the character parity should be the same regardless of the data transmission technique, the transmission facility, speed, or modulation technique, and should not preclude the use of any technique.

• Equipment complexity should be minimized when alternately handling other codes or random binary data.

APPENDIX "B" DESIGN CONSIDERATIONS

System factors considered in this standard are transmission efficiency, reliability, error control, media requirements, equipment complexity, maintenance confusion, and transition to and from alternate non-ASCII codes or random binary data.

Character Structure and Bit-to-Channel Relationship

• The overriding consideration affecting the choice of character structure is compatibility with serial-by-bit data communication in order to minimize confusion. An eight-bit character structure (7 ASCII bits and parity) satisfies this requirement as well as all other criteria.

• The overriding consideration affecting the assignment of the bits to the channels is the need for a simple and orderly relationship. This requirement and all other criteria are satisfied by a b_1 to channel 1, b_2 to channel 2, etc. relationship.

Sense of Character Parity

• The choice of character parity sense, odd or even, involves a choice between clearly conflicting sets of criteria. Consistency with the standard for serial-by-bit data communication cannot resolve this choice since the standard specifies EVEN parity sense for asynchronous transmission and ODD parity sense of synchronous transmission. Essentially, the remaining criteria present a choice between media consistency with paper tape (EVEN argument) and the possibility of detecting character presence from the data alone (ODD argument). Since it is desirable to allow character detection without the requirement for a timing channel, and the character parity sense can be inverted by the EDP terminal if required by the particular medium, ODD character parity sense was chosen.

• This implies that the data channels themselves must contain sufficient information to define character timing. If successive characters are different, a change of binary state defines the presence of a character. Such a character sequence limitation is neither allowable, nor is it necessary provided at least one change of binary state occurs in every character. This can be accomplished if both of the following criteria are met:

(a) Defining a "1" (or mark) as a change of binary state (NRZI coding);

(b) Defining the character parity sense as odd.

If this is done, every character will contain at least one "1" and therefore at least one transition. This transition can be used in lieu of a timing signal to define the presence of a character on the line.

• The use of odd character parity is consistent with the Proposed American Standard for Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in the ASCII for synchronous data communication. Since the use of synchronous systems is increasing rapidly, this consistency is important. ODD parity has also been designated as the standard for all military systems.

EXPOSITORY REMARKS

Subcommittee Report

• The X3.3 Subcommittee was assigned the responsibility for developing recommendations for digital data communication speeds and formats, specifications for system performance and end-to-end control characteristics, a glossary of data communication terms, and liaison with other groups concerned with the above or

who have an interest or related involvement in data communication.

- Task Group 3, on Data Transmission Formats was organized in late 1962 and was charged with the responsibility for the development of standards of formating, or data transmission of characters within a hierarchy of groupings (e.g., words, blocks, messages, etc.) including group error control and ordering (for sequencing) of bits within characters, including parity. The task group is also responsible for determination of the character parity sense, determination of character framing, defining a standard format for the reverse channel, the number of channels and bit-defining assignments, and defining the character format of the subsets and supersets of ASCII.

- Proposed American Standards for Bit Sequencing of the ASCII in Serial-by-Bit Data Transmission and for Character Structure and Character Parity Sense for Serial-by-Bit Data Communications have been developed and are currently being processed.

- There is as yet insufficient experience to allow proper consideration of reverse channel formats. For this reason, the development of a standard has been postponed.

- This proposal defines the structure of a character in parallel transmission, including the assignment of bits and the definition of parity.

Character Structure

- There have been many historical arrangements that have developed to achieve the parallel transfer of information. In teletypewriter equipment, the parallel transfer occurred from tape through sensing pins to a mechanical cam or distributor where the signal was transmitted serially. The use of channel or track designations evolved from the "bit designation" given to the holes in the tape which, in turn, evolved from the order of transmission of the bit stream. In 5-track tape the bit designation was 1-2-Feed Hole-3-4-5. In 6-track teletypesetter tape, the paper tape nomenclature became 0-1-2-Feed Hole-3-4-5 for easy reference on the tape while transmission on line was bit 1-2-3-4-5-0 for technical reasons.

- In ASCII development, the bits of the character were first defined as b_1 through b_7. Early equipment using ASCII carried forth the paper tape nomenclature, i.e., track 0-7 representing b_1-b_7, P. However, it was soon realized that a track representation consistent with the bit designation was desirable. The tracks were renumbered 1-8 and a consistent bit-to-track relationship was specified.

- A common parallel-by-bit data set uses a channel designation based upon technical considerations for the timing channel. The convention assumed for channel numbering was that the timing channel should be at the middle of the band with the other channels assigned to the bits of a character. For example:

Frequency Assignment (Cycle/Second)										
Channel Number	Mark	730	900	1070	1240	1410	1580	1750	1920	2090
	Space	800	970	1140	1310	1480	1650	1820	1990	2160
		1	2	3	4	Timing	5	6	7	8

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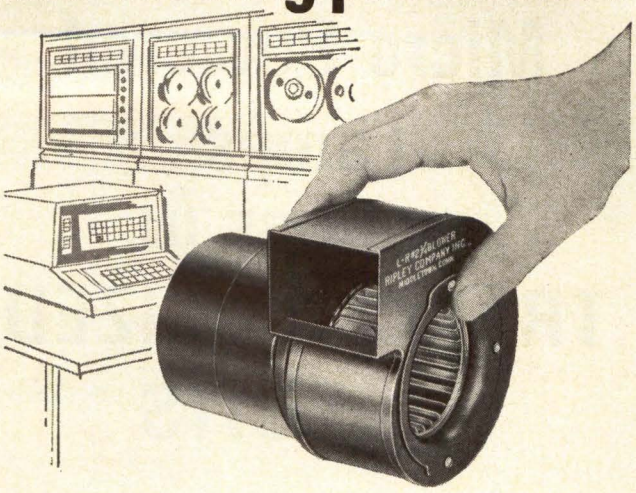

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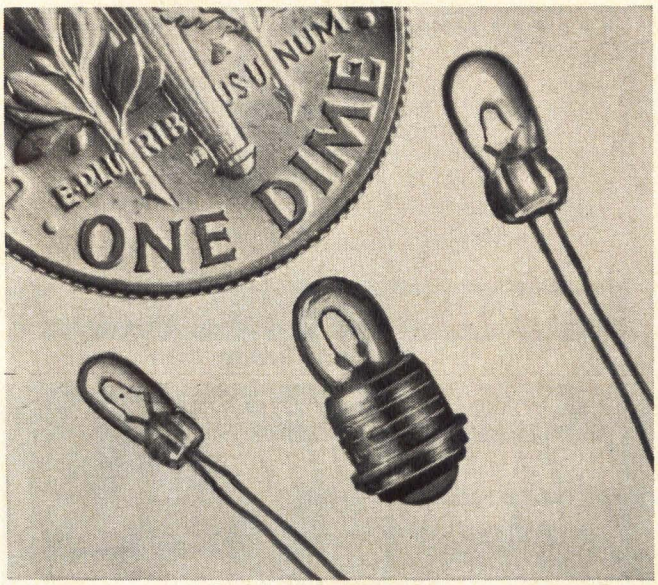
Micro-Powered Lamps
FOR USE IN TRANSISTORIZED CIRCUITS



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• The bit position is to be assigned at the interface between the data processing equipment and the data communications equipment. It appears logical to assign the ASCII bits to the interface in an ascending order, starting at b_1, to conform to the proposed EIA standard channel designation. The channel and bit numbering is therefore the same for all media; in some media (e.g., paper tape), this also results in a corresponding track number; in others (e.g., magnetic tape) track numbers would be different.

Timing Channel

• The use of a timing channel with some parallel transmission systems should not affect the assignment of the ASCII bits to the parallel interface. It is expected that the designation of the timing channel will be independent of the channel designations.

Transmission of a Character Parity Bit with ASCII

• Two alternatives exist: (1) a character parity bit is always transmitted and, (2) transmission of a character parity bit is optional.

• Since a character parity bit is transmitted in some equipment, there is an advantage in always specifying its inclusion, i.e., the character structure would always be the same. Including a character parity bit permits simple error checking. However, transmission throughput can be increased if the character parity bit is not transmitted. This is desirable in at least two cases: (1) where error checking is not used and, (2) where the system employs other means of error control.

• The proposed American Standard for Character Structure and Character Parity Sense in Serial-by-Bit Data Communications includes the parity bit in synchronous and asynchronous transmission.

• In order to provide a consistent proposal for all data communication, a parity bit was also included as a part of the character structure in parallel-by-bit transmission.

Character Parity Sense Within Media

• The American Standard Perforated Tape Code for Information Interchange specifies EVEN parity sense per character so that the Null and Delete characters retain the all "0's" and all "1's" combinations respectively, including parity. It is expected that EVEN character parity sense will be used in edge-punched documents for the same reason.

• The proposed American Standard Recorded Magnetic Tape for Information Interchange specifies ODD character parity sense over the nine tracks so that the Null character may be recorded and sensed on magnetic tape.

• The representation of ASCII in punched cards is still under consideration and as yet there are no parity sense requirements in 12-row punched cards unless it is decided that ASCII be represented in direct binary.

In the case of direct binary representation of ASCII in punched cards, EVEN parity sense would be required to handle the Null and Delete characters.

• Optically and magnetically scanned document character parity sense requirements are not defined at this time. There are various optical or magnetic document reading techniques in use. No preferred technique has yet evolved. The relationship of the technique to the definition of the character parity sense appears to depend on two criteria:

(a) Whether or not the media can be erased. A requirement to erase by overwriting with Delete characters implies an all "1's" character which demands EVEN character parity sense.

(b) Whether or not a separate timing channel is used. If not, at least one "1" bit per character is required, implying ODD character parity sense.

• There are other media which may utilize ASCII. Among these are badges, time clock cards, switch or keyboard entry, etc. The representation of ASCII in these media may not be in any of the forms described above. There seems to be little evidence for any particular parity sense requirements except insofar as these media are susceptible to the same criteria listed above.

CHOICE OF CHARACTER PARITY SENSE

• The use of EVEN character parity is consistent with the American Standard Perforated Tape Code for Information Interchange. This specifies EVEN character parity sense to allow overwriting with the Delete character. It is expected that edge-punched documents will utilize EVEN character parity sense.

• The use of EVEN character parity is consistent with the Proposed American Standard for Character Structure and Character Parity Sense for Serial-by-Bit Data Communication in the ASCII for asynchronous data communication. Since parallel-by-bit and asynchronous transmission systems operate in the same speed range, this consistency is important.

• Some 8-level foreign code transmission terminals are used to transmit both ASCII and other 8-level codes interchangeably. If this is a paper tape terminal, ODD parity would require an inversion in the 8th bit position.

END

Government Reports ★★

SEQUENTIAL DECISION PROCESSES

An elucidation of the class of optimization problems that can be solved by dynamic programming techniques and a general method for solving terminating dynamic programming problems are covered by a 40-page report. An algorithm that can be used to analyze a broad array of sequential decision processes is included.

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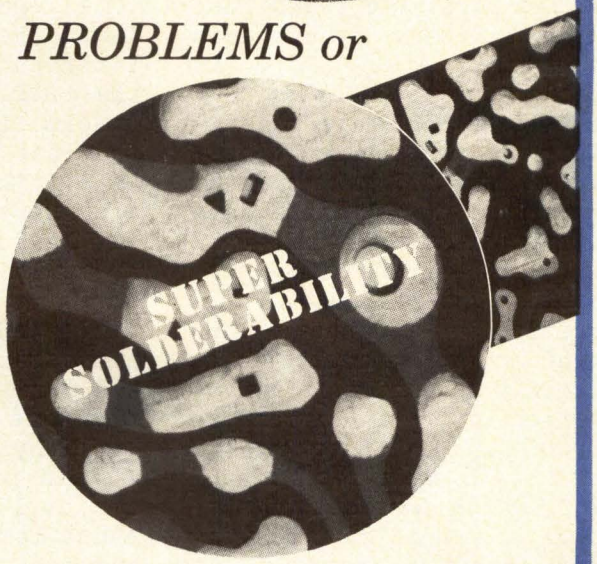

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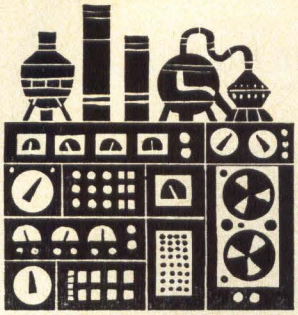

INDUSTRY NEWS

AN ADVANCED COMMUNICATIONS TECHNIQUE THAT CAN DOUBLE THE SPEED AT WHICH IBM COMPUTERS "TALK" TO EACH OTHER BY TELEPHONE was announced by IBM Corp. The technique, called Binary Synchronous Communications (BSC), is designed specifically for IBM System/360 Teleprocessing networks. The new transmission method is being used in a high-performance data transmission terminal — the IBM 2780 — introduced recently, as well as in two previously announced communications products. The ability to send more information over a communications line in a given period of time is made possible by BSC, which consists of special electronic circuitry and computer programs. It can increase the speed at which data is sent and received from 25 to 100 percent by more effectively regulating the flow of data characters into the transmission line.

COMPUTERS WILL NEVER REPLACE LAWYERS BUT THEY MAY WELL REVOLUTIONIZE THE PRACTICE OF LAW, predicts a University of Southern California educator. Vaughn C. Ball, who is Legion Lex Professor of Law in USC's Law Center, foresees a day in the not-too-distant future when a lawyer will write his own computer program, transmit it from his office by direct line to a computer center, and have an answer to a legal question in seconds. Ball believes the computer will be used to search legal literature, analyze problems of law, and even simulate legal processes. The fantastic increase in legal literature will make use of the computer, as a tool for information retrieval, an absolute necessity, says Ball. "Case records alone are increasing at the rate of 70 million words a year," he explained. "I don't see how we can possibly disregard the advantages data processing offers. Because the computer can work all of the time and perform with both high speed and accuracy it can produce results no man could get — only because he would first die of old age. Furthermore, with the aid the computer can give, the legal profession can simply do a better job all around." The USC law professor anticipates resistance from the legal profession to the whole computer idea. But this will be overcome, although it may take a considerable period of time, he believes.

THE NATIONAL CASH REGISTER COMPANY HAS ENTERED INTO AN AGREEMENT WITH THE RADIO CORPORATION OF AMERICA UNDER WHICH EACH COMPANY GRANTS RIGHTS TO THE OTHER under its patents in the EDP field. This cross-licensing agreement is designed to free both companies from patent infringement conflicts which could arise in the increasingly complex computer field, NCR pointed out, but it does not involve any exchange of know-how. The agreement covers not only patents on NCR and RCA computers, as such, but also patents pertaining to other products of the two companies when those products are employed as direct, "on-line" components of computer systems.

AN INTEGRATED ELECTRONIC CIRCUIT WHICH PROVIDES THE BASIS FOR A NEW TYPE OF HIGH-SPEED COMPUTER SCRATCHPAD MEMORY THAT COULD RUN ON THE POWER OF FLASHLIGHT BATTERIES has been developed by RCA. The new circuits, each about the size of a housefly's eye, were achieved by using a novel "silicon-on-sapphire" fabrication technique developed at RCA's David Sarnoff Research Center, Princeton, N. J., in a program supported in part by the U. S. Air Force Cambridge Research Laboratories. Dr. William M. Webster, Staff Vice President, Materials and Device Research, RCA Laboratories, said the new circuits can be interconnected in large arrays to form extremely high-speed memories. An experimental memory employing the circuits and capable of storing nine bits of information already has been built by RCA, according to Dr. Webster. He said that it will lead eventually to similar memories that can store up to 256 words, each 16 bits long, and process the information at a rate of 20 million words per second. Credit for the development was given to two research teams, one headed by Dr. Charles W. Mueller which developed the silicon-on-sapphire technology, and the other headed by Gerald B. Herzog which designed the memory circuits.

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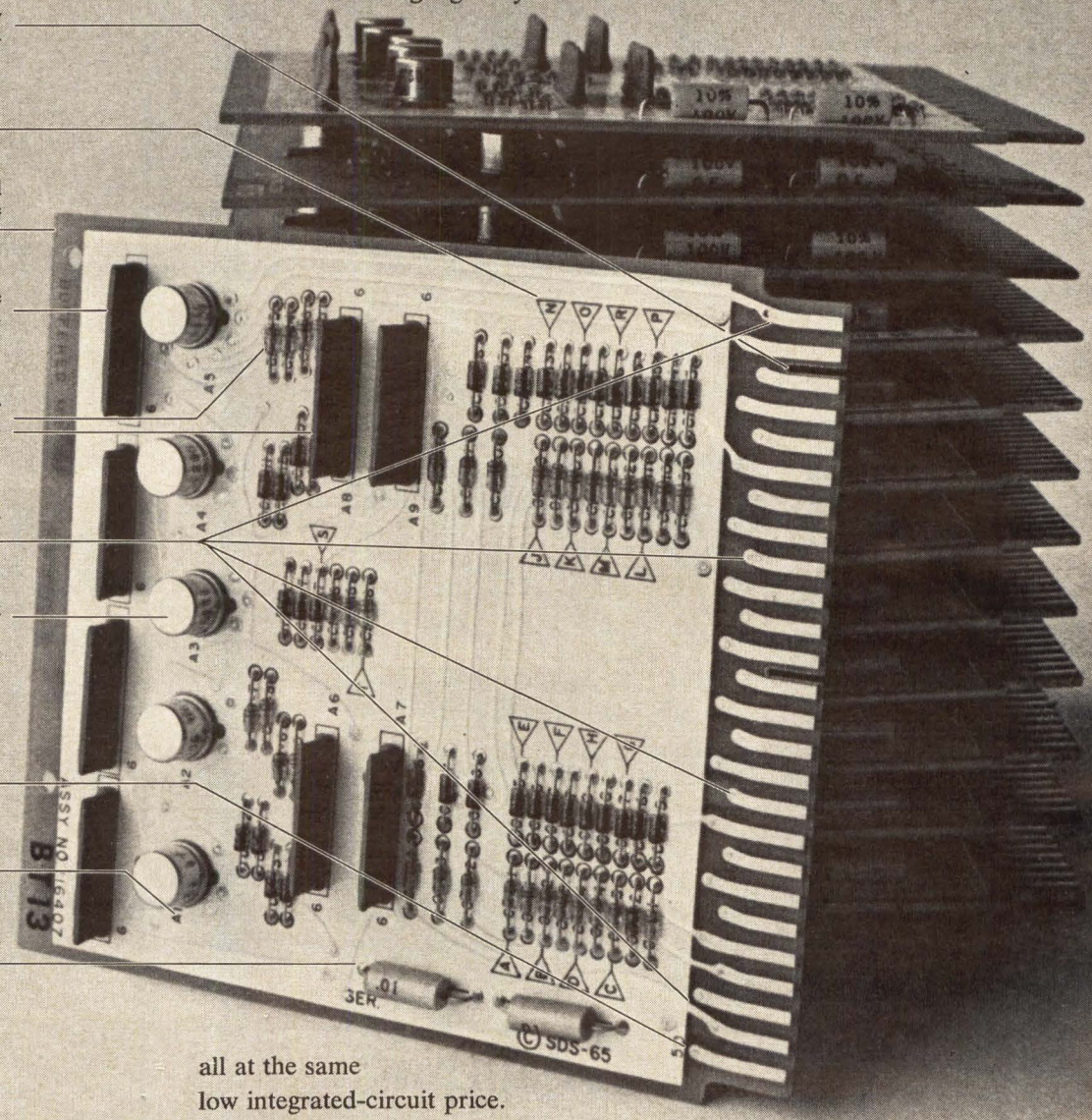
First come first served.

You can have all the SDS T Series integrated circuit modules you want now. We're in full production.

All T Series active elements are integrated circuits and guarantee reliable operation at clock rates to 10 mc. Each circuit output drives 14 unit loads, even after generous allowances for wiring capacitance.

Outputs switch 60 ma (4 times more than standard IC's). Noise rejection is at least 1.5 volts at the 0 and 4-volt logic levels.

SDS Natural Logic gives you AND and OR as well as NAND and NOR—



all at the same
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We designed these modules for our new Sigma computers, but we also intend to become the largest manufacturer of logic modules for system designers.

We don't want to give away any of our Sigma secrets.

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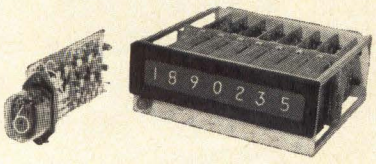
IC COUNTER
MODULES...

Transitron

Transitron's new integrated-circuit, high-speed decade counter modules have been developed for use by equipment manufacturers who need low-cost, highly-reliable counter operation. The new ND 500 Series includes 25mHz decade counters, 25mHz decade dividers, and 5mHz bi-directional counters. All units can be serially cascaded.

Integrated circuit design provides excellent reliability, high noise immunity.



Custom models cost less than you think

Special counter modules, custom-designed to meet your specific requirements, can be produced at surprisingly low prices . . . for fast delivery.

Numerical Displays

Complete "Transindicator" counter/display units are also available in both standard and custom designs.

Send for complete data on this new counter series.

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INDUSTRY NEWS

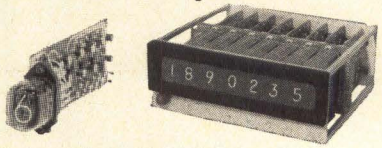
CONTROL DATA CORP. HAS ANNOUNCED A NEW MEDIUM-SCALE DATA PROCESSING SYSTEM, THE CDC 3150. According to the company, the 3150 provides a sound base for easy expansion. Its central processing capability, memory capacity, and peripheral equipment can be enlarged or modified as workload demands increase or computing applications change. The operating system provided for the 3150 is Control Data's disc pack storage system with an extensive and varied software product set. This system is said to provide a capability for time-sharing the 3150 between a foreground stacked-job activity and a background I/O or real-time activity. The 3150 computer system includes a central processor with desk console, I/O typewriter, 16K memory with a 1.75 usec. cycle time, two twelve-bit data channels, one twenty-four-bit data channel, peripheral controller electronics, one card reader, two disc storage drives with two disc packs, and one line printer.

SPONSORED BY THE ST. LOUIS-SAN FRANCISCO RAILWAY COMPANY, TWO RESEARCH ASSOCIATES ARE WORKING WITH THE NATIONAL BUREAU OF STANDARDS TO EXPAND THE USEFULNESS OF A COMPUTER SIMULATION MODEL of a railroad network. The railroad network model is a management tool for evaluating the effects of alternative operating policies on the total performance of a railroad network. According to the report the network analysis will deal with only freight train problems. Apparently, there are no problems with passenger trains.

FOR DEPENDABLE
NUMERICAL
DISPLAY...

Transitron

High-speed, integrated-circuit counter/display units providing high performance at low cost are available from Transitron's Special Products Division. Utilizing high-visibility, in-line neon display tubes, modules are available for side or end viewing. Both continuous and latching display types can be ordered, with options of 8- or 4-line output, 8421 or 2421. Complete decades (counter and display) or separate decoder/display units are available as standard products. Most standard models are presently in stock, ready for immediate shipment.



Custom displays cost less than you think

Special decades and display modules, designed to meet the requirements of a specific system, can be produced at surprisingly low cost . . . for fast delivery. Try us.

IC Counter Modules

Individual, IC counters (without display) are also available. Line includes 25mHz decade counters, 25mHz decade dividers, and 5mHz bi-directional counters.

Send for complete data on this new numerical display series.

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CIRCLE NO. 46 ON INQUIRY CARD

Reminder . . .

Don't miss the next issue of Computer Design . .

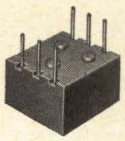
A revolutionary new number system will be introduced in the May issue . . .

Don't miss it!!!

PENNSYLVANIA'S DEPARTMENT OF PUBLIC INSTRUCTION IS PLANNING AN "EDUCATIONAL MANAGEMENT INFORMATION SYSTEM" that will eventually put 500 school districts and 14 colleges into direct communication with a computer located in Harrisburg. The system, key to which is a National Cash Register 315 computer, will in the first phase handle teacher certification records, professional personnel records, and appropriation accounting. Input initially will be by cards punched from information generated in the various district offices and colleges, and sent to Harrisburg. However, a completely "on-line" system via direct wire linkage is visualized for the future.

Did you know Sprague makes...?

HIGH SPEED, FLAT T.C. MEMORY TRANSFORMERS



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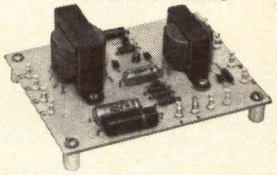

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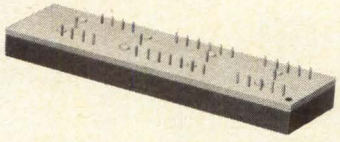

Single or multiple delay in lumped constant or distributed constant designs are tailored to meet customer requirements. Furnished in either cast epoxy or molded cases. Applications include digital circuits in computers, radar equipment, etc.

Circle No. 13 On Inquiry Card

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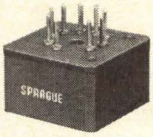

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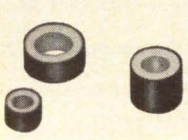

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INDUSTRY NEWS

PUBLICATION OF THE "ANNUAL REVIEW IN AUTOMATIC PROGRAMMING," WHICH LAST APPEARED IN 1964 UNDER THE EDITORSHIP OF THE LATE RICHARD GOODMAN, IS BEING RESUMED UNDER THE DIRECTION OF AN INTERNATIONAL BOARD OF EDITORS, including Professor Louis Bolliet of the University of Grenoble (Boite Postale 7, Saint-Martin-D'Heres, Isere, France), Professor Robert W. Floyd of the Carnegie Institute of Technology (Schenley Park, Pittsburgh, Pennsylvania 15213), Mr. Mark Halpern of Lockheed Missiles and Space Company (3251 Hanover Street, Palo Alto, California 94304), Mr. Christopher J. Shaw of System Development Corporation (2500 Colorado Avenue, Santa Monica, California 90406), and Professor Andrei P. Yershov (Computation Center, Novosibirsk 90, U.S.S.R.) The editors plan to publish substantial, authoritative, and well-written papers, in English, reporting on advances or describing the state-of-the-art in automatic programming, which is defined as the use of the computer itself as a tool in developing and applying computer programs. The series, to be published by Pergamon Press, will resume annual publication in late 1967 or early 1968. To meet this schedule, noteworthy papers from 5,000 to 25,000 words in length are urgently needed. Contributions, inquiries regarding contributions, or suggestions for contributions may be directed to the editors.

Now...

add light pen capability to your display for less than $1,000

Sanders new solid state PHOTOPEN® Model EO-PT system enables you to perform all symbol sensing functions in high data rate CRT displays using a wide variety of character generation techniques with push button ease.

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Fast response . . . output pulse is practically coincident with the leading edge of the CRT light pulse. Typical time delay is less than 1 microsecond — matches fastest CRT writing speed.

Versatility . . . can be used with a variety of character generation techniques, including shaped beam, monoscope, stroke and dot matrix types.

High sensitivity . . . adjustable to trigger on CRT symbols too dim for human eye detection, yet accommodates intensities above the comfortable viewing level. Spectral response spans the range from 4000 to 11,000 Angstroms.

Foolproof . . . special circuitry eliminates false or multiple triggering from long persistence phosphors, ambient light and CRT face and implosion shield reflections.

Pinpoint accuracy . . . an illuminated finder-circle "zeros in" the exact CRT area being sampled.

No special power supplies . . . power requirement is 117 volts, available at any standard ac outlet.

For less than $1000, you can get greater flexibility and performance from your data display equipment — with Sanders new PHOTOPEN system. For further information or a demonstration, contact Sanders Associates, Inc., Microwave Division, Nashua, New Hampshire 03060. Phone: (603) 883-3321. Ext. 7291. TWX: 228-1887, SA Microwave.

*T.M., Sanders Associates, Inc.

SANDERS ASSOCIATES, INC.
MICROWAVE DIVISION
Creating New Directions in Electronics

CIRCLE NO. 47 ON INQUIRY CARD

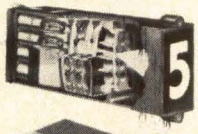
IN THE BUSINESS PUBLICATIONS INDUSTRY, 49.2% OF THE PUBLISHING COMPANIES ARE NOW USING COMPUTERS AND AN ADDITIONAL 45.5% WILL FOLLOW SUIT WITHIN THE NEXT 18 MONTHS, according to details of an American Business Press, Inc. survey just released. The survey was conducted for ABP by Computing Technology Incorporated of Tuxedo, N. Y. The computers are now or will be employed for circulation fulfillment, file maintenance, reader inquiry service, research analysis, and label printing, and secondarily for personnel records, bookkeeping, financial reporting, and payroll, to mention a few. (So if you happen to miss an issue of COMPUTER DESIGN, it may be your fault.)

Reader's Choice

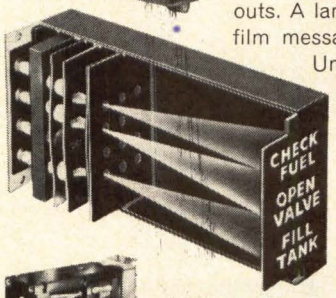
IEE bright, legible, wide-angle readouts:

Any characters desired
Any colors or combinations
Any input, BCD or decimal
Any input signal level
Any mounting, vertical or horizontal

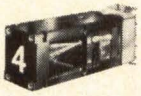
Many sizes
Many configurations
Many lamp lives (to 100,000 hours)
Many brightness choices
Many options and accessories



Standard Readouts: Rear projection principle, like all IEE readouts. A lamp in the rear of the unit illuminates one of the 12 film messages, and projects it to the front viewing screen. Unbeatable readability and versatility.



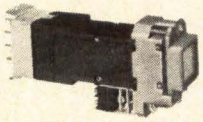
Large Screen Readouts: For reading distances up to 100 feet. Maximum character size 3¾".



Miniature Readouts: Only 1" wide x 1-5/16" high, yet can be read at 30 feet because of clarity of one-plane projection. Character size: ⅝".

Micro-Miniature Readouts: Only ½" wide x ¾" high, but 20 foot viewing distance and maximum 175° viewing angle because of front-plane display. Character size: ⅜".

Hi-Brite Readouts: Special lens system increases character brightness 50%. Particularly good when high ambient light conditions exist.



Cue-Switch Readouts: Rear projection readout with push-button viewing screen. Combination switch and display device.

Bina-View Readout: Accepts binary or teletype code, decodes, and displays the proper character.

Status Indicator Readout: Displays up to 12 different messages, individually or in combination. Viewing screen only 3 sq. in.

Indicator Assemblies: Available with up to 11 rear projection readouts, for indicating seconds, minutes, hours, days, etc.

Driver/Decoder Module: Designed to work with IEE Readouts. Accepts a variety of binary codes for decimal conversion.

The new IEE Display Devices catalog gives complete information and specifications on these products, and their accessories. Ask for it.

"I-double-E", the world's largest manufacturer of rear projection readouts.
Industrial Electronic Engineers, Inc. 7720 Lemona Avenue, Van Nuys, California

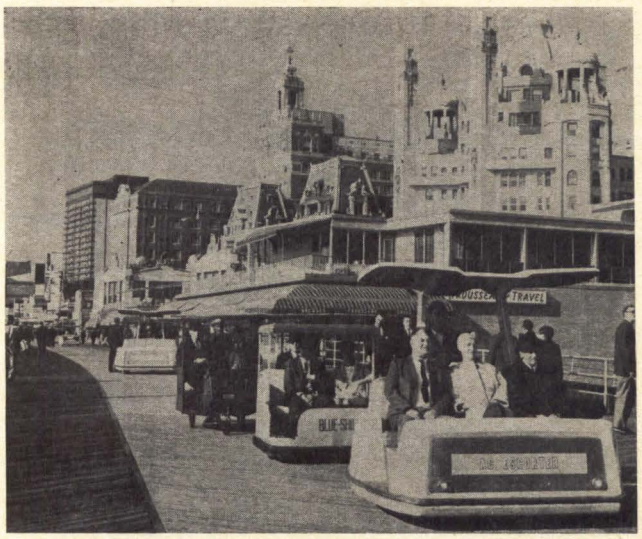
CIRCLE NO. 48 ON INQUIRY CARD

Aerial view of Atlantic City showing its famed Boardwalk and beach. At the left is Convention Hall, the nation's largest complete convention facility.

1967 SJCC

Convention Hall, Atlantic City, N.J.

April 18, 19, 20



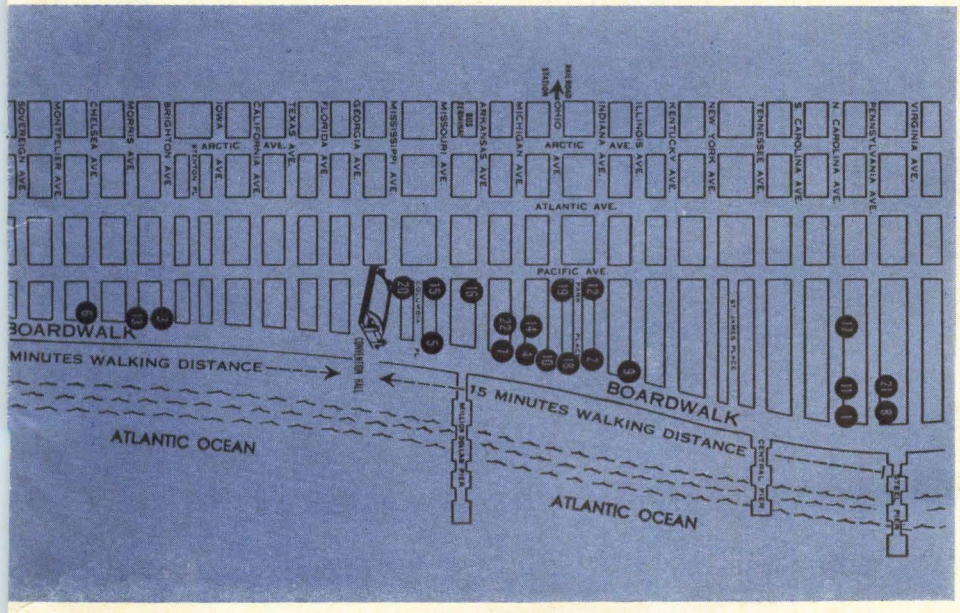
Atlantic City's famed five-mile long Boardwalk is an all-year haven for sightseers and shoppers on foot or in the legendary rolling chairs. Here are the three models — the 80-year-old "push" type, the 15-year-old motorized version, and the new "AC Escorter."

The 1967 Spring Joint Computer Conference is being held in Atlantic City's Convention Hall. The Conference Headquarters Hotel is the Chalfonte-Haddon Hall. The opening session, science theatres, technical sessions, and exhibits will be held in Convention Hall. The banquet and reception will be held in the Chalfonte-Haddon Hall.

Round-trip shuttle service will be provided free of charge by the Conference between Chalfonte-Haddon Hall and Convention Hall. Ample public parking is available in an underground garage at Convention Hall. A parking lot and garage is adjacent to Chalfonte-Haddon Hall.

Atlantic City's weather in April is changeable — it may be chilly or balmy. Come prepared with a warm coat or sweater and a comfortable pair of shoes for strolling the boardwalk at night. A coat checkroom is located in the Main Lobby of Convention Hall to the right of the entrance.

Advance registration will take place on Monday afternoon, April 17, at the Chalfonte-Haddon Hall. A no-host Pre-Conference Cocktail Party will be held in the Pennsylvania Room of the Chalfonte-Haddon Hall beginning 5:30 p.m. on Monday evening.



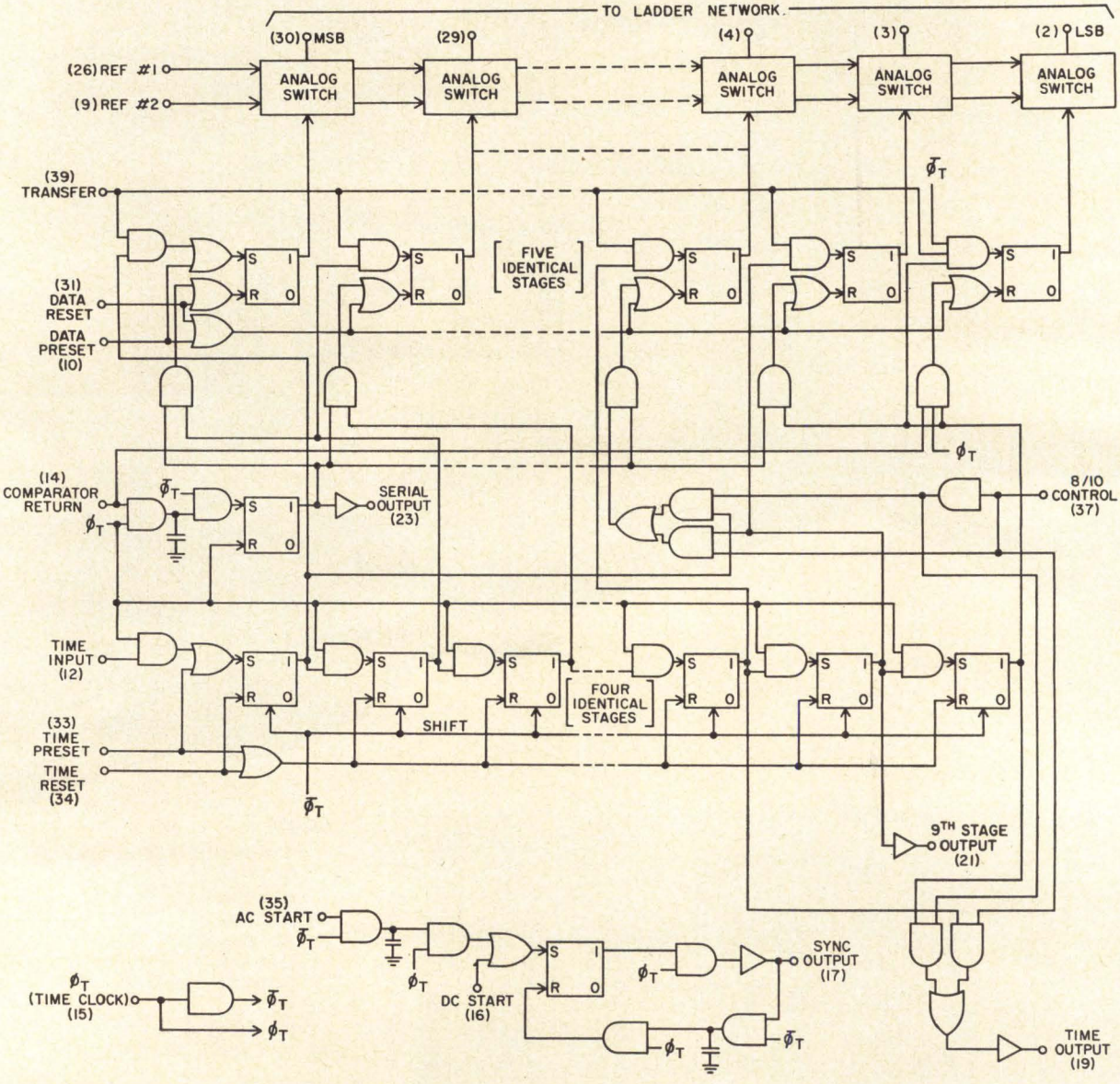
HOTELS

1. CHALFONTE-HADDON HALL
2. CLARIDGE
3. DEAUVILLE
4. DENNIS
5. HOLIDAY
6. LaCONCHA
7. SHELBURNE-EMPRESS
8. SEASIDE
9. TRAYMORE
10. MARLBOROUGH-BLENHEIM

MOTELS

11. CORONET
12. CRILLON
13. DEAUVILLE
14. DENNIS
15. FOUR SEASONS
16. HOWARD JOHNSON'S
17. LaFAYETTE
18. MARLBOROUGH-BLENHEIM
19. MT. ROYAL
20. PAGEANT
21. SEASIDE
22. SHELBURNE-EMPRESS

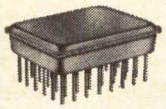
this is LSI...



Another MTOS First... This Monolithic A/D-D/A Converter incorporates General Instrument's **exclusive** MTOS (Metal-Thick-Oxide-Silicon) process which provides Large Scale Integration without the need for high-cost discretionary wiring.

the first available monolithic analog-to-digital digital-to-analog converter

And only General Instrument makes and delivers these advanced LSI devices...today!



Actual Size

MEM 5014 A/D-D/A Converter..... $268.00 each*

General Instrument's MEM 5014 is a Monolithic MTOS Integrated Circuit containing 350 active components on a chip 62x104 mils. It performs all the logic and analog switching functions for 10-bit successive approximation analog-to-digital conversion. In addition, it operates in two other major modes—as a 10-bit digital-to-analog converter or a 10-channel analog multiplexer.

As an analog-to-digital converter, the MEM 5014 is used in conjunction with an external precision ladder network and voltage comparator. This mode provides both serial and parallel binary outputs. The MEM 5014 is packaged in a 40 lead hermetically sealed in-line package which can be soldered to a printed circuit board or used with a 40 pin socket. Write for complete data and application notes.

**in quantities of 100*

GENERAL INSTRUMENT

GENERAL INSTRUMENT CORPORATION • 600 WEST JOHN STREET, HICKSVILLE, L. I., NEW YORK

CIRCLE NO. 49 ON INQUIRY CARD

CONFERENCE AT A GLANCE

Monday, April 17

12 NOON — INFORMATION CENTER OPENS (CHALFONTE-HADDON HALL HOTEL)
4:00 PM — ADVANCE REGISTRATION OPENS (CHALFONTE-HADDON HALL HOTEL)
11:00 PM — ADVANCE REGISTRATION AND INFORMATION CENTER CLOSES

Tuesday, April 18

8:30 AM — REGISTRATION OPENS
9:30 AM — KEYNOTE SESSION
11:00 AM — EXHIBITS OPEN
1:00 PM — SESSIONS 1, 2, 3, 4, and 5
1:30 PM — SCIENCE THEATER OPENS
3:30 PM — SESSIONS 6, 7, 8, 9, and 10
5:00 PM — REGISTRATION CLOSES
5:30 PM — SCIENCE THEATER CLOSES
6:00 PM — CONFERENCE RECEPTION (CHALFONTE-HADDON HALL HOTEL)
6:00 PM — EXHIBITS CLOSE
8:45 PM — SPONSOR SOCIETIES' TECH. SESSIONS

Wednesday, April 19

8:30 AM — REGISTRATION OPENS
9:00 AM — SESSIONS 11, 12, 13, 14, and 15
9:00 AM — SCIENCE THEATER OPENS
10:00 AM — EXHIBITS OPEN
1:15 PM — SESSIONS 16, 17, 18, 19, and 20
3:30 PM — SESSIONS 21, 22, 23, and 24
5:00 PM — REGISTRATION CLOSES
5:30 PM — SCIENCE THEATER CLOSES
6:00 PM — EXHIBITS CLOSE
6:30 PM — CONFERENCE BANQUET (CHALFONTE-HADDON HALL HOTEL)

Thursday, April 20

8:30 AM — REGISTRATION OPENS
9:00 AM — SESSIONS 25, 26, 27, 28, and 29
9:00 AM — SCIENCE THEATER OPENS
9:30 AM — SPECIAL SESSION
10:00 AM — EXHIBITS OPEN
12 NOON — SCIENCE THEATER CLOSES
1:30 PM — SESSIONS 30, 31, 32, 33, and 34
5:00 PM — EXHIBITS CLOSE

Friday, April 21

9:00 AM to 5:00 PM .....
SPONSOR SOCIETIES' TECHNICAL SESSIONS

TECHNICAL PROGRAM SUMMARY

TUESDAY, APRIL 18

KEYNOTE SESSION .... 9:30-11:30 AM, BALLROOM

NATIONAL DATA BANKS AND PRIVACY

The keynote speaker, Representative Cornelius E. Gallagher, and other specialists will give appraisals and possible solutions concerning the problem of safeguarding individual privacy in a computerized society.

SESSION 1 ..... 1:00-3:00 PM, ROOM H-J

DYNAMIC ALLOCATION OF COMPUTING RESOURCES

Resource allocation, the heart of programming, has become an identified topic of importance only in the context of large computing utilities used for concurrent execution of many independently-initiated computations. With logical constraints imposed by the definition of a complex computational task, there normally is a large area of choice, both in the sequencing of sub-tasks and the assignment of alternate computer sub-units. The choice is among alternate storage areas, registers, processing units, channels; and in allocation of resources to sub-tasks. Thus, the programmer always solves a resource allocation problem. Papers on dynamic resource allocation are really papers about widely applicable programming policies, capable of embodiment in scheduling and allocating programs. In this session, three papers will be synopsized by their authors. Each will be followed by critical commentary on the part of a panel.

SESSION 2 ..... 1:30-3:00 PM, BALLROOM

MANAGING THE DEVELOPMENT OF COMPUTER PROGRAMS — A User's Viewpoint

This session concerns methods and procedures that can be used to control the development of computer programs. The session's theme is based on the proposition that computer programs, like hardware, are the end items of an orderly, describable process than can be effectively managed. The practices presented cover such items as specifications, configuration management, and testing of computer programs. They were developed for and are being used by several organizations that are heavy users of computer-based systems.

SESSION 3 ..... 1:00-3:00 PM, ROOM 20

COMPUTER LOGIC AND ORGANIZATION

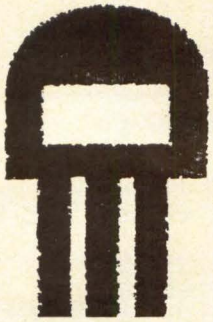
With the demand for larger data processing systems, attention increasingly has been focused on improving total system performance. However, most of the "multiple" techniques such as multiprocessing and multiprocessors, which theoretically should accomplish this goal, inherently seem to increase control functions. This actually reduces potential system performance. Improvements, therefore, must tend to embrace both hardware and software techniques and the interplay between the two. This session explores specific organizations offering these improvements.

SESSION 4 ..... 1:00-3:00 PM, ROOM 21

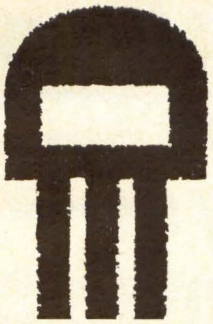
VISUAL OUTPUT RECORDING

The objective of this session is to introduce concepts for improved visual recording in a time-sharing complex. A panel discussion by the authors concerning the future of computer visual output recording will be conducted.

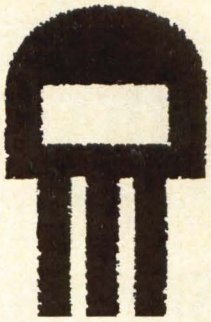
9 good reasons why Philco Epoxy Transistors (PET) are your best buy.



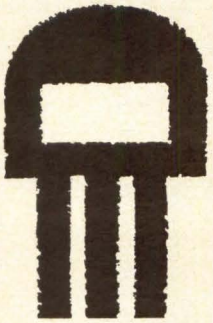
1. PET TO-18 is rated from 360 to 675 mW at 25°C (chip dependent).



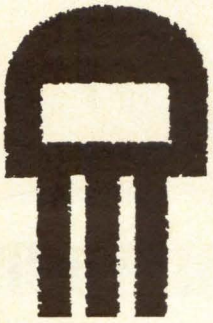
2. PET TO-5 is rated from 550 mW to 1.2 W at 25°C (chip dependent).



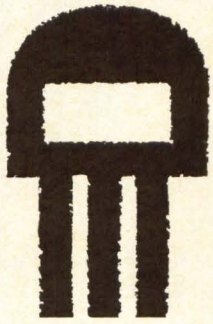
3. PET packages have reliability factors equal to or exceeding that of *metal* cans.



4. PET's are immediately available in large volume production quantities.

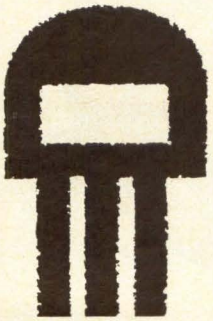


5. PET's have a special deep-well interlock construction that insures hermeticity and reliability.

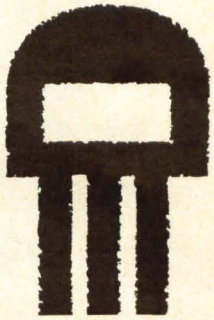


6. PET packages are permanently and legibly marked—lettered black on white.

7. PET's are packaged in our low-cost Taiwan production facility—to keep *your* cost low.



8. PET amplifiers operate on currents ranging from 10 μA to 1 A; PET switches to speeds 8 ns turn on and 11 ns turn off.



9. PET's cover frequencies from 40 MHz to 1400 MHz.

Call or write: **Philco-Ford Corporation Microelectronics Division Sales Offices:** 2920 San Ysidro Way, Santa Clara, California (408-245-2966) / 999 North Sepulveda, El Segundo, California (213-772-6226) / Northwest Industrial Park, Second Avenue, Burlington, Mass. (617-272-1600) / Benson Manor, Suite 114B, Washington Lane, Jenkintown, Pa. (215-885-0430) / 1215 Drew St., Clearwater, Florida (813-446-0124) / 815 Connecticut Avenue, N.W., Washington, D.C. (202-298-7810) / Suite 208, 700-108th St., N.E., Bellevue, Washington (206-454-5061) / New York, N.Y. (212-244-1373).

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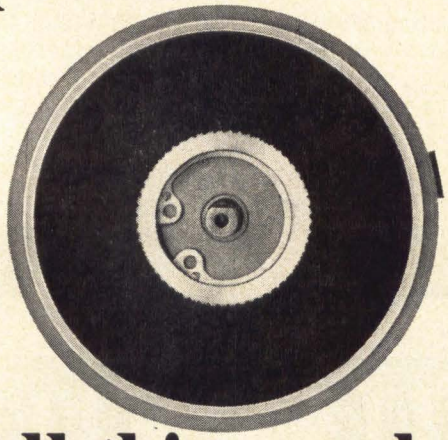
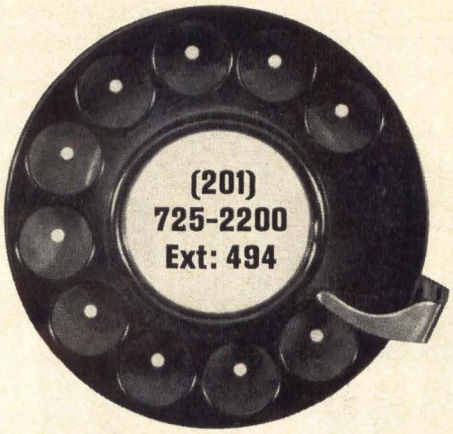
Microelectronics Division
Santa Clara, California • 95051

CIRCLE NO. 50 ON INQUIRY CARD

If you're not happy with your present delivery of special motors...



Call this number collect.



And if this gives you the idea that we may be among the last of the Big Spenders, good! We think we've earned the reputation when it comes to special motors. We've just spent 1.5 million dollars on new facilities to speed up the production and delivery of instrument servo motors, special induction, D-C, and hysteresis synchronous motors. We've gambled that these facilities will produce more of these motors, faster, than any of our competition . . . and *deliver* them faster too. Here's one example of how fast it is now: our delivery of instrument servo motors is eight weeks from receipt of order!

You know our reputation for product quality and company stability. On top of that now, put fast delivery of production quantities. To find out how fast, just call John Kachmar or Jim Ryan, Customer Service Department, THE SINGER COMPANY, Diehl Division (201) 725-2200.

SINGER
INDUSTRIAL CONTROLS

D-121

CIRCLE NO. 51 ON INQUIRY CARD

SESSION 5 . . . . . 1:00-3:00 PM, ROOM 13

APPLICATIONS OF ANALOG AND HYBRID COMPUTERS

This session should be of special interest to computer personnel concerned with analog and hybrid computation. Two situations will be discussed in detail — one that makes optimum use of hybrid simulation and one that does not. The session also will point up two unique and especially interesting applications of these computer systems. One is the production of animated films using a hybrid system, and the other is a special hybrid system used for simulation studies of learning machines.

SESSION 6 . . . . . 3:30-5:30 PM, BALLROOM

DATA MANAGEMENT

One of the key problems facing designers of management information systems, command and control systems, and intelligence data handling systems is the lack of tools to accept, modify, update, maintain and make available, large volumes of data, of varied and complex logical structures, found in the real world. In this session, design solutions to the problem of generalized data management will be reported, and the role of generalized data management in third generation information processing systems will be discussed by a panel of authors and software designers.

SESSION 7 . . . . . 3:30-5:30 PM, ROOM 11

HANDLING THE GROWTH BY DEFINITION OF MECHANICAL LANGUAGES — A Special Tutorial Session

In this session, Professor Saul Gorn attacks intercommunication problems by considering a strongly structured category of language functions in which alphabets may change by "explicit definitions."

SESSION 8 . . . . . 3:30-5:30 PM, ROOM H-J

ILLIAC IV — An Orientation Session

This special session was arranged to acquaint those planning to attend the Wednesday panel discussion on "The Best Approach to Large Computing Capability" with the basic concepts of this advanced system. However, since it will be the first description of ILLIAC IV to be presented at a general computing conference, it may be of great interest to the general audience as well.

SESSION 9 . . . . . 3:30-5:30 PM, ROOM 21

I/O DEVICES

This session is devoted to papers describing recently-developed peripheral devices which feature novel design approaches. Emphasis is on hardware, stressing those details of the design which are unique.

SESSION 10 . . . . . 3:30-5:30 PM, ROOM 13

BIOMEDICAL COMPUTER APPLICATIONS

While medicine was initially slow in applying computing power to its research and practice, inroads into simulation and statistical correlations and analysis are now being made. This session presents three examples of computational solutions to problems in medical research. A fourth report on learning networks includes impressive experimental results.

WEDNESDAY, APRIL 19

SESSION 11 ..... 9:00-12:00 NOON, BALLROOM

SECURITY AND PRIVACY IN COMPUTER SYSTEMS

This session provides a coordinated discussion of the security/privacy problem. It is not concerned with the existence or nature of the problem in a moral, ethical, legal, political, or social sense. The focus is rather on the technical aspects of guaranteeing protection of information.

SESSION 12 ..... 9:00-12:00 NOON, ROOM 20

COMPUTING ALGORITHMS

This session will discuss the effects of hardware design on implementation of numerical routines and mappings from a set of internal to a set of external number representations. Some surprising properties of these mappings are established and their implications are discussed.

SESSION 13 ..... 9:00-12:00 NOON, ROOM F-G

MACROMODULAR COMPUTER SYSTEMS

The properties of macromodular systems are of growing importance in the search for more effective information processing systems. Papers in this session will cover a functional description and the logical design of macro-modules and system examples.

SESSION 14 ..... 9:00-12:00 NOON, ROOM H-J

SOME ASPECTS OF COMPUTER-ASSISTED INSTRUCTION

This session deals with the development of a suitable system for computer-assisted instruction. The topics include aspects of hardware economics, appropriate software for course presentation, and hardware selection as influenced by educational/student consideration.

SESSION 15 ..... 9:00-12:00 NOON, ROOM 13

ANALOG/HYBRID TECHNIQUES FOR SOLVING PARTIAL DIFFERENTIAL EQUATIONS

Implementing analog or hybrid computer program to solve a particular P.D.E. problem requires the analyst to choose from among many methods and algorithms, without a sufficient arsenal of theories to compare meaningfully their relative value. This arsenal of theories still is in the development stage. Furthermore, even many completed theoretical works have received too little publicity and still are largely unknown to the computer users' community. The panelists of this session have been directly engaged in this area. They will discuss some of the recent advances that have been made.

SESSION 16 ..... 1:15-3:15 PM, ROOM H-J

INFORMATION PROCESSING IN THE BUSINESS ENVIRONMENT

This session considers the collection, classification, organization, and selective dissemination of information in the business environment. The source and character of errors in on-line data collection systems is the concern of one paper. Another defines the attributes of an information retrieval facility in terms of the user's requirements. The third paper describes a utility information system designed primarily to service customers, but which also provides essential facts for key personnel.

SESSION 17 ..... 1:15-3:15 PM, BALLROOM

TECHNIQUES IN PROGRAMMING LANGUAGES — Part 1

This session concerns itself with three methods of construction of programs; a technique of using a questionnaire to define a program in an application area and constructing the program; a system for generating a compiler whose source and object languages may be rigorously defined by the user; and a system which supplies a general-purpose compiler whose input languages may be defined by the user. The session will conclude with a panel discussion of the papers.

SESSION 18 ..... 1:15-3:15 PM, ROOM 20

THE BEST APPROACH TO LARGE COMPUTING CAPABILITY — A Debate

Large computing capabilities can be achieved either through faster single processors or through configuration of conventional or unconventional computer hardware sharing the load. But, which approach produces the greatest performance per unit cost? One of these configurations may be better than its competitors for certain special problems. The debate will center around which problems can be best handled in one or the other configuration, and whether one of these configurations is better for general-purpose environments.

SESSION 19 ..... 1:15-3:15 PM, ROOM 13

THE EXPANDING ROLES OF ANALOG AND HYBRID COMPUTERS IN EDUCATION

A panel consisting of a select group of educators from the fields of chemistry, mathematics, physics, chemical engineering, mechanical engineering, and electrical engineering will discuss their own experiences, make recommendations to the industry, and answer questions concerning the place of analog/hybrid computer techniques in today's school curricula.

SESSION 20 ..... 1:15-4:15 PM, ROOM 21

LOGIC-IN-MEMORY

The papers in this session will describe magnetic, semiconductor, and superconductor techniques for special-purpose memories which have logic capability within the memory cells.

SESSION 21 ..... 3:30-5:30 PM, ROOM 20

SCIENTIFIC PROGRAMMING APPLICATIONS

From among the large number of papers submitted in this category, three have been selected that have general interst, either because of the potential importance of the application itself, or by virtue of the novel techniques employed in making the computer application successful.

SESSION 22 ..... 3:30-5:30 PM, BALLROOM

TECHNIQUES IN PROGRAMMING LANGUAGES — Part 2

This session includes a FORTRAN language extension to include the use of graphic display devices, and an ALGOL extension for on-line programming. These papers are followed by descriptions of a special language for data reduction applications, a command language for on-line problem solving, and an experimental time-sharing system.

SESSION 23 . . . . . 3:30-5:30 PM, ROOM H-J

WILL INTEGRATED CIRCUITS REMOVE THE MILITARY/COMMERCIAL COMPUTER SPLIT?

It seems that the traditional cost-reliability tradeoff is undergoing drastic transformation, and that previously unheard-of combinations of high reliability and low cost shortly will become available. Will this produce a convergence of commercial and military computer technology? Are we approaching an era in which best commercial practice will intrinsically satisfy the critical military reliability requirement? The panel will address itself to various aspects of these questions.

SESSION 24 . . . . . 3:30-5:30 PM, ROOM F-G

PAPERS OF SPECIAL INTEREST

Not every paper of quality and interest that warrants presentation conforms to the planned theme of a conference session. Papers concerned with unique subject areas or unsupported by additional submissions of comparable quality would be by-passed were it not for a themeless session such as this one. The papers presented will be of interest to persons in several major fields of computing research and industry.

THURSDAY, APRIL 20

SESSION 25 . . . . . 9:00-11:00 AM, ROOM H-J

ADVANCES IN SOFTWARE DEVELOPMENT

For this session, "software" is defined as programming tools for the computer programmer and designer in building and maintaining programming systems. The first part of this session will reflect significant new software developments, and will cover a new report generator, a system designed to produce efficient code, and a system developed to help evaluate hardware and program interaction. The second part will call attention to the failure of software to keep in step with advances in computer hardware.

SESSION 26 . . . . . 9:00-11:00 AM, ROOM F-G

TECHNIQUES IN PROGRAMMING LANGUAGES — Part 3

This session represents a broad spectrum of techniques for the development and specification of programming languages and includes: (1) Machine Synthesis of Programs; (2) Applications of Languages; (3) On-Line Programming Systems; and (4) Syntax-Oriented Recognizers and Compilers. Three distinguished panelists will offer a critique after each group of papers is presented.

SESSION 27 . . . . . 9:00-11:00 AM, ROOM 20

SOME IDEAS FROM SWITCHING THEORY

This session discusses some relatively-new switching-theory ideas that may influence the computer field in the years ahead. Two papers will focus on logic modules, considering both the choice of the module itself and how to design computers with them. One paper takes the point of view of combinational logic; the other, the point of view of adaptive systems. The third paper investigates error detection by developing a technique for designing diagnosable sequential machines.

SESSION 28 . . . . . 9:00-11:00 AM, ROOM 21

NON-ROTATING MASS MEMORY

The first paper in this session describes the system experience which has been gained by using a mass core store for job-shop and real-time applications. The other two are concerned with engineering aspects of a mass core store and simulation of a system utilizing this memory.

SESSION 29 . . . . . 9:00-12:00 NOON, ROOM 13

FAILURE FINDING IN LOGICAL SYSTEMS

The current tendency toward larger, more sophisticated logical systems has produced a great deal of concern about the growing problem of failure finding. Failures are getting harder to find, and system downtime is becoming more critical. A broad spectrum of approaches to this problem is presented in this session, ranging from a highly-theoretical development of a structurally-oriented diagnostic procedure to a practical description of failure finding in a telephone central exchange.

SESSION 30 . . . . . 1:30-3:30 PM, BALLROOM

LEGAL PROTECTION OF COMPUTER SOFTWARE

The panel (including legal experts in this field from industry, government and private practice, as well as software management people) will consider the legal and economic impact of computer program patents on the data processing industry. The panel will deal with the following questions: (1) What are the policy considerations in filing patent applications on computer program inventions? (2) What protection will such patents afford? (3) What is the likelihood of obtaining such patents? (4) What alternatives are available for the protection of proprietary rights in software?

SESSION 31 . . . . . 1:30-3:30 PM, ROOM H-J

WHAT'S NEW IN PROGRAMMING?

The panel will discuss new developments in the field of universal versus specialized languages, new techniques, and new directions for the future.

SESSION 32 . . . . . 1:30-3:30 PM, ROOM F-G

SHOULD THERE BE STANDARDIZATION OF MACHINE INSTRUCTIONS?

Panelists will develop the question from differing viewpoints. They will explore the need for such standardization as well as its disadvantages.

SESSION 33 . . . . . 1:30-3:30 PM, ROOM 20

COMPUTERS FOR INDUSTRIAL PROCESS ANALYSIS AND CONTROL

This session will treat some of the current advances made by a user, s systems supplier, and a combined computer manufacturer and systems supplier.

SESSION 34 . . . . . 1:30-3:30 PM, ROOM 21

SIMULATION LANGUAGES — A Tutorial Session

The purpose of this session is to present the basic principles involved in both discrete and continuous systems application areas of simulation languages and to compare and/or contrast their objectives and techniques.

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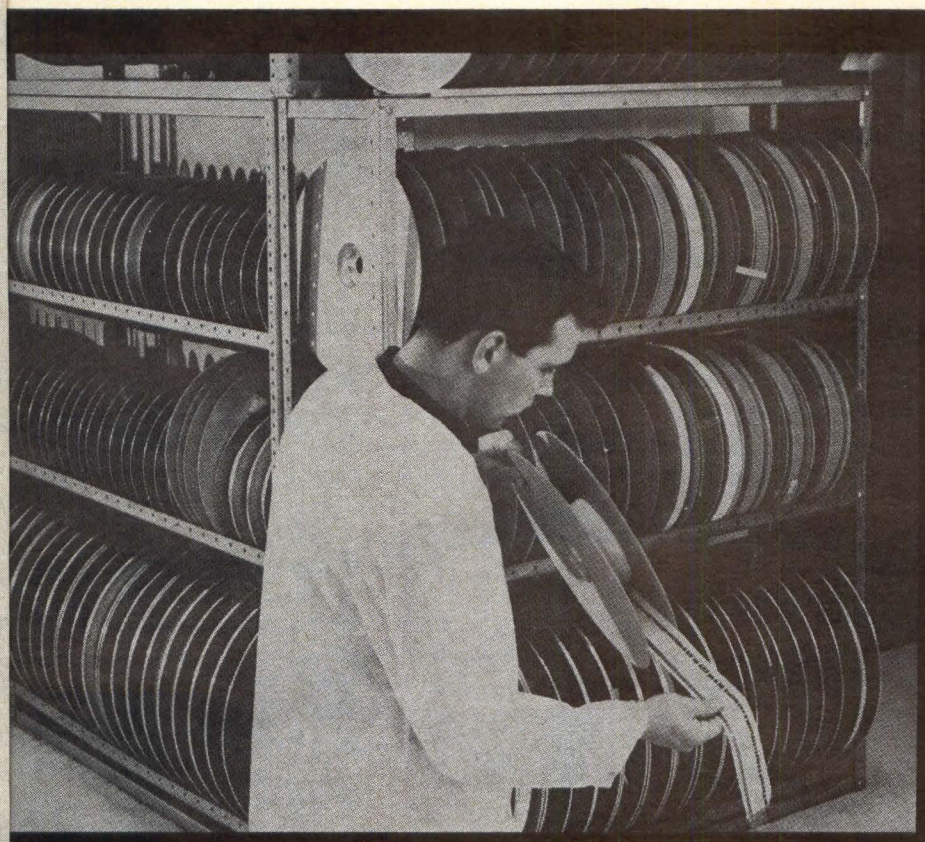

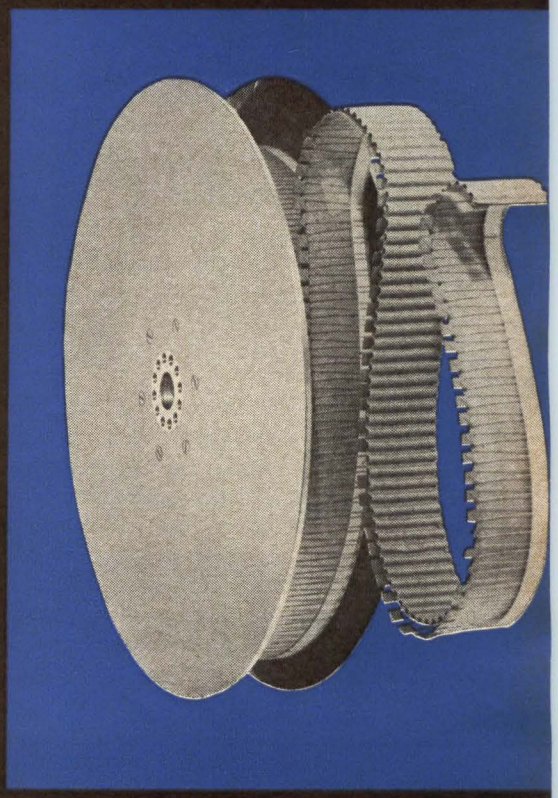

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A SMALL TIME-SHARED COMPUTER

In the midst of the battle between large time-shared computers and small stand-alone computers, the author presents a case for a small, slow, time-shared computer.

LARRY L. CONSTANTINE,
Senior Consultant,
Information Systems Institute,
Cambridge, Mass.

Two complementary trends are observable in the computing world. On the one hand is the move toward ever larger, faster, and more expensive computers for time-sharing, based on the belief that the amortized (per-user) costs will decrease as the potential number of users per machine rises. On the other hand is the effort to produce smaller, cheaper "personal" computers, which currently are more economical per user, in the belief that this position will continue for some time.

But what is cheaper than a cheap computer? Why not a time-shared cheap computer? The computer described here is such a machine. The class of machines to which the TMC (Time Multiplexed Computer) machine belongs is that of small, "ordinary" (perhaps even "obsolete") units using acoustic delay lines for memory. Acoustic delay lines, especially those based on magnetostrictive techniques, were long used as the primary storage medium for computers of modest capabilities. They work by storing information bits as acoustic (sound) waves serially in a solid medium such as nickel wire. Bits are entered at one end and are presented sequentially at the other after a delay proportional to the length of the line. The chief advantage of serial delay line storage is its low cost. In addition, delay lines are free from the mechanical limitations associated with other low-cost, low-speed media, such as magnetic drums and discs.

The principle disadvantage of delay lines is a function of the direct relationship between length, that is size in bits, and access time to a given bit or word. Inherent characteristics of magnetostrictive lines have stabilized the maximum usable bit-rate at about two million bits per second. A computer constructed around a small memory of 2000 bits will thus have a main cycle time of one millisecond. Traditional approaches to circumventing this problem and expanding the size of such memories use independent delay line systems as separate sections of memory, but as this method is carried further and further, part of the cost advantages disappear. Very long delay line memories (20,000 bits or more) are now available as stock items at essentially the same cost as much shorter lines, giving a storage cost of slightly more than 1 cent per bit. The low cost, however, is usually considered offset by the very long main cycle dictated by delays of this length. Since only one addressable instruction can be executed each cycle, a conventional computer constructed around long delay lines would execute few instructions per second.

However, there are certain unique characteristics of serial, circulating memory systems that can be exploited for special purposes. One of these is the fact that, in each full memory cycle, one gets "a look at" every word stored in the system. This allows the construction of associative memories without any penalty in speed. It also enables the implementation of rather novel hardware instructions and unusual programming approaches. Another characteristic, often ignored as unimportant, is that the separation of words in what might be called the address domain is duplicated in the time domain. That is, items of information located at different addresses are, of necessity, displaced in time. This leads directly to the possibility of time-sharing a serial delay line memory.

The TMC uses this latter feature to allow several users to time-share a single memory and central processor. The design is such that each user "sees" a medium-to-small-scale computer of modest capability which is autonomous and not subject to any effects related to the usage of the equipment by others. Its organization is distinct from current trends in time-sharing evolution. The user is not screened from the fundamental machine characteristics by a monitor or executive nor is it necessary to relinquish memory space or time to such a supervisor. Further, there is no restricted subset of instructions reserved for a Monitor or Executive or Scheduler. All capabilities of the computer are available directly to the user. It is a true time-shared computer, as opposed to a time-shared facility.

External Characteristics

The particular version of the TMC design described here (referred to as the TMC-1), was chosen primarily for the sake of concrete presentation. The size of the instruction set, length of the memory, and input-output structure reflect an orientation to a class of potential users whose requirements now fall below the lower end of the computer spectrum, in particular, for educational institutions in teaching computer courses and in laboratory use, and

for filling the needs of small businesses. However, the key design features, the automatic time-sharing of a serial memory medium, and, consequently, of a central processor, could form the basis for other variants, such as a computer designed around a very long, glass, delay line.

The TMC-1 is really five computers in one, that is, five users can operate simultaneously. The memory of the TMC-1 has a 16-bit word (two ASCII characters with parity) and a total storage of 4096 words. The instruction format is single address, allowing four bits for operation code. Table 1 shows the list of commands.

Each user must have his own complement of input-output devices, such as a medium-speed paper tape reader and punch capable of about 50 characters per second and/or a typewriter-like device for direct man-machine communication and hard-copy output. The range of devices that can be operated successfully with the TMC-1 is, in general, limited to devices with transfer rates of 200 characters per second or less.

TABLE 1

Instruction Set for the TMC-1

CODE	MEANING		
01	LA	y	(y) → (AR)
02	LE	y	(y) → (ER)
03	DA	y	(AR) → (y)
04	DE	y	(ER) → (y)
05	AD	y	(AR) + (y) → (AR)
06	SB	y	(AR) − (y) → (AR)
07	MP	y	(AR) × (y) → (AR, ER)
10	DR	y	(AR, ER)/(y) → (AR)
11	TR	y	y → (PC)
12	TD	y	(PC) → (y), y + 1 → (PC)
13	CM	y	(AR) : (ER), HI or EQ INDICATOR SET
14	SK	m	micro-programmed skip group to skip on compares, AR and ER sign bits, overflow, I-O indicators, etc.
15	OP	m	micro-programmed operate group to clear and complement AR, ER, shift, etc.
16	I-O	m	input-output group, transfers a character to or from ER and/or signals a device.
17	LG	m	micro-programmed, inter-register logic group (AND, OR, etc.).
00	AX		Auxiliary group which might include sort and lookup instructions.

Hardware Organization

The primary memory of the TMC-1 complex is a single bank of sixteen magnetostrictive acoustic delay lines, operated bit-parallel, word-serial, and locked in synchronism by a common clock. Using delay lines of 20,000-plus bits, which are now available off-the-shelf, the overall master cycle time of the TMC-1 complex would be approximately ten milliseconds.

It is difficult to define the processing speed of the computer. If the discussion is limited to addressable instructions, then the execution rate is an extremely modest 100 instructions per second. (The design allows, however, any number of sequential-operate-class instructions to be executed during a single main memory cycle, which yields a theoretical maximum of 400,000 executions per second.) While each user is getting 100 instructions executed per second, the complex is servicing five users, hence executing a total of 500 per second. If particular applications require less memory, the number of users can be expanded to ten, or even twenty, or the main cycle decreased. Except that each user must have his own I-O, almost no additional hardware is needed, and the cost per user becomes smaller.

Conceptually, the 20K memory of the complex is divided into five 4K blocks of contiguous words, one block being associated with each of the five users. Since the storage is word-serial, the spatial separation of user's blocks is duplicated by a time displacement. With each user assigned a contiguous block of words which are mutually exclusive of those assigned to all other users, the processing facility need service only that user which is active at any given time, that is, whose block is circulating through the read amplifiers of the delay lines. No other user's area will be accessible, since other areas will exist only as acoustic waves in the lines. This characteristic affords an automatic or inherent memory protection feature, and no separate device is needed to eliminate accidental user interaction. This organization does not require a separate processing facility for each user, but only one capable of functioning for a given block as if it were the sole property of that user.

The Central Processor

A processor which can function in this time-sharing manner must be capable of storing information pertinent to a section, sufficient to define the state of that section completely so that its operation may be resumed upon the next master cycling. In conventional time-sharing systems, this often means dumping the current contents of memory and selected active registers onto some auxiliary storage device. In the TMC-1, since each user has a unique, permanently assigned, section of memory, it is only necessary to save the state of the pro-

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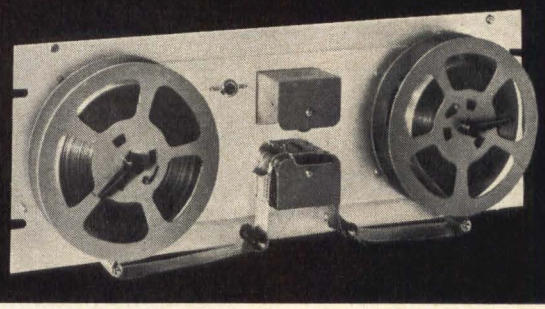

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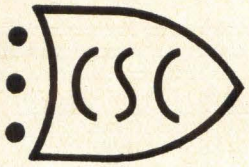
cessor itself. To store the relatively-small number of bits needed to define the state of the processor at the terminal boundary of a user's area, simple flip-flop registers or a small core storage could be used. It is not necessary, however, to employ such relatively expensive methods, since the auxiliary memory which is used to store the processor state at the boundary between user blocks, can be low-cost delay line storage. Many schemes are possible, subject only to the requirement that for an N-user complex, the processor state for a given user must become available at the initial boundary precisely N-1 block-times later.

The details of the requisite processor characteristics can best be understood by following through the processor cycle. We shall assume that the terminal boundary of some user's memory area has just been reached, the state of the processor has just been stored in auxiliary storage, and that the area of storage associated with user 3 has been entered. Immediately upon entering user 3's block, the address counter (AC) is reset to zero. The AC will be used to compare for coincidence with other address registers in order to fetch or store a given word and, therefore, will be incremented by one each time a word passes through the read section of the delay memory. In addition, the processor has been set to correspond to the state last recorded in the auxiliary storage by user 3. Let us assume that there is no instruction waiting for completion and that the processor state as restored indicates that the next instruction to be executed is at location 104 (that is, word number 104, counted from the start of this user's block). In other words, the program counter contains 104.

When word 104 is accessible (as indicated by the count in AC) it will be read into the instruction decoders. Let us say that the contents of 104 required fetching the contents of location 70 into the accumulator register (AR). Word 70 has already passed, so the terminal boundary for user 3 will be reached without the word having been fetched. At the boundary, the processor state (i.e., the computer is wating for word 70) will be saved, the processor will be restored from the state last recorded for the next user, user 4, and



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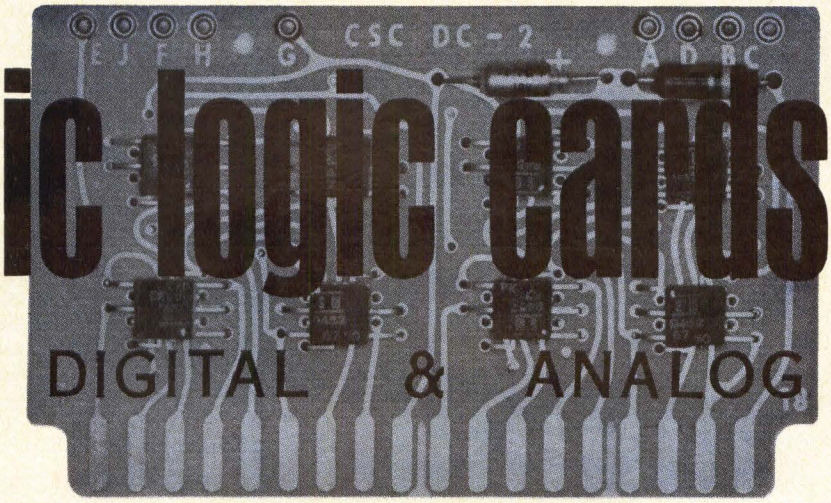

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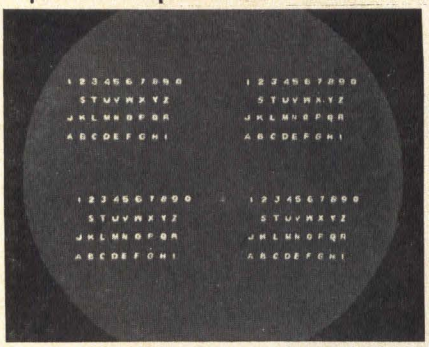
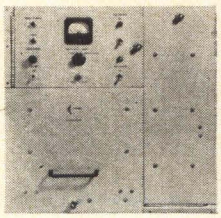


a computer. It is only one example of a computer display using the Electrostore, Model 221.



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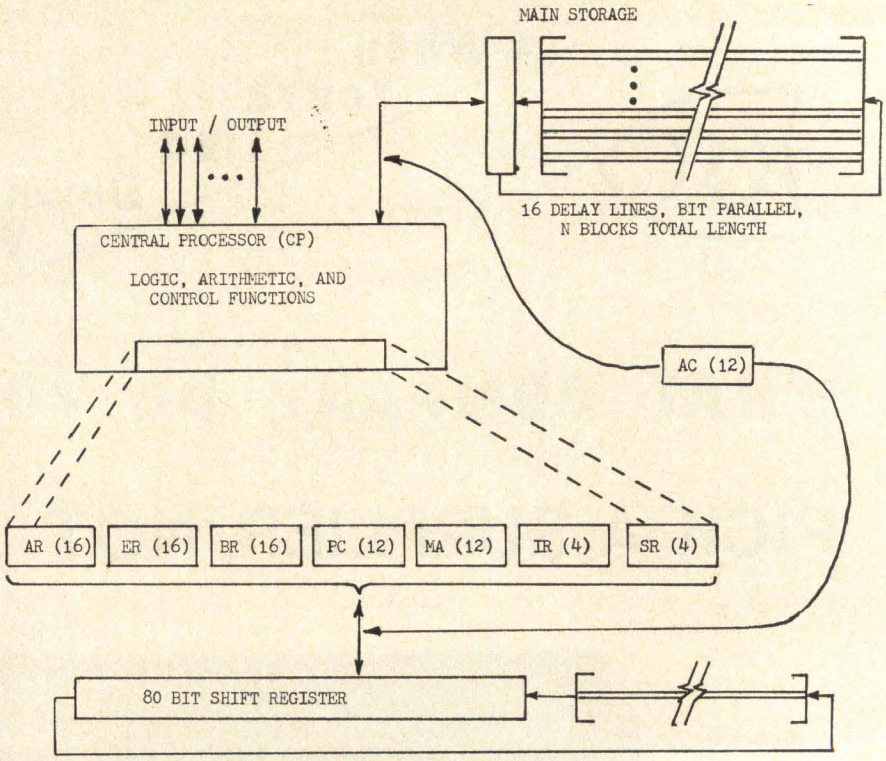


Central Processor Auxiliary Storage (CPAS)

Total Delay Length is N-1 Blocks for N Users

Key — Length in bits in parentheses			
		PC	Program Counter
		MA	Memory Address
AR	Arithmetic Register	IR	Instruction Register
ER	Extension Register	SR	State Register
BR	Memory Buffer Register	AC	Address Counter

Fig. 1. Organization of the TMC-1.

the AC reset to zero.

When the initial boundary of user 3 is reached again, the state as restored from the auxiliary memory will cause the computer to wait for location 70, load its contents into the AR, and then wait for location 105 (the next sequential instruction). If 105 contains a non-memory-referencing instruction, say a shift, this can be executed immediately. With sufficiently-fast decoding and arithmetic logic units, this can be completed by the time word 106 is read from memory, and the instruction in 106 could then be executed in the same cycle.

It is clear from the preceding discussion that the appearance of the TMC to the user, or more correctly, the user's program, is precisely that of a "typical" small delay line computer with a memory size equal to the user's assigned block length. The facts that memory reference instructions are completed in a single main cycle, rather than two as with static storage, and that any number of consecutive non-addressable (operate class) instructions can be executed in a single cycle could be employed in any delay line computer.

The foregoing discussion, while somewhat elementary, illustrates the principal characteristics of the TMC-1, which allows the hardware time-sharing of a very large, serial delay line memory system and the associated central processor among several users at very low cost. It can be seen from the organization diagram (Fig. 1) that the only difference between the main frame of the TMC-1 and a single-user machine with a 4K mem-

ory is the length of the delay lines and the provision of the auxiliary memory in the time-sharing version.

Applications

Currently there are several very small-scale digital computers on the market designed for use as instructional devices in classes in programming and computer applications. For this type of purpose, cost is usually the paramount consideration. Slow speed is not considered a great disadvantage and restricted instruction sets are even considered by some to be advantageous for teaching. The hope has been to bring the cost of such a device within the budget of small colleges and even high schools.

However, for effective classroom utilization, what is really needed are several small computers, enabling a significant fraction of the class or even different classes in different departments to be using a computer at the same time. The use of consoles, linked to a large time-shared facility, is a possibility but poses the problem that the student is separated from the computer by several "layers" of languages, monitors, executives, and supervisors. Whether or not this is wholly desirable is still in debate. Further, there are very few large facilities of the sort that could offer a service to small colleges and high schools and none have chosen to as yet. The TMC offers one possible solution for these educational users. For very little more than the cost of a simple, single user computer, an institution could have a computer that could serve five or more students simultaneously. If the memory requirements are relaxed, the computer is much cheaper. If a thousand words for each of five users is sufficient, not only is less memory required, but the slower effective word rate enables the use of slower (hence, cheaper) logic in the central processor.

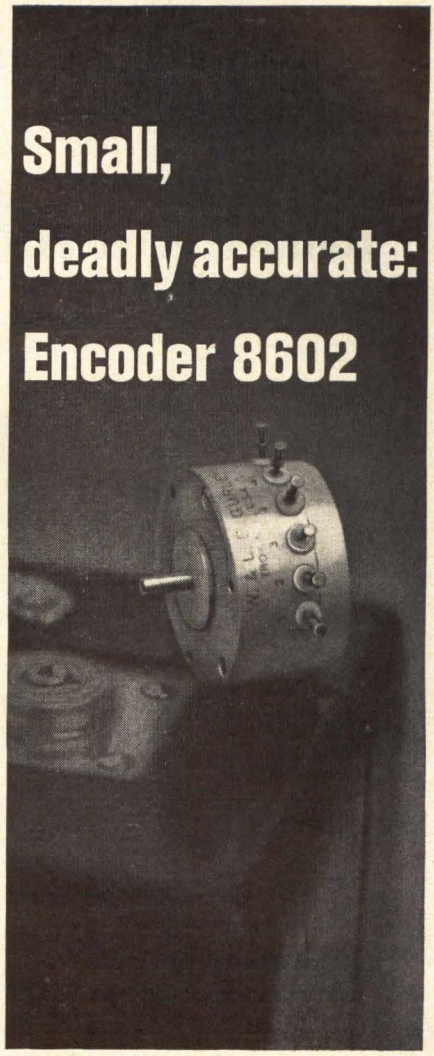
The small and very small business user could also make good use of this class of equipment, rather than using much faster equipment in a batch processing arrangement. This small, relatively-slow computer could handle transactions as they occur with only occasional waits when two or more arrive simultaneously. (It is not true that real-time operation requires very high-speed equipment; this depends on the arrival rate of information and information requests and the complexity of processing associated with each transaction. In the small business, both the arrival rate and complexity are low.) Further, the TMC is not inapplicable to batch processing problems for, if the equipment is inexpensive enough, the fact that it may take a full shift to process a payroll is tolerable.

The TMC also has multiple use capability. One section could be permanently relegated to inventory control, another to payroll processing, a third to billing, invoicing, and other automated typing applications, and a fourth used for program debugging and maintenance. The last one might be left free for miscellaneous applications. Further, businesses which cannot now afford a computer could form alliances, sharing a single TMC with each business getting the number of consoles it can use and is willing to pay for.

Whereas educational users are probably best served by a more or less standard instruction set, business users could benefit from special instructions. In particular, serial or tabular operations can often be implemented with rather simple hardware at great savings in execution time. For example, the table look-up and sort instructions mentioned in Table 1 would be highly desirable and useful in small business applications. To facilitate achieving maximum input-output rates, it would be desirable to have I-O instructions transfer entire blocks as well as operate on a character-at-a-time basis.

Conclusions

Based on the simple principle that, in a serial storage medium, information separated in the address domain is also separated in the time domain, a straightforward technique for time-sharing such a memory has been described. The Time Multiplexed Computer embodies this technique in a rudimentary computer of modest capability. While not so limited, hardware of this design seems to have the greatest potential for small, budget-limited, educational and business users. With careful choice of applications and appropriate special instruction sets, the TMC could fill both needs at low cost. END



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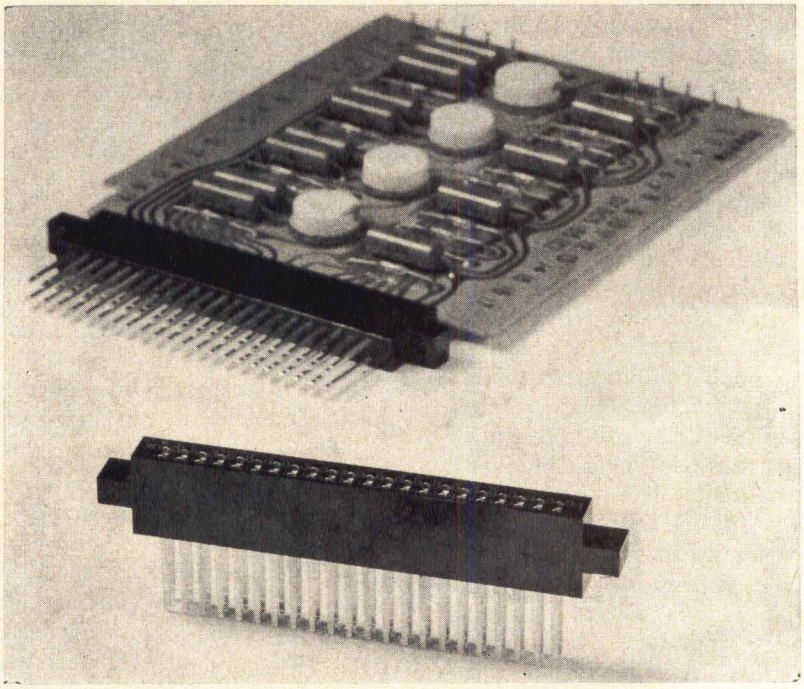

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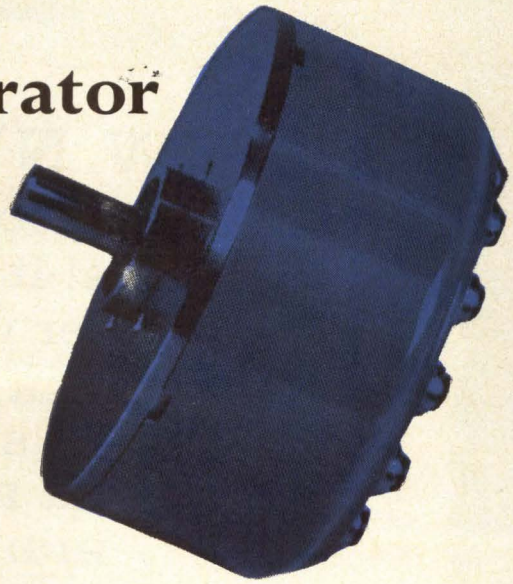

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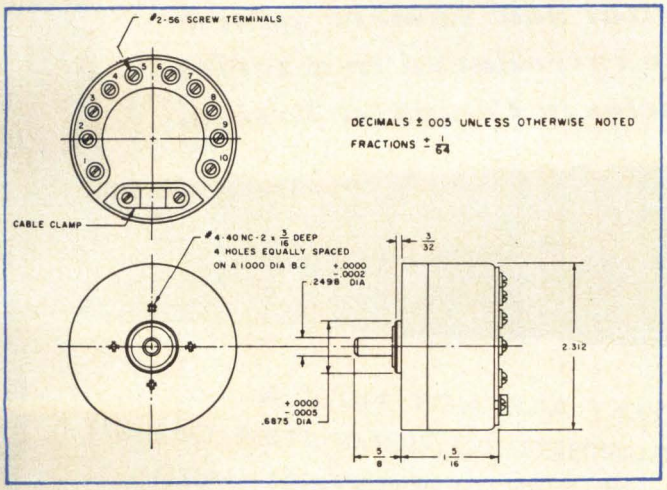

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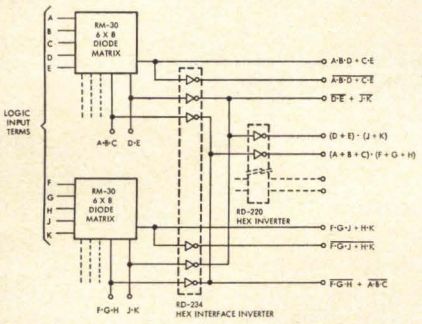

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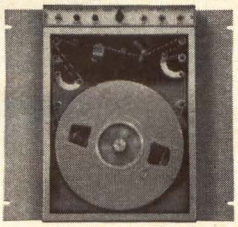

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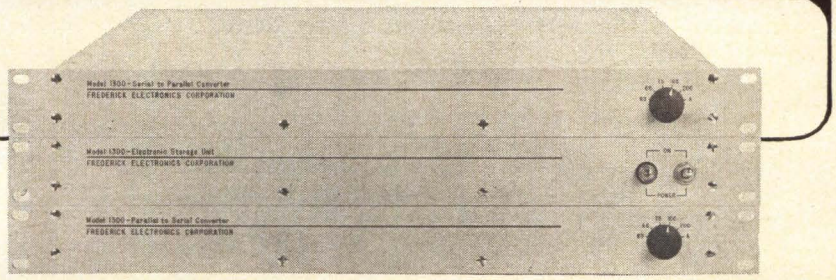

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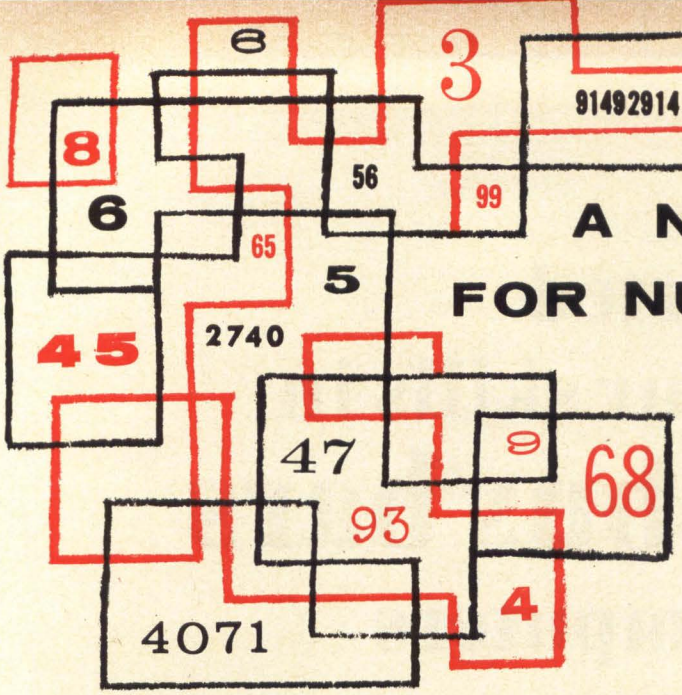

A NEW METHOD FOR NUMBER SYSTEM CONVERSION

There are many methods for converting numbers from one base to another. This article outlines a new method which is simpler than any now used. The Hartmann method will convert any number, including fractions, from one base to another in a few, easily-remembered steps, and can be either used manually or implemented by a computer. For instance, to convert 97 base 10 to binary, the following operations are performed:

1. Write the BCD of 9	1001
2. Shift two places to the left	1001
3. Write the BCD of 7 shifted one place to the right	111
4. The sum is the answer	$1100001_2 = 97_{10}$

The Hartmann method follows a consistent set of rules and is mechanical in nature. These rules are listed in Table 1. Because of the simplicity of the binary number used in Table 1, it might appear that the Hartmann method provides no real simplification. However, once the method is understood, it will become clear that it is a powerful tool for converting from one base to another for both integers and fractions. A few examples will illustrate this.

Example: Octal to Decimal

To convert octal 777 to decimal: (Note that arithmetic is done in decimal base)

1. $M = 8 - 10 = -2$
2. Multiply left digit (MSD) by M and move one place to the right and sum.

$$\begin{array}{r} 777 \\ -2 \times 7 = -14 \\ \hline 63 \end{array}$$

3. Multiply remainder by M, move one place to the right, bring down the next MSD, and sum:

$$\begin{array}{r} 637 \\ -2 \times 63 = -126 \\ \hline 511_{10} = 777_8 \end{array}$$

Example: Decimal to Octal

To convert decimal 511 to octal: (Note that arithmetic is done in octal base)

1. $M = 10 - 8 = 2$
2. $(2 \times 5)_8 = 12_8$

$$\begin{array}{r} 511_{10} \\ 12_8 \\ \hline 63_8 \end{array}$$

3. $(2 \times 63)_8 = 146_8$

$$\begin{array}{r} 631_8 \\ 146_8 \\ \hline 777_8 = 511_{10} \end{array}$$

Example: Decimal to Binary

To convert decimal 971 to binary:

1. All arithmetic must be done in binary, therefore, each decimal integer must first be converted into an equivalent BCD number:

9 = 1001 (Most Significant Character, MSC)
7 = 0111 (Second MSC)
1 = 0001 (Least Significant Character, LSC)

2. $M = 10 - 2 = 8_{10} = 1000_2$

Further care must be exercised in following the stated rules. In the previous examples, the number being converted from one base to another had the same integers in either base; e.g., $5_{10} = 5_8$. As a result of this compatibility, the entire number to be converted could be written down and operated upon digit-by-digit. In this example, each digit is considered separately.

3. Write down the MSC:	1001
4. Multiply MSC by M: $1001_2 \times 1000_2 = 1001000$	
5. Move the M-product one place to the right:	1001000
6. Move the second (next) MSC one place to the right:	0111
7. Partial Sum:	1100001
8. Multiply result by M	
9. Repeat step 5:	1100001000
10. Repeat step 6:	001
11. Answer (repeat step 7)	$1111001011_2 = 971_{10}$

This article presents a new technique for either manual or mechanized conversion of any number, from any base to any other base, using one simple set of rules. The technique, known as the Hartmann method, may well be the most significant contribution to number conversion since John Couleur's BIDEC in 1958.

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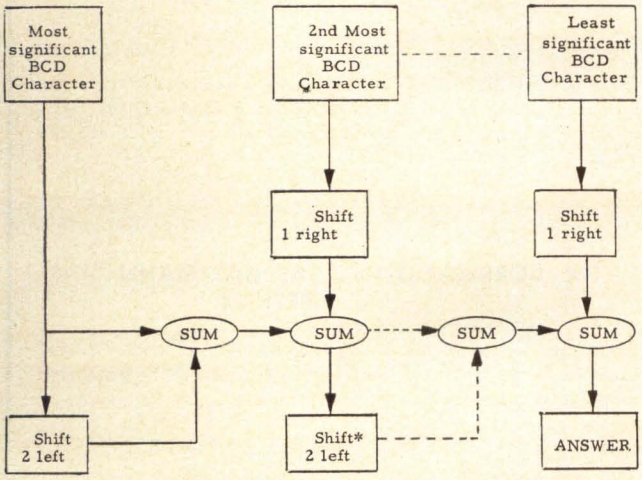

Fig. 1 Flow diagram for BCD to binary conversion. The asterisk refers to the fact that when the LSC has been summed, the answer will appear and further shifts are not necessary.

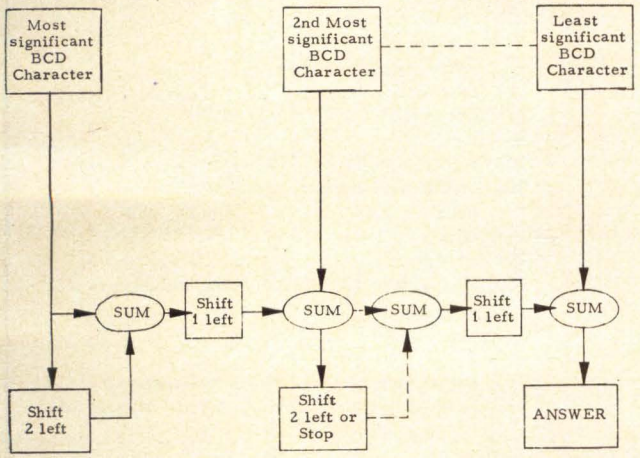

Fig. 2 Decimal to binary conversion flow diagram.

COMPUTER CONVERSION OF DECIMAL TO BINARY

The Hartmann method can be further simplified for decimal-to-binary conversion. The resulting process is simple for either manual or computer implementation, since only iterative shifts and additions are required. The manual process explained in the preceding example (conversion of decimal 971 to binary) can be simplified by the following equivalent set of rules:

TABLE 1
RULES FOR THE HARTMANN METHOD

RULES	EXAMPLE
Note: All arithmetic is to be performed in the new base	Convert binary 1101 to its decimal equivalent
1. Subtract the new base from the old base. The result is the magic number, M.	$M = 2 - 10 = -8$
2. Multiply the Most Significant Digit (MSD) in the number by M.	-8×1 (MSD) $= -8$
3. Move the product (of the above calculation) one to the right and sum with the MSD and the second MSD (regard the sign and carry or borrow as appropriate).	1101 − 8 3
4. Multiply the result by M.	$-8 \times 3 = -24$
5. Move the product one to the right and sum with the second and the third MSD.	30 − 24 6
6. Repeat the procedure in steps 4 and 5, moving on to the next MSD, until the LSD is reached.	$-8 \times 6 = -48$
7. The result is the number in the new base.	61 − 48 13_{10}

Once the method is understood, the actual arithmetic would be:

1101_2
− 8

30
− 24

61
− 48

13_{10}

TABLE 2 • PROOF OF THE METHOD

Any whole number N_b to any base b can be expressed by the following mathematical expression:

$$N_b = \sum_{i=0}^{K} a_i b^i \qquad \text{(Eq. 1)}$$

where b and a are the multiplying constants. The problem is to find the equivalence between the constants in two number systems, when both are describing the value N. The following symbols will be utilized:

b_n = new base
b_o = old base
a_i = multiplying constants of b_o
c_j = multiplying constants of b_n

Find c_j in terms of a_i so that the following equality is true.

$$N_{b_o} = \sum_{i=0}^{K} a_i b^i{}_o = N_{b_n} = \sum_{j=0}^{L} c_j b^j{}_n \qquad \text{(Eq. 2)}$$

Since $a_0 b^0{}_o = a_o$, then:

$$\sum_{i=0}^{K} a_i b^i{}_o = a_0 + \sum_{i=1}^{K} a_i b^i{}_o \qquad \text{(Eq. 3)}$$

When $b^i{}_n$ is added and subtracted to the right-most term of Eq. 3, and the identity of Eq. 2 is employed, the following equation results:

$$N_{b_n} = N_{b_o} = a_0 + \sum_{i=1}^{K} a_i \left[b^i{}_n + (b^i{}_o - b^i{}_n) \right] \qquad \text{(Eq. 4)}$$

To put Eq. 4 in a more usable form, an expansion of $(b^i{}_o - b^i{}_n)$ is helpful. By long division (or reference to an algebra text):

$$b^i{}_o - b^i{}_n = (b_o - b_n)(b^{i-1}{}_n\, b^0{}_o + b^{i-2}{}_n\, b^1{}_o + b^{i-3}{}_n\, b^2{}_o \ldots b^0{}_n\, b^{i-1}{}_o) \qquad \text{(Eq. 5)}$$

for $i \geq 1$.

Substituting Eq. 5 into Eq. 4, the following equation results:

$$N_{b_n} = N_{b_o} = a_0 + \sum_{i=1}^{K} a_i \left[b_n{}^i + M(b_n{}^{i-1} + b_n{}^{i-2} b_o{}^1 + b_n{}^{i-3} b_o{}^2 \ldots b_n{}^0 b_o{}^{i-1}) \right] \qquad \text{(Eq. 6)}$$

where $M = (b_o - b_n)$, and $b^0{}_o$ has been dropped since it is equal to 1; $b_n{}^0$ has been retained because the powers of b_n determine the position of factors in the new base. Proof Example 1: Convert binary 1101 to decimal.

$$N_{b_o} = 1101 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0.$$

The terms of Eq. 6 are, by inspection:

$K = 3$, $a_3 = 1$, $a_2 = 1$, $a_1 = 0$, $a_0 = 1$, $b_o = 2$ and $b_n = 10$.

Therefore $M = b_o - b_n = -8$

Applying Eq. 6:

$$N_{b_o} = N_{b_n} = 1 + 0\left[10 + (-8)(1)\right] + 1\left[100 + (-8)(10 + 2)\right] + 1\left[1000 + (-8)(100 + 20 + 4)\right]$$

$$N_{b_n} = 1 + 4 + 8 = 13_{10}.$$

Therefore $c_1 = 1$ and $c_o = 3$.

Proof Example 2: Convert 13_{10} to binary.

$$N_{b_o} = a_1 \times b^1{}_o + a_0 \times b^0{}_o = 13_{10} = 1 \times 10^1 + 3 \times 10^0$$

Therefore: $b_o = 10_{10}$, $b_n = 2_{10}$, $a_1 = 1_{10}$, $a_0 = 3_{10}$

And $M = 10 - 2 = 8_{10}$.

From Eq. 6:

$$N_{b_n} = 3_{10} + 1_{10}\left[2^1{}_{10} + (10 - 2)_{10}\, 2^0{}_{10}\right]$$

Expressing all numbers in terms of the new base (2):

$$N_{b_n} = 011 + 1\,(10 + 1000) = 1101_2.$$

Therefore $c_3 = 1$, $c_2 = 1$, and $c_1 = 0$ and $c_0 = 1$.

The following shows how this technique is developed into a fast method of conversion. By rearranging and following the terms in Proof Example 1, the correlation between the proof and the method is shown.

THE CORRELATION

When the terms of the Proof Example 1 are arranged vertically and grouped by powers in b_n the example will appear as follows:

1000	contribution by positive $b^3{}_n$ term
100	contribution by positive $b^2{}_n$ term
00	contribution by positive $b^1{}_n$ term
1	contribution by positive $b^0{}_n$ term
1101	sum plus terms
− 800	contribution by negative $b^2{}_n$ term
301	partial sum
− 160	contribution by negative $b^1{}_n$ term
− 80	
61	partial sum
− 32	contribution by negative $b^1{}_n$ term
− 16	
0 x (−8) − 0	
13_{10}	final sum

THE HARTMANN METHOD

Determine the magic number M = (old base) − (new base) = − 8

1101	write down number
− 8	multiply MSD × M
3	partial sum (p_1)
30	bring down next MSD and
− 24	multiply p_1 × M
6	partial sum (p_2)
61	bring down next MSD
− 48	multiply p_2 by M
13_{10}	sum

The calculation reduces to the following:

1101
− 8
30
− 24
61
− 48
13_{10}

ARITHMETIC	HARTMANN METHOD
1001	MSC
1001	Shift MSC "two" left
101101	First Partial Sum
0111	Second MSC shift "one" right
1100001	Second Partial Sum
1100001	Shift 2nd Partial Sum "two" left
111100101	Third Partial Sum
0001	LSC shift "one" right
1111001011_2	Final Sum

Fig. 1 illustrates a hardware/software implementation that will convert a decimal number (in BCD) to the equivalent binary number, following the arithmetic of the above example. A better computer implementation is obtained by deleting the "Shift 1 Right" and adding a "Shift 1 Left" as shown in Fig. 2.

CONVERSION OF FRACTIONS

The method is especially useful in converting a fraction in one base to the equivalent fraction in any other base. The proof of this method of number base conversion states that the process will work for any whole number. (It can be shown that the method fails for negative exponents.) Therefore to convert a fraction from one base to another, the number is treated as consisting of a whole number in the numerator and a whole number in the denominator. When converting a mixed number, first convert the whole number and then the fractional part. The following examples demonstrate the principle of base conversion of fractions.

Binary Fraction To A Decimal Fraction

To convert 0.011 in binary to decimal:

1. Apply the method as previously explained, disregarding the binary point; i.e., convert 11_2 to the base ten:

$$M = 2 - 10 = -8$$

$$11$$
$$-\ 8$$

$$3_{10} = \text{numerator}$$

2. Find the denominator by raising the old base to a power equivalent to the number of places. Hence, the denominator is equal to $2^n = 2^3 = 8$, and the fraction to the base ten is $\frac{3}{8}$.

Octal Fraction To A Decimal Fraction

To convert octal 0.400 to the decimal:

1. Find the numerator:

$$M = 8 - 10 = -2$$

$$400$$
$$-8$$

$$320$$
$$-64$$

$$256_{10} = \text{Numerator}$$

2. Find the denominator:

$$8^n = 8^3 = 512_{10} = \text{Denominator}$$

$$\text{Hence } 0.400_8 = \left(\frac{256}{512}\right)_{10} = 0.500_{10}$$

SUMMARY

This simple method for converting from one base to another is useful for anyone working in computer technology. It is easily-remembered, and easily implemented in either hardware or software. A proof of the validity of this method of conversion is given in Table 2, together with illustrations relating the algebraic proof with the simple mechanics of the method. Further information on the Hartmann method will be included in S. Hartmann's "Fundamentals and Design Concepts of Digital Computers," to be published by John Wiley and Sons in the first quarter of 1967. END

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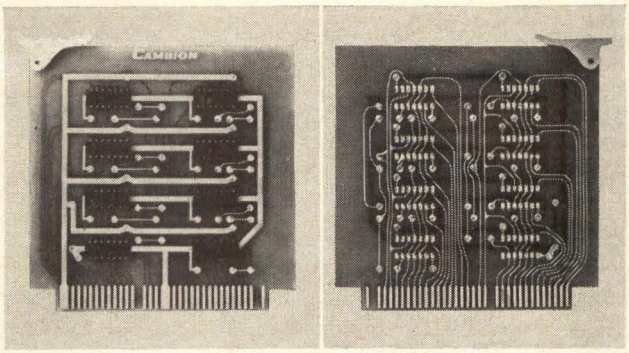

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SMALL ECONOMICAL DIGITAL SYSTEMS USING MULTI-SECTOR CORE MEMORIES

Mass-production has significantly altered the cost/performance characteristics of core memory systems. In this article, the author contends that many tasks for which small computers are currently being selected can be done more economically adding a minimum of circuitry to core memory systems.

EDWIN PODSIADLO, Product Mgr.,
Memory Systems Div.,
Ferroxcube Corp.,
Denver, Colo.

The modern general-purpose, coincident-current core memory is actually usable as a versatile data-manipulating system, capable of many functions other than simple data storage. This versatility is made possible by the fact that memory systems are now mass-produced in forms that provide, as standard features, many of control, access, and operating-mode functions formerly associated with custom-designed systems. The mass-produced memory of today is a true general-purpose device, designed to provide most, or all, of the operating and access modes listed in Table 1. The low-cost, general-purpose memory is not yet capable of the highest speeds available in state-of-the-art custom designs but it is, with the addition of a minimum of external circuitry, perfectly adequate for the majority of everyday data-processing tasks — including most of those ordinarily assigned to small-scale EDP machines — and it provides this versatility at low cost-per-bit and cost-per-function operations, unprecedented in the industry.

As an example, a standard "off-the-shelf," medium-speed memory, as illustrated in Fig. 1, can be turned into a small data-processing system by adding to it only five standard logic cards (four in the adder/subtractor and one containing steering gates and control flip-flops) as shown in Fig. 2. The complete system costs only about $400 more than the memory, or about one-third of the cost of the smallest "desk-model" computer. Such a system will perform all of the following functions:

- Data storage
- Code conversion
- Random-access data search
- Sequencing of data
- Grouping of data
- Format conversion
- Time buffering (between elements having different data rates)
- Gating of data (in response to commands)
- Table look-up (using a stored-program).

System Example

To illustrate this capability let us assume that we wish to set up a small department store inventory-control system. As shown in the data-flow diagram of Fig. 3, it must perform the following functions.

- Accept batched "transaction" data from a primary medium such as keyboard-loaded paper tape or punched cards.
- Use the transaction data to update a permanent inventory of the stock in a local warehouse or storeroom.
- Compare the inventory with preestablished minimum stock levels, and issue orders that will replenish the stock adequately.
- Link the system to a remote central warehouse by Teletype, or to a local typewriter that will prepare purchase orders.
- Provide a permanent record, on magnetic tape, of both the transactions processed, and the orders placed.
- Provide a printed record, on command, of the inventory levels in any or all categories of products.

The key to the use of a coincident-current memory as a multi-function data-processing device is to divide the memory into sectors, each of which has a special function, and to use the sectors independently in the many possible access and operating mode combinations of a general-purpose memory. This use of the memory is practical because not only is a modern core memory equipped to function in many different access and operating modes, as shown in

TABLE 1

OPERATING & ACCESS MODES IN CORE MEMORIES

FULL-CYCLE OPERATION	Read/restore (unload). The information stored at a selected address location is read out, then restored in the same location. Clear/write (load). The information stored at a selected address location is erased by the clear operation, and new information is written into the same location.
SPLIT-CYCLE OPERATION	Information at one selected address location is read out and externally modified; then, on command, the modified information is restored to the original address location.
HALF-CYCLE OPERATION	Read-only — stored information is read out of one selected address during each half-cycle operation. Write-only — information is written into one selected address during each half-cycle operation.
RANDOM ACCESS MODE (Full-cycle, Half-cycle, or Split-cycle)	Memory addresses are selected individually, for readout and/or storage, by loading an appropriately-coded instruction into the address register.
SEQUENTIAL ACCESS MODE (Full-cycle or Half-cycle)	Addresses are loaded or unloaded in a preselected sequence, under the control of a counter.
SEQUENTIAL-INTERLACE ACCESS MODE (Full-cycle or Half-cycle)	Permits independent reading and writing; information may be written at any series of addresses, interlaced with reading out other previously-stored information at any other series of addresses, under the control of two separate counters.

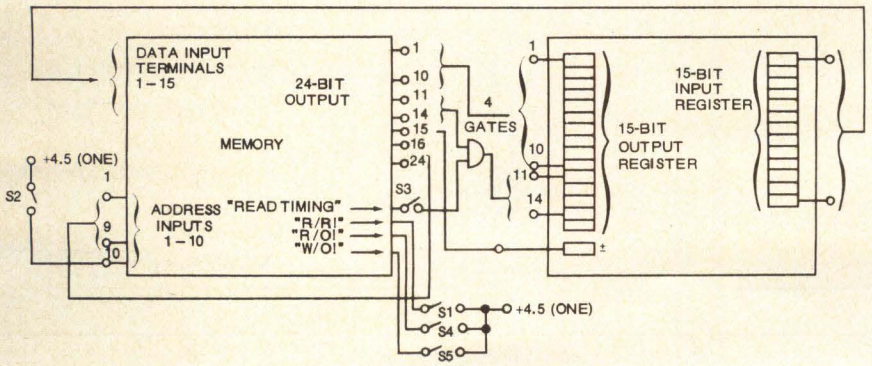

Fig. 1. Basic core memory system.

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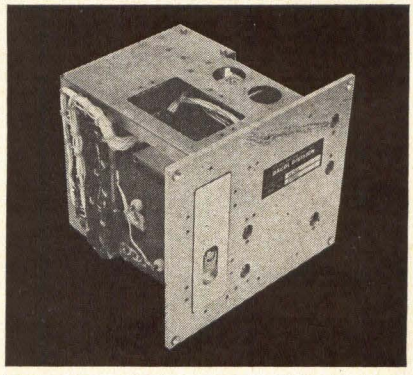

STORAGE MEDIUM	½", 7 track, cartridge loaded magnetic tape.
STORAGE CAPACITY	500,000 data bits on 36 feet of tape at a density of 200 characters per inch.
OPERATING MODES	Read, Rewind, Search, Standby.
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TABLE 2

SUMMARY OF SYSTEM OPERATION

OPERATION	STEP	MEMORY MODE	SECTOR(S) USED	NOTES
LOAD RAW DATA	1	Full-cycle, clear/write	A	
CORRECT STOCK LEVELS	2	Full-cycle, read restore	A	Into adder/subtractor
	3	Random-access, half-cycle, read-only	B	Into adder/subtractor
	4	Random-access, half-cycle, write-only	B	From adder/subtractor back into B
RECORD TRANSACTIONS	5	Sequential access, half-cycle, read-only	A	To magnetic tape recorder from A
CHECK STOCK LEVELS	6	Sequential access, read/restore	B	Into adder/subtractor
		Random-access, read/restore	C	Into adder/subtractor
		Random-access, half-cycle, write-only	D	Writes a ONE into 24th bit position of selected word.
ISSUE ORDERS	7	Sequential access, full-cycle, read/restore	D	Searches for a ONE in 24th bit pos.
		Random-access, full-cycle, read/restore	F or G	Executes order by Teletype or typewriter
RECORD ORDERS	8	Sequential access, full-cycle, read/restore	D into E	Collects orders in sequence, without gaps
		Random-access, full-cycle, read/restore	E and H	H acts as code converter, to permanent record (magnetic tape)
		Sequential access, half-cycle, read-only	E	E is purged of data
REPORT STOCK	9	Random-access, split-cycle, read-modify/write	B	Printer controls the write timing. (No actual modification of data.)

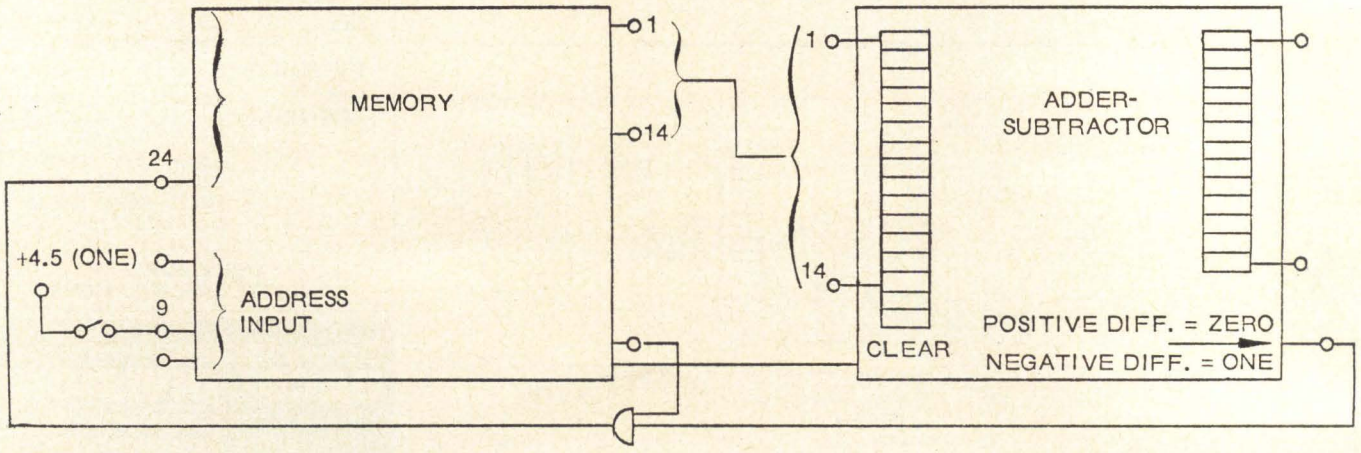
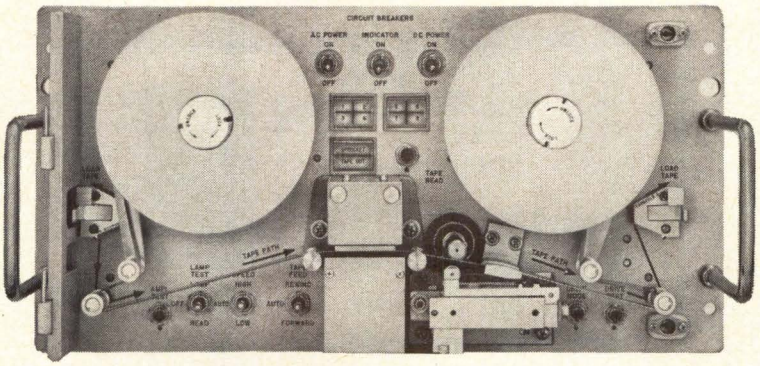


Fig. 2. Core memory processing system.



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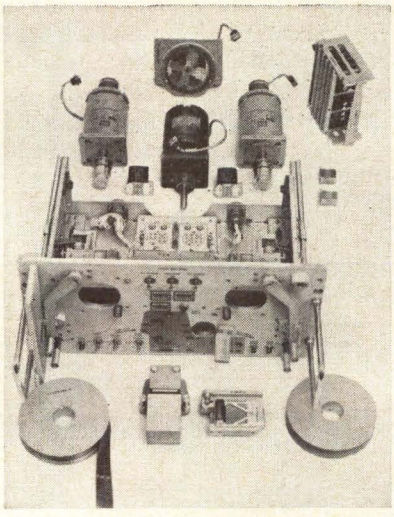

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TABLE 3

DETAILED IMPLEMENTATION OF SYSTEM EXAMPLE

Step 1: **LOAD RAW DATA** — Up to 1024 words of raw data are loaded into Sector A, operating as a sequential access, full-cycle, clear/write buffer. Each word contains 24 bits; ten show the quantity of the item sold or returned, four show which department originated the transaction, one shows the nature of the transaction *(does it raise or lower inventory on hand?)*, and the last nine designate the specific item involved.

Step 2: **CORRECT STOCK LEVELS** — In the sequential access, full-cycle, read/restore mode, the memory reads the first address in Sector A. As the 24-bit word is read out, the 10-bit quantity segment is fed into the shift register that forms the input to the 15-bit serial adder/subtractor; the transaction bit goes to the add/subtract flip-flop, and the 9-item identification bits are routed back to the address register of the memory, to be used in the next step. At the end of the cycle, all 24 bits are also restored in their original location in Sector A.

Step 3: **CORRECT STOCK LEVELS** — The 9-bit identification segment stored in the address register 2^{10} added to it (a one on the 10th line) which adds 1024 to the address number, thus directing the 9-bit segment to its corresponding segment stored in Sector B (locations 1025 through 1536). In addition to this identification segment, each word in Sector B contains a 14-bit quantity segment showing the stock level of the item. With Sector B in the random-access, half-cycle, read-only mode, the 14-bit quantity segment at that location in Sector B is fed to the adder/subtractor, where it is raised or lowered by the quantity previously stored from Sector A in Step 2.

Step 4: **CORRECT STOCK LEVELS** — Sector B is switched to the random access, half-cycle, write-only mode, and the new stock level from the adder/subtractor is restored to the same address used in Step 3. Steps 2 through 4 are repeated until all 1024 addresses in Sector A have been used to correct the stock levels they affect in Sector B.

Step 5: **RECORD TRANSACTIONS** — Sector A is now used as a sequential access, half-cycle, read-only buffer to record all 1024 transaction words on mag tape; after this operation the sector is clear and ready for new raw data.

Step 6: **CHECK STOCK LEVELS** — Each stock level stored in Sector B is compared with the corresponding minimum inventory figure already stored in Sector C; the C address is simply the B address plus 512. Both quantities are fed into the adder/subtractor (and restored in their original places) and the C quantity is subtracted from the B quantity. If the difference is negative, an order must be issued, in which case an ordering bit is stored in the 24th bit position of the corresponding address in Sector D (which is simply the B address plus 1024).

Step 7: **ISSUE ORDERS** — It is most practical to check stock levels and issue orders at the end of every day — or less often, if desired. Sector D stores the information that a reorder is needed for an indefinite period, even if the system has been shut down, because a core memory is non-volatile. When we are ready to reorder, Sector D is scanned sequentially until a ONE is found in a 24th bit position, at which time, the first 12 bits of the D word are used to address either Sector F or Sector G. Sector F and G words identify the item and quantity to be ordered, and in the 24th bit position store a ONE if the order is to be Teletyped to a remote warehouse, or a ZERO if it is to be locally typewritten for issue.

Step 8: **RECORD ORDERS** — If it is desirable to record the orders issued on magnetic tape in a different code from that used in Sectors D, F, & G, we have a stored-program in Sector H, in which every address has an order quantity and item-identification in the magnetic tape code. To record orders, we again scan Sector D, looking for ONE in the 24th bit position, but this time using bit positions 13-23 of the D word, which (with a one added) will locate the corresponding newly-coded word in Sector H. The orders can be consolidated in a continuous sequence, so that the tape recording may be efficient and without gaps, by using Sector E as a "scratch pad" and writing bits 13-23 of every word from Sector D containing a 24th bit ONE, into successive addresses in Sector E, then using Sector E to address Sector H. Here, Sector E is used in the sequential-interlace, half-cycle, read-only mode, in order to purge itself of the order data. Sector H is used in the random-access, full-cycle, read/restore mode, so as not to lose the stored program.

Step 9: **REPORT STOCK LEVELS** — To report stock levels at a given time, Sector B is used as a sequential-address, split-cycle, read/restore memory to print out each 14-bit quantity segment and the address from which it comes, (which identifies the item). The split cycle is used to allow the printer to control the timing and avoid the need for a separate buffer; the end-of-print signal acts as the restore command.

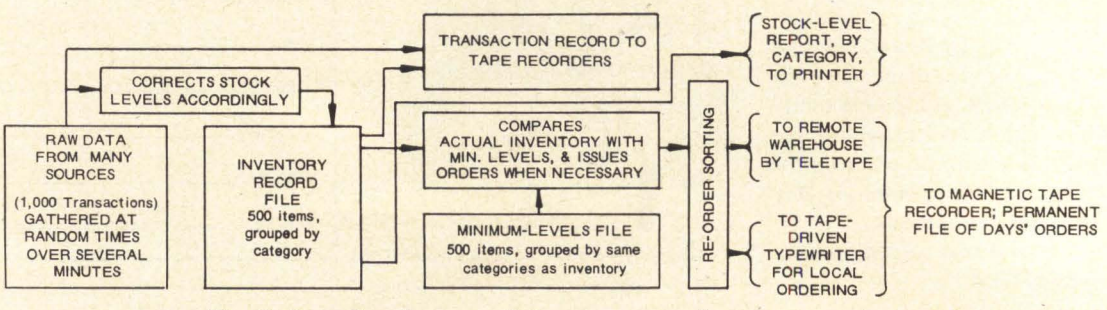


Fig. 3. Data flow for a small inventory control system example.

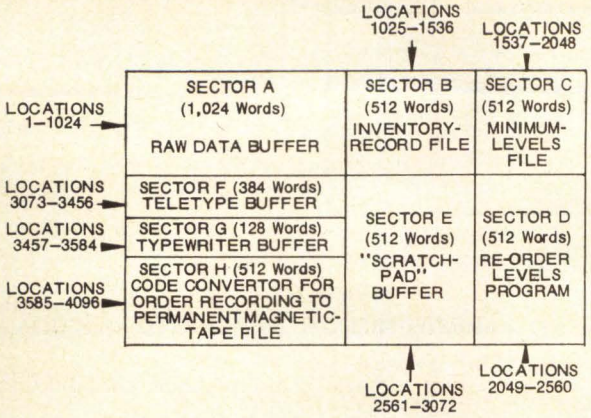


Fig. 4. Memory sector assignments.

Table 1, but it may be easily switched from one mode to another by means of very simple external circuitry — often no more than a single-line signal. The inventory stock in the above example consists of different quantities of some 500-odd separate items (e.g., 1200 of Item A, 50 of Item B, 300 of Item C, etc.), and these stock levels must be processed as outlined above. We shall, therefore, need a memory divided into several sectors, two or more of which are involved in each of the processes contemplated, and each containing 512 "addresses" — one for each item. A larger sector of, for example, 1024 addresses will be required to handle our initial raw individual transaction data. Planning from the flow diagram of Fig. 3, we select a memory of 4096 words and sector it as shown in Fig. 4. This memory, together with the external circuitry previously shown in Fig. 2, will perform the required operations summarized in Table 2. The step-by-step process is described in Table 3.

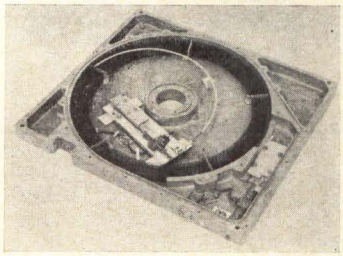
By using a single, small, relatively inexpensive core memory, and by adding to it one logic card with 12 gates and 6 flip-flops, and four logic cards containing the lowest-cost adder-subtractor circuit, we have implemented every one of the requirements imposed on the system. Furthermore, we have designed a more reliable, more efficient, and smaller system than could be done by adapting a static flip-flop EDP machine to our needs. Nothing has been lost except a few seconds per hour of cycle time, which are not needed in this system. As it is, the memory will be active only about 5% of the time between batches of raw data. Most of the time, it is waiting for the printer, or the Teletype transmitter, or the typewriter.

Modern core memories offer so many built-in logical functions beyond mere data storage that the alert designer can simplify and lower the cost of almost any digital system employing core storage. Moreover, he can almost always add more functional capability to that system or machine, at little or no additional cost, by using more of the core memory's "logic power." It is particularly important to note that many of the small EDP machines — the so-called "desk-top" economy models — contain little more than what we have described above, with provisions for adding (at extra cost) a variety of interface and programming accessories. Beyond a flexible core memory and a modest arithmetic unit, these "computers" offer little more than well-organized groups of input/output terminals. In the author's opinion, they are a poor choice for fixed-operation data processing, and are certainly overpriced for such tasks as described in this article.

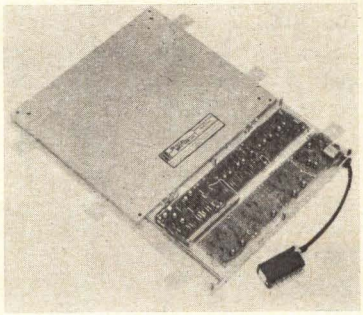
Conclusion

Now that medium-speed core memories have reached mass-production volume, their cost-per-bit and cost-per-function have decreased dramatically. It is reasonable to feel that even the designs of older systems and machines, which have already been put into large-scale production, should be reviewed for possible adaptation to "memory processing." Certainly all new designs should contemplate the use of a core memory as the data processor. END

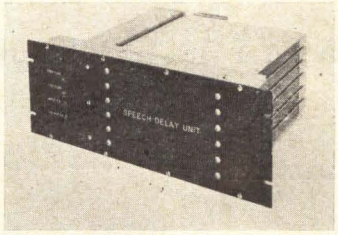
DELAY LINES



MEMORY SYSTEMS



SPECIAL SUBSYSTEM



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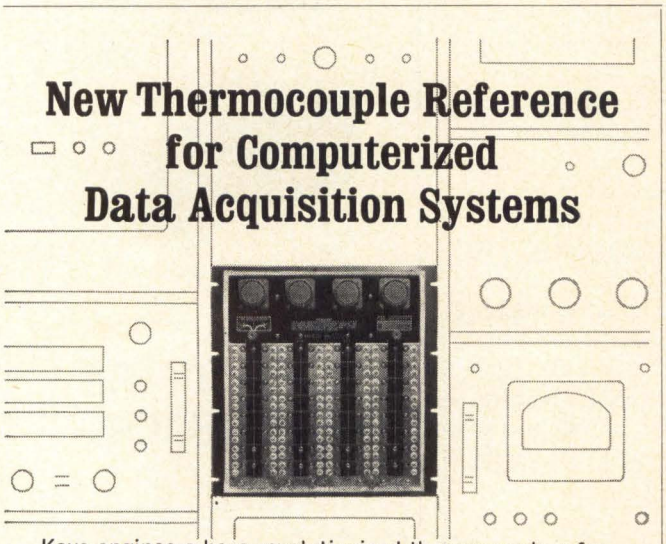

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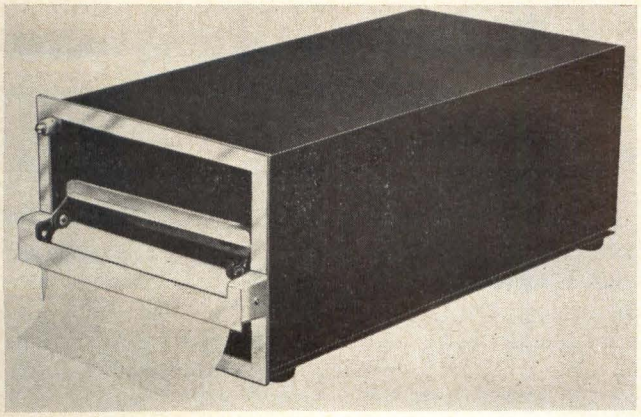

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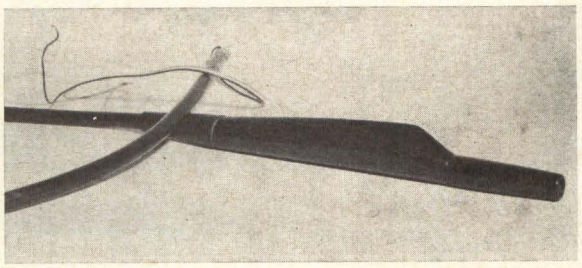

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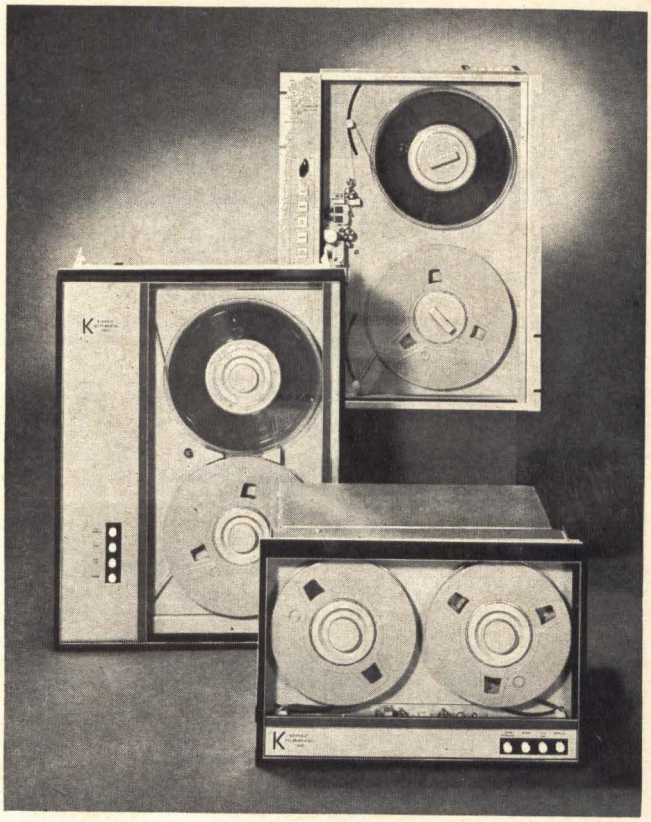

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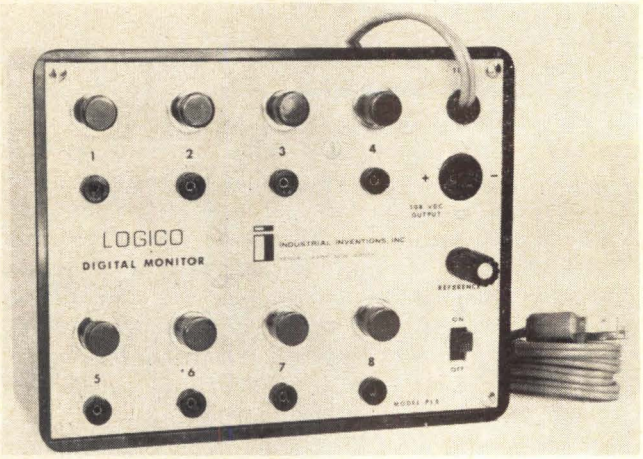
A new metal-encapsulated solid tantalum capacitor is so compact in shape that 14 of them can be stacked in less than a cubic inch. The new polar capacitor starts as a high-purity slab (rectangular) anode, fitting tightly into a metal case that is hermetically sealed to a mating, all-metal top. The construction makes it especially suitable for use on printed circuit boards where space is at a premium and where volumetric efficiency is mandatory. Working voltages are 6, 10, 15, 25, 35, and 50. The permissible temperature operating range is from −80 to +125 degrees C. The capacitors come in two case sizes. In the Y case the height is 0.385″, the length 0.360″, and the width 0.170″. In the Z case the height is the same, the length 0.600″, and the width 0.195″. All measurements are ±0.015″. Each capacitor has solder-coated, high purity Kovar wire leads uniformly-spaced 0.200″ apart to fit printed boards and a glass seal. This particular construction feature is said to eliminate the problem of destroying hermeticity during wave soldering applications. Union Carbide Corp., Greenville, S. C.

Circle No. 280 on Inquiry Card



DIGITAL SYSTEMS TESTER

By providing a simultaneous visual indication of the logic states of up to 18 digital or binary circuits, a new test instrument gives a total insight into the operation of any discrete or integrated system. The unit will not affect the circuit under test and can be used with any commonly used logic voltage system in use today. Called the Logico, the testing instrument can replace an oscilloscope in numerous applications and can be left permanently in the circuit while breadboarding a system. It is said to be extremely useful for trouble shooting, life, and temperature testing. Industrial Inventions, Inc., Monmouth Junction, N. J.

Circle No. 295 on Inquiry Card

INCREMENTAL PHOTOELECTRIC ENCODER

A new photoelectric encoder is said to be ideally suited for use as an electrical tachometer or shaft-angle measuring device in numerically-controlled machine tools, computer tape transports, processing equipment, and in applications demanding accurate determination of rotational speed or angular displacement. The Model 8608 is 2½ inches in diameter, with rugged all-metal case construction, and is fully shielded from dust, oil, and moisture. Mechanical features include low moment of inertial — 2.5 x 10^{-5} oz. in./sec.^{2}; low torque 0.2 in. oz. starting and 0.1 in. oz. running; and light weight — 8 oz. The encoder delivers a 2-volt peak to peak quasi sine wave output, zero centered, into a 10,000 ohm load. A number of standard stock code patterns are available for use with this assembly, providing single track, quadrature, and index pulse outputs. Custom disc patterns can be made to specific requirements. W. & L. E. Gurley, Troy, N. Y.

Circle No. 282 on Inquiry Card

DIGITAL LINE RECEIVER

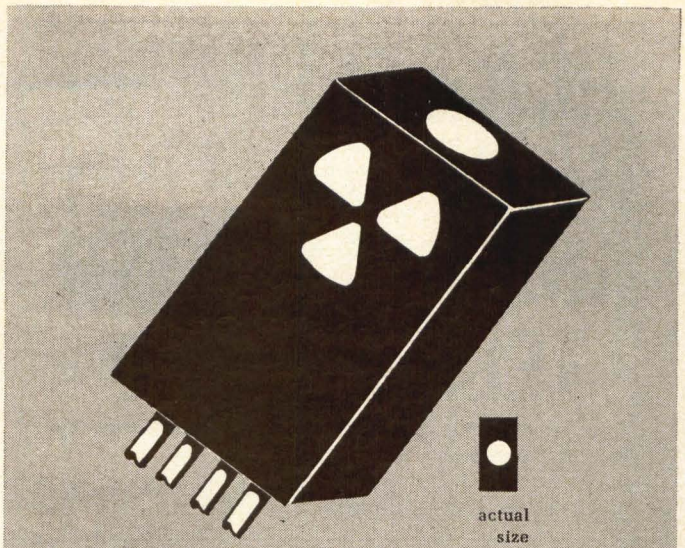
An integrated circuit digital line receiver was developed for military and industrial logic applications requiring high noise immunity. Designed primarily as a signal discriminator at the end of a coax transmission line in digital data systems, the circuit is also useful as a voltage comparator. Consisting of two gates driven by a differential amplifier, it has a TTL input and complementary outputs compatible with DTL and TTL logic. Input threshold is set by the differential amplifier reference voltage which may be adjusted over a 3- to 4.5-volt range. Propagation delay time is typically 40 nsec at 25°C. Nominal supply voltages are 3.6 volts bias, +5 volts gate supply, and +12 volts differential amplifier supply. Typical power dissipation is 100 mw. Siliconix, Inc., Sunnyvale, Cal.

Circle No. 276 on Inquiry Card

TIMER/COUNTER

Laboratory instrument combines timing or counting functions in one low-cost package. When used in the counting mode, it can indicate 1,500 counts/minute. When in the timing mode, it can indicate to 0.001 minute. Among the possible uses, the unit may perform as a delay-interval times, an event timer, a stop clock, a totalizing counter, or predetermining counter. It can operate passively as a timer or totalizer, or can operate other equipment a predetermined length of time or number of operations. Digital readout (999,999 maximum count or 999,999 minutes maximum time) provides fine resolution for large total time. Maximum timing error is ±0.001 minute over the total 16-hour 40-minute timing period. Heli-Coil Corporation, Danbury, Conn.

Circle No. 287 on Inquiry Card



NEW Microminiature "BITE"* Indicators

Continuously monitor circuit and system performance.

**BITE . . . Built-In Test Equipment is now required by DOD on avionic equipment down to the module level where possible. These indicators give a visual indication if circuit or system performance falls below design parameters.*

Now you can design a microminiature indicator into any electrical or electronic circuit to alert operators if equipment performance is faulty or below desired operational levels. Even if the failure is transient, the indicator continues to register the fault by means of magnetic latching until a reset signal is applied to the terminals. Normal appearance of the case is black. If a fault develops, the windows show white in sharp contrast to the case.

TYPICAL APPLICATIONS

In-flight monitoring of 400 cycle alternators.

Voltage sensors to determine if voltage variations exceed an allowable excursion range.

Servo loop in aircraft control system. Indicator has a built-in time delay. When a control signal is applied to the system, the indicator detects any failure to respond within 10 milliseconds, after which the time delay triggers the BITE indicator to signal failure.

Ground-support computer equipment. Indicator continuously monitors the complement of the output code and signals if an erroneous code is generated.

GENERAL SPECIFICATIONS

These units measure only .7″ x .2″ x .4″, a volume of only .056 cu. in. Operating range is 17-29 VDC. Response is to a pulse width as low as 15 milliseconds; special units will respond in 5 microseconds. They can be supplied with internal switching so power is used during indication transfer only. Several variations are available: Units utilizing a 4 volt fault signal; round types; pop-up indicators; and units with special interface circuitry. All meet the applicable requirements of MIL-E-5400H (ASG) Class 1-A Equipment.

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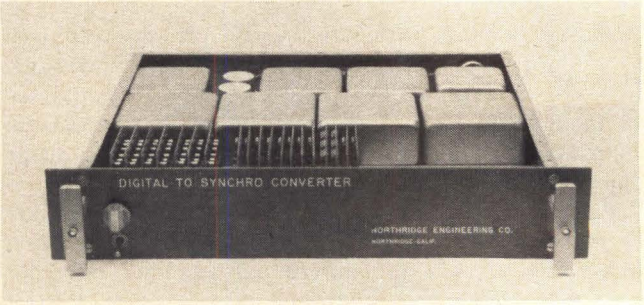
CIRCLE NO. 71 ON INQUIRY CARD

NEW PRODUCTS

12-STAGE COUNTER

A 12-stage counter circuit card is particularly useful in time base generators and as frequency dividers. Capable of operation in binary or BCD code, the 12 flip-flop stages of the counter may be used as a 4 bit to 12 bit binary or as a 1 to 3 digit BCD counter. Two or more cards may be used to construct counters of any length. The overall counter is set up in three independent 4 bit groups, each with separate reset and counter inputs. For operation in BIN or BCD code, feedback terminations from each group are wired in at the connector. Control gates associated with the counting inputs allow gated operation for period and frequency measurement. Counters operate from dc to 1 mc and have a maximum propagation delay per decade of 120 ns. Control Logic, Inc., Natick, Mass.

Circle No. 290 on Inquiry Card



DIGITAL-TO-SYNCHRO CONVERTER

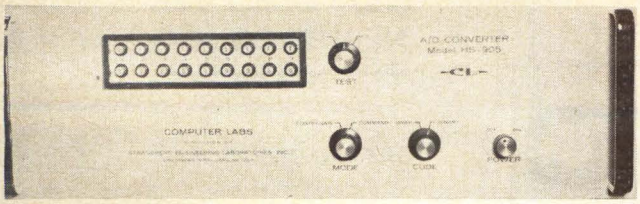
New dual-channel digital-to-synchro converter accepts parallel binary words and converts to precise synchro output signals slew rate is 36,000 degrees per second. Input is 8 to 14 bit binary angle or sine/cosine binary. Output is 60 HZ synchro or sine/cosine. Unique circuit is said to accomplish trigonometric conversion and analog conversion in a single step without sequential logic. No motors, gears, encoders, or adjustments are used in the converters. Monolithic integrated circuit logic allows packaging in a 3½" chassis. An interface transmitter is available to operate converters from remote data source. Northridge Engineering Co., Northridge, Cal.

Circle No. 294 on Inquiry Card

MONOLITHIC OPERATIONAL AMPLIFIERS

New operational amplifier is manufactured with a silicon planar epitaxial construction technique on a single monolithic substrate. It may be used as a single or dual input amplifier. One single chip monolithic technique provides low offset voltage and current along with high thermal stability and high common mode rejection capabilities. Continental Device Corp., Hawthorne, Cal.

Circle No. 288 on Inquiry Card



A-D CONVERTERS

A new principle of A/D conversion is employed in a full line of new converters which is said to permit greater speed with fewer parts. The new line encompasses a range from one bit at 50 MHz to nine bits at 5 MHz. Model HS-710, for instance, produces a 7-bit word at a rate of 10 MHz. It is capable of encoding an analog band width of 5 MHz, such as high-quality television video information. With only ±0.75 nanoseconds aperture time, the converters offer continuous encoding as well as external command encoding at any random or periodic rate up to the maximum word rate. Both gray and binary outputs are provided. All models include sample-and-hold circuitry as well as power supplies in conventional packages for convenient 19″ or 24″ rack mounting. Computer Labs Div., Strandberg Engineering Labs., Inc., Greensboro, N. C.

Circle No. 278 on Inquiry Card

TIME CODE GENERATOR

New time code generator generates any popular analog or digital time code (NASA, IRIG, AMR etc.). It can encode any five simultaneous analog (modulated carrier) time codes and also generate a digital level shift code, a parallel binary coded decimal indication of time, pulse rate outputs, and a front panel display of time in days, hours, minutes, and seconds. It can be used as a basic time standard for data logging, computer applications, range timing, and display. The entire unit, including the front panel display, will automatically switch over to operation from an external battery in the event of a primary ac power failure without disrupting the time code. Dynalectron Corp., Wash., D.C.

Circle No. 277 on Inquiry Card

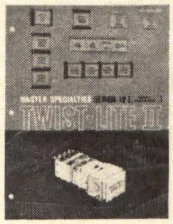
BUFFER MEMORY

New delay line buffer provides storage for up to 67,000 bits of information at a 2 MHz bit rate. The system recirculation rate is 33 msec corresponding to 30 per second refresh rate used in most TV display applications. The package consists of four conservatively-rated magnetostrictive delay lines, each complete with read, write and re-timing electronics. A separate interface board matches buffer electronics with external system logic. Standard boards provide compatibility with integrated logic circuits. Quantity prices approach 1¢ per bit including recirculation and interface electronics. Digital Devices, Inc., Syosset, N. Y.

Circle No. 293 on Inquiry Card

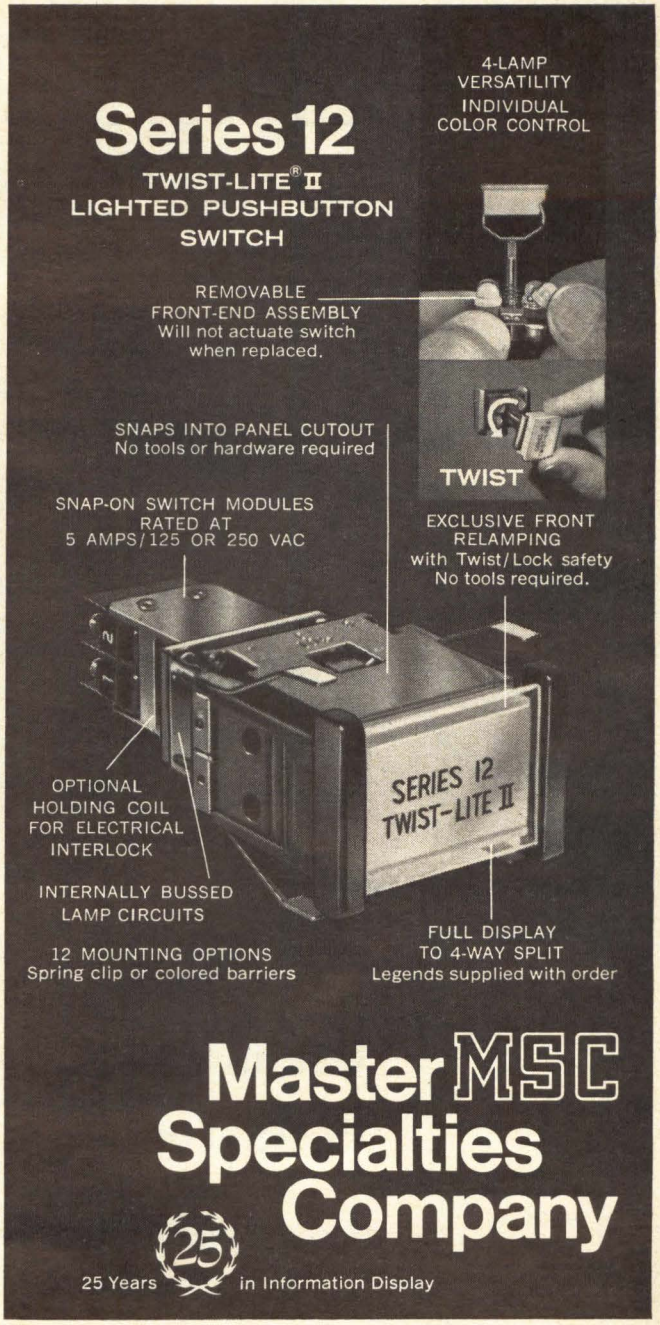
The lighted pushbutton switch with aerospace quality at commercial prices!

The MSC Series 12 embodies aerospace features that reduce installation costs, increase performance and simplify maintenance, yet it is priced for commercial use. Compare the features below. From the Twist/Lock front end removal for easy lamp, legend and color filter change to the time and cost saving internally bussed lamp circuits, you'll see why it is your best buy for industrial controls and any commercial equipment.



GET THE 20-PAGE CATALOG 2001

It details the many options offered by the versatile Series 12. Use the reader service card . . . or write on your letterhead and ask for an operating demonstration by your nearby MSC specialist.



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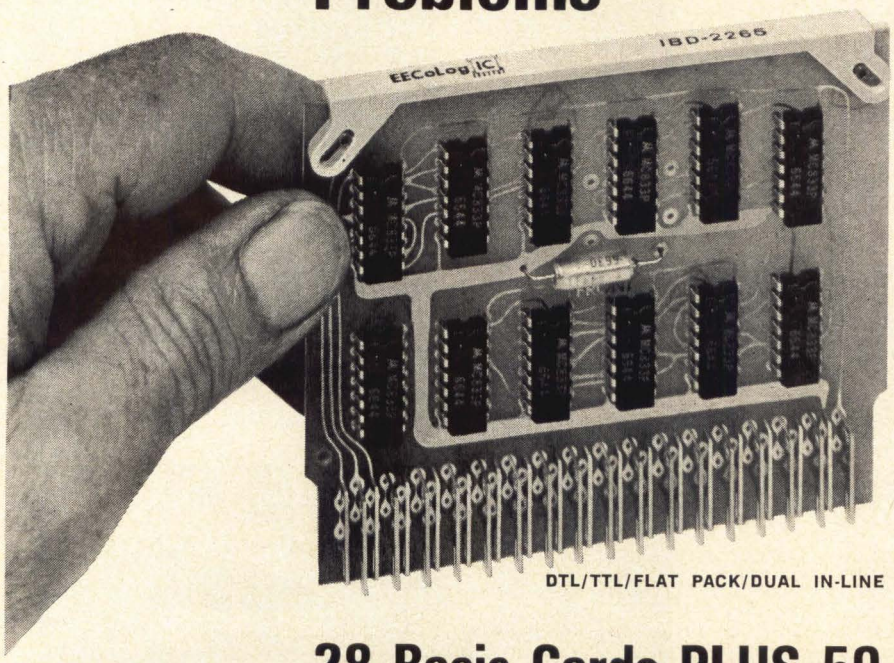

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CIRCLE NO. 73 ON INQUIRY CARD

NEW PRODUCTS

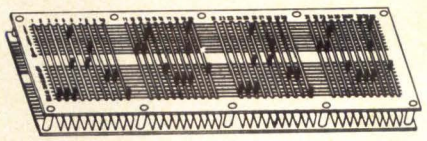
DATA GENERATOR

Data simulation capabilities of a new book-size data generator include bit rates to 10 MHz, easily expanded 16-bit cycle lengths, continuous or command recycle, variable baseline offset to ±10V, and 1V-10V data output amplitude. Any pulse generator may be used as a clock for NRZ formated outputs. Any asynchronously gated pulse generator may be used as a clock source for RZ formats. The new Model 201 data generator is identical in size to the company's Model 101 pulse generator. A 201/101 combination provides a 10 MHz RZ/NRZ data simulation system for under $1100.00 with variable width and delay to 10 ms and rise times to 5 ns. The two units require only 3½" of rack panel height. Datapulse, Inc., Inglewood, Cal.

Circle No. 231 on Inquiry Card

SELECTOR SWITCH

New crossbar selector switch is said to offer important advantages to builders of equipment with rapid program changing requirements. Such equipment might include collators, sorters, and data processing machines. According to the manufacturer, the switch is easier to operate than rotary switches, and it offers higher density than either pinboards or rotaries. Other advan-



tages claimed for the unit are its high reliability and extremely low cost of installation in multiple circuit situations. The Model C10-04A is a 4-module, basic-type switch in which 40 crossbar slider rails and 20 rhodium-plated printed circuit strips form 800 crosspoints. Variations can be provided to meet specific electrical and mechanical requirements. Cherry Electrical Products Corp., Highland Park, Ill.

Circle No. 203 on Inquiry Card

COMMUNICATION TRANSCEIVER

A new communication transceiver weighs less than 5 lbs and provides the capability to operate a Teletype or similar device as a portable remote computer terminal. Designated the Audio Magnetic Data Transceiver, the terminal may be used to communicate with a computer connected through a data set from any location where an ordinary telephone is available. The transceiver is connected to the Teletype by an interface adaptor. By simply dialing the number of the computer from the telephone and placing the telephone handset on the transceiver, information can be transmitted to and from the terminal device and computer over standard telephone lines. Tymshare, Inc., Los Altos, Cal.

Circle No. 250 on Inquiry Card

CYLINDRICAL CONNECTORS

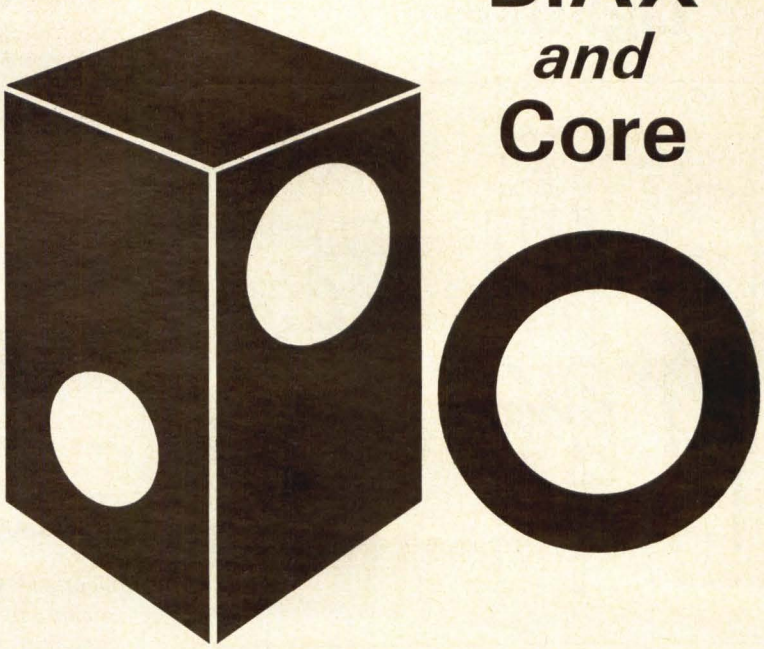
New line of high reliability, compact, miniature round connectors, was designed to meet the needs for reduced weight, higher temperature environments, and higher density. The new, lightweight connectors have short rugged pin contacts which are guided into closed-entry socket contacts, eliminating mismating. A complete line of termination hardware is also available. Burndy Corp., Norwalk, Conn.

Circle No. 240 on Inquiry Card

REED RELAYS

New line of reed relays is available in three standard and three miniature sizes. Features include individually supported reed switches to eliminate glass breakage with all coils wrapped with magnetic foil to minimize flux leakage. Reed switches are terminated to non-magnetic terminal stakes in the nylon bobbin, making it impossible to change operating characteristics when terminals are cut following soldering to printed circuit boards. All relays used rhodium plated contacts with high ampere turn switches. Automatic Controls Div., Cook Electric Co., Chicago, Ill.

Circle No. 226 on Inquiry Card



BIAX® and Core

Two ways to remember Raytheon Computer.

Raytheon Computer now makes DRO core memories as well as NDRO BIAX memories. The new 300 Memory System is a 900 nanosecond, 2½D core memory for large capacity, high-speed random access storage. Systems come in 8K and 16K modules with word lengths to 72 bits and are delivered complete with power supply and built-in self-tester. If you need an 8K or 16K memory with 28 bits or less, we can ship you a system in just a few weeks.

Since the first of this year, engineering sales representatives throughout the U.S. and Canada have been primed on both core and BIAX memories. If you'd like fast answers on prices, technical details and delivery, call any one of them today.

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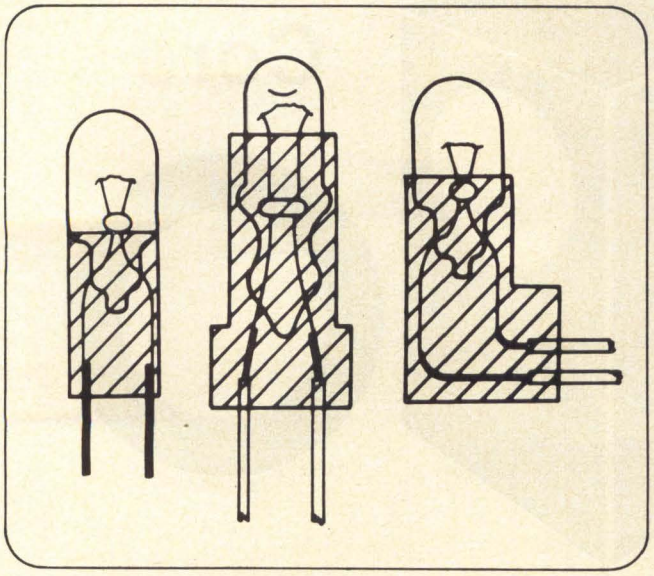
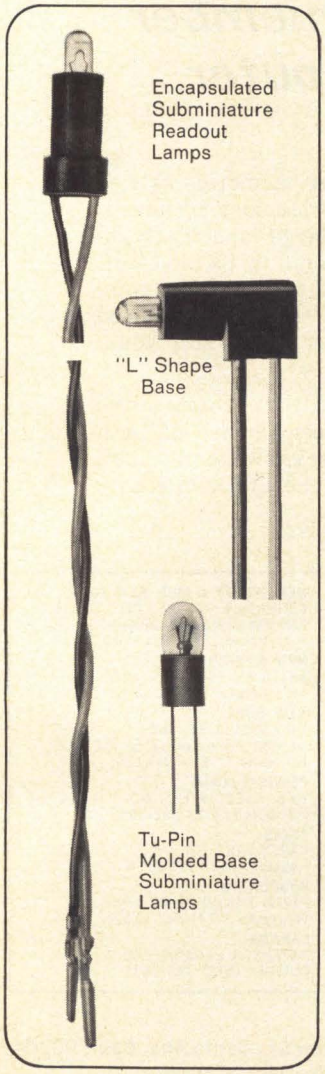
CIRCLE NO. 74 ON INQUIRY CARD

The idea here is economy in Instrumentation Lighting





Wherever small bulbs are used for instrument illumination or computer applications, equipment manufacturers will find economy in the Tung-Sol concept. If circuit board type of mounting is practicable, Tung-Sol molded base lamps can provide high reliability with real manufacturing economy. No mounting receptacle is required so you don't have that cost. In addition, the Tung-Sol molded base lamp is more reliable because it completely eliminates the usual cemented-on metal, or plastic base. Installation is as simple as soldering in a semiconductor. In fact, the Tung-Sol Tu-Pin lamp can be applied by automated equipment. Tung-Sol can also mold bases to special configurations and can harness to your specifications. Let's discuss your application in the design stage. Chances are we can save you even more on your assembly costs. Try us. Tung-Sol Division, Wagner Electric Corporation, One Summer Ave., Newark, N.J. 07104.

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MOLDED BASE SUBMINIATURE LAMPS

CIRCLE NO. 75 ON INQUIRY CARD

NEW PRODUCTS

COMPUTER TAPE TESTER

New Magnetic tape tester was designed for users of the new generation of 3200 fci (1600 bpi) computer tape. The Model 3200 in a single pass operation checks the tape in accordance with quality standards chosen for the specific installation or application. The total surface of the tape is tested using nine overlapping tracks in the IBM 5+4 array. Flaws are indicated on a counter and on a circular graphic recorder. Built-in cleaning devices upgrade the tape quality prior to testing. A convenient illuminated work station is provided for visual inspection and manual repair of tape flaws. The modes of operation include: evaluation, rehabilitation, and certification. General Kinetics Inc., Arlington, Va.

Circle No. 279 on Inquiry Card

CHIP CAPACITORS

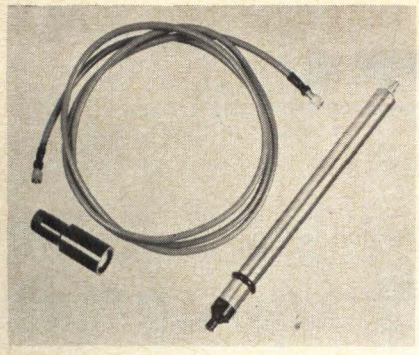
Designed for use in hybrid and integrated circuits and encapsulation in capacitor bodies, multilayer ceramic capacitor elements offer a capacitance of 5 picofarads to 1 microfarad. These chips are composed of up to 40 layers of high "K" ceramic dielectric and platinum electrodes. They are available in square and rectangular configurations and 10 basic sizes. Volumetric efficiency of 70 uf per cubic inch with a temperature stability of $\pm 13\%$ over a range of -55 to $+150°C$ is standard. They carry a voltage rating of 50 to 200 Vdc. Ultronix, Inc., Grand Junction, Colo.

Circle No. 291 on Inquiry Card

FLAT-PACK VOLTAGE REGULATORS

A new line of series regulators offers regulated output voltages from 6 to 24 volts. Models are operable from any available type of source and usable both as point-of-load voltage regulators fed by a remote common source or as integral components of single- or multiple-output master supplies. These modules are solid-state, encapsulated flat-pack units with over-all measurements of 1.25 inches wide, 1.5 inches long, and 0.6 inches thick. An integral copper heat sink enables effective dissipation of internally-generated heat in a variety of ways. The module may be mounted on a PC board with the sink exposed to free air or a metal fin may be bolted to the sink for increased dissipation or the module may be mounted in firm contact with a chassis, finned sink, or cold plate to achieve the maximum rated dissipation of 25 watts. This power rating represents the product of the voltage "stored" across the regulator, and the load current. The storage value may vary widely since these regulators are designed to accommodate broad ranges of input voltages (as much as five times the regulated output voltage). Trio Laboratories, Inc., Plainview, N. Y.

Circle No. 285 on Inquiry Card



LIGHT PEN

High resolution, high sensitivity, light pen uses a phototransistor as the light sensing element. A fiber optic bundle usually employed in such devices has been eliminated. Elimination of the fiber optics, according to the manufacturer, has resulted in a unit which is much lighter in weight, has a lighter weight cable, has greater sensitivity, has a broader spectral response, does not require high voltages for a photomultiplier, and minimizes operator fatigue. The new light pen also features a touch-sensitive actuator which, unlike the usual mechanical shutter or microswitch, has no moving parts. In order to permit the unit to see light, the operator has only to touch a metallic band placed where the index finger falls naturally during operation. Abacus Div., Information Control Corp., El Segundo, Cal.

Circle No. 248 on Inquiry Card

MINIATURE PCB RETAINERS

Designed for integrated circuit boards and for applications where space is at a premium, a new printed circuit board retainer uses only 1/8" (maximum) of board height while providing the spring retention and shock protection qualities of a standard-size retainer. Board spacing as close as 1/4" is possible; design provides minimum impedance to air flow. Retainers are available for 1/32" and 1/16" boards, in lengths from 1" to 6", in 1/2" increments. Standard material is beryllium copper. Retainers mount easily in card files with two 0.067" rivets. The Birtcher Corp., Industrial Div., Monterey Park, Cal.

Circle No. 235 on Inquiry Card

Monitor is a prime source for integrated circuit logic cards.

We want to sell you fewer of them.

Fewer than you'd need if you used competitive logic cards. We've taken a sensible, systems approach to logic card design. As a result, our Monilogic™ cards include related, auxiliary functions that would normally require additional cards. (Built-in gating and storage registers in our D-to-A converters, for example.) The benefits of this approach are obvious in the considerable savings you realize. Fewer cards mean savings in space, savings in money.

We've taken the only sensible way out of the DTL-TTL thicket, too. We're producing both types and, furthermore, they're compatible with each other. Regardless of your preference, we can supply you from stock. And you save still more money (about 40%) now that both types are available with dual in-line IC packages. Of course, we still have a broad line of cards with flat-pack devices. (We happen to have the most comprehensive line of logic circuit cards available today: over 140 different compatible types at last count.)

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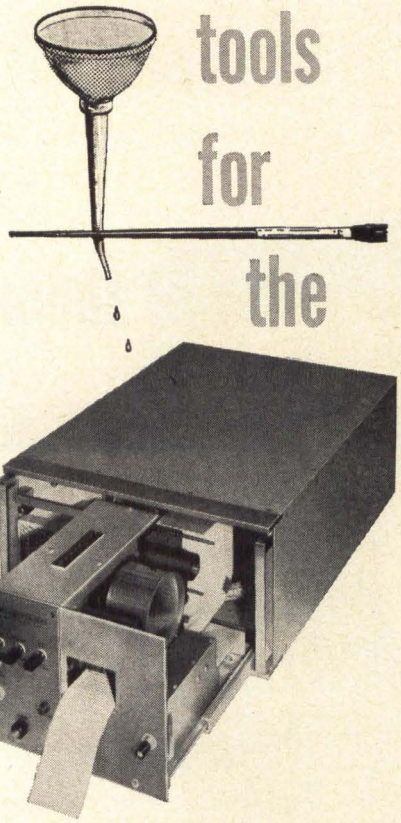

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LITERATURE

Data Display System

An 8-page technically-oriented brochure discusses the operation of a cathode ray tube display system. A general as well as a complete technical description is included, as are complete specifications and lists of applications and operating advantages. Laboratory For Electronics, Inc., Boston, Mass.

Circle No. 324 on Inquiry Card

Computer Handbook

Unique 544-page handbook details a small computer product line. The handbook contains detailed material on computer fundamentals and programming examples and three user manuals fully describing the company's family of scientific/engineering computers. Digital Equipment Corp., Maynard, Mass.

Circle No. 325 on Inquiry Card

Core Memory System

Bulletin describes line of core memory systems which exhibit cycle times of 0.6 μsec. to 1.0 μsec. The bulletin includes a block diagram of the system, a system timing diagram, complete electrical and mechanical specifications, and a list of optional features. Burroughs Corp., Electronic Components Div., Plainfield, N. J.

Circle No. 323 on Inquiry Card

Terminals/Connectors

Bare insulated, insulation grip miniature terminals, connectors, and specialty products for electronic applications for wires, ranging from No. 22 and up, are detailed in a 12-page catalog. The color-coded pages provide charted dimension information on 31 items. Crescent Insulated Wire and Cable Co., Trenton, N. J.

Circle No. 322 on Inquiry Card

Analog-To-Digital Converter

Bulletin describes a versatile high-speed analog-to-digital converter providing digitizing rates to 50 KHz. Unipolar or bipolar models are available with input ranges to 10.0 volts unipolar or $\pm$10.0 volts bipolar. Output word structure can be binary or BCD limited to 15 bit binary or 17 bits BCD. Serial code ouput from the Model 521 provides data transfer as each bit of the digital word is generated, therefore, eliminating unnecessary delay when working in real-time applications. Systems Engrg. Labs., Fort Lauderdale, Florida.

Circle No. 300 on Inquiry Card

RTL Logic

A comprehensive summary of mW resistor-transistor logic includes system design rules. Information is also given on noise margins, propagation delay, and power consumptions, along with a description of various RTL circuit applications. Sprague Electric Co., North Adams, Mass.

Circle No. 303 on Inquiry Card

Component Catalog

A 25-page catalog offers a ready reference to plugs, jacks, switches, connectors, molded cable assemblies, adapters, and audio accessories available for off-the-shelf delivery at factory prices. Switchcraft, Inc., Chicago, Ill.

Circle No. 306 on Inquiry Card

Static Power Converters

A 6-page bulletin includes information on high power rectifier inverters, cycloconverters, direct digital control for precise positioning, vehicular drive systems, and static nonbreak continuous ac power supplies. The Louis Allis Co., Milwaukee, Wis.

Circle No. 302 on Inquiry Card

Cooling Systems

A 24-page catalog details seven specific series of RFI-shieldable cabinet cooling blowers. Standard blower systems shown have capacities from 200 to 1200 cfm and fit standard 19″ racks. Catalog contains listing of applicable military and federal specifications, photos and dimensional drawings of the units, mechanical and electrical specs, and air delivery curves for each series. Technical engineering data with characteristic curves for blower selection, noise level, and horsepower requirements are included. Zero Manufacturing Co., Burbank, Calif.

Circle No. 328 on Inquiry Card

Interconnection System

An 8-page bulletin describes a modular interconnection concept for perpendicular or parallel stacking of printed circuit boards. The system involves posts and receptacles with a multi-selection of contact spacings to maximize packaging flexibility. The receptacle utilizes a two-beam contact concept providing wide mouth entry to permit unusually wide post-to-receptacle alignment tolerance, and featuring low insertion forces with anti-overstress protection. The receptacle contacts are adaptable to automatic machine clinching for attachment to printed wiring boards in selective groupings at rates up to 1800 per hour. Receptacle designs are available to provide crimp-type "snap-in" contacts for individual wires, coaxial cable, and flat flexible cable. This feature is accommodated with a high-contact pressure to insure low-contact resistance. Male posts are 0.031″ x 0.062″ x 0.022″ x 0.036″ or 0.025″ square and may be staked directly to printed wiring assemblies or used with nylon housings supported in metal or plastic panels. A special post is available for staking directly to metal panels for grounding. The modular interconnection system is provided with center-to-center contact spacing of 0.100, 0.125, and 0.156. Spacing on the free standing receptacles and posts can be anything greater than 0.100. Amp Inc., Harrisburg, Penna.

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CIRCLE NO. 78 ON INQUIRY CARD

LITERATURE

Automated Data Systems

A recent development in multiplex data handling technology — an automatic computer-controlled data processing system (analog, FM, and time multiplex) — is discussed in an informative 16-page booklet. Intended primarily for aerospace telemetry applications, the automated system also can perform as a flexible checkout system, simulation system, and in real-time data processing and control applications. The system combines a central processor unit and modular telemetry processor units which can be programmed and controlled by the CPU or operated manually. Under program control telemetry system setup, operation, checkout, calibration, and preventive maintenance are performed automatically. Electro-Mechanical Research, Inc., Princeton, N. J.

Circle No. 331 on Inquiry Card

Digital-To-Analog Converters

An 8-page brochure describes a series of multi-channel (up to 512 channels) digital-to-analog converters with word lengths from 8 to 15 bits and full scale accuracies of $\pm 0.05\%$ and $\pm 0.01\%$. Brochure includes complete specifications, description of operation, input/output circuit characteristics, model identification tables with description of options, and mechanical dimensions. Redcor Corp., Canoga Park, Cal.

Circle No. 326 on Inquiry Card

Pulse Transformers

A 6-page brochure discusses definitions, measurements, and specifications of pulse transformer parameters. This explanation of the fundamentals of transformer design includes diagrams. Contemporary Electronics, Minn., Minn.

Circle No. 330 on Inquiry Card

Data Transmission Set

An 8-page bulletin covers a new data set for transmission of serial binary data over microwave or leased lines at speeds up to 1800 bits per second. The publication describes the equipment and gives details on its operating characteristics. General Electric Communication Products Dept., Lynchburg, Va.

Circle No. 316 on Inquiry Card

IC Logic Cards

A 4-page brochure includes information on sixty different IC logic cards, including several additions to the line, as well as power supplies, card files, card drawers, accessory parts, an automatic module tester, and an "experimenter" for breadboarding up to a ten-card system. Also included is a discount schedule and other ordering information. Wyle Laboratories, El Segundo, Cal.

Circle No. 318 on Inquiry Card

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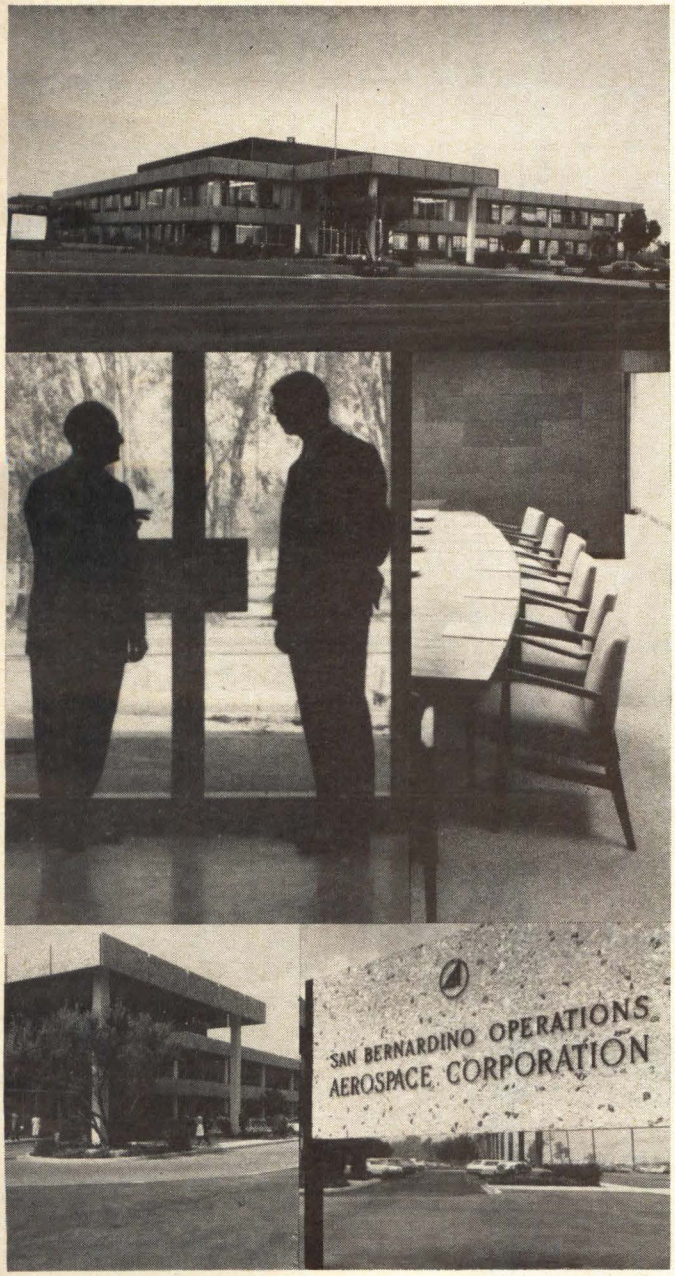

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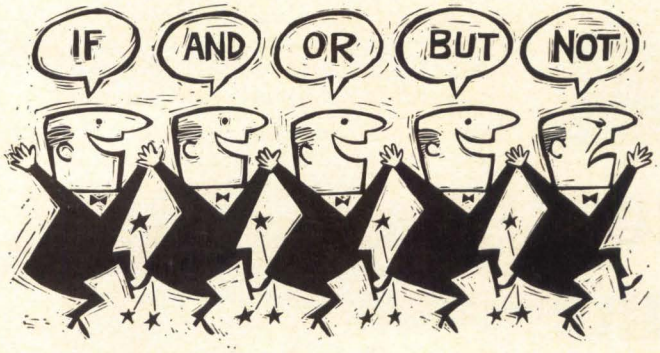

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LITERATURE

Computer Motors

An 8-page publication describes a new line of dc-servo motors for use in EDP peripheral equipment. The motors are said to meet the need for instant response with inertial time constants low as one millisecond and torque-to-inertia ratios approaching 350,000 rad/sec^2. Units were designed for use in equipment such as magnetic tape transports, memory disc packs, card readers, high-speed printers, and document handlers. Illustrated bulletin contains design and application information, performance charts and graphs, speed-torque curves, and ordering information. Bulletin also provides information on computer cooling fan assemblies. General Electric Co., Fort Wayne, Ind.

Circle No. 309 on Inquiry Card

Data Modem

A two-page bulletin and technical specification is available on a new data modem specifically developed to transmit 2400 bits per second on unconditioned voice-grade, schedule 4 telephone lines. The new model requires only 800 Hz of the available bandwidth of the telephone line channel. It is said to eliminate the need for special line conditioning and to allow additional data to be transmitted simultaneously over the remaining bandwidth. Milgo Electronic Corp., Miami, Florida.

Circle No. 312 on Inquiry Card

Magnetic Tape

A 6-page brochure describes a precision computer tape made especially for new high-speed computers. The brochure includes specifications, microphotographs, profilometer readings, charts on durability and drop-out activity, and a description of Tensaflex, a new backing material. Memorex Corporation, Santa Clara, Cal.

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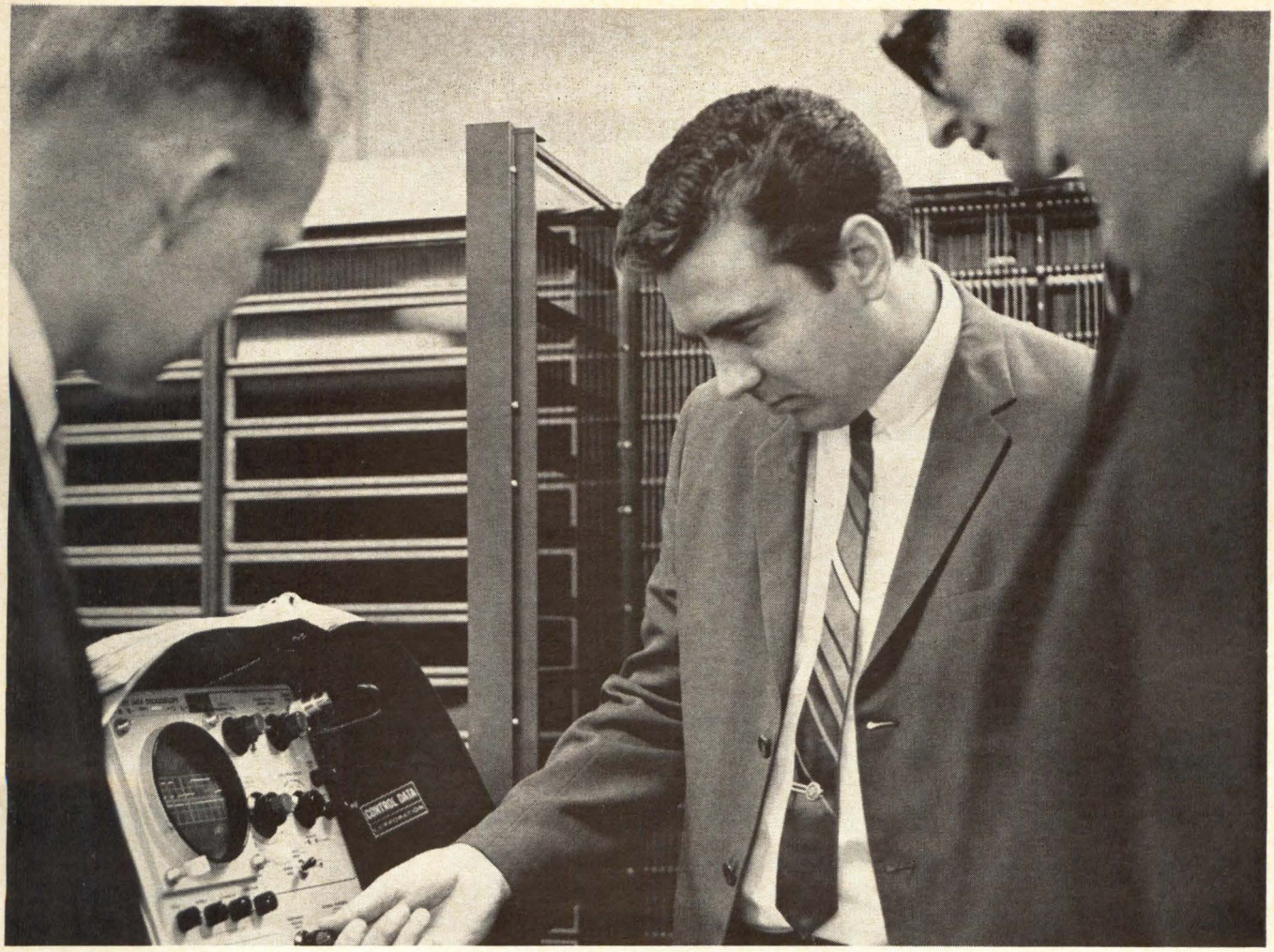

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Circle No. 319 on Inquiry Card

Integrated Circuit Handbook

An integrated circuit data handbook contains complete specifications, performance data and application information for high level TTL circuits. The handbook features several new series on gates, flip-flops, and memory cells in standard and high speed classifications for both industrial and military parameters. The new handbook, priced at $15.00, will be provided to all qualified recipients. Transitron Electronic Corporation, Wakefield, Mass.

Circle No. 327 on Inquiry Card

Indicator Lights

A complete line of one- and two-terminal edge lighting assemblies is described in an 8-page catalog. These indicator lights are designed to emit light through a colored filter radially into the plastic plate. Included are descriptions, data and ordering information for one- and two-terminal assemblies conforming to MS25010 — Revision D. Also detailed are inset lens top indicator lights, and dimming and non-dimming indicators with extended neck to pass through MIL-P-7788 panels. Dialight Corp., Brooklyn, N. Y.

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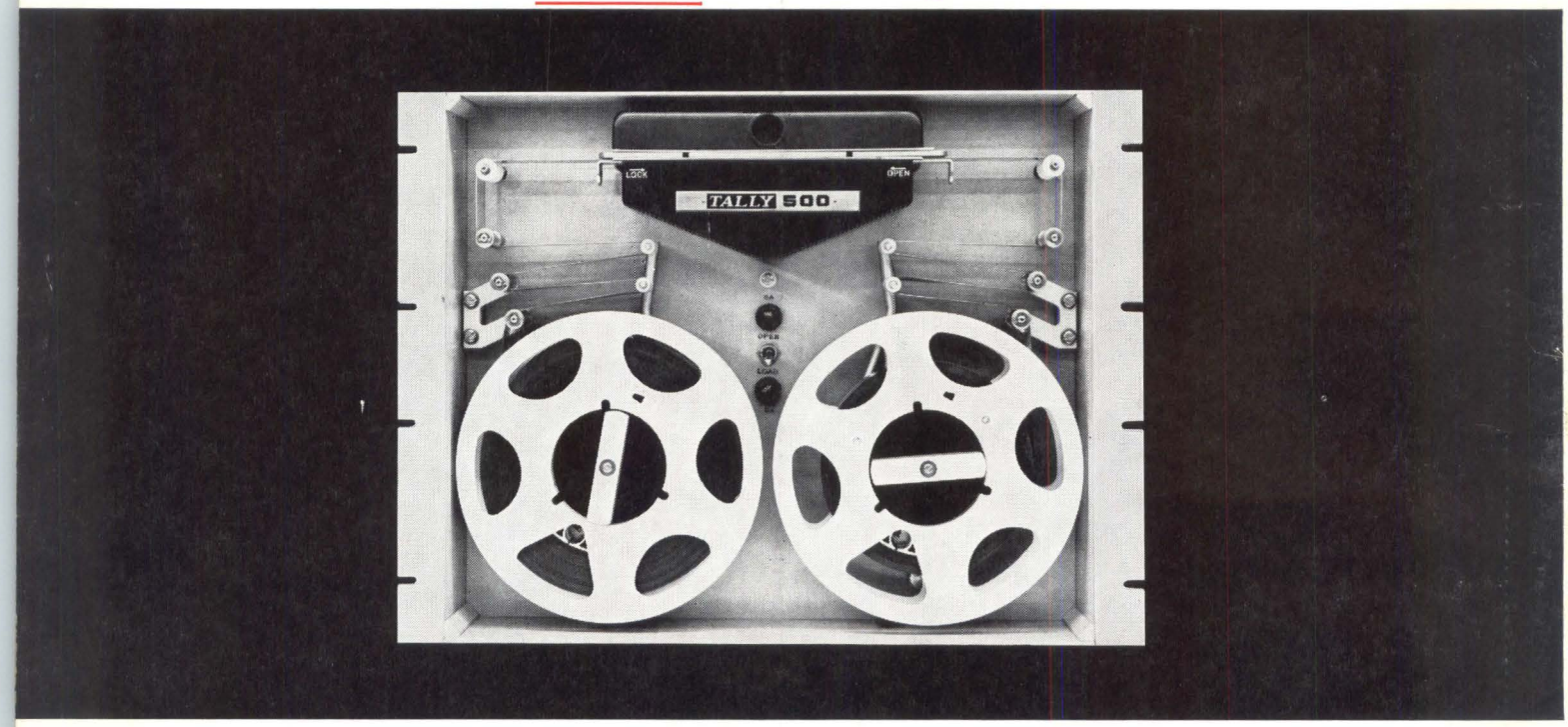

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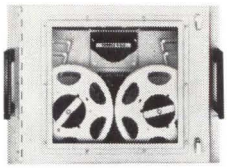
MIL-SPEC reader, Model 500RM and "ruggedized" reader, Model 500RF/10

Fully militarized, the Model 500RM is the first high speed reader that meets all applicable military specifications without exception. Featuring the same basic design as other Series 500 photoelectric readers, this unit will work in environments of −40°F to +145°F, in humidities of 100%, and take more than 15 g's shock. Pertinent RFI specs are met. MTBF is 5,000 hours. Expected life is 10,000 hours minimum.

Where severe environmental conditions are not encountered, the Model 500 RF/10 will perform with the same accuracy and life for about half the cost. Reading speeds for both readers are 150 char/sec asynchronously, 500 char/sec synchronously, and 1000 char/sec wind/search.



Model 500 RM

Full disclosure. For all the facts, call your full service Tally sales engineer (see EEM), or write Ken Crawford, Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. In the U.K. and Europe, address Tally Europe, Ltd., Radnor House, 1272 London Road, London, S.W. 16, England.

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