S7100

Version 1.0f

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Before you begin…

Check the box contents!

The retail motherboard package should contain the following:

	1 x S7100 Motherboard
	1 x Rear IO shielding
	1 x S7100 Quick Installation Guide
	1 x TYAN® Driver CD
	2 x SATA Single Cable
	CPU clip for Narrow Non-Fabric CPU Carrier x 2

IMPORTANT NOTE:
Sales sample may not come with the accessory listed above. Please contact your sales representative to help order accessory for your evaluation.

Chapter 1: Instruction

1.1 Congratulations

You have purchased the powerful TYAN® S7100 motherboard, based on the Intel® C621 chipset. The S7100 is designed to support Intel® Xeon® Scalable Processor Families, and Up to 384GB RDIMM/ 768GB LRDIMM/ 1,536GB RDIMM 3DS/LRDIMM 3DS 2666MHz / DDR4 memory. Leveraging advanced technology from Intel®, the S7100 is capable of offering scalable 32 and 64-bit computing, high-bandwidth memory design, and lightning-fast PCI-E bus implementation.

The S7100 not only empowers you in today's demanding IT environment but also offers a smooth path for future application upgradeability. All of these rich feature sets provide the S7100 with the power and flexibility to meet demanding requirements for today's IT environments.

Remember to visit the TYAN® website at **http://www.tyan.com**. There you can find all the information on all TYAN® products as well as all the supporting documentation, FAQs, Drivers and BIOS upgrades.

1.2 Hardware Specifications

S7100GM2NR

Processor	**Socket Type / Q'ty**	LGA3647/ (2)
	Supported CPU Series	Intel Xeon Scalable Processor Family
	Thermal Design Power (TDP) wattage	Max up to 205W
Chipset	**PCH**	Intel C621
Memory	**Supported DIMM Qty**	(6)+(6) DIMM slots
	DIMM Type / Speed	DDR4 RDIMM/RDIMM 3DS/LRDIMM/LRDIMM 3DS 2666
	Capacity	Up to 384GB RDIMM/ 768GB LRDIMM/ 1,536GB RDIMM 3DS/LRDIMM 3DS *Follow latest Intel DDR4 Memory POR
	Memory channel	6 Channels per CPU
	Memory voltage	1.2V
Expansion Slots	**PCI-E**	(4) PCI-E Gen3 x16 slots, (3) PCI-E Gen3 x8 slots

	Others:		(2) PCI-E Gen3 x4 for M.2 socket (2242/2260/2280)
LAN	**Port Q'ty**		(2) GbE ports (1) port shared with IPMI)
	Controller		Intel I350-AM2
Storage	**SATA**	**Connector**	(2) Mini-SAS HD (8-ports)
		Controller	Intel C621
		Speed	6.0 Gb/s
		RAID	RAID 0/1/10/5 (Intel RSTe)
	M.2 connector		(1) M.2 connector (2242) by PCI-E interface / (1) M.2 connector (2242/2260/2280) by PCI-E interface
	sSATA	**Connector**	(1) Mini-SAS HD (4-ports) + (2) SATA-III / SATADOM (sSATA Port4, sSATA Port5)
		Controller	Intel C621
		Speed	6.0 Gb/s
		RAID	RAID 0/1/10/5 (Intel RSTe) only for 4 SATA devices
Graphic	**Connector type**		D-Sub 15-pin
	Resolution		Up to 1920x1200
	Chipset		Aspeed AST2500
Input /Output	**USB**		(3) USB 2.0 ports (2 via cable, 1 TYPE-A), (6) USB 3.0 ports (4 at rear, 2 via cable)
	COM		(1) header
	RJ-45		(2) GbE ports
	Front Panel		(1) 2 x 5 header
	SATA		(2) SATA-III connectors + (3) Mini-SAS HD (4-in-1) connectors
	Power		ATX 24 pin + (2) 8-pin power connectors
	Others		(1) ID button
TPM (Optional)	**TPM Support**		Please refer to our TPM supported list.
System Monitoring	**Chipset**		Aspeed AST2500
	Fan		Total (6) 4-pin headers
	Temperature		Monitors temperature for CPU &

		memory & system environment
	Voltage	Monitors voltage for CPU, memory, chipset & power supply
	LED	Over temperature warning indicator, Fan & PSU fail LED indicator
	Others	Watchdog timer support
Server Management	**AST2500 iKVM Feature**	IPMI 2.0 compliant baseboard management controller (BMC), Supports storage over IP and remote platform-flash, USB 2.0 virtual hub
	AST2500 IPMI Feature	24-bit high quality video compression, 10/100/1000 Mb/s MAC interface
BIOS	**Brand / ROM size**	AMI, 32MB
	Feature	PXE boot support, ACPI 5.0, SMBIOS 3.0/PnP/Wake on LAN, ACPI sleeping states S3,S4,S5, User-configurable H/W monitoring
Physical Dimension	**Form Factor**	SSI EEB
	Board Dimension	12"x13" (305x330mm)
Regulation	**FCC (DoC)**	Class B
	CE (DoC)	Yes
Operating Environment	**Operating Temp.**	10° C ~ 35° C (50° F~ 95° F)
	Non-operating Temp.	- 40° C ~ 70° C (-40° F ~ 158° F)
	In/Non-operating Humidity	90%, non-condensing at 35° C
RoHS	**RoHS 6/6 Compliant**	Yes
Operating System	**OS supported list**	Please refer to our Intel OS supported list.
Package Contains	**Motherboard**	(1) S7100 Motherboard
	Manual	(1) Web User's manual, (1) Quick Installation Guide
	Installation CD	(1) TYAN installation CD

S7100AG2NR

Processor	**Socket Type / Q'ty**		LGA3647/ (2)
	Supported CPU Series		Intel Xeon Scalable Processor Families
	Thermal Design Power (TDP) wattage		Max up to 205W
Chipset	**PCH**		Intel C621
Memory	**Supported DIMM Qty**		(6)+(6) DIMM slots
	DIMM Type / Speed		DDR4 RDIMM/RDIMM 3DS/LRDIMM/LRDIMM 3DS 2666
	Capacity		Up to 384GB RDIMM/ 768GB LRDIMM/ 1,536GB RDIMM 3DS/LRDIMM 3DS *Follow latest Intel DDR4 Memory POR
	Memory channel		6 Channels per CPU
	Memory voltage		1.2V
Expansion Slots	**PCI-E**		(4) PCI-E Gen3 x16 slots, (3) PCI-E Gen3 x8 slots
	Others:		(2) PCI-E Gen3 x4 for M.2 socket (2242/2260/2280)
LAN	**Port Q'ty**		(2) GbE ports
	Controller		Intel I350-AM2
Storage	**SATA**	**Connector**	(2) Mini-SAS HD (8-ports)
		Controller	Intel C621
		Speed	6.0 Gb/s
		RAID	RAID 0/1/10/5 (IntelRSTe)
	M.2 connector		(1) M.2 connector (2242) by PCI-E interface / (1) M.2 connector (2242/2260/2280) by PCI-E interface
	sSATA	**Connector**	(1) Mini-SAS HD (4-ports) + (2) SATA-III / SATADOM (sSATA Port4, sSATA Port5)
		Controller	Intel C621
		Speed	6.0 Gb/s
		RAID	RAID 0/1/10/5 (Intel RSTe) only for 4 SATA devices
Graphic	**Connector type**		D-Sub 15-pin

	Resolution	Up to 1920x1200
	Chipset	Aspeed AST2510
Audio	**Chipset**	Realtek ALC892-GR
	Feature	High Definition Audio, 7.1 ch
Input /Output	**USB**	(3) USB 2.0 ports (2 via cable, 1 TYPE-A), (6) USB 3.0 ports (4 at rear, 2 via cable)
	COM	(1) header
	RJ-45	(2) GbE ports
	Front Panel	(1) 2 x 5 header
	SATA	(2) SATA-III connectors + (3) Mini-SAS HD (4-in-1) connectors
	Power	ATX 24 pin + (2) 8-pin power connectors
	Others	(1) ID button
TPM (Optional)	**TPM Support**	Please refer to our TPM supported list.
System Monitoring	**Chipset**	Aspeed AST2510
	Fan	Total (6) 4-pin headers
	Temperature	Monitors temperature for CPU & memory & system environment
	Voltage	Monitors voltage for CPU, memory, chipset & power supply
	LED	Over temperature warning indicator, Fan & PSU fail LED indicator
	Others	Watchdog timer support
BIOS	**Brand / ROM size**	AMI, 32MB
	Feature	PXE boot support, ACPI 5.0, SMBIOS 3.0/PnP/Wake on LAN, ACPI sleeping states S3,S4,S5, User-configurable H/W monitoring
Physical Dimension	**Form Factor**	SSI EEB
	Board Dimension	12"x13" (305x330mm)
Regulation	**FCC (DoC)**	Class B
	CE (DoC)	Yes
Operating Environment	**Operating Temp.**	10° C ~ 35° C (50° F~ 95° F)
	Non-operating Temp.	- 40° C ~ 70° C (-40° F ~ 158° F)
	In/Non-operating	90%, non-condensing at 35° C

	Humidity	
RoHS	**RoHS 6/6 Compliant**	Yes
Operating System	**OS supported list**	Please refer to our Intel OS supported list.
Package Contains	**Motherboard**	(1) S7100 Motherboard
	Manual	(1) Web User's manual, (1) Quick Installation Guide
	Installation CD	(1) TYAN installation CD

S7100AGM2NR-EX

Processor	**Q'ty / Socket Type**		(2) LGA3647
	Supported CPU Series		Intel Xeon Scalable Processor
	Thermal Design Power (TDP) Wattage		Max up to 205W
	System Bus		Up to 10.4/9.6 GT/s with Intel UltraPath Interconnect (UPI) support
Chipset	**PCH**		Intel C621
Memory	**Supported DIMM Qty**		(6)+(6) DIMM slots
	DIMM Type / Speed		DDR4 RDIMM/RDIMM 3DS/LRDIMM/LRDIMM 3DS 2666
	Capacity		Up to 384GB RDIMM/ 768GB LRDIMM/ 1,536GB RDIMM 3DS/LRDIMM 3DS *Follow latest Intel DDR4 Memory POR
	Memory channel		6 Channels per CPU
	Memory voltage		1.2V
Expansion Slots	**PCI-E**		(4) PCI-E Gen3 x16 slots, (3) PCI-E Gen3 x8 slots
LAN	**Q'ty / Port**		(2) GbE ports (1 port shared with IPMI)
	Controller		Intel I350-AM2
Storage	**SATA**	**Connector**	(2) Mini-SAS HD (8-ports)
		Controller	Intel C621
		Speed	6.0 Gb/s
		RAID	RAID 0/1/10/5 (Intel RSTe)

	sSATA	Connector	(2) SATA-DOM, (1) Mini-SAS HD (4-ports)
		Controller	Intel C621
		Speed	6.0 Gb/s
		RAID	RAID 0/1/10/5 (Intel RSTe)
	NVMe	Connector (M.2)	(1) 2242 (by PCI-E interface), (1) 2280/2260/2242 (by PCI-E interface)
Graphic	Connector type		D-Sub 15-pin
	Resolution		Up to 1920x1200
	Chipset		Aspeed AST2510
Audio	Chipset		Realtek ALC892-GR
	Feature		High Definition Audio, 7.1 ch
Input /Output	Others		(1) ID button
	USB		(3) USB 2.0 ports (2 via cable, 1 Type-A), (6) USB3.0 ports (4 at rear, 2 via cable)
	COM		(1) header
	VGA		(1) D-Sub 15-pin VGA port (at rear)
	RJ-45		(2) GbE ports
	Audio		(1) SPDIF OUT Connector, (1) 26-pin 7.1 ch HD Connector
	Front Panel		(1) 2 x 5 header
	SATA		(2) SATA/SATA-DOM connectors + (3) Mini-SAS (4-in-1) connectors
	Power		SSI 24-pin + 8-pin + 8-pin power connectors
TPM (Optional)	TPM Support		Please refer to our TPM supported list.
System Monitoring	Chipset		Aspeed AST2510
	Fan		Total (6) 4-pin headers
	Temperature		Monitors temperature for CPU & memory & system environment
	Voltage		Monitors voltage for CPU, memory, chipset & power supply
	LED		Over temperature warning indicator, Fan & PSU fail LED indicator

	Others	Watchdog timer support
Server Management	**AST2500 iKVM Feature**	IPMI 2.0 compliant baseboard management controller (BMC), Supports storage over IP and remote platform-flash, USB 2.0 virtual hub
	AST2500 IPMI Feature	24-bit high quality video compression, 10/100/1000 Mb/s MAC interface
BIOS	**Brand / ROM size**	AMI, 32MB
	Feature	Hardware Monitor, SMBIOS 3.0/PnP/Wake on LAN, Boot from USB device/PXE via LAN/Storage, User Configurable FAN PWM Duty Cycle, Console Redirection, ACPI sleeping states S4,S5, ACPI 6.1
Physical Dimension	**Form Factor**	SSI EEB
	Board Dimension	12"x13" (305x330mm)
Regulation	**FCC (DoC)**	Class B
	CE (DoC)	Class B
Operating Environment	**Operating Temp.**	0° C ~ 55° C (32° F~ 131° F)
	Non-operating Temp.	- 40° C ~ 70° C (-40° F ~ 158° F)
	In/Non-operating Humidity	90%, non-condensing at 35° C
RoHS	**RoHS 6/6 Compliant**	Yes
Operating System	**OS supported list**	Please refer to our AVL support lists.
Package Contains	**Motherboard**	(1) S7100 Motherboard
	Manual	(1) Quick Installation Guide
	Installation CD	(1) TYAN Device Driver CD

1.3 Software Specifications

For the latest AST2500 User's Guide and OS (operation system) support, please visit the Tyan's Web site at http://www.tyan.com for the latest information

Chapter 2: Board Installation

You are now ready to install your motherboard.

How to install our products right… the first time

The first thing you should do is read this user's manual. It contains important information that will make configuration and setup much easier. Here are some precautions you should take when installing your motherboard:

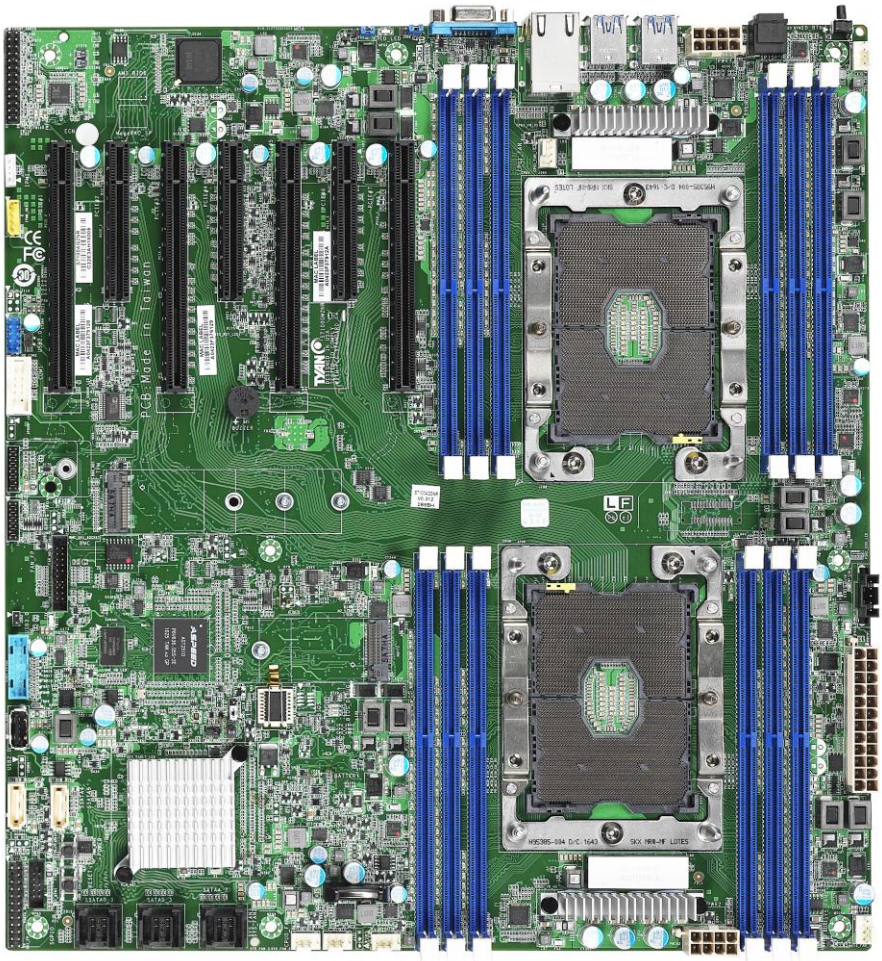
(1) Ground yourself properly before removing your motherboard from the antistatic bag. Unplug the power from your computer power supply and then touch a safely grounded object to release static charge (i.e. power supply case). For the safest conditions, MiTAC recommends wearing a static safety wrist strap.
(2) Hold the motherboard by its edges and do not touch the bottom of the board, or flex the board in any way.
(3) Avoid touching the motherboard components, IC chips, connectors, memory modules, and leads.
(4) Place the motherboard on a grounded antistatic surface or on the antistatic bag that the board was shipped in.
(5) Inspect the board for damage.

The following pages include details on how to install your motherboard into your chassis, as well as installing the processor, me
mory, disk drives and cables.

Caution!

1. To avoid damaging the motherboard and associated components, do not use torque force greater than 7kgf/cm (6.09 lb/in) on each mounting screw for motherboard installation.
2. Do not apply power to the board if it has been damaged.

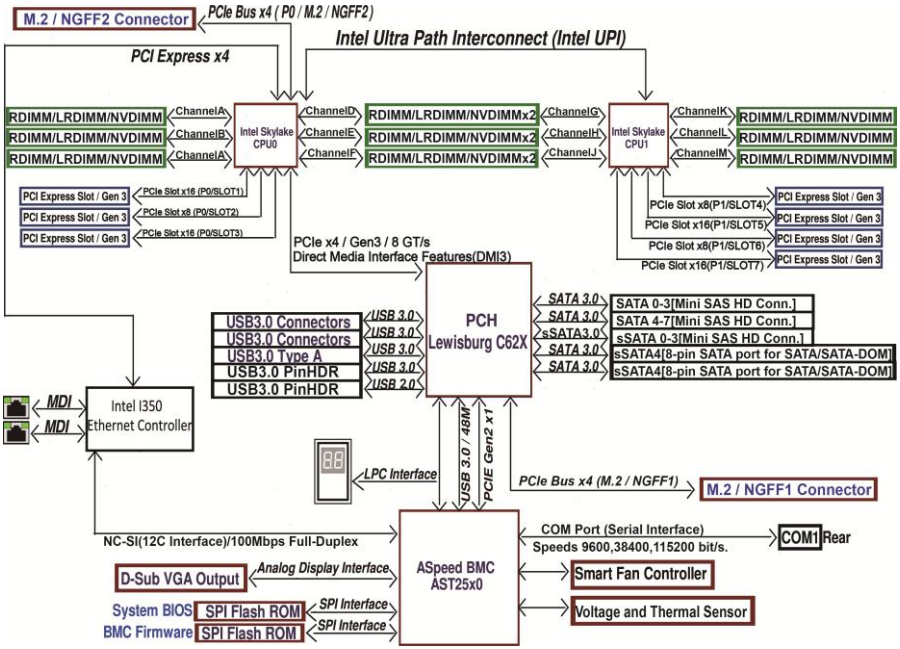
2.1 Board Image



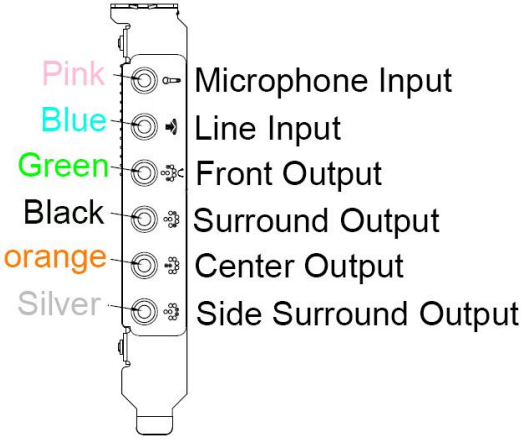
S7100

This picture is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above picture.

2.2 Block Diagram

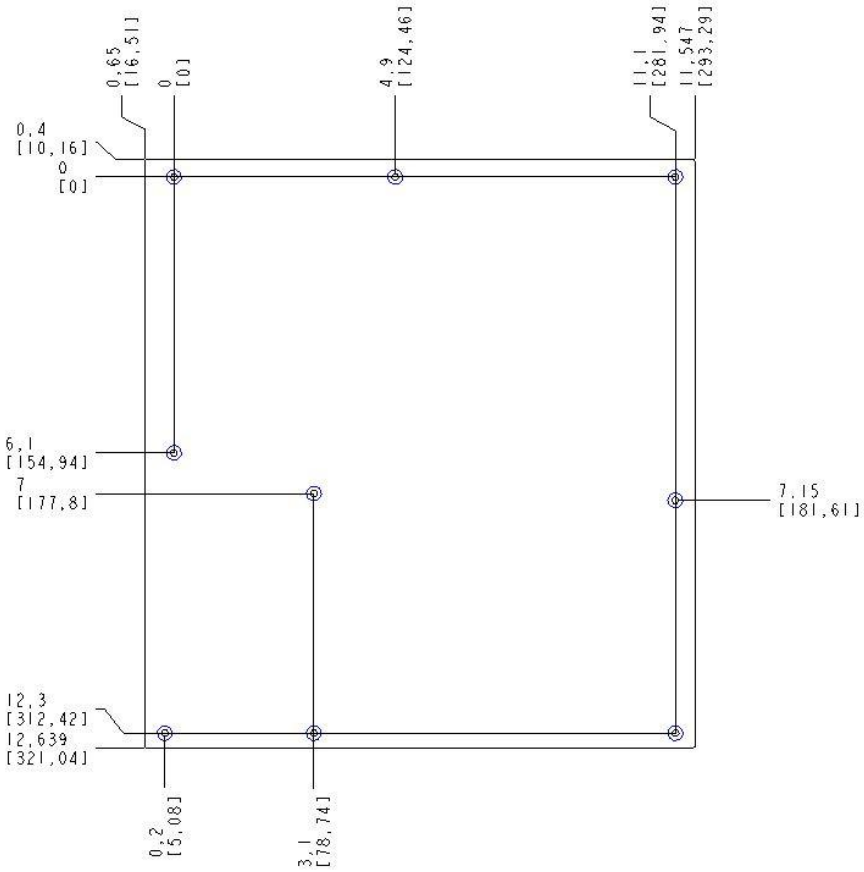


S7100 Block Diagram

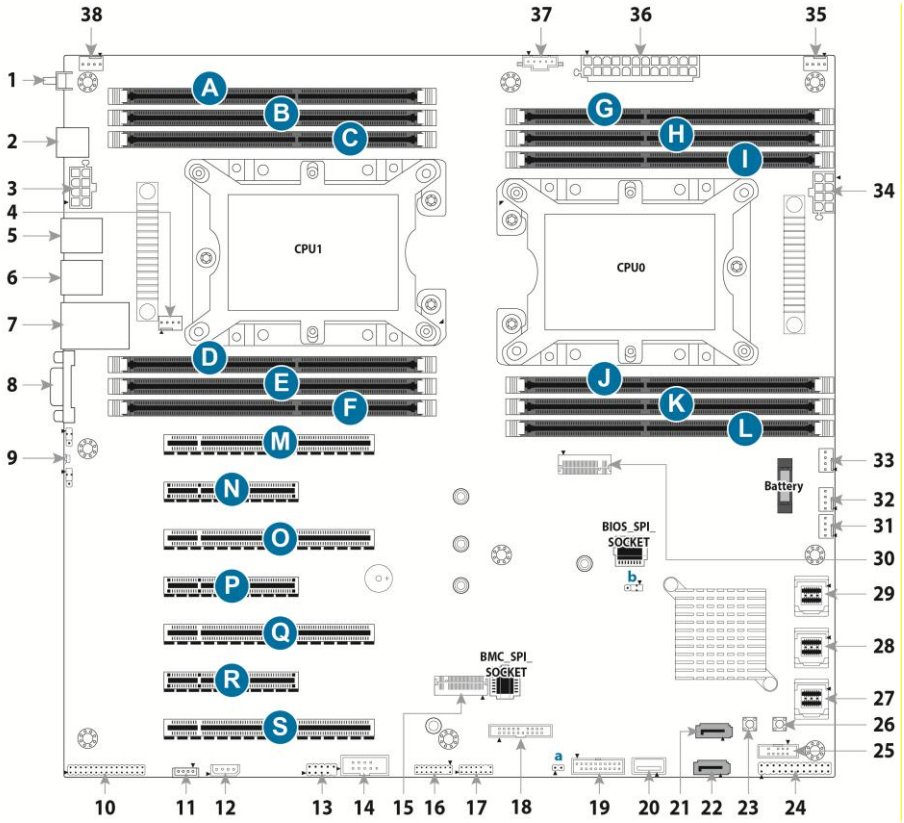


Audio Kit

2.3 Motherboard Mechanical Drawing



2.4 Board Parts, Jumpers and Connectors



This diagram is representative of the latest board revision available at the time of publishing. The board you receive may not look exactly like the above diagram. The DIMM slot numbers shown above can be used as a reference when reviewing the DIMM population guidelines shown later in the manual. For the latest board revision, please visit our web site at **http://www.tyan.com.**

Motherboard Components

Connectors	
1. Rear IDLED Button (ID LED_BTN1)	20. USB TYPEA Connector (TYPEA_USB2)
2. Audio-SPDIF OUT (J205)	21. sSATA: sSerial Advanced Technology Attachment Gen3 (SSATA5)
3. 8-pin Power Connector (PWCN2)	22. sSATA: sSerial Advanced Technology Attachment Gen3 (SSATA4)
4. CPU1 Fan Connector (CPU1_FAN)	23. System Power Button (PWR_BTN1)
5. Rear USB 3.0 x 2 (J125)	24. Front Panel Header (SSI_FP)
6 Rear USB 3.0 x 2 (J124)	25. SSATA SGPIO Header (SSATA_SGPIO)
7. LAN1& LAN2 (J123, RJ45)	26. System Reset Button (RST_BTN1)
8. Rear VGA Connector (VGA1)	27. sSATA: sSerial Advanced Technology Attachment Gen3 (SSATA0_3)
9. Rear ID LED (ID_LED)	28. SATA: Serial Advanced Technology Attachment Gen3 (SATA0-3)
10. Front Audio Header (FRONT_AUDIO)	29. SATA: Serial Advanced Technology Attachment Gen3 (SATA4-7)
11. VROC Header (J122)	30. M.2 Socket, TYPE 2242 (NGFF2)
12 IPMB Pin Header (IPMB_HD1)	31. System FAN Connector (SYS_FAN_3)
13. USB 2.0 Header (J43)	32. System FAN Connector (SYS_FAN_2)
14. COM2 Port Header (HD_COM2)	33. CPU FAN Connector (CPU0_FAN)
15. M.2 Socket, type 2242/2260/2280(NGFF1)	34. 8-pin Power Connector (PWCN3)
16. TYAN Module Header (DBG_HD1)	35.System Fan Connector(SYS_FAN_1)
17. VGA2 Header (VGA2)	36. 24-pin Power Connector (PWCN1)
18. System Fan Header (Fan_HD1)	37. PSMI Connector (SP_PSMI)
19. Front USB 3.0 Header (USB3_FPIO2)	38. System FAN Connector (SYS_FAN_4)
Jumpers	
a. INTRUDER Jumper (J202)	b. CLEAR CMOS Jumper (J104)
Slots	
A. CPU1 Memory Slot (CPU1_DIMM_F0)	B. CPU1 Memory Slot (CPU1_DIMM_E0)
C. CPU1 Memory Slot (CPU1_DIMM_D0)	D. CPU1 Memory Slot (CPU1_DIMM_A0)
E. CPU1 Memory Slot (CPU1_DIMM_B0)	F. CPU1 Memory Slot (CPU1_DIMM_C0)
G. CPU0 Memory Slot (CPU0_DIMM_C0)	H. CPU0 Memory Slot (CPU0_DIMM_B0)
I. CPU0 Memory Slot (CPU0_DIMM_A0)	J. CPU0 Memory Slot (CPU0_DIMM_D0)
K. CPU0 Memory Slot (CPU0_DIMM_E0)	L. CPU0 Memory Slot (CPU0_DIMM_F0)
M. PCI Express Gen 3 x16 (PCIE_7)	N. PCI Express Gen 3 x8 (PCIE_6)
O. PCI Express Gen 3 x16 (PCIE_5)	P. PCI Express Gen 3 x8 (PCIE_4)
Q. PCI Express Gen 3 x16 (PCIE_3)	R. PCI Express Gen 3 x8 (PCIE_2)
S. PCI Express Gen 3 x16 (PCIE_1)	

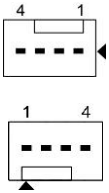
ID LED_BTN1: Rear IO IDLED Button

Signal	Pin	Pin	Signal
FP_IDLED_BTN_N	1	2	GND

TYPEA_USB2: Vertical (Type A) USB2.0 Connector

Pin	1	2	3	4
Signal	5V_AUX	USB_DN	USB_DP	GND

CPU0/1 FAN: 4-pin CPU Fan Connector

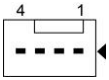


Pin	1	2	3	4
Signal	GND	VCC12	TACHOMETER	PWM

Use this header to connect the cooling fan to your motherboard to keep the system stable and reliable.

Note: A 4-pin fan is required for fan support 4pin Control

SYS FAN1~4: 4-pin FAN Connector

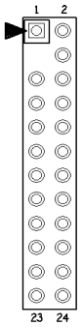


Pin	1	2	3	4
Signal	GND	VCC12	TACHOMETER	PWM

Use this header to connect the cooling fan to your motherboard to keep the system stable and reliable.

Note: A 4-pin fan without FAN speed Control

FPIO: Front Panel Header

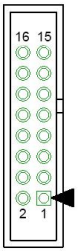


Signal	Pin	Pin	Signal
PW_LED+	1	2	FP_PWR
KEY	3	4	ID_LED+
PWR_LED	5	6	ID_LED-
HDD_LED+	7	8	FAULT_LED1-
HDD_LED-	9	10	FAULT_LED2-
PWR_SW#	11	12	LAN1 ACTLED+
GND1	13	14	LAN1_ACTLED-
RST_SW#	15	16	SMBDATA
GND2	17	18	SMBCLK
SYS_ID_SW#	19	20	INTRUSION#
TEMP SENSOR	21	22	LAN2_ACTLED+
NMI_SW#	23	24	LAN2_ACTLED-

FRONT_AUDIO: Front Audio Header

Signal	Pin	Pin	Signal
MIC_L	1	2	AGND
MIC_R	3	4	AUD_DETECT
LINE_R	5	6	MIC1_JD
FIO_SENSE	7	8	GND
LINE_L	9	10	LINE1_JD
FRONT_L	11	12	AGND
FRONT_R	13	14	FRONT_JD
SURR_R	15	16	AGND
SURR_L	17	18	SURR_JD
CENTEROUT_L	19	20	AGND
CENTEROUT_R	21	22	CENTEROUT_JD
SIDESURR_R	23	24	AGND
SIDESURR_L	25	26	SIDESURR_JD

DBG_HD1: TYAN Module Header

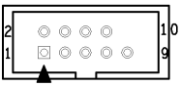


Signal	Pin	Pin	Signal
P3V3	1	2	FRAME_N
LAD0	3	4	KEY
LAD1	5	6	PLT_RST_N
LAD2	7	8	GND
LAD3	9	10	CLK_24M
DBG_SERIRQ	11	12	GND
DBG_PRES_N	13	14	VCC3_AUX
TPM_ADDR_MB	15	16	PCH_TPM_PP_EN

USB3_FPIO2: Front USB3.0 Header

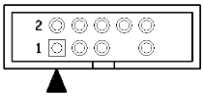
Signal	Pin	Pin	Signal
VCC1	1	2	P0_RX_N
P0_RX_P	3	4	GND1
P0_TX_N	5	6	P0_TX_P
GND2	7	8	P0_N
P0_P	9	10	OC_N
P1_P	11	12	USB_DN
GND3	13	14	P1_TX_P
P1_TX_N	15	16	GND4
P1_RX_P	17	18	P1_RX_N
VCC2	19	20	Key

HD_COM2: COM Header



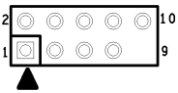
Signal	Pin	Pin	Signal
COM_DCD	1	2	COM_DSR
COM_RXD	3	4	COM_RTS
COM_TXD	5	6	COM_CTS
COM_DTR	7	8	COM_NRI
GND	9	10	KEY

SSATA_SGPIO: SSATA SGPIO Header



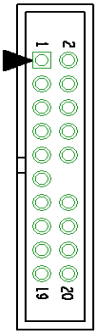
Signal	Pin	Pin	Signal
SMBCLK	1	2	SDATA IN
SMBDATA	3	4	SDATA OUT
GND	5	6	SLOAD
KEY	7	8	SCLOCK
VCC3_AUX	9	10	HD_ERROR_LED

J43: USB 2.0 Header



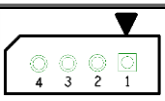
Signal	Pin	Pin	Signal
VCC1	1	2	VCC2
USB2_N	3	4	USB2_N
USB2_P	5	6	USB2_P
GND1	7	8	GND2
KEY	9	10	NC

FAN_HD1: System Fan Header



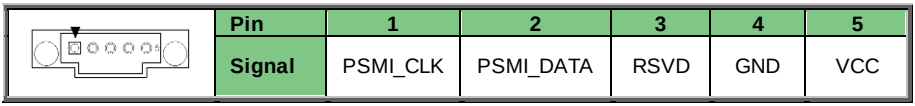
Signal	Pin	Pin	Signal
TACH1	1	2	TACH6
TACH2	3	4	TACH7
TACH3	5	6	TACH8
TACH4	7	8	TACH9
TACH5	9	10	TACH10
GND	11	12	KEY
PWM2	13	14	PWM1
TACH11	15	16	SMB_DATA
TACH12	17	18	SMB_CLK
VCC3_AUX	19	20	PWM3

IPMB_HD1: IPMB Pin Header



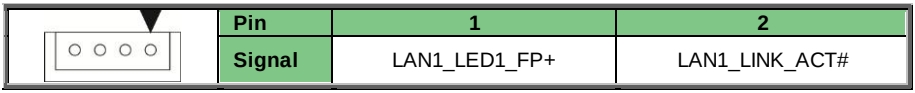
Signal	Pin	Pin	Signal
IPMB_DAT	1	2	GND1
IPMB_CLK	3	4	VCC

PSIM1: PSMI Connector



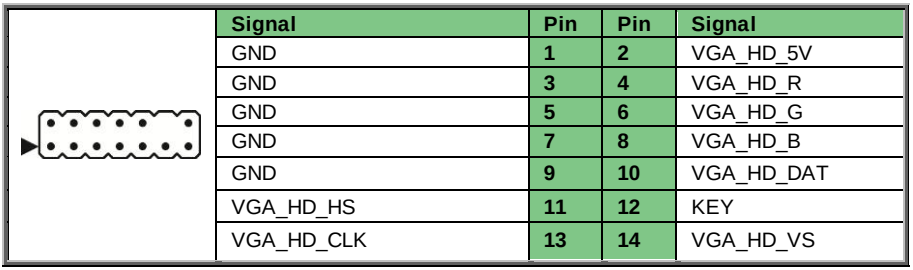
Pin	1	2	3	4	5
Signal	PSMI_CLK	PSMI_DATA	RSVD	GND	VCC

J122: VROC Header (HW Key for Intel VROC – NVMe only)



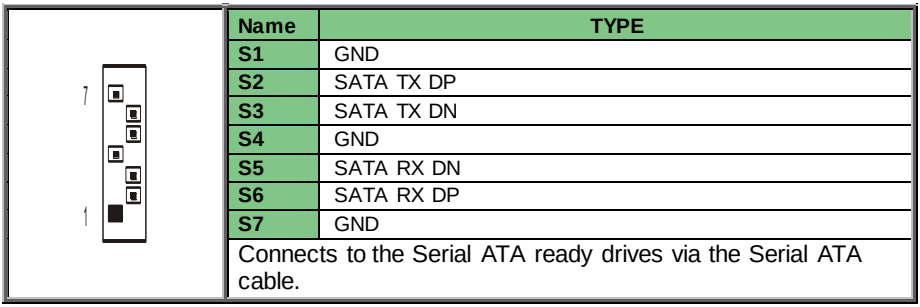
Pin	1	2
Signal	LAN1_LED1_FP+	LAN1_LINK_ACT#

VGA2: VGA2 Header



Signal	Pin	Pin	Signal
GND	1	2	VGA_HD_5V
GND	3	4	VGA_HD_R
GND	5	6	VGA_HD_G
GND	7	8	VGA_HD_B
GND	9	10	VGA_HD_DAT
VGA_HD_HS	11	12	KEY
VGA_HD_CLK	13	14	VGA_HD_VS

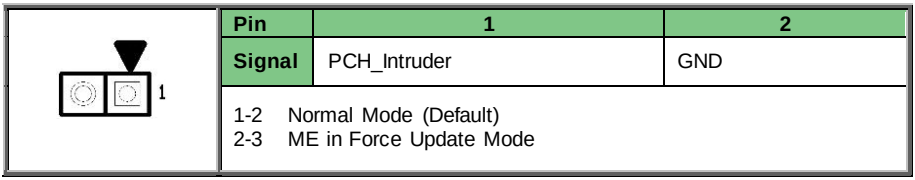
SSATA4/SSATA5: sSerial Advanced Technology Attachment Gen3(sSATA)



Name	TYPE
S1	GND
S2	SATA TX DP
S3	SATA TX DN
S4	GND
S5	SATA RX DN
S6	SATA RX DP
S7	GND

Connects to the Serial ATA ready drives via the Serial ATA cable.

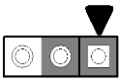
J202: INTRUDER Jumper



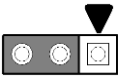
Pin	1	2
Signal	PCH_Intruder	GND

1-2 Normal Mode (Default)
2-3 ME in Force Update Mode

J104: Clear CMOS Jumper



Normal
(**Default**)



Clear CMOS

Pin	1	2	3
Signal	TP_RST_RTCRST_N	RST_RTCRST_N	PD_RST_RTCRST_N

1-2 Normal RTC Reset (DEFAULT)
2-3 Clear RTC Registers

You can reset the CMOS settings by using this jumper. This can be useful if you have forgotten your system/setup password, or need to clear the system BIOS setting.

1. Power off system and disconnect power connectors from the motherboard.
2. Remove the jumper from Pin_1 and Pin_2 (Default setting).
3. Move the jumper cap to close Pin_2 and Pin_3 for several seconds to Clear CMOS.
4. Put jumper cap back to Pin_1 and Pin_2 (Default setting).
5. Reconnect power connectors to the motherboard and power on system.

2.5 Installing the Processor and Heatsink

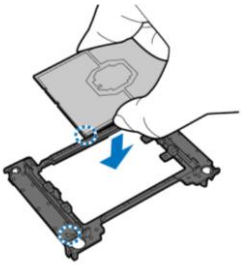
The types of processors supported by the S7100 are listed in the ***1.2 Hardware*** Specifications section on page 4. Check our website at **http://www.tyan.com** for the latest list of validated **Intel**® processors for this specific motherboard.

> **NOTE:** MiTAC is not liable for damage as a result of operating an unsupported configuration.

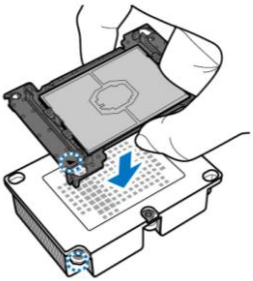
Processor Installation (Dual Socket P/ LGA3647 for Intel Skylake CPU)

Follow the steps below to install the processors and heat sinks.
Please note that the illustrations are based on LGA3647 socket which may not look exactly like the motherboard you purchased. Therefore, the illustrations should be held for your reference only.
NOTE: Please save and replace the flip CPU protection cap when returning for service.

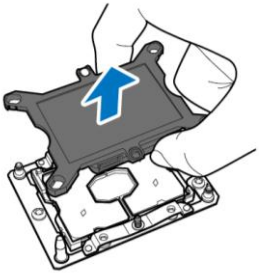
1. Align and install the processor on the carrier.



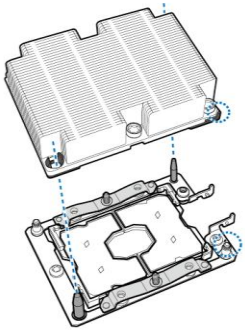
2. Carefully flip the heatsink. Then install the carrier assembly on the bottom of the heatsink and make sure the gold arrow is located in the correct direction.



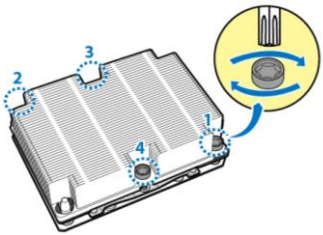
3. Remove the CPU cover. **NOTE: Save and replace the CPU cover if the processor is removed from its socket.**



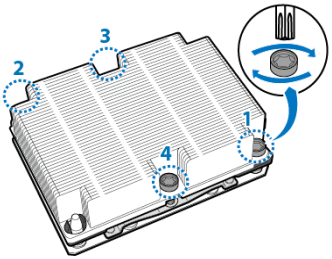
4. Align the heatsink with the CPU socket by the guide pins and make sure the gold arrow is located in the correct direction. Then place the heatsink onto the top of the CPU socket.



5. Align the heatsink by the guide pins and make sure the gold arrow is located in the correct direction. Then place the heatsink onto the top of the processor.

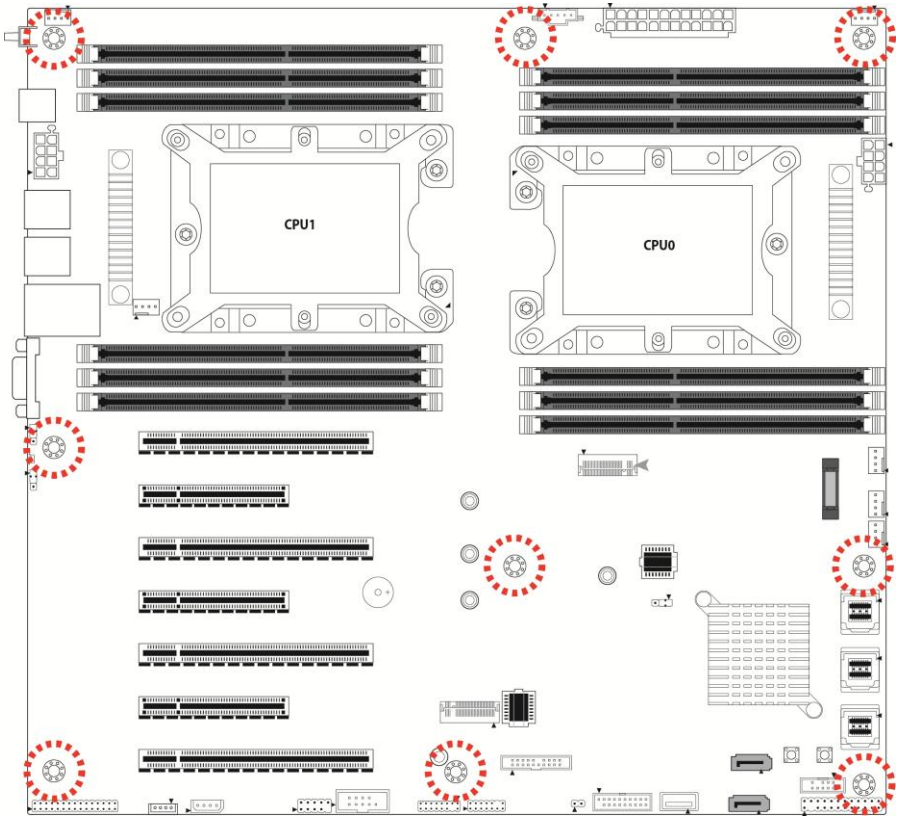


6. To secure the heatsink, use a Security T30 Security Torx to tighten the screws in a sequential order (1->2->3->4). When dissembling the heatsink, loosen the screws in reverse order (4->3->2->1).



2.6 Tips on Installing Motherboard in Chassis

Before installing your motherboard, make sure your chassis has the necessary motherboard support studs installed. These studs are usually metal and are gold in color. Usually, the chassis manufacturer will pre-install the support studs. If you are unsure of stud placement, simply lay the motherboard inside the chassis and align the screw holes of the motherboard to the studs inside the case. If there are any studs missing, you will know right away since the motherboard will not be able to be securely installed.

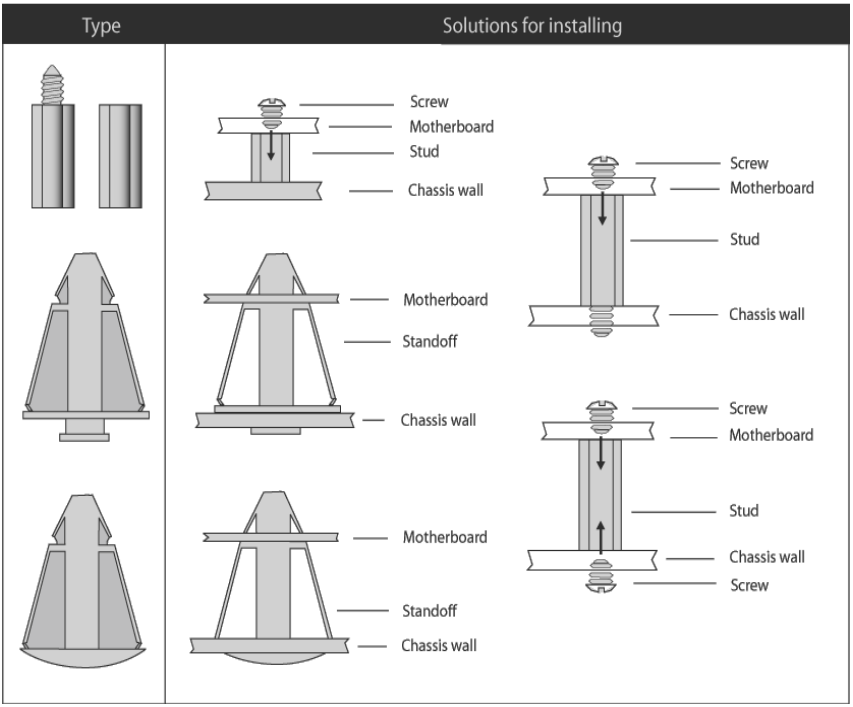


Note: Be especially careful to look for extra stand-offs. If there are any stand-offs present that are not aligned with a mounting hole on the motherboard, it will likely short components on the back of the motherboard when installed. This will cause malfunction and/or damage to your motherboard.

Some chassis include plastic studs instead of metal. Although the plastic studs are usable, MiTAC recommends using metal studs with screws that will fasten the motherboard more securely in place.

Below is a chart detailing what the most common motherboard studs look like and how they should be installed.

Mounting the Motherboard



2.7 Installing the Memory

Before installing memory, ensure that the memory you have is compatible with the motherboard and processor. Check the TYAN Web site at http://www.tyan.com for details of the type of memory recommended for your motherboard.

- Supports up to (6+6) R-DDR-4 up to 2666MHz memory
- Supports DDR4/DDR4LV/DDR4 LR and Apache Pass, need to link out all memory channel
- All installed memory will automatically be detected and no jumpers or settings need changing
- All memory must be of the **same type and density**

DDR4 Memory POR

Type	Ranks Per DIMM and Data Width	DIMM Capacity (GB)		Speed (MT/s); Voltage (V); Slots per Channel (SPC) & DIMMs per Channel (DPC)		
				1 Slot per Channel	2 Slots per Channel	
		DRAM Density		1DPC	1DPC	2DPC
		4Gb	8Gb	1.2V	1.2V	1.2V
RDIMM	SRx4	8GB	16GB	2666	2666	2666
RDIMM	SRx8	4GB	8GB			
RDIMM	DRx8	8GB	16GB			
RDIMM	DRx4	16GB	32GB			
RDIMM 3DS	QRx4	N/A	2H-64GB			
	8Rx4	N/A	4H-128GB			
LRDIMM	QRx4	32GB	64GB			
LRDIMM 3DS	QRx4	N/A	2H-64GB			
	8Rx4	N/A	4H-128GB			

Recommended Memory Population Table (Single CPU)

Quantity of memory installed	Single CPU Installed (CPU0 only)					
	1	2	3	4	5	6
P0_MCO_DIM_CH_A0	√	√	√	√	√	√
P0_MCO_DIM_CH_B0		√	√	√	√	√
P0_MCO_DIM_CH_C0			√	√	√	√
P0_MCO_DIM_CH_D0				√	√	√
P0_MCO_DIM_CH_E0					√	√
P0_MCO_DIM_CH_F0						√

NOTE: 1.√ indicates a populated DIMM slot.

2. Use paired memory installation for max performance.

3. Populate the same DIMM type in each channel, specifically

- Use the same DIMM size
- Use the same # of ranks per DIMM

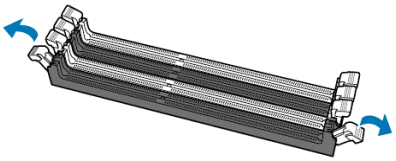
Recommended Memory Population Table (Dual CPU)

	Dual CPU installed (CPU0 and CPU1)					
Quantity of Memory installed	**2**	**4**	**6**	**8**	**10**	**12**
P0_MCO_DIM_CH_A0	√	√	√	√	√	√
P0_MCO_DIM_CH_B0		√	√	√	√	√
P0_MCO_DIM_CH_C0			√	√	√	√
P0_MCO_DIM_CH_D0				√	√	√
P0_MCO_DIM_CH_E0					√	√
P0_MCO_DIM_CH_F0						√
P1_MCO_DIM_CH_A0	√	√	√	√	√	√
P1_MCO_DIM_CH_B0		√	√	√	√	√
P1_MCO_DIM_CH_C0			√	√	√	√
P1_MCO_DIM_CH_D0				√	√	√
P1_MCO_DIM_CH_E0					√	√
P1_MCO_DIM_CH_F0						√

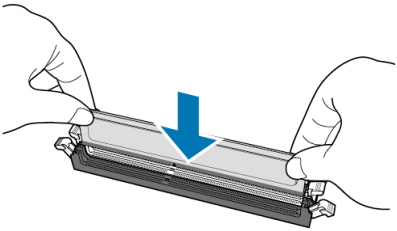
Memory Installation Procedure

Follow these instructions to install memory modules into the S7100.

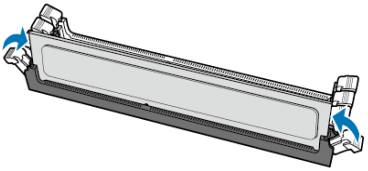
1. Unlock a DIMM socket by Press the retaining clip outwardly in the following illustration.



2. Align the memory module with the socket，such that the DIMM NOTCH match the KEY SLOT on the socket.



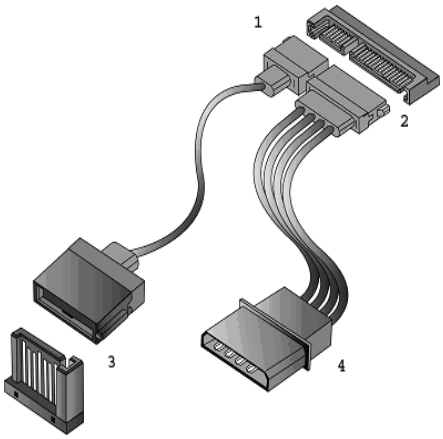
3. Seat the module firmly into the socket by gently pressing down until it sits flush with the socket. The locking levers pop up into place.



2.8 Attaching Drive Cables

Attaching SATA Cables

The following illustrates how to make a SATA Cable connection. If you are in need of SATA/SAS cables or power adapters please contact your local sales representative.



1. SATA drive cable connection

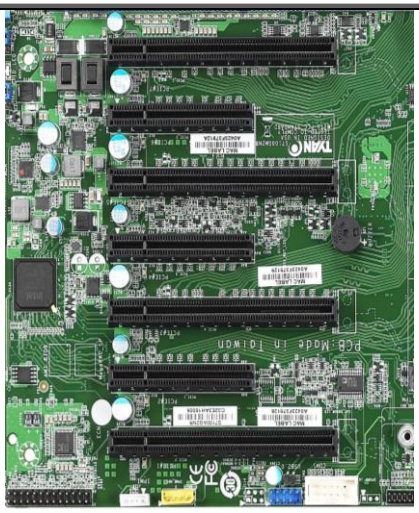
2. SATA drive power connection

3. SATA cable motherboard connector

4. SATA drive power adapter

2.9 Installing Add-In Cards

Before installing add-in cards, it's helpful to know if they are fully compatible with your motherboard. For this reason, we've provided the diagrams below, showing the slots that may appear on your motherboard.



1.Slot #7: PCI-E G3 x16 slot (x16 link) (f/ CPU1)
2.Slot #6: PCI-E G3 x8 slot (x8) (f/ CPU1) open-end type
3.Slot #5: PCI-E G3 x16 slot (x16 link) (f/ CPU1)
4.Slot #4: PCI-E G3 x8 slot (x8 link) (f/ CPU1) open-end type
5.Slot #3: PCI-E G3 x16 slot (x16 link) (f/ CPU0)
6.Slot #2: PCI-E G3 x8 slot (x8 link) (f/ CPU0) open-end type
7. Slot #1: PCI-E G3 x16 slot (x16 link) (f/ CPU0)

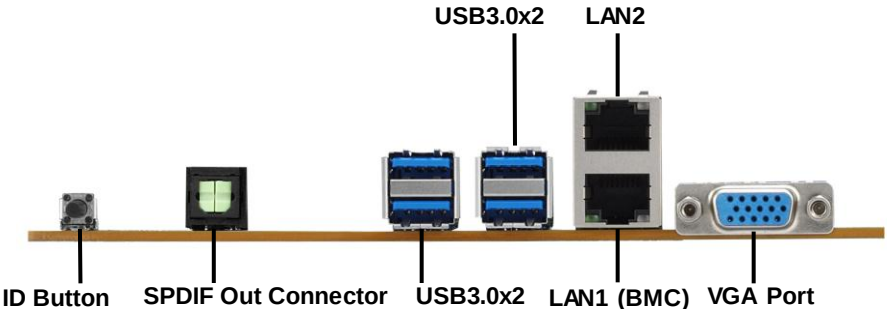
Simply find the appropriate slot for your add-in card and insert the card firmly. Do not force any add-in cards into any slots if they do not seat in place. It is better to try another slot or return the faulty card rather than damaging both the motherboard and the add-in card.

TIP: It's a good practice to install add-in cards in a staggered manner rather than making them directly adjacent to each other. Doing so allows air to circulate within the chassis more easily, thus improving cooling for all installed devices.

NOTE: You must always unplug the power connector from the motherboard before performing system hardware changes to avoid damaging the board or expansion device.

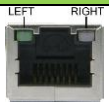
2.10 Connecting External Devices

Connecting external devices to the motherboard is an easy task. The motherboard supports a number of different interfaces through connecting peripherals. See the following diagrams for the details.



Onboard LAN LED Color Definition

The **two (2)** onboard Ethernet ports have green and yellow LEDs to indicate LAN status. The chart below illustrates the different LED states.

10/100/1000 Mbps LAN Link/Activity LED Scheme			
		**Left LED**	**Right LED**
10 Mbps	**Link**	Green	Off
	Active	Blinking Green	Off
100 Mbps	**Link**	Green	Green
	Active	Blinking Green	Green
1000 Mbps	**Link**	Green	Amber
	Active	Blinking Green	Amber
No Link		Off	Off

2.11 Installing the Power Supply

There are **Three (3)** power connectors on your S7100 motherboard. The S7100 supports EPS 12V power supply.

PWCN1: 24-Pin Power Connector

Signal	Pin	Pin	Signal
+3.3V_1	1	13	+3.3V_4
+3.3V_2	2	14	-12V
COM_1	3	15	COM_4
+5V_1	4	16	PS-ON#
COM_2	5	17	COM_5
+5V_2	6	18	COM_6
COM_3	7	19	COM_7
PWR_OK	8	20	RES
5VSB	9	21	+5V_3
+12V_1	10	22	+5V_4
+12V_2	11	23	+5V_5
+3.3V_3	12	24	COM_8

PWRCN2/CN3: ATX 8-pin Power Connector

Signal	Pin	Pin	Signal
COM_1	1	5	+12VDIG_1
COM_2	2	6	+12VDIG_2
COM_3	3	7	+12VDIG_3
COM_4	4	8	+12VDIG_4

2.12 Finishing Up

Congratulations on making it this far! You have finished setting up the hardware aspect of your computer. Before closing up your chassis, make sure that all cables and wires are connected properly, especially SATA cables and most importantly, jumpers. You may have difficulty powering on your system if the motherboard jumpers are not set correctly.

In the rare circumstance that you have experienced difficulty, you can find help by asking your vendor for assistance. If they are not available for assistance, please find setup information and documentation online at our website or by calling your vendor's support line.

Chapter 3: BIOS Setup

3.1 About the BIOS

The BIOS is the basic input/output system, the firmware on the motherboard that enables your hardware to interface with your software. The BIOS determines what a computer can do without accessing programs from a disk. The BIOS contains all the code required to control the keyboard, display screen, disk drives, serial communications, and a number of miscellaneous functions. This chapter describes the various BIOS settings that can be used to configure your system.

The BIOS section of this manual is subject to change without notice and is provided for reference purposes only. The settings and configurations of the BIOS are current at the time of print and are subject to change, and therefore may not match exactly what is displayed on screen.

This section describes the BIOS setup program. The setup program lets you modify basic configuration settings. The settings are then stored in a dedicated, battery-backed memory (called NVRAM) that retains the information even when the power is turned off.

To start the BIOS setup utility:

1. Turn on or reboot your system.
2. Press <**Del>** during POST to start the BIOS setup utility.

3.1.1 Setup Basics

The table below shows how to navigate in the setup program using the keyboard.

Key	Function
↑ ↓ →←	Move cursor
<Enter>	Execute command or select submenu
<->/<+>	Select the previous or next value/setting of the field
<ESC>	Exit current menu
<F1>	General help
<F2>	Previous values
<F3>	Load the Optimal default configuration values of the menu
<F4>	Save and exit
<PgUp> / <PgDn>	Move cursor to next/previous page

3.1.2 Getting Help

Pressing [**F1**] will display a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window, press [**ESC**] or the [**Enter**] key again.

3.1.3 In Case of Problems

If you have trouble booting your computer after making and saving the changes with the BIOS setup program, you can restart the computer by holding the power button down until the computer shuts off (usually within 4 seconds); resetting by pressing CTRL-ALT-DEL; or clearing the CMOS.
The best advice is to only alter settings that you thoroughly understand. In particular, do not change settings in the Chipset section unless you are absolutely sure of what you are doing. The Chipset defaults have been carefully chosen either by MiTAC or your system manufacturer for best performance and reliability. Even a seemingly small change to the Chipset setup options may cause the system to become unstable or unusable.

3.1.4 Setup Variations

Not all systems have the same BIOS setup layout or options. While the basic look and function of the BIOS setup remains more or less the same for most systems, the appearance of your Setup screen may differ from the charts shown in this section. Each system design and chipset combination requires a custom configuration. In addition, the final appearance of the Setup program depends on the system designer. Your system designer may decide that certain items should not be available for user configuration, and remove them from the BIOS setup program.

NOTE: The following pages provide the details of BIOS menu. Please be aware that the BIOS menus are continually changing due to continual BIOS updates over the product lifespan of the motherboard. The BIOS menus provided are current as of the date when this manual was written. Please visit TYAN's website at http://www.tyan.com for information on BIOS updates available for this specific motherboard.

3.2 Main Menu

In this section, you can alter general features such as the date and time.
Note that the options listed below are for options that can directly be changed within the Main Setup screen.

BIOS Information
It displays BIOS related information.

Platform Information
It displays Platform information.

Memory Information
This displays the total memory size.

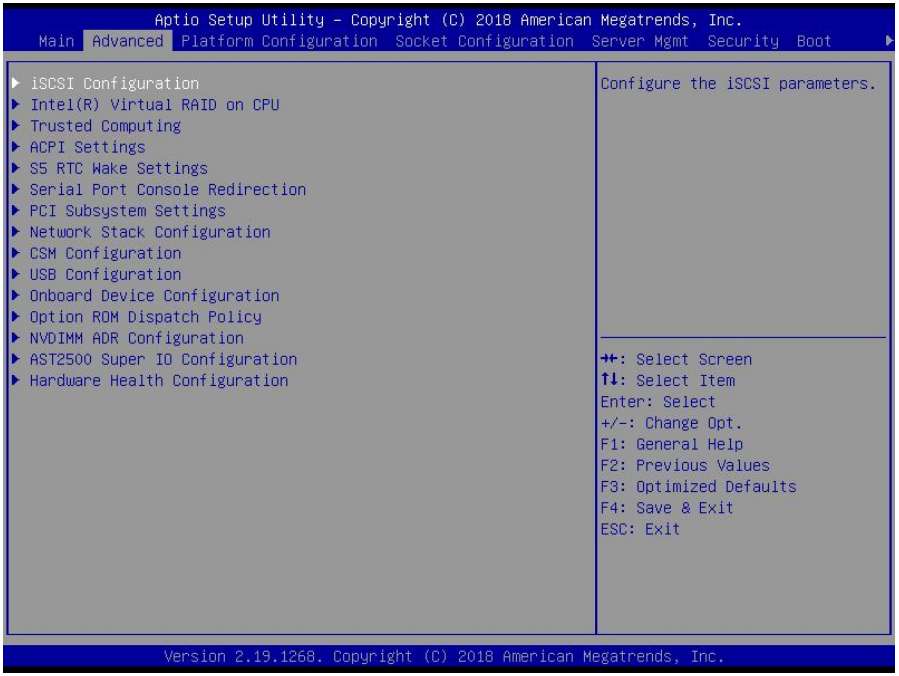
System Language
Choose the system default language.

System Date
Adjust the system date.
MM (Months): DD (Days): YYYY (Years)

System Time
Adjust the system clock.
HH (24 hours format): MM (Minutes): SS (Seconds)

3.3 Advanced Menu

This section facilitates configuring advanced BIOS options for your system.



iSCSI Configuration
Configure the iSCSI parameters

Intel® Virtual RAID on CPU
This formset allows the user to manage Intel® Virtual RAID on CPU

Trusted Computing
Trusted Computing settings.

ACPI Settings
System ACPI Parameters.

S5 RTC Wake Settings
Enable system to wake from S5 using RTC alarm

Serial Port Console Redirection
Serial Port Console Redirection

PCI Subsystem Settings
PCI, PCI-X and PCI Express Settings

Network Stack Configuration
Network Stack Setting

CSM Configuration
CSM Configuration: Enable/Disable Option ROM execution settings, etc

USB Configuration
USB Configuration Parameters.

Onboard Device Configuration
Onboard Device and Function Configuration.

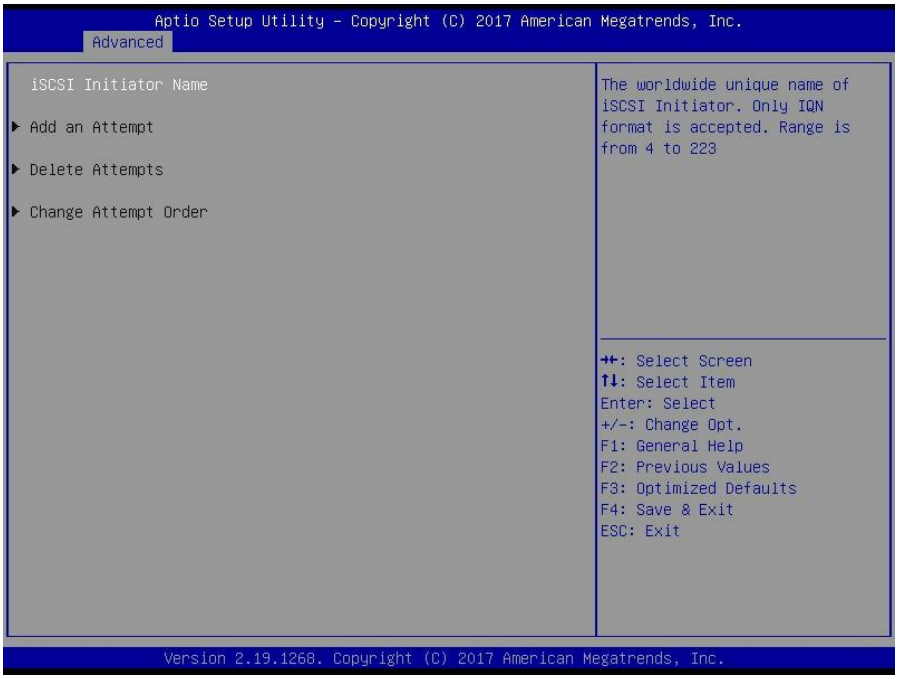
Option ROM Dispatch Policy
Option ROM Dispatch Policy

NVDIMM ADR Configuration
NVDIMM ADR Configuration

AST2500 Super IO Configuration
System Super IO Chip Parameters

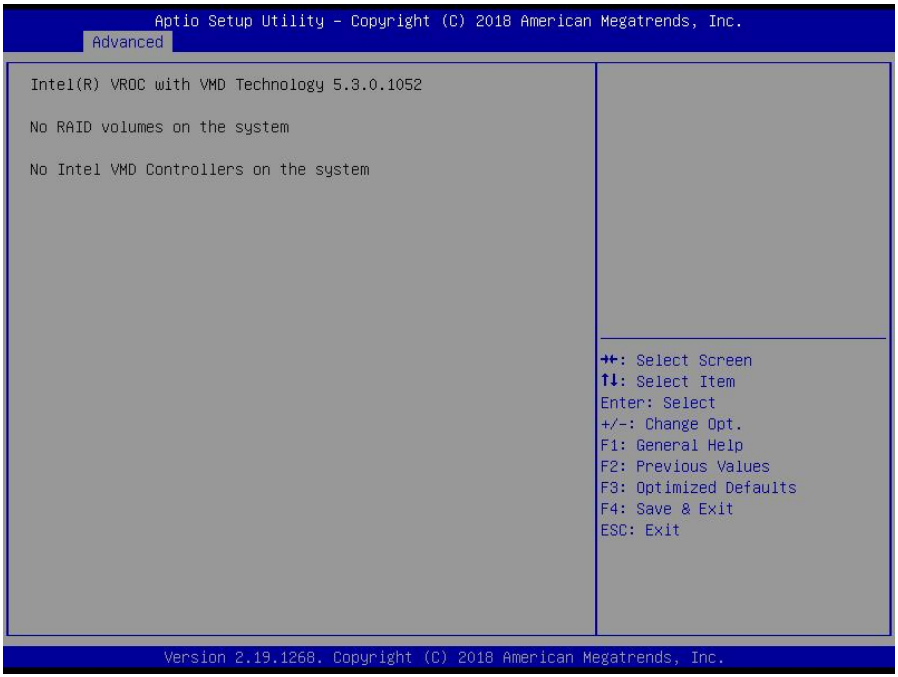
Hardware Health Configuration
Hardware Health Configuration

3.3.1 iSCSI Configuration



iSCSI Name
The worldwide unique name of iSCSI Initiator. Only IQN format is accepted. Range is from 4 to 223.

3.3.2 Intel(R) Virtual RAID on CPU



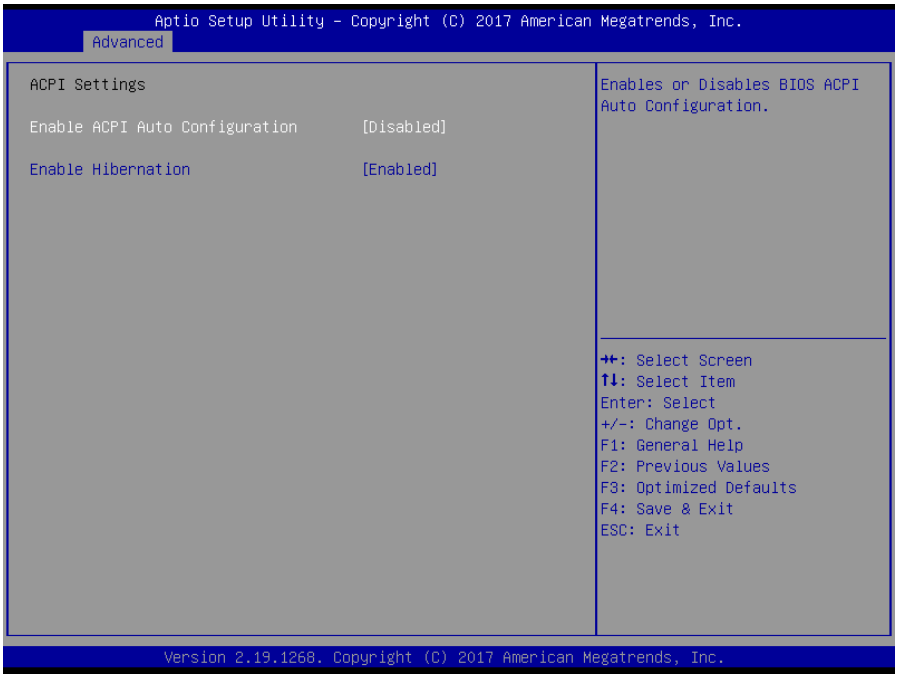
3.3.3 Trusted Computing

Security Device Support

Enable or disable BIOS support for security device. O.S. will not show Security device. TCG EFI protocol and INT1A interface will not be available.

Enabled **/ Disabled**

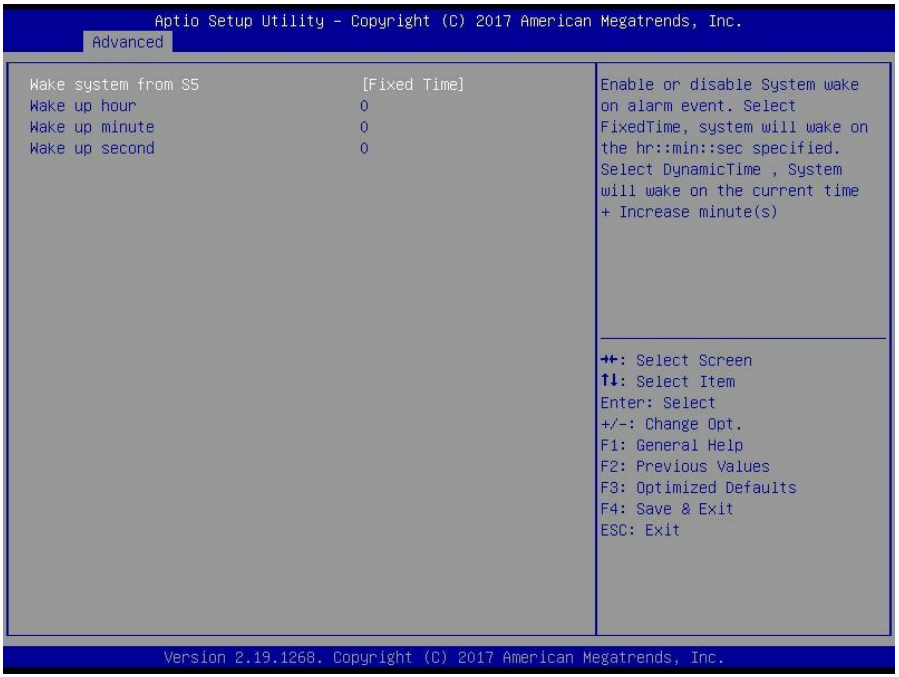
3.3.4 ACPI Settings



Enable ACPI Auto Configuration
Enables or Disables BIOS ACPI Auto Configuration
Disabled / Enabled

Enable Hibernation
Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may not be effective with some operation systems.
Disabled / **Enabled**

3.3.5 S5 RTC Wake Settings



Wake system from S5
Enable or disable system wake on alarm event. Select Fixed time, system will wake on the hr::min::sec specified. Select dynamic time, system will wake on the current time+ increase minute(s)

Disabled / Fixed time / Dynamic time

NOTE: When set **Wake system from S5** to **[Fixed Time]** the following menu will appear

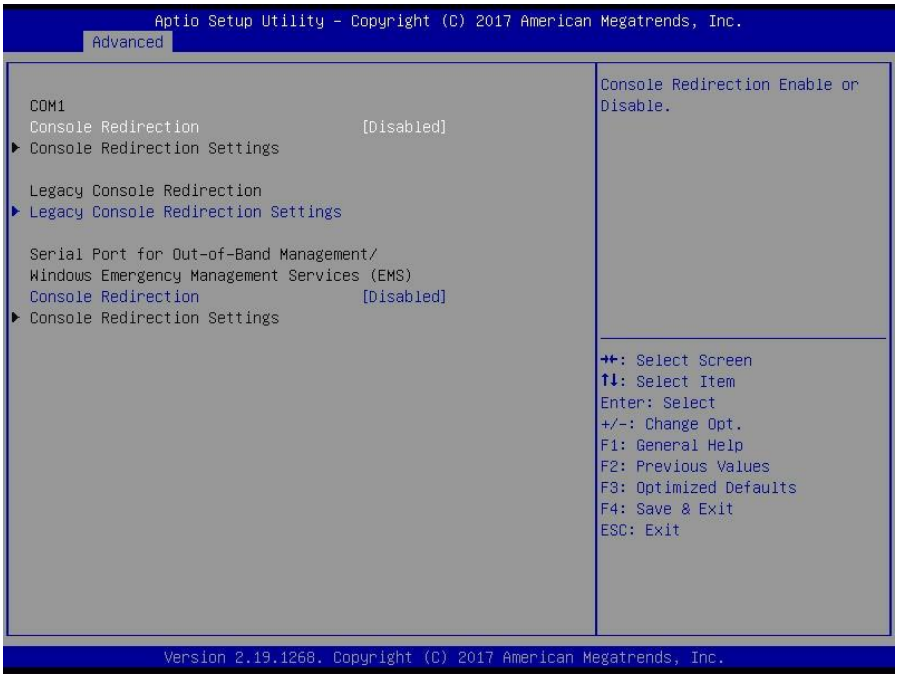
wake up hour
Select 0-23 for example enter 8 for 3am and 15 for 3pm

wake up minute
Select 0-59

wake up second
Select 0-59

NOTE: When set **Wake system from S5** to **[Dynamic Time]**
Wake up minute increase
1

3.3.6 Serial Port Console Redirection



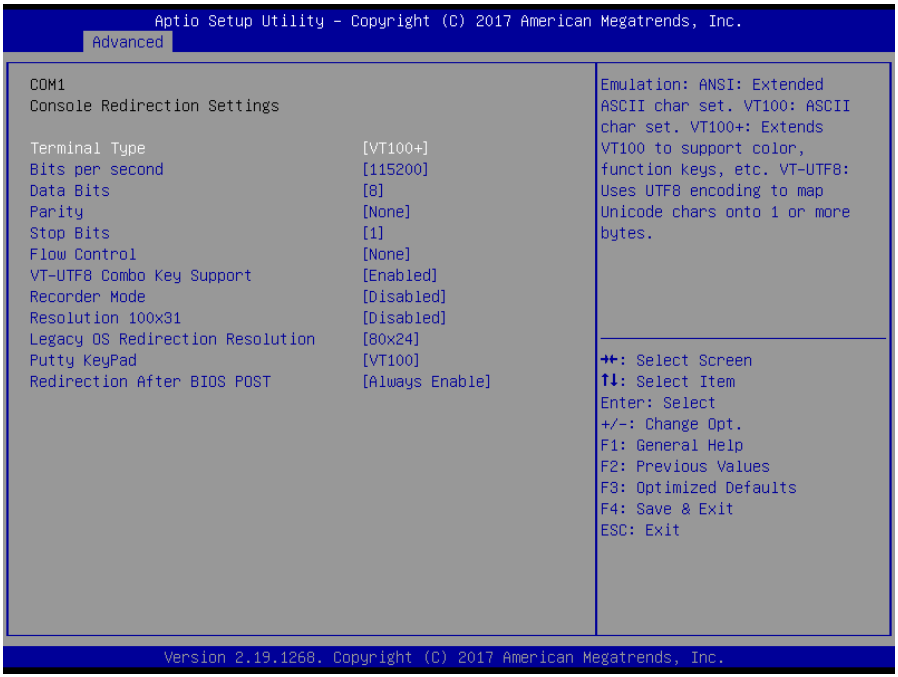
COM1
Console Redirection
Console redirection enable or disable.
Disabled / Enabled

Legacy Console Redirection
Legacy Console Redirection Settings

Serial Port for Out-Of-Band Management/Windows Emergency Services (EMS) Console Redirection
Console redirection enable or disable.
Disabled / Enabled

Console Redirection Settings
The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
NOTE: Console Redirection Settings menu only appear when **Console Redirection** was set to **[Enabled].**

3.3.6.1 Console Redirection Settings



Terminal Type

Emulation: ANSI: Extended ASCII char set.
VT100: ASCII char set.
VT100+: Extends VT100 to support color function keys, etc.
VT-UTF8: Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.

VT-UTF8 **/** VT100 / **VT100+** / ANSI

Bits per Second

Select serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

38400 **/** 9600 / 19200 / **115200** / 57600

Data Bits

8 / 7

Parity

A parity bit can be sent with the data bits to detect some transmission errors. Even: parity bit is 0 if the num of 1's in the data bits is even. Odd: parity bit is 0 if the num of 1's in the data bits is odd. Mark: parity bit is always 1. Space: parity bit is always 0. Mark and Space parity do not allow for error detection.

None / Even / Odd / Mark / Space

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.

1 / 2

Flow Control

Flow Control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signal.

None / Hardware RTS/CTS

VT-UTF8 Combo Key Support

Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals.

Enabled / Disabled

Recorder Mode

With this mode enabled only text will be sent. This is to capture Terminal data.

Disabled / Enabled

Resolution 100x31

Enable or disable extended terminal resolution.

Disabled / Enabled

Legacy OS Redirection Resolution

On Legacy OS, the number of rows and columns supported redirection.

80x24 / 80x25

Putty KeyPad

Select FunctionKey and KeyPad on Putty.

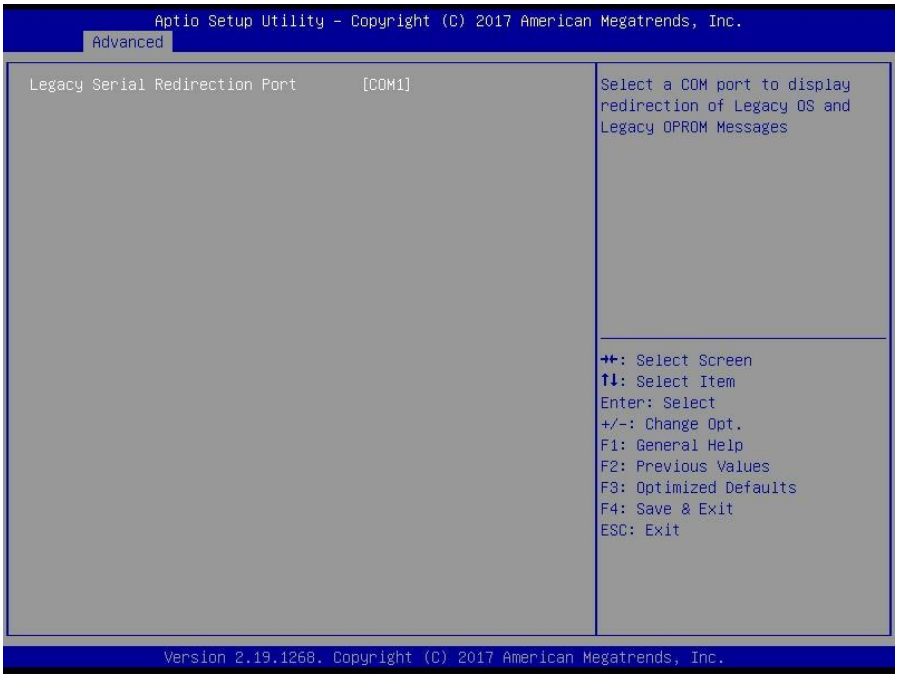
VT100 / LINUX / XTERMR6 / SCO / ESCN / VT400

Redirection After BIOS POST

The settings specify if BootLoader is selected than Legacy console redirection is disabled before booting to Legacy OS. Default value is always enable means Legacy.

Always Enable / Bootloader

3.3.6.2 Legacy Console Redirection Settings

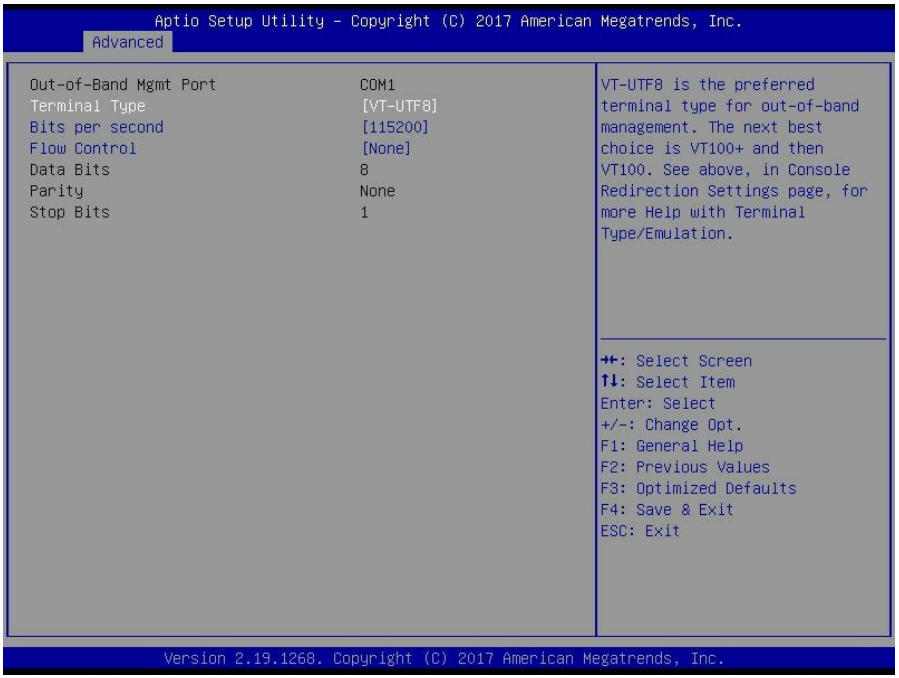


Legacy Serial Redirected Port

Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages

COM1

3.3.6.3 Serial Port for Out-Of-Band Management/Windows Emergency Services (EMS) Console Redirection Settings



Out-of Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allows for remote management of a Windows Server OS through a serial port.

COM1

Terminal Type

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100. See above, in Console Redirection Settings page, for more Help with Terminal Type/Emulation.

VT-UTF8 / VT100 / VT100+ / ANSI

Bits per Second

Select serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.

115200 / 9600 / 19200 / 57600

Flow Control

Flow Control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a 'stop' signal can be sent to stop the data flow. Once the buffers are empty, a 'start' signal can be sent to restart the flow. Hardware flow control uses two wires to send start/stop signal.

None / Hardware RTS / CTS / Software Xon / Xoff

Data Bits / Parity / Stop Bits

Read only.

3.3.7 PCI Subsystem settings

Above 4G Decoding

Enables or Disables 64 bit capable Devices to be Decoded in Above 4G Address Space(Only if System Supports 64 bit PCI Decoding).

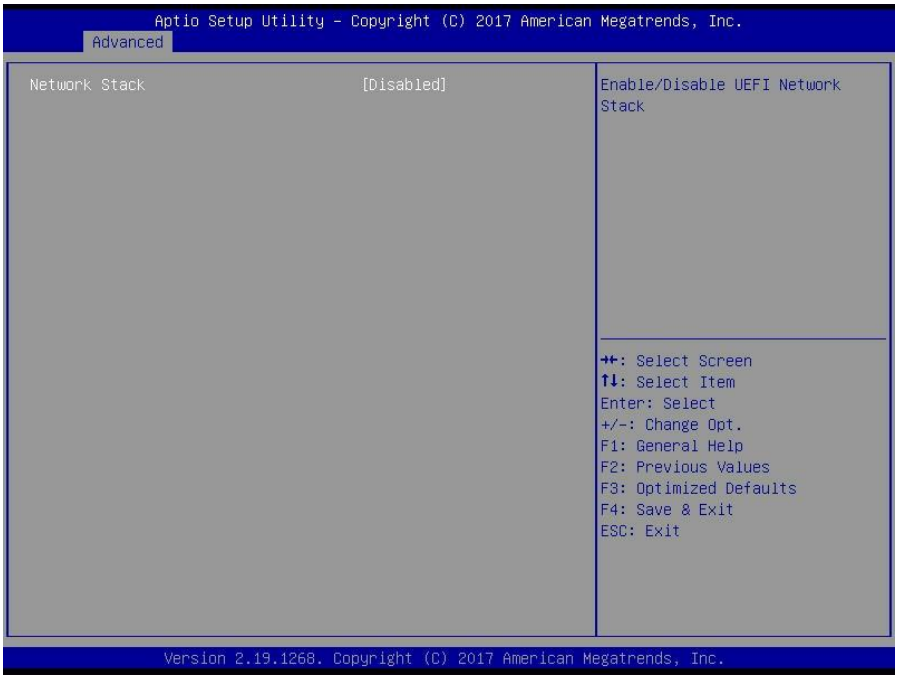
Disabled / **Enabled**

SR-IOV Support

If system has SR-IOV capable PCIe Devices,this option Enables or Disables Single Root IO virtualization Support.

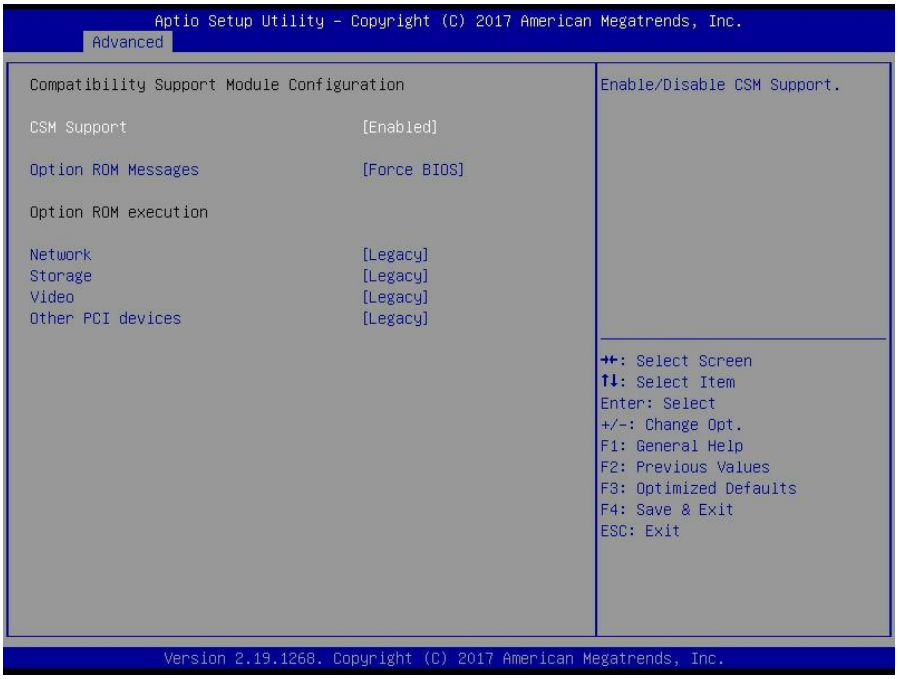
Disabled / **Enabled**

3.3.8 Network Stack Configuration



Network Stack
Enable / Disable UEFI Network Stack.
Disabled / Enabled

3.3.9 CSM Configuration



CSM support
Enable/Disable CSM Support
Enabled / Disabled

Option ROM Messages
Set display mode for Option ROM
Force BIOS / Keep Current

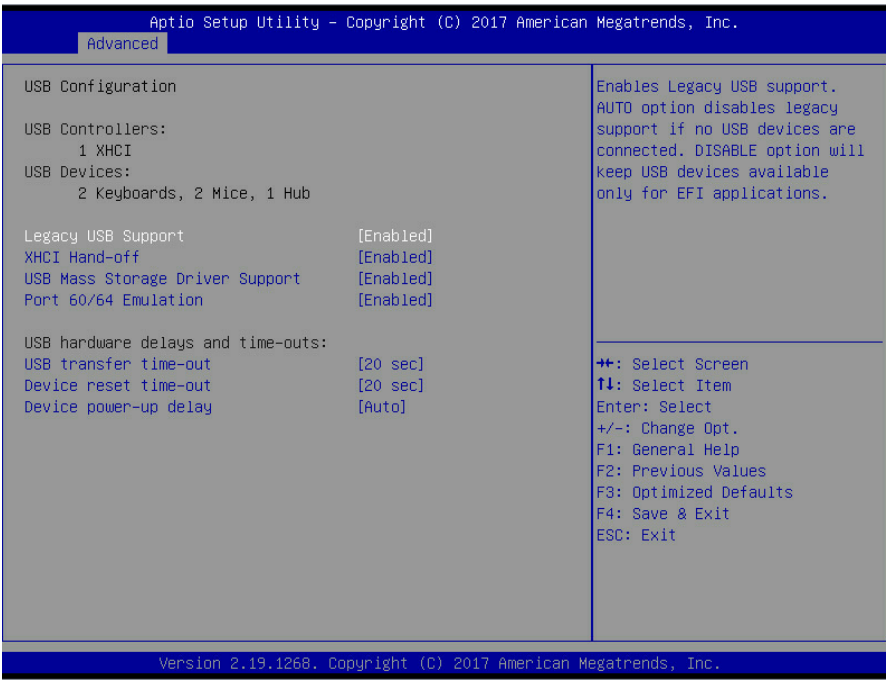
Network
Controls the execution of UEFI and Legacy PXE OpROM
Do not launch / UEFI / **Legacy**

Storage
Controls the execution of UEFI and Legacy Storage OpROM
Do not launch / UEFI / **Legacy**

Video
Controls the execution of UEFI and Legacy Video OpROM
Do not launch / UEFI / **Legacy**

Other PCI devices
Determines OpRom execution policy for devices other than Network, Storage, or Video
UEFI / **Legacy**

3.3.10 USB Configuration



Legacy USB Support
Enables USB legacy support. AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

Enabled / Disabled / Auto

XHCI Hand-off
This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

Enabled / Disabled

USB Mass Storage Driver Support
Enable/Disable USB Mass Storage Driver Support.

Disabled / **Enabled**

Port 60/64 Emulation
Enable I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

Disabled / **Enabled**

USB transfer time-out

The time-out value for Control, Bulk and Interrupt transfers.

20 sec / 10 sec / 5 sec / 1 sec

Device reset time-out

USB mass storage device Start Unit command time-out.

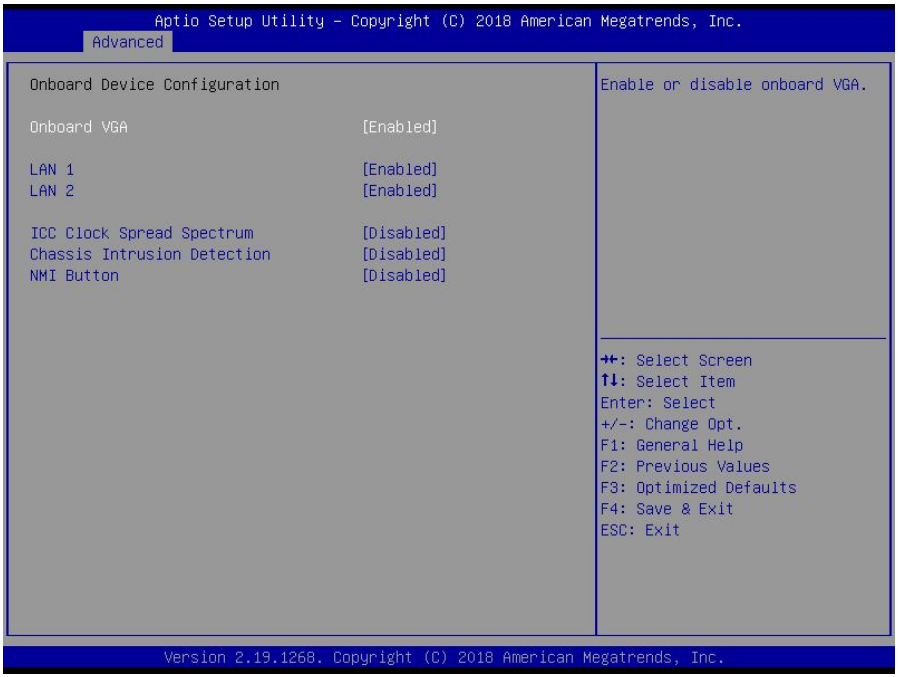
20 sec / 10 sec / 30 sec / 40 sec

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. AUTO uses default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor.

Auto / Manual

3.3.11 Onboard Device Configuration



Onboard VGA
Enable or disable onboard VGA
Disabled **/ Enabled**

LAN1
LAN Enable/Disable control function.
Disabled / **Enabled**

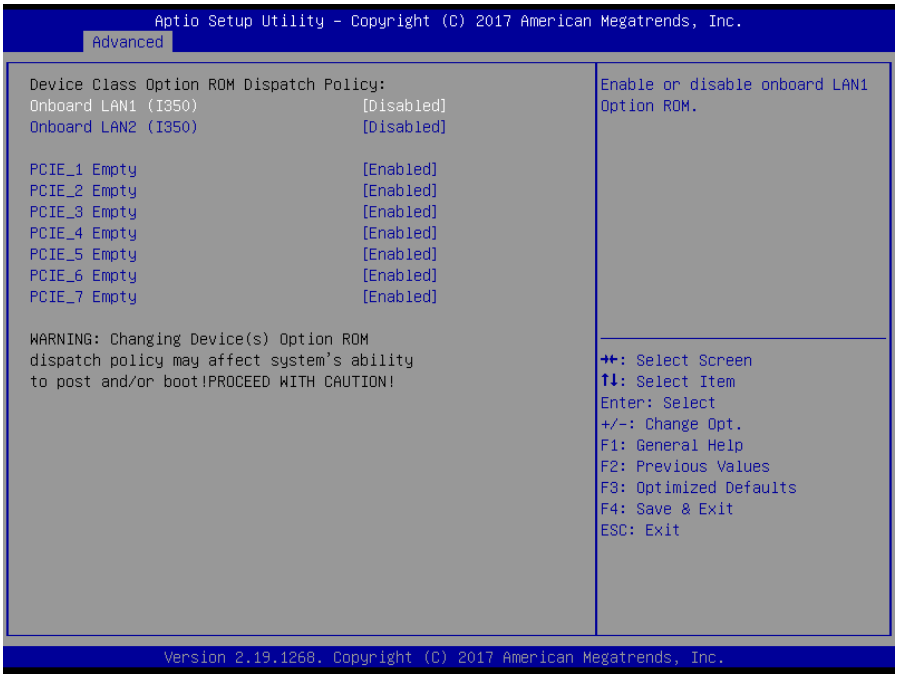
LAN2
LAN Enable/Disable control function. .
Disabled / **Enabled**

ICC Clock Spread Spectrum
Turn on/ off Spread Spectrum Setting for IsCLK
Disabled / Enabled

Chassis Intrusion Detection
ENABLED: When a chassis open event is detected, the BIOS will record the event.
Disabled / Enabled

NMI Button
Enable or Disable NMI button
Disabled / Enabled

3.3.12 Option ROM Dispatch Policy Configuration

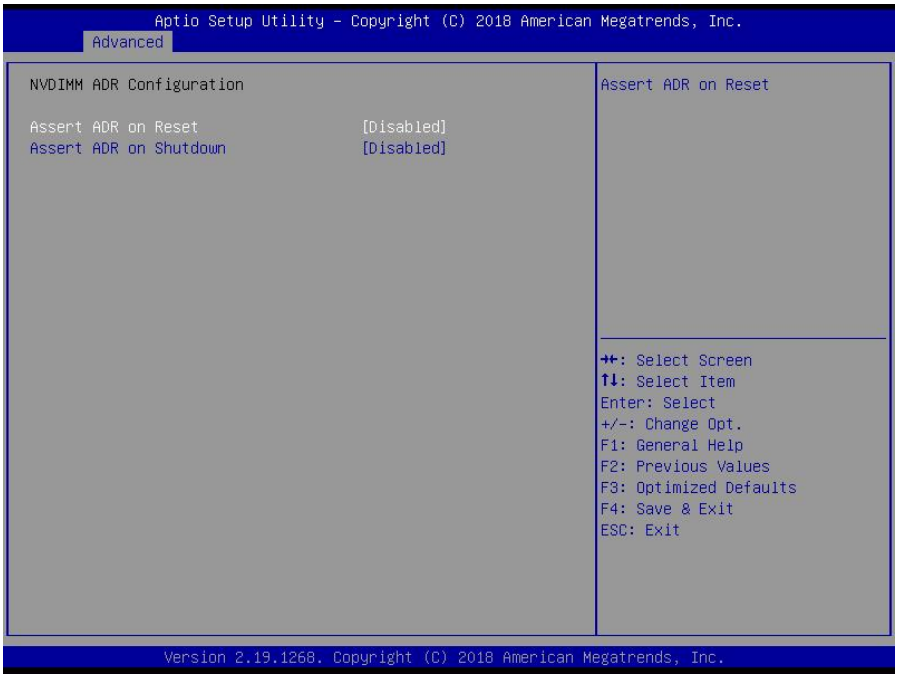


Onboard LAN1 (I350)
Enable or Disable onboard LAN1 Option ROM.
Disabled / Enabled

Onboard LAN2 (I350)
Enable or Disable onboard LAN2 Option ROM.
Disabled / Enabled

PCIE_1/2/3/4/5/6/7 Empty
Enable or Disable Option ROM execution for selected Slot
Disabled **/ Enabled**

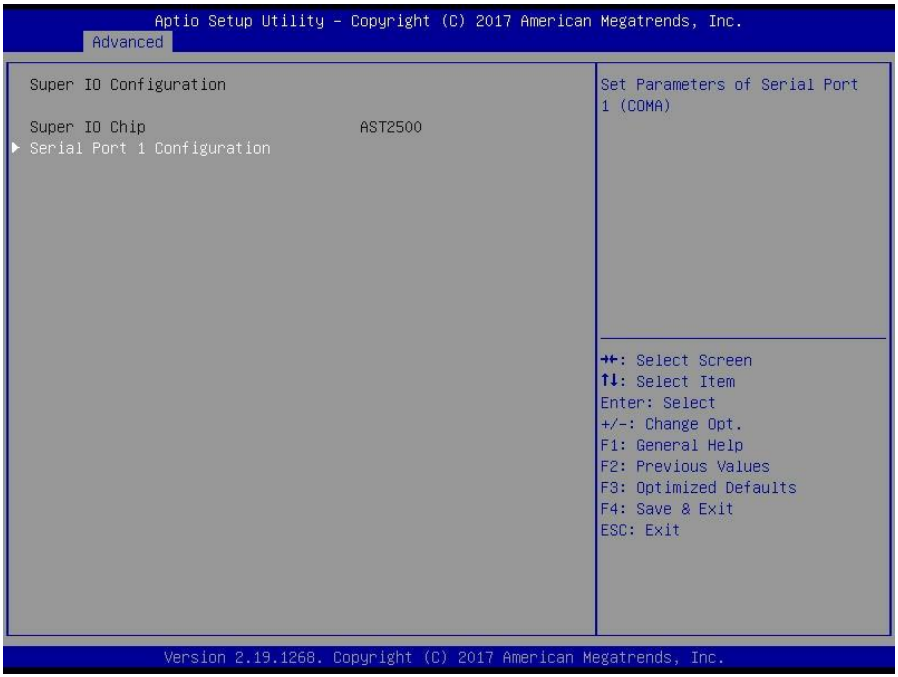
3.3.13 NVDIMM ADR Configuration



Assert ADR on Reset
Assert ADR on Reset
Disabled / Enabled

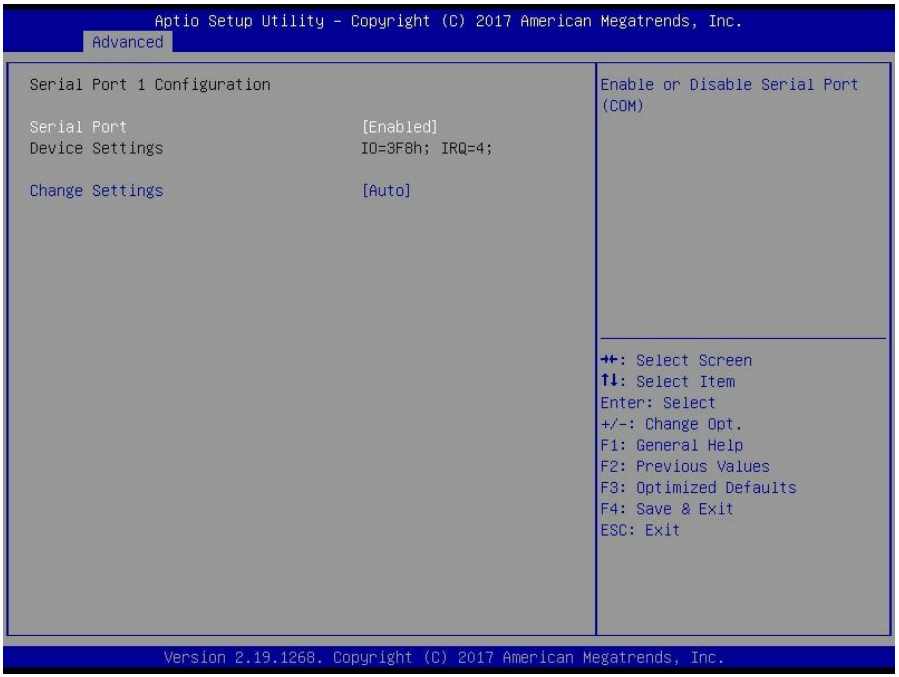
Assert ADR on Shutdown
Assert ADR on Shutdown
Disabled / Enabled

3.3.14 AST2500 Super IO Configuration



Super IO Chip
Read only.

3.3.14.1 Serial Port 1 Configuration



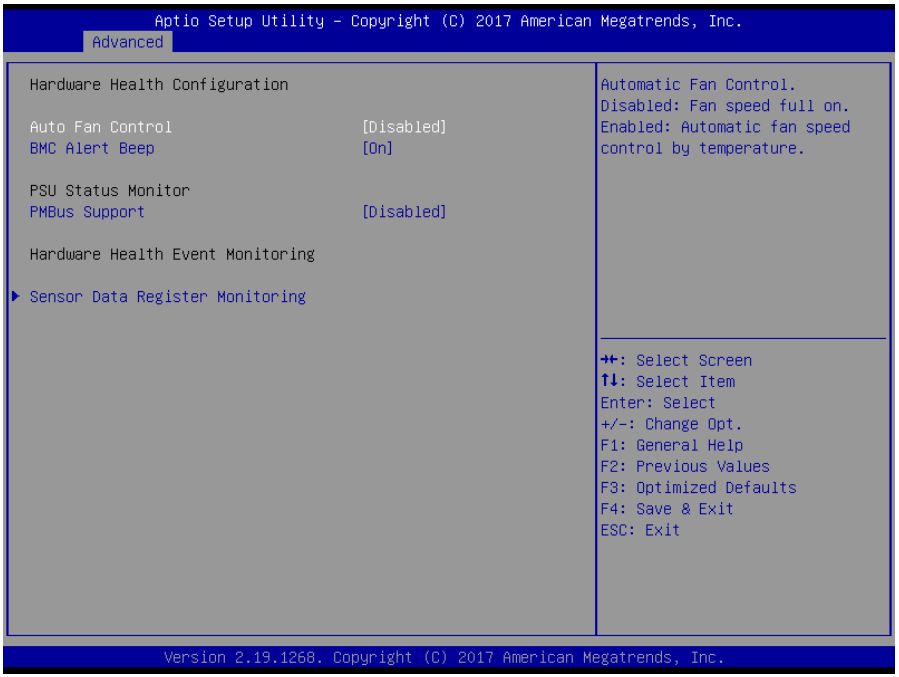
Serial Port 1 Configuration
Set parameters of Serial Port 1 (COMA)

Serial Port
Enable or disable Serial Port (COM).
Enabled / Disabled

Device Settings
Read only.

Change Settings
Select an optimal setting for Super IO Device.
Auto / IO=2F8h; IRQ=3;
/ IO=3F8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
/ IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
/ IO=3E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;
/ IO=2E8h, IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;

3.3.15 Hardware Health Configuration



Auto Fan Control

Auto Fan Control help.

Disabled / Enabled

NOTE: When **Auto Fan Control was set to [Enabled] PWM Minimal Duty Cycle Item will appear.**

PWM Minimal Duty Cycle

PWM Minimal Duty Cycle

15% Duty Cycle / 30% Duty Cycle / 45% Duty Cycle

BMC Alert Beep

Enable/Disable BMC Alert Beep

On / Off

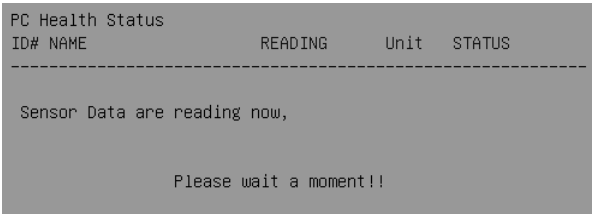
PMBus Support

PMBus Support

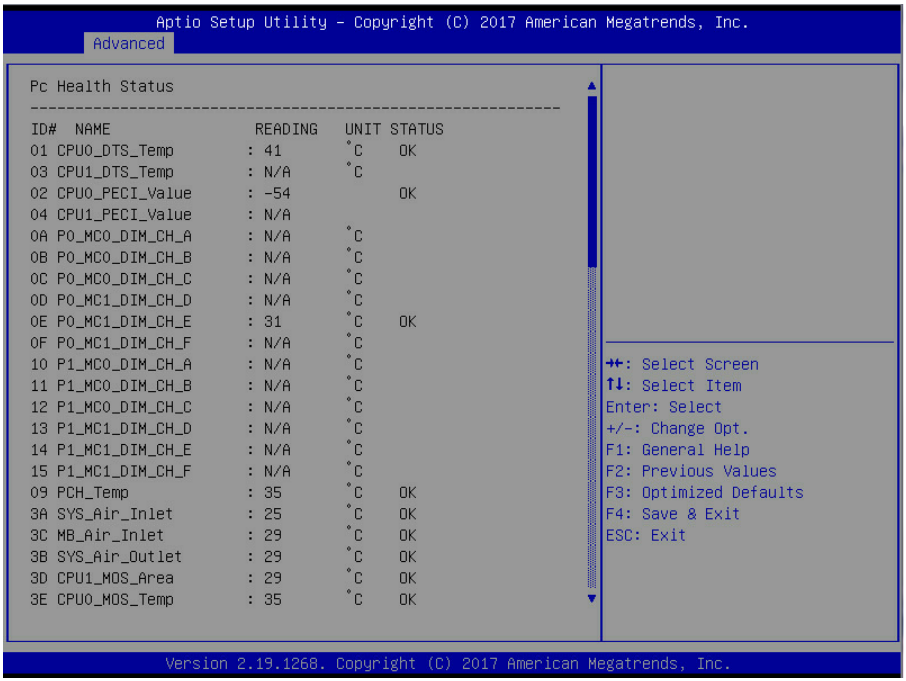
Disabled / Enabled

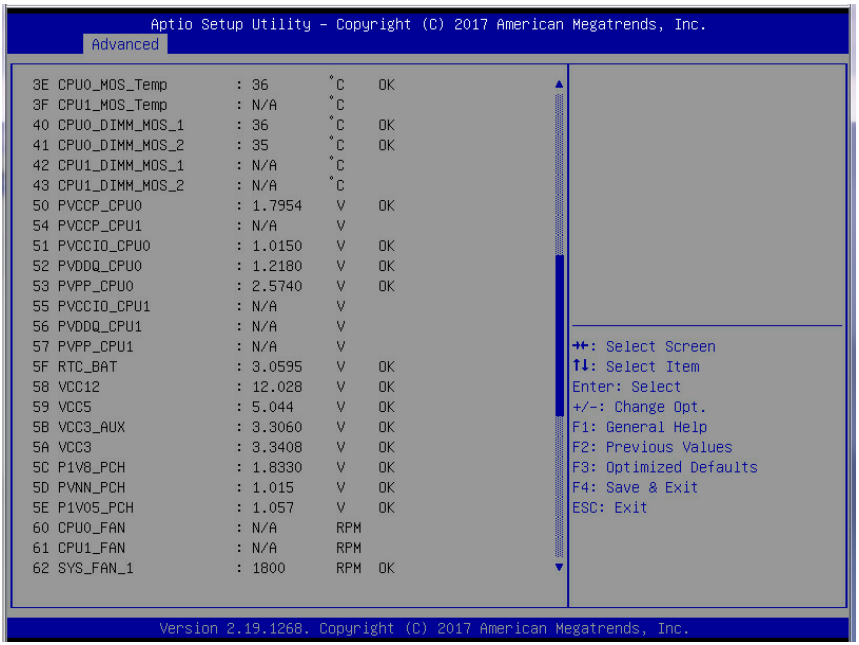
3.3.15.1 Sensor Data Register Monitoring

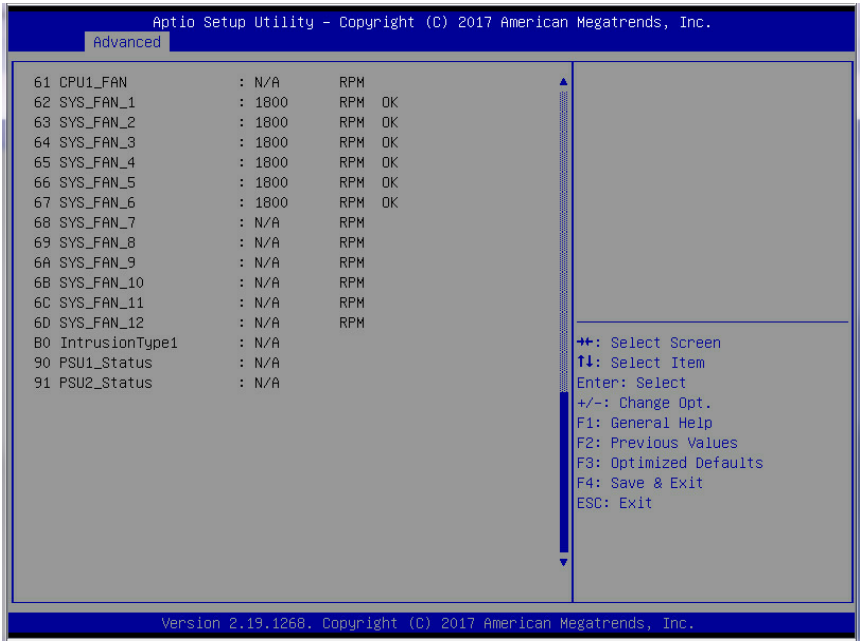
When you enter the **Sensor Data Register Monitoring** submenu, you will see the following dialog window pop out. Please wait 8~10 seconds.



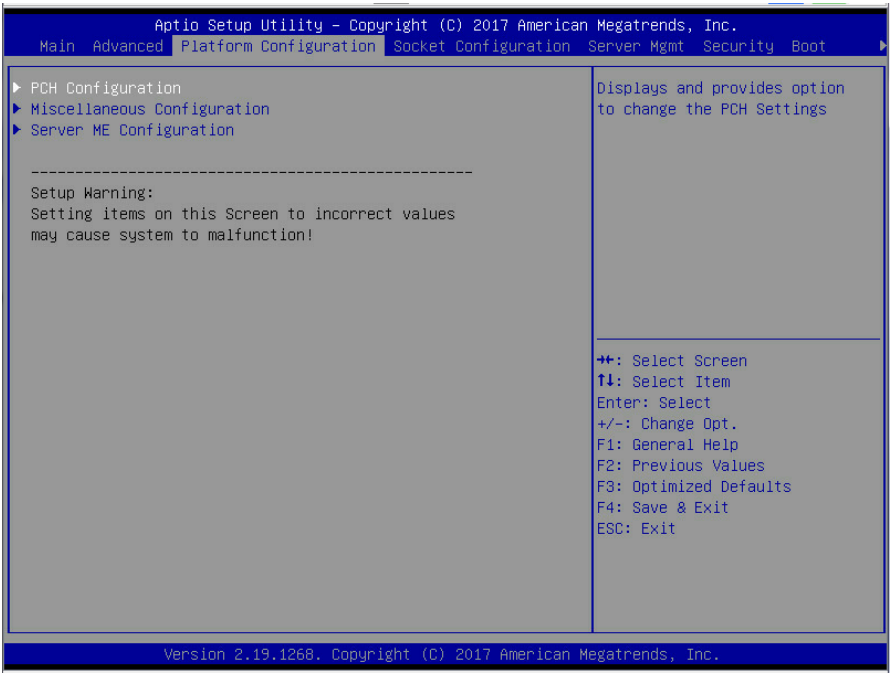
NOTE 1: SDR can not be modified. Read only.




Aptio Setup Utility – Copyright (C) 2017 American Megatrends, Inc.
Advanced
3E CPU0_MOS_Temp : 36 °C OK
3F CPU1_MOS_Temp : N/A °C
40 CPU0_DIMM_MOS_1 : 36 °C OK
41 CPU0_DIMM_MOS_2 : 35 °C OK
42 CPU1_DIMM_MOS_1 : N/A °C
43 CPU1_DIMM_MOS_2 : N/A °C
50 PVCCP_CPU0 : 1.7954 V OK
54 PVCCP_CPU1 : N/A V
51 PVCCIO_CPU0 : 1.0150 V OK
52 PVDDQ_CPU0 : 1.2180 V OK
53 PVPP_CPU0 : 2.5740 V OK
55 PVCCIO_CPU1 : N/A V
56 PVDDQ_CPU1 : N/A V
57 PVPP_CPU1 : N/A V
5F RTC_BAT : 3.0595 V OK
58 VCC12 : 12.028 V OK
59 VCC5 : 5.044 V OK
5B VCC3_AUX : 3.3060 V OK
5A VCC3 : 3.3408 V OK
5C P1V8_PCH : 1.8330 V OK
5D PVNN_PCH : 1.015 V OK
5E P1V05_PCH : 1.057 V OK
60 CPU0_FAN : N/A RPM
61 CPU1_FAN : N/A RPM
62 SYS_FAN_1 : 1800 RPM OK
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.19.1268. Copyright (C) 2017 American Megatrends, Inc.


Aptio Setup Utility – Copyright (C) 2017 American Megatrends, Inc.
Advanced
61 CPU1_FAN : N/A RPM
62 SYS_FAN_1 : 1800 RPM OK
63 SYS_FAN_2 : 1800 RPM OK
64 SYS_FAN_3 : 1800 RPM OK
65 SYS_FAN_4 : 1800 RPM OK
66 SYS_FAN_5 : 1800 RPM OK
67 SYS_FAN_6 : 1800 RPM OK
68 SYS_FAN_7 : N/A RPM
69 SYS_FAN_8 : N/A RPM
6A SYS_FAN_9 : N/A RPM
6B SYS_FAN_10 : N/A RPM
6C SYS_FAN_11 : N/A RPM
6D SYS_FAN_12 : N/A RPM
B0 IntrusionType1 : N/A
90 PSU1_Status : N/A
91 PSU2_Status : N/A
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.19.1268. Copyright (C) 2017 American Megatrends, Inc.

3.4 Platform Configuration Menu

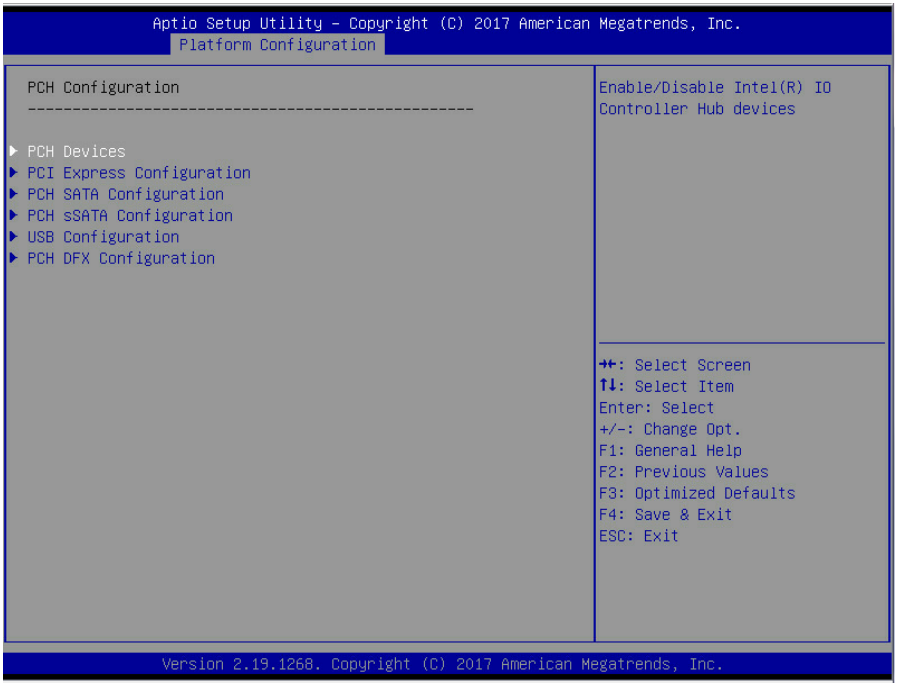


PCH Configuration
Displays and provides option to change the PCH Settings.

Miscellaneous Configuration
Miscellaneous Configuration

Server ME Configuration
Configure Server ME technology Parameters

3.4.1 PCH Configuration



PCH Devices
Enable/Disable Intel(R) IO Controller Hub devices

PCI Express Configuration
PCI Express Configuration settings

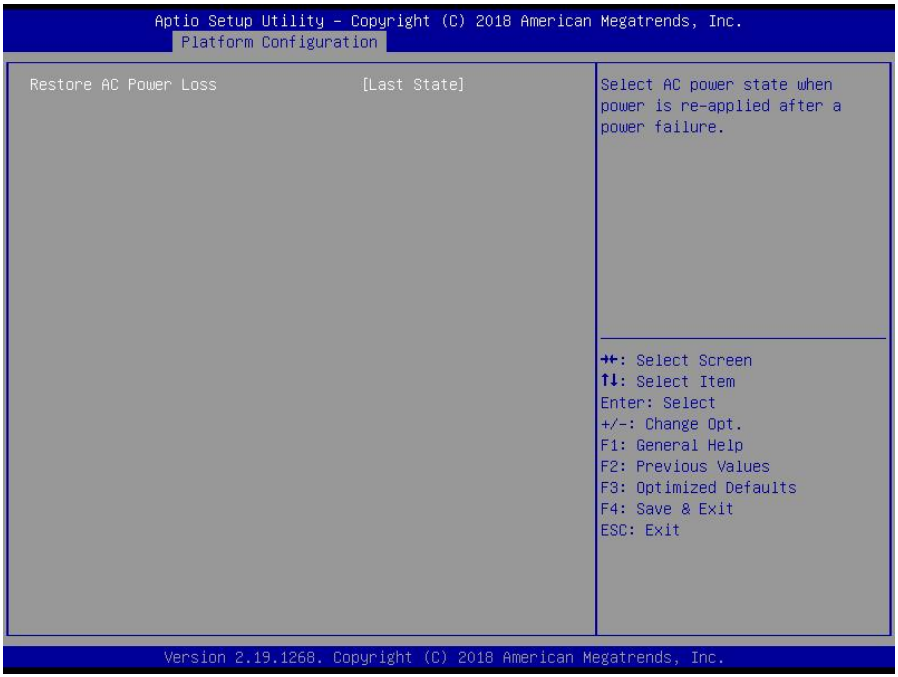
PCH SATA Configuration
SATA devices and settings

PCH sSATA Configuration
sSATA devices and settings

USB Configuration
USB Configuration Settings

PCH DFX Configuration
PCH DFX Configuration Options

3.4.1.1 PCH Devices Configuration

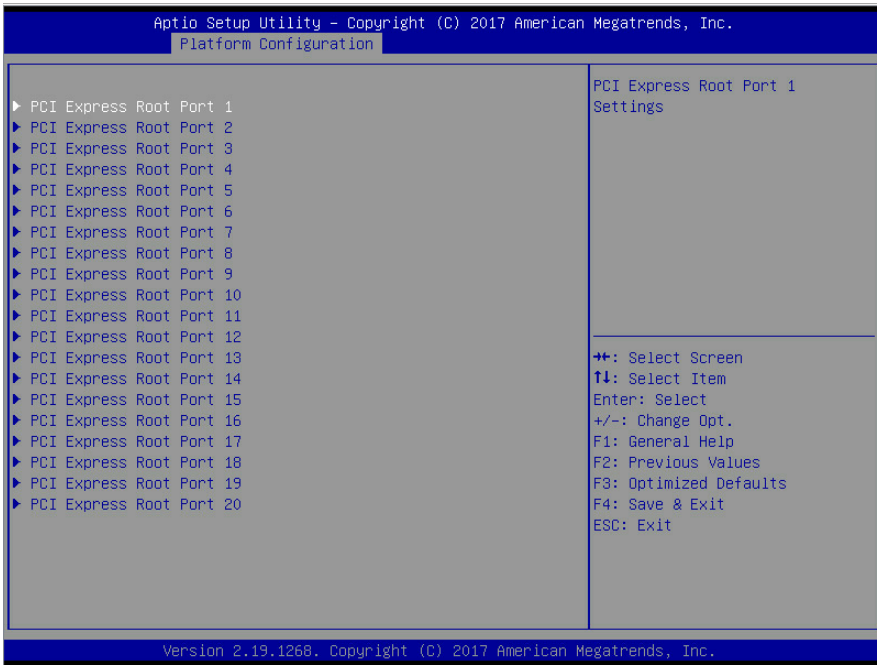


Restore AC Power Loss

Select AC power state when power is re-applied after a power failure.

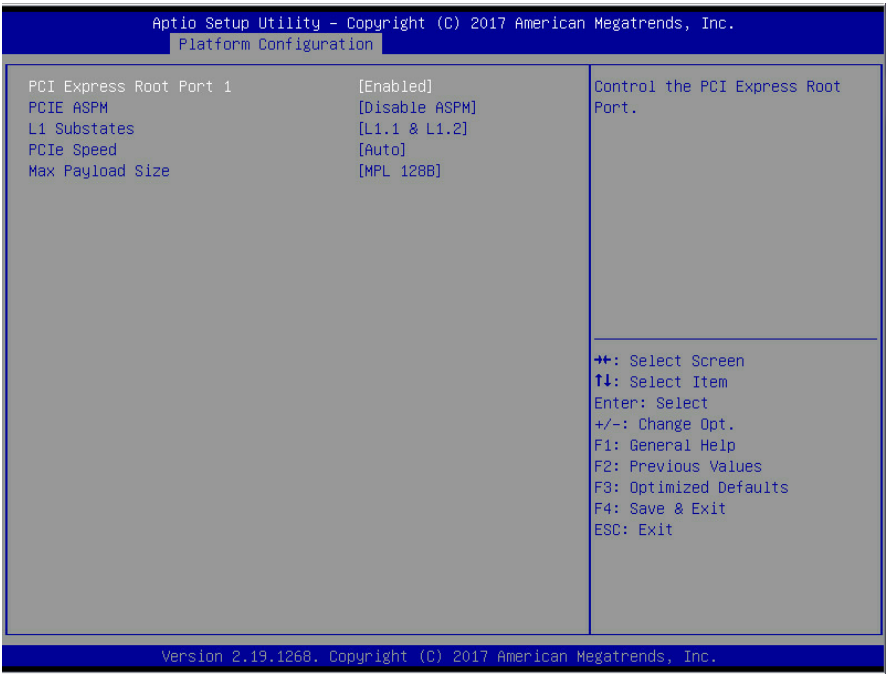
Power On /Power Off / **Last state**

3.4.1.2 PCI Express Configuration



PCI Express Root Port 1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20
PCI Express Root Port Settings

3.4.1.2.1 PCI Express Root Port 1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20 Configuration



PCI Express Root Port 1/2/3/4/5/6/7/8/9/10/11/12/13/14/15/16/17/18/19/20

Control the PCI Express Root Port

Disabled **/ Enabled**

PCIE ASPM

PCI Express Root port ASPM Setting

Disable ASPM / ASPM L1 / ASPM Auto

L1 Substates

PCI Express L1 Substates settings.

Disabled / L1.1 / L1.2 / **L1.1 & L1.2**

PCIe Speed

PCI Express Root Port Completion Timer TO settings

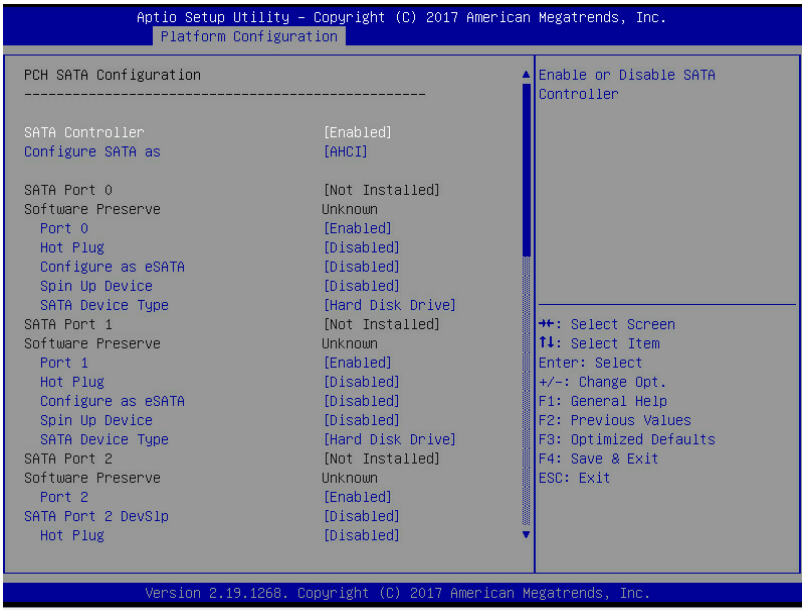
Auto / Gen1 / Gen2 / Gen3

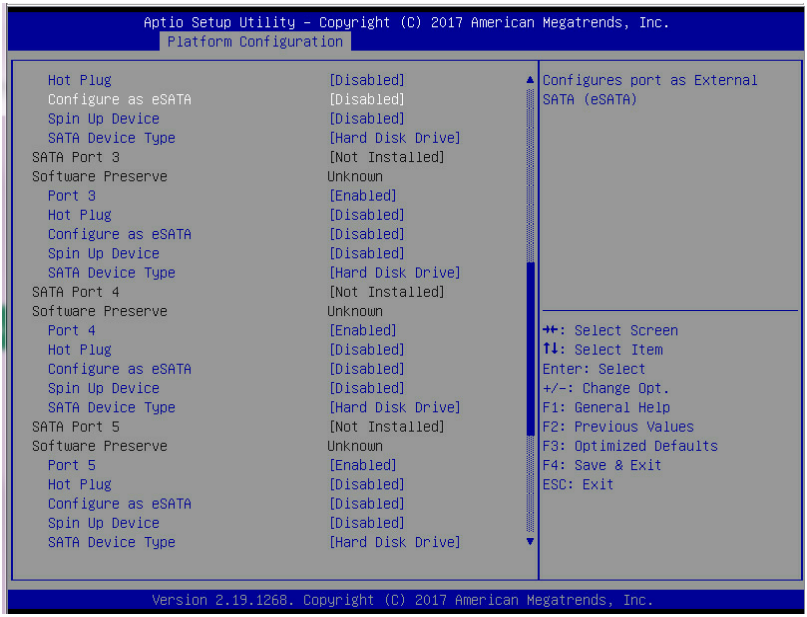
Max Payload Size

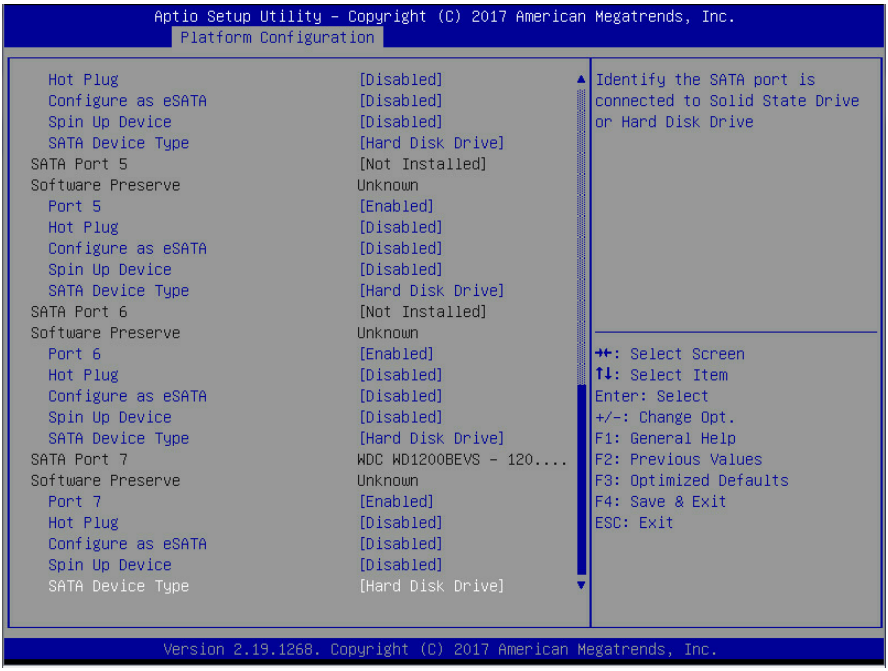
PCIE Max Payload Size Selection.

MPL 128B / MPL 256B

3.4.1.3 PCH SATA Configuration Submenu







SATA Controller
Enable or Disable SATA Controller
Disabled **/ Enabled**

Configure SATA as
Indentify the SATA port is connected to Solid State Drive or Hard Disk Drive
AHCI / RAID

SATA Port 0/1/2/3/4/5/6/7
Port 0/1/2/3/4/5/6/7
Disabled **/ Enabled**

Hot Plug
Enable/Disable SATA Ports Hot Plug Support.
Disabled / Enabled

Configure as eSATA
Configures port as External SATA (eSATA)
Disabled / Enabled

Spin Up Device

AHCI Supports Staggered Spin-up

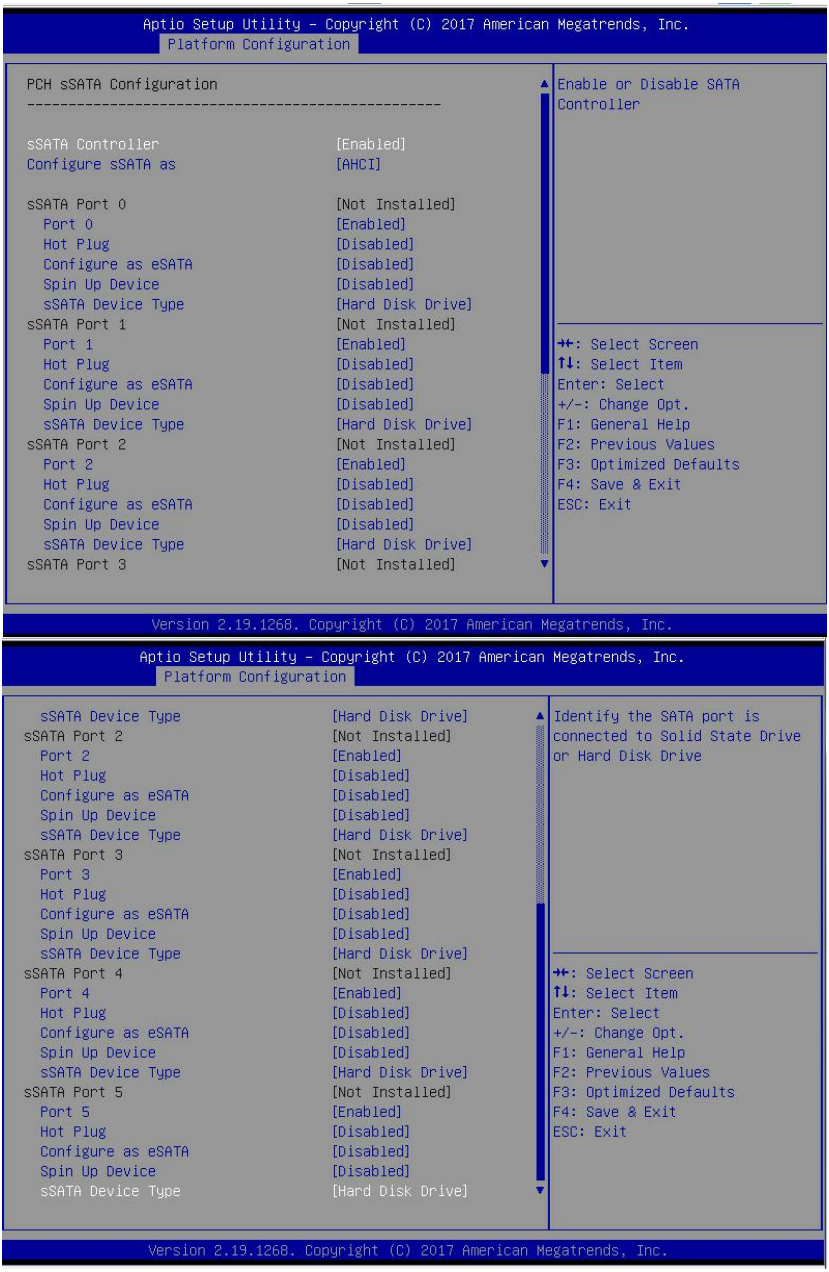
Disabled / Enabled

SATA Device Type

Indentify the SATA port is connected to Solid State Drive or Hard Disk Drive

Hard Disk Drive / Solid State Drive

3.4.1.4 PCH sSATA Configuration Submenu



sSATA Controller

Enable or Disable SATA Controller

Disable **/ Enable**

Configure sSATA as

Indentify the SATA port is connected to Solid State Drive or Hard Disk Drive

AHCI / RAID

sSATA Port 0/1/2/3/4/5

Enable or Disable SATA Port

Disable **/ Enable**

Hot Plug

Designates this port as Hot Pluggable

Disable **/** Enable

Configure as eSATA

Configures port as External SATA (eSATA)

Disable **/** Enable

Spin Up Device

If enabled for any of ports Staggerred Spin Up will be performed and only the drives witch have this option enabled will spin up at boot. Otherwise all drives spin up at boot.

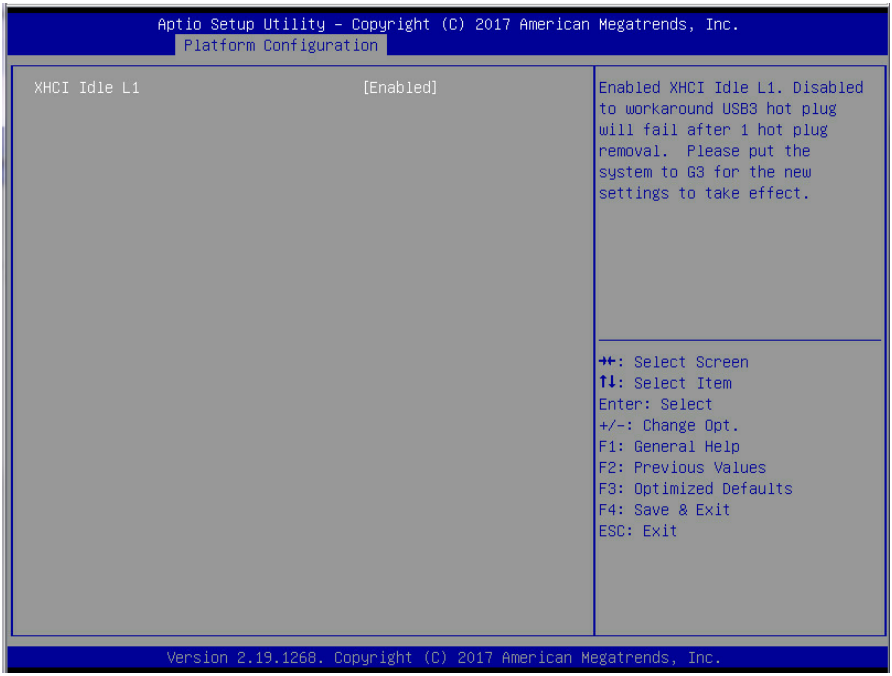
Disable **/** Enable

sSATA Device Type

Indentify the SATA port is connected to Solid State Drive or Hard Disk Drive

Hard Disk Drive / Solid State Drive

3.4.1.5 USB Configuration Submenu

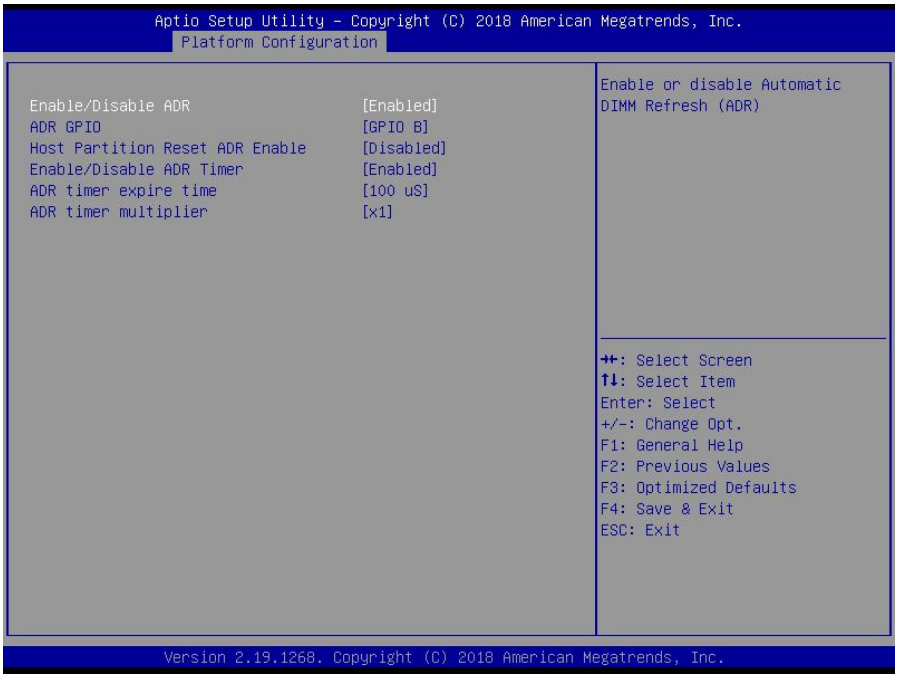


XHCI Idle L1

Enable XHCI Idle L1. Disabled to workaround USB3 hot plug will fail after 1 hot plug removal. Please put the system to G3 for the new settings to take effect.

Disabled **/ Enabled**

3.4.1.6 PCH DFX Configuration Submenu



Enable/Disable ADR
Enable or disable Automatic DIMM Refresh (ADR)
Platform-POR **/ Enabled /** Disabled

ADR GPIO
Select between GPIO_B or GPIO_C
GPIO B / GPIO C

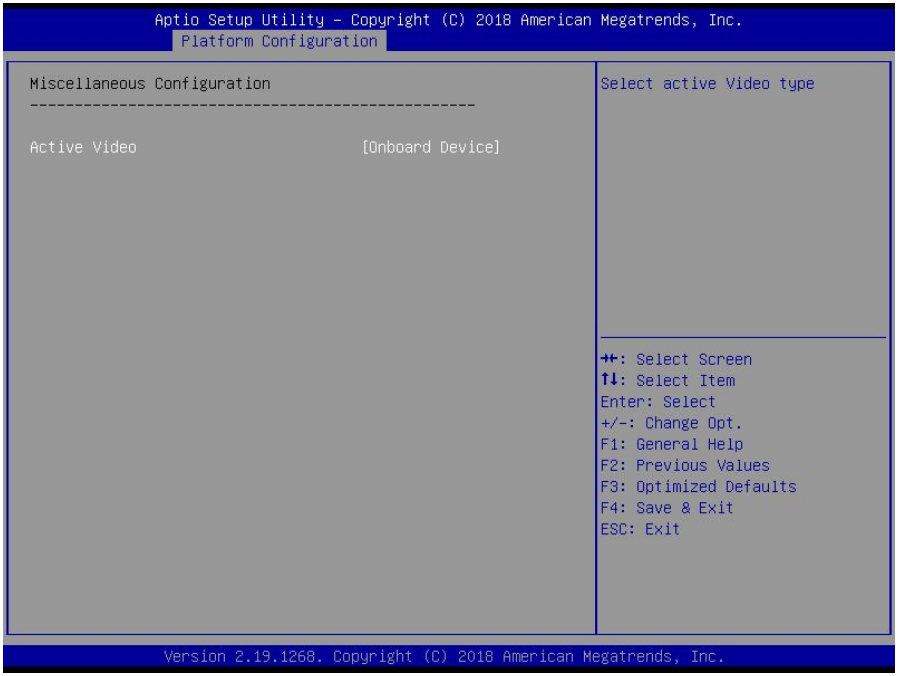
Host Partition Reset ADR Enable
Enables/Disables ADR on Host Partition Reset
Platform-POR **/** Enabled **/ Disabled**

Enable/Disable ADR Timer
Held-off for DEBUG PURPOSES ONLY!
Platform-POR **/ Enabled /** Held-off

ADR timer expire time
Select proper ADR timer value: 25uS,50uS,100uS or 0.
Platform-POR / 25 uS / 50 uS / **100 uS** / 0 uS

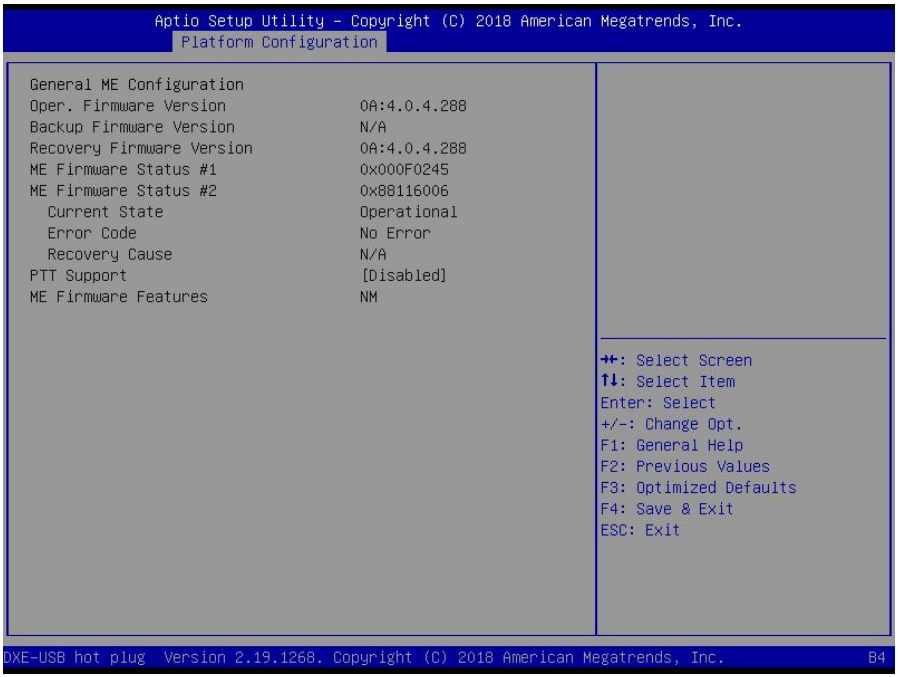
ADR timer multiplier
Select proper ADR timer multiplier: x1,8,24,40,56,64,72,80,88,96.
Platform-POR / **x1** / x8 / x24 / x40 / x56 / x64 / x72 / x80 / x88 /x96

3.4.2 Miscellaneous Configuration Submenu



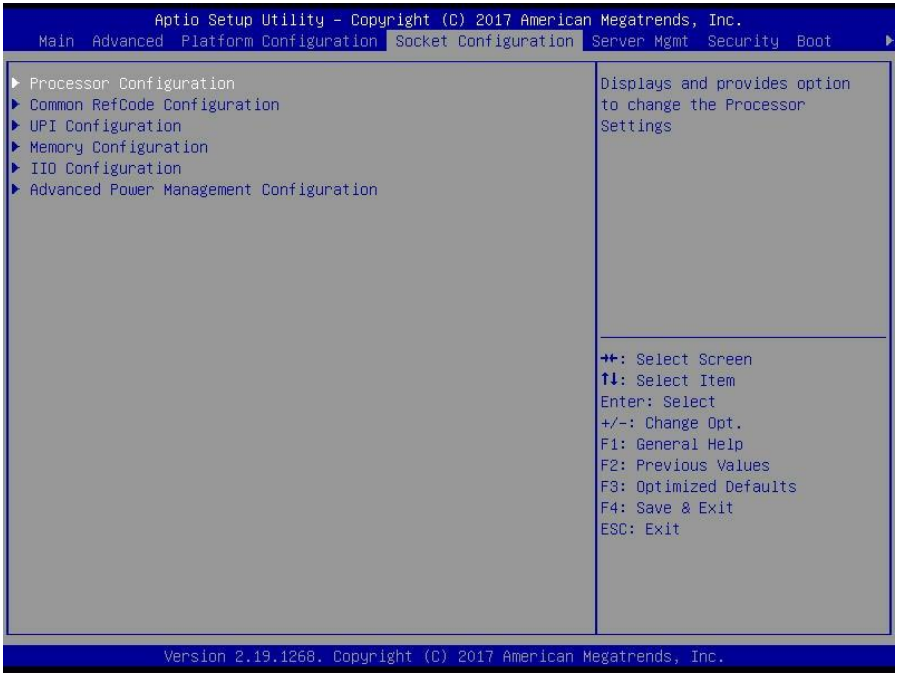
Active Video
Select active Video type
Onboard Device / Offboard Device

3.4.3 Server ME Configuration Submenu



Only Read

3.5 Socket Configuration



Processor Configuration
Displays and provides option to change the Processor Settings.

Common RefCode Configuration
Displays and provides option to change the Common RefCode Settings

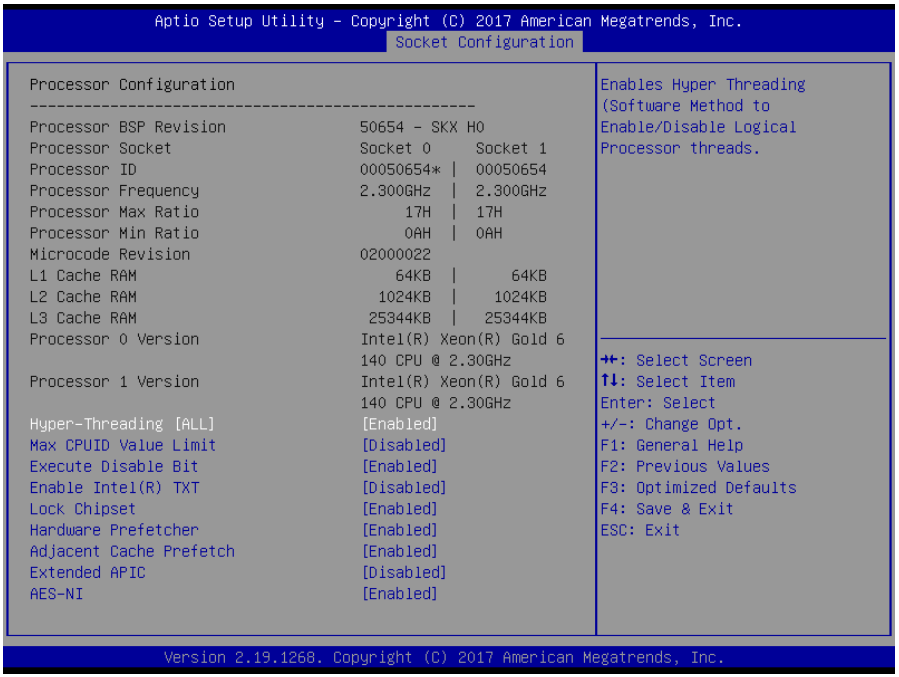
UPI Configurtion
Displays and provides option to change the UPI Settings

Memory Configuration
Displays and provides option to change the Memory Settings

IIO Configuration
Displays and provides option to change the IIO Settings

Advance Power Management Configuration
Displays and provides option to change the Power Management Settings

3.5.1 Processor Configuration Submenu



Hyper-Threading [ALL]
Enables Hyper Threading (Software Method to Enable/Disable logical Processor threads.

Disabled / **Enabled**

Max CPUID Value Limit
This should be enabled in order to boot legacy OSes that cannot support CPUs with extended CPUID functions.

Disabled / Enabled

Execute Disable Bit
When disabled, forces the XD feature flag to always return 0.

Disabled / **Enabled**

Enable Intel(R) TXT
Enables Intel(R) TXT

Disabled / Enabled

Lock Chipset
Lock or Unlock chipset
Disabled **/ Enabled**

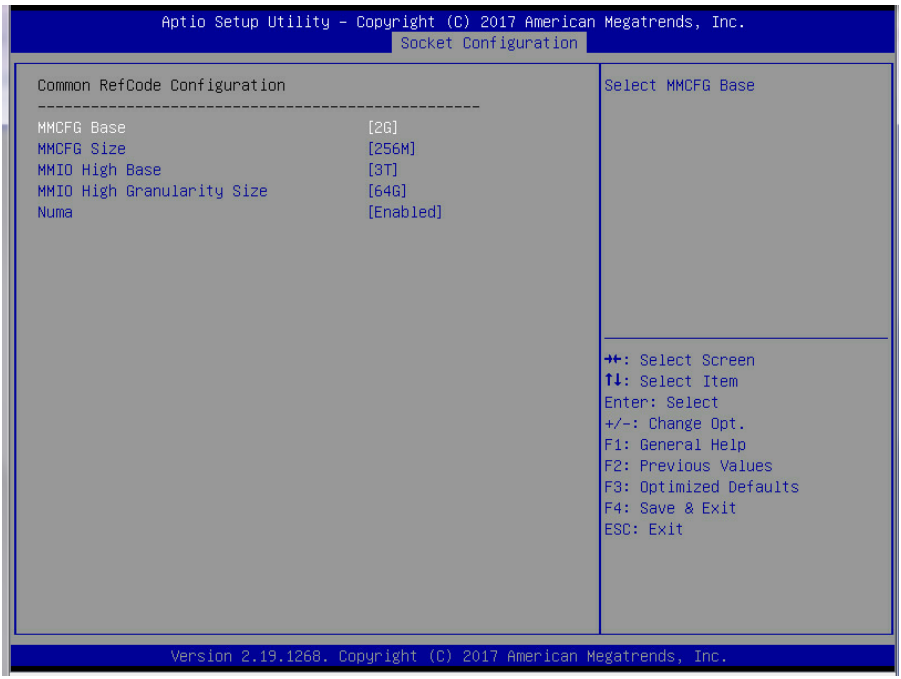
Hardware Prefetcher
MLC Streamer Prefetcher (MSR 1A4h Bit [0])
Disabled **/ Enabled**

Adjacent Cache Prefetch
MLC Spatial Prefetcher (MSR 1A4h Bit [1])
Disabled **/ Enabled**

Extended APIC
Enable/disable extended APIC support
Disabled **/** Enabled

AES-NI
Enable/disable AES-NI support
Disabled **/ Enabled**

3.5.2 Common RefCode Configuration Submenu



MMCFG Base

Select MMCFG Base

1G /1.5G / 1.75G / **2G** / 2.25G /3G

MMCFG Size

Select MMCFG Size

64M / 128M / **256M** / 512M / 1G / 2G

MMIO High Base

Select MMIO High Base

56T / 40T / 24T /16T / 4T/ **3T** / 2T / 1T

MMIO High Granularity Size

Selects the allocation size used to assign mmioh resources. Total mmioh space can be up to 32x granularity.

Per stack mmioh resource assignments are multiples of the granularity where 1 unit Per stack is the default allocation.

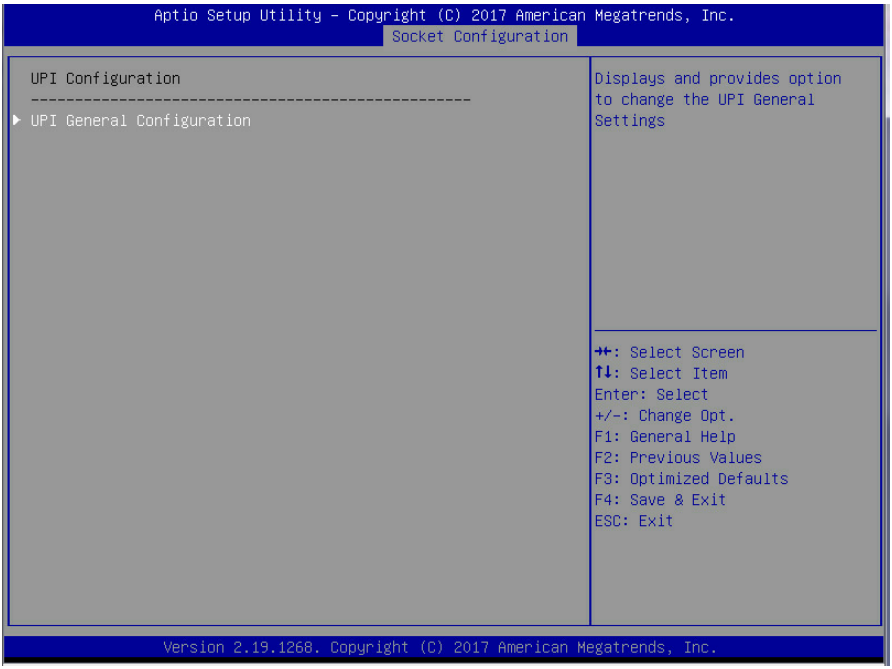
1G / 4G / 16G / **64G** / 256G / 1024G

Numa

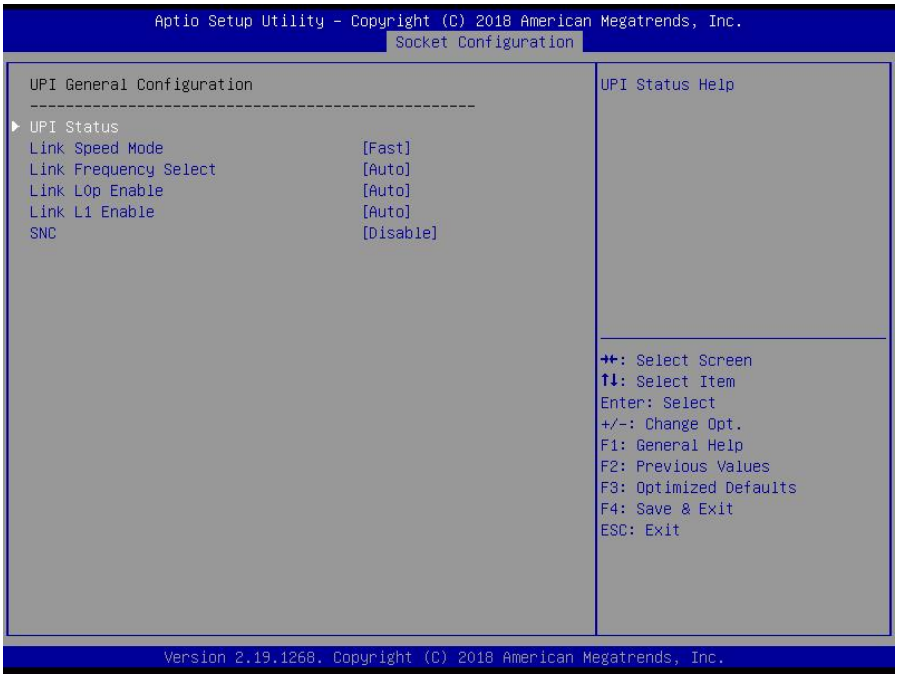
Enable or Disable non uniform Memory Access. (NUMA)

Enabled / Disabled

3.5.3 UPI Configuration Submenu



3.5.3.1 UPI General Configuration Submenu



UPI Status
UPI Status Help.

Link Speed Mode
Select the UPI link speed as either the POR speed (Fast) or default speed (Slow)
Slow / **Fast**

Link Frequency Select
Allows for selecting the UPI Link frequency
9.6GB/s / 10.4GB/s / **Auto** / Use Per Link Setting

Link L0p Enable
Enable – Set the c_L0p_en, Disable – Reset it, Auto – Auto decides based on Si Compatibility
Disable / Enable / **Auto**

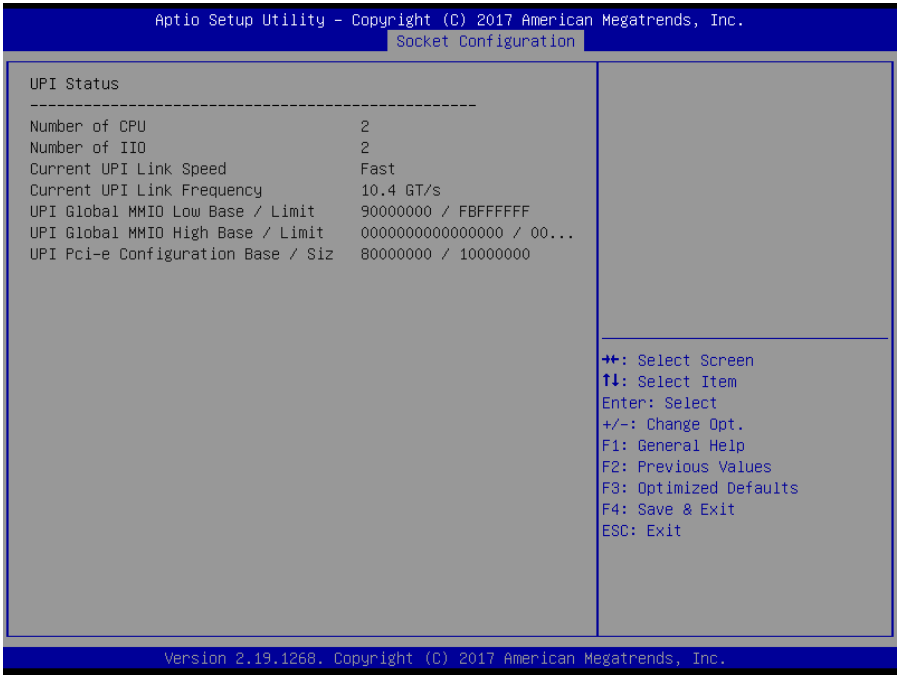
Link L1 Enable
Enable – Set the c_L1_en, Disable – Reset it, Auto – Auto decides based on Si Compatibility
Disable / Enable / **Auto**

SNC

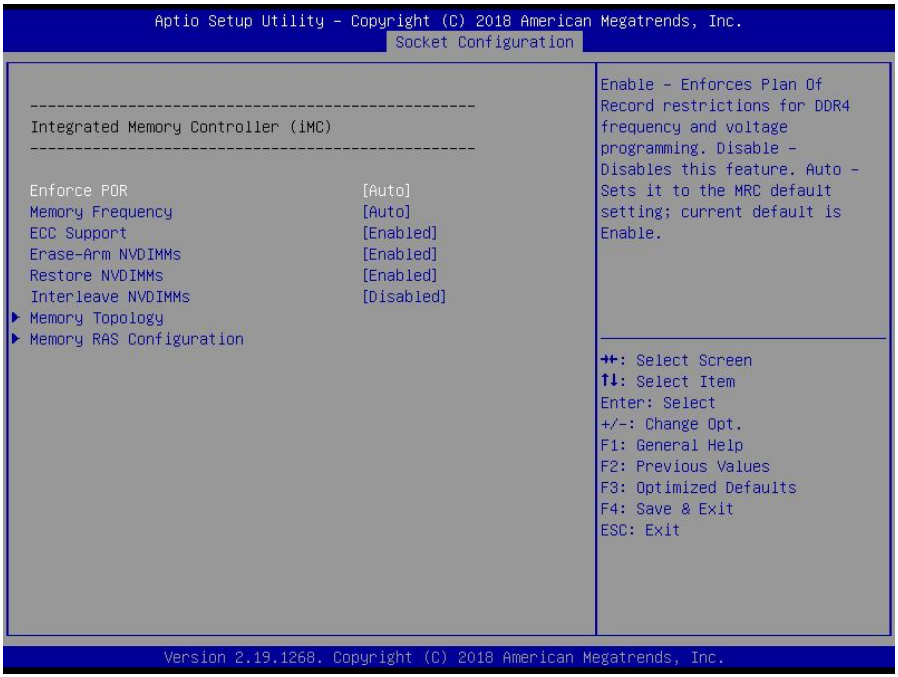
AUTO supports 1-cluster or 2-clusters depending on IMC interleave. SNC and IMC interleave both AUTO will support 1-cluster (XPT/KTI Prefetch enable) 2-IMC way interleave. SNC Enable supports Full SNC (2 clusters and 1-way IMC interleave.

Disable / Enable / Auto

3.5.3.2 UPI Status Configuration Submenu



3.5.4 Memory Configuration Submenu



Enforce POR

Enable – Enforce Plan Of Record restrictions for DDR4 frequency and voltage programming .Disable – Disables this feature. Auto – Sets it to the MRC default setting; current default is Enable.

Auto / POR / Disable

Memory Frequency

Maximum Memory Frequency Selections in Mnz. Do not select Reserved

Auto / 2133 / 2400 / 2666

ECC Support

Enable – Enables DDR ECC Support. Disable – Disables this feature. Auto – Sets it to MRC default setting; current default is Enable.

Disabled **/ Enabled**

Erase –Arm NVDIMMs

Enable/Disable Erasing and Arming NVDIMMs

Disabled **/ Enabled**

Restore NVDIMMs

Enables/Disables. Automatic resotring of NVDIMMs

Disabled **/ Enabled**

Interleave NVDIMMs

Controls if NVDIMMs are interleaved together or not

Disabled / Enabled

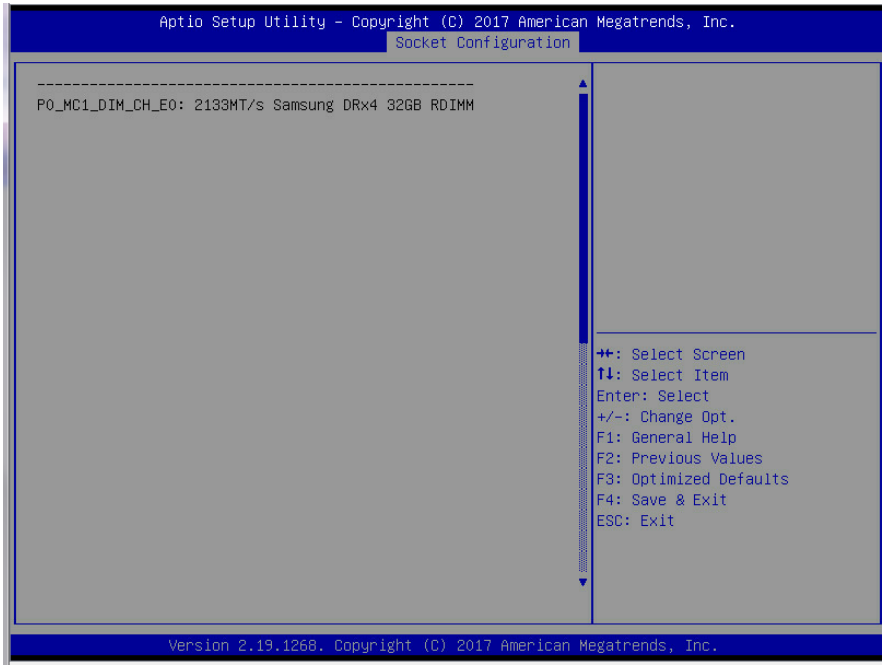
Memory Topology

Displays memory topology with Dimm population information

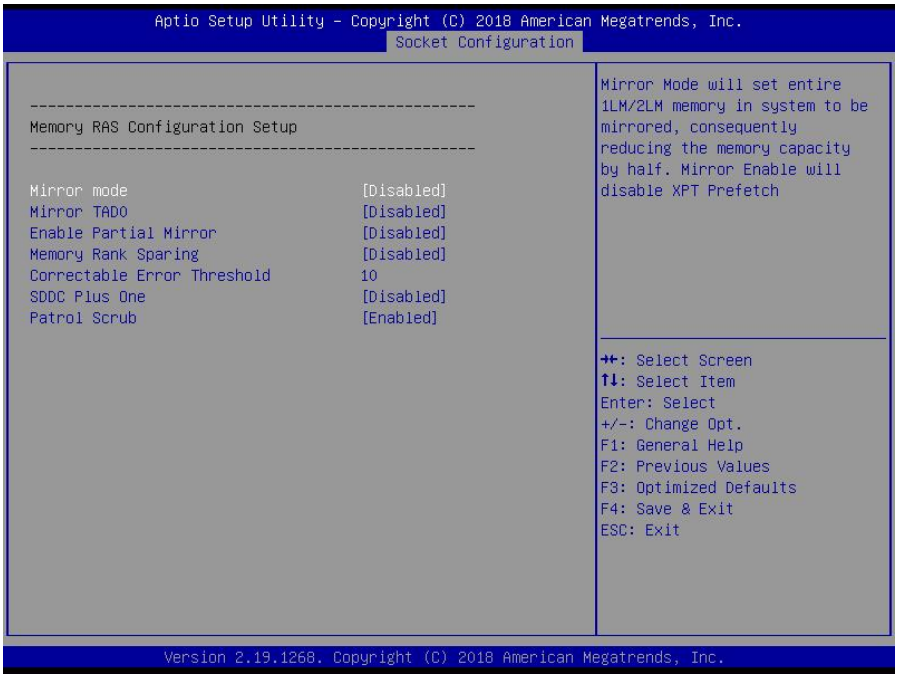
Memory RAS Configuration

Displays and provides option to change the Memory Ras Settings

3.5.4.1 Memory Topology Configuration Submenu



3.5.4.2 Memory RAS Configuration Submenu



Mirror mode
Mirror Mode will set entire 1LM/2LM memory in system to be mirrored, consequently reducing the memory capacity by half. Mirror Enable will disable XPT Prefetch.

Disabled / Enabled

Mirror TAD0
Enable Mirror on entire memory for TAD0

Disabled / Enabled

Enable Partial Mirror
Partial mirror mode will enable the required size of memory to be mirrored. If rank sparing is enabled partial mirroring will not take effect. Mirror Enable will disable XPT Prefetch.

Disabled / Enabled

Memory Rank Sparing
Enable/Disable Memory Rank Sparing

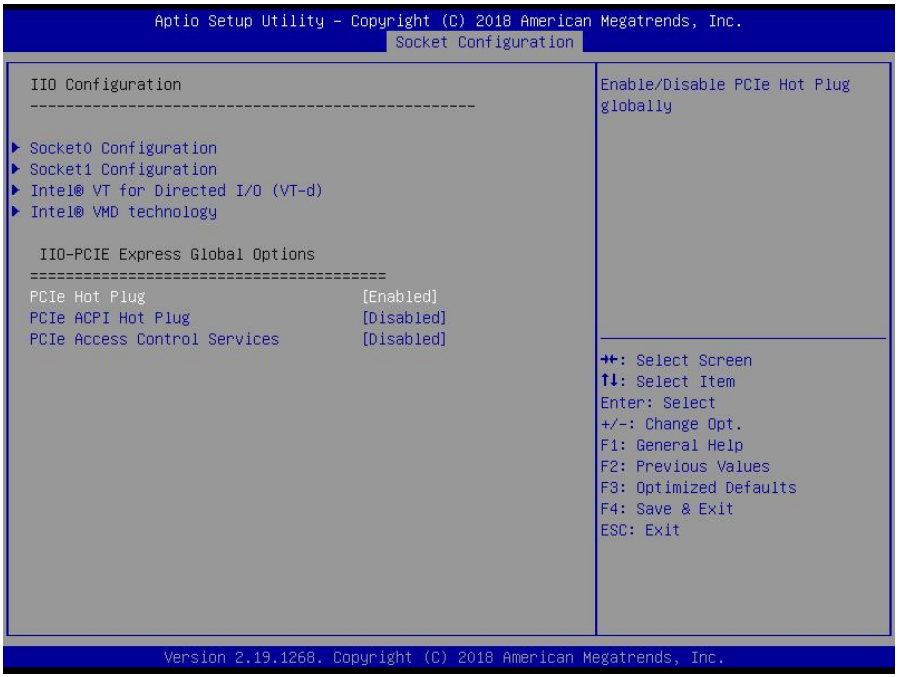
Disabled / Enabled

Correctable Error Threshold
Enable/ Disable Memory Rank Sparing

SDDC Plus One
Selects the address mode between System Physical Address (or) Reverse Address
Disabled / Enabled

Patrol Scrub
Enable/Disable Patrol Scrub
Disable / **Enabled**

3.5.5 IIO Configuration



Socket0 Configuration
Socket 0 Configuration

Socket1 Configuration
Socket 1 Configuration

Intel® VT for Directed I/O (VT-d)
Press <Enter> to bring up the Intel® VT for Directed I/O (VT-d) Configuration menu.

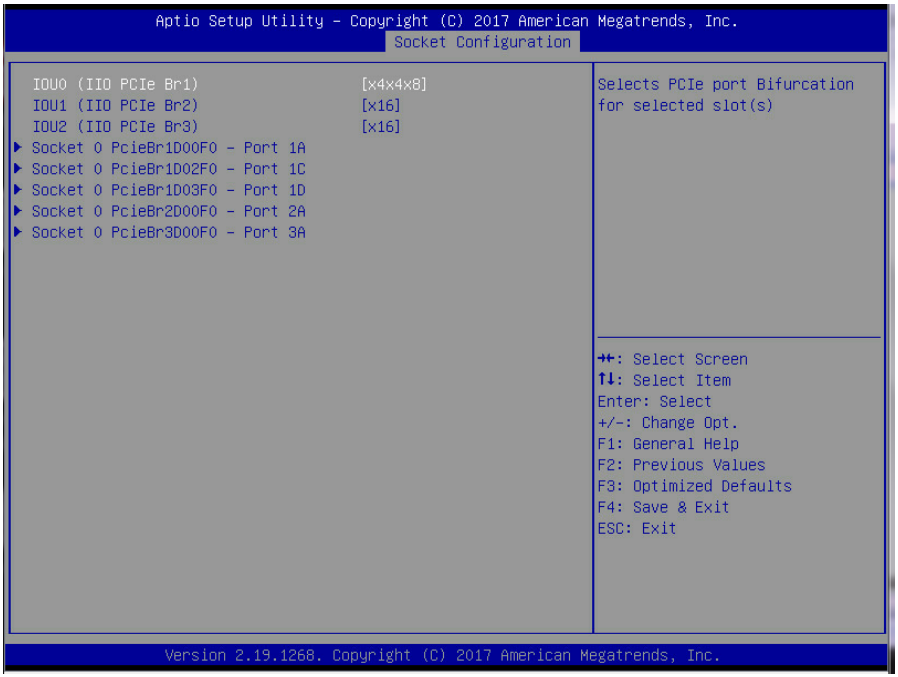
Intel® VMD technology
Press <Enter> to bring up the Intel® VMD for Volume Management Device Configuration menu.

PCIe Hot Plug
Enable/Disable PCIe Hot Plug globally.
Disabled / **Enabled**

PCIe ACPI Hot Plug
Enable/Disable PCIe ACPI Hot Plug globally, or allow per-port control. When Disabled, MSI is generated on HP event. When Enabled, _HPGPE message is generated.
Disabled / Enabled

PCIe Access Control Service
Enable or disable Access Control Services (ACS) in PCIe Downstream Switch Port.
Disabled / Enabled

3.5.5.1 Socket0 Submenu



IOU0 (IIO PCIe Br1)
Select PCIe port Bifurcation for PCIE_2 slot
x4x4x4x4 / **x4x4x8**

IOU1 (IIO PCIe Br2)
Selects PCIe port Bifurcation for PCIE_3 slot
x4x4x4x4 / x8x8 / **x16**

IOU2 (IIO PCIe Br3)
Selects PCIe port Bifurcation for PCIE_1 slot
x4x4x4x4 / x8x8 / **x16**

Socket 0 PcieBr1D00F0 – Port 1A
Settings related to PCI Express PortS
(0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

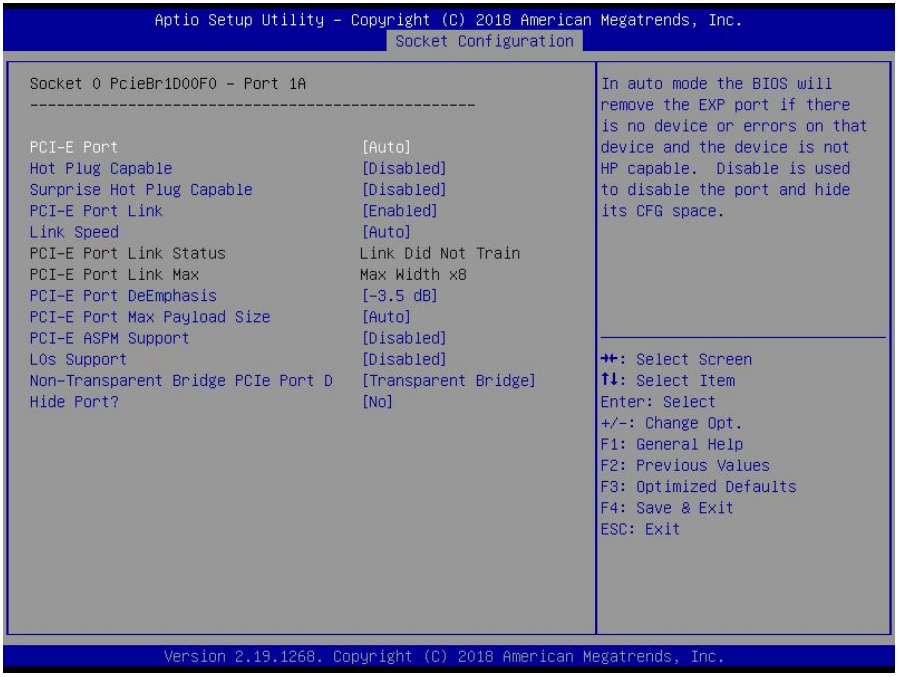
Socket 0 PcieBr1D02F0 – Port 1C
Settings related to PCI Express PortS
(0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

Socket 0 PcieBr1D03F0 – Port 1D
Settings related to PCI Express PortS (0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

Socket 0 PcieBr2D00F0 – Port 2A
Settings related to PCI Express PortS (0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

Socket 0 PcieBr3D00F0 – Port 3A
Settings related to PCI Express PortS (0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

3.5.5.1.1 Socket0 - Port 1A Submenu



PCI-E Port
In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its DFG space.

Auto / Disabled / Enabled

Hot Plug Capable
This option specifies if the link is considered Hot Plug capable.
Disabled / Enabled

Surprise Hot Plug Capable
This option specifies if the link is considered Surprise Hot Plug capable
Disabled / Enabled

PCI-E Port Link
This option disables the Link so that the no training occurs but the DFG space is still active
Disabled / **Enabled**

Link Speed
Choose Link Speed for this PCIe port
Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis
De-Emphais control (LNKCON2[6]) for this PCIe port.
-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size
Set Maxpayload size to 256B if possible
128B / 256B **/ Auto**

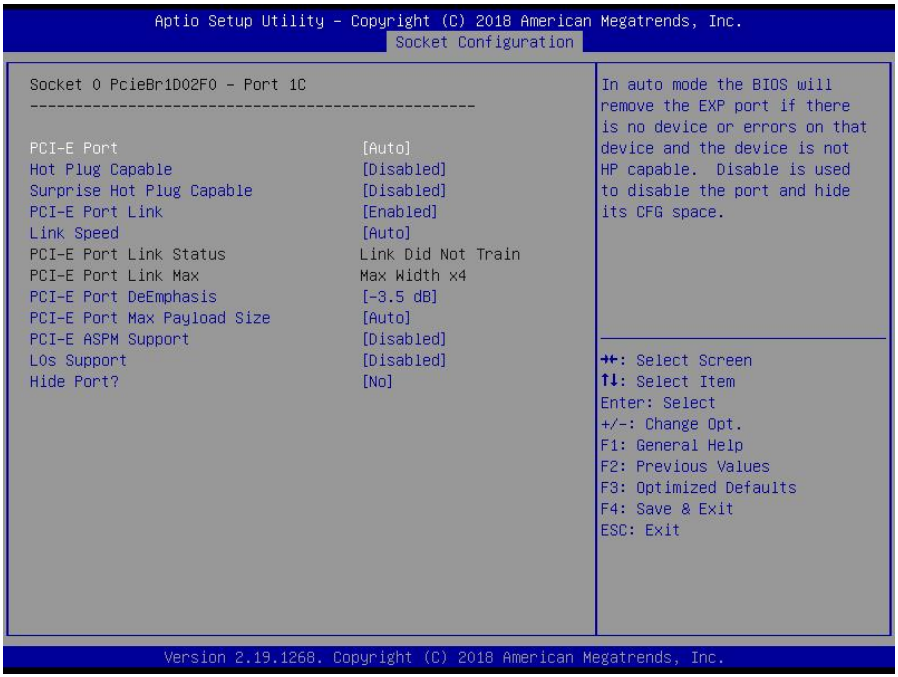
PCI-E ASPM Support
This option enables / disables the ASPM (L1) support for the downstream devices.
Auto / L1 Only / **Disabled**

L0s Support
When disabled, IIO never puts its transmitter in L0s state
Disabled / Enabled

Non-Transparent Bridge PCIe Port Definition
Configures port as TB, NTB-NTB, or NTB-RP
Transparent Bridge / NTB to NTB / NTB to RP

Hide Port
User can force to hide this root port from OS
NO / Yes

3.5.5.1.2 Socket0 - Port 1C Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed
Choose Link Speed for this PCIe port
Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis
De-Emphais control (LNKCON2[6]) for this PCIe port.
-6.0 dB **/ -3.5 dB**

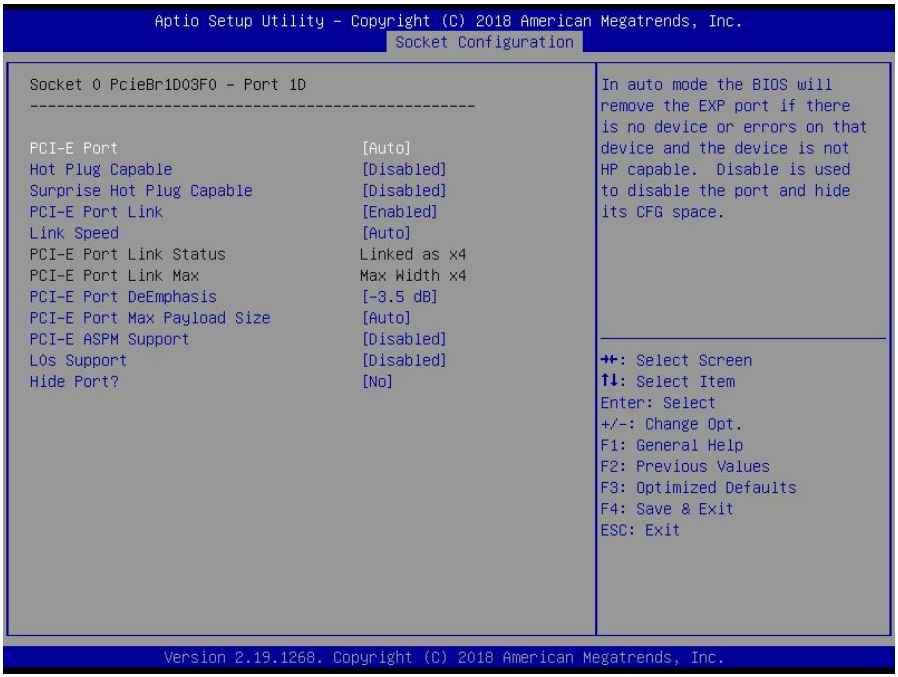
PCI-E Port Max Payload Size
Set Maxpayload size to 256B if possible
128B / 256B **/ Auto**

PCI-E ASPM Support
This option enables / disables the ASPM (L1) support for the downstream devices.
Auto / L1 Only / **Disabled**

L0s Support
When disabled, IIO never puts its transmitter in L0s state
Disabled / Enabled

Hide Port
User can force to hide this root port from OS
NO / Yes

3.5.5.1.3 Socket0 - Port 1D Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed
Choose Link Speed for this PCIe port
Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis
De-Emphais control (LNKCON2[6]) for this PCIe port.
-6.0 dB **/ -3.5 dB**

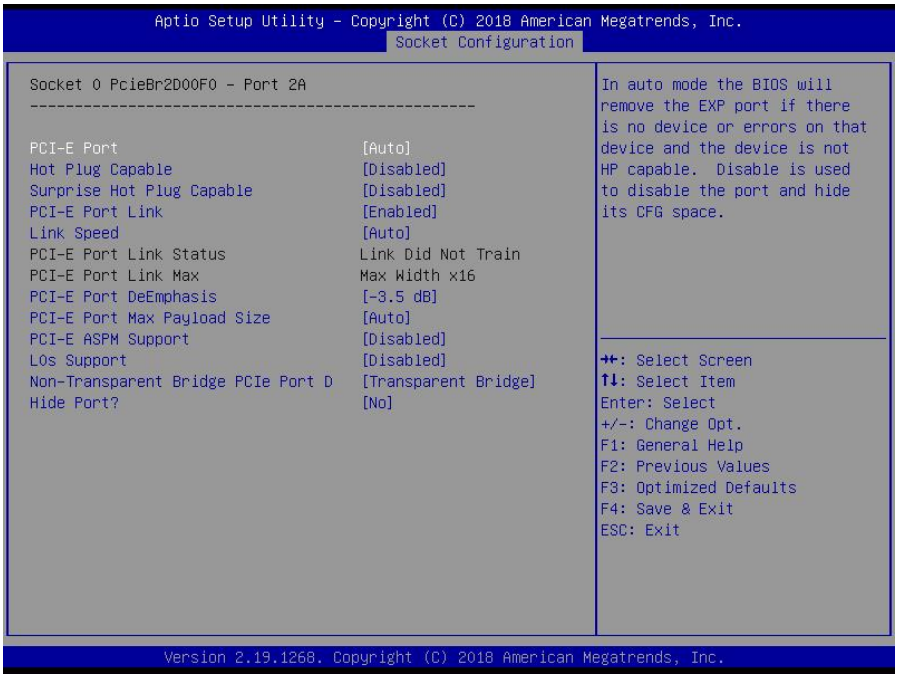
PCI-E Port Max Payload Size
Set Maxpayload size to 256B if possible
128B / 256B **/ Auto**

PCI-E ASPM Support
This option enables / disables the ASPM (L1) support for the downstream devices.
Auto / L1 Only / **Disabled**

L0s Support
When disabled, IIO never puts its transmitter in L0s state
Disabled / Enabled

Hide Port
User can force to hide this root port from OS
NO / Yes

3.5.5.1.4 Socket0 - Port 2A Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed

Choose Link Speed for this PCIe port

Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis

De-Emphais control (LNKCON2[6]) for this PCIe port.

-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size

Set Maxpayload size to 256B if possible

128B / 256B **/ Auto**

PCI-E ASPM Support

This option enables / disables the ASPM (L1) support for the downstream devices.

Auto / L1 Only / **Disabled**

L0s Support

When disabled, IIO never puts its transmitter in L0s state

Disabled / Enabled

Non-Transparent Bridge PCIe Port Definition

Configures port as TB, NTB-NTB, or NTB-RP

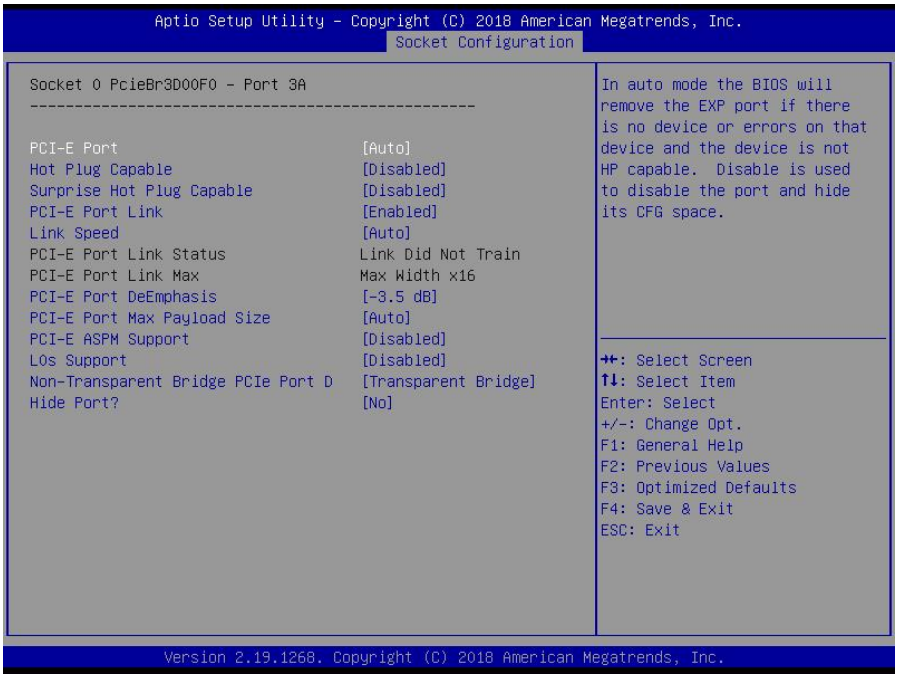
Transparent Bridge / NTB to NTB / NTB to RP

Hide Port

User can force to hide this root port from OS

NO / Yes

3.5.5.1.5 Socket0 - Port 3A Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed

Choose Link Speed for this PCIe port

Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis

De-Emphais control (LNKCON2[6]) for this PCIe port.

-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size

Set Maxpayload size to 256B if possible

128B / 256B **/ Auto**

PCI-E ASPM Support

This option enables / disables the ASPM (L1) support for the downstream devices.

Auto / L1 Only / **Disabled**

L0s Support

When disabled, IIO never puts its transmitter in L0s state

Disabled / Enabled

Non-Transparent Bridge PCIe Port Definition

Configures port as TB, NTB-NTB, or NTB-RP

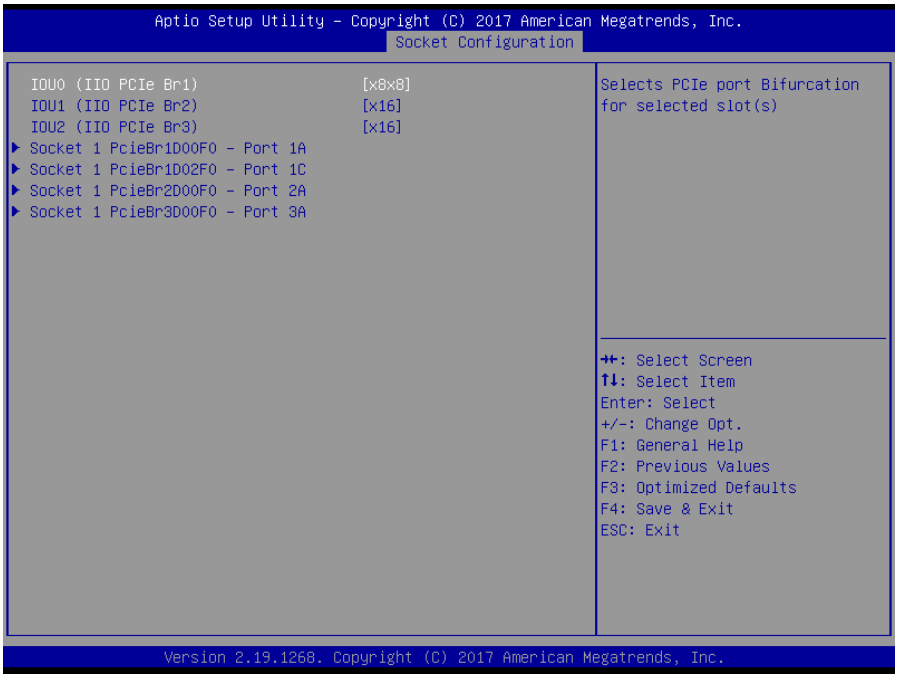
Transparent Bridge / NTB to NTB / NTB to RP

Hide Port

User can force to hide this root port from OS

NO / Yes

3.5.5.2 Socket1 Submenu



IOU0 (IIO PCIe Br1)
Select PCIe port Bifurcation for PCIE_4 slot/ PCIE_6 slots
x4x4x4x4 / x4x4x8 / x8x4x4 / **x8x8**

IOU1 (IIO PCIe Br2)
Selects PCIe port Bifurcation for PCIE_7 slot
x4x4x4x4 / x8x8 / **x16**

IOU2 (IIO PCIe Br3)
Selects PCIe port Bifurcation for PCIE_5 slot
x4x4x4x4 / x8x8 / **x16**

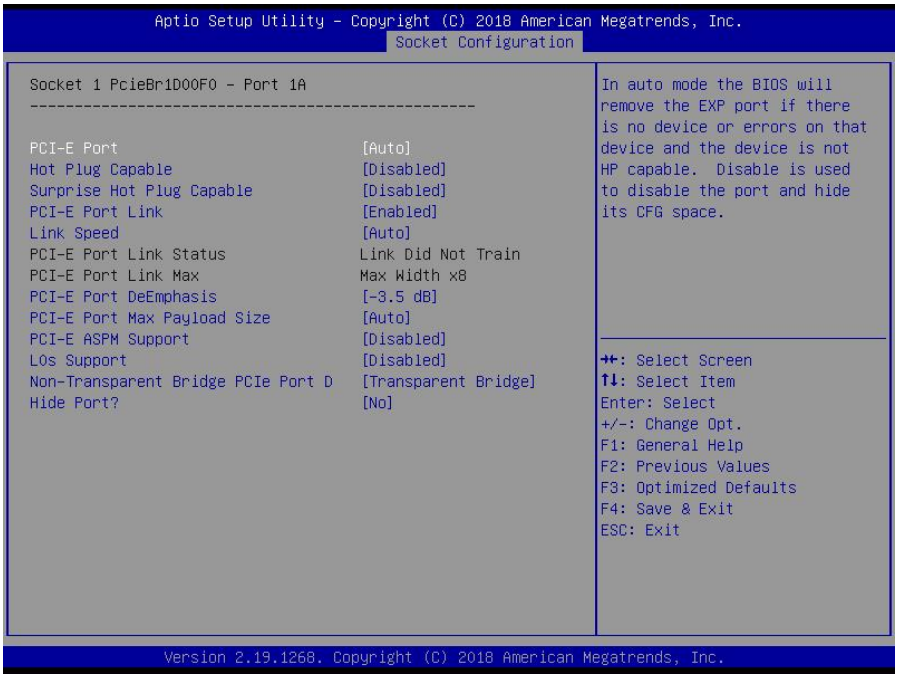
Socket 1 PcieBr1D00F0 – Port 1A
Settings related to PCI Express PortS
(0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

Socket 1 PcieBr1D02F0 – Port 1C
Settings related to PCI Express PortS
(0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

Socket 1 PcieBr2D00F0 – Port 2A
Settings related to PCI Express PortS
(0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

Socket 1 PcieBr3D00F0 – Port 3A
Settings related to PCI Express PortS
(0/1A/1B/1C/1D/2A/2B/2C/2D/3A/3B/3C/3D/4A/5A)

3.5.5.2.1 Socket1 - Port 1A Submenu



PCI-E Port
In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its DFG space.

Auto / Disabled / Enabled

Hot Plug Capable
This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable
This option specifies if the link is considered Surprise Hot Plug capable
Disabled / Enabled

PCI-E Port Link
This option disables the Link so that the no training occurs but the DFG space is still active
Disabled / **Enabled**

Link Speed
Choose Link Speed for this PCIe port
Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis
De-Emphais control (LNKCON2[6]) for this PCIe port.
-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size
Set Maxpayload size to 256B if possible
128B / 256B **/ Auto**

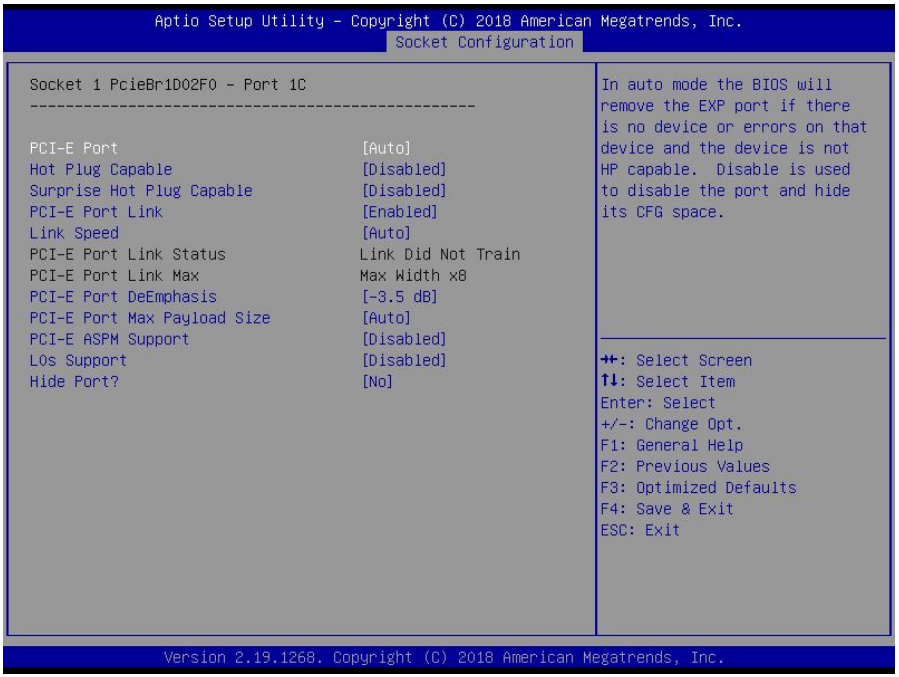
PCI-E ASPM Support
This option enables / disables the ASPM (L1) support for the downstream devices.
Auto / L1 Only / **Disabled**

L0s Support
When disabled, IIO never puts its transmitter in L0s state
Disabled / Enabled

Non-Transparent Bridge PCIe Port Definition
Configures port as TB, NTB-NTB, or NTB-RP
Transparent Bridge / NTB to NTB / NTB to RP

Hide Port
User can force to hide this root port from OS
NO / Yes

3.5.5.2.2 Socket1 - Port 1C Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed

Choose Link Speed for this PCIe port

Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis

De-Emphais control (LNKCON2[6]) for this PCIe port.

-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size

Set Maxpayload size to 256B if possible

128B / 256B **/ Auto**

PCI-E ASPM Support

This option enables / disables the ASPM (L1) support for the downstream devices.

Auto / L1 Only / **Disabled**

L0s Support

When disabled, IIO never puts its transmitter in L0s state

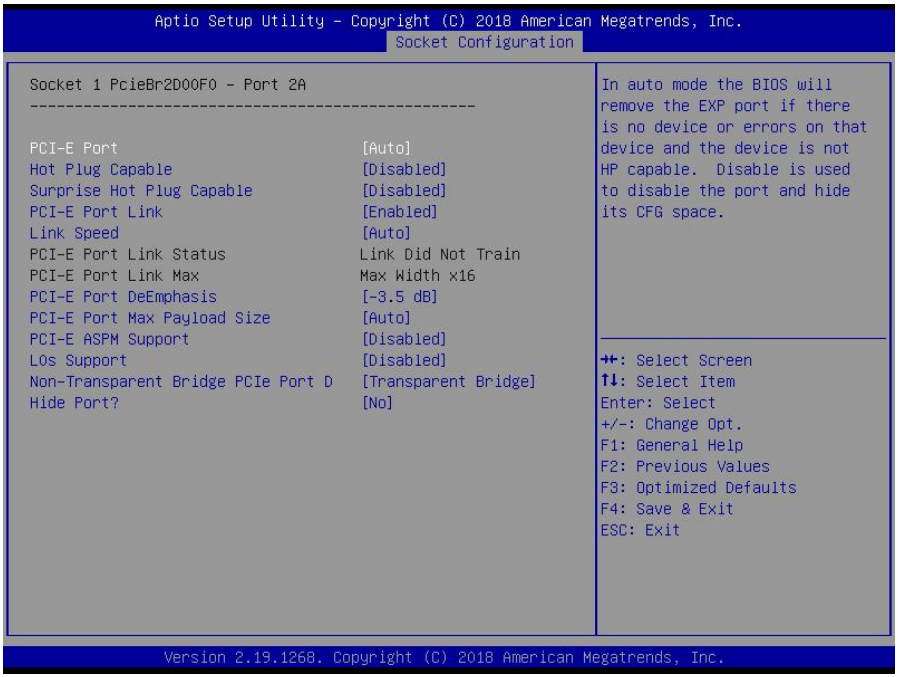
Disabled / Enabled

Hide Port

User can force to hide this root port from OS

NO / Yes

3.5.5.2.3 Socket1 - Port 2A Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed

Choose Link Speed for this PCIe port

Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis

De-Emphais control (LNKCON2[6]) for this PCIe port.

-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size

Set Maxpayload size to 256B if possible

128B / 256B **/ Auto**

PCI-E ASPM Support

This option enables / disables the ASPM (L1) support for the downstream devices.

Auto / L1 Only / **Disabled**

L0s Support

When disabled, IIO never puts its transmitter in L0s state

Disabled / Enabled

Non-Transparent Bridge PCIe Port Definition

Configures port as TB, NTB-NTB, or NTB-RP

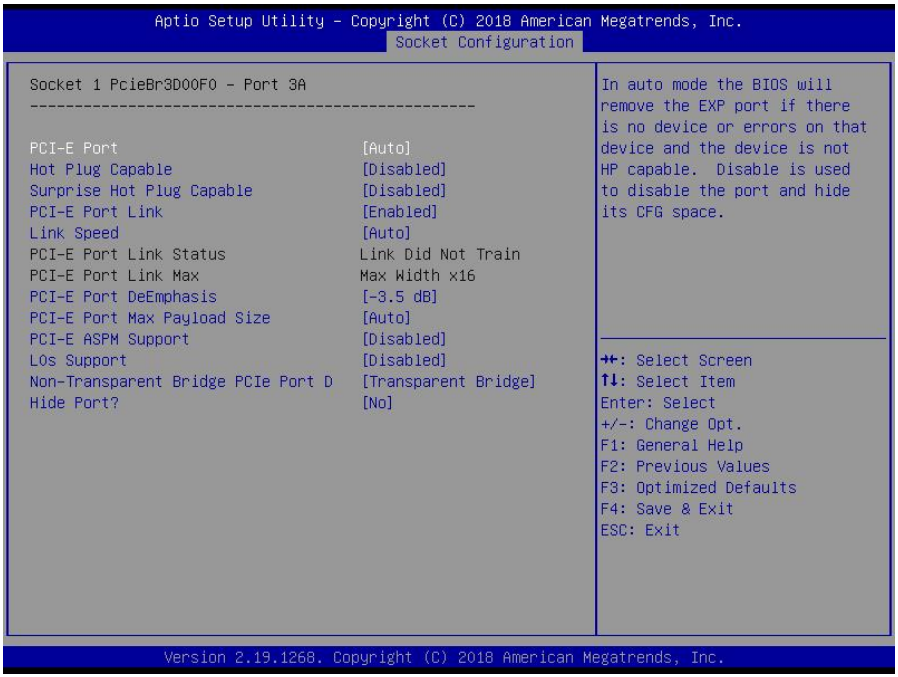
Transparent Bridge / NTB to NTB / NTB to RP

Hide Port

User can force to hide this root port from OS

NO / Yes

3.5.5.2.4 Socket1 - Port 3A Submenu



PCI-E Port

In auto mode the BIOS will remove the EXP port if there is no device or errors on that device and the device is not HP capable. Disable is used to disable the port and hide its CFG space.

Auto / Disabled / Enabled

Hot Plug Capable

This option specifies if the link is considered Hot Plug capable.

Disabled / Enabled

Surprise Hot Plug Capable

This option specifies if the link is considered Surprise Hot Plug capable

Disabled / Enabled

PCI-E Port Link

This option disables the Link so that the no training occurs but the DFG space is still active

Disabled / **Enabled**

Link Speed

Choose Link Speed for this PCIe port

Auto / Gen1 (2.5GT/s) / Gen2 (5GT/s) / Gen3 (8 GT/s)

PCI-E Port DeEmphasis

De-Emphais control (LNKCON2[6]) for this PCIe port.

-6.0 dB **/ -3.5 dB**

PCI-E Port Max Payload Size

Set Maxpayload size to 256B if possible

128B **/** 256B **/ Auto**

PCI-E ASPM Support

This option enables / disables the ASPM (L1) support for the downstream devices.

Auto / L1 Only / **Disabled**

L0s Support

When disabled, IIO never puts its transmitter in L0s state

Disabled / Enabled

Non-Transparent Bridge PCIe Port Definition

Configures port as TB, NTB-NTB, or NTB-RP

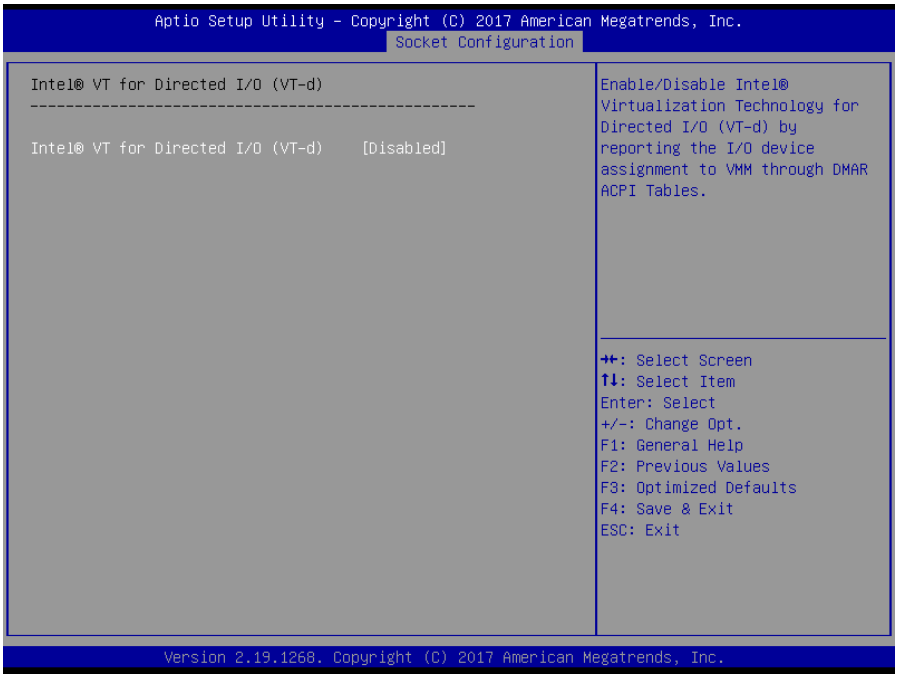
Transparent Bridge / NTB to NTB / NTB to RP

Hide Port

User can force to hide this root port from OS

NO / Yes

3.5.5.3 Intel® VT for Directed I/O (VT-d) Submenu

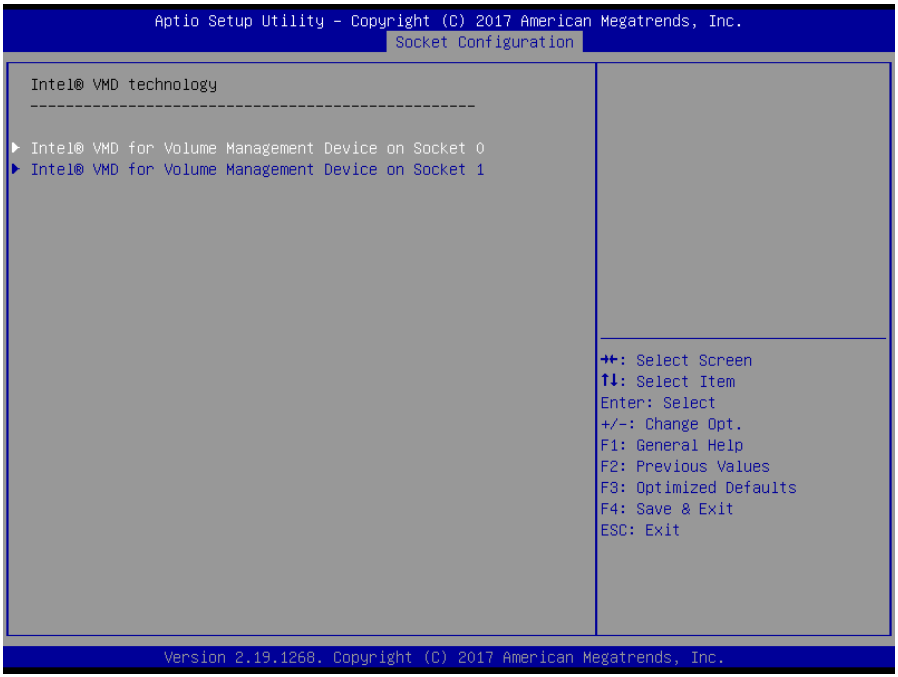


Intel® VT for Directed I/O (VT-d)

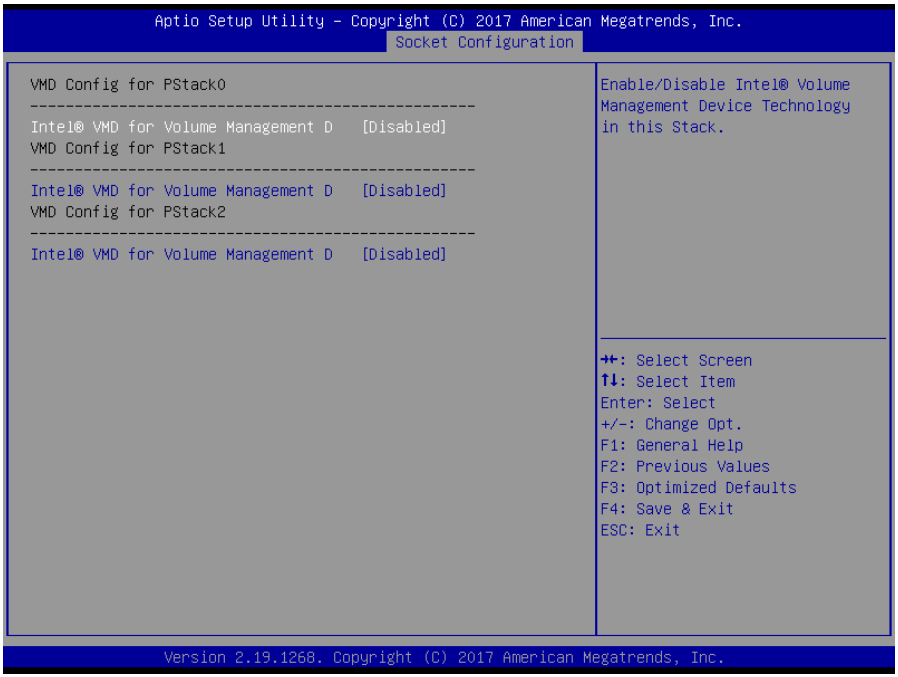
Enable/Disable Intel® Virtualization Technology for Directed I/O (VT-d) by reporting the I/O device assignment to VMM through DMAR ACPI Tables.

Disabled / Enabled

3.5.5.4 Intel® VMD technology Submenu

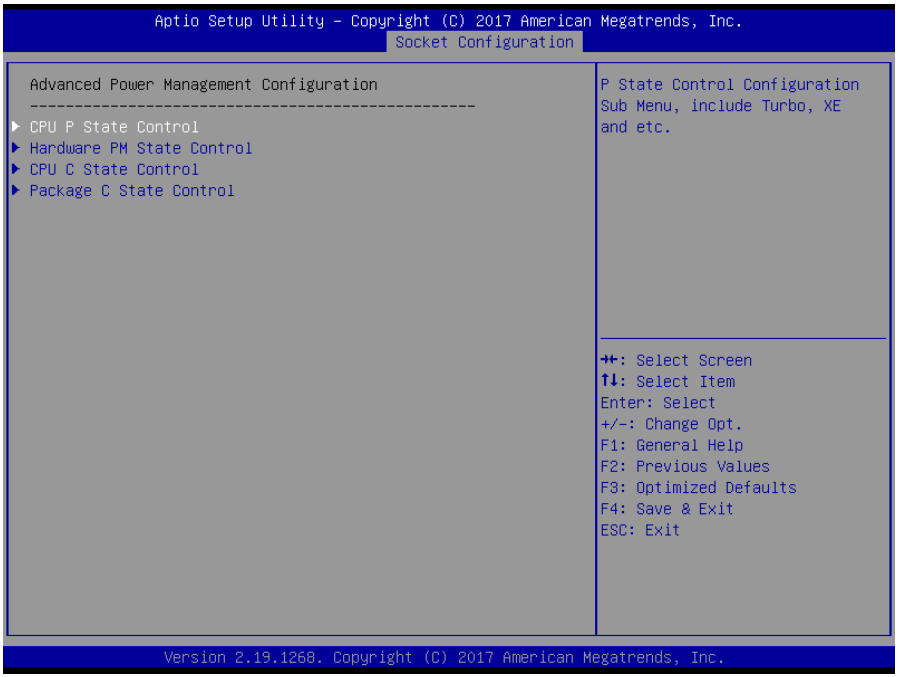


3.5.5.4.1 Intel® VMD for Volume Management Socket0/1 Submenu



VMD Config for PStack 0/1/2
Intel® VMD for Volume Management D
Enable/Disable Intel® Volume Management Device Technology in this Stack.
Disabled / Enabled

3.5.5 Advance Power Management Configuration



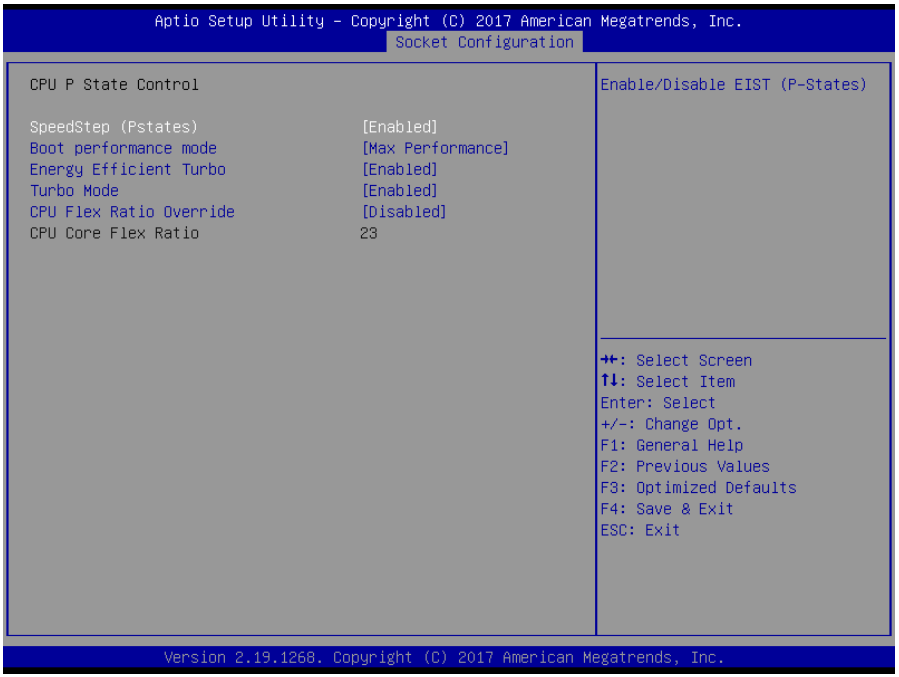
CPU P State Control
P State Control Configuration Sub Menu, include Turbo, XE and etc.

Hardware PM State Control
Hardware P-State setting

CPU C State Control
CPU C State setting

Package C State Control
Package C State setting

3.5.5.1 CPU P State Control Submenu



SpeedStep (Pstates)
Enable/Disable EIST (P-States)
Disabled / **Enabled**

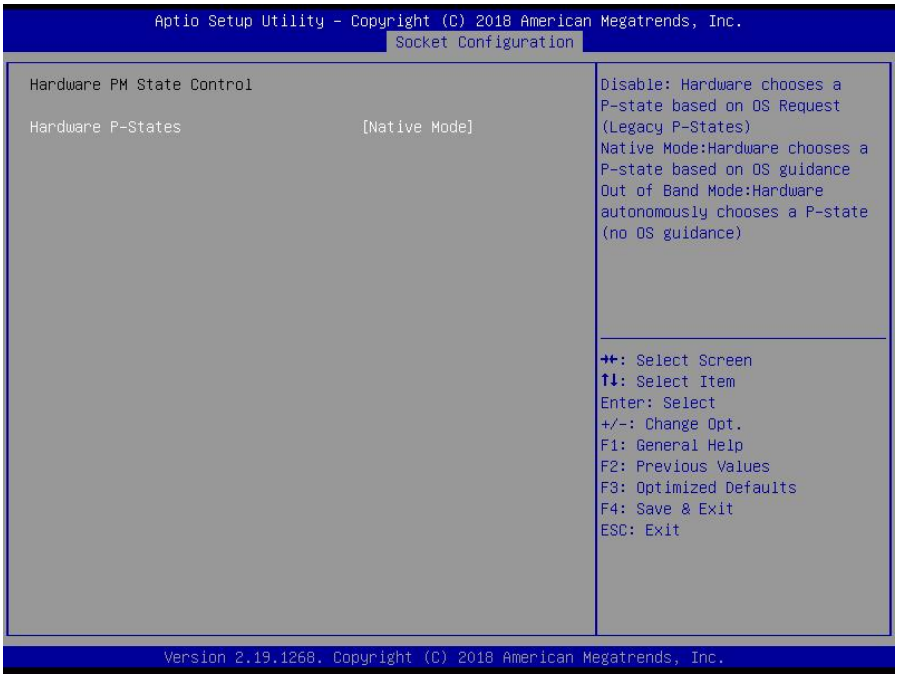
Boot performance mode
Select the performance state that the BIOS will set before OS hand off.
Max Performance / Max Efficient / Set by Intel Node

Energy Efficient Turbo
Energy Efficient Turbo Disable, MSR 0x1FC [19]
Disabled / **Enabled**

Turbo Mode
Enable/Disable processor Turbo Mode (requires EMTTM enabled too).
Disabled / **Enabled**

CPU Flex Ratio Override
Enable/Disable CPU Flex Ratio Programming
Disabled / Enabled

3.5.5.2 Hardware PM State Control Submenu

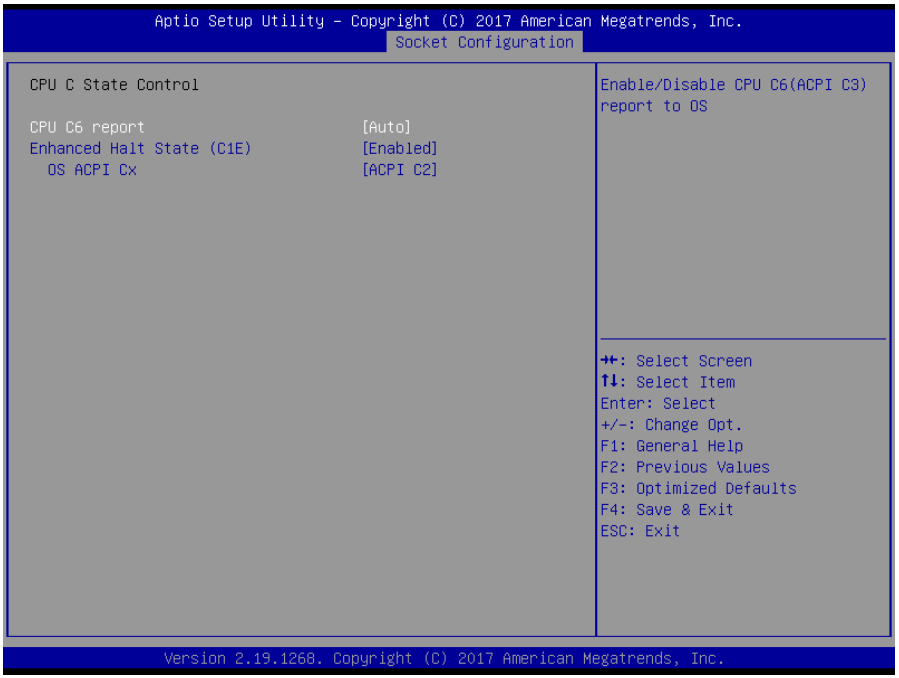


Hardware P-States

Disable: Hardware choose a P-state based on OS Request (Legacy P-States)
Native Mode: Hardware choose a P-state based on OS guidance
Out of Band Mode: Hardware autonomously choose a P-state (No OS guidance)

Disable / **Native Mode** / Out of Band Mode

3.5.5.3 CPU C State Control Submenu

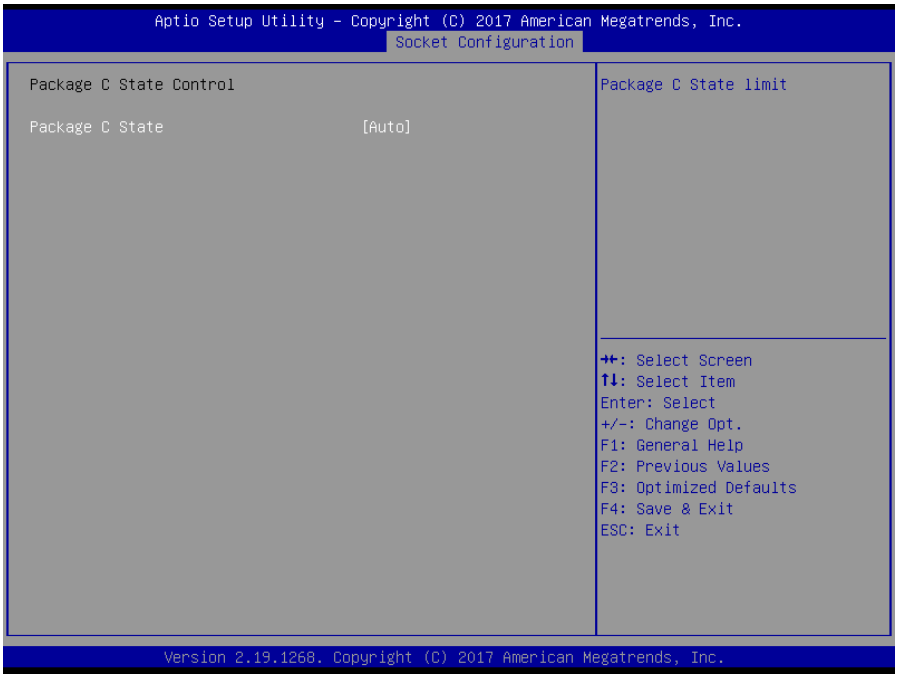


CPU C6 report
Enable/Disable CPU C6(ACPI C3) report to OS
Auto / Enable / Disable

Enhanced Halt State (C1E)
Enables the Enhanced C1E state of the CPU, takes effect after reboot
Enabled / Disabled

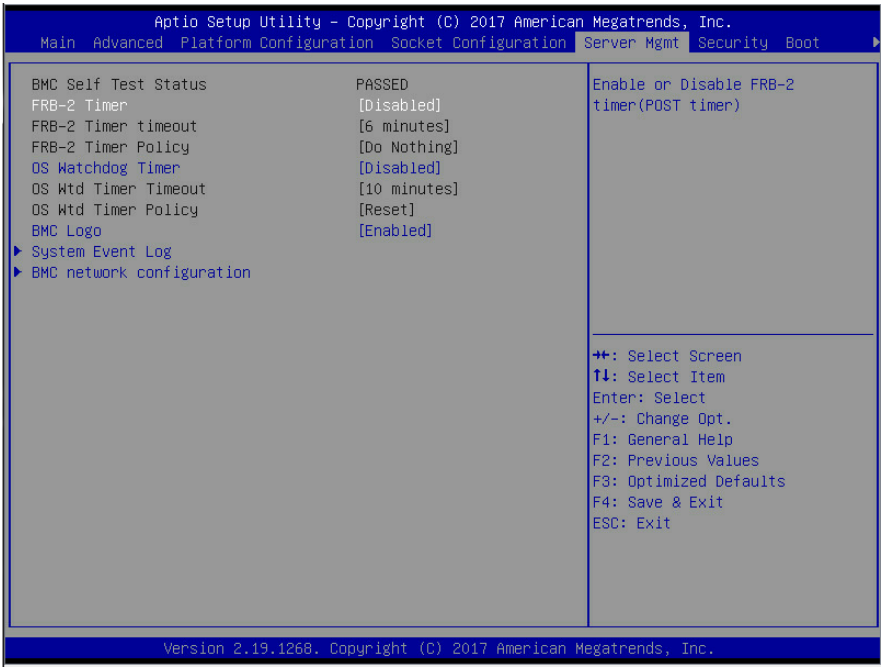
OS ACPI Cx
Report CC3/CC6 to OS ACPI C2 or ACPI C3
ACPI C2 / ACPI C3

3.5.5.4 Package C State Control Submenu



Package C State
Package C State Limit
C0/C1 state / C2 state / C6(non Retention) state / C6(Retention) state / No Limit / **Auto**

3.6 Server Management



FRB-2 Timer

Enable or Disable FRB-2 timer (POST timer)

Disabled / Enabled

NOTE: When [FRB-2 Timer] is set to [Enabled], the following items will be available.

FRB-2 Timer timeout

Enter value Between 3 to 6 min for FRB-2 Timer Expiration value

3 minutes **/** 4 minutes **/** 5 minutes **/ 6 minutes**

FBR-2 Timer Policy

Configure how the system should respond if the FRB-2 Timer expires. Not available if FRB-2 Timer is disabled.

Do Nothing / Reset / Power Down / Power Cycle

OS Watchdog Timer

If enabled, starts a BIOS timer which can only be shut off by management Software after the OS loads. Helps determine that the OS successfully loaded or follows the OS Boot Watchdog Timer policy.

Disabled / Enabled

NOTE: When [OS Watchdog Timer] is set to [Enabled], the following items will be available.

OS Wtd Timer Timeout
Configure the length of the OS Boot Watchdog Timer. Not available if OS Boot Watchdog Timer is disabled.
5 minutes **/ 10 minutes / 1**5 minutes **/** 20 minutes

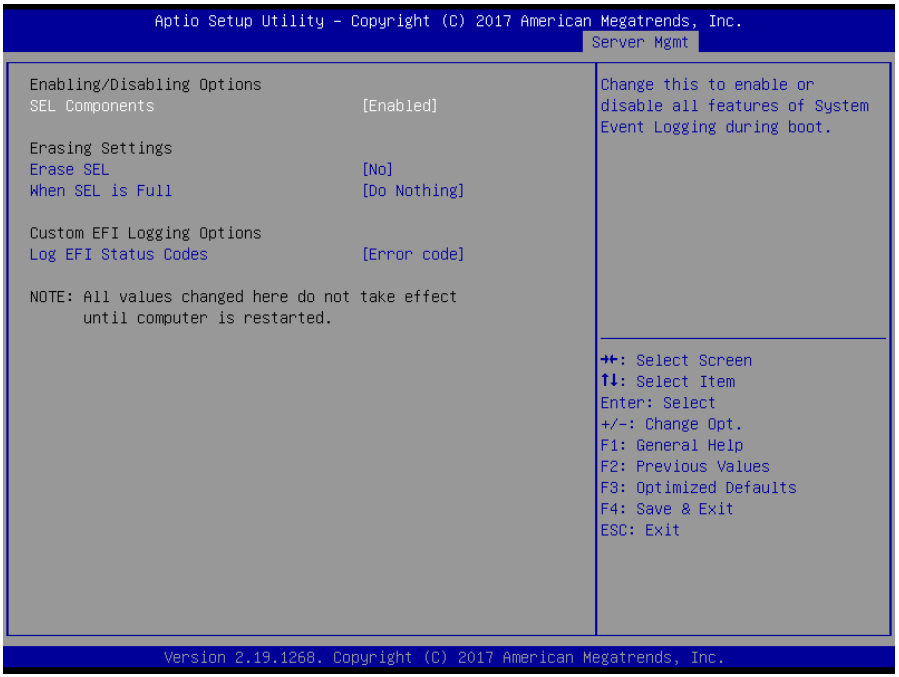
OS Wtd Timer Policy
Configure how the system should respond if the OS Boot Watchdog Timer expires. Not available if OS Boot Watchdog Timer is disabled.
Do Nothing **/ Reset /** Power Down **/** Power Cycle

BMC Logo
Enable or Disable BMC logo
Disabled / **Enabled**

System Event Log
Press<Enter> to change the SEL event log configuration.

BMC network configuration
Configure BMC network parameters

3.6.1 System Event Log Submenu



SEL Components

Change this to enable or disable all features of System Event Logging during boot.

Enabled / Disabled

Erase SEL

Choose options for erasing SEL.

No / Yes, on next reset / No, on every reset

When SEL is Full

Choose options for reactions to a full SEL.

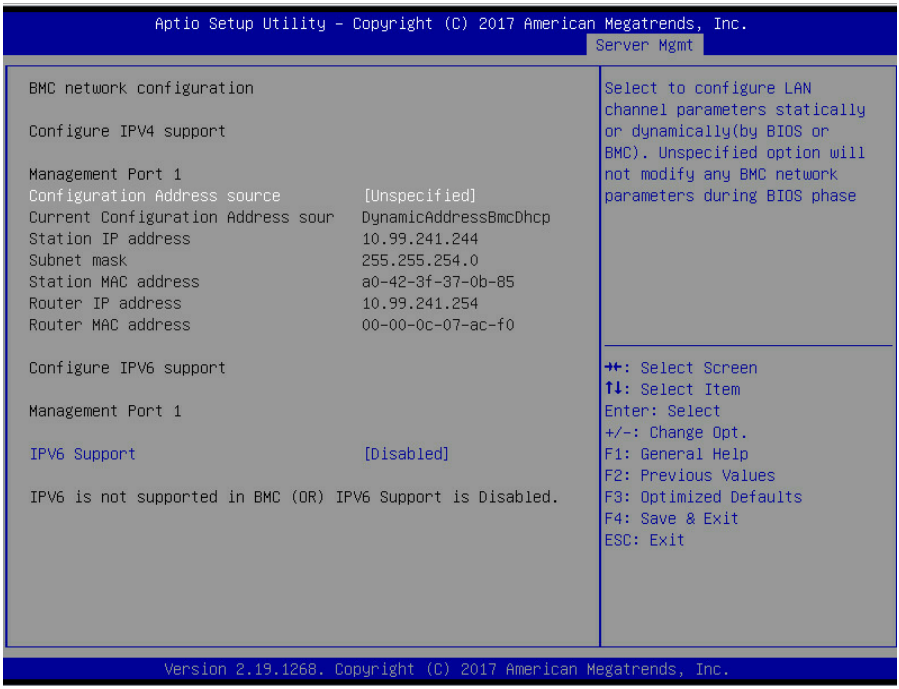
Do Nothing / Erase Immediately

Log EFI Status Codes

Disable the logging of EFI Status Codes or log only error code or only progress code or both.

Both / Disabled / **Error Code** / Progress Code

3.6.2 BMC Network Configuration Submenu



Configuration Address Source

Select the configure LAN channel parameters statically or dynamically (by BIOS or BMC). Unspecified option will not modify any BMC network parameters during BIOS phase.

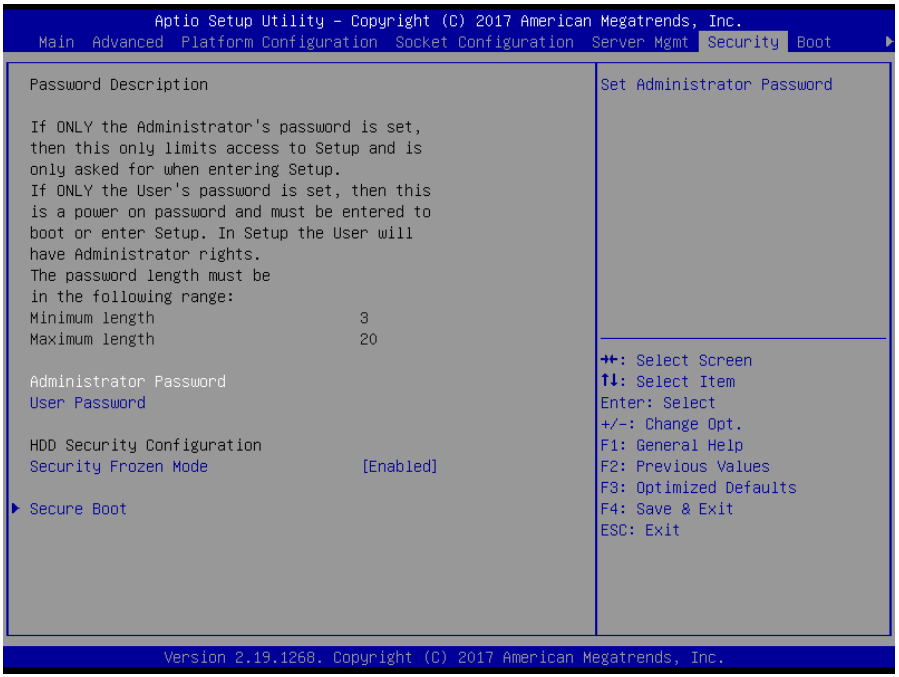
Unspecified / Static / DynamicBmcDhcp / DynamicBmcNonDhcp

IPV6 Support

Enable or Disable LAN1 IPV6 Support

Disabled / Enabled

3.7 Security



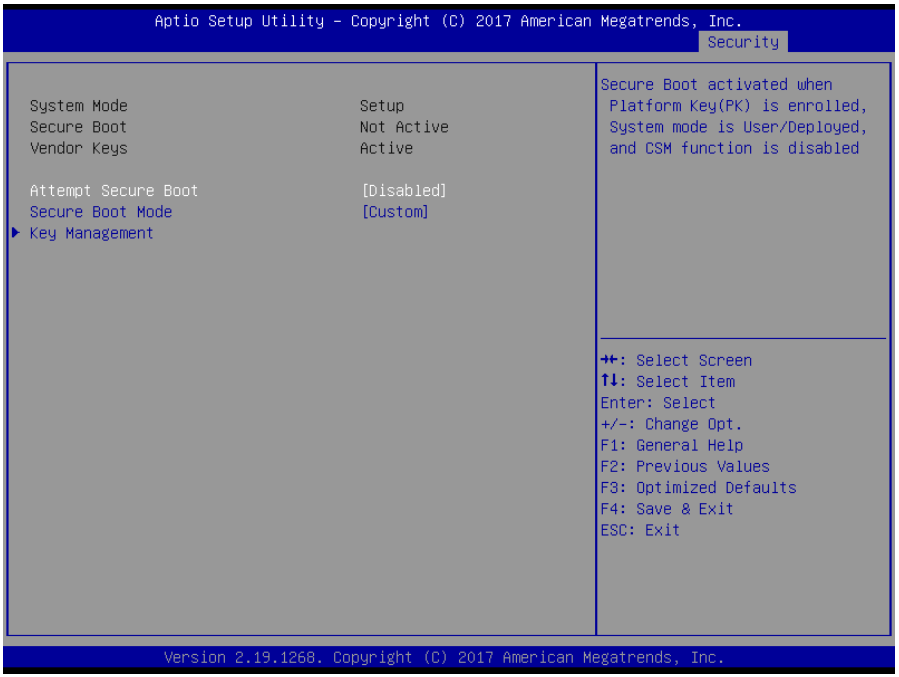
Administrator Password
Set Administrator Password.

User Password
Set User Password.

Security Frozen Mode
Enable or disable HDD security freeze lock.
Disable to support secure erase function.
Disabled / **Enabled**

Secure Boot
Customizable Secure Boot settings

3.7.1 Secure Boot Configuration Submenu

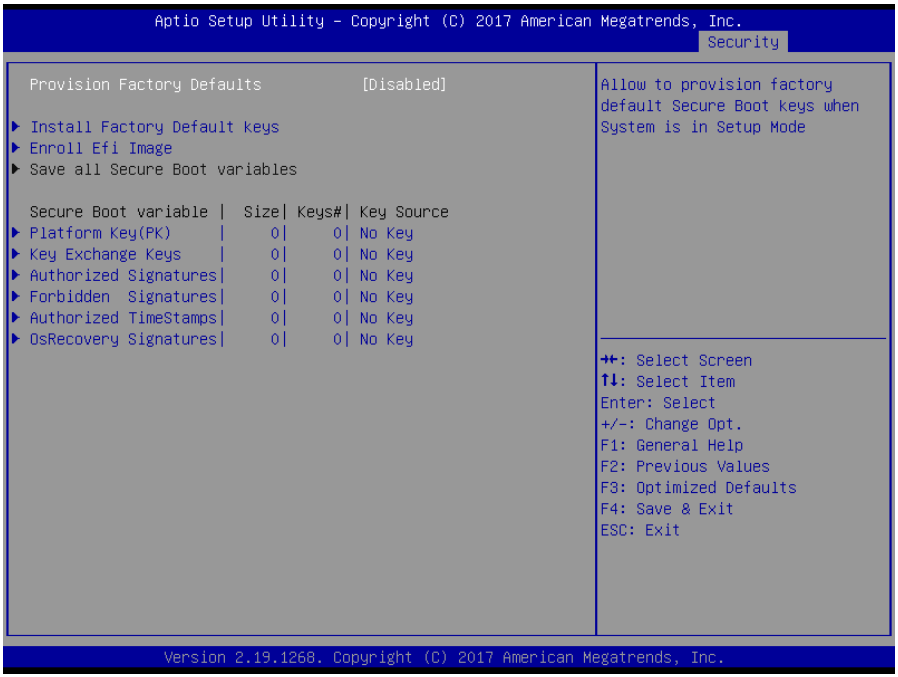


Attempt Secure Boot
Secure boot activated when Platform Key(PK) is enrolled,
System mode is User/Deployed, and CSM function is disabled
Enabled / **Disabled**

Secure Boot Mode
Secure Boot mode selector. 'Custom' mode enables users to change Image execution policy and manage secure boot keys.
Standard / **Custom**

Key Management
Enables experienced users to modify Secure Boot variables

3.7.2 Key Management



Provision Factory Default Keys
Install factory default Secure Boot Keys when System is in Setup Mode.
Enabled / **Disabled**

Install Factory Default Keys
Force System to User Mode-install all Factory Default keys

Enroll Efi Image
Allow the image to run in Secure Boot mode. Enroll SHA256 hash of the binary into Autorized Signature Database (db)

Platform Key (PK)
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER encoded)
c) EFI_CERT_RSA2048 (bin)
d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable

3. EFI PE/COFF Image(SHA256)
Key Source:
Default, External, Mixed, Test
Set New

Key Exchange Keys
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER encoded)
c) EFI_CERT_RSA2048 (bin)
d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable
3. EFI PE/COFF Image(SHA256)
Key Source:
Default, External, Mixed, Test

Authorized Signatures
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER encoded)
c) EFI_CERT_RSA2048 (bin)
d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable
3. EFI PE/COFF Image(SHA256)
Key Source:
Default, External, Mixed, Test

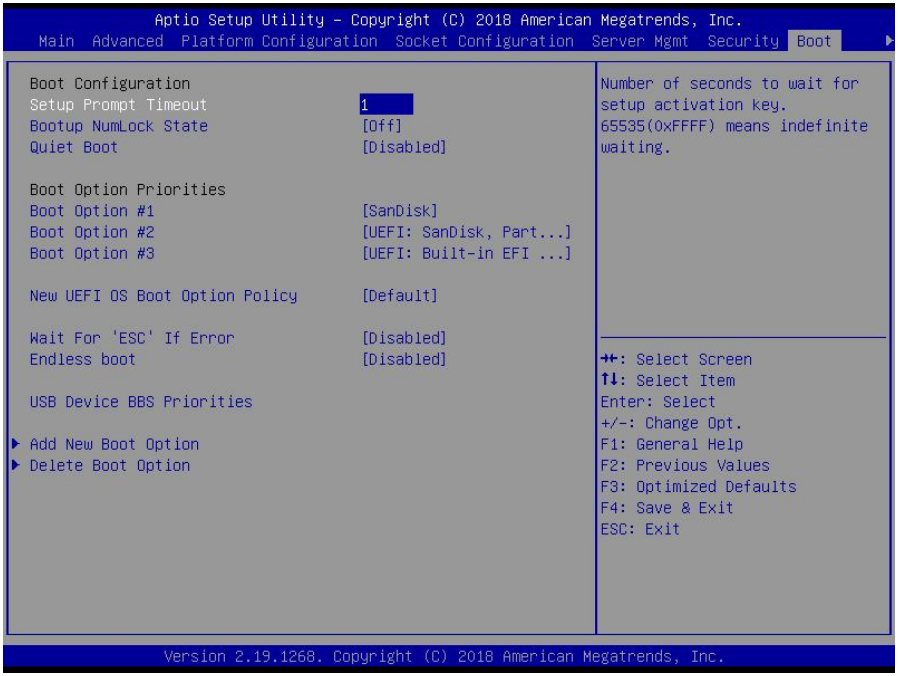
Forbidden Signatures
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER encoded)
c) EFI_CERT_RSA2048 (bin)
d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable
3. EFI PE/COFF Image(SHA256)
Key Source:
Default, External, Mixed, Test

Authorized TimeStamps
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER encoded)
c) EFI_CERT_RSA2048 (bin)

d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable
3. EFI PE/COFF Image(SHA256)
Key Source:
Default, External, Mixed, Test

OsRecovery Signatures
Enroll Factory Defaults or load certificates from a file:
1. Public Key Certificate in:
a) EFI_SIGNATURE_LIST
b) EFI_CERT_X509 (DER encoded)
c) EFI_CERT_RSA2048 (bin)
d) EFI_CERT_SHA256,384,512
2. Authenticated UEFI Variable
3. EFI PE/COFF Image(SHA256)
Key Source:
Default, External, Mixed, Test

3.8 Boot



Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535 (0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Off / On

Quiet Boot

Enable or disable Quiet Boot option.

Disabled / Enabled

Boot Option Priorities

Boot Option #1 #2 #3

Sets the system boot order.

Device Name / Disabled

New UEFI OS Boot Option Policy

Controls the placement of newly detected UEFI boot options.

Default / Place First / Place Last

Wait For "ESC" If Error

Wait for "ESC" key to be pressed if error occurs.

Disabled / Enabled

Endless Boot

Continuously searches for the Legacy PXE boot image until it is found or the process is aborted (press Ctrl+Alt+Del).

Disabled / Enabled

Hard Drive BBS Priorities

Set the order of the legacy devices in this group

USB Device BBS priorities

Set the order of the legacy devices in this group

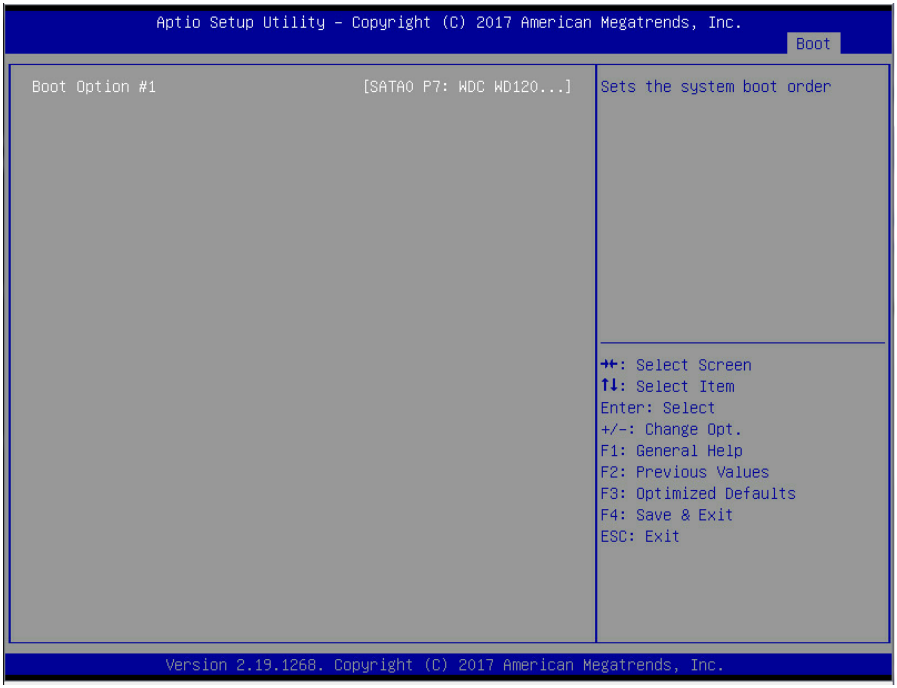
Add New Boot Options

Add a new EFI boot option to the boot order

Delete Boot Option

Remove an EFI boot option from the boot order

3.8.1 Hard Drive BBS Priorities Configuration

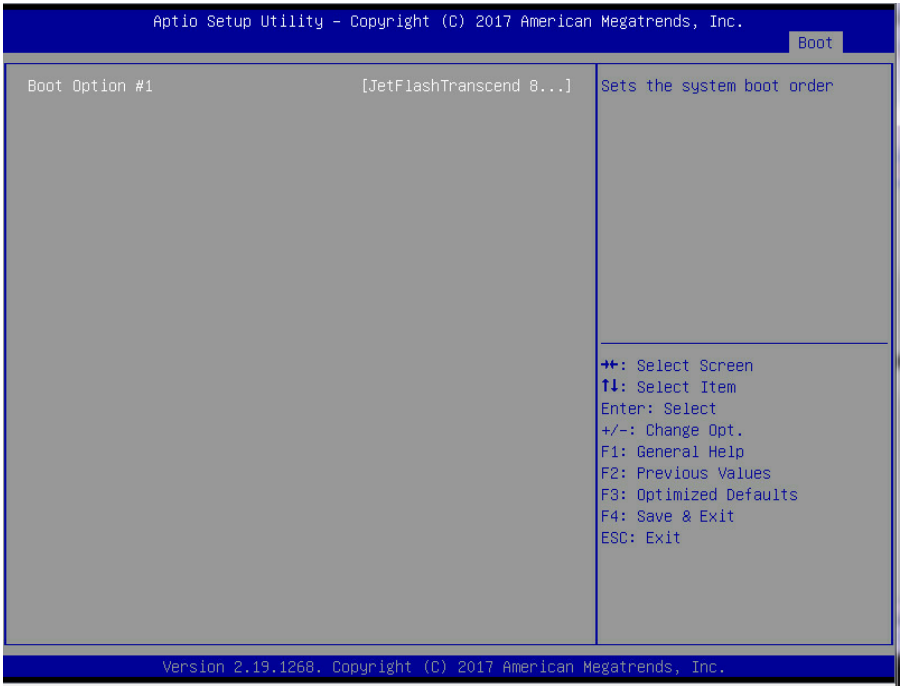


Boot Option #1

Sets the system boot order

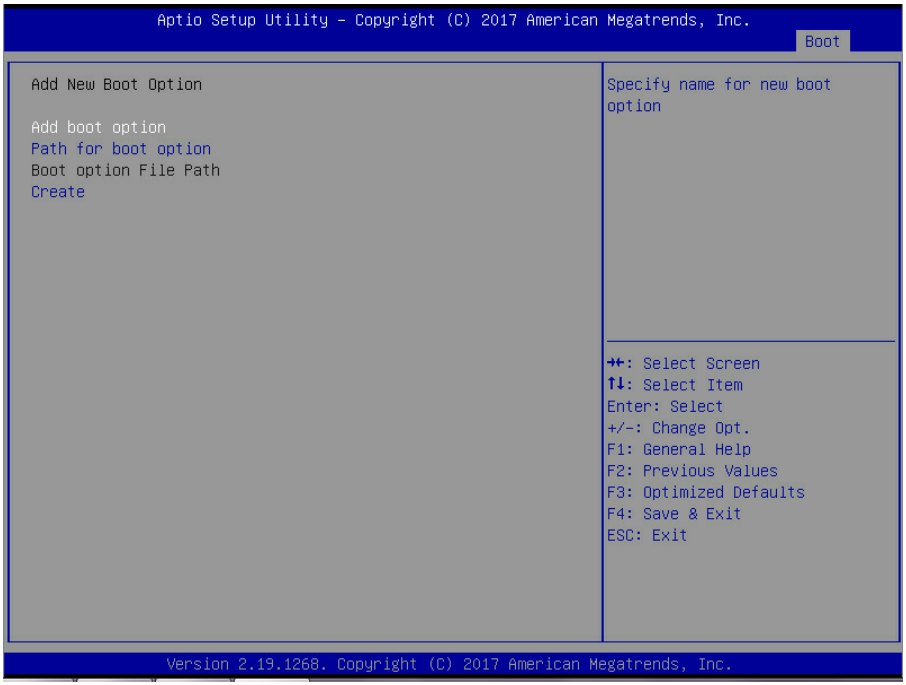
Device Name / Disabled

3.8.2 USB Device BBS Priorities Configuration



Boot Option #1
Sets the system boot order
Device Name / Disabled

3.8.3 Add New Boot Option Configuration

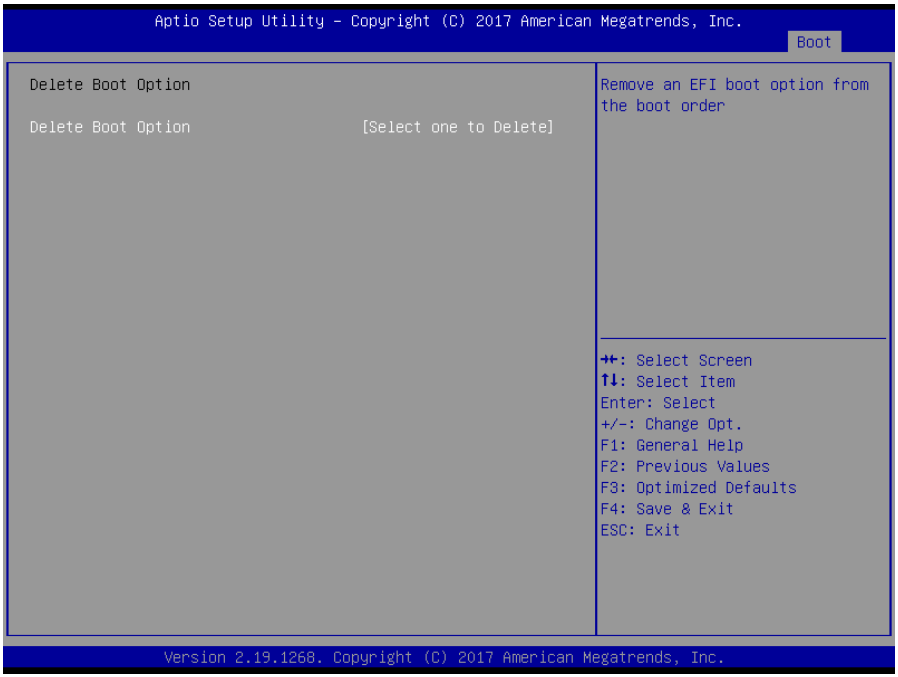


Add boot option
Specify name for new boot option

Path for boot option
Enter the path to the boot option in the format Fsx:\path\filename.efi

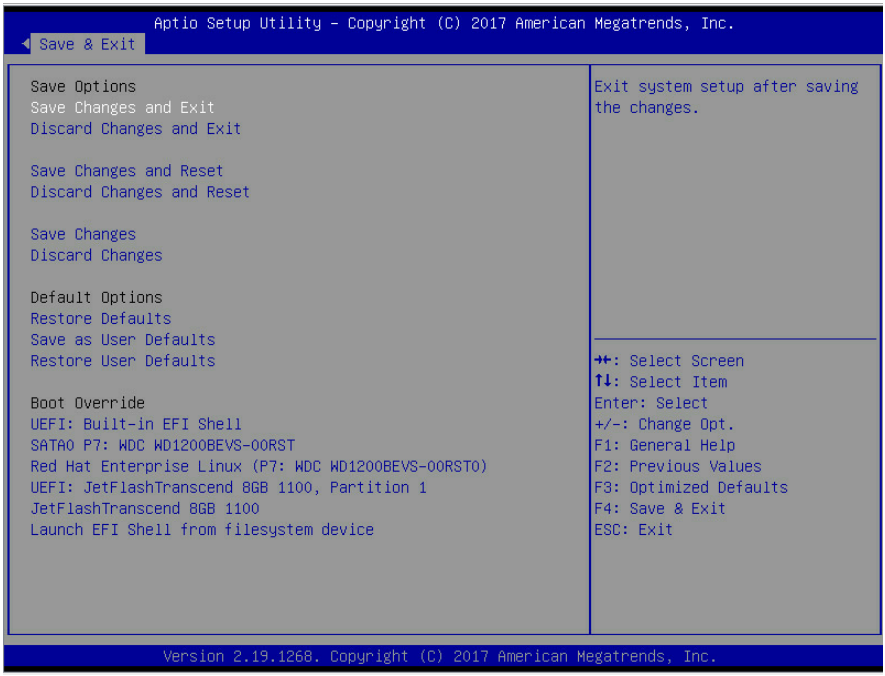
Create
Creates the newly formed boot option

3.8.4 Delete Boot Option Configuration



Delete Boot Option
Sets the system boot order.
Device Name / Select one to Delete

3.9 Save & Exit



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save changes done so far to any of the setup options.

Discard Changes
Discard changes done so far to any of the setup options.

Restore Defaults
Restore/Load Default values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Boot Override
Device Name

Chapter 4: Diagnostics

NOTE: if you experience problems with setting up your system, always check the following things in the following order:

Memory, Video, CPU

By checking these items, you will most likely find out what the problem might have been when setting up your system. For more information on troubleshooting, check the TYAN website at http://www.tyan.com.

4.1 Flash Utility

Every BIOS file is unique for the motherboard it was designed for. For Flash Utilities, BIOS downloads, and information on how to properly use the Flash Utility with your motherboard, please check the TYAN web site at http://www.tyan.com

NOTE: Please be aware that by flashing your BIOS, you agree that in the event of a BIOS flash failure, you must contact your dealer for a replacement BIOS. There are no exceptions. TYAN does not have a policy for replacing BIOS chips directly with end users. In no event will TYAN be held responsible for damages done by the end user.

4.2 AMIBIOS Post Code (Aptio)

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint Ranges

Status Code Range	Description
0x01 – 0x0B	SEC execution
0x0C – 0x0F	Sec errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0x8F	DXE execution up to BDS
0x90 – 0xCF	BDS execution
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xF0 – 0xF8	Recovery (PEI)
0xF9 – 0xFF	Recovery errors (PEI)

Standard Checkpoints

SEC Phase

Status Code	Description
0x00	Note used
Progress Codes	
0x01	Power on. Reset type detection (soft/hard).
0x02	AP initialization before microcode loading
0x03	North Bridge initialization before microcode loading
0x04	South Bridge initialization before microcode loading
0x05	OEM initialization before microcode loading
0x06	Microcode loading
0x07	AP initialization after microcode loading
0x08	North Bridge initialization after microcode loading
0x09	South Bridge initialization after microcode loading
0x0A	OEM initialization after microcode loading
0x0B	Cache initialization

SEC Error Codes	
0x0C – 0x0D	Reserved for future AMI SEC error codes
0x0E	Microcode not found
0x0F	Microcode not found

SEC Phase

None

PEI Phase

Status Code	Description
Progress Codes	
0x10	PCI Core is started
0x11	Pre-memory CPU initialization is started
0x12	Pre-memory CPU initialization (CPU module specific)
0x13	Pre-memory CPU initialization (CPU module specific)
0x14	Pre-memory CPU initialization (CPU module specific)
0x15	Pre-memory North Bridge initialization is started
0x16	Pre-Memory North Bridge initialization (North Bridge module specific)
0x17	Pre-memory North Bridge initialization (North Bridge module specific)
0x18	Pre-Memory North Bridge initialization (North Bridge module specific)
0x19	Pre-memory South Bridge initialization is started
0x1A	Pre-Memory South Bridge initialization (South Bridge module specific)
0x1B	Pre-memory South Bridge initialization (South Bridge module specific)
0x1C	Pre-Memory South Bridge initialization (South Bridge module specific)
0x1D – 0x2A	OEM pre-memory initialization codes
0x2B	Memory initialization. Serial Presence Detect (SPD) data reading
0x2C	Memory initialization. Memory presence detection
0x2D	Memory initialization. Programming memory timing information
0x2E	Memory initialization. Configuring memory
0x2F	Memory initialization (other)
0x30	Reserved for ASL (see ASL Status Codes section below)
0x31	Memory Installed
0x32	CPU post-memory initialization is started.
0x33	CPU post-memory initialization. Cache initialization
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization

Status Code	Description
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization
0x37	Post-Memory North Bridge initialization is started.
0x38	Post-Memory North Bridge initialization (North Bridge module specific)
0x39	Post-Memory North Bridge initialization (North Bridge module specific)
0x3A	Post-Memory North Bridge initialization (North Bridge module specific)
0x3B	Post-Memory South Bridge initialization is started
0x3C	Post-Memory South Bridge initialization (South Bridge module specific)
0x3D	Post-Memory South Bridge initialization (South Bridge module specific)
0x3E	Post-Memory South Bridge initialization (South Bridge module specific)
0x3F – 0x4E	OEM post memory initialization codes
0x4F	DXE PIL is started
PCI Error Codes	
0x50	Memory initialization error. Invalid memory type or incompatible memory speed
0x51	Memory initialization error. SPD reading has failed.
0x52	Memory initialization error. Invalid memory size or memory modules do not match.
0x53	Memory initialization error. No usable memory detected
0x54	Unspecified memory initialization error
0x55	Memory not installed
0x56	Invalid CPU type or speed
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU microcode is not found or microcode update is failed.
0x5A	Internal CPU error
0x5B	Reset PPI is not available.
0x5C – 0x5F	Reserved for future AMI error codes
S3 Resume Progress Codes	
0xE0	S3 Resume is started (S3 Resume PPI is called by the DXE IPL).
0xE1	S3 Boot Script execution
0xE2	Video repost
0xE3	OS S3 wake vector call
0xE4 – 0xE7	Reserved for future AMI progress codes

Status Code	Description
S3 Resume Error Codes	
0xE8	S3 Resume failed
0xE9	S3 Resume PPI not found
0xEA	S3 Resume Boot Script error
0xEB	S3 OS wake error
0xEC – 0xEF	Reserved for future AMI error codes
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found.
0xF4	Recovery firmware image is loaded.
0xF5 – 0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available.
0xF9	Recovery capsule is not found.
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

PEI Beep Codes

# of Beeps	Description
Progress Codes	
1	Memory not installed
1	Memory was installed twice (installPEIMemory routine in PEI Core called twice).
2	Recovery started
3	DXEIPL was not found.
3	DXE Core Firmware Volume was not found.
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available.

DXE Phase

Status Code	Description
0x60	DXE Core is started.
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services

Status Code	Description
0x63	CPU DXE initialization is started.
0x64	CPU DXE initialization (CPU module specific)
0x65	CPU DXE initialization (CPU module specific)
0x66	CPU DXE initialization (CPU module specific)
0x67	CPU DXE initialization (CPU module specific)
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started.
0x6A	North Bridge DXE SMM initialization is started.
0x6B	North Bridge DXE initialization (North Bridge module specific)
0x6C	North Bridge DXE initialization (North Bridge module specific)
0x6D	North Bridge DXE initialization (North Bridge module specific)
0x6E	North Bridge DXE initialization (North Bridge module specific)
0x6F	North Bridge DXE initialization (North Bridge module specific)
0x70	South Bridge DXE initialization is started.
0x71	South Bridge DXE SMM initialization is started.
0x72	South Bridge devices initialization
0x73	South Bridge DXE initialization (South Bridge module specific)
0x74	South Bridge DXE initialization (South Bridge module specific)
0x75	South Bridge DXE initialization (South Bridge module specific)
0x76	South Bridge DXE initialization (South Bridge module specific)
0x77	South Bridge DXE initialization (South Bridge module specific)
0x78	ACPI module initialization
0x79	CSM initialization
0x7A – 0x7F	Reserved for future AMI DXE codes
0x80 – 0x8F	OEM DXE initialization codes
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller initialization
0x94	PCI Bus Enumeration
0x95	PCI BUS Request Resources
0x96	PCI Bus Assign Resources
0x97	Console output devices connect
0x98	Console Input devices connect
0x99	Super IO initialization
0x9A	USB initialization is started.

Status Code	Description
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0x9E -0x9F	Reserved for future AMI codes
0xA0	IDE initialization is started
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started.
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAA	Reserved for ASL (see ASL Status Codes section below)
0xAB	Setup Input Wait
0xAC	Reserved for ASL (see ASL Status Codes section below)
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
0xB8 – 0xBF	Reserved for future AMI codes
0xC0 – 0xCF	OEM BDS initialization codes
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources

Status Code	Description
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found.
0xD7	No Console Input Devices are found.
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error).
0xDB	Flash update is failed.
0xDC	Reset protocol is not available.

DXE Beep Codes

# of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available.
5	No Console Output Devices are found.
5	No Console Input Devices are found.
6	Flash update is failed.
7	Reset protocol is not available.
8	Platform PCI resource requirements cannot be met.

ACPI/ASL Checkpoints

Status Code	Description
0x01	System is entering S1 sleep state.
0x02	System is entering S2 sleep state.
0x03	System is entering S3 sleep state.
0x04	System is entering S4 sleep state.
0x05	System is entering S5 sleep state.
0x10	System is waking up from the S1 sleep state.
0x20	System is waking up from the S2 sleep state.
0x30	System is waking up from the S3 sleep state.
0x40	System is waking up from the S4 sleep state.
0xAC	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.
0xAA	System has transitioned into ACPI mode. Interrupt controller is in APIC mode.

Appendix I: How to recover UEFI BIOS

Important Notes:

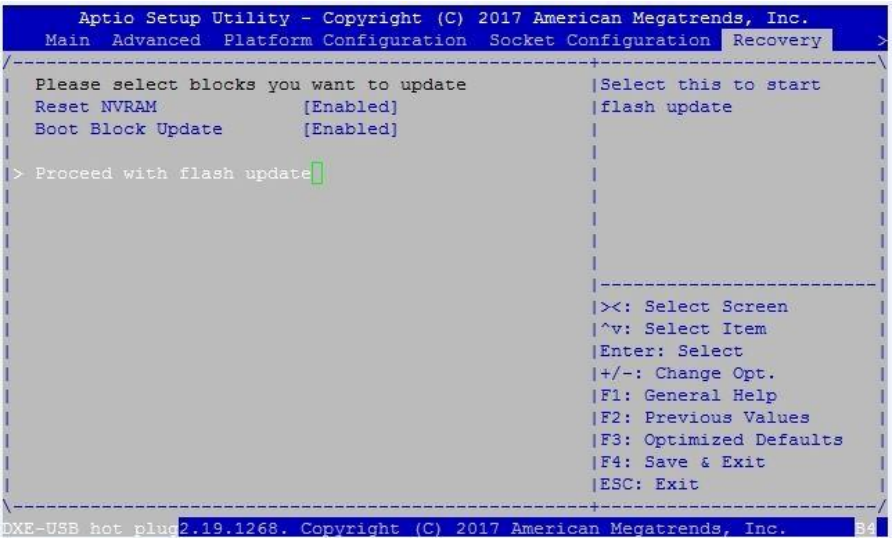
The emergency UEFI BIOS Recovery process is only used to rescue a system with a failed or corrupted BIOS image that fails to boot to an OS. It is not intended to be used as a general purpose BIOS flashing procedure and should not be used as such. Please do not shutdown or reset the system while the BIOS recovery process is underway or there is risk of damage to the UEFI recovery bootloader that would prevent the recovery process itself from working. In no event shall Tyan be liable for direct, indirect, incidental, special or consequential damages arising from the BIOS update or recovery.

The BIOS Recovery file is named xxxx.cap, where the 'xxxx' portion is the motherboard model number. Examples: 5630.cap, 7106.cap, 7109.cap, etc. Please make sure that you are using the correct BIOS Recovery file from Tyan's web site.

BIOS Recovery Process

1. Place the recovery BIOS file (xxxx.cap) in the root directory of a USB disk.
2. Ensure that the system is powered off.
3. Insert the USB disk to any USB port on the motherboard or chassis.
4. Power the system on while pressing “Ctrl” and “Home” simultaneously on the keyboard. Continue to hold these keys down until the following Tyan screen is displayed on the monitor:

5.The system will boot to BIOS setup. A new menu item will appear at the far right of the screen. Scroll to the 'Recovery' tab, move the curser to “Proceed with flash update” and press the "Enter" key on the keyboard to start the BIOS recovery process.

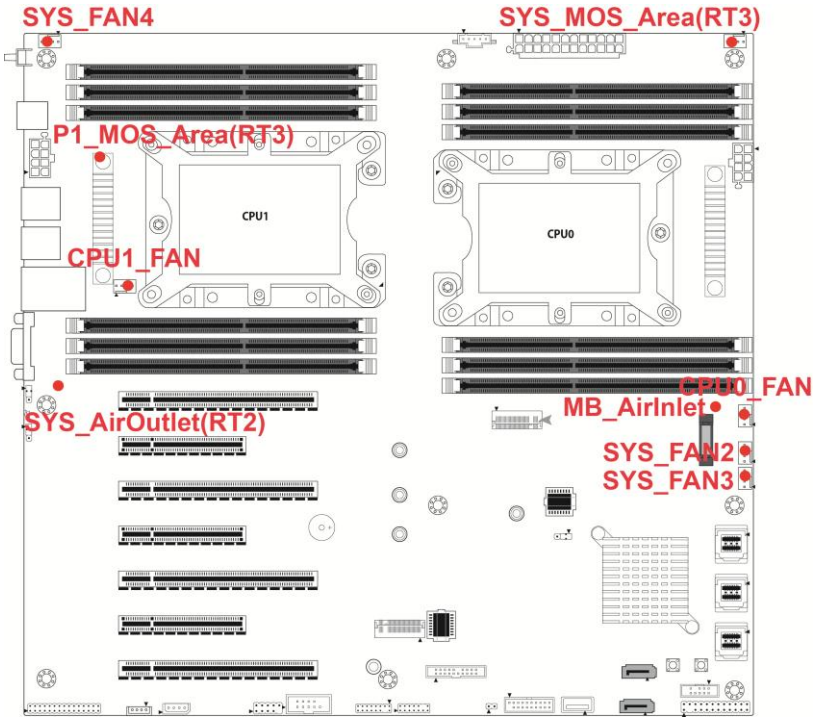


6.IMPORTANT: Do not power off or reboot the server during the BIOS recovery process. This can damage the BIOS recovery bootloader and prevent it from loading a subsequent time.
7.Wait for the BIOS recovery procedure to complete. Completion is signified with the message “Flash update completed. Press any key to reset the system” displayed on screen.
8.Remove the USB disk and reboot.

If your system does not have video output or the POST code halts at “FF” on the right-lower portion of the screen, please contact Tyan representatives for RMA service.

Appendix II: Fan and Temp Sensors

This section aims to help readers identify the locations of some specific FAN and Temp Sensors on the motherboard. A table of BIOS Temp sensor name explanation is also included for readers' reference.

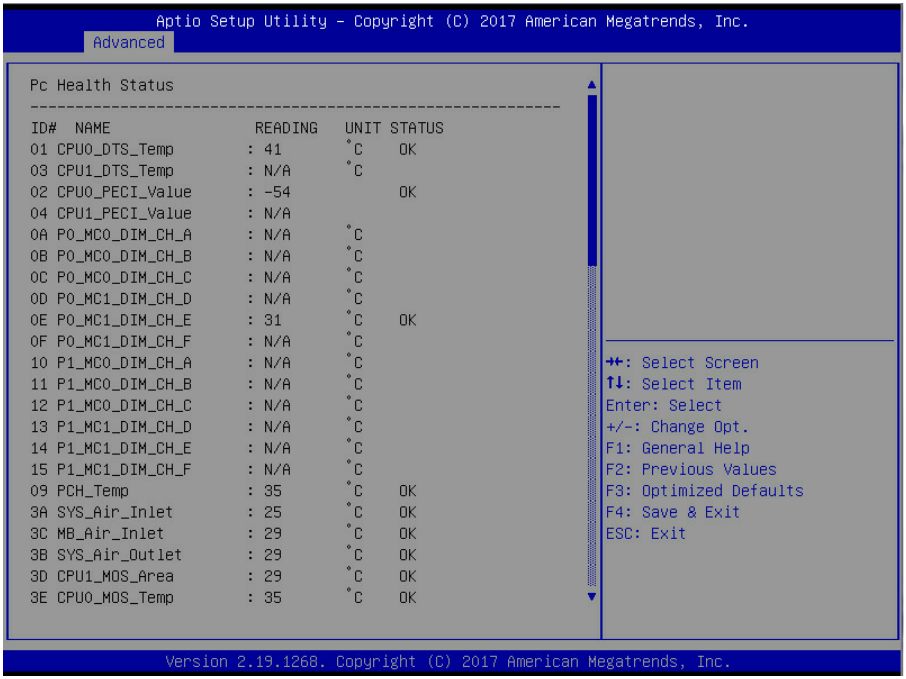


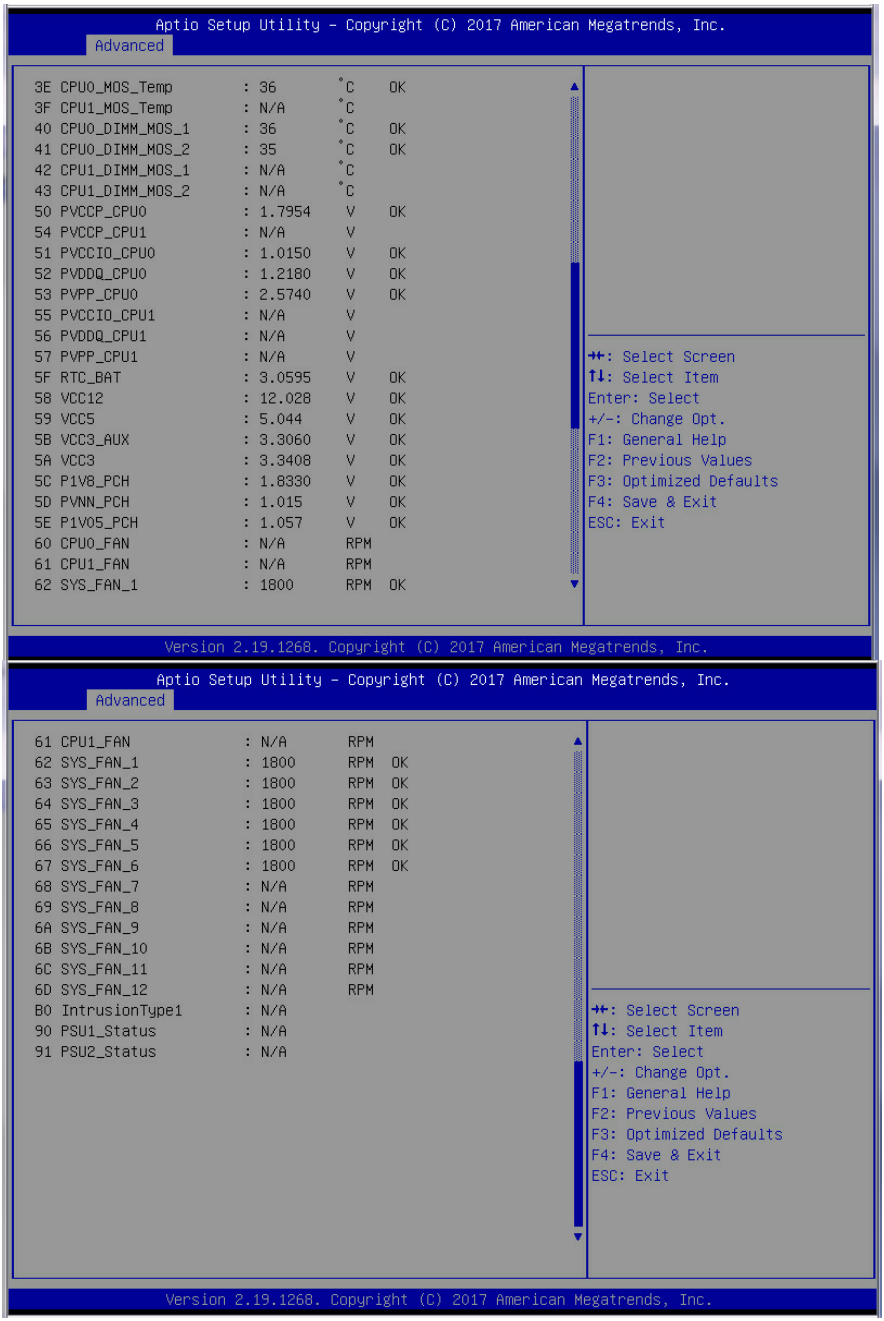
NOTE: The red dot indicates the sensor.

Fan and Temp Sensor Location:

1. Fan Sensor: It is located in the third pin of the fan connector, which detects the fan speed (rpm)
2. Temp Sensor: P1_MOS_Area(RT3) & SYS_AirOutlet(RT2). They detect the system temperature around.
   NOTE: The system temperature is measured in a scale defined by **Intel**, not in Fahrenheit or Celsius.

BIOS Temp Sensor Name Explanation:




Aptio Setup Utility – Copyright (C) 2017 American Megatrends, Inc.
Advanced
3E CPU0_MOS_Temp : 36 °C OK
3F CPU1_MOS_Temp : N/A °C
40 CPU0_DIMM_MOS_1 : 36 °C OK
41 CPU0_DIMM_MOS_2 : 35 °C OK
42 CPU1_DIMM_MOS_1 : N/A °C
43 CPU1_DIMM_MOS_2 : N/A °C
50 PVCCP_CPU0 : 1.7954 V OK
54 PVCCP_CPU1 : N/A V
51 PVCCIO_CPU0 : 1.0150 V OK
52 PVDDQ_CPU0 : 1.2180 V OK
53 PVPP_CPU0 : 2.5740 V OK
55 PVCCIO_CPU1 : N/A V
56 PVDDQ_CPU1 : N/A V
57 PVPP_CPU1 : N/A V
5F RTC_BAT : 3.0595 V OK
58 VCC12 : 12.028 V OK
59 VCC5 : 5.044 V OK
5B VCC3_AUX : 3.3060 V OK
5A VCC3 : 3.3408 V OK
5C P1V8_PCH : 1.8330 V OK
5D PVNN_PCH : 1.015 V OK
5E P1V05_PCH : 1.057 V OK
60 CPU0_FAN : N/A RPM
61 CPU1_FAN : N/A RPM
62 SYS_FAN_1 : 1800 RPM OK
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.19.1268. Copyright (C) 2017 American Megatrends, Inc.
Aptio Setup Utility – Copyright (C) 2017 American Megatrends, Inc.
Advanced
61 CPU1_FAN : N/A RPM
62 SYS_FAN_1 : 1800 RPM OK
63 SYS_FAN_2 : 1800 RPM OK
64 SYS_FAN_3 : 1800 RPM OK
65 SYS_FAN_4 : 1800 RPM OK
66 SYS_FAN_5 : 1800 RPM OK
67 SYS_FAN_6 : 1800 RPM OK
68 SYS_FAN_7 : N/A RPM
69 SYS_FAN_8 : N/A RPM
6A SYS_FAN_9 : N/A RPM
6B SYS_FAN_10 : N/A RPM
6C SYS_FAN_11 : N/A RPM
6D SYS_FAN_12 : N/A RPM
B0 IntrusionType1 : N/A
90 PSU1_Status : N/A
91 PSU2_Status : N/A
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.19.1268. Copyright (C) 2017 American Megatrends, Inc.

CPU0_DTS_Temp	Temperature of the CPU Digital Temperature Sensor
CPU1_DTS_Temp	Temperature of the CPU Digital Temperature Sensor
CPU0_PECI_Value	Temperature of the CPU Platform Environment Control Interface
CPU1_PECI_Value	Temperature of the CPU Platform Environment Control Interface
P0_MC0_DIM_CH_A	The highest temperature of CPU0 DIMM channel A slot
P0_MC0_DIM_CH_B	The highest temperature of CPU0 DIMM channel B slot
P0_MC0_DIM_CH_C	The highest temperature of CPU0 DIMM channel C slot
P0_MC1_DIM_CH_D	The highest temperature of CPU0 DIMM channel D slot
P0_MC1_DIM_CH_E	The highest temperature of CPU0 DIMM channel E slot
P0_MC1_DIM_CH_F	The highest temperature of CPU0 DIMM channel F slot
P1_MC0_DIM_CH_A	The highest temperature of CPU1 DIMM channel A slot
P1_MC0_DIM_CH_B	The highest temperature of CPU1 DIMM channel B slot
P1_MC0_DIM_CH_C	The highest temperature of CPU1 DIMM channel C slot
P1_MC1_DIM_CH_D	The highest temperature of CPU1 DIMM channel D slot
P1_MC1_DIM_CH_E	The highest temperature of CPU1 DIMM channel E slot
P1_MC1_DIM_CH_F	The highest temperature of CPU1 DIMM channel F slot
PCH_Temp	Temperature of PCH
SYS_Air_Inlet	Temperature of the SYS_Air_Inlet Area
MB_Air_ Inlet	Temperature of the MB_Air_Inlet Area
CPU1_MOS_Area	Temperature of CPU1_MOS_Area
CPU0_MOS_Temp	Temperature of CPU0_MOS_Temp
CPU1_MOS_Temp	Temperature of CPU1_MOS_Temp
CPU0_DIMM_MOS_1	Temperature of CPU0_DIMM_MOS_1
CPU0_DIMM_MOS_2	Temperature of CPU0_DIMM_MOS_2
CPU1_DIMM_MOS_1	Temperature of CPU1_DIMM_MOS_1
CPU1_DIMM_MOS_2	Temperature of CPU1_DIMM_MOS_2
BIOS FAN Sensor	**Name Explanation**
CPU0_FAN	Fan speed of CPU0_FAN
CPU1_FAN	Fan speed of CPU1_FAN
SYS_FAN1	Fan speed of SYS_FAN1
SYS_FAN2	Fan speed of SYS_FAN2
SYS_FAN3	Fan speed of SYS_FAN3
SYS_FAN4	Fan speed of SYS_FAN4
SYS_FAN5	Fan speed of SYS_FAN5
SYS_FAN6	Fan speed of SYS_FAN6
SYS_FAN7	Fan speed of SYS_FAN7
SYS_FAN8	Fan speed of SYS_FAN8
SYS_FAN9	Fan speed of SYS_FAN9

SYS_FAN10	Fan speed of SYS_FAN10
SYS_FAN11	Fan speed of SYS_FAN11
SYS_FAN12	Fan speed of SYS_FAN12

NOTE

Glossary

ACPI (Advanced Configuration and Power Interface): a power management specification that allows the operating system to control the amount of power distributed to the computer's devices. Devices not in use can be turned off, reducing unnecessary power expenditure.

AGP (Accelerated Graphics Port): a PCI-based interface which was designed specifically for demands of 3D graphics applications. The 32-bit AGP channel directly links the graphics controller to the main memory. While the channel runs only at 66 MHz, it supports data transmission during both the rising and falling ends of the clock cycle, yielding an effective speed of 133 MHz.

ATAPI (AT Attachment Packet Interface): also known as IDE or ATA; a drive implementation that includes the disk controller on the device itself. It allows CD-ROMs and tape drives to be configured as master or slave devices, just like HDDs.

ATX: the form factor designed to replace the AT form factor. It improves on the AT design by rotating the board 90 degrees, so that the IDE connectors are closer to the drive bays, and the CPU is closer to the power supply and cooling fan. The keyboard, mouse, USB, serial, and parallel ports are built-in.

Bandwidth: refers to carrying capacity. The greater the bandwidth, the more data the bus, phone line, or other electrical path can carry. Greater bandwidth results in greater speed.

BBS (BIOS Boot Specification): a feature within the BIOS that creates, prioritizes, and maintains a list of all Initial Program Load (IPL) devices, and then stores that list in NVRAM. IPL devices have the ability to load and execute an OS, as well as provide the ability to return to the BIOS if the OS load process fails. At that point, the next IPL device is called upon to attempt loading of the OS.

BIOS (Basic Input/Output System): the program that resides in the ROM chip, which provides the basic instructions for controlling your computer's hardware. Both the operating system and application software use BIOS routines to ensure compatibility.

Buffer: a portion of RAM which is used to temporarily store data; usually from an application though it is also used when printing and in most keyboard drivers. The CPU can manipulate data in a buffer before copying it to a disk drive. While this improves system performance (reading to or writing from a disk drive a single time is much faster than doing so repeatedly) there is the possibility of losing your data should the system crash. Information in a buffer is temporarily stored, not permanently saved.

Bus: a data pathway. The term is used especially to refer to the connection between the processor and system memory, and between the processor and PCI or ISA local buses.

Bus mastering: allows peripheral devices and IDEs to access the system memory without going through the CPU (similar to DMA channels).

Cache: a temporary storage area for data that will be needed often by an application. Using a cache lowers data access times since the information is stored in SRAM instead of slower DRAM. Note that the cache is also much smaller than your regular memory: a typical cache size is 512KB, while you may have as much as 4GB of regular memory.

Closed and open jumpers: jumpers and jumper pins are active when they are "on" or "closed", and inactive when they are "off" or "open".

CMOS (Complementary Metal-Oxide Semiconductors): chips that hold the basic startup information for the BIOS.

COM port: another name for the serial port, which is called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another). Parallel ports transmit the bits of a byte on eight different wires at the same time (that is, in parallel form, eight bits at the same time).

DDR (Double Data Rate): a technology designed to double the clock speed of the memory. It activates output on both the rising and falling edge of the system clock rather than on just the rising edge, potentially doubling output.

DIMM (Dual In-line Memory Module): faster and more capacious form of RAM than SIMMs, and do not need to be installed in pairs.

DIMM bank: sometimes called DIMM socket because the physical slot and the logical unit are the same. That is, one DIMM module fits into one DIMM socket, which is capable of acting as a memory bank.

DMA (Direct Memory Access): channels that are similar to IRQs. DMA channels allow hardware devices (like soundcards or keyboards) to access the main memory without involving the CPU. This frees up CPU resources for other tasks. As with IRQs, it is vital that you do not double up devices on a single line. Plug-n-Play devices will take care of this for you.

DRAM (Dynamic RAM): widely available, very affordable form of RAM which looses data if it is not recharged regularly (every few milliseconds). This refresh requirement makes DRAM three to ten times slower than non-recharged RAM such as SRAM.

ECC (Error Correction Code or Error Checking and Correcting): allows data to be checked for errors during run-time. Errors can subsequently be corrected at the same time that they're found.

EEPROM (Electrically Erasable Programmable ROM): also called Flash BIOS, it is a ROM chip which can, unlike normal ROM, be updated. This allows you to keep up with changes in the BIOS programs without having to buy a new chip. TYAN®'s BIOS updates can be found at http://**www.tyan.com**

ESCD (Extended System Configuration Data): a format for storing information about Plug-n-Play devices in the system BIOS. This information helps properly configure the system each time it boots.

Firmware: low-level software that controls the system hardware.

Form factor: an industry term for the size, shape, power supply type, and external connector type of the Personal Computer Board (PCB) or motherboard. The standard form factors are the AT and ATX.

Global timer: onboard hardware timer, such as the Real-Time Clock (RTC).

HDD: stands for Hard Disk Drive, a type of fixed drive.

H-SYNC: controls the horizontal synchronization/properties of the monitor.

HyperTransport™: a high speed, low latency, scalable point-to-point link for interconnecting ICs on boards. It can be significantly faster than a PCI bus for an equivalent number of pins. It provides the bandwidth and flexibility critical for today's networking and computing platforms while retaining the fundamental programming model of PCI.

IC (Integrated Circuit): the formal name for the computer chip.

IDE (Integrated Device/Drive Electronics): a simple, self-contained HDD interface. It can handle drives up to 8.4 GB in size. Almost all IDEs sold now are in fact Enhanced IDEs (EIDEs), with maximum capacity determined by the hardware controller.

IDE INT (IDE Interrupt): Hardware interrupt signal that goes to the IDE.

I/O (Input/Output): the connection between your computer and another piece of hardware (mouse, keyboard, etc.)

IRQ (Interrupt Request): an electronic request that runs from a hardware device to the CPU. The interrupt controller assigns priorities to incoming requests and delivers them to the CPU. It is important that there is only one device hooked up to each IRQ line; doubling up devices on IRQ lines can lock up your system. Plug-n-Play operating systems can take care of these details for you.

Latency: the amount of time that one part of a system spends waiting for another part to catch up. This occurs most commonly when the system sends data out to a peripheral device and has to wait for the peripheral to spread (peripherals tend to be slower than onboard system components).

NVRAM: ROM and EEPROM are both examples of Non-Volatile RAM, memory that holds its data without power. DRAM, in contrast, is volatile.

Parallel port: transmits the bits of a byte on eight different wires at the same time.

PCI (Peripheral Component Interconnect): a 32 or 64-bit local bus (data pathway) which is faster than the ISA bus. Local buses are those which operate within a single system (as opposed to a network bus, which connects multiple systems).

PCI PIO (PCI Programmable Input/Output) modes: the data transfer modes used by IDE drives. These modes use the CPU for data transfer (in contrast, DMA channels do not). PCI refers to the type of bus used by these modes to communicate with the CPU.

PCI-to-PCI Bridge: allows you to connect multiple PCI devices onto one PCI slot.

Pipeline burst SRAM: a fast secondary cache. It is used as a secondary cache because SRAM is slower than SDRAM, but usually larger. Data is cached first to the faster primary cache, and then, when the primary cache is full, to the slower secondary cache.

PnP (Plug-n-Play): a design standard that has become ascendant in the industry. Plug-n-Play devices require little set-up to use. Devices and operating systems that are not Plug-n-Play require you to reconfigure your system each time you add or change any part of your hardware.

PXE (Preboot Execution Environment): one of four components that together make up the Wired for Management 2.0 baseline specification. PXE was designed to define a standard set of preboot protocol services within a client with the goal of allowing networked-based booting to boot using industry standard protocols.

RAID (Redundant Array of Independent Disks): a way for the same data to be stored in different places on many hard drives. By using this method, the data is stored redundantly and multiple hard drives will appear as a single drive to the operating system. RAID level 0 is known as striping, where data is striped (or overlapped) across multiple hard drives, but offers no fault-tolerance. RAID level 1 is known as mirroring, which stores the data within at least two hard drives, but does not stripe. RAID level 1 also allows for faster access time and fault-tolerance, since either hard drive can be read at the same time. RAID level 0+1 is striping and mirroring, providing fault-tolerance, striping, and faster access all at the same time.

RAIDIOS: RAID I/O Steering (Intel)

RAM (Random Access Memory): technically refers to a type of memory where any byte can be accessed without touching the adjacent data and is often referred to the system's main memory. This memory is available to any program running on the computer.

ROM (Read-Only Memory): a storage chip which contains the BIOS; the basic instructions required to boot the computer and start up the operating system.

SDRAM (Synchronous Dynamic RAM): called as such because it can keep two sets of memory addresses open simultaneously. By transferring data alternately from one set of addresses and then the other, SDRAM cuts down on the delays associated with non-synchronous RAM, which must close one address bank before opening the next.

Serial port: called as such because it transmits the eight bits of a byte of data along one wire, and receives data on another single wire (that is, the data is transmitted in serial form, one bit after another).

SCSI Interrupt Steering Logic (SISL): Architecture that allows a RAID controller, such as AcceleRAID 150, 200 or 250, to implement RAID on a system board-embedded SCSI bus or a set of SCSI busses. SISL: SCSI Interrupt Steering Logic (LSI) (only on LSI SCSI boards)

Sleep/Suspend mode: in this mode, all devices except the CPU shut down.

SDRAM (Static RAM): unlike DRAM, this type of RAM does not need to be refreshed in order to prevent data loss. Thus, it is faster and more expensive.

SLI (Scalable Link Interface): NVIDIA SLI technology links two graphics cards together to provide scalability and increased performance. NVIDIA SLI takes advantage of the increased bandwidth of the PCI Express bus architecture, and features hardware and software innovations within NVIDIA GPUs (graphics processing units) and NVIDIA MCPs (media and communications processors). Depending on the application, NVIDIA SLI can deliver as much as two times the performance of a single GPU configuration.

Standby mode: in this mode, the video and hard drives shut down; all other devices continue to operate normally.

UltraDMA-33/66/100: a fast version of the old DMA channel. UltraDMA is also called UltraATA. Without a proper UltraDMA controller, your system cannot take advantage of higher data transfer rates of the new UltraDMA/UltraATA hard drives.

USB (Universal Serial Bus): a versatile port. This one port type can function as a serial, parallel, mouse, keyboard or joystick port. It is fast enough to support video transfer, and is capable of supporting up to 127 daisy-chained peripheral devices.

VGA (Video Graphics Array): the PC video display standard

V-SYNC: controls the vertical scanning properties of the monitor.

ZCR (Zero Channel RAID): PCI card that allows a RAID card to use the onboard SCSI chip, thus lowering cost of RAID solution

ZIF Socket (Zero Insertion Force socket): these sockets make it possible to insert CPUs without damaging the sensitive CPU pins. The CPU is lightly placed in an open ZIF socket, and a lever is pulled down. This shifts the processor over and down, guiding it into the board and locking it into place.

Technical Support

If a problem arises with your system, you should first turn to your dealer for direct support. Your system has most likely been configured or designed by them and they should have the best idea of what hardware and software your system contains. Hence, they should be of the most assistance for you. Furthermore, if you purchased your system from a dealer near you, take the system to them directly to have it serviced instead of attempting to do so yourself (which can have expensive consequences).

If these options are not available for you then TYAN® Computer Corporation can help. Besides designing innovative and quality products for over a decade, TYAN has continuously offered customers service beyond their expectations. TYAN®'s website (**www.tyan.com**) provides easy-to-access FAQ searches and online Trouble Ticket creation as well as Instant Chat capabilities with our Support Agents. TYAN® also provides easy-to-access resources such as in-depth Linux Online Support sections with downloadable Linux drivers and comprehensive compatibility reports for chassis, memory and much more. With all these convenient resources just a few keystrokes away, users can easily find the latest software and operating system components to keep their systems running as powerful and productive as possible. TYAN® also ranks high for its commitment to fast and friendly customer support through email. By offering plenty of options for users, TYAN® serves multiple market segments with the industry's most competitive services to support them.

"TYAN's tech support is some of the most impressive we've seen, with great response time and exceptional organization in general" - Anandtech.com

Help Resources:

1. See the beep codes section of this manual.
2. See the TYAN® website for FAQ's, bulletins, driver updates, and other information: **http://www.tyan.com**
3. Contact your dealer for help BEFORE calling TYAN®.
4. Check the TYAN® user group in Google Forum: **alt.comp.periphs.mainboard.TYAN**

Returning Merchandise for Service

During the warranty period, contact your distributor or system vendor FIRST for any product problems. This warranty only covers normal customer use and does not cover damages incurred during shipping or failure due to the alteration, misuse, abuse, or improper maintenance of products.

NOTE:
A receipt or copy of your invoice marked with the date of purchase is required before any warranty service can be rendered. You may obtain service by calling the manufacturer for a Return Merchandise Authorization (RMA) number. The RMA number Should be prominently displayed on the outside of the shipping carton and the package should be mailed prepaid. TYAN® will pay to have the board shipped back to you.

Notice for the USA
Compliance Information Statement (Declaration of Conformity Procedure) DoC
FCC Part 15: This device complies with part 15 of the FCC Rules

Operation is subject to the following conditions:

This device may not cause harmful interference, and this device must accept any interference received including interference that may cause undesired operation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try one or more of the following measures:
Reorient or relocate the receiving antenna.
Increase the separation between the equipment and the receiver.
Plug the equipment into an outlet on a circuit different from that of the receiver.
Consult the dealer on an experienced radio/television technician for help.

Notice for Canada
This apparatus complies with the Class B limits for radio interference as specified in the Canadian Department of Communications Radio Interference Regulations. (Cet appareil est conforme aux norms de Classe B d'interference radio tel que specifie par le Ministere Canadien des Communications dans les reglements d'ineteference radio.)

CAUTION: Lithium battery included with this board. Do not puncture, mutilate, or dispose of battery in fire. There is danger of an explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by manufacturer. Dispose of used battery according to manufacturer instructions and in accordance with your local regulations.

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