Inverting Amplifier Datasheet AMPINV V 4.3

Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	Flash	RAM	
CY8C29/27/24/23/22xxx, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52						
	0	1	0	64	0	1

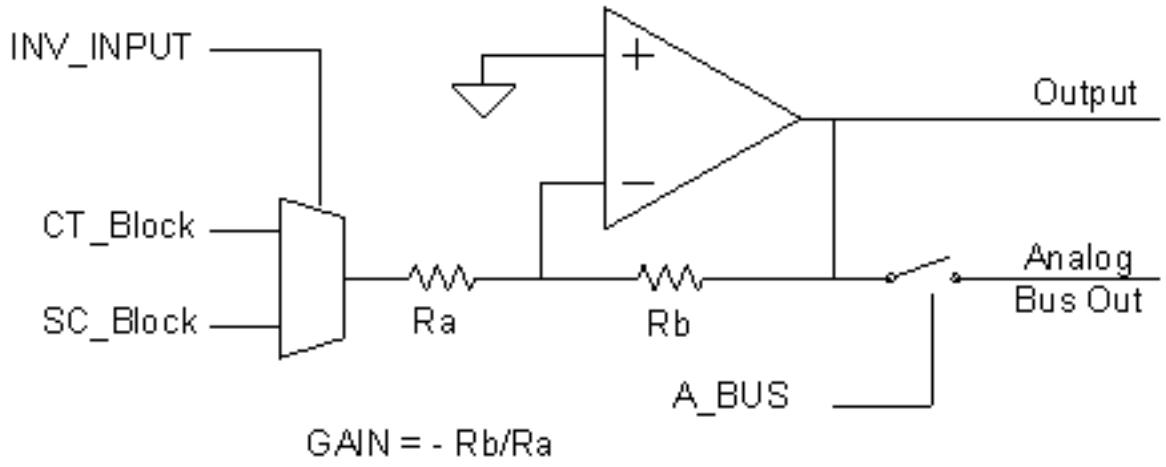
For one or more fully configured, functional example projects that use this user module go to www.cypress.com/psocexampleprojects.

Features and Overview

- 18 user-programmable gain options with a maximum gain of -47.0 for the CY8C29/27/24/23/22xxxdevice family
- 16 user-programmable gain options with a maximum gain of -15.0 for the CY8C26/25xxxdevice family
- Single-ended output referenced to analog ground

The AMPINV User Module implements a single opamp inverting amplifier. The gain, source and output enable are set by the user from tables of values in the Device Editor.

Figure 1. AMPINV Block Diagram



Functional Description

The AMPINV User Module amplifies an internal signal referenced to the analog ground. The gain of the inverting amplifier is set by programming the selectable resistor array tap in a continuous time analog PSoC block. The gain, input, and analog output bus connection are set by the user from tables of values in the Device Editor. The amplifier has the following transfer function:

Equation 1

$$V_O = (V_{IN} - V_{AGND}) \cdot \left(-\frac{R_b}{R_a}\right) + V_{AGND}$$

In Equation 1, V_{AGND} is the user selected analog ground, typically 2*$V_{BandGap}$ or $V_{dd}/2$. V_{ss} cannot be used as analog ground, as input and output voltages are limited to values above V_{ss}. The input and output voltage ranges of the amplifier do not extend to the power supplies (that is, they are not "rail-to-rail" opamps). The allowed input range is a combination of input limit, output limit, power supply voltage, and selected gain. This is illustrated in the DC and AC Electrical Characteristics section of this user module.

The user selects the Gain (the value for $-R_b/R_a$) from the values in the Device Editor. The Device Editor then programs appropriate resistor taps in the PSoC block. API routines are provided for Start, Stop, SetPower, and SetGain functions.

DC and AC Electrical Characteristics

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the tables following, TA = 25°C, Vdd= 5.0V, Power HIGH, Op-Amp Bias LOW, output referenced to Analog Ground = 2*VBandGap.

Table 1. 5.0V AMPINV DC Electrical Characteristics, CY8C29/27/24/23/22xxx Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Gain				
Deviation from Nominal at G=-47	9.0	--	%	
Deviation from Nominal at G=-23	4.8	--	%	
Deviation from Nominal at G=-15	3.8	--	%	
Deviation from Nominal at G=-4.33	1.1	--	%	
Deviation from Nominal at G=-1	0.3	--	%	
Input				
Input Offset Voltage	7.8	--	mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
PSRR	60	--	dB	

Parameter	Typical	Limit	Units	Conditions and Notes
Operating Current				
Low Power	141	--	µA	
Med Power	535	--	µA	
High Power	2062	--	µA	

Table 2. 5.0V AMPINV AC Electrical Characteristics, CY8C29/27/24/23/22xxxFamily of PSoC Devices

Parameter	Typical[4]	Limit[4]	Units	Conditions and Notes
Slew Rate (20% to 80%) [2]				
Low Power	0.4		V/µs	Gain=-1.00, 2.0V step at input
Med Power	1.5		V/µs	
High Power	6.0		V/µs	
Settling Time[2]				
Low Power	10.6		µs	To 0.1%, Gain = -1.00
Med Power	3.4		µs	
High Power	3.2		µs	
Noise[2]				Referred to input
Low Power	250		nV/√Hz	OpAmp bias low except at High Power.
Med Power	79		nV/√Hz	
High Power	70		nV/√Hz	

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25°C, Vdd = 3.3V, Power HIGH, Op-Amp Bias LOW, output referenced to Analog Ground = Vdd/2.

Table 3. 3.3V AMPINV DC Electrical Characteristics, CY8C29/27/24/23/22xxxFamily of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Gain				
Deviation from Nominal at G=-47	10.3	--	%	
Deviation from Nominal at G=-23	5.4	--	%	
Deviation from Nominal at G=-15	4.0	--	%	
Deviation from Nominal at G=-4.33	1.3	--	%	
Deviation from Nominal at G=-1	0.2	--	%	
Input				

Parameter	Typical	Limit	Units	Conditions and Notes
Input Offset Voltage	6.9	--	mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
PSRR	60	--	dB	
Operating Current				
Low Power	136	--	µA	
Med Power	519	--	µA	
High Power	1986	--	µA	

Table 4. 3.3V AMPINV AC Electrical Characteristics, CY8C29/27/24/23/22xxxFamily of PSoC Devices

Parameter	Typical[4]	Limit[4]	Units	Conditions and Notes
Slew Rate (20% to 80%) [2]				
Low Power	0.4		V/µs	Gain=-1.00, 2.0V step at input
Med Power	1.4		V/µs	
High Power	5.7		V/µs	
Settling Time[2]				
Low Power	10.1		µs	To 0.1%, Gain = -1.00
Med Power	3.3		µs	
High Power	3.0		µs	
Noise[2]				Referred to input
Low Power	250		nV/√Hz	OpAmp bias low except at High Power.
Med Power	79		nV/√Hz	
High Power	70		nV/√Hz	

Note Electrical Characteristics Notes

1. To provide a direct comparison with other user modules, these specifications Include I/O pin measurements. In practice, however, the input connects only to other PSoC blocks, and not directly to the device pins.
2. Based on device simulation.
3. PSRR typical value is for input signal referenced to analog ground.
4. PSRR limit value is for input signal referenced to Vss, where VAGND error algebraically adds to input offset voltage.
5. Output swing is for internal signals. External output swing (at pins) is limited by analog output buffer.
6. AC specifications are for internal signals. Slew rate and settling time (at pins) are limited by analog output buffer.

Figure 2. AMPINV Typical Gain Deviation from Nominal

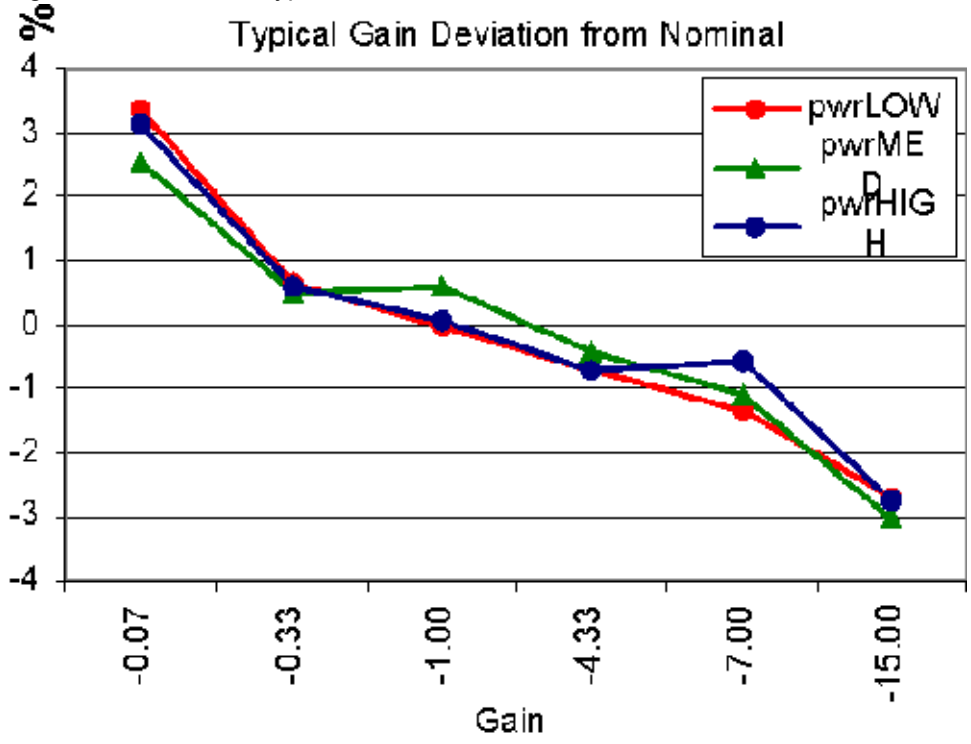


Figure 3. AMPINV Vin Range at Vcc = 5V

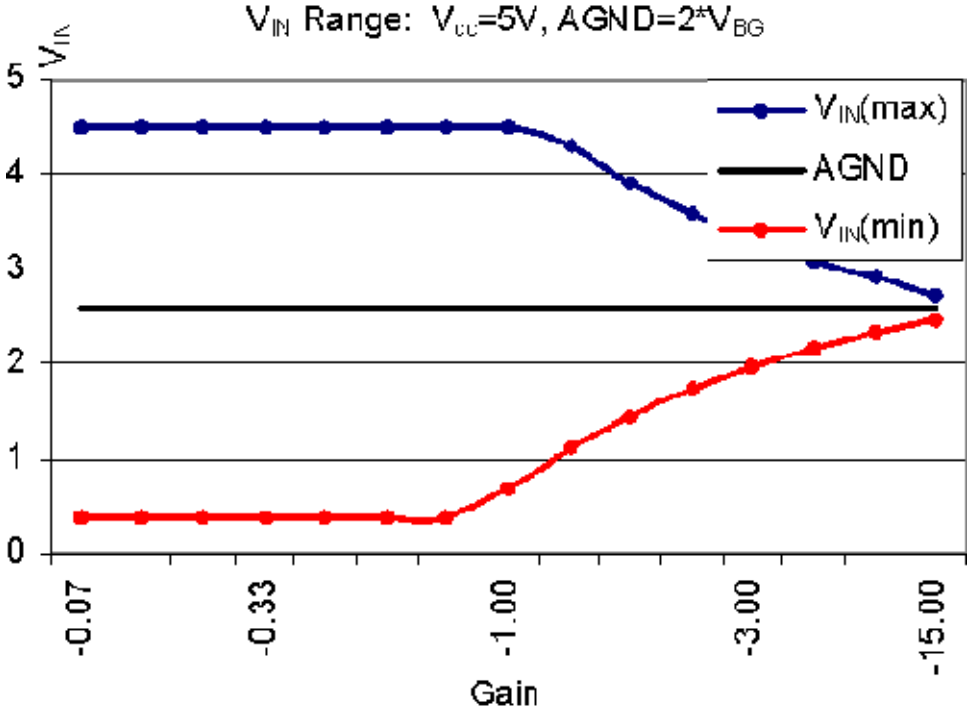
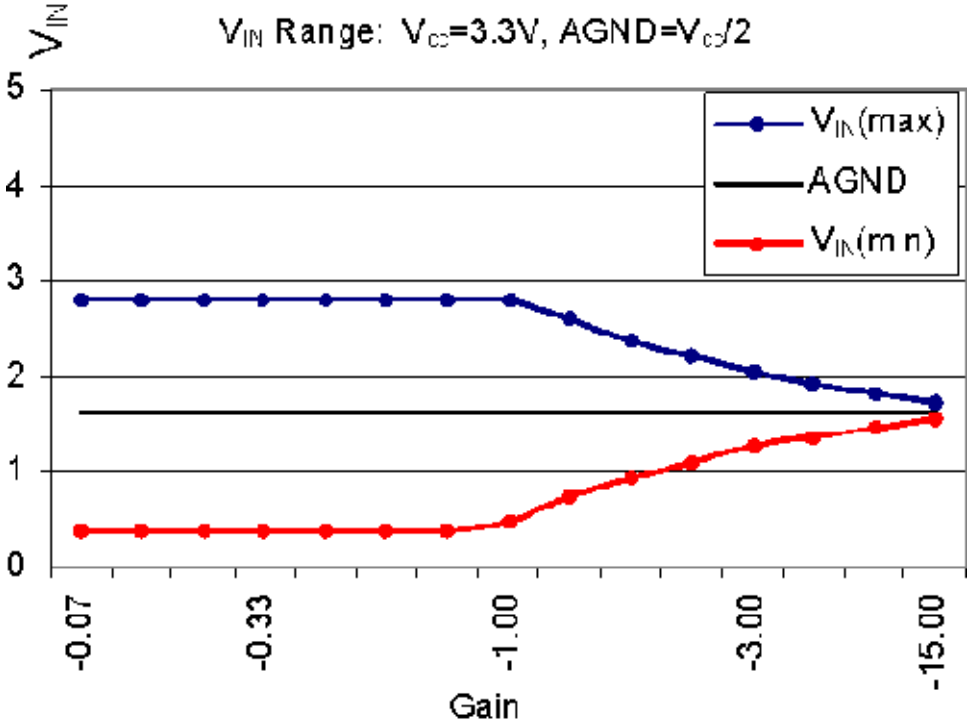
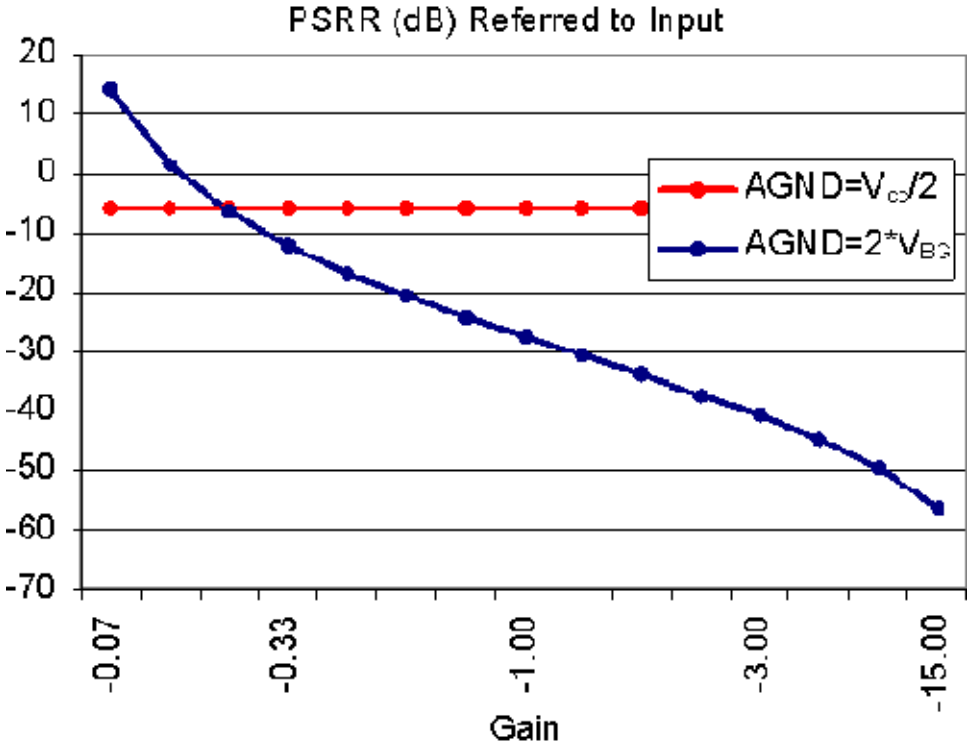


Figure 4. AMPINV Vin Range at Vcc = 3.3V



Power supply rejection is determined by variation in the analog ground reference. At low gains, the ground variation adds as a fixed offset and may be larger than the input signal.

Figure 5. AMPINV Power Supply Rejection Ratio



Placement

The AMPINV maps freely onto any of the continuous time PSoC blocks in the device. However, if the AnalogBus output is enabled onto the bus, ensure that no other user module tries to drive the same bus.

Parameters and Resources

Gain

The Gain is selected from values ranging from -0.067 to -47.00, using PSoC Designer or the SetGain routine provided in the API. Gain accuracy is dependent on gain value and power level. High power offers the greatest accuracy at high gain values.

Input

The inputs to the inverting amplifier are driven only by the outputs of adjacent PSoC blocks. When selecting the input, it is important to know the input-signal integrity with respect to the source and sampling clock. The input from a switched capacitor analog block is connected to the non-sampled and held output of the source. When the source is a DAC User Module, this signal is auto-zero and valid only during one phase of the analog clock. When the source is a Filter User Module, the signal is not auto-zero and valid all of the time. You can select the specific input in the Device Editor.

Reference

The gain of the AMPINV is referenced to the analog ground selected in the global resources window. Choices include $2*V_{BandGap}$, $V_{dd}/2$, and the voltage applied on Port 2[4]. V_{ss} cannot be used because the input and output voltage ranges do not include the range below ground.

AnalogBus

The output may be routed through the analog PSoC block array's network of local interconnections and/or through an analog output bus. Setting the AMPINV User Module AnalogBus parameter to Disable, the default value, restricts the set of possible connections to the local network. Choosing Enable extends the set of possible connections to an associated analog output buffer that can drive a pin and to some additional input multiplexers not afforded by the local network.

Application Programming Interface

The Application Programming Interface (API) routines are provided as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants provided by the “include" files.

Note

In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X before the call if those values are required after the call. This “registers are volatile" policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API function may leave A and X unchanged, there is no guarantee they may do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to perserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

The following are the API programming routines provided for the AMPINV User Module.

AMPINV_Start

Description:

Performs all required initialization for this user module and sets the power level for the continuous time PSoC block. The user module output is driven.

C Prototype:

```
void  AMPINV_Start(BYTE bPowerSetting)
```

Assembler:

```
mov   A, bPowerSetting
lcall  AMPINV_Start
```

Parameters:

bPowerSetting: One byte that specifies the power level to the analog PSoC block. Following reset and configuration, the PSoC block assigned to the instrumentation amplifier is powered down. Symbolic names provided in C and assembly, and their associated values, are listed in the following table:

Symbolic Name	Value
AMPINV_OFF	0
AMPINV_LOWPOWER	1
AMPINV_MEDPOWER	2
AMPINV_HIGHPOWER	3

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

AMPINV_SetPower

Description:

Sets the power level for the continuous time PSoC blocks. May be used to turn the blocks off and on. When the power level is set for any power except off, the output is driven.

C Prototype:

```
void  AMPINV_Start(BYTE bPowerSetting)
```

Assembler:

```
mov   bPowerSetting
lcall  AMPINV_SetPower
```

Parameters:

bPowerSetting: Same as the bPowerSetting used for the Start entry point.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

AMPINV_SetGain

Description:

Sets the gain for the continuous time PSoC block.

C Prototype:

```
void  AMPINV_SetGain(BYTE bGain)
```

Assembler:

```
mov   A, bGain
lcall  AMPINV_SetGain
```

Parameters:

bGain: Symbolic names provided in C and assembly, and their associated values are given in the following table. Programmed gain of -15.0 uses declared name of ....G15_0.

Table 5. CY8C29/27/24/23/22xxx Gain Parameters

Symbolic Name	Value		Symbolic Name	Value
AMPINV_G47_0	04h		AMPINV_G1_00	70h
AMPINV_G23_0	14h		AMPINV_G0_78	80h
AMPINV_G15_0	00h		AMPINV_G0_60	90h
AMPINV_G7_00	10h		AMPINV_G0_46	A0h
AMPINV_G4_33	20h		AMPINV_G0_33	B0h

Symbolic Name	Value		Symbolic Name	Value
AMPINV_G3_00	30h		AMPINV_G0_23	C0h
AMPINV_G2_20	40h		AMPINV_G0_14	D0h
AMPINV_G1_67	50h		AMPINV_G0_06	E0h
AMPINV_G1_27	60h			

Return Value:

None

Side Effects:

In the CY8C29/27/24/23/22xxxfamily of PSoC devices, there may be a gain glitch while changing between a low gain setting (less than 23) and a high gain setting (23 or 47). This glitch should be less than 1usec when the CPU clock is set to 12 MHz. The A and X registers may be altered by this function.

AMPINV_Stop

Description:

Powers the user module off.

C Prototype:

```
void  AMPINV_Stop(void)
```

Assembler:

```
lcall  AMPINV_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

Sample Firmware Source Code

The sample code initializes and starts an amplifier with the gain fixed to -7.00, over-riding the gain value set in the PSoC Designer configuration screen.

```
;;-------------------------------------------------------------------
;;Sample Code for the AMPINV.
;; Turn on power and set gain to -7.00.
;;-------------------------------------------------------------------

include "m8c.inc"           ; part specific constants and macros
include "memory.inc"        ; Constants & macros for SMM/LMM and Compiler
include "PSoCAPI.inc"       ; PSoC API definitions for all User Modules

export _main

_main:

  mov A, AMPINV_G7_00      ; Specify amplifier gain
      call AMPINV_SetGain      ; Set amplifier gain
      mov A, AMPINV_HIGHPOWER  ; Specify amplifier power level
      call AMPINV_Start        ; Start the amplifier operation

.terminate:                    ; Repeat in this loop forever
    jmp .terminate
```

The following C sample code has the same functionality as the assembly code:

```
//-------------------------------------------------------------------------
// This sample C code sets and Inverting Amplifier user module's gain to
// -7.00 and then starts the user module operation.
//-------------------------------------------------------------------------

#include <m8c.h>        // part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules


void main(void)
{
    AMPINV_SetGain(AMPINV_G7_00);// Set AMPINV gain at -7.00
    AMPINV_Start(AMPINV_HIGHPOWER);// Start AMPINV in HIGH power mode

while(1);// Repeat forever
}
```

Configuration Registers

The topology of inverting amplifier user module sets most of the bits in the configuration registers for the chosen Analog CT PSOC block. These include values for opamp compensation, comparator mode, and feedback connection.

Table 6. INVAMP PSoC Block Registers for the CY8C29/27/24/23/22xxxFamily of PSoC Devices

Register	7	6	5	4	3	2	1	0
CR0	Gain					1	Input	
CR1	AnalogBus	0	1	0	0	0	1	1
CR2	0	0	1	0	0	0	Power	
CR3	0	0	0	0	0	0	0	EXGAIN

Gain sets the gain value per selection. Reference sets the reference point (effective "ground") for gain.

Input is established by the selection of a value for the Input parameter in the device editor.

AnalogBus determines whether the GAIN PSoC block drives the bus. The value of this bit-field is determined by the choice made for the parameter of the same name in user module Interconnect View of the Device Editor. Input is the value selected in PSoC Designer.

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, or Stop entry points in the API.

The EXGAIN bit is automatically set whenever a gain of -23 or -47 is selected.

Version History

Version	Originator	Description
4.3	DHA	Added Version History

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.