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*****
*
*           T A B L E   O F   C O N T E N T S
*
* PARAGRAPH                                     PAGE
*
* 1. PURPOSE . . . . . 1A
*
* 2. REQUIREMENTS . . . . . 1A
*
* 3. USE PROCEDURE . . . . . 1A
*
* 4. PRINTOUTS . . . . . 1A
*
* 5. COMMENTS . . . . . 1A
*
* 6. APPENDIX A
* CHARACTER CODES AND CONTROLS. . . . . 2
*
* APPENDIX B
* SCOPE LOOP PROGRAMS . . . . . 3
*
* 6.01 * CORE STORAGE CHECK 3A000230
*
* 6.02 * CONSOLE PRINTER 3A000250
*
* 6.03 * KEYBOARD 3A000270
*
* 6.04 * PAPER TAPE PUNCH 3A000290
*
* 6.05 * PAPER TAPE READER 3A000310
*
* 6.06 * 1442 PUNCH 3A000330
*
* 6.07 * 1442 READER 3A000350
*
* 6.08 * 2310 SEEK 3A000370
*
* 6.09 * 2310 READ/WRITE/COMPARE 3A000390
*
* 6.10 * 1627 PLOTTER 3A000410
*
* 6.11 * 2501 READER 3A000430
*
* 6.12 * 1403 PRINTER 3A000450
*
* 6.13 * 1132 PRINTER 3A000470
*
*****
3A000020
3A000030
3A000040
3A000050
3A000060
3A000070
3A000080
3A000090
3A000100
3A000110
3A000120
3A000130
3A000140
3A000150
3A000160
3A000170
3A000180
3A000190
3A000200
3A000210
3A000220
3A000230
3A000240
3A000250
3A000260
3A000270
3A000280
3A000290
3A000300
3A000310
3A000320
3A000330
3A000340
3A000350
3A000360
3A000370
3A000380
3A000390
3A000400
3A000410
3A000420
3A000430
3A000440
3A000450
3A000460
3A000470
3A000480
3A000490

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*****
*
* 1. PURPOSE
* ONE CARD PROGRAMS THAT PROVIDE THE C.E. WITH THE
* ABILITY TO EXERCISE VARIOUS FUNCTIONS OF THE
* 1130 SYSTEM. EACH CARD IS IDENTIFIED BY THE
* NUMBER IN COLUMNS 79 AND 80. THIS NUMBER REFERS
* TO A PARAGRAPH WITHIN THE APPENDIX.
*
* 2. REQUIREMENTS
* THE C.E. MUST HAVE THE 1130 SYSTEM AND A MEANS
* TO ENTER THE PROGRAM.
*
* 3. USE PROCEDURE
*
* 3.1 SETUP AND OPERATION
* CHECK EACH WRITE-UP FOR SWITCH SETTINGS BEFORE
* AND AFTER LOADING.
*
* 3.2 LOADING
* THE PROGRAM IS LOADED IN IPL MODE FROM CARDS,
* PAPER TAPE OR MAY BE BIT-SWITCHED IN.
*
* 3.3 WAITS
* WAITS ARE IDENTIFIED BY THE B-REGISTER. THEY
* HAVE THE FOLLOWING MEANING,
*
* B-REG 3001 BIT SWITCH SETTINGS REQUIRED.
*
* 3002 ONE PASS OF THE PROGRAM HAS BEEN
* COMPLETED.
*
* 3003 NO INTERRUPT RECEIVED AFTER A
* WRITE COMMAND.
*
* 3004 NO INTERRUPT RECEIVED AFTER A READ
* COMMAND.
*
* 3005 NO INTERRUPT RECEIVED AFTER A
* CONTROL COMMAND.
*
* 3006 ERROR, SEE INDIVIDUAL PROGRAM.
*
* 3007 ERROR, SEE INDIVIDUAL PROGRAM.
*
* 3.4 TERMINATION
* PRESS IMMEDIATE STOP. IF PROGRAM STOP IS PRESSED
* THE PROGRAM MAY NOT RUN BY PRESSING START BE-
* CAUSE INTERRUPT 5 IS ON.
*
* 3.5 RESTART
* PRESS IMMEDIATE STOP AND RESET. PRELOADING
* SWITCHES MAY BE SET AS DESIRED. PRESS START. AT
* WAIT 1 MAKE REQUIRED BIT SWITCH SETTINGS.
*
* 4. PRINTOUTS
* NONE EXCEPT FOR DEVICES THAT PRINT CHARCTERS
* ENTERED FROM THE BIT SWITCHES.
*
* 5. COMMENTS
* IN MOST CASES A SPECIFIED *LOX* MAY REPLACE A
* WAIT TO ALLOW RUNNING WITHOUT INTERRUPT. ERROR
* WAITS MAY BE REPLACED BY A *NOP*. OTHER COMMENTS
* WILL BE FOUND IN EACH PROGRAM. AN INSTRUCTION
* FOLLOWED BY ** WILL BE ALTERED. THIS IS DUE TO
* THE LIMITATIONS OF 1130 IPL MODE. THE ALTERED
* INSTRUCTION WILL FOLLOW THE **.
*
*****
3A000510
3A000520
3A000530
3A000540
3A000550
3A000560
3A000570
3A000580
3A000590
3A000600
3A000610
3A000620
3A000630
3A000640
3A000650
3A000660
3A000670
3A000680
3A000690
3A000700
3A000710
3A000720
3A000730
3A000740
3A000750
3A000760
3A000770
3A000780
3A000790
3A000800
3A000810
3A000820
3A000830
3A000840
3A000850
3A000860
3A000870
3A000880
3A000890
3A000900
3A000910
3A000920
3A000930
3A000940
3A000950
3A000960
3A000970
3A000980
3A000990
3A001000
3A001010
3A001020
3A001030
3A001040
3A001050
3A001060
3A001070
3A001080
3A001090
3A001100

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1130 SCOPE LOOP PROGRAMS

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6. APPENDIX A
* CHAR * 1132 * 1403 * KEY/BD * CON/PTR U/C * CON/PTR L/C* 3A001120
* A * C1 * 64 * A000 * 3E * 3C * 3A001130
* B * C2 * 25 * 8800 * 1A * 18 * 3A001140
* C * C3 * 26 * 8400 * 1E * 1C * 3A001150
* D * C4 * 67 * 8200 * 32 * 30 * 3A001160
* E * C5 * 68 * 8100 * 36 * 34 * 3A001170
* F * C6 * 29 * 8080 * 12 * 10 * 3A001180
* G * C7 * 2A * 8040 * 16 * 14 * 3A001190
* H * C8 * 6B * 8020 * 26 * 24 * 3A001200
* I * C9 * 2C * 8010 * 22 * 20 * 3A001210
* J * D1 * 58 * 5000 * 7E * 7C * 3A001220
* K * D2 * 19 * 4800 * 5A * 58 * 3A001230
* L * D3 * 1A * 4400 * 5E * 5C * 3A001240
* M * D4 * 5B * 4200 * 72 * 70 * 3A001250
* N * D5 * 1C * 4100 * 76 * 74 * 3A001260
* O * D6 * 5D * 4080 * 52 * 50 * 3A001270
* P * D7 * 5E * 4040 * 56 * 54 * 3A001280
* Q * D8 * 1F * 4020 * 66 * 64 * 3A001290
* R * D9 * 20 * 4010 * 62 * 60 * 3A001300
* S * E2 * 0D * 2800 * 9A * 98 * 3A001310
* T * E3 * 0E * 2400 * 9E * 9C * 3A001320
* U * E4 * 4F * 2200 * B2 * 80 * 3A001330
* V * E5 * 10 * 2100 * B6 * 84 * 3A001340
* W * E6 * 51 * 2080 * 92 * 90 * 3A001350
* X * E7 * 52 * 2040 * 96 * 94 * 3A001360
* Y * E8 * 13 * 2020 * A6 * A4 * 3A001370
* Z * E9 * 54 * 2010 * A2 * A0 * 3A001380
* 0 * F0 * 49 * 2000 * C4 * ***** 3A001390
* 1 * F1 * 40 * 1000 * FC * 3A001400
* 2 * F2 * 01 * 0800 * D8 * ***** 3A001410
* 3 * F3 * 02 * 0400 * DC * ** CONSOLE * 3A001420
* 4 * F4 * 43 * 0200 * F0 * ** PRINTER * 3A001430
* 5 * F5 * 04 * 0100 * F4 * ** CONTROLS* 3A001440
* 6 * F6 * 45 * 0080 * D0 * ***** 3A001450
* 7 * F7 * 46 * 0040 * D4 * ** CARRIER * 3A001460
* 8 * F8 * 07 * 0020 * E4 * ** RETURN * 3A001470
* 9 * F9 * 08 * 0010 * E0 * ** 81 * 3A001480
* = * 7E * 4A * 00A0 * C2 * ***** 3A001490
* $ * 5B * 62 * 4420 * 40 * ** TAB * 3A001500
* . * 4B * 6E * 8420 * 00 * ** 41 * 3A001510
* ' * 7D * 0B * 0120 * E6 * ***** 3A001520
* , * 6B * 16 * 2420 * 80 * ** SPACE * 3A001530
* ( * 4D * 57 * 8120 * FE * ** 21 * 3A001540
* - * 60 * 61 * 4000 * 84 * ***** 3A001550
* ) * 5D * 2F * 4120 * F6 * **BACK/SPACE* 3A001560
* + * 4E * 6D * 80A0 * DA * ** 11 * 3A001570
* / * 61 * 4C * 3000 * BC * ***** 3A001580
* * * 5C * 23 * 4220 * D6 * ** SHIFT TO * 3A001590
* & * 50 * 15 * 8000 * 44 * ** RED * 3A001600
* SPACE * 00 * 7F * 0000 * 21 * ** 09 * 3A001610
* NUMBER *-----* 0420 * C0 * ** * 3A001620
* AT *-----* 0220 * 04 * ***** 3A001630
* LS THN *-----* 8220 * DE * ** SHIFT TO * 3A001640
* LOG/NOT*-----* 4060 * F2 * ** BLACK * 3A001650
* SEM/CLM*-----* 40A0 * D2 * ** 05 * 3A001660
* QUOTE *-----* 0060 * E2 * ***** 3A001670
* LOG/OR *-----* 8060 * C6 * ** LINE FEED* 3A001680
* UNSCORE*-----* 2120 * BE * ** 03 * 3A001690
* QST MK *-----* 2060 * 86 * ***** 3A001700
* COLON *-----* 0820 * 82 * 3A001710
* GRT THN*-----* 20A0 * 46 * 3A001720
* EXCLAIM*-----* 4820 * 42 * 3A001730
* PERCENT*-----* 2220 * 06 * 3A001740
* CENT *-----* 8820 * 02 * 3A001750
* EOF *-----* 0008 * ***** 3A001760
* ER CHR *-----* 0004 * 3A001770
* ER FLD *-----* 0002 * 3A001780
* 0-8-2 *-----* 2820 * 3A001790

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1130 SCOPE LOOP PROGRAMS

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***** 3A001800
* PLOTTER BIT SWITCH CONTROL * PAPER TAPE BIT SW * 3A001810
***** CONTROL AND BINARY* 3A001820
* PATTERN DATA. * 3A001830
***** 3A001840
* BIT SWS FUNCTION ***** 3A001840
* 0 AND 8 --- PEN DOWN * 3A001850
* 1 AND 9 --- DRUM DOWN * 3A001860
* 2 AND 10 --- DRUM UP ** * * 3A001870
* 3 AND 11 --- CARR. RIGHT * * * * * 3A001880
* 4 AND 12 --- CARR. LEFT * * * 0* * * 3A001890
* 5 AND 13 --- PEN UP * * 0 0 * 0 * 3A001900
* SET CHAR. 1 IN BIT SWS 0-5 * 0 0 * 3A001910
* SET CHAR. 2 IN BIT SWS 8-13 * 0 0 0 0 * 3A001920
***** 0 0 0 0 * 3A001930
* 0 0 0 0 * 3A001940
* 0 0 * 3A001950
* 0 0 0 0 * 3A001960
* 0 0 0 0 * 3A001970
* DECIMAL TO HEX * 0 0 * 3A001980
* CONVERSION TABLE * 0 * 3A001990
***** 0 0 0 0 0 * 3A002000
* CYL * BIT SW * 0 0 0 0 * 3A002010
* NUMBER * SETTING * 0 0 0 0 * 3A002020
* IN HEX * IN HEX * 0 0 0 * 3A002030
***** 0 0 0 0 * 3A002040
* 10 * 0A * 0 0 0 * 3A002050
* 20 * 14 * 0 0 0 * 3A002060
* 30 * 1E * 0 0 * 3A002070
* 40 * 28 * 0 0 0 0 * 3A002080
* 50 * 32 * 0 0 0 0 * 3A002090
* 60 * 3C * 0 0 0 * 3A002100
* 70 * 46 * 0 0 * 3A002110
* 80 * 50 * 0 0 0 * 3A002120
* 90 * 5A * 0 0 * 3A002130
* 100 * 64 * 0 0 * 3A002140
* 110 * 6E * 0 * 3A002150
* 120 * 78 * 0 0 0 0 * 3A002160
* 130 * 82 * 0 0 0 0 * 3A002170
* 140 * 8C * 0 0 0 0 * 3A002180
* 150 * 96 * 0 0 * 3A002190
* 160 * A0 * 0 0 0 0 * 3A002200
* 170 * AA * 0 0 0 * 3A002210
* 180 * B4 * 0 0 * 3A002220
* 190 * BE * 0 * 3A002230
* 200 * C8 * 0 0 0 0 * 3A002240
***** 0 0 0 * 3A002250
* 0 0 * 3A002260
* 0 * 3A002270
* 0 0 * 3A002280
* 0 * 3A002290
* TO READ/COMPARE BINARY * 0 * 3A002300
* PATTERN, LOAD TAPE HERE ----* * 3A002310
* * * 3A002320
* PAPER * * 3A002330
* TAPE ***** 3A002340
* CHANNEL -- 8 7 6 5 4 3 2 1 3A002350
* 3A002360
* CHAR 1 BIT SWS -- 0 1 2 3 4 5 6 7 3A002370
* 3A002380
* CHAR 2 BIT SWS -- 8 9 1 1 1 1 1 1 3A002390
* 0 0 0 0 0 0 3A002400
* 3A002410
***** 3A002420

```

1130 SCOPE LOOP PROGRAMS

1130 SCOPE LOOP PROGRAMS

6. 1 STORAGE CHECK

A. PRELOAD SWS

B. LOADING

C. WAIT

D. RESTART

E. COMMENTS

```

*****
*
* EACH CORE LOCATION IS CHECKED WITH A PATTERN
* SET IN THE BIT SWITCHES. IF BIT 14 IS ON THE BIT
* SWITCHES ARE USED AS AN ADDRESS TO BE CHECKED
* AND THE PATTERN IS /5555.
*
* BIT SW 15- HALT AFTER ONE PASS.
* 14- USE ONE ADDRESS
* 3- 4 K MEMORY
* 2- 8 K
* 1- 16 K
* 0- 32 K
*
* IPL MODE FROM CARDS OR PAPER TAPE.
*
* SET PATTERN OR ADDRESS IN BIT SWITCHES.
*
* ONE PASS COMPLETED, PRESS START TO CONTINUE.
*
* PATTERN CHANGED. THE BIT THAT WAS DROPPED OR
* PICKED IS ON IN THE ACCUMULATOR. FAILING ADDRESS
* IS IN ADDRESS LOCATION 2. PRESS START TO
* CONTINUE OR DO A RESTART.
*
* PRESS IMMEDIATE STOP AND RESET. PRELOADING
* SWITCHES MAY BE SET AS DESIRED. PRESS START.
*
* THIS PROGRAM WILL WRITE AND READ ALL CORE
* ADDRESSES OUT SIDE THE PROGRAM AREA.
* EACH ADDRESS IS WRITTEN AND CHECKED 2 TIMES.
* IF AN ADDRESS IS FOUND TO BE A PROBLEM, SET BIT
* 14 ON AND RESTART. PLACE THE ADDRESS IN THE BIT
* SWITCHES AT WAIT 1.
* THE PROGRAM WILL CHECK ONLY THAT ADDRESS WITH
* THE PATTERN /5555.
*****
ABS
ORG 0
LDX STGST
STGSW DC *-# BIT SWITCH STG
STGLC DC *-# ADRS LOCATION
STGPN DC *-# STORAGE PATTERN
STGCR DC *-# SIZE OF CORE
STGHL DC *-# BIT 15- HALT
* BIT 14- USE 1 ADRS
STGRD DC /0001
DC /003A ** DC /3A00 RD BIT SW
STGXX DC /0015 CONSTANT
STGST LDX STGBD ** LD STGXX
SLA 6 * PATTERN TO USE
OR STGXX * UNLESS ALTERNATE
SLA 6 * IS SELECTED
OR STGXX
STO STGPN
XIO STGRD READ BIT SWS
LD STGSW GET BIT SW SETTINGS
STO STGHL SET HALT IF B 15 ON
SRA 2
SLA 2
S STGRD ADJ CORE SIZE
STO STGCR STORE CORE SIZE
WAIT 1 SET SWS FOR PATTERN
* OR ADDRESS
XIO STGRD READ BIT SWS
LD STGSW GET BIT SW SETTINGS
RTF 16 * AND SAVE IN Q REG

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001A 0 COEA LD STGHL GET CNTL WORD 3A003120
001B 0 1801 SRA 1 3A003130
001C 0 4804 BSC E USE SWS AS ADRS 3A003140
001D 0 7003 MDX STG7 * YES 3A003150
001E 0 18D0 RTE 16 * NO 3A003160
001F 0 D0E3 STO STGPN 3A003170
0020 0 7002 MDX STG0 3A003180
0021 0 18D0 STG7 RTE 16 3A003190
0022 0 D0E1 STO STGCR SET ADRS IN CORE SIZE 3A003200
0023 0 COE0 STG0 LD STGCR LD CORE SIZE 3A003210
0024 0 D0DD STO STGLC STORE IN XR 2 3A003220
0025 0 C0DD STG1 LD STGPN LD PATTERN TO USE 3A003230
0026 0 00D2 STG2 DC /00D2 *A* TO STO 2 0 3A003240
0027 0 00C2 DC /00C2 *A* TO LD 2 0 3A003250
0028 0 1000 NOP 3A003260
0029 0 F0DC EOR STGRD CHG BIT 15 3A003270
002A 0 00D2 STG3 DC /00D2 *A* TO STO 2 0 3A003280
002B 0 00C2 DC /00C2 *A* TO LD 2 0 3A003290
002C 0 F0D9 EOR STGRD CHG BIT 15 BACK 3A003300
002D 0 F0D5 EOR STGPN CK STARTING PATTERN 3A003310
002E 0 4820 BSC Z IS PATTERN THE SAME 3A003320
002F 0 3006 WAIT 6 * NO 3A003330
0030 0 C0D4 LD STGHL * YES 3A003340
0031 0 1801 SRA 1 3A003350
0032 0 4804 BSC E USE ONLY 1 ADRS 3A003360
0033 0 7006 MDX STG10 * YES 3A003370
0034 0 C0CD LD STGLC * NO, GET ADRS 3A003380
0035 0 90D0 S STGRD REDUCF ADRS 3A003390
0036 0 D0CB STO STGLC STORE IN XR 2 3A003400
0037 0 9006 S STGPG SUB PROG SIZE 3A003410
0038 0 4830 BSC Z- REACHED LAST ADRS 3A003420
0039 0 70EB MDX STG1 * NO 3A003430
003A 0 C0CA STG10 LD STGHL * YES 3A003440
003B 0 4804 BSC E HALT PROGRAM 3A003450
003C 0 3002 WAIT 2 * YES 3A003460
003D 0 70E5 MDX STG0 * NO 3A003470
003E 0 003E STGPG DC STGPG LAST ADRS OF PROG 3A003480
* 3A003490
* INITIALIZATION ROUTINE 3A003500
* 3A003510
STGBD LD STGSP 3A003520
STO STGST 3A003530
LD STGRD+1 BUILD RD BIT SW IOCC 3A003540
SLA 8 3A003550
STO STGRD+1 3A003560
LDD STG2 BUILD STO AND LD 3A003570
RTE 24 * WITH XR 2 3A003580
STD STG2 3A003590
STD STG3 3A003600
STGRS LDX STGST GO TO PGM START 3A003610
STGSP LD X STGXX-1-STGST 3A003620
*****
004A 0 0000 DC 0 SPACE FILLER 3A003640
004B 0 0040 DC /0040 THE LAST FIVE WORDS ARE 3A003650
004C 0 9000 DC /9000 * USED FOR PROGRAM 3A003660
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A003670
004E 0 2000 DC /2000 * FOR THE PID AND TWO FOR 3A003680
004F 0 1000 DC /1000 * SEQUENCE. 3A003690

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1130 SCOPE LOOP PROGRAMS

1130 SCOPE LOOP PROGRAMS

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***** 3A003710
*
6.02 CONSOLE PRINTER
* 1. THE PROGRAM PRINTS ALTERNATE CHARACTERS OR
* EXECUTES ALTERNATE CONTROL FUNCTIONS WHICH
* HAVE BEEN SELECTED IN THE BIT SWITCHES. 3A003720
* 2. AN OPTION IS AVAILABLE TO SET UP A VARIABLE
* DELAY BETWEEN XIO WRITE EXECUTIONS. 3A003730
* 3. AN OPTION IS AVAILABLE TO HALT THE PROGRAM
* AFTER THE COMPLETION OF THE EXECUTION OF
* AN ALTERNATE XIO SEQUENCE. 3A003740
*
A. PRELOAD SWS
* 1. IF DELAY IS DESIRED, SET DELAY CONTROL
* VALUE IN BIT SWITCHES 1 THRU 13. 3A003750
* *NOTE* SWS 1 THRU 13 ALL ON, MAX DELAY. 3A003760
* SWS 1 THRU 13 ALL OFF, NO DELAY. 3A003770
* 2. IF A WAIT AFTER EACH PROGRAM PASS IS
* DESIRED, TURN ON BIT SWITCH 15. 3A003780
*
B. LOADING
* LOAD IPL FROM CARD OR PAPER TAPE. 3A003790
*
C. WAITS
1 * SET DESIRED CHAR/CONTROL CODES IN BIT SWITCHES
* 0 THRU 15. SEE PAGE 2 FOR BIT SW CODES. 3A003800
* 1ST CHAR/CONTROL IN SWS 0 THRU 7. 3A003810
* 2ND CHAR/CONTROL IN SWS 8 THRU 15. 3A003820
* DEPRESS START. 3A003830
*
2 * NORMAL PROGRAM WAIT IF 1 PASS OPTION HAS BEEN
* SELECTED. DEPRESS START TO MAKE ANOTHER PASS. 3A003840
*
3 * NO INTERRUPT GENERATED AFTER XIO WRITE
* COMMAND WAS GIVEN. SEE COMMENTS. 3A003850
*
D. RESTART
* 1. TO RESTART PROGRAM OR RESET INITIAL PRELOAD
* SWITCH SETTINGS, DEPRESS IMMEDIATE
* STOP AND RESET PUSH BUTTONS. 3A003860
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS. 3A003870
* 3. DEPRESS START. 3A003880
*
E. COMMENTS
* 1. LAST DSW SENSED IS DISPLAYED IN THE Q REG. 3A003890
* 2. IF PROGRAM LOOPS, CHECK Q REG FOR NOT RDY
* OR BUSY DSW BITS BEING ON. 3A003900
* 3. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON
* OR TO BYPASS THE INTERRUPT WAIT, LOAD /602D
* INTO LOCATION /002A AND DO A PROGRAM RESTART. 3A003910
* 4. TO SET UP LOOP TO EXECUTE XIO, LOAD /602D
* INTO LOCATION /002A AND LOAD /1000 INTO
* LOCATION /0031 AND DO A PROGRAM RESTART. 3A003920
*
***** 3A003930
*
0000 ORG 0 3A003930
0000 0 6012 CPBGN LDX CPBLD *A* TO LDX CPRDS /6024 3A003940
0001 0 0001 CPONE DC 1 CONSTANT ONE 3A003950
0002 0 0006 CPBSW DC CPDSW BIT SW SAVE AREA 3A003960
0003 0 003A DC /003A *A* TO /3A00 RD BIT SW 3A003970
0004 0 0006 CPWRT DC CPDSW CHARACTER ADDRESS 3A003980
0005 0 9000 DC /9000 *A* TO /0900 XIO PRINT 3A003990
0006 0 0000 CPDSW DC *-* BIT SW READIN AREA 3A004000
0007 0 F010 DC /F010 *A* TO /0F01 XIO SENSE 3A004010
0008 0 0000 CPSET DC *-* SW OPTION/DELAY SAVE 3A004020
0009 0 601D CPCTL LDX CPRDS 2ND CHAR SW/RESET MOD 3A004030
000A 0 0000 DC *-* 3A004040
000B 0 0000 CPDSV DC *-* DSW SAVE AREA 3A004050
000C 0 002C DC CPIN4 INTERRUPT ADDRESS 3A004060
000D 0 1810 CPALT SRA 16 CLR 2ND CHAR SW 3A004070
000E 0 DOFA STO CPCTL * 3A004080
000F 0 7012 MDX CPSEN GO CHK IF PRINT BUSY 3A004090
0010 0 3002 WAIT 2 COMPLETED PROG PASS 3A004100
0011 0 700F MDX CPSEN-1 RESTART PROGRAM 3A004110

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0012 0 C0F2 CPBLD LD CPWRT&1 BUILD WRITE IOCC 3A004390
0013 0 1804 SRA 4 * 3A004400
0014 0 D0F0 STO CPWRT&1 * 3A004410
0015 0 C0F1 LD CPDSW&1 BUILD SENSE RESET 3A004420
0016 0 1804 SRA 4 * DSW IOCC 3A004430
0017 0 D0EF STO CPDSW&1 * 3A004440
0018 0 C0EA LD CPBSW&1 BUILD READ BIT SW 3A004450
0019 0 1008 SLA 8 * IOCC 3A004460
001A 0 D0E8 STO CPBSW&1 * 3A004470
001B 0 C0ED LD CPCTL SET UP RESET AND 3A004480
001C 0 D0E3 STO CPBGN * START BRANCH 3A004490
001D 0 08E4 CPRDS XIO CPBSW READ BIT SWS FOR 3A004500
001E 0 C0E7 LD CPDSW * PROG OPTS/DELAY 3A004510
001F 0 D0F8 STO CPSET * 3A004520
0020 0 3001 WAIT 1 SET CHARS IN SWS 3A004530
0021 0 08E0 XIO CPBSW READ BIT SWS 3A004540
0022 0 C8E7 CPSEN LDD CPDSV-1 LOAD LAST DSW IN Q 3A004550
0023 0 08E2 XIO CPDSW CHK DEVICE NOT BUSY 3A004560
0024 0 D0E6 STO CPDSV * OR NOT READY AND 3A004570
0025 0 1004 SLA 4 * SAVE DSW 3A004580
0026 0 4820 BSC 2 * 3A004590
0027 0 70FA MDX CPSEN * 3A004600
0028 0 C8E1 LDD CPDSV-1 LOAD LAST DSW IN Q 3A004610
0029 0 08DA XIO CPWRT WRITE CHARACTER 3A004620
002A 0 3003 WAIT 3 WAIT FOR INTERRUPT 3A004630
002B 0 7006 MDX CPRET BRANCH TO DELAY 3A004640
002C 0 0000 DC *-* INTERRUPT LEVEL 4 3A004650
002D 0 08D8 XIO CPDSW SENSE RESET DSW 3A004660
002E 0 D0DC STO CPDSV SAVE DSW 3A004670
002F 0 C8DB LDD CPDSV LOAD DSW INTO Q REG 3A004680
0030 0 4850 BOSC - RESET INT LEVEL 3A004690
0031 0 70FB MDX CPIN4&1 RESENSE DSW 3A004700
0032 0 C8D7 CPRET LDD CPDSV-1 LOAD LAST DSW IN Q 3A004710
0033 0 C0D4 LD CPSET SET UP DELAY AND 3A004720
0034 0 1804 SRA 4 * EXECUTE DELAY 3A004730
0035 0 1003 SLA 3 * 3A004740
0036 0 90CA CPLOP S CPONE * 3A004750
0037 0 4810 BSC - * 3A004760
0038 0 70FD MDX CPLOP * 3A004770
0039 0 C0CC LD CPDSW LD, SET UP 2ND CHAR 3A004780
003A 0 1008 SLA 8 * 3A004790
003B 0 D0CA STO CPDSW * 3A004800
003C 0 C0CC LD CPCTL CHK IF 2ND CHAR SW 3A004810
003D 0 4820 BSC 2 * OFF 3A004820
003E 0 70CE MDX CPALT NO, BRANCH 3A004830
003F 0 68C9 STX CPCTL YES, SET 2ND CHAR SW 3A004840
0040 0 C0C7 LD CPSET CHK 1 PASS OPTION SW 3A004850
0041 0 4804 BSC E * 3A004860
0042 0 70CD MDX CPALT&3 SW ON, GO TO WAIT 2 3A004870
0043 0 70DD MDX CPSEN-1 SW OFF, LOOP PROGRAM 3A004880
*****
0044 0 0000 DC 0 SPACE FILLER 3A004890
0045 0 0000 DC 0 * 3A004900
0046 0 0000 DC 0 * 3A004910
0047 0 0000 DC 0 * 3A004920
0048 0 0000 DC 0 * 3A004930
0049 0 0000 DC 0 * 3A004940
004A 0 0000 DC 0 * 3A004950
004B 0 0040 DC /0040 THE LAST FIVE WORDS ARE 3A004970
004C 0 9000 DC /9000 * USED FOR PROGRAM 3A004980
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A004990
004E 0 2000 DC /2000 * FOR THE PID AND TWO FOR 3A005000
004F 0 0800 DC /0800 * SEQUENCE. 3A005010

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1130 SCOPE LOOP PROGRAMS

6.03 KEYBOARD

```

***** 3A005030
* 3A005040
* 1. THE PROGRAM SELECTS KEYBOARD AND DISPLAYS 3A005050
* THE CHARACTER READ OR THE DSW SENSED WHEN A 3A005060
* KEY IS DEPRESSED. 3A005070
* 2. THE PROGRAM ALSO CHECKS THE INTERRUPT REQUEST 3A005080
* KEY OPERATION. 3A005090
* 3. AN OPTION IS AVAILABLE TO HALT PROGRAM BEFORE 3A005100
* A KEY IS DEPRESSED, OR LOOP IN A SELECT 3A005110
* KEYBOARD AND SENSE DSW MODE. 3A005120
* 4. SEE PAGE 2 FOR KEYBOARD CHAR CODES. 3A005130
*
* 3A005140
* A. PRELOAD SWS * NONE, SWITCHES MAY BE CHANGED AT ANY TIME. 3A005150
*
* 3A005160
* B. LOADING * LOAD IPL FROM CARD OR PAPER TAPE. 3A005170
*
* 3A005180
* C. WAITS 1 * SET DESIRED PROGRAM OPTIONS IN BIT SWS 14 AND 15. 3A005190
* 14 ON -- DISPLAY LAST CHAR READ IN Q REG. 3A005200
* 14 OFF - DISPLAY LAST DSW IN Q REG. 3A005210
* 15 ON -- WAIT AFTER EACH PROGRAM PASS. 3A005220
* 15 OFF - LOOP IN SELECT KEYBOARD AND SENSE 3A005230
* DSW MODE. 3A005240
*
* 3A005250
* DEPRESS START. 3A005260
*
* 3A005270
* 2 * NORMAL PROGRAM WAIT IF BIT SW 15 IS ON. SELECT 3A005270
* LIGHT SHOULD BE ON. 3A005280
* LAST CHAR READ AND LAST DSW ARE DISPLAYED IN 3A005290
* ACCUMULATOR OR Q REG, DEPENDING ON BIT SW 14. 3A005300
* DEPRESS DESIRED KEYBOARD KEY OR DEPRESS INT. REQ. 3A005310
*
* 3A005320
* D. RESTART * 1. TO RESTART PROGRAM, DEPRESS IMMEDIATE STOP 3A005330
* AND RESET PUSH BUTTONS. 3A005340
*
* 3A005350
* 2. DEPRESS START. 3A005360
*
* 3A005370
* E. COMMENTS * 1. LAST DSW SENSED OR LAST CHARACTER READ IS 3A005370
* DISPLAYED IN THE Q REG. SEE WAIT 1. 3A005380
*
* 3A005390
* 2. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON, 3A005390
* EXECUTE BIT SW 15 OFF OPTION. 3A005400
*
* 3A005410
***** 3A005420
* 3A005430
* 3A005440
* 3A005450
* 3A005460
* 3A005470
* 3A005480
* 3A005490
* 3A005500
* 3A005510
* 3A005520
* 3A005530
* 3A005540
* 3A005550
* 3A005560
* 3A005570
* 3A005580
* 3A005590
* 3A005600
* 3A005610
* 3A005620
* 3A005630
* 3A005640
* 3A005650
* 3A005660
* 3A005670
* 3A005680
* 3A005690
* 3A005700

```

```

0000
0000 0 6024
0001 0 0001
0002 0 0004
0003 0 003A
0004 0 6032
0005 0 F010
0006 0 0000
0007 0 C000
0008 0 000A
0009 0 A000
000A 0 0000
000B 0 0000
000C 0 0011
000D 0 C8FC
000E 0 18D0
000F 0 D8FA
0010 0 7011
0011 0 0000
0012 0 08EF
0013 0 08F0
0014 0 D0F6
0015 0 1001
0016 0 4850
0017 0 7001
0018 0 7003
0019 0 1001
001A 0 4850

```

```

ORG 0
KYBGN LDX KYBLD *A* TO /6032 LDX KYRST
KYONE DC 1 CONSTANT 1
KYBSW DC KYDSW BIT SW SAVE AREA
DC /003A *A* TO /3A00 RD BIT SWS
KYDSW LDX KYRST RESET VECT/BIT SWS
DC /F010 *A* TO /0F01 XIO SENSE DSW
KYSEL DC 0
DC /C000 *A* TO /0C00 XIO SEL KYBD
KYRD DC KYKEY KEYED RD/IN AREA
DC /A000 *A* TO /0A00 XIO KEY RD
KYKEY DC *-* KEYED RD/IN AREA
KYDSV DC *-* LAST DSW SENSED
DC KYIN4 INTERRUPT ADDR
KYDCH LDD KYKEY LOAD LAST CHAR READ
RTE 16 SWAP LAST CHAR/DSW
STD KYKEY *
MDX KYDSP
KYIN4 DC *-* INTERRUPT ENTRY
XIO KYBSW READ BIT SWS
XIO KYDSW SENSE RESET DSW
STD KYDSV SAVE DSW
SLA 1 CK IF RESPONSE
BOSC - *
MDX KYRFQ NO, CHK IF REQUEST
MDX KYRDW YES, READ CHAR CODE
KYREQ SLA 1 CHECK IF REQUEST
BOSC - *

```

1130 SCOPE LOOP PROGRAMS

```

001B 0 701A MDX KYSET NO, RESENSE DSW 3A005710
001C 0 08EB KYRDW XIO KYRD YES, READ LAST CHAR 3A005720
001D 0 08E8 XIO KYSEL SELECT KEYBOARD 3A005730
001E 0 C0F5 LD KYDSW CK IF CHAR/DSW IN Q 3A005740
* 3A005750
001F 0 100F SLA 14 * 3A005750
* 3A005760
0020 0 4828 BSC &Z * 3A005760
* 3A005770
0021 0 70EB MDX KYDCH DISPLAY CHAR IN Q 3A005770
0022 0 C8E7 KYDSP LDD KYKEY DISPLAY DSW IN Q 3A005780
0023 0 7012 MDX KYSET GO SELECT KEYBOARD 3A005790
0024 0 C0DE KYBLD LD KYBSW&1 BUILD IOCCS AND 3A005800
* 3A005810
0025 0 1008 SLA 8 * RESET/START VECT 3A005810
* 3A005820
0026 0 D0DC STD KYBSW&1 * 3A005820
* 3A005830
0027 0 C0DD LD KYDSW&1 * 3A005830
* 3A005840
0028 0 1804 SRA 4 * 3A005840
* 3A005850
0029 0 D0DB STD KYDSW&1 * 3A005850
* 3A005860
002A 0 C0DC LD KYSEL&1 * 3A005860
* 3A005870
002B 0 1804 SRA 4 * 3A005870
* 3A005880
002C 0 D0DA STD KYSEL&1 * 3A005880
* 3A005890
002D 0 C0DB LD KYRD&1 * 3A005890
* 3A005900
002E 0 1804 SRA 4 * 3A005900
* 3A005910
002F 0 D0D9 STD KYRD&1 * 3A005910
* 3A005920
0030 0 C0D3 LD KYDSW * 3A005920
* 3A005930
0031 0 D0CE STD KYBGN * 3A005930
* 3A005940
0032 0 3001 KYRST WAIT 1 SET PROGRAM OPTIONS 3A005940
* 3A005950
0033 0 08D2 XIO KYSEL SELECT KEYBOARD 3A005950
* 3A005960
0034 0 1010 SLA 16 CL LAST CHAR KEYED 3A005960
* 3A005970
0035 0 D0D4 STD KYKEY * 3A005970
* 3A005980
0036 0 08CB KYSET XIO KYBSW RD BIT SWS FOR OPTS 3A005980
* 3A005990
0037 0 C0CC LD KYDSW CHK IF SEL/RD LOOP 3A005990
* 3A006000
0038 0 100F SLA 15 * 3A006000
* 3A006010
0039 0 4810 BSC - * OPTION IS SELECTED 3A006010
* 3A006020
003A 0 70D7 MDX KYIN4&1 YES, GO SENSE DSW 3A006020
* 3A006030
003B 0 C8CE LDD KYKEY DISPLAY CHAR/DSW IN Q 3A006030
* 3A006040
003C 0 3002 WAIT 2 DEPRESS DESIRED KEY 3A006040
* 3A006050
003D 0 70D4 MDX KYIN4&1 GO SENSE DSW 3A006050
*****
DC 0 SPACE FILLER 3A006060
DC 0 * 3A006070
DC 0 * 3A006080
DC 0 * 3A006090
DC 0 * 3A006100
DC 0 * 3A006110
DC 0 * 3A006120
DC 0 * 3A006130
DC 0 * 3A006140
DC 0 * 3A006150
DC 0 * 3A006160
DC 0 * 3A006170
DC 0 * 3A006180
DC 0 * 3A006190
DC /0040 THE LAST FIVE WORDS ARE 3A006200
DC /9000 * USED FOR PROGRAM 3A006210
DC /2000 * IDENTIFICATION. THREE 3A006220
DC /2000 * FOR THE PID AND TWO FOR 3A006230
DC /0040 * SFQUENCE. 3A006240

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1130 SCOPE LOOP PROGRAMS

```

***** 3A006260
* 3A006270
6.04 PAPER TAPE * 1. THE PROGRAM PUNCHES ALTERNATE CHARACTERS 3A006280
PUNCH * WHICH HAS BEEN SELECTED IN THE BIT SWS, 3A006290
* OR A BINARY PATTERN. 3A006300
* 2. AN OPTION IS AVAILABLE TO SET UP A VARIABLE 3A006310
* DELAY BETWEEN XIO PUNCH EXECUTIONS. 3A006320
* 3. AN OPTION IS AVAILABLE TO HALT THE PROGRAM 3A006330
* AFTER THE COMPLETION OF THE EXECUTION OF 3A006340
* A PROGRAM PASS. 3A006350
* 4. SEE PAGE 2A FOR BIT SW CONTROL BINARY PATTERN. 3A006360
* 5. THIS TAPE MAY BE USED IN THE PAPER TAPE 3A006370
* READER SCOPE LOOP, 6.05. 3A006380
* 3A006390
A. PRELOAD SWS * 1. IF DELAY IS DESIRED, SET DELAY CONTROL 3A006400
* VALUE IN BIT SWITCHES 1 THRU 13. 3A006410
* *NOTE* SWS 1 THRU 13 ALL ON, MAX DELAY. 3A006420
* SWS 1 THRU 13 ALL OFF, NO DELAY. 3A006430
* 2. IF A BINARY PATTERN IS DESIRED, TURN ON 3A006440
* BIT SWITCH 14. 3A006450
* 3. IF A WAIT AFTER EACH PROGRAM PASS IS 3A006460
* DESIRED, TURN ON BIT SWITCH 15. 3A006470
* 3A006480
B. LOADING * LOAD IPL FROM CARD OR PAPER TAPE. 3A006490
* 3A006500
C. WAITS 1 * SET DESIRED CHARACTERS TO BE PUNCHED IN BIT SWS 3A006510
* 0 THRU 15. SEE PAGE FOR BIT SW CODES. 3A006520
* 1ST CHARACTER IN SWS 0 THRU 7. 3A006530
* 2ND CHARACTER IN SWS 8 THRU 15. 3A006540
* MAKE PAPER TAPE PUNCH READY. 3A006550
* DEPRESS START. 3A006560
* 3A006570
2 * NORMAL PROGRAM WAIT IF 1 PASS OPTION HAS BEEN 3A006580
* SELECTED. DEPRESS START TO MAKE ANOTHER PASS. 3A006590
* 3A006600
3 * NO INTERRUPT GENERATED AFTER XIO PUNCH 3A006610
* COMMAND WAS GIVEN. SEE COMMENTS. 3A006620
* 3A006630
D. RESTART * 1. TO RESTART PROGRAM OR RESET INITIAL PRELOAD 3A006640
* SWITCH SETTINGS, DEPRESS IMMEDIATE 3A006650
* STOP AND RESET PUSH BUTTONS. 3A006660
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS. 3A006670
* 3. DEPRESS START. 3A006680
* 3A006690
E. COMMENTS * 1. LAST DSW SENSED IS DISPLAYED IN THE Q REG. 3A006700
* 2. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON 3A006710
* OR TO BYPASS THE INTERRUPT WAIT, LOAD /6034 3A006720
* INTO LOCATION /0031 AND DO A PROGRAM RESTART. 3A006730
* 3. TO SET UP LOOP TO EXECUTE XIO, LOAD /6034 3A006740
* INTO LOCATION /0031 AND LOAD /603A INTO 3A006750
* LOCATION /0039 AND DO A PROGRAM RESTART. 3A006760
* 3A006770
***** 3A006780
0000 ORG 0 3A006790
0000 0 600D TPBGN LDX TPBLD *A* TO LDX TPRDS /6024 3A006800
0001 0 0001 TPONE DC 1 CONSTANT ONE 3A006810
0002 0 0006 TPBSW DC TPDSW BIT SW SAVE AREA 3A006820
0003 0 003A DC /003A *A* TO /3A00 RD BIT SWS 3A006830
0004 0 0006 TPDSW DC TPDSW CHARACTER ADDRESS 3A006840
0005 0 0019 DC /0019 *A* TO /1900 XIO PUNCH 3A006850
0006 0 0000 TPDSW DC *- BIT SW READIN AREA 3A006860
0007 0 001F DC /001F *A* TO /1F01 SENSE DSW 3A006870
0008 0 0000 TPSET DC *- SW OPTION/DELAY SAVE 3A006880
0009 0 601C TPCTL LDX TPRDS 2ND CHAR SW/RESET MOD 3A006890
000A 0 0000 TP100 DC *- *A* TO /0100 PATT BUILD 3A006900
000B 0 0000 TPDSV DC *- DSW SAVE AREA 3A006910
000C 0 0033 DC TPIN4 INTERRUPT ADDRESS 3A006920
000D 0 COF7 TPBLD LD TPWRT&1 BUILD WRITE IOCC 3A006930

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1130 SCOPE LOOP PROGRAMS

```

000E 0 1008 SLA 8 * 3A006940
000F 0 D0F5 STO TPWRT&1 * 3A006950
0010 0 COF6 LD TPDSW&1 BUILD SENSE RESET 3A006960
0011 0 1008 SLA 8 * 3A006970
0012 0 E8EE OR TPONE * 3A006980
0013 0 D0F3 STO TPDSW&1 * 3A006990
0014 0 COEE LD TPBSW&1 BUILD READ BIT SW 3A007000
0015 0 1008 SLA 8 * IOCC 3A007010
0016 0 D0EC STO TPBSW&1 * 3A007020
0017 0 COE9 LD TPONE BUILD PATTERN WORD 3A007030
0018 0 1008 SLA 8 * 3A007040
0019 0 D0F0 STO TP100 * 3A007050
001A 0 COEE LD TPCTL SET UP RESET AND 3A007060
001B 0 D0E4 STO TPBGN * START BRANCH 3A007070
001C 0 08E5 TPRDS XIO TPBSW READ BIT SWS FOR 3A007080
001D 0 COE8 LD TPDSW * PROG OPTS/DELAY 3A007090
001E 0 D0E9 STO TPSET * 3A007100
001F 0 3001 WAIT 1 SET CHARS IN SWS 3A007110
0020 0 1010 SLA 16 CLR PUNCH WD LOC 3A007120
0021 0 D0E4 STO TPDSW 3A007130
0022 0 COE5 LD TPSET CHK PUNCH OPTION 3A007140
0023 0 100E SLA 14 * 3A007150
0024 0 4828 BSC &Z * 3A007160
0025 0 7002 MDX TPPAT BIT 14 ON, PCH PATT 3A007170
0026 0 08DB XIO TPBSW READ BIT SWS 3A007180
0027 0 7005 MDX TPSEN GO SENSE DSW 3A007190
0028 0 C0DD TPPAT LD TPDSW LOAD PATTERN WORD 3A007200
0029 0 80E0 A TP100 BUILD NEXT WORD 3A007210
002A 0 D0DB STO TPDSW * 3A007220
002B 0 1010 TPALT SLA 16 CLR 2ND CHAR SW 3A007230
002C 0 D0DC STO TPCTL * 3A007240
002D 0 08DB TPSEN XIO TPDSW SENSE DSW 3A007250
002E 0 D0DC STO TPDSV SAVE DSW 3A007260
002F 0 C8DA LDD TPDSV-1 LOAD LAST DSW IN Q 3A007270
0030 0 08D3 XIO TPWRT PUNCH CHARACTER 3A007280
0031 0 3003 WAIT 3 WAIT FOR INTERRUPT 3A007290
0032 0 7007 MDX TPRET BRANCH TO DELAY 3A007300
0033 0 0000 TPIN4 DC *- INTERRUPT LEVEL 4 3A007310
0034 0 C8D5 LDD TPDSV-1 LOAD LAST DSW INTO Q 3A007320
0035 0 08D0 XIO TPDSW SENSE RESET DSW 3A007330
0036 0 D0D4 STO TPDSV SAVE DSW 3A007340
0037 0 1003 SLA 3 CK IF PUNCH RESPONSE 3A007350
0038 0 4850 BOSC - RESET INT LEVEL 3A007360
0039 0 70FA MDX TPIN4&1 RESENSE DSW 3A007370
003A 0 COCD TPRET LD TPSET SET UP DELAY AND 3A007380
003B 0 1801 SRA 1 * EXECUTE DELAY 3A007390
003C 0 90C4 TPLOP S TPONE * 3A007400
003D 0 4810 BSC - * 3A007410
003E 0 70FD MDX TPLOP * 3A007420
003F 0 COC9 LD TPCTL CHK IF 2ND CHAR SW 3A007430
0040 0 4818 BSC &- * CLEARED 3A007440
0041 0 7004 MDX TPNOT YES 3A007450
0042 0 COC3 LD TPDSW NO, SET UP 2ND CHAR 3A007460
0043 0 1008 SLA 8 * 3A007470
0044 0 D0C1 STO TPDSW * 3A007480
0045 0 70E5 MDX TPALT PUNCH 2ND CHAR 3A007490
0046 0 68C2 TPNOT STX TPCTL SET 2ND CHAR SW 3A007500
0047 0 COC0 LD TPSET CHK 1 PASS OPTION SW 3A007510
0048 0 4804 BSC E * 3A007520
0049 0 3002 WAIT 2 COMPLETED PROG PASS 3A007530
004A 0 70D7 MDX TPRDS&6 LOOP PROGRAM 3A007540
*****
004B 0 0040 DC /0040 THE LAST FIVE WORDS ARE 3A007550
004C 0 9000 DC /9000 * USED FOR PROGRAM 3A007560
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A007580
004E 0 2000 DC /2000 * FOR THE PID AND TWO FOR 3A007590
004F 0 0020 DC /0020 * SEQUENCE. 3A007600

```

6.05 PAPER TAPE READER

A. PRELOAD SWS

B. LOADING

C. WAITS

D. RESTART

E. COMMENTS

```

*****
* 1. THE PROGRAM READS CHARACTERS WHICH HAVE BEEN
* PUNCHED IN THE TAPE AND COMPARES THEM WITH
* A BINARY PATTERN OR ALTERNATE BIT SWITCH
* CHARACTERS.
* 2. AN OPTION IS AVAILABLE TO SET UP A VARIABLE
* DELAY BETWEEN XIO READ EXECUTIONS.
* 3. AN OPTION IS AVAILABLE TO BYPASS WAIT 6
* ON COMPARE ERRORS.
*
* 1. IF DELAY IS DESIRED, SET DELAY CONTROL
* VALUE IN BIT SWITCHES 1 THRU 13.
* *NOTE* SWS 1 THRU 13 ALL ON, MAX DELAY.
* SWS 1 THRU 13 ALL OFF, NO DELAY.
* 2. IF A BINARY PATTERN IS DESIRED, TURN ON
* BIT SWITCH 14.
* 3. IF BYPASS COMPARE ERROR WAIT 6 OPTION IS
* DESIRED, TURN ON BIT SWITCH 15.
*
* LOAD IPL FROM CARD OR PAPER TAPE.
*
* 1 * LOAD PAPER TAPE INTO READER. SEE PAGE 2A FOR
* LOADING A BINARY PATTERN TAPE.
* PLACE 1ST CHARACTER TO BE READ FROM THE TAPE,
* JUST BEHIND SENSING PINS.
* SET DESIRED CHARACTERS TO COMPARE IN BIT SWS
* 0 THRU 15. SEE PAGE 2A FOR BIT SW CODES.
* 1ST CHARACTER IN SWS 0 THRU 7.
* 2ND CHARACTER IN SWS 8 THRU 15.
* DEPRESS START.
*
* 5 * NO INTERRUPT GENERATED AFTER XIO TAPE ADVANCE
* COMMAND WAS GIVEN. SEE COMMENTS.
*
* 6 * COMPARE ERROR. ACCUMULATOR CONTAINS THE CHAR
* READ. THIS CHARACTER IS NOW LOCATED 1 CHARACTER
* PAST THE SENSING PINS.
* TO READ/COMPARE NEXT CHARACTER, DEPRESS START.
* TO LOOP ON COMPARE ERROR, SEE PRELOAD SWS.
*
* 1. TO RESTART PROGRAM OR RESET INITIAL PRELOAD
* SWITCH SETTINGS, DEPRESS IMMEDIATE
* STOP AND RESET PUSH BUTTONS.
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS.
* 3. DEPRESS START.
*
* 1. LAST DSW SENSED IS DISPLAYED IN THE Q REG.
* 2. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON
* OR TO BYPASS THE INTERRUPT WAIT, LOAD /6002
* INTO LOCATION /0042 AND DO A PROGRAM RESTART.
* 3. TO SET UP LOOP TO EXECUTE XIO, LOAD /6002
* INTO LOCATION /0042 AND LOAD /601A INTO
* LOCATION /0006 AND DO A PROGRAM RESTART.
*
0000 ORG 0
0000 0 6021 TRBGN LDX TRBLD *A* TO /602F LDX TRRST
0001 0 602F TRIN4 LDX TRRST INTERRUPT ENTRY
0002 0 0809 XIO TRDSW SENSE DSW
0003 0 0021 STD TRDSV SAVE DSW
0004 0 1001 SLA 1 CK FOR OP COMPLETE
0005 0 4850 BOSC - *
0006 0 70FB MDX TRIN4&1 NO, RESENSE DSW
0007 0 0806 XIO TRRD YES, READ TAPE
0008 0 C01B LD TRARA COMPARE TO EXPECTED
0009 0 7008 MDX TRI4A GO TO TRI4A
000A 0 D000 TRADV DC /D000 BUILD CONSTANT
000B 0 F000 DC /E000 *A* TO /1C00 XIO ADVANCE
000C 0 0001 TRDSW DC /0001 INT ADR/CONSTANT 1
000D 0 F808 DC /F808 *A* TO /1F01 XIO SENSE

```

```

3A007620
3A007630
3A007640
3A007650
3A007660
3A007670
3A007680
3A007690
3A007700
3A007710
3A007720
3A007730
3A007740
3A007750
3A007760
3A007770
3A007780
3A007790
3A007800
3A007810
3A007820
3A007830
3A007840
3A007850
3A007860
3A007870
3A007880
3A007890
3A007900
3A007910
3A007920
3A007930
3A007940
3A007950
3A007960
3A007970
3A007980
3A007990
3A008000
3A008010
3A008020
3A008030
3A008040
3A008050
3A008060
3A008070
3A008080
3A008090
3A008100
3A008110
3A008120
3A008130
3A008140
3A008150
3A008160
3A008170
3A008180
3A008190
3A008200
3A008210
3A008220
3A008230
3A008240
3A008250
3A008260
3A008270
3A008280
3A008290

```

```

000E 0 0024
000F 0 001A
0010 0 0023
0011 0 003A
0012 0 F010
0013 0 4818
0014 0 7005
0015 0 C00B
0016 0 4804
0017 0 7002
0018 0 C80B
0019 0 3006
001A 0 C809
001B 0 C005
001C 0 1801
001D 0 90EE
001E 0 4810
001F 0 70FD
0020 0 7014
0021 0 C0EF
0022 0 1008
0023 0 D0ED
0024 0 C0E8
0025 0 1803
0026 0 D0E6
0027 0 1008
0028 0 D0F9
0029 0 C8E0
002A 0 18C3
002B 0 D0E3
002C 0 D8DD
002D 0 C0D3
002E 0 D0D1
002F 0 08E0
0030 0 C0F2
0031 0 D0EF
0032 0 3001
0033 0 1010
0034 0 D0EE
0035 0 C0EB
0036 0 100E
0037 0 4828
0038 0 700F
0039 0 08D6
003A 0 C0EB
003B 0 4820
003C 0 7006
003D 0 68E8
003E 0 C0E4
003F 0 1008
0040 0 D0E2
0041 0 08C8
0042 0 3005
0043 0 1010
0044 0 D0E1
0045 0 C0DD
0046 0 180B
0047 0 70F7
0048 0 C0DA
0049 0 80D8
004A 0 70F5
004B 0 0040
004C 0 9000
004D 0 2000
004E 0 2000
004F 0 0010

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```

TRRD DC TRARA READ/IN ADDR
DC /001A *A* TO /1A00 XIO READ
TRBSW DC TRSBW BIT SW SAVE ADDR
DC /003A *A* TO /3A00 RD BIT SWS
TRI4A FOR TRSBW *
BSC E- *
MDX TRLOP-3 OK, GO TO DELAY
LD TRBLD ERR, CK LOOP/ERR OPT
BSC E *
MDX TRLOP-3 LOOP/ERR SELECTED
LDD TRARA LD WD READ AND DSW
WAIT 6 COMPARE ERROR WAIT
LDD TRARA LOAD DSW INTO Q
LD TRBLD SET UP DELAY
SRA 1 *
TRLOP S TRDSW *
BSC - *
MDX TRLOP *
MDX TRSTR CK ON PATT OPT
TRBLD LD TRBSW&1 BUILD PROGRAM
TR100 SLA 8 *A* TO /0100 PATT. BUILD
TRBSW STD TRBSW&1 *A* TO *- COMP S/B WORD
TRARA LD TRDSW&1 *A* TO *- WORD READ
TRDSV SRA 3 *A* TO *- SAVED DSW
TRCTL STD TRDSW&1 *A* TO *- ALT CHAR SW
SLA 8 *
STD TR100 *
LDD TRADV *
RTE 3 *
STD TRRD&1 *
STD TRADV *
LD TRIN4 *
STD TRBGN *
TRRST XIO TRBSW RD SWS DELAY/OPTIONS
LD TRSBW SAVE DELAY/OPTIONS
STD TRBLD *
WAIT 1 SET CHARACTERS IN SWS
SLA 16 INITIALIZE S/B WD
STD TRSBW *
TRSTR LD TRBLD CK WHICH PATT OPTION
SLA 14 *
BSC E2 *
MDX TRPAT BINARY PATT SELECTED
XIO TRBSW READ BIT SWS-CHARS
LD TRCTL CK WHICH CHAR
BSC Z *
MDX TRNOT SEL LEFT CHAR
STX TRCTL SET ALT CHAR SW
LD TRSBW LOAD BIT SWS
TRALT SLA 8 SET UP RIGHT CHAR
STD TRSBW SAVE IN S/B
XIO TRADV ADVANCE TAPE
WAIT 5 WAIT FOR INTERRUPT
TRNOT SLA 16 CL ALT CHAR SW
STD TRCTL *
LD TRSBW SET UP RIGHT CHAR
SRA 8 *
MDX TRALT *
TRPAT LD TRSBW SET UP BINARY PATT
A TR100 *
MDX TRALT&1 *
*****
DC /0040 THE LAST FIVE WORDS ARE
DC /9000 * USED FOR PROGRAM
DC /2000 * IDENTIFICATION. THREE
DC /2000 * FOR THE PID AND TWO FOR
DC /0010 * SEQUENCE.

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3A008300
3A008310
3A008320
3A008330
3A008340
3A008350
3A008360
3A008370
3A008380
3A008390
3A008400
3A008410
3A008420
3A008430
3A008440
3A008450
3A008460
3A008470
3A008480
3A008490
3A008500
3A008510
3A008520
3A008530
3A008540
3A008550
3A008560
3A008570
3A008580
3A008590
3A008600
3A008610
3A008620
3A008630
3A008640
3A008650
3A008660
3A008670
3A008680
3A008690
3A008700
3A008710
3A008720
3A008730
3A008740
3A008750
3A008760
3A008770
3A008780
3A008790
3A008800
3A008810
3A008820
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3A008850
3A008860
3A008870
3A008880
3A008890
3A008900
3A008910
3A008920
3A008930
3A008940
3A008950
3A008960

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1130 SCOPE LOOP PROGRAMS

1130 SCOPE LOOP PROGRAMS

```

*****
* THIS PROGRAM WILL PUNCH THE DATA IN BIT SWITCHES
* 0-11 IN ALL COLUMN UNLESS BIT 12 IS ON AND THEN
* ONLY THE FIRST COLUMN IS PUNCHED. THESE CARDS
* MAY BE USED IN THE READER SCOPE LOOP 6.07 AND
* 6.11.
*
A. PRELOAD SWS * NONE, SWITCHES MAY BE SET AT ANY TIME.
*
B. LOADING * IPL MODE FROM CARDS OR PAPER TAPE.
*
C. WAIT 1 * SET DESIRED BIT SWITCHES AS FOLLOWS,
* BIT 15- HALT
* BIT 14- STACKER SELECT
* BIT 13- FEED A CARD
* BIT 12- TERMINATE PUNCHING
* 0 TO 11- PUNCHING PATTERN
*
2 * ONE PASS COMPLETED, PRESS START TO CONTINUE.
*
3 * LOST PUNCH INTERRUPT.
*
5 * LOST FEED OR INTIATE PUNCH INTERRUPT.
*
D. RESTART * PRESS IMMEDIATE STOP AND RESET. PRELOADING
* SWITCHES MAY BE SET AS DESIRED. PRESS START.
*
E. COMMENTS * 1. TO RUN THE PROG WITH INTERRUPT DELAY SWITCH
* ON OR BYPASS THE INTERRUPT WAIT LOAD /6012
* INTO LOCATION /0021 AND /0032 AND RESTART.
*
* 2. TO GET A FASTER LOOP THAN THE ABOVE PLACE
* /7OFF IN THE NEXT LOCATION AFTER THE XIO. THE
* XIO WILL BE EXECUTED AFTER EACH BRANCH.
*****
0000 ORG 0
0000 0 6037 PHFED LDX PHBLD *A* TO /600F LDX PH1
0001 0 0003 DC /0003 *A* DC /1402 FD A CD
0002 0 0000 PHCTR DC *-* COLUMN COUNTER
0003 0 0000 PHSWS DC *-* BIT SWITCH STG
0004 0 0003 PHBSW DC /0003 READ IN ADRS
0005 0 003A DC /003A *A* DC /3A00
0006 0 0003 PHPCH DC PHSWS PCH I/O AREA
0007 0 0011 DC /0011 *A* DC /1100
0008 0 0011 PHPST DC PHINT COL INTR ADRS
0009 0 A008 DC /A008 *A* DC /1401
000A 0 0008 PHDSW DC /0008 PCH TERMINATOR
000B 0 8818 DC /B818 *A* DC /1703
000C 0 0011 PHSTK DC PHINT OP COMP INTR ADRS
000D 0 0029 DC /0029 *A* DC /1480
000E 0 00F0 PHK50 DC /00F0 80 COLS TIMES 3
000F 0 3001 PH1 WAIT 1 SET BIT SWS
0010 0 701F MDX PH2
0011 0 0000 PHINT DC *-* INTERREPT ENTRY
0012 0 08F7 XIO PHDSW SENSE DSW
0013 0 1001 SLA 1
0014 0 4850 BOSC - COL INTR ON
0015 0 700C MDX PH6 * NO, TRY OP COMP
0016 0 08ED XIO PHBSW
0017 0 C0EA LD PHCTR COLUMN COUNTER
0018 0 80EB A PHBSW ADD THREE
0019 0 D0E8 STO PHCTR
001A 0 F0F3 EOR PHK50 CHECK FOR LAST COLUMN
001B 0 4820 BSC Z IS IT LAST COLUMN
001C 0 7003 MDX PH4
001D 0 C0E5 LD PHSWS GET DATA TO BE PUNCHED

```

```

001E 0 E8EB OR PHDSW * AND OR IN PCH TERM
001F 0 D0E3 STO PHSWS * ANS STORE BACK
0020 0 08E5 PH4 XIO PHPCH PUNCH A COLUMN
0021 0 3003 WAIT 3 WAIT FOR INTERRUPT
0022 0 1003 PH6 SLA 3
0023 0 4850 BOSC -
0024 0 6012 LDX PHINT&1 OP COMP ON
0025 0 1010 SLA 16 * NO, SENSE AGAIN
0026 0 D0DB STO PHCTR * LEVEL 4- OP COMP
0027 0 08DC XIO PHSWS CLEAR COLUMN COUNTER
0028 0 CODA LD PHSWS READ BIT SWITCHES
0029 0 4804 BSC E GET SW SETTING
002A 0 3002 WAIT 2 HALT PROGRAM
002B 0 1801 SRA 1 * YES
002C 0 4804 BSC E * NO
002D 0 7005 MDX PH8 DO STACKER SELECT
002E 0 1801 SRA 1 * YES
002F 0 4804 BSC E * NO
0030 0 08CF PH2 XIO PHFED WHAT OPERATION
0031 0 08D6 XIO PHPST FEED A CARD
0032 0 3005 WAIT 5 START THE PUNCH
0033 0 08D8 PH8 XIO PHSTK * PCH FROM SWS
0034 0 C0CE LD PHSWS GIVE STACKER COMMAND
0035 0 1802 SRA 2 RESTORE ACC
0036 0 70F8 MDX PH2-1
*
PHBLD LD PHRES BUILD XIO COMMANDS
STO 0 SET UP RESTART
LD PHPST+1 * INIT PCH
SRA 3 *
STO PHPST+1 *
EOR PHFED&1 * FEED A CARD
STO PHFED&1 *
LD PHSW+1 * READ BIT SWITCHES
SLA 8 *
STO PHBSW+1 *
LD PHDSW+1 * SENSE DSW
SRA 3 *
STO PHDSW+1 *
LD PHPCH+1 * PCH A COLUMN
SLA 8 *
STO PHPCH+1 *
LD PHSTK+1 * STACK SELECT
SLA 7 *
STO PHSTK&1 *
PHRES LDX PH1
*****
DC /0040 THE LAST FIVE WORDS ARE
DC /9000 * USED FOR PROGRAM
DC /2000 * IDENTIFICATION. THREE
DC /2000 * FOR THE PID AND TWO FOR
DC /0008 * SEQUENCE.

```


6.07 1442 READER

A. PRELOAD SWS

P. LOADING

C. WAITS

D. RESTART

E. COMMENTS

0000
0000 0 601F
0001 0 00FF
0002 0 0006
0003 0 003A
0004 0 0001
0005 0 0012
0006 0 602D
0007 0 8818
0008 0 000F
0009 0 2808
000A 0 0000
000B 0 0000
000C 0 000F
000D 0 00FF
000E 0 0001
000F 0 0000
0010 0 08F5
0011 0 00F9
0012 0 4850
0013 0 7024

* 1. THE PROGRAM READS A COLUMN OF DATA FROM
* THE CARD AND COMPARES IT WITH THE BIT SWS.
* 2. AN OPTION IS AVAILABLE TO SET UP A VARIABLE
* DELAY BETWEEN XIO READ EXECUTIONS.
* 3. AN OPTION IS AVAILABLE TO BYPASS WAIT 6
* ON COMPARE ERRORS.
* 1. IF DELAY IS DESIRED, SET DELAY CONTROL
* VALUE IN BIT SWITCHES 1 THRU 13.
* *NOTE* SWS 1 THRU 13 ALL ON, MAX DELAY.
* SWS 1 THRU 13 ALL OFF, NO DELAY.
* 2. IF BYPASS COMPARE ERROR WAIT 6 OPTION IS
* DESIRED, TURN ON BIT SWITCH 15.
* LOAD IPL FROM CARD OR PAPER TAPE.
* 1 * SET BIT SWITCHES 0 THRU 11 TO EXPECTED COLUMN
* DATA AND SET BITS 12 THRU 15 OFF.
* LOAD PREPUNCHED CARDS INTO READER AND MAKE RDY.
* DEPRESS START.
* 4 * NO INTERRUPT GENERATED AFTER XIO READ.
* COMMAND WAS GIVEN. SEE COMMENTS.
* 6 * COMPARE ERROR. ACCUMULATOR CONTAINS BITS READ.
* IF ACCUMULATOR CONTAINS /00FF, COLUMN READ WAS
* NOT STORED INTO READ/IN AREA.
* DEPRESS START TO READ NEXT CARD.
* TO BYPASS COMPARE ERROR WAIT, SEE PRELOAD.
* 1. TO RESTART PROGRAM OR RESET INITIAL PRELOAD
* SWITCH SETTINGS, DEPRESS IMMEDIATE
* STOP AND RESET PUSH BUTTONS.
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS.
* 3. DEPRESS START.
* 1. LAST DSW SENSED IS DISPLAYED IN THE Q REG.
* 2. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON
* OR TO BYPASS THE INTERRUPT WAIT, LOAD /6010
* INTO LOCATION /0037 AND DO A PROGRAM RESTART.
* 3. TO SET UP LOOP TO EXECUTE XIO, LOAD /6010
* INTO LOCATION /0037 AND LOAD /1000 INTO
* LOCATION /003A AND DO A PROGRAM RESTART.

ORG 0
RDRGN LDX RDBLD ** TO /602D LDX RDRST
RDARA DC /00FF READ IN AREA
RDPSW DC RDPSW BIT SW SAVE AREA
DC /003A ** TO /3A00 RD BIT WSW
RDPRD DC RDARA READ IN AREA ADDR
DC /0012 ** TO /1200 XIO READ
RDPSW LDX RDRST BIT SW SAVE AREA
DC /8818 ** TO /1703 XIO SENSE
RDRGO DC RDIO4 INTERRUPT ADDR
DC /2808 ** TO /1404 XIO START
RDERR DC *- LAST RDR COMPARE ERR
RDPSV DC *- LAST DSW SENSED
DC RDIO4 INTERRUPT ADDR
RDIOFF DC /00FF CONSTANT /00FF
RDONE DC 1 CONSTANT 1
RDIO4 DC *- INTERRUPT ENTRY
XIO RDPSW SENSE AND SAVE DSW
STO RDPSV *
BOSC - CK FOR RD RESPONSE
MDX RDCCOP NO, CK OP COMPLETE

3A010190
3A010200
3A010210
3A010220
3A010230
3A010240
3A010250
3A010260
3A010270
3A010280
3A010290
3A010300
3A010310
3A010320
3A010330
3A010340
3A010350
3A010360
3A010370
3A010380
3A010390
3A010400
3A010410
3A010420
3A010430
3A010440
3A010450
3A010460
3A010470
3A010480
3A010490
3A010500
3A010510
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3A010570
3A010580
3A010590
3A010600
3A010610
3A010620
3A010630
3A010640
3A010650
3A010660
3A010670
3A010680
3A010690
3A010700
3A010710
3A010720
3A010730
3A010740
3A010750
3A010760
3A010770
3A010780
3A010790
3A010800
3A010810
3A010820
3A010830
3A010840
3A010850
3A010860

0014 0 08FF XIO RDRRD YES, READ COLUMN 3A010870
0015 0 C0F0 LD RDPSW CK IF COMPARE TO SWS 3A010880
0016 0 1804 SRA 4 * 3A010890
0017 0 1004 SLA 4 * 3A010900
0018 0 F0E8 EDR RDARA * 3A010910
0019 0 4818 BSC E- * 3A010920
001A 0 701C MDX RDINT YES, WAIT NXT INTRPT 3A010930
001B 0 C0E5 LD RDARA NO,SAVE COL READ 3A010940
001C 0 D0ED STO RDERR * 3A010950
001D 0 6802 STX RDESW SET ERR SW 3A010960
001E 0 7018 MDX RDINT WAIT FOR NXT INTRPT 3A010970
001F 0 C0E3 RDBLD LD RDBSW&1 BUILD IOCCS AND 3A010980
0020 0 1008 RDESW SLA 8 * RESET/START BRANCH 3A010990
0021 0 D0E1 STO RDBSW&1 * 3A011000
0022 0 C0E4 LD RDPSW&1 * 3A011010
0023 0 1803 SRA 3 * 3A011020
0024 0 D0E2 STO RDPSW&1 * 3A011030
0025 0 C0F3 LD RDRGO&1 * 3A011040
0026 0 1801 SRA 1 * 3A011050
0027 0 D0E1 STO RDRGO&1 * 3A011060
0028 0 C0DC LD RDRRD&1 * 3A011070
0029 0 1008 SLA 8 * 3A011080
002A 0 D0DA STO RDRRD&1 * 3A011090
002B 0 C0DA LD RDPSW * 3A011100
002C 0 D0D3 STO RDRGN * 3A011110
002D 0 08D4 RDRST XIO RDBSW READ SWS DELAY/OPT 3A011120
002E 0 C0D7 LD RDPSW * SAVE DELAY/OPTION 3A011130
002F 0 D0EF STO RDBLD * 3A011140
0030 0 3001 WAIT 1 SET READ PATTERN 3A011150
0031 0 C0DB LD RDOFF * 3A011160
0032 0 D0CE STO RDARA * 3A011170
0033 0 1010 SLA 16 INITIALIZE AND READ 3A011180
0034 0 D0EB STO RDESW * BIT SWS 3A011190
0035 0 08CC XIO RDRSW * 3A011200
0036 0 08D1 XIO RDRGO START READER 3A011210
0037 0 3004 RDINT WAIT 4 WAIT FOR INTERRUPT 3A011220
0038 0 1004 RDCOP SLA 4 CK FOR OP COMPLETE 3A011230
0039 0 4850 BOSC - * 3A011240
003A 0 70D5 MDX RDIO4&1 NO, RESENSE DSW 3A011250
003B 0 C8CE LDD RDPSV-1 YES, LOAD DSW IN Q 3A011260
003C 0 C0E2 LD RDBLD SET UP DELAY 3A011270
003D 0 1801 SRA 1 * 3A011280
003E 0 90CF RDLDP S RDONE * 3A011290
003F 0 4810 BSC - * 3A011300
0040 0 70FD MDX RDLDP * 3A011310
0041 0 CODE LD RDESW CK IF ERR SW ON 3A011320
0042 0 4818 BSC E- * 3A011330
0043 0 70ED MDX RDRST&4 NO, RD NXT CARD 3A011340
0044 0 C0DA LD RDBLD YES, CK IF LOOP 3A011350
0045 0 100F SLA 15 * ON ERROR(BIT 15) 3A011360
0046 0 4820 BSC Z * 3A011370
0047 0 70ED MDX RDINT-2 YES, RD BIT SWS 3A011380
0048 0 C8C1 LDD RDPSV-1 NO, DISPLAY RD ERR 3A011390
0049 0 3006 WAIT 6 * AND DSW AT WAIT 6 3A011400
004A 0 70E6 MDX RDRST&4 RD NEXT CARD 3A011410

DC /0040 THE LAST FIVE WORDS ARE 3A011420
DC /9000 * USED FOR PROGRAM 3A011430
DC /2000 * IDENTIFICATION. THREE 3A011440
DC /2000 * FOR THE PID AND TWD FOR 3A011450
DC /0004 * SEQUENCE. 3A011460

```
***** 3A011490
* 3A011500
6.08 2310 DISK SEEK * 1. THE PROGRAM ALLOWS THE HEAD TO ACCESS BACK 3A011510
* AND FORTH BETWEEN 2 CYLINDERS WHICH ARE 3A011520
* CONTROLLED BY THE OPERATOR. 3A011530
* 2. AN OPTION IS AVAILABLE TO ALLOW A WAIT AFTER 3A011540
* EACH SEEK OPERATION. 3A011550
* 3. THE PROGRAM CAN BE USED TO POSITION THE HEAD 3A011560
* BEFORE LOADING THE 2310 WRT/RD/COMPARE 3A011570
* PROGRAM. 6.09 3A011580
* 3A011590
A. PRELOAD SWS * 1. SET DESIRED DISK DRIVE AREA CODE IN BIT 3A011600
* SWITCHES 0 THRU 7. 3A011610
* DRIVE 0 --- 20XX 3A011620
* DRIVE 1 --- 88XX 3A011630
* DRIVE 2 --- 90XX 3A011640
* DRIVE 3 --- 98XX 3A011650
* DRIVE 4 --- A0XX 3A011660
* 2. IF WAIT AFTER EACH SEEK OPERATION IS DESIRED, 3A011670
* SET BIT SWITCH 15 ON. 3A011680
* 3A011690
B. LOADING * LOAD IPL FROM CARD OR PAPER TAPE. 3A011700
* 3A011710
C. WAITS 1 * SET DESIRED HEX CYLINDER ADDRESS IN BIT 3A011720
* SWITCHES 0 THRU 7. SEE PAGE 2A. 3A011730
* SET DESIRED HEX NUMBER OF CYLINDERS TO SEEK IN 3A011740
* BIT SWITCHES 8 THRU 15. 3A011750
* DEPRESS START. 3A011760
* 3A011770
5 * NO INTERRUPT GENERATED AFTER INITIAL XIO SEEK 3A011780
* HOME WAS EXECUTED. SEE COMMENTS 3A011790
* 3A011800
6 * NO INTERRUPT GENERATED AFTER XIO SEEK WAS 3A011810
* EXECUTED. SEE COMMENTS 3A011820
* 3A011830
D. RESTART * 1. TO RESTART PROGRAM OR RESET SWITCH SETTINGS, 3A011840
* DEPRESS IMMEDIATE STOP AND RESET PUSH BUTTONS. 3A011850
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS. 3A011860
* 3. DEPRESS START. 3A011870
* 3A011880
E. COMMENTS * 1. LAST DSW SENSED IS DISPLAYED IN THE Q REG. 3A011890
* 2. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON 3A011900
* AND TO BYPASS THE INTERRUPT WAIT, LOAD /6012 3A011910
* INTO LOCATIONS /0039 AND /0041. 3A011920
* DO A PROGRAM RESTART. 3A011930
* 3A011940
***** 3A011950
0000 ORG 0 3A011960
0000 0 601B DKBGN LDX DKBLD *A* TO /6020 LDX DKRST 3A011970
0001 0 0000 DKENT DC *-* INTERRUPT ENTRY SW 3A011980
0002 0 000E DKBSW DC DKBIT BIT SW SAVE 3A011990
0003 0 003A DC /003A *A* TO /3A00 RD BIT SWS 3A012000
0004 0 00CA DKHME DC 202 MAX NUMBER OF SEEKS 3A012010
0005 0 0000 DC *-* IOCC-SEEK HOME 3A012020
0006 0 0000 DKSEK DC *-* NUMBER OF SEEKS 3A012030
0007 0 0000 DC *-* IOCC-SEEK 3A012040
0008 0 0000 DKDSW DC *-* AREA CODE/SW OPTIONS 3A012050
0009 0 0000 DC *-* IOCC-SENSE RESET DSW 3A012060
000A 0 0011 DC DKIN2 INTERRUPT ADDRESS 3A012070
000B 0 0000 DKDSV DC *-* LAST DSW 3A012080
000C 0 0004 DK004 DC /0004 CONSTANT 4 3A012090
000D 0 00FF DKOFF DC /00FF CONSTANT FF 3A012100
000E 0 6020 DKBIT LDX DKRST RESET VECTER 3A012110
000F 0 7010 DKBD1 DC /7010 DSW BUILD WORD 3A012120
0010 0 0808 DKBD2 DC /0808 SEEK BUILD WORD 3A012130
0011 0 0000 DKIN2 DC *-* OP COMPLETE INTRPT 3A012140
0012 0 08F5 XIO DKDSW SENSE RESET DSW 3A012150
0013 0 D0F7 STO DKDSV SAVE DSW 3A012160
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0014 0 1002 SLA 2 CK RDY, NOT BUSY 3A012170
0015 0 4868 BOSC 8Z * 3A012180
0016 0 6012 LDX DKIN2&1 NO, LOOP 3A012190
0017 0 C0E9 LD DKENT LD INTERRUPT ENTRY SW 3A012200
0018 0 4820 BSC Z CHECK IF ON 3A012210
0019 0 7020 MDX DKMOV NO, SEEK HOME ENTRY 3A012220
001A 0 7027 MDX DKCON YES, SEEK ENTRY 3A012230
001B 0 C0F2 DKBLD LD DKBIT BUILD RD BIT SW IOCC 3A012240
001C 0 D0E3 STO DKBGN * AND SET PRG RESET 3A012250
001D 0 C0E5 LD DKBSW&1 * AND START VECTER 3A012260
001E 0 1008 SLA 8 * 3A012270
001F 0 D0E3 STO DKBSW&1 * 3A012280
0020 0 08E1 DKRST XIO DKBSW RD AREA CODE AND 3A012290
0021 0 C0EC LD DKBIT * PROG OPTIONS 3A012300
0022 0 D0E5 STO DKDSW SAVE SWS 3A012310
0023 0 180B SRA 11 SET UP AREA CODE 3A012320
0024 0 100B SLA 11 * 3A012330
0025 0 D0E8 STO DKBIT SAVE AREA CODE 3A012340
0026 0 C0E8 LD DKBD1 BUILD DSW AND SFEK 3A012350
0027 0 1804 SRA 4 * IOCCS 3A012360
0028 0 E8E5 OR DKBIT * 3A012370
0029 0 D0DF STO DKDSW&1 * 3A012380
002A 0 C0E5 LD DKBD2 * 3A012390
002B 0 1801 SRA 1 * 3A012400
002C 0 E8E1 OR DKBIT * 3A012410
002D 0 D0D7 STO DKHME&1 * 3A012420
002E 0 D0D8 STO DKSEK&1 * 3A012430
002F 0 3001 WAIT 1 SET STARTING CYL. 3A012440
0030 0 08D1 XIO DKBSW * AND NUM OF CYLS. 3A012450
0031 0 C0DC LD DKBIT * TO SEEK IN BIT SWS 3A012460
0032 0 1808 SRA 8 SET UP START CYL. 3A012470
0033 0 D0D2 STO DKSEK * 3A012480
0034 0 08D3 XIO DKDSW SENSE DSW 3A012490
0035 0 D0D5 STO DKDSV SAVE DSW 3A012500
0036 0 C8D3 LDD DKDSV-1 LOAD DSW IN Q REG 3A012510
0037 0 68C9 STX DKENT TURN ON INTRPT ENTRY SW 3A012520
0038 0 08CB XIO DKHME SEEK HOME 3A012530
0039 0 3005 WAIT 5 WAIT FOR INTERRUPT 3A012540
003A 0 C0CC DKMOV LD DKSEK&1 SET UP SEEK 3A012550
003B 0 F0D0 EOR DK004 * DIRECTION 3A012560
003C 0 D0CA STO DKSEK&1 * 3A012570
003D 0 C8CC LDD DKDSV-1 LOAD DSW IN Q REG 3A012580
003E 0 1010 SLA 16 TURN OFF INTERRUPT 3A012590
003F 0 D0C1 STO DKENT * ENTRY SW 3A012600
0040 0 08C5 XIO DKSEK SEEK 3A012610
0041 0 3006 WAIT 6 WAIT FOR INTERRUPT 3A012620
0042 0 C0CB DKCON LD DKBIT SET UP NUM OF SEEKS 3A012630
0043 0 E0C9 AND DKOFF * 3A012640
0044 0 D0C1 STO DKSEK * 3A012650
0045 0 C0C2 LD DKDSW CK FOR SEEK AND WAIT 3A012660
0046 0 4804 BSC E * 3A012670
0047 0 3002 WAIT 2 YES, WAIT 3A012680
0048 0 70F1 MDX DKMOV NO, GO SEEK 3A012690
***** 3A012700
0049 0 0000 DC 0 SPACE FILLER 3A012710
004A 0 0000 DC 0 * 3A012720
004B 0 0040 DC /0040 THE LAST FIVE WORDS ARE 3A012730
004C 0 9000 DC /9000 * USED FOR PROGRAM 3A012740
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A012750
004E 0 2000 DC /2000 * FOR THE PID AND TWO FOR 3A012760
004F 0 0002 DC /0002 * SEQUENCE. 3A012770
```

1130 SCOPE LOOP PROGRAMS

```

***** 3A012790
* 3A012800
6.09 2310 WRITE-  * THIS PROGRAM WRITES ON SECTOR 0, A DATA PATTERN 3A012810
READ-COMPARE * WHICH WAS SET IN THE BIT SWS. THE DATA IS THEN 3A012820
* READ AND COMPARED TO THE BIT SWITCHES. THE HEAD 3A012830
* MAY BE POSITIONED WITH SCOPE LOOP 6.08. THIS 3A012840
* WILL DESTROY THE SECTOR ADDRESS. IT MAY BE RE- 3A012850
* STORED BY PLACING THE SECTOR NUMBER IN THE BIT 3A012860
* SWITCHES AND EXECUTING THE PROGRAM ONCE. 3A012870
* THE PROGRAM WILL HALT AT WAIT 2 AFTER EACH PASS. 3A012880
* 3A012890
A. PRELOAD SWS * SET THE AREA CODE IN 0-7 FOR THE DISC TO BE USED 3A012900
* 3A012910
* DRIVE 0 --- 20XX 3A012920
* DRIVE 1 --- 88XX 3A012930
* DRIVE 2 --- 90XX 3A012940
* DRIVE 3 --- 98XX 3A012950
* DRIVE 4 --- A0XX 3A012960
* 3A012970
B. LOADING * LOAD IPL FROM CARD OR PAPER TAPE. 3A012980
* 3A012990
C. WAITS 1 * SET DATA IS BE WRITTEN IN SWITCHES 0-15. 3A013000
* 3A013010
2 * HALT AFTER ONE PASS. TO LOOP PROGRAM, LOAD /1000 3A013020
* INTO LOCATION /001E. 3A013030
* 3A013040
3 * LOST WRITE INTERRUPT. SEE COMMENTS. 3A013050
* 3A013060
4 * LOST READ INTERRUPT. SEE COMMENTS. 3A013070
* 3A013080
6 * COMPARE ERROR BETWEEN THE DATA READ AND THE BIT 3A013090
* SWITCHES. THE BITS IN ERROR WILL BE ON IN THE 3A013100
* ACCUMULATOR. TO LOOP ON ERROR, LOAD /1000 INTO 3A013110
* LOCATION /0017. 3A013120
* 3A013130
D. RESTART * 1. TO RESTART PROGRAM OR RESET SWITCH SETTINGS, 3A013140
* DEPRESS IMMEDIATE STOP AND RESET PUSH BUTTONS 3A013150
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS. 3A013160
* 3. DEPRESS START. 3A013170
* 3A013180
E. COMMENTS * 1. TO RUN THE PROG WITH INTERRUPT DELAY SWITCH 3A013190
* ON OR BYPASS THE INTERRUPT WAIT LOAD /600C 3A013200
* INTO LOCATION /0047 AND /004A AND RESTART. 3A013210
* 3A013220
* 2. TO GET A FASTER LOOP THAN THE ABOVE PLACE 3A013230
* /70FE IN THE NEXT LOCATION AFTER THE XIO. THE 3A013240
* XIO WILL BE EXECUTED AFTER EACH BRANCH. 3A013250
* 3A013260
* 3. IF INTERRUPT IS LOST, B REG WILL CONTAIN 3A013270
* DATA WORD AND ARITH REG WILL CONTAIN WAIT 3A013280
* NUMBER /0003 OR /0004. 3A013290
* 3A013300
***** 3A013310
0000 ORG 0 3A013320
0000 0 6020 DCBGN LDX DCBLD GO TO PROG 3A013330
0001 0 0000 DCSWS DC *- SW READ IN AREA 3A013340
0002 0 003A DCON5 DC /003A CONSTANT 3A013350
0003 0 0000 DCXR3 DC *- INDEX REG 3 3A013360
0004 0 6000 DCON1 DC /6000 CONSTANT 3A013370
0005 0 7010 DC /7010 CONSTANT 3A013380
0006 0 2820 DCON2 DC /2820 CONSTANT 3A013390
0007 0 00C3 DC /00C3 CONSTANT 3A013400
0008 0 0001 DCBSW DC DCSWS SW READ IN ADRS 3A013410
0009 0 0000 DC /0000 *A* DC /3A00 READ BIT SWS 3A013420
000A 0 000B DC DCINT INTERRUPT ADRS 3A013430
000B 0 0000 DCINT DC *- INTERRUPT ENTRY 3A013440
000C 0 083F XIO DCDSW SENSE DSW 3A013450
000D 0 1001 DCON3 SLA 1 ALSO A CONSTANT 3A013460
000E 0 1001 SLA 1 *

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1130 SCOPE LOOP PROGRAMS

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000F 0 4868 BOSC E2 IS DISK READY 3A013470
0010 0 600C LDX DCINT&1 * NO 3A013480
0011 0 C03A LD DCDSW * YES 3A013490
0012 0 4818 BSC E- WAS LAST OP A READ 3A013500
0013 0 7034 MDX DC6 * NO 3A013510
0014 0 0000 DC5 DC /0000 *A* LD 3 1 3A013520
0015 0 FOEB EOR DCSWS COMPARE SWS 3A013530
0016 0 4820 BSC Z ANY ERRORS 3A013540
0017 0 3006 WAIT 6 * YES 3A013550
0018 0 COEA LD DCXR3 ADJ I/O ADRS 3A013560
0019 0 80EE A DCBSW * 3A013570
001A 0 D0E8 STO DCXR3 * 3A013580
001B 0 F02F EOR DCEND * 3A013590
001C 0 4820 BSC Z REACHED LIMIT 3A013600
001D 0 70F6 MDX DC5 * NO 3A013610
001E 0 3002 WAIT 2 ONE PASS COMPLETE 3A013620
001F 0 701C MDX DC1 START OVER 3A013630
* 3A013640
DCBLD LD DCBLD DCN5 INITIALIZATION 3A013650
0020 0 C0E1 SLA 8 GET CONSTANT 3A013660
0021 0 1008 STD DCBSW&1 READ BIT SW IOCC 3A013670
0022 0 D0E6 XIO DCBSW READ SWS 3A013680
0023 0 08E4 LDD DCSWS GET AREA CODE 3A013690
0024 0 C8DC RTE 12 A- /000X Q- /000X 3A013700
0025 0 18CC AD DCON1 A- /600X Q- /701X 3A013710
0026 0 88DD RTE 4 A- /X600 Q- /X701 3A013720
0027 0 18C4 STD DCDSW SET DSW IOCC 3A013730
0028 0 D823 RTE 16 A- /X701 Q- /X600 3A013740
0029 0 18D0 LD DCON1 A- /6000 Q- /X600 3A013750
002A 0 C0D9 SRA 8 A- /0060 Q- /X600 3A013760
002B 0 1808 STD DCRD SET READ IOCC 3A013770
002C 0 D821 RTE 11 A- /C000 Q- /0C0X 3A013780
002D 0 18CB EOR DCON1 A- /A000 Q- /0C0X 3A013790
002E 0 F0D5 RTE 21 A- /0060 Q- /X500 3A013800
002F 0 18D5 STD DCWR SET WRITE IOCC 3A013810
0030 0 D81F LDD DCON2 A- /2820 Q- /00C3 3A013820
0031 0 C8D4 SRA 5 A- /0141 Q- /00C3 3A013830
0032 0 1805 STO /0060 SET WORD COUNT 3A013840
0033 0 D02C A DCWR A- /01A1 Q- /00C3 3A013850
0034 0 801B STO DCXR3 SET INDEX REG 3 3A013860
0035 0 D0CD STO DCEND SET LIMIT CNTL 3A013870
0036 0 D014 RTE 8 A- /C301 Q- /A100 3A013880
0037 0 18C8 STD DC5 SET LD 3 1 3A013890
0038 0 D0DB EOR DCON3 A- /D300 Q- /A100 3A013900
0039 0 F0D3 STO DC3 SET STO 3 0 3A013910
003A 0 D003 WAIT 1 SET DATA PATTERN 3A013920
003B 0 3001 DC1 XIO DCBSW READ BIT SWS 3A013930
003C 0 08CB LD DCSWS GET BIT SWS 3A013940
003D 0 C0C3 DC3 DC /0000 *A* STO 3 0 3A013950
003E 0 0000 LD DCXR3 ADJ I/O ADRS 3A013960
003F 0 C0C3 S DCBSW * 3A013970
0040 0 90C7 STO DCXR3 * 3A013980
0041 0 D0C1 EOR DCWR 3A013990
0042 0 F00D BSC Z REACHED LIMIT 3A014000
0043 0 4820 MDX DC3-1 * NO 3A014010
0044 0 70F8 STO DCDSW * YES, CLEAR SW 3A014020
0045 0 D006 XIO DCWR WRITE A RECORD 3A014030
0046 0 0809 WAIT 3 WAIT FOR WRITE INTR 3A014040
0047 0 3003 DC6 STX DCDSW SET SWITCH 3A014050
0048 0 6803 XIO DCRD READ A RECORD 3A014060
0049 0 0804 WAIT 4 WAIT FOR READ INTR 3A014070
004A 0 3004 ***** 3A014080
004B 0 0040 DCEND DC /0040 THE NEXT FIVE WORDS ARE 3A014090
004C 0 9000 DCDSW DC /9000 * USED FOR PROGRAM 3A014100
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A014110
004E 0 2000 DCRD DC /2000 * FOR THE PID AND TWO FOR 3A014120
004F 0 0001 DC /0001 * SEQUENCE. 3A014130
0050 0 DCWR EQU DCRD&2 3A014140

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***** 3A014160
* 3A014170
6.10 1627 PLOTTER * 1. THE PROGRAM EXECUTES ALTERNATE FUNCTIONS
* 3A014180 WHICH HAVE BEEN SELECTED IN THE BIT SWS
* 3A014190
* 2. AN OPTION IS AVAILABLE TO SET UP A VARIABLE
* 3A014200 DELAY BETWEEN XIO WRITE EXECUTIONS.
* 3A014210
* 3. AN OPTION IS AVAILABLE TO HALT THE PROGRAM
* 3A014220 AFTER THE COMPLETION OF THE EXECUTION OF
* 3A014230 AN ALTERNATE XIO SEQUENCE.
* 3A014240
* 3A014250
A. PRELOAD SWS * 1. IF DELAY IS DESIRED, SET DELAY CONTROL
* 3A014260 VALUE IN BIT SWITCHES 1 THRU 13.
* 3A014270 *NOTE* SWS 1 THRU 13 ALL ON, MAX DELAY.
* 3A014280 SWS 1 THRU 13 ALL OFF, NO DELAY.
* 3A014290
* 2. IF A WAIT AFTER EACH PROGRAM PASS IS
* 3A014300 DESIRED, TURN ON BIT SWITCH 15.
* 3A014310
* 3A014320
B. LOADING * LOAD IPL FROM CARD OR PAPER TAPE.
* 3A014330
* 3A014340
C. WAITS 1 * SET DESIRED FUNCTION CODES IN BIT SWITCHES
* 3A014350 0 THRU 15. SEE PAGE 2A FOR BIT SW CODES.
* 3A014360 1ST FUNCTION CODE IN SWS 0 THRU 5.
* 3A014370 2ND FUNCTION CODE IN SWS 8 THRU 13.
* 3A014380
* 3A014390 TURN ON PLOTTER AND MAKE READY.
* 3A014400 DEPRESS START.
* 3A014410
* 3A014420
2 * NORMAL PROGRAM WAIT IF 1 PASS OPTION HAS BEEN
* 3A014430 SELECTED. DEPRESS START TO MAKE ANOTHER PASS.
* 3A014440
* 3A014450
3 * NO INTERRUPT GENERATED AFTER XIO WRITE
* 3A014460 COMMAND WAS GIVEN. SEE COMMENTS.
* 3A014470
* 3A014480
D. RESTART * 1. TO RESTART PROGRAM OR RESET INITIAL PRELOAD
* 3A014490 SWITCH SETTINGS, DEPRESS IMMEDIATE
* 3A014500 STOP AND RESET PUSH BUTTONS.
* 3A014510
* 3A014520 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS.
* 3A014530
* 3A014540
* 3A014550
* 3A014560
* 3. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON
* 3A014570 OR TO BYPASS THE INTERRUPT WAIT, LOAD /600D
* 3A014580 INTO LOCATION /0034 AND DO A PROGRAM RESTART.
* 3A014590
* 3A014600
* 3A014610
* 3A014620
* 3A014630
* 3A014640
***** 3A014650
0000 ORG 0
0000 0 6012 PLBGN LDX PLBLD *A* TO /601E LDX PLRDS
0001 0 0001 PLONE DC 1 CONSTANT ONE
0002 0 0006 PLBSW DC PLDSW BIT SW SAVE AREA
0003 0 003A DC /003A *A* TO /3A00 RD BIT SWS
0004 0 0006 PLOT DC PLDSW CHARACTER ADDRESS
0005 0 0029 DC /0029 *A* TO /2900 XIO WRITE
0006 0 0000 PLDSW DC *-* BIT SW READIN AREA
0007 0 002F DC /002F *A* TO /2F01 XIO SENSE
0008 0 601E PLRST LDX PLRDS RESET START MOD
0009 0 0000 PLDSV DC *-* DSW SAVE AREA
000A 0 0000 PLSET DC *-* SW OPTION/DELAY SAVE
000B 0 000C DC PLIN3 INTERRUPT ADDRESS
000C 0 0000 PLIN3 DC *-* INTERRUPT LEVEL 3
000D 0 08F8 XIO DC PLDSW SENSE RESET DSW
000E 0 D0FA STO PLDSV SAVE DSW
000F 0 4850 BOSC - RESET INT LEVEL
0010 0 70FC MDX PLIN3&1 RESENSE DSW
0011 0 7023 MDX PLRET BRANCH TO DELAY
3A014830

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0012 0 C0F2 PLBLD LD PLOT&1 BUILD WRITE IOCC 3A014840
0013 0 1008 PLCTL SLA 8 * 2ND CHAR SW 3A014850
0014 0 D0F0 STO PLOT&1 * 3A014860
0015 0 C0F1 LD PLDSW&1 BUILD SENSE RESET 3A014870
0016 0 1008 SLA 8 * 3A014880
0017 0 E8E9 OR PLONE * 3A014890
0018 0 D0EE STO PLDSW&1 * 3A014900
0019 0 C0E9 LD PLBSW&1 BUILD READ BIT SW 3A014910
001A 0 1008 SLA 8 * IOCC 3A014920
001B 0 D0E7 STO PLBSW&1 * 3A014930
001C 0 C0EB LD PLRST SET UP RESET AND 3A014940
001D 0 D0E2 STO PLBGN * START BRANCH 3A014950
001E 0 08E3 PLRDS XIO PLBSW READ BIT SWS FOR 3A014960
001F 0 C0E6 LD PLDSW * PROG OPTS/DELAY 3A014970
0020 0 D0E9 STO PLSET * 3A014980
0021 0 3001 WAIT 1 SET CHARS IN SWS 3A014990
0022 0 08DF PLSTR XIO PLBSW READ BIT SWS 3A015000
0023 0 C0E2 LD PLDSW CK FOR NO COMMAND 3A015010
0024 0 180A SRA 10 * ENTERED 3A015020
0025 0 4808 BSC & * 3A015030
0026 0 70FA MDX PLSTR-1 * NO, SENSE SWS 3A015040
0027 0 CODE LD PLDSW * 3A015050
0028 0 1008 SLA 8 * 3A015060
0029 0 180A SRA 10 * 3A015070
002A 0 4808 BSC & * 3A015080
002B 0 70F5 MDX PLSTR-1 * NO, SENSE SWS 3A015090
002C 0 C8DB PLSEN LDD PLDSV-1 LOAD LAST DSW IN Q . 3A015100
002D 0 08DB XIO PLDSW CHK DEVICE NOT BUSY 3A015110
002E 0 D0DA STO PLDSV SAVE DSW 3A015120
002F 0 1004 SLA 4 * 3A015130
0030 0 4828 BSC &Z * 3A015140
0031 0 70FA MDX PLSEN * 3A015150
0032 0 C8D5 LDD PLDSV-1 LOAD LAST DSW IN Q . 3A015160
0033 0 08D0 XIO PLOT WRITE CHARACTER 3A015170
0034 0 3003 WAIT 3 WAIT FOR INTERRUPT 3A015180
0035 0 C8D2 PLRET LDD PLDSV-1 LOAD LAST DSW IN Q . 3A015190
0036 0 C0D3 LD PLSET SET UP DELAY AND 3A015200
0037 0 1801 SRA 1 * EXECUTE DELAY 3A015210
0038 0 90C8 PLLOP S PLONE * 3A015220
0039 0 4810 BSC - * 3A015230
003A 0 70FD MDX PLLOP * 3A015240
003B 0 COCA LD PLDSW LD, SET UP 2ND CHAR 3A015250
003C 0 4804 BSC E CHK IF WAIT REQUESTED 3A015260
003D 0 3002 WAIT 2 YES 3A015270
003E 0 1802 SRA 2 NO, CHK 2ND CHAR OK 3A015280
003F 0 4818 BSC &- * 3A015290
0040 0 70E0 MDX PLSTR-1 NO, GO TO WAIT 1 3A015300
0041 0 100A SLA 10 YES, SET UP 2ND CHAR 3A015310
0042 0 D0C3 STO PLDSW * 3A015320
0043 0 C0CF LD PLCTL CHK IF 2ND CHAR SW 3A015330
0044 0 4820 BSC Z * OFF 3A015340
0045 0 7002 MDX PLALT NO, BRANCH 3A015350
0046 0 68CC STX PLCTL YES, SET 2ND CHAR SW 3A015360
0047 0 70DA MDX PLSTR GO LOOP PROGRAM 3A015370
0048 0 1010 PLALT SLA 16 CLR 2ND CHAR SW 3A015380
0049 0 D0C9 STO PLCTL * 3A015390
004A 0 70E1 MDX PLSEN GO CHK IF PRINT BUSY 3A015400
***** 3A015410
004B 0 0040 DC /0040 THE LAST FIVE WORDS ARE 3A015420
004C 0 9000 DC /9000 * USED FOR PROGRAM 3A015430
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A015440
004E 0 1000 DC /1000 * FOR THE PID AND TWO FOR 3A015450
004F 0 2000 DC /2000 * SEQUENCE. 3A015460

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1130 SCOPE LOOP PROGRAMS

1130 SCOPE LOOP PROGRAMS

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*****
6.11 2501 READER
* 1. THE PROGRAM READS 80 COLUMNS OF DATA AND
*   COMPARES EACH WORD WITH THE BIT SWITCHES.
* 2. AN OPTION IS AVAILABLE TO SET UP A VARIABLE
*   DELAY BETWEEN XIO READ EXECUTIONS.
* 3. AN OPTION IS AVAILABLE TO BYPASS WAIT 6
*   ON COMPARE ERRORS.
A. PRELOAD SWS
* 1. IF DELAY IS DESIRED, SET DELAY CONTROL
*   VALUE IN BIT SWITCHES 1 THRU 13.
*   *NOTE* SWS 1 THRU 13 ALL ON, MAX DELAY.
*   SWS 1 THRU 13 ALL OFF, NO DELAY.
* 2. IF BYPASS COMPARE ERROR WAIT 6 OPTION IS
*   DESIRED, TURN ON BIT SWITCH 15.
B. LOADING
* LOAD IPL FROM CARD OR PAPER TAPE.
C. WAITS
1 * SET BIT SWS 0 THRU 11 TO EXPECTED COLUMN
* DATA AND SET BITS 12 THRU 15 OFF.
* LOAD PREPUNCHED CARDS INTO READER AND MAKE READY.
* DEPRESS START.
4 * NO INTERRUPT GENERATED AFTER XIO READ.
* COMMAND WAS GIVEN. SEE COMMENTS.
6 * COMPARE ERROR. ACCUMULATOR CONTAINS BITS READ.
* IF ACCUMULATOR CONTAINS /DOCB, COLUMN READ WAS
* NOT STORED INTO READ/IN AREA.
* DEPRESS START TO COMPARE NEXT COLUMN.
* TO BYPASS COMPARE ERROR WAIT, SEE PRELOAD.
D. RESTART
* 1. TO RESTART PROGRAM OR RESET INITIAL PRELOAD
*   SWITCH SETTINGS, DEPRESS IMMEDIATE
*   STOP AND RESET PUSH BUTTONS.
* 2. SET DESIRED PRELOAD BIT SWITCH SETTINGS.
* 3. DEPRESS START.
E. COMMENTS
* 1. LAST DSW SENSED IS DISPLAYED IN THE Q REG.
* 2. TO RUN PROGRAM WITH INTERRUPT DELAY SW ON
*   OR TO BYPASS THE INTERRUPT WAIT, LOAD /600F
*   INTO LOCATION /002F AND DO A PROGRAM RESTART.
* 3. TO SET UP LOOP TO EXECUTE XIO, LOAD /600F
*   INTO LOCATION /002F AND LOAD /6027 INTO
*   LOCATION /0013 AND DO A PROGRAM RESTART.
*****
0000      ORG      0
0001 0 6035  CRBGN LDX  CRBLD  *A* TO /6030 LDX CRRST
0002 0 0001  CRONE DC   1      CONSTANT 1
0003 0 0004  CRBSW DC   CRDSW  BIT SW SAVE ADDR
0004 0 003A  DC       /003A  *A* TO /3A00 RD BIT SWS
0005 0 6030  CRDSW LDX  CRRST  BIT SW SAVE AREA
0006 0 0027  DC       /0027  *A* TO /4F01 XIO SENSE DSW
0007 0 0036  CRRDR DC   CRARA  CARD READ IN ADDR
0008 0 0027  DC       /0027  *A* TO /4E00 XIO START RDR
0009 0 00FF  CRERR DC   /00FF  SAVE READ ERROR
0010 0 0000  CRDSV DC   *--    LAST DSW SENSED
0011 0 0000  CREND DC   *--    *A* TO /D11A END OF RD AREA
0012 0 C022  CRSRA DC   /C022  LD READ AREA
0013 0 000E  DC       CRIN4  INTERRUPT ADDR
0014 0 0005  CR080 DC  /0005  *A* TO /0050 CONSTANT 80
0015 0 0000  CRIN4 DC   *--    INTERRUPT ENTRY
0016 0 08F4  XIO     CRDSW  SENSE DSW
0017 0 00F8  STO     CRDSV  SAVE DSW
0018 0 1004  SLA     4      CK FOR OP COMPLETE
0019 0 4850  BOSC   -      *
0020 0 70FB  MDX     CRIN4&1 NO, RESENSE DSW

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0014 0 C022  CRLD  LD     CRARA&1  LOAD COLUMN READ
0015 0 00F2  STO     CRERR   SAVE BITS READ
0016 0 F0ED  FOR     CRDSW   COMPARE WITH PATT WD
0017 0 4818  BSC     &-     CK FOR COMPARE ERR
0018 0 7006  MDX     CRMOD   NO, SET UP NEXT CHK
0019 0 C01B  LD     CRBLD   YES, CK LOOP OPT
001A 0 100F  SLA     15     *
001B 0 4828  BSC     &Z   *
001C 0 700A  MDX     CRLOP-3 LOOP ERR OPTION ON
001D 0 C8FA  LDD     CRERR   LD DSW AND ERR BITS
001E 0 3006  WAIT    6     COMPARE ERROR WAIT
001F 0 C0F4  CRMOD  LD     CRLD   SET UP NEXT COMPARE
0020 0 80E0  A       CRONE  *
0021 0 00F2  STO     CRLD   *
0022 0 90E7  S       CREND   CK IF ALL COLUMNS
0023 0 4828  BSC     &Z   * CHECKED
0024 0 70EF  MDX     CRLD   NO, COMPARE NXT COL
0025 0 C0F5  LD     CRSRA  SET UP FOR NXT CARD
0026 0 D0ED  STO     CRLD   *
0027 0 C8F0  LDD     CRERR   LOAD LAST DSW IN Q
0028 0 C00C  LD     CRBLD  SET UP DELAY
0029 0 1801  SRA     1      *
002A 0 90D6  CRLDP  S     CRONE  *
002B 0 4810  BSC     -     *
002C 0 70FD  MDX     CRLOP  *
002D 0 08D4  CRSTR  XIO  CRBSW  RD BIT SWS PATT WD
002E 0 08D7  XIO     CRRDR  READ A CARD
002F 0 3004  WAIT    4     WAIT FOR INTERRUPT
0030 0 08D1  CRRST  XIO  CRBSW  RD SWS FOR DELAY/OPT
0031 0 C0D2  LD     CRDSW  SAVE DELAY/OPTIONS
0032 0 D002  STO     CRBLD  *
0033 0 3001  WAIT    1     SET PATTERN IN SWS
0034 0 70F8  MDX     CRSTR  GO READ BIT SWS
0035 0 C0CD  CRBLD  LD     CRBSW&1 BUILD PROGRAM
0036 0 1008  CRARA  SLA   8     *A* TO /0050 WD CNT 80
0037 0 D0CB  STO     CRBSW&1 *A* TO *-- READ/IN AREA
0038 0 C0CB  LD     CRDSW  *
0039 0 D0C6  STO     CRBGN  *
003A 0 C0CA  LD     CRDSW&1 *
003B 0 1001  SLA     1      *
003C 0 E8C4  OR     CRONE  *
003D 0 1008  SLA     8      *
003E 0 E8C2  OR     CRONE  *
003F 0 D0C5  STO     CRDSW&1 *
0040 0 C0C6  LD     CRRDR&1 *
0041 0 1009  SLA     9      *
0042 0 D0C4  STO     CRRDR&1 *
0043 0 C0C9  LD     CR080  *
0044 0 1004  SLA     4      *
0045 0 D0F0  STO     CRARA  *
0046 0 80C4  A       CRSRA  *
0047 0 D0C2  STO     CREND  *
0048 0 70E7  MDX     CRRST  EXECUTE PROGRAM
*****
0049 0 0000  DC     0      SPACE FILLER
004A 0 0000  DC     0      *
004B 0 0040  DC     /0040 THE LAST FIVE WORDS ARE
004C 0 9000  DC     /9000 * USED FOR PROGRAM
004D 0 2000  DC     /2000 * IDENTIFICATION. THREE
004E 0 1000  DC     /1000 * FOR THE PID AND TWO FOR
004F 0 1000  DC     /1000 * SEQUENCE.

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***** 3A016780
* 3A016790
6.12 1403 PRINTER * THIS PROGRAM WILL PRINT ANY CHARACTER ENTERED 3A016800
* IN THE BIT SWITCHES 1-7 AND 9-15. IF BIT 14 IS ON 3A016810
* THE BIT SWS 1-12 WILL BE THE CHANNEL THAT THE 3A016820
* CARRIAGE WILL SKIP TO AFTER PRINTING. 3A016830
* 3A016840
A. PRELOAD SWS * BIT SW 15- HALT AFTER ONE PASS. 3A016850
* 14- CARR SKIP FUNCTION. 3A016860
* 1 THRU 12- CHANNEL NUMBER TO USE FOR SKIP. 3A016870
* 3A016880
B. LOADING * IPL MODE FROM CARDS OR PAPER TAPE. 3A016890
* 3A016900
C. WAIT 1 * SET CHARACTER TO PRINT, 1-7 AND 9-15. 3A016910
* 3A016920
2 * ONE PASS COMPLETED, PRESS START TO CONTINUE. 3A016930
* 3A016940
3 * LOST PRINTER INTERRUPT. 3A016950
* 3A016960
5 * LOST CARRIAGE INTERRUPT. 3A016970
* 3A016980
6 * PARITY ERROR FOUND IN THE DSW. 3A016990
* 3A017000
D. RESTART * PRESS IMMEDIATE STOP AND RESET. PRELOADING 3A017010
* SWITCHES MAY BE SET AS DESIRED. PRESS START. 3A017020
* 3A017030
E. COMMENTS * 1. TO RUN THE PROG WITH INTERRUPT DELAY SWITCH 3A017040
* ON OR BYPASS THE INTERRUPT WAIT LOAD /60IF 3A017050
* INTO LOCATION /001D AND /0030 AND RESTART. 3A017060
* 3A017070
* 2. TO GET A FASTER LOOP THAN THE ABOVE PLACE 3A017080
* /70FE IN THE NEXT LOCATION AFTER THE XIO. THE 3A017090
* XIO WILL BE EXECUTED AFTER EACH BRANCH. 3A017100
* 3A017110
***** 3A017120
0000 ORG 0 3A017130
0000 0 6033 LDX FPBLD *A* LDX FPSTR 3A017140
0001 0 0000 FPSWS DC *- * BIT SWITCH STG 3A017150
0002 0 0000 FPDSW DC /D000 *A* WORD COUNTER 3A017160
0003 0 F010 DC /F010 *A* DC /AF01 3A017170
0004 0 9000 FPCAR DC /9000 CHANNEL BITS 3A017180
0005 0 C000 DC /C000 *A* DC /AC00 CARR CNTL 3A017190
0006 0 0001 FPBSW DC FPSWS BIT SW STG ADRS & ONE 3A017200
0007 0 003A DC /003A *A* DC /3A00 READ BIT SWS 3A017210
0008 0 0004 FPSKP DC FPCAR CARR CHAN ADRS 3A017220
0009 0 9000 DC /9000 *A* DC /A900 SKIP IOCC 3A017230
000A 0 0033 FPPRT DC FPOUT&1 PRINT AREA ADRS 3A017240
000B 0 000A DC /000A *A* DC /AD00 PRINT IOCC 3A017250
000C 0 001E DC FPINT INTERRUPT ADRS 3A017260
* 3A017270
* START AND RESTART OF PROGRAM 3A017280
* 3A017290
* 3A017300
FPSTR XIO FPBSW READ BIT SWITCHES 3A017310
LD FPSWS GET SW SETTINGS 3A017320
STO FPSWS-3 * AND SAVE 3A017330
SRA 3 3A017340
STO FPCAR SET CHAN NUMBER 3A017350
WAIT 1 SET CONSOLE SWS 3A017360
FP1 XIO FPBSW READ PRINTER CODE 3A017370
LD FPOUT GET WORD COUNT 3A017380
STO FPDSW LOAD XR 2 3A017390
LD FPSWS GET PRINT CODE 3A017400
FP2 DC /00D2 *A* STO 2 FPOUT 3A017410
LD FPDSW GET COUNT AND 3A017420
S FPBSW * SUB ONE 3A017430
BSC Z AREA FILLED 3A017440
MDX FP2-2 * NO 3A017450
XIO FPPRT PRINT A LINE

```

```

001D 0 3003 WAIT 3 WAIT FOR PRINT INTERRUPT 3A017460
001E 0 0000 FPINT DC *- * INTERRUPT ENTRY 3A017470
001F 0 08E2 XIO FPDSW SENSE DSW 3A017480
0020 0 4844 BOSC E IS PRINTER READY 3A017490
0021 0 601F LDX FPINT&1 * NO 3A017500
0022 0 4828 BSC &Z PARITY ERROR 3A017510
0023 0 3006 WAIT 6 * YES 3A017520
0024 0 1002 SLA 2 * NO 3A017530
0025 0 4810 BSC - PRINT COMPLETE 3A017540
0026 0 70EC MDX FP1 * NO, CARR INTR 3A017550
0027 0 C0D6 LD FPSWS-3 GET CONTROLS 3A017560
0028 0 4804 BSC E HALT ON 3A017570
0029 0 3002 WAIT 2 * YES 3A017580
002A 0 100E SLA 14 * NO 3A017590
002B 0 4810 BSC - CARR SKIP FUNC 3A017600
002C 0 7002 MDX FP8 * NO 3A017610
002D 0 08DA XIO FSKP SKIP TO CHAN 3A017620
002E 0 7001 MDX FP&E1 GO WAIT INTERRUPT 3A017630
002F 0 08D4 XIO FPCAR * YES, SPACE 3A017640
0030 0 3005 WAIT 5 WAIT FOR CARR INTR 3A017650
* 3A017660
* FPO01 DC /0001 CONSTANT 3A017670
* FPOUT DC 60 WORD COUNT 3A017680
* 3A017690
* THIS WILL BE THE PRINT AREA AFTER 3A017700
* INITIALIZATION 3A017710
* 3A017720
* 3A017730
FPBLD LD FPRES 3A017740
STO 0 * SET RESTART 3A017750
LDD FPPRT+1 * A- /000A Q- /000A 3A017760
AD FPCAR * A- /C00A Q- /900A 3A017770
RTE 4 * A- /AC00 Q- /A900 3A017780
STD FPCAR * CONTROL IOCC 3A017790
STO FSKP&1 * SKIP IOCC 3A017800
LDD FPPRT+1 * A- /000A Q- /000A 3A017810
AD FPDSW * A- /D00A Q- /F01A 3A017820
RTE 4 * A- /AD00 Q- /AF01 3A017830
STD FPDSW * SENSE DSW IOCC 3A017840
STO FPPRT&1 * PRINT IOCC 3A017850
LD FPBSW&1 * 3A017860
SLA 8 * 3A017870
STO FPBSW&1 * READ BIT SW IOCC 3A017880
LD FP2 * 3A017890
SLA 8 * 3A017900
OR FPPRT * 3A017910
S FPO01 ADJUST DISPLACEMENT 3A017920
STO FP2 * BUILD STO 2 FPPRT 3A017930
FPRES LDX FPSTR GO TO PROGRAM 3A017940
***** 3A017950
DC 0 SPACE FILLER 3A017960
DC 0 * 3A017970
DC 0 * 3A017980
DC /0040 THE LAST FIVE WORDS ARE 3A017990
DC /9000 * USED FOR PROGRAM 3A018000
DC /2000 * IDENTIFICATION. THREE 3A018010
DC /1000 * FOR THE PID AND TWD FOR 3A018020
DC /0800 * SEQUENCE.

```

1130 SCOPE LOOP PROGRAMS

1130 SCOPE LOOP PROGRAMS

```

***** 3A018040
* 3A018050
6.13 1132 PRINTER * THE CHARACTER ENTERED IN SWS 0-7 IS PRINTED IN
* ALL PRINT POSITIONS. 3A018060
* 3A018070
* 3A018080
A. PRELOAD SWS * BIT SW 15--HALT AFTER EACH LINE PRINTED. SW 15 3A018090
* ALSO CAUSES ONE EXTRA IDLE SCAN CYCLE. 3A018100
* THIS HAS A NEGLIGIBLE AFFECT ON SPEED. 3A018110
* 8-15--PRINT SPEED CONTROL--ENTER THE 3A018120
* DESIRED NUMBER OF IDLE SCAN CYCLES 3A018130
* TO BE TAKEN BETWEEN PRINT CYCLES. 3A018140
* 0-7=VALID CHARACTER--PRINT CHARACTER AS 3A018150
* SHOWN ON PAGE 2. 3A018160
* 0-7=INVALID CHARACTER--IDLE CONTINUOUSLY. 3A018170
* 3A018180
* NOTE--PROGRAM ALWAYS TURNS ON BIT 10 TO PREVENT 3A018190
* OPERATING AT EXCESSIVE SPEEDS. SPEED MAY 3A018200
* BE INCREASED BY MANUALLY CHANGING CONSTANT 3A018210
* AT CORE LOCATION 0008. USE CAUTION. 3A018220
* 3A018230
* SWITCH SETTINGS MAY BE CHANGED AT ANY TIME. 3A018240
* 3A018250
B. LOADING * IPL MODE FROM CARDS OR PAPER TAPE 3A018260
* 3A018270
C. WAIT 2 * ONE PASS COMPLETED, PRESS START TO CONTINUE. 3A018280
* 3A018290
3 * NO EMITTER RESPONSE INTRPT, RESTART TO CONTINUE 3A018300
* 3A018310
5 * NO SPACE RESPONSE INTERRUPT, RESTART TO CONTINUE 3A018320
* 3A018330
D. RESTART * PRESS IMMEDIATE STOP AND RESET. PRELOADING 3A018340
* SWITCHES MAY BE SET AS DESIRED. PRESS START. 3A018350
* 3A018360
E. COMMENTS * TO RUN WITHOUT INTERRUPTS..MANUALLY ENTER 3A018370
* HEX 600B AT CORE LOCATIONS 0001 AND 003A. 3A018380
* 3A018390
* TO CHANGE POSITIONS PRINTED..MANUALLY ENTER 3A018400
* DESIRED PATTERN IN CORE LOCATIONS 001E AND 001F. 3A018410
* AT LEAST ONE BIT MUST BE ON IN SECOND WORD 001F. 3A018420
* 3A018430
***** 3A018440
0000 ORG 0 3A018450
0000 0 6017 PRGO LDX PRDSW-1 *A* XIO PRSPS SPACE PTR 3A018460
0001 0 3005 WAIT 5 WAIT FOR INTERRUPT 3A018470
* 3A018480
0002 0 001A PRRDS DC PRSWS 3A018490
0003 0 00FF DC /00FF *A* DC /3A32 RD SWS 3A018500
0004 0 0018 PRRD DC PREMT 3A018510
0005 0 E8C8 DC /E8C8 *A* DC /3200 RD EMITTER 3A018520
0006 0 7013 DC /7013 3A018530
0007 0 4803 DC /4803 3A018540
0008 0 0020 PRIDL DC /0020 MINIMUM IDLE SCAN CYCLES 3A018550
0009 0 000A DC PRINT INTERRUPT ADDRESS 3A018560
000A 0 0827 PRINT DC /0827 INTERRUPT ENTRY 3A018570
000B 0 080C XIO PRDSW 3A018580
000C 0 4850 BOSC - EMITTER RESPONSE 3A018590
000D 0 7023 MDX PRSPR * NO, TRY SPACE RESPONSE 3A018600
000E 0 C018 LD PRSCN+7 3A018610
000F 0 4820 BSC Z SCAN FIELD ZERO 3A018620
0010 0 7018 MDX PREND * NO, GO STOP PRINTER 3A018630
0011 0 C039 LD PRDLY 3A018640
0012 0 4808 BSC + LAST IDLE SCAN CYCLE 3A018650
0013 0 7027 MDX PRPRT * YES, GO PRINT 3A018660
0014 0 9034 S PR DECRE IDLE COUNT BY ONE 3A018670
0015 0 D035 STD PRDLY 3A018680
0016 0 7023 MDX PRWT3 3A018690
0017 0 C0F2 LD PRINT 3A018700
0018 0 D0E7 PRDSW STO PRGO 3A018710

```

```

0019 0 C8EC LD PRRD+2 *A* DC /3701 SENSE DSW 3A018720
001A 0 18C4 PRSTR RTE 4 3A018730
001B 0 D0FD STO PRDSW+1 *A* DC /3480 START PTR 3A018740
001C 0 18D0 PRSTP RTE 16 3A018750
001D 0 D0FD STO PRSTR+1 *A* DC /3440 STOP PTR 3A018760
001E 0 F02B PRFLD EOR PRDLY-1 *A* DC /FFFF 3A018770
001F 0 D0FD STO PRSTP+1 *A* DC /FFFF 3A018780
0020 0 C8F2 PRSCN LDD PRRDS+1 3A018790
0021 0 18C8 RTE 8 3A018800
0022 0 88E0 AN PRRDS+1 3A018810
0023 0 D8FA STD PRFLD 3A018820
0024 0 C0E0 LD PRRD+1 3A018830
0025 0 1802 SRA 2 3A018840
0026 0 D0DC STO PRRDS+1 3A018850
0027 0 1008 SLA 8 3A018860
0028 0 D0DC PRSPS STO PRRD+1 3A018870
0029 0 C01C LD PR-3 *A* DC /3401 SPACE PTR 3A018880
002A 0 1802 SRA 2 3A018890
002B 0 D0FD STO PRSPS+1 3A018900
002C 0 08EF PREND XIO PRSTP STOP PRINTER 3A018910
002D 0 C0FC LD PRSWS 3A018920
002E 0 4804 BSC E BIT SW 15 ON 3A018930
002F 0 3002 WAIT 2 * YES, WAIT 3A018940
0030 0 70CF MDX PRGO 3A018950
001A 0 PRSWS EQU PRSTR 3A018960
001B 0 PREMT EQU PRDSW 3A018970
0031 0 1002 PRSPR SLA 2 3A018980
0032 0 4850 BOSC - SPACE RESPONSE 3A018990
0033 0 70D7 MDX PRINT+1 * NO, CHECK DSW AGAIN 3A019000
0034 0 10E0 SLC 32 3A019010
0035 0 D8EA STD PRSCN CLEAR 3A019020
0036 0 D8FB STD PRSCN+2 OR SET 3A019030
0037 0 D8EC STD PRSCN+4 SCAN 3A019040
0038 0 D8ED STD PRSCN+6 FIELD 3A019050
0039 0 08E0 XIO PRSTR START PRINTER 3A019060
003A 0 3003 PRWT3 WAIT 3 WAIT FOR INTERRUPT 3A019070
003B 0 08C6 PRPRT XIO PRRDS READ BIT SWITCHES 3A019080
003C 0 08C7 XIO PRRD READ EMITTER 3A019090
003D 0 C0DC LD PRSWS GET SWS 3A019100
003E 0 E8C9 OR PRIDL OR MINIMUM IDLES 3A019110
003F 0 18C8 RTE 8 3A019120
0040 0 1008 SLA 8 ISOLATE CHARACTER 3A019130
0041 0 4820 BSC Z SKIP IF NO CHAR ENTERED 3A019140
0042 0 F0D5 FDR PREMT COMPARE WITH EMITTER 3A019150
0043 0 4820 BSC Z SKIP IF SAME CHAR 3A019160
0044 0 70F5 MDX PRWT3 3A019170
0045 0 10C8 SLC 8 3A019180
0046 0 D004 STD PRDLY SET IDLE COUNT 3A019190
0047 0 C8D6 LDD PRFLD 3A019200
0048 0 70EC MDX PRSPR+4 3A019210
0049 0 0001 PR DC /0001 3A019220
004A 0 00C0 DC /00C0 3A019230
***** 3A019240
004B 0 0040 PRDLY DC /0040 THE LAST FIVE WORDS ARE 3A019250
004C 0 9000 DC /9000 * USED FOR PROGRAM 3A019260
004D 0 2000 DC /2000 * IDENTIFICATION. THREE 3A019270
004E 0 1000 DC /1000 * FOR THE PID AND TWO FOR 3A019280
004F 0 0040 DC /0040 * SEQUENCE. 3A019290
0050 0000 END 0 3A019300

```

NO STATEMENTS FLAGGED IN THE ABOVE ASSEMBLY

1130 SCOPE LOOP PROGRAMS

1130 SCOPE LOOP PROGRAMS

CPALT 000D 003E 0042
 CPBGN 0000 001C
 CPBLD 0012 0000
 CPBSW 0002 0018 001A 001D 0021
 CPCTL 0009 000E 001B 003C 003F
 CPDSV 000B 0022 0024 0028 002E 002F 0032
 CPDSW 0006 0002 0004 0015 0017 001E 0023 002D 0039 003B
 CPIN4 002C 000C 0031
 CPLOP 0036 0038
 CPONE 0001 0036
 CPRDS 001D 0009
 CPRET 0032 002B
 CPSEN 0022 000F 0011 0027 0043
 CPSET 0008 001F 0033 0040
 CPWRT 0004 0012 0014 0029
 CRARA 0036 0006 0014 0045
 CRBGN 0000 0039
 CRBLD 0035 0000 0019 0028 0032
 CRBSW 0002 002D 0030 0035 0037
 CRDSV 0009 0010
 CRDSW 0004 0002 000F 0016 0031 0038 003A 003F
 CREND 000A 0022 0047
 CRERR 0008 0015 001D 0027
 CRIN4 000E 000C 0013
 CRLD 0014 001F 0021 0024 0026
 CRLOP 002A 001C 002C
 CRMOD 001F 0018
 CRONE 0001 0020 002A 003C 003E
 CRRDR 0006 002E 0040 0042
 CRRST 0030 0004 0048
 CRSRA 000B 0025 0046
 CRSTR 002D 0034
 CRO80 000D 0043
 DCBGN 0000
 DCBLD 0020 0000
 DCBSW 0008 0019 0022 0023 003C 0040
 DCDSW 004C 000C 0011 0028 0045 0048
 DCEND 004B 001B 0036
 DCINT 000B 000A 0010
 DCON1 0004 0026 002A 002E
 DCON2 0006 0031
 DCON3 000D 0039
 DCON5 0002 0020
 DCRD 004E 002C 0049
 DCSWS 0001 0008 0015 0024 003D
 DCWR 0050 0030 0034 0042 0046
 DCXR3 0003 0018 001A 0035 003F 0041
 DC1 003C 001F
 DC3 003E 003A 0044
 DC5 0014 001D 0038
 DC6 0048 0013
 DKBD1 000F 0026
 DKBD2 0010 002A
 DKBGN 0000 001C
 DKBIT 000E 0002 001B 0021 0025 0028 002C 0031 0042
 DKBLD 001B 0000
 DKBSW 0002 001D 001F 0020 0030
 DKCON 0042 001A
 DKDSV 000B 0013 0035 0036 003D
 DKDSW 0008 0012 0022 0029 0034 0045
 DKENT 0001 0017 0037 003F
 DKHME 0004 002D 0038
 DKIN2 0011 000A 0016
 DKMOV 003A 0019 0048
 DKRST 0020 000E
 DKSEK 0006 002E 0033 003A 003C 0040 0044
 DKOFF 000D 0043
 DK004 000C 0038

FPBLD 0033 0000
 FPBSW 0006 000D 0013 0019 003F 0041
 FPCAR 0004 0008 0011 002F 0036 0038
 FPDSW 0002 0015 0018 001F 003B 003D
 FPINT 001E 000C 0021
 FPOUT 0032 000A 0014
 FPPRT 000A 001C 0035 003A 003E 0044
 FPRES 0047 0033
 FPSKP 0008 002D 0039
 FPSTR 000D 0047
 FPSWS 0001 0006 000E 000F 0016 0027
 FP001 0031 0045
 FP1 0013 0026
 FP2 0017 001B 0042 0046
 FP8 002F 002C 002E
 KYBGN 0000 0031
 KYBLD 0024 0000
 KYBSW 0002 0012 0024 0026 0036
 KYDCH 000D 0021
 KYDSP 0022 0010
 KYDSV 000B 0014
 KYDSW 0004 0002 0013 001E 0027 0029 0030 0037
 KYIN4 0011 000C 003A 003D
 KYKEY 000A 0008 000D 000F 0022 0035 003B
 KYONE 0001
 KYRD 0008 001C 002D 002F
 KYRDW 001C 0018
 KYREQ 0019 0017
 KYRST 0032 0004
 KYSEL 0006 001D 002A 002C 0033
 KYSET 0036 001B 0023
 PHBLD 0037 0000
 PHBSW 0004 0016 0018 0027 003E 0040
 PHCTR 0002 0017 0019 0026
 PHDSW 000A 0012 001E 0041 0043
 PHFED 0000 0030 003C 003D
 PHINT 0011 0008 000C 0024
 PHK50 000E 001A
 PHPCH 0006 0020 0044 0046
 PHPST 0008 0031 0039 003B
 PHRES 004A 0037
 PHSTK 000C 0033 0047 0049
 PHSWS 0003 0006 001D 001F 0028 0034
 PH1 000F 004A
 PH2 0030 0010 0036
 PH4 0020 001C
 PH6 0022 0015
 PH8 0033 002D
 PLALT 0048 0045
 PLBGN 0000 001D
 PLBLD 0012 0000
 PLBSW 0002 0019 001B 001E 0022
 PLCTL 0013 0043 0046 0049
 PLDSV 0009 000E 002C 002F 0032 0035
 PLDSW 0006 0002 0004 000D 0015 0018 001F 0023 0027 002D 003B 0042
 PLIN3 000C 000B 0010
 PLLOP 0038 003A
 PLONE 0001 0017 0038
 PLOT 0004 0012 0014 0033
 PLRDS 001E 0008
 PLRFT 0035 0011
 PLRST 0008 001C
 PLSN 002C 0031 004A
 PLSET 000A 0020 0036
 PLSTR 0022 0026 002B 0040 0047
 PR 0049 0014 0029
 PRDLY 004B 0011 0015 001E 0046
 PRDSW 0018 0000 000B 001B

1130 SCOPE LOOP PROGRAMS

PREMT 0018 0004 0042
 PRFND 002C 0010
 PRFLD 001E 0023 0047
 PRGD 0000 0018 0030
 PRIDL 0008 003E
 PRINT 000A 0009 0017 0033
 PRPRT 003B 0013
 PRRD 0004 0019 0024 0028 003C
 PRRDS 0002 0020 0022 0026 0038
 PRSCN 0020 000E 0035 0036 0037 0038
 PRSPR 0031 000D 0048
 PRSPS 0028 002B
 PRSTP 001C 001F 002C
 PRSTR 001A 001D 0039
 PRSWS 001A 0002 002D 003D
 PRWT3 003A 0016 0044
 RDARA 0001 0004 0018 001B 0032
 RDBGN 0000 002C
 RDBLD 001F 0000 002F 003C 0044
 RDBSW 0002 001F 0021 002D 0035
 RDCOP 0038 0013
 RDNSV 000B 0011 0038 0048
 RDNSW 0006 0002 0010 0015 0022 0024 002B 002E
 RDERR 000A 001C
 RDESW 0020 001D 0034 0041
 RDINT 0037 001A 001E 0047
 RDIO4 000F 0008 000C 003A
 RDLOP 003E 0040
 RDONE 000E 003E
 RDRGN 0008 0025 0027 0036
 RDRRD 0004 0014 0028 002A
 RDRST 002D 0006 0043 004A
 RDOFF 000D 0031
 STGBD 003F 0009
 STGCR 0004 0015 0022 0023
 STGHL 0005 0011 001A 0030 003A
 STGLC 0002 0024 0034 0036
 STGPG 003E 0037 003E
 STGPN 0003 000E 001F 0025 002D
 STGRD 0006 000F 0014 0017 0029 002C 0035 0041 0043
 STGRS 0048
 STGSP 0049 003F
 STGST 0009 0000 0040 0048 0049
 STGSW 0001 0010 0018
 STGXX 0008 000B 000D 0049
 STGO 0023 0020 003D
 STG1 0025 0039
 STG10 003A 0033
 STG2 0026 0044 0046
 STG3 002A 0047
 STG7 0021 001D
 TPALT 002B 0045
 TPBGN 0000 001B
 TPBLD 000D 0000
 TPBSW 0002 0014 0016 001C 0026
 TPCTL 0009 001A 002C 003F 0046
 TPDSV 000B 002E 002F 0034 0036
 TPDSW 0006 0002 0004 0010 0013 001D 0021 0028 002A 002D 0035 0042 0044
 TPIN4 0033 000C 0039
 TPLOP 003C 003E
 TPNOT 0046 0041
 TPONE 0001 0012 0017 003C
 TPPAT 0028 0025
 TPRDS 001C 0009 004A
 TPRET 003A 0032
 TPSEN 002D 0027
 TPSET 0008 001E 0022 003A 0047
 TPWRT 0004 000D 000F 0030

1130 SCOPE LOOP PROGRAMS

TP100 000A 0019 0029
 TRADV 000A 0029 002C 0041
 TRALT 003F 0047 004A
 TRARA 0024 0008 000E 0018 001A
 TRBGN 0000 002E
 TRBLD 0021 0000 0015 0018 0031 0035
 TRBSW 0010 0021 0023 002F 0039
 TRCTL 0026 003A 003D 0044
 TRDSV 0025 0003
 TRDSW 000C 0002 001D 0024 0026
 TRIN4 0001 0006 002D
 TRI4A 0012 0009
 TRLOP 001D 0014 0017 001F
 TRNOT 0043 003C
 TRPAT 0048 0038
 TRRD 000E 0007 002B
 TRRST 002F 0001
 TRSBW 0023 0010 0012 0030 0034 003E 0040 0045 0048
 TRSTR 0035 0020
 TR100 0022 0028 0049
 END OF ASSEMBLY

----- LAST PAGE -----

CORE STORAGE FUNCTION TEST

TABLE OF CONTENTS

PARAGRAPH	PAGE
1. PURPOSE	01A
2. PREREQUISITES	01A
3. USE PROCEDURE	01A
3.1 PROGRAM LOADING	
3.2 OPERATING PROCEDURE	
3.3 TERMINATING PROCEDURE	
3.4 NORMAL WAITS	
3.5 ERROR WAITS	
4. PRINTOUTS (NONE)	
5. COMMENTS	02A
5.1 DESCRIPTION OF HIGH-CORE TEST	
5.1.1 INITIALIZATIONS (PSKOS)	
5.1.2 READ/WRITE-IN-MEMORY AND ADDRESSING TEST (RSAB1)	
5.1.3 BIT-ISOLATION TEST (RSABR)	
5.1.4 WORST-CASE-PATTERN TEST (RSACJ)	
5.1.5 COMMON-PROGRAM/PROGRAM-END ROUTINE (RSASA)	
5.1.6 ERROR ROUTINE TO SERVICE NON-INTERRUPT ERRORS (RSDDD)	
5.1.7 NORMAL CONDITION OF SWITCHES	
5.2 DESCRIPTION OF CORE TEST (0 THROUGH 9 CORES)	
5.2.1 INITIALIZATIONS (RSSTA)	
5.2.2 LOAD-ZEROS-IN-CORES TEST (RSR01)	
5.2.3 LOAD-ONES-IN-CORES TEST (RSR02)	
5.2.4 ADDRESSING TEST (RSR03)	
5.2.5 BIT-ISOLATION TEST (RSR04)	
5.2.6 PROGRAM-END ROUTINE (RSPER)	
5.2.7 ERROR ROUTINE (RSEOR)	
5.3 DESCRIPTION OF LOW-CORE TEST	
5.3.1 INITIALIZATIONS (RSOKS)	
5.3.2 READ/WRITE-IN-MEMORY ADDRESSING TEST (RSAB1)	
5.3.3 BIT-ISOLATION TEST	
5.3.4 WORST-CASE-PATTERN TEST (RSACJ)	
5.3.5 COMMON-PROGRAM/PROGRAM-END ROUTINE (RSADA)	
5.3.6 ERROR ROUTINE TO SERVICE NON-INTERRUPT ERRORS (RSDDD)	
6. APPENDIX (NONE)	

LIST OF TABLES

TABLE	PAGE
1. PROGRAM OPTIONS	02

CORE STORAGE FUNCTION TEST

1. PURPOSE

THE CORE TEST TESTS THE CORES, CORE READ/WRITE CIRCUITRY, AND THE CORE-ADDRESSING CIRCUITRY OF THE 1131 CENTRAL PROCESSING UNIT (CPU). THE TEST CONSISTS OF THREE PARTS, WHICH ARE LOADED AND EXECUTED IN THE FOLLOWING ORDER,

- A. HIGH-CORE TEST. TESTS MEMORY LOCATIONS ABOVE 2048.
- B. 0-THROUGH-9-TEST, TESTS THE THREE HIGHEST LOCATIONS OF CORE IN ADDITION TO LOCATIONS 0-9 IN ORDER TO TEST THE WRAP-AROUND FEATURE OF CORE.
- C. LOW-CORE TEST. TESTS CORE LOCATIONS 9 THROUGH 2047.

2. PREREQUISITES

THE CORE TEST DECK MUST BE PRECEDED BY THE 1130 BASIC DIAGNOSTIC LOADER IN ORDER TO BE LOADED. EQUIPMENT REQUIRED CONSISTS OF THE 1442 CARD READ/PUNCH OR PAPER TAPE READER, AND 1131 CPU.

3. USE PROCEDURE

3.1 PROGRAM LOADING

- 1. PLACE CARDS/PAPER TAPE IN READER.
- 2. MAKE READER READY.
- 3. PRESS THE 1131 RESET KEY.
- 4. PRESS THE 1131 PROGRAM LOAD KEY.
- 5. IF PROGRAM FAILS TO LOAD OR STOPS AT A WAIT BELOW LOCATION 012C, REFER TO BASIC LOADER DOCUMENTATION SECT. 3.2.

3.2 OPERATION PROCEDURE

- A. HIGH CORE TEST WILL LOAD AND RUN FOR ABOUT 2 TO 10 MINUTES, DEPENDING ON CORE SIZE. IF NO ERRORS OCCUR, AND CONSOLE ENTRY SWITCHES 13, 14 AND 15 ARE OFF, THE NEXT TEST SECTION WILL BE AUTOMATICALLY LOADED.
- B. 0-9 CORE TEST WILL LOAD, AND RUN BRIEFLY. IF NO ERRORS OCCUR, AND CONSOLE ENTRY SWITCHES 13, 14 AND 15 ARE OFF, THE NEXT TEST SECTION WILL BE AUTOMATICALLY LOADED.
- C. LOW CORE TEST WILL LOAD AND RUN ABOUT 1 MINUTE, THEN STOP AT END OF TEST WAIT, 30FF, WITH 09CD IN INSTRUCTION ADDRESS REGISTER.
- D. ERRORS ARE INDICATED BY ERROR WAITS. SEE PARAGRAPH 3.5
- E. PROGRAM OPTIONS MAY BE ENTERED IN CONSOLE ENTRY SWITCHES AT ANY TIME; SEE TABLE 1.

CORE STORAGE FUNCTION TEST

TABLE 1. PROGRAM OPTIONS

DATA ENTRY SWITCHES	HIGH CORE	0-9 CORE	LOW CORE	
SW 15 ON	X	X		WAIT AT END OF TEST SECTION. TO RERUN SECTION PUSH PROG START.
SW 15 OFF	X	X		LOAD AND EXECUTE NEXT TEST SECTION.
SW 14 ON	X	X	X	LOOP TEST SECTION NOW RUNNING.
SW 13 ON	X	X	X	LOOP ROUTINE NOW RUNNING.
SW 12 ON	X	X	X	BYPASS ERROR WAIT.
SW 11 ON	X	X	X	LOOP ON A PARTICULAR ADDRESS. USED FOR SCOPING

3.3 PROGRAM TERMINATION

IN NORMAL OPERATION, THE PROGRAM WILL TERMINATE AFTER ALL THREE PARTS HAVE BEEN EXECUTED, UNLESS CONSOLE ENTRY SWITCH 13, OR 14 IS ON (LOOP ROUTINE, LOOP PROGRAM). TURN OFF SWITCH TO ALLOW PROGRAM TO TERMINATE.

3.4 NORMAL WAITS

IAR	ADDR	SBR	MEANING
0319	0318	3000	WAIT AT END OF TEST SECTION - SW 15 ON.
01FC	01FB	3060	
09CC	09CC	30FF	END OF PROGRAM WAIT - ALL SECTIONS COMPLETE.

3.5 ERROR WAITS

IAR	SBR	MEANING
0392	3000	ERROR IN HIGH-CORE TEST.
		A. THE ACCUMULATOR WILL DISPLAY THE SAME INFORMATION AS IT DID WHEN THE ERROR WAS DETECTED.
		B. THE ACCUMULATOR EXTENSION WILL DISPLAY THE CONTENTS OF THE INSTRUCTION ADDRESS REGISTER AT THE TIME THE ERROR WAS DETECTED.
		C. THE STATUS OF CARRY AND OVERFLOW WILL BE RESTORED.
		D. INDEX REGISTER XR1 WILL CONTAIN THE ADDRESS THAT FAILED UNDER TEST.
		E. INDEX REGISTER XR2 WILL CONTAIN THE CORRECT BIT PATTERN, IF THIS WAS AN ERROR-3 CONDITION.

021D 3XXX ERROR IN 0-9 TEST.

- A. THE ACCUMULATOR WILL DISPLAY THE SAME INFORMATION AS IT DID WHEN THE ERROR WAS DETECTED.
- B. THE ACCUMULATOR EXTENSION WILL DISPLAY THE ADDRESS OF THE BSI L RSCOR INSTRUCTION THAT TRANSFERRED THE PROGRAM TO THE ERROR ROUTINE.
- C. THE STATUS OF CARRY AND OVERFLOW HAVE NO SIGNIFICANCE
- D. THE 11 LEAST SIGNIFICANT BITS OF THE VALUE OF THE ADDRESS UNDER TEST WILL BE STORED IN THE 11 LEAST SIGNIFICANT BIT POSITIONS OF THE ERROR WAIT. THIS WILL BE DISPLAYED IN THE STORAGE BUFFER REGISTER.

CORE STORAGE FUNCTION TEST

0A46 3000 ERROR IN LOW-CORE TEST.

- A. THE ACCUMULATOR WILL DISPLAY THE SAME INFORMATION AS IT DID WHEN THE ERROR WAS DETECTED.
- B. THE ACCUMULATOR EXTENSION WILL DISPLAY THE CONTENTS OF THE INSTRUCTION ADDRESS REGISTER AT THE TIME THE ERROR WAS DETECTED.
- C. THE STATUS OF CARRY AND OVERFLOW WILL BE RESTORED.
- D. INDEX REGISTER XR1 WILL CONTAIN THE ADDRESS THAT FAILED UNDER TEST.
- E. INDEX REGISTER XR2 WILL CONTAIN THE CORRECT BIT PATTERN, IF THIS WAS AN ERROR-3 CONDITION.

IF PROGRAM FAILS TO LOAD, OR IF ERROR WAITS OCCUR AT LOCATIONS BELOW 012C, SEE BASIC LOADER DOCUMENTATION.

4. PRINTOUTS (NONE)

5. COMMENTS

5.1 DESCRIPTION OF HIGH-CORE MEMORY TEST

5.1.1 INITIALIZATIONS (RSOKS)

THE INITIALIZATION ROUTINE ESTABLISHES THE BOOTSTRAP BRANCH, DETERMINES MACHINE TYPE, DETERMINES MEMORY SIZE, AND ESTABLISHES AREA CODES.

5.1.2 READ/WRITE-IN-MEMORY AND ADDRESSING TEST (RSABI)

THE READ/WRITE-IN-MEMORY AND ADDRESSING TEST LOADS EACH CORE POSITION WITH ITS OWN ADDRESS. THE TEST THEN COMPARES THE CONTENTS OF EACH CORE POSITION WITH THE ADDRESS INTERROGATED TO ASSURE THAT THE CORES CAN BE CORRECTLY ADDRESSED.

5.1.3 BIT-ISOLATION TEST (RSABR)

THE BIT-ISOLATION TEST IS IN TWO PARTS. THE FIRST PART CHECKS THE ABILITY TO READ AND WRITE ZEROS IN MEMORY. A FAILURE TO READ OR WRITE ZEROS WILL RESULT IN AN ERROR WAIT. THE SECOND PART IS A BIT-ISOLATION TEST. THIS TEST DETERMINES THE ABILITY OF MEMORY TO DISTINGUISH EACH ONE OF THE 16 BITS IN A STORED WORD. THE PATTERN READ INTO MEMORY HAS FIFTEEN 0 BITS AND A SINGLE 1 BIT IN EACH WORD. FIRST THE 1 BIT IS PLACED IN POSITION 0. THE BIT IS THEN MOVED TO THE RIGHT ONE POSITION PER PASS FOR A TOTAL 15 TIMES UNTIL THE ENTIRE CORE WORD HAS BEEN TESTED.

5.1.4 WORST-CASE-PATTERN TEST (RSACJ)

THE WORST-CASE-PATTERN TEST ESTABLISHES A WORST-CASE PATTERN CONSISTING OF BLOCKS OF WORDS CONTAINING EITHER ALL ONES OR ALL ZEROS. THIS PATTERN IS READ AND STORED INTO MEMORY AND IS THEN COMPLEMENTED AND STORED AGAIN. IF ANY BITS ARE OMITTED OR ADDED, BECAUSE OF THIS WORST-CASE (MAXIMUM NOISE) EXERCISE, AN ERROR WILL OCCUR.

5.1.5 COMMON-PROGRAM/PROGRAM-END ROUTINE (RSADA)

THIS ROUTINE CONTAINS THE PROGRAM-PASS COUNTER AND THE INSTRUCTIONS NECESSARY TO SENSE CONSOLE ENTRY SWITCHES 14 AND 15. WITH SWITCH 15 ON, A WAIT-AT-RSQAS INSTRUCTION SIGNIFIES PROGRAM END.

CORE STORAGE FUNCTION TEST

5.1.6 ERROR ROUTINE TO SERVICE NON-INTERRUPT ERRORS (RSDDD)

THIS ROUTINE PROCESSES AND IDENTIFIES THE ERRORS THAT ARE DETECTED BY THE PROGRAM'S TEST ROUTINES. AN ERROR WAIT IS EXECUTED. SEE SECTION 3.5, ERROR WAITS.

5.1.7 PROPER CONDITION OF SWITCHES

WITH CONSOLE ENTRY SWITCH 12 OFF (NORMAL), EACH ROUTINE IS EXECUTED FOUR TIMES PER EACH PROGRAM PASS, AND THE PROGRAM IS REPEATED THREE TIMES. THIS RESULTS IN A RUN TIME OF BETWEEN 1 AND 10 MINUTES DEPENDING ON MEMORY SPEED AND CORE SIZE.

5.2 DESCRIPTION OF MEMORY TEST (0 THROUGH 9 CORES)

5.2.1 INITIALIZATIONS (RSSTA)

THE INITIALIZATIONS DETERMINE THE MACHINE TYPE, ESTABLISH THE MEMORY SIZE, AND ESTABLISH PROPER IOCC AREA-CODE MODIFIERS.

5.2.2 LOAD-ZEROS-IN-CORES TEST (RSR01)

THIS TEST TESTS THE ABILITY OF THE MEMORY TO READ AND WRITE ALL ZEROS.

5.2.3 LOAD-ONES-IN-CORES TEST (RSR02)

THIS TEST TESTS THE ABILITY OF THE MEMORY TO READ AND WRITE ALL ONES.

5.2.4 ADDRESSING TEST (RSR03)

THIS TEST ATTEMPTS TO PLACE WITHIN EACH MEMORY WORD ITS OWN ADDRESS. THE MEMORY IS THEN READ TO ASSURE THAT PROPER ADDRESSING HAS TAKEN PLACE.

5.2.5 BIT-ISOLATION TEST (RSR04)

THIS TEST CHECKS BIT ISOLATION BY RIPPLING A 1 BIT THROUGH EACH BIT POSITION WITHIN THE MEMORY WORD. AT ANY TIME DURING THIS ROUTINE, THE WORD UNDER TEST SHOULD CONTAIN NO MORE THAN ONE 1 BIT IN ANY WORD.

5.2.6 PROGRAM-END ROUTINE (RSPER)

THIS ROUTINE INCREMENTS THE PROGRAM PASS COUNTER AND INTERROGATES CONSOLE ENTRY SWITCHES 14 AND 15.

5.2.7 ERROR ROUTINE (RSEOR)

THE ERROR ROUTINE IS USED WHENEVER AN ERROR OCCURS. THE ERROR ROUTINE EXECUTES A WAIT-AT-RSERW INSTRUCTION.

NOTE

THIS PART OF THE TEST DOES NOT HAVE THE BOOTSTRAP-BRANCH FEATURE. THE EXECUTION TIME FOR THIS PART OF THE TEST WILL BE LESS THAN 10 SECONDS IF NO ERRORS ARE DETECTED.

5.3 DESCRIPTION OF LOW-CORE MEMORY TEST

5.3.1 INITIALIZATIONS (RSOKS)

THE INITIALIZATIONS DETERMINE MACHINE TYPE AND ESTABLISH AREA CODES.

CORE STORAGE FUNCTION TEST

5.3.2 READ/WRITE-IN-MEMORY ADDRESSING TEST (RSABI)

THIS TEST LOADS EACH CORE POSITION WITH ITS OWN ADDRESS AND COMPARES THE CONTENTS OF EACH CORE POSITION WITH THE ADDRESS INTERROGATED TO ASSURE THAT THE CORES CAN BE CORRECTLY ADDRESSED.

5.3.3 BIT-ISOLATION TEST

THIS TEST DETERMINES THE ABILITY OF MEMORY TO DISTINGUISH EACH ONE OF THE 16 BITS IN A STORED WORD. FIRST THE 1 BIT IS PLACED IN POSITION ZERO. THEN, THE BIT MOVED TO THE RIGHT ONE POSITION PER PASS FOR A TOTAL 15 PASSES UNTIL THE ENTIRE CORE WORD HAS BEEN TESTED.

5.3.4 WORST-CASE-PATTERN TEST (RSACJ)

THE WORST-CASE-PATTERN TEST ESTABLISHES A WORST-CASE PATTERN CONSISTING OF BLOCKS OF WORDS CONTAINING EITHER ALL ONES OR ALL ZEROS. THIS PATTERN IS READ AND STORED INTO MEMORY AND IS THEN COMPLEMENTED AND STORED AGAIN. IF ANY BITS ARE DROPPED OR ADDED DURING THIS WORST-CASE (MAXIMUM NOISE) EXERCISE, AN ERROR WAIT WILL OCCUR.

5.3.5 COMMON-PROGRAM/PROGRAM-END ROUTINE (RSADA)

THIS ROUTINE CONTAINS THE PROGRAM-PASS COUNTER AND INTERROGATES CONSOLE ENTRY SWITCH 14. A WAIT-AT-RSEXI INSTRUCTION SIGNIFIES PROGRAM END.

5.3.6 ERROR ROUTINE TO SERVICE NON-INTERRUPT ERRORS (RSDDD)

THIS ROUTINE PROCESSES AND IDENTIFIES THE ERRORS THAT ARE DETECTED BY THE PROGRAM'S TESTS. AN ERROR WAIT INSTRUCTION IS EXECUTED.

NOTE

AFTER THIS PART OF THE TEST HAS COMPLETED ITS INITIALIZATION ON THE FIRST PASS, A BOOTSTRAP BRANCH IS AVAILABLE FOR RESTARTING THE PROGRAM. THIS BOOTSTRAP BRANCH IS INITIATED BY DEPRESSING THE STOP, RESET, AND START PUSHBUTTONS AND WILL RESULT IN A BRANCH TO THE START OF THE PROGRAM. EACH ROUTINE IS EXECUTED FOUR TIMES FOR EACH PROGRAM PASS AND THE PROGRAM IS REPEATED THREE TIMES. THIS RESULTS IN A RUN TIME OF BETWEEN ONE AND TWO MINUTES DEPENDING ON MEMORY SPEED. THE PROGRAM DESTROYS THE 1130 BASIC DIAGNOSTIC LOADER, MAKING IT IMPOSSIBLE TO CHAIN TO ANOTHER PROGRAM.

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

```

*
*
*
* MEMORY TEST-HIGH CORE
*
      ABS
02BC   ORG      300
012C 0 C839   RSDKR LDD  RSAAN
0127 00 DC000000 STD  L  0
012F 0 C834   RSDKS LDD  RSAAM
0130 00 DC000004 STD  L  4
0132 0 C015   LD      RSAAE      CLEAR Q REGISTER
0133 0 1890   SRT      16
0134 0 C018   LD      RSFAC      INITIALIZE MEM SIZE
0135 0 D013   STO      RSAAH

* MACHINE DETERMINATION ROUTINE
*
0136 0 C011   LD      RSAAE
0137 00 D4000003 STO  L  3
0139 00 6700FFFF LDX  L3 /FFFF
0138 00 C4000003 LD   L  3
013D 00 4C200141 BSC  L  RSAAB,Z
013F 0 C007   LD      RSAAD
0140 0 7001   MDX  X  1
0141 0 C004   RSAAB LD   RSAAC
0142 0 D007   STO      RSAAK
0143 00 67000000 LDX  L3 /0000      CLEAR XR 3
0145 0 7008   MDX      RSAAF

* STORAGE AREAS FOR INITIALIZATIONS
*
0146 0 0001   RSAAC DC   1      1130 CONSTANT
0147 0 FFFE   RSAAD DC  -2     1800 CONSTANT
0148 0 0000   RSAAE DC   0     CONSTANT ZERO
0149 0 0800   RSAAH DC  /0800  MEMORY SIZE
014A 0 0000   RSAAK DC   0     MACHINE TYPE
014B 0 0003   RSFAA DC   3     NUMBER OF PROGRAM PASSES
014C 0 0000   RSFAB DC   0     PROGRAM PASS BUFFER
014D 0 0800   RSFAC DC  /0800  INITIALIZE MEM SIZE

* MEMORY SIZE ROUTINE
*
014E 0 C0F9   RSAAF LD   RSAAE
014F 00 D4000000 STO  L  0
0151 0 C0F7   LD      RSAAH
0152 0 D001   RSAAJ STO  RSAAG+1
0153 00 D4000149 RSAAG STO  L  RSAAH
0155 00 C4000000 LD   L  0
0157 00 4C18015C BSC  L  RSAAI,+
0159 0 90EC   S      RSAAC
015A 0 D0EE   STO      RSAAH
015B 0 7015   MDX      RSABA
015C 0 C0EC   RSAAI LD  RSAAH
015D 0 1001   SLA      1
015E 0 D0EA   STO      RSAAH
015F 0 70F2   MDX      RSAAJ

* STORAGE AREAS PART 1
*
0160 0 7003   RSAAL MDX X  3
0162 0 0002   BSS  E  2
0164 00 4C00012F RSAAM BSC L  RSDKS      BOOTSTRAP BRANCH INST
0166 00 4C00012F RSAAN BSC L  RSDKS
0168 0 016E   RSQAF DC   RSQAL      READ BIT SWITCH IOCC
0169 0 3A40   RSQAO DC  /3A40      SECOND HALF IOCC-113

```

```

HCT00000
HCT00010
HCT00020
HCT00030
HCT00040
HCT00050
HCT00060
HCT00070
HCT00080
HCT00090
HCT00100
HCT00110
HCT00120
HCT00130
HCT00140
HCT00150
HCT00160
HCT00170
HCT00180
HCT00190
HCT00200
HCT00210
HCT00220
HCT00230
HCT00240
HCT00250
HCT00260
HCT00270
HCT00280
HCT00290
HCT00300
HCT00310
HCT00320
HCT00330
HCT00340
HCT00350
HCT00360
HCT00370
HCT00380
HCT00390
HCT00400
HCT00410
HCT00420
HCT00430
HCT00440
HCT00450
HCT00460
HCT00470
HCT00480
HCT00490
HCT00500
HCT00510
HCT00520
HCT00530
HCT00540
HCT00550
HCT00560
HCT00570
HCT00580
HCT00590
HCT00600
HCT00610
HCT00620
HCT00630
HCT00640
HCT00650
HCT00660
HCT00670

```

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

```

016A 0 0480   RSQAC DC   RSEND+2      FND OF PROGRAM IN CORE
016B 0 031D   RSQAD DC   RSCCA      INTERRUPT LEVEL ZERO VECT
016C 0 0000   RSQAE DC   0          WORK AREA
016D 0 0240   RSQAP DC  /0240      SECOND HALF IOCC-180
016E 0 0000   RSQAL DC   0          BIT SWITCH BUFFER AREA
016F 0 0F03   RSQAU DC  /0F03      2ND HALF IOCC-1800 D W
0170 0 0902   RSQAV DC  /0902      2ND HALF-1800 TYPE

* INITIALIZE MASKS AND INTERRUPTS TO LEVEL ZERO
* 1800 ONLY
*
RSABA LD   RSAAL      STORE BOOTSTRAP BRAN H AT
      STO  L  0          LOCATION ZERO
      LD   RSAAK
      BSC  L  RSABI,E   IF 1130-GO TO FIRST ROUTI
      LD   RSQAP        CHANGE SECCND HALF I CC
      STO  RSQAD        FOR 1800 READ BIT SW
      LD   RSQAD        INTERRUPT LEVEL ERRO VECT
      STO  L  8
      LD   RSQAU        DSW 1800
      STO  L  TWSNS+1   PRO1
      LD   RSQAV        XIO WRITE 1800
      STO  L  TWWRT+1   PRO2

* FIRST ROUTINE-READ + WRITE IN MEMORY
*
RSABI LD   RSFAA      INITIALIZE PROGRAM
      STO  RSFAB        PASS COUNTER
RSABH LDX  X2  4        ADDRESSING PASSES
RSABB LDX  I1  RSQAC
RSABC STX  I  RSQAE
      LD   RSQAE
      STO  I  RSQAE
      EOR  RSAAH
      BSC  L  RSABD,+
      MDX  X1  1        INCR TO NEXT ADDRESS
      MDX
RSABD LDX  I1  RSQAC
RSABE STX  I  RSQAE
      LD   I  RSQAE
      EOR  RSQAE
      BSC  L  RSABF,+
      STO  L  RSQAN     ERROR 1 DETECTED
      XIO  L  RSQAF     STORE ACCUM FOR ERROR ROU
      LD   L  RSQAL
      AND  L  RSRAI
      BSC  L  RSABE,Z
      BSI  L  RSDDD
      DC   /FFFE
      RSABF XIO  RSQAF     ERROR 1 CONSTANT
      LD   L  RSQAL     READ BIT SWITCHES
      AND  L  RSRAI
      BSC  L  RSABE,Z   ISOLATE BIT SW 11
      LD   RSQAE        IF BIT SW 11 ON-REPEAT AD
      EOR  RSAAH
      BSC  L  RSABG,+
      MDX  X1  1        INCR TO NEXT ADDRESS
      MDX
RSABG MDX  X2  -1      COUNT PASSES
      MDX
      XIO  L  RSQAF     REPEAT ROUTINE IF SW13 ON
      LD   L  RSQAL
      AND  L  RSRAG
      BSC  L  RSABH,Z   REPEAT ADDRESSING RO TINE

* SECOND ROUTINE
* BIT ISOLATION TEST-BIT BY BIT-ADRESS BY ADDRESS
*

```

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

```

01BC 0 6304      RSABR LDX X3 4      BIT ISOLATION PASSES      HCT01360
01BD 00 C400016A RSABP LD L RSQAC      HCT01370
01BF 0 005A      RSABN STO RSQAH      HCT01380
01C0 00 6580021A LDX I1 RSQAF      HCT01390
01C2 0 C058      LD RSQAI      HCT01400
01C3 00 0480021A STO I RSQAH      HCT01410
01C5 00 C480021A LD I RSQAH      HCT01420
01C7 00 4C180106 BSC L RSARJ,+-- ERROR 2 DETECTED      HCT01430
01C9 00 4400037F BSI L RSDDD      HCT01440
01CB 0 FFFD      DC /FFFD      ERROR 2 CONSTANT      HCT01441
01CC 00 0400021F STO L RSQAN      STORE ACC FOR ERROR OUTI      HCT01450
01CF 00 0C000168 XIO L RSQAF      HCT01460
01D0 00 C400016E LD L RSQAL      HCT01470
01D2 00 F400028C AND L RSRAI      HCT01480
01D4 00 4C2001C0 BSC L RSARN+1,Z      HCT01490
01D6 00 0C000168 RSABJ XIO L RSQAF      IF BIT SW 11 ON REPE T AD      HCT01510
01D8 00 C400016E LD L RSQAL      HCT01520
01DA 00 E400028C AND L RSRAI      HCT01530
01DC 00 4C2001C0 BSC L RSARN+1,Z      HCT01540
01DE 0 C03D      LD RSQAJ      HCT01550
01DF 0 003D      STO RSQAK      HCT01560
01E0 0 C03C      RSABL LD RSQAK      HCT01570
01E1 00 0480021A RSABQ STO I RSQAH      HCT01580
01E3 00 6580021D LDX I2 RSQAK      HCT01590
01E5 00 C480021A LD I RSQAH      HCT01600
01E7 0 F035      ENR RSQAK      HCT01610
01E8 00 4C1801F7 BSC L RSABK,+-- ERROR 3 DETECTED      HCT01620
01EA 00 0400021F STO L RSQAN      HCT01630
01EC 00 0C000168 XIO L RSQAF      HCT01640
01EE 00 C400016E LD L RSQAL      HCT01650
01F0 00 E400028C AND L RSRAI      HCT01660
01F2 00 4C2001E0 BSC L RSABL,Z      HCT01670
01F4 00 4400037F BSI L RSDDD      HCT01680
01F6 0 FFFB      DC /FFFB      ERROR 3 CONSTANT      HCT01690
01F7 00 0C000168 RSABK XIO L RSQAF      HCT01700
01F9 00 C400016E LD L RSQAL      HCT01710
01FA 00 E400028C AND L RSRAI      ISOLATE BIT 11      HCT01720
01FD 00 4C2001E0 BSC L RSABL,Z      IF BIT SW 11 ON-REPE T BI      HCT01730
01FF 0 C01D      LD RSQAK      HCT01740
0200 0 4804      BSC E      IF ODD-BIT 15 IS REA HED      HCT01750
0201 0 7003      MDX RSABM      BRANCH TO INCRE ADR ROUTI      HCT01760
0202 0 1801      SRA I      INCREMENT BIT      HCT01770
0203 0 0019      STO RSQAK      POSITION BY ONE      HCT01780
0204 0 70DC      MDX RSABQ      HCT01790
0205 0 C014      RSABM LD RSQAH      TEST FOR MEMORY END      HCT01800
0206 00 F4000149 EDR L RSAAH      HCT01810
0208 00 4C18020D BSC L RSABO,+--      HCT01820
020A 0 C00F      LD RSQAH      INCREMENT TO TEST NE T      HCT01830
020B 0 9012      A RSQAM      MEMORY LOCATION      HCT01840
020C 0 70B2      MDX RSAAN      HCT01850
020D 0 73FF      RSABO MDX X3 -1      COUNT PASSES      HCT01860
020E 0 70AE      MDX RSABP      HCT01870
020F 00 0C000168 XIO L RSQAF      HCT01880
0211 00 C400016E LD L RSQAL      HCT01890
0213 00 E400028A AND L RSRAG      HCT01900
0215 00 4C2001BC BSC L RSABR,Z      REPEAT BIT ISOLATION      HCT01910
0217 0 7008      MDX RSACJ      HCT01920
HCT01930
HCT01940
HCT01950
HCT01960
HCT01970
HCT01980
HCT01990
HCT02000
HCT02010
HCT02020
HCT02030

```

* STORAGE AREAS PART 2

```

0218 0 0004      RSQAQ DC 4      WORST CASE PASSES
0219 0 0000      RSQAR DC 0      WORST CASE PASS COUN
021A 0 0000      RSQAH DC 0      WORK AREA-ADR
021B 0 0000      PSQAI DC 0      CONST ZERO
021C 0 8000      RSQAJ DC /8000    BIT ZERO CONSTANT
021D 0 0000      RSQAK DC 0      WORK AREA-BIT
021E 0 0001      RSQAM DC 1      CONST 1
021F 0 0000      RSQAN DC 0      STORAGE FOR ACCUM

```

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

```

0220 00 66000000 RSACJ LDX L2 /0000      HCT02040
0222 00 6700FFFF LDX L3 /FFFF      HCT02050
0224 0 C0F3      LD RSQAF      INITIALIZE WORST CAS      HCT02060
0225 0 00F3      STO RSQAR      PASS COUNTER      HCT02070
0226 00 74FF0219 RSACK MDX L RSQAR,-1      COUNT WORST CASE PAS ES      HCT02080
0228 0 7001      MDX RSACK      HCT02090
0229 0 7053      MDX RSACW      HCT02100
022A 0 6AEF      RSACX STX 2 RSQAH      COMPLEMENT XR2      HCT02110
022B 0 C0EE      LD RSQAH      HCT02120
022C 00 F4000287 EDR L RSRAC      HCT02130
022E 0 D0EB      STO RSQAH      HCT02140
022F 00 6580021A LDX I2 RSQAH      HCT02150
0231 0 68E8      STX 3 RSQAH      COMPLEMENT XR3      HCT02160
0232 0 C0E7      LD RSQAH      HCT02170
0233 00 F4000287 EDR L RSRAC      HCT02180
0235 0 D0E4      STO RSQAH      HCT02190
0236 00 6780021A LDX I3 RSQAH      HCT02200
0238 00 C400016A LD L RSQAC      HCT02210
023A 0 D04A      STO RSRAA      HCT02220
023B 0 C049      RSACB LD RSRAA      HCT02230
023C 0 1806      SRA 6      HCT02240
023D 0 D048      STO RSRAB      HCT02250
023E 0 1802      SRA 2      HCT02260
023F 0 8046      A RSRAB      HCT02270
0240 00 4C040245 BSC L RSACA,E      HCT02280
0242 00 6E800285 STX I2 RSRAA      HCT02290
0244 0 7002      MDX RSACD      HCT02300
0245 00 6F800285 RSACA STX I3 RSRAA      HCT02310
0247 0 C03D      RSACD LD RSRAA      HCT02320
0248 00 F4000149 EDR L RSAAH      TEST FOR MEMORY END      HCT02330
024A 00 4C18024F BSC L RSADB,+--      HCT02340
024C 00 74010285 MDX L RSRAA,1      ADR=ADR+1      HCT02350
024E 0 70EC      MDX RSACB      HCT02360
HCT02370
HCT02380
HCT02390
HCT02400
HCT02410
HCT02420
HCT02430
HCT02440
HCT02450
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HCT02600
HCT02610
HCT02620
HCT02630
HCT02640
HCT02650
HCT02660
HCT02670
HCT02680
HCT02690
HCT02700
HCT02710

```

* ESTABLISH WORST CASE PATTERN

```

*
RSACJ LDX L2 /0000
LDX L3 /FFFF
LD RSQAF
STO RSQAR
RSACK MDX L RSQAR,-1
MDX RSACK
MDX RSACW
RSACX STX 2 RSQAH
LD RSQAH
EDR L RSRAC
STO RSQAH
LDX I2 RSQAH
STX 3 RSQAH
LD RSQAH
EDR L RSRAC
STO RSQAH
LDX I3 RSQAH
LD L RSQAC
STO RSRAA
LD RSRAA
SRA 6
STO RSRAB
SRA 2
A RSRAB
BSC L RSACA,E
STX I2 RSRAA
MDX RSACD
RSACA STX I3 RSRAA
RSACD LD RSRAA
EDR L RSAAH
BSC L RSADB,+--
MDX L RSRAA,1
MDX RSACB

```

COMPLEMENT XR2

COMPLEMENT XR3

TEST FOR MEMORY END

ADR=ADR+1

* WORST CASE TEST LOAD AND STORE THEN

* COMPLEMENT AND REPEAT

```

*
RSADB LDX I1 RSQAC      LOAD STARTING ADR IN XR1
RSACL STX 1 RSRAA      HCT02440
RSACH LD RSRAJ      INITIALIZE COMPLEMENT CNTR      HCT02450
STO RSRAK      HCT02460
RSACG LD I RSRAA      HCT02470
BSC L RSACE,Z      HCT02480
FOR RSRAC      HCT02490
MDX RSACF      HCT02500
RSACE EDR RSRAC      HCT02510
BSC L RSACF,+--      ERROR 4 DETECTED      HCT02520
STO L RSQAN      HCT02530
XIO L RSQAF      HCT02540
LD L RSQAL      HCT02550
AND L RSRAI      HCT02560
BSC L RSACH,Z      HCT02570
BSI L RSDDD      HCT02580
DC /FFFF      ERROR 4 CONSTANT      HCT02590
STO I RSRAA      HCT02600
MDX L RSRAK,-2      HCT02610
MDX RSACG      BRANCH FOR COMPLEMEM PAS      HCT02620
XIO L RSQAF      HCT02630
LD L RSQAL      HCT02640
AND RSRAI      ISOLATE BIT SW 11      HCT02650
BSC L RSACH,Z      IF BIT SW 11 ON-REPE T AD      HCT02660
LD RSRAA      HCT02670
EDR L RSAAH      TEST FOR MEMORY END      HCT02680
BSC L RSACK,+--      HCT02690
MDX X1 1      MEM ADR=ADR+1      HCT02700

```

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

```

027C 0 70D4 MDX RSACL HCT02720
027D 00 0C000168 RSACW XIO L RSQAF HCT02730
027F 00 C400016E LD L RSQAL HCT02740
0281 0 E008 AND RSRAG LOOP ROUTINE IF SW 1 ON HCT02750
0282 00 4C200220 BSC L RSACJ,Z HCT02760
0284 0 700B MDX RSACV HCT02770
*
* STORAGE AREAS PART 3
*
0285 0 0000 RSRAA DC 0 WORK AREA-ADDRESS HCT02810
0286 0 0000 RSRAB DC 0 BUFFER AREA-WORST CASE PA HCT02820
0287 0 FFFF RSRAC DC /FFFF HCT02830
0288 0 0000 RSRAD DC 0 WORK AREA-ADDRESS HCT02840
0289 0 0000 RSRAF DC 0 CONST ZERO HCT02850
028A 0 0004 RSRAG DC /0004 BIT 13 ISOLATION CONST HCT02860
028B 0 0002 RSRAH DC /0002 BIT 14 ISOLATION CONST HCT02870
028C 0 0010 RSRAL DC /0010 BIT 11 ISOLATION CONST HCT02880
028D 0 0020 RSRAX DC /0020 BIT 10 ISOLATION CONST HCT02890
028E 0 0003 RSRAY DC 3 HCT02900
028F 0 0000 RSRAC DC 0 COMPLEMENT PASS COUN ER HCT02910
*
* STORAGE PROTECTION TEST ROUTINES
*
0290 00 C400014A RSACV LD L RSAAK HCT02920
0292 00 4C080296 BSC L RSACU,+ HCT02930
0294 00 64000305 LDX L RSADA NOT 1800 BRANCH TO E D HCT02940
*
* WRITE ZEROS ON PROTECTED AREA OF ONES
*
0296 0 6204 RSACV LDX X2 4 STORAGE PROTECT PASS S HCT02950
0297 00 C400016A RSACS LD L RSQAC HCT02960
0299 0 D0EE STO RSRAE HCT02970
029A 0 0008 STG RSACO INITIALIZE STS ADDRESS HCT02980
029B 00 C4000373 LD L RSSAH TELL INTERRUPT ROUTI E TO HCT02990
029D 00 04000371 STO L RSSAF DISREGARD SP ERROR HCT03000
029F 0 C0E7 RSACN LD RSRAC ACC=/FFFF HCT03010
02A0 00 04800288 STO I RSRAE HCT03020
02A2 0 2C41 DC /2C41 ADD SP BITS HCT03030
02A3 0 0480 RSACO DC RSEND+2 HCT03040
02A4 00 65800288 LDX I1 RSRAE HCT03050
02A6 0 C0E2 LD RSRAF ACCUM=0 HCT03060
02A7 00 04800288 STO I RSRAE STO SHOULD NOT OCCUR HCT03070
02A9 00 C4800288 LD I RSRAE HCT03080
02AB 0 F0DB EOR RSRAC HCT03090
02AC 00 4C180288 BSC L RSACM,+ ERROR 5 DETECTED HCT03100
02AE 00 0400021F STO L RSQAN HCT03110
02B0 00 0C000168 XIO L RSQAF HCT03120
02B2 00 C400016E LD L RSQAL HCT03130
02B4 00 E400028C AND L RSRAL HCT03140
02B6 00 4C20029F BSC L RSACN,Z HCT03150
02B8 00 4400037E BSI L RSDDD HCT03160
02BA 0 FFEF DC /FFEF ERROR 5 CONSTANT HCT03170
02BB 00 0C000168 RSACM XIO L RSQAF HCT03180
02BD 00 C400016E LD L RSQAL HCT03190
02BF 0 E0CC AND RSRAL HCT03200
02C0 00 4C20029F BSC L RSACN,Z IF BIT SW 11 ON-REPE T AD HCT03210
02C2 0 C0C5 LD RSRAE HCT03220
02C3 00 84C0021E A L RSQAM HCT03230
02C5 0 D0C2 STO RSRAE HCT03240
02C6 0 D0DC STO RSRAC HCT03250
02C7 00 F4000149 EOR L RSAAH HCT03260
02C9 00 4C20029F BSC L RSACN,Z RETURN WITH ADR=ADR+ HCT03270
*
* UNPROTECT AND CLEAR MEMORY OF ONES
*
02CB 00 C4000372 LD L RSSAG SERVICE STORAGE PROT CT HCT03280
02CD 00 04000371 STO L RSSAF HCT03290
02CF 00 C400016A LD L RSQAC HCT03300

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CORE STORAGE FUNCTION TEST
HIGH CORE TEST

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02D1 0 00B6 STO RSRAE HCT03400
02D2 0 0001 STO RSRAC INITIALIZE STS ADDRESS HCT03410
02D3 0 2C40 RSACQ DC /2C40 CLEAR SP BITS HCT03420
02D4 0 0480 RSACR DC RSEND+2 HCT03430
02D5 00 65800288 LDX I1 RSRAE HCT03440
02D7 0 C0B1 LD RSRAF ACC=/0000 HCT03450
02D8 00 04800288 STO I RSRAE HCT03460
02DA 00 C4800288 LD I RSRAE HCT03470
02DC 00 4C1802EB BSC L RSACM,+ ERROR 6 DETECTED HCT03480
02DE 00 0400021F STO L RSQAN HCT03490
02E0 00 0C000168 XIO L RSQAF HCT03500
02E2 00 C400016E LD L RSQAL HCT03510
02E4 00 E400028C AND L RSRAL HCT03520
02E6 00 4C2002D3 BSC L RSACQ,Z HCT03530
02E8 00 4400037E BSI L RSDDD HCT03540
02EA 0 FFD FDC /FFDF ERROR 6 CONSTANT HCT03550
02EB 00 0C000168 RSACP XIO L RSQAF REPEAT LOOP IF SW 11 ON HCT03560
02ED 00 C400016E LD L RSQAL HCT03570
02EF 0 E09C AND RSRAL HCT03580
02F0 00 4C2002D3 BSC L RSACQ,Z REPEAT ADDRESS HCT03590
02F2 0 C095 LD RSRAE HCT03600
02F3 00 8400021E A L RSQAM HCT03610
02F5 0 0092 STO RSRAE HCT03620
02F6 0 00DD STO RSRAC HCT03630
02F7 00 F4000149 EOR L RSAAH HCT03640
02F9 00 4C2002D3 BSC L RSACQ,Z BRANCH WITH ADR=ADR+ HCT03650
02FB 0 72FF MDX X2 -1 HCT03660
02FC 0 709A MDX RSACS LOOP ROUTINE FOR 5 P SSES HCT03670
02FD 00 0C000168 XIO L RSQAF LOOP ROUTINE IF SW 13 ON HCT03680
02FF 00 C400016E LD L RSQAL HCT03690
0301 00 E400028A AND L RSRAG HCT03700
0303 00 4C200296 BSC L RSACU,Z REPEAT SP ROUTINE HCT03710
*
* COMMON PROGRAM END
*
0305 00 74FF014C RSADA MDX L RSFAB,-1 HCT03720
0307 0 7013 MDX RSCCQ HCT03730
0308 00 0C000168 XIO L RSQAF HCT03740
030A 00 C400016E LD L RSQAL HCT03750
030C 00 E4000288 AND L RSRAL HCT03760
030E 00 4C200182 BSC L RSABH,Z REPEAT PROG-SW 14 ON HCT03770
0310 00 0C000168 RSEXI XIO L RSQAF HCT03780
0312 00 C400016E LD L RSQAL HCT03790
0314 00 4C040318 BSC L RSQAS,E INTERROGATE SW 15 HCT03800
0316 00 64000050 RSQAW LDX L /0050 LINK TO NEXT PROG HCT03810
0318 0 3000 RSQAS WAIT PROGRAM END-PRESS START HCT03820
0319 00 6400012F LDX L RSDKS TO RE-RUN PROGRAM HCT03830
031B 00 64000184 RSCCQ LDX L RSABH LOOP PROGRAM HCT03840
*
* INTERRUPT LEVEL ERROR ROUTINE
*
031D 0 0000 RSCCA DC 0 RETURN ADDR TO MAIN LINE HCT03850
031E 0 004C STO RSSAA SAVE A HCT03860
031F 0 2847 STS RSCCE STORE STATUS CARY+OFLO HCT03870
0320 0 084D XIO RSSAC SENSE ILSW FOR LEVEL ERROR HCT03880
0321 0 004E STO RSSAD HCT03890
0322 00 4C400324 BOSC L NEXT HCT03900
0324 00 0C000168 NEXT XIO L RSQAF TEST FOR THE ILLEGAL HCT03910
0326 00 C400016E LD L RSQAL SWITCH COMBINATION-S 10 HCT03920
0328 0 F052 AND RSSAD ON AND SW 12 OFF HCT03930
0329 0 F052 EOR RSSAP HCT03940
032A 00 4C180394 BSC L RSDDK,+ BRANCH IF ILLEGAL HCT03950
032C 0 C043 LD RSSAD RESTORE STATUS OF IL W HCT03960
032D 0 E046 AND RSSAE ISOLATE STGE PRT ERROR HCT03970
032E 00 4C180343 BSC L RSCCB,+ TEST FOR STORAGE PRO VIOL HCT03980
0330 0 C040 LD RSSAF HCT03990
0331 00 4C10033F BSC L RSCCG,- BYPASS PRINTOUT IF I SP HCT04000
0333 00 0C000168 XIO L RSQAF SW 10 TO BYPASS PRINTOUT HCT04010

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CORE STORAGE FUNCTION TEST
HIGH CORE TEST

0335 00 C400016E LD L RSQAL HCT04080
0337 00 E400028D AND L RSRAX HCT04090
0339 00 4C200359 BSC L RSCCD,Z BYPASS PRINTOUT IF B ANCH HCT04100
0338 00 44000397 BSI L LOG HCT04110
0330 0 0473 DC MES03 ERROR INT-STORG PROT HCT04120
033E 0 7004 MDX RSCCB HCT04130
033F 0 C030 RSCCG LD RSSAD IF IN SP ROUTINE AN P HCT04140
0340 0 F033 EOR RSSAE ERROR ONLY THEN RETURN TO HCT04150
0341 00 4C98031D BSC I RSCCA,+ MAINLINE HCT04160
0343 00 0C000168 RSCCB XIO L RSQAF SW 10 TO BYPASS PRINTOUT HCT04170
0345 00 C400016E LD L RSQAL HCT04180
0347 00 E400028D AND L RSRAX HCT04190
0349 00 4C200359 BSC L RSCCD,Z BYPASS PRINTOUT IF B ANCH HCT04200
0348 0 C024 LD RSSAD LOAD ILSW FOR ERROR INTRUP HCT04210
034C 0 E028 AND RSSAI ISOLATE PARITY ERROR HCT04220
034D 00 4C180352 BSC L RSCCC,+ HCT04230
034F 00 44000397 BSI L LOG HCT04240
0351 0 047F DC MES04 ERROR INT-PARITY HCT04250
0352 0 C01D RSCCC LD RSSAD TEST FOR INVALID OP ODE HCT04260
0353 0 E022 AND RSSAJ ISOLATE INV OP ERROR HCT04270
0354 00 4C180359 BSC L RSCCD,+ HCT04280
0356 00 44000397 BSI L LOG HCT04290
0358 0 0489 DC MES05 ERROR INT-INV OP COD HCT04300
0359 00 0C000168 RSCCD XIO L RSQAF IF BIT SW 12 ON THEN STOR HCT04310
0358 00 C400016E LD L RSQAL HCT04320
0350 0 E019 AND RSSAK ACCUM, INS CTR, STATUS HCT04330
035E 00 4C88031D BSC I RSCCA,+ AND WAIT HCT04340
0360 0 C00F LD RSSAD LOAD ILSW FOR ERROR HCT04350
0361 0 180C SRA 12 PLACE BITS 0-4 OF IL W IN HCT04360
0362 0 E817 OR RSSAN 11-15 AND OR IN WAIT OP HCT04370
0363 0 0004 STO RSCCH STORE IN WAIT HCT04380
0364 0 C088 LD RSCCA LOAD INS CTR IN ACCUM HCT04390
0365 0 1890 SRT 16 TRANSFER INS CTR TO HCT04400
0366 0 C004 LD RSSAA RESTORE ACCUM CONTENTS HCT04410
0367 0 2000 RSCCE LDS 0 RESTORE DFLO+CARRY 1 DICA HCT04420
0368 0 3000 RSCCH WAIT HCT04430
0369 00 4C80031D BSC I RSCCA RETURN TO MAINLINE HCT04440
* HCT04450
* STORAGE AREAS FOR ERROR ROUTINES HCT04460
* HCT04470
0368 0 0000 RSSAA DC 0 SAVED ACCUMULATOR BU FER HCT04480
036C 0002 BSS E 2 HCT04490
036E 0 0000 RSSAC DC /0000 SENSE ILSW FOR HCT04500
036F 0 0300 DC /0300 LEVEL ZERO HCT04510
0370 0 0000 RSSAD DC 0 STORAGE FOR ILSW HCT04520
0371 0 FFFF RSSAF DC -1 IN SP ROUTINE -IND, 2YES HCT04530
0372 0 FFFF RSSAG DC -1 NOT IN SP ROUTINE HCT04540
0373 0 0002 RSSAH DC 2 IN STORAGE PROTECT ROUTIN HCT04550
0374 0 2000 RSSAE DC /2000 HCT04560
0375 0 4000 RSSAI DC /4000 HCT04570
0376 0 8000 RSSAJ DC /8000 HCT04580
0377 0 0008 RSSAK DC /0008 ISOLATE BIT SW 12 HCT04590
0378 0 000E RSSAL DC 14 HCT04600
0379 0 0001 RSSAM DC 1 HCT04610
037A 0 3000 RSSAN DC /3000 WAIT INSTRUCTION HCT04620
037B 0 0028 RSSAO DC /0028 HCT04630
037C 0 0020 RSSAP DC /0020 HCT04640
037D 0 5555 RSSAQ DC /5555 HCT04650
* HCT04660
* ERROR ROUTINE TO SERVICE NON-INTERRUPT ERRORS HCT04670
* HCT04680
037E 0 0000 RSDDD DC 0 STORAGE FOR RETURN ADDRES HCT04690
037F 0 2910 STS RSDDJ STORE STATUS DFLO+CA RY HCT04700
0380 0 C0FD RSDDX LD RSDDD HCT04710
0381 0 90F6 S RSSAL CORRECT I REG HCT04720
0382 0 1890 SRT 16 STORE I REG IN Q HCT04730
0383 0 C0FA LD RSDDD HCT04740
0384 0 90F4 A RSSAM INCREMENT RETURN ADDRESS HCT04750

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

0385 0 00F8 STO RSDDD BY 1 TO AVOID DC IN AINL HCT04760
0386 00 0C000168 XIO L RSQAF IF SW 12 ON-CORRECT CONSL HCT04770
0388 00 C400016E LD L RSQAL HCT04780
038A 00 E4000377 AND L RSSAK INDICATOR LAMPS AND WAIT HCT04790
038C 00 4CA0037E PSC I RSDDD,Z HCT04800
038E 00 C400021F LD L RSQAN RELOAD A REG AS PER ERROR HCT04810
0390 0 2000 RSDDJ LDS 0 SAVE CARY+OFLO STATU HCT04820
0391 0 3000 WAIT HCT04830
0392 00 4C80037E BSC I RSDDD HCT04840
0394 0 C0E8 RSDDK LD RSSAQ HCT04850
0395 00 4C40012F BOSC L RSDKS RESET INTER-RETURN START HCT04860
***** HCT04870
* LOG ROUTINE * HCT04880
***** HCT04890
* HCT04900
0397 0 0000 LOG DC 0 SE HCT04910
0398 0 6B1B LOG01 STX 3 LOG06+1 SAVE IX 3 HCT04920
0399 00 0C000168 XIO L RSQAF HCT04930
0398 00 C400016E LD L RSQAL HCT04940
039D 00 4C100389 BSC L TWRTR,- BRANCH IF 1053 OUTPU HCT04950
* HCT04960
039F 00 C4800397 LD I LOG GET MESSAGE ADDRESS HCT04970
03A1 0 D052 STO PRWRT SET IN ICCE HCT04980
* HCT04990
03A2 0 084D LOG02 XIO PRSNS CHECK PRINTER READY HCT05000
03A3 00 4C0403A9 BSC L LOG03,E BRANCH IF NOT READY HCT05010
03A5 0 1801 SRA 1 HCT05020
03A6 00 4CC403AB BSC L LOG04,E BRANCH IF BUSY HCT05030
03A8 0 7004 MDX LOG05 READY AND NOT BUSY HCT05040
* HCT05050
03A9 0 300A LOG03 WAIT 10 NOT READY HCT05060
03AA 0 70F7 MDX LOG02 CHECK AGAIN HCT05070
* HCT05080
03AB 0 300B LOG04 WAIT 11 BUSY HCT05090
03AC 0 70F5 MDX LOG02 CHECK AGAIN HCT05100
* HCT05110
03AD 0 0846 LOG05 XIO PRWRT OUTPUT MESSAGE HCT05120
* HCT05130
* XIO PRSN CHECK FOR OP COMPLT HCT05140
03AE 0 0943 XIO PRSN HCT05150
03AF 0 1002 SLA 2 HCT05160
03B0 0 4810 BSC - HCT05170
03B1 0 70FC MDX *-4 HCT05180
03B2 0 0830 XIO PRSNS RESET DSW HCT05190
* HCT05200
* PRINTING COMPLETE HCT05210
* HCT05220
03B3 00 67000000 LCC06 LDX L3 0 RESTORE IX 3 HCT05220
03B5 00 74010397 MDX L LOG,1 BUMP RETURN HCT05230
* HCT05240
03B7 00 4C800397 BSC I LOG RETURN TO USER SX HCT05250
* HCT05260
03B9 0 1010 TWRTR SLA 16 HCT05270
03BA 0 0032 STO WRDSW HCT05280
03BB 0 083A XIO TWSNS CHECK IF TYPEWRITER HCT05290
03BC 0 1005 SLA 5 READY HCT05300
03BD 0 130F SRA 15 HCT05310
03BE 00 4C1803C2 BSC L TWR01,+ HCT05320
* HCT05330
03C0 0 300C WAIT 12 NOT READY HCT05340
03C1 0 70F9 MDX TWRTR+2 HCT05350
* HCT05360
03C2 0 C028 TWR01 LD TWRTO CARRAIGE RETURN AND HCT05370
03C3 0 002A STO IOARA LINE SPACE TO IO ARA HCT05380
* HCT05390
03C4 0 0833 XIO TWWRT CARG RETURN/LINE SP HCT05400
* HCT05410
03C5 0 0830 XIO TWSNS HANG TILL NOT BUSY HCT05420
03C6 0 180B SRA 11 HCT05430

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

0431 0 0449	DC	ZONE2	11 ZONE
0432 0 0453	DC	ZONE3	12 ZONE
* ZONEN			
0433 0 0021	DC	/0021	SPACE
0434 0 00FC	DC	/00FC	1
0435 0 00DR	DC	/00DR	2
0436 0 00DC	DC	/00DC	3
0437 0 00FG	DC	/00FG	4
0438 0 00F4	DC	/00F4	5
0439 0 00D0	DC	/00D0	6
043A 0 00D4	DC	/00D4	7
043B 0 00E4	DC	/00E4	8
043C 0 00E0	DC	/00E0	9
043D 0 00C4	DC	/00C4	0
* ZONE1			
043E 0 0000	DC	0	
043F 0 0000	DC	0	
0440 0 009A	DC	/009A	S
0441 0 009E	DC	/009E	T
0442 0 00B2	DC	/00B2	U
0443 0 00B6	DC	/00B6	V
0444 0 0092	DC	/0092	W
0445 0 0096	DC	/0096	X
0446 0 00A6	DC	/00A6	Y
0447 0 00A2	DC	/00A2	Z
0448 0 0021	DC	/0021	SPACE
* ZONE2			
0449 0 0000	DC	0	
044A 0 007E	DC	/007E	J
044B 0 005A	DC	/005A	K
044C 0 005E	DC	/005E	L
044D 0 0072	DC	/0072	M
044E 0 0076	DC	/0076	N
044F 0 0052	DC	/0052	D
0450 0 0056	DC	/0056	P
0451 0 0066	DC	/0066	Q
0452 0 0062	DC	/0062	R
* ZONE3			
0453 0 0000	DC	0	
0454 0 003E	DC	/003E	A
0455 0 001A	DC	/001A	B
0456 0 001E	DC	/001E	C
0457 0 0032	DC	/0032	D
0458 0 0036	DC	/0036	E
0459 0 0012	DC	/0012	F
045A 0 0016	DC	/0016	G
045B 0 0026	DC	/0026	H
045C 0 0022	DC	/0022	I
045D 0 0086	DC	/0086	O ERROR
045E 0 0000	DC	/0000	PERIOD
* MES01			
045F 0 000A	DC	10	WORD CT
0460 0 2435	DC	/2435	ME
0461 0 2426	DC	/2426	MO
0462 0 2918	DC	/2918	RY
0463 0 0013	DC	/0013	T
0464 0 3512	DC	/3512	ES
0465 0 1300	DC	/1300	T
0466 0 3839	DC	/3839	HI
0467 0 0033	DC	/0033	C
0468 0 2629	DC	/2629	OR
0469 0 3500	DC	/3500	E
046A 0 FFFF	DC	/FFFF	TERM
* MES02			
046B 0 0006	DC	6	WD CT
046C 0 2729	DC	/2729	PR
046D 0 2637	DC	/2637	OG
046E 0 2931	DC	/2931	RA
046F 0 2400	DC	/2400	M
0470 0 3525	DC	/3525	FN
0471 0 3400	DC	/3400	D

HCT06800
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HCT07450
HCT07460
HCT07470

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

0472 0 FFFF	DC	/FFFF	TERM
* MES03			
0473 0 000B	DC	11	WD CT
0474 0 3529	DC	/3529	ER
0475 0 2926	DC	/2926	RO
0476 0 2900	DC	/2900	R
0477 0 3925	DC	/3925	IN
0478 0 1300	DC	/1300	T
0479 0 1213	DC	/1213	ST
047A 0 2629	DC	/2629	OR
047B 0 3700	DC	/3700	G
047C 0 2729	DC	/2729	PR
047D 0 2613	DC	/2613	OT
047E 0 FFFF	DC	/FFFF	TERM
* MES04			
047F 0 0008	DC	8	WD CT
0480 0 3529	DC	/3529	ER
0481 0 2926	DC	/2926	RO
0482 0 2900	DC	/2900	R
0483 0 3925	DC	/3925	IN
0484 0 1300	DC	/1300	T
0485 0 2731	DC	/2731	PA
0486 0 2939	DC	/2939	RI
0487 0 1318	DC	/1318	TY
0488 0 FFFF	DC	/FFFF	TERM
* MES05			
0489 0 000B	DC	11	WD CT
048A 0 3529	DC	/3529	ER
048B 0 2926	DC	/2926	RO
048C 0 2900	DC	/2900	R
048D 0 3925	DC	/3925	IN
048E 0 1300	DC	/1300	T
048F 0 3925	DC	/3925	IN
0490 0 1500	DC	/1500	V
0491 0 2627	DC	/2627	DP
0492 0 0033	DC	/0033	C
0493 0 2634	DC	/2634	OD
0494 0 3500	DC	/3500	E
0495 0 FFFF	DC	/FFFF	TERM
* MES06			
0496 0 0002	DC	2	WD CT
0497 0 3529	DC	/3529	ER
0498 0 0001	DC	/0001	1
0499 0 FFFF	DC	/FFFF	TERM
* MES07			
049A 0 0002	DC	2	WD CT
049B 0 3529	DC	/3529	ER
049C 0 0002	DC	/0002	2
049D 0 FFFF	DC	/FFFF	TERM
* MES08			
049E 0 0002	DC	2	WD CT
049F 0 3529	DC	/3529	ER
04A0 0 0003	DC	/0003	3
04A1 0 FFFF	DC	/FFFF	TERM
* MES09			
04A2 0 0002	DC	2	WD CT
04A3 0 3529	DC	/3529	ER
04A4 0 0004	DC	/0004	4
04A5 0 FFFF	DC	/FFFF	TERM
* MES10			
04A6 0 0002	DC	2	WD CT
04A7 0 3529	DC	/3529	ER
04A8 0 0005	DC	/0005	5
04A9 0 FFFF	DC	/FFFF	TERM
* MES11			
04AA 0 0002	DC	2	WD CT
04AB 0 3529	DC	/3529	ER
04AC 0 0006	DC	/0006	6

HCT07480
HCT07490
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HCT08090
HCT08100
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HCT08120
HCT08130
HCT08140
HCT08150

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

04AD 0	FFFF		DC	/FFFF	TERM
04AE 0	0000	RSEND	DC	0	
04AF 0	0000		DC	0	
04B0 0	0000		DC	0	
04B2	012C		END	RSDKR	

HCT08160
HCT08170
HCT08180
HCT08190
HCT08200

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
CODCV	03FA	03D4,0428
CODC1	0401	041D
CODC2	0413	0412
CODC3	041E	0418
CODC4	0422	03FB,03FC,03FD
CODWD	042A	03CF,03D6,0401,0421
COD00	042C	0408,0409,040D,040E
COD01	042D	0415,041E
COD02	042E	0420
IOARA	03FE	03C3,03D8,03E1,03E3,03F8
LHIND	042B	03FF,0403,0417,041A
LOG	0397	033B,034F,0356,039F,03B5,03B7,03CA
LOG01	0398	
LOG02	03A2	03AA,03AC
LOG03	03A9	03A3
LOG04	03AB	03A6
LOG05	03AD	03A8
LOG06	03B3	0398,03D2
MES01	045F	
MES02	046B	
MES03	0473	033D
MES04	047F	0351
MES05	0489	0358
MES06	0496	
MES07	049A	
MES08	049E	
MES09	04A2	
MES10	04A6	
MES11	04AA	
NEXT	0324	0322
PRSN	03F2	03AE
PRSNS	03F0	03A2,03B2
PRWRT	03F4	03A1,03AD
RSAA B	0141	013D
RSAA C	0146	0141,0159
RSAA D	0147	013F
RSAA E	0148	0132,0136,014E
RSAA F	014E	0145
RSAA G	0153	0152
RSAA H	0149	0135,0151,0153,015A,015C,015E,0188,01A9,0206,0248,0277,02C7,02F7
RSAA I	015C	0157
RSAA J	0152	015F
RSAA K	014A	0142,0174,0290
RSAA L	0160	0171
RSAA M	0164	012F
RSAA N	0166	012C
RSAA B A	0171	015B
RSAA B B	0185	0183
RSAA B C	0187	018F
RSAA B D	0190	018C
RSAA B E	0192	01A0,01AA,01B1
RSAA B F	01A5	0196
RSAA B G	01B2	01AE
RSAA B H	0184	01BA,031B
RSAA B I	0182	0175,030E
RSAA B J	01D6	01C7
RSAA B K	01F7	01E8
RSAA B L	01E0	01F2,01FD
RSAA B M	0205	0201
RSAA B N	01BF	01D4,01DC,020C
RSAA B O	0200	0208
RSAA B P	01B0	020E
RSAA B Q	01E1	0204
RSAA B R	01BC	0215

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

RSACA	0245	0240
RSACB	0238	024E
RSACD	0247	0244
RSACE	025A	0256
RSACF	026A	0259,025B
RSACG	0254	026E
RSACH	0252	0265,0274
RSACJ	0220	0217,0282
RSACK	0226	0279
RSACL	0251	027C
RSACM	028B	02AC
RSACN	029F	02B6,02C0,02C9
RSACO	02A3	029A,02C6
RSACP	02EB	02DC
RSACQ	02D3	02E6,02F0,02F9
RSACR	02D4	02D2,02F6
RSACS	0297	02FC
RSACU	0296	0292,0303
RSACV	0290	0284
RSACW	027D	0229
RSACX	022A	0228
RSADA	0305	0294
RSADB	024F	024A
RSCCA	031D	0168,0341,035E,0364,0369
RSCCB	0343	032E,033E
RSCCC	0352	034D
RSCCD	0359	0339,0349,0354
RSCCE	0367	031F
RSCCG	033F	0331
RSCCH	0368	0363
RSCCQ	0318	0307
RSDDD	037E	01A2,01C9,01F4,0267,02B8,02E8,0380,0383,0385,038C, 0392
RSDDJ	0390	037F
RSDDK	0394	032A
RSDDX	0380	
RSDKR	012C	0481
RSOKS	012F	0164,0166,0319,0395
RSEND	04AE	016A,02A3,02D4
RSEXI	0310	
RSFAA	0148	0182
RSFAB	014C	0183,0305
RSFAC	014D	0134
RSQAC	016A	0185,0190,01BD,0238,024F,0297,02CF
RSQAD	016B	0179
RSQAE	016C	0187,0188,0189,0192,0193,0195,01AC
RSQAF	0168	019A,01A5,01B4,01CE,01D6,01EC,01F7,020F,025F,026F, 027D,0280,028B,02E0,02EB,02FD,0308,0310,0324,0333, 0343,0359,0386,0399
RSQAH	021A	018F,01C0,01C3,01C5,01E1,01E5,0205,020A,022A,022B, 022E,022F,0231,0232,0235,0236
RSQAI	021B	01C2
RSQAJ	021C	01DE
RSQAK	021D	01DF,01E0,01E3,01E7,01FF,0203
RSQAL	016E	0168,019C,01A6,01B6,01D0,01D8,01EE,01F9,0211,0261, 0271,027F,0282,028D,02E2,02ED,02FF,030A,0312,0326, 0335,0345,035B,0388,039B
RSQAM	021E	020B,02C3,02F3
RSQAN	021F	0198,01CC,01EA,025D,02AE,02DE,038E
RSQAO	0169	0178
RSQAP	016D	0177
RSQAQ	0218	0224
RSQAR	0219	0225,0226
RSQAS	0318	0314
RSQAU	016F	017C
RSQAV	0170	017F
RSQAW	0316	
RSRAA	0285	023A,023B,0242,0245,0247,024C,0251,0254,026A,0276

CORE STORAGE FUNCTION TEST
HIGH CORE TEST

RSRAB	0286	023D,023F
RSRAC	0287	022C,0233,0258,025A,029F,02AB
RSRAE	0288	0299,02A0,02A4,02A7,02A9,02C2,02C5,02D1,02D5,02D8, 02DA,02F2,02F5
RSRAF	0289	02A6,02D7
RSRAG	028A	0188,0213,0281,0301
RSRAH	028B	030C
RSRAI	028C	019E,01A8,01D2,01DA,01F0,01F8,0263,0273,02B4,02BF, 02E4,02EF
RSRAJ	028E	0252
RSRAK	028F	0253,026C
RSRAX	028D	0337,0347
RSSAA	036B	031E,0366
RSSAC	036E	0320
RSSAD	0370	0321,032C,033F,034B,0352,0360
RSSAE	0374	032D,0340
RSSAF	0371	029D,02CD,0330
RSSAG	0372	02CB
RSSAH	0373	029B
RSSAI	0375	034C
RSSAJ	0376	0353
RSSAK	0377	035D,038A
RSSAL	0378	0381
RSSAM	0379	0384
RSSAN	037A	0362
RSSAO	037B	0328
RSSAP	037C	0329
RSSAQ	037D	0394
TWRTR	03B9	039D,03C1
TWRTO	03EB	03C2
TWRT1	03EC	03D1
TWR01	03C2	038E
TWR02	03CD	03CC,03EA
TWR03	05E7	03E0
TWSNS	03F6	017D,038B,03C5,03DA
TWVRT	03F8	0180,03C4,03D9
WRDSW	03ED	038A,03DE,03E4,03E8
XIOSN	03DA	03DD
XIOWR	03D9	03E6
ZONE	042F	0410
ZONEN	0433	042F
ZONE1	043E	0430
ZONE2	0449	0431
ZONE3	0453	0432

CORE STORAGE FUNCTION TEST
0-9 CORE TEST

```

*
* STORAGE PROTECT TEST
*
018D 00 C4000187 RSPPT LD L RSLAE ACC=/FFFF
018F 00 D4000003 STO L 3
01C1 0 6300 LDX X3 0
01C2 00 C4000003 LD L 3
01C4 00 4C1801F6 BSC L RSPER,+
01C6 0 C0EF RSR05 LD RSLAD ACC=/0000
01C7 00 D4800185 STO I RSLAC
01C9 0 2CC1 DC /2CC1 STORAGE PRT-IA
01CA 0 01B5 DC RSLAC
01CB 0 C0EC LD RSLAF ACC=/FFFF
01CC 00 D4800185 STO I RSLAC
01CE 00 C4800185 LD I RSLAC
01D0 00 4C1801D5 BSC L RSQ05,+
01D2 00 44000202 BSI L RSEOR
01D4 0 70F1 MDX RSR05
01D5 00 44000238 RSQ05 BSI L RSL0P
01D7 0 2CC0 RSR06 DC /2CC0 CLEAR SP-IA
01D8 0 01B5 DC RSLAC
01D9 0 CODE LD RSLAF ACC=/FFFF
01DA 00 D4800185 STO I RSLAC
01DC 00 C4800185 LD I RSLAC
01DE 0 F0D9 EOR RSLAF
01DF 00 4C1801F4 BSC L RSQ06,+
01E1 00 44000202 BSI L RSEOR
01E3 0 70F3 MDX RSR06
01E4 00 44000238 RSQ06 BSI L RSL0P
*
* PROGRAM END ROUTINE
*
01E6 00 74FF0231 RSPER MDX L RSPPC,-1 COUNT PRGM PASSES
01E8 0 708C MDX RSR01
01E9 0 C010 LD RSR5X
01EA 00 D4000008 STO L /8
*
* WAIT TO TURN DISABLE INTERRUPT SWITCH
* TO OFF POSITION-1800 ONLY
*
01EC 0 1000 WAITB SLA 0 ENABLE INTERRUPTS
01ED 0 083R RSPES XIO RSBSB REPEAT PROG IF SW 14 ON
01EE 0 C03A LD RSBSB
01EF 0 F03F AND RSB14
01F0 00 4C20012F BSC L RSSTA,Z
01F2 0 C036 LD RSBSB
01F3 0 E03C AND RSB15
01F4 00 4C2001FB BSC L RSHOP,Z
01F6 00 64000050 RSFIN LDX L /0050 LINK TO NEXT PROG
01F8 0000 BSS E 0
01F8 0 0000 RSSIC DC 0
01F9 0 0300 DC /0300
01FA 0 01FE RSR5X DC RSR5I
01FB 0 3000 RSHOP WAIT
01FC 00 6400012F RSBTB LDX L RSSTA
01FE 0 0000 RSR5I DC 0
01FF 0 08FR XIO RSSIC
0200 00 4C4001ED BCSC L RSPES
*
* ERROR ROUTINE
*
0202 0 0000 RSEOR DC /0000 RETURN ADDRESS FOR E ROR
0203 0 D026 STO RSRAB
0204 0 0821 XIO RSRBS SENSE SW 11 FOR SCOP NG LD
0205 0 C023 LD RSBSB
0206 0 E025 AND RSB11
0207 00 4C18020B BSC L RSSBT,+ CONTINUE IF 11 OFF
0209 00 4C800202 BSC I RSEOR

```

CORE STORAGE FUNCTION TEST
0-9 CORE TEST

```

020B 0 C01D RSBT LD RSBSB SENSE SW 12 FOR HALT ON E
020C 0 C01C LD RSBSB
020D 0 E01F AND RSB12
020E 00 4C080212 BSC L RSHOE,+
0210 00 4C800202 BSC I RSEOR
0212 00 C4000185 RSHOE LD L RSLAC
0214 0 E01F AND RSCON
0215 0 F81D OR RSWAT
0216 0 D005 STO RSERW
0217 0 C0EA LD RSEOR
0218 00 940001BA S L RSLAH
021A 0 1890 SRT 16 LOAD I IN Q
021B 0 C00E LD RSRAB
021C 0 3000 RSERW WAIT
021D 00 4C800202 BSC I RSEOR
021F 0 C017 RSILC LD RSALT
0220 0 3000 RSWSC WAIT
0221 00 6400012F LDX L RSSTA
*
* STORAGE AREAS-2
*
0224 0002 BSS E 2
0226 0 0229 RSRBS DC RSBSB
0227 0 3A40 DC /3A40
0228 0 0000 RSBAB DC 0
0229 0 0000 RSBSB DC 0 BIT SWITCH BUFFER
022A 0 0000 RSRAB DC 0 SAVE A REG BUFFER
022B 0 0020 RSB10 DC /0020
022C 0 0010 RSB11 DC /0010
022D 0 0008 RSB12 DC /0008
022E 0 0004 RSB13 DC /0004
022F 0 0002 RSB14 DC /0002
0230 0 0001 RSB15 DC /0001
0231 0 0000 RSPPC DC 0
0232 0 0032 RSNPP DC 50
0233 0 3000 RSWAT DC /3000
0234 0 0FFF RSCON DC /0FFF
0235 0 0028 RSKXA DC /0028
0236 0 0020 RSKXB DC /0020
0237 0 5555 RSALT DC /5555
*
* CHECK SWITCH 13 TO LOOP ON ROUTINE
*
0238 0 0000 RSL0P DC 0
0239 00 C4000185 LD L RSLAC
023B 00 F4000189 EOR L RSLAG
023D 00 4C180249 BSC L RSCSE,+
023F 00 C4000185 LD L RSLAC
0241 00 8400018A A L RSLAH
0243 00 D4000185 STO L RSLAC
0245 00 74FD0238 MDX L RSL0P,-3
0247 00 4C800238 BSC I RSL0P
0248 00 D4000185 RSCSE LD L RSLAA LOAD LOWEST ADDRESS
024D 0 09D8 XIO RSRBS READ SW 13 TO LOOP R UTINE
024E 0 C0DA LD RSBSB
024F 0 E0DE AND RSB13
0250 00 4C980238 BSC I RSL0P,+
0252 00 74FD0238 MDX L RSL0P,-3
0254 00 4C800238 BSC I RSL0P
*****
* LOG ROUTINE *
*****
LOG DC 0 SE
LOG01 STX 3 LOG06+1 SAVE IX 3
XIO L RSRBS
LD L RSBSB

```

CORE STORAGE FUNCTION TEST
0-9 CORE TEST

025C 00 4C10027R	BSC L	TWRTR,-	BRANCH IF 1053 OUTPU	0-902720
025E 00 C4800256	LD I	LOG	GET MESSAGE ADDRESS	0-902730
0260 0 0051	STO	PRWRT	SET IN IOCC	0-902740
0261 0 084C	LOGO2 XIO	PRSNS	CHECK PRINTER READY	0-902750
0262 00 4C040268	BSC L	LOGO3,E	BRANCH IF NOT READY	0-902760
0264 0 1801	SKA	1		0-902770
0265 00 4C04026A	BSC L	LOGO4,E	BRANCH IF BUSY	0-902780
0267 0 70C4	MDX	LOGO5	READY AND NOT BUSY	0-902790
0268 0 300A	LOGO3 WAIT	10	NOT READY	0-902800
0269 0 70F7	MDX	LUGO2	CHECK GAIN	0-902810
026A 0 300B	LUGO4 WAIT	11	BUSY	0-902820
026B 0 70F5	MDX	LOGO2	CHECK AGAIN	0-902830
026C 0 0845	LOGO5 XIO	PRWRT	CUTPUT MESSAGE	0-902840
026D 0 0842	XIO	PRSN	CHECK FOR OP COMPLT	0-902850
026E 0 1002	SLA	2		0-902860
026F 0 4810	BSC	-		0-90287C
0270 0 70FC	MDX	*-4		0-902880
0271 0 083C	XIO	PRSNS	RESET DSW	0-902890
			PRINTING COMPLETE	0-902900
0272 00 67000000	LOGO6 LDX	L3 0	RESTORE IX 3	0-902910
0274 00 74010256	MDX L	LOG,1	BUMP RETURN	0-902920
0276 00 4C800256	BSC I	LOG	RETURN TO USER	0-902930
0278 0 1010	TWRTR SLA	16		0-902940
0279 0 0032	STO	WRDSW		0-902950
027A 0 0839	XIO	TWSNS	CHECK IF TYPEWRITER	0-902960
027B 0 1005	SLA	5	READY	0-902970
027C 0 180F	SRA	15		0-902980
027D 00 4C180281	BSC L	TWR01,+		0-902990
027F 0 300C	WAIT	12	NOT READY	0-903000
0280 0 70F9	MDX	TWRTR+2		0-903010
0281 0 C028	TWR01 LD	TWRTO	CARRAIGE RETURN AND	0-903020
0282 0 002A	STO	IOARA	LINE SPACE TO IO ARA	0-903030
0283 0 0832	XIO	TWWRT	CARG RETURN/LINF SP	0-903040
0284 0 082F	XIO	TWSNS	HANG TILL NOT BUSY	0-903050
0285 0 180R	SRA	11		0-903060
0286 0 4804	BSC	E		0-903070
0287 0 70FC	MDX	*-4		0-903080
0288 0 6301	LDX	3 1	BYPASS 1443 WORD COU T	0-903090
0289 00 C4800256	LD I	LOG	GET MESSAGE ADDRESS	0-903100
028B 0 0001	STO	TWR02+1		0-903110
028C 00 C7000000	TWR02 LD	L3 0	GET WORD TO PRINT	0-903120
028E 00 040002E8	STO L	CODWD	SFT IN CONVERSION RT	0-903130
0290 0 F01A	EOR	TWR1	CHECK IF TERMINATOR	0-903140
0291 00 4C180272	BSC L	LOGO6,+	BRANCH IF TERMINATOR	0-903150
0293 00 44000288	BSI L	CODCV	GO CONVERT 43 TO TW SRC	0-903160
0295 00 C40002E8	LD L	CODWD		0-903170
0297 0 0015	STO	IOARA		0-903180

CORE STORAGE FUNCTION TEST
0-9 CORE TEST

0298 0 081D	XIOWR XIO	TWWRT	WRITE CHARACTER	0-903400
0299 0 081A	XIOSN XIO	TWSNS	HANG ON BUSY	0-903410
029A 0 180B	SRA	11		0-903420
029B 0 4804	BSC	E		0-903430
029C 0 70FC	MDX	XIOSN	BUSY	0-903440
			CHECK IF 1ST 1/2 WORD	0-903450
029D 0 C00E	LD	WRDSW	GET 1/2 WORD SWITCH	0-903460
029E 0 4804	BSC	E		0-903470
029F 0 7006	MDX	TWR03	GO SET UP NEXT WORD	0-903480
			SET UP FOR 2ND 1/2 WORD	0-903490
02A0 0 C00C	LD	IOARA		0-903500
02A1 0 1008	SLA	8	POSITION 2ND 1/2 WD	0-903510
02A2 0 000A	STO	IOARA		0-903520
02A3 00 740102AC	MDX L	WRDSW,1	BUMP WORD SWITCH	0-903530
02A5 0 70F2	MDX	XIOWR	GO WRITE 2ND 1/2 WD	0-903540
			SET UP FOR NEXT WORD	0-903550
02A6 0 7301	TWR03 MDX	3 1	NEXT WORD INDEX	0-903560
02A7 00 740102AC	MDX L	WRDSW,1	BUMP WORD SWITCH	0-903570
02A9 0 70E2	MDX	TWR02	GO GET NEXT WORD	0-903580
			LOG CONSTANTS	0-903590
02AA 0 9103	TWRTO DC	/8103	LINE SP/CARRAIGE RTN	0-903600
02AB 0 FFFF	TWR1 DC	/FFFF	TERMINATOR	0-903610
02AC 0 0000	WRDSW DC	0	1/2 WORD SWITCH	0-903620
02AD 0 0000	IOARA DC	0	OUTPUT AREA	0-903630
02AE 0000	BSS E	0		0-903640
02AE 0 0000	PRSNS DC	/0000	PRINTER SENSE IOCC	0-903650
02AF 0 3701	DC	/3701		0-903660
02B0 0 0000	PRSN DC	0	NON RESET SENSE	0-903670
02B1 0 3700	DC	/3700		0-903680
02B2 0 0000	PRWRT DC	/0000	PRINTER WRITE IOCC	0-903690
02B3 0 3500	DC	/3500		0-903700
02B4 0 0000	TWSNS DC	/0000	TYPEWTR SENSE IOCC	0-903710
02B5 0 0F01	DC	/0F01	DSW RESET	0-903720
02B6 0 02AD	TWWRT DC	IOARA	TYPEWTR WRITE IOCC	0-903730
02B7 0 0900	DC	/0900	WR TYPEWRITER	0-903740
				0-903750
				0-903760
				0-903770
				0-903780
				0-903790
				0-903800
				0-903810
				0-903820
				0-903830
				0-903840
				0-903850
				0-903860
				0-903870
				0-903880
				0-903890
				0-903900
				0-903910
				0-903920
				0-903930
				0-903940
				0-903950
				0-903960
				0-903970
				0-903980
				0-903990
				0-904000
				0-904010
				0-904020
				0-904030
				0-904040
				0-904050
				0-904060
				0-904070

CORE STORAGE FUNCTION TEST
0-9 CORE TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
CDDCV	0288	0293,02E6
CDDC1	028F	02D8
CDDC2	02D1	02D0
CDDC3	02DC	02D6
CDDC4	02E0	02B9,02BA,02BB
CODWD	02E8	028E,0295,02BF,02DF
COD00	02EA	02C6,02C7,02C8,02CC
COD01	02EB	02D3,02DC
COD02	02EC	02DE
IOARA	02AD	0282,0297,02A0,02A2,02B6
LHIND	02E9	028D,02C1,02D5,02D8
LOG	0256	025E,0274,0276,0289
LOG01	0257	
LOG02	0261	0269,0268
LOG03	0268	0262
LOG04	026A	0265
LOG05	026C	0267
LOG06	0272	0257,0291
MES12	0310	
MES13	0329	
MES14	0336	
PRSN	028C	026D
PRSNS	02AE	0261,0271
PRWRT	02B2	0260,026C
RSAAN	0172	012C
RSALT	0237	021F
RSARB	022A	0203,021B
RSBAB	0228	
RSBIL	01AF	01AB
RSBSB	0229	01ED,01EE,01F2,0205,0208,020C,0226,024E,025A
RSBTB	01FC	
RSB10	022B	
RSB11	022C	0206
RSB12	022D	020D
RSB13	022E	024F
RSB14	022F	01EF
RSB15	0230	01F3
RSCON	0234	0214
RSCSE	0249	023D
RSDMS	014E	013E
RSD18	016D	0143
RSEDR	0202	017C,0189,0196,01A5,01D2,01E1,0209,0210,0217,021D
RSERW	021C	0216
RSFIN	01F6	
RSHOE	0212	020E
RSHOP	01FB	01F4
RSILC	021F	
RSKBA	0154	0153
RSKBC	0153	016A
RSKBD	0165	0158
RSKXA	0235	
RSKXB	0236	
RSLAA	0184	0135,0151,0154,015C,0165,0168,0249
RSLAB	0183	015A
RSLAC	0185	015E,0176,0178,0182,0184,018E,018F,0191,0193,019E, 01A0,01C7,01CA,01CC,01CE,01D8,01DA,01DC,0212,0239, 023F,0243,024B
RSLAD	0196	0175,01C6
RSLAE	0187	0137,0181,0186,018D
RSLAF	0198	019C,019D,01A2,01A8,01AA,01CB,01D9,01DE
RSLAG	0189	0162,023B
RSLAH	018A	0218,0241
RSLAI	018B	0198
RSLAJ	018C	0133
RSLAQ	0182	0160

CORE STORAGE FUNCTION TEST
0-9 CORE TEST

RSLOP	0238	017F,018C,0199,01AF,01D5,01E4,0245,0247,0250,0252, 0254
RSNPP	0232	012F
RSPER	01E6	01C4
RSPES	01ED	0200
RSPPC	0231	0131,01E6
RSQ01	017F	017A
RSQ02	018C	0187
RSQ03	0199	0194
RSQ04	01A8	01A3
RSQ05	01D5	01D0
RSQ06	01E4	01DF
RSR8S	0226	0141,0204,024D,0258
RSRSI	01FE	01FA
RSRSX	01FA	01E9
RSR01	0175	017E,01E8
RSR02	0191	018B
RSR03	018E	0198
RSR04	019D	01A7,01AD
RSR05	01C6	01D4
RSR06	01D7	01E3
RSR18	016B	0140
RSSBT	020B	0207
RSSIC	01F8	01FF
RSSPT	01BD	0181
RSSTA	012F	0172,01F0,01FC,0221
RSSTB	012C	033B
RST18	016C	0116
RSVBB	019B	01AE
RSWAT	0233	0215
RSWSC	0220	
RSZRO	016E	014E
TWRTR	0278	025C,0280
TWRTO	02AA	0281
TWRT1	02AB	0290
TWR01	0281	027D
TWR02	028C	0288,02A9
TWR03	02A6	029F
TWSNS	02B4	0144,027A,0284,0299
TWWRT	02B6	0147,0283,0298
WAITA	0174	014A,0164
WAITB	01EC	014C
WAITO	016F	0149
WRDSW	02AC	0279,029D,02A3,02A7
XIDSN	0299	029C
XIOWR	0298	02A5
ZONE	02ED	02CE
ZONEN	02F1	02ED
ZONE1	02FC	02EE
ZONE2	0307	02EF
ZONE3	0311	02F0

CORE STORAGE FUNCTION TEST
LOW CORE TEST

```

*
*
*
* MEMORY TEST-LOW CORE
*
028C          ABS
0800 0 C921   ORG      2048
0801 00 0C000000 RSDKR LDD  RSAAM
0803 0 C81E   RSUKS LDD  RSAAM
0804 00 0C000004 STD    L  4
0806 0 C013   LD      RSAAE      CLEAR Q REGISTER
0807 0 1890   SRT      16

* MACHINE DETERMINATION ROUTINE
*
0808 0 C011   LD      RSAAE
0809 00 04000003 STO    L  3
080B 00 6700FFFF LDX   L3 /FFFF
080D 00 C4000003 LD    L  3
080F 00 4C200813 BSC   L  RSAAB,Z
0811 0 C007   LD      RSAAD
0812 0 7004   MDX   X  1
0813 0 C004   RSAAB LD   RSAAC
0814 0 D007   STO    RSAAK
0815 00 67000000 LDX   L3 /0000      CLEAR XR 3
0817 0 7015   MDX   RSAAB

* STORAGE AREAS FOR INITIALIZATIONS
*
0818 0 0001   RSAAC DC   1      1130 CONSTANT
0819 0 FFFE   RSAAD DC  -2      1800 CONSTANT
081A 0 0000   RSAAE DC   0      CONSTANT ZERO
081B 0 07FD   RSAAH DC  2045   HIGHEST ADR TO TEST
081C 0 0000   RSAAK DC   0      MACHINE TYPE
081D 0 0003   RSFAA DC   3      NUMBER OF PROGRAM PA SES
081E 0 0000   RSFAB DC   0      PROGRAM PASS BUFFER

* STORAGE AREAS PART 1
*
081F 0 7003   RSAAL MDX  X  3
0820 0002    BSS   E  2
0822 00 4C000803 RSAAM BSC  L  RSDKS      BOOTSTRAP BRANCH INS
0824 0 082A   RSQAF DC   L  RSQAL      READ BIT SWITCH IOCC
0825 0 3A40   RSQAO DC   L  /3A40      SECOND HALF IOCC-113
0826 0 0009   RSQAC DC   L  9          LOWEST ADDRESS TO TEST
0827 0 0901   RSQAD DC   L  RSQCA      INTERRUPT LEVEL ZERO VECT
0828 0 0000   RSQAE DC   L  0          WORK AREA
0829 0 0240   RSQAP DC   L  /0240      SECOND HALF IOCC-180
082A 0 0000   RSQAL DC   L  0          BIT SWITCH BUFFER AREA
082B 0 0F03   RSQAU DC   L  /0F03      2ND HALF IOCC-1800 D W
082C 0 0902   RSQAV DC   L  /0902      2ND HALF IOCC-1800 TYPE

* INITIALIZE MASKS AND INTERRUPTS TO LEVEL ZERO
* 1800 ONLY
*
082D 0 C0F1   RSABA LD   RSAAL      STORE BOOTSTRAP BRAN H AT
082E 00 04000000 STO    L  0      LOCATION ZERO
0830 0 C0E8   LD      RSAAK
0831 00 4C04083E BSC   L  RSABI,E    IF 1130-GO TO FIRST ROUTI
0833 0 C0F5   LD      RSQAP      CHANGE SECOND HALF I CC
0834 0 00F0   STO    RSQAD      FOR 1800 READ BIT SW
0835 0 C0F1   LD      RSQAD      INTERRUPT LEVEL ERRO VECT
0836 00 04000009 STO    L  8
0838 0 C0F2   LD      RSQAU      DSW 1800
LCT00020
LCT00030
LCT00040
LCT00050
LCT00060
LCT00070
LCT00080
LCT00090
LCT00100
LCT00110
LCT00120
LCT00130
LCT00140
LCT00150
LCT00160
LCT00170
LCT00180
LCT00190
LCT00200
LCT00210
LCT00220
LCT00230
LCT00240
LCT00250
LCT00260
LCT00270
LCT00280
LCT00290
LCT00300
LCT00310
LCT00320
LCT00330
LCT00340
LCT00350
LCT00360
LCT00370
LCT00380
LCT00390
LCT00400
LCT00410
LCT00420
LCT00430
LCT00440
LCT00450
LCT00460
LCT00470
LCT00480
LCT00490
LCT00500
LCT00510
LCT00520
LCT00530
LCT00540
LCT00550
LCT00560
LCT00570
LCT00580
LCT00590
LCT00600
LCT00610
LCT00620
LCT00630
LCT00640
LCT00650
LCT00660
LCT00670
LCT00680
LCT00690

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CORE STORAGE FUNCTION TEST
LOW CORE TEST

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0839 00 04000AAB STO    L  TWSNS+1
083B 0 C0F0     LD      RSQAV      XIO WRITE 1800
083C 00 04000AAD STO    L  TWRWT+1

* FIRST ROUTINE-READ + WRITE IN MEMORY
*
083E 0 CODE   RSABI LD   RSFAA      INITIALIZE PROGRAM
083F 0 D0DE   STO    RSFAB      PASS COUNTER
0840 0 6204   RSABH LDX  X2 4      ADDRESSING PASSES
0841 00 65800826 RSABB LDX  I1 RSQAC
0843 0 69E4   RSABC STX  I  RSQAE
0844 0 C0E3   LD      RSQAE
0845 00 04800828 STO    I  RSQAE
0847 0 F0D3   EOR    RSAAH
0848 00 4C18084C BSC   L  RSABD,+
084A 0 7101   MDX   X1 1      INCR TO NEXT ADDRESS
084B 0 70F7   MDX   RSABC
084C 00 65800826 RSABD LDX  I1 RSQAC
084E 0 69D9   RSABE STX  I  RSQAE
084F 00 4C800828 LD    I  RSQAE
0851 0 F0D6   EOR    RSQAE
0852 00 4C180861 BSC   L  RSABF,+
0854 00 0400080B STC   L  RSQAN      ERROR 1 DETECTED
0856 00 0C000824 XIO   L  RSQAF      STORE ACCUM FOR ERROR ROU
0858 00 4C00082A LD    L  RSQAL
085A 00 44000948 AND   L  RSRAI
085C 00 4C20084E BSC   L  RSABE,Z
085E 00 44000A32 BSI   L  RSDDD
0860 0 FFFE   DC      /FFFF      ERROR 1 CONSTANT
0861 0 08C2   RSABF XIL  RSQAF      READ BIT SWITCHES
0862 00 4C00082A LD    L  RSQAL
0864 00 44000948 AND   L  RSRAI      ISOLATE BIT SW 11
0866 00 4C20084E BSC   L  RSABE,Z    IF BIT SW 11 ON-REPEAT AD
0868 0 C0BF   LD      RSQAE
0869 0 F0B1   EOR    RSAAH
086A 00 4C18086E BSC   L  RSABG,+
086C 0 7101   MDX   X1 1      INCR TO NEXT ADDRESS
086D 0 70E0   MDX   RSABE
086E 0 72FF   RSABG MDX  X2 -1    COUNT PASSES
086F 0 70D1   MDX   RSABB
0870 00 0C000824 XIO   L  RSQAF      REPEAT ROUTINE IF SW13 ON
0872 00 4C00082A LD    L  RSQAL
0874 00 44000948 AND   L  RSRAG
0876 00 4C200840 BSC   L  RSABH,Z    REPEAT ADDRESSING RO TINE

* SECOND ROUTINE
* BIT ISOLATION TEST-BIT BY BIT-ADRESS BY ADDRESS
*
0878 0 6304   RSABR LDX  X3 4      BIT ISOLATION PASSES
0879 00 4C000826 RSABP LD   L  RSQAC
087B 0 D05A   RSABN STO  L  RSQAH
087C 00 65800806 LDX   I1 RSQAH
087E 0 C058   LD    RSQAI
087F 00 04800806 STO    I  RSQAH
0881 00 4C800806 LD    I  RSQAH
0883 00 4C180892 BSC   L  RSABJ,+
0885 00 44000A32 BSI   L  RSDDD      ERRCR 2 DETECTED
0887 0 FFFD   DC      /FFFF      ERROR 2 CONSTANT
0888 00 04000809 STO    L  RSQAN      STORE ACC FOR ERROR OUTI
088A 00 0C000824 XIO   L  RSQAF
088C 00 4C00082A LD    L  RSQAL
088E 00 44000948 AND   L  RSRAI
0890 00 4C20087C BSC   L  RSABN+1,Z
0892 00 0C000824 RSABJ XIO  L  RSQAF      IF BIT SW 11 ON REPE T AD
0894 00 4C00082A LD    L  RSQAL
0896 00 44000948 AND   L  RSRAI
0898 00 4C20087C BSC   L  RSABN+1,Z
089A 0 C03D   LD    RSQAJ
LCT00700
LCT00710
LCT00720
LCT00730
LCT00740
LCT00750
LCT00760
LCT00770
LCT00780
LCT00790
LCT00800
LCT00810
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LCT00980
LCT00990
LCT01000
LCT01010
LCT01020
LCT01030
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LCT01200
LCT01210
LCT01220
LCT01230
LCT01240
LCT01250
LCT01260
LCT01270
LCT01280
LCT01290
LCT01300
LCT01310
LCT01320
LCT01330
LCT01340
LCT01350
LCT01360
LCT01370

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CORE STORAGE FUNCTION TEST
LOW CORE TEST

0898 0 003D	STO	RSQAK	LCT01380
089C 0 C03C	RSABL LD	RSQAK	LCT01390
089D 00 048008D6	RSABQ STO I	RSQAH	LCT01400
089F 00 668008D9	LDX I2	RSQAK	LCT01410
08A1 00 C48008D6	LD I	RSQAH	LCT01420
08A3 0 F035	EOR	RSQAK	LCT01430
08A4 00 4C180893	BSC L	RSABK,+-	LCT01440
08A6 00 040008D8	STO L	RSQAN	LCT01450
08A8 00 0C000824	XIJ L	RSQAF	LCT01460
08AA 00 C400082A	LD L	RSQAL	LCT01470
08AC 00 E4000948	AND L	RSRAI	LCT01480
08AE 00 4C20089C	BSC L	RSABL,Z	LCT01490
08B0 00 44000A32	BSI L	RSDDD	LCT01500
08B2 0 FFFB	DC	/FFFF	LCT01510
08B3 00 0C000824	RSABK XIJ L	RSQAF	LCT01520
08B5 00 C400082A	LD L	RSQAL	LCT01530
08B7 00 F4000948	AND L	RSRAI	LCT01540
08B9 00 4C20089C	BSC L	RSABL,Z	LCT01550
08BB 0 C01D	LD	RSQAK	LCT01560
08BC 0 4804	BSC	E	LCT01570
08BD 0 7003	MDX	RSABM	LCT01580
08BE 0 1801	SRA	I	LCT01590
08BF 0 0019	STO	RSQAK	LCT01600
08C0 0 700C	MDX	RSABQ	LCT01610
08C1 0 C014	RSABM LD	RSQAH	LCT01620
08C2 00 F4000819	EOR L	RSAAH	LCT01630
08C4 00 4C1808C9	BSC L	RSABD,+-	LCT01640
08C6 0 C00F	LD	RSQAH	LCT01650
08C7 0 8012	A	RSQAM	LCT01660
08C8 0 70B2	MDX	RSABN	LCT01670
08C9 0 73FF	RSABD MDX X3	-1	LCT01680
08CA 0 70AE	MDX	RSABP	LCT01690
08CB 00 0C000824	XIJ L	RSQAF	LCT01700
08CD 00 C400082A	LD L	RSQAL	LCT01710
08CF 00 E4000946	AND L	RSRAG	LCT01720
08D1 00 4C200878	BSC L	RSABR,Z	LCT01730
08D3 0 7008	MDX	RSACJ	LCT01740
* STOPAGE AREAS PART 2			
08D4 0 0004	RSQAQ DC	4	LCT01750
08D5 0 0000	RSQAR DC	0	LCT01760
08D6 0 0000	RSQAH DC	0	LCT01770
08D7 0 0000	RSQAI DC	0	LCT01780
08D8 0 8000	RSQAJ DC	/8000	LCT01790
08D9 0 0000	RSQAK DC	0	LCT01800
08DA 0 0001	RSQAM DC	1	LCT01810
08DB 0 0000	RSQAN DC	0	LCT01820
* ESTABLISH WORST CASE PATTERN			
08DC 00 66000000	RSACJ LDX L2	/0000	LCT01830
08DE 00 6700FFFF	LDX L3	/FFFF	LCT01840
08E0 0 C0F3	LD	RSQAQ	LCT01850
08E1 0 00F3	STC	RSQAR	LCT01860
08E2 00 74FF08D5	RSACK MDX L	RSQAR,-1	LCT01870
08E4 0 7001	MDX	RSACX	LCT01880
08E5 0 7053	MDX	RSACW	LCT01890
08E6 0 4AEF	RSACX STX 2	RSQAH	LCT01900
08E7 0 C0FE	LD	RSQAH	LCT01910
08E8 00 F4000943	EOR L	RSRAC	LCT01920
08EA 0 00FB	STO	RSQAH	LCT01930
08EB 00 668008D6	LDX I2	RSQAH	LCT01940
08ED 0 68E8	STX 3	RSQAH	LCT01950
08EE 0 C0E7	LD	RSQAH	LCT01960
08EF 00 F4000943	EOR L	RSRAC	LCT01970
08F1 0 00E4	STO	RSQAH	LCT01980
08F2 00 678008D6	LDX I3	RSQAH	LCT01990

CORE STORAGE FUNCTION TEST
LOW CORE TEST

08F4 00 C4000826	LD L	RSQAC	LCT02060
08F6 0 004A	STO	RSRAA	LCT02070
08F7 0 C049	RSACB LD	RSRAA	LCT02080
08F8 0 1806	SRA	6	LCT02090
08F9 0 0048	STO	RSRAB	LCT02100
08FA 0 1802	SRA	2	LCT02110
08FB 0 8046	A	RSRAB	LCT02120
08FC 00 4C040901	BSC L	RSACA,E	LCT02130
08FE 00 6E800941	STX I2	RSRAA	LCT02140
0900 0 7002	MDX	RSACD	LCT02150
0901 00 6F800941	RSACA STX I3	RSRAA	LCT02160
0903 0 C03D	RSACD LD	RSRAA	LCT02170
0904 00 F4000818	EOR L	RSAAH	LCT02180
0906 00 4C180908	BSC L	RSADB,+-	LCT02190
0908 00 74010941	MDX L	RSRAA,1	LCT02200
090A 0 70EC	MDX	RSACB	LCT02210
* WORST CASE TEST LOAD AND STORE THEN			
* COMPLEMENT AND REPEAT			
0908 00 65800826	RSADB LDX I1	RSQAC	LCT02220
090D 0 6933	RSACL STX 1	RSRAA	LCT02230
090E 0 C03B	RSACH LD	RSRAJ	LCT02240
090F 0 0C3B	STO	RSRAK	LCT02250
0910 00 C4800941	RSACG LD I	RSRAA	LCT02260
0912 00 4C200916	BSC L	RSACE,Z	LCT02270
0914 0 F02E	EOR	RSRAC	LCT02280
0915 0 7010	MDX	RSACF	LCT02290
0916 0 F02C	RSACE EOR	RSRAC	LCT02300
0917 00 4C180926	BSC L	RSACF,+-	LCT02310
0919 00 040008D8	STO L	RSQAN	LCT02320
091B 00 0C000824	XIJ L	RSQAF	LCT02330
091D 00 C400082A	LD L	RSQAL	LCT02340
091F 00 E4000948	AND L	RSRAI	LCT02350
0921 00 4C20090E	BSC L	RSACH,Z	LCT02360
0923 00 44000A32	BSI L	RSDDD	LCT02370
0925 0 FFF7	DC	/FFF7	LCT02380
0926 00 04800941	RSACF STO I	RSRAA	LCT02390
0928 00 74FE0943	MDX L	RSRAK,-2	LCT02400
092A 0 70E5	MDX	RSACG	LCT02410
092B 00 0C000824	XIJ L	RSQAF	LCT02420
092D 00 C400082A	LD L	RSQAL	LCT02430
092F 0 E018	AND	RSRAI	LCT02440
0930 00 4C20090E	BSC L	RSACH,Z	LCT02450
0932 0 C00E	LD	RSRAA	LCT02460
0933 00 F4000818	EOR L	RSAAH	LCT02470
0935 00 4C1808E2	BSC L	RSACK,+-	LCT02480
0937 0 7101	MDX X1	1	LCT02490
0938 0 70D4	MDX	RSACL	LCT02500
0939 00 0C000824	RSACW XIJ L	RSQAF	LCT02510
093B 00 C400082A	LD L	RSQAL	LCT02520
093D 0 E008	AND	RSRAG	LCT02530
093E 00 4C2008DC	BSC L	RSACJ,Z	LCT02540
0940 0 700B	MDX	RSACV	LCT02550
* STORAGE AREAS PART 3			
0941 0 0000	RSRAA DC	0	LCT02560
0942 0 0000	RSRAB DC	0	LCT02570
0943 0 FFFF	RSRAC DC	/FFFF	LCT02580
0944 0 0000	RSRAE DC	0	LCT02590
0945 0 0000	RSRAF DC	0	LCT02600
0946 0 0004	RSRAG DC	/0004	LCT02610
0947 0 0002	RSRAH DC	/0002	LCT02620
0948 0 0010	RSRAI DC	/0010	LCT02630
0949 0 0020	RSRAJ DC	/0020	LCT02640
094A 0 0003	RSRAK DC	3	LCT02650
094B 0 0000	RSRAK DC	0	LCT02660

CORE STORAGE FUNCTION TEST LOW CORE TEST

* STORAGE PROTECTION TEST ROUTINES
* WRITE ZEROS ON PROTECTED AREA OF ONES
* UNPROTECT AND CLEAR MEMORY OF ONES
094C 00 C400081C
094E 00 4C080352
0950 00 640009C1
0952 0 6204
0953 00 C4000826
0955 0 D0EE
0956 0 D008
0957 00 C4000A27
0959 00 D4000A25
095B 0 COE7
095C 00 D4800944
095E 0 2C41
095F 0 0862
0960 00 65800944
0962 0 COE2
0963 00 D4800944
0965 00 C4800944
0967 0 F0DB
0968 00 4C180977
096A 00 D4000908
096C 00 0C000824
096E 00 C400082A
0970 00 E4000948
0972 00 4C200958
0974 00 44000A32
0976 0 FFEF
0977 00 0C000824
0979 00 C400082A
097B 0 E0CC
097C 00 4C200958
097E 0 C0C5
097F 00 840008DA
0981 0 D0C2
0982 0 D0DC
0983 00 F4000818
0985 00 4C200958
0987 00 C4000A26
0989 00 D4000A25
098B 00 C4000826
098D 0 D0B6
098E 0 D001
098F 0 2C40
0990 0 0862
0991 00 65800944
0993 0 C0B1
0994 00 D4800944
0996 00 C4800944
0998 00 4C1809A7
099A 00 D40008DB
099C 00 0C000824
099E 00 C400082A
09A0 00 E4000948
09A2 00 4C20098F
09A4 00 44000A32
09A6 0 FFD7
09A7 00 0C000824
09A9 00 C400082A
09AB 0 E09C
09AC 00 4C20098F

LCT02740
LCT02750
LCT02760
LCT02770
LCT02780
LCT02790
LCT02800
LCT02810
LCT02820
LCT02830
LCT02840
LCT02850
LCT02860
LCT02870
LCT02880
LCT02890
LCT02900
LCT02910
LCT02920
LCT02930
LCT02940
LCT02950
LCT02960
LCT02970
LCT02980
LCT02990
LCT03000
LCT03010
LCT03020
LCT03030
LCT03040
LCT03050
LCT03060
LCT03070
LCT03080
LCT03090
LCT03100
LCT03110
LCT03120
LCT03130
LCT03140
LCT03150
LCT03160
LCT03170
LCT03180
LCT03190
LCT03200
LCT03210
LCT03220
LCT03230
LCT03240
LCT03250
LCT03260
LCT03270
LCT03280
LCT03290
LCT03300
LCT03310
LCT03320
LCT03330
LCT03340
LCT03350
LCT03360
LCT03370
LCT03380
LCT03390
LCT03400
LCT03410

CORE STORAGE FUNCTION TEST LOW CORE TEST

09AF 0 C095
09AF 00 840008DA
09B1 0 D092
09B2 0 D0DD
09B3 00 F4000818
09B5 00 4C20098F
09B7 0 72FF
09B8 0 709A
09B9 00 0C000824
09BB 00 C400082A
09BD 00 E4000946
09BF 00 4C200952
09C1 00 74FF081E
09C3 0 7008
09C4 00 0C000824
09C6 00 C400082A
09C8 00 E4000947
09CA 00 4C20083E
09CC 0 30FF
09CD 00 64000803
09CF 00 64000840
09D1 0 C000
09D2 0 D04C
09D3 0 2947
09D4 0 084D
09D5 0 D04E
09D6 00 4C4009D8
09D8 00 0C000824
09DA 00 C400082A
09DC 0 E052
09DD 0 F052
09DE 00 4C180A48
09E0 0 C043
09E1 0 E046
09E2 00 4C1809F7
09E4 0 C040
09E5 00 4C1009F3
09E7 00 0C000824
09E9 00 C400082A
09EB 00 E4000949
09ED 00 4C200A0D
09EF 00 44000A48
09F1 0 0925
09F2 0 7004
09F3 0 C030
09F4 0 F033
09F5 00 4C9809D1
09F7 00 0C000824
09F9 00 C400082A
09FB 00 E4000949
09FD 00 4C200A0D
0A00 0 E028
0A01 00 4C180A06
0A03 00 44000A48
0A05 0 0B31
0A06 0 C01D
0A07 0 E022
0A08 00 4C180A0D
0A0A 00 44000A48
0A0C 0 0838
0A0D 00 0C000824
LD RSRAE
A L RSQAM
STO RSRAE
STO RSACR
EOR L RSAAH
BSC L RSACQ,Z
MDX X2 -1
MDX RSACS
XIO L RSQAF
LD L RSQAL
AND L RSRAG
BSC L RSACU,Z
RSADA MDX L RSFAB,-1
MDX RSCCQ
XIO L RSQAF
LD L RSQAL
AND L RSRAM
BSC L RSABI,Z
RSEXI WAIT -1
LDX L RSDKS
RSCCQ LDX L RSABH
RSCCA DC 0
STO RSSAA
STS RSCCE
XIO RSSAC
STO RSSAD
BOSC L NEXT
XIO L RSQAF
LD L RSQAL
AND RSSAD
EOR RSSAP
BSC L RSDDK,+
LD RSSAD
AND RSSAE
BSC L RSCCB,+
LD RSSAF
BSC L RSCCG,-
XIO L RSQAF
LD L RSQAL
AND L RSRAX
BSC L RSCCD,Z
BSI L LOG
DC MES17
MDX RSCCB
LD RSSAD
EOR RSSAE
BSC I RSCCA,+
XIO L RSQAF
LD L RSQAL
AND L RSRAX
BSC L RSCCD,Z
LD RSSAD
AND RSSAI
BSC L RSCCC,+
BSI L LOG
DC MES18
RSCCC LD RSSAD
AND RSSAJ
BSC L RSCCD,+
BSI L LOG
DC MES19
RSCCD XIO L RSQAF
RETURN ADDR TO MAIN INE
SAVE A
STORE STATUS CARY+OF 0
SENSE ILSW FOR LEVEL ERROR
TEST FOR THE ILLEGAL SWITCH COMBINATION-SW 10 ON AND SW 12 OFF
BRANCH IF ILLEGAL
RESTORE STATUS OF ILSW
ISOLATE STGE PRT ERR R
TEST FOR STORAGE PROT VIOL
BYPASS PRINTOUT IF IN SP SW 10 TO BYPASS PRIN OUT
IF IN SP ROUTINE AN SP ERROR ONLY THEN RETU N TO MAINLINE
SW 10 TO BYPASS PRIN OUT
BYPASS PRINTOUT IF BRANCH LOAD ILSW FOR ERROR NTRUP ISOLATE PARITY ERROR
ERROR INT-PARITY
TEST FOR INVALID OP CODE
ISOLATE INV OP ERROR
ERROR INT-INV OP CODE
IF BIT SW 12 ON THEN STOR

CORE STORAGE FUNCTION TEST
LOW CORE TEST

0A0F 00 C40002A	LD L	RSQAL	LCT04100
0A11 0 E919	AND	RSQAK	LCT04110
0A12 00 4C8809D1	BSC I	RSCCA,+	LCT04120
0A14 0 C00F	LD	RSSAD	LCT04130
0A15 0 180C	SRA	12	LCT04140
0A16 0 E817	OR	RSSAN	LCT04150
0A17 0 0904	STO	RSCCH	LCT04160
0A18 0 C088	LD	RSCCA	LCT04170
0A19 0 1890	SRT	16	LCT04180
0A1A 0 C004	LD	RSSAA	LCT04190
0A1B 0 2000	RSCCE LDS	0	LCT04200
0A1C 0 3000	RSCCH WAIT		LCT04210
0A1D 00 4C8009D1	BSC I	RSCCA	LCT04220
* STORAGE AREAS FOR ERROR ROUTINES			
0A1F 0 0000	RSSAA DC	0	LCT04230
0A20 0 0002	BSS E	2	LCT04240
0A22 0 0000	RSSAC DC	/0000	LCT04250
0A23 0 0300	DC	/0300	LCT04260
0A24 0 0000	RSSAD DC	0	LCT04270
0A25 0 FFFF	RSSAF DC	-1	LCT04280
0A26 0 FFFF	RSSAG DC	-1	LCT04290
0A27 0 0002	RSSAH DC	2	LCT04300
0A28 0 2000	RSSAE DC	/2000	LCT04310
0A29 0 4000	RSSAJ DC	/4000	LCT04320
0A2A 0 8000	RSSAJ DC	/8000	LCT04330
0A2B 0 0009	RSSAK DC	/0008	LCT04340
0A2C 0 000E	RSSAL DC	14	LCT04350
0A2D 0 0001	RSSAM DC	1	LCT04360
0A2E 0 3000	RSSAN DC	/3000	LCT04370
0A2F 0 0028	RSSAO DC	/0028	LCT04380
0A30 0 0020	RSSAP DC	/0020	LCT04390
0A31 0 5555	RSSAQ DC	/5555	LCT04400
* ERROR ROUTINE TO SERVICE NON-INTERRUPT ERR RS			
0A32 0 0000	RSDDD DC	0	LCT04410
0A33 0 2810	STS	RSDDJ	LCT04420
0A34 0 C0FD	RSDDX LD	RSDDD	LCT04430
0A35 0 90F6	S	RSSAL	LCT04440
0A36 0 1890	SRT	16	LCT04450
0A37 0 C0FA	LD	RSDDD	LCT04460
0A38 0 80F4	A	RSSAM	LCT04470
0A39 0 00F8	STO	RSDDD	LCT04480
0A3A 00 0C000824	XIO L	RSQAF	LCT04490
0A3C 00 C400082A	LD L	RSQAL	LCT04500
0A3E 00 E4000A2B	AND L	RSSAK	LCT04510
0A40 00 4CA00A32	BSC I	RSDDD,Z	LCT04520
0A42 00 C40008D3	LD L	RSQAN	LCT04530
0A44 0 2000	RSEDJ LDS	0	LCT04540
0A45 0 3000	WAIT		LCT04550
0A46 00 4C800A32	BSC I	RSDDD	LCT04560
0A48 0 C0E8	RSDDK LD	RSSAQ	LCT04570
0A49 00 4C400803	BOSEC L	RSDDK	LCT04580
* LOG ROUTINE			
0A4B 0 0000	LOG DC	0	LCT04590
0A4C 0 6818	LOG01 STX	3 LOG06+1	LCT04600
0A4D 00 0C000824	XIO L	RSQAF	LCT04610
0A4F 00 C400082A	LD L	RSQAL	LCT04620
0A51 00 4C100A6D	BSC L	TWRTR,-	LCT04630
0A53 00 C4800A4B	LD I	LOG	LCT04640
0A55 0 D052	STO	PRWRT	LCT04650

CORE STORAGE FUNCTION TEST
LOW CORE TEST

0A56 0 084D	LOG02 XIO	PRSNS	CHECK PRINTER READY	LCT04780
0A57 00 4C040A5D	BSC L	LOG03,E	BRANCH IF NOT READY	LCT04790
0A59 0 1901	SRA	1		LCT04800
0A5A 00 4C040A5F	BSC L	LOG04,E	BRANCH IF BUSY	LCT04810
0A5C 0 7004	MDX	LOG05	READY AND NOT BUSY	LCT04820
0A5D 0 300A	LOG03 WAIT	10	NOT READY	LCT04830
0A5E 0 70F7	MDX	LOG02	CHECK AGAIN	LCT04840
0A5F 0 300B	LOG04 WAIT	11	BUSY	LCT04850
0A60 0 70F5	MDX	LOG02	CHECK AGAIN	LCT04860
0A61 0 0846	LOG05 XIO	PRWRT	OUTPUT MESSAGE	LCT04870
0A62 0 0843	XIO	PRSN	CHECK FOR OP COMPLT	LCT04880
0A63 0 1002	SLA	2		LCT04890
0A64 0 4810	BSC	-		LCT04900
0A65 0 70FC	MDX	*-4		LCT04910
0A66 0 093D	XIO	PRSNS	RESET DSW	LCT04920
* PRINTING COMPLETE				LCT04930
0A67 00 67000000	LOG06 LDX	L3 0	RESTORE IX 3	LCT04940
0A69 00 74010A4B	MDX	L LOG,1	BUMP RETURN	LCT04950
0A6B 00 4C800A4B	BSC I	LOG	RETURN TO USER	LCT04960
0A6D 0 1010	TWRTR SLA	16		LCT04970
0A6E 0 D032	STO	WRDSW		LCT04980
0A6F 0 083A	XIO	TWSNS	CHECK IF TYPEWRITER	LCT04990
0A70 0 1005	SLA	5	READY	LCT05000
0A71 0 180F	SRA	15		LCT05010
0A72 00 4C180A76	BSC L	TWR01,+		LCT05020
0A74 0 300C	WAIT	12	NOT READY	LCT05030
0A75 0 70F9	MDX	TWRTR+2		LCT05040
0A76 0 C028	TWR01 LD	TWRTO	CARRIAGE RETURN AND	LCT05050
0A77 0 D02A	STO	IOARA	LINE SPACE TO IO ARA	LCT05060
0A78 0 0833	XIO	TWRTR	CARG RETURN/LINE SP	LCT05070
0A79 0 0830	XIO	TWSNS	HANG TILL NOT BUSY	LCT05080
0A7A 0 180B	SRA	11		LCT05090
0A7B 0 4804	BSC	E		LCT05100
0A7C 0 70FC	MDX	*-4		LCT05110
0A7D 0 6301	LDX	3 1	BYPASS 1443 WORD COU T	LCT05120
0A7E 00 C4800A4B	LD I	LOG	GET MESSAGE ADDRESS	LCT05130
0A80 0 0001	STO	TWR02+1		LCT05140
0A81 00 C7000000	TWR02 LD	L3 0	GET WORD TO PRINT	LCT05150
0A83 00 D4000ADE	STO L	CODWD	SET IN CONVERSION RT	LCT05160
0A85 0 F01A	EOR	TWRTR	CHECK IF TERMINATOR	LCT05170
0A86 00 4C180A67	BSC L	LOG06,+	BRANCH IF TERMINATOR	LCT05180
0A88 00 44000AAE	BSI L	CODCV	GO CONVERT 43 TO TH SRC	LCT05190
0A8A 00 C4000ADE	LD L	CODWD		LCT05200
0A8C 0 D015	STO	IOARA		LCT05210
0A8D 0 081E	XIDWR XIO	TWRTR	WRITE CHARACTER	LCT05220

CORE STORAGE FUNCTION TEST
LOW CORE TEST

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0A8F 0 081B      XIOSN XIO  TWSNS  HANG ON BUSY      LCT05460
0A8F 0 180B      SRA      11      LCT05470
0A90 0 4804      BSC      E       LCT05480
0A91 0 70FC      MDX      XIOSN  BUSY      LCT05490
* * * * *
* * * * *
0A92 0 000E      LD       WRDSW  GET 1/2 WORD SWITCH  LCT05520
0A93 0 4804      BSC      E       LCT05530
0A94 0 7006      MDX      TWRO3  GO SET UP NEXT WORD  LCT05540
* * * * *
* * * * *
0A95 0 000C      LD       IOARA  LCT05550
0A96 0 1008      SLA      8       LCT05560
0A97 0 000A      STO      IOARA  LCT05570
0A98 0 74010AA1 MDX L WRDSW,1 BUMP WORD SWITCH  LCT05580
0A9A 0 70F2      MDX      XIOWR  GO WRITE 2ND 1/2 WD  LCT05590
* * * * *
* * * * *
0A9B 0 7301      TWRO3 MDX 3 1   NEXT WORD INDEX  LCT05600
0A9C 0 74010AA1 MDX L WRDSW,1 BUMP WORD SWITCH  LCT05610
0A9E 0 70E2      MDX      TWRO2  GO GET NEXT WORD  LCT05620
* * * * *
* * * * *
0A9F 0 3103      TWRT0 DC   /8103  LINE SP/CARRAIGE RTN  LCT05630
0AAC 0 FFFF      TWRT1 DC   /FFFF  TERMINATOR           LCT05640
0AA1 0 0000      WRDSW DC   0     1/2 WORD SWITCH     LCT05650
0AA2 0 0000      IOARA DC   0     OUTPUT AREA         LCT05660
* * * * *
* * * * *
0AA4 0 0000      BSS E 0
* * * * *
* * * * *
0AA4 0 0000      PRSNS DC   /0000  PRINTER SENSE IOCC  LCT05670
0AA5 0 3701      DC       /3701  LCT05680
0AA6 0 0000      PRSN DC   0     NON RESET SENSE     LCT05690
0AA7 0 3700      DC       /3700  LCT05700
0AA8 0 0000      PRWRT DC   /0000  PRINTER WRITE IOCC  LCT05710
0AA9 0 3500      DC       /3500  LCT05720
0AAA 0 0000      TWSNS DC   /0000  TYPEWTR SENSE IOCC  LCT05730
0AAB 0 0F01      DC       /0F01  DSW RESET           PM01 LCT05740
0AAC 0 0AA2      TWWRT DC   IOARA  TYPEWTR WRITE IOCC  LCT05750
0AAD 0 0900      DC       /0900  WR TYPEWRITER       PM02 LCT05760
* * * * *
* * * * *
*****
* * * * *
* * * * *
1443 CODE TO 1816/1053 *
* * * * *
CODE CONVERSION ROUTINE *
* * * * *
*****
0AAE 0 0000      CODCV DC   0     SE
0AAF 0 6927      STX 1 CODC4+1  SAVE INDEX REGS
0AB0 0 6A28      STX 2 CODC4+3
0AB1 0 6829      STX 3 CODC4+5
* * * * *
* * * * *
0AB2 0 1010      SLA      16     CLEAR LEFT HALF WORD  LCT06010
0AB3 0 0028      STO     LHIND  *INDICATOR          LCT06020
0AB4 0 6300      LDX     3 0
* * * * *
* * * * *
0AB5 0 0228      CODC1 LD   CODWD  GET WORD TO CONVERT  LCT06030
0AB6 0 1890      SRT     16     SET IN Q             LCT06040
0AB7 0 0027      LD     LHIND  LCT06050
0AB8 0 4820      BSC     Z     SKIP IF LEFT HALF  LCT06060
0AB9 0 1088      SLT     8     POSITION RIGHT HALF  LCT06070
* * * * *
* * * * *
0ABA 0 1010      SLA      16     ZONE TO ACCUM       LCT06080
0ABB 0 1084      SLT     4     LCT06090
0ABC 0 0023      STO     COD00  LCT06100
LCT06110
LCT06120
LCT06130

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CORE STORAGE FUNCTION TEST
LOW CORE TEST

```

0ABD 00 65800AE0      LDX 11 COD00  IX 1 = ZONE      LCT06140
* * * * *
0ABF 0 1010      SLA      16     LCT06150
0ACO 0 1084      SLT     4     DIGIT TO ACCUM    LCT06160
0AC1 0 001E      STO     COD00  LCT06170
0AC2 00 66800AE0      LDX 12 COD00  IX 2 = DIGIT     LCT06180
* * * * *
* * * * *
0AC4 00 05000AE3      LD     L1 ZONE  GET ZONE TABLE ADDRS  LCT06190
0AC6 0 0001      STO     CODC2+1 SET IN CONVERSION WD  LCT06200
* * * * *
* * * * *
0AC7 00 06000000      CODC2 LD   L2 0   GET CONVERTED CODE  LCT06210
0AC9 00 07000AE1      STO     L3 COD01 LCT06220
* * * * *
* * * * *
0ACB 0 0013      LD     LHIND  LCT06230
0ACC 00 4C200AD2      BSC L CODC3,Z BRNCH IF RIGHT HALF  LCT06240
0ACE 00 74010ADF      MDX L LHIND,1 LCT06250
0ADD 0 7301      MDX 3 1     LCT06260
0AD1 0 70F3      MDX      CODC1  GO CONVERT RIGHT HLF  LCT06270
* * * * *
* * * * *
0AD2 0 000E      CODC3 LD   COD01  PACK CONVERTED CODES  LCT06280
0AD3 0 1008      SLA      8     LCT06290
0AD4 0 E80D      OR      COD02  LCT06300
0AD5 0 0008      STO     CODWD  LCT06310
* * * * *
* * * * *
0AD6 00 65000000      CODC4 LDX L1 0   RESTORE INDEX REGS  LCT06320
0AD8 00 66000000      LDX L2 0     LCT06330
0ADA 00 67000000      LDX L3 0     LCT06340
* * * * *
* * * * *
0ADC 00 4C800AAE      BSC I CODCV  RETURN TO USER  SX  LCT06350
* * * * *
* * * * *
CONSTANTS
LCT06360
LCT06370
LCT06380
LCT06390
LCT06400
LCT06410
LCT06420
LCT06430
LCT06440
LCT06450
LCT06460
LCT06470
LCT06480
LCT06490
LCT06500
LCT06510
LCT06520
LCT06530
LCT06540
LCT06550
LCT06560
LCT06570
LCT06580
LCT06590
LCT06600
LCT06610
LCT06620
LCT06630
LCT06640
LCT06650
LCT06660
LCT06670
LCT06680
LCT06690
LCT06700
LCT06710
LCT06720
LCT06730
LCT06740
LCT06750
LCT06760
LCT06770
LCT06780
LCT06790
LCT06800
LCT06810

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CORE STORAGE FUNCTION TEST
LOW CORE TEST

OAFB 0	00A2	DC	/00A2	Z
O AFC 0	0021	DC	/0021	SPACE
OAFD 0	0000	ZONE2 DC	0	
OAFE 0	007E	DC	/007E	J
OAFF 0	005A	DC	/005A	K
OB00 0	005E	DC	/005E	L
OB01 0	0072	DC	/0072	M
OB02 0	0076	DC	/0076	N
OB03 0	0052	DC	/0052	O
OB04 0	0056	DC	/0056	P
OB05 0	0066	DC	/0066	Q
OB06 0	0062	DC	/0062	R
OB07 0	0000	ZONE3 DC	0	
OB08 0	003E	DC	/003E	A
OB09 0	001A	DC	/001A	B
OB0A 0	001E	DC	/001E	C
OB0B 0	0032	DC	/0032	D
OB0C 0	0036	DC	/0036	E
OB0D 0	0012	DC	/0012	F
OB0E 0	0016	DC	/0016	G
OB0F 0	0026	DC	/0026	H
OB10 0	0022	DC	/0022	I
OB11 0	0086	DC	/0086	O ERROR
OB12 0	0000	DC	/0000	PERIOD
OB13 0	000A	* MES15 DC	10	WD CT
OB14 0	2435	DC	/2435	ME
OB15 0	2426	DC	/2426	MD
OB16 0	2918	DC	/2918	RY
OB17 0	0013	DC	/0013	T
OB18 0	3512	DC	/3512	ES
OB19 0	1300	DC	/1300	T
OB1A 0	2326	DC	/2326	LO
OB1B 0	1600	DC	/1600	W
OB1C 0	3326	DC	/3326	CO
OB1D 0	2935	DC	/2935	RE
OB1E 0	FFFF	DC	/FFFF	TERM
OB1F 0	0004	* MES16 DC	4	WDCT
OB20 0	2729	DC	/2729	PR
OB21 0	2637	DC	/2637	JG
OB22 0	0035	DC	/0035	E
OB23 0	2534	DC	/2534	ND
OB24 0	FFFF	DC	/FFFF	TERM
OB25 0	000A	* MES17 DC	10	WD CT
OB26 0	3529	DC	/3529	ER
OB27 0	2926	DC	/2926	RO
OB28 0	2900	DC	/2900	R
OB29 0	3925	DC	/3925	IN
OB2A 0	1300	DC	/1300	T
OB2B 0	1213	DC	/1213	ST
OB2C 0	2629	DC	/2629	OR
OB2D 0	3700	DC	/3700	G
OB2E 0	2729	DC	/2729	PR
OB2F 0	2613	DC	/2613	OT
OB30 0	FFFF	DC	/FFFF	TERM
OB31 0	0008	* MES18 DC	8	WD CT
OB32 0	3529	DC	/3529	ER
OB33 0	2926	DC	/2926	RO
OB34 0	2900	DC	/2900	R
OB35 0	3925	DC	/3925	IN
OB36 0	1300	DC	/1300	T
OB37 0	2731	DC	/2731	PA
OB38 0	2939	DC	/2939	RI
OB39 0	1318	DC	/1318	TY
OB3A 0	FFFF	DC	/FFFF	TERM

LCT06820
LCT06830
LCT06840
LCT06850
LCT06860
LCT06870
LCT06880
LCT06890
LCT06900
LCT06910
LCT06920
LCT06930
LCT06940
LCT06950
LCT06960
LCT06970
LCT06980
LCT06990
LCT07000
LCT07010
LCT07020
LCT07030
LCT07040
LCT07050
LCT07060
LCT07070
LCT07080
LCT07090
LCT07100
LCT07110
LCT07120
LCT07130
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LCT07150
LCT07160
LCT07170
LCT07180
LCT07190
LCT07200
LCT07210
LCT07220
LCT07230
LCT07240
LCT07250
LCT07260
LCT07270
LCT07280
LCT07290
LCT07300
LCT07310
LCT07320
LCT07330
LCT07340
LCT07350
LCT07360
LCT07370
LCT07380
LCT07390
LCT07400
LCT07410
LCT07420
LCT07430
LCT07440
LCT07450
LCT07460
LCT07470
LCT07480
LCT07490

CORE STORAGE FUNCTION TEST
LOW CORE TEST

OB3B 0	000C	* MES19 DC	12	WD CT
OB3C 0	3529	DC	/3529	ER
OB3D 0	2926	DC	/2926	RO
OB3E 0	2900	DC	/2900	R
OB3F 0	3925	DC	/3925	IN
OB40 0	1300	DC	/1300	T
OB41 0	3925	DC	/3925	IN
OB42 0	1500	DC	/1500	V
OB43 0	2627	DC	/2627	OP
OB44 0	0033	DC	/0033	C
OB45 0	2634	DC	/2634	OD
OB46 0	3500	DC	/3500	E
OB47 0	FFFF	DC	/FFFF	TERM
OB48 0	0002	* MES20 DC	2	WD CT
OB49 0	3529	DC	/3529	ER
OB4A 0	0001	DC	/0001	1
OB4B 0	FFFF	DC	/FFFF	TERM
OB4C 0	0002	* MES21 DC	2	WD CT
OB4D 0	3529	DC	/3529	ER
OB4E 0	0002	DC	/0002	2
OB4F 0	FFFF	DC	/FFFF	TERM
OB50 0	0002	* MES22 DC	2	WD CT
OB51 0	3529	DC	/3529	ER
OB52 0	0003	DC	/0003	3
OB53 0	FFFF	DC	/FFFF	TERM
OB54 0	0002	* MES23 DC	2	WD CT
OB55 0	3529	DC	/3529	ER
OB56 0	0004	DC	/0004	4
OB57 0	FFFF	DC	/FFFF	TERM
OB58 0	0002	* MES24 DC	2	WD CT
OB59 0	3529	DC	/3529	ER
OB5A 0	0005	DC	/0005	5
OB5B 0	FFFF	DC	/FFFF	TERM
OB5C 0	0002	* MES25 DC	2	WD CT
OB5D 0	3529	DC	/3529	ER
OB5E 0	0006	DC	/0006	6
OB5F 0	FFFF	DC	/FFFF	TERM
OB60 0	0000	* RSEND DC	0	
OB61 0	0000	DC	0	
OB62 0	0000	DC	0	
OB64 0	0900	END	RSDKR	

LCT07500
LCT07510
LCT07520
LCT07530
LCT07540
LCT07550
LCT07560
LCT07570
LCT07580
LCT07590
LCT07600
LCT07610
LCT07620
LCT07630
LCT07640
LCT07650
LCT07660
LCT07670
LCT07680
LCT07690
LCT07700
LCT07710
LCT07720
LCT07730
LCT07740
LCT07750
LCT07760
LCT07770
LCT07780
LCT07790
LCT07800
LCT07810
LCT07820
LCT07830
LCT07840
LCT07850
LCT07860
LCT07870
LCT07880
LCT07890
LCT07900
LCT07910
LCT07920
LCT07930
LCT07940
LCT07950
LCT07960
LCT07970
LCT07980

CORE STORAGE FUNCTION TEST
LOW CORE TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
C0DCV	0AAF	0A88,0ADC
C0DC1	0AB5	0AD1
C0DC2	0AC7	0AC6
C0DC3	0AD2	0ACC
C0DC4	0AD6	0AAF,0AB0,0AB1
C0DWD	0ADE	0A83,0A8A,0AB5,0AD5
C0D00	0AF0	0ARC,0ABD,0AC1,0AC2
C0D01	0AE1	0AC9,0AD2
C0D02	0AE2	0AD4
IDARA	0AA2	0A77,0ARC,0A95,0A97,0AAC
LHIND	0ADF	0AB3,0AB7,0ACB,0ACE
LOG	0A4B	09EF,0A03,0A0A,0A53,0A69,0A6B,0A7E
LOG01	0A4C	
LOG02	0A56	0A5E,0A60
LOG03	0A50	0A57
LOG04	0A5F	0A5A
LOG05	0A61	0A5C
LOG06	0A67	0A4C,0A86
MES15	0913	
MES16	091F	
MES17	0825	09F1
MES18	0831	0A05
MES19	0838	0A0C
MES20	0848	
MES21	084C	
MES22	0850	
MES23	0854	
MES24	0858	
MES25	085C	
NEXT	09D8	09D6
PRSN	0AA6	0A62
PRSNS	0AA4	0A56,0A66
PRWRT	0AA8	0A55,0A61
RSAB	0813	080F
RSAC	0819	0813
RSAD	0819	0811
RSAAE	091A	0806,0808
RSAAH	091B	0847,0869,08C2,0904,0933,0983,0983
RSAAK	091C	0814,0830,094C
RSAAI	081F	082D
RSAAJ	0822	0800,0803
RSABA	082D	0817
RSABB	0941	086F
RSABC	0843	0848
RSABD	084C	0848
RSABE	084E	085C,0866,086D
RSABF	0861	0852
RSABG	086E	086A
RSABH	0840	0876,09CF
RSABI	083E	0831,09CA
RSABJ	0892	0883
RSABK	0883	08A4
RSABL	089C	08AE,0889
RSABM	09C1	088D
RSABN	0878	0890,0898,08C8
RSABO	08C9	08C4
RSABP	0979	09CA
RSABQ	0990	09C0
RSABR	0978	08D1
RSACA	0901	08FC
RSACB	09F7	09CA
RSACD	0903	0900
RSACE	0916	0912
RSACF	0926	0915,0917
RSACG	0910	092A

CORF STORAGE FUNCTION TEST
LOW CORE TEST

RSACH	090E	0921,0930
RSACJ	08DC	08D3,093E
RSACK	09E2	0935
RSACL	090D	0938
RSACM	0977	0968
RSACN	095B	0972,097C,0985
RSACO	095F	0956,0982
RSACP	09A7	0998
RSACQ	098F	09A2,09AC,0985
RSACR	0990	098E,0982
RSACS	0953	0988
RSACU	0952	094E,09BF
RSACV	094C	0940
RSACW	0939	08E5
RSACX	08E6	08E4
RSADA	09C1	0950
RSADR	090B	0906
RSCCA	09D1	0827,09F5,0A12,0A18,0A1D
RSCCB	09F7	09E2,09F2
RSCCC	0A06	0A01
RSCCD	0A0D	09ED,09FD,0A08
RSCCE	0A1B	09D3
RSCCG	09F3	09E5
RSCCH	0A1C	0A17
RSCCQ	09CF	09C3
RSDD	0A32	085E,0885,0880,0923,0974,09A4,0A34,0A37,0A39,0A40,0A46,0A33,09DE
RSDDJ	0A44	
RSDDK	0A48	
RSDDX	0A34	
RSDKR	0800	0863
RSDKS	0803	0822,09CD,0A49
RSEND	0860	095F,0990
RSEXI	09CC	
RSFAA	081D	083E
RSFAB	081E	083F,09C1
RSQAC	0826	0841,084C,0879,08F4,0908,0953,0988
RSQAD	0827	0835
RSQAE	0928	0843,0844,0845,084E,084F,0851,0868
RSQAF	0824	0856,0861,0870,088A,0892,08A8,08B3,08C8,0918,0928,0939,096C,0977,099C,09A7,09B9,09C4,09D8,09E7,09F7,0A0D,0A3A,0A4D
RSQAH	08D6	0A7B,087C,087F,0881,089D,08A1,08C1,08C6,08E6,08E7,08EA,08EB,08ED,08EE,08F1,08F2
RSQAI	08D7	087E
RSQAJ	09D8	089A
RSQAK	08D9	089B,089C,089F,08A3,088B,089F
RSQAL	082A	0924,0858,0862,0872,088C,0894,08AA,08B5,08CD,091D,092D,093B,096E,0979,099E,09A9,09BB,09C6,09DA,09E9,09F9,0A0F,0A3C,0A4F
RSQAM	08DA	08C7,097F,09AF
RSQAN	09DB	0854,0888,08A6,0919,096A,099A,0A42
RSQAO	0825	0834
RSQAP	0829	0833
RSQAQ	08D4	08E0
RSQAR	08D5	08E1,08E2
RSQAU	082B	0838
RSQAV	082C	083B
RSRAA	0941	08F6,08F7,08FE,0901,0903,0908,090D,0910,0926,0932
RSRAB	0942	08F9,08FB
RSRAC	0943	08E8,08EF,0914,0916,095B,0967
RSRAF	0944	0955,095C,0960,0963,0965,097E,0981,098D,0991,0994,0996,09AE,09B1
RSRAF	0945	0962,0993
RSRAG	0946	0974,08CF,093D,098D
RSRAH	0947	09C8
RSRAI	0948	085A,0864,088E,0896,08AC,08B7,091F,092F,0970,097B,09A0,09AB

CORE STORAGE FUNCTION TEST
LOW CORE TEST

RSRAJ	094A	090E
RSRAK	094B	090F,0928
RSRAX	0949	09E8,09FB
RSSAA	0A1F	09D2,0A1A
RSSAC	0A22	09D4
RSSAD	0A24	09D5,09E0,09F3,09FF,0A06,0A14
RSSAE	0A28	09E1,09F4
RSSAF	0A25	0959,0989,09E4
RSSAG	0A26	0987
RSSAH	0A27	0957
RSSAI	0A29	0A00
RSSAJ	0A2A	0A07
RSSAK	0A23	0A11,0A3E
RSSAL	0A2C	0A35
RSSAM	0A2D	0A38
RSSAN	0A2E	0A16
RSSAO	0A2F	09DC
RSSAP	0A30	09DD
RSSAQ	0A31	0A48
TWRTR	0A6D	0A51,0A75
TWRTO	0A9F	0A76
TWRT1	0AA0	0A85
TWRO1	0A76	0A72
TWRO2	0A81	0A80,0A9E
TWRO3	0A9B	0A94
TWSNS	0AAA	0839,0A6F,0A79,0A8E
TWVRT	0AAC	083C,0A78,0A8D
WRDSW	0AA1	0A6E,0A92,0A98,0A9C
XIOSN	0A8E	0A91
XIOWR	0A8D	0A9A
ZONE	0AE3	0AC4
ZONEN	0AE7	0AE3
ZONE1	0AF2	0AE4
ZONE2	0AFD	0AE5
ZONE3	0B07	0AE6

METER TEST

TABLE OF CONTENTS

1. PURPOSE 01A

2. PREREQUISITES 01A

 2.1 PROGRAM

 2.2 EQUIPMENT

3. USE PROCEDURE 01A

 3.1 LOADING

 3.2 OPERATION

 3.2.1 SYSTEMS I/O CONFIGURATION

 3.2.2 I/O READY

 3.2.3 C.E. METER TEST

 3.2.4 CUSTOMER METER TEST

 3.2.5 CONTROL CIRCUITRY

 3.3 WAITS

 3.4 TERMINATIONS

4. PRINTOUTS (NONE)

5. COMMENTS (METHOD OF TEST) G2A

6. APPENDIX (NONE)

METER TEST

1. PURPOSE

- A. TO CHECK THE ACCURACY OF ALL OF THE USE METERS.
- B. WHEN THE 1131 USE METER IS SWITCHED TO C.E. MODE, ONLY THE C.E. METER ADVANCES.

2. PREREQUISITES

2.1 PROGRAM

THIS PROGRAM DOES NOT RUN UNDER CONTROL OF THE 1130 DIAGNOSTIC MONITOR. IT IS SELF LOADING. (USES THE BASIC DIAGNOSTIC LOADER)

2.2 EQUIPMENT

CUSTOMER ENGINEER USE METER KEY.

3. USE PROCEDURE

THE OPERATING PROCEDURE CONSISTS OF THE FOLLOWING STEPS.

- 1. RECORD ALL METER READINGS
- 2. LOAD THE PROGRAM
- 3. ENTER SYSTEM I/O CONFIGURATION IN THE CONSOLE ENTRY SWITCHES. (WAIT1)
- 4. SET THE NUMBER OF 72 SECOND LOOPS DESIRED. (WAIT2)
- 5. CHECK METERS WHILE IN C.E. MODE. (THIS SECTION IS OPTIONAL)
- 6. CHECK THE CUSTOMER METERS
- 7. COMPUTE THE ELAPSED TIME. (BY HAND)
- 8. CHECK THE METER CONTROL CIRCUITS.

3.1 LOADING

- 1. RECORD THE READINGS ON ALL OF THE CUSTOMER METERS. THE CUSTOMER M MUST BE GIVEN CREDIT FOR THIS TEST TIME.
- 2. PUT THE 1131 METER IN C.E. MODE.
- 3. PLACE CARDS/PAPER TAPE IN READER.
- 4. PUT READER IN READY CONDITION
- 5. PRESS THE 1131 RESET KEY
- 6. PRESS THE 1131 PROGRAM LOAD KEY.

NOTE
IF THE PROGRAM LOADED CORRECTLY, IT WILL STOP AT WAIT 1. (LOC 0208)

3.2 OPERATION

THE SYSTEM I/O CONFIGURATION MUST NOW BE SET IN THE CONSOLE ENTRY SWITCHES. USE THE FOLLOWING FORMAT.

- BIT 13 ON = SYSTEM HAS 1132
- BIT 14 ON = SYSTEM HAS 1442
- BIT 15 ON = SYSTEM HAS DISK STORAGE.

FOR EXAMPLE, IF A SYSTEM HAS ALL THREE OF THE I/O DEVICES, ALL THREE BIT SWITCHES WOULD BE TURNED ON. PRESS 1131 START BUTTON. PROGRAM WILL GO TO WAIT 2. (LOC 0216)

3.2.2 MAKE THE I/O UNITS READY:

- 1442- PLACE A FEW CARDS IN THE FEED HOPPER AND PRESS THE 1442 START KEY. THE 1442 READY LAMP SHOULD GLOW.
- 1132 - TURN ON THE POWER SWITCH, AND PRESS THE 1132 START KEY. THE 1132 READY LAMP SHOULD GLOW.

METER TEST

3.2.3 TO CHECK C.F. MODE (THIS SECTION IS OPTIONAL)

1. SET THE CONSOLE ENTRY SWITCHES TO INDICATE THE NUMBER OF 72 SECOND LOOPS THAT YOU WISH TO MAKE. IF ONE LOOP IS DESIRED, TURN ON BIT 15. IF TWO LOOPS ARE DESIRED, TURN ON BIT 14. ETC.
2. RECORD ALL METER READINGS.
3. PRESS 1131 START KEY.

NOTE

IF THE PROGRAM STOPS AT:

WAIT 3 (LOC.0225) THE 1442 IS NOT READY.
WAIT 4 (LOC.022A) THE 1132 IS NOT READY.
WAIT 6 (LOC.0237) THE DISK IS NOT READY.

4. PROGRAM WILL STOP AT WAIT 5 (LOC.0245) WHEN THE DESIRED DELAY IS COMPLETED. METER ACCURACY SHOULD BE PLUS OR MINUS XX.
5. C.E. METER SHOULD HAVE ADVANCED .02 HOURS FOR EACH LOOP RUN. THE CUSTOMER METERS SHOULD NOT HAVE MOVED.
6. TO REPEAT LOOP, PRESS START KEY.
7. SWITCH 1131 METER OFF OF CE MODE.

3.2.4 TO CHECK CUSTOMER METERS

1. SET THE CONSOLE ENTRY SWITCHES TO INDICATE THE NUMBER OF 72 SECOND LOOPS THAT YOU WISH TO MAKE. IF ONE LOOP IS DESIRED, TURN ON BIT 15. IF TWO LOOPS ARE DESIRED, TURN ON BIT 14. ETC.
2. RECORD ALL METER READINGS.
3. PRESS 1131 START KEY.

NOTE

IF THE PROGRAM STOPS AT:

WAIT 3 (LOC.0225) THE 1442 IS NOT READY.
WAIT 4 (LOC.022A) THE 1132 IS NOT READY.
WAIT 6 (LOC.0237) THE DISK IS NOT READY.

4. PROGRAM WILL STOP AT WAIT 5 (LOC.0245) WHEN THE DESIRED DELAY IS COMPLETED. METER ACCURACY SHOULD BE PLUS OR MINUS XX.
5. THE CUSTOMER METERS SHOULD HAVE ADVANCED .02 HOURS FOR EACH LOOP RUN. THE C.E. METER SHOULD NOT HAVE MOVED.
6. TO REPEAT LOOP, PRESS START KEY.

3.2.5 CONTROL CIRCUITRY CHECK

1. WHILE RUNNING THE PROGRAM IN A 72 SECOND DELAY LOOP.
 - A. THE 1132 METER SHOULD STOP IF THE 1132 CARRIAGE RESTORE OR CARRIAGE SPACE KEY IS PRESSED.
 - B. THE 1442 METER SHOULD STOP IF THE 1442 NPRO KEY IS PRESSED.
2. CHECK THAT NO METERS ARE MOVING WHILE PROGRAM IS AT WAIT 5.
3. WHENEVER THE 1131 METER IS TURNED ON, THERE IS A DELAY CIRCUIT THAT KEEPS THE METER RUNNING FOR A MINIMUM OF 400 MILLISECONDS. TO CHECK THIS CIRCUIT, SET THE 1131 MODE SWITCH TO SINGLE INSTRUCTION(SI). WHEN THE 1131 START KEY IS PRESSED, THE RUN LAMP SHOULD GLOW FOR AN INSTANT (400M.S.) IF TROUBLE IS SUSPECTED AN OSCILLOSCOPE SHOULD BE USED.

METER TEST

3.3 WAITS

- WAIT 1 (LOC 020B) SET THE I/O CONFIGURATION IN THE CONSOLE ENTRY SWITCHES. PRESS THE 1131 START BUTTON.
- WAIT 2 (LOC 0216) SET THE CONSOLE ENTRY SWITCHES TO INDICATE THE NUMBER OF 72 SECOND (.02 HOURS) LOOPS DESIRED. PRESS 1131 START BUTTON TO BEGIN TEST.
- WAIT 3 (LOC.0225) THE 1442 IS NOT READY. TO RESTART, PUT 1442 IN READY STATUS, AND START THE PROGRAM AT 'SENSE' (LOC 0217) (CONSOLE ENTRY SWITCHES SHOULD STILL HAVE NUMBER OF LOOPS DESIRED)
- WAIT 4 (LOC022A) THE 1132 IS NOT READY. TO RESTART, PUT 1132 IN READY STATUS, AND START THE PROGRAM AT 'SENSE' (LOC.0217). (CONSOLE ENTRY SWITCHES SHOULD STILL HAVE THE NUMBER OF LOOPS DESIRED.)
- WAIT 5 (LOC 0245) END OF TEST. PRESS 1131 START BUTTON TO REPEAT TEST.
- WAIT 6 (LOC 0237) THE DISK IS NOT READY. TO RESTART, PUT THE DISK IN 'READY' STATUS, AND START THE PROGRAM AT 'SENSE' (LOC.0217) (CONSOLE ENTRY SWITCHES SHOULD STILL HAVE THE NUMBER OF LOOPS DESIRED.)

3.4 TERMINATIONS

THE PROGRAM WILL STOP AT WAIT 5 (LOC.0245) WHEN THE TEST IS COMPLETED. TO REPEAT TEST, PRESS 1131 START BUTTON.

4. PRINTOUTS (NONE)

5. COMMENTS

THE TESTING METHOD IS ACCOMPLISHED ONE OF TWO WAYS.

1. IF THE SYSTEM IS EQUIPPED WITH DISK STORAGE, 7.2 SECONDS OF EACH 72 SECOND DELAY LOOP WILL BE USED TO ACCESS THE DISK CARRIAGE. THIS CHECKS THE CIRCUITRY TO THE 'USE METER' FROM THE 'SEEK' CIRCUITS. THE REMAINING 64.8 SECOND DELAY IS ACCOMPLISHED BY ADDITION IN THE ACCUMULATOR. 7.2 SECONDS = ONE DIVISION ON THE 'USE METER'.
2. IF THE SYSTEM IS NOT EQUIPPED WITH DISK STORAGE, THE ENTIRE 72 SECOND DELAY IS ACCOMPLISHED IN THE ACCUMULATOR.

METER TEST

```

028C      ARS
          ORG      500
*
*****
* INTERRUPT TRANSFER VECTORS *
*****
BEGIN LDX L1 INT1
      STX L1 /0009
      LDX L1 INT2
      STX L1 /000A
      LDX L1 INT4
      STX L1 /000C
*
*****
* CLEAR 1132 SCAN FIELD *
*****
      LDX 2 32
      LDX 1 7
      LD L DSWR1      SET ACC TO 0
      CLEAR STO 2      SET PRINT AREA TO 0
      MDX 2 1
      MDX 1 -1
      MDX CLEAR
      LD L HOME
      STO 2      SET LOC 39 TO 0001
*****
* READ THE CONSOLE ENTRY SWITCHES TO
* DETERMINE THE SYSTEM CONFIGURATION
*
      BIT 15= DISK
      BIT 14= 1442
      BIT 13= 1132
*****
WAIT1 WAIT 1      ENTER SYS CONF.
      XIO CESWS
      LD COUNT
      STO DISK1
      SRA 1
      STO SRP1
      SRA 1
      STO PRTR2
      LD DISK1
      BSC E
      MDX DISK
*
*****
* READ THE CONSOLE ENTRY SWITCHES
* START THE 1132 AND THE 1442 METERS
*****
WAIT2 WAIT 2      ENTER NO OF DLY LOOPS
SENSE XIO CESWS      SENSE CON ENTRY SWS
      LDX 13 COUNT      XR3= LOOP COUNT
      LD SRP1
      BSC E
      MDX SRP2      START 1442
      LD PRTR2
      BSC E
      MDX PRTR3      START 1132
      LD DISK1
      BSC E
      MDX TESTO
      MDX ADD1
      MDX SRP
      XIO SRP      START 1442.
      WAIT3 WAIT 3      NO RESP. FROM 1442
      BSC E      IS 1442 READY
      MDX WAIT3
      MDX SNS1
      PRTR3 XIO PRTR      START 1132.
      WAIT4 WAIT 4      NO RESP. FROM 1132

```

```

UMT00000
UMT00010
UMT00020
UMT00030
UMT00040
UMT00050
UMT00060
UMT00070
UMT00080
UMT00090
UMT00100
UMT00110
UMT00120
UMT00130
UMT00140
UMT00150
UMT00160
UMT00170
UMT00180
UMT00190
UMT00200
UMT00210
UMT00220
UMT00230
UMT00240
UMT00250
UMT00260
UMT00270
UMT00280
UMT00290
UMT00300
UMT00310
UMT00320
UMT00330
UMT00340
UMT00350
UMT00360
UMT00370
UMT00380
UMT00390
UMT00400
UMT00410
UMT00420
UMT00430
UMT00440
UMT00450
UMT00460
UMT00470
UMT00480
UMT00490
UMT00500
UMT00510
UMT00520
UMT00530
UMT00540
UMT00550
UMT00560
UMT00570
UMT00580
UMT00590
UMT00600
UMT00610
UMT00620
UMT00630
UMT00640
UMT00650
UMT00660
UMT00670

```

METER TEST

```

022B 0 084C      XIO PRTR1 STOP THE 1132 INTR
022C 0 70F3      MDX SNS2
*
*****
* SET DISK TO HOME *
*****
DISK XIO L DSWR1      IS DISK RDY
      SLA 2
      BSC L WAIT6,+2      IF NOT RDY GO TO WT6
      SLA 2
      BSC L WAIT2,+2      IS CARR HOME
      SEEK XIO L HOME      SEEK -1 CYL
      WAIT6 WAIT 6      DISK NOT READY
      SLA 4
      BSC -      IS CARR HOME
      MDX SEEK
      MDX WAIT2
*****
* METER TEST
* 72 SECOND DELAY USING ONLY THE CPU
*****
ADD1 LDX 1 72      CONSTANT
ADD2 LD NUM
ADD3 A HOME      ADD 1 TO ACCUM
      BSC Z
      MDX ADD3
      MDX 1 -1      MODIFY CONSTANT
      MDX ADD2
      MDX 3 -1      MODIFY LOOP COUNT
      MDX ADD1
      WAITS WAIT 5      END OF TEST
      BSC L SENSE
*
*****
* METER TEST
* 72 SECOND DELAY USING THE DISK AND THE CPU*
*****
TESTO XIO DLY1      SEEK+202 CYL
      WAIT
      XIO DLY2      SEEK-202 CYL
      WAIT
      XIO DLY1      SEEK+202 CYL
      WAIT
      XIO DLY2      SEEK-202 CYL
      WAIT
      XIO DLY3      SEEK+76 CYL
      WAIT
      XIO DLY4      SEEK-76 CYL
      WAIT
      LD DSWR1      CLEAR ACCUM
      LDX 1 60      CONSTANT
      ADD A HOME      ADD 1 TO ACCUM
      BSC Z
      MDX ADD
      MDX 1 -1      MODIFY CONSTANT
      MDX ADD
      MDX 3 -1      MODIFY LOOP COUNT
      MDX TESTO
      MDX WAITS
*
*****
* INTERRUPT SUBROUTINES *
*****
INT1 BSS 1      1132
      XIO L DSWR3      SENSE DSW
      BOSC I INT1
INT2 BSS 1      DISK
      XIO L DSWR1      SENSE DSW

```

```

UMT00680
UMT00690
UMT00700
UMT00710
UMT00720
UMT00730
UMT00740
UMT00750
UMT00760
UMT00770
UMT00780
UMT00790
UMT00800
UMT00810
UMT00820
UMT00830
UMT00840
UMT00850
UMT00860
UMT00870
UMT00880
UMT00890
UMT00900
UMT00910
UMT00920
UMT00930
UMT00940
UMT00950
UMT00960
UMT00970
UMT00980
UMT00990
UMT01000
UMT01010
UMT01020
UMT01030
UMT01040
UMT01050
UMT01060
UMT01070
UMT01080
UMT01090
UMT01100
UMT01110
UMT01120
UMT01130
UMT01140
UMT01150
UMT01160
UMT01170
UMT01180
UMT01190
UMT01200
UMT01210
UMT01220
UMT01230
UMT01240
UMT01250
UMT01260
UMT01270
UMT01280
UMT01290
UMT01300
UMT01310
UMT01320
UMT01330
UMT01340
UMT01350

```

METER TEST

```

0266 00 4CC00263      BOSC I INT2
0268 0001      INT4 BSS 1      1442
0269 00 0C000282      XIO L DSWR2      SENSE DSM
026B 00 4CC00268      BOSC I INT4
*
*****
* I/O CONTROL COMMANDS AND CONSTANTS *
*****
026E 0000      BSS E 0
026E 0 0C01      HOME DC /0001      IOCC TO SEEK HOME
026F 0 2404      DC /2404
0270 0 0000      DSWR1 DC /0000      IOCC TO SENSE AND
0271 0 2701      DC /2701      RESET DISK
0272 0 0286      CESWS DC COUNT      IOCC TO RD CE SWS
0273 0 3A00      DC /3A00
0274 0 0000      S4P DC /0000      IOCC TO START 1442
0275 0 1402      DC /1402      METER
0276 0 0000      PRTR DC /0000      IOCC TO START 1132
0277 0 3480      DC /3480      METER
0278 0 0000      PRTR1 DC /0000      IOCC TO STOP 1132
0279 0 3440      DC /3440      EMIT INTERRUPTS
027A 0 00CA      DLY1 DC /00CA      IOCC SEEK TO 202
027B 0 2400      DC /2400      FROM HOME
027C 0 00CA      DLY2 DC /00CA      IOCC SEEK TO HOME
027D 0 2404      DC /2404      FROM 202
027E 0 004C      DLY3 DC /004C      IOCC SEEK TO 076
027F 0 2400      DC /2400      FROM HOME
0280 0 004C      DLY4 DC /004C      IOCC SEEK TO HOME
0281 0 2404      DC /2404      FROM 076
0282 0 0000      DSWR2 DC /0000      IOCC TO SENSE AND
0283 0 1702      DC /1702      RESET 1442 DSM
0284 0 0000      DSWR3 DC /0000      IOCC TO SENSE AND
0285 0 3701      DC /3701      RESET 1132 DSM
0286 0 0000      COUNT DC /0000      CON ENTRY SW SETTING
0287 0 0000      SRP1 DC 0000      SYSTEM HAS 1442
0288 0 0000      PRTR2 DC 0000      SYSTEM HAS 1132
0289 0 0000      DISK1 DC 0000      SYSTEM HAS DISK
028A 0 1340      NUM DC /1340
028C 01F4      END BEGIN

```

```

UMT01360
UMT01370
UMT01380
UMT01390
UMT01400
UMT01410
UMT01420
UMT01430
UMT01440
UMT01450
UMT01460
UMT01470
UMT01480
UMT01490
UMT01500
UMT01510
UMT01520
UMT01530
UMT01540
UMT01550
UMT01560
UMT01570
UMT01580
UMT01590
UMT01600
UMT01610
UMT01620
UMT01630
UMT01640
UMT01650
UMT01660
UMT01670
UMT01680
UMT01690
UMT01700
UMT01710
UMT01720
UMT01730
UMT01740

```

METER TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
ADD	0256	0258,025A
ADD1	023C	0223,0244
ADD2	023D	0242
ADD3	023E	0240
BEGIN	01F4	028B
CESWS	0272	020C,0217
CLEAR	0204	0207
COUNT	0286	020D,0218,0272
DISK	022D	0215
DISK1	0289	020E,0213,0220
DLY1	027A	0248,024C
DLY2	027C	024A,024E
DLY3	027E	0250
DLY4	0280	0252
DSWR1	0270	0202,022D,0254,0264
DSWR2	0282	0269
DSWR3	0284	025F
HOME	026E	0208,0235,023E,0256
INT1	025E	01F4,0261
INT2	0263	01F8,0266
INT4	0268	01FC,026B
NUM	028A	023D
PRTR	0276	0229
PRTR1	0278	022B
PRTR2	0288	0212,021D
PRTR3	0229	021F
SEEK	0235	023A
SENSE	0217	0246
SNS1	021D	0228
SNS2	0220	022C
SRP	0274	0224
SRP1	0287	0210,021A
SRP2	0224	021C
TEST0	0248	0222,025C
WAIT1	020B	
WAIT2	0216	0233,023B
WAIT3	0225	0227
WAIT4	022A	
WAIT5	0245	025D
WAIT6	0237	0230

CORE STORAGE ADJUSTMENT TEST

CORE ADJUSTMENT TEST

TABLE OF CONTENTS

PARAGRAPH	PAGE
1. PURPOSE	01A
2. PREREQUISITES	01A
2.1 PROGRAM PREREQUISITES	
2.2 EQUIPMENT PREREQUISITES	
3. USE PROCEDURE	01A
4. PRINT OUTS (NONE)	
5. COMMENTS	01A
6. APPENDIX (NONE)	

CORE STORAGE ADJUSTMENT TEST

1. PURPOSE

THE CORE ADJUSTMENT PROGRAM LOADS CORE WITH THE BEST CORE PATTERN (BCP) SPECIFIED IN THE ENGINEERING SPECIFICATIONS FOR SJ-2 STORAGE. THIS ALLOWS ADJUSTMENT OF THE CORE VOLTAGES AS SPECIFIED IN THE 1130 MAINTENANCE MANUAL.

2. PREREQUISITES

2.1 PROGRAM PREREQUISITES

THE CORE ADJUSTMENT PROGRAM IS LOADED BY THE 1130 BASIC DIAGNOSTIC LOADER.

2.2 EQUIPMENT PREREQUISITES

- a. 1131 CPU
- b. 1442 OR 1054 READER.

3. USE PROCEDURE

3.1 PROGRAM LOADING

- 1. PLACE CARDS/PAPER TAPE IN READER.
- 2. MAKE READER READY.
- 3. PRESS THE 1131 RESET KEY.
- 4. PRESS THE 1131 PROGRAM LOAD KEY.
- 5. IF PROGRAM FAILS TO LOAD OR STOPS AT A WAIT BELOW LOCATION 012C, REFER TO BASIC LOADER DOCUMENTATION SECT. 3.2.

3.2 OPERATING PROCEDURE

- 1. PROGRAM WILL LOAD, RUN BRIEFLY, THEN STOP AT END-OF-PROGRAM WAIT 30FF AT LOCATION 0149.
- 2. REFER TO 1130 MAINTENANCE MANUAL SECT. 4 FOR CORE ADJUSTMENT PROCEDURES.
- 3. PROGRAM MAY BE RERUN BY PRESSING PROGRAM START WHILE AT END-OF-PROGRAM WAIT.

4. PRINT OUTS (NONE)

5. COMMENTS

THE CORE ADJUSTMENT PROGRAM LOADS THE BEST CORE PATTERN IN ALL LOCATIONS ABOVE 017C.

THE SIZE OF CORE IS AUTOMATICALLY DETERMINED BY THE PROGRAM.

THE CORE ADJUSTMENT PROGRAM SHOULD NOT BE EXECUTING WHILE THE CORE UNIT IS BEING ADJUSTED.

CORE ADJUSTMENT TEST

```

02BC          ABS          ADJ00000
              ORG          ADJ00010
              300          ADJ00020
              *           ADJ00030
012C 0 1010   START SLA 16   FIND CORE SIZE ADJ00040
012D 00 D4000000 STD L 0     ADJ00050
012F 0 C00A   LD          KON ADJ00060
0130 0 D00A   STC          SIZE ADJ00070
0131 00 D480013B AA STC I SIZE ADJ00080
0133 00 74000000 MDX L 0,0 ADJ00090
0135 0 7006   MDX          CONT ADJ00100
0136 0 1001   SLA          1 ADJ00110
0137 00 D400013B STO L SIZE ADJ00120
0139 0 70F7   MDX          AA ADJ00130
013A 0 1000   KON DC /1000 ADJ00140
013B 0 0000   SIZE DC 0 ADJ00150
013C 0 C0FE   CDNT LD SIZE ADJ00160
013D 00 4C28014B BSC L NEGN,+Z ADJ00170
013F 0 903C   S          LAST ADJ00180
0140 0 D001   STO SETX+1 ADJ00190
0141 00 66000000 SETX LDX L2 0 SET X2 = NO. LOCS TO ADJ00200
0143 00 6500017D LDX1 LDX L1 FIRST * PLACE DATA ADJ00210
0145 00 4400014E REPT BSI L PLACE SET A PATTERN ADJ00220
0147 0 72FF   MDX 2 -1 CK FOR DONE ALL CORE ADJ00230
0148 0 70FC   MDX REPT NO ADJ00240
0149 0 30FF   WAIT -1 DONE ALL CORE, END PROG ADJ00250
014A 0 70E1   MDX START ADJ00260
              *           ADJ00270
014B 00 66007E82 NEGN LDX L2 /7FFF-FIRST ADJ00280
014D 0 70F5   MDX LDX1 ADJ00290
              *           ADJ00300
014E 0 0000   PLACE DC 0 PLACE PATTERN SUBRT ADJ00310
014F 0 6925   STX 1 TLOC GET TEST LOC ADDR ADJ00320
0150 0 C024   LD TLOC ADJ00330
0151 0 1003   SLA 3 ADJ00340
0152 0 4828   BSC +Z SKIP IF X3 = 0 ADJ00350
0153 0 701B   MDX FX3 ADJ00360
0154 0 C020   LD TLOC ADJ00370
0155 0 E020   AND CON1 CON1 = /0F00 ADJ00380
0156 0 F020   EOR CON2 CON2 = /0100 ADJ00390
0157 00 4C18016D BSC L LD1S,+ BRNH IF X4X5X6X7 = 0001 ADJ00400
0159 0 C01B   LD TLOC ADJ00410
015A 0 E01D   AND CON3 CON3 = /0F80 ADJ00420
015B 0 F01D   EOR CON4 CON4 = /0780 ADJ00430
015C 00 4C18016D BSC L LD1S,+ BRNH IF X4X5X6X7X8 =01111 ADJ00440
015E 0 1810   LDZS SRA 16 ADJ00450
015F 00 D4800175 STO I TLOC ADJ00460
0161 0 C013   LD TLOC ADJ00470
0162 0 E017   AND CON5 CON5 = /0040 ADJ00480
0163 0 4818   3SC +- SKIP IF Y9 = 1 ADJ00490
0164 0 7005   MDX DONE ADJ00500
0165 00 C4800175 LD I TLOC ADJ00510
0167 0 F013   EOR CON6 CON6 = /FFFF ADJ00520
0168 00 D4800175 STO I TLOC ADJ00530
016A 0 7101   DONE MDX 1 1 ADJ00540
016B 00 4C80014E BSC I PLACE EXIT FROM SUBRT ADJ00550
016D 0 C00D   LD CON6 CON6 = /FFFF ADJ00560
016E 0 70F0   MDX LDZS+1 ADJ00570
016F 0 C005   FX3 LD TLOC ADJ00580
0170 0 E005   AND CON1 CON1 = /0F00 ADJ00590
0171 0 F004   EOR CON1 CON1 = /0F00 ADJ00600
0172 00 4C18015E BSC L LDZS,+ BR IF X4X5X6X7 = 1111 ADJ00610
0174 0 70F8   MDX LD1S ADJ00620
0175 0 0000   TLJC DC 0 ADJ00630
0176 0 0F00   CON1 DC /0F00 ADJ00640
0177 0 0100   CON2 DC /0100 ADJ00650
0178 0 0F80   CON3 DC /0F80 ADJ00660
0179 0 0780   CON4 DC /0780 ADJ00670
017A 0 0040   CON5 DC /0040

```

CORE ADJUSTMENT TEST

```

017B 0 FFFF   CON6 DC /FFFF ADJ00680
017C 0 017D   LAST DC /FIRST ADJ00690
017D 0 0000   FIRST DC 0 ADJ00700
017E 0 012C   END START FIRST LOC OF PATTERN ADJ00710

```

CORE ADJUSTMENT TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
AA	0131	0139
CUNT	013C	0135
CON1	0176	0155, 0170, 0171
CON2	0177	0156
CON3	0178	015A
CON4	0179	015B
CON5	017A	0162
CON6	017B	0167, 016D
DDNE	016A	0164
FIRST	017D	0143, 0148, 017C
FX3	016F	0153
KDN	013A	012F
LAST	017C	013F
LDX1	0143	0140
LDZ5	015E	016E, 0172
LD15	016D	0157, 015C, 0174
NEGN	014B	013D
PLACE	014E	0145, 016B
REPT	0145	0148
SETX	0141	0140
SIZE	013B	0130, 0131, 0137, 013C
START	012C	014A, 017E
TLOC	0175	014F, 0150, 0154, 0159, 015F, 0161, 0165, 0168, 016F

CORE ADJUSTMENT TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
AA	0131	0139
CONT	013C	0135
CON1	0176	0155,0170,0171
CON2	0177	0156
CON3	0178	015A
CON4	0179	015B
CON5	017A	0162
CON6	017B	0167,016D
DONE	016A	0164
FIRST	017D	0143,017C
FX3	016F	0153
KON	013A	012F
LAST	017C	013F,0148
LDX1	0143	014D
LDZ5	015E	016E,0172
LD15	016D	0157,015C,0174
NEGN	0148	013D
PLACE	014E	0145,0168
REPT	0145	0148
SETX	0141	0140
SIZE	013B	0130,0131,0137,013C
START	012C	014A,017E
TLOC	0175	014F,0150,0154,0159,015F,0161,0165,0168,016F

TABLE OF CONTENTS

PARAGRAPH	PAGE	0001
1. PURPOSE		
2. PREREQUISITES		
2.1 PROGRAM PREREQUISITES		
2.2 EQUIPMENT PREREQUISITES		
3. OPERATING PROCEDURES		
3.1 PROGRAM LOADING		
3.2 PROGRAM OPERATIONS		
3.3 WAITS AND LOOPS		
3.4 C.E. SCOPE OPTIONS		
4. PRINTOUTS (NONE)		
5. PROGRAM PHILOSOPHY		
6. APPENDIX (NONE)		

1. PURPOSE

THE 1130 INTERRUPT TEST PROGRAM IS DESIGNED TO ISOLATE INTERRUPT FAILURES WHICH COULD PREVENT THE LOADING OF OTHER PROGRAMS WITH THE BASIC DIAGNOSTIC LOADER IN THE 'LOAD AND GO MODE.' THE PROGRAM EXECUTES 2 BASIC TESTS OR AN AUTOMATIC LEVEL RESET LOOP FOR SCOPING THE CAUSE OF A LEVEL NOT BEING RESET. TEST 1 IS RUN ON ALL DEVICES AND CHECKS THE BASIC OPERATION OF THE INTERRUPT FORCED BRANCH, THE PROPER EXECUTION OF A LEVEL 4 INTERRUPT, AND ISOLATES INTERRUPT LEVELS WHICH ARE NOT BEING RESET.

TEST 2 IS RUN ON THE 1442 READER AND CHECKS THE PROPER EXECUTION OF A LEVEL 4 INTERRUPT IN CONJUNCTION WITH A LEVEL 0 INTERRUPT, THE ARRIVAL OF AN END OF EITHER TOO SOON OR TOO LATE IN CONJUNCTION WITH THE COLUMN INTERRUPT, AND PROPER EXECUTION OF A LEVEL 0 INTERRUPT. BOTH TESTS PROVIDE ERROR WAITS, ERROR LOOPS, AND SCOPE LOOP ROUTINES TO HELP DIAGNOSE THE FAILURE AND AID IN A QUICK REPAIR.

THE AUTOMATIC LEVEL RESET LOOP MODE IS FOR SCOPING THE RESET PROBLEM AND A WAIT INDICATE THE RESETTING OF THE INTERRUPT, IF IT OCCURS.

2. PREREQUISITES

2.1 PROGRAM PREREQUISITES

1130 BASIC DIAGNOSTIC LOADER.

2.2 EQUIPMENT PREREQUISITES

CARD READER OR PAPER TAPE READER.

3. OPERATING PROCEDURES

3.1 PROGRAM LOADING

1. THE 1130 INTERRUPT TEST IS LOADED BY THE 1130 BASIC DIAGNOSTIC

LOADER.

2. SET THE C. E. INTERRUPT DELAY SWITCH TO THE 'ON' POSITION.
3. SEE BASIC DIAGNOSTIC LOADER DOCUMENTATION FOR LOADING PROCEDURE.

3.2 PROGRAM OPERATION

1. AFTER THE PROGRAM IS LOADED, A WAIT OF WILL OCCUR. AT THIS TIME, THE I/O DEVICE BY WHICH THE PROGRAM WAS LOADED, AND THE PROGRAM MODE ARE TO BE SELECTED VIA THE BIT SWITCHES. SEE TABLE A, WAIT 1.

THE REASON THE DEVICE WHICH LOADED THE PROGRAM MUST BE SELECTED, IS THAT WITH THE C.E. INTERRUPT DELAY SWITCH IN THE ON POSITION, THE BASIC LOADER GENERATES A LEVEL 4 INTERRUPT WHICH CAN NOT BE SERVICED. WHEN THE C.E. INTERRUPT DELAY SWITCH IS TURNED OFF, THE LEVEL 4 INTERRUPT MUST BE SERVICED BEFORE ANY OTHER INTERRUPT CAN BE EXECUTED.

2. IF THE PROGRAM DETECTS NO ERRORS, AND THE AUTOMATIC LOOP RESET MODE IS NOT SELECTED, THE PROGRAM WILL HALT AT WAIT 4. IF A RERUN OF THE PROGRAM IS DESIRED, DEPRESS START.

3. ALL OTHER WAITS AND LOOPS ARE EXPLAINED IN TABLES A, B, AND C OF 3.3.

4. TO GO INTO A SCOPE LOOP AFTER A FAILURE HAS BEEN DETECTED, DEPRESS START. THE SCOPE LOOP IS SET UP FOR A 2 FEED/CYCLE PER SECOND RATE, AND A WAIT AFTER 100 FEED CYCLES HAVE BEEN EXECUTED. THE C.E. HAS AN OPTION TO CHANGE THESE VALVES. (SEE 3.4)

3.3 WAITS AND LOOPS

1. TABLE A - TEST 1 WAITS AND SCOPE LOOPS -

WAIT 0---OP CODE 0000. NO TRANSFER TOOK PLACE FROM I/O BUSS TO B REG. LOGIC KM201.

WAIT F---'INITIAL' DEVICE SELECTION AND PROGRAM MODE SELECTION.

A. MAKE PROGRAM READ IN DEVICE READY.

B. SELECT PROGRAM READ IN DEVICE, USING BIT SWITCHES. 0, 1, OR 2 AS FOLLOWS,

1. BIT 0-ON AND BITS 1 AND 2 OFF.. 1442 READER
2. BIT 1-ON AND BITS 0 AND 2 OFF.. P.T. READER
3. BIT 2-ON AND BITS 0 AND 1 OFF.. 2501 READER

C. IF AUTOMATIC RESET MODE IS DESIRED, SELECT LEVEL INVOLVED, USING BIT SWITCHES 4 THROUGH 7 AS FOLLOWS.

1. LEVEL 0-BIT 4
2. LEVEL 1-BIT 7
3. LEVEL 2-BIT 6
4. LEVEL 3-BITS 6 AND 7
5. LEVEL 4-BIT 5
6. LEVEL 5-BITS 5 AND 7
7. NO BITS SELECTED - LEVEL AUTOMATIC RESET MODE WAS NOT SELECTED.

D. DEPRESS START

WAIT 1---DEVICE SELECTION

A. MAKE DESIRED DEVICE READY.

B. SELECT DESIRED DEVICE, USING BIT SWITCHES 0, 1, OR 2 AS FOLLOWS. TURN OFF BIT SW B, IF ON.

1. BIT 0-ON AND BITS 1 AND 2 OFF.. 1442 READER
2. BIT 1-ON AND BITS 0 AND 2 OFF.. P.T. READER
3. BIT 2-ON AND BITS 0 AND 1 OFF.. 2501 READER

C. DEPRESS START

WAIT 2--DESIRED NUMBER OF FEED CYCLES DURING SCOPE LOOP, MAKE SUR THERE ARE ENOUGH CARDS OR TAPE TO MAKE ANOTHER PASS. PUSH START TO CONTINUE SCOPE LOOP.

WAIT 3--DEVICE WENT NOT READY. LOAD CARDS OR TAPE AND PUSH START TO CONTINUE.

WAIT 4--DEVICE TESTED, RAN SUCCESSFULLY. TO RERUN TEST, DEPRESS START.

WAIT 5--THE 1442 IS THE DEVICE SELECTED ON WHICH THE TEST WILL BE RUN. IF SOME OTHER DEVICE IS DESIRED, AND THIS IS NOT THE INITIAL WAIT 5, MAKE NEW SELECTION, USING CONSOLE ENTRY SWITCHES. (SEE WAIT 1) TURN INTERRUPT DELAY SW OFF IF IT IS ON, AND DEPRESS START IF PROG. DOES NOT START OPERATION BECAUSE OF A PENDING INTERRUPT.

WAIT 6--PAPER TAPE IS THE DEVICE SELECTED ON WHICH THE TEST WILL BE RUN. IF SOME OTHER DEVICE IS DESIRED, AND THIS IS NOT THE INITIAL WAIT 6, MAKE NEW SELECTION, USING CONSOLE ENTRY SWITCHES. (SEE WAIT 1) TURN INTERRUPT DELAY SW OFF IF IT IS ON, AND DEPRESS START IF PROG DOES NOT START OPERATING BECAUSE OF A PENDING INTERRUPT.

WAIT 7--THE 2501 IS THE DEVICE SELECTED ON WHICH THE TEST WILL BE RUN. IF SOME OTHER DEVICE IS DESIRED, AND THIS IS NOT THE INITIAL WAIT 7, MAKE NEW SELECTION, USING CONSOLE ENTRY SWITCHES. (SEE WAIT 1) TURN INTERRUPT DELAY SW OFF IF IT IS ON, AND DEPRESS START IF PROG DOES NOT START OPERATING BECAUSE OF A PENDING INTERRUPT.

WAIT 8--NO DEVICE WAS SELECTED. MAKE SELECTION USING CONSOLE ENTRY SWITCHES. (SEE WAIT 1) DEPRESS START.

WAIT A--1442 WAS DEVICE SELECTED AND IT WAS FOUND NOT READY. MAKE 1442 READY, AND DEPRESS START.

WAIT B--PAPER TAPE READER WAS DEVICE SELECTED AND FOUND NOT READY. MAKE P.T. READER READY, AND DEPRESS START.

WAIT C--2501 WAS DEVICE SELECTED AND IT WAS FOUND NOT READY. MAKE 2501 READY, AND DEPRESS START.

WAIT 11--NO INTERRUPTS GENERATED. PROGRAM IS CHECKING ABILITY TO SET RUN TRIGGER WITH INTERRUPT OCCURRING DURING A WAIT GP. TO FURTHER CHECK RUN TRIGGER WITH PROGRAM, PUSH START.

WAIT 12--NO INTERRUPT GENERATED. RUN TRIGGER HAS BEEN ELIMINATED AS CAUSE OF FAILURE. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM321.

WAIT 13--DROPPED ADDR BIT 13 WHEN GATING INTERRUPT ADDRESS FROM I/O BUSS TO B REG DURING BSI 12 CYCLE. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 14--A LEVEL 1 INTERRUPT ADDRESS WAS GENERATED. TO GO INTO

SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 15--A LEVEL 2 INTERRUPT ADDRESS WAS GENERATED. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 16--A LEVEL 3 INTERRUPT ADDRESS WAS GENERATED. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 17--PICK ADDR BIT 15 WHEN GATING INTERRUPT ADDR FROM I/O BUSS TO B REG DURING BSI 12 CYCLE. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 18--DROPPED ADDR BIT 12 WHEN GATING INTERRUPT ADDR FROM I/O BUSS TO B REG DURING BSI 12 CYCLE. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 19--PICKED ADDR BIT 14 WHEN GATING INTERRUPT ADDR FROM I/O BUSS TO B REG DURING BSI 12 CYCLE. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 1A--NO INTERRUPT ADDR BITS GATED FROM I/O BUSS TO B REG DURING BSI 12 CYCLE. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 1C--INTERRUPT OPERATION WAS NORMAL WHEN MASKING OUT WAIT OP. SUSPECT RUN TRIGGER IS NOT BEING SET. PUSHING START WILL CAUSE 1 FEED CYCLE EACH TIME IT IS PUSHED. LOGIC KA101.

LOOP LEVEL 0 ON--LEVEL 0 CANNOT BE RESET. AN AUTOMATIC SCOPE LOOP IS SET UP WITH THE PROG TRYING TO RESET IT. LOGIC KM201.

LOOP LEVEL 1 ON--LEVEL 1 CANNOT BE RESET. AN AUTOMATIC SCOPE LOOP IS SET UP WITH THE PROGRAM TRYING TO RESET IT. LOGIC KM201.

LOOP LEVEL 2 ON--LEVEL 2 CANNOT BE RESET. AN AUTOMATIC SCOPE LOOP IS SET UP WITH THE PROGRAM TRYING TO RESET IT. LOGIC KM201.

LOOP LEVEL 3 ON--LEVEL 3 CANNOT BE RESET. AN AUTOMATIC SCOPE LOOP IS SET UP WITH THE PROGRAM TRYING TO RESET IT. LOGIC KM201.

LOOP LEVEL 5 ON--LEVEL 5 CANNOT BE RESET. AN AUTOMATIC SCOPE LOOP IS SET UP WITH PROGRAM TRYING TO RESET IT. LOGIC KM201.

2. TABLE B - TEST 2 WAITS AND SCOPE LOOPS

WAIT 21--NO INTERRUPTS WERE GENERATED WITHIN 500 MSEC. AFTER A CARD IS FED. THIS SHOULD HAVE BEEN ENOUGH TIME TO RECEIVE 80 COLUMN INTERRUPTS AND AN END OF INTERRUPT. TO GO INTO SCOPE LOOP, PUSH START. IF AN INTERRUPT IS GENERATED DURING THE SCOPE LOOP, A WAIT WILL IDENTIFY IT LOGIC KM30

WAIT 22--NO LEVEL 4 INTERRUPT WAS GENERATED AFTER AT LEAST 1 COLUMN INTERRUPT WAS RECEIVED. THE ACTUAL NUMBER OF COLUMN INTERRUPTS IS DISPLAYED IN THE A REG. POSSIBLE CAUSE COULD BE LEVEL 0 NOT BEING RESET. TO GO INTO SCOPE LOOP, PUSH START LOGIC KM321.

WAIT 23--MORE THAN 80 COLUMN INTERRUPTS WERE RECEIVED WHEN END OP WAS GENERATED. THE ACTUAL NUMBER OF COLUMN INTERRUPTS IS DISPLAYED IN THE A REG. POSSIBLE CAUSE COULD BE DEVICE EMITTER. TO GO INTO SCOPE LOOP, PUSH START.

WAIT 24--LESS THAN 80 COLUMN INTERRUPTS WERE RECEIVED WHEN END

OP WAS GENERATED. THE ACTUAL NUMBER OF COLUMN INTERRUPTS IS DISPLAYED IN THE A REG. POSSIBLE CAUSE COULD BE DEVICE EMITTER. TO GO INTO SCOPE LOOP, PUSH START.

WAIT 25-INTERRUPT GENERATED CAUSE A LEVEL 1 ADDRESS TO BE GENERATED. POSSIBLE CAUSE COULD BE THAT ADDRESS BIT 15 WAS PICKED WHEN TRANSFERRING INTERRUPT ADDRESS FROM I/O BUSS TO B REG DURING 12 CYCLE OF A LEVEL 0 INTERRUPT. COLUMN COUNT IS DISPLAYED IN A REG. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 26-INTERRUPT GENERATE CAUSE A LEVEL 2 ADDRESS TO BE GENERATE POSSIBLE CAUSE COULD BE THAT ADDRESS BIT 14 WAS PICKED WH TRANSFERRING INTERRUPT ADDRESS FROM I/O BUSS TO B REG DURING 12 CYCLE OF A LEVEL 0 INTERRUPT. COLUMN COUNT IS DISPLAYED IN A REG. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 27-INTERRUPT GENERATED CAUSED A LEVEL 3 ADDRESS TO BE GENERATED. POSSIBLE CAUSE COULD BE THAT ADDRESS BITS 14 AND 15 WERE PICKED WHEN TRANSFERKING INTERRUPT ADDRESS FROM I/O BUSS TO B REG DURING 12 CYCLE OF A LEVE 0 INTERRUPT. COLUMN COUNT IS DISPLAYED IN A REG. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 28-INTERRUPT GENERATED CAUSED A LEVEL 3 ADDRESS TO BE PICKED WHEN TRANSFERRING INTERRUPT ADDRESS FROM I/O BUSS TO B REG DURING 12 CYCLE OF A LEVEL 0 INTERRUPT. COLUMN COUNT IS DISPLAYED IN A REG. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201.

WAIT 29-BIT 12 WAS DROPPED WHEN TRANSFERRING INTERRUPT ADDRESS FROM I/O BUSS TO B REG DURING 12 CYCLE OF A LEVEL 0 INTERRUPT. COLUMN COUNT IS DISPLAYED IN A REG. TO GO INTO SCOPE LOOP, PUSH START. LOGIC KM201

3. TABLE C - AUTOMATIC LOOP RESET MODE WAITS

WAIT 3F - AUTOMATIC LOOP RESET MODE SELECTED. TURN C.E. INTERRUPT DELAY SWITCH OFF. THIS SHOULD CAUSE AN AUTOMATIC RESET LOOP FOR THE LEVEL SELECTED IN BIT SWITCHES 4 THROUGH 7 LOGIC KT311.

WAIT 30 - LEVEL 0 WAS SELECTED IN AUTOMATIC RESET LOOP MODE. A RESET OF THIS LEVEL DID OCCUR. DEPRESS START TO GO TO WAIT 1.

WAIT 31 - LEVEL 1 WAS SELECTED IN AUTOMATIC RESET LOOP MODE. A RESET OF THIS LEVEL DID OCCUR. DEPRESS START TO GO TO WAIT 1.

WAIT 32 - LEVEL 2 WAS SELECTED IN AUTOMATIC RESET LOOP MODE. A RESET OF THIS LEVEL DID OCCUR. DEPRESS START TO GO TO WAIT 1.

WAIT 33 - LEVEL 3 WAS SELECTED IN AUTOMATIC RESET LOOP MODE. A RESET OF THIS LEVEL DID OCCUR. DEPRESS START TO GO TO WAIT 1.

WAIT 34 - LEVEL 4 WAS SELECTED IN AUTOMATIC RESET LOOP MODE. A RESET OF THIS LEVEL DID OCCUR. DEPRESS START TO GO TO WAIT 1.

WAIT 35 - LEVEL 5 WAS SELECTED IN AUTOMATIC RESET LOOP MODE. A RESET OF THIS LEVEL DID OCCUR. DEPRESS START TO GO TO WAIT 1.

3.4 C.E. SCOPE LOOP OPTIONS

1. THE FEED CYCLE RATE IS PROGRAMED FOR 2 CYCLE PER SECONO. THIS RATE CAN BE CHANGED BY THE C.E. THROUGH THE SETTING OF BIT SWITCHES 8, 9, 10, OR 11 AS FOLLOWS

1. BIT SW.8 ON - 4 CYCLES PER SECONO.
2. BIT SW.9 ON - 8 CYCLES PER SECONO.
3. BIT SW10 ON - 16 CYCLES PER SECONO.
4. BIT SW11 ON - MAX PROGRAMED SPEED.
5. NO SWS ON - 2 CYCLES PER SECONO.

THESE SWITCHES MAY BE CHANGED AT ANY TIME DURING SCOPE LOOP.

2. THE NUMBER OF FEED CYCLES BETWEEN WAIT TWOS ARE PROGRAMED FOR 100. THIS NUMBER CAN BE CHANGED BY THE C.E. THROUGH THE SETTING OF BIT SWITCHES 12, 13, 14, OR 15 AS FOLLOWS.

1. BIT 12 ON - 25000 FEED CYCLES
2. BIT 13 ON - 250 FEED CYCLES
3. BIT 14 ON - 50 FEED CYCLES
4. BIT 15 ON - 10 FEED CYCLES
5. NO BITS ON - 100 FEED CYCLES

THE SWITCHES MAY BE CHANGED AT ANY TIME DURING THE SCOPE LOOP.

3. THE C.E. HAS THE OPTION TO TERMINATE THE SCOPE LOOP AND RETURN TO WAIT 1 FOR ANY NEW SET UP BY TURNING ON BIT SWITCH 03.

4. PRINTOUTS (NONE)
5. PROGRAM PHILOSOPHY

INTERRUPT TEST WILL BE RUN AFTER PROBLEMS ARE ENCOUNTERED WHEN TRYING TO LOAD A PROGRAM WITH THE BASIC LOADER IN THE LOAD AND GO MODE. THE CE INTERRUPT DELAY SWITCH IS THEN PLACED IN THE ON POSITION AND THE C.P.U. TEST IS THEN LOADED, AGAIN USING THE BASIC LOADER. THE SWITCH BEING ON, ALLOWS THE C.P.U. TEST TO BE LOADED WITHOUT THE INTERRUPT CIRCUITRY. IF THE C.P.U. TEST RUNS SUCCESSFULLY, THEN THE INTERRUPT CIRCUITRY WOULD BECOME THE PRIME AREA OF SUSPICION AS CAUSE OF THE LOADING PROBLEM. THE INTERRUPT TEST WOULD THEN BE RUN NEXT.

THE INTERRUPT TEST DOES NOT CHECK ON DATA TRANSFER, BUT DOES CHECK THE PROPER OPERATION OF THE INTERRUPT FORCED BRANCH INSTRUCTION AND THE PROPER LEVEL INTERRUPT ADDRESS. IN MOST CASES, AFTER THE TEST LOCATES THE PROBLEM AND IDENTIFIES IT WITH THE PROPER WAIT, A SCOPING LOOP CAN BE ENTERED BY DEPRESSING START. THE C.E. HAS 3 OPTIONS AT HIS CONTROL WHILE IN THE SCOPING LOOP. THESE ARE.

1. DELAY BETWEEN FEED CYCLES
2. NUMBER OF FEED CYCLES BETWEEN WAIT 2
3. AN OPTION TO SELECT ANOTHER DEVICE IF THERE IS ONE AVAILABLE

THE INTERRUPT TEST ALSO ALLOWS THE C.E. TO SELECT AN AUTOMATIC LEVEL RESET LOOP MODE. THIS OPTION IS TO BE USED WHEN A LEVEL CANNOT BE RESET. IF THIS WERE THE CASE, MOST OF THE PROGRAM'S TIME WOULD BE SPENT TRYING TO SERVICE THE INTERRUPT LEVEL AND PROGRAM OPERATION WOULD BE VERY ERRATIC. THEREFORE, THIS OPTION IS SET UP WITH A MINIMUM OF PROGRAM STEPS AFTER THE C.E. INTERRUPT DELAY SWITCH IS TURNED OFF. IF THE INTERRUPT LEVEL IS RESET, A WAIT WILL INDICATE SO.

THE INTERRUPT TEST AIDS IN LOCATING PROBLEMS IN 3 BASIC AREAS. THEY ARE.

1. LEVEL 4 (END OP) OF THE READ IN DEVICES
2. LEVEL 0 (COLUMN) OF THE 1442
3. LEVELS WHICH CANNOT BE RESET

1130 INTERRUPT TEST

LEVEL 4 - AT THE END OF A FEED OPERATION, THIS INTERRUPT IS GENERATED. THE TEST TRAPS SUCH FAILURES AS. NO INTERRUPT GENERATED DURING A WAIT OP, NO INTERRUPT GENERATED WHILE PROGRAM IS RUNNING, NO TRANSFER OF BSI L INSTRUCTION BITS OR INTERRUPT ADDRESS BITS FROM I/O BUSS TO B REG, DROPPING OR PICKING BITS BETWEEN I/O BUSS AND B REG, AND THE DETECTION OF AN INTERRUPT LEVEL NOT BEING RESET WHILE THIS TEST IS BEING RUN. ALL READ/IN DEVICES USE THIS PHASE OF THE TEST AND THE WAITS ARE IDENTIFIED BY WAIT 1X WHERE X IS THE PROBLEM IDENTIFIER.

LEVEL 0 - THE 1442 IS THE ONLY READ/IN DEVICE USING THIS PHASE OF THE TEST. THE TEST TRAPS PROBLEMS AS. NO INTERRUPT GENERATED, NO LEVEL 4 INTERRUPT GENERATED AFTER AT LEAST 1 LEVEL 0 INTERRUPT, PICKED OR DROPPED ADDRESS BITS ASSOCIATED WITH A LEVEL 0 INTERRUPT, LESS THAN 80 COLUMN INTERRUPTS BEFORE AN END OP, AND MORE THAN 80 COLUMNS BEFORE AN END OP. THE WAITS ASSOCIATED WITH THIS PHASE ARE-WAIT 2X, WHERE X IDENTIFIES THE PROBLEM.

AUTOMATIC LEVEL RESET LOOP - ALLOW SCOPING OF LEVELS WHICH CANNOT BE RESET. THIS MODE IS IDENTIFIED BY WAIT 3F. IF THE LEVEL IS RESET WHILE LOOPING, THE PROGRAM WILL WAIT. THE WAITS ASSOCIATED WITH THIS PHASE ARE-WAIT 3X, WHERE X IDENTIFIES THE LEVEL. DEPRESSING START WILL CAUSE THE PROGRAM TO GO TO WAIT 1, WHERE A NEW SETUP CAN BE MADE.

THE TEST IS DYNAMIC WHILE TESTING LEVEL 0 AND LEVEL 4 INTERRUPT OPERATION. IF AN INTERMITTENT FAILURE IS ENCOUNTERED, THE PROGRAM WILL INDICATE EACH FAILURE. IF THE TEST IS IN A SCOPE LOOP AND THE TROUBLE DISAPPEARS, THE PROGRAM AUTOMATICALLY RECOVERS AND TRIES TO COMPLETE A SUCCESSFUL RUN OR TRAP ANY OTHER FAILURE THAT MIGHT OCCUR.

6. APPENDIX (NONE)

INTERRUPT TEST

```

ABS
ORG /500
BEGIN NOP
WAITF WAIT /F
*****
*
*           WAIT F
*
* IF PROGRAM IS BEING RUN BECAUSE AN INTRPT
* INDICATOR IS NOT BEING CLEARED, SET COSOLE
* ENTRY SWITCHES 4---7 TO IDENTIFY LEVEL AT
* FAULT AND SELECT DEVICE TO BE USED IN TEST
* MAKE DEVICE READY AND PUSH START.
*
* IF PROGRAM IS BEING RUN BECAUSE OF SOME
* OTHER REASON THAN STATED ABOVE,
* A. SELECT DEVICE VIA CONSOLE SWITCHES
* 0---2.
* B. MAKE DEVICE READY.
* C. PRESS START.
* NOTE INITIAL WAIT F , SELECT PROGRAM READ
* IN DEVICE
*****
* INTERRUPT VECTOR SETUP.
*****
MAPIT LDX L1 VEC00
STX L1 /0008 LEVEL 0
LDX L1 VEC01
STX L1 /0009 LEVEL 1
LDX L1 VEC02
STX L1 /000A LEVEL 2
LDX L1 VEC03
STX L1 /000B LEVEL 3
LDX L1 VEC04
STX L1 /000C LEVEL 4
LDX L1 VEC05
STX L1 /000D LEVEL 5
LDX L1 BAD12 BIT 12 DROPPED
LDX L1 BAD14 BIT 14 PICKED
STX L1 /000E BIT 14 PICKED
LDX L1 NOADR
STX L1 /0000 NO INTERRUPT ADDR
*
MDX WHICH
*
WAIT1 WAIT 1
*****
*
*           WAIT 1
*
* A. SELECT DEVICE VIA CONSOLE SWITCHES
* 0---2.
* B. MAKE DEVICE WHICH
* C. PRESS START.
*****
WHICH LDX L1 /1000
STX L1 WAIT1-1
XIO L BITSW READ BIT SWITCHES
LD L BITS1 LOAD BIT SWITCHES
SRA 12 SET UP FOR DEVICE
STO L BITS2

```

```

3A800000
3A800010
3A800020
3A800030
3A800040
3A800050
3A800060
3A800070
3A800080
3A800090
3A800100
3A800110
3A800120
3A800130
3A800140
3A800150
3A800160
3A800170
3A800180
3A800190
3A800200
3A800210
3A800220
3A800230
3A800240
3A800250
3A800260
3A800270
3A800280
3A800290
3A800300
3A800310
3A800320
3A800330
3A800340
3A800350
3A800360
3A800370
3A800380
3A800390
3A800400
3A800410
3A800420
3A800430
3A800440
3A800450
3A800460
3A800470
3A800480
3A800490
3A800500
3A800510
3A800520
3A800530
3A800540
3A800550
3A800560
3A800570
3A800580
3A800590
3A800600
3A800610
3A800620
3A800630
3A800640
3A800650
3A800660
3A800670

```

INTERRUPT TEST

```

0532 0 1801
0533 00 4C0405CB
0535 0 1801
0536 00 4C0405C1
0538 0 1801
0539 00 4C0405B8
053B 0 3008
053C 00 4C000528
053E 00 0C000A66
0540 00 4C000A77
0542 0 1808
0543 00 04000A79
0545 0 1803
0546 00 4C040580
0548 00 4C000A79
054A 00 4C040578
054C 0 1801
054D 00 4C040590
054F 0 1801
0550 00 4C0405A4
0552 00 4C000A6E
0554 00 65003030
0556 00 6D000739
0558 00 65003031
055A 00 6D000749
055C 00 65003032
055E 00 6D000759
0560 00 65003033
0562 00 6D000769
0564 00 65003035
0566 00 6D0007C0
0568 00 4C00091E
056A 00 0400073F
056C 00 0400074F
056E 00 0400075F
0570 00 0400076F
0572 00 040007C6
0574 0 303F
0575 00 4C000527
0577 0 70FD
0578 0 1801
0579 00 4C04059A
057B 0 1801
057C 00 4C0405AE

```

```

SRA 1
BSC L WHAT3,E CHECK FOR 2501
SRA 1
BSC L WHAT2,E CHECK FOR PAPER TAPE
SRA 1
BSC L WHAT1,E CHECK FOR 1442
*****
*
*           WAIT 8
*
* NO DEVICE WAS FOUND TO BE SELECTED.
* MAKE SELECTION AND PRESS START.
*****
WAIT8 WAIT 8 NO DEVICE SELECTED
BSC L WHICH SET UP TO CHK AGAIN
*
CKLOP XIO L BITSW READ BIT SWITCHES
LD L BITS1 LOAD BIT SWITCHES
SRA 8 LEVEL ON CHECK
STO L BITS3 LEVEL CHECK BITS
SRA 3 CHECK FOR LEVEL 0 ON
BSC L VECT0,E SET UP LEVEL 0 LOOP
LD L BITS3 LEVEL CHECK BITS
BSC L CKBIT,E NUM OF LEVEL IS ODD
SRA 1 CHECK FOR LEVEL 2 ON
BSC L VECT2,E SET UP LEVEL 2 LOOP
SRA 1 CHECK FOR LEVEL 4 ON
BSC L VECT4,E SET UP LEVEL 4 LOOP
BSC L CLRIX NO RESET LOOP SEL.
*
*****
*
*           WAIT 3F
*
* LEVEL RESET LOOP OPTION HAS BEEN CHOSEN.
* TURN C.E. INTERRUPT SWITCH - OFF. THIS
* SHOULD SET UP AN AUTOMATIC RESET LOOP FOR
* DEVICE AND LEVEL SELECTED, FOR SCOPE/WORK.
*****
* RESTORE LEVEL RESET LOOP WAITS
*****
GOLOP LDX L1 /3030
STX L1 MOD13 RESTORE WAIT 30
LDX L1 /3031
STX L1 MOD14 RESTORE WAIT 31
LDX L1 /3032
STX L1 MOD15 RESTORE WAIT 32
LDX L1 /3033
STX L1 MOD16 RESTORE WAIT 33
LDX L1 /3035
STX L1 MOD17 RESTORE WAIT 35
*
LD L MOD12+1 SET UP WAIT 1 RETURN
STO L MOD13+6
STO L MOD14+6
STO L MOD15+6
STO L MOD16+6
STO L MOD17+6
*
LOOPS WAIT /3F
BSC L WAIT1 *-
MDX LOOPS+1
*
CKBIT SRA 1 CHECK FOR LEVEL 3 ON
BSC L VECT3,E SET UP LEVEL 3 LOOP
SRA 1 CHECK FOR LEVEL 5
BSC L VECT5,E SET UP LEVEL 5 LOOP

```

```

3A800680
3A800690
3A800700
3A800710
3A800720
3A800730
3A800740
3A800750
3A800760
3A800770
3A800780
3A800790
3A800800
3A800810
3A800820
3A800830
3A800840
3A800850
3A800860
3A800870
3A800880
3A800890
3A800900
3A800910
3A800920
3A800930
3A800940
3A800950
3A800960
3A800970
3A800980
3A800990
3A810000
3A810100
3A810200
3A810300
3A810400
3A810500
3A810600
3A810700
3A810800
3A810900
3A811000
3A811100
3A811200
3A811300
3A811400
3A811500
3A811600
3A811700
3A811800
3A811900
3A812000
3A812100
3A812200
3A812300
3A812400
3A812500
3A812600
3A812700
3A812800
3A812900
3A813000
3A813100
3A813200
3A813300
3A813400
3A813500

```

INTERRUPT TEST

```

057E 00 4C000586      BSC L VECT1      SET UP LEVEL 1 LOOP      3A801360
*
0580 00 65000731      VECT0 LDX L1 LOOP0+1      3A801370
0582 00 6D000576      STX L1 LOOPS+2      SET LEV LOOP VECTOR      3A801380
0584 00 4C000554      BSC L GOLOP      SET UP,GO TO WAIT 3F      3A801390
*
0586 00 65000741      VECT1 LDX L1 LOOP1+1      3A801400
0588 00 6D000576      STX L1 LOOPS+2      SET LEV LOOP VECTOR      3A801410
058A 00 65000740      LDX L1 LOOP1      3A801420
058C 00 6D000009      STX L1 /0009      3A801430
058E 00 4C000554      BSC L GOLOP      SET UP,GO TO WAIT 3F      3A801440
*
0590 00 65000751      VECT2 LDX L1 LOOP2+1      3A801450
0592 00 6D000576      STX L1 LOOPS+2      SET LEV LOOP VECTOR      3A801460
0594 00 65000751      LDX L1 LOOP2+1      3A801470
0596 00 6D00000A      STX L1 /000A      3A801480
0598 00 4C000554      BSC L GOLOP      SET UP,GO TO WAIT 3F      3A801490
*
059A 00 65000761      VECT3 LDX L1 LOOP3+1      3A801500
059C 00 6D000576      STX L1 LOOPS+2      SET LEV LOOP VECTOR      3A801510
059E 00 65000760      LDX L1 LOOP3      3A801520
05A0 00 6D00000B      STX L1 /000B      3A801530
05A2 00 4C000554      BSC L GOLOP      SET UP,GO TO WAIT 3F      3A801540
*
05A4 00 6500081E      VECT4 LDX L1 LOOP4+1      3A801550
05A6 00 6D000576      STX L1 LOOPS+2      SET LEV LOOP VECTOR      3A801560
05A8 00 6500081D      LDX L1 LOOP4      3A801570
05AA 00 6D00000C      STX L1 /000C      3A801580
05AC 00 4C000554      BSC L GOLOP      SET UP,GO TO WAIT 3F      3A801590
*
05AE 00 65000788      VECT5 LDX L1 LOOP5+1      3A801600
05B0 00 6D000576      STX L1 LOOPS+2      SET LEV LOOP VECTOR      3A801610
05B2 00 65000787      LDX L1 LOOP5      3A801620
05B4 00 6D00000D      STX L1 /000D      3A801630
05B6 00 4C000554      BSC L GOLOP      SET UP,GO TO WAIT 3F      3A801640
*
05B8 00 0C000A58      WHAT1 XID L SENSE      SENSE 1442 READY      3A801650
05BA 00 4C04058E      BSC L NRDYA,E      CHK NOT READY      3A801660
05BC 00 4C0005D4      BSC L SET42      SET UP 1442 PRG VEC      3A801670
*****
*          WAIT A          *
* 1442 SELECTED AND NOT READY. MAKE IT READY*
* OR SOME OTHER DEVICE SELECTION VIA CONSOLE*
* ENTRY SWITCHES. PUSH START. *
*****
05BE 0 300A          NRDYA WAIT /A          SEL 1442/NOT READY      3A801680
05BF 00 4C000528      BSC L WHICH          CHK DEVICE AGAIN      3A801690
*
05C1 00 0C000A5A      WHAT2 XID L SENPT      SENSE P.T. READY      3A801700
05C3 0 180A          SRA 10              3A801710
05C4 00 4C0405C8      BSC L NRDYB,E      CHK NOT READY      3A801720
05C6 00 4C00061E      BSC L SETPT          SET UP P.T. PRG VEC      3A801730
*****
*          WAIT B          *
* P.T. SELECTED AND NOT READY. MAKE IT READY*
* OR SOME OTHER DEVICE SELECTION VIA CONSOLE*
* ENTRY SWITCHES. PUSH START. *
*****
05C8 0 300B          NRDYB WAIT /B          SEL P.T./NOT READY      3A801740
05C9 00 4C000528      BSC L WHICH          CHK DEVICE AGAIN      3A801750
*
05CB 00 0C000A5C      WHAT3 XID L SEN25      SENSE 2501 READY      3A801760
05CD 00 4C0405D1      BSC L NRDYC,E      CHK NOT READY      3A801770
05CF 00 4C000666      BSC L SET25          SET UP 2501 PRG VEC      3A801780
*****
*          WAIT C          *
* 2501 SELECTED AND NOT READY. MAKE IT READY*
* OR SOME OTHER DEVICE SELECTION VIA CONSOLE*
*****

```

INTERRUPT TEST

```

* ENTRY SWITCHES. PUSH START. *
*****
05D1 0 300C          NRDYC WAIT /C          SEL 2501/NOT READY      3A802040
05D2 00 4C000528      BSC L WHICH          CHK DEVICE AGAIN      3A802050
*
05D4 00 65000A58      SET42 LDX L1 SENSE      SET UP 1442 SENSE WD      3A802060
05D6 00 6D0006DC      STX L1 BUSY+1      3A802070
05D8 00 6D0006EA      STX L1 TEST1+3      3A802080
05DA 00 6D00072A      STX L1 WAITG+2      3A802090
05DC 00 6D000736      STX L1 VEC00+2      3A802100
05DE 00 6D000746      STX L1 VEC01+2      3A802110
05E0 00 6D000756      STX L1 VEC02+2      3A802120
05E2 00 6D000766      STX L1 VEC03+2      3A802130
05E4 00 6D000772      STX L1 VEC04+2      3A802140
05E6 00 6D00078D      STX L1 VEC05+2      3A802150
05E8 00 6D0007C9      STX L1 CKDOK+2      3A802160
05EA 00 6D0007DD      STX L1 BAD12+2      3A802170
05EC 00 6D0007E9      STX L1 BAD14+2      3A802180
05EE 00 6D0007F5      STX L1 NOADR+2      3A802190
05F0 00 6D000802      STX L1 DSMCK+3      3A802200
05F2 00 6D000808      STX L1 DSMCK+12     3A802210
*
05F4 00 65800ABC      LDX I1 SRA01          SET UP 1442 BUSY CHK      3A802220
05F6 00 6D0006DD      STX L1 BUSY+2      3A802230
*
05F8 00 65800A8B      LDX I1 NOPIT          SET UP 1442 CONTROLS      3A802240
05FA 00 6D0006EB      STX L1 TEST1+4      3A802250
05FC 00 6D000803      STX L1 DSMCK+4      3A802260
05FE 00 6D00080C      STX L1 DSMCK+13     3A802270
*
0600 00 65000A6A      LDX L1 FEED          SET UP 1442 XID          3A802280
0602 00 6D0006EF      STX L1 TEST1+B      3A802290
*
0604 00 65000A85      LDX L1 K100          SET UP 1442 LOOP CNT      3A802300
0606 00 6D0006FE      STX L1 NUMBR+1      3A802310
0608 00 6D000723      STX L1 NUMCK+1      3A802320
*
060A 00 65000A82      LDX L1 K010          SET UP 1442 GOOD CNT      3A802330
060C 00 6D0007A9      STX L1 FINSH+1      3A802340
*
060E 00 65000829      LDX L1 SETUP          SET UP 1442 TEST VEC      3A802350
0610 00 6D0007AB      STX L1 FINSH+3      3A802360
*****
*          WAIT 5          *
*****
* 1442 WAS FOUND READY AND WILL BE THE *
* DEVICE USED IN THE TEST. *
* IF INTERRUPT DELAY SW ON, TURN OFF *
* IF PROGRAM DOES NOT START RUNNING BECAUSE *
* OF A PENDING INTERRUPT, DEPRESS START. *
*****
0612 0 3005          WAIT 5              1442 SELECTED      3A802370
0613 00 0C000A66      XID L BITSW          READ BIT SWITCHES      3A802380
0615 00 4C000A77      LD L BITS1          LOAD BIT SWITCHES      3A802390
0617 0 180C          SRA 12              3A802400
0618 00 94000A78      S L BITS2          LAST DEVICE SELECTED      3A802410
061A 00 4C18053E      BSC L CKLOP,+      CHK FOR LEVEL LOOP      3A802420
061C 00 4C000528      BSC L WHICH          NEW DEVICE SELECTED      3A802430
*
061E 00 65000A5A      SETPT LDX L1 SENPT      SET UP PT SENSE WD      3A802440
0620 00 6D0006DC      STX L1 BUSY+1      3A802450
0622 00 6D0006EA      STX L1 TEST1+3      3A802460
0624 00 6D00072A      STX L1 WAITG+2      3A802470
0626 00 6D000736      STX L1 VEC00+2      3A802480
0628 00 6D000746      STX L1 VEC01+2      3A802490

```

INTERRUPT TEST

```

062A 00 6D000756 STX L1 VEC02+2
062C 00 6D000766 STX L1 VEC03+2
062E 00 6D000772 STX L1 VEC04+2
0630 00 6D000780 STX L1 VEC05+2
0632 00 6D0007C9 STX L1 CKDOK+2
0634 00 6D0007DD STX L1 BAD12+2
0636 00 6D0007E9 STX L1 BAD14+2
0638 00 6D0007F5 STX L1 NODADR+2
063A 00 6D000802 STX L1 DSMCK+3
063C 00 6D000808 STX L1 DSMCK+12
*
063E 00 65800A8E LDX I1 SRA11 SET UP P.T. BUSY CHK
0640 00 6D0006DD STX L1 BUSY+2
*
0642 00 65800A8D LDX I1 SRA10 SET UP P.T. MDY CHK
0644 00 6D0006E8 STX L1 TEST1+4
0646 00 6D000803 STX L1 DSMCK+4
0648 00 6D00080C STX L1 DSMCK+13
*
064A 00 65000A72 LDX L1 CNTRL SET UP P.T. XIO
064C 00 6D0006EF STX L1 TEST1+8
*
064E 00 65000A85 LDX L1 K100 SET UP P.T. CHAR CNT
0650 00 6D0006FE STX L1 NUMBR+1
0652 00 6D000723 STX L1 NUMCK+1
0654 00 6D0007A9 STX L1 FINSH+1
*
0656 00 65000912 LDX L1 WAITA SET UP P.T. TEST VEC
0658 00 6D0007A8 STX L1 FINSH+3
*
*****
*
* WAIT 6
*
* PAPER TAPE WAS FOUND READY AND WILL BE THE
* DEVICE USED IN THE TEST.
* IF INTERRUPT DELAY SW ON, TURN OFF
* IF PROGRAM DOES NOT START RUNNING BECAUSE
* OF A PENDING INTERRUPT, DEPRESS START.
*
*****
065A 0 3006 WAIT 6 PAPER TAPE SELECTED
065B 00 0C000A66 XIO L BITSW READ BIT SWITCHES
065D 00 C4000A77 LD L BITS1 LOAD BIT SWITCHES
065F 0 180C SRA 12
0660 00 94000A78 S L BITS2 LAST DEVICE SELECTED
0662 00 4C18053E BSC L CKLOP,+-- CHK FOR LEVEL LOOP
0664 00 4C000528 BSC L WHICH NEW DEVICE SELECTED
*
0666 00 65000A5C SET25 LDX L1 SEN25 SET UP 2501 SENSE WD
0668 00 6D0006DC STX L1 BUSY+1
066A 00 6D0006EA STX L1 TEST1+3
066C 00 6D00072A STX L1 WAIT6+2
066E 00 6D000736 STX L1 VEC00+2
0670 00 6D000746 STX L1 VEC01+2
0672 00 6D000756 STX L1 VEC02+2
0674 00 6D000766 STX L1 VEC03+2
0676 00 6D000772 STX L1 VEC04+2
0678 00 6D000780 STX L1 VEC05+2
067A 00 6D0007C9 STX L1 CKDOK+2
067C 00 6D0007DD STX L1 BAD12+2
067E 00 6D0007E9 STX L1 BAD14+2
0680 00 6D0007F5 STX L1 NODADR+2
0682 00 6D000802 STX L1 DSMCK+3
0684 00 6D000808 STX L1 DSMCK+12
*
0686 00 65800A8C LDX I1 SRA01 SET UP 2501 BUSY CHK
0688 00 6D0006DD STX L1 BUSY+2

```

INTERRUPT TEST

```

068A 00 65800A88 * LDX I1 MOPIT SET UP 2501 CONTROLS
068C 00 6D0006EB STX L1 TEST1+4
068E 00 6D000803 STX L1 DSMCK+4
0690 00 6D00080C STX L1 DSMCK+13
*
0692 00 65000A6C LDX L1 FEEDS SET UP 2501 XIO
0694 00 6D0006EF STX L1 TEST1+8
*
0696 00 65000A85 LDX L1 K100 SET UP 2501 CARD CNT
0698 00 6D0006FE STX L1 NUMBR+1
069A 00 6D000723 STX L1 NUMCK+1
069C 00 6D0007A9 STX L1 FINSH+1
*
069E 00 65000912 LDX L1 WAITA SET UP 2501 TEST VEC
06A0 00 6D0007A8 STX L1 FINSH+3
*
*****
*
* WAIT 7
*
* 2501 WAS FOUND READY AND WILL BE THE
* DEVICE USED IN THE TEST.
* IF SOME OTHER DEVICE IS DESIRED, MAKE THAT
* DEVICE READY AND MAKE NEW DEVICE SELECTION
* VIA THE CONSOLE ENTRY SWITCHES.
*
*****
06A2 0 3007 WAIT 7 2501 SELECTED
06A3 00 0C000A66 XIO L BITSW READ BIT SWITCHES
06A5 00 C4000A77 LD L BITS1 LOAD BIT SWITCHES
06A7 0 180C SRA 12
06A8 00 94000A78 S L BITS2 LAST DEVICE SELECTED
06AA 00 4C18053E BSC L CKLOP,+-- CHK FOR LEVEL LOOP
06AC 00 4C000528 BSC L WHICH NEW DEVICE SELECTED
*
06AE 0 6300 CLRIX LDX 3 0
06AF 0 6200 LDX 2 0
06B0 0 6100 LDX 1 0
06B1 00 65000770 LDX L1 VEC04
06B3 00 6D00000C STX L1 /000C
06B5 00 C4000727 LD L NUMCK+5 RESTORE LOOP CHK VEC
06B7 00 D400073F STO L MOD13+6
06B9 00 D400074F STO L MOD14+6
06BB 00 D400075F STO L MOD15+6
06BD 00 D400076F STO L MOD16+6
06BF 00 D40007C6 STO L MOD17+6
06C1 00 D40007E6 STO L MOD18+6
06C3 00 D40007F2 STO L MOD19+6
06C5 00 D40007FE STO L MOD1A+6
06C7 00 65003013 LDX L1 /3013
06C9 00 6D000739 STX L1 MOD13 RESTORE WAIT 13
06CB 00 65003014 LDX L1 /3014
06CD 00 6D000749 STX L1 MOD14 RESTORE WAIT 14
06CF 00 65003015 LDX L1 /3015
06D1 00 6D000759 STX L1 MOD15 RESTORE WAIT 15
06D3 00 65003016 LDX L1 /3016
06D5 00 6D000769 STX L1 MOD16 RESTORE WAIT 16
06D7 00 65003017 LDX L1 /3017
06D9 00 6D0007C0 STX L1 MOD17 RESTORE WAIT 17
*
06DB 00 0C000A58 BUSY XIO L SENSE SENSE DSW
06DD 0 1801 SRA 1 SET UP TO CHK BUSY
06DE 00 4C0406DB BSC L BUSY+E CHECK FOR BUSY
06E0 00 0C000A66 XIO L BITSW SENSE BIT SWITCHES
06E2 00 C4000A77 LD L BITS1 LOAD BIT SWITCHES
06E4 0 180C SRA 12 CHK FOR WAIT 1 OPT
06E5 00 4C040771 BSC L VEC04+1,E SET UP FOR RESTORE

```


INTERRUPT TEST

```

06E7 00 67800A7D TEST1 LDX 13 DELAY 500 MSEC DELAY
06E9 00 0C000A58 X10 L SENSE SENSE FOR READY
06EB 0 1000 NOP
06EC 00 4C0407FF BSC L DSWCK,E CHECK FOR READY
06EE 00 0C000A6A X10 L FEED FEED

*****
* WAIT 11 *
* NO INTERRUPTS *
* WERE GENERATED. *
* TO CHECK OUT RUN *
* TRIGGER, PUSH *
* START *
*****
NO INTERRUPTS
SET UP RUN TRIG CHK
DECREMENT DELAY BY 1

*****
* WAIT 12 *
* NO INTERRUPTS *
* WERE GENERATED. *
* SETTING OF RUN *
* TRIGGER APPEARS *
* NOT TO BE THE *
* CAUSE OF THE *
* FAILURE. *
* TO GO INTO SCOPE *
* LOOP, PUSH START.*
*****
NO INT-RUN TRIG CKED

SET UP LEVEL 4 VEC
NOP
SET UP SCOPE LOOP

BRANCH TO SCOPE LOOP

SET UP RUN TRIG CHK

CHECK RUN TRIGGER

RESET GOOD PASS CNTR
CHK COUNT OPTION

STEP DOWN DELAY
LOAD LOOP COUNT
ADD 1 TO LOOP CNT
STORE LOOP CNT
CHECK FOR STUP LOOP
CHECK FOR WAIT 2
FEED AGAIN

```

```

3A804080
3A804090
3A804100
3A804110
3A804120
3A804130
3A804140
3A804150
3A804160
3A804170
3A804180
3A804190
3A804200
3A804210
3A804220
3A804230
3A804240
3A804250
3A804260
3A804270
3A804280
3A804290
3A804300
3A804310
3A804320
3A804330
3A804340
3A804350
3A804360
3A804370
3A804380
3A804390
3A804400
3A804410
3A804420
3A804430
3A804440
3A804450
3A804460
3A804470
3A804480
3A804490
3A804500
3A804510
3A804520
3A804530
3A804540
3A804550
3A804560
3A804570
3A804580
3A804590
3A804600
3A804610
3A804620
3A804630
3A804640
3A804650
3A804660
3A804670
3A804680
3A804690
3A804700
3A804710
3A804720
3A804730
3A804740
3A804750

```

INTERRUPT TEST

```

*****
* WAIT 2 *
* NORMAL WAIT AFTER DESIRED NUMBER OF LOOPS *
* PASSES HAVE BEEN MADE. PUSH START TO MAKE *
* ANOTHER LOOP CYCLE. *
*****
WAITG WAIT 2 STOP SCOPE LOOP
X10 L SENSE
LDX 1 0
STX L1 LPCNT RESET LOOP COUNT
BSC L FDCYC

*****
* LEVEL 0 AUTO *
* LEVEL RESET LOOP *
*****
* LEVEL 0 RESET *
* SCOPE LOOP *
*****
* INTERRUPT 0 LEVEL*
* WAIT 30 *
* RESET DURING AUTO*
* SCOPE LOOP. *
* PUSH START TO GO *
* TO WAIT 1. *
*****
* WAIT 13 *
* DROPPED ADDR BIT *
* 13. PUSH START *
* FOR SCOPE LOOP *
*****
* MDX ERROR *
*****
* WAIT 31 *
* INTERRUPT 1 LEVEL*
* RESET DURING AUTO*
* SCOPE LOOP. *
* PUSH START TO GO *
* TO WAIT 1. *
*****
* WAIT 14 *
* INTERRUPT CAUSED *
* A LEVEL 1 ADDR TO*
* BE GENERATED. *
* PUSH START FOR *
* SCOPE LOOP. *
*****
* MDX ERROR *
*****

```

```

3A804760
3A804770
3A804780
3A804790
3A804800
3A804810
3A804820
3A804830
3A804840
3A804850
3A804860
3A804870
3A804880
3A804890
3A804900
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3A804920
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3A804990
3A805000
3A805010
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3A805100
3A805110
3A805120
3A805130
3A805140
3A805150
3A805160
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3A805180
3A805190
3A805200
3A805210
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3A805240
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3A805350
3A805360
3A805370
3A805380
3A805390
3A805400
3A805410
3A805420
3A805430

```

INTERRUPT TEST

```

*
*
* *****
*   WAIT 32   *
* INTERRUPT 2 LEVEL*
* RESET DURING AUTO*
* SCOPE LOOP.  *
* PUSH START TO GO *
* TO WAIT 1.   *
* *****
0750 0 0000      LOOP2 DC      0
0751 00 0C000A5E XIO L DISK
0753 0 7001      MDX      VEC02+1
*
0754 0 0000      VEC02 DC      0
0755 00 0C000A58 XIO L SENSE
0757 00 4C400759 BOSC L MOD15
*
*
0759 0 3032      MOD15 WAIT   /32
*
*
075A 00 65800A92 LDX I1 MOFYD
075C 00 6D000759 STX L1 MOD15
075E 00 4C000502 BSC L MAPIT
*
*
* *****
*   WAIT 15   *
* INTERRUPT CAUSED *
* A LEVEL 2 ADDR TO*
* BE GENERATED.  *
* PUSH START FOR  *
* SCOPE LOOP.    *
* *****
075A 00 65800A92 LDX I1 MOFYD
075C 00 6D000759 STX L1 MOD15
075E 00 4C000502 BSC L MAPIT
*
*
* *****
*   WAIT 33   *
* INTERRUPT 3 LEVEL*
* RESET DURING AUTO*
* SCOPE LOOP.    *
* PUSH START TO GO *
* TO WAIT 1.    *
* *****
0760 0 0000      LOOP3 DC      0
0761 00 0C000A60 XIO L PLOT
0763 0 7001      MDX      VEC03+1
*
0764 0 0000      VEC03 DC      0
0765 00 0C000A58 XIO L SENSE
0767 00 4C400769 BOSC L MOD16
*
*
0769 0 3033      MOD16 WAIT   /33
*
*
076A 00 65800A93 LDX I1 MOFYE
076C 00 6D000769 STX L1 MOD16
076E 00 4C000502 BSC L MAPIT
*
*
0770 0 0000      VEC04 DC      0
0771 00 0C000A58 XIO L SENSE
0773 0 6100      LDX      1 0
0774 00 6D000A7C STX L1 LPCNT
0776 00 65800A98 LDX I1 MOFYL
0778 00 6D0006F1 STX L1 MOD11
077A 00 65003011 LDX L1 /3011
077C 00 6D0006F0 STX L1 RUNCK
077E 00 65003012 LDX L1 /3012
0780 00 6D000701 STX L1 RUNOK
0782 00 65003013 LDX L1 /3013

```

INTERRUPT TEST

```

0784 00 6D000739 STX L1 MOD13
0786 00 65003014 LDX L1 /3014
0788 00 6D000749 STX L1 MOD14
078A 00 65003015 LDX L1 /3015
078C 00 6D000759 STX L1 MOD15
078E 00 65003016 LDX L1 /3016
0790 00 6D000769 STX L1 MOD16
0792 00 65003017 LDX L1 /3017
0794 00 6D0007C0 STX L1 MOD17
0796 00 65003018 LDX L1 /3018
0798 00 6D0007E0 STX L1 MOD18
079A 00 65003019 LDX L1 /3019
079C 00 6D0007EC STX L1 MOD19
079E 00 6500301A LDX L1 /301A
07A0 00 6D0007F8 STX L1 MOD1A
07A2 00 04000A7A LD L GDCNT
07A4 00 84000A81 A L K001
07A6 00 04000A7A STO L GDCNT
07A8 00 94000A82 FINSH S L K010
07AA 00 4C500829 BOSC L SETUP,-
07AC 00 0C000A66 XIO L BITSW
07AE 00 4C000A77 LD L RITS1
07B0 0 180C      SRA      12
07B1 00 4C440913 BOSC L WAITA+1,E
07B3 00 4C4006AE BOSC L CLR1X
*
07B5 00 4C00071A GAPIT BSC L ERROR
*
07B7 0 0000      LOOPS DC      0
07B8 00 0C000A68 XIO L STOP
07BA 0 7001      MDX      VEC05+1
*
07BB 0 0000      VEC05 DC      0
07BC 00 0C000A58 XIO L SENSE
07BE 00 4C4007C0 BOSC L MOD17
*
*
* *****
*   WAIT 35   *
* INTERRUPT 5 LEVEL*
* RESET DURING AUTO*
* SCOPE LOOP.    *
* PUSH START TO GO *
* TO WAIT 1.    *
* *****
07C0 0 3035      MOD17 WAIT   /35
*
*
07C1 00 65800A94 LDX I1 MOFYF
07C3 00 6D0007C0 STX L1 MOD17
07C5 00 4C000502 BSC L MAPIT
*
*
07C7 0 0000      CKDOK DC      0
07C8 00 0C000A58 XIO L SENSE
07CA 00 4C4007CC BOSC L WAITC
*
07CC 0 301C      WAITC WAIT   /1C
*
*
07CD 00 65003011 LDX L1 /3011
07CF 00 6D0006F0 STX L1 RUNCK
07D1 00 65800ABF LDX I1 MOFYA
07D3 00 6D0006F1 STX L1 MOD11
07D5 00 65000770 LDX L1 VEC04
07D7 00 6D00000C STX L1 /000C

```

INTERRUPT TEST

```

07D9 00 4C4006DB      BOSC L  BUSY      ERROR TRAP      3A806800
*                               *                               *
07DB 0  0000      * BAD12 DC      0                               *
07DC 00 0C000A58      XIO L  SENSE      *                               *
07DE 00 4C4007E0      BOSC L  MOD18      * WAIT 18      *
07E0 0  3018      MOD18 WAIT /18      * DROPPED ADDR BIT *
*                               *                               *
*                               *                               *
*                               *                               *
07E1 00 65800A95      LDX I1 MOFYG      *                               *
07E3 00 6D0007E0      STX L1 MOD18      * 12. PUSH START *
07E5 00 4C000715      BSC L  FDCYC      * FOR SCOPE LOOP *
*                               *                               *
*                               *                               *
07E7 0  0000      * BAD14 DC      0                               *
07E8 00 0C000A58      XIO L  SENSE      *                               *
07EA 00 4C4007EC      BOSC L  MOD19      * WAIT 19      *
07EC 0  3019      MOD19 WAIT /19      * PICKED ADDR BIT *
*                               *                               *
*                               *                               *
*                               *                               *
07ED 00 65800A96      LDX I1 MOFYH      *                               *
07EF 00 6D0007EC      STX L1 MOD19      * 14. PUSH START *
07F1 00 4C000715      BSC L  FDCYC      * FOR SCOPE LOOP *
*                               *                               *
*                               *                               *
07F3 0  0000      * N0ADR DC      0                               *
07F4 00 0C000A58      XIO L  SENSE      *                               *
07F6 00 4C4007F8      BOSC L  MOD1A      * WAIT 1A      *
07F8 0  301A      MOD1A WAIT /1A      * NO ADDR TRANSFER *
*                               *                               *
*                               *                               *
*                               *                               *
07F9 00 65800A97      LDX I1 MOFYJ      *                               *
07FB 00 6D0007F8      STX L1 MOD1A      * 14. PUSH START *
07FD 00 4C000715      BSC L  FDCYC      * FOR SCOPE LOOP *
*                               *                               *
*                               *                               *
*                               *                               *
* OP/CODE 0, WAIT 0.-----NO READOUT OF BSI *
* OR INTERRUPT ADDRESS. *
*                               *
*                               *
07FF 00 D4000A7E      DSWCK STD L DSW1      STORE DSW
0801 00 0C000A58      XIO L  SENSE      SENSE FOR READY
0803 0  1000      NOP
0804 00 94000A7E      S L DSW1      SUBTRACT LAST DSW
0806 00 4C18080A      BSC L DSWCK+11,+--
0808 00 4C0006E9      BSC L TEST1+2      DSW CHANGED
080A 00 0C000A58      XIO L  SENSE      CHECK FOR READY
080C 0  1000      NOP
080D 0  6100      LDX I 0
080E 00 6D000A7E      STX L1 DSW1      RESET STORED DSW
0810 00 4C040814      BSC L WAIT3,E      NOT READY
0812 00 4C0006EE      BSC L TEST1+7      READY
0814 0  3003      WAIT3 WAIT 3
*                               *
*                               *
*                               *
*                               *
0815 00 4C0006E9      BSC L  TEST1+2      READER READY
*                               *
*                               *
*                               *
*                               *
* DESIRED NUMBER OF *
* LOOP PASSES,WHILE*
* IN SCOPE LOOP. *
* PUSH START TO *
* ANOTHER SCOPE *
* LOOP PASS. *

```

INTERRUPT TEST

```

0817 0  3002      * WAIT2 WAIT 2      *                               *
0818 0  6100      LDX I 0      * STOP SCOPE LOOP *
0819 00 6D000A7C      STX L1 LPCNT      * RESET LOOP COUNT *
081B 0C 4C000715      BSC L  FDCYC      * CONTINUE TEST *
*                               *
*                               *
081D 0  0000      * LOOP4 DC      0      *                               *
081E 00 0C000A58      XIO L  SENSE      * LEVEL 4 AUTO *
0820 00 0C000A64      XIO L  CONSL      * LEVEL RESET LOOP *
0822 00 0C000A5A      XIO L  SENPT      * *
0824 00 4C400826      BOSC L  MOD20      * *
*                               *
*                               *
*                               *
0826 0  3034      * MOD20 WAIT /34      *                               *
0827 00 4C000502      BSC L  MAPIT      *                               *
*                               *
*                               *
*                               *
0829 0  6100      * SETUP LDX I 0      *                               *
082A 00 6D000A7A      STX L1 GDCNT      * RESET GOOD PASS CNT *
082C 00 65000897      LDX L1 INT00
082E 00 6D000008      STX L1 /0008
0830 00 6500092D      LDX L1 INT01
0832 00 6D000009      STX L1 /0009
0834 00 65000942      LDX L1 INT02
0836 00 6D00000A      STX L1 /000A
0838 00 65000957      LDX L1 INT03
083A 00 6D00000B      STX L1 /000B
083C 00 650008B2      LDX L1 INT04
083E 00 6D00000C      STX L1 /000C
0840 00 6500096C      LDX L1 INT05
0842 00 6D00000D      STX L1 /000D
0844 00 65000981      LDX L1 ADR12
0846 00 6D000000      STX L1 /0000
*                               *
*                               *
0848 0  6100      * RESET LDX I 0
0849 0  6200      LDX I 2
084A 0  6300      LDX I 3
*                               *
*                               *
084B 00 0C000A58      * BUZY XIO L SENSE      SENSE DSW
084D 0  1801      SRA I 1      SET UP TO CHK BIT 14
084E 00 4C04084B      BSC L BUZY,E      CHECK FOR BUSY
0850 00 0C000A66      XIO L BITSW      SENSE BIT SWITCHES
0852 00 4C000A77      LD L BITS1      LOAD BIT SWITCHES
0854 0  180C      SRA I 12      CHK FOR WAIT 1 OPT
0855 00 4C0408DA      BSC L CNTOK,E      SET UP FOR RESTORE
*                               *
*                               *
0857 00 67800A7D      * START LDX I3 DELAY      SET UP DELAY
0859 00 0C000A58      XIO L SENSE      SENSE FOR READY
085B 00 4C04087F      BSC L CKRDY,E      CHECK FOR READY
085D 00 0C000A70      XIO L RESTR
*                               *
*                               *
085F 0  73FF      * LESS1 MDX 3 -1
0860 0  70FE      MDX LESS1
*                               *
*                               *
*                               *
*                               *
*                               *
* NO INTERRUPTS WERE GENERATED WITHIN 500 *
* MSEC. AFTER A READS WAS GIVEN. THIS SHOULD*

```

INTERRUPT TEST

```

* HAVE BEEN ENOUGH TIME TO RECEIVE 80 COLUMN*
* INTERRUPTS AND AN END OP INTERRUPT. *
* PUSH START FOR SCOPE LOOP. *
*****
0861 0 3021 MOD21 WAIT /21 NO LEV. 0 OR 4 INTRPT
*****
* SCOPE LOOP *
* TO USE SCOPE LOOP, PRESS START. THIS WILL *
* FEED CARDS AT A 2 CARD/SEC RATE WITH *
* A HALT AFTER 100 CARDS. *
* IF AN INTERRUPT IS GENERATED DURING THIS *
* SCOPE LOOP, A WAIT WILL IDENTIFY IT. *
* MAKE SURE THERE IS A SUFFICIENT AMOUNT OF *
* BLANK CARDS IN READER TO ALLOW FURTHER *
* CHECKING. *
*****
0862 0 6100 CARDS LDX 1 0
0863 00 6D000A7A STX L1 GDCNT RESET GOOD PASS CNTR
0865 00 65001000 LDX L1 /1000 NOP
0867 00 6D000861 STX L1 MOD21 ALLOW LOOP
0869 00 4C0009FD BSC L CNTIT CHK COUNT OPTIOM
086B 00 4C000A7C RETRN LD L LPCNT LOOP CARD COUNTER
086D 00 84000A81 A L K001 ADD 1
086F 00 D4000A7C STO L LPCNT
0871 00 94000A85 TOTAL S L K100 SUBTRACT 100
0873 00 4C100B76 BSC L CHECK,-- 100 CARDS FED
0875 0 70D5 MDX BUZY CHECK FOR BUSY
*
0876 00 C4000A7B CHECK LD L CLCNT LOAD COLUMN COUNT
*****
* WAIT 2 *
*
* NORMAL WAIT AFTER DESIRED NUMBER OF CARDS *
* HAVE BEEN READ. PRESS START TO READ THE *
* NUMBER OF BLANK CARDS DESIRED *
*****
0878 0 3002 WAIT 2 100 CARDS FED
*
0879 0 6200 LDX 2 0
087A 00 6E000A7C STX L2 LPCNT RESET LOOP COUNT
087C 00 6E000A7B STX L2 CLCNT RESET COLUMN COUNT
087E 0 70CC MDX BUZY RESTART LOOP CHECK
*
087F 00 D4000A7E CKRDY STO L DSW1 STORE DSW
0881 00 0C000A58 XIO L SENSE SENSE FOR READY
0883 00 94000A7E S L DSW1 SUBTRACT LAST DSW
0885 00 4C180689 BSC L CKRDY+10,+--
0887 00 4C000859 BSC L START+2 DSW CHANGED
0889 00 0C000A58 XIO L SENSE RESET DSW
088B 0 6100 LDX 1 0
088C 00 6D000A7E STX L1 DSW1 RESET STORED DSW
088E 00 4C040892 BSC L NRDY,E NOT READY
0890 00 4C00085D BSC L START+6 READY
*
* ***** *
* WAIT 3 *
* READER NOT READY *
* ***** *
0892 0 3003 NRDY WAIT 3 READER NOT READY
0893 00 0C000A58 XIO L SENSE SENSE + RESET
0895 00 4C000859 BSC L START+2 READER READY

```

```

3A808160
3A808170
3A808180
3A808190
3A808200
3A808210
3A808220
3A808230
3A808240
3A808250
3A808260
3A808270
3A808280
3A808290
3A808300
3A808310
3A808320
3A808330
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3A808370
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3A808390
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3A808690
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3A808830

```

INTERRUPT TEST

```

*
0897 0 0000 INT00 DC 0
0898 00 0C000A58 XIO L SENSE
089A 00 74010A7B MDX L CLCNT,+1 ADD 1 TO COLUMN CNT
089C 00 650008B2 LDX L1 INT04 RESTORE LEVEL 4 VEC.
089E 00 6D00000C STX L1 /000C
08A0 00 66800A9A LDX I2 MDYF3 MDX WAIT 22
08A2 0 6ABE STX 2 MOD21 CHECK FOR LEVEL 4
08A3 00 4C4008A5 BOSC L COLGO RESET LEVEL 0
*
08A5 00 6C000A74 COLGO XIO L READ
08A7 00 4C00085F BSC L LESS1
*****
* WAIT 22 *
*
* AT LEAST 1 COLUMN INTERRUPT WAS GENERATED *
* AND NO END OP GENERATED FOR LAST CARD. *
* THE NUMBER OF COLUMNS READ IS DISPLAYED *
* IN THE A REG. *
* PUSH START FOR SCOPE LOOP. *
*****
08A9 0 3022 MOD22 WAIT /22 NO LEVEL 4 RECIEVED
*****
* SCOPE LOOP *
*****
08AA 00 65000001 LDX L1 /0001 NOP
08AC 00 6D0008A9 STX L1 MOD22 ALLOW LOOP
08AE 0 6100 LDX 1 0 RESET COLUMN COUNT
08AF 00 6D000A7B STX L1 CLCNT
08B1 0 70B0 MDX MOD21+1 BRANCH TO LOOP
*
08B2 0 0000 INT04 DC 0
08B3 00 0C000A58 XIO L SENSE
08B5 00 74010A7A MDX L GDCNT,+1 ADD 1 TO GOOD PASS
08B7 00 65003021 LDX L1 /3021
08B9 00 6D000861 STX L1 MOD21 RESTORE WAIT 21
08BB 00 65003022 LDX L1 /3022
08BD 00 6D0008A9 STX L1 MOD22 RESTORE WAIT 22
08BF 00 C4000A7B LD L CLCNT LOAD COLUMN COUNT
08C1 00 94000A84 S L K080 CHECK FOR 80 COLUMNS
08C3 00 4C5808DA BOSC L CNTOK,+-- CHECKED OK
08C5 00 4C680921 BOSC L MOD24,Z+ BRANCH LESS THAN 80
08C7 00 4C4008C9 BOSC L CLERR
08C9 00 C4000A7B CLERR LD L CLCNT LOAD COLUMN COUNT
*****
* WAIT 23 *
*
* MORE THAN 80 COLUMN INTERRUPTS RECEIVED *
* WHEN END OP INTERRUPT WAS GENERATED,NUMBER*
* OF COLUMN INTERRUPTS IS DISPLAYED IN A REG*
* PUSH START FOR SCOPE LOOP. *
*****
08CB 0 3023 MOD23 WAIT /23 MORE THAN 80 COLUMNS
08CC 0 6100 LDX 1 0 RESET COLUMN COUNT
08CD 00 6D000A7B STX L1 CLCNT
08CF 00 66800A9B LDX I2 MDYF4
08D1 00 6E0008CB STX L2 MOD23 ALLOW LOOP
08D3 00 4C400862 BOSC L CARDS BRANCH TO LOOP
*
08D5 0 6100 HOPIT LDX 1 0
08D6 00 6D000A7B STX L1 CLCNT RESET COLUMN COUNT
08D8 00 4C00085F BSC L LESS1
*
08DA 00 65003021 CNTOK LDX L1 /3021
08DC 00 6D000861 STX L1 MOD21 RESTORE WAIT 21
08DE 00 65003022 LDX L1 /3022

```

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3A808840
3A808850
3A808860
3A808870
3A808880
3A808890
3A808900
3A808910
3A808920
3A808930
3A808940
3A808950
3A808960
3A808970
3A808980
3A808990
3A809000
3A809010
3A809020
3A809030
3A809040
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3A809060
3A809070
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3A809090
3A809100
3A809110
3A809120
3A809130
3A809140
3A809150
3A809160
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3A809190
3A809200
3A809210
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3A809370
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3A809500
3A809510

```

INTERRUPT TEST

```

08E0 00 6D0008A9 STX L1 MOD22 RESTORE WAIT 22
08E2 00 65003023 LDX L1 /3023
08E4 00 6D0008CB STX L1 MOD23 RESTORE WAIT 23
08E6 00 65003024 LDX L1 /3024
08E8 00 6D000923 STX L1 MOD24+2 RESTORE WAIT 24
08FA 00 65003025 LDX L1 /3025
08EC 00 6D000938 STX L1 MOD25 RESTORE WAIT 25
08EE 00 65003026 LDX L1 /3026
08F0 00 6D00094D STX L1 MOD26 RESTORE WAIT 26
08F2 00 65003027 LDX L1 /3027
08F4 00 6D000962 STX L1 MOD27 RESTORE WAIT 27
08F6 00 65003028 LDX L1 /3028
08F8 00 6D000977 STX L1 MOD28 RESTORE WAIT 28
08FA 00 65003029 LDX L1 /3029
08FC 00 6D00098C STX L1 MOD29 RESTORE WAIT 29
08FE 00 C4000A7A LD L GDCNT LOAD CARD COUNT
0900 00 94000A82 S L K010 SUBTRACT 10
0902 00 4C100912 BSC L WAITA,- CHK NUMBER OF PASSES
0904 0 6100 LDX 1 0
0905 00 6D000A7B STX L1 CLCNT RESET COLUMN COUNT
0907 00 6D000A7C STX L1 LPCNT RESET LOOP CARD CNT
0909 00 0C000A66 XIO L BITSW SENSE BIT SWITCHES
090B 00 C4000A77 LD L BITS1 LOAD BIT SWITCHES
090D 0 180C SRA 12 CHK FOR WAIT 1 OPT
090E 00 4C040913 BSC L WAITA+1,E RESTORE/GO TO WAIT 1
0910 00 4C00082C BSC L SETUP+3 NOT 10 PASSES
*
* *****
* * WAIT 4 *
* * DEVICE TESTED, *
* * RAN SUCCESSFUL. *
* *****
* * RERUN *
* * TO RERUN PROGRAM PRESS START. *
* *****
0913 0 6100 LDX 1 0
0914 00 6D000A7B STX L1 CLCNT RESET COLUMN COUNT
0916 00 6D000A7A STX L1 GDCNT RESET CARD COUNT
0918 00 0C000A66 XIO L BITSW
091A 00 C4000A77 LD L BITS1
091C 0 180C SRA 12
091D 00 4C040502 MOD12 BSC L MAPIT,E
091F 00 4C0006AE BSC L CLRIX RERUN PROGRAM
*
* MOD24 LD L CLCNT LOAD COLUMN COUNT
* *****
* * WAIT 24 *
* * LESS THAN 80 COLUMN INTERRUPTS RECEIVED *
* * WHEN END OP INTERRUPT WAS GENERATED,NUMBER *
* * OF COLUMN INTERRUPTS IS DISPLAYED IN A REG *
* * PUSH START FOR SCOPE LOOP. *
* *****
0923 0 3024 WAIT /24
*
* LDX 1 0 RESET COLUMN COUNT
0924 0 6100
0925 00 6D000A7B STX L1 CLCNT
0927 00 66800A9C LDX I2 MDYF5
0929 00 6E000921 STX L2 MOD24 ALLOW LOOP
092B 00 4C000862 BSC L CARDS BRANCH TO LOOP
*
* INT01 DC 0 INTERRUPT 1
092D 0 0000
092E 00 0C000A58 XIO L SENSE
0930 00 C4000A7B LD L CLCNT LOAD COLUMN COUNT

```

```

3A809520
3A809530
3A809540
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3A809620
3A809630
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3A809650
3A809660
3A809670
3A809680
3A809690
3A809700
3A809710
3A809720
3A809730
3A809740
3A809750
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3A809770
3A809780
3A809790
3A809800
3A809810
3A809820
3A809830
3A809840
3A809850
3A809860
3A809870
3A809880
3A809890
3A809900
3A809910
3A809920
3A809930
3A809940
3A809950
3A809960
3A809970
3A809980
3A809990
3A810000
3A810010
3A810020
3A810030
3A810040
3A810050
3A810060
3A810070
3A810080
3A810090
3A810100
3A810110
3A810120
3A810130
3A810140
3A810150
3A810160
3A810170
3A810180
3A810190

```

INTERRUPT TEST

```

0932 00 6600092D LDX L2 INT01
0934 00 6F00000C STX L2 /000C
0936 00 4C400938 BOSC L MOD25
*
* *****
* * WAIT 25 *
* * INTERRUPT GENERATED,CAUSED A LEVEL 1 *
* * ADDRESS TO BE GENERATED. *
* * PUSH START FOR SCOPE LOOP. *
* *****
0938 0 3025 MOD25 WAIT /25 LEV 0 PICKED HIT 15
*
* LDX 1 0 RESET COLUMN COUNT
0939 0 6100
093A 00 6D000A7B STX L1 CLCNT
093C 00 66800A9D LDX I2 MDYF6 ALLOW LOOP
093E 00 6E000938 STX L2 MOD25 ALLOW LOOP
0940 00 4C000862 BSC L CARDS BRANCH TO LOOP
*
* INT02 DC 0 INTERRUPT 2
0942 0 0000
0943 00 0C000A58 XIO L SENSE
0945 00 C4000A7B LD L CLCNT LOAD COLUMN COUNT
0947 00 66000942 LDX L2 INT02
0949 00 6E00000C STX L2 /000C
094B 00 4C40094D BOSC L MOD26
*
* *****
* * WAIT 26 *
* * INTERRUPT GENERATED,CAUSED A LEVEL 2 *
* * ADDRESS TO BE GENERATED. *
* * PUSH START FOR SCOPE LOOP. *
* *****
094D 0 3026 MOD26 WAIT /26 LEV 0 PICKED BIT 14
*
* LDX 1 0 RESET COLUMN COUNT
094E 0 6100
094F 00 6D000A7B STX L1 CLCNT
0951 00 66800A9E LDX I2 MDYF7 ALLOW LOOP
0953 00 6E00094D STX L2 MOD26
0955 00 4C000862 BSC L CARDS BRANCH TO LOOP
*
* INT03 DC 0 INTERRUPT 3
0957 0 0000
0958 00 0C000A58 XIO L SENSE
095A 00 C4000A7B LD L CLCNT LOAD COLUMN COUNT
095C 00 66000957 LDX L2 INT03
095E 00 6E00000C STX L2 /000C
0960 00 4C400962 BOSC L MOD27
*
* *****
* * WAIT 27 *
* * INTERRUPT GENERATED,CAUSED A LEVEL 3 *
* * ADDRESS TO BE GENERATED. *
* * PUSH START FOR SCOPE LOOP. *
* *****
0962 0 3027 MOD27 WAIT /27 LEV 0 PICKED 14+15
*
* LDX 1 0 RESET COLUMN COUNT
0963 0 6100
0964 00 6D000A7B STX L1 CLCNT
0966 00 66800A9F LDX I2 MDYF8 ALLOW LOOP
0968 00 6E000962 STX L2 MOD27
096A 00 4C000862 BSC L CARDS BRANCH TO LOOP
*
* INT05 DC 0 INTERRUPT 5
096C 0 0000
096D 00 0C000A58 XIO L SENSE
096F 00 C4000A7B LD L CLCNT LOAD COLUMN COUNT
0971 00 6600096C LDX L2 INT05
0973 00 6E00000C STX L2 /000C

```

```

3A810200
3A810210
3A810220
3A810230
3A810240
3A810250
3A810260
3A810270
3A810280
3A810290
3A810300
3A810310
3A810320
3A810330
3A810340
3A810350
3A810360
3A810370
3A810380
3A810390
3A810400
3A810410
3A810420
3A810430
3A810440
3A810450
3A810460
3A810470
3A810480
3A810490
3A810500
3A810510
3A810520
3A810530
3A810540
3A810550
3A810560
3A810570
3A810580
3A810590
3A810600
3A810610
3A810620
3A810630
3A810640
3A810650
3A810660
3A810670
3A810680
3A810690
3A810700
3A810710
3A810720
3A810730
3A810740
3A810750
3A810760
3A810770
3A810780
3A810790
3A810800
3A810810
3A810820
3A810830
3A810840
3A810850
3A810860
3A810870

```

INTERRUPT TEST

```

0975 00 4C400977      ROSC L MOD28
*****
                      *
                      *      WAIT 28
                      *
* INTERRUPT GENERATED,CAUSED A LEVEL 5
* ADDRESS TO BE GENERATED.
* PUSH START FOR SCOPE LOOP.
*****
0977 0  3028          MOD28 WAIT /28      LEV 0 PICKED 13+15
*
0978 0  6100          LDX  1 0          RESET COLUMN COUNT
0979 00 6D000A7B      STX  L1 CLCNT
097B 00 66800AA0      LDX  L2 MODFY9      ALLOW LOOP
097D 00 6E000977      STX  L2 MOD28
097F 00 4C000862      BSC  L CARDS      BRANCH TO LOUP
*
0981 0  0000          ADR12 DC  0
0982 00 0C000A58      XIO  L SENSE
0984 00 4C000A7B      LD   L CLCNT
0986 00 66000981      LDX  L2 ADR12
0988 00 6E00000C      STX  L2 /000C
098A 00 4C40098C      BOSC L MOD29
*****
                      *
                      *      WAIT 29
                      *
* BIT 12 WAS DROPPED WHEN INTERRUPT LEVEL
* 0 WAS GENERATED.
* PUSH START FOR SCOPE LOOP.
*****
098C 0  3029          MOD29 WAIT /29      INT 0 DROPPED BIT 12
*
098D 0  6100          LDX  1 0          RESET COLUMN COUNT
098E 00 6D000A7B      STX  L1 CLCNT
0990 00 66800A99      LDX  L2 MODFY2      ALLOW LOOP
0992 00 6E00098C      STX  L2 MOD29
0994 00 4C000862      BSC  L CARDS      BRANCH TO LOOP
*
0996 00 4C0008D5      JUMP  BSC  L MOPIT
*
0998 00 0C000A66      CNTCK XIO  L BITSW      READ BIT SWITCHES
099A 00 4C000A77      LD   L BITS1          LOAD BIT SWITCHES
099C 00 4C0409AF      BSC  L KNT01,E        SELECT COUNT OF 10
099E 0  1801          SRA  1              CHK COUNT OF 50
099F 00 4C0409B7      BSC  L KNT02,E        SELECT COUNT OF 50
09A1 0  1801          SRA  1              CHK COUNT OF 250
09A2 00 4C0409BF      BSC  L KNT03,E        SELECT COUNT OF 250
09A4 0  1801          SRA  1              CHK COUNT OF 25000
09A5 00 4C0409C7      BSC  L KNT04,E        SEL COUNT OF 25000
09A7 00 65000A85      LDX  L1 K100
09A9 00 6D0006FE      STX  L1 NUMBR+1      SET UP CNT OF 100
09AB 00 05000723      STD  L1 NUMCK+1      SET UP LOOP COUNT
09AD 00 4C0009CF      BSC  L CKOVR
*
09AF 00 65000A82      KNT01 LDX  L1 K010
09B1 00 6D0006FE      STX  L1 NUMBR+1      SET UP CNT OF 10
09B3 00 05000723      STD  L1 NUMCK+1      SET UP LOOP COUNT
09B5 00 4C0009CF      BSC  L CKOVR
*
09B7 00 65000A83      KNT02 LDX  L1 K050
09B9 00 6D0006FE      STX  L1 NUMBR+1      SET UP CNT OF 50
09BB 00 05000723      STD  L1 NUMCK+1      SET UP LOOP COUNT
09BD 00 4C0009CF      BSC  L CKOVR
*
09BF 00 65000A86      KNT03 LDX  L1 K250
09C1 00 6D0006FE      STX  L1 NUMBR+1      SET UP CNT OF 250

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INTERRUPT TEST

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09C3 00 05000723      STO  L1 NUMCK+1      SET UP LOOP COUNT
09C5 00 4C0009CF      BSC  L CKOVR
*
09C7 00 65000A87      KNT04 LDX  L1 KMAX
09C9 00 6D0006FE      STX  L1 NUMBR+1      SET UP CNT OF 25000
09CB 00 05000723      STO  L1 NUMCK+1      SET UP LOOP COUNT
09CD 00 4C0009CF      BSC  L CKOVR
*
09CF 00 0C000A66      CKOVR XIO  L BITSW      READ BIT SWITCHES
09D1 00 4C000A77      LD   L BITS1          LOAD BIT SWITCHES
09D3 0  1804          SRA  4              DELAY CHANGE
09D4 00 4C0409E5      BSC  L NUDLY,E        NO DELAY SELECTE
09D6 0  1801          SRA  1              CHECK FOR DELAY
09D7 00 4C0409EB      BSC  L DLY01,E        SELECTED DELAY
09D9 0  1801          SRA  1              CHECK FOR DELAY
09DA 00 4C0409F1      BSC  L DLY02,E        SELECTED DELAY
09DC 0  1801          SRA  1              CHECK FOR DELAY
09DD 00 4C0409F7      BSC  L DLY03,E        SELECTED DELAY
09DF 00 65000A7D      LDX  L1 DELAY        SET DELAY FOR .5 SEC
09E1 00 6D0006E8      STX  L1 TEST1+1      SET UP DELAY
09E3 00 4C0006DB      BSC  L BUSY
*
09E5 00 65000A80      NODLY LDX  L1 K000      LOAD ZERO
09E7 00 6D0006E8      STX  L1 TEST1+1      SET UP NO DELAY
09E9 00 4C0006DB      BSC  L BUSY
*
09EB 00 65000A88      DLY01 LDX  L1 TIME1
09ED 00 6D0006E8      STX  L1 TEST1+1      SET UP DELAY
09EF 00 4C0006DB      BSC  L BUSY
*
09F1 00 65000A89      DLY02 LDX  L1 TIME2
09F3 00 6D0006E8      STX  L1 TEST1+1      SET UP DELAY
09F5 00 4C0006DB      BSC  L BUSY
*
09F7 00 65000A8A      DLY03 LDX  L1 TIME3
09F9 00 6D0006E8      STX  L1 TEST1+1      SET UP DELAY
09FB 00 4C0006DB      BSC  L BUSY
*
09FD 00 0C000A66      CNTIT XIO  L BITSW      READ BIT SWITCHES
09FF 00 4C000A77      LD   L BITS1          LOAD BIT SWITCHES
0A01 00 4C040A12      BSC  L CNT01,E        SEL CARD CNT OF 10
0A03 0  1801          SRA  1              CHK CARD CNT OF 50
0A04 00 4C040A18      BSC  L CNT02,E        SEL CARD CNT OF 50
0A06 0  1801          SRA  1              CHK CARD CNT OF 250
0A07 00 4C040A1E      BSC  L CNT03,E        SEL CARD CNT OF 250
0A09 0  1801          SRA  1              CHK CARD CNT OF 25K
0A0A 00 4C040A24      BSC  L CNT04,E        SEL CARD CNT OF 25K
0A0C 00 65000A82      LDX  L1 K010
0A0E 00 6D000872      STX  L1 TOTAL+1      SET UP CNT OF 10
0A10 00 4C000A2A      BSC  L ENDCK
*
0A12 00 65000A82      CNT01 LDX  L1 K010
0A14 00 6D000872      STX  L1 TOTAL+1      SET UP CNT OF 10
0A16 00 4C000A2A      BSC  L ENDCK
*
0A18 00 65000A83      CNT02 LDX  L1 K050
0A1A 00 6D000872      STX  L1 TOTAL+1      SET UP CNT OF 50
0A1C 00 4C000A2A      BSC  L ENDCK
*
0A1E 00 65000A86      CNT03 LDX  L1 K250
0A20 00 6D000872      STX  L1 TOTAL+1      SET UP CNT OF 250
0A22 00 4C000A2A      BSC  L ENDCK
*
0A24 00 65000A87      CNT04 LDX  L1 KMAX
0A26 00 6D000872      STX  L1 TOTAL+1      SET UP CNT OF 25000
0A28 00 4C000A2A      BSC  L ENDCK
*
0A2A 00 0C000A66      ENDCK XIO  L BITSW      READ BIT SWITCHES

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INTERRUPT TEST

0A2C 00 C4000A77	LD	L	BITS1	LOAD BIT SWITCHES	3A812240
0A2E 0 1804	SRA		4	DELAY CHANGE	3A812250
0A2F 00 4C040A40	BSC	L	DLYND,E	NO DELAY SELECTED	3A812260
0A31 0 1801	SRA		1	CHECK FOR DELAY	3A812270
0A32 00 4C040A46	BSC	L	DLAY1,E	SELECTED DELAY	3A812280
0A34 0 1801	SRA		1	CHECK FOR DELAY	3A812290
0A35 00 4C040A4C	BSC	L	DLAY2,E	SELECTED DELAY	3A812300
0A37 0 1801	SRA		1	CHECK FOR DELAY	3A812310
0A38 00 4C040A52	BSC	L	DLAY3,E	SELECTED DELAY	3A812320
0A3A 00 65000A7D	LGX	L1	DELAY	SET DELAY FOR .5 SEC	3A812330
0A3C 00 6D000858	STX	L1	START+1	SET UP DELAY	3A812340
0A3E 00 4C000868	BSC	L	RETRN		3A812350
*					
0A40 00 65000A80	DLYND	LX	L1 K000	LOAD ZERO	3A812360
0A42 00 6D000858	STX	L1	START+1	SET UP NO DELAY	3A812370
0A44 00 4C000868	BSC	L	RETRN		3A812380
*					
0A46 00 65000A88	DLAY1	LX	L1 TIME1		3A812390
0A48 00 6D000858	STX	L1	START+1	SET UP DELAY	3A812400
0A4A 00 4C000868	BSC	L	RETRN		3A812410
*					
0A4C 00 65000A89	DLAY2	LX	L1 TIME2		3A812420
0A4E 00 6D000858	STX	L1	START+1	SET UP DELAY	3A812430
0A50 00 4C000868	BSC	L	RETRN		3A812440
*					
0A52 00 65000A8A	DLAY3	LX	L1 TIME3		3A812450
0A54 00 6D000858	STX	L1	START+1	SET UP DELAY	3A812460
0A56 00 4C000868	BSC	L	RETRN		3A812470
*					
0A58 0000	BSS	E	0		3A812480
0A58 0 0000	SENSE	DC	0	RESET DSM	3A812490
0A59 0 1703	DC		/1703		3A812500
0A5A 0 0000	SENPT	DC	0		3A812510
0A5B 0 1F01	DC		/1F01		3A812520
0A5C 0 0000	SEN25	DC	0	SENSE 2501 DSM	3A812530
0A5D 0 4F03	DC		/4F03		3A812540
0A5E 0 0000	DISK	DC	0		3A812550
0A5F 0 2701	DC		/2701		3A812560
0A60 0 0000	PLOT	DC	0		3A812570
0A61 0 2F01	DC		/2F01		3A812580
0A62 0 0000	PRINT	DC	0		3A812590
0A63 0 3701	DC		/3701		3A812600
0A64 0 0000	CONSL	DC	0		3A812610
0A65 0 0F01	DC		/0F01		3A812620
0A66 0 0A77	BITSM	DC	BITS1		3A812630
0A67 0 3A00	DC		/3A00		3A812640
0A68 0 0000	STOP	DC	0		3A812650
0A69 0 3F01	DC		/3F01		3A812660
0A6A 0 0000	FEED	DC	0		3A812670
0A6B 0 1402	DC		/1402		3A812680
0A6C 0 0A6E	FEEDS	DC	TABLE		3A812690
0A6D 0 4E00	DC		/4E00		3A812700
0A6E 0 0001	TABLE	DC	1		3A812710
0A6F 0 0000	DC		0		3A812720
0A70 0 0000	RESTR	DC	0		3A812730
0A71 0 1404	DC		/1404	READER START	3A812740
0A72 0 0000	CNTRL	DC	0		3A812750
0A73 0 1C00	DC		/1C00	ADVANCE TAPE	3A812760
0A74 0 0A76	READ	DC	RAREA		3A812770
0A75 0 1200	DC		/1200		3A812780
0A76 0001	RAREA	BSS	1		3A812790
0A77 0 0000	BITS1	DC	0	BIT SWITCH SETTINGS	3A812800
0A78 0 0000	BITS2	DC	0	LAST DEVICE SELECTED	3A812810
0A79 0 0000	BITS3	DC	0	LEVEL ON BITS	3A812820
0A7A 0 00C0	GDCMT	DC	0	GOOD PASS COUNT	3A812830
0A7B 0 0000	CLCNT	DC	0	COLUMN COUNT	3A812840
0A7C 0 0000	LPCMT	DC	0	LOOP COUNT	3A812850
0A7D 0 F700	DELAY	DC	/F700	SCOPE LOOP DELAY	3A812860

INTERRUPT TEST

0A7E 0 0000	DSW1	DC	0		3A812920
0A7F 0 0001	ADD01	DC	1		3A812930
0A80 0 0000	K000	DC	0	CONSTANT ZERO	3A812940
0A81 0 0001	K001	DC	1	CONSTANT 1	3A812950
0A82 0 000A	K010	DC	10	CONSTANT 10	3A812960
0A83 0 0032	K050	DC	50	CONSTANT 50	3A812970
0A84 0 0050	K080	DC	80	CONSTANT 80	3A812980
0A85 0 0064	K100	DC	100	CONSTANT 100	3A812990
0A86 0 00FA	K250	DC	250	CONSTANT 250	3A813000
0A87 0 61A8	KMAX	DC	/61A8	CONSTANT 25000	3A813010
0A88 0 0DE0	TIME1	DC	/0DE0	DELAY - 62.5 MSEC	3A813020
0A89 0 1EE0	TIME2	DC	/1FE0	DELAY - 125 MSEC	3A813030
0A8A 0 3DC0	TIME3	DC	/3DC0	DELAY - 250 MSEC	3A813040
0A8B 0 1000	NOPIT	DC	/1000		3A813050
0A8C 0 1801	SRA01	DC	/1801		3A813060
0A8D 0 180A	SPA10	DC	/180A		3A813070
0A8E 0 180B	SRA11	DC	/180B		3A813080
0A8F 0 70E9	MOFYA	MDX	X	BUSY-MOD11-1	3A813090
0A90 0 707B	MOFYB	MDX	X	GAPIT-MOD13-1	3A813100
0A91 0 706B	MOFYC	MDX	X	GAPIT-MOD14-1	3A813110
0A92 0 705B	MOFYD	MDX	X	GAPIT-MOD15-1	3A813120
0A93 0 704B	MOFYE	MDX	X	GAPIT-MOD16-1	3A813130
0A94 0 70F4	MOFYF	MDX	X	GAPIT-MOD17-1	3A813140
0A95 0 70D4	MOFYG	MDX	X	GAPIT-MOD18-1	3A813150
0A96 0 70C8	MOFYH	MDX	X	GAPIT-MOD19-1	3A813160
0A97 0 708C	MOFYJ	MDX	X	GAPIT-MOD1A-1	3A813170
0A98 0 701A	MOFYL	MDX	X	CKRUN-MOD11-1	3A813180
0A99 0 7009	MDFY2	MDX	X	JUMP-MOD29-1	3A813190
0A9A 0 7047	MDFY3	MDX	X	MOD22-MOD21-1	3A813200
0A9B 0 7009	MDFY4	MDX	X	HOPIT-MOD23-1	3A813210
0A9C 0 7083	MDFY5	MDX	X	HOPIT-MOD24-1	3A813220
0A9D 0 709C	MDFY6	MDX	X	HOPIT-MOD25-1	3A813230
0A9E 0 7087	MDFY7	MDX	X	HOPIT-MOD26-1	3A813240
0A9F 0 7033	MDFY8	MDX	X	JUMP-MOD27-1	3A813250
0AA0 0 701E	MDFY9	MDX	X	JUMP-MOD28-1	3A813260
0AA2 0 G500	END		BEGIN		3A813270

INTERRUPT TEST

CROSS REFERENCE LISTING

SYMBOL	VALUE	REFERENCES
ADD01	0A7F	06F9
AUR12	0981	0844,0986
BAD12	07DB	051A,05EA,0634,067C
BAD14	07E7	051E,05EC,0636,067E
BEGIN	0500	0AA1
BITSW	0A66	0528,053E,0613,065B,06A3,06E0,07AC,0850,0909,0918,0998,09CF,09FD,0A2A
BITS1	0A77	052D,0540,0615,065D,06A5,06E2,07AE,0852,090B,091A,099A,09D1,09FF,0A2C,0A66
BITS2	0A78	0530,0618,0660,06A8
BIT53	0A79	0543,0548
BUSY	06DB	05D6,05F6,0620,0640,0668,0688,06DE,0714,07D9,09E3,09E9,09EF,09F5,09FB,0A8F
BUZY	084B	084E,0875,087E
CARDS	0862	08D3,092B,0940,0955,096A,097F,0994
CHECK	0876	0873
CKBIT	0578	054A
CKDOK	07C7	05E8,0632,067A,0710
CKLOP	053E	061A,0662,06AA
CKOVR	09CF	09AD,09R5,09BD,09C5,09C0
CKRDY	087F	085B,0885
CKRUN	070C	06F1,0A98
CLCNT	0A7B	0876,087C,089A,08AF,08BF,08C9,08CD,08D6,0905,0914,0921,0925,0930,093A,0945,094F,095A,0964,096F,0979,0984,098E
CLERR	08C9	08C7
CLR1X	06AE	0552,07B3,091F
CNTCK	0998	0718
CNTIT	09FD	0869
CNTOK	08DA	0855,08C3
CNTRL	0A72	064A
CNT01	0A12	0A01
CNT02	0A18	0A04
CNT03	0A1E	0A07
CNT04	0A24	0A0A
COLGO	08A5	08A3
CONSL	0A64	0820
DELAY	0A7D	06E7,0857,09DF,0A3A
DISK	0A5E	0751
DLAY1	0A46	0A32
DLAY2	0A4C	0A35
DLAY3	0A52	0A38
DLYNO	0A40	0A2F
DLY01	09EB	09D7
DLY02	09F1	09DA
DLY03	09F7	09DD
DSWCK	07FF	05F0,05F2,05FC,05FE,063A,063C,0646,0648,0682,0684,068E,0690,06EC,0806
DSW1	0A7E	07FF,0804,080E,087F,0883,088C
ENDCK	0A2A	0A10,0A16,0A1C,0A22,0A28
ERRDR	071A	0718,07B5
FDCYC	0715	070B,0726,072E,07E5,07F1,07FD,081B
FEED	0A6A	0600,06EE
FEEDS	0A6C	0692
FINSH	07A8	060C,0610,0654,0658,069C,06A0
GAPIT	07B5	0A90,0A91,0A92,0A93,0A94,0A95,0A96,0A97
GDCNT	0A7A	06F5,0716,07A2,07A6,082A,0863,0885,08FE,0916
GOLOP	0554	0584,058E,0598,05A2,05AC,05B6
HOPIT	08D5	0996,0A9B,0A9C,0A9D,0A9E
INT00	0697	082C
INT01	092D	0830,0932
INT02	0942	0834,0947
INT03	0957	0838,095C
INT04	08B2	083C,089C
INT05	096C	0840,0971

INTERRUPT TEST

JUMP	0996	0A99,0A9F,0AA0
KMAX	0A87	09C7,0A24
KNT01	09AF	099C
KNT02	09B7	099F
KNT03	09BF	09A2
KNT04	09C7	09A5
K000	0A80	09E5,0A40
K001	0A81	071E,07A4,086D
K010	0A82	060A,07A8,0900,09AF,0A0C,0A12
K050	0A83	09B7,0A18
K080	0A84	08C1
K100	0A85	0604,064E,0696,06FD,0722,0871,09A7
K250	0A86	09BF,0A1E
LESS1	085F	0860,08A7,08DB
LOOPS	0574	0577,0582,0588,0592,059C,05A6,05B0
LOOP0	0730	0580
LOOP1	0740	0586,058A
LOOP2	0750	0590,0594
LOOP3	0760	059A,059E
LOOP4	081D	05A4,05A8
LOOP5	07B7	05AE,05B2
LPcnt	0A7C	06F7,06FB,071C,0720,072C,0774,0819,086B,086F,087A,0907
MAPIT	05C2	073E,074E,075E,076E,07C5,0827,091D
MDFY2	0A99	0990
MDFY3	0A9A	08A0
MDFY4	0A9B	08CF
MDFY5	0A9C	0927
MDFY6	0A9D	093C
MDFY7	0A9E	0951
MDFY8	0A9F	0966
MDFY9	0AA0	097B
MOD1A	07F8	06C5,07A0,07F6,07FB,0A97
MOD11	06F1	06F3,0709,070F,0778,07D3,0A8F,0A98
MOD12	091D	0568
MOD13	0739	0556,056A,06B7,06C9,0737,073C,0784,0A90
MOD14	0749	055A,056C,06B9,06CD,0747,074C,0788,0A91
MOD15	0759	055E,056E,06B8,06D1,0757,075C,078C,0A92
MOD16	0769	0562,0570,06BD,06D5,0767,076C,0790,0A93
MOD17	07C0	0566,0572,06BF,06D9,0794,07BE,07C3,0A94
MOD18	07E0	06C1,0798,07DE,07E3,0A95
MOD19	07EC	06C3,079C,07EA,07EF,0A96
MOD20	0826	0824
MOD21	0861	0867,08A2,08B1,08B9,08DC,0A9A
MOD22	08A9	08AC,08BD,08E0,0A9A
MOD23	08CB	08D1,08E4,0A9B
MOD24	0921	08C5,08E8,0929,0A9C
MOD25	0938	06EC,0936,093E,0A9D
MOD26	094D	08F0,094B,0953,0A9E
MOD27	0962	08F4,0960,0968,0A9F
MOD28	0977	08F8,0975,097D,0AA0
MOD29	098C	08FC,098A,0992,0A99
MOFYA	0A8F	07D1
MOFYB	0A90	073A
MOFYC	0A91	074A
MOFYD	0A92	075A
MOFYE	0A93	076A
MOFYF	0A94	07C1
MOFYG	0A95	07E1
MOFYH	0A96	07ED
MOFYJ	0A97	07F9
MOFYL	0A98	0776
NOADR	07F3	0522,05EE,0638,0680
NODLY	09E5	09D4
NOPIT	0A8B	05F8,068A
NURDY	0892	08BE
NRDYA	05BE	05BA
NRDYB	05C8	05C4

INTERRUPT TEST

MRDYC	05D1	05CD
NUMBR	06FD	0606,0650,0698,09A9,09B1,09B9,09C1,09C9
NUMCK	0722	0608,0652,069A,06B5,09AB,09B3,09B8,09C3,09CB
PLOT	0A60	0761
PRINT	0A62	0741
RAREA	0A76	0A74
READ	0A74	08A5
RESET	0848	
RESTR	0A70	085D
RETRN	066B	0A3E,0A44,0A4A,0A50,0A56
RUNCK	06F0	C708,070E,077C,07CF
RUNUK	J701	070A,0780
SENPT	0A5A	05C1,061E,0731,0822
SENSE	0A58	058R,05D4,06DB,06E9,0729,0735,0745,0755,0765,0771, 078C,07C8,07DC,07E8,07F4,0801,080A,081E,084B,0859, 0881,0889,0893,0898,08B3,092E,0943,0958,096D,0982
SEN25	0A5C	05CB,0666
SETPT	061E	05C6
SETUP	0829	060E,07AA,0910
SET25	0666	05CF
SET42	05D4	058C
SRA01	0A8C	05F4,0686
SRA10	0A8D	0642
SRA11	0A8E	063E
START	0857	0887,0890,0895,0A3C,0A42,0A48,0A4E,0A54
STOP	0A68	0788
TABLE	0A6E	0A6C
TEST1	06E7	05D8,05FA,0602,0622,0644,064C,066A,068C,0694,0808, 0812,0815,09E1,09E7,09ED,09F3,09F9
TIME1	0A88	09E8,0A46
TIME2	0A89	09F1,0A4C
TIME3	0A8A	09F7,0A52
TOTAL	0871	0A0E,CA14,0A1A,0A20,0A26
VECT0	0580	0546
VECT1	0586	057E
VECT2	0590	054D
VECT3	059A	0579
VECT4	05A4	0550
VECT5	05AE	057C
VEC00	0734	0502,05DC,0626,066E,0733
VEC01	0744	0506,05DE,0628,0670,0743
VEC02	0754	050A,05E0,062A,0672,0753
VEC03	0764	050E,05E2,062C,0674,0763
VEC04	0770	0512,05E4,062E,0676,06B1,06E5,0702,0705
VEC05	0788	0516,05E6,0630,0678,078A
WAITA	0912	0656,069E,0781,0902,090E
WAITC	07CC	07CA
WAITF	0501	
WAITG	0728	05DA,0624,066C,0724
WAIT1	0527	052A,0575
WAIT2	0817	06FF
WAIT3	0814	0810
WAIT8	0538	
WHAT1	0588	0539
WHAT2	05C1	0536
WHAT3	05C8	0533
WHICH	0528	0526,053C,05BF,05C9,05D2,061C,0664,06AC

CE UTILITY PROGRAMS

1130 ON LINE DISK ADJUSTMENT PROGRAM

1. PURPOSE

```

***** 30A00020
* 30A00030
* THE 1130 DISK ACCESS PROGRAM WAS DESIGNED TO BE 30A00040
* USED WITH THE ACCESS ADJUSTMENT PROCEDURE FOUND 30A00050
* IN THE SDS MAINTENANCE MANUAL. 30A00060
* 30A00070
* THE PROGRAM WILL MOVE THE CARRIAGE BETWEEN 30A00080
* TRACKS 2 AND 200, AND COMPARE SECTOR ZERO 30A00090
* ADDRESSES AT THOSE TRACKS. 30A00100
* 30A00110
* THE SEEK OPERATION CAN BE SELECTED IN EITHER 10 30A00120
* OR 20 MILL MODE. 30A00130
* 30A00140

```

2. REQUIREMENTS

```

***** 30A00150
* 30A00160
* THE C.E. MUST HAVE A 1130 SYSTEM WITH CARD 30A00170
* READER OR PAPER TAPE INPUT. 30A00180
* 30A00190
* THE CARD READER PROGRAM CONSISTS OF 4 CARDS. 30A00200
* THE 1ST CARD IS AN IPL LOADER, THE OTHER 3 30A00210
* ARE PUNCHED IN 8/8 FORMAT AND CONTAINS THE 30A00220
* MAIN PORTION OF THE PROGRAM. 30A00230
* 30A00240

```

3. USE PROCEDURE

3.1 SETUP AND START

```

***** 30A00250
* 30A00260
* A. LOAD PROGRAM IN READER AND MAKE READER 30A00270
* READY. ADD A BLANK CARD. 30A00280
* 30A00290
* B. DEPRESS RESET AND PROGRAM LOAD PUSH 30A00300
* BUTTONS. PROGRAM WILL STOP AT WAIT 0. 30A00310
* 30A00320
* C. AT WAIT 0, ENTER DISK DRIVE AREA CODE OF 30A00330
* DESIRED DRIVE IN CONSOLE BIT SWITCHES 30A00340
* 0 THRU 4 AND CLEAR BITS 5 THRU 15. 30A00350
* 30A00360
* DRIVE BIT SW SETTING 30A00370
* 0...../2000 30A00380
* 1...../8800 30A00390
* 2...../9000 30A00400
* 3...../9800 30A00410
* 4...../A000 30A00420
* 30A00430

```

3.2 OPERATION

```

***** 30A00460
* 30A00470
* THE PROGRAM WILL START OUT IN 20 MILL MODE. 30A00480
* 30A00490
* THE CARRIAGE WILL SEEK HOME, GO TO TRACK 2, 30A00500
* READ SECTOR ZERO AND COMPARE FOR TRACK ADDR. 2 30A00510
* 30A00520
* A GOOD COMPARE CAUSES THE CARRIAGE TO GO TO 30A00530
* TRACK 200, WHERE SECTOR ZERO IS READ AND 30A00540
* COMPARED FOR TRACK ADDR. 200 30A00550
* 30A00560
* A GOOD COMPARE WILL CAUSE THE CARRIAGE TO GO 30A00570
* BACK TO TRACK 2 AND REPEAT ABOVE OPERATION. 30A00580
* 30A00590
* IF A COMPARE ERROR IS DETECTED, AN ERROR WAIT 30A00600
* ENCOUNTERED. SEE ERROR WAITS....(3.3). 30A00610
* 30A00620
* TO STOP PROGRAM, DEPRESS IMMEDIATE STOP. 30A00630
* 30A00640
* TO START PROGRAM, DEPRESS START. 30A00650
* 30A00660
* TO CHANGE FROM 20 MILL MODE OPERATION TO 10 30A00670
* MILL OPERATION, OR FROM 10 MILL OPERATION TO 30A00680
* 20 MILL OPERATION, A. DEPRESS IMMEDIATE STOP. 30A00690

```

CE UTILITY PROGRAMS

1130 ON LINE DISK ADJUSTMENT PROGRAM

```

* B. DEPRESS PROGRAM RESET. 30A00700
* C. DEPRESS START. 30A00710
* 30A00720

```

3.3 WAITS

```

/3000 * ENTER DISK DRIVE AREA CODE. ( SEE 3.1 C ) 30A00750
* 30A00760

```

ERROR WAITS

```

/30F1 * THE ADDRESS OF TRACK 2, SECTOR ZERO WAS READ 30A00770
* AND FOUND INVALID. 30A00780
* 30A00790
* 30A00800
* 30A00810
* CHECK IF CARRIAGE IS SETTING AT DETENT 2. 30A00820
* 30A00830
* IF CARRIAGE IS 'NOT' IN CORRECT DETENT, 30A00840
* DEPRESS START TO CONTINUE ADJUSTMENT. 30A00850
* 30A00860
* IF CARRIAGE IS IN CORRECT DETENT, DO A SECTOR 30A00870
* REWRITE. ***** 30A00880
* ***** CAUTION ***** 30A00890
* ***** 30A00900
* 30A00910
* * ONLY USE TRACK 2 REWRITE OPTION * 30A00920
* * WHEN SETTING AT WAIT /30F1. * 30A00930
* * 30A00940
* * REWRITE OPTION WILL DESTROY * 30A00950
* * ORIGINAL SECTOR DATA. * 30A00960
* * 30A00970
* ***** 30A00980
* 30A00990

```

```

* A. LOAD I REG TO /0043. 30A01000
* B. PLACE CONSOLE SW IN RUN. 30A01010
* C. DEPRESS START. 30A01020
* 30A01030

```

/30F2

```

* THE ADDRESS OF TRACK 200, SECTOR ZERO WAS READ 30A01040
* AND FOUND INVALID. 30A01050
* 30A01060
* 30A01070
* 30A01080
* CHECK IF CARRIAGE IS SETTING AT DETENT 200. 30A01090
* 30A01100
* IF CARRIAGE IS 'NOT' IN CORRECT DETENT, 30A01110
* DEPRESS START TO CONTINUE ADJUSTMENT. 30A01120
* 30A01130
* IF CARRIAGE IS IN CORRECT DETENT, DO A SECTOR 30A01140
* REWRITE. ***** 30A01150
* ***** CAUTION ***** 30A01160
* ***** 30A01170
* * ONLY USE TRACK 200 REWRITE OPTION * 30A01180
* * WHEN SETTING AT WAIT /30F2. * 30A01190
* * 30A01200
* * REWRITE OPTION WILL DESTROY * 30A01210
* * ORIGINAL SECTOR DATA. * 30A01220
* * 30A01230
* * 30A01240
* ***** 30A01250
* 30A01260
* A. LOAD I REG TO /0046. 30A01270
* B. PLACE CONSOLE SW IN RUN. 30A01280
* C. DEPRESS START. 30A01290
* 30A01300

```

/30F3

```

* LOST INTERRUPT WHILE READING IN PROGRAM. 30A01310
* 30A01320
* 30A01330
* 30A01340

```

3.4 TERMINATION

```

***** 30A01350
* TO TERMINATE PROGRAM DEPRESS IMMEDIATE STOP. 30A01360
* 30A01370

```

CE UTILITY PROGRAMS

CE UTILITY PROGRAMS

1130 ON LINE DISK ADJUSTMENT PROGRAM

1130 ON LINE DISK ADJUSTMENT PROGRAM

```

*
4 PRINTOUTS * 30A01380
* 30A01390
* 30A01400
* NONE 30A01410
* 30A01420
5 COMMENTS ***** 30A01430
* 30A01440
* TO RERUN PROGRAM ON ANOTHER DRIVE, PROGRAM MUST
* BE RELOADED. 30A01450
* 30A01460
* 30A01470
***** 30A01480
ABS 30A01490
ORG 0 30A01500
* 30A01510
***** 30A01520
* 30A01530
* 3 CARD LOADER PROGRAM * 30A01540
* 30A01550
***** 30A01560
* 30A01570
0000 0 603B BGN LDX BUILD GO BUILD IOCCS
* LDX PROGM IF P.T.
DSW DC *-# CARD RD IN AREA
0001 0 0000 DC *-#
0002 0 0000 DC
0003 0 8818 DC /B818 IOCC-SENSE/RESET DSW
0004 0 0000 RDIN DC *-# COL RD IN ADDR
0005 0 4800 DC /4800 IOCC-READ COLUMN
0006 0 0001 ONE DC 1 CONSTANT 1
0007 0 0004 FOUR DC 4 CONSTANT 4
0008 0 000E RDCRD DC INT RDR INTERRUPT ADDR
0009 0 2808 DC /2808 IOCC-START READER
000A 0 003D DC INT2 DISK INTERRUPT ADDR
000B 0 0003 LAST DC 3 LOADER CARD COUNT
000C 0 000E DC INT READER INTERRUPT ADD
000D 0 0034 DC INT5 PROG STOP INTERRUPT
*
000E 0 0000 INT DC *-# READER INTERRUPT
000F 0 08F2 XIO DSW * SERVICE ROUTINE
0010 0 4850 BOSC - *
0011 0 7001 MDX INT1 BR IF NOT RESPONSE
0012 0 7005 MDX WAITI&1 BR IF RESPONSE
0013 0 4848 INT1 BOSC & RESET OP COMPLETE
0014 0 0000 DC
0015 0 7011 MDX ENCRD BR, END OF CARD
0016 0 08F1 XIO RDCRD START READER
*
0017 0 30F3 WAITI WAIT -/D WAIT FOR INTERRUPT
0018 0 08EB XIO RDIN RD COL. ONE-HALF WD
0019 0 C0EA LD RDIN *
001A 0 F0EB EOR ONE SW READ/IN AREA, EVN
001B 0 D0E8 STO RDIN * COLS. IN 0, ODD IN 1
001C 0 4820 BSC Z CHK BOTH HALVES IN
001D 0 70F9 MDX WAITI NO, WAIT 2ND HALF
001E 0 C0E1 LD BGN YES, PACK BOTH HAVES
001F 0 1808 SRA 8 *
0020 0 F0E0 EOR BGN&1 *
*
0021 0 00D4 STORE DC /00D4 1ST WORD OF STO L
0022 0 003B DC BUILD 2ND WORD OF STO L
0023 0 C0FE LD STORE&1 SET UP NEXT STORE
0024 0 80E1 A ONE * ADDRESS
0025 0 D0FC STO STORE&1 *
0026 0 70F0 MDX WAITI GO WAIT FOR NEXT COL
*
0027 0 C0E3 ENCRD LD LAST CHK FOR LAST CARD
0028 0 90DD S ONE LOADED
0029 0 D0E1 STO LAST *
002A 0 4808 BSC & *

```

```

002B 0 6030 LDX PROGM YES, BRANCH TO PROG
*
LD STORE&1 NO, SET UP NEXT READ
S FOUR * IN AREA
STO STORE&1 *
MDX WAITI-1 GO READ NEXT CARD
*
PROGM LDD RESRT * SET AREA CODE IN
STD BGN ** BIT SWITCHES
DC /3000 **
MDX AGAN1-2 *
*
INT5 DC *-# *
XIO SPDSW ** PROGRAM STOP
LDX INT5A * INTERRUPT ROUTINE
DC
DC
*
BUILD LD DSW&1 BUILD SENSE DSW
SRA 3 *****
STO DSW&1 * NOTE *
LD RDCRD&1 * INSTRUCTIONS FROM*
SRA 1 * BUILD THRU INT5A *
STO RDCRD&1 * DO NOT APPEAR ON *
LD RDIN&1 * PAPER TAPE *
SRA 2 *****
STO RDIN&1 *
LD STORE *
SLA 8 *
STO STORE *
LDX WAITI-1 GO START READER
*****
*
ORG BUILD
*****
*
DISK ADJUSTMENT PROGRAM *
*****
*
INT5A BOSC I INT5 EXIT TO RETURN
*
INT2 DC *-# *
XIO SNDSW ** DISK INTERRUPT
BOSC L TEST&2 * ROUTINE
*
TOGGL DC *-# MODE TOGGLE
AREA DC *-# CURRENT AREA CODE
*
WTTWO XIO WRT02 * WRITE ADDRESS AT
BSI TEST * TRACK 2
MDX SKHME *
*
WTHND XIO WRT20 * WRITE ADDRESS AT
BSI TEST * TRACK 200
*
SKHME XIO HOME * GO HOME
BSI TEST *
XIO TRK2 ** GO TO TRACK
BSI TEST ** 2
MDX CHCK2 *
*
LDX 2 16 *
XIO RDSPS **
AGAN1 LD 2 SNDSW-1 *
OR AREA * * SET AREA CODE

```

```

30A02060
30A02070
30A02080
30A02090
30A02100
30A02110
30A02120
30A02130
30A02140
30A02150
30A02160
30A02170
30A02180
30A02190
30A02200
30A02210
30A02220
30A02230
30A02240
30A02250
30A02260
30A02270
30A02280
30A02290
30A02300
30A02310
30A02320
30A02330
30A02340
30A02350
30A02360
30A02370
30A02380
30A02390
30A02400
30A02410
30A02420
30A02430
30A02440
30A02450
30A02460
30A02470
30A02480
30A02490
30A02500
30A02510
30A02520
30A02530
30A02540
30A02550
30A02560
30A02570
30A02580
30A02590
30A02600
30A02610
30A02620
30A02630
30A02640
30A02650
30A02660
30A02670
30A02680
30A02690
30A02700
30A02710
30A02720
30A02730

```

CE UTILITY PROGRAMS

1130 ON LINE DISK ADJUSTMENT PROGRAM

```

0051 0 D273      STO 2 SNDSW-1  * * INTO IOCC
0052 0 72FE      MDX 2 -2      * *
0053 0 70FB      MDX      AGAN1   **
0054 0 70F3      MDX      SKHME   *
*
0055 0 C0EB      ONWDO LD      TOGGL   *
0056 0 4C20 005E BSC L  ONWD1,Z  ** BR IF 10 MIL MODE
0058 0 C01B      LD      SNDSW   * *
0059 0 D026      STO      TWHND   * *
005A 0 D027      STO      TWO     * *
005B 0 6201      LDX 2 1      * *
005C 0 6301      LDX 3 1      * * SET PROPER
005D 0 7006      MDX      CMND1   * * MODE
005E 0 6201      ONWD1 LDX 2 1   * *
005F 0 6A20      STX 2 TWHND  * *
0060 0 6A21      STX 2 TWO     * *
0061 0 C012      LD      SNDSW   **
0062 0 D09F      STO      BGN&2   *
0063 0 D09F      STO      BGN&3   *
*
0064 0 081B      CMND1 XIO     TWHND   *
0065 0 4024      BSI      TEST    ** GO TO TRACK 200
0066 0 72FF      MDX 2 -1      **
0067 0 70FC      MDX      CMND1   *
0068 0 0811      XIO      READ    *
0069 0 4020      BSI      TEST    **
006A 0 C037      LD      INPUT&1  * *
006B 0 F01D      EOR      OUT20&1 * * READ/COMPARE
006C 0 4C18 0091 BSC L  CMND2,&-  * * ADDR AT TRK 200
006E 0 30F2      DC      /30F2   ** ERROR, DID NOT
006F 0 70D8      MDX      SKHME   * COMPARE
*
0070 0000      BSS E
0070 0 4C00 009D RESRT BSC L  RSTRT  MODE CHANGE SET/UP
0072 0 0000      SPDSW DC
0073 0 3F01      DC      /3F01   IOCC-SENSE RESET (5)
0074 0 00C6      SNDSW DC      198   CONSTANT 198
0075 0 0701      DC      /0701   IOCC-SENSE/RESET DSW
0076 0 0086      WRT02 DC      OUT02  IOCC-WRITE TRACK 2
0077 0 0500      DC      /0500
0078 0 0088      WRT20 DC      OUT20  IOCC-WRITE TRACK 200
0079 0 0500      DC      /0500
007A 0 00A1      READ  DC      INPUT  IOCC-READ ADDRESS
007B 0 0600      DC      /0600
007C 0 00CA      HOME  DC      202   IOCC-SEEK HOME
007D 0 0404      DC      /0404
007E 0 0002      TRK2  DC      2     IOCC-GO TO TRK 2
007F 0 0400      DC      /0400
0080 0 0000      TWHND DC      *-*
0081 0 0400      DC      /0400   IOCC-GO TO TRK 200
0082 0 0000      TWO  DC      *-*
0083 0 0404      DC      /0404   IOCC-BACK TO TRK 2
0084 0 0042      RDSPS DC      AREA  IOCC-READ BIT SWS
0085 0 3A00      DC      /3A00   WRT TRK 2 TABLE
0086 0 0001      OUT02 DC      1     *
0087 0 0010      DC      /0010
0088 0 0001      OUT20 DC      1     WRT TRK 200 TABLE
0089 0 0640      DC      /0640   *
*
008A 0 0000      TEST  DC      *-*   *
008B 0 08E8      XIO   SNDSW   **
008C 0 180D      SRA   13     * * CHECK FOR FILE
008D 0 4804      BSC   E      * * READY
008E 0 70FC      MDX   TEST&1 **
008F 0 4C80 008A BSC I  TEST   *
*
0091 0 08F0      CMND2 XIO     TWO     *
0092 0 40F7      BSI   TEST    * GO TO TRACK 2
    
```

CE UTILITY PROGRAMS

1130 ON LINE DISK ADJUSTMENT PROGRAM

```

0093 0 73FF      MDX 3 -1      *
0094 0 70FC      MDX      CMND2   *
0095 0 08E4      CHCK2 XIO     READ    *
0096 0 40F3      BSI      TEST    **
0097 0 C00A      LD      INPUT&1  * *
0098 0 F0EE      EOR      OUT02&1 * * READ/COMPARE
0099 0 4C18 0055 BSC L  ONWDO,&-  * * ADDR AT TRK 2
009B 0 30F1      DC      /30F1   ** ERROR, DID NOT
009C 0 70AB      MDX      SKHME   * COMPARE
*
009D 0 C0A3      RSTRT LD      TOGGL   *
009E 0 F0E7      EOR      OUT02   ** CHANGE MODE
009F 0 D0A1      STO      TOGGL   **
00A0 0 70A7      MDX      SKHME   *
*
00A1 0 0002      INPUT DC      2     INPUT AREA
00A2 0002      BSS 2
00A4 0000      END  BGN
NO STATEMENTS FLAGGED IN THE ABOVE ASSEMBLY
    
```

CE UTILITY PROGRAMS

1130 ON LINE DISK ADJUSTMENT PROGRAM

C R O S S R E F E R E N C E

NAME	VALUE	REFERENCES
AGAN1	004F	0033,0053
AREA	0042	0050,0084
BGN	0000	001E,0020,0031,0062,0063,00A4
BUILD	003B	0000,0022
CHCK2	0095	004C
CMND1	0064	005D,0067
CMND2	0091	006C,0094
DSW	0002	000F,003B,003D
ENCRD	0027	0015
FOUR	0007	002D
HOME	007C	0048
INPUT	00A1	006A,007A,0097
INT	000E	0008,000C
INT1	0013	0011
INT2	003D	000A
INT5	0034	000D,003B
INT5A	003B	0036
LAST	000B	0027,0029
ONE	0006	001A,0024,0028
ONWDO	0055	0099
ONWD1	005E	0056
OUT02	0086	0076,0098,009E
OUT20	0088	006B,0078
PROGM	0030	002B
RDCRD	0008	0016,003E,0040
RDIN	0004	0018,0019,001B,0041,0043
RDSPS	0084	004E
READ	007A	0068,0095
RESRT	0070	0030
RSTRT	009D	0070
SKHME	0048	0045,0054,006F,009C,00A0
SNDSW	0074	003E,004F,0051,0058,0061,008B
SPDSW	0072	0035
STORE	0021	0023,0025,002C,002E,0044,0046
TEST	008A	003F,0044,0047,0049,004B,0065,0069,008E,008F,0092,0096
TOGGL	0041	0055,009D,009F
TRK2	007E	004A
TWHND	0080	0059,005F,0064
TWO	0082	005A,0060,0091
WAITI	0017	0012,001D,0026,002F,0047
WRT02	0076	0043
WRT20	0078	0046
WTHND	0046	
WTTWD	0043	

END OF ASSEMBLY

----- LAST PAGE -----