Design Checklist for LTC388X Family of PSM Buck Current Mode Converters

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INTRODUCTION

Please follow this checklist to insure a working LTC388X Current Mode design. If you make any exceptions to these checks, please call your local LTC Field Application Engineer for advice.

POWER CIRCUIT

1. ☐ $INTV_{CC}$
    a. ☐ 10.0uF min bulk cap (10V X7R)
    b. ☐ 0.1uF ceramic to PGND
    c. ☐ If V_{IN} is below 6V, tie $INTV_{CC}$ to V_{IN} and add 1-2.2Ohm resistor between bulk C and 4.7uF at pin
    d. ☐ Do not drive externally
2. ☐ Output Filter
    a. ☐ Proper sized L that will not saturate or overheat
    b. ☐ Proper sized C that will give correct ripple voltage
    c. ☐ Acceptable DCR/ESR losses
3. ☐ Input Filter
    a. ☐ Use bulk and ceramic capacitor (X5R/X7R), locate ceramic next to MOSFETs
    b. ☐ Make sure input filter will not cause resonance with converter stage
4. ☐Current sensing and voltage sensing.
    a. ☐ DCR kelvin sensing lines, and R/C properly placed connected
    b. ☐ DCR V_{DCR} scaled properly
    c. ☐ DCR resistor divider if signal too large
    d. ☐ DCR Bias currents compensated with R
    e. ☐ DCR Bias current R has 1uF in parallel

f. □ Add pi filter when Rsensing

g. □ Route current sensing lines differentially

h. □ Route voltage sensing lines differentially

5. □ Temperature Sensing (Output Inductor)

    a. □ Make Sure the PNP sensing transistor is close to inductor

    b. □ 10.0nF ceramic filter capacitor at transistor

    c. □ Route temperature sensing differentially

6. □ Power MOSFET Switches

    a. □ Top switch optimized for switching losses (low Qgd)

    b. □ Bottom switch optimized resistive losses (low Rdson)

    c. □ Ensure gate threshold is logic level

7. □ Gate drive

    a. □ Add 1-5Ohm boost pin resistor to reduce switch ringing

8. □ Compensation

    a. □ Add R/C compensation components to ITH to SGND

    b. □ Filter C in parallel to compensation components on ITH pin to SGND

DIGITAL/LOGIC

1. □ Connect Logic/coordination signals

    a. □ Tie all ALERTB together; pull up to 3.3V with resistor

    b. □ Tie all SCL/SDA together; pull up to 3.3V with resistor

    c. □ Tie all SHARE_CLK together; pull up to 3.3V with resistor

    d. □ Tie all Run0/Run1 together; pull up to 3.3V with resistor

    e. □ Tie all GPIOB together; pull up to 3.3V with resister

    f. □ Tie all WP together; add one pull up resistor to 3.3V and one pull down resistor to ground

2. □ Addressing

    a. □ ASELs (double check correct values)

    b. □ Check for collision with other devices on the bus and any global addresses published in their datasheets (i.e. cannot use LTC4306)

    c. □ Check address is not 0x5A, 0x5B, 0x7C, or less than 0x10

d. □ Must have a single base address for in system programming

   i. It is recommended that you use 0xXF (i.e. 0x4F) as the single, common base address

   ii. You will need to program MFR_ADDRESS (command 0xE6) to this value (i.e. 0x4F)

   iii. Hardware ASELs on 3880/3 will set the lower nibble directly (0x40 to 0x4F in this example)

   iv. Hardware ASELS on 3887 will set lower nibble if one resistor used, or entire byte if two resistors are used.

3. □ Open Drain Pins

   a. □ GPIOn, SYNC, SHARE_CLOCK have 10K pull up to 3.3V

   b. □ SDA, SCL, SYNC, ALERT/ have 8.33K pull up to 3.3V

   c. □ Reduce pull up resistor size on above pins if stray C is large

   d. □ RUN pin should only be driven by open collector to prevent contention and high currents

   e. □ GPIOn should only be driven by open collector to prevent contention and high currents

4. RCONFIG PINS

   a. □ Resistor dividers to V2.5 and SGND

   b. □ 1% resistors

   c. □ Values match table entries

   d. □ ASEL values unique (between devices)

5. □ Use time base sequencing so faults can be shared as a FAULT bus using GPIOB. Event based sequencing requires configuring GPIOB as PGOOD which eliminates a shared FAULT bus.

6. □ Programming

   a. □ Add PFET to disconnect dongle 3.3V when VIN present

   b. □ Ensure VIN, V3.3, V2.5 are high impedance when dongle connected without VIN

   c. □ Do not use any body diodes between SDA/SCL from any slave device

7. □ Test and Validation

   a. □ Add 5Ohm bode plot insertion resistor or pads with shorting resistor

   b. □ Add VOUT/GND feed through for impedance measurement for rails that require PDN validation

8. □ Poly-Phase rails

   a. □ Tie all SNYC pins together

b. □ (LTC3880/3) For any given SYNC group, only **one chip** (we call this the frequency master) can specify a FREQUENCY_SWITCH value (i.e. 500kHz). All other chips must specify FREQUENCY_SWITCH=0x8000 ('External Clock')

c. □ (LTC3887) For any given SYNC group, set FREQUENCY_SWITCH to the same value, from 250Khz to 1000Khz). Only use external oscillator if there is an external clock chip.

d. □ Check RCONFIG for FREQ_CFG to make sure there is only one master and the phasing is set properly

e. □ Tie all ITH together – when using multiple devices for a single output and use one set of compensation components

f. Tie all VOUTs together

g. (LTC3887) Make sure only 1 part has the SYNC clocking enabled MFR_CONFIG_ALL bit 4 set to a 0, all other chips sharing the SYNC pin should disable the SYNC clocking.

9. □All faults acted upon (fault response is not 'ignore', especially in polyphase applications) should be propagated via MFR_GPIO_PROPAGATE on first power up

10. □ The MFR_GPIO RESPONSE should be inhibit on first power up

11. □ In MFR_PWM_CONFIG_LTC3880 SHARE_CLOCK_ENABLE set to a 1 (default setting)

12. □ In MFR_CHAN_CONFIG_LTC3880 ShareClkControl set to a 1 (default setting)

13. Run DRCs and make sure your configuration file is clean.

REVISION HISTORY

Rev	Date	Description	Page Number
1.1	6/2/15	Remove LTC3882. Improve polyphase rail items. Remove comments. Clean up text to improve accuracy.	All