AN10999

Application with TDA8035 - Demonstration board description

Rev. 1.0 — 1 February 2012 Application note

Document information

Info	Content
Keywords	TDA8035, Cake8035, Smart Card Interface, Pay TV, STB, ISO 7816-3, NDS
Abstract	The application note describes the Cake8035 demo board for TDA8035: schematics, layout and use of this board.

Revision history

Rev	Date	Description
1.0	20120201	First released version

Contact information

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1. Introduction

The TDA8035HN is proposed in HVQFN32 package.

In the document, the TDA8035HN will be referred as TDA8035.

This application board is a single board embedding the TDA8035, its capacitors, some connectors for external signals and a smart card connector.

This demonstration board is planned to be used as daughter board, plugged on a mother board embedding the correct connectors.

The evaluation mother board Cake80xxMBA can be purchased from NXP for evaluation purpose.

For a first evaluation, the board can also be connected to a microcontroller board with a few wires.

2. Hardware

The following pictures present the whole board:

- Electronic schematic
- Layout
- Components position

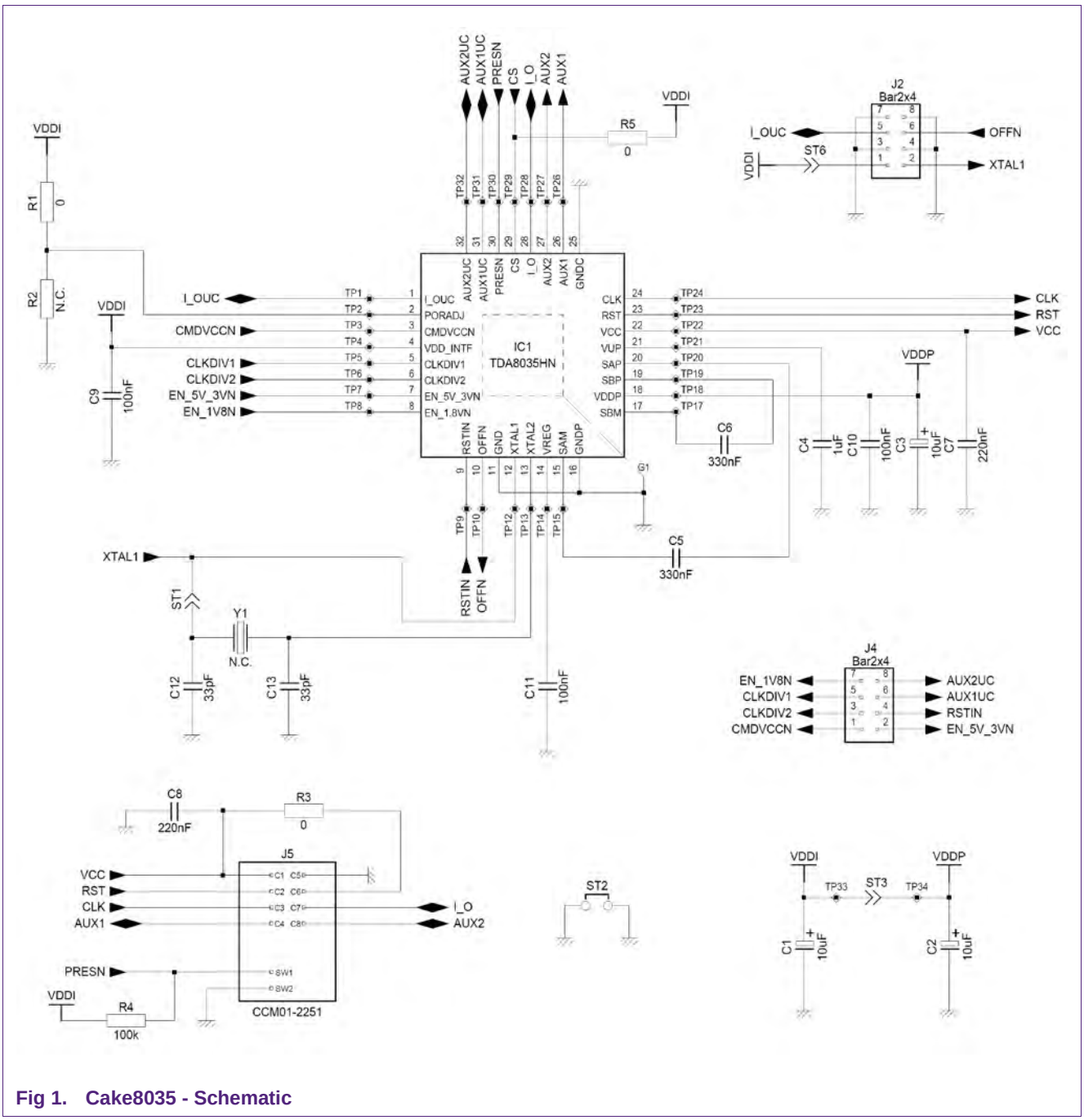

Fig 1. Cake8035 - Schematic

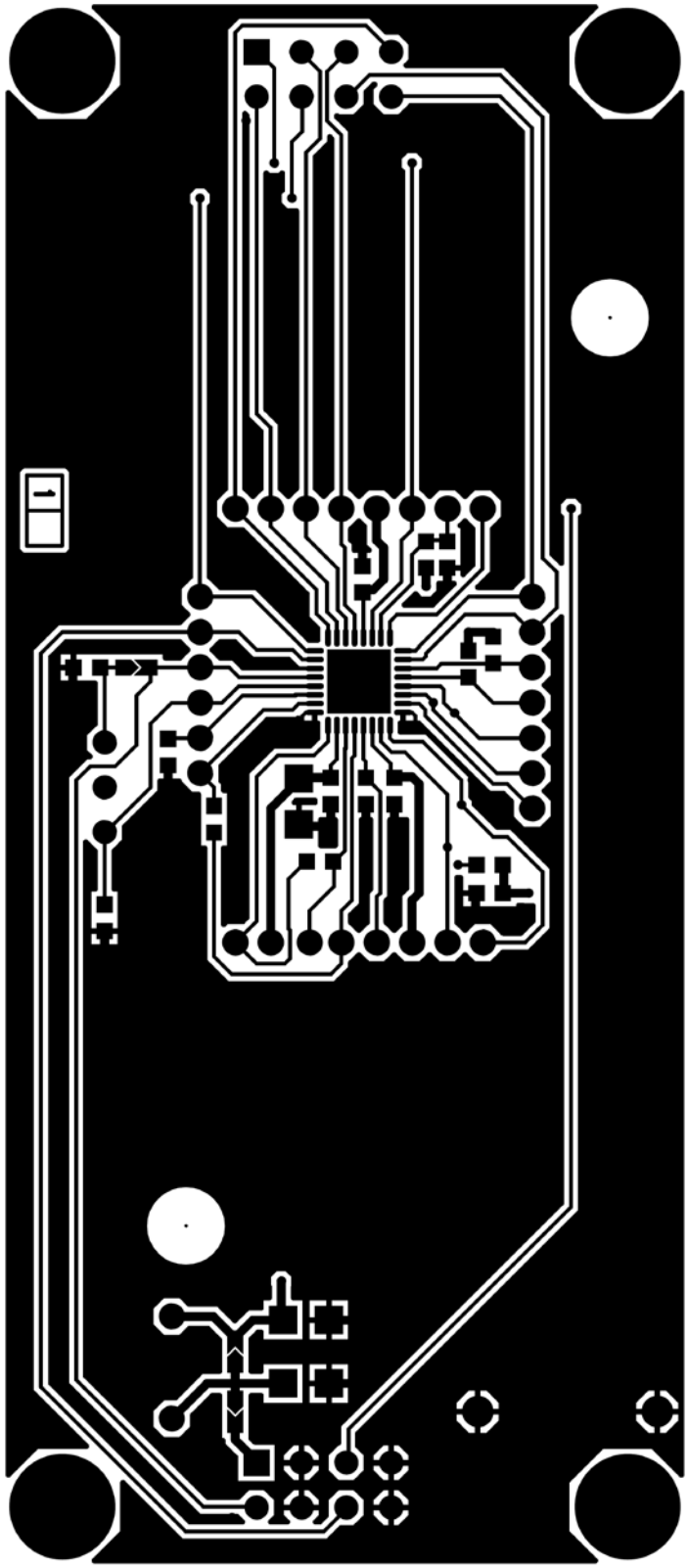

Fig 2. Cake8035 – Layout Top view

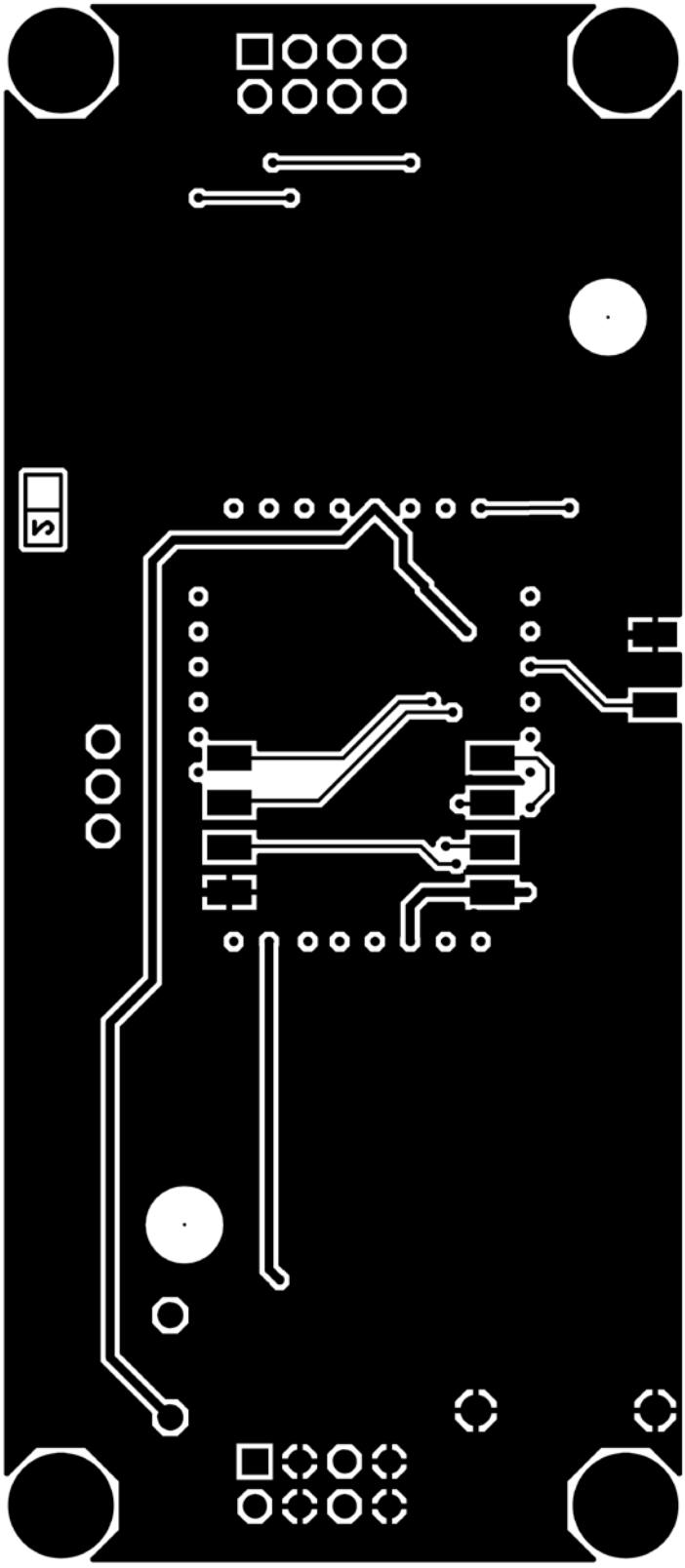

Fig 3. Cake8035 – Layout Bottom view

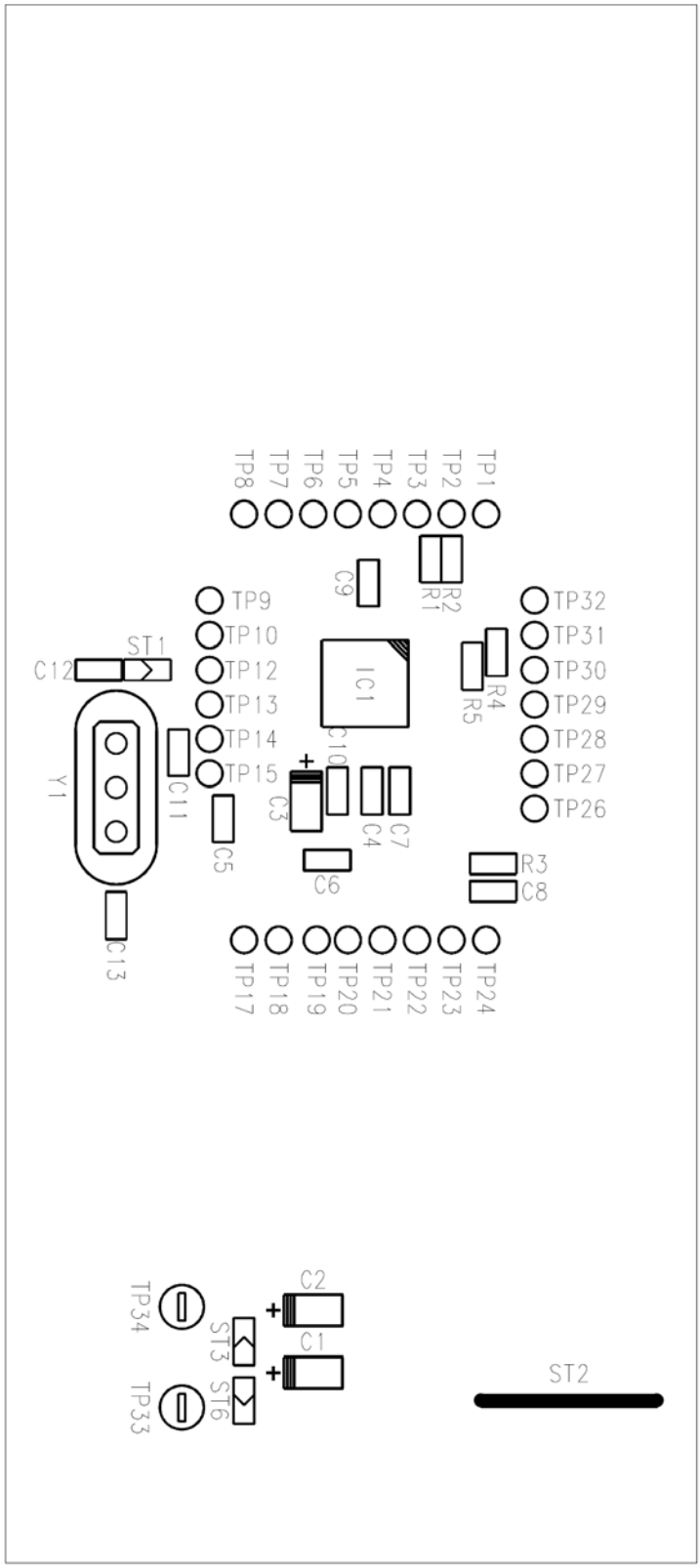

Fig 4. Cake8035 – Components Top view

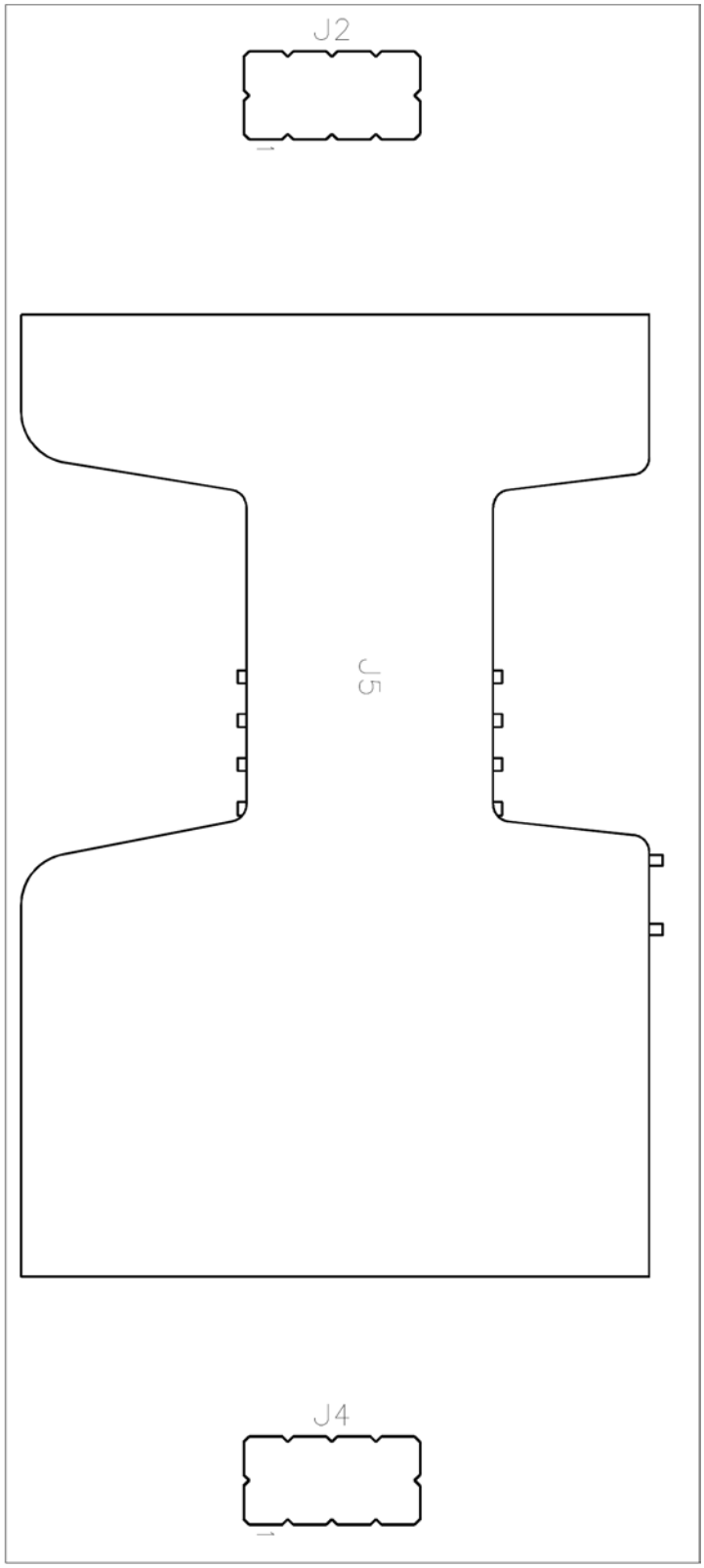

Fig 5. Cake8035 – Components Bottom view

COMPANY PART NO.	COUNT	REFERENCE	GEOMETRY	DESCRIPTION	Fournisseur
25ECNDA3GN105	1	C4	c0603	1uF, Capacite X5R 0603 16V, 10%	
25ECNDA3GN334	2	C5 C6	c0603	330nF, Capacite X5R 0603 16V, 10%	
25ECNDB3GQ224	2	C7 C8	c0603	220nF, Capacite X7R 0603 25V, 10%	
25ECNDB3GS104	3	C9 C10 C11	c0603	100nF, Capacite X7R 0603 50V, 10%	
25ECNDD3FS330	2	C12 C13	c0603	33pF, Capacite COG 0603 50V, 5%	
25ECNDJAGL106	3	C1 C2 C3	cap_320x160x160_a	10uF, Capacite Tantalium Package TAJA AVX:TAJA106K010R, 10%, 10V-85 degres / 7V-125 degres	
25ECNTA1K0017	2	J2 J4	con_bar_254_2x4_md	Bar2x4, Barrette male droite double rangee, 2x4 points, Pas:2.54mm, H=7mm	
25ECNTM000001KN	2	TP33 TP34	tp_boucle_d100	5001, TestPoint:KEYSTONE:5001 Noir	
25ECNTZ700001IT	1	J5	con_itt_ccm01_2251	CCM01-2251, ITT_CANNON: CM01-2251LFT, Lecteur de carte 8 voies plus detectior	NXP
25EINTK000003KK	1	ST2	cav_1016	CAV_10.16, Cavalier dore 10.16mm KONTEK:3130676000500	
25ERESA3D000B	3	R1 R3 R5	r0603	0, Resistance Package CMS 0603 1% 0.1W	
25ERESA3D1003	1	R4	r0603	100k, Resistance Package CMS 0603 1% 0.1W	
pnsx_chev_citr_s	2	ST3 ST6	chev_citr_o_bom	A_SOUDER, Chevron Citroen 0603 !!! A SOUDER !!!	
pnsx_hc49s_NC_plot	1	Y1	xtal_hc49s_plot	N.C., Quartz package HC49/S ***NON CABLE*** sur plot femelle	
pnsx_r0603_nc	1	R2	r0603	N.C., Resistance Package CMS 0603 1% 0.1W ***NON CABLE***	
pnsx_tda8035hn	1	IC1	hvqfn32_050_500x500_sot617_3	TDA8035HN, NXP: TDA8035HN IC Card Interface package:hvqfn32	NXP
zbulle01	1			Circuit_imprime:BSX0207-1	
ztulipe03	1			BULLE06:barrette_femelle_tulipe_3points_type_E-TEC:SIB132S04701	

Fig 6. Cake8035 – Bill of material

3. Daughter board

The Cake8035 can be plugged on a mother board to be tested in a prototype.

The contact between the mother and the daughter board is made by the connectors named J2 and J4. The connectors used are a male straight HE10 2x4 pins for J2 and 2x5 pins for J4. The pitch is 2.54 mm.

3.1 Connection

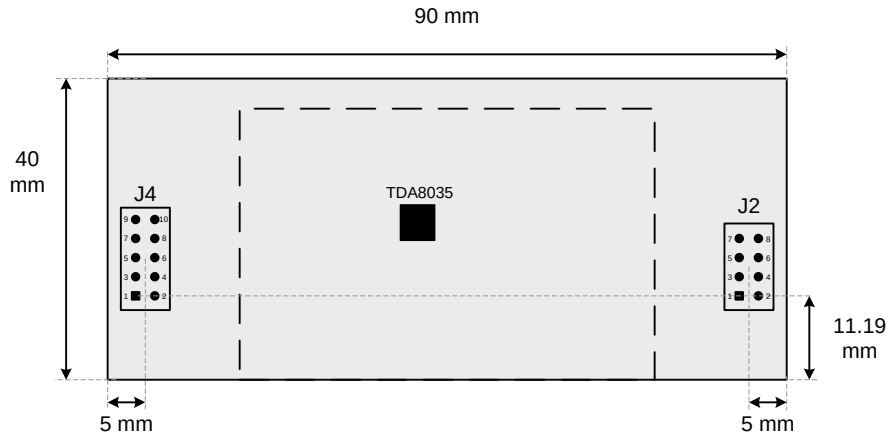

Fig 7. TDA8035 daughter board: size and position of the connectors

All the contact interfaces needed to drive the TDA8035 are available on the J2 and J4 connectors. These signals are defined below.

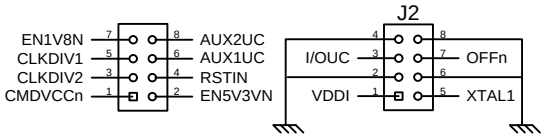

Fig 8. J2 and J4 contacts for TDA8035 – Cake8035

3.2 Power supply

Using this application, there are two power supply inputs for the TDA8035:

a. VDDI available directly from the mother board connector: J2-1, or from a test point: TP33

b. VDDP available from a test point: TP34

VDDI can be supplied using the test point or the J2 connector. The solder jumper ST6 can be used to select the input: if input from TP33: ST6 must be open. If J2 is used; ST6 must be closed.

VDDP can be supplied from TP34 or directly connected to VDDI. The choice is made with the solder jumper: ST3.

If TP34 is used: ST3 must be open. If VDDP comes from VDDI, ST3 must be closed.

The default use of the evaluation board is:

c. VDDI supplied from the mother board through J2 → **ST6 closed**

d. VDDP connected to VDDI → **ST3 closed**

To use the board in this configuration, the power supply must be in the allowed range for VDDI and VDDP: 2.7 < VDDI = VDDP < 3.6.

Typically a 3.3 V power supply is the right choice.

3.3 Clock

With the TDA8035 demo board, the default use is with the clock supplied by the mother board through the XTAL1 pin of J2 (pin 2).

In this case, the crystal doesn't need to be present on the board, and the solder jumper ST1 is open to avoid conflict in the case a crystal is connected.

If the host cannot supply the clock, a crystal must be plugged in the Y1 connector. Two 33 pF capacitors (C8, C9) are already present on the board for this option. If a crystal is connected, the jumper ST1 must be soldered to connect the crystal to the XTAL1 pin of the TDA8035.

3.4 Application

To develop an application with these boards, refer to the TDA8035 Application note AN10997.

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