UG0722
User Guide
PolarFire FPGA Packaging and Pin Descriptions

Microsemi
a Microchip company

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 12.0

The following is a summary of the changes made in revision 12.0 of this document.

- Updated Table 1 on page 3.
- Added "IOD Interfaces" section on page 9.

1.2 Revision 11.0

The following is a summary of the changes made in revision 11.0 of this document.

- Updated Table 1 on page 3.
- Added Figure 9, page 18 and Figure 10, page 18.
- Updated Figure 13, page 20, Figure 14, page 21, Figure 21, page 24, Figure 22, page 24, Figure 29, page 27, and Figure 30, page 28.
- Updated Table 18 on page 32.
- Updated Table 19 on page 32.

1.3 Revision 10.0

The following is a summary of the changes made in revision 10.0 of this document.

- PPAT files website link was updated in "Packaging Pin Assignment" section on page 9.
- Updated Table 4 on page 10 in HSIO column for the Cold sparing I/O feature.
- Updated "Dedicated I/O Bank Pins" section on page 15 and "JTAG Pins" section on page 15.
- Updated "Dedicated I/O Bank Pins" section on page 15.
- A note regarding the ball pinout and spacing are the same on both packages (that is, MPF100 and MPF200), which allows the user to use one PCB footprint was updated. "Mechanical Drawings" section on page 18.
- Updated Figure 1, page 4 through Figure 8, page 8.
- Updated Table 2 on page 8.

1.4 Revision 9.0

MPF300-FCG784N mechanical drawings were added in this revision. See Figure 15, page 21, Figure 16, page 22, and Figure 17, page 22.

1.5 Revision 8.0

The following is a summary of the changes made in revision 8.0 of this document.

- Information about Supply Pins, page 11 was updated.
- A note regarding I/O bank locations was updated. See note below Figure 6, page 7, Figure 7, page 7, Figure 5, page 6 and Figure 8, page 8.
- Information about preferred clock inputs was updated. See Clocking Pins, page 14.
- Information about Package Material Information was updated.

1.6 Revision 7.0

The following is a summary of the changes made in revision 7.0 of this document.

- Information about special pins was added. See Table 13, page 16.
- Information about vent hole diameter was updated. See Table 20, page 33.
- FF_EXIT_N pin was changed to RESERVED as Flash*Freeze is de-featured in the Libero SoC PolarFire software. See Table 13, page 16.

1.7 Revision 6.0

The following is a summary of the changes made in revision 6.0 of this document.

- Information about VDD18 was updated. See Table 5, page 11.
- Information about Pin compatible packages was added. See Table 16, page 17.
- FCG484 mechanical drawings were added. See Figure 21, page 24, Figure 22, page 24, Figure 23, page 25, Figure 24, page 25, Figure 26, page 26, and Figure 27, page 26.
- Information about package material was added. See Package Material Information, page 32.
- Information about Packaging Pin Assignment, page 9 was added.

1.8 Revision 5.0

Information about I/O bank locations was updated. See Figure 1, page 4, Figure 2, page 5, Figure 3, page 5, Figure 4, page 6, Figure 6, page 7, Figure 7, page 7, Figure 5, page 6, and Figure 8, page 8.

1.9 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Information about shield output pin was updated. See Table 13, page 16.
- Information about VDDIx (JTAG bank) and VDD_XCVR_CLK operating voltage was updated. See Table 5, page 11.
- Information about auxiliary supply for I/O circuits was updated. See Table 5, page 11.
- Information about Thermal resistance was updated. See Thermal Specifications, page 34.
- Information about PCB design rules was added. See Recommended PCB Design Rules for BGA Packages, page 39.
- Information about heat sink guidelines was added. See Thermal Management, page 36.
- FCSG325 and FCSG536 mechanical drawings were added. See Figure 31, page 29, Figure 32, page 29, Figure 33, page 30, Figure 34, page 30, Figure 35, page 31, and Figure 36, page 31.

1.10 Revision 3.0

The following is a summary of the changes made in revision 3.0 of this document.

- Information about Package marking was added. See Package Marking, page 35
- Information about thermal resistances of PolarFire Package device was added. See Thermal Specifications, page 34.
- Information about packing and shipping was added. See Packing and Shipping, page 36.
- Table 3, page 9 and Table 17, page 32 were added.

1.11 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Figure 6, page 7 and Figure 7, page 7 were updated.
- Information about unused condition of pins was updated. See Table 5, page 11, Table 11, page 15, Table 12, page 15, Table 13, page 16, and Table 14, page 16.

1.12 Revision 1.0

The first publication of this document.

2 PolarFire FPGA Packaging and Pin Descriptions

This guide provides pin and packaging information (such as bank assignments and mechanical information) for PolarFire® FPGAs.

PolarFire FPGAs feature a flexible I/O structure that supports a range of mixed voltages (1.1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank selection. The HSIO and GPIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, see *UG0686: PolarFire FPGA User I/O User Guide*.

2.1 Packaging Overview

PolarFire FPGAs are available in multiple packages. Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. HSIO and GPIO banks have a maximum supply voltage of 1.8 V and 3.3 V, respectively.

The following table lists the PolarFire FPGA variants, with user I/O and XCVR lanes, in Pb-free packages.

Table 1 • **PolarFire FPGA Product Family[1]**

Features		MPF100T	MPF200T	MPF300T	MPF500T
FPGA Fabric	Logic Elements (4 LUT + DFF)	109	192	300	481
	Math Blocks (18 × 18 MACC)	336	588	924	1480
	LSRAM Blocks (20 kbit)	352	616	952	1520
	µSRAM Blocks (64 × 12)	1008	1764	2772	4440
	Total RAM (Mbits)	7.6	13.3	20.6	33
	µPROM (Kbits 9-bit bus)	297	297	459	513
	User DLLs/PLLs	8	8	8	8
High-Speed I/O	250 Mbps to 10.3125 Gbps Transceiver Lanes	8	16	16	24
	PCIe Gen2 End Points/Root Ports	2	2	2	2
Total I/Os	Total User I/Os	284	368	512	584

Table 1 • **PolarFire FPGA Product Family[1] *(continued)***

Features		MPF100T	MPF200T	MPF300T	MPF500T
Packaging	Type/Size/Pitch	Total User I/O (HSIO/GPIO)/Transceivers			
	FCSG325 (11 mm × 11 mm, 11 mm × 14.5 mm, 0.5 mm)	170(84/86)/4	170(84/86)/4		
	FCSG536 (16 mm × 16 mm, 0.5 mm)		300(120/180)/4	300(120/180)/4	
	FCVG484 (19 mm × 19 mm, 0.8 mm)	284(120/164)/4	284(120/164)/4	284(120/164)/4	
	FCG484 (23 mm × 23 mm, 1.0 mm)	244(96/148)/8	244(96/148)/8	244(96/148)/8	
	FCG784 (29 mm × 29 mm, 1.0 mm)		364(132/232)/16	388(156/232)/16	388(156/232)/16
	FCG1152 (35 mm × 35 mm, 1.0 mm)			512(276/236)/16	584(324/260)/24

1. Devices in the same package are pin compatible.

For more information about multiple speed grades, temperatures, and package combinations, refer to **Ordering Information** section in *PolarFire FPGA Product Overview*.

2.2 Bank Locations

PolarFire FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the MPF100T, MPF200T, MPF300T, and MPF500T devices with available package combinations.

Figure 1 • **PolarFire MPF500T-FCG1152 I/O Bank Locations**

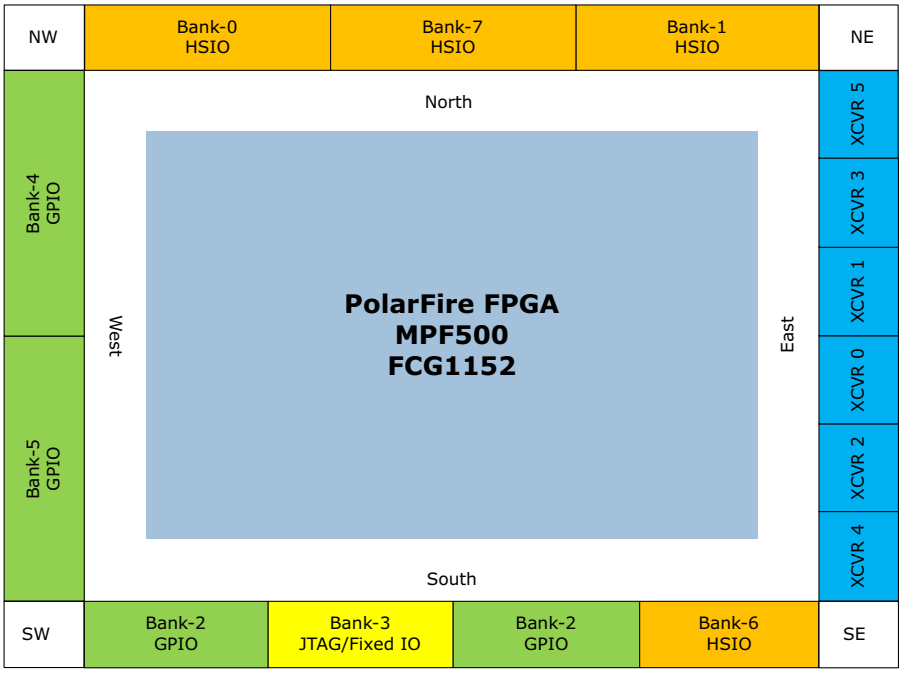


Figure 2 • **PolarFire MPF300T-FCG1152 I/O Bank Locations**

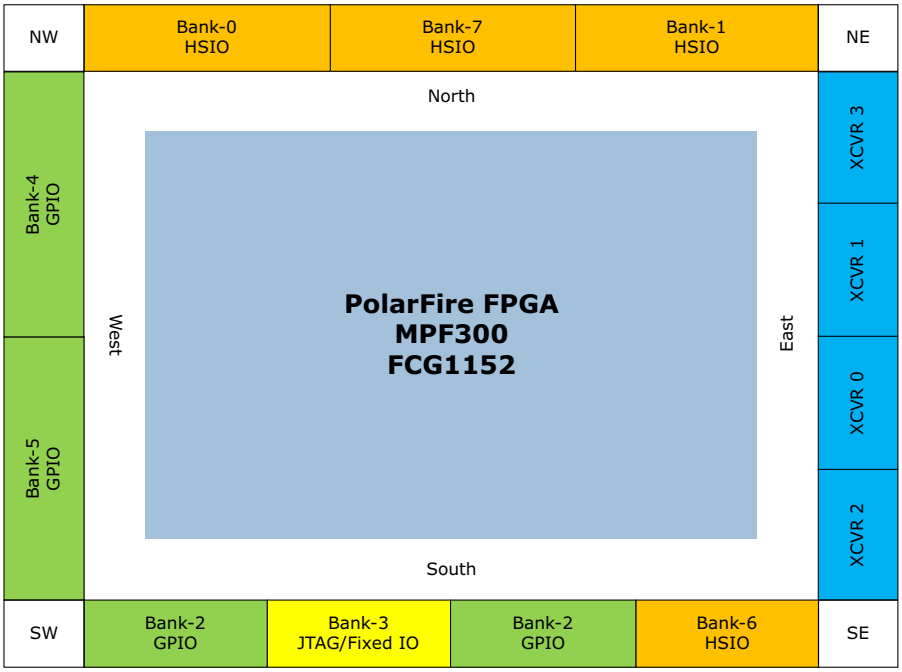


Figure 3 • **PolarFire MPF500T/MPF300T-FCG784 I/O Bank Locations**

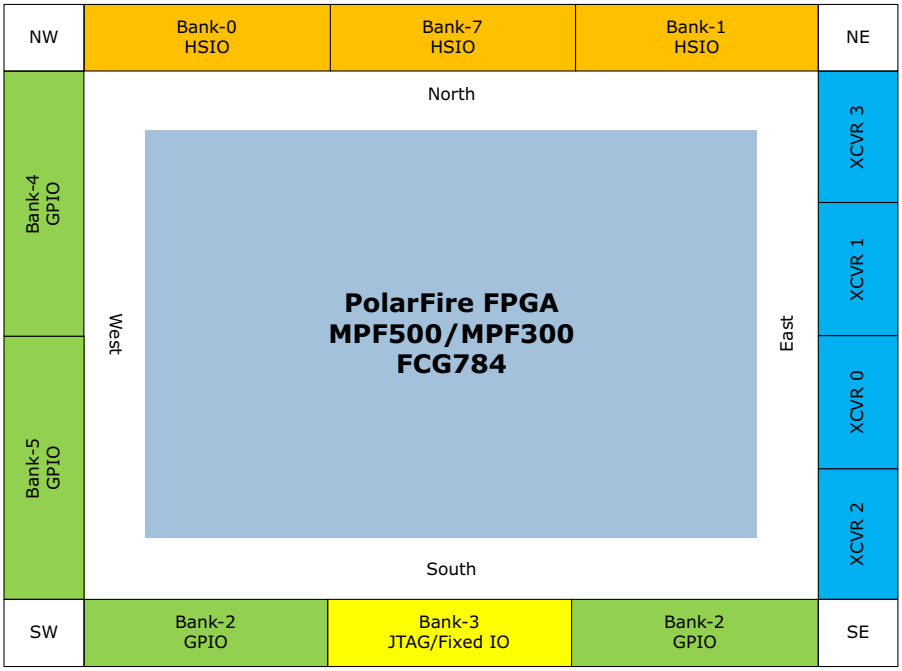


Figure 4 • **PolarFire MPF200T-FCG784 I/O Bank Locations**

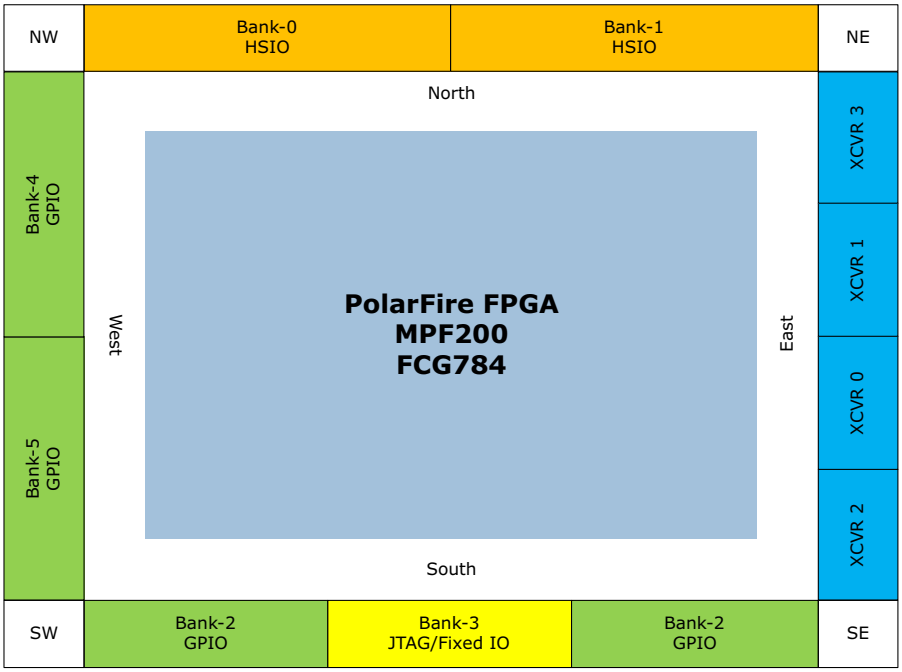
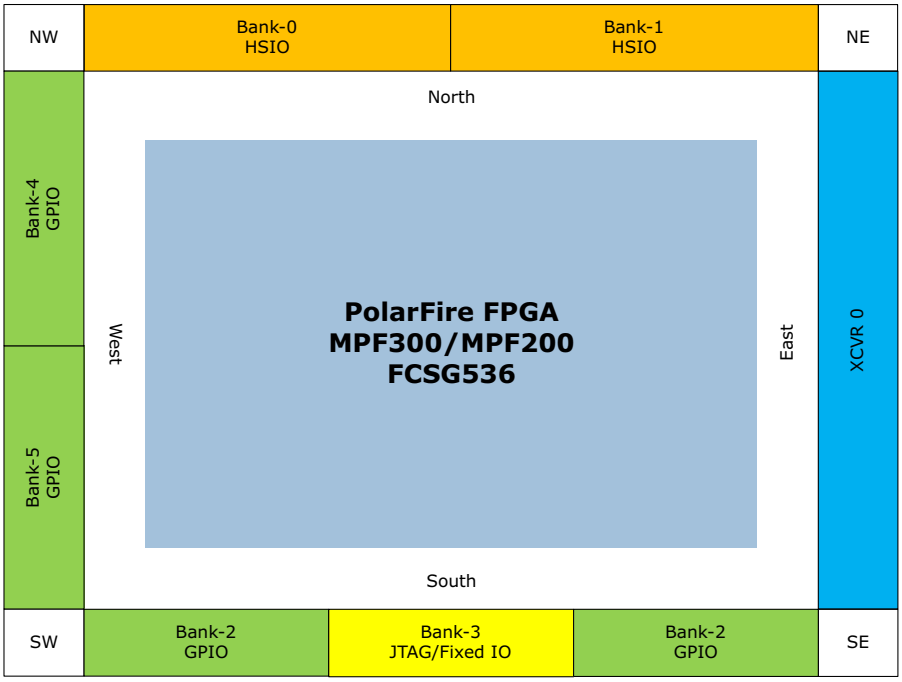
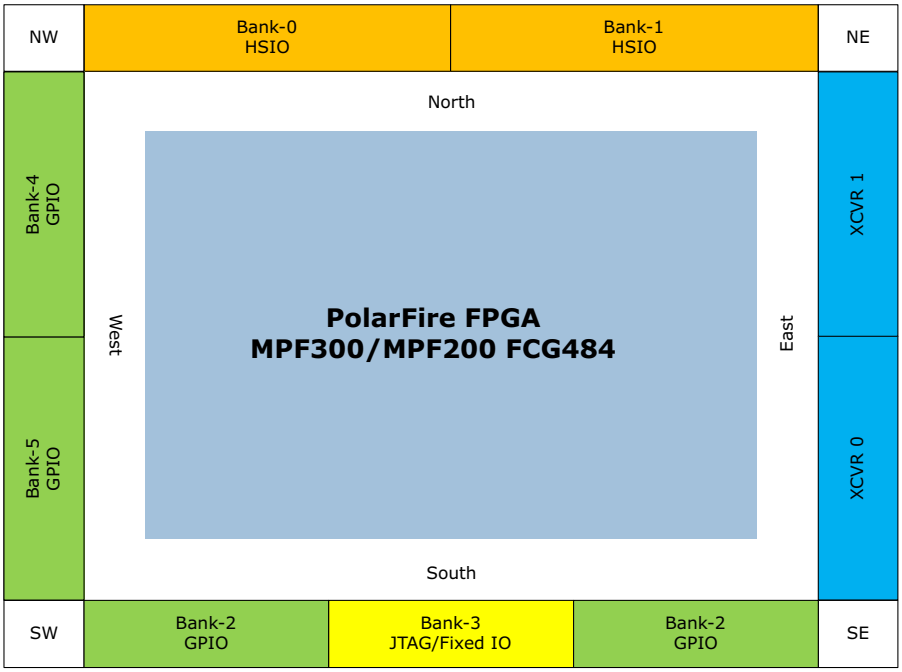


Figure 5 • **PolarFire MPF300T/MPF200T-FCSG536 I/O Bank Locations**



Note: Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively - within the package substrate for pin migration compatibility.

Figure 6 • **PolarFire MPF300T/MPF200T-FCG484 I/O Bank Locations**



Note: In MPF300T and MPF200T devices, Bank 5 VDDI and VDDAUX power pins are connected to Bank 4 VDDI and VDDAUX power pins, respectively - within the package substrate for pin migration compatibility.

Figure 7 • **PolarFire MPF100T-FCVG484 I/O Bank Locations**

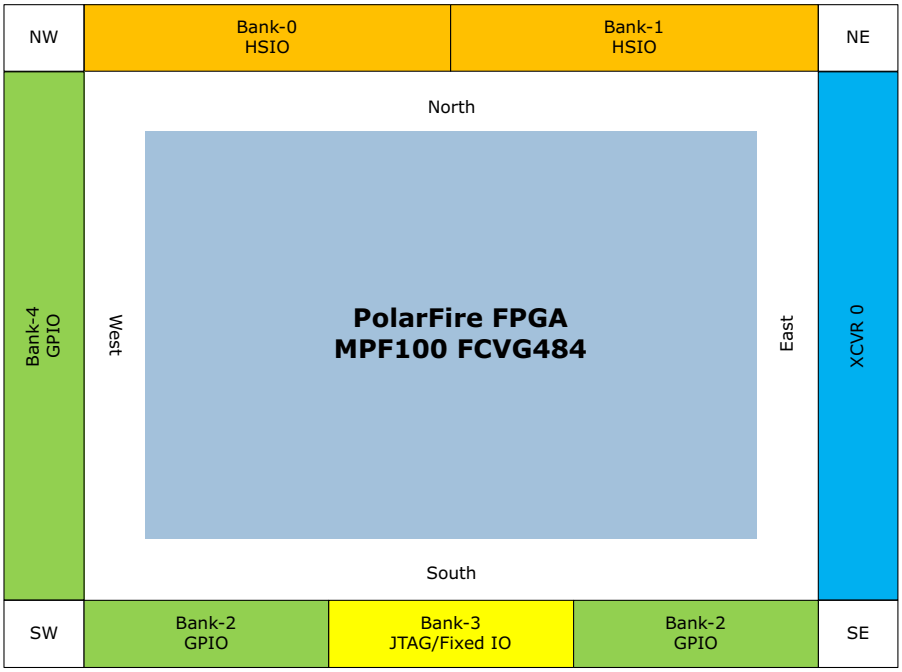
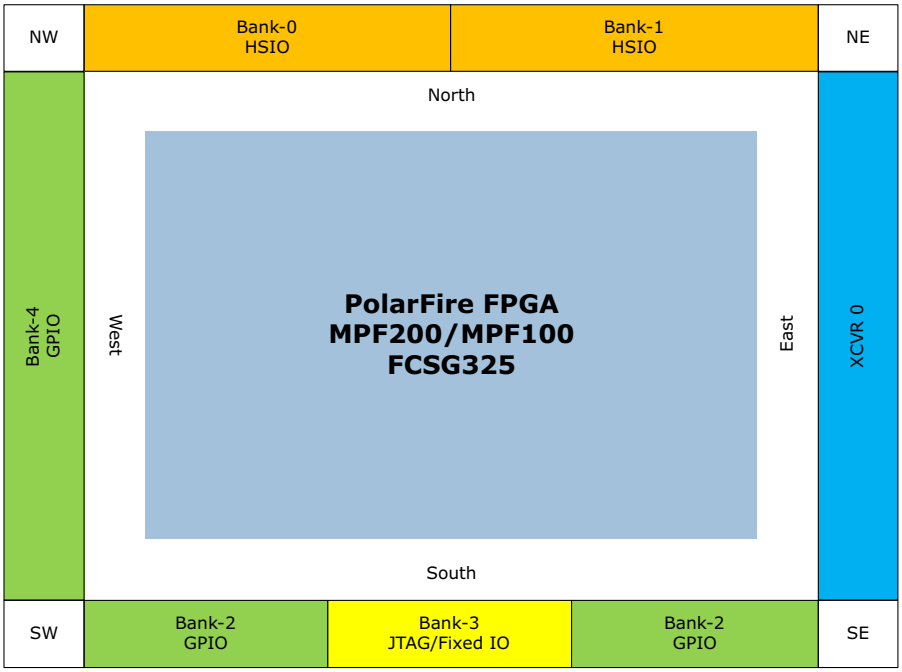


Figure 8 • **PolarFire MPF200T/MPF100T-FCSG325 I/O Bank Locations**



The following table lists the organization of the I/O banks in PolarFire FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe is supported only in XCVR0.

Table 2 • **Organization of I/O Banks**

	FCG1152		FCG784		FCSG536	FCG484		FCSG325
Bank Number	**MPF500T**	**MPF300T**	**MPF500T MPF300T**	**MPF200T**	**MPF300T MPF200T**	**MPF300T MPF200T**	**MPF100T**	**MPF200T MPF100T**
Bank 0	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 1	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO	HSIO
Bank 2	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 3	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O	JTAG/ FIXED I/O
Bank 4	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
Bank 5	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO		
Bank 6	HSIO	HSIO						
Bank 7	HSIO	HSIO	HSIO					
XCVR 0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
XCVR 1	Yes	Yes	Yes	Yes		Yes		
XCVR 2	Yes	Yes	Yes	Yes				
XCVR 3	Yes	Yes	Yes	Yes				
XCVR 4	Yes							
XCVR 5	Yes							

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane.

For more information about DDR lanes for each package in Package Pin Assignment Tables (PPATs), see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*.

The following table lists the XCVR channels for PolarFire device/package.

Table 3 • **Serial Transceiver Channels**

Device	FCG1152	FCG784	FCG484	FCVG484	FCSG536	FCSG325
MPF500T	24	16				
MPF300T	16	16	8	4	4	
MPF200T		16	8	4	4	4
MPF100T			8	4		4

2.3 Packaging Pin Assignment

The Packaging Pin Assignment Table, that is, PPAT information is available in the Packing section, for more information, refer to: *PolarFire FPGAs Documentation web page*. PPAT contains information about recommended DDR pin-outs, PCI Express capability for XCVR-0, DDR Lane information for IO CDR, and generic IOD interface pin placement.

2.4 IOD Interfaces

PolarFire pinouts can migrate between device densities in same packages with regard to compatible PCB footprints. This is generally true for power and ground and general purpose pin usage as well as XCVR lanes.

However, upward and downward pin migration of different PolarFire logic densities in the same package can vary when using high-speed IOD interfaces such as memory interfaces or generic DDR interfaces.

Microchip recommends initially targeting the intended lowest density device to achieve the full I/O migration with IOD interfaces before committing a final footprint to a PCB design.

Using Libero SoC to verify the pinout in the same package with the lowest density will allow footprint compatibility for smoother density migration with the IOD interfaces. This approach allows designs to initially use a larger density while providing the path to reduce to lower density.

2.5 Pin Descriptions

PolarFire device has user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

2.5.1 User I/O

PolarFire FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1 V and 1.8 V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards, and operating supplies ranging from 1.2 V to 3.3 V. GPIO supports multiple standards, including 3.3 V with an integrated clock data recovery (CDR) to high-speed serial interfaces such as 1GbE.

Each PolarFire FPGA user I/O uses a IOxyBz naming convention, where:

- **IO** = the type of I/O.
- **x** = the I/O pair number in bank z.
- **y** = P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- **B** = bank (see note in Supported I/O Features, page 10).
- **z** = bank number.

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

2.5.1.1 Supported I/O Features

The following table lists the I/O features supported on HSIO and GPIO.

Table 4 • **Supported I/O Features**

I/O Feature	HSIO	GPIO	Additional Information
Programmable on/off clamp		Yes	
Hot-plug		Yes	
Cold sparing	Yes[1]	Yes	
True differential output driver		Yes	
Programmable on/off 100 Ω differential termination		Yes	
PVT-compensated output drive	Yes	Yes	
Programmable slew control		Yes	
PVT compensated slew control	Yes		
Programmable input hysteresis	Yes	Yes	
Mobile industry processor interface (MIPI) (input)		Yes	High-speed and low-power.
MIPI (output)		Yes	High-speed.

1. HSIO is **pseudo-cold spare** that is, it requires the spare device to have its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes.

2.5.2 Supply Pins

The following table lists multiple power supply pins required for proper device operation. For information about unused conditions and power sequence, see *UG0726: PolarFire FPGA Board Design User Guide*.

Table 5 • **Supply Pins**

Name	Description	Operating Voltage
XCVR_VREF[1]	Voltage reference for transceiver.	0.9 V/1.25 V
VDD_XCVR_CLK	Provides common power to all transceiver reference clock buffers.	2.5 V/3.3 V
VDDA25	Transceiver PLL power	2.5 V
VDDA	Power for transceiver Tx and Rx lanes 0, 1, 2, 3.	1.0 V/1.05 V
VSS	Core digital ground.	
VDD	Device core digital supply.	1.0 V/1.05 V
VDDIx (JTAG Bank)	Supply for I/O circuits in a bank.	1.8 V/2.5 V/3.3 V
VDDIx (GPIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V/2.5 V/ 3.3 V
VDDIx (HSIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V
VDD25	Power for corner PLLs and PNVM.	2.5 V
VDD18	Power for programming and HSIO receiver. HSIO auxiliary power supply.	1.8 V
VDDAUXx	Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5 V or 3.3 V and must be always equal to or higher than VDDIx of GPIO banks.	Greater than or equal to VDDI

1. SSTL25 (stub series terminated logic) I/O standard for 1.25 V VREF, SSTL18 I/O standard for 0.9 V, and HSUL18 I/O standard for 0.9 V.

2.5.2.1 Packaging Decoupling Capacitors

PolarFire 0.8 mm and 1.0 mm pitch packages contain decoupling capacitors to support high-speed I/O operation.

Small, low-profile CSP packages (0.5 mm ball pitch, 16 mm × 16 mm and smaller) do not have package decoupling capacitors.

The following table lists the packaging decoupling capacitors contained in non-CSP packages.

Table 6 • **Packaging Decoupling Capacitors**

Power Supply	0.8 mm Pitch		1 mm Pitch	
	Number of Capacitors	Value	Caps available	Value
VDDI0			1	1 µF
VDDI1			1	1 µF
VDDI2			1	1 µF
VDDI4			1	1 µF
VDDI5			1	1 µF
VDDI6[1]			1	1 µF
VDDI7[1]			1	1 µF
VDD			1	2.2 µF
VDD18			2	1 µF
VDDA	2	4.7 nF 1.0 nF	4	4.7 nF 2.2 nF 1.5 nF 1.0 nF

1. 0.8 mm pitch PolarFire packages do not support VDDI6 and VDDI7.

Table 7 • **Package De-capacitor Part Number and ESR Values**

Capacitance value	Part numbers	Package	ESR (Ω)
4.7 nF	GRM033R70J472KA01	0201	0.09724812
2.2 nF	GRM033R70J222KA01	0201	0.16111
1.5 nF	GRM033R70J152KA01	0201	0.194915396
1 nF	CGA1A2X7R1C102K030BA	0201	0.2444
1 uF	LL185C70J105ME14K (GPIO)	0306	0.005475757
1 uF	LL185C70G105ME01L (HSIO and HSIO_AUX)	0306	0.005009904
2.2 uF	W2L14C225MAT1A	0508	0.003964

2.5.3 Memory Interface

Valid locations for DDR memory interfaces are shown in Package Pin Assignment Tables (PPATs), see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview*. By using the Libero® SoC PolarFire configurator, all individual DDR interface pins are identified from the macro. For more information on the memory interface, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide*.

The following table lists the reference receiver modes of I/O standards.

Table 8 • **Reference Receiver Modes**

I/O Standard	V_{DDIx}	V_{REF}	On-die Termination (ODT) (in Ω)	Bank Type	Speed (Mbps)	Application
SSTL18	1.8 V	0.9 V	40/50/60/80/120/240	GPIO, HSIO	800 1066	RLDRAM2
SSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	1066 1333	DDR3
SSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	1333	DDR3L
HSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	900 1100	QDRII+
HSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	1066	RLDRAM3
HSUL12	1.2 V	0.6 V	60/120/40	HSIO	1066 1333	LPDDR3
HSTL12	1.2 V	0.6 V	60/120/240	HSIO	1266	QDRII+
POD12	1.2 V	0.6 V	20/30/40/60/120	HSIO	1600	DDR4

2.5.4 DDR Interface

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR3, DDR3, and DDR4 memories. It supports 16-, 32-, and 64-bit data bus width modes with ECC support. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC PolarFire software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information on DDR signals, see *UG0676: PolarFire FPGA DDR Memory Controller User Guide.*

2.5.5 Clocking Pins

CCC blocks, located at each corner of the PolarFire FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information on clocking pins, see *UG0684: PolarFire FPGA Clocking Resources User Guide*. Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. The following table lists the clocking pin names and descriptions. See Table 5, page 11 for more information on CCC pin voltage.

Table 9 • **Clocking Pins[1]**

Name	Description	When Unused
CCC_NW_PLL0_OUT[0:1]	Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of PolarFire device to route the clocks to and from the PLLs and DLLs.	Do not connect (DNC)
CCC_NW_PLL1_OUT[0:1]		
CCC_NE_PLL0_OUT[0:1]		
CCC_NE_PLL1_OUT[0:1]		
CCC_SE_PLL0_OUT[0:1]		
CCC_SE_PLL1_OUT[0:1]		
CCC_SW_PLL0_OUT[0:1]		
CCC_SW_PLL1_OUT[0:1]		
CCC_SE_CLKIN_S_[8:15]	Preferred clock inputs that connect external clock signals to the CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs, and fabric logic.	DNC
CCC_SW_CLKIN_S_[0:3]		
CCC_SW_CLKIN_W_[0:3]		
CCC_NW_CLKIN_W_[4:7]		
CCC_NW_CLKIN_N_[0:3]		
CCC_NE_CLKIN_N_[8:11]		
CLKIN_S_[4:7]	Preferred clock inputs directly routed to internal global buffers through MUXes.	DNC
CLKIN_N_[4:7]		

1. Some of the preferred clock inputs have connections to feedback clock input of the PLL/DLL present in the CCC. It is required to choose a preferred clock input which has connection to the PLL reference clock input for clock frequency synthesis. See *UG0684: PolarFire FPGA Clocking Resources User Guide* for preferred clock inputs connectivity to PLLs/DLLs and global clock network.
   For example:
   The package pin T9 of MPF300T-FCG1152 device has pin name as follows:
   GPIO219PB4/CLKIN_W_3/CCC_SW_CLKIN_W_3
   The T9 pin can be used as a preferred clock input which can connect to global clock network or CCC_SW. Inside the CCC_SW, the T9 pin is connected to feedback clock inputs of PLLs and reference clock inputs of DLLs.

2.5.6 Dedicated I/O Bank Pins

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the PolarFire controller is not using them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the PolarFire controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up. For information about unused conditions, see *UG0726: PolarFire FPGA Board Design User Guide*.

The JTAG bank voltages can be set to operate at 1.8 V, 2.5 V, or 3.3 V. The following table lists the JTAG pins.

Table 10 • **JTAG Pins**

Pin Names	Direction	Weak Pull-Up/Unused Condition	Description
TMS	Input	Yes/DNC	JTAG test mode select.
TRSTB	Input	Yes[1]	JTAG test reset. Must be held low during device operation.
TDI	Input	Yes/DNC	JTAG test data in. In ATPG or test mode, when using a 4-bit tdi bus, this IO is used as tdi[0].
TCK	Input	No[2]	JTAG test clock
TDO	Output	No/DNC	JTAG test data out.

1. If TRSTB is unused and in the avionics mode, either an external 1 kΩ pull-down resistor should be connected to it, to override the weak internal pull-up or it should be driven low from the external source.
2. In unused condition, must be connected to VSS through 10 kΩ resistor.

Table 11 • **Device Reset Pins**

Name	Direction	Weak Pull-up	Description
DEVRST_N	Input	22 KΩ	Device reset (asserted low).

Table 12 • **SPI Interface Pins**

Name	Direction	Description
SCK	Bi-directional	SPI clock.
SS	Bi-directional	SPI slave select.
SDI	Input	SDI input for the shared SPI interface.
SDO	Output	SDO output for the shared SPI interface.
SPI_EN	Input	Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a master or a slave. Dedicated to the system controller. 0: SPI slave interface 1: SPI master interface

Table 13 • **Special Pins**

Name	Direction	Description	Unused Condition
NC	–	No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device.	–
DNC	–	Do not connect pin. DNC pins must not be connected to any signals on the PCB, and they must be left unconnected.	–
LPRB_A	Output	Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following: – Live probe – User I/O (HSIO)	Libero-defined DNC.
LPRB_B	Output		Libero-defined DNC.
FF_EXIT_N	Input	RESERVED	–
Shield Signal	Output	Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity.	Only when DDR controller is in use.

2.5.7 XCVR Interface

The transceiver I/O available in the PolarFire device is dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design.

Table 14 • **XCVR Interface Pins**

Name	Direction	Description	Unused Condition
XCVR_xy_REFCLK_P	Input	Differential serial reference clock xy - location x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	DNC.
XCVR_xy_REFCLK_N			
XCVR_x_TXy_P	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC.
XCVR_x_TXy_N			
XCVR_x_RXy_P	Input	Differential serial receive pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC, see *UG0677: PolarFire FPGA Transceiver User Guide.*
XCVR_x_RXy_N			

2.6 Package Pin-outs

The following table lists packaging pin-outs of PolarFire device. Detailed PPATs are available for download and they contain revision history, device specification, power supplies, pin-outs, and BGA graphic. For more information about PPATs, see *https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#documentation/packaging*.

Table 15 • **Package Pin Outs**

	Packages					
Device	**FCG1152**	**FCG784**	**FCG484**	**FCVG484**	**FCSG536**	**FCSG325**
MPF500T	Yes	Yes				
MPF300T	Yes	Yes	Yes	Yes	Yes	
MPF200T		Yes	Yes	Yes	Yes	Yes
MPF100T			Yes	Yes		Yes

2.6.1 Pin Compatibility Between Devices

The following table lists the pin compatible packages of PolarFire device.

Table 16 • **Pin Compatible Packages**

Package	Devices
FCG1152	MPF500T/300T
FCG784	MPF500T/300T/200T
FCG484	MPF300T/200T/100T
FCVG484	MPF300T/200T/100T
FCSG536	MPF300T/200T
FCSG325	MPF200T/100T

2.7 Mechanical Drawings

The following illustrations show the top, bottom, and side views and dimensions for the PolarFire FPGAs.

Figure 9 • **MPF500TS-FC1152M Package Top-View and Side-View**

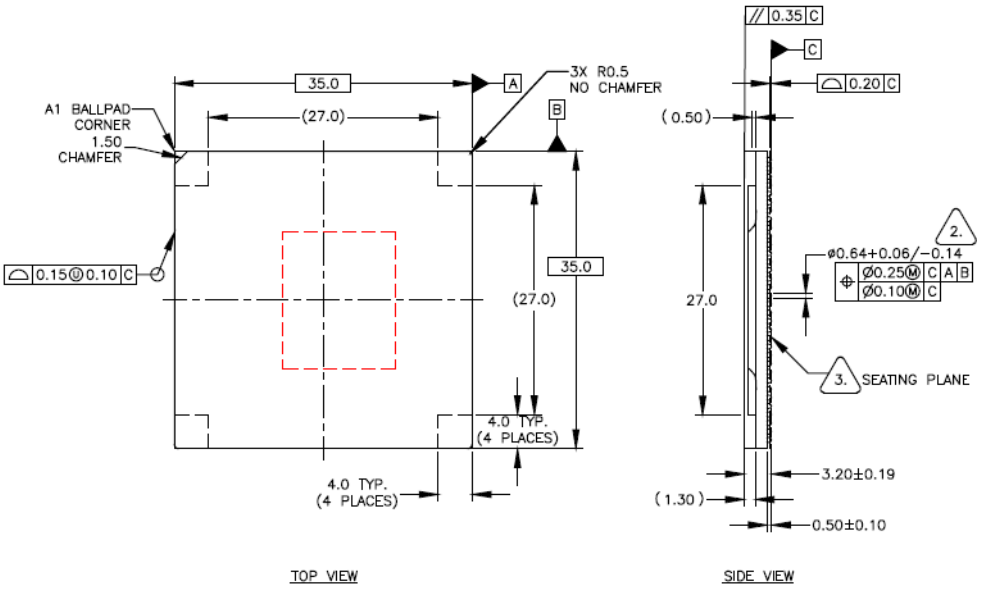


Figure 10 • **MPF500TS-FC1152M Package Bottom-View**

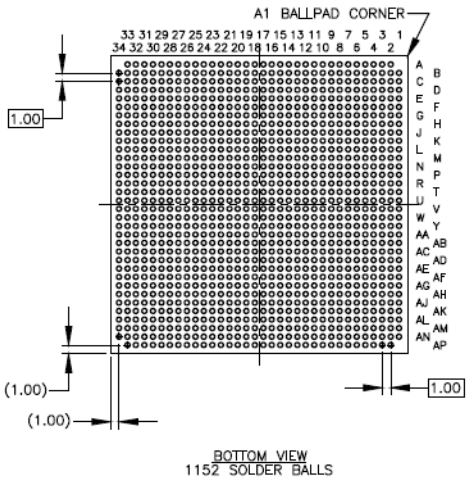
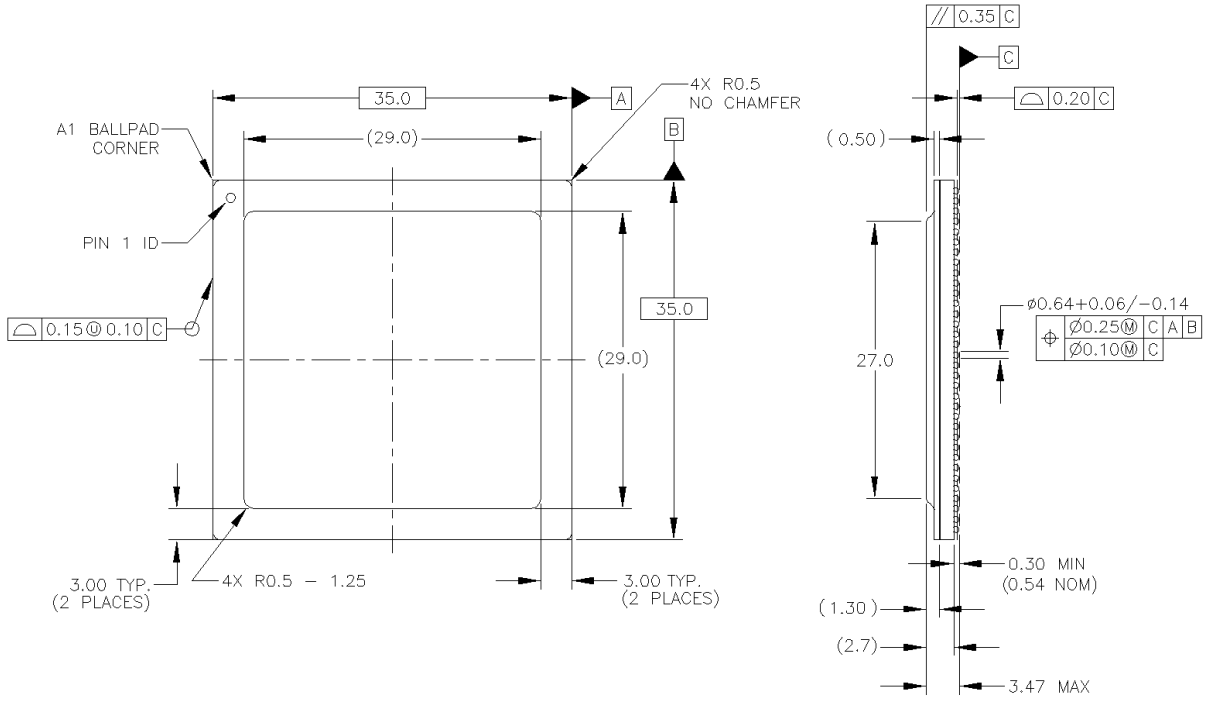


Figure 11 • **MPF500T/MPF300T-FCG1152 Package Top-View and Side-View**



Units: mm

Figure 12 • **MPF500T/MPF300T-FCG1152 Package Bottom-View**

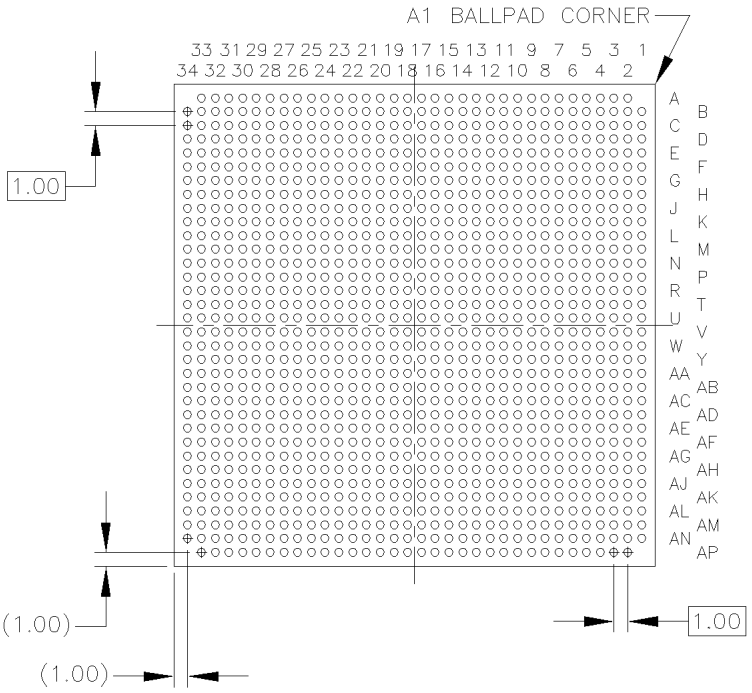
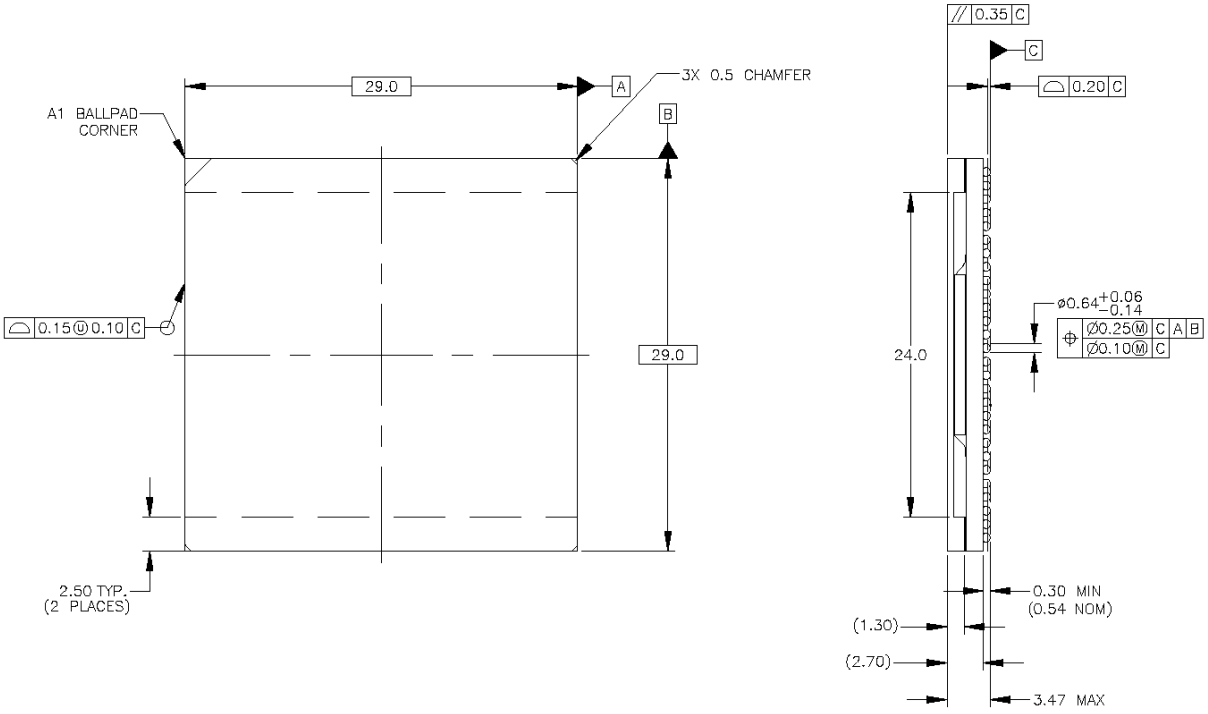


Figure 13 • **MPF500T/TS/MPF300T/TS/MPF200T-FCG784/FC784M Package Top-View and Side-View**



Units: mm

Figure 14 • **MPF500T/TS/MPF300T/TS/MPF200T-FCG784/FC784M Package Bottom-View**

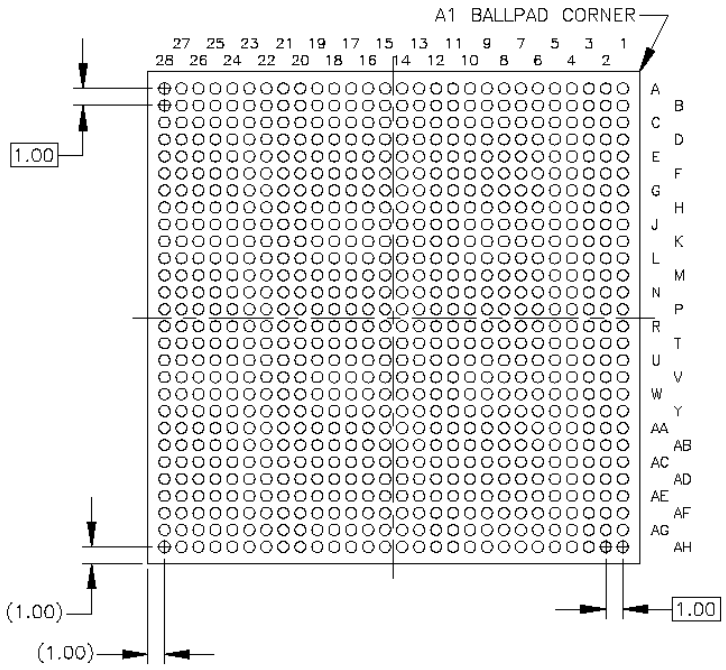


Figure 15 • **MPF300-FCG784N Package Top-View and Side-View**

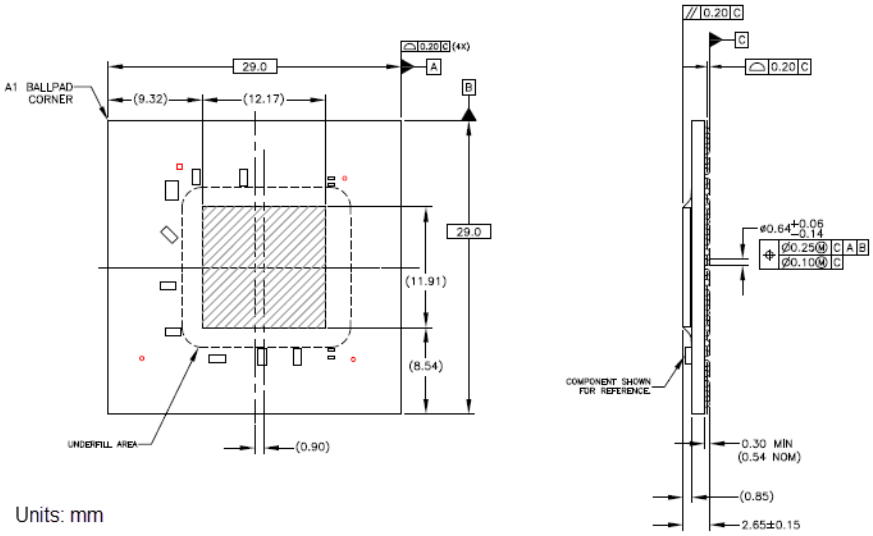


Figure 16 • **MPF300-FCG784N Package Bottom-View**

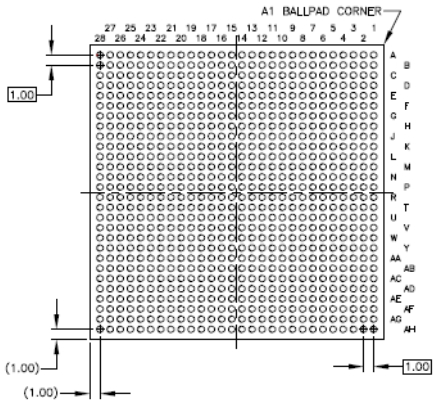


Figure 17 • **MPF300-FCG784N—Decoupling Capacitor Locations**

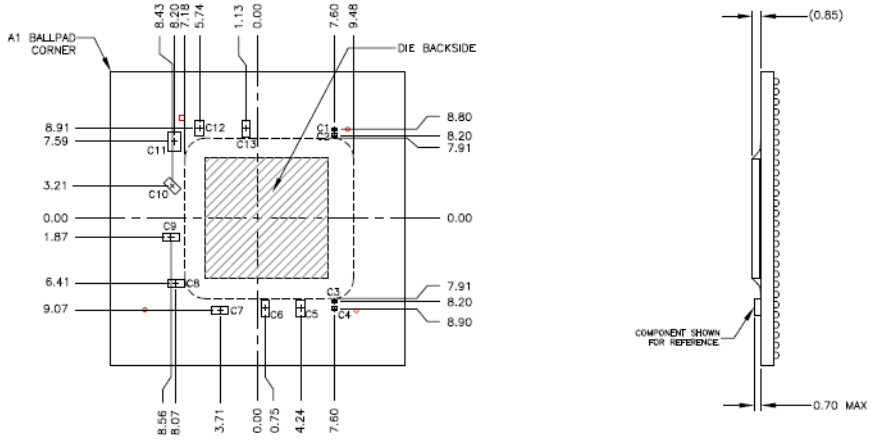


Figure 18 • **MPF300T-FCG484 Package Top-View and Side-View**

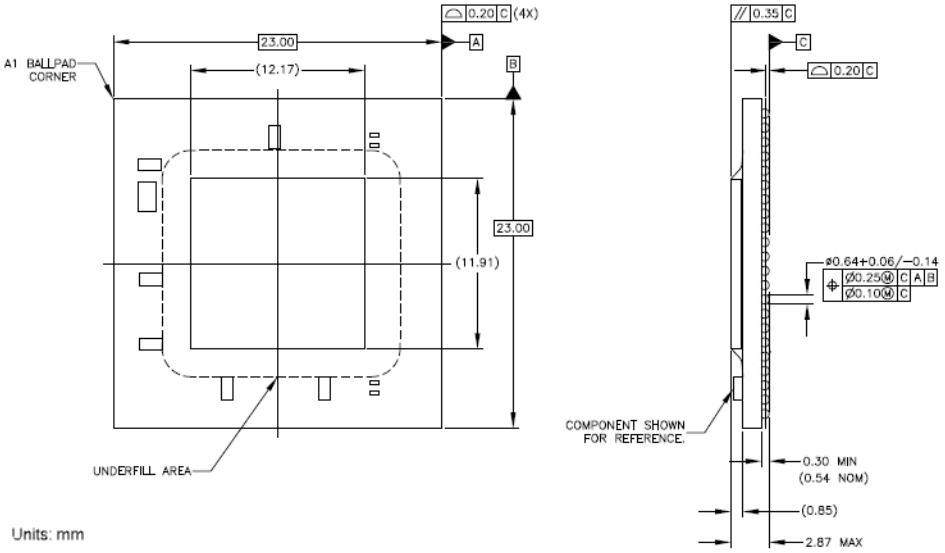


Figure 19 • **MPF300T-FCG484 Package Bottom-View**

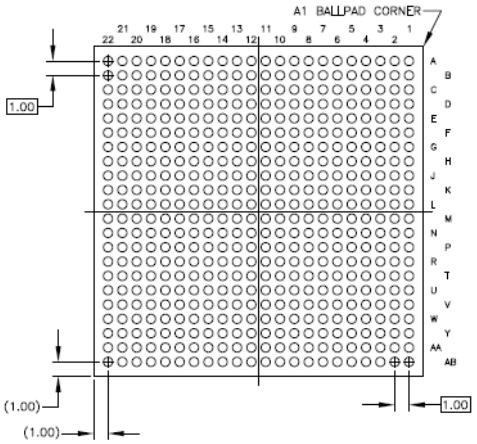


Figure 20 • **MPF300T-FCG484—Decoupling Capacitor Locations**

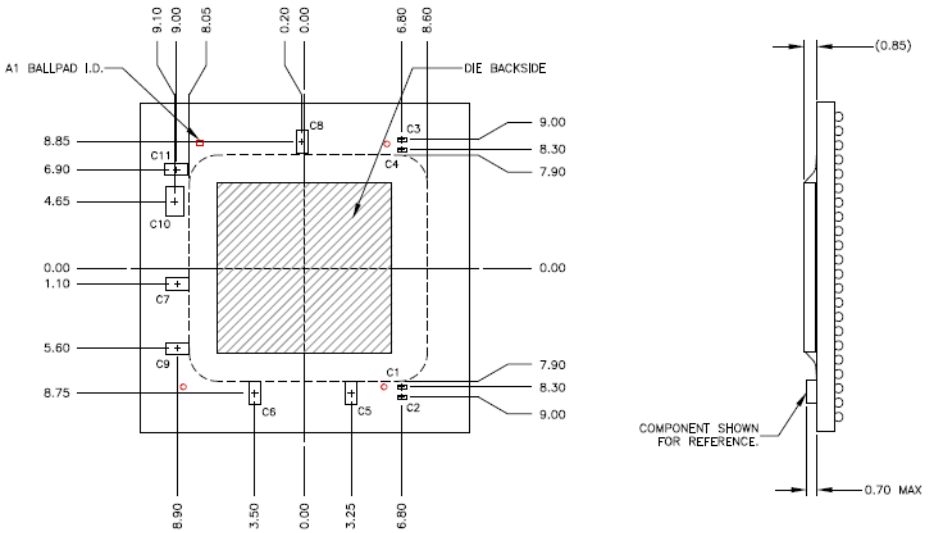


Figure 21 • **MPF300T/TS-FC484M Package Top-View and Side-View**

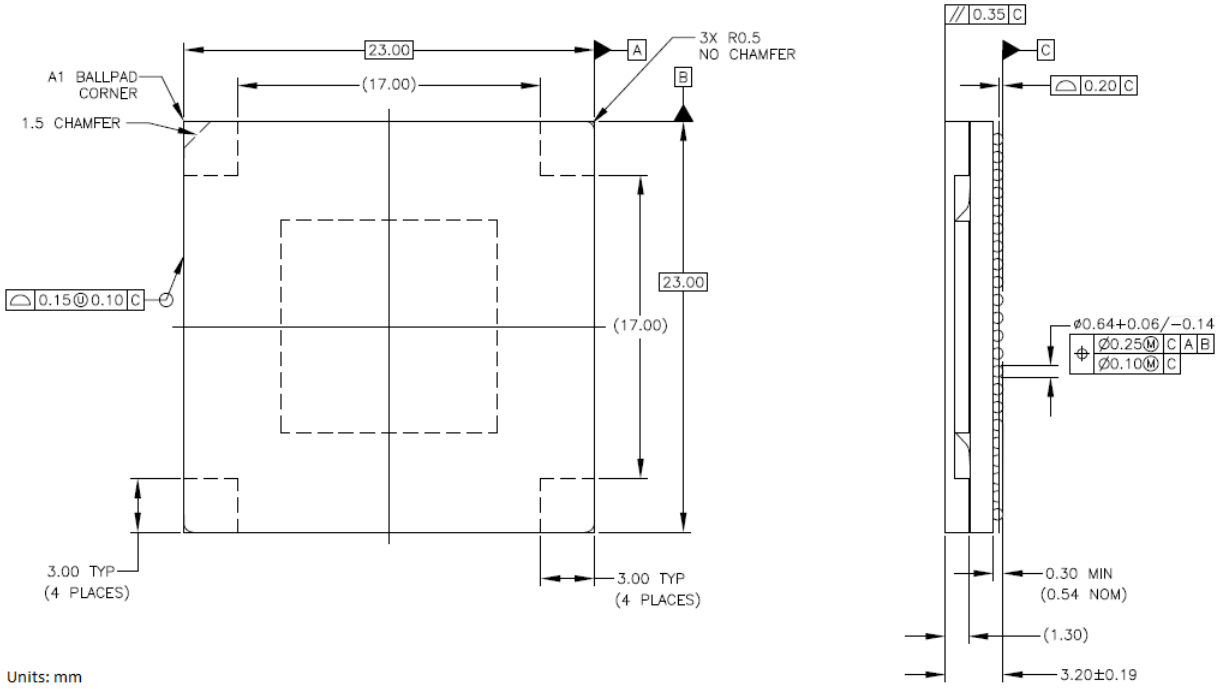


Figure 22 • **MPF300T/TS-FC484M Package Bottom-View**

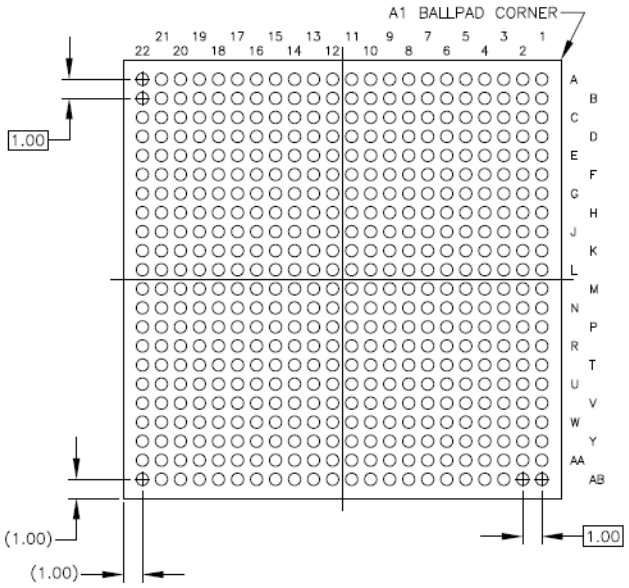


Figure 23 • **MPF200T-FCG484 Package Top-View and Side-View**

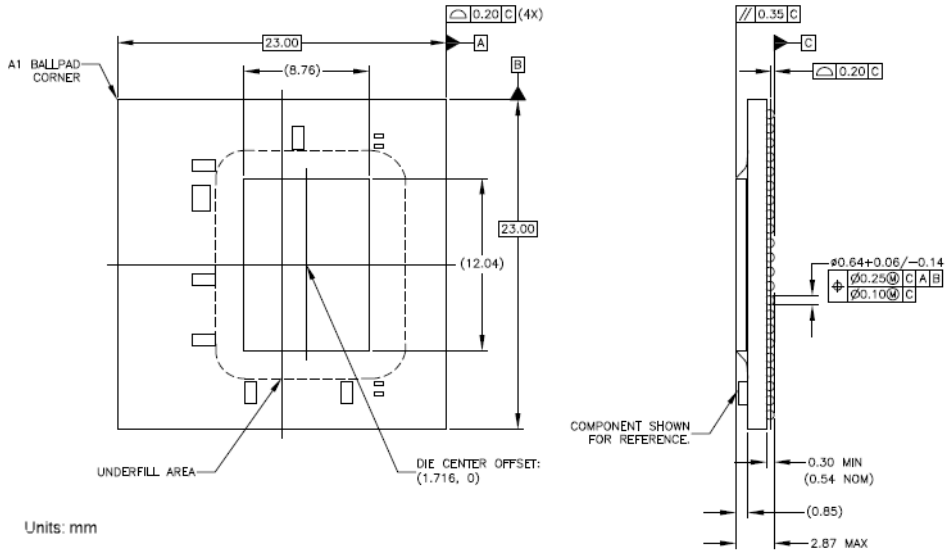


Figure 24 • **MPF200T-FCG484 Package Bottom-View**

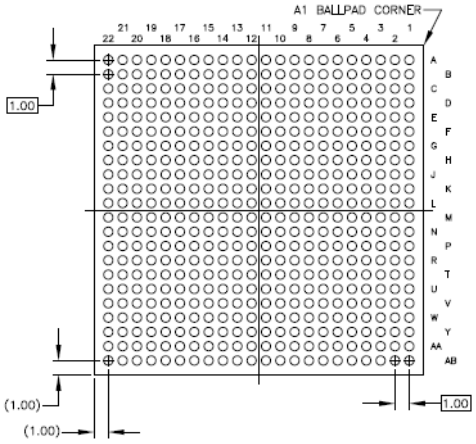
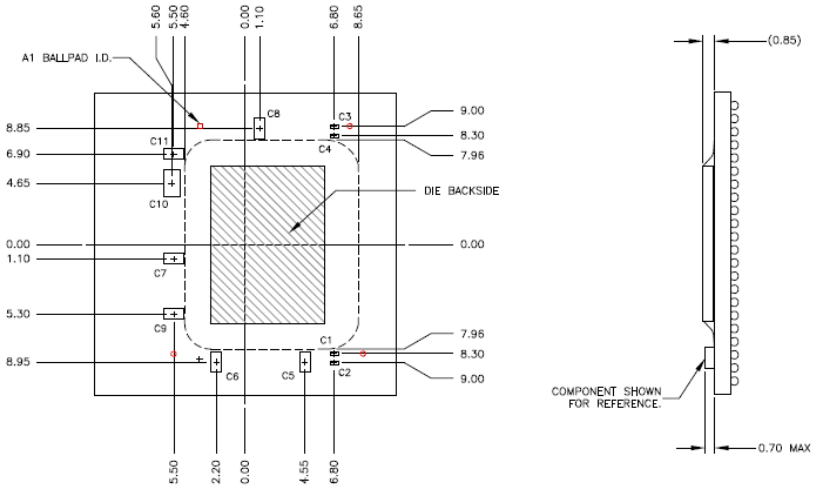


Figure 25 • **MPF200T-FCG484—Decoupling Capacitor Locations**



Note: The ball pinout and spacing are the same on both packages (that is, MPF100 and MPF200), which allows the user to use one PCB footprint.

Figure 26 • **MPF100T-FCG484 Package Top-View and Side-View**

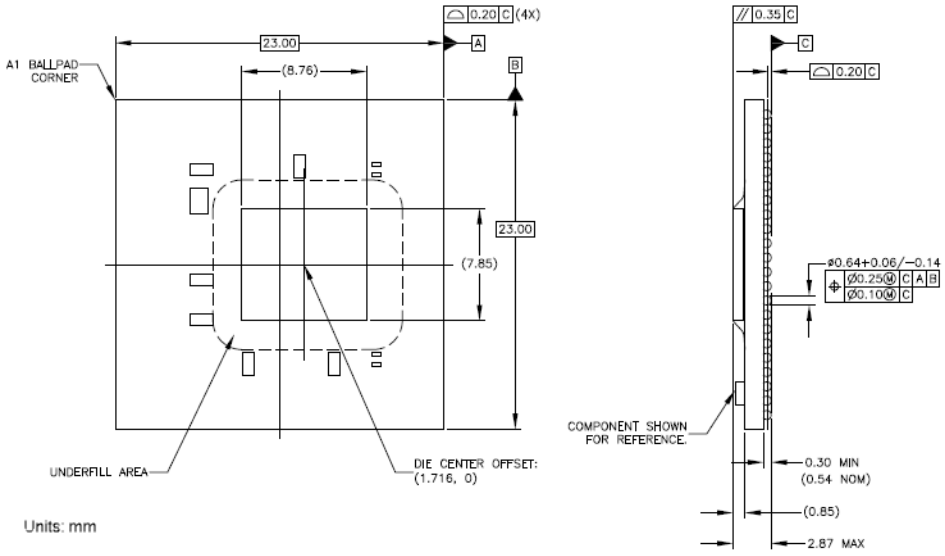


Figure 27 • **MPF100T-FCG484 Package Bottom-View**

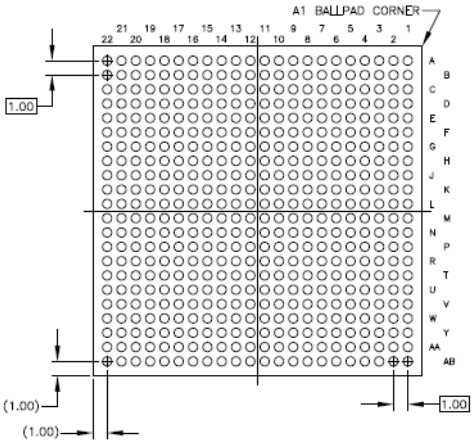


Figure 28 • **MPF100T-FCG484—Decoupling Capacitor Locations**

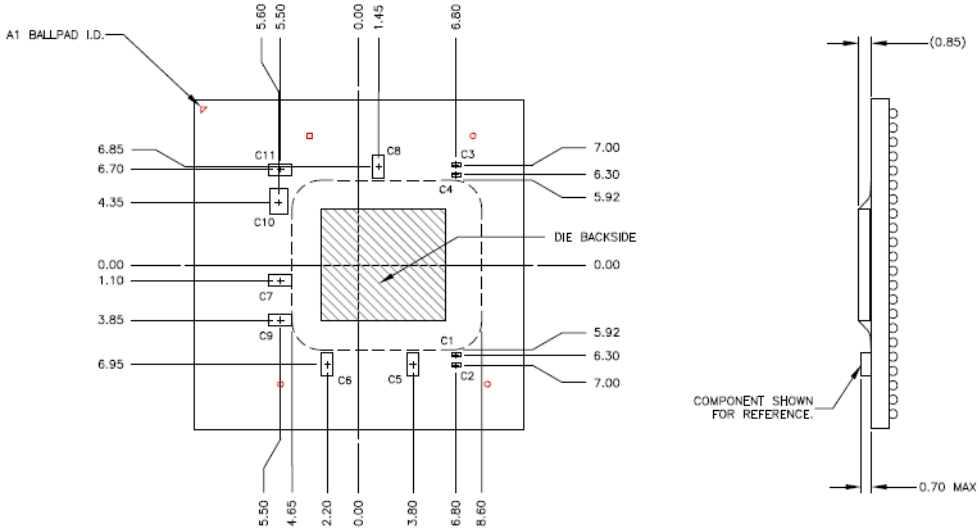
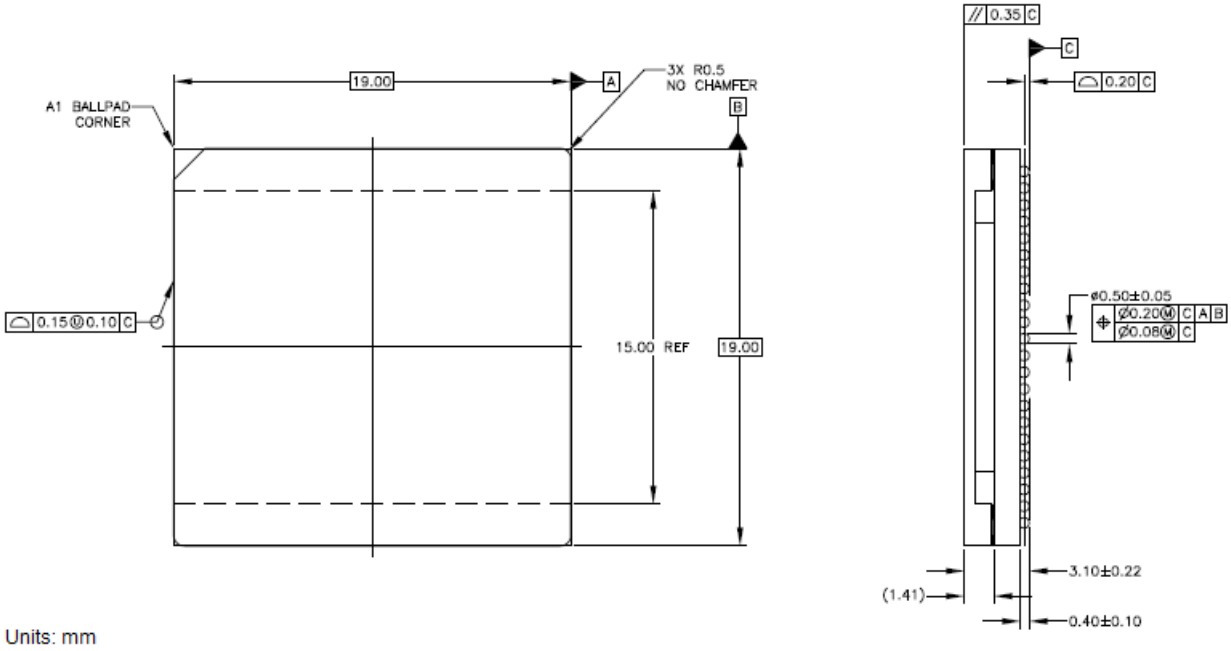


Figure 29 • **MPF300T/TS/MPF200T/MPF100T-FCVG484/FCV484M Package Top-View and Side-View**



Units: mm

Figure 30 • **MPF300T/TS/MPF200T/MPF100T-FCVG484/FCV484M Package Bottom-View**

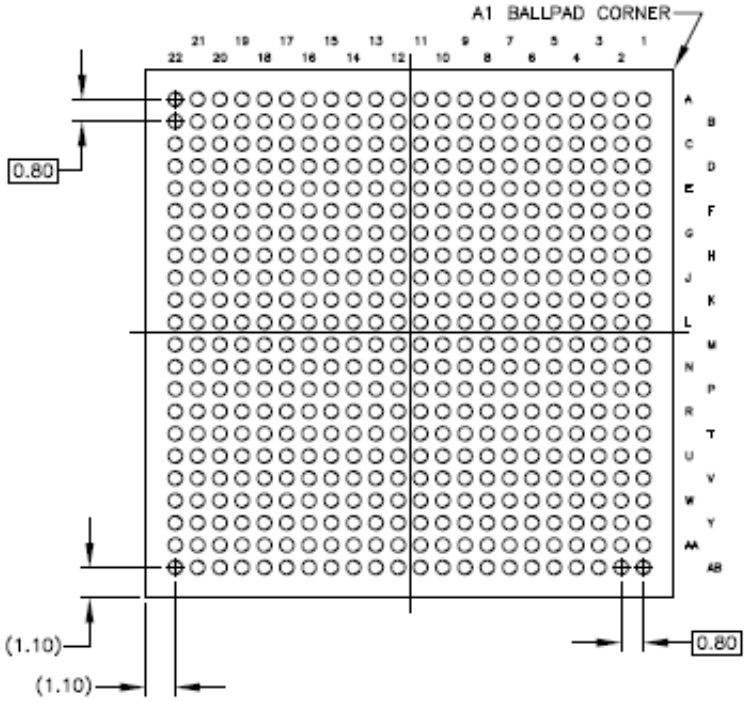


Figure 31 • **MPF300T/MPF200T-FCSG536 Package Top-View and Side-View**

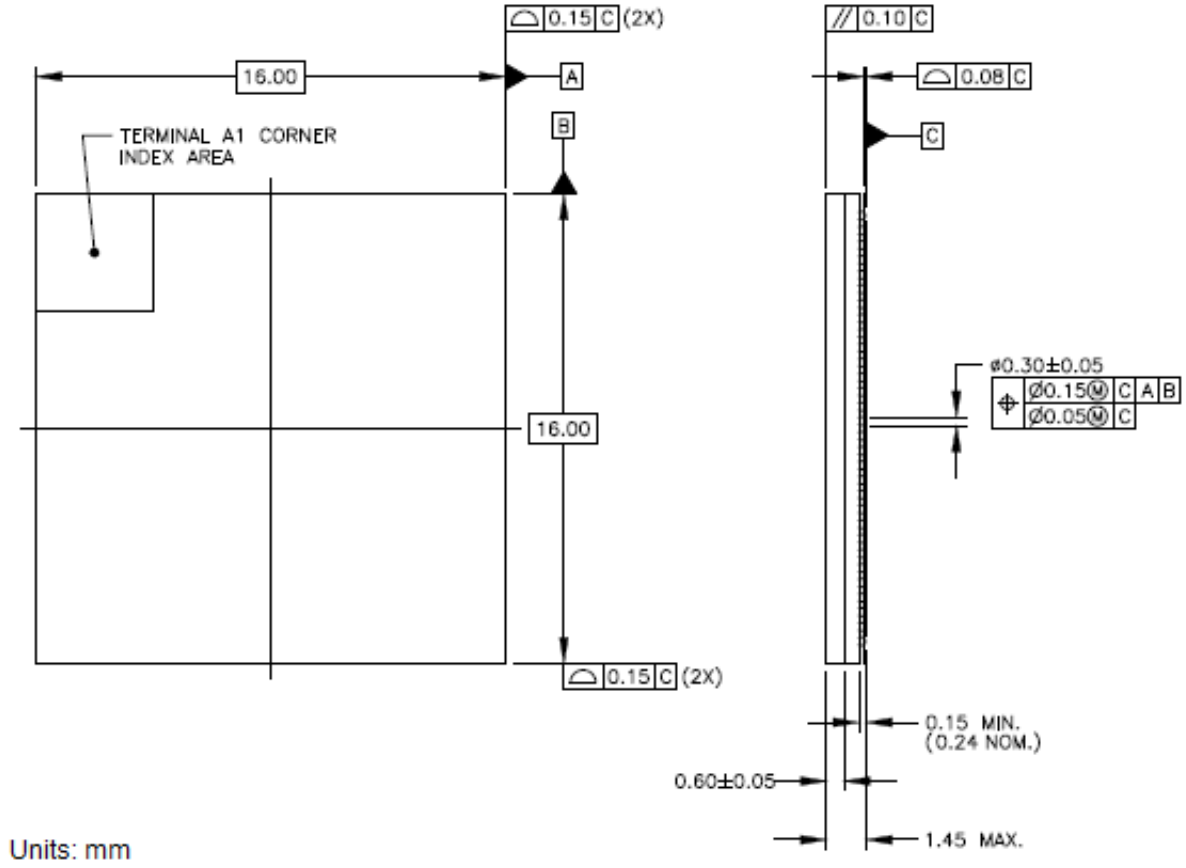


Figure 32 • **MPF300T/MPF200T-FCSG536 Package Bottom-View**

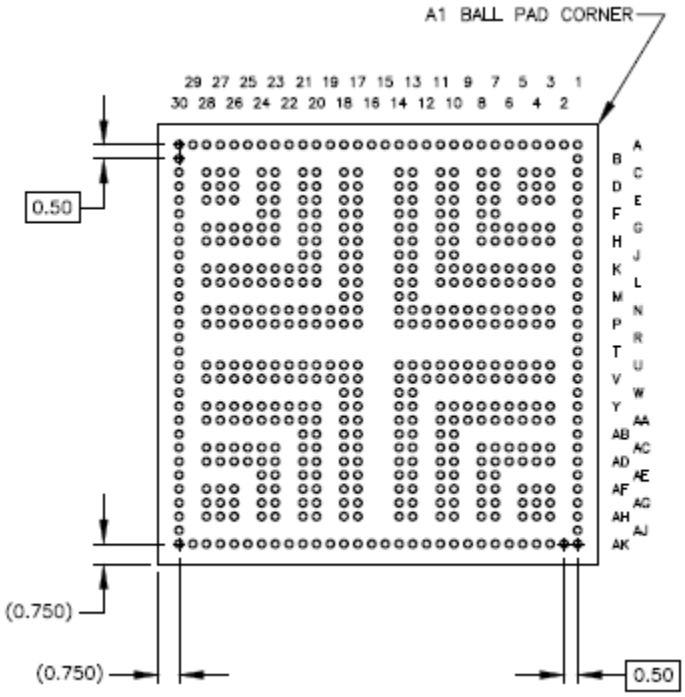


Figure 33 • **MPF200T-FCSG325 Package Top-View and Side-View**

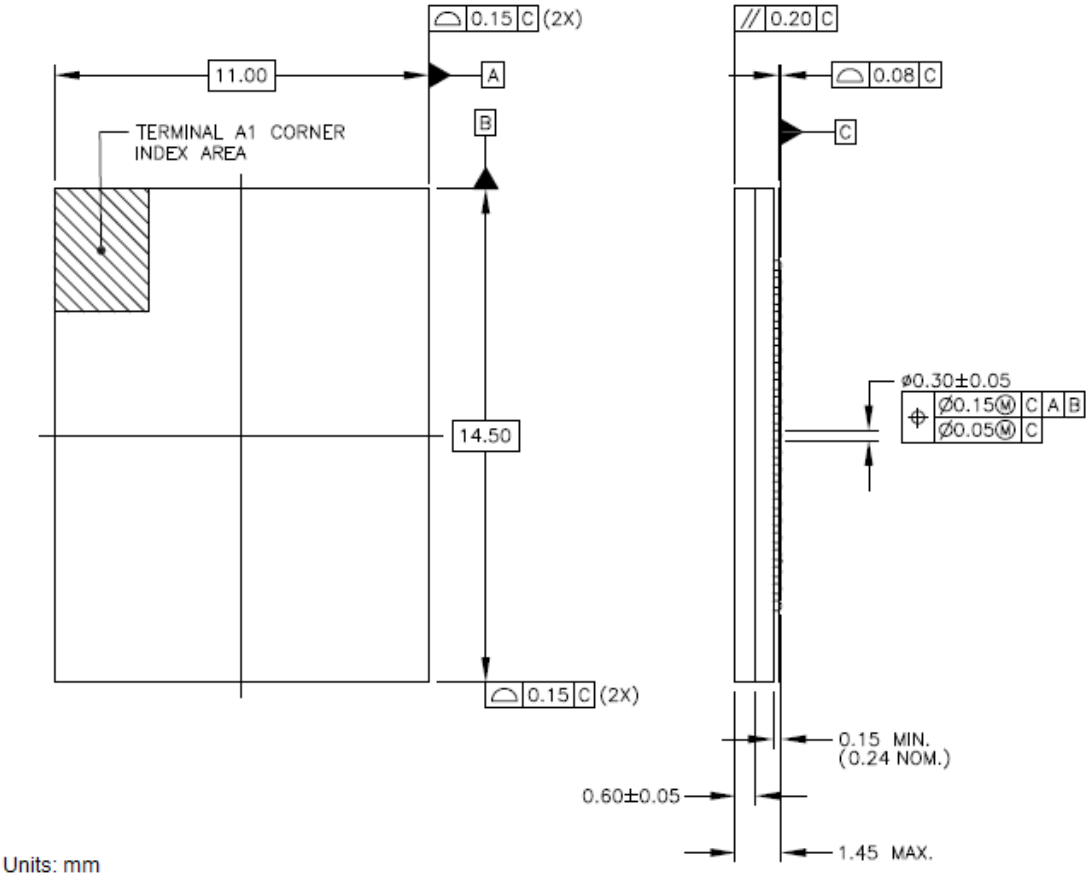


Figure 34 • **MPF200T-FCSG325 Package Bottom-View**

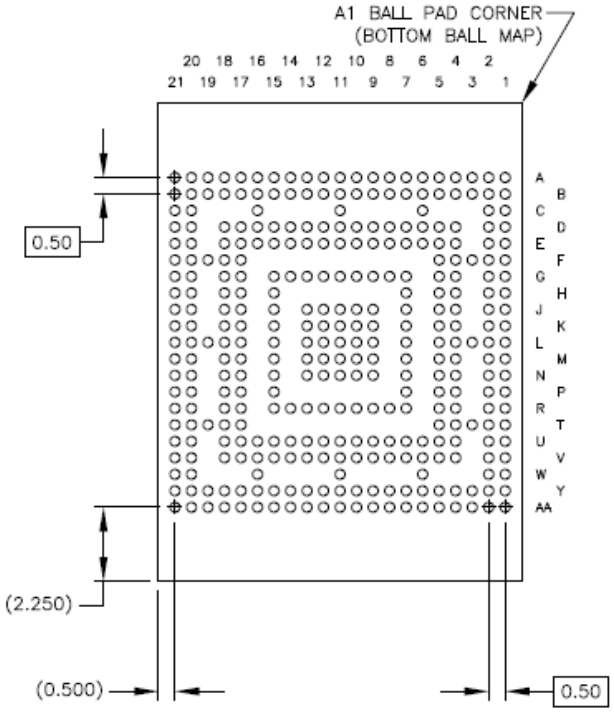


Figure 35 • **MPF100T-FCSG325 Package Top-View and Side-View**

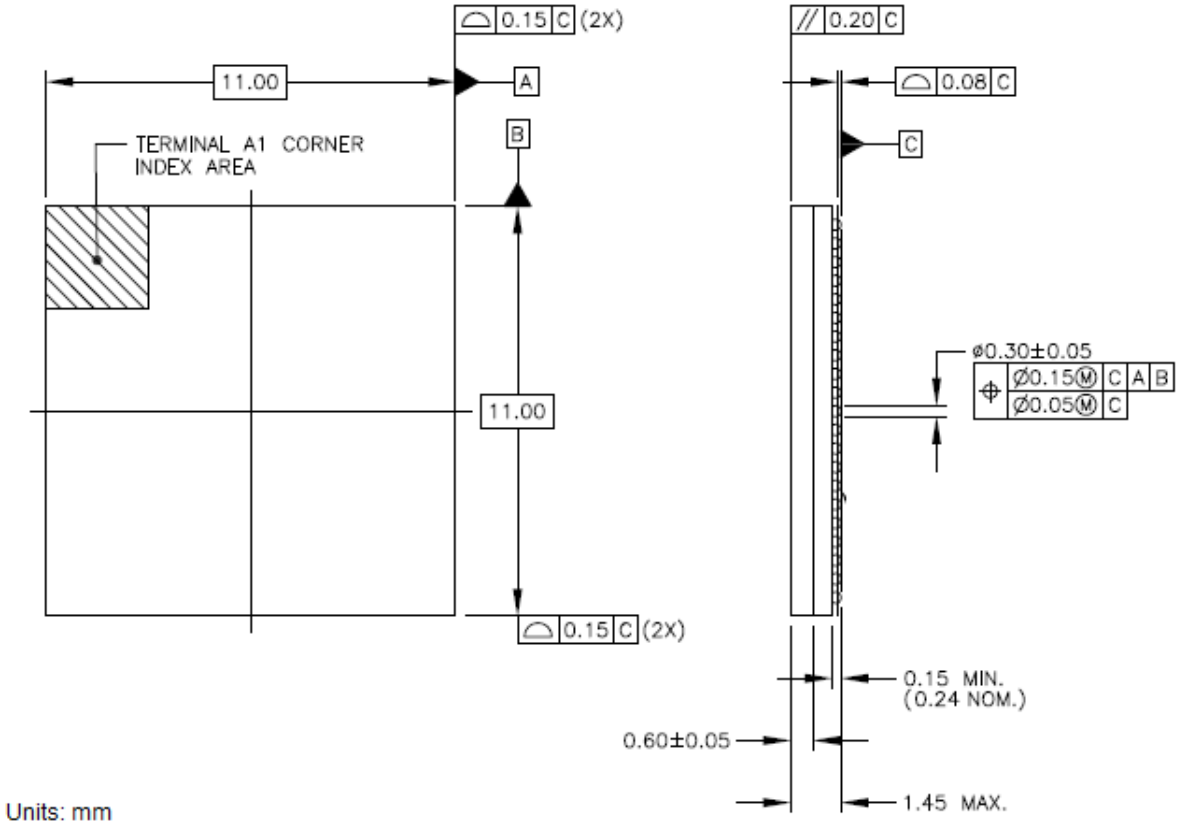
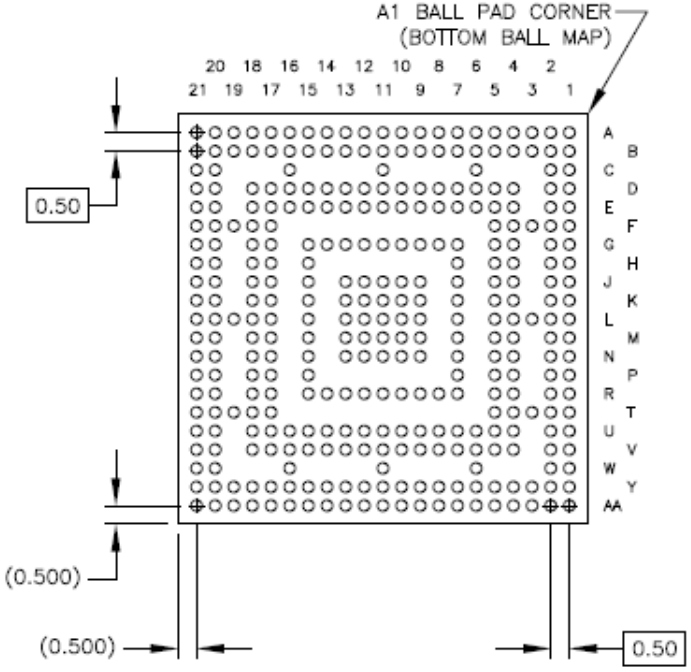


Figure 36 • **MPF100T-FCSG325 Package Bottom-View**



The following table lists the PolarFire FPGAs Package description and specification.

Table 17 • **PolarFire FPGAs Package Information**

		Package Specifications			
Package	**Description**	**Package type**	**Pitch (mm)**	**Size (mm)**	**Maximum I/Os**
FCG1152	Flip-chip with lid	BGA	1	35 × 35	512
FCG784	Flip-chip with lid	BGA	1	29 × 29	388
FCG484	Flip-chip	BGA	1	23 × 23	244
FCVG484	Flip-chip with lid	BGA	0.8	19 × 19	284
FCSG536	Flip-chip	CSP	0.5	16 × 16	300
FCSG325	Flip-chip	CSP	0.5	11 × 11, 11 × 14.5	170

2.8 Package Material Information

The following table lists the PolarFire ball grid array RoHS packages.

Table 18 • **PolarFire RoHS Packages**

Package Balls	**FCG1152**	**FCG784**	**FCG484**	**FCVG484**	**FCSG536**	**FCSG325**
Package Pitch	1 mm	1 mm	1 mm	0.8 mm	0.5 mm	0.5 mm
Substrate Material	Epoxy Glass	Epoxy Glass	Epoxy Glass	Epoxy Glass	BT Resin	BT Resin
Solder Ball Composition RoHS	SAC305	SAC305	SAC305	SAC305	SAC305	SAC105
Wafer Bump Material	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Cu Pillar + Solder Cap	Cu Pillar + Solder Cap

The following table lists the PolarFire ball grid array leaded packages.

Table 19 • **PolarFire Mil Temp Packages**

Package Balls	**FC1152M**	**FC784M**	**FC484M**	**FCV484M**	**FCS536M**	**FCS325M**
Package Pitch	1 mm	1 mm	1 mm	0.8 mm	0.5 mm	0.5 mm
Substrate Material	Epoxy Glass	Epoxy Glass	Epoxy Glass	Epoxy Glass	BT Resin	BT Resin
Solder Ball Composition RoHS	Sn63/Pb37	Sn63/Pb37	Sn63/Pb37	Sn63/Pb37	Sn63/Pb37	Sn63/Pb37
Wafer Bump Material	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Sn98.2/Ag1.8	Cu Pillar + Solder Cap	Cu Pillar + Solder Cap

All flip-chip BGA packages—FCG1152, FCG784, and FCVG484—are vented. FCG484 is a bare die package.

Table 20 • **PolarFire Ball Grid Array for RoHS and Leaded Packages**

Flip-chip Packages	Ball Pad Diameter (mm)	Ball Pad Opening (mm)	Vent Dimension (mm)	Vented Package
MPF500T - FCG1152 (with heat spreader)	0.60	0.50	1.0 ± 0.25	Yes (Vent hole diameter at Pin1 location)
MPF500T - FC1152M (with heat spreader)	0.60	0.50	1.0 ± 0.25	Yes (Vent hole diameter at Pin1 location)
MPF300T - FCG1152 (with heat spreader)	0.60	0.50	1.0 ± 0.25	Yes (Vent hole diameter at Pin1 location)
MPF500T - FCG784 (with heat spreader)	0.60	0.50	24 × 0.9	Yes (east and west side)
MPF500T - FC784M (with heat spreader)	0.60	0.50	24 × 0.9	Yes (east and west side)
MPF300T - FCG784 (with heat spreader)	0.60	0.50	24 × 0.9	Yes (east and west side)
MPF200T - FCG784 (with heat spreader)	0.60	0.50	24 × 0.9	Yes (east and west side)
MPF300T - FCG484 (Bare Die)	0.60	0.50		Bare Die
MPF300T - FC484M (with heat spreader)	0.60	0.50	17 × 0.9	Yes (north, south, east, and west)
MPF300T - FCV484M (with heat spreader)	0.50	0.40	15 × 0.9	Yes (east and west side)
MPF200T - FCG484 (Bare Die)	0.60	0.50		Bare Die
MPF100T - FCG484 (Bare Die)	0.60	0.50		Bare Die
MPF300T - FCVG484 (with heat spreader)	0.50	0.40	15 × 0.9	Yes (east and west side)
MPF200T - FCVG484 (with heat spreader)	0.50	0.40	15 × 0.9	Yes (east and west side)
MPF100T - FCVG484 (with heat spreader)	0.50	0.40	15 × 0.9	Yes (east and west side)
MPF300T - FCSG536 Over-mold	0.35	0.275		No (molded)
MPF300T - FCS536M Over-mold	0.35	0.275		No (molded)
MPF200T - FCSG325 Over-mold	0.35	0.275		No (molded)

2.9 Thermal Specifications

The following table lists the thermal resistances of PolarFire FPGA package device.

Table 21 • **PolarFire Package Thermal Resistance**

Package	Environment	Theta-JA	Theta-JB	Theta-JC	Psi-JB	Psi-JT	Unit
MPF500T-FCG1152/ MPF500T-FC1152M	Still Air	7.76	1.88	0.293	1.71	0.182	C/W
	1.0 m/s	5.81			2.69	0.185	
	2.5 m/s	4.98			2.57	0.187	
MPF300T-FCG1152	Still Air	8.00	2.09	0.429	1.96	0.290	C/W
	1.0 m/s	6.04			2.92	0.288	
	2.5 m/s	5.21			2.79	0.290	
MPF500T-FCG784/ MPF500T-FC784M	Still Air	9.31	2.72	0.199	2.23	0.081	C/W
	1.0 m/s	7.19			2.23	0.095	
	2.5 m/s	6.35			2.18	0.101	
MPF300T-FCG784	Still Air	9.51	2.95	0.254	2.46	0.114	C/W
	1.0 m/s	7.36			2.43	0.126	
	2.5 m/s	6.51			2.37	0.132	
MPF300T-FCG784N (Bare Die)	Still Air	11.21	3.52	0.045	3.37	0.009	C/W
	1.0 m/s	9.22			3.54	0.011	
	2.5 m/s	8.52			3.60	0.012	
MPF200T-FCG784	Still Air	9.68	3.10	0.345	2.65	0.156	C/W
	1.0 m/s	7.51			2.58	0.171	
	2.5 m/s	6.66			2.52	0.180	
MPF300T-FCG484 (Bare Die)	Still Air	12.40	5.09	0.047	4.16	0.010	C/W
	1.0 m/s	9.88			5.64	0.015	
	2.5 m/s	8.70			5.32	0.016	
MPF300T-FC484M (4-corner lid)	Still Air	11.74	4.69	0.476	3.68	0.170	C/W
	1.0 m/s	8.92			4.85	0.192	
	2.5 m/s	7.56			4.44	0.207	
MPF200T-FCG484 (Bare Die)	Still Air	12.80	5.56	0.622	4.58	0.014	C/W
	1.0 m/s	10.29			6.05	0.018	
	2.5 m/s	9.12			5.73	0.020	
MPF100T-FCG484 (Bare Die)	Still Air	13.52	6.37	0.979	5.30	0.021	C/W
	1.0 m/s	11.02			6.76	0.022	
	2.5 m/s	9.86			6.46	0.024	
MPF300T-FCVG484/ MPF300T-FCV484M	Still Air	13.19	4.51	0.251	3.66	0.100	C/W
	1.0 m/s	11.11			3.96	0.110	
	2.5 m/s	9.88			3.81	0.116	

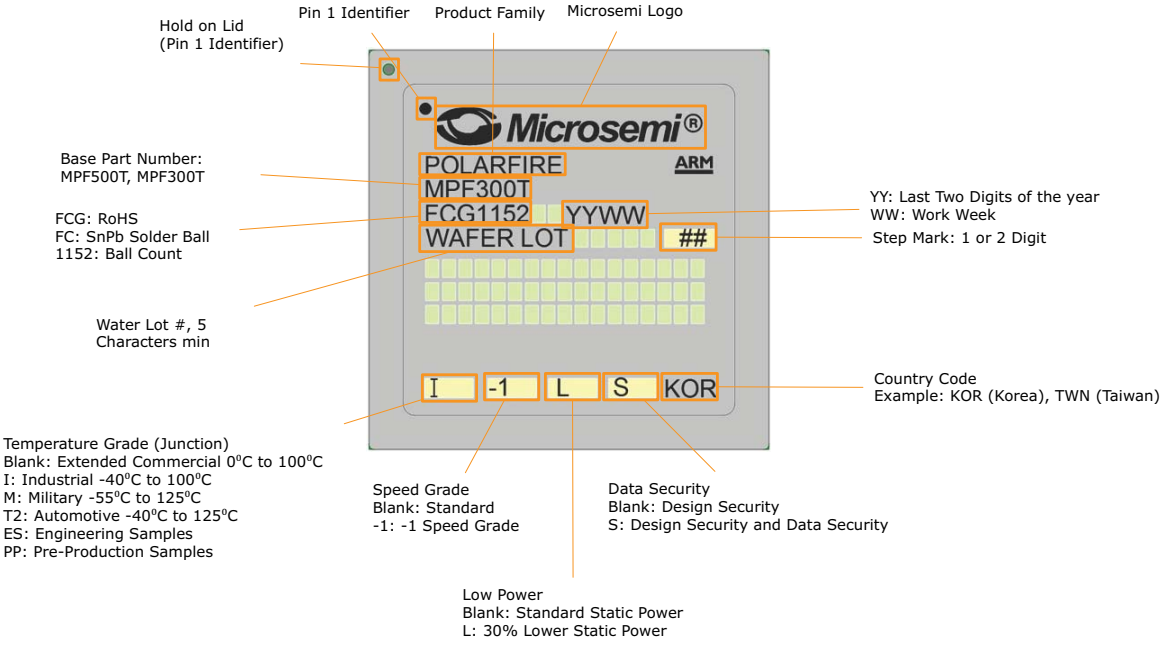
Table 21 • **PolarFire Package Thermal Resistance *(continued)***

Package	Environment	Theta-JA	Theta-JB	Theta-JC	Psi-JB	Psi-JT	Unit
MPF200T-FCVG484	Still Air	13.39	4.75	0.341	3.90	0.144	C/W
	1.0 m/s	11.30			4.18	0.157	
	2.5 m/s	10.06			4.02	0.166	
MPF100T-FCVG484	Still Air	13.67	5.02	0.509	4.17	0.247	C/W
	1.0 m/s	11.58			4.45	0.264	
	2.5 m/s	10.34			4.29	0.274	
MPF300T-FCSG536/ MPF300T-FCS536M	Still Air	14.17	3.46	1.749	3.57	0.054	C/W
	1.0 m/s	11.49			6.73	0.113	
	2.5 m/s	10.40			6.47	0.159	
MPF200T-FCSG536	Still Air	14.90	4.45	2.123	4.10	0.059	C/W
	1.0 m/s	12.32			7.53	0.119	
	2.5 m/s	11.19			7.23	0.187	
MPF200T-FCSG325/ MPF200T-FCS325M	Still Air	20.57	6.16	2.538	6.73	0.066	C/W
	1.0 m/s	17.31			11.75	0.167	
	2.5 m/s	15.64			11.20	0.268	
MPF100T-FCSG325	Still Air	21.18	6.88	3.570	5.83	0.074	C/W
	1.0 m/s	17.78			11.93	0.173	
	2.5 m/s	16.28			11.51	0.286	

2.10 Package Marking

Microsemi normally marks the full ordering part number on the top of each device. The following figure provides details for each character code present on Microsemi's PolarFire FPGA device.

Figure 37 • **Detailed Marking for Each Character Code**



2.11 Packing and Shipping

The PolarFire series device is packed in trays, which are used to pack most of the Microsemi surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

Table 22 • **Standard Device Counts per Tray and Carton**

Package	Maximum Number of Devices Per Tray	Maximum Number Trays Per Stack	Maximum Number of Units per Inner Carton
FCG1152	24	5	120
FCG484	60	5	300
FCVG484	84	5	420
FCSG536	90	5	450
FCSG325	176	5	880

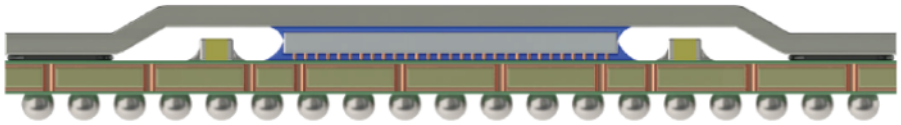
2.12 Thermal Management

Microsemi PolarFire FPGAs are offered in lidded flip-chip BGA (FCBGA) format. Lidded FCBGA features a controlled bond-line thermal interface material (TIM) thickness that reduces the thermal resistance (Theta-JC) between the junction and the externally applied thermal solution. The lid or heat spreader also spreads the heat away from the die to the package perimeter and to the printed circuit board.

Optimized package electrical performance with multiple power and ground planes to take care of signal return paths, and dense core via under the die to improve power delivery adds benefit in dissipating heat through the bottom of the package and to the board.

PolarFire FPGAs in FCG484 are also available in bare die FCBGA. Bare die flip-chip BGA produces the lowest possible thermal resistance (Theta-JC) between the junction and any externally applied thermal solution.

Figure 38 • **Heat Spreader with Thermal Interface Material**



2.12.1 System Level Heat Sink Solutions

The use of external heat sinks, component placement in the PCB, and air flow in the system depends on the physical and mechanical limitations of the system. A system level thermal design engineer must understand these limitations and device capabilities to effectively manage the complete thermal strategy.

2.13 Thermal Interface Material

When using external heat sinks, a suitable thermal interface material must be considered to effectively transfer the heat from the component to the heat sink, and eventually to the environment.

For bare-die flip-chip BGAs, the surface of the silicon contacts the heat sink. For lidded flip-chip BGAs, the lid contacts the heat sink. The surface size of the bare-die flip-chip BGA and lidded flip-chip BGAs are different. Microsemi recommends a different type of thermal material for long-term use with each type of flip-chip BGAs package.

For lidded flip-chip BGAs, the lid contacts the external heat sink while bare die flip-chip BGAs, the surface of the silicon contacts the external heat sink. The surface areas of lidded flip-chip BGAs and bare die flip-chip BGAs are different. The system level thermal design engineer must choose the appropriate TIM to be used.

Thermal interface material is required because the surfaces of both the PolarFire package and heat sinks base are not smooth. The surface roughness reduces the effective contact area between the package and the heat sinks base. The insulating air gaps created by voids between contacting surfaces are too large. The thermal interface materials fills these gaps and allows an effective conductive transfer of heat from the package to the external heat sink.

Selection of the appropriate thermal interface material is critical to ensure the lowest thermal contact resistance. One must consider the thermal conductivity of the TIM—flatness of the surface contact areas, the applied pressure on the thermal interface material and the total thermal contact area. In addition to thermal performance, TIMs are selected based on the ease of use in assembly and long term reliability.

2.13.1 Heat Sink Attachments

There are six main methods for heat sink attachment. The following table lists their advantages and disadvantages.

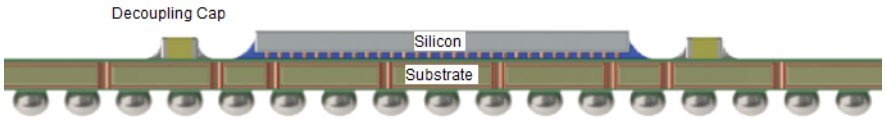
- Thermal tape
- Thermally conductive adhesive
- Wire form Z-clips
- Plastic clip-ons
- Threaded stand-offs (PEMs) and compression springs
- Push-pins and compression springs
- Thermal compound (also called as thermal gel, thermal grease, thermal paste, heat-sink paste or heat-sink compound)

2.14 Heat Sink Guidelines for Bare-die Flip-Chip Packages

Heat sinks can be attached to the package in multiple ways. For heat to dissipate effectively, the advantages and disadvantages of each heat sink attachment method must be considered. Factors influencing the selection of the heat sink attachment method include the package type, contact area of the heat source, and the heat sink type.

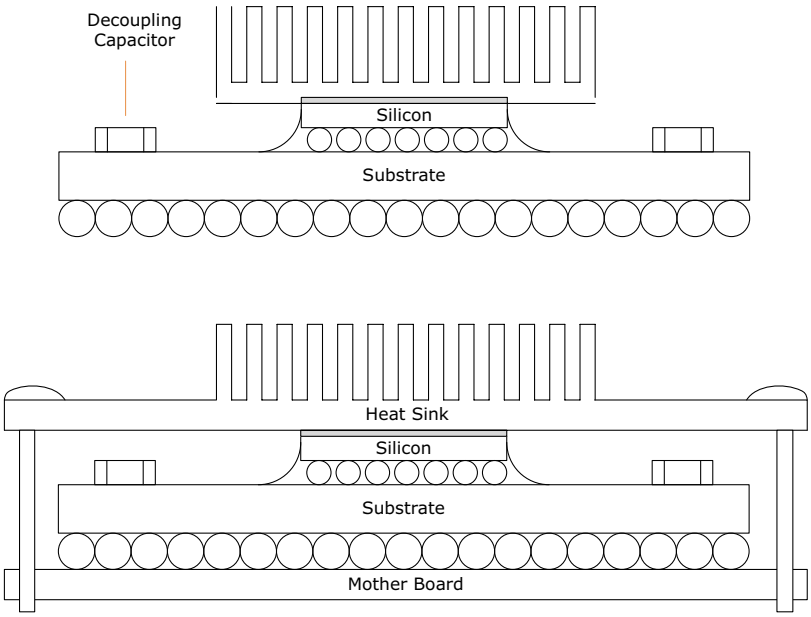
When designing heat sink attachments for bare-die flip-chip BGA packages, the height of the die above the substrate and also the height of decoupling capacitors must be considered. This is to prevent electrical shorting between the heat sink (metal) and the decoupling capacitors. When attaching the heat sink to the bare-die flip-chip BGA, ensure that the TIM thickness and the force applied during heat sink placement are even.

Figure 39 • **Cross Section of Bare-die Flip-chip BGA**



Care must be taken while attaching a heat sink to the bare-die package after the component is placed onto the PCBs.

Figure 40 • **Recommended Application of Heat Sink**



2.15 Heat Sink Removal Procedure

The heat spreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heat sink subjects the lid adhesion joint to continuous tension or shear, extra support might be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heat sink joint from the corners and carefully pry the heat sink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

2.16 Recommended PCB Design Rules for BGA Packages

Microsemi provides the diameter of a land pad on the package side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are shown in the following figure and summarized in Table 23, page 39. For Microsemi BGA packages, non-solder mask defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter) and the solder mask opening (diameter) as shown in the following figure.

The space between the NSMD pad and the solder mask; the actual signal trace widths and via dimensions depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Figure 41 • **Ball and Via Dimensions**

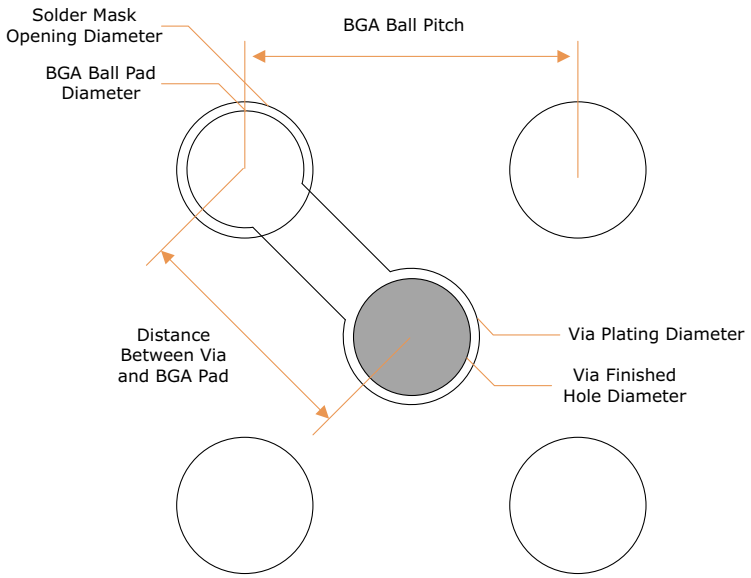


Table 23 • **Recommended PCB Design Rules**

	0.5 mm Pitch	0.8 mm Pitch	1.0 mm Pitch
Design Rule for Packages	**FCSG**	**FCVG**	**FCG**
BGA Ball Pad Diameter	0.27 mm	0.4 mm	0.51 mm
Solder mask opening diameter	0.3 mm	0.43 mm	0.54 mm
BGA Ball pitch	0.5 mm (19.7 mils)	0.8 mm (31.5 mils)	1.00 mm (39.37 mils)
Line width between via and solder land	0.13 mm	0.13 mm	0.15 mm
Distance between via and solder Land	0.35 mm	0.56 mm	0.7 mm
Via Finished hole diameter	0.1 mm	0.33 mm	0.33 mm
Via Plating Diameter	0.25 mm	0.48 mm	0.48 mm

Note: For more information about package fanout, see *AC462: PolarFire FPGA Package Fanout Application Note*.

2.17 Moisture Sensitive Level

The following table lists Microsemi PolarFire packages moisture sensitive levels (MSL). For information about solder re-flow guidelines for Sn/Pb and Pb-free, see *https://www.microsemi.com/company/quality/soldering-profiles*

Table 24 • **Moisture Sensitive Levels**

Package	MSL
FCG1152	4
FCG784	4
FCG484	4
FCVG484	4
FCSG536	3
FCSG325	3