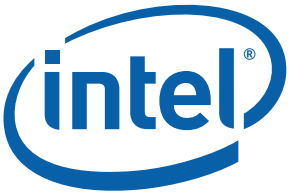

Intel® Xeon® Processor E7-8800/4800/2800 v2 Product Family

Datasheet - Volume One

Electrical, Mechanical and Thermal Specifications - Volume 1 of 3

February 2014

Reference Number: 329594-001

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Revision History

Document Number	Revision Number	Description	Revision Date
329594	001	Initial Release	February 2014

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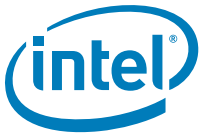


1 Overview

1.1 Introduction

ALL INFORMATION IN THIS DOCUMENT IS PRELIMINARY AND SUBJECT TO CHANGE.

The *Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family Datasheet - Volume One* provides DC and AC electrical specifications, signal integrity, differential signaling specifications, land and signal definitions, and an overview of additional processor feature interfaces.

This document is intended to be distributed as a part of the complete EDS document which consists of three volumes.

The Intel® Xeon® E7 v2 processors are the next generation of 64-bit, multi-core enterprise processors built on 22-nanometer process technology. Throughout this document, the Intel® Xeon® E7 v2 processor may be referred to as simply the processor. Based on the low-power/high performance Intel® Xeon® E7 v2 processor microarchitecture, the processor is designed for a three-chip platform as opposed to the previous four-chip platform. The three-chip platform consists of a processor, memory buffer, and the Platform Controller Hub (PCH) and enables higher performance, easier validation, and improved x-y footprint. The Intel® Xeon® E7 v2 processor is designed for enterprise workloads and maximum memory expendability**.** The Intel® Xeon® E7 v2 processor supports scalable server and HPC platforms of two or more processors, including “glueless” 8-way platforms.

These processors feature per socket, four Intel® Scalable Memory Interconnect (Intel® SMI) Gen 2 memory links with speeds up to 2.67 GT/s, three Intel® QuickPath Interconnect (Intel® QPI) point-to-point links capable of up to 8.0 GT/s, up to 32 lanes of PCI Express* 3.0 links capable of 8.0 GT/s, and 4 lanes of DMI2/PCI Express* 2.0 interface with a peak transfer rate of 5.0 GT/s. The processor supports up to 46 bits of physical address space and 48-bit of virtual address space.

Included in this family of processors is integrated I/O (IIO) (such as PCI Express and DMI2) on a single silicon die. This single die solution is known as a monolithic processor.

Figure 1-1, Figure 1-2, and Figure 1-3, show the Intel® Xeon® E7 v2 2-socket, 4-socket and 8 socket platform configurations. The “Legacy CPU” is the boot processor that is connected to the PCH component, this socket is set to NodeID[0]. In the 4-socket configuration, the “Remote CPU” is the processor which is not connected to the Legacy PCH.

Figure 1-1. Intel® Xeon® E7 v2 Processor on a 2 Socket Platform

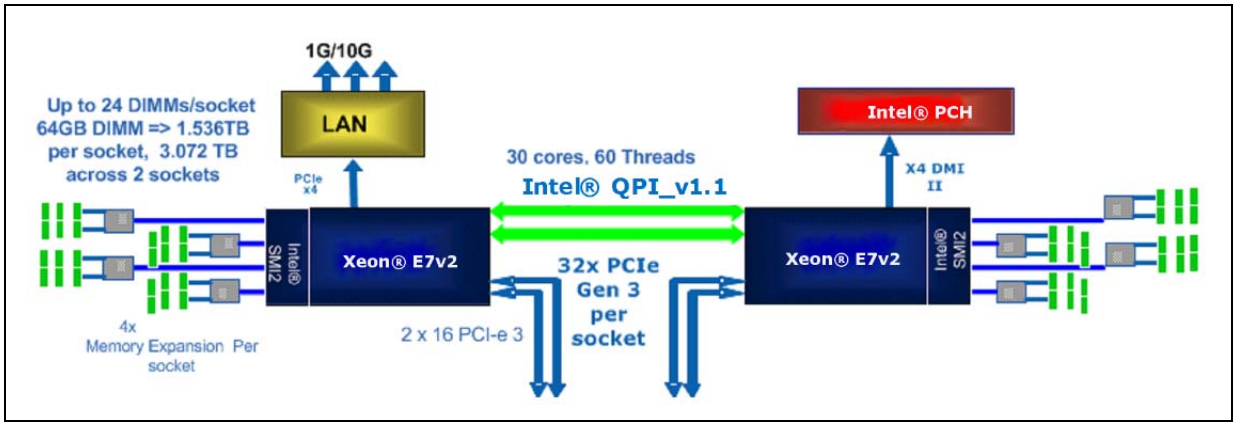


Figure 1-2. Intel® Xeon® E7 v2 Processor on a 4 Socket Platform

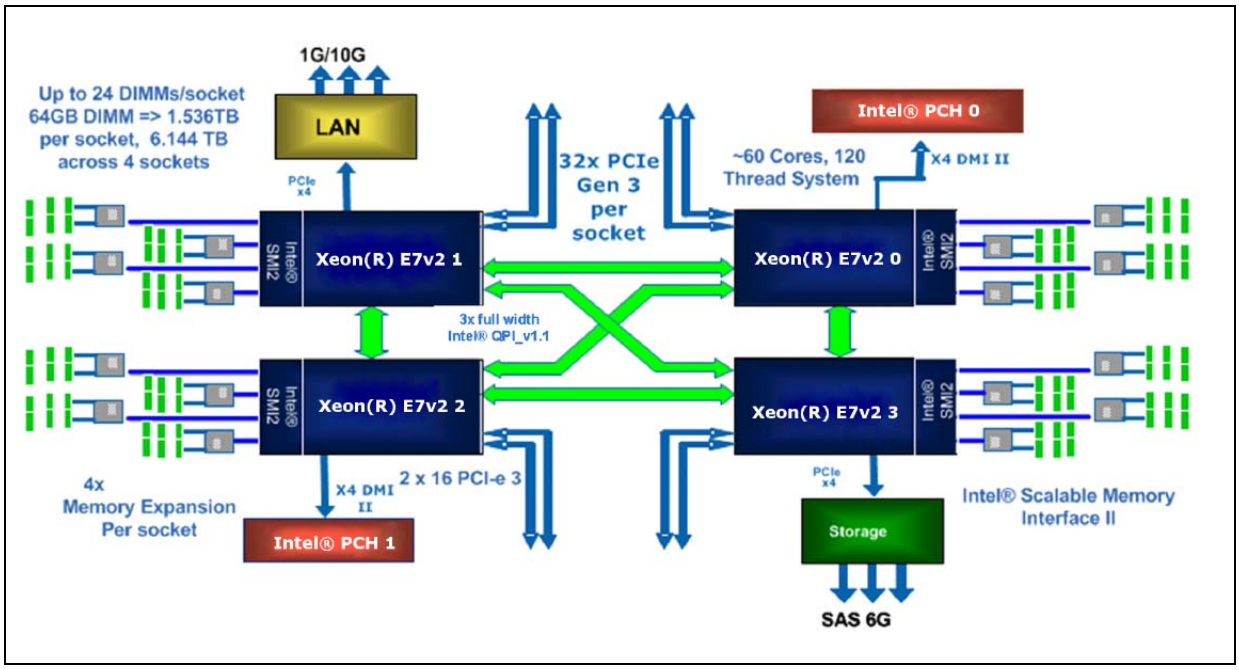
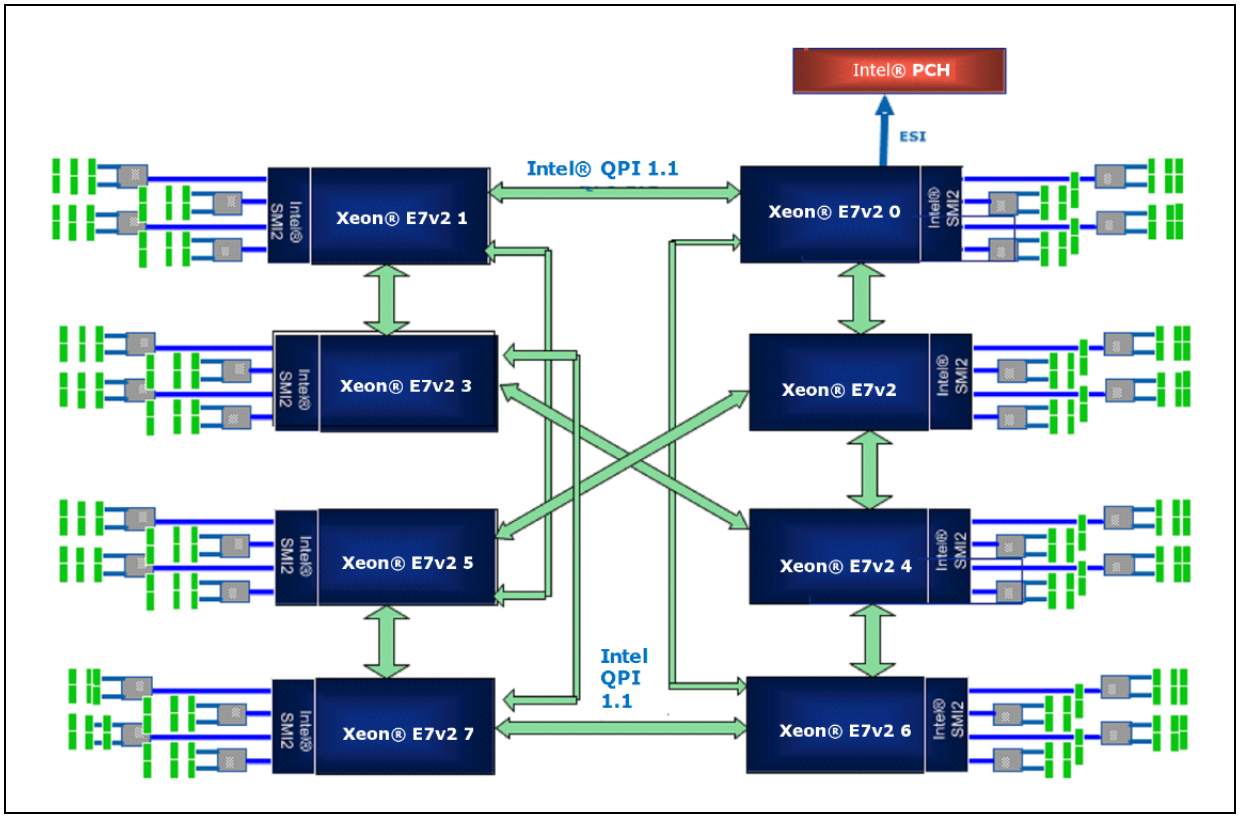


Figure 1-3. Intel® Xeon® E7 v2 Processor on a 8 Socket Platform



1.1.1 Processor Feature Details

- Each core supports two threads (Intel® Hyper-Threading Technology), up to 30 threads per socket
- 46-bit physical addressing and 48-bit virtual addressing
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data mid-level (L2) cache for each core
- Up to 37.5 MB last level cache (LLC): up to 2.5 MB per core instruction/data last level cache (LLC), shared among all cores
- The Intel® Xeon® E7 v2 processor supports Directory Mode to reduce unnecessary Intel QuickPath Interconnect traffic by tracking cache lines present in remote sockets.

1.1.2 Supported Technologies

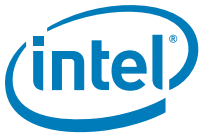
- Intel® Virtualization Technology (Intel® VT)
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® 64 Architecture
- Intel® Streaming SIMD Extensions 4.1 (Intel® SSE4.1)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)

- Intel® Advanced Vector Extensions (Intel® AVX)
- Intel® Hyper-Threading Technology
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Intel® Intelligent Power Technology
- Enhanced Intel SpeedStep® Technology

1.2 Interfaces

1.2.1 System Memory Support

- Intel® Xeon® E7 v2 processor supports 4 Intel® SMI Gen2 channels
- Registered DDR3 DIMMs
- LR DIMM (Load Reduced DIMM) for buffered memory solutions demanding higher capacity memory subsystems
- Independent channel mode or lockstep mode
- Data burst length of eight cycles for independent channel mode and burst length of 4 cycles for lockstep mode
- Memory DDR3 data transfer rates of 1066, 1333, and 1600 MT/s
- 64-bit wide channels plus 8-bits of ECC support for each channel
- DDR3 standard I/O Voltage of 1.5 V and DDR3 Low Voltage of 1.35 V
- 2-GB, 4-GB and 8-GB DDR3 DRAM technologies supported
- Up to 24 DIMMs supported per socket
- RAS Support (including and not limited to):
  - Rank Level Sparing
  - Demand and Patrol Scrubbing
  - DRAM Single Device Data Correction (SDDC) for any single x4 or x8 DRAM device failure in lock step mode, and x4 in independent mode
  - Lockstep mode where channels 0 & 1 and channels 2 & 3 are operated in lockstep mode
  - The combination of rank sparing and memory mirroring is not supported
  - Data scrambling with address to ease detection of write errors to an incorrect address
  - Error reporting via Machine Check Architecture
  - Read Retry during CRC error handling checks by iMC
  - Channel mirroring within a memory controller on a socket
  - Channel Mirroring mode is supported on memory channels 0 & 1 and channels 2 & 3
  - Error Containment Recovery
- Improved Thermal Throttling with dynamic Closed Loop Thermal Throttling (CLTT)
- Memory thermal monitoring support for DIMM temperature via two memory pins, MEM_HOT_C{01/23}_N



1.2.2 PCI Express*

- The PCI Express* port(s) are fully-compliant to the *PCI Express* Base Specification, Revision 3.0 (PCIe 3.0)*
- Support for PCI Express* 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s)
- Up to 32 lanes of PCI Express* interconnect for general purpose PCI Express* devices at PCIe* 3.0 speeds that are configurable for up to 8 independent ports
- 4 lanes of PCI Express* at PCIe* 2.0 speeds when not using DMI2 port (Port 0), also can be downgraded to x2 or x1
- Negotiating down to narrower widths is supported
  - — x16 port (Port 2 & Port 3) may negotiate down to x8, x4, x2, or x1
  - — x8 port (Port 1) may negotiate down to x4, x2, or x1
  - — x4 port (Port 0) may negotiate down to x2, or x1
  - — When negotiating down to narrower widths, there are caveats as to how lane reversal is supported
- Address Translation Services (ATS) 1.0 support
- Hierarchical PCI-compliant configuration mechanism for downstream devices.
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space
- PCI Express* Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset
- Supports receiving and decoding 64 bits of address from PCI Express*
  - — Memory transactions received from PCI Express* that go above the top of physical address space (when Intel VT-d is enabled, the check would be against the translated HPA (Host Physical Address) address) are reported as errors by the processor
  - — Outbound access to PCI Express* will always have address bits 63 to 46 cleared
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- Power Management Event (PME) functions
- Message Signaled Interrupt (MSI and MSI-X) messages
- Degraded Mode support and Lane Reversal support
- Static lane numbering reversal and polarity inversion support

1.2.3 Direct Media Interface Gen 2 (DMI2)

- Serves as the chip-to-chip interface to the Intel® C600 series chipset PCH
- The DMI2 port supports x4 link width and only operates in a x4 mode when in DMI2
- Operates at PCI Express* 1.0 or 2.0 speeds
- Transparent to software
- Processor and peer-to-peer writes and reads with 64-bit address support

- APIC and Message Signaled Interrupt (MSI) support. Will send Intel-defined “End of Interrupt” broadcast message when initiated by the processor.
- System Management Interrupt (SMI), SCI, and SERR error indication
- Static lane numbering reversal support
- Supports DMI2 virtual channels VC0, VC1, VCm, and VCp

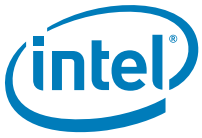
1.2.4 Intel® QuickPath Interconnect (Intel® QPI)

- Compliant with Intel QuickPath Interconnect v1.1 standard packet formats
- Implements three full width Intel QPI ports
- Full width port includes 20 data lanes and 1 clock lane
- 64 byte cache-lines
- Home snoop based coherency
- 4-bit Node ID
- 46-bit physical addressing support
- No Intel QuickPath Interconnect bifurcation support
- Differential signaling
- Forwarded clocking
- Up to 8.0 GT/s data rate (up to 16 GB/s per direction peak bandwidth per port)
  - — Ports 0 & 1 run at same operational frequency
  - — Port 2 may run at a separate operational frequency
  - — Reference Clock is 100 MHz
  - — Slow boot speed initialization at 50 MT/s
- Common reference clocking (same clock generator for both sender and receiver)
- Intel® Interconnect Built-In-Self-Test (Intel® IBIST) for high-speed testability
- Polarity and Lane reversal

1.2.5 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master. The PECI interface is based on revision 3.0 of the *RS - Platform Environment Control Interface (PECI) Specification*.

- Supports operation at up to 2 Mbps data transfers
- Link layer improvements to support additional services and higher efficiency over PECI 2.0 generation
- Services include CPU thermal and estimated power information, control functions for power limiting, P-state and T-state control, and access for Machine Check Architecture registers and PCI configuration space (both within the processor package and downstream devices)
- PECI address determined by SOCKET_ID configuration
- Single domain (Domain 0) is supported



1.3 Power Management Support

1.3.1 Processor Package and Core States

- ACPI C-states as implemented by the following processor C-states:
  - Package: PC0, PC1/PC1E, PC3, PC6
  - Core: CC0, CC1/CC1E, CC3, CC6
- Enhanced Intel SpeedStep Technology

1.3.2 System States Support

- S0, S1(transitional only),S4, S5

1.3.3 Memory Controller

- Memory thermal monitoring via MEM_HOT_C01_N and MEM_HOT_C23_N pins

1.3.4 PCI Express*

- L0s and L1 low power states

1.3.5 Intel® QPI

- L0s, L0p, and L1 power management capabilities

1.4 Thermal Management Support

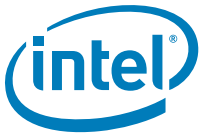
- Digital Thermal Sensor with multiple on-die temperature zones
- Adaptive Thermal Monitor
- THERMTRIP_N and PROCHOT_N signal support
- On-Demand mode clock modulation
- Closed Loop Thermal Throttling
- Fan speed control with DTS
- Two integrated SMBus masters for accessing thermal data from DIMMs
- New Memory Thermal Throttling features via MEM_HOT_C{01/23}_N pins
- Running Average Power Limit (RAPL), Processor and DRAM Thermal and Power Optimization Capabilities

1.5 Package Summary

The Intel® Xeon® E7 v2 processor socket type is noted as Socket R1. It is a 52.5 x 45 mm FCLGA package (LGA2011-1).

1.6 Terminology

Term	Description
ASPM	Active State Power Management
BMC	Baseboard Management Controllers
Cbo	Cache and Core Box. It is a term used for internal logic providing ring interface to LLC and Core.
DDR3	Third generation Double Data Rate SDRAM memory technology that is the successor to DDR2 SDRAM
DMA	Direct Memory Access
DMI	Direct Media Interface
DMI2	Direct Media Interface Gen 2
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Flit	Flow Control Unit. The Intel QPI Link layer's unit of transfer; 1 Flit = 80-bits.
Functional Operation	Refers to the normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical, and thermal, are satisfied.
IMC	The Integrated Memory Controller. A Memory Controller that is integrated in the processor die.
IIO	The Integrated I/O Controller. An I/O controller that is integrated in the processor die.
Intel® ME	Intel® Management Engine (Intel® ME)
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Turbo Boost Technology	Intel® Turbo Boost Technology is a way to automatically run the processor core faster than the marked frequency if the part is operating under power, temperature, and current specifications limits of the Thermal Design Power (TDP). This results in increased performance of both single and multi-threaded applications.
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology (Intel® VT)	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist for enabling I/O device virtualization. It is under system software (Virtual Machine Manager or OS) control. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.



Term	Description
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
IOV	I/O Virtualization
LGA2011-1 Socket	The 2011-0 land FCLGA package mates with the system board through this surface mount, 2011-0 contact socket.
LLC	Last Level Cache
LRDIMM	Load Reduced Dual In-line Memory Module
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
NEBS	Network Equipment Building System. NEBS is the most common set of environmental design guidelines applied to telecommunications equipment in the United States.
PCH	Platform Controller Hub. The next generation chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PCU	Power Control Unit
PCI Express* 3.0	The third generation PCI Express* specification that operates 60% faster than PCI Express* 2.0 (8 GB/s); however, PCI Express* 3.0 is completely backward compatible with PCI Express* 1.0 and 2.0.
PCI Express 3.0	PCI Express* Generation 3.0
PCI Express 2.0	PCI Express* Generation 2.0
PCI Express 1.0	PCI Express* Generation 2.0/3.0
PECI	Platform Environment Control Interface
Phit	Physical Unit. An Intel® QPI terminology defining units of transfer at the physical layer. 1 Phit is equal to 20 bits in ‘full width mode’ and 10 bits in ‘half width mode’
Processor	The 64-bit, single-core or multi-core component (package)
Processor Core	The term “processor core” refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
RDIMM	Registered Dual In-line Module
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR3 DIMM.
Intel® Xeon® E7 v2 Processor	Intel® Xeon® E7 v2 processor supports scalable server and HPC platforms for two or more processors, including glueless four-way and glueless eight-way platforms.
Scalable-2S,4S, 8S	Targeted for scalable designs, including those using third party Node Controller chips. In these designs, Node Controller is used to scale the design beyond two/four/eight sockets.
SCI	System Control Interrupt. Used in ACPI protocol.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
SKU	A processor Stock Keeping Unit (SKU) to be installed in either server or workstation platforms. Electrical, power and thermal specifications for these SKU’s are based on specific use condition assumptions. Server processors may be further categorized as Efficient Performance server, workstation and HPC SKUs. For further details on use condition assumptions, please refer to the latest Product Release Qualification (PRQ) Report available via your Customer Quality Engineer (CQE) contact.
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I2C* two-wire serial bus from Philips Semiconductor.

Term	Description
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to “free air” (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TSOD	Thermal Sensor on DIMM
UDIMM	Unbuffered Dual In-line Module
Uncore	The portion of the processor comprising the shared cache, IMC, HA, PCU, UBox, and Intel QPI link interface.
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,…., t_k then the UI at instance “n” is defined as: $UI_n = t_n - ()t_{n-1}$)
V_{CC}	Processor core power supply
V_{SS}	Processor ground
$V_{VMSE\_}01$, $V_{VMSE\_}23$	Variable power supply for the processor system memory interface. VVMSE is the generic term for VVMSE_01, VVMSE_23.
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.7 Related Documents

Refer to the following documents for additional information.

Table 1-1. Processor Documents

Document	Document Number
Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family Datasheet - Volume Two: Functional Description	329595-001
Intel® Xeon® Processor E7-2800/4800/8800 v2 Processor Thermal/Mechanical Design Guide	329596-001
Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family Specification Update	329597-001
Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family BSDL (Boundary Scan Description Language)	329598-001

Table 1-2. Public Specifications (Sheet 1 of 2)

Document	Document Number/ Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express® Base Specification - Revision 2.1 and 1.1 *PCI Express® Base Specification - Revision 3.0 DRAFT*	http://www.pcisig.com
System Management Bus (SMBus) Specification	http://smbus.org/

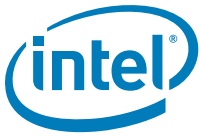


Table 1-2. Public Specifications (Sheet 2 of 2)

Document	Document Number/ Location
DDR3 SDRAM Specification	http://www.jedec.org
Low (JESD22-A119) and High (JESD-A103) Temperature Storage Life Specifications	http://www.jedec.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals • Volume 1: Basic Architecture • Volume 2A: Instruction Set Reference, A-M • Volume 2B: Instruction Set Reference, N-Z • Volume 3A: System Programming Guide • Volume 3B: System Programming Guide *Intel® 64 and IA-32 Architectures Optimization Reference Manual*	http://www.intel.com/products/processor/manuals/index.htm
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	http://download.intel.com/technology/computing/vptech/Intel(r)_VT_for_Direct_IO.pdf
Intel® Trusted Execution Technology Software Development Guide	http://www.intel.com/technology/security/

1.8 State of Data

The data contained within this document is the most accurate information available by the publication date of this document. The information in this revision of the document is based on silicon characterization data. Values may change prior to production.

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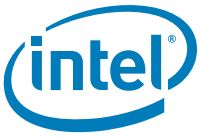
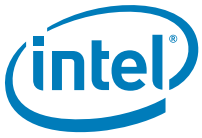




2 Technologies

2.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

- Intel® Virtualization Technology (Intel® VT) for Intel® 64 and IA-32 Intel® Architecture (Intel® VT-x) adds hardware support in the processor to improve the virtualization performance and robustness. Intel VT-x specifications and functional descriptions are included in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B and is available at http://www.intel.com/products/processor/manuals/index.htm
- Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) adds processor implementations to support and improve I/O virtualization performance and robustness. The Intel VT-d spec and other Intel VT documents can be referenced at http://www.intel.com/technology/virtualization/index.htm

2.1.1 Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- Robust: VMMs no longer need to use para-virtualization or binary translation. This means that they will be able to run off-the-shelf OS's and applications without any special steps.
- Enhanced: Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- More reliable: Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- More secure: The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

2.1.2 Intel VT-x Features

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)
  - Hardware assisted page table virtualization
  - Eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor core hardware structures (for example, TLBs)
  - This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

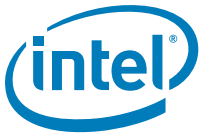
2.1.3 Intel® VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system, or there can be multiple operating system instances running on the same system – offering benefits such as system consolidation, legacy migration, activity partitioning or security.

2.1.3.1 Intel VT-d Features Supported

The processor supports the following Intel VT-d features:

- Root entry, context entry, and default context
- Support for 4-K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
  - Support for fault collapsing based on Requester ID
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
  - Support for non-caching of invalid page table entries



- Support for hardware based flushing of translated but pending writes and pending reads upon IOTLB invalidation.
- Support for page-selective IOTLB invalidation.
- Support for ARI (Alternative Requester ID - a PCI SIG ECR for increasing the function number count in a PCIe device) to support IOV devices.

2.1.3.2 Intel VT-d Intel Xeon E7 v2 Processor Feature Additions

The following are new features supported in Intel VT-d on Intel Xeon E7 v2 processor:

- Improved invalidation architecture
- End point caching support
- Interrupt remapping
- 2M/1G super page support

2.1.4 Intel VT Intel Xeon E7 v2 Processor Extensions

The processor supports the following Intel VT Intel Xeon E7 v2 Processor Extensions features:

- Large Intel VT-d Pages
  - — Adds 2 MB and 1 GB page sizes to Intel VT-d implementations
  - — Matches current support for Extended Page Tables (EPT)
  - — Ability to share CPU's EPT page-table (with super-pages) with Intel VT-d
  - — Benefits:
    - Less memory foot-print for I/O page-tables when using super-pages
    - Potential for improved performance - Due to shorter page-walks, allows hardware optimization for IOTLB
- Transition latency reductions expected to improve virtualization performance without the need for VMM enabling. This reduces the VMM overheads further and increase virtualization performance.

2.2 Security Technologies

2.2.1 Intel® Trusted Execution Technology (Intel® TXT)

Intel TXT defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

For more information on Intel Trusted Execution Technology, see http://www.intel.com/technology/security/

2.2.2 Intel® Trusted Execution Technology – Server Extensions

- Software binary compatible with Intel® Trusted Execution Technology for Servers
- Provides measurement of runtime firmware, including SMM
- Enables run-time firmware in trusted session: BIOS and SSP
- Covers support for existing and expected future Server RAS features
- Only requires portions of BIOS to be trusted, for example, Option ROMs need not be trusted
- Supports S3 State without teardown: Since BIOS is part of the trust chain

For more information on Intel TXT Server Extensions, refer to the *Intel® Trusted Execution Technology (Intel® TXT) Server Extensions - BIOS Specification.*

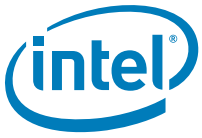
2.2.3 Intel® AES New Instructions (Intel® AES-NI)

These instructions enable fast and secure data encryption and decryption, using the Intel® AES New Instructions (Intel® AES-NI) (Advanced Encryption Standard [AES]) which is defined by FIPS Publication number 197. Since AES is the dominant block cipher, and it is deployed in various protocols, the new instructions will be valuable for a wide range of applications.

The architecture consists of six instructions that offer full hardware support for Intel AES. Four instructions support the Intel AES-NI encryption and decryption, and the other two instructions support the Intel AES-NI key expansion. Together, they offer a significant increase in performance compared to pure software implementations.

The Intel AES-NI have the flexibility to support all three standard Intel AES-NI key lengths, all standard modes of operation, and even some nonstandard or future variants.

Beyond improving performance, the Intel AES-NI instructions provide important security benefits. Since the instructions run in data-independent time and do not use lookup tables, they help in eliminating the major timing and cache-based attacks that threaten table-based software implementations of Intel AES-NI. In addition, these



instructions make Intel AES-NI simple to implement, with reduced code size. This helps reducing the risk of inadvertent introduction of security flaws, such as difficult-to-detect side channel leaks.

2.2.4 Execute Disable Bit

Intel's Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system.

- Allows the processor to classify areas in memory by where application code can execute and where it cannot.
- When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation.

2.3 Intel® Hyper-Threading Technology

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology), which allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled via the BIOS and requires operating system support.

For more information on Intel Hyper-Threading Technology, see http://www.intel.com/products/ht/threading_more.htm.

2.4 Intel® Turbo Boost Technology

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating frequency if it is operating below power, temperature, and current limits. The result is increased performance in multi-threaded and single threaded workloads. It should be enabled in the BIOS for the processor to operate with maximum performance.

2.4.1 Intel® Turbo Boost Operating Frequency

The processor’s rated frequency assumes that all execution cores are running an application at the thermal design power (TDP). However, under typical operation, not all cores are active. Therefore most applications are consuming less than the TDP at the rated frequency. To take advantage of the available TDP headroom, the active cores can increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:

- The number of cores operating in the C0 state.
- The estimated current consumption.
- The estimated power consumption.
- The temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Boost Technology is only active if the operating system is requesting the P0 state. For more information on P-states and C-states refer to Chapter 3, "Power Management."

2.5 Enhanced Intel SpeedStep® Technology

The processor supports Enhanced Intel SpeedStep Technology as an advanced means of enabling very high performance while also meeting the power-conservation needs of the platform.

Enhanced Intel SpeedStep Technology builds upon that architecture using design strategies that include the following:

- **Separation between Voltage and Frequency Changes**. By stepping voltage up and down in small increments separately from frequency changes, the processor is able to reduce periods of system unavailability (which occur during frequency change). Thus, the system is able to transition between voltage and frequency states more often, providing improved power/performance balance.
- **Clock Partitioning and Recovery**. The bus clock continues running during state transition, even when the core clock and Phase-Locked Loop are stopped, which allows logic to remain active. The core clock is also able to restart more quickly under Enhanced Intel SpeedStep Technology.

For additional information on Enhanced Intel SpeedStep Technology see Section 3.2.1.

2.6 Intel® Advanced Vector Extensions (Intel® AVX)

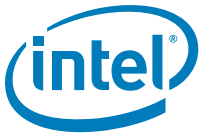
Intel® Advanced Vector Extensions (Intel® AVX) is a new 256-bit vector SIMD extension of Intel Architecture. Intel AVX accelerates the trend of parallel computation in general purpose applications like image, video, and audio processing, engineering applications such as 3D modeling and analysis, scientific simulation, and financial analysts.

Intel AVX is a comprehensive ISA extension of the Intel 64 Architecture. The main elements of Intel AVX are:

- Support for wider vector data (up to 256-bit) for floating-point computation.
- Efficient instruction encoding scheme that supports 3 operand syntax and headroom for future extensions.
- Flexibility in programming environment, ranging from branch handling to relaxed memory alignment requirements.
- New data manipulation and arithmetic compute primitives, including broadcast, permute, fused-multiply-add, and so forth.

The key advantages of Intel AVX are:

- **Performance** - Intel AVX can accelerate application performance via data parallelism and scalable hardware infrastructure across existing and new application domains:
  - 256-bit vector data sets can be processed up to twice the throughput of 128-bit data sets.
  - Application performance can scale up with number of hardware threads and number of cores.
  - Application domain can scale out with advanced platform interconnect fabrics, such as Intel QPI.



- **Power Efficiency** - Intel AVX is extremely power efficient. Combined with the high performance that it can deliver, applications that lend themselves heavily to using Intel AVX can be much more energy efficient and realize a higher performance-per-watt.
- **Extensibility** - Intel AVX has built-in extensibility for the future vector extensions:
  - OS context management for vector-widths beyond 256 bits is streamlined.
  - Efficient instruction encoding allows unlimited functional enhancements:
    - Vector width support beyond 256 bits
    - 256-bit Vector Integer processing
    - Additional computational and/or data manipulation primitives.
- **Compatibility** - Intel AVX is backward compatible with previous ISA extensions including Intel SSE4:
  - Existing Intel® SSE applications/library can:
    - Run unmodified and benefit from processor enhancements
    - Recompile existing Intel® SSE intrinsic using compilers that generate Intel AVX code
    - Inter-operate with library ported to Intel AVX
  - Applications compiled with Intel AVX can inter-operate with existing Intel SSE libraries.

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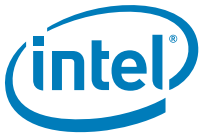


3 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- System States
- Processor Core/Package States
- Integrated Memory Controller (IMC) and System Memory States
- Direct Media Interface Gen 2 (DMI2)/PCI Express Link States
- Intel QuickPath Interconnect States

3.1 ACPI States Supported

The ACPI states supported by the processor are described in this section.

3.1.1 System States

Table 3-1. System States

State	Description
G0/S0	Full On
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

3.1.2 Processor Package and Core States

Table 3-2 lists the package C-state support as:

- The shallowest core C-state that allows entry into the package C-state
- The additional factors that will restrict the state from going any deeper
- The actions taken with respect to the Core, PLL and LLC

Table 3-2. Package C-State Support (Sheet 1 of 2)

Package C-State	Core States	Limiting Factors	Retention and PLL-Off	LLC Fully Flushed	Notes[1]
PC0 - Active	CC0	N/A	No	No	2
PC2 - Snoopable Idle	CC3-CC6	• PCIe/PCH and Remote Socket Snoops • PCIe/PCH and Remote Socket Accesses • Interrupt response time requirement • DMI • Sidebands • Configuration Constraints	VccMin Freq = MinFreq PLL = ON	No	2

Table 3-2. Package C-State Support (Sheet 2 of 2)

Package C-State	Core States	Limiting Factors	Retention and PLL-Off	LLC Fully Flushed	Notes[1]
PC3 - Light Retention	CC3-CC6	• Core C-state • Snoop Response Time • Interrupt Response Time • Non Snoop Response Time	Vcc = retention PLL = OFF	No	2,3,4
PC6 - Deeper Retention	CC6	• LLC ways open • Snoop Response Time • Non Snoop Response Time • Interrupt Response Time	Vcc = retention PLL = OFF	No	2,3,4

Notes:
1. C2 is a transition state only.
2. All package states exit back into the LFM point upon execution resume
3. The mapping of actions for PC3, and PC6 are suggestions - microcode will dynamically determine which actions should be taken based on the desired exit latency parameters.
4. CC3/CC6 will all use a voltage below the VccMin operational point; The exact voltage selected will be a function of the snoop and interrupt response time requirements made by the devices (PCIe* and DMI) and the operating system.

Table 3-3. Core C-State Support

Core C-State	Global Clock	PLL	L1/L2 Cache	Core VCC	Context
CC0	Running	On	Coherent	Active	Maintained
CC1	Stopped	On	Coherent	Active	Maintained
C1E	Stopped	On	Coherent	Request LFM	Maintained
CC3	Stopped	On	Flushed to LLC	Request Retention	Maintained
CC6	Stopped	Off	Flushed to LLC	Power Gate	Flushed to LLC

3.1.3 Integrated Memory Controller States

Table 3-4. System Memory Power States (Sheet 1 of 2)

State	Description
Power Up/Normal Operation	CKE asserted. Active Mode, highest power consumption.
CKE Power Down	Opportunistic, per rank control after idle time: • Active Power Down (APD) (default mode) — CKE de-asserted. Power savings in this mode, relative to active idle state is about 55% of the memory power. Exiting this mode takes 3 – 5 DCLK cycles. • Pre-charge Power Down Fast Exit (PPDF) — CKE de-asserted. DLL-On. Also known as Fast CKE. Power savings in this mode, relative to active idle state is about 60% of the memory power. Exiting this mode takes 3 – 5 DCLK cycles. • Pre-charge Power Down Slow Exit (PPDS) — CKE de-asserted. DLL-Off. Also known as Slow CKE. Power savings in this mode, relative to active idle state is about 87% of the memory power. Exiting this mode takes 3 – 5 DCLK cycles until the first command is allowed and 16 cycles until first data is allowed. • Register CKE Power Down: — IBT-ON mode: Both CKE's are de-asserted, the Input Buffer Terminators (IBTs) are left "on". — IBT-OFF mode: Both CKE's are de-asserted, the Input Buffer Terminators (IBTs) are turned "off".

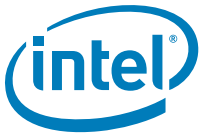


Table 3-4. System Memory Power States (Sheet 2 of 2)

State	Description
Self-Refresh	CKE de-asserted. In this mode, no transactions are executed and the system memory consumes the minimum possible power. Self refresh modes apply to all memory channels for the processor. • IO-MDLL Off: Option that sets the IO master DLL off when self refresh occurs. • PLL Off: Option that sets the PLL off when self refresh occurs. In addition, the register component found on registered DIMMs (RDIMMs) is complemented with the following power down states: — Clock Stopped Power Down with IBT-On — Clock Stopped Power Down with IBT-Off

3.1.4 DMI2/PCI Express Link States

Table 3-5. DMI2/PCI Express Link States

State	Description
L0	Full on – Active transfer state.
L1	Lowest Active State Power Management (ASPM) - Longer exit latency.

Note: L1 is only supported when the DMI2/PCI Express port is operating as a PCI Express port.

3.1.5 Intel QuickPath Interconnect States

Table 3-6. Intel® QPI States

State	Description
L0	Link on. This is the power on active working state.
L0s	A low power state when the link is no traffic flowing over the link
L0p	A lower power state from L0 that reduces the link from full width to half width
L1	A low power state with longer latency and lower power than L0s and is activated in conjunction with package C-states below C0.

3.1.6 G, S, and C State Combinations

Table 3-7. G, S and C State Combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6	Deep Power Down	On	Deep Power Down
G1	S4	Power off		Off, except RTC	Suspend to Disk
G2	S5	Power off		Off, except RTC	Soft Off
G3	N/A	Power off		Power off	Hard off

3.2 Processor Core/Package Power Management

While executing code, Enhanced Intel SpeedStep Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

3.2.1 Enhanced Intel SpeedStep® Technology

The following are the key features of Enhanced Intel SpeedStep® Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on temperature, leakage, power delivery loadline and dynamic capacitance.
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up to an optimized voltage. This voltage is signaled by the SVID Bus to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the SVID Bus.
  - All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested amongst all active cores is selected.
  - Software-requested transitions are accepted at any time. The processor has a new capability from the previous processor generation, it can preempt the previous transition and complete the new request without waiting for this request to complete.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per second are possible.

3.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occurs at the processor core, and processor package level. Thread level C-states are available if Intel HT Technology is enabled. Entry and exit of the C-States at the thread and core level are shown in Figure 3-2.

Figure 3-1. Idle Power Management Breakdown of the Processor Cores

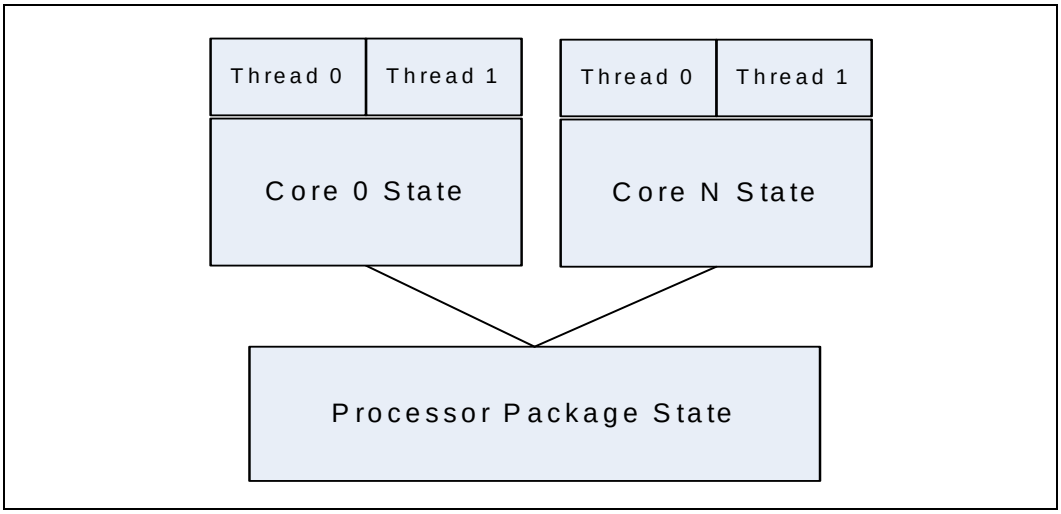
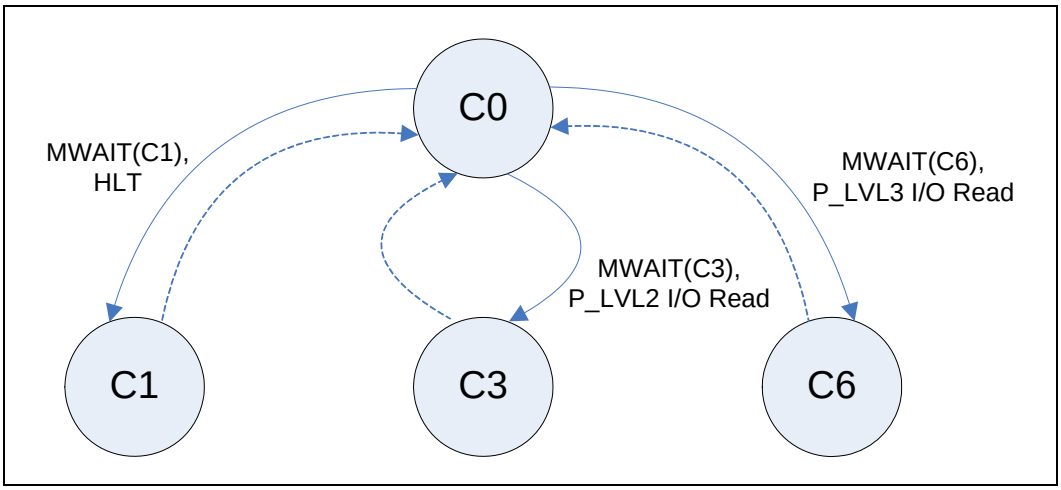


Figure 3-2. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

3.2.3 Requesting Low-Power Idle States

The package C-state will be C1E if all actives cores have also resolved a core C1 state or higher.

The primary software interfaces for requesting low power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions via I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS.

Note: The P_LVLx I/O Monitor address needs to be set up before using the P_LVLx I/O read interface. Each P-LVLx is mapped to the supported MWAIT(Cx) instruction as follows.

Table 3-8. P_LVLx to MWAIT Conversion

P_LVLx	MWAIT(Cx)	Notes
P_LVL2	MWAIT(C3)	The P_LVL2 base address is defined in the PMG_IO_CAPTURE MSR
P_LVL3	MWAIT(C6)	C6. No sub-states allowed.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range does not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT substates cannot be defined. The MWAIT substate is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature which triggers a wakeup on an interrupt even if interrupts are masked by EFLAGS.IF.

3.2.4 Core C-states

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (for example, Thread 0 requests C1 while Thread 1 requests C3, resulting in a core C1 state).
- A core transitions to C0 state when:
  - An interrupt occurs.
  - There is an access to the monitored address if the state was entered via an MWAIT instruction.
- For core C1, and core C3, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- Any interrupt coming into the processor package may wake any core.

3.2.4.1 Core C0 State

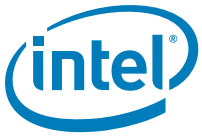
The normal operating state of a core where code is being executed.

3.2.4.2 Core C1 State

C1 is a low power state entered when all threads within a core execute a HLT or MWAIT(C1) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1 state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide* for more information.

While a core is in C1 state, it processes bus snoops and snoops from other threads.



3.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

3.2.4.4 Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM. Once complete, a core will have its voltage reduced to zero volts. In addition to flushing core caches core architecture state is saved to the uncore. Once the core state save is completed, core voltage is reduced to zero. During exit, the core is powered on and its architectural state is restored.

3.2.4.5 Delayed Deep C-States

The Delayed Deep C-states (DDCst) feature on this processor replaces the "C-state auto-demotion" scheme used in the previous processor generation. Deep C-states are defined as CC3 and CC6

The Delayed Deep C-states are intended to allow a staged entry into deeper C-states whereby the processor enters a lighter, short exit-latency C-state (core C1) for a period of time before committing to a long exit-latency deep C-state (core C3 and core C6). This is intended to allow the processor to get past the cluster of short duration idles providing each of those with a very fast wake-up time, but to still get the power benefit of the deep C-states on the longer idles.

3.2.5 Package C-States

The processor supports C0, C1, C3, and C6 power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless otherwise specified:

- A package C-state request is determined by the lowest numerical core C-state amongst all processor partitions.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
  - — Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - — The platform may allow additional power savings to be realized in the processor.
- For package C-states, the processor is not required to enter C0 before entering any other C-state.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - — If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.

  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

The package C-states fall into two categories: independent and coordinated. C0/C1 are independent, while C3/C6 are coordinated across processors.

Package C-states are based on exit latency requirements which are accumulated from the PCIe* devices, PCH, and software sources. The level of power savings that can be achieved is a function of the exit latency requirement from the platform. As a result, there is no fixed relationship between the coordinated C-state of a package, and the power savings that will be obtained from the state. Coordinated package C-states offer a range of power savings which is a function of the guaranteed exit latency requirement from the platform.

There is also a concept of Execution Allowed (EA), when EA status is 0, the cores in a socket are in C3 or a deeper state, a socket initiates a request to enter a coordinated package C-state. The coordination is across all sockets and the PCH.

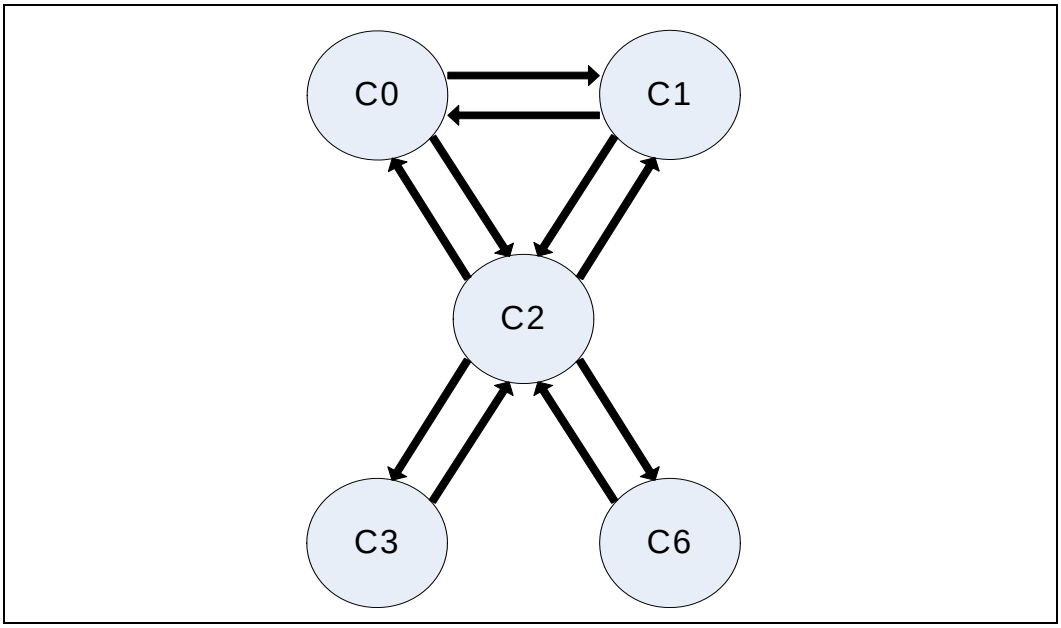
Table 3-9 shows an example of a dual-core processor package C-state resolution. Figure 3-3 summarizes package C-state transitions with package C2 as the interim between PC0 and PC1 prior to PC3 and PC6. Note that this is only an interim state.

Table 3-9. Coordination of Core Power States at the Package Level

Package C-State		Core 1			
		C0	C1	C3	C6
Core 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

1. The package C-state will be C1E if all actives cores have resolved a core C1 state or higher.

Figure 3-3. Package C-State Entry and Exit



3.2.5.1 Package C0 State

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

3.2.5.2 Package C1 State

No additional power reduction actions are taken in the package C1 state. However, if the C1E substate is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage. Autonomous power reduction actions which are based on idle timers, can trigger depending on the activity in the system.

The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

3.2.5.3 Package C2 State

Package C2 state is an intermediate state which represents the point at which the system level coordination is in progress. The package cannot reach this state unless all cores are in at least C3.

3.2.5.4 Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform.

- L3 shared cache retains context and becomes inaccessible in this state.
- Additional power savings actions, as allowed by the exit latency requirements, include putting Intel QPI and PCIe* links in L1, the uncore is not available, further voltage reduction can be taken.

In package C3, the ring will be off and as a result no accesses to the LLC are possible. The content of the LLC is preserved.

3.2.5.5 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.
- L3 shared cache retains context and becomes inaccessible in this state.
- Additional power savings actions, as allowed by the exit latency requirements, include putting Intel SMI Gen2, Intel QPI and PCIe* links in L1, the uncore is not available, further voltage reduction can be taken.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The LLC retains context, but no accesses can be made to the LLC in this state, the cores must break out to the internal state package C2 for snoops to occur.

3.2.6 Package C-State Power Specifications

See Chapter 6, “Electrical Specifications”.

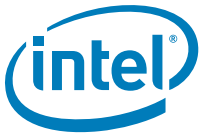
3.3 System Memory Power Management

The DDR3 power states can be summarized as the following:

- Normal operation (highest power consumption).
- CKE Power-Down: Opportunistic, per rank control after idle time. There may be different levels.
  - Active Power-Down.
  - Precharge Power-Down with Fast Exit.
  - Precharge power Down with Slow Exit.
- Self Refresh: In this mode no transaction is executed. The DDR consumes the minimum possible power.

3.3.1 CKE Power-Down

The CKE input land is used to enter and exit different power-down modes. The memory controller has a configurable activity timeout for each rank. Whenever no reads are present to a given rank for the configured interval, the memory controller will transition the rank to power-down mode.



The memory controller transitions the DRAM to power-down by de-asserting CKE and driving a NOP command. The memory controller will tri-state all DDR interface lands except CKE (de-asserted) and ODT while in power-down. The memory controller will transition the DRAM out of power-down state by synchronously asserting CKE and driving a NOP command.

When CKE is off the internal DDR clock is disabled and the DDR power is significantly reduced.

The DDR defines three levels of power-down:

- Active power-down: This mode is entered if there are open pages when CKE is de-asserted. In this mode the open pages are retained. Existing this mode is 3 - 5 DCLK cycles.
- Precharge power-down fast exit: This mode is entered if all banks in DDR are precharged when de-asserting CKE. Existing this mode is 3 - 5 DCLK cycles. Difference from the active power-down mode is that when waking up all page-buffers are empty.
- Precharge power-down slow exit: In this mode the data-in DLL's on DDR are off. Existing this mode is 3 - 5 DCLK cycles until the first command is allowed, but about 16 cycles until first data is allowed.

3.3.2 Self Refresh

The Power Control Unit (PCU) may request the memory controller to place the DRAMs in self refresh state. Self refresh per channel is supported. The BIOS can put the channel in self-refresh if software remaps memory to use a subset of all channels. Also processor channels can enter self refresh autonomously without PCU instruction when the package is in a package C0 state.

3.3.2.1 Self Refresh Entry

Self refresh entrance can be either disabled or triggered by an idle counter. Idle counter always clears with any access to the memory controller and remains clear as long as the memory controller is not drained. As soon as the memory controller is drained, the counter starts counting, and when it reaches the idle-count, the memory controller will place the DRAMs in self refresh state.

Power may be removed from the memory controller core at this point. But V_{VMSE} supply (1.5 V or 1.35 V) to the DDR IO must be maintained.

3.3.2.2 Self Refresh Exit

Self refresh exit can be either a message from an external unit (PCU in most cases, but also possibly from any message-channel master) or as reaction for an incoming transaction.

Here are the proper actions on self refresh exit:

- CK is enabled, and four CK cycles driven.
- When proper skew between Address/Command and CK are established, assert CKE.
- Issue NOPs for tXSRD cycles.
- Issue ZQCL to each rank.
- The global scheduler will be enabled to issue commands.

3.3.2.3 DLL and PLL Shutdown

Self refresh, according to configuration, may be a trigger for master DLL shut-down and PLL shut-down. The master DLL shut-down is issued by the memory controller after the DRAMs have entered self refresh.

The PLL shut-down and wake-up is issued by the PCU. The memory controller gets a signal from PLL indicating that the memory controller can start working again.

3.3.3 DRAM I/O Power Management

Unused signals are tristated to save power. This includes all signals associated with an unused memory channel.

The I/O buffer for an unused signal should be tristated (output driver disabled), the input receiver (differential sense-amp) should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

3.4 DMI2/PCI Express Power Management

Active State Power Management (ASPM) support using L0s and L1 state.

§

4 Thermal Management Specifications

4.1 Package Thermal Specifications

The Intel® Xeon® E7v2 processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system, see section Section 6.7.1, “Storage Conditions Specifications”. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

This section provides data necessary for developing a complete thermal solution. For more information on designing a component level thermal solution, refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide.*

4.1.1 Thermal Specifications

To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile. Thermal solutions not designed to provide sufficient thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide.*

The Intel® Xeon® E7v2 processors implement a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor’s Platform Environment Control Interface (PECI).

If the DTS value is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile, but the DTS value must remain at or below TCONTROL.

For T_{CASE} implementations, if DTS is greater than TCONTROL, then the case temperature must meet the T_{CASE} based Thermal Profiles.

For DTS implementations:

- T_{CASE} thermal profile can be ignored during processor run time.
- If DTS is greater than Tcontrol then follow DTS thermal profile specifications for fan speed optimization.

The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT_N (see Section 6, “Electrical Specifications”). Systems that implement fan speed control must be designed to use this data. Systems that do not alter the fan speed need to guarantee the case temperature meets the thermal profile specifications.

With single thermal profile, it is expected that the Thermal Control Circuit (TCC) would be activated for very brief periods of time when running the most power intensive applications. Utilization of a thermal solution that does not meet the thermal profile will violate the thermal specifications and may result in permanent damage to the processor. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for details on system thermal solution design, thermal profiles and environmental considerations. The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the associated T_{CASE} value.

(x = TDP and y = T_{CASE_MAX} @ TDP) represents a thermal solution design point. In actuality the processor case temperature will not reach this value due to TCC activation.

Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP). The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.

4.1.2 T_{CASE} and DTS Based Thermal Specifications

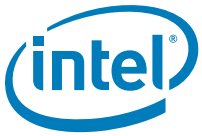
To simplify compliance to thermal specifications at processor run time, the Intel® Xeon® E7v2 processor has added a Digital Thermal Sensor (DTS) based thermal specification. Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature. T_{CASE} thermal based specifications are used for heat sink sizing and DTS based specs are used for acoustic and fan speed optimizations. For the Intel® Xeon® E7v2 processor family, firmware (for example, BMC or other platform management devices) will have DTS based specifications for all SKUs programmed by the customer. SKUs may share T_{CASE} thermal profiles but they will have separate T_{DTS} based thermal profiles.

The processor fan speed control is managed by comparing DTS thermal readings via PECI against the processor-specific fan speed control reference point, or Tcontrol. Both Tcontrol and DTS thermal readings are accessible via the processor PECI client. At a one time readout only, the Fan Speed Control firmware will read the following:

- IA32_TEMPERATURE_TARGET MSR
- Tcontrol via PECI - RdPkgConfig()
- TDP via PECI - RdPkgConfig()
- Core Count - RdPCIConfigLocal()

DTS PECI commands will also support DTS temperature data readings.

Also, refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for details on DTS based thermal solution design considerations.



4.1.3 Intel® Xeon® E7v2 Processor Thermal Profiles

Table 4-1. Intel® Xeon® E7v2 Processor SKU Summary Table

TDP SKUs	Thermal Profile	
	Tcase	DTS
155W	Figure 4-1	Figure 4-2, Figure 4-5, Figure 4-6
130W	Figure 4-7	Figure 4-8
105W	Figure 4-7	Figure 4-8

Note: SKUs are subject to change. Please contact your Intel Field Representative to obtain the latest SKU information.

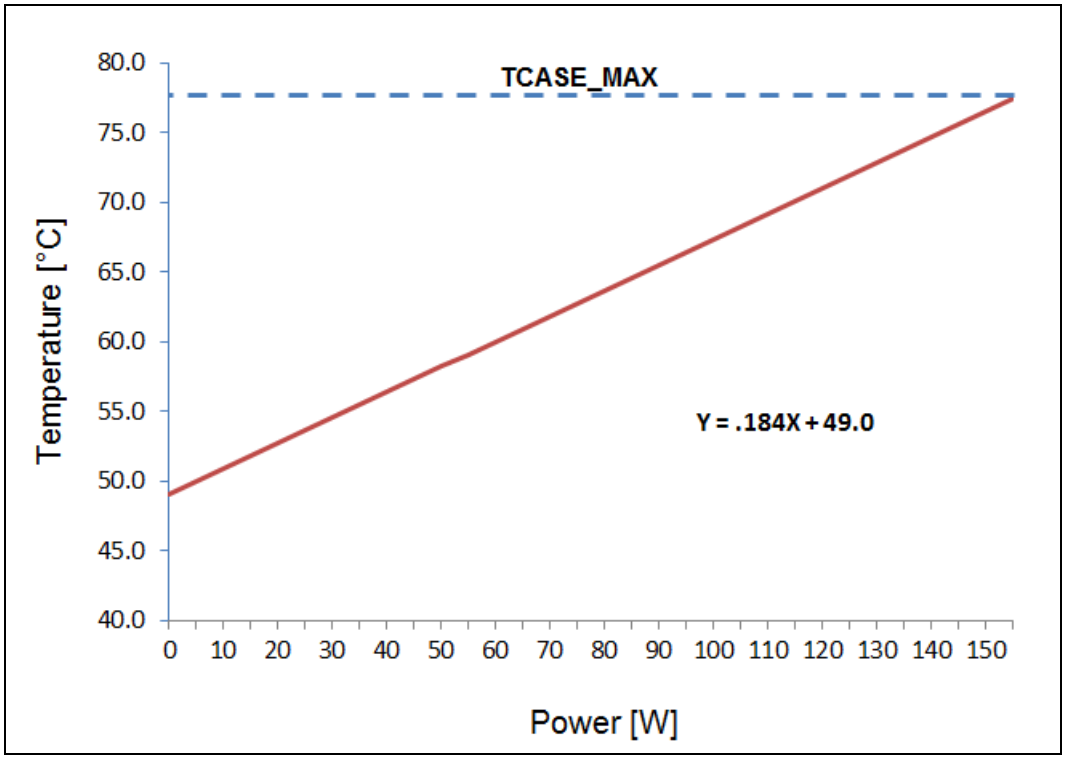
4.1.3.1 155W Thermal Specifications

Table 4-2. Tcase: 155W Thermal Specifications

Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
155	5	See Figure 4-1 and Table 4-5.	1, 2, 3, 4, 5

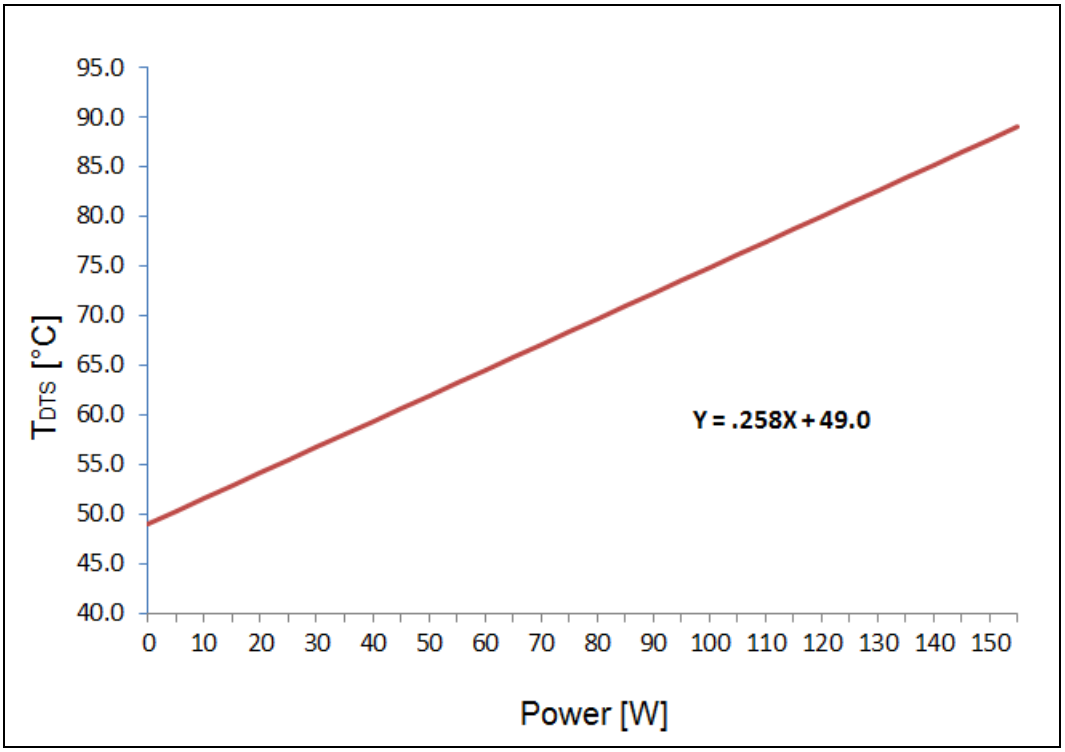
Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified ICC.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.
4. Power specifications are defined at all VIDs. The Intel® Xeon® E7v2 processor may be delivered under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 4-1. Tcase: 155W Thermal Profile



Notes:
1. Please refer to Table 4-5 for discrete points that constitute this thermal profile.
2. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

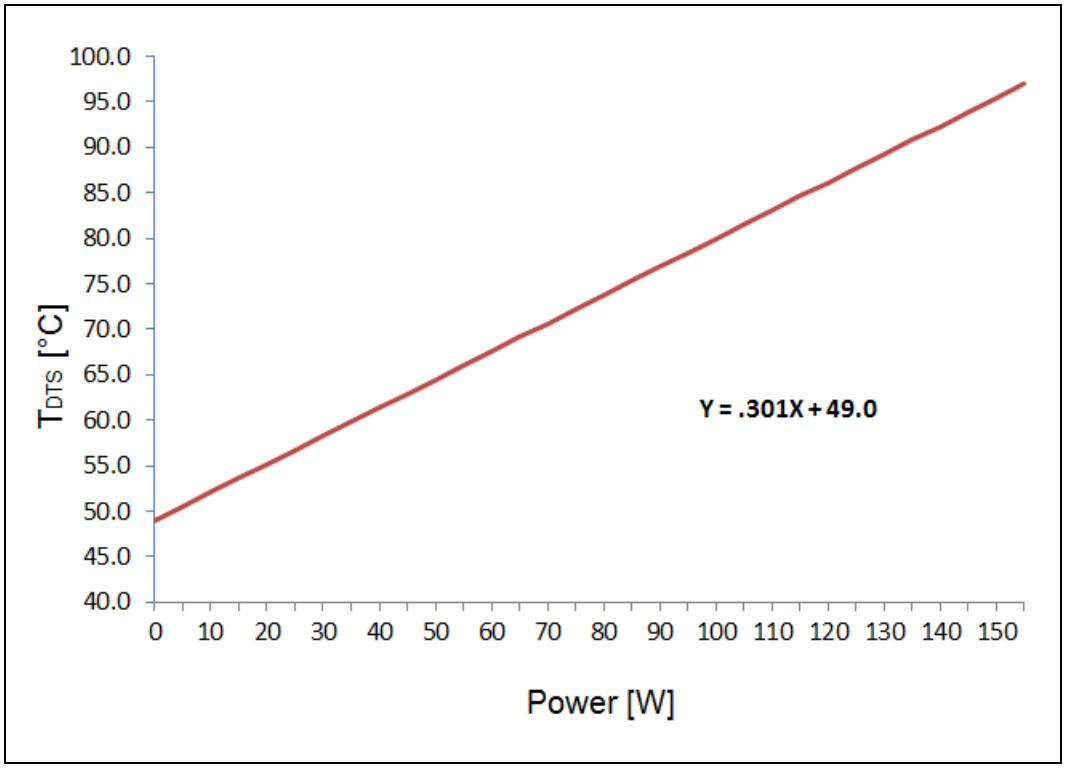
Figure 4-2. DTS: 155W 15 Core Thermal Profile



Notes:

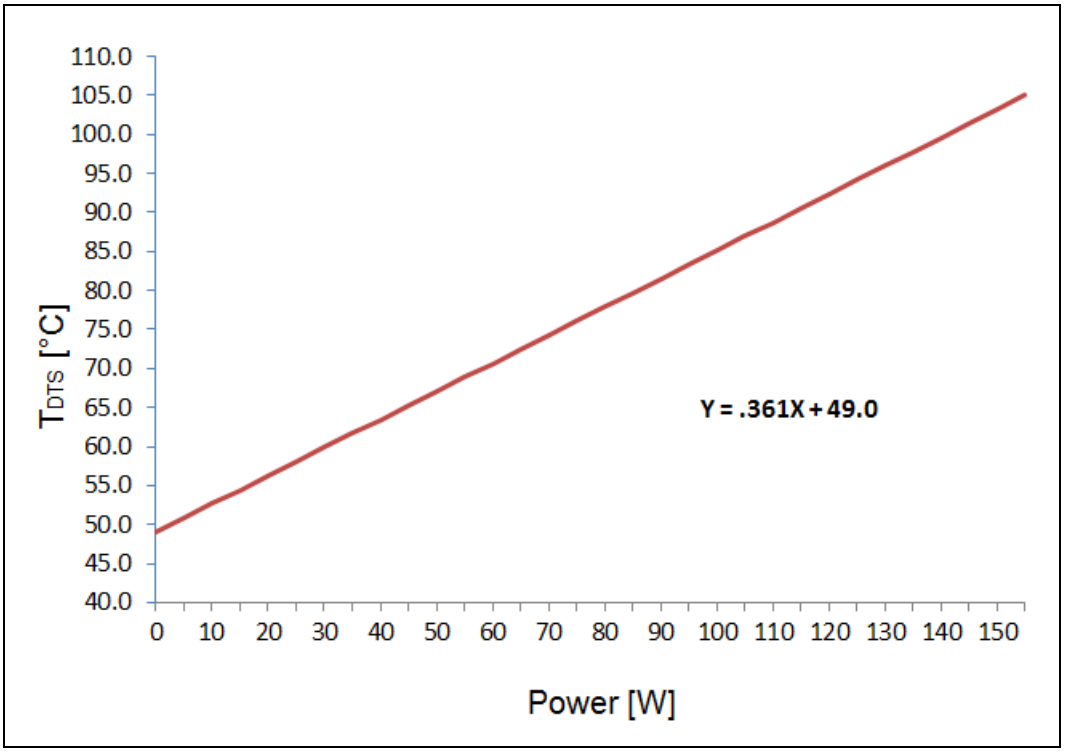
1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-5 for discrete points that constitute the thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Figure 4-3. DTS: 155W 10 Core Thermal Profile



Notes:
1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-5 for discrete points that constitute the thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Figure 4-4. DTS: 155W 6 Core Thermal Profile



Notes:
1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-5 for discrete points that constitute the thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Table 4-3. 155W Thermal Profile Table (Sheet 1 of 2)

Power (W)	Max T_{CASE} (°C)	15 Core Max DTS (°C)	10 Core Max DTS (°C)	6 Core Max DTS (°C)
0	49.0	49.0	49.0	49.0
5	49.9	50.3	50.5	50.8
10	50.8	51.6	52.1	52.6
15	51.8	52.9	53.6	54.4
20	52.7	54.2	55.2	56.2
25	53.6	55.5	56.7	58.0
30	54.5	56.7	58.3	59.8
35	55.4	58.0	59.8	61.6
40	56.4	59.3	61.4	63.5
45	57.3	60.6	62.9	65.3
50	58.2	61.9	64.5	67.1
55	59.1	63.2	66.0	68.9
60	60.0	64.5	67.6	70.7
65	61.0	65.8	69.1	72.5
70	61.9	67.1	70.7	74.3
75	62.8	68.4	72.2	76.1
80	63.7	69.6	73.8	77.9

Table 4-3. 155W Thermal Profile Table (Sheet 2 of 2)

Power (W)	Max T_{CASE} (°C)	15 Core Max DTS (°C)	10 Core Max DTS (°C)	6 Core Max DTS (°C)
85	64.6	70.9	75.3	79.7
90	65.5	72.2	76.9	81.5
95	66.5	73.5	78.4	83.3
100	67.4	74.8	80.0	85.1
105	68.3	76.1	81.5	86.9
110	69.2	77.4	83.1	88.7
115	70.1	78.7	84.6	90.5
120	71.1	80.0	86.2	92.4
125	72.0	81.3	87.7	94.2
130	72.9	82.5	89.3	96.0
135	73.8	83.8	90.8	97.8
140	74.7	85.1	92.4	99.6
145	75.7	86.4	93.9	101.4
150	76.6	87.7	95.5	103.2
155	77.5	89.0	97.0	105.0

4.1.3.2 130W Thermal Specifications

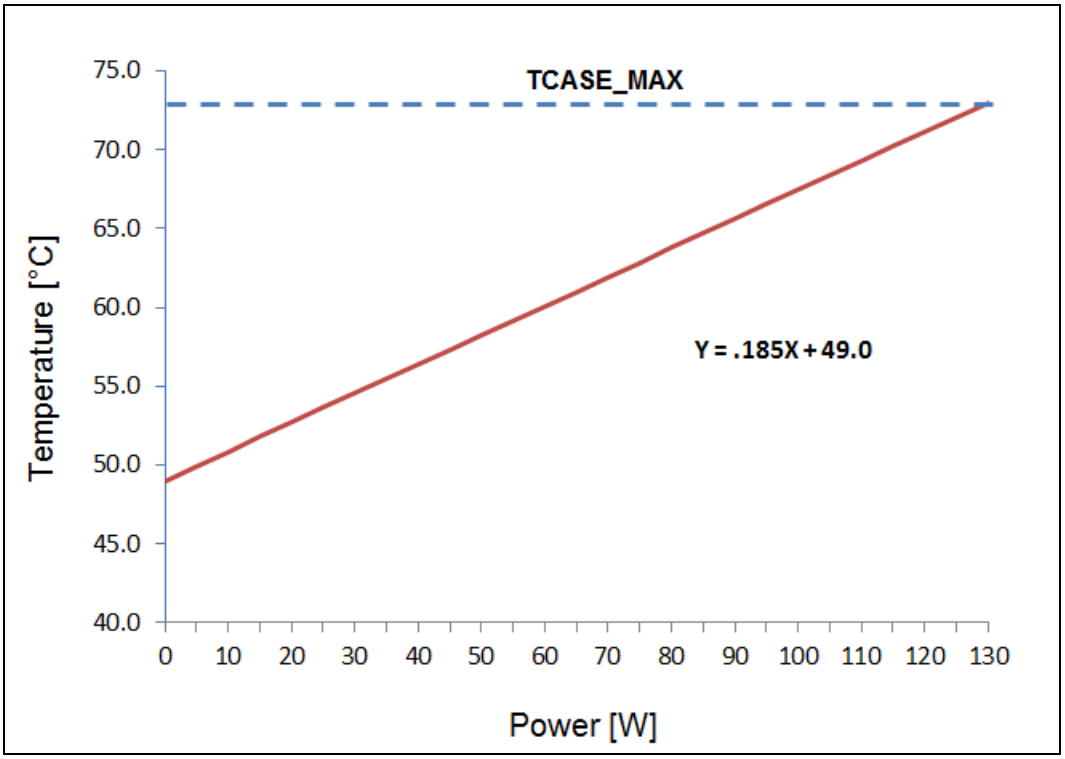
Table 4-4. Tcase: 130W Thermal Specifications

Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
130	5	See Figure 4-5 and Table 4-5.	1, 2, 3, 4, 5

Notes:

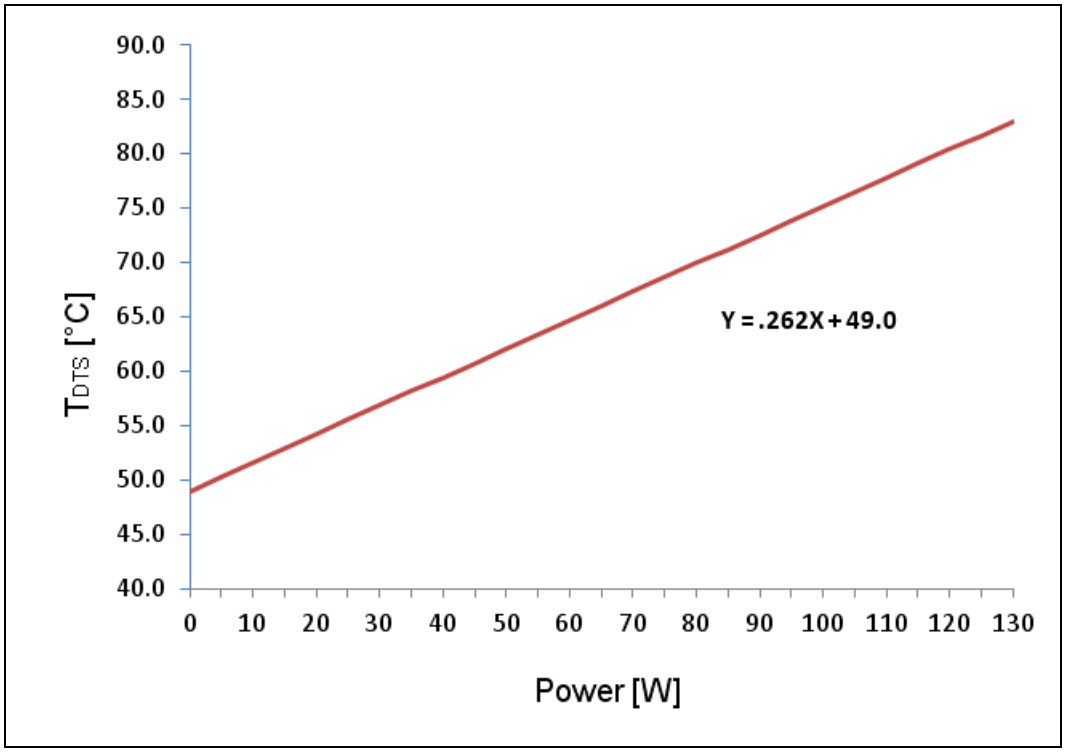
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified ICC.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.
4. Power specifications are defined at all VIDs. The Intel® Xeon® E7v2 processor may be delivered under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 4-5. Tcase: 130W Thermal Profile



Notes:
1. Please refer to Table 4-7 for discrete points that constitute this thermal profile.
2. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Figure 4-6. DTS: 130W 12-15 Core Thermal Profile



Notes:
1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-5 for discrete points that constitute the thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Table 4-5. 130W Thermal Profile Table (Sheet 1 of 2)

Power (W)	Max T_{CASE} (°C)	12-15 Core Max DTS (°C)
0	49.0	49.0
5	49.9	50.3
10	50.8	51.6
15	51.8	52.9
20	52.7	54.2
25	53.6	55.5
30	54.5	56.8
35	55.5	58.2
40	56.4	59.5
45	57.3	60.8
50	58.2	62.1
55	59.2	63.4
60	60.1	64.7
65	61.0	66.0
70	61.9	67.3
75	62.8	68.6
80	63.8	69.9
85	64.7	71.2

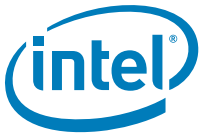


Table 4-5. 130W Thermal Profile Table (Sheet 2 of 2)

Power (W)	Max T_{CASE} (°C)	12-15 Core Max DTS (°C)
90	65.6	72.5
95	66.5	73.8
100	67.5	75.2
105	68.4	76.5
110	69.3	77.8
115	70.2	79.1
120	71.2	80.4
125	72.1	81.7
130	73.0	83

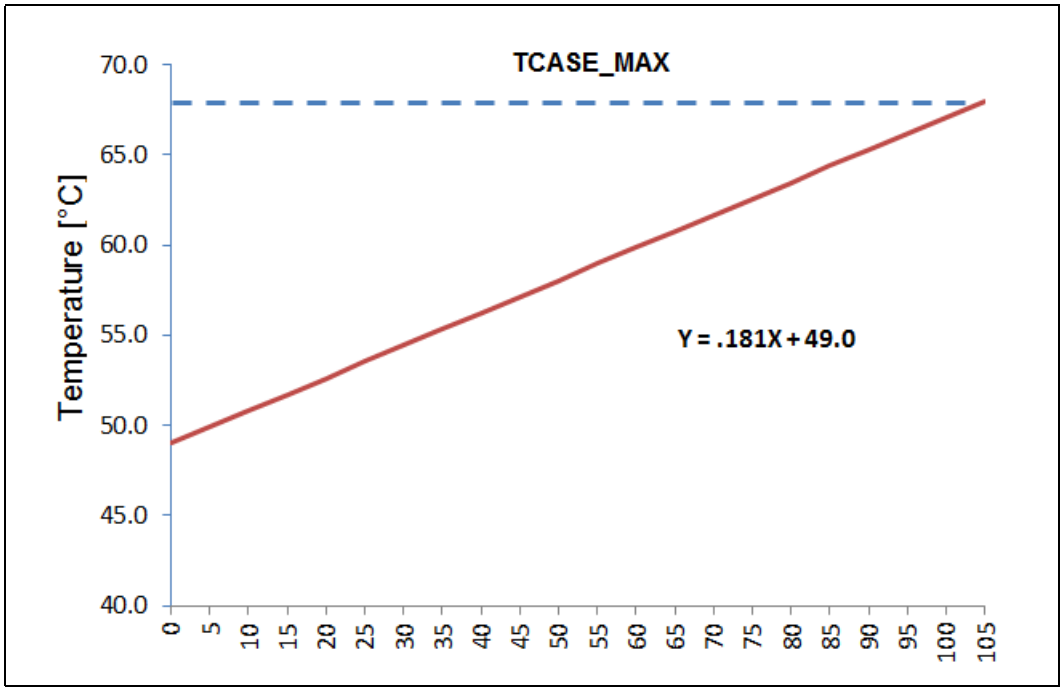
4.1.3.3 105W Thermal Specifications

Table 4-6. Tcase: 105W Thermal Specifications

Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
105	5	See Figure 4-7 and Table 4-7	1, 2, 3, 4, 5

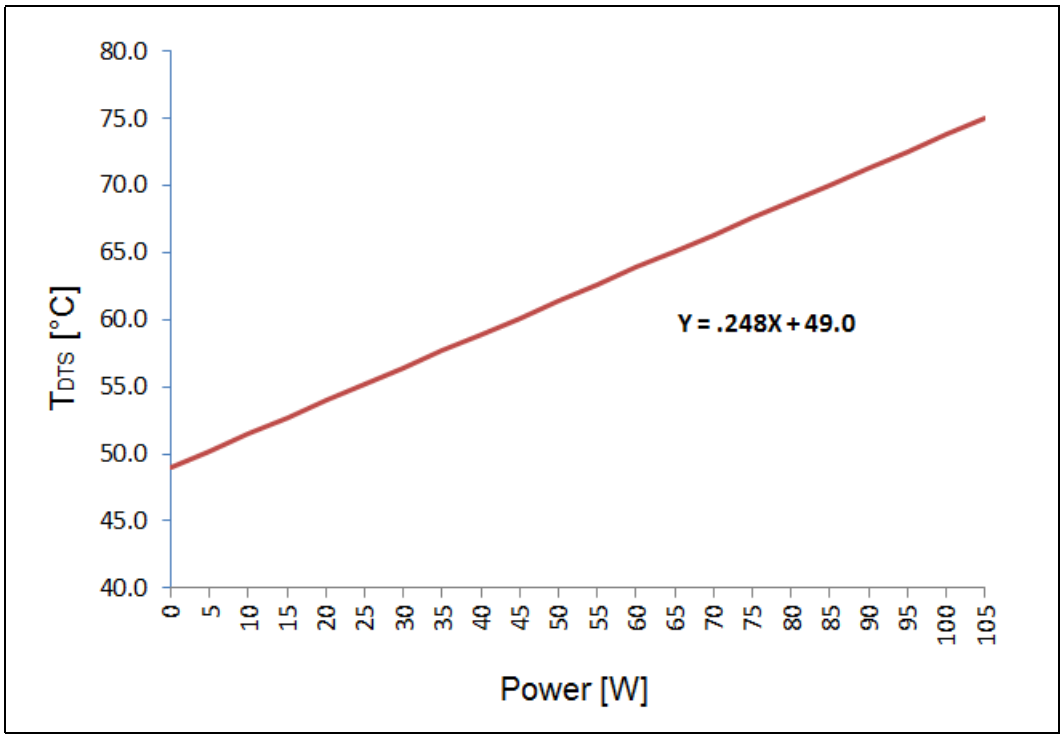
Notes:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified ICC.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
3. These specifications are based on initial pre-silicon simulations, which will be updated as further characterization data becomes available.
4. Power specifications are defined at all VIDs. The Intel® Xeon® E7v2 processor may be delivered under multiple VIDs for each frequency.
5. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 4-7. Tcase: 105W Thermal Profile



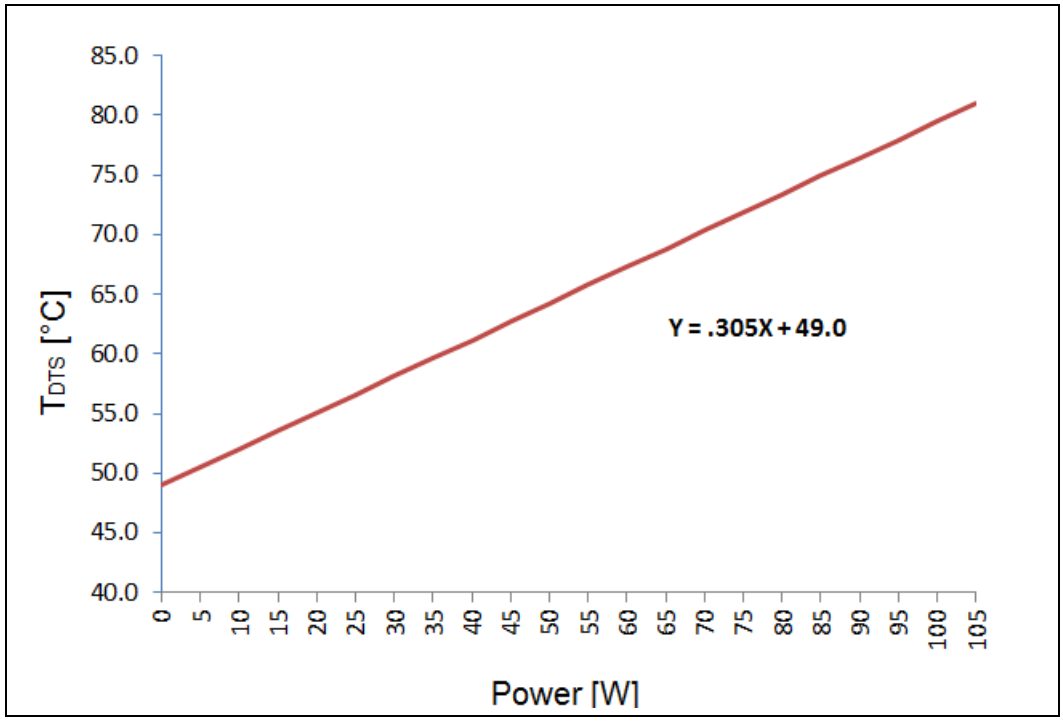
Notes:
1. Please refer to Table 4-7 for discrete points that constitute the thermal profile.
2. Implementation of this Thermal Profile should result in virtually no TCC activation. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Figure 4-8. DTS: 105W 12 - 15 Core Thermal Profile



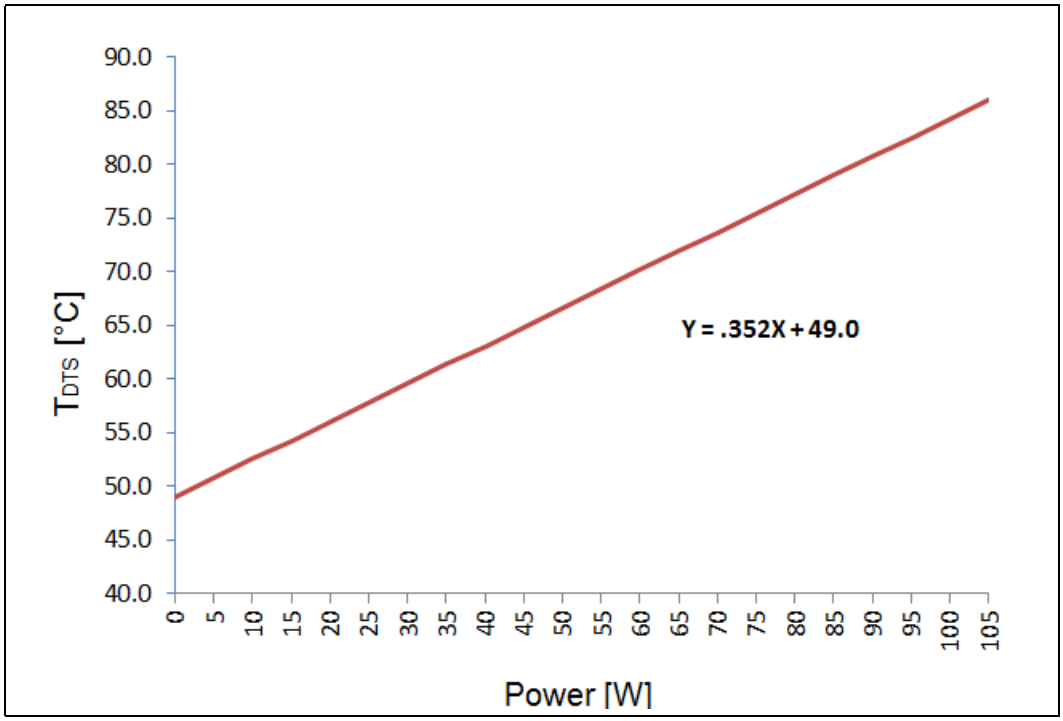
Notes:
1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-7 for discrete points that constitute this thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Figure 4-9. DTS: 105W 8 - 10 Core Thermal Profile



Notes:
1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-7 for discrete points that constitute this thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Figure 4-10. DTS: 105W 6 Core Thermal Profile



Notes:

1. Some processor units may be tested to lower TDP and the IA32_TEMPERATURE_TARGET MSR will be aligned to that lower TDP.
2. Please refer to Table 4-7 for discrete points that constitute this thermal profile.
3. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for system and environmental implementation details.

Table 4-7. 105W Thermal Profile Table (Sheet 1 of 2)

Power (W)	Max T_{CASE} (°C)	Max 12/15 Core DTS (°C)	Max 8/10 Core DTS (°C)	Max 6Core DTS (°C)
0	49.0	49.0	49.0	49.0
5	49.9	50.2	50.5	50.8
10	50.8	51.5	52.0	52.5
15	51.7	52.7	53.6	54.3
20	52.6	54.0	55.1	56.0
25	53.5	55.2	56.6	57.8
30	54.4	56.4	58.1	59.6
35	55.3	57.7	59.7	61.3
40	56.2	58.9	61.2	63.1
45	57.1	60.1	62.7	64.9
50	58.0	61.4	64.2	66.6
55	59.0	62.6	65.8	68.4
60	59.9	63.9	67.3	70.1
65	60.8	65.1	68.8	71.9

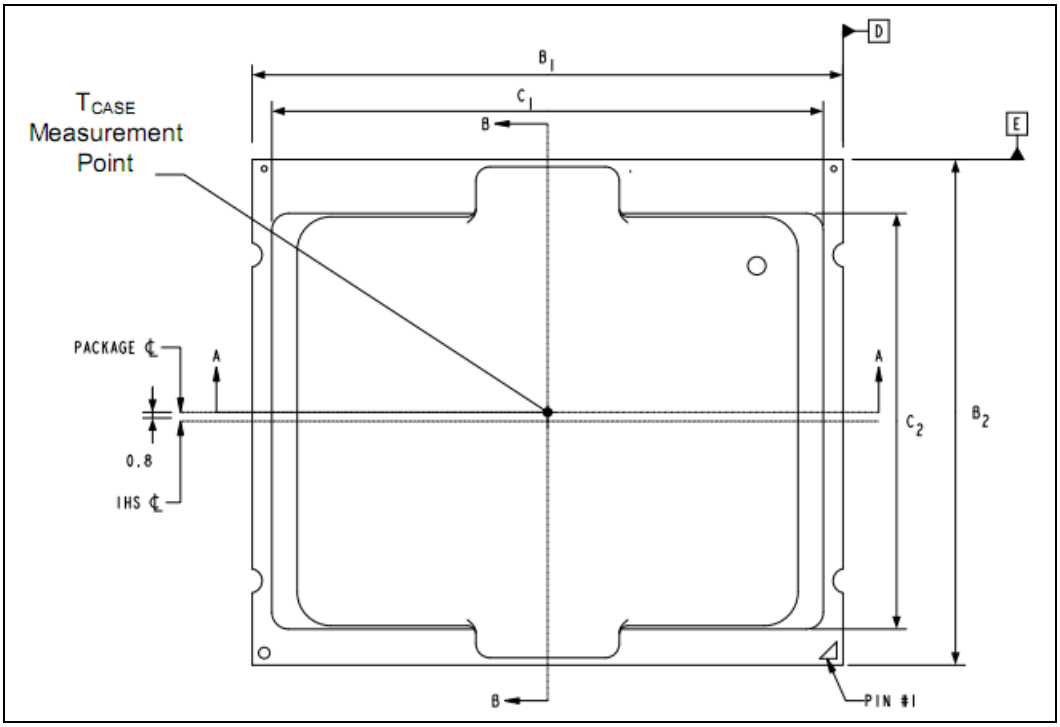
Table 4-7. 105W Thermal Profile Table (Sheet 2 of 2)

Power (W)	Max T_{CASE} (°C)	Max 12/15 Core DTS (°C)	Max 8/10 Core DTS (°C)	Max 6Core DTS (°C)
70	61.7	66.3	70.3	73.7
75	62.6	67.6	71.9	75.4
80	63.5	68.8	73.4	77.2
85	64.4	70.0	74.9	79.0
90	65.3	71.3	76.4	80.7
95	66.2	72.5	78.0	82.5
100	67.1	73.8	79.5	84.2
105	68.0	75.0	81.0	86.0

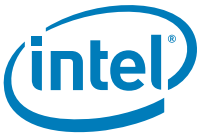
4.1.4 Thermal Metrology

The minimum and maximum case temperatures (T_{CASE}) specified in Table 4-3 through Table 4-7 are measured at the geometric top center of the processor integrated heat spreader (IHS). Figure 4-11 illustrates the location where T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide*.

Figure 4-11. Case Temperature (T_{CASE}) Measurement Location



Notes:
1. Figure is not to scale and is for reference only.
2. See the processor package mechanical drawing for the dimensions of the features.



4.2 Processor Core Thermal Features

4.2.1 Processor Temperature

A new feature in the Intel® Xeon® E7v2 processor is a software readable field in the IA32_TEMPERATURE_TARGET register that contains the minimum temperature at which the TCC will be activated and PROCHOT_N will be asserted. The TCC activation temperature is calibrated on a part-by-part basis and normal factory variation may result in the actual TCC activation temperature being higher than the value listed in the register. TCC activation temperatures may change based on processor stepping, frequency or manufacturing efficiencies.

4.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature provides an enhanced method for controlling the processor temperature when the processor silicon reaches its maximum operating temperature. Adaptive Thermal Monitor uses Thermal Control Circuit (TCC) activation to reduce processor power via a combination of methods. The first method (Frequency/SVID control) involves the processor adjusting its operating frequency (via the core ratio multiplier) and input voltage (via the SVID signals). This combination of reduced frequency and voltage results in a reduction to the processor power consumption. The second method (clock modulation) reduces power consumption by modulating (starting and stopping) the internal processor core clocks. The processor intelligently selects the appropriate TCC method to use on a dynamic basis. BIOS is not required to select a specific method.

The Adaptive Thermal Monitor feature must be enabled for the processor to be operating within specifications. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature which may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Intel® Xeon® Product 2800/4800/8800 v2 Product FamilyIntel® Xeon® Product 2800/4800/8800 v2 Product Family Thermal/Mechanical Design Guide* for information on designing a compliant thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

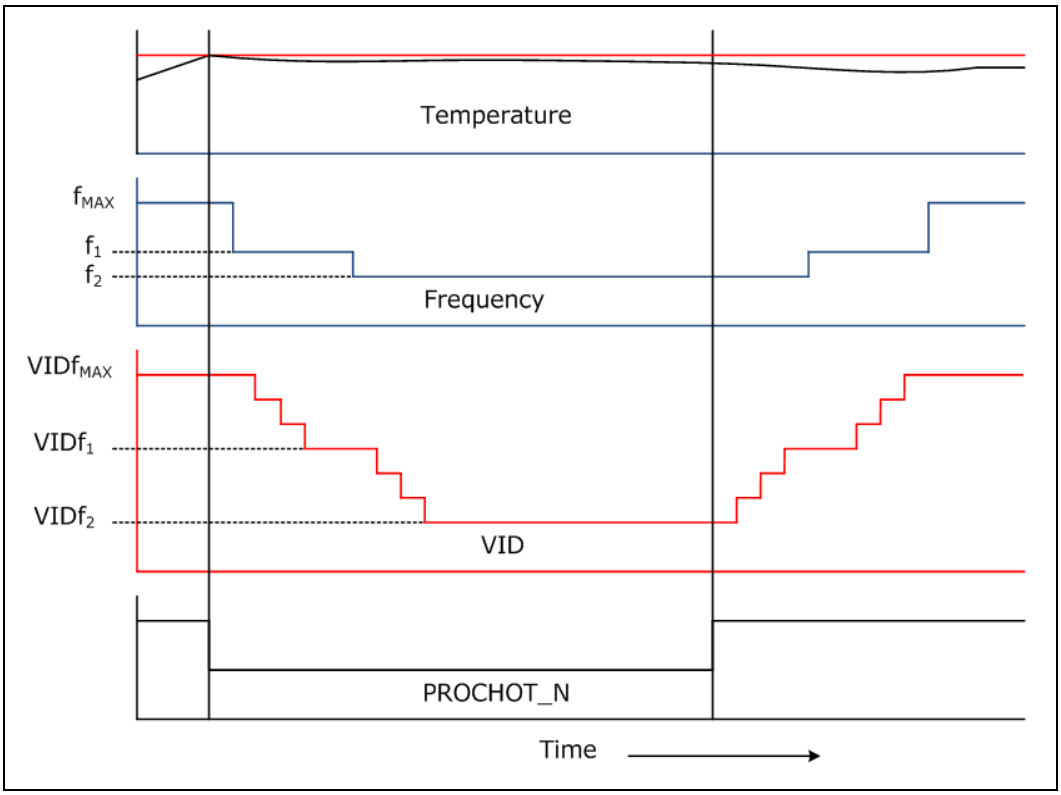
4.2.2.1 Frequency/SVID Control

The processor uses Frequency/SVID control whereby TCC activation causes the processor to adjust its operating frequency (via the core ratio multiplier) and VCC input voltage (via the SVID signals). This combination of reduced frequency and voltage results in a reduction to the processor power consumption.

This method includes multiple operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor. The remaining points consist of both lower operating frequencies and voltages. When the TCC is activated, the processor automatically transitions to the new lower operating frequency. This transition occurs very rapidly (on the order of microseconds). Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new SVID code to the VCC voltage regulator. The voltage regulator must support dynamic SVID steps to support this method. During the voltage change, it will be necessary to transition through multiple SVID codes to reach the target operating voltage. The processor continues to execute instructions during the voltage transition. Operation at the lower voltages reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point via the intermediate SVID/frequency points. Transition of the SVID code will occur first, to insure proper operation once the processor reaches its normal operating frequency. Refer to Figure 4-12 for an illustration of this ordering.

Figure 4-12. Frequency and Voltage Ordering



4.2.2.2 Clock Modulation

Clock modulation is performed by alternately turning the clocks off and on at a duty cycle specific to the processor (factory configured to 37.5% on and 62.5% off for TM1). The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. A small amount of hysteresis has

been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the TCC activation when the Frequency/SVID targets are at their minimum settings. It may also be initiated by software at a configurable duty cycle.

4.2.3 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Adaptive Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems must not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32_CLOCK_MODULATION MSR is set to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:0 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 6.25% on / 93.75% off to 93.75% on / 6.25% off in 6.25% increments. On-Demand mode may be used in conjunction with the Adaptive Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

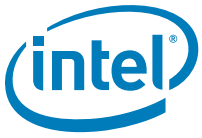
4.2.4 PROCHOT_N Signal

An external signal, PROCHOT_N (processor hot), is asserted when the processor core temperature has reached its maximum operating temperature. If Adaptive Thermal Monitor is enabled (note it must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT_N is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT_N.

The PROCHOT_N signal is bi-directional in that it can either signal when the processor (any core) has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT_N can provide a means for thermal protection of system components.

As an output, PROCHOT_N will go active when the processor temperature monitoring sensor detects that one or more cores has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT_N by the system will activate the TCC, if enabled, for all cores. TCC activation due to PROCHOT_N assertion by the system will result in the processor immediately transitioning to the minimum frequency and corresponding voltage (using Freq/SVID control). Clock modulation is not activated in this case. The TCC will remain active until the system de-asserts PROCHOT_N.

PROCHOT_N can allow voltage regulator (VR) thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on PROCHOT_N as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power.



With a properly designed and characterized thermal solution, it is anticipated that PROCHOT_N will be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT_N in the anticipated ambient environment may cause a noticeable performance loss.

4.2.5 THERMTRIP_N Signal

Regardless of whether Adaptive Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP_N definition in Section 5, “Signal Descriptions”). At this point, the THERMTRIP_N signal will go active and stay active. THERMTRIP_N activation is independent of processor activity and does not generate any Intel® QuickPath Interconnect transactions. If THERMTRIP_N is asserted, all processor supplies must be removed within the timeframe provided in Table 6-28. The temperature at which THERMTRIP_N asserts is not user configurable and is not software visible.

4.2.6 Integrated Memory Controller (IMC) Thermal Features

4.2.6.1 DRAM Throttling Options

The Integrated Memory Controller (IMC) has an independent mechanism that can cause system memory throttling:

- Closed Loop Thermal Throttling (CLTT)

4.2.6.1.1 Closed Loop Thermal Throttling (CLTT)

The processor periodically samples temperatures from the DIMM TSoD devices over a programmable interval. The PCU determines the hottest DIMM rank from TSoD data and informs the integrated memory controller for use in bandwidth throttling decisions.

4.2.6.2 MEM_HOT_C01_N and MEM_HOT_C23_N Signal

The processor includes a pair of new bi-directional memory thermal status signals useful for manageability schemes. Each signal presents and receives thermal status for a pair of memory channels (channels 0 & 1 and channels 2 & 3).

- Input Function: The processor can periodically sense the MEM_HOT_{C01/C23}_N signals to detect if the platform is requesting a memory throttling event. Manageability hardware could drive this signal due to a memory voltage regulator thermal or electrical issue or because of a detected system thermal event (for example, fan is going to fail) other system devices are exceeding their thermal target. The input sense period of these signals are programmable,100 us is the default value. The input sense assertion time recognized by the processor is programmable, 1us is the default value. See Table 6-28, for more timing information. If the sense assertion time is programmed to zero, then the processor ignores all external assertions of MEM_HOT_{C01/C23}_N signals (in effect they become outputs).
- Output Function: The output behavior of the MEM_HOT_{C01/C23}_N signals supports Level mode. In this mode, MEM_HOT_{C01/C23}_N event temperatures are programmable via TEMP_OEM_HI, TEMP_LOW, TEMP_MID, and TEMP_HI threshold settings in the iMC. In Level mode, when asserted, the signal indicates to the platform that a BIOS-configured thermal threshold has been reached by one or more DIMMs in the covered channel pair.

4.2.6.3 Integrated Dual SMBus Master Controllers for System Memory Interface

The processor includes two integrated SMBus master controllers running at 100 KHz for dedicated PCU access to the serial presence detect (SPD) devices and thermal sensors (TSoD) on the DIMMs. Each controller is responsible for a pair of memory channels and supports up to eight SMBus slave devices. Note that clock-low stretching is not supported by the processor. To avoid design complexity and minimize package C-state transitions, the SMBus interface between the processor and DIMMs must be connected. The SMBus controllers for the system memory interface support the following SMBus protocols/commands:

- Random byte Read
- Byte Write
- I^2C* Write to Pointer Register
- I^2C Present Pointer Register Word Read
- I^2C Pointer Write Register Read.

Refer to the *System Management Bus (SMBus) Specification, Revision 2.0* for standing timing protocols and specific command structure details.

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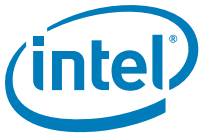


5 Signal Descriptions

This chapter describes the Intel® Xeon® E7v2 processor signals. They are arranged in functional groups according to their associated interface or category.

5.1 System Memory Interface

Table 5-1. Memory Channel Signals

Signal Name	Description
MEM_SCL_C{3:0} MEM_SDA_C{3:0}	SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs.
VMSE{0/1/2/3}_CLK_N VMSE{0/1/2/3}_CLK_P	Clocks to the memory buffer. This clock is used to capture the VCMD# signals.
VMSE{0/1/2/3}_CMD[16:0]	Command signals.
VMSE{0/1/2/3}_DQ[63:0]	Data Bus. DDR3 Data bits.
VMSE{0/1/2/3}_DQS_P[8:0] VMSE{0/1/2/3}_DQS_N[8:0]	Data strobes. Driven with edges in center of data, receive edges are aligned with data edges.
VMSE{0/1/2/3}_ECC[7:0]	Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability
VMSE{0/1/2/3}_ERR_N	Parity Error detected by Registered DIMM (one for each channel).
VMSE_PWR_OK	Power good input signal used to indicate that the power supply is stable for memory channels.

5.2 PCI Express Based Interface Signals

Note: PCI Express Ports 0 and 1 signals are receive and transmit differential pairs.

Table 5-2. PCI Express* Port Signals

Signal Name	Description
PE{1:0}_RX_N[15:0] PE{1:0}_RX_P[15:0]	PCIe Receive Data Input
PE{1:0}_TX_N[15:0] PE{1:0}_TX_P[15:0]	PCIe Receive Data Output

5.3 DMI2/PCI Express Port Signals

Table 5-3. DMI2 to Port 0 Signals

Signal Name	Description
DMI_RX_DN[3:0] DMI_RX_DP[3:0]	DMI2 Receive Data Input
DMI_TX_DP[3:0] DMI_TX_DN[3:0]	DMI2 Transmit Data Output

5.4 Intel QuickPath Interconnect Signals

Table 5-4. Intel QPI Port 0, 1 and 2 Signals

Signal Name	Description
QPI{2:0}_CLKRX_DN/DP	Reference Clock Differential Input. These pins provide the PLL reference clock differential input. 100 MHz typ.
QPI{2:0}_CLKTX_DN/DP	Reference Clock Differential Output. These pins provide the PLL reference clock differential input. 100 MHz typ.
QPI{2:0}_DRX_DN/DP[19:00]	Intel QPI Receive data input.
QPI{2:0}_DTX_DN/DP[19:00]	Intel QPI Transmit data output.

5.5 PECI Signal

Table 5-5. PECI Signals

Signal Name	Description
PECI	PECI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management. Details regarding the PECI electrical specifications, protocols and functions can be found in the Platform Environment Control Interface Specification.

5.6 System Reference Clock Signals

Table 5-6. System Reference Clock (BCLK{0/1}) Signals

Signal Name	Description
BCLK{0/1}_D[N/P]	Reference Clock Differential input. These pins provide the PLL reference clock differential input into the processor. 100 MHz typical BCLK0 is the Intel® QPI reference clock (system clock) and BCLK1 is the PCI Express* reference clock.

5.7 JTAG and TAP Signals

Table 5-7. JTAG and TAP Signals (Sheet 1 of 2)

Signal Name	Description
BPM_N[7:0]	Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
EAR_N	External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die.
PRDY_N	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	Probe Mode Request is used by debug tools to request debug operation of the processor.
TCK	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).

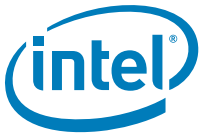


Table 5-7. JTAG and TAP Signals (Sheet 2 of 2)

Signal Name	Description
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRST_N	TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on Reset.

5.8 Serial VID Interface (SVID) Signals

Table 5-8. SVID Signals

SVIDALERT_N	Serial VID alert.
SVIDCLK	Serial VID clock.
SVIDDATA	Serial VID data out.
SVID_IDLE_N	Output pin used to indicate when the SVID bus is IDLE. When asserted true (low), it will assert for two SVID clock cycles. It guarantees that the SVID bus will remain idle for two SVID clocks after it deasserts.

5.9 PIROM Signals

Table 5-9. PIROM Signals

PIROM_ADDR[2:0]	Address for PIROM (Processor Information ROM/OEM scratchpad).
SM_WP	WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to VCCSTBY33.
SMBCLK	The SMBus Clock (SMBCLK) signal is an input clock which is required for operation of PIROM. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor.
SMBDAT	The SMBus Data (SMBDAT) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices.

5.10 Processor Asynchronous Sideband and Miscellaneous Signals

Table 5-10. Processor Asynchronous Sideband Signals (Sheet 1 of 2)

Signal Name	Description
CAT_ERR_N	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CAT_ERR_N for nonrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CAT_ERR_N for all processors. Since this is an I/O land, external agents are allowed to assert this land which will cause the processor to take a machine check exception. On Intel® Xeon® E7v2 processors, CAT_ERR_N is used for signaling the following types of errors: — Legacy MCERR's, CAT_ERR_N is asserted for 16 BCLKs, and samples it for 28 BCLKs to determine if it is driven by an external agent indicating a fatal or uncorrected error. — Legacy IERR's, CAT_ERR_N remains asserted until warm or cold reset.
ERROR_N[2:0]	Error status signals for integrated I/O (IIO) unit: • 0 = Hardware correctable error (no operating system or firmware action necessary) • 1 = Non-fatal error (operating system or firmware action required to contain and recover) • 2 = Fatal error (system reset likely required to recover)
MEM_HOT_C01_N MEM_HOT_C23_N	Memory throttle control. MEM_HOT_C01_N and MEM_HOT_C23_N signals have two modes of operation – input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor and has two modes - level mode and duty cycle mode. In level mode, the output indicates that a particular branch of memory subsystem is hot. In duty cycle mode, the output indicates the hottest DIMM's temperature by altering the percentage of assertion (duty cycle). MEM_HOT_C01_N is used for memory channels 0 & 1 while MEM_HOT_C23_N is used for memory channels 2 & 3.
PMSYNC	Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor. Sourced from VTT.
PROCHOT_N	PROCHOT_N will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. If PROCHOT_N is asserted at the deassertion of RESET_N, the processor will tristate its outputs.
PWRGOOD	Power good input signal used to indicate that the VCC power supply is stable. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET_N	Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. Note some PLL, Intel QuickPath Interconnect and error states are not effected by reset and only PWRGOOD forces them to a known state.
SAFE_MODE_BOOT	

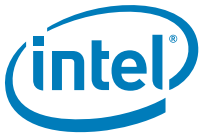


Table 5-10. Processor Asynchronous Sideband Signals (Sheet 2 of 2)

Signal Name	Description
THERMTRIP_N	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures via the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (VCC), VTTA, VTTQ, VSA, VCCPLL, VVMSE supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS.
TSC_SYNC	Time stamp counter sync. Used to help align the time stamp counters of a newly onlined socket to the time stamp counters of existing sockets.

Table 5-11. Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description
BIST_ENABLE	Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die. This strap is latched during all reset modes.
BMCINIT	Indicates whether Service Processor Boot Mode should be used. Used in conjunction with FRMAGENT and SOCKET_ID inputs. • 0: No Service Processor boot. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it), Intel QPI Link Boot (for processors one hop away from the FW agent), or Intel QPI Link Init (for processors more than one hop away from the firmware agent). • 1: Service Processor boot. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a “GO” handshake signal via a firmware scratchpad register. Needs 240 Ohm pull up/pull down (see boot mode).
DEBUG_EN_N	This pin is used to enable certain features used by ITP (for example, probemode). This pin should be connected to the ITP XDP_PRESENT_N# signal as a security measure to validate user had physical access to the target platform. Next generation CPU only. Needs 240 Ohm pull up.
EX_LEGACY_SKT	BMCINIT, FRMAGENT, LEGACY_SKT together determine the boot mode (SSP, Intel QPI Link boot modes, DCF boot), whether local or remote, whether the boot PCH is attached, whether the socket is legacy and whether port0 is DMI or PCIe (Gen1/2. With one exception, this input configuration strap indicates to the processor that it is the legacy socket. The legacy SKT must be strapped for NODE ID 0, via the SKIT-ID pins. There is only 1 legacy SKT in a partition.
FRMAGENT	This input configuration strap indicates to the processor that it is a bootable firmware agent, that is, that the firmware flash ROM is located behind the local PCH attached to the processor via the DMI2 interface.This signal is pulled down on the die, refer to Table 6-6 for details. Needs 240 Ohm pull up/pull down (see boot mode).
MSMI_N	Next generation CPUs only.
PROC_ID[1:0]	These outputs can be used by the platform to determine if the installed processor is an Intel® Xeon® E7v2 processor or a future processor planned for the platform. In the order of PROC_ID1, PROC_ID0, 00 refers to a Intel® Xeon® E7v2 processor. There is no connection to the processor silicon for this signal.
NMI	Interrupt input. Active high.
PM_FAST_WAKE_N	Next generation processors only
PWR_DEBUG_N	This is a debug signal for power debug using ITP on next generation processors.

Table 5-11. Miscellaneous Signals (Sheet 2 of 2)

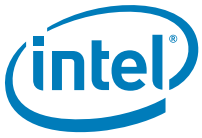
Signal Name	Description
RSVD	RESERVED. All signals that are RSVD must be left unconnected on the board.
SKTOCC_N	SKTOCC_N (Socket occupied) will be pulled to ground in the processor package to indicate that the processor is present. There is no connection to the processor silicon for this signal. 4.7kW pull-up to 3.3V
SOCKET_ID[2:0]	Socket identification configuration straps for establishing the PECI address, Intel® QPI Node ID, and other settings. Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries.
TEST[13:0]	Test[13:0] must be individually connected to an appropriate power source or ground through a resistor for proper processor operation.
TXT_AGENT	Indicates the Intel® Trusted Execution Technology (Intel® TXT) Agent. This feature is disabled by default via internal pull-down resistor. Strap to VCCIO on the legacy socket only via 240 Ohm resistor to enable the feature.
TXT_PLTEN	Intel® TXT disable. This feature is enabled by default via an internal pull-up resistor. Strap to 0 on all sockets to disable the feature. Use a zero ohm resistor if future flexibility is desirable.

5.11 Processor Power and Ground Supplies

Table 5-12. Power and Ground Signals

Signal Name	Description
VCC	Variable power supply for the processor cores, last level caches (LLC), ring interface, and home agent. It is provided by a VRM/EVRD12.5 compliant regulator for each CPU socket. The valid voltage of this supply is indicated by the processor using the serial voltage ID (SVID) interface.
VCC_SENSE VSS_VCC_SENSE	VCC_SENSE and VSS_VCC_SENSE provide an isolated, low impedance connection to the processor core power and ground. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage (that is, processor voltage) remains within specification.
VCC33	VCC33 supplies 3.3 V to PIROM/OEM Scratch ROM. This supply is required for PIROM usage.
VCCIO_IN	Next generation processor only power supply
VCCPLL	Fixed power supply (1.8 V) for the processor phased lock loop (PLL). Also known as VCCsfr
VTTA and VTTQ	Combined fixed analog and quiet analog supply for VMSE, Power Control Unit (PCU), miscellaneous IO, Direct Media Interface Gen 2 (DMI2) interface, Intel QPI interface and PCI Express* interface at VTT voltage (1.0 V). Also known as VCCio
VTT_SENSE VSS_VTT_SENSE	VTT_SENSE and VSS_VTT_SENSE provide an isolated, low impedance connection to the processor I/O power plane. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage (that is, processor voltage) remains within specification.
VCCPECI	Power supply for PECI. Next generation processors only.
VSA	Variable power supply for the processor system agent units. These include logic (non-I/O) for the integrated I/O controller, the integrated memory controller (iMC), and the Intel QPI agent.
VSA_SENSE VSS_VSA_SENSE	VSA_SENSE and VSS_VSA_SENSE provide an isolated, low impedance connection to the processor system agent (VSA) power plane. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage (that is, processor voltage) remains within specification.
VSS	Processor ground node.
VVMSE01 and VVMSE23	1.35 volt power supply for the processor system memory interface. VVMSE is generic for VVMSE01, VVMSE23. ***Note:*** The processor must be provided VVMSE011 and VVMSE23 for proper operation, even in configurations where no memory is populated.

§



6 Electrical Specifications

6.1 Processor Signaling

Intel® Xeon® E7 v2 processors include 2011 lands, which utilize various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include Intel® Scalable Memory Interface Gen 2 (Intel SMI2) (Reference Clock, Command, Control, and Data), PCI Express*, DMI2, Intel® QuickPath Interconnect, Platform Environmental Control Interface (PECI), System Reference Clock, SMBus, JTAG and Test Access Port (TAP), SVID Interface, Processor Asynchronous Sideband, Miscellaneous, and Power/Other signals. Refer to Table 6-5 for details.

Intel strongly recommends performing analog simulations of all interfaces. Please refer to Section 1.7, “Related Documents” for signal integrity model availability.

6.1.1 System Memory Interface Signal Groups

The system memory interface utilizes Intel SMI2 technology, which consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals, which may utilize various signaling technologies. Please refer to Table 6-5 for further details. Throughout this chapter the system memory interface maybe referred to as Intel SMI2.

6.1.2 PCI Express Signals

The PCI Express Signal Group consists of PCI Express* ports 1 and 2 and PCI Express miscellaneous signals. Please refer to Table 6-5 for further details.

6.1.3 DMI2/PCI Express Signals

The Direct Media Interface Gen 2 (DMI2) sends and receives packets and/or commands to the PCH. The DMI2 is an extension of the standard PCI Express Specification. The DMI2/PCI Express Signals consist of DMI2 receive and transmit input/output signals and a control signal to select DMI2 or PCIe* 2.0 operation for port 0. Please refer to Table 6-5 for further details.

6.1.4 Intel® QuickPath Interconnect (Intel® QPI)

The Intel® Xeon® E7 v2 processor provides two Intel QPI ports for high-speed serial transfer between other processors. Each port consists of two uni-directional links (for transmit and receive). A differential signaling scheme is utilized, which consists of opposite-polarity (DP, DN) signal pairs.

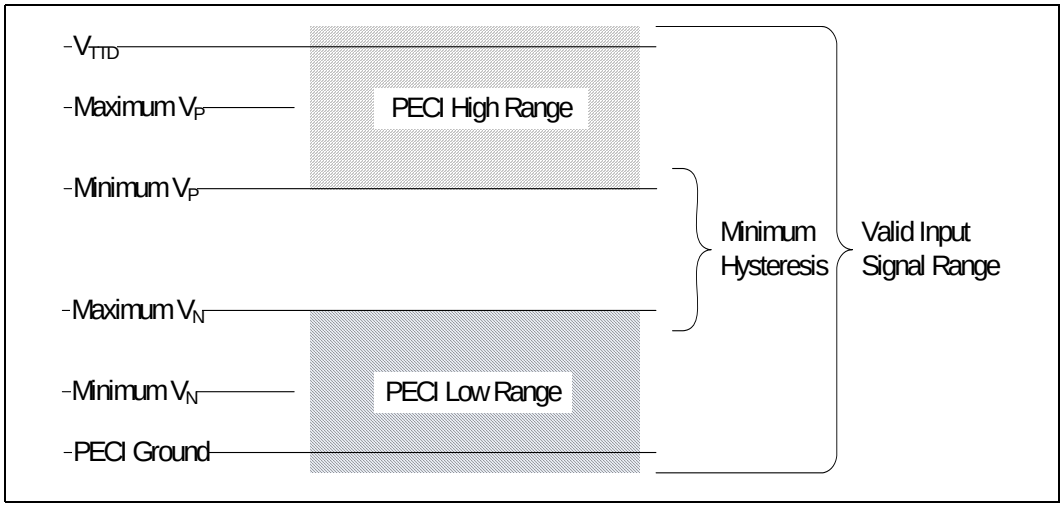
6.1.5 Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external system management logic and thermal monitoring devices. The Intel® Xeon® E7 v2 processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics.

6.1.5.1 Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Please refer to Figure 6-1 and Table 6-20.

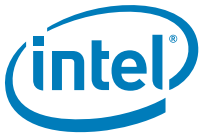
Figure 6-1. Input Device Hysteresis



6.1.6 System Reference Clocks (BCLK{0/1}_DP, BCLK{0/1}_DN)

The processor core, processor uncore, Intel® QuickPath Interconnect link, PCI Express* and VMSE memory interface frequencies) are generated from BCLK{0/1}_DP and BCLK{0/1}_DN signals. There is no direct link between core frequency and Intel QuickPath Interconnect link frequency (for example, no core frequency to Intel QuickPath Interconnect multiplier). The processor maximum core frequency, Intel QuickPath Interconnect link frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software. This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured via the IA32_PERF_CTL MSR (MSR 199h); Bits [15:0].



Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1}_DP, BCLK{0/1}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1}_DP, BCLK{0/1}_DN inputs are provided in Table 6-21 and AC specifications in Table 6-26. These specifications must be met while also meeting the associated signal quality specifications outlined in Section 6.12.

Details regarding BCLK{0/1}_DP, BCLK{0/1}_DN driver specifications are provided in the *CK420BQ Clock Synthesizer/Driver Specification*.

6.1.6.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor.

6.1.7 JTAG and Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

6.1.8 Processor Sideband Signals

Intel® Xeon® E7 v2 processors include asynchronous sideband signals that provide asynchronous input, output or I/O signals between the processor and the platform or Platform Controller Hub. Details can be found in Table 6-5.

All Processor Asynchronous Sideband input signals are required to be asserted/deasserted for a defined number of BCLKs in order for the processor to recognize the proper signal state, these are outlined in Table 6-21 and Table 6-28 (DC and AC specifications). Refer to Section 6.12 for applicable signal integrity specifications.

6.1.9 Power, Ground and Sense Signals

Processors also include various other signals including power/ground and sense points. Details can be found in Table 6-5.

6.1.9.1 Power and Ground Lands

All V_{CC}, V_{CCPLL}, V_{SA}, V_{CC33}, V_{TT}, and V_{VMSE} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane.

For clean on-chip power distribution, processors include lands for all required voltage supplies. These are listed in Table 6-1.

Table 6-1. Power and Ground Lands

Power and Ground Lands	Number of Lands	Comments
V_{CC}	218	Each V_{CC} land must be supplied with the voltage determined by the SVID Bus signals. Table 6-3 Defines the voltage level associated with each core SVID pattern.Table 6-12, Figure 6-2, and Figure 6-4 represent V_{CC} static and transient limits. VCC has a VBOOT setting of 0.0 V.
V_{CC33}	1	V_{CC33} supplies a fixed 3.3 volt stand by voltage to supply PIROM and the OEM scratch ROM.
V_{CCPLL}	3	Each V_{CCPLL} land is connected to a variable 1.80 V supply, power the Phase Lock Loop (PLL) clock generation circuitry. An on-die PLL filter solution is implemented within the Intel® Xeon® E7 v2 processor.
V_{VMSE_01} V_{VMSE_23}	16	Provides power to the processor SMI2 interface with fixed 1.35 V supply.
V_{TT}	43	V_{TT} including lands VTTA, and VTTQ must be supplied by a fixed 1.00 V supply.
V_{SA}	12	Each V_{SA} land must be supplied with the voltage determined by the SVID Bus signals. VSA has a VBOOT setting of 0.9 V.
V_{SS}	726	Ground

6.1.9.2 Decoupling Guidelines

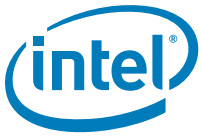
Due to its large number of transistors and high internal clock speeds, the Intel® Xeon® E7 v2 processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (C_{BULK}), help maintain the output voltage during current transients, for example coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 6-12. Failure to do so can result in timing violations or reduced lifetime of the processor.

6.1.9.3 Voltage Identification (VID)

The reference voltage or the VID setting is set via the SVID communication bus between the processor and the voltage regulator controller chip. The VID settings are the nominal voltages to be delivered to the processor's $V_{CC\ and}$ V_{SA} lands when current draw equals zero. Table 6-3 specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The voltage will change due to temperature and/or current load changes in order to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two processor units with the same core frequency may have different default VID settings.

The Intel® Xeon® E7 v2 processor uses voltage identification signals to support automatic selection of $V_{CC\ and}$ V_{SA} power supply voltages. If the processor socket is empty (SKTOCC_N high), or a “not supported” response is received from the SVID bus, then the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a “not supported” acknowledgement.



6.1.9.3.1 SVID Commands

The Intel® Xeon® E7 v2 processor provides the ability to operate while transitioning to a new VID setting and its associated processor voltage rail ($V_{CC\ and}\ V_{SA}$). This is represented by a DC shift. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target voltage. Transitions above the maximum specified VID are not supported. The processor supports the following VR commands:

- SetVID_fast (20 mV/us),
- SetVID_slow (5 mV/us), and
- Slew Rate Decay (downward voltage only and it's a function of the output capacitance's time constant) commands. Table 6-3 and Table 6-26 includes SVID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 6-12.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

6.1.9.3.2 SetVID Fast Command

The SetVID-fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register. Typically 10 to 20 mV/uS depending on platform and the amount of decoupling capacitance.

The SetVID-fast command is preemptive, the VR interrupts its current processes and moves to the new VID. The SetVID-fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit.

6.1.9.3.3 SetVID Slow

The SetVID-slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a "slow" slew rate as defined in the slow slew rate data register. Typically the SetVID_Slow is 4x slower than the SetVID_fast slew rate.

The SetVID-slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-state voltage change. This command is used in the processor for the Intel Enhanced SpeedStep Technology transitions.

6.1.9.3.4 SetVID Decay

The SetVID-Decay command is the slowest of the DVID transitions. It is normally used for VID down transitions. The VR does not control the slew rate, the output voltage declines with the output load current only.

The SetVID- Decay command is preemptive, the VR interrupts its current processes and moves to the new VID. This command is used in the processor for package C6 entry, allowing capacitor discharge by the leakage, thus saving energy.This command is normally used in VID down direction in the processor package C6 entry.

6.1.9.3.5 SVID Power State Functions: SetPS

The processor has three power state functions and these will be set seamlessly via the SVID bus using the SetPS command. Based on the power state command, the SetPS commands sends information to VR controller to configure the VR to improve efficiency, especially at light loads. For example, typical power states are:

- PS(00h): Represents full power or active mode
- PS(01h): Represents a light load 5A to 20A
- PS(02h): Represents a very light load <5A

The VR may change its configuration to meet the processor's power needs with greater efficiency. For example, it may reduce the number of active phases, transition from CCM (Continuous Conduction Mode) to DCM (Discontinuous Conduction Mode) mode, reduce the switching frequency or pulse skip, or change to asynchronous regulation. For example, typical power states are 00h = run in normal mode; a command of 01h= shed phases mode, and an 02h=pulse skip.

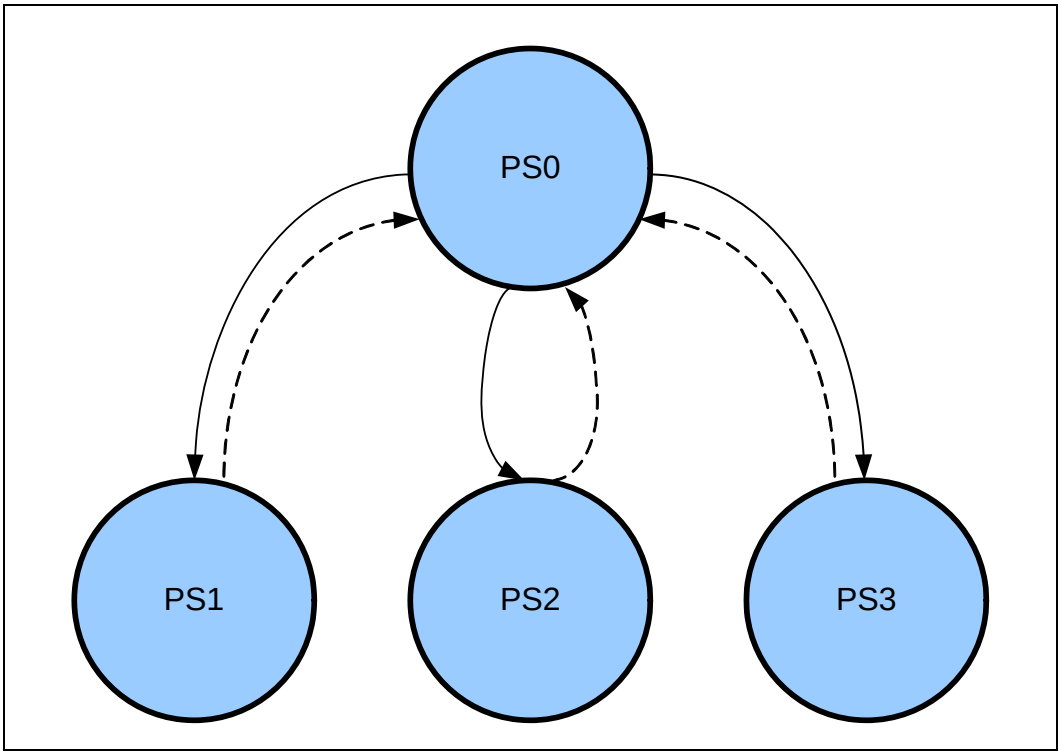
The VR may reduce the number of active phases from PS(00h) to PS(01h) or PS(00h) to PS(02h) for example. There are multiple VR design schemes that can be used to maintain a greater efficiency in these different power states, please work with your VR controller suppliers for optimizations.

The SetPS command sends a byte that is encoded as to what power state the VR should transition to.

If a power state is not supported by the controller, the slave should acknowledge with command rejected (11b).

If the VR is in a low power state and receives a SetVID command moving the VID up then the VR exits the low power state to normal mode (PS0) to move the voltage up as fast as possible. The processor must re-issue low power state (PS1, PS2, or PS3) command if it is in a low current condition at the new higher voltage. See Figure 6-2 for VR power state transitions.

Figure 6-2. VR Power-State Transitions



6.1.9.3.6 SVID Voltage Rail Addressing

The processor addresses 2 different voltage rail control segments within VR12 (VCC and VSA). The SVID data packet contains a 4-bit addressing code:

Table 6-2. SVID Address Usage

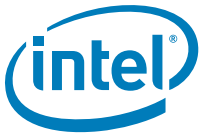
PWM Address (HEX)	Intel® Xeon® E7v2
00	V_{cc}
01	V_{sa}
02	VMSE MC0
03	+1 not used
04	VMSE MC0
05	+1 not used
06	VMSE MC1
07	+1 not used
08	VMSE MC1

Notes:
1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.
4. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.

Table 6-3. VR12.0 Reference Code Voltage Identification (VID)

HEX	VCC, VSA	HEX	VCC, VSA	HEX	VCC, VSA	HEX	VCC, VSA	HEX	VCC, VSA	HEX	VCC, VSA
00	0.00000	55	0.67000	78	0.84500	9B	1.02000	BE	1.19500	E1	1.37000
33	0.50000	56	0.67500	79	0.85000	9C	1.02500	BF	1.20000	E2	1.37500
34	0.50500	57	0.68000	7A	0.85500	9D	1.03000	C0	1.20500	E3	1.38000
35	0.51000	58	0.68500	7B	0.86000	9E	1.03500	C1	1.21000	E4	1.38500
36	0.51500	59	0.69000	7C	0.86500	9F	1.04000	C2	1.21500	E5	1.39000
37	0.52000	5A	0.69500	7D	0.87000	A0	1.04500	C3	1.22000	E6	1.39500
38	0.52500	5B	0.70000	7E	0.87500	A1	1.05000	C4	1.22500	E7	1.40000
39	0.53000	5C	0.70500	7F	0.88000	A2	1.05500	C5	1.23000	E8	1.40500
3A	0.53500	5D	0.71000	80	0.88500	A3	1.06000	C6	1.23500	E9	1.41000
3B	0.54000	5E	0.71500	81	0.89000	A4	1.06500	C7	1.24000	EA	1.41500
3C	0.54500	5F	0.72000	82	0.89500	A5	1.07000	C8	1.24500	EB	1.42000
3D	0.55000	60	0.72500	83	0.90000	A6	1.07500	C9	1.25000	EC	1.42500
3E	0.55500	61	0.73000	84	0.90500	A7	1.08000	CA	1.25500	ED	1.43000
3F	0.56000	62	0.73500	85	0.91000	A8	1.08500	CB	1.26000	EE	1.43500
40	0.56500	63	0.74000	86	0.91500	A9	1.09000	CC	1.26500	EF	1.44000
41	0.57000	64	0.74500	87	0.92000	AA	1.09500	CD	1.27000	F0	1.44500
42	0.57500	65	0.75000	88	0.92500	AB	1.10000	CE	1.27500	F1	1.45000
43	0.58000	66	0.75500	89	0.93000	AC	1.10500	CF	1.28000	F2	1.45500
44	0.58500	67	0.76000	8A	0.93500	AD	1.11000	D0	1.28500	F3	1.46000
45	0.59000	68	0.76500	8B	0.94000	AE	1.11500	D1	1.29000	F4	1.46500
46	0.59500	69	0.77000	8C	0.94500	AF	1.12000	D2	1.29500	F5	1.47000
47	0.60000	6A	0.77500	8D	0.95000	B0	1.12500	D3	1.30000	F6	1.47500
48	0.60500	6B	0.78000	8E	0.95500	B1	1.13000	D4	1.30500	F7	1.48000
49	0.61000	6C	0.78500	8F	0.96000	B2	1.13500	D5	1.31000	F8	1.48500
4A	0.61500	6D	0.79000	90	0.96500	B3	1.14000	D6	1.31500	F9	1.49000
4B	0.62000	6E	0.79500	91	0.97000	B4	1.14500	D7	1.32000	FA	1.49500
4C	0.62500	6F	0.80000	92	0.97500	B5	1.15000	D8	1.32500	FB	1.50000
4D	0.63000	70	0.80500	93	0.98000	B6	1.15500	D9	1.33000	FC	1.50500
4E	0.63500	71	0.81000	94	0.98500	B7	1.16000	DA	1.33500	FD	1.51000
4F	0.64000	72	0.81500	95	0.99000	B8	1.16500	DB	1.34000	FE	1.51500
50	0.64500	73	0.82000	96	0.99500	B9	1.17000	DC	1.34500	FF	1.52000
51	0.65000	74	0.82500	97	1.00000	BA	1.17500	DD	1.35000		
52	0.65500	75	0.83000	98	1.00500	BB	1.18000	DE	1.35500		
53	0.66000	76	0.83500	99	1.01000	BC	1.18500	DF	1.36000		
54	0.66500	77	0.84000	9A	1.01500	BD	1.19000	E0	1.36500		

Notes:
1. 00h = Off State
2. VID Range HEX 01-32 are not used by the Intel® Xeon® E7 v2 processor.
3. For VID Ranges supported see Table 6-12.



6.1.10 Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to power, ground or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 7, "Processor Land Listing" for a land listing of the processor and the location of all Reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace.

6.2 Signal Group Summary

Signals are grouped by buffer type and similar characteristics as listed in Table 6-5. The buffer type indicates which signaling technology and specifications apply to the signals.

Table 6-4. Signal Description Buffer Types

Signal	Description
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Asynchronous[1]	Signal has no timing relationship with any system reference clock.
CMOS	CMOS buffers: 1.05 V or 1.5 V tolerant
SMI2	Scalable Memory Interface Gen 2. These signals are the interface between the Intel® Xeon® E7v2 and the scalable memory buffer. The pin names start with VMSE.
DMI2	Direct Media Interface Gen 2 signals. These signals are compatible with PCI Express 2.0 and 1.0 Signaling Environment AC Specifications.
Intel® QPI	Current-mode 6.4 GT/s and 8.0 GT/s forwarded-clock Intel QuickPath Interconnect signaling
Open Drain CMOS	Open Drain CMOS (ODCMOS) buffers: 1.05V tolerant
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 3.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
Reference	Voltage reference signal.
SSTL	Source Series Terminated Logic (JEDEC SSTL_15)

1. Qualifier for a buffer type.

Table 6-5. Signal Groups (Sheet 1 of 3)

Differential/Single Ended	Buffer Type	Signals[1]
Intel SMI2 Reference Clocks[2]		
Differential	SSTL Output	VMSE{0/1/2/3}_CLK_D[N/P]
Intel SMI2 Command Signals[2]		
Single ended	SSTL Output	VMSE{0/1/2/3}_CMD[16:0]

Table 6-5. Signal Groups (Sheet 2 of 3)

Differential/Single Ended	Buffer Type	Signals[1]
Intel SMI2 Data Signals[2]		
Differential	SSTL Input/Output	VMSE{0/1/2/3}_DQS_D[N/P][8:0]
Single ended	SSTL Input/Output	VMSE{0/1/2/3}_DQ[63:0] VMSE{0/1/2/3}_ECC[7:0]
	SSTL Input	VMSE{0/1/2/3}_ERR_N
Intel SMI2 Miscellaneous Signals[2]		
Single ended	CMOS Input	VMSE_PWR_OK
PCI Express* Port 1, 2, & 3 Signals		
Differential	PCI Express* Input	PE0_RX_[N/P][15:0] PE1_RX_[N/P][15:0]
Differential	PCI Express* Output	PE0_TX_[N/P][15:0] PE1_TX_[N/P][15:0]
DMI2/PCI Express* Signals		
Differential	DMI2 Input	DMI_RX_D[N/P][3:0]
	DMI2 Output	DMI_TX_D[N/P][3:0]
Intel® QuickPath Interconnect (QPI) Signals		
Differential	Intel® QPI Input	QPI{0/1/2}_DRX_D[N/P][19:00] QPI{0/1/2}_CLKRX_D[N/P]
	Intel® QPI Output	QPI{0/1/2}_DTX_D[N/P][19:00] QPI{0/1/2}_CLKTX_D[N/P]
Platform Environmental Control Interface (PECI)		
Single ended	PECI	PECI
System Reference Clock (BCLK{0/1})		
Differential	CMOS1.05v Input	BCLK{0/1}_D[N/P]
SMBus		
Single ended	Open Drain CMOS Input/Output	MEM_SCL_C{3:0} MEM_SDA_C{3:0} VPPSCL VPPSDA
JTAG & TAP Signals		
Single ended	CMOS1.05v Input	TCK, TDI, TMS, TRST_N , EAR_N
	CMOS1.05v Input/Output	PREQ_N
	CMOS1.05v Output	
	Open Drain CMOS Input/Output	BPM_N[7:0]
	Open Drain CMOS Output	TDO, PRDY_N
Serial VID Interface (SVID) Signals		
Single ended	CMOS1.05v Input	SVIDALERT_N
	Open Drain CMOS Input/Output	SVIDDATA
	Open Drain CMOS Output	SVIDCLK

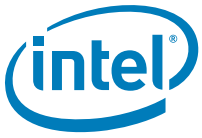


Table 6-5. Signal Groups (Sheet 3 of 3)

Differential / Single Ended	Buffer Type	Signals[1]
Processor Asynchronous Sideband Signals		
Single ended	CMOS1.05v Input	BIST_ENABLE BMCINIT FRMAGENT PWRGOOD PMSYNC RESET_N SOCKET_ID[2:0] TXT_AGENT TXT_PLTEN
	Open Drain CMOS Input/Output	CAT_ERR_N CPU_ONLY_RESET MEM_HOT_C{01/23}_N PROCHOT_N
	Open Drain CMOS Output	ERROR_N[2:0] THERMTRIP_N
Miscellaneous Signals		
N/A	Output	PROC_ID[1:0] SKTOCC_N
Power / Other Signals		
	Power / Ground	V_{CC}, V_{TT}, V_{VMSE_01}, V_{VMSE_23}, V_{CCPLL}, V_{SA}, V_{CC33}, V_{PECI} and V_{SS}
	Sense Points	VCC_SENSE VSS_VCC_SENSE VSS_VTT_SENSE VTT_SENSE VSA_SENSE VSS_VSA_SENSE

1. Refer to Section 5, "Signal Descriptions" for signal description details.

Table 6-6. Signals with On-Die Termination (Sheet 1 of 2)

Signal Name	Pull Up / Pull Down	Rail	Value	Units	Notes
BIST_ENABLE	PD		1k-6k	Ohms	1
BMCINIT	PD		1k-6k	Ohms	1
DEBUG_EN_N	PU	VTT	1k-6k	Ohms	1
EAR_N	PU	VTT	1k-6k	Ohms	2
EX_LEGACY_SKT	PD		1k-6k	Ohms	1
FRMAGENT	PD		1k-6k	Ohms	1
LGSPARE	PU	VTT	1k-6k	Ohms	1
MSMI_N	PU	VTT	1k-6k	Ohms	1
NMI	PD		1k-6k	Ohms	1
PM_FAST_WAKE_N	PU	VTT	1k-6k	Ohms	1
PWR_DEBUG_N	PU	VTT	1k-6k	Ohms	1
SAFE_MODE_BOOT	PD		1k-6k	Ohms	1
SOCKET_ID[2:0]	PD		1k-6k	Ohms	1

Table 6-6. Signals with On-Die Termination (Sheet 2 of 2)

Signal Name	Pull Up /Pull Down	Rail	Value	Units	Notes
SVID_IDLE_N	PU	VTT	1k-6k	Ohms	1
TCK	PD		1k-6k	Ohms	1
TDI	PU	VTT	1k-6k	Ohms	1
TRST_N	PU	VTT	1k-6k	Ohms	1
TMS	PU	VTT	1k-6k	Ohms	1
TXT_AGENT	PD		1k-6k	Ohms	1
TXT_PLTEN	PU	VTT	1K-6K	Ohms	1

Notes:
1. Refer to Table 6-19 for details on the R_{ON} (Buffer on Resistance) value for this signal.

6.3 Power-On Configuration (POC) Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET_N, or upon assertion of PWRGOOD (inactive-to-active transition). For specifics on these options, please refer to Table 6-7.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset transition of the latching signal (RESET_N or PWRGOOD).

Table 6-7. Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
Output tri state	PROCHOT_N	1
Execute BIST (Built-In Self Test)	BIST_ENABLE	2
Enable Service Processor Boot Mode	BMCINIT	3
Enable Intel® Trusted Execution Technology (Intel® TXT) Platform	TXT_PLTEN	3
Power-up Sequence Halt for ITP configuration	EAR_N	3
Enable Bootable Firmware Agent	FRMAGENT	3
Enable Intel Trusted Execution Technology (Intel TXT) Agent	TXT_AGENT	3
Used in conjunction with FRMAGENT	EX_LEGACY_SKT	
Configure Socket ID	SOCKET_ID[1:0]	3

Notes:
1. Output tri-state option enables Fault Resilient Booting (FRB), for FRB details see Section 6.4. The signal used to latch PROCHOT_N for enabling FRB mode is RESET_N.
2. This signal is sampled at cold reset / PWRGOOD-reset and warm reset. This is setup before PWRGOOD asserts and held after reset deasserts.
3. This signal is sampled at cold reset / PWRGOOD-reset. This is setup before powergood asserts and held after reset deasserts.

6.4 Fault Resilient Booting (FRB)

The Intel® Xeon® E7 v2 processor supports both socket and core level Fault Resilient Booting (FRB), which provides the ability to boot the system as long as there is one processor functional in the system. One limitation to socket level FRB is that the system cannot boot if the legacy socket that connects to an active PCH becomes unavailable

since this is the path to the system BIOS. See Table 6-9 for a list of output tri-state FRB signals.

Socket level FRB will tri-state processor outputs via the PROCHOT_N signal. Assertion of the PROCHOT_N signal through RESET_N de-assertion will tri-state processor outputs. Note, that individual core disabling is also supported for those cases where disabling the entire package is not desired.

The Intel® Xeon® E7v2 processor extends the FRB capability to the core granularity by maintaining a register in the uncore so that BIOS or another entity can disable one or more specific processor cores.

Table 6-8. Fault Resilient Booting (Output Tri-State) Signals

Output Tri-State Signal Groups	Signals
Intel QPI	QPI0_CLKTX_DN[1:0] QPI0_CLKTX_DP[1:0] QPI0_DTX_DN[19:00] QPI0_DTX_DP[19:00] QPI1_CLKTX_DN[1:0] QPI1_CLKTX_DP[1:0] QPI1_DTX_DN[19:00] QPI1_DTX_DP[19:00]
SMBus	MEM_SCL_C[3:0] MEM_SDA_C[3:0] VPP_SCL VPP_SDA
JTAG & TAP	TDO
Processor Sideband	CAT_ERR_N CPU_ONLY_RESET ERROR_N[2:0] MEM_HOT_C01_N MEM_HOT_C23_N BPM_N[7:0] PRDY_N THERMTRIP_N PROCHOT_N PECI TSC_SYNC
SVID	SVIDCLK SVID_DATA SVID_IDLE_N

6.5 Mixing Processors

Intel supports and validates two and four processor configurations only in which all processors operate with the same Intel QuickPath Interconnect frequency, core frequency, power segment, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.

Note: Processors within a system must operate at the same frequency per bits [15:8] of the FLEX_RATIO MSR (Address: 194h); however this does not apply to frequency transitions initiated due to thermal events, Extended HALT, Enhanced Intel SpeedStep Technology transitions signal.

Mixing processors of different steppings but the same model (as per CPUID instruction) is supported. Details regarding the CPUID instruction are provided in the *AP-485, Intel® Processor Identification and the CPUID Instruction* application note.

6.6 Flexible Motherboard Guidelines (FMB)

The Flexible Motherboard (FMB) guidelines are estimates of the maximum values the Intel® Xeon® E7 v2 processor will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. Processors may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future Intel® Xeon® E7 v2 processors.

6.7 Absolute Maximum and Minimum Ratings

Table 6-9 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 6-9. Processor Absolute Minimum and Maximum Ratings

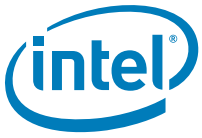
Symbol	Parameter	Min	Typical	Max	Unit
V_{CC}	Processor core voltage with respect to Vss	-0.3		1.4	V
V_{CCPLL}	Processor PLL voltage with respect to Vss	-0.3	1.8	2.0	V
V_{SA}	Processor SA voltage with respect to V_{SS}	-0.3	0.78	1.4	V
V_{VMSE}	Processor VMSE voltage with respect to V_{SS}	-.04	1.35	1.6	V
V_{TT}	Processor analog IO voltage with respect to V_{SS}	-0.3	1.00	1.4	V

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 6.12.5. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.

6.7.1 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes in Table 6-10 for post board attach limits).

Table 6-10 specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum



device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality & reliability may be affected.

Table 6-10. Storage Condition Ratings

Symbol	Parameter	Min	Max	Unit
$T_{absolute\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-25	125	°C
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5	40	°C
$T_{short\ term\ storage}$	The ambient storage temperature (in shipping media) for a short period of time.	-20	85	°C
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24		°C
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with sustained storage conditions Unopened bag, includes 6 months storage time by customer.	0	30	months
$Time_{short\ term\ storage}$	A short period of time (in shipping media).	0	72	hours

Notes:
1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non-operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28C).
5. Device storage temperature qualification methods follow JEDEC High and Low Temperature Storage Life Standards: *JESD22-A119* (low temperature) and *JESD22-A103* (high temperature).

6.8 Power Limit Specifications

The maximum power limits for associated states are listed below.

Table 6-11. Package C-State Power Specifications

TDP SKUs	C0 (Pmax)	C1	C3	C6
155W	270	40	25	18
130W	230	40	25	18
105W	200	40	25	22

Notes:
1. SKU's are subject to change. Please contact your Intel Field Representative to obtain the latest SKU information.
2. C0 is the performance state of the processor, and includes all P-states, including Turbo Boost Technology.

6.9 DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature (T_{CASE} specified in Section 4), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

6.9.1 Voltage and Current Specifications

Table 6-12. Voltage Specification

Symbol	Parameter	Voltage Plane	Min	Typ	Max	Unit	Notes[1]
V_{CC} VID	V_{CC} VID Range		0.6		1.25	V	2, 3
V_{CC}	Core Voltage (Launch - FMB)	V_{CC}	See Table 6-13 and Figure 6-3			V	3, 4, 7, 8, 12, 14, 18
V_{VID_STEP} (Vcc, Vsa)	VID step size during a transition			5.0		mV	10
V_{CCPLL}	PLL Voltage	V_{CCPLL}	1.773	1.8	1.827	V	11, 12, 13, 17
V_{VMSE} (V_{VMSE_01}, V_{VMSE_23})	I/O Voltage for SMI2 (Standard Voltage)	V_{VMSE}	1.303	1.35	1.391	V	11, 13, 14, 16, 17
V_{TT}	Uncore Voltage (Launch - FMB)	V_{TT}	0.959	1.00	1.036	V	3, 5, 9, 12, 13
V_{SA_VID}	Vsa VID Range	V_{SA}	0.6	0.78	1.20	V	2, 3, 14, 15
V_{SA}	System Agent Voltage (Launch - FMB)	V_{SA}	V_{SA} - 0.075	0.78	V_{SA} + 0.078	V	3, 6, 12, 14, 19

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
2. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different settings.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
4. The V_{CC} voltage specification requirements are measured across the remote sense pin pairs (VCC_SENSE and VSS_VCC_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
5. The V_{TT} voltage specification requirements are measured across the remote sense pin pairs (VTT_SENSE and VSS_VTT_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
6. The V_{SA} voltage specification requirements are measured across the remote sense pin pairs (VSA_SENSE and VSS_VSA_SENSE) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
7. The processor should not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
8. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor case temperature (T_{CASE}) shown in Chapter 4, "Thermal Management Specifications". I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 5 seconds. Refer to Figure 6-4 for further details on the average processor current draw over various time durations.
9. The processor should not be subjected to any static V_{TTA}, V_{TTD} level that exceeds the V_{TT_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
10. This specification represents the V_{CC} reduction or V_{CC} increase due to each VID transition, see Section 6.1.9.3, "Voltage Identification (VID)". AC timing requirements for VID transitions are included in Figure 6-20.
11. Baseboard bandwidth is limited to 20 MHz.

12. FMB is the flexible motherboard guidelines. See Section 6.6 for FMB details.
13. DC + AC + Ripple = Total Tolerance
14. For Power State Functions see Section 6.1.9.3.5.
15. V_{SA_VID} does not have a loadline, the output voltage is expected to be the VID value.
16. V_{VMSE} tolerance at processor pins. Tolerance for VR at remote sense is ±2.0%*V_{VMSE}.
17. The V_{CCPLL}, V_{VMSE01}, V_{VMSE23} voltage specification requirements are measured across vias on the platform. Choose V_{CCPLL}, V_{VMSE01}, or V_{VMSE23} vias close to the socket and measure with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1M Ω minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
18. VCC has a Vboot setting of 0.0V and is not included in the PWRGOOD indication.
19. VSA has a Vboot setting of 0.9V. Also, the values shown for typical is simply the center of the distribution. Values will vary significantly.

Table 6-13. Current (I_{CC_MAX} and I_{CC_TDC}) Specification

Symbol	Parameter	Voltage Plane	Current	Unit	Notes[1]
I_{CC_MAX} I_{CCP_MAX} I_{SA_MAX} I_{VMSE_MAX} I_{CC33_MAX} I_{CCPLL_MAX} $I_{CCIO\_IN\_MAX}$	Max. Processor Current: (TDP - 155W) (Launch - FMB)	V_{CC} V_{TT} V_{SA} V_{VMSE} V_{CC33} V_{CCPLL} V_{CCIO_IN}	220 24 18 5 .075 1.5 0.10	A A A A A A A	2, 4,6
	Max. Processor Current: (TDP - 130W) (Launch - FMB)		190 24 18 5 .075 1.5	A A A A A A	2, 4,6
	Max. Processor Current: (TDP - 105W) (Launch - FMB)		165 24 18 5 .075 1.5	A A A A A A	2, 4, 6
I_{CC_TDC} I_{CCP_TDC} I_{SA_TDC} I_{VMSE_TDC} I_{CC33_TDC} I_{CCPLL_TDC}	Thermal Design Current: (TDP - 155W) (Launch - FMB)	V_{CC} V_{TT} V_{SA} V_{VMSE} V_{CC33} V_{CCPLL}	165 20 14 4 .075 1.5	A A A A A A	2, 3, 5
	Thermal Design Current: (TDP - 130W) (Launch - FMB)		140 20 14 4 .075 1.5	A A A A A A	2, 3, 5
	Thermal Design Current: (TDP - 105W) (Launch - FMB)		115 20 14 4 .075 1.5	A A A A A A	2, 3, 5

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
2. FMB is the flexible motherboard guidelines. See Section 6.6 for FMB details.

3. I_{CC_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.
4. Specification is at T_{CASE} = 50 °C. Characterized by design (not tested).
5. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor case temperature (T_{CASE}) shown in Section 4, "Thermal Management Specifications". I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 5 seconds. Refer to Figure 6-4 for further details on the average processor current draw over various time durations.
6. I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 5 seconds. Refer to Figure 6-4 for further details on the average processor current draw over various time durations.

Table 6-14. V_{CC} Static and Transient Tolerance Intel® Xeon® E7 v2 Processor (Sheet 1 of 2)

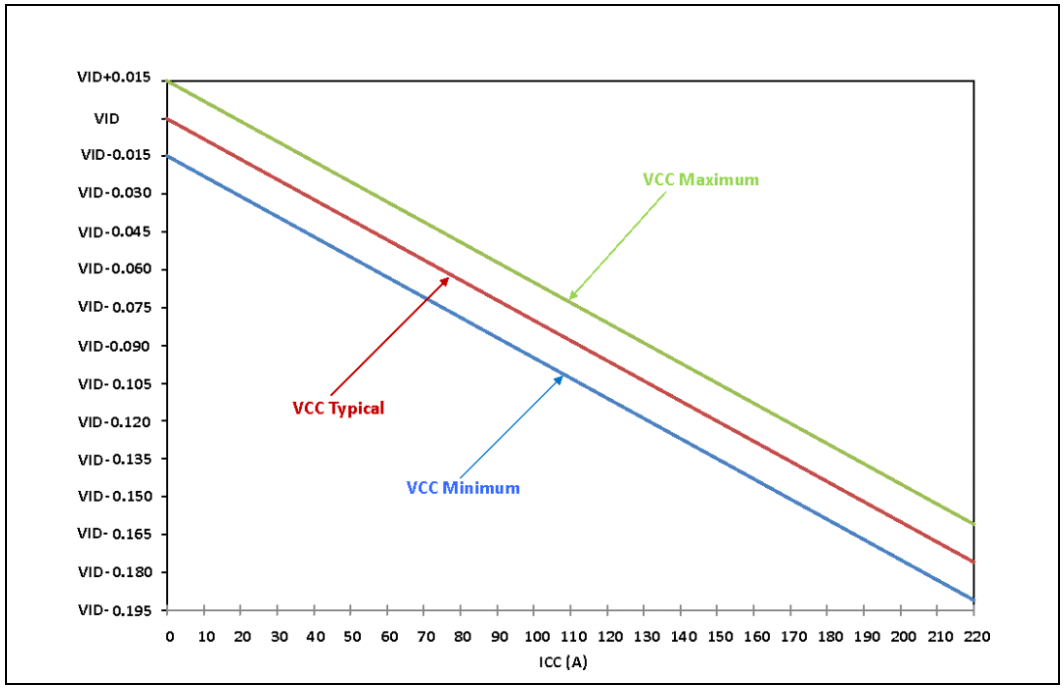
I_{CC} (A)	V_{CC_MAX} (V)	V_{CC_TYP} (V)	V_{CC_MIN} (V)	Notes
0	VID + 0.015	VID - 0.000	VID - 0.015	1,2,3,4,5
5	VID + 0.011	VID - 0.004	VID - 0.019	1,2,3,4,5
10	VID + 0.007	VID - 0.008	VID - 0.023	1,2,3,4,5
15	VID + 0.003	VID - 0.012	VID - 0.027	1,2,3,4,5
20	VID - 0.001	VID - 0.016	VID - 0.031	1,2,3,4,5
25	VID - 0.005	VID - 0.020	VID - 0.035	1,2,3,4,5
30	VID - 0.009	VID - 0.024	VID - 0.039	1,2,3,4,5
35	VID - 0.013	VID - 0.028	VID - 0.043	1,2,3,4,5
40	VID - 0.017	VID - 0.032	VID - 0.047	1,2,3,4,5
45	VID - 0.021	VID - 0.036	VID - 0.051	1,2,3,4,5
50	VID - 0.025	VID - 0.040	VID - 0.055	1,2,3,4,5
55	VID - 0.029	VID - 0.044	VID - 0.059	1,2,3,4,5
60	VID - 0.033	VID - 0.048	VID - 0.063	1,2,3,4,5
65	VID - 0.037	VID - 0.052	VID - 0.067	1,2,3,4,5
70	VID - 0.041	VID - 0.056	VID - 0.071	1,2,3,4,5
75	VID - 0.045	VID - 0.060	VID - 0.075	1,2,3,4,5
80	VID - 0.049	VID - 0.064	VID - 0.079	1,2,3,4,5,6
85	VID - 0.053	VID - 0.068	VID - 0.083	1,2,3,4,5,6
90	VID - 0.057	VID - 0.072	VID - 0.087	1,2,3,4,5,6
95	VID - 0.061	VID - 0.076	VID - 0.091	1,2,3,4,5,6
100	VID - 0.065	VID - 0.080	VID - 0.095	1,2,3,4,5,6
105	VID - 0.069	VID - 0.084	VID - 0.099	1,2,3,4,5,6
110	VID - 0.073	VID - 0.088	VID - 0.103	1,2,3,4,5,6
115	VID - 0.077	VID - 0.092	VID - 0.107	1,2,3,4,5,6
120	VID - 0.081	VID - 0.096	VID - 0.111	1,2,3,4,5,6
125	VID - 0.085	VID - 0.100	VID - 0.115	1,2,3,4,5,6
130	VID - 0.089	VID - 0.104	VID - 0.119	1,2,3,4,5,6
135	VID - 0.093	VID - 0.108	VID - 0.123	1,2,3,4,5,6
140	VID - 0.097	VID - 0.112	VID - 0.127	1,2,3,4,5,6
145	VID - 0.101	VID - 0.116	VID - 0.131	1,2,3,4,5,6
150	VID - 0.105	VID - 0.120	VID - 0.135	1,2,3,4,5,6
155	VID - 0.109	VID - 0.124	VID - 0.139	1,2,3,4,5,6
160	VID - 0.113	VID - 0.128	VID - 0.143	1,2,3,4,5,6

Table 6-14. V_{CC} Static and Transient Tolerance Intel® Xeon® E7 v2 Processor (Sheet 2 of 2)

I_{CC} (A)	V_{CC_MAX} (V)	V_{CC_TYP} (V)	V_{CC_MIN} (V)	Notes
165	VID - 0.117	VID - 0.132	VID - 0.147	1,2,3,4,5,6
170	VID - 0.121	VID - 0.136	VID - 0.151	1,2,3,4,5,6
175	VID - 0.125	VID - 0.140	VID - 0.155	1,2,3,4,5,6
180	VID - 0.129	VID - 0.144	VID - 0.159	1,2,3,4,5,6
185	VID - 0.133	VID - 0.148	VID - 0.163	1,2,3,4,5,6
190	VID- 0.137	VID - 0.152	VID - 0.167	1,2,3,4,5,6
195	VID - 0.141	VID - 0.156	VID - 0.171	1,2,3,4,5,6
200	VID - 0.145	VID - 0.160	VID - 0.175	1,2,3,4,5,6
205	VID - 0.149	VID - 0.164	VID - 0.179	1,2,3,4,5,6
210	VID - 0.153	VID - 0.168	VID - 0.183	1,2,3,4,5,6
215	VID - 0.157	VID - 0.172	VID - 0.187	1,2,3,4,5,6
220	VID - 0.161	VID - 0.176	VID - 0.191	1,2,3,4,5,6

Notes:
1. The loadline specification includes both static and transient limits.
2. This table is intended to aid in reading discrete points on graph in Figure 6-3.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_VCC_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC_SENSE and VSS_VCC_SENSE lands.
4. The Vcc_min and Vcc_max loadlines represent static and transient limits. Please see Section 5 for Vcc Overshoot specifications.
5. The Adaptive Loadline Positioning slope is 0.8 mΩ and the tolerance is ±15mV.
6. The core Icc ranges are as follows:
   - 0-220 A for Intel® Xeon® E7 v2 Processor (155 W)
   - 0-170 A for Intel® Xeon® E7 v2 Processor (130 W)
   - 0-160 A for Intel® Xeon® E7 v2 Processor (105 W

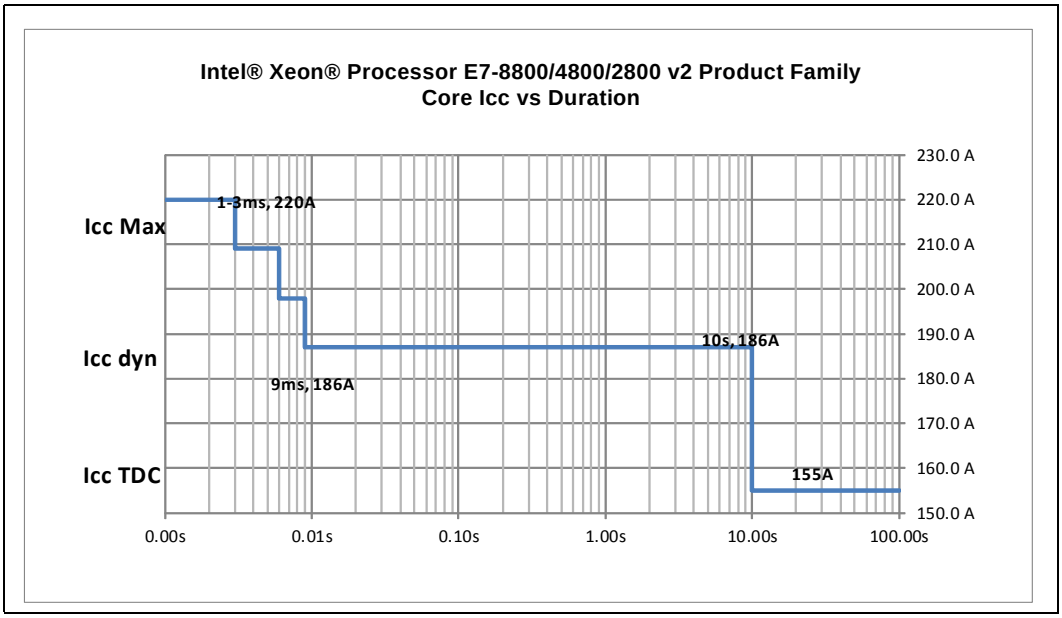
Figure 6-3. V_{CC} Static and Transient Tolerance Loadlines Intel® Xeon® E7 v2 Processor



6.9.2 Die Voltage Validation

Core voltage (V_{CC}) overshoot events at the processor must meet the specifications in Table 6-15 when measured across the VCC_SENSE and VSS_VCC_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

Figure 6-4. Load Current Versus Time



Notes:
1. In an IccMax condition, the CPU will respond to reduce the current within 3ms. It will then respond in a step wise fashion to bring the current down to the Icc dynamic condition.
2. Icc dynamic is not expected to last longer than 10 seconds with a heat sink which meets but does not significantly exceed the specifications set forth in this document. Current suggested value is 1.2x TDP.
3. Turbo performance may be impacted by failing to meet durations specified in this graph. Ensure that the platform design can handle peak and average current based on the specification.
4. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
5. Not 100% tested. Specified by design characterization.

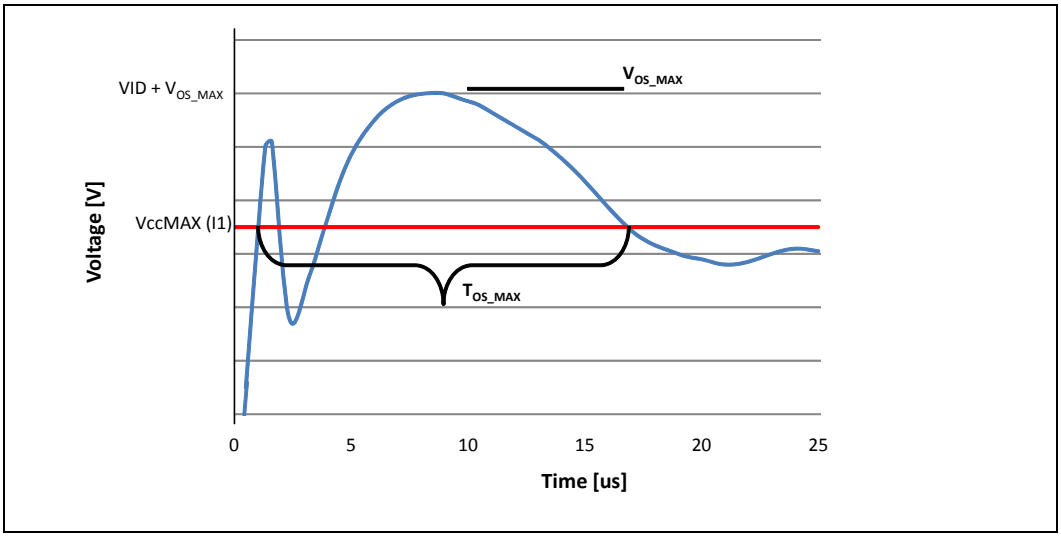
6.9.2.1 V_{CC} Overshoot Specifications

The Intel® Xeon® E7 v2 processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_VCC_SENSE lands.

Table 6-15. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID		65	mV	6-5	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VccMAX value at the new lighter load		25	uS	6-5	

Figure 6-5. V_{CC} Overshoot Example Waveform



Notes:
1. V_{OS_MAX} is the measured overshoot voltage.
2. T_{OS_MAX} is the measured time duration above VccMAX(I1).
3. Istep: Load Release Current Step, for example, I2 to I1, where I2 > I1.
4. VccMAX(I1) = VID - I1*RLL + 15 mV

6.9.3 Signal DC Specifications

Table 6-16. PECI DC Specifications

Symbol	Definition and Conditions	Min	Max	Units	Figure	Notes[1]
V_{In}	Input Voltage Range	-0.150	Vtt	V		
$V_{Hysteresis}$	Hysteresis	0.1 * Vtt		V		
V_N	Negative-edge threshold voltage	0.275 * Vtt	0.50 * Vtt	V	6-1	2
V_P	Positive-edge threshold voltage	0.55 * Vtt	0.725 * Vtt	V	6-1	2
R_{Pullup} Resistance	Pullup Resistance V_{OH} = 0.75 * V_{PECI}	N/A	50	Ohms		
I_{Leak+}	High impedance state leakage to V_{PECI} (V_{leak} = V_{OL})	N/A	50	uA		3
I_{Leak-}	High impedance leakage to GND (V_{leak} = V_{OH})	N/A	25	uA		3
C_{Bus}	Bus capacitance per node	N/A	10	pF		4,5
V_{Noise}	Signal noise immunity above 300 MHz	0.1 * Vtt	N/A	V_{p-p}		

Notes:
1. Vtt supplies the PECI interface for Intel® Xeon® E7v2.
2. It is expected that the PECI driver will take into account the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits.
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

Table 6-17. System Reference Clock (BCLK{0/1}) DC Specifications

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	Differential	0.150	N/A	V	6-13	
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	Differential		-0.150	V	6-13	
V_{cross} (abs)	Absolute Crossing Point	Single Ended	0.250	0.550	V	6-10 6-14	2, 4, 7
V_{cross}(rel)	Relative Crossing Point	Single Ended	0.250 + 0.5*(VH_{avg} - 0.700)	0.550 + 0.5*(VH_{avg} - 0.700)	V	6-10	3, 4, 5
ΔV_{cross}	Range of Crossing Points	Single Ended	N/A	0.140	V	6-15	6
V_{TH}	Threshold Voltage	Single Ended	Vcross - 0.1	Vcrloss + 0.1	V		
I_{IL}	Input Leakage Current	N/A		1.50	uA		8
C_{pad}	Pad Capacitance	N/A	0.9	1.1	pF		

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using “Vtop” on Agilent* and “High” on Tektronix oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
8. For Vin between 0 and Vih.

Table 6-18. SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*V_{TT}	V	
V_{IH}	Input High Voltage	0.7*VTT		V	
V_{OL}	Output Low Voltage		0.2*V_{TT}	V	
V_{OH}	Output High Voltage		$V_{TT(max)}$	V	
R_{ON}	Buffer On Resistance		14	W	
I_L	Leakage Current Signals MEM_SCL_C[3:0], MEM_SDA_C[3:0]	-100	+100	uA	
I_L	Leakage Current Signals VPP_SCL, VPP_SDA (R_{TEST} = 50 ohm)		+900	uA	

Table 6-19. JTAG and TAP Signals DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*V_{TT}	V	
V_{IH}	Input High Voltage	0.7*V_{TT}		V	
V_{OL}	Output Low Voltage (R_{TEST} = 500 ohm)		0.12*V_{TT}	V	
V_{OH}	Output High Voltage (R_{TEST} = 500 ohm)	0.88*V_{TT}		V	
R_{ON}	Buffer On Resistance Signals BPM_N[7:0], TDO, EAR_N		14	W	
I_{IL}	Input Leakage Current Signals PREQ_N, TCK, TDI, TMS, TRST_N	-50	+50	uA	

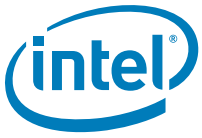


Table 6-19. JTAG and TAP Signals DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
I_{IL}	Input Leakage Current Signals BPM_N[7:0], TDO, EAR_N (R_{TEST} = 50 ohm)		+900	uA	
I_O	Output Current Signal PRDY_N (R_{TEST} = 500 ohm)	-1.50	+1.50	uA	
	Input Edge Rate Signals: BPM_N[7:0], EAR_N, PREQ_N, TCK, TDI, TMS, TRST_N	0.05		V/ns	1

Note:
1. These are measured between VIL and VIH.

Table 6-20. Serial VID Interface (SVID) DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	CPU I/O Voltage	V_{TT} - 3%	1.05	V_{TT} + 3%	V	
V_{IL}	Input Low Voltage Signals SVIDDATA, SVIDALERT_N			0.3*V_{TT}	V	1
V_{IH}	Input High Voltage Signals SVIDDATA, SVIDALERT_N	0.7*V_{TT}			V	1
V_{OH}	Output High Voltage Signals SVIDCLK, SVIDDATA			$V_{TT(max)}$	V	1
R_{ON}	Buffer On Resistance Signals SVIDCLK, SVIDDATA			14	Ohms	2
I_{IL}	Input Leakage Current Signals SVIDCLK, SVIDDATA			+900	uA	3,4
I_{IL}	Input Leakage Current Signal SVIDALERT_N	-500		+500	uA	3,4

Notes:
1. V_{TT} refers to instantaneous V_{TT}
2. Measured at 0.31*V_{TT}
3. Vin between 0V and V_{TT}

Table 6-21. Processor Asynchronous Sideband DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
	Input Edge Rate Signals: CAT_ERR_N, CPU_ONLY_RESET, MEM_HOT_C{01/23}_N, PMSYNC, PROCHOT_N, PWRGOOD, RESET_N	0.05		V/ns	5
CMOS1.0v Signals					
$V_{IL\_CMOS1.0v}$	Input Low Voltage		0.3*V_{TT}	V	1,2
$V_{IH\_CMOS1.0v}$	Input High Voltage	0.7*V_{TT}		V	1,2
V_{IL_MAX}	Input Low Voltage Signal PWRGOOD		0.320	V	1,2,4,
V_{IH_MIN}	Input High Voltage Signal PWRGOOD	0.640		V	1,2,4
$V_{OL\_CMOS1.0v}$	Output Low Voltage		0.12*V_{TT}	V	1,2
$V_{OH\_CMOS1.0v}$	Output High Voltage	0.88*V_{TT}		V	1,2
$I_{IL\_CMOS1.0v}$	Input Leakage Current	-50	+50	uA	1,2

Table 6-21. Processor Asynchronous Sideband DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
$I_{O\_CMOS1.0v}$	Output Current (R_{TEST} = 500 ohm)	-1.50	+1.50	uA	1,2
A_{NM_Rise}	Non-Monotonicity Amplitude, Rising Edge Signal PWRGOOD		0.135	V	4
A_{NM_Fall}	Non-Monotonicity Amplitude, Falling Edge Signal PWRGOOD		0.165	V	4
Open Drain CMOS (ODCMOS) Signals					
V_{IL_ODCMOS}	Input Low Voltage		$0.3*V_{TT}$	V	1,2
V_{IH_ODCMOS}	Input High Voltage	$0.7*V_{TT}$		V	1,2
V_{OH_ODCMOS}	Output High Voltage Signals: CAT_ERR_N, ERROR_N[2:0], THERMTRIP_N, PROCHOT_N, CPU_ONLY_RESET		$V_{TT(max)}$	V	1,2
I_{OL}	Output Leakage Current, Signal MEM_HOT_C{01/23}_N	-100	+100	uA	3
I_{OL}	Output Leakage Current (R_{TEST} = 50 ohm)		+900	uA	3
R_{ON}	Buffer On Resistance Signals: CAT_ERR_N, CPU_ONLY_RESET, ERROR_N[2:0], MEM_HOT_C{01/23}_N, PROCHOT_N, THERMTRIP_N		14	Ohms	1,2

Note:
1. This table applies to the processor sideband and miscellaneous signals specified in Table 6-5.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. For Vin between 0 and Voh.
4. PWRGOOD Non Monotonicity duration (T_{NM}) time is maximum 1.3 ns. See Figure 6-24 “PWRGOOD Signal Waveform”.
5. These are measured between VIL and VIH.

Table 6-22. Miscellaneous Signals DC Specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
SKTOCC_N Signal						
$V_{O\_ABS\_MAX}$	Output Absolute Max Voltage		3.30	3.50	V	
I_{OMAX}	Output Max Current			1	mA	

6.9.3.1 PCI Express* DC Specifications

Intel® Xeon® E7 v2 processor DC specifications for the PCI Express* are available in the *PCI Express® Base Specification - Revision 3.0*. This document will provide only the processor exceptions to the *PCI Express® Base Specification - Revision 3.0*.

6.9.3.2 DMI2/PCI Express DC Specifications

Intel® Xeon® E7 v2 processor DC specifications for the DMI2/PCI Express* are available in the *PCI Express® Base Specification 2.0 and 1.0*. This document will provide only the processor exceptions to the *PCI Express® Base Specification 2.0 and 1.0*.

6.9.3.3 Intel QuickPath Interconnect DC Specifications

Intel QuickPath Interconnect specifications are defined at the processor lands. P In most cases, termination resistors are not required as these are integrated into the processor silicon.

Intel® Xeon® E7 v2 processor DC specifications for the Intel® QPI interface are available in the *Intel® QuickPath Interconnect V1.1 Base Electrical Specification and Validation Methodologies*. This document will provide only the processor exceptions to the *Intel® QuickPath Interconnect V1.1 Base Electrical Specification and Validation Methodologies*.

6.9.3.4 Reset and Miscellaneous Signal DC Specifications

For a power-on Reset, RESET_N must stay active for at least 3.5 millisecond after V_{CC} and BCLK{0/1} have reached their proper specifications. RESET_N must not be kept asserted for more than 100 ms while PWRGOOD is asserted. RESET_N must be held asserted for at least 3.5 millisecond before it is deasserted again. RESET_N must be held asserted before PWRGOOD is asserted. This signal does not have on-die termination and must be terminated on the system board.

6.10 AC Specifications

AC specifications are defined at the processor pads, unless otherwise noted. Therefore, proper simulation is the only means to verify proper timing and signal quality. Timings specified in this section should be used in conjunction with processor signal integrity models provided by Intel. Care should be taken to read all notes associated with each parameter.

6.10.1 Signal AC Specifications

Table 6-23. System Reference Clock (BCLK{0/1}) AC Specifications

Parameter	Signal	Min	Typical	Max	Unit	Figure	Notes[1,2]
Reference Clock Frequency	Differential		100		MHz		3
BCLK Period	Differential		10		ns		3
BCLK Edge Rate	Differential	1		4	V/ns	6-12	5
$T_{BCLK-Dutycycle}$	Differential	40	50	60	%	6-11	
$T_{BCLK-diff-jit}$	Differential			500	ps		4
$V_{RB-Diff}$	Differential	-100		100	mV	6-13	6
T_{Stable}	Differential	500			psec	6-13	7

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. For clock jitter specifications, refer to *CK420BQ Clock Synthesizer/Driver Specifications*.
3. Average Period.
4. The phase drift between reference clocks at the two connected ports, that is the two reference clocks going to the processor.
5. Edge Rate time slopes (V/ns) are measured between +150 mV and -150 mV of the differential output of reference clock.
6. Measurement taken from differential waveform.
7. T_{Stable} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges, before it is allowed to droop back into the VRB ±100 mV range. See Figure 6-13.

Table 6-24. BCLK{0/1} Periods with Spread Spectrum Clocking (SSC)

	Measurement Window							
SSC State	1 Clock	1 us	0.1s	0.1s	0.1s	1 us	1 Clock	Units
	-Jitter c-c Absolute PerMin	- SSC Short-Term AveMin	- ppm Long-Term AveMin	Ideal Period Nominal	+ ppm Long Term AveMax	+ SSC Short-Term AveMax	+Jitter c-c Absolute PerMax	
SSC Off	9.94900	N/A	9.99900	10.00000	10.00100	N/A	10.05100	ns

Table 6-24. BCLK{0/1} Periods with Spread Spectrum Clocking (SSC)

SSC On	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns

Notes:
1. SSC is Spread Spectrum Clocking. The processor core clock frequency is derived from BCLK{0/1}. The system reference clock to processor core clock ratio is determined during initialization.
2. **Ideal Period Nominal:** This is as an ideal reference target (0 ppm) to use for calculating the rest of the period measurement values.
3. **0.1-second Measurement Window (frequency counter):** A valuable measurement done using a frequency counter to determine near DC average frequency (filtering out all jitter including SSC and cycle to cycle). This is used to determine if the system has a frequency static offset caused usually by incorrect crystal, crystal loading, or incorrect clock configuration.
4. **1.0-ms Measurement Window (scope):** This measurement is only used in conjunction with clock post processing software (for example, Jit3 Advanced) with "filters = LPF 3RD order 1-MHz pole" to filter out high frequency jitter (FM) and shows the underlying SSC profile. The numbers here bound the SSC Min/Max excursions (SSC magnitude).
5. **1 Clock (No Filter):** Any 1 Period measured with a scope. It is measured on a real time Oscilloscope using no filters, a simple period measurement (or a Jit3 period measurement which is more accurate), and provides absolute Min/Max timing information.

Table 6-25. SMBus Signal AC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes[1,2]
Transmitter and Receiver Timings						
F_{SMB}	SMBCLK Frequency	10	100	kHz		
TCK	SMBCLK Period	10	100	uS		
t_{LOW}	SMBCLK High Time	4		uS	6-16	
t_{HIGH}	SMBCLK Low Time	4.7		uS	6-16	
t_R	SMBus Rise Time		1	uS	6-16	3
t_F	SMBus Fall Time		0.3	uS	6-16	3
$t_{SU;DAT}$	SMBus Input Setup Time	250		ns	6-16	
$t_{HD;DAT}$	SMBus Input Hold Time	300		ns	6-16	
t_{BUF}	Bus Free Time between Stop and Start Condition	4.7		uS	6-16	4 5
$t_{HD;STA}$	Hold Time after Repeated Start Condition	4.0		uS	6-16	
$t_{SU;STA}$	Repeated Start Condition Setup Time	4.7		uS	6-16	
$t_{SU;STO}$	Stop Condition Setup Time	4.0		uS	6-16	
T_5	SMBus Output Valid Delay	0.1	4.5	uS	6-17	
	SMBus Edge Rate	0.5	1.5	V/ns		6

1. These parameters are based on design characterization and are not tested.
2. All AC timings for the SMBus signals are referenced at V_{IL_MAX} or V_{IL_MIN} and measured at the processor pins.
3. Rise time is measured from (V_{IL_MAX} - 0.15V) to (V_{IH_MIN} + 0.15V). Fall time is measured from (0.9 * V_{CC}) to (V_{IL_MAX} - 0.15V).
4. Minimum time allowed between request cycles.
5. Following a write transaction, an internal write cycle time of 10 ms must be allowed before starting the next transaction.
6. Edge rate measured at 20/80 percent of the signal level with a 50 ohm load.

Table 6-26. JTAG and TAP Signal AC Specifications (Sheet 1 of 2)

T# Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2]
T1: TDI, TDO, TMS Pulse Width	1			TCK	6-18	
T1: TRST_N Input Pulse Width	2			TCK	6-18	
T1: TRST_N Assert Time and TCK Pulse Width	2			TCK	6-18	5
T1: BPM_N[7:0] Input Pulse Width	5			ns	6-18	
T1: BPM_N[7:0] Output Pulse Width	10			ns	6-18	
T1: EAR_N Output Pulse Width	200			BCLK0	6-18	
T3: EAR_N Transition Time (V_{IL} to V_{IH})		5		ns	6-18	

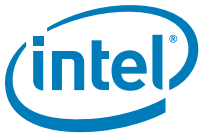


Table 6-26. JTAG and TAP Signal AC Specifications (Sheet 2 of 2)

T# Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2]
T5: TDO Clock to Output Valid Delay			5	ns	6-17	4
T5: BCLK0 to BPM_N [7:0] Output Valid Delay	1		8.6	ns	6-17	
T5: BCLK0 to PRDY_N Output Valid Delay	N/A		5	ns	6-17	
T_s: TDI, TMS Setup Time	6.5			ns	6-18	3
T_h: TDI, TMS Hold Time	6.5			ns	6-18	3
T_s: EAR_N Setup Time	1			uS	6-18	
T_h: EAR_N Hold Time	2			BCLK0	6-18	68
Boundary scan all non test output/float delay	0.5		25	ns		7
Boundary scan all non test input setup	15			ns		7,8
Boundary scan all non test input hold	15			ns		7,8

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. Referenced to the rising edge of TCK. Assuming minimum edge rate of 0.5 V/ns.
4. Referenced to the falling edge of TCK at the processor pad.
5. TRST_N is synchronized to TCK and asserted for 5 TCK periods while TMS is asserted.
6. Synchronous to PWRGOOD Input.
7. Referenced to the falling edge of TCK.
8. Referenced to the rising edge of TCK.

Table 6-27. Serial VID (SVID) Interface AC Timing Specifications

Symbol	Parameter	Min	Typ	Max	Units	Figure	Notes
	SVIDCLK Frequency		16.667		MHz	6-20	1
T_{Period}	Absolute Minimum SVIDCLK Period	59.3	62.5	62.6	ns	6-20	1
T_{co}	SVIDDATA Output Delay from SVIDCLK			5	ns	6-20	1,2
T_S	SVIDDATA Input Setup Time	1			ns	6-20	1
T_h	SVIDDATA Input Hold Time	5			ns	6-20	1,2
$T_{High/Low}$	SVIDCLK High and Low Time	30.0	31.5	33.0	ns		1,3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Referenced to the rising edge of SVIDCLK at $0.5*V_{TT.}$
3. T_{High} is measured with respect to $0.7 * V_{TT}$. T_{Low} time is measured with respect to $0.3 * V_{TT}$.

Table 6-28. Processor Asynchronous Sideband and Miscellaneous Signals AC Specifications (Sheet 1 of 2)

Parameter	Min	Max	Unit	Figure	Notes[1]
T2: PROCHOT_N Input Pulse Width Low	500		uS	6-18	
T1: PROCHOT_N Input Pulse Width High	5		uS	6-18	
T2: PROCHOT_N Output Pulse Width Low	500		uS	6-18	
T1: PROCHOT_N Output Pulse Width High	500		uS	6-18	
T_s: PROCHOT_N Setup Time	1		uS	6-19	
T_h: PROCHOT_N Hold Time		∞	uS	6-19	
T7: FRB Cold Boot: RESET_N de-assertion to PROCHOT_N de-assertion	1		uS	6-21	
T8: FRB Warm Boot: PROCHOT_N assertion to RESET_N assertion	1		uS	6-21	

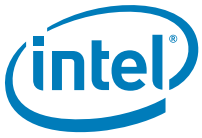
Table 6-28. Processor Asynchronous Sideband and Miscellaneous Signals AC Specifications (Sheet 2 of 2)

Parameter	Min	Max	Unit	Figure	Notes[1]
T9: FRB Warm Boot: RESET_N de-assertion to PROCHOT_N de-assertion	1		uS	6-21	
T2: PMSYNC Input Pulse Width Low	4		BCLK0	6-18	
T1: PMSYNC Input Pulse Width High	4	68	BCLK0	6-18	
T2: CAT_ERR_N Input Pulse Width Low	2		BCLK0	6-18	6
T1: CAT_ERR_N Input Pulse Width High	1		BCLK0	6-18	
T2: CAT_ERR_N Output Pulse Width Low	16		BCLK0	6-18	
T1: CAT_ERR_N Output Pulse Width High	1		BCLK0	6-18	
T2: CPU_ONLY_RESET Output Pulse Width Low	479		BCLK0	6-18	
T1: CPU_ONLY_RESET Output Pulse Width High	479		BCLK0	6-18	
T10: THERMTRIP_N assertion until V_{CC}/V_{TT} /V_{VMSE}/V_{SA} /V_{CCPLL}removed		500	ms	6-24	6
MEM_HOT_C{01/23}_N Output Pulse Width Low and High	1		VCLK		2,3
MEM_HOT_C{01/23}_N Input Pulse Width Low	>MH_SENSE _PERIOD	<=MH_SENSE_ PERIOD	uS	6-23	4
T3:PWRGOOD Input Signals Rise Time T4:PWRGOOD Input Signals Fall Time		20	ns	6-18	5
T11: BCLK0 stable to PWRGOOD assertion	10		BCLK0	6-22	
T12: PWRGOOD assertion to RESET_N de-assertion	5.0	100	ms	6-22	7, 8
V_{CCPLL} stable to PWRGOOD assertion	1		ms	6-22	
T13: $T_{Setup:}$ Power-On Configuration Setup Time to PWRGOOD assertion, Signals: BMCINIT, TXT_PLTEN, FRMAGENT, TXT_AGENT, SAFE_MODE_BOOT, SOCKET_ID[1:0]	1		uS	6-22	6
T14: $T_{Hold:}$ Power-On Configuration Hold Time, Signals: BMCINIT, TXT_PLTEN, FRMAGENT, TXT_AGENT, SAFE_MODE_BOOT, SOCKET_ID[1:0]	∞		uS	6-22	6
T18: VSA Assertion to PWRGOOD Assertion	2		ms	6-22	

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. VCLK is VMSE{0/1/2/3}_CLK_DN/DP[3:0].
3. Maximum High pulse width is constant High when there are no MEM_HOT_C{01/23}_N events, and the MH_SENSE_EN=0.
4. MH_SENSE_PERIOD is the MEM_HOT_C{01/23}_N sense period and guarantees external assertion detection, see *Intel® Xeon® Processor E7-2800/4800/8800 v2 Product Family Datasheet - Volume Two: Functional Description* for details. This is the configurable sense period and sense assertion time. When sense assertion time is set to zero, and the processor is asserting MEM_HOT_C{01/23}_N it will ignore externally asserted MEM_HOT_C{01/23}_N.
   a. Sense period: 50 uS, 100 uS, 200 uS, or 400 uS.
   b. Sense assertion time: 0, 1 uS, 1.5 uS, 2 uS, 2.5 uS, 3 uS, or 3.5 uS
5. $T_{pwrgood\_fall}$ and $T_{pwrgood\_rise}$ are measured 0.3*VTT to 0.7*VTT.
6. These signals are sampled after PWRGOOD assertion.
7. To meet TSC (Time Stamp Counter) multi-socket sampling, PWRGOOD must arrive to all processors within 1 BCLK{0/1} and the BCLK{0/1} skew between the sockets should be less than one-half (1/2) BCLK{0/1} cycle.
8. If EAR_N is used in the design, this signal requires a minimum of 100 us delay from PWRGOOD assertion.

6.10.1.1 PCI Express AC Specifications

Intel® Xeon® E7 v2 processor AC specifications for the PCI Express* are available in the *PCI Express® Base Specification - Revision 3.0*. This document will provide only the processor exceptions to the *PCI Express® Base Specification - Revision 3.0*.



6.10.1.2 DMI2/PCI Express AC Specifications

Intel® Xeon® E7 v2 processor AC specifications for the PCI Express* are available in the *PCI Express® Base Specification 2.0 and 1.0*. This document will provide only the processor exceptions to the *PCI Express® Base Specification 2.0 and 1.0*.

6.10.1.3 Intel® QuickPath Interconnect AC Specifications

Intel® QuickPath Interconnect specifications are defined at the processor lands.

Intel® Xeon® E7 v2 processor AC specifications for the Intel® QPI interface are available in the *Intel® QuickPath Interconnect V1.1 Base Electrical Specification and Validation Methodologies*. This document will provide only the processor exceptions to the *Intel® QuickPath Interconnect V1.1 Base Electrical Specification and Validation Methodologies*.

6.10.1.4 SMBus Signal AC Specifications

Intel® Xeon® E7 v2 processor AC specifications for the SMBus are available in the *System Management Bus (SMBus) Specification, Revision 2.0*. This document will provide only the processor exceptions to the *System Management Bus (SMBus) Specification, Revision 2.0*.

6.10.1.5 Reset and Miscellaneous Signal AC Specifications

For a power-on Reset, RESET_N must stay active for at least 3.5 millisecond after V_{CC} and BCLK{0/1} have reached their proper specifications. RESET_N must not be kept asserted for more than 100 ms while PWRGOOD is asserted. RESET_N must be held asserted for at least 3.5 millisecond before it is deasserted again. RESET_N must be held asserted before PWRGOOD is asserted. This signal does not have on-die termination and must be terminated on the system board.

6.11 AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Figure 6-7 through Figure 6-25.

Note: The circuit used to test the AC specification is shown in Figure 6-6.

Figure 6-6. Electrical Test Circuit

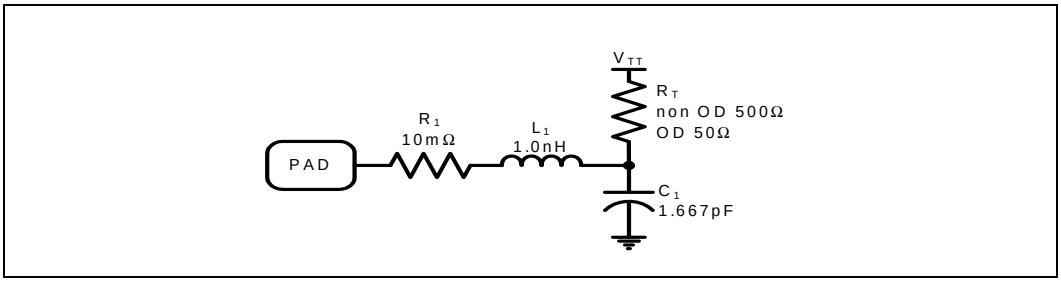


Figure 6-7. VMSE Command / Control and Clock Timing Waveform

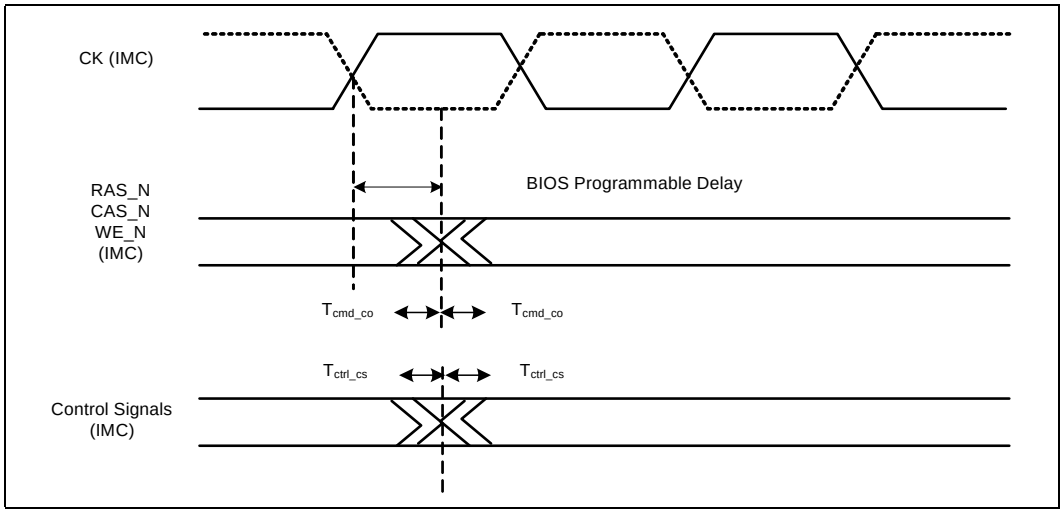


Figure 6-8. VMSE Clock to Output Timing Waveform

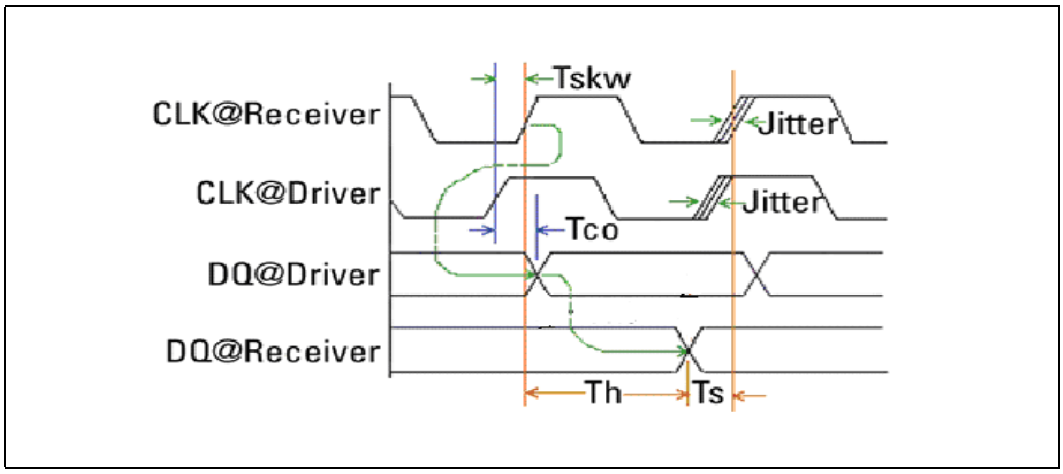


Figure 6-9. VMSE Clock to DQS_DN Skew Timing Waveform

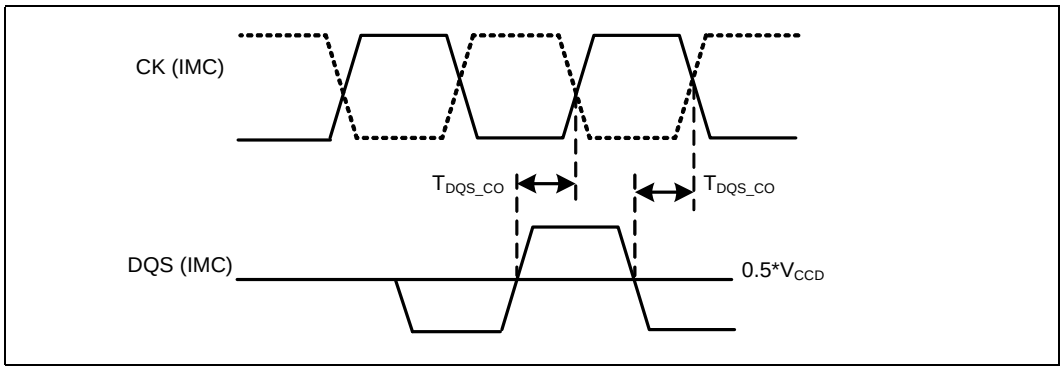


Figure 6-10. BCLK{0/1} Differential Clock Crosspoint Specification

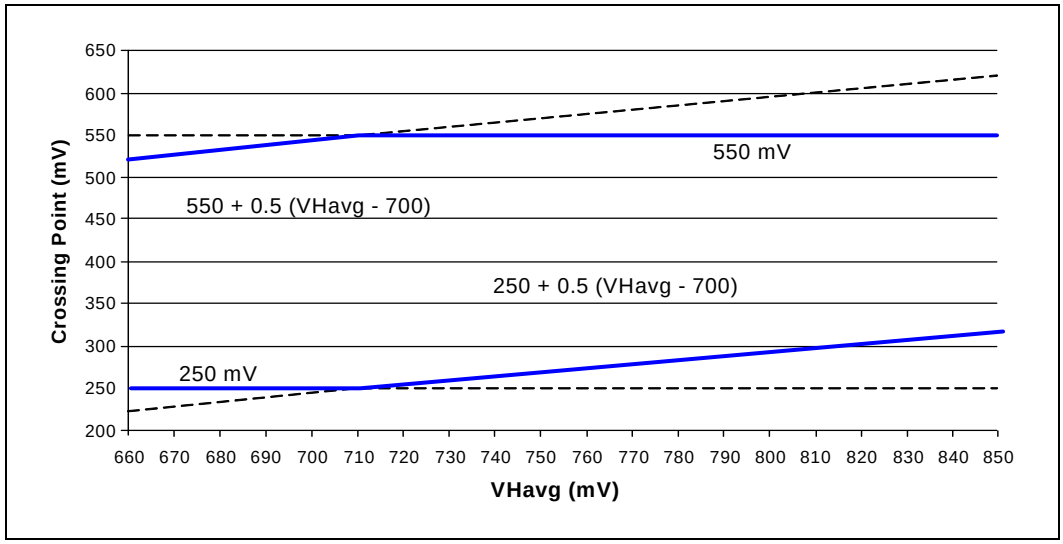


Figure 6-11. BCLK{0/1} Differential Clock Measurement Points for Duty Cycle and Period

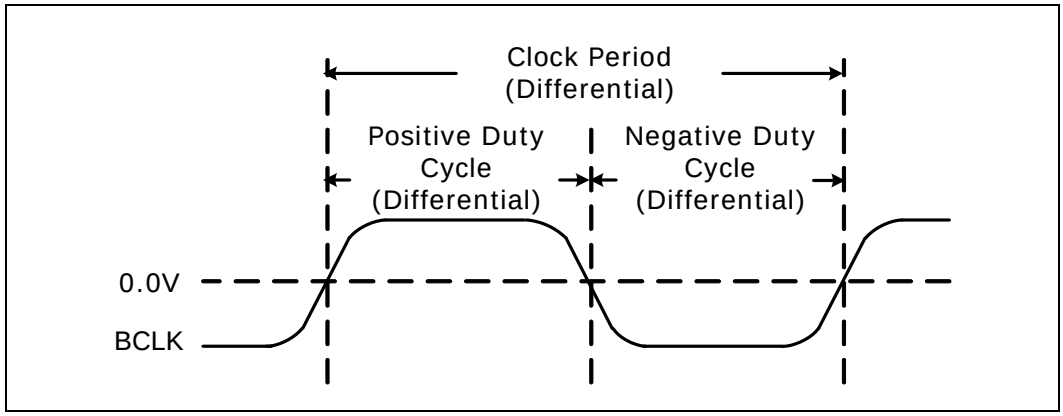


Figure 6-12. BCLK{0/1} Differential Clock Measurement Points for Edge Rate

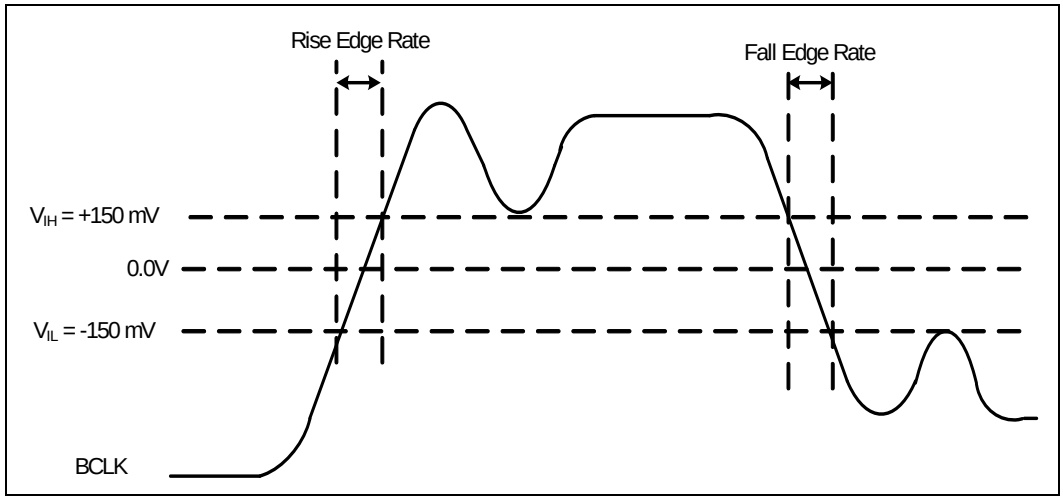


Figure 6-13. BCLK{0/1} Differential Clock Measurement Point for Ringback

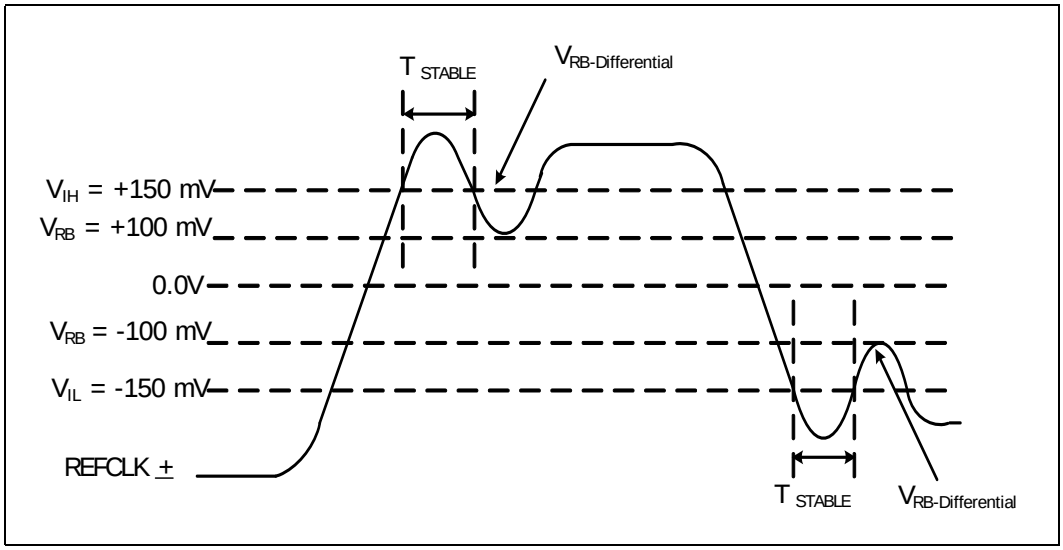


Figure 6-14. BCLK{0/1} Single Ended Clock Measurement Points for Absolute Cross Point and Swing

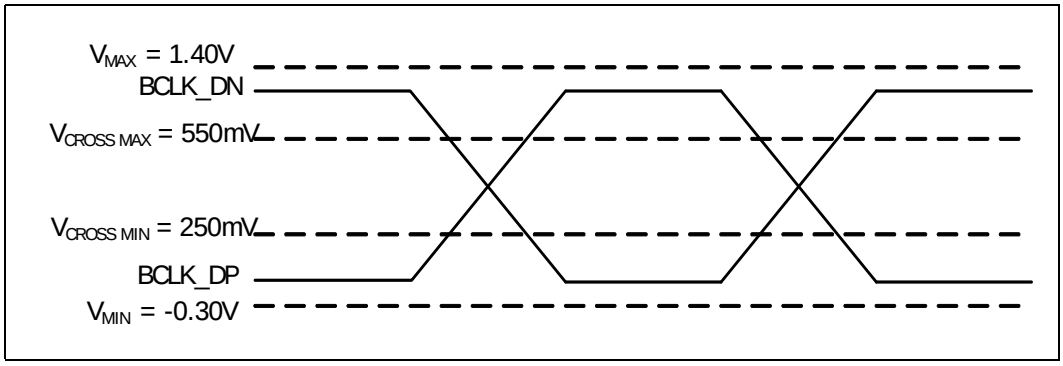


Figure 6-15. BCLK{0/1} Single Ended Clock Measurement Points for Delta Cross Point

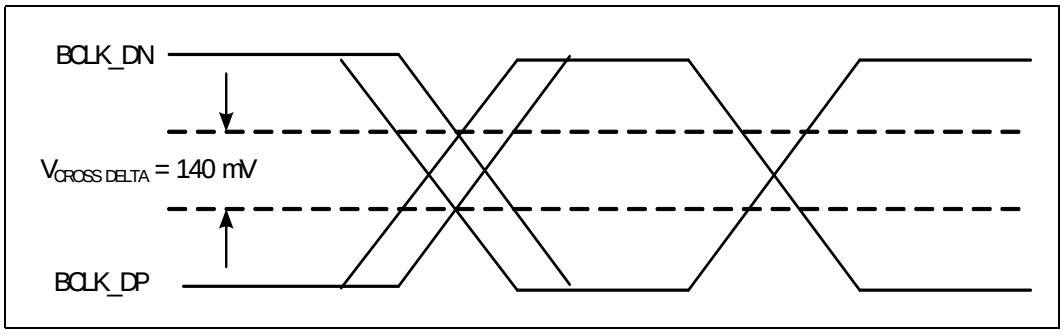


Figure 6-16. SMBus Timing Waveform

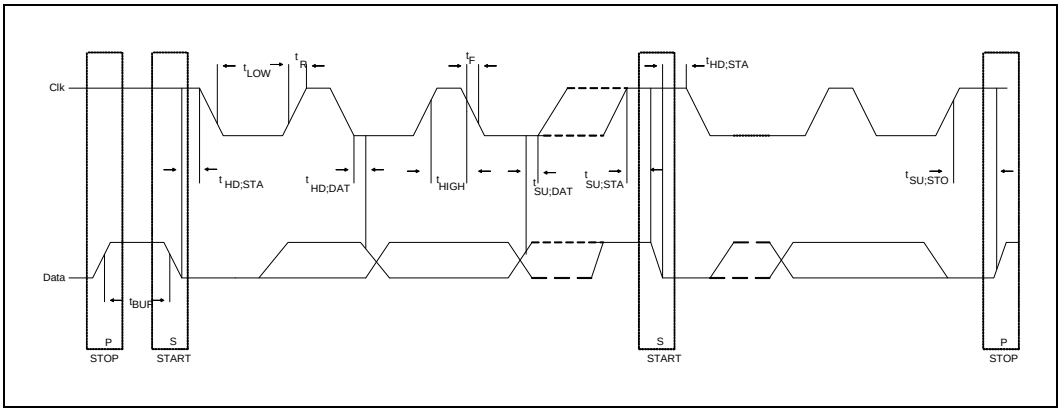


Figure 6-17. BCLK to JTAG/TAP Signals Output Valid Delay

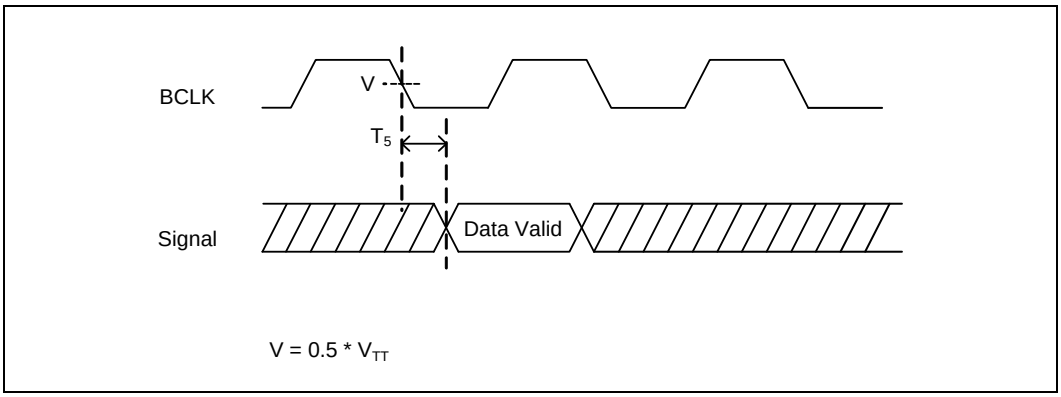


Figure 6-18. JTAG/TAP Output Valid Delay Timing Waveform

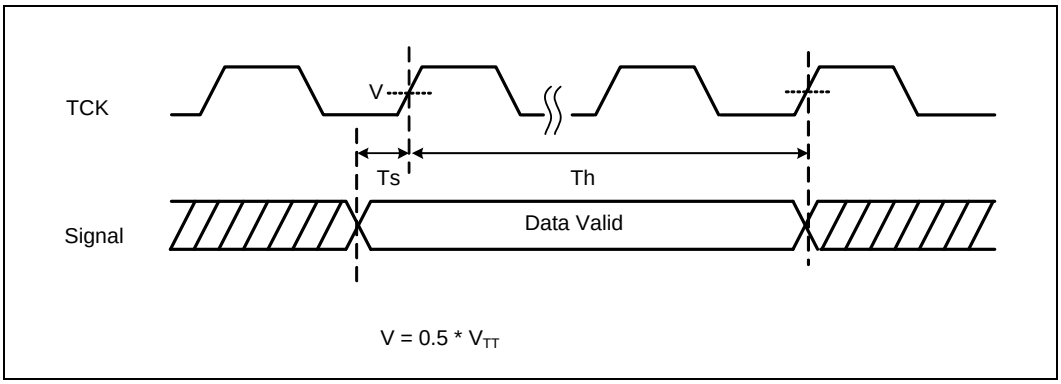


Figure 6-19. PROCHOT_N Setup and Hold Timing Waveforms

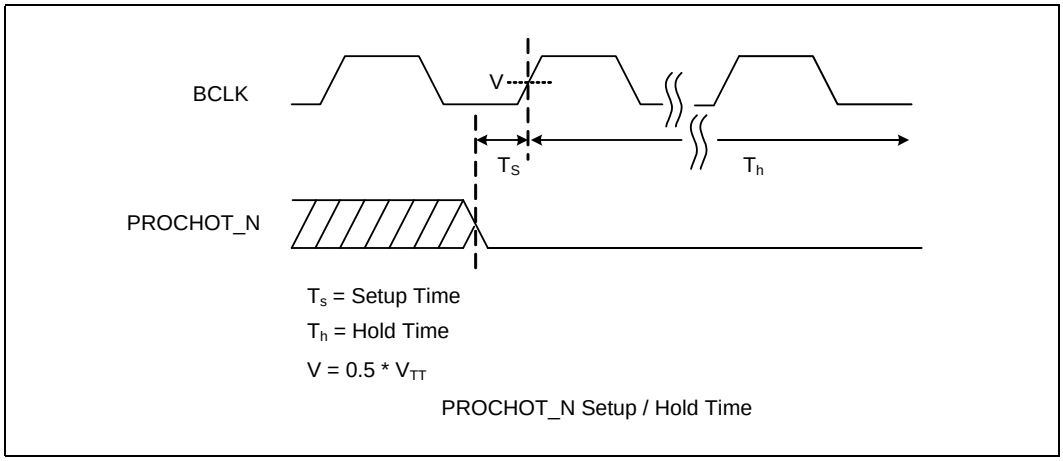


Figure 6-20. Serial VID Interface (SVID) Signals Clock Timings

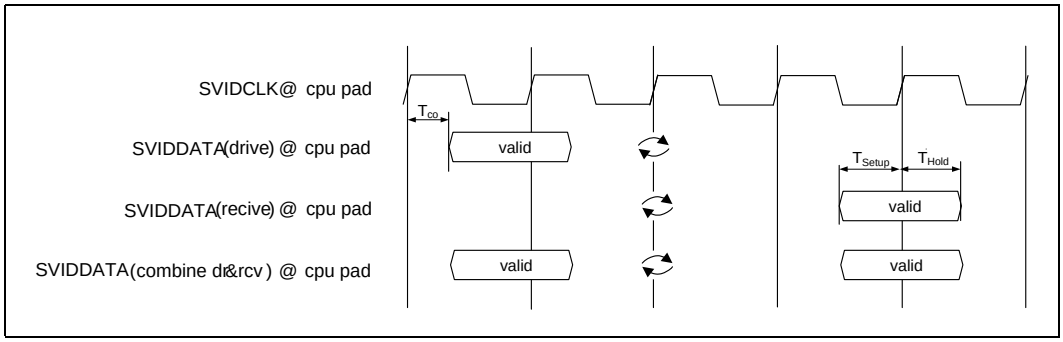


Figure 6-21. Fault Resilient Booting (FRB) Timing Requirements

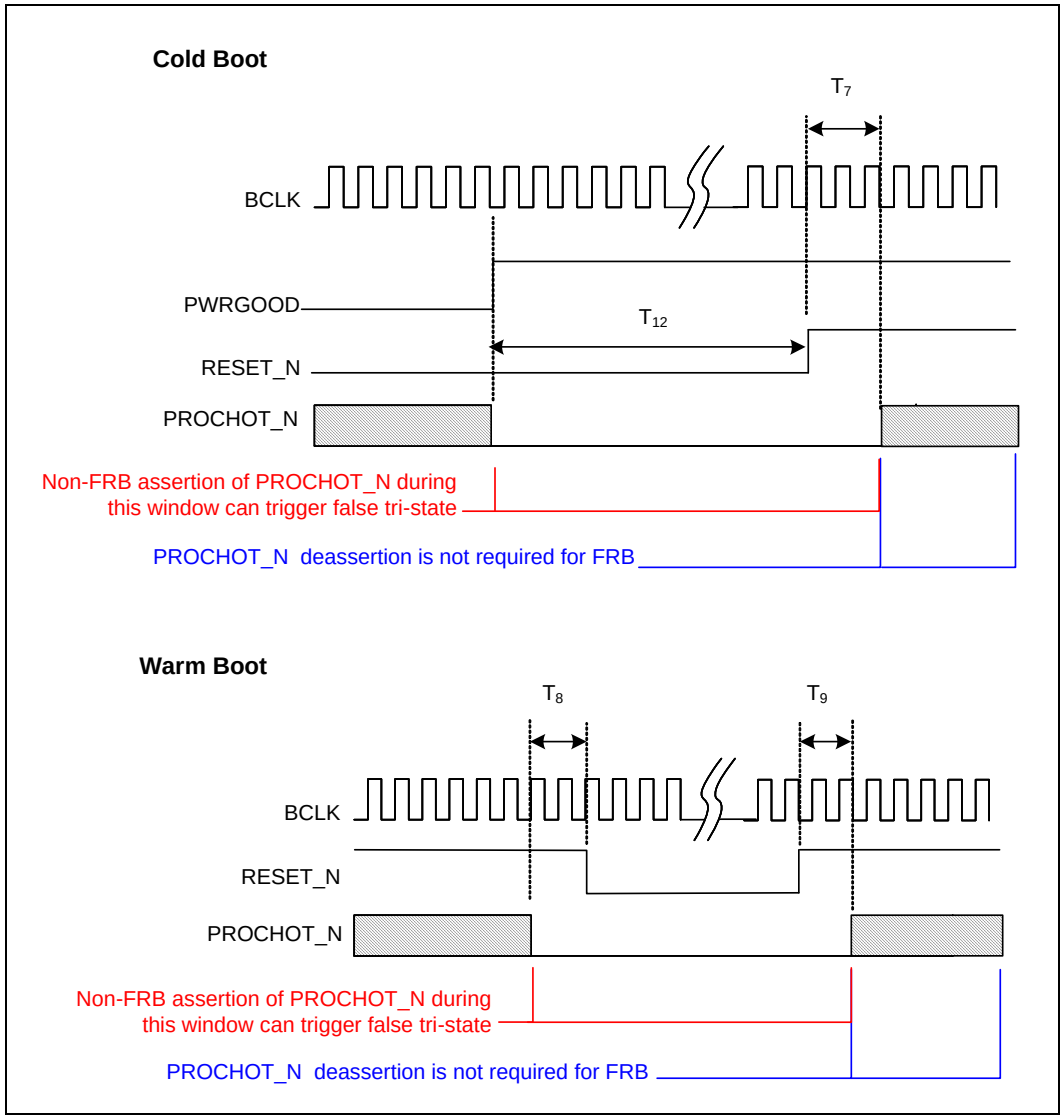
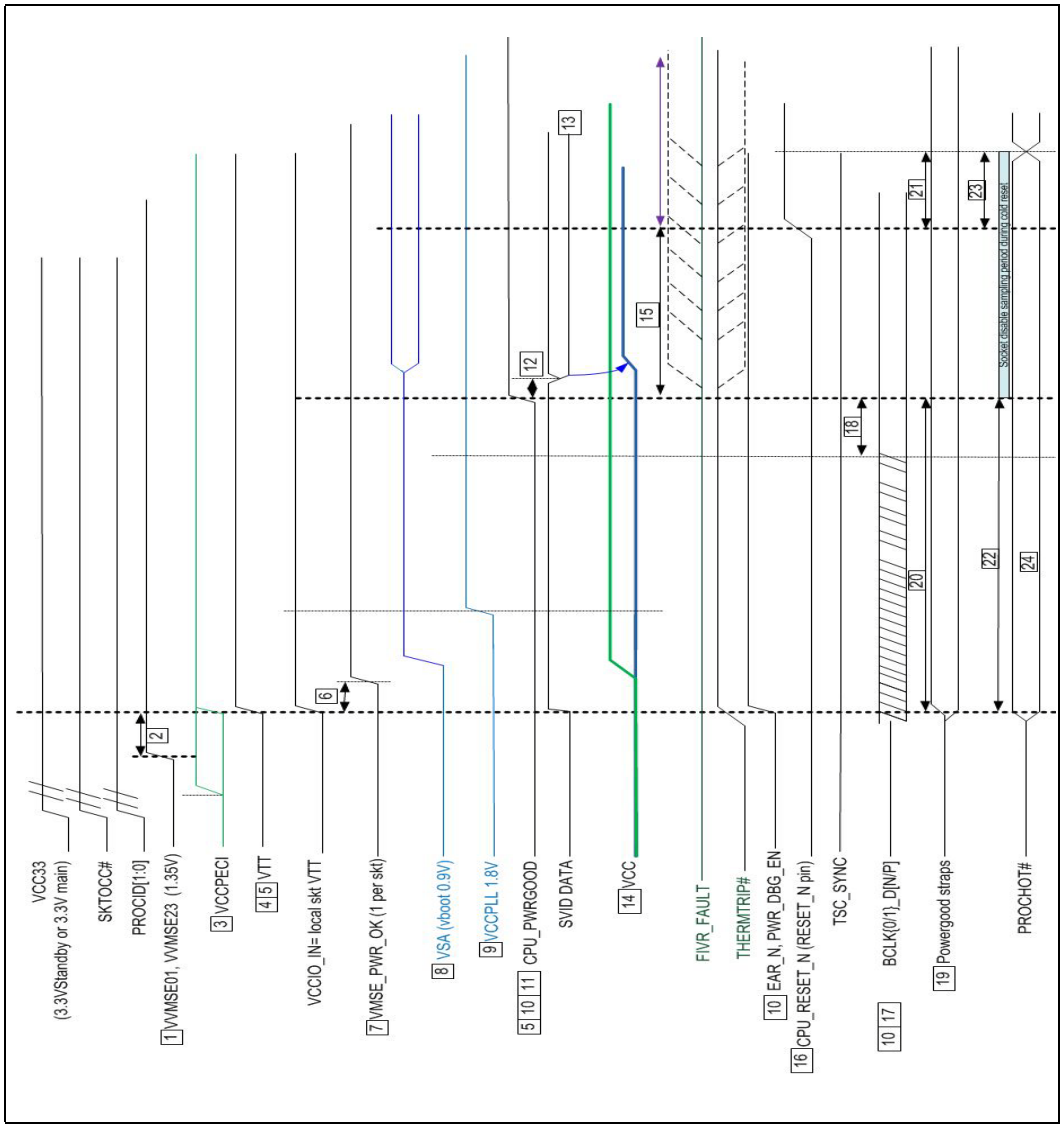


Figure 6-22. Voltage Sequence Timing Requirements



Notes:

1. Once up, VVMSE and VVMSE23, must stay up, even during memory hot plug.
2. Timing must be greater than 0ms.
3. VCCPECI is used by next generation CPUs. The pad is a no connect on package for Intel® Xeon® E7v2. Can be supplied via local VTT (and VCCIO_IN) of each socket, in which case VCCPECI somes up with VTT. Could also be supplied with Intel® C600 series chipset VPROC_IO (VCC_CPU_IO) at 1.0V, in which case VCCPECI comes up much earlier than VVMSE. Both usage cases are valid.
4. All sockets within a node, sharing common signals power up VTT together. Shared common CPU signals are pulled up by one VTT VR.
5. Memory can power on with the system, or when enabled by BIOS. When powered on with the system, there is no specific VVMSE ordering (unless shared with CPU and VR). Turn on the memory power before CPU PWRGOOD to allow SVID loads to power up before the CPU drives SVID. Also recommend power on Intel® C102/C104 Scalable Memory Buffer's Vcore with CPU VTT.
6. Timing must be equal to or greater than 1ms
7. Must be pulled up to VTT. Reflects the status of VTT and VMSE.
8. PWRGOOD_VMSE required to rise and be stable prior to rise of VSA. For next generation CPUs, VSA will never ramp. VSA required to rise and be stable prior to rise of VCCPLL. Values are per VR 12.5.
9. VSA required to rise and be stable prior to rise of VCCPLL. Values are per VR 12.5. For follow on CPUs VCCPLL will never ramp.
10. For BCLK, PWRGOOD, EAR_N, or PWR_DEBUG_N, delays from any driver to that pin on each socket in a system must be within 1 base clock cycle. BCLK pair wire latency between sockets must be within 1/2 base clock cycle.

11. If necessary, staggering of processor loads assumes all eternal rails to the processor in a node are powered on together, and staggering occurs with the PWRGOOD signals. If the PWRGOOD signals are staggered, then assertions of PWRGOOD must be at every 864 bclocks for Intel® Xeon® E7v2 and 384 bclocks for later CPUs. There is no setup or hold requirement to the bclock.
12. <5ms
13. SVID driven by processor
14. For Intel® Xeon® E7v2, VCC is 0V until SVID drives data. For follow on CPUs, VCC is Vboot at ~1.7-1.8V. Also, VCC comes up after VMSE_PWR_OK.
15. Platform (all CPUs) = 5 ms min and 500 ms max. For follow on CPUs, FIVR_FAULT may assert no sooner than 1.8ms after CPU_PWRGOOD assertion. When FIVR_FAULT asserts, THERMTRIP_N will also assert.
16. When the CPU is held in reset, it uses ~10% of its TDP power.
17. BCLKs may be enabled before the processor gets any power.
18. BCLK needs to be stable 10 BLCKs minimum before CPU_PWRGOOD
19. BMCINIT, FRMAGENT, LEGACY_SKT, BIST_ENABLE, TXT_PLTEN, TXT_AGENT, SOCKET_ID[2:0]
20. 1us is the minimum set up time between power good straps and CPU_PWRGOOD
21. Hold until next power cycle
22. PROCHOT needs to be valid 0ns min
23. 100 BLCKs
24. PROCHOT# for socket disable sampling
25. The CPU warm reset requirement is 3.5ms minimum and 100ms maximum.
26. Power down requirements are as follows: For Intel® Xeon® E7v2 VCCPLL goes off first, followed by VSA and VCC which can go down together. VTT(VCCIO_IN) are last. For follow on CPUs, VCCPLL goes off first, followed by VCC_IN and then VTT.
27. Power up sequence is not to scale. Blue signals are Intel® Xeon® E7v2 specific. Green signals are specific to later CPUs.

Figure 6-23. MEM_HOT_C{01/23}_N Event Assertion Waveform

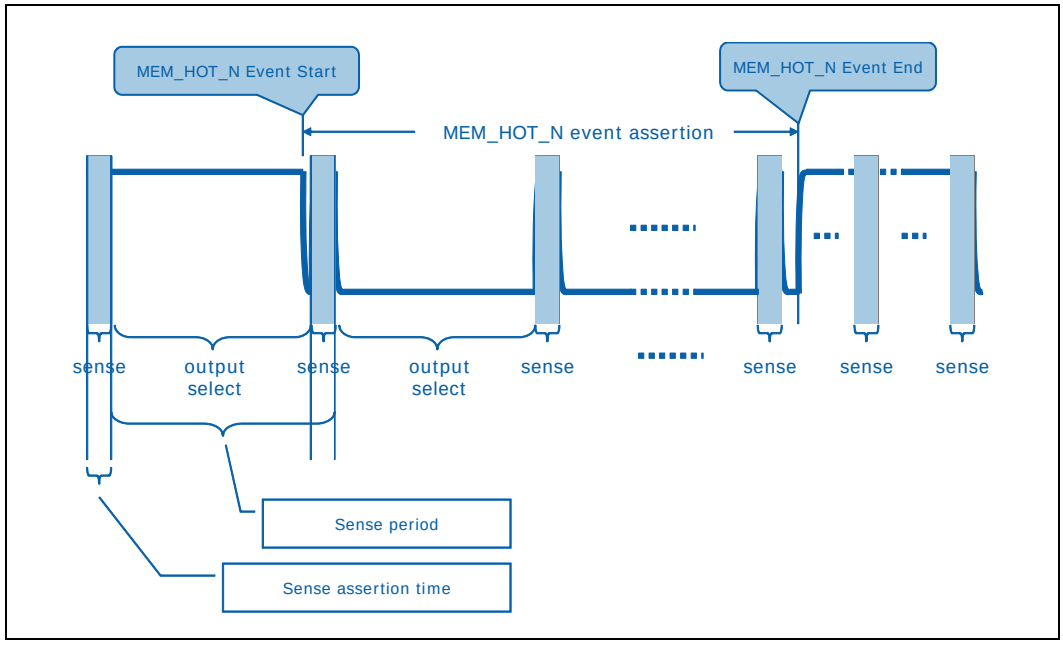
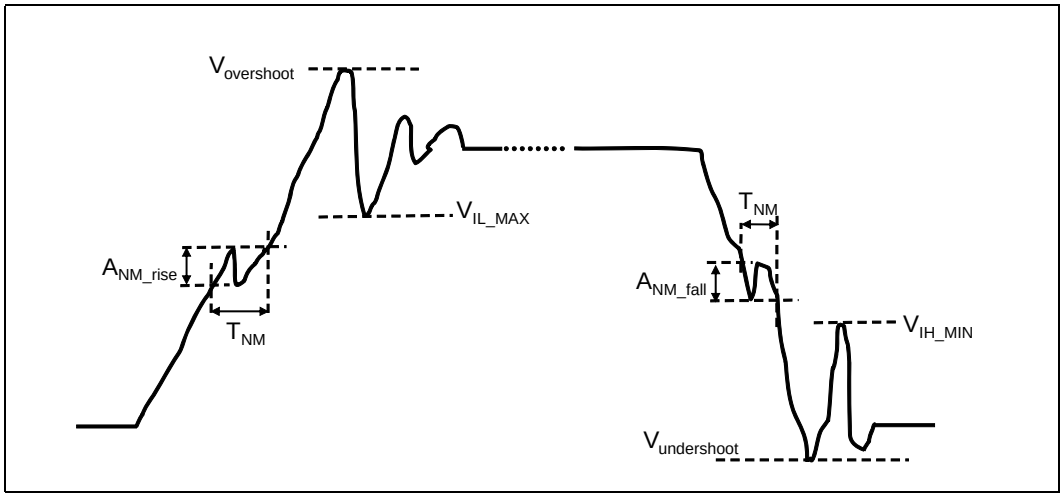


Figure 6-24. PWRGOOD Signal Waveform



6.12 Signal Quality

Data transfer requires the clean reception of data signals and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

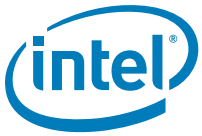
This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper simulation is the only way to verify proper timing and signal quality.

6.12.1 SMI2 Signal Quality Specifications

Various scenarios for the SMI2 Signals have been simulated to generate a set of layout guidelines.

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond specified maximum voltages or V_{SS} due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (that is, if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 6-29 will insure reliable IO performance for the lifetime of the processor.



6.12.2 I/O Signal Quality Specifications

Signal Quality specifications for PCIe Signals are included as part of the PCIe DC specifications and PCIe AC specifications. Various scenarios have been simulated to generate a set of layout guidelines.

6.12.3 Intel® QuickPath Interconnect Signal Quality Specifications

Signal Quality specifications for Differential Intel® QuickPath Interconnect Signals are included as part of the Intel QuickPath Interconnect defined in the *Intel® QuickPath Interconnect V1.1 Base Electrical Specification and Validation Methodologies*. Various scenarios have been simulated to generate a set of layout guidelines.

6.12.4 Input Reference Clock Signal Quality Specifications

Overshoot/Undershoot and Ringback specifications for BCLK{0/1}_D[N/P] are found in Table 6-29. Overshoot/Undershoot and Ringback specifications for the DDR3 Reference Clocks are specified by the DIMM.

6.12.5 Overshoot/Undershoot Tolerance

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below $V_{SS,}$ see Figure 6-25. The overshoot/undershoot specifications limit transitions beyond V_{VMSE} or V_{SS} due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (that is, if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 6-29 will insure reliable IO performance for the lifetime of the processor.

6.12.5.1 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to V_{SS}. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

The pulse magnitude and duration must be used to determine if the overshoot/undershoot pulse is within specifications.

6.12.5.2 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

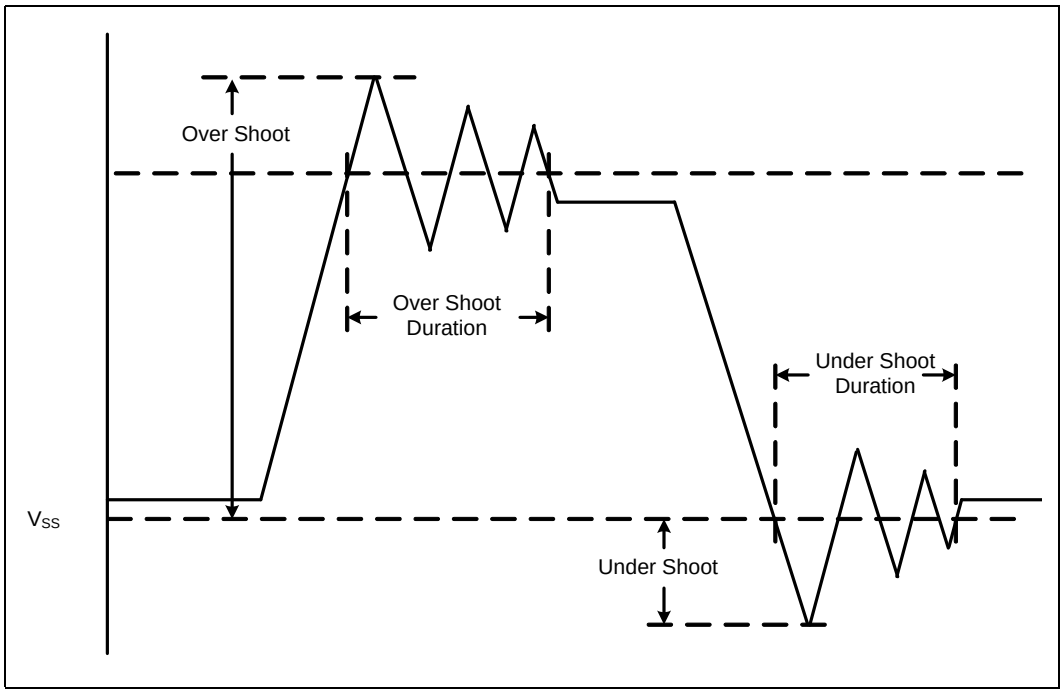
Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 6-29. Processor I/O Overshoot/Undershoot Specifications

Signal Group	Minimum Undershoot	Maximum Overshoot	Overshoot Duration	Undershoot Duration	Notes
Intel QuickPath Interconnect	-0.2 * VTT	1.2 * VTT	39 ps	15 ps	1,2
Processor Asynchronous Sideband Signals	-0.35 * VTT	1.35 * VTT	1.25 ns	0.5 ns	1,2
System Reference Clock (BCLK{0/1})	-0.3V	1.15V	N/A	N/A	1,2
Miscellaneous Signals	-0.35*Vtt	1.35*Vtt			
PWRGOOD Signal	-0.420V	VTT + 0.28	N/A	N/A	4

Notes:
1. These specifications are measured at the processor pad.
2. Refer to Figure 6-25 for description of allowable Overshoot/Undershoot magnitude and duration.
3. T_{CH} is the minimum high pulse width duration, see Table 6-25 through Table 6-28 for details on VMSE T_{CH}.
4. For PWRGOOD DC specifications see Table 6-21 and Figure 6-24 "PWRGOOD Signal Waveform".

Figure 6-25. Maximum Acceptable Overshoot/Undershoot Waveform



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7 Processor Land Listing

This chapter provides sorted land list in Section 7.1 and Section 7.2. Table 7-1 is a listing of all Intel® Xeon® E7v2 processor lands ordered alphabetically by land name. Table 7-2 is a listing of all processor lands ordered by land number.

7.1 Listing by Land Name

Table 7-1. Land Name (Sheet 1 of 50)

Land Name	Land No.	Buffer Type	Direction
BCLK0_DN	AF46	CMOS	I
BCLK0_DP	AH46	CMOS	I
BCLK1_DN	AE9	CMOS	I
BCLK1_DP	AF10	CMOS	I
BIST_ENABLE	AY50	CMOS	I
BMCINIT	AP50	CMOS	I
BPM_N[0]	K58	CMOS	I/O
BPM_N[1]	L57	CMOS	I/O
BPM_N[2]	E57	CMOS	I/O
BPM_N[3]	C55	CMOS	I/O
BPM_N[4]	B54	CMOS	I/O
BPM_N[5]	A53	CMOS	I/O
BPM_N[6]	D54	CMOS	I/O
BPM_N[7]	D56	CMOS	I/O
CATERR_N	AG35	CMOS	I/O
DEBUG_EN_N	BD10		
DMI_RX_N[0]	AY8	CMOS	I
DMI_RX_N[1]	BB8	CMOS	I
DMI_RX_N[2]	BD8	CMOS	I
DMI_RX_N[3]	BF8	CMOS	I
DMI_RX_P[0]	BA7	CMOS	I
DMI_RX_P[1]	BC7	CMOS	I
DMI_RX_P[2]	BE7	CMOS	I
DMI_RX_P[3]	BG7	CMOS	I
DMI_TX_N[0]	AK8	CMOS	O
DMI_TX_N[1]	AM8	CMOS	O
DMI_TX_N[2]	AP8	CMOS	O
DMI_TX_N[3]	AT8	CMOS	O
DMI_TX_P[0]	AL7	CMOS	O
DMI_TX_P[1]	AN7	CMOS	O
DMI_TX_P[2]	AR7	CMOS	O
DMI_TX_P[3]	AU7	CMOS	O

Table 7-1. Land Name (Sheet 2 of 50)

Land Name	Land No.	Buffer Type	Direction
EAR_N	CY58	CMOS	I/O
ERROR_N[0]	AR11	Open Drain	O
ERROR_N[1]	AT10	Open Drain	O
ERROR_N[2]	AN11	Open Drain	O
EX_LEGACY_SKT	H8	CMOS	I
FIVR_FAULT	AF36	CMOS	O
FRMAGENT	AD50	CMOS	I
MEM_HOT_C01_N	CB48	Open Drain	I/O
MEM_HOT_C23_N	CV12	Open Drain	I/O
MEM_SCL_C0	CN53	Open Drain	I/O
MEM_SCL_C1	DA29	Open Drain	I/O
MEM_SCL_C2	CB18	Open Drain	I/O
MEM_SCL_C3	CF6	Open Drain	I/O
MEM_SDA_C0	BR47	Open Drain	I/O
MEM_SDA_C1	CN41	Open Drain	I/O
MEM_SDA_C2	CJ11	Open Drain	I/O
MEM_SDA_C3	BK12	Open Drain	I/O
MSMI_N	BE53	CMOS	I/O
NMI	AE11	GTL	I
PE0_RX_N[0]	W35	PCIEX3	I
PE0_RX_N[1]	Y36	PCIEX3	I
PE0_RX_N[10]	G45	PCIEX3	I
PE0_RX_N[11]	H46	PCIEX3	I
PE0_RX_N[12]	W43	PCIEX3	I
PE0_RX_N[13]	Y44	PCIEX3	I
PE0_RX_N[14]	Y46	PCIEX3	I
PE0_RX_N[15]	W45	PCIEX3	I
PE0_RX_N[2]	W37	PCIEX3	I
PE0_RX_N[3]	Y38	PCIEX3	I
PE0_RX_N[4]	W39	PCIEX3	I
PE0_RX_N[5]	Y40	PCIEX3	I
PE0_RX_N[6]	W41	PCIEX3	I

Table 7-1. Land Name (Sheet 3 of 50)

Land Name	Land No.	Buffer Type	Direction
PE0_RX_N[7]	Y42	PCIEX3	I
PE0_RX_N[8]	G43	PCIEX3	I
PE0_RX_N[9]	H44	PCIEX3	I
PE0_RX_P[0]	AA35	PCIEX3	O
PE0_RX_P[1]	AB36	PCIEX3	I
PE0_RX_P[10]	J45	PCIEX3	I
PE0_RX_P[11]	K46	PCIEX3	I
PE0_RX_P[12]	AA43	PCIEX3	I
PE0_RX_P[13]	AB44	PCIEX3	I
PE0_RX_P[14]	AB46	PCIEX3	I
PE0_RX_P[15]	AA45	PCIEX3	I
PE0_RX_P[2]	AA37	PCIEX3	I
PE0_RX_P[3]	AB38	PCIEX3	I
PE0_RX_P[4]	AA39	PCIEX3	I
PE0_RX_P[5]	AB40	PCIEX3	I
PE0_RX_P[6]	AA41	PCIEX3	I
PE0_RX_P[7]	AB42	PCIEX3	I
PE0_RX_P[8]	J43	PCIEX3	I
PE0_RX_P[9]	K44	PCIEX3	I
PE0_TX_N[0]	N41	PCIEX3	O
PE0_TX_N[1]	P40	PCIEX3	O
PE0_TX_N[10]	G41	PCIEX3	O
PE0_TX_N[11]	P42	PCIEX3	O
PE0_TX_N[12]	N43	PCIEX3	O
PE0_TX_N[13]	P44	PCIEX3	O
PE0_TX_N[14]	N45	PCIEX3	O
PE0_TX_N[15]	P46	PCIEX3	O
PE0_TX_N[2]	N39	PCIEX3	O
PE0_TX_N[3]	N35	PCIEX3	O
PE0_TX_N[4]	P36	PCIEX3	O
PE0_TX_N[5]	N37	PCIEX3	O
PE0_TX_N[6]	P38	PCIEX3	O
PE0_TX_N[7]	H38	PCIEX3	O
PE0_TX_N[8]	G39	PCIEX3	O
PE0_TX_N[9]	H40	PCIEX3	O
PE0_TX_P[0]	R41	PCIEX3	O
PE0_TX_P[1]	T40	PCIEX3	O
PE0_TX_P[10]	J41	PCIEX3	O
PE0_TX_P[11]	T42	PCIEX3	O
PE0_TX_P[12]	R43	PCIEX3	O
PE0_TX_P[13]	T44	PCIEX3	O

Table 7-1. Land Name (Sheet 4 of 50)

Land Name	Land No.	Buffer Type	Direction
PE0_TX_P[14]	R45	PCIEX3	O
PE0_TX_P[15]	T46	PCIEX3	O
PE0_TX_P[2]	R39	PCIEX3	O
PE0_TX_P[3]	R35	PCIEX3	O
PE0_TX_P[4]	T36	PCIEX3	O
PE0_TX_P[5]	R37	PCIEX3	O
PE0_TX_P[6]	T38	PCIEX3	O
PE0_TX_P[7]	K38	PCIEX3	O
PE0_TX_P[8]	J39	PCIEX3	O
PE0_TX_P[9]	K40	PCIEX3	O
PE1_RX_N[0]	AA11	PCIEX3	I
PE1_RX_N[1]	W11	PCIEX3	I
PE1_RX_N[10]	B14	PCIEX3	I
PE1_RX_N[11]	D14	PCIEX3	I
PE1_RX_N[12]	E11	PCIEX3	I
PE1_RX_N[13]	A11	PCIEX3	I
PE1_RX_N[14]	C11	PCIEX3	I
PE1_RX_N[15]	A9	PCIEX3	I
PE1_RX_N[2]	U11	PCIEX3	I
PE1_RX_N[3]	R11	PCIEX3	I
PE1_RX_N[4]	N11	PCIEX3	I
PE1_RX_N[5]	L11	PCIEX3	I
PE1_RX_N[6]	J11	PCIEX3	I
PE1_RX_N[7]	G11	PCIEX3	I
PE1_RX_N[8]	H14	PCIEX3	I
PE1_RX_N[9]	F14	PCIEX3	I
PE1_RX_P[0]	AB10	PCIEX3	I
PE1_RX_P[1]	Y10	PCIEX3	I
PE1_RX_P[10]	C13	PCIEX3	I
PE1_RX_P[11]	E13	PCIEX3	I
PE1_RX_P[12]	F10	PCIEX3	I
PE1_RX_P[13]	B10	PCIEX3	I
PE1_RX_P[14]	D10	PCIEX3	I
PE1_RX_P[15]	B8	PCIEX3	I
PE1_RX_P[2]	V10	PCIEX3	I
PE1_RX_P[3]	T10	PCIEX3	I
PE1_RX_P[4]	P10	PCIEX3	I
PE1_RX_P[5]	M10	PCIEX3	I
PE1_RX_P[6]	K10	PCIEX3	I
PE1_RX_P[7]	H10	PCIEX3	I
PE1_RX_P[8]	J13	PCIEX3	I

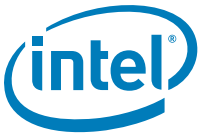

Table 7-1. Land Name (Sheet 5 of 50)

Land Name	Land No.	Buffer Type	Direction
PE1_RX_P[9]	G13	PCIEX3	I
PE1_TX_N[0]	AA17	PCIEX3	O
PE1_TX_N[1]	W17	PCIEX3	O
PE1_TX_N[10]	C17	PCIEX3	O
PE1_TX_N[11]	Y14	PCIEX3	O
PE1_TX_N[12]	V14	PCIEX3	O
PE1_TX_N[13]	M14	PCIEX3	O
PE1_TX_N[14]	P14	PCIEX3	O
PE1_TX_N[15]	T14	PCIEX3	O
PE1_TX_N[2]	U17	PCIEX3	O
PE1_TX_N[3]	R17	PCIEX3	O
PE1_TX_N[4]	N17	PCIEX3	O
PE1_TX_N[5]	L17	PCIEX3	O
PE1_TX_N[6]	J17	PCIEX3	O
PE1_TX_N[7]	G17	PCIEX3	O
PE1_TX_N[8]	E17	PCIEX3	O
PE1_TX_N[9]	A17	PCIEX3	O
PE1_TX_P[0]	AB16	PCIEX3	O
PE1_TX_P[1]	Y16	PCIEX3	O
PE1_TX_P[10]	D16	PCIEX3	O
PE1_TX_P[11]	AA13	PCIEX3	O
PE1_TX_P[12]	W13	PCIEX3	O
PE1_TX_P[13]	N13	PCIEX3	O
PE1_TX_P[14]	R13	PCIEX3	O
PE1_TX_P[15]	U13	PCIEX3	O
PE1_TX_P[2]	V16	PCIEX3	O
PE1_TX_P[3]	T16	PCIEX3	O
PE1_TX_P[4]	P16	PCIEX3	O
PE1_TX_P[5]	M16	PCIEX3	O
PE1_TX_P[6]	K16	PCIEX3	O
PE1_TX_P[7]	H16	PCIEX3	O
PE1_TX_P[8]	F16	PCIEX3	O
PE1_TX_P[9]	B16	PCIEX3	O
PECI	AE41	PECI	I/O
PIROM_ADDR[0]	Y8		I/O
PIROM_ADDR[1]	L5		I/O
PIROM_ADDR[2]	P8		I/O
PM_FAST_WAKE_N	AG11	CMOS	I/O
PMSYNC	AE45	CMOS	I
PRDY_N	AE39	CMOS	O
PREQ_N	AE35	CMOS	I

Table 7-1. Land Name (Sheet 6 of 50)

Land Name	Land No.	Buffer Type	Direction
PROC_ID[0]	AH8		O
PROC_ID[1]	AG9		O
PROCHOT_N	AV56	Open Drain	I/O
PWR_DEBUG_N	BJ9	CMOS	I
PWRGOOD	BL55	CMOS	I
QPI0_CLKRX_DN	A43	Intel QPI	I
QPI0_CLKRX_DP	C43	Intel QPI	I
QPI0_CLKTX_DN	AE53	Intel QPI	O
QPI0_CLKTX_DP	AF52	Intel QPI	O
QPI0_DRX_DN[0]	F34	Intel QPI	I
QPI0_DRX_DN[1]	G35	Intel QPI	I
QPI0_DRX_DN[10]	B44	Intel QPI	I
QPI0_DRX_DN[11]	A45	Intel QPI	I
QPI0_DRX_DN[12]	B46	Intel QPI	I
QPI0_DRX_DN[13]	A47	Intel QPI	I
QPI0_DRX_DN[14]	B48	Intel QPI	I
QPI0_DRX_DN[15]	A49	Intel QPI	I
QPI0_DRX_DN[16]	B50	Intel QPI	I
QPI0_DRX_DN[17]	C51	Intel QPI	I
QPI0_DRX_DN[18]	D52	Intel QPI	I
QPI0_DRX_DN[19]	E53	Intel QPI	I
QPI0_DRX_DN[2]	H36	Intel QPI	I
QPI0_DRX_DN[3]	A35	Intel QPI	I
QPI0_DRX_DN[4]	B36	Intel QPI	I
QPI0_DRX_DN[5]	A37	Intel QPI	I
QPI0_DRX_DN[6]	B38	Intel QPI	I
QPI0_DRX_DN[7]	A39	Intel QPI	I
QPI0_DRX_DN[8]	B40	Intel QPI	I
QPI0_DRX_DN[9]	A41	Intel QPI	I
QPI0_DRX_DP[0]	H34	Intel QPI	I
QPI0_DRX_DP[1]	J35	Intel QPI	I
QPI0_DRX_DP[10]	D44	Intel QPI	I
QPI0_DRX_DP[11]	C45	Intel QPI	I
QPI0_DRX_DP[12]	D46	Intel QPI	I
QPI0_DRX_DP[13]	C47	Intel QPI	I
QPI0_DRX_DP[14]	D48	Intel QPI	I
QPI0_DRX_DP[15]	C49	Intel QPI	I
QPI0_DRX_DP[16]	D50	Intel QPI	I
QPI0_DRX_DP[17]	E51	Intel QPI	I
QPI0_DRX_DP[18]	F52	Intel QPI	I
QPI0_DRX_DP[19]	G53	Intel QPI	I

Table 7-1. Land Name (Sheet 7 of 50)

Land Name	Land No.	Buffer Type	Direction
QPI0_DRX_DP[2]	K36	Intel QPI	I
QPI0_DRX_DP[3]	C35	Intel QPI	I
QPI0_DRX_DP[4]	D36	Intel QPI	I
QPI0_DRX_DP[5]	C37	Intel QPI	I
QPI0_DRX_DP[6]	D38	Intel QPI	I
QPI0_DRX_DP[7]	C39	Intel QPI	I
QPI0_DRX_DP[8]	D40	Intel QPI	I
QPI0_DRX_DP[9]	C41	Intel QPI	I
QPI0_DTX_DN[0]	G49	Intel QPI	O
QPI0_DTX_DN[1]	J49	Intel QPI	O
QPI0_DTX_DN[10]	AJ55	Intel QPI	O
QPI0_DTX_DN[11]	AL55	Intel QPI	O
QPI0_DTX_DN[12]	AN55	Intel QPI	O
QPI0_DTX_DN[13]	AR55	Intel QPI	O
QPI0_DTX_DN[14]	AU55	Intel QPI	O
QPI0_DTX_DN[15]	AW55	Intel QPI	O
QPI0_DTX_DN[16]	BA55	Intel QPI	O
QPI0_DTX_DN[17]	BC55	Intel QPI	O
QPI0_DTX_DN[18]	BE55	Intel QPI	O
QPI0_DTX_DN[19]	BG55	Intel QPI	O
QPI0_DTX_DN[2]	L49	Intel QPI	O
QPI0_DTX_DN[3]	L53	Intel QPI	O
QPI0_DTX_DN[4]	N53	Intel QPI	O
QPI0_DTX_DN[5]	R53	Intel QPI	O
QPI0_DTX_DN[6]	U53	Intel QPI	O
QPI0_DTX_DN[7]	W53	Intel QPI	O
QPI0_DTX_DN[8]	AA53	Intel QPI	O
QPI0_DTX_DN[9]	AC53	Intel QPI	O
QPI0_DTX_DP[0]	H48	Intel QPI	O
QPI0_DTX_DP[1]	K48	Intel QPI	O
QPI0_DTX_DP[10]	AK54	Intel QPI	O
QPI0_DTX_DP[11]	AM54	Intel QPI	O
QPI0_DTX_DP[12]	AP54	Intel QPI	O
QPI0_DTX_DP[13]	AT54	Intel QPI	O
QPI0_DTX_DP[14]	AV54	Intel QPI	O
QPI0_DTX_DP[15]	AY54	Intel QPI	O
QPI0_DTX_DP[16]	BB54	Intel QPI	O
QPI0_DTX_DP[17]	BD54	Intel QPI	O
QPI0_DTX_DP[18]	BF54	Intel QPI	O
QPI0_DTX_DP[19]	BH54	Intel QPI	O
QPI0_DTX_DP[2]	M48	Intel QPI	O

Table 7-1. Land Name (Sheet 8 of 50)

Land Name	Land No.	Buffer Type	Direction
QPI0_DTX_DP[3]	M52	Intel QPI	O
QPI0_DTX_DP[4]	P52	Intel QPI	O
QPI0_DTX_DP[5]	T52	Intel QPI	O
QPI0_DTX_DP[6]	V52	Intel QPI	O
QPI0_DTX_DP[7]	Y52	Intel QPI	O
QPI0_DTX_DP[8]	AB52	Intel QPI	O
QPI0_DTX_DP[9]	AD52	Intel QPI	O
QPI1_CLKRX_DN	AF58	Intel QPI	I
QPI1_CLKRX_DP	AG57	Intel QPI	I
QPI1_CLKTX_DN	AK52	Intel QPI	O
QPI1_CLKTX_DP	AL51	Intel QPI	O
QPI1_DRX_DN[0]	BF58	Intel QPI	I
QPI1_DRX_DN[1]	BD58	Intel QPI	I
QPI1_DRX_DN[10]	AD56	Intel QPI	I
QPI1_DRX_DN[11]	AB56	Intel QPI	I
QPI1_DRX_DN[12]	Y56	Intel QPI	I
QPI1_DRX_DN[13]	V56	Intel QPI	I
QPI1_DRX_DN[14]	T56	Intel QPI	I
QPI1_DRX_DN[15]	P56	Intel QPI	I
QPI1_DRX_DN[16]	M56	Intel QPI	I
QPI1_DRX_DN[17]	K56	Intel QPI	I
QPI1_DRX_DN[18]	H56	Intel QPI	I
QPI1_DRX_DN[19]	F56	Intel QPI	I
QPI1_DRX_DN[2]	BB58	Intel QPI	I
QPI1_DRX_DN[3]	AY58	Intel QPI	I
QPI1_DRX_DN[4]	AV58	Intel QPI	I
QPI1_DRX_DN[5]	AT58	Intel QPI	I
QPI1_DRX_DN[6]	AP58	Intel QPI	I
QPI1_DRX_DN[7]	AM58	Intel QPI	I
QPI1_DRX_DN[8]	AK58	Intel QPI	I
QPI1_DRX_DN[9]	AH58	Intel QPI	I
QPI1_DRX_DP[0]	BG57	Intel QPI	I
QPI1_DRX_DP[1]	BE57	Intel QPI	I
QPI1_DRX_DP[10]	AE55	Intel QPI	I
QPI1_DRX_DP[11]	AC55	Intel QPI	I
QPI1_DRX_DP[12]	AA55	Intel QPI	I
QPI1_DRX_DP[13]	W55	Intel QPI	I
QPI1_DRX_DP[14]	U55	Intel QPI	I
QPI1_DRX_DP[15]	R55	Intel QPI	I
QPI1_DRX_DP[16]	N55	Intel QPI	I
QPI1_DRX_DP[17]	L55	Intel QPI	I

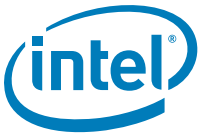

Table 7-1. Land Name (Sheet 9 of 50)

Land Name	Land No.	Buffer Type	Direction
QPI1_DRX_DP[18]	J55	Intel QPI	I
QPI1_DRX_DP[19]	G55	Intel QPI	I
QPI1_DRX_DP[2]	BC57	Intel QPI	I
QPI1_DRX_DP[3]	BA57	Intel QPI	I
QPI1_DRX_DP[4]	AW57	Intel QPI	I
QPI1_DRX_DP[5]	AU57	Intel QPI	I
QPI1_DRX_DP[6]	AR57	Intel QPI	I
QPI1_DRX_DP[7]	AN57	Intel QPI	I
QPI1_DRX_DP[8]	AL57	Intel QPI	I
QPI1_DRX_DP[9]	AJ57	Intel QPI	I
QPI1_DTX_DN[0]	BK52	Intel QPI	O
QPI1_DTX_DN[1]	BH52	Intel QPI	O
QPI1_DTX_DN[10]	AL49	Intel QPI	O
QPI1_DTX_DN[11]	AJ49	Intel QPI	O
QPI1_DTX_DN[12]	AG49	Intel QPI	O
QPI1_DTX_DN[13]	AE49	Intel QPI	O
QPI1_DTX_DN[14]	AC49	Intel QPI	O
QPI1_DTX_DN[15]	AA49	Intel QPI	O
QPI1_DTX_DN[16]	W49	Intel QPI	O
QPI1_DTX_DN[17]	U49	Intel QPI	O
QPI1_DTX_DN[18]	R49	Intel QPI	O
QPI1_DTX_DN[19]	N49	Intel QPI	O
QPI1_DTX_DN[2]	BF52	Intel QPI	O
QPI1_DTX_DN[3]	BD52	Intel QPI	O
QPI1_DTX_DN[4]	BB52	Intel QPI	O
QPI1_DTX_DN[5]	AY52	Intel QPI	O
QPI1_DTX_DN[6]	AV52	Intel QPI	O
QPI1_DTX_DN[7]	AT52	Intel QPI	O
QPI1_DTX_DN[8]	AP52	Intel QPI	O
QPI1_DTX_DN[9]	AM52	Intel QPI	O
QPI1_DTX_DP[0]	BL51	Intel QPI	O
QPI1_DTX_DP[1]	BJ51	Intel QPI	O
QPI1_DTX_DP[10]	AM48	Intel QPI	O
QPI1_DTX_DP[11]	AK48	Intel QPI	O
QPI1_DTX_DP[12]	AH48	Intel QPI	O
QPI1_DTX_DP[13]	AF48	Intel QPI	O
QPI1_DTX_DP[14]	AD48	Intel QPI	O
QPI1_DTX_DP[15]	AB48	Intel QPI	O
QPI1_DTX_DP[16]	Y48	Intel QPI	O
QPI1_DTX_DP[17]	V48	Intel QPI	O
QPI1_DTX_DP[18]	T48	Intel QPI	O

Table 7-1. Land Name (Sheet 10 of 50)

Land Name	Land No.	Buffer Type	Direction
QPI1_DTX_DP[19]	P48	Intel QPI	O
QPI1_DTX_DP[2]	BG51	Intel QPI	O
QPI1_DTX_DP[3]	BE51	Intel QPI	O
QPI1_DTX_DP[4]	BC51	Intel QPI	O
QPI1_DTX_DP[5]	BA51	Intel QPI	O
QPI1_DTX_DP[6]	AW51	Intel QPI	O
QPI1_DTX_DP[7]	AU51	Intel QPI	O
QPI1_DTX_DP[8]	AR51	Intel QPI	O
QPI1_DTX_DP[9]	AN51	Intel QPI	O
QPI2_CLKRX_DN	AF2	Intel QPI	I
QPI2_CLKRX_DP	AG1	Intel QPI	I
QPI2_CLKTX_DP	AE7	Intel QPI	O
QPI2_CLKTX_DN	AF6	Intel QPI	O
QPI2_DRX_DN[0]	F4	Intel QPI	I
QPI2_DRX_DN[1]	H4	Intel QPI	I
QPI2_DRX_DN[10]	AH2	Intel QPI	I
QPI2_DRX_DN[11]	AK2	Intel QPI	I
QPI2_DRX_DN[12]	AM2	Intel QPI	I
QPI2_DRX_DN[13]	AP2	Intel QPI	I
QPI2_DRX_DN[14]	AT2	Intel QPI	I
QPI2_DRX_DN[15]	AV2	Intel QPI	I
QPI2_DRX_DN[16]	AY2	Intel QPI	I
QPI2_DRX_DN[17]	BB2	Intel QPI	I
QPI2_DRX_DN[18]	BD2	Intel QPI	I
QPI2_DRX_DN[19]	BF2	Intel QPI	I
QPI2_DRX_DN[2]	H2	Intel QPI	I
QPI2_DRX_DN[3]	K4	Intel QPI	I
QPI2_DRX_DN[4]	M4	Intel QPI	I
QPI2_DRX_DN[5]	P4	Intel QPI	I
QPI2_DRX_DN[6]	T4	Intel QPI	I
QPI2_DRX_DN[7]	V4	Intel QPI	I
QPI2_DRX_DN[8]	Y4	Intel QPI	I
QPI2_DRX_DN[9]	AB4	Intel QPI	I
QPI2_DRX_DP[0]	G3	Intel QPI	I
QPI2_DRX_DP[1]	J3	Intel QPI	I
QPI2_DRX_DP[10]	AJ1	Intel QPI	I
QPI2_DRX_DP[11]	AL1	Intel QPI	I
QPI2_DRX_DP[12]	AN1	Intel QPI	I
QPI2_DRX_DP[13]	AR1	Intel QPI	I
QPI2_DRX_DP[14]	AU1	Intel QPI	I
QPI2_DRX_DP[15]	AW1	Intel QPI	I

Table 7-1. Land Name (Sheet 11 of 50)

Land Name	Land No.	Buffer Type	Direction
QPI2_DRX_DP[16]	BA1	Intel QPI	I
QPI2_DRX_DP[17]	BC1	Intel QPI	I
QPI2_DRX_DP[18]	BE1	Intel QPI	I
QPI2_DRX_DP[19]	BG1	Intel QPI	I
QPI2_DRX_DP[2]	J1	Intel QPI	I
QPI2_DRX_DP[3]	L3	Intel QPI	I
QPI2_DRX_DP[4]	N3	Intel QPI	I
QPI2_DRX_DP[5]	R3	Intel QPI	I
QPI2_DRX_DP[6]	U3	Intel QPI	I
QPI2_DRX_DP[7]	W3	Intel QPI	I
QPI2_DRX_DP[8]	AA3	Intel QPI	I
QPI2_DRX_DP[9]	AC3	Intel QPI	I
QPI2_DTX_DN[0]	E7	Intel QPI	O
QPI2_DTX_DN[1]	G7	Intel QPI	O
QPI2_DTX_DN[10]	AG5	Intel QPI	O
QPI2_DTX_DN[11]	AJ5	Intel QPI	O
QPI2_DTX_DN[12]	AL5	Intel QPI	O
QPI2_DTX_DN[13]	AN5	Intel QPI	O
QPI2_DTX_DN[14]	AR5	Intel QPI	O
QPI2_DTX_DN[15]	AU5	Intel QPI	O
QPI2_DTX_DN[16]	AW5	Intel QPI	O
QPI2_DTX_DN[17]	BA5	Intel QPI	O
QPI2_DTX_DN[18]	BC5	Intel QPI	O
QPI2_DTX_DN[19]	BE5	Intel QPI	O
QPI2_DTX_DN[2]	J7	Intel QPI	O
QPI2_DTX_DN[3]	L7	Intel QPI	O
QPI2_DTX_DN[4]	N7	Intel QPI	O
QPI2_DTX_DN[5]	R7	Intel QPI	O
QPI2_DTX_DN[6]	U7	Intel QPI	O
QPI2_DTX_DN[7]	W7	Intel QPI	O
QPI2_DTX_DN[8]	AA7	Intel QPI	O
QPI2_DTX_DN[9]	AC7	Intel QPI	O
QPI2_DTX_DP[0]	F6	Intel QPI	O
QPI2_DTX_DP[1]	H6	Intel QPI	O
QPI2_DTX_DP[10]	AH4	Intel QPI	O
QPI2_DTX_DP[11]	AK4	Intel QPI	O
QPI2_DTX_DP[12]	AM4	Intel QPI	O
QPI2_DTX_DP[13]	AP4	Intel QPI	O
QPI2_DTX_DP[14]	AT4	Intel QPI	O
QPI2_DTX_DP[15]	AV4	Intel QPI	O
QPI2_DTX_DP[16]	AY4	Intel QPI	O

Table 7-1. Land Name (Sheet 12 of 50)

Land Name	Land No.	Buffer Type	Direction
QPI2_DTX_DP[17]	BB4	Intel QPI	O
QPI2_DTX_DP[18]	BD4	Intel QPI	O
QPI2_DTX_DP[19]	BF4	Intel QPI	O
QPI2_DTX_DP[2]	K6	Intel QPI	O
QPI2_DTX_DP[3]	M6	Intel QPI	O
QPI2_DTX_DP[4]	P6	Intel QPI	O
QPI2_DTX_DP[5]	T6	Intel QPI	O
QPI2_DTX_DP[6]	V6	Intel QPI	O
QPI2_DTX_DP[7]	Y6	Intel QPI	O
QPI2_DTX_DP[8]	AB6	Intel QPI	O
QPI2_DTX_DP[9]	AD6	Intel QPI	O
RESET_N	AF38	CMOS	I
RSVD	AC51		
RSVD	AE37		
RSVD	DC3		
RSVD	DB2		
RSVD	DC55		
RSVD	DF52		
RSVD	DE53		
RSVD	CW1		
RSVD	DB4		
RSVD	BY44		
RSVD	CT46		
RSVD	BR45		
RSVD	DC39		
RSVD	DA3		
RSVD	DD6		
RSVD	CU1		
RSVD	DC5		
RSVD	BD46		
RSVD	BF48		
RSVD	AR49		
RSVD	AR47		
RSVD	BD48		
RSVD	BE49		
RSVD	BB48		
RSVD	BA49		
RSVD	BE47		
RSVD	BB46		
RSVD	AM46		
RSVD	AV46		

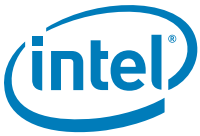

Table 7-1. Land Name (Sheet 13 of 50)

Land Name	Land No.	Buffer Type	Direction
RSVD	AP46		
RSVD	AT46		
RSVD	AT48		
RSVD	AV48		
RSVD	BA47		
RSVD	AU49		
RSVD	AW47		
RSVD	AW49		
RSVD	B6		
RSVD	A5		
RSVD	E3		
RSVD	F2		
RSVD	A7		
RSVD	C3		
RSVD	D2		
RSVD	H58		
RSVD	F58		
RSVD	G37		
RSVD	J37		
RSVD	B52		
RSVD	J53		
RSVD	K52		
RSVD	C5		
RSVD	D4		
RSVD	AC13		
RSVD	AB14		
RSVD	BM50		
RSVD	W47		
RSVD	AF44		
RSVD	AD44		
RSVD	DA57		
RSVD	DB56		
SAFE_MODE_BOOT	BF56	CMOS	I
SKTOCC_N	BJ3		O
SM_WP	AP10		I
SMBCLK	AL11		I/O
SMBDAT	AM10		I/O
SOCKET_ID[0]	AK56	CMOS	I
SOCKET_ID[1]	AB54	CMOS	I
SOCKET_ID[2]	V54	CMOS	I
SVIDALERT_N	AU11	CMOS	I

Table 7-1. Land Name (Sheet 14 of 50)

Land Name	Land No.	Buffer Type	Direction
SVIDCLK	AV10	Open Drain	O
SVIDDATA	AW11	Open Drain	I/O
SVID_IDLE_N	CF36	CMOS	O
TCK	BG49	CMOS	I
TDI	BF50	CMOS	I
TDO	AJ47	Open Drain	O
TEST_0	CU35		
TEST_1	DE55		
TEST_2	BW53		
TEST_3	CW15		
TEST_4	BV10		
TEST_5	BT14		
TEST_6	BY2		
TEST_7	CV58		
TEST_8	AF40		
TEST_9	AG51		
TEST_10	DB54		
TEST_11	AP6		
TEST_12	BD6		
TEST_13	BA3		
THERMTRIP_N	BF46	CMOS	O
TMS	AH50	CMOS	I
TRST_N	AK46	CMOS	I
TSC_SYNC	M54	Open Drain	I/O
TXT_AGENT	AK10	CMOS	I
TXT_PLTEN	AJ9	CMOS	I
VCC	A19	PWR	
VCC	A21	PWR	
VCC	A23	PWR	
VCC	A33	PWR	
VCC	AA21	PWR	
VCC	AA25	PWR	
VCC	AA27	PWR	
VCC	AA31	PWR	
VCC	AA33	PWR	
VCC	AB20	PWR	
VCC	AB22	PWR	
VCC	AB26	PWR	
VCC	AB28	PWR	
VCC	AB32	PWR	
VCC	AC21	PWR	

Table 7-1. Land Name (Sheet 15 of 50)

Land Name	Land No.	Buffer Type	Direction
VCC	AC25	PWR	
VCC	AC27	PWR	
VCC	AC31	PWR	
VCC	AC33	PWR	
VCC	AD20	PWR	
VCC	AD22	PWR	
VCC	AD26	PWR	
VCC	AD28	PWR	
VCC	AD32	PWR	
VCC	AE13	PWR	
VCC	AE15	PWR	
VCC	AE17	PWR	
VCC	AE21	PWR	
VCC	AE25	PWR	
VCC	AE27	PWR	
VCC	AE31	PWR	
VCC	AE33	PWR	
VCC	AF12	PWR	
VCC	AF14	PWR	
VCC	AF16	PWR	
VCC	AF20	PWR	
VCC	AF22	PWR	
VCC	AF26	PWR	
VCC	AF28	PWR	
VCC	AF32	PWR	
VCC	AG13	PWR	
VCC	AG15	PWR	
VCC	AG17	PWR	
VCC	AG21	PWR	
VCC	AG25	PWR	
VCC	AG27	PWR	
VCC	AG31	PWR	
VCC	AG33	PWR	
VCC	AG37	PWR	
VCC	AG39	PWR	
VCC	AG41	PWR	
VCC	AH12	PWR	
VCC	AH14	PWR	
VCC	AH16	PWR	
VCC	AH42	PWR	
VCC	AH44	PWR	

Table 7-1. Land Name (Sheet 16 of 50)

Land Name	Land No.	Buffer Type	Direction
VCC	AJ13	PWR	
VCC	AJ15	PWR	
VCC	AJ17	PWR	
VCC	AJ43	PWR	
VCC	AJ45	PWR	
VCC	AK12	PWR	
VCC	AK14	PWR	
VCC	AK16	PWR	
VCC	AK42	PWR	
VCC	AK44	PWR	
VCC	AL43	PWR	
VCC	AL45	PWR	
VCC	AM42	PWR	
VCC	AM44	PWR	
VCC	AN13	PWR	
VCC	AN15	PWR	
VCC	AN17	PWR	
VCC	AP12	PWR	
VCC	AP14	PWR	
VCC	AP16	PWR	
VCC	AR13	PWR	
VCC	AR15	PWR	
VCC	AR17	PWR	
VCC	AR43	PWR	
VCC	AR45	PWR	
VCC	AT12	PWR	
VCC	AT14	PWR	
VCC	AT16	PWR	
VCC	AT42	PWR	
VCC	AT44	PWR	
VCC	AU13	PWR	
VCC	AU15	PWR	
VCC	AU17	PWR	
VCC	AU43	PWR	
VCC	AU45	PWR	
VCC	AV12	PWR	
VCC	AV14	PWR	
VCC	AV16	PWR	
VCC	AV42	PWR	
VCC	AV44	PWR	
VCC	AW43	PWR	

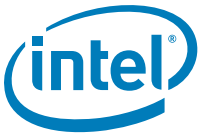

Table 7-1. Land Name (Sheet 17 of 50)

Land Name	Land No.	Buffer Type	Direction
VCC	AW45	PWR	
VCC	B20	PWR	
VCC	B22	PWR	
VCC	B24	PWR	
VCC	B32	PWR	
VCC	BA13	PWR	
VCC	BA15	PWR	
VCC	BA17	PWR	
VCC	BB12	PWR	
VCC	BB14	PWR	
VCC	BB16	PWR	
VCC	BB42	PWR	
VCC	BB44	PWR	
VCC	BC13	PWR	
VCC	BC15	PWR	
VCC	BC17	PWR	
VCC	BC43	PWR	
VCC	BC45	PWR	
VCC	BD12	PWR	
VCC	BD14	PWR	
VCC	BD16	PWR	
VCC	BD42	PWR	
VCC	BD44	PWR	
VCC	BE13	PWR	
VCC	BE15	PWR	
VCC	BE17	PWR	
VCC	BE43	PWR	
VCC	BE45	PWR	
VCC	BF12	PWR	
VCC	BF14	PWR	
VCC	BF16	PWR	
VCC	BF42	PWR	
VCC	BF44	PWR	
VCC	C19	PWR	
VCC	C21	PWR	
VCC	C25	PWR	
VCC	C33	PWR	
VCC	D20	PWR	
VCC	D22	PWR	
VCC	D26	PWR	
VCC	D32	PWR	

Table 7-1. Land Name (Sheet 18 of 50)

Land Name	Land No.	Buffer Type	Direction
VCC	E21	PWR	
VCC	E25	PWR	
VCC	E27	PWR	
VCC	E31	PWR	
VCC	E33	PWR	
VCC	F20	PWR	
VCC	F22	PWR	
VCC	F26	PWR	
VCC	F28	PWR	
VCC	F32	PWR	
VCC	G21	PWR	
VCC	G25	PWR	
VCC	G27	PWR	
VCC	G31	PWR	
VCC	G33	PWR	
VCC	H20	PWR	
VCC	H22	PWR	
VCC	H26	PWR	
VCC	H28	PWR	
VCC	H32	PWR	
VCC	J21	PWR	
VCC	J25	PWR	
VCC	J27	PWR	
VCC	J31	PWR	
VCC	J33	PWR	
VCC	K20	PWR	
VCC	K22	PWR	
VCC	K26	PWR	
VCC	K28	PWR	
VCC	K32	PWR	
VCC	L21	PWR	
VCC	L25	PWR	
VCC	L27	PWR	
VCC	L31	PWR	
VCC	L33	PWR	
VCC	M20	PWR	
VCC	M22	PWR	
VCC	M26	PWR	
VCC	M28	PWR	
VCC	M32	PWR	
VCC	N21	PWR	

Table 7-1. Land Name (Sheet 19 of 50)

Land Name	Land No.	Buffer Type	Direction
VCC	N25	PWR	
VCC	N27	PWR	
VCC	N31	PWR	
VCC	N33	PWR	
VCC	P20	PWR	
VCC	P22	PWR	
VCC	P26	PWR	
VCC	P28	PWR	
VCC	P32	PWR	
VCC	R21	PWR	
VCC	R25	PWR	
VCC	R27	PWR	
VCC	R31	PWR	
VCC	R33	PWR	
VCC	T20	PWR	
VCC	T22	PWR	
VCC	T26	PWR	
VCC	T28	PWR	
VCC	T32	PWR	
VCC	U21	PWR	
VCC	U25	PWR	
VCC	U27	PWR	
VCC	U31	PWR	
VCC	U33	PWR	
VCC	V20	PWR	
VCC	V22	PWR	
VCC	V26	PWR	
VCC	V28	PWR	
VCC	V32	PWR	
VCC	W21	PWR	
VCC	W25	PWR	
VCC	W27	PWR	
VCC	W31	PWR	
VCC	W33	PWR	
VCC	Y20	PWR	
VCC	Y22	PWR	
VCC	Y26	PWR	
VCC	Y28	PWR	
VCC	Y32	PWR	
VCC_SENSE	AF42		O
VCC33	BE11	PWR	

Table 7-1. Land Name (Sheet 20 of 50)

Land Name	Land No.	Buffer Type	Direction
VCCIO_IN	AN9		
VTTA	BP42	PWR	
VTTA	BT42	PWR	
VTTA	BV42	PWR	
VTT_SENSE	J51		O
VTTA	AA15	PWR	
VTTA	AB12	PWR	
VTTA	AC47	PWR	
VTTA	H54	PWR	
VTTA	M12	PWR	
VTTA	M42	PWR	
VTTA	N15	PWR	
VTTA	N47	PWR	
VTTA	P50	PWR	
VTTA	T12	PWR	
VTTA	U51	PWR	
VTTA	V36	PWR	
VTTA	V42	PWR	
VTTA	V44	PWR	
VTTA	V46	PWR	
VTTA	Y50	PWR	
VTTQ	AC9	PWR	
VTTQ	AH56	PWR	
VTTQ	AJ53	PWR	
VTTQ	AU53	PWR	
VTTQ	N9	PWR	
VTTQ	W9	PWR	
VCCPECI	AD10	PWR	
VTTA	A13	PWR	
VTTA	C15	PWR	
VTTA	BY24	PWR	
VTTA	D42	PWR	
VTTA	E9	PWR	
VTTA	F12	PWR	
VTTA	F36	PWR	
VTTA	F38	PWR	
VTTA	F42	PWR	
VTTA	G47	PWR	
VTTA	H50	PWR	
VTTA	J47	PWR	
VTTQ	BY30	PWR	

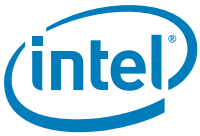

Table 7-1. Land Name (Sheet 21 of 50)

Land Name	Land No.	Buffer Type	Direction
VTTQ	BY36	PWR	
VTTQ	BY42	PWR	
VTTQ	J15	PWR	
VTTQ	J9	PWR	
VTTQ	K14	PWR	
VSA	AJ3	PWR	
VSA	AJ7	PWR	
VSA	AK6	PWR	
VSA	AU3	PWR	
VSA	AV8	PWR	
VSA	AW9	PWR	
VSA	AY10	PWR	
VSA	AY6	PWR	
VSA	BE3	PWR	
VSA	BJ17	PWR	
VSA	BL17	PWR	
VSA	BN17	PWR	
VSA_SENSE	BG5		O
VMSE_PWR_OK	DC19	SMI2	I
VMSE0_CLK_N	BM44	SMI2	O
VMSE0_CLK_P	BN45	SMI2	O
VMSE0_CMD[0]	BH44	SMI2	O
VMSE0_CMD[1]	BV46	SMI2	O
VMSE0_CMD[10]	BM48	SMI2	O
VMSE0_CMD[11]	BL47	SMI2	O
VMSE0_CMD[12]	BJ49	SMI2	O
VMSE0_CMD[13]	BM46	SMI2	O
VMSE0_CMD[14]	BL49	SMI2	O
VMSE0_CMD[15]	BH46	SMI2	O
VMSE0_CMD[16]	BJ47	SMI2	O
VMSE0_CMD[2]	BV44	SMI2	O
VMSE0_CMD[3]	BJ45	SMI2	O
VMSE0_CMD[4]	BJ43	SMI2	O
VMSE0_CMD[5]	BT46	SMI2	O
VMSE0_CMD[6]	BT44	SMI2	O
VMSE0_CMD[7]	BW45	SMI2	O
VMSE0_CMD[8]	BL43	SMI2	O
VMSE0_CMD[9]	BL45	SMI2	O
VMSE0_DQ[0]	DE47	SMI2	I/O
VMSE0_DQ[1]	DC49	SMI2	I/O
VMSE0_DQ[10]	CW51	SMI2	I/O

Table 7-1. Land Name (Sheet 22 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE0_DQ[11]	CU51	SMI2	I/O
VMSE0_DQ[12]	CU47	SMI2	I/O
VMSE0_DQ[13]	CY48	SMI2	I/O
VMSE0_DQ[14]	CT50	SMI2	I/O
VMSE0_DQ[15]	CY50	SMI2	I/O
VMSE0_DQ[16]	CU53	SMI2	I/O
VMSE0_DQ[17]	CY54	SMI2	I/O
VMSE0_DQ[18]	CU57	SMI2	I/O
VMSE0_DQ[19]	CW57	SMI2	I/O
VMSE0_DQ[2]	DC51	SMI2	I/O
VMSE0_DQ[20]	CW53	SMI2	I/O
VMSE0_DQ[21]	CT54	SMI2	I/O
VMSE0_DQ[22]	CY56	SMI2	I/O
VMSE0_DQ[23]	CT56	SMI2	I/O
VMSE0_DQ[24]	CH54	SMI2	I/O
VMSE0_DQ[25]	CH56	SMI2	I/O
VMSE0_DQ[26]	CM56	SMI2	I/O
VMSE0_DQ[27]	CP58	SMI2	I/O
VMSE0_DQ[28]	CG55	SMI2	I/O
VMSE0_DQ[29]	CK54	SMI2	I/O
VMSE0_DQ[3]	DC53	SMI2	I/O
VMSE0_DQ[30]	CN57	SMI2	I/O
VMSE0_DQ[31]	CN55	SMI2	I/O
VMSE0_DQ[32]	CN49	SMI2	I/O
VMSE0_DQ[33]	CM52	SMI2	I/O
VMSE0_DQ[34]	CK48	SMI2	I/O
VMSE0_DQ[35]	CJ49	SMI2	I/O
VMSE0_DQ[36]	CN51	SMI2	I/O
VMSE0_DQ[37]	CM48	SMI2	I/O
VMSE0_DQ[38]	CJ51	SMI2	I/O
VMSE0_DQ[39]	CK52	SMI2	I/O
VMSE0_DQ[4]	DF48	SMI2	I/O
VMSE0_DQ[40]	CF50	SMI2	I/O
VMSE0_DQ[41]	CE53	SMI2	I/O
VMSE0_DQ[42]	CB52	SMI2	I/O
VMSE0_DQ[43]	CB50	SMI2	I/O
VMSE0_DQ[44]	CF52	SMI2	I/O
VMSE0_DQ[45]	CE49	SMI2	I/O
VMSE0_DQ[46]	CC49	SMI2	I/O
VMSE0_DQ[47]	CC53	SMI2	I/O
VMSE0_DQ[48]	BV48	SMI2	I/O

Table 7-1. Land Name (Sheet 23 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE0_DQ[49]	BR49	SMI2	I/O
VMSE0_DQ[5]	DC47	SMI2	I/O
VMSE0_DQ[50]	BV52	SMI2	I/O
VMSE0_DQ[51]	BR51	SMI2	I/O
VMSE0_DQ[52]	BW49	SMI2	I/O
VMSE0_DQ[53]	BT48	SMI2	I/O
VMSE0_DQ[54]	BT52	SMI2	I/O
VMSE0_DQ[55]	BW51	SMI2	I/O
VMSE0_DQ[56]	BT54	SMI2	I/O
VMSE0_DQ[57]	BM54	SMI2	I/O
VMSE0_DQ[58]	BN57	SMI2	I/O
VMSE0_DQ[59]	BK58	SMI2	I/O
VMSE0_DQ[6]	DD52	SMI2	I/O
VMSE0_DQ[60]	BN53	SMI2	I/O
VMSE0_DQ[61]	BR55	SMI2	I/O
VMSE0_DQ[62]	BL57	SMI2	I/O
VMSE0_DQ[63]	BP58	SMI2	I/O
VMSE0_DQ[7]	DF50	SMI2	I/O
VMSE0_DQ[8]	CW47	SMI2	I/O
VMSE0_DQ[9]	CT48	SMI2	I/O
VMSE0_DQS_N[0]	DD50	SMI2	I/O
VMSE0_DQS_N[1]	CW49	SMI2	I/O
VMSE0_DQS_N[2]	CU55	SMI2	I/O
VMSE0_DQS_N[3]	CM54	SMI2	I/O
VMSE0_DQS_N[4]	CM50	SMI2	I/O
VMSE0_DQS_N[5]	CE51	SMI2	I/O
VMSE0_DQS_N[6]	BT50	SMI2	I/O
VMSE0_DQS_N[7]	BP56	SMI2	I/O
VMSE0_DQS_N[8]	BV56	SMI2	I/O
VMSE0_DQS_P[0]	DE49	SMI2	I/O
VMSE0_DQS_P[1]	CU49	SMI2	I/O
VMSE0_DQS_P[2]	CW55	SMI2	I/O
VMSE0_DQS_P[3]	CL55	SMI2	I/O
VMSE0_DQS_P[4]	CK50	SMI2	I/O
VMSE0_DQS_P[5]	CC51	SMI2	I/O
VMSE0_DQS_P[6]	BV50	SMI2	I/O
VMSE0_DQS_P[7]	BM56	SMI2	I/O
VMSE0_DQS_P[8]	BY56	SMI2	I/O
VMSE0_ECC[0]	CD56	SMI2	I/O
VMSE0_ECC[1]	BW55	SMI2	I/O
VMSE0_ECC[2]	BY58	SMI2	I/O

Table 7-1. Land Name (Sheet 24 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE0_ECC[3]	BU57	SMI2	I/O
VMSE0_ECC[4]	BY54	SMI2	I/O
VMSE0_ECC[5]	CC55	SMI2	I/O
VMSE0_ECC[6]	BV58	SMI2	I/O
VMSE0_ECC[7]	CA57	SMI2	I/O
VMSE0_ERR_N	BY48	SMI2	I/O
VMSE1_CLK_N	CY40	SMI2	O
VMSE1_CLK_P	CW41	SMI2	O
VMSE1_CMD[0]	DA39	SMI2	O
VMSE1_CMD[1]	CW37	SMI2	O
VMSE1_CMD[10]	CY44	SMI2	O
VMSE1_CMD[11]	CT44	SMI2	O
VMSE1_CMD[12]	CW45	SMI2	O
VMSE1_CMD[13]	CT42	SMI2	O
VMSE1_CMD[14]	CU45	SMI2	O
VMSE1_CMD[15]	CY42	SMI2	O
VMSE1_CMD[16]	CW43	SMI2	O
VMSE1_CMD[2]	CT36	SMI2	O
VMSE1_CMD[3]	CU39	SMI2	O
VMSE1_CMD[4]	CT38	SMI2	O
VMSE1_CMD[5]	CU37	SMI2	O
VMSE1_CMD[6]	CT40	SMI2	O
VMSE1_CMD[7]	CY36	SMI2	O
VMSE1_CMD[8]	CY38	SMI2	O
VMSE1_CMD[9]	CR41	SMI2	O
VMSE1_DQ[0]	CC31	SMI2	I/O
VMSE1_DQ[1]	CF32	SMI2	I/O
VMSE1_DQ[10]	CJ33	SMI2	I/O
VMSE1_DQ[11]	CK34	SMI2	I/O
VMSE1_DQ[12]	CN31	SMI2	I/O
VMSE1_DQ[13]	CK30	SMI2	I/O
VMSE1_DQ[14]	CM34	SMI2	I/O
VMSE1_DQ[15]	CN33	SMI2	I/O
VMSE1_DQ[16]	CV30	SMI2	I/O
VMSE1_DQ[17]	DA31	SMI2	I/O
VMSE1_DQ[18]	CV34	SMI2	I/O
VMSE1_DQ[19]	CY34	SMI2	I/O
VMSE1_DQ[2]	CC35	SMI2	I/O
VMSE1_DQ[20]	CY30	SMI2	I/O
VMSE1_DQ[21]	CU31	SMI2	I/O
VMSE1_DQ[22]	DA33	SMI2	I/O

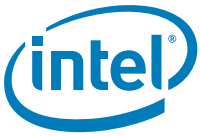

Table 7-1. Land Name (Sheet 25 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE1_DQ[23]	CU33	SMI2	I/O
VMSE1_DQ[24]	DD32	SMI2	I/O
VMSE1_DQ[25]	DC35	SMI2	I/O
VMSE1_DQ[26]	DC37	SMI2	I/O
VMSE1_DQ[27]	DF38	SMI2	I/O
VMSE1_DQ[28]	DF34	SMI2	I/O
VMSE1_DQ[29]	DE33	SMI2	I/O
VMSE1_DQ[3]	CE35	SMI2	I/O
VMSE1_DQ[30]	DD38	SMI2	I/O
VMSE1_DQ[31]	DF36	SMI2	I/O
VMSE1_DQ[32]	CK36	SMI2	I/O
VMSE1_DQ[33]	CN37	SMI2	I/O
VMSE1_DQ[34]	CK40	SMI2	I/O
VMSE1_DQ[35]	CM40	SMI2	I/O
VMSE1_DQ[36]	CM36	SMI2	I/O
VMSE1_DQ[37]	CJ37	SMI2	I/O
VMSE1_DQ[38]	CN39	SMI2	I/O
VMSE1_DQ[39]	CJ39	SMI2	I/O
VMSE1_DQ[4]	CE31	SMI2	I/O
VMSE1_DQ[40]	CC37	SMI2	I/O
VMSE1_DQ[41]	CF38	SMI2	I/O
VMSE1_DQ[42]	CC41	SMI2	I/O
VMSE1_DQ[43]	CE41	SMI2	I/O
VMSE1_DQ[44]	CE37	SMI2	I/O
VMSE1_DQ[45]	CB38	SMI2	I/O
VMSE1_DQ[46]	CF40	SMI2	I/O
VMSE1_DQ[47]	CB40	SMI2	I/O
VMSE1_DQ[48]	CK42	SMI2	I/O
VMSE1_DQ[49]	CN43	SMI2	I/O
VMSE1_DQ[5]	CB32	SMI2	I/O
VMSE1_DQ[50]	CK46	SMI2	I/O
VMSE1_DQ[51]	CM46	SMI2	I/O
VMSE1_DQ[52]	CM42	SMI2	I/O
VMSE1_DQ[53]	CJ43	SMI2	I/O
VMSE1_DQ[54]	CN45	SMI2	I/O
VMSE1_DQ[55]	CJ45	SMI2	I/O
VMSE1_DQ[56]	CE43	SMI2	I/O
VMSE1_DQ[57]	CB44	SMI2	I/O
VMSE1_DQ[58]	CE47	SMI2	I/O
VMSE1_DQ[59]	CC47	SMI2	I/O
VMSE1_DQ[6]	CF34	SMI2	I/O

Table 7-1. Land Name (Sheet 26 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE1_DQ[60]	CC43	SMI2	I/O
VMSE1_DQ[61]	CF44	SMI2	I/O
VMSE1_DQ[62]	CB46	SMI2	I/O
VMSE1_DQ[63]	CF46	SMI2	I/O
VMSE1_DQ[7]	CB34	SMI2	I/O
VMSE1_DQ[8]	CM30	SMI2	I/O
VMSE1_DQ[9]	CJ31	SMI2	I/O
VMSE1_DQS_N[0]	CE33	SMI2	I/O
VMSE1_DQS_N[1]	CM32	SMI2	I/O
VMSE1_DQS_N[2]	CV32	SMI2	I/O
VMSE1_DQS_N[3]	DE35	SMI2	I/O
VMSE1_DQS_N[4]	CK38	SMI2	I/O
VMSE1_DQS_N[5]	CC39	SMI2	I/O
VMSE1_DQS_N[6]	CM44	SMI2	I/O
VMSE1_DQS_N[7]	CE45	SMI2	I/O
VMSE1_DQS_N[8]	DE43	SMI2	I/O
VMSE1_DQS_P[0]	CC33	SMI2	I/O
VMSE1_DQS_P[1]	CK32	SMI2	I/O
VMSE1_DQS_P[2]	CY32	SMI2	I/O
VMSE1_DQS_P[3]	DD36	SMI2	I/O
VMSE1_DQS_P[4]	CM38	SMI2	I/O
VMSE1_DQS_P[5]	CE39	SMI2	I/O
VMSE1_DQS_P[6]	CK44	SMI2	I/O
VMSE1_DQS_P[7]	CC45	SMI2	I/O
VMSE1_DQS_P[8]	DD42	SMI2	I/O
VMSE1_ECC[0]	DF40	SMI2	I/O
VMSE1_ECC[1]	DF42	SMI2	I/O
VMSE1_ECC[2]	DF44	SMI2	I/O
VMSE1_ECC[3]	DE45	SMI2	I/O
VMSE1_ECC[4]	DC41	SMI2	I/O
VMSE1_ECC[5]	DD40	SMI2	I/O
VMSE1_ECC[6]	DC45	SMI2	I/O
VMSE1_ECC[7]	DC43	SMI2	I/O
VMSE1_ERR_N	CR35	SMI2	I/O
VMSE2_CLK_N	CY18	SMI2	O
VMSE2_CLK_P	CV18	SMI2	O
VMSE2_CMD[0]	CW17	SMI2	O
VMSE2_CMD[1]	CT14	SMI2	O
VMSE2_CMD[10]	CT22	SMI2	O
VMSE2_CMD[11]	CU21	SMI2	O
VMSE2_CMD[12]	CR23	SMI2	O

Table 7-1. Land Name (Sheet 27 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE2_CMD[13]	CU19	SMI2	O
VMSE2_CMD[14]	CY22	SMI2	O
VMSE2_CMD[15]	CY20	SMI2	O
VMSE2_CMD[16]	CT20	SMI2	O
VMSE2_CMD[2]	CW13	SMI2	O
VMSE2_CMD[3]	CR17	SMI2	O
VMSE2_CMD[4]	CT16	SMI2	O
VMSE2_CMD[5]	CU15	SMI2	O
VMSE2_CMD[6]	CT18	SMI2	O
VMSE2_CMD[7]	CY14	SMI2	O
VMSE2_CMD[8]	CY16	SMI2	O
VMSE2_CMD[9]	DA19	SMI2	O
VMSE2_DQ[0]	CK12	SMI2	I/O
VMSE2_DQ[1]	CN13	SMI2	I/O
VMSE2_DQ[10]	CW11	SMI2	I/O
VMSE2_DQ[11]	CR11	SMI2	I/O
VMSE2_DQ[12]	CU7	SMI2	I/O
VMSE2_DQ[13]	CY8	SMI2	I/O
VMSE2_DQ[14]	CT10	SMI2	I/O
VMSE2_DQ[15]	CV10	SMI2	I/O
VMSE2_DQ[16]	CK18	SMI2	I/O
VMSE2_DQ[17]	CN19	SMI2	I/O
VMSE2_DQ[18]	CK22	SMI2	I/O
VMSE2_DQ[19]	CM22	SMI2	I/O
VMSE2_DQ[2]	CK16	SMI2	I/O
VMSE2_DQ[20]	CM18	SMI2	I/O
VMSE2_DQ[21]	CJ19	SMI2	I/O
VMSE2_DQ[22]	CN21	SMI2	I/O
VMSE2_DQ[23]	CJ21	SMI2	I/O
VMSE2_DQ[24]	DE13	SMI2	I/O
VMSE2_DQ[25]	DC15	SMI2	I/O
VMSE2_DQ[26]	DC17	SMI2	I/O
VMSE2_DQ[27]	DF18	SMI2	I/O
VMSE2_DQ[28]	DF14	SMI2	I/O
VMSE2_DQ[29]	DC13	SMI2	I/O
VMSE2_DQ[3]	CM16	SMI2	I/O
VMSE2_DQ[30]	DD18	SMI2	I/O
VMSE2_DQ[31]	DF16	SMI2	I/O
VMSE2_DQ[32]	CC25	SMI2	I/O
VMSE2_DQ[33]	CF26	SMI2	I/O
VMSE2_DQ[34]	CF28	SMI2	I/O

Table 7-1. Land Name (Sheet 28 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE2_DQ[35]	CE29	SMI2	I/O
VMSE2_DQ[36]	CE25	SMI2	I/O
VMSE2_DQ[37]	CB26	SMI2	I/O
VMSE2_DQ[38]	CC29	SMI2	I/O
VMSE2_DQ[39]	CB28	SMI2	I/O
VMSE2_DQ[4]	CM12	SMI2	I/O
VMSE2_DQ[40]	CE19	SMI2	I/O
VMSE2_DQ[41]	CB20	SMI2	I/O
VMSE2_DQ[42]	CE23	SMI2	I/O
VMSE2_DQ[43]	CC23	SMI2	I/O
VMSE2_DQ[44]	CC19	SMI2	I/O
VMSE2_DQ[45]	CF20	SMI2	I/O
VMSE2_DQ[46]	CB22	SMI2	I/O
VMSE2_DQ[47]	CF22	SMI2	I/O
VMSE2_DQ[48]	CM24	SMI2	I/O
VMSE2_DQ[49]	CJ25	SMI2	I/O
VMSE2_DQ[5]	CJ13	SMI2	I/O
VMSE2_DQ[50]	CM28	SMI2	I/O
VMSE2_DQ[51]	CK28	SMI2	I/O
VMSE2_DQ[52]	CK24	SMI2	I/O
VMSE2_DQ[53]	CN25	SMI2	I/O
VMSE2_DQ[54]	CJ27	SMI2	I/O
VMSE2_DQ[55]	CN27	SMI2	I/O
VMSE2_DQ[56]	CY24	SMI2	I/O
VMSE2_DQ[57]	CU25	SMI2	I/O
VMSE2_DQ[58]	CU27	SMI2	I/O
VMSE2_DQ[59]	CV28	SMI2	I/O
VMSE2_DQ[6]	CN15	SMI2	I/O
VMSE2_DQ[60]	DA25	SMI2	I/O
VMSE2_DQ[61]	CV24	SMI2	I/O
VMSE2_DQ[62]	CY28	SMI2	I/O
VMSE2_DQ[63]	DA27	SMI2	I/O
VMSE2_DQ[7]	CJ15	SMI2	I/O
VMSE2_DQ[8]	CW7	SMI2	I/O
VMSE2_DQ[9]	CT8	SMI2	I/O
VMSE2_DQS_N[0]	CM14	SMI2	I/O
VMSE2_DQS_N[1]	CW9	SMI2	I/O
VMSE2_DQS_N[2]	CK20	SMI2	I/O
VMSE2_DQS_N[3]	DE15	SMI2	I/O
VMSE2_DQS_N[4]	CC27	SMI2	I/O
VMSE2_DQS_N[5]	CE21	SMI2	I/O

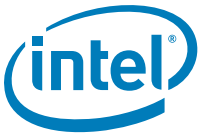

Table 7-1. Land Name (Sheet 29 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE2_DQS_N[6]	CK26	SMI2	I/O
VMSE2_DQS_N[7]	CY26	SMI2	I/O
VMSE2_DQS_N[8]	DE23	SMI2	I/O
VMSE2_DQS_P[0]	CK14	SMI2	I/O
VMSE2_DQS_P[1]	CU9	SMI2	I/O
VMSE2_DQS_P[2]	CM20	SMI2	I/O
VMSE2_DQS_P[3]	DD16	SMI2	I/O
VMSE2_DQS_P[4]	CE27	SMI2	I/O
VMSE2_DQS_P[5]	CC21	SMI2	I/O
VMSE2_DQS_P[6]	CM26	SMI2	I/O
VMSE2_DQS_P[7]	CV26	SMI2	I/O
VMSE2_DQS_P[8]	DD22	SMI2	I/O
VMSE2_ECC[0]	DF20	SMI2	I/O
VMSE2_ECC[1]	DF22	SMI2	I/O
VMSE2_ECC[2]	DF24	SMI2	I/O
VMSE2_ECC[3]	DD26	SMI2	I/O
VMSE2_ECC[4]	DC21	SMI2	I/O
VMSE2_ECC[5]	DD20	SMI2	I/O
VMSE2_ECC[6]	DE25	SMI2	I/O
VMSE2_ECC[7]	DC23	SMI2	I/O
VMSE2_ERR_N	CU13	SMI2	I/O
VMSE3_CLK_N	BK14	SMI2	O
VMSE3_CLK_P	BM14	SMI2	O
VMSE3_CMD[0]	BJ15	SMI2	O
VMSE3_CMD[1]	BU11	SMI2	O
VMSE3_CMD[10]	BW15	SMI2	O
VMSE3_CMD[11]	BV14	SMI2	O
VMSE3_CMD[12]	BV16	SMI2	O
VMSE3_CMD[13]	BR15	SMI2	O
VMSE3_CMD[14]	BT16	SMI2	O
VMSE3_CMD[15]	BW13	SMI2	O
VMSE3_CMD[16]	BY12	SMI2	O
VMSE3_CMD[2]	BU9	SMI2	O
VMSE3_CMD[3]	BN13	SMI2	O
VMSE3_CMD[4]	BH14	SMI2	O
VMSE3_CMD[5]	BW11	SMI2	O
VMSE3_CMD[6]	BR13	SMI2	O
VMSE3_CMD[7]	BW9	SMI2	O
VMSE3_CMD[8]	BJ13	SMI2	O
VMSE3_CMD[9]	BN15	SMI2	O
VMSE3_DQ[0]	BK10	SMI2	I/O

Table 7-1. Land Name (Sheet 30 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE3_DQ[1]	BL7	SMI2	I/O
VMSE3_DQ[10]	BP2	SMI2	I/O
VMSE3_DQ[11]	BP4	SMI2	I/O
VMSE3_DQ[12]	BK2	SMI2	I/O
VMSE3_DQ[13]	BL5	SMI2	I/O
VMSE3_DQ[14]	BN5	SMI2	I/O
VMSE3_DQ[15]	BN1	SMI2	I/O
VMSE3_DQ[16]	BU7	SMI2	I/O
VMSE3_DQ[17]	BU3	SMI2	I/O
VMSE3_DQ[18]	BW3	SMI2	I/O
VMSE3_DQ[19]	BY4	SMI2	I/O
VMSE3_DQ[2]	BP8	SMI2	I/O
VMSE3_DQ[20]	BT6	SMI2	I/O
VMSE3_DQ[21]	BW7	SMI2	I/O
VMSE3_DQ[22]	BY6	SMI2	I/O
VMSE3_DQ[23]	BU1	SMI2	I/O
VMSE3_DQ[24]	CB16	SMI2	I/O
VMSE3_DQ[25]	CC13	SMI2	I/O
VMSE3_DQ[26]	CF14	SMI2	I/O
VMSE3_DQ[27]	CF16	SMI2	I/O
VMSE3_DQ[28]	CB14	SMI2	I/O
VMSE3_DQ[29]	CC17	SMI2	I/O
VMSE3_DQ[3]	BP10	SMI2	I/O
VMSE3_DQ[30]	CE17	SMI2	I/O
VMSE3_DQ[31]	CE13	SMI2	I/O
VMSE3_DQ[32]	CJ9	SMI2	I/O
VMSE3_DQ[33]	CK6	SMI2	I/O
VMSE3_DQ[34]	CN7	SMI2	I/O
VMSE3_DQ[35]	CN9	SMI2	I/O
VMSE3_DQ[36]	CJ7	SMI2	I/O
VMSE3_DQ[37]	CK10	SMI2	I/O
VMSE3_DQ[38]	CM10	SMI2	I/O
VMSE3_DQ[39]	CM6	SMI2	I/O
VMSE3_DQ[4]	BK8	SMI2	I/O
VMSE3_DQ[40]	CA1	SMI2	I/O
VMSE3_DQ[41]	CC3	SMI2	I/O
VMSE3_DQ[42]	CG3	SMI2	I/O
VMSE3_DQ[43]	CJ3	SMI2	I/O
VMSE3_DQ[44]	CC5	SMI2	I/O
VMSE3_DQ[45]	CB2	SMI2	I/O
VMSE3_DQ[46]	CH4	SMI2	I/O

Table 7-1. Land Name (Sheet 31 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE3_DQ[47]	CE5	SMI2	I/O
VMSE3_DQ[48]	DA5	SMI2	I/O
VMSE3_DQ[49]	DD8	SMI2	I/O
VMSE3_DQ[5]	BL11	SMI2	I/O
VMSE3_DQ[50]	DE11	SMI2	I/O
VMSE3_DQ[51]	DC11	SMI2	I/O
VMSE3_DQ[52]	DC7	SMI2	I/O
VMSE3_DQ[53]	DB6	SMI2	I/O
VMSE3_DQ[54]	DB10	SMI2	I/O
VMSE3_DQ[55]	DF10	SMI2	I/O
VMSE3_DQ[56]	CR1	SMI2	I/O
VMSE3_DQ[57]	CW3	SMI2	I/O
VMSE3_DQ[58]	CM4	SMI2	I/O
VMSE3_DQ[59]	CR5	SMI2	I/O
VMSE3_DQ[6]	BN11	SMI2	I/O
VMSE3_DQ[60]	CN3	SMI2	I/O
VMSE3_DQ[61]	CT2	SMI2	I/O
VMSE3_DQ[62]	CU5	SMI2	I/O
VMSE3_DQ[63]	CV4	SMI2	I/O
VMSE3_DQ[7]	BN7	SMI2	I/O
VMSE3_DQ[8]	BK4	SMI2	I/O
VMSE3_DQ[9]	BL1	SMI2	I/O
VMSE3_DQS_N[0]	BN9	SMI2	I/O
VMSE3_DQS_N[1]	BL3	SMI2	I/O
VMSE3_DQS_N[2]	BU5	SMI2	I/O
VMSE3_DQS_N[3]	CC15	SMI2	I/O
VMSE3_DQS_N[4]	CK8	SMI2	I/O
VMSE3_DQS_N[5]	CD4	SMI2	I/O
VMSE3_DQS_N[6]	DC9	SMI2	I/O
VMSE3_DQS_N[7]	CR3	SMI2	I/O
VMSE3_DQS_N[8]	CE9	SMI2	I/O
VMSE3_DQS_P[0]	BL9	SMI2	I/O
VMSE3_DQS_P[1]	BN3	SMI2	I/O
VMSE3_DQS_P[2]	BW5	SMI2	I/O
VMSE3_DQS_P[3]	CE15	SMI2	I/O
VMSE3_DQS_P[4]	CM8	SMI2	I/O
VMSE3_DQS_P[5]	CE3	SMI2	I/O
VMSE3_DQS_P[6]	DE9	SMI2	I/O
VMSE3_DQS_P[7]	CT4	SMI2	I/O
VMSE3_DQS_P[8]	CC9	SMI2	I/O
VMSE3_ECC[0]	CC7	SMI2	I/O

Table 7-1. Land Name (Sheet 32 of 50)

Land Name	Land No.	Buffer Type	Direction
VMSE3_ECC[1]	CF8	SMI2	I/O
VMSE3_ECC[2]	CC11	SMI2	I/O
VMSE3_ECC[3]	CE11	SMI2	I/O
VMSE3_ECC[4]	CE7	SMI2	I/O
VMSE3_ECC[5]	CB8	SMI2	I/O
VMSE3_ECC[6]	CF10	SMI2	I/O
VMSE3_ECC[7]	CB10	SMI2	I/O
VMSE3_ERR_N	BT12	SMI2	I/O
VPP_SCL	BC11	CMOS	I/O
VPP_SDA	BB10	CMOS	I/O
VCCPLL	BF10	PWR	
VCCPLL	BG11	PWR	
VCCPLL	BH10	PWR	
VSS	A15	GND	
VSS	A51	GND	
VSS	AA19	GND	
VSS	AA23	GND	
VSS	AA29	GND	
VSS	AA47	GND	
VSS	AA5	GND	
VSS	AA51	GND	
VSS	AA9	GND	
VSS	AB18	GND	
VSS	AB24	GND	
VSS	AB30	GND	
VSS	AB34	GND	
VSS	AB50	GND	
VSS	AB8	GND	
VSS	AC11	GND	
VSS	AC15	GND	
VSS	AC17	GND	
VSS	AC19	GND	
VSS	AC23	GND	
VSS	AC29	GND	
VSS	AC35	GND	
VSS	AC37	GND	
VSS	AC39	GND	
VSS	AC41	GND	
VSS	AC43	GND	
VSS	AC45	GND	
VSS	AC5	GND	

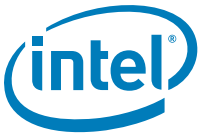

Table 7-1. Land Name (Sheet 33 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	AD12	GND	
VSS	AD14	GND	
VSS	AD16	GND	
VSS	AD18	GND	
VSS	AD24	GND	
VSS	AD30	GND	
VSS	AD34	GND	
VSS	AD36	GND	
VSS	AD38	GND	
VSS	AD4	GND	
VSS	AD40	GND	
VSS	AD42	GND	
VSS	AD46	GND	
VSS	AD54	GND	
VSS	AD8	GND	
VSS	AE19	GND	
VSS	AE23	GND	
VSS	AE29	GND	
VSS	AE3	GND	
VSS	AE47	GND	
VSS	AE5	GND	
VSS	AE51	GND	
VSS	AE57	GND	
VSS	AF18	GND	
VSS	AF24	GND	
VSS	AF30	GND	
VSS	AF34	GND	
VSS	AF4	GND	
VSS	AF50	GND	
VSS	AF54	GND	
VSS	AF56	GND	
VSS	AF8	GND	
VSS	AG19	GND	
VSS	AG23	GND	
VSS	AG29	GND	
VSS	AG3	GND	
VSS	AG43	GND	
VSS	AG45	GND	
VSS	AG47	GND	
VSS	AG53	GND	
VSS	AG55	GND	

Table 7-1. Land Name (Sheet 34 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	AG7	GND	
VSS	AH10	GND	
VSS	AH52	GND	
VSS	AH54	GND	
VSS	AH6	GND	
VSS	AJ11	GND	
VSS	AJ51	GND	
VSS	AK50	GND	
VSS	AL13	GND	
VSS	AL15	GND	
VSS	AL17	GND	
VSS	AL3	GND	
VSS	AL47	GND	
VSS	AL53	GND	
VSS	AL9	GND	
VSS	AM12	GND	
VSS	AM14	GND	
VSS	AM16	GND	
VSS	AM50	GND	
VSS	AM56	GND	
VSS	AM6	GND	
VSS	AN3	GND	
VSS	AN43	GND	
VSS	AN45	GND	
VSS	AN47	GND	
VSS	AN49	GND	
VSS	AN53	GND	
VSS	AP42	GND	
VSS	AP44	GND	
VSS	AP48	GND	
VSS	AP56	GND	
VSS	AR3	GND	
VSS	AR53	GND	
VSS	AR9	GND	
VSS	AT50	GND	
VSS	AT56	GND	
VSS	AT6	GND	
VSS	AU47	GND	
VSS	AU9	GND	
VSS	AV50	GND	
VSS	AV6	GND	

Table 7-1. Land Name (Sheet 35 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	AW13	GND	
VSS	AW15	GND	
VSS	AW17	GND	
VSS	AW3	GND	
VSS	AW53	GND	
VSS	AW7	GND	
VSS	AY12	GND	
VSS	AY14	GND	
VSS	AY16	GND	
VSS	AY42	GND	
VSS	AY44	GND	
VSS	AY46	GND	
VSS	AY48	GND	
VSS	AY56	GND	
VSS	B12	GND	
VSS	B18	GND	
VSS	B34	GND	
VSS	B42	GND	
VSS	BA11	GND	
VSS	BA43	GND	
VSS	BA45	GND	
VSS	BA53	GND	
VSS	BA9	GND	
VSS	BB50	GND	
VSS	BB56	GND	
VSS	BB6	GND	
VSS	BC3	GND	
VSS	BC47	GND	
VSS	BC49	GND	
VSS	BC53	GND	
VSS	BC9	GND	
VSS	BD50	GND	
VSS	BD56	GND	
VSS	BE9	GND	
VSS	BF6	GND	
VSS	BG13	GND	
VSS	BG15	GND	
VSS	BG17	GND	
VSS	BG3	GND	
VSS	BG43	GND	
VSS	BG45	GND	

Table 7-1. Land Name (Sheet 36 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	BG47	GND	
VSS	BG53	GND	
VSS	BG9	GND	
VSS	BH12	GND	
VSS	BH16	GND	
VSS	BH2	GND	
VSS	BH4	GND	
VSS	BH42	GND	
VSS	BH48	GND	
VSS	BH50	GND	
VSS	BH56	GND	
VSS	BH58	GND	
VSS	BH8	GND	
VSS	BJ1	GND	
VSS	BJ11	GND	
VSS	BJ5	GND	
VSS	BJ53	GND	
VSS	BJ55	GND	
VSS	BJ57	GND	
VSS	BJ7	GND	
VSS	BK16	GND	
VSS	BK42	GND	
VSS	BK44	GND	
VSS	BK46	GND	
VSS	BK48	GND	
VSS	BK50	GND	
VSS	BK54	GND	
VSS	BK56	GND	
VSS	BK6	GND	
VSS	BL13	GND	
VSS	BL15	GND	
VSS	BL53	GND	
VSS	BM10	GND	
VSS	BM12	GND	
VSS	BM16	GND	
VSS	BM2	GND	
VSS	BM4	GND	
VSS	BM42	GND	
VSS	BM52	GND	
VSS	BM58	GND	
VSS	BM6	GND	

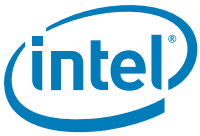

Table 7-1. Land Name (Sheet 37 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	BM8	GND	
VSS	BN43	GND	
VSS	BN47	GND	
VSS	BN49	GND	
VSS	BN51	GND	
VSS	BN55	GND	
VSS	BP12	GND	
VSS	BP14	GND	
VSS	BP16	GND	
VSS	BP44	GND	
VSS	BP46	GND	
VSS	BP48	GND	
VSS	BP50	GND	
VSS	BP52	GND	
VSS	BP54	GND	
VSS	BP6	GND	
VSS	BR1	GND	
VSS	BR11	GND	
VSS	BR17	GND	
VSS	BR3	GND	
VSS	BR43	GND	
VSS	BR5	GND	
VSS	BR53	GND	
VSS	BR57	GND	
VSS	BR7	GND	
VSS	BR9	GND	
VSS	BT10	GND	
VSS	BT2	GND	
VSS	BT4	GND	
VSS	BT56	GND	
VSS	BT58	GND	
VSS	BT8	GND	
VSS	BU13	GND	
VSS	BU15	GND	
VSS	BU17	GND	
VSS	BU43	GND	
VSS	BU45	GND	
VSS	BU47	GND	
VSS	BU49	GND	
VSS	BU51	GND	
VSS	BU53	GND	

Table 7-1. Land Name (Sheet 38 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	BU55	GND	
VSS	BV12	GND	
VSS	BV2	GND	
VSS	BV4	GND	
VSS	BV54	GND	
VSS	BV6	GND	
VSS	BV8	GND	
VSS	BW1	GND	
VSS	BW17	GND	
VSS	BW43	GND	
VSS	BW47	GND	
VSS	BW57	GND	
VSS	BY10	GND	
VSS	BY14	GND	
VSS	BY16	GND	
VSS	BY18	GND	
VSS	BY20	GND	
VSS	BY22	GND	
VSS	BY26	GND	
VSS	BY28	GND	
VSS	BY32	GND	
VSS	BY34	GND	
VSS	BY38	GND	
VSS	BY40	GND	
VSS	BY46	GND	
VSS	BY50	GND	
VSS	BY52	GND	
VSS	BY8	GND	
VSS	C23	GND	
VSS	C53	GND	
VSS	C7	GND	
VSS	C9	GND	
VSS	CA11	GND	
VSS	CA13	GND	
VSS	CA15	GND	
VSS	CA17	GND	
VSS	CA19	GND	
VSS	CA21	GND	
VSS	CA23	GND	
VSS	CA25	GND	
VSS	CA27	GND	

Table 7-1. Land Name (Sheet 39 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	CA29	GND	
VSS	CA3	GND	
VSS	CA31	GND	
VSS	CA33	GND	
VSS	CA35	GND	
VSS	CA37	GND	
VSS	CA39	GND	
VSS	CA41	GND	
VSS	CA43	GND	
VSS	CA45	GND	
VSS	CA47	GND	
VSS	CA49	GND	
VSS	CA5	GND	
VSS	CA51	GND	
VSS	CA53	GND	
VSS	CA55	GND	
VSS	CA7	GND	
VSS	CA9	GND	
VSS	CB12	GND	
VSS	CB24	GND	
VSS	CB30	GND	
VSS	CB36	GND	
VSS	CB4	GND	
VSS	CB42	GND	
VSS	CB54	GND	
VSS	CB56	GND	
VSS	CB6	GND	
VSS	CD10	GND	
VSS	CD12	GND	
VSS	CD14	GND	
VSS	CD16	GND	
VSS	CD18	GND	
VSS	CD20	GND	
VSS	CD22	GND	
VSS	CD24	GND	
VSS	CD26	GND	
VSS	CD28	GND	
VSS	CD30	GND	
VSS	CD32	GND	
VSS	CD34	GND	
VSS	CD36	GND	

Table 7-1. Land Name (Sheet 40 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	CD38	GND	
VSS	CD40	GND	
VSS	CD42	GND	
VSS	CD44	GND	
VSS	CD46	GND	
VSS	CD48	GND	
VSS	CD50	GND	
VSS	CD52	GND	
VSS	CD6	GND	
VSS	CD8	GND	
VSS	CE55	GND	
VSS	CF18	GND	
VSS	CF30	GND	
VSS	CF4	GND	
VSS	CF48	GND	
VSS	CF54	GND	
VSS	CF56	GND	
VSS	CG11	GND	
VSS	CG13	GND	
VSS	CG15	GND	
VSS	CG17	GND	
VSS	CG19	GND	
VSS	CG21	GND	
VSS	CG23	GND	
VSS	CG25	GND	
VSS	CG27	GND	
VSS	CG29	GND	
VSS	CG31	GND	
VSS	CG33	GND	
VSS	CG35	GND	
VSS	CG37	GND	
VSS	CG39	GND	
VSS	CG41	GND	
VSS	CG43	GND	
VSS	CG45	GND	
VSS	CG47	GND	
VSS	CG49	GND	
VSS	CG5	GND	
VSS	CG51	GND	
VSS	CG53	GND	
VSS	CG7	GND	

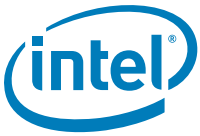

Table 7-1. Land Name (Sheet 41 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	CG9	GND	
VSS	CH10	GND	
VSS	CH12	GND	
VSS	CH14	GND	
VSS	CH16	GND	
VSS	CH18	GND	
VSS	CH20	GND	
VSS	CH22	GND	
VSS	CH24	GND	
VSS	CH26	GND	
VSS	CH28	GND	
VSS	CH30	GND	
VSS	CH32	GND	
VSS	CH34	GND	
VSS	CH36	GND	
VSS	CH38	GND	
VSS	CH40	GND	
VSS	CH42	GND	
VSS	CH44	GND	
VSS	CH46	GND	
VSS	CH48	GND	
VSS	CH50	GND	
VSS	CH52	GND	
VSS	CH6	GND	
VSS	CH8	GND	
VSS	CJ17	GND	
VSS	CJ23	GND	
VSS	CJ29	GND	
VSS	CJ41	GND	
VSS	CJ53	GND	
VSS	CJ55	GND	
VSS	CK4	GND	
VSS	CK56	GND	
VSS	CL11	GND	
VSS	CL13	GND	
VSS	CL15	GND	
VSS	CL17	GND	
VSS	CL19	GND	
VSS	CL21	GND	
VSS	CL23	GND	
VSS	CL25	GND	

Table 7-1. Land Name (Sheet 42 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	CL27	GND	
VSS	CL29	GND	
VSS	CL3	GND	
VSS	CL31	GND	
VSS	CL33	GND	
VSS	CL35	GND	
VSS	CL37	GND	
VSS	CL39	GND	
VSS	CL41	GND	
VSS	CL43	GND	
VSS	CL45	GND	
VSS	CL47	GND	
VSS	CL49	GND	
VSS	CL5	GND	
VSS	CL51	GND	
VSS	CL53	GND	
VSS	CL7	GND	
VSS	CL9	GND	
VSS	CN11	GND	
VSS	CN23	GND	
VSS	CN29	GND	
VSS	CN35	GND	
VSS	CN47	GND	
VSS	CN5	GND	
VSS	CP10	GND	
VSS	CP12	GND	
VSS	CP14	GND	
VSS	CP16	GND	
VSS	CP18	GND	
VSS	CP2	GND	
VSS	CP20	GND	
VSS	CP22	GND	
VSS	CP26	GND	
VSS	CP28	GND	
VSS	CP30	GND	
VSS	CP32	GND	
VSS	CP34	GND	
VSS	CP36	GND	
VSS	CP38	GND	
VSS	CP4	GND	
VSS	CP40	GND	

Table 7-1. Land Name (Sheet 43 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	CP42	GND	
VSS	CP44	GND	
VSS	CP46	GND	
VSS	CP48	GND	
VSS	CP50	GND	
VSS	CP52	GND	
VSS	CP54	GND	
VSS	CP56	GND	
VSS	CP6	GND	
VSS	CP8	GND	
VSS	CR13	GND	
VSS	CR15	GND	
VSS	CR19	GND	
VSS	CR21	GND	
VSS	CR25	GND	
VSS	CR27	GND	
VSS	CR31	GND	
VSS	CR33	GND	
VSS	CR37	GND	
VSS	CR39	GND	
VSS	CR43	GND	
VSS	CR45	GND	
VSS	CR47	GND	
VSS	CR49	GND	
VSS	CR51	GND	
VSS	CR53	GND	
VSS	CR55	GND	
VSS	CR57	GND	
VSS	CR7	GND	
VSS	CR9	GND	
VSS	CT12	GND	
VSS	CT24	GND	
VSS	CT26	GND	
VSS	CT28	GND	
VSS	CT30	GND	
VSS	CT32	GND	
VSS	CT34	GND	
VSS	CT58	GND	
VSS	CT6	GND	
VSS	CU11	GND	
VSS	CU17	GND	

Table 7-1. Land Name (Sheet 44 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	CU23	GND	
VSS	CU29	GND	
VSS	CU3	GND	
VSS	CU41	GND	
VSS	CU43	GND	
VSS	CV14	GND	
VSS	CV16	GND	
VSS	CV2	GND	
VSS	CV20	GND	
VSS	CV22	GND	
VSS	CV36	GND	
VSS	CV38	GND	
VSS	CV42	GND	
VSS	CV44	GND	
VSS	CV46	GND	
VSS	CV48	GND	
VSS	CV50	GND	
VSS	CV52	GND	
VSS	CV54	GND	
VSS	CV56	GND	
VSS	CV6	GND	
VSS	CV8	GND	
VSS	CW19	GND	
VSS	CW21	GND	
VSS	CW23	GND	
VSS	CW25	GND	
VSS	CW27	GND	
VSS	CW29	GND	
VSS	CW31	GND	
VSS	CW33	GND	
VSS	CW35	GND	
VSS	CW39	GND	
VSS	CW5	GND	
VSS	CY10	GND	
VSS	CY12	GND	
VSS	CY2	GND	
VSS	CY4	GND	
VSS	CY46	GND	
VSS	CY52	GND	
VSS	D12	GND	
VSS	D18	GND	

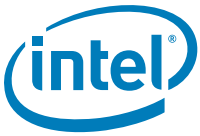

Table 7-1. Land Name (Sheet 45 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	D24	GND	
VSS	D34	GND	
VSS	D6	GND	
VSS	D8	GND	
VSS	DA11	GND	
VSS	DA13	GND	
VSS	DA15	GND	
VSS	DA17	GND	
VSS	DA21	GND	
VSS	DA23	GND	
VSS	DA35	GND	
VSS	DA37	GND	
VSS	DA41	GND	
VSS	DA43	GND	
VSS	DA45	GND	
VSS	DA47	GND	
VSS	DA49	GND	
VSS	DA51	GND	
VSS	DA53	GND	
VSS	DA55	GND	
VSS	DA7	GND	
VSS	DA9	GND	
VSS	DB14	GND	
VSS	DB16	GND	
VSS	DB18	GND	
VSS	DB20	GND	
VSS	DB22	GND	
VSS	DB24	GND	
VSS	DB26	GND	
VSS	DB28	GND	
VSS	DB30	GND	
VSS	DB32	GND	
VSS	DB34	GND	
VSS	DB36	GND	
VSS	DB38	GND	
VSS	DB40	GND	
VSS	DB42	GND	
VSS	DB44	GND	
VSS	DB48	GND	
VSS	DB50	GND	
VSS	DB52	GND	

Table 7-1. Land Name (Sheet 46 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	DB58	GND	
VSS	DB8	GND	
VSS	DC33	GND	
VSS	DD10	GND	
VSS	DD12	GND	
VSS	DD14	GND	
VSS	DD24	GND	
VSS	DD34	GND	
VSS	DD44	GND	
VSS	DD46	GND	
VSS	DD48	GND	
VSS	DD54	GND	
VSS	DE17	GND	
VSS	DE19	GND	
VSS	DE21	GND	
VSS	DE37	GND	
VSS	DE39	GND	
VSS	DE41	GND	
VSS	DE51	GND	
VSS	DE7	GND	
VSS	DF12	GND	
VSS	DF26	GND	
VSS	DF46	GND	
VSS	DF8	GND	
VSS	E1	GND	
VSS	E15	GND	
VSS	E19	GND	
VSS	E23	GND	
VSS	E29	GND	
VSS	E35	GND	
VSS	E37	GND	
VSS	E39	GND	
VSS	E41	GND	
VSS	E43	GND	
VSS	E45	GND	
VSS	E47	GND	
VSS	E49	GND	
VSS	E5	GND	
VSS	E55	GND	
VSS	F18	GND	
VSS	F24	GND	

Table 7-1. Land Name (Sheet 47 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	F30	GND	
VSS	F40	GND	
VSS	F44	GND	
VSS	F46	GND	
VSS	F48	GND	
VSS	F50	GND	
VSS	F54	GND	
VSS	F8	GND	
VSS	G1	GND	
VSS	G15	GND	
VSS	G19	GND	
VSS	G23	GND	
VSS	G29	GND	
VSS	G5	GND	
VSS	G51	GND	
VSS	G57	GND	
VSS	G9	GND	
VSS	H12	GND	
VSS	H18	GND	
VSS	H24	GND	
VSS	H30	GND	
VSS	H42	GND	
VSS	H52	GND	
VSS	J19	GND	
VSS	J23	GND	
VSS	J29	GND	
VSS	J5	GND	
VSS	J57	GND	
VSS	K12	GND	
VSS	K18	GND	
VSS	K2	GND	
VSS	K24	GND	
VSS	K30	GND	
VSS	K34	GND	
VSS	K42	GND	
VSS	K50	GND	
VSS	K54	GND	
VSS	K8	GND	
VSS	L1	GND	
VSS	L13	GND	
VSS	L15	GND	

Table 7-1. Land Name (Sheet 48 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	L19	GND	
VSS	L23	GND	
VSS	L29	GND	
VSS	L35	GND	
VSS	L37	GND	
VSS	L39	GND	
VSS	L41	GND	
VSS	L43	GND	
VSS	L45	GND	
VSS	L47	GND	
VSS	L9	GND	
VSS	M18	GND	
VSS	M2	GND	
VSS	M24	GND	
VSS	M30	GND	
VSS	M34	GND	
VSS	M36	GND	
VSS	M38	GND	
VSS	M40	GND	
VSS	M44	GND	
VSS	M46	GND	
VSS	M50	GND	
VSS	M8	GND	
VSS	N19	GND	
VSS	N23	GND	
VSS	N29	GND	
VSS	N5	GND	
VSS	N51	GND	
VSS	P12	GND	
VSS	P18	GND	
VSS	P24	GND	
VSS	P30	GND	
VSS	P34	GND	
VSS	P54	GND	
VSS	R15	GND	
VSS	R19	GND	
VSS	R23	GND	
VSS	R29	GND	
VSS	R47	GND	
VSS	R5	GND	
VSS	R51	GND	

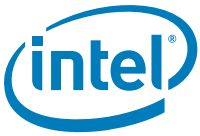

Table 7-1. Land Name (Sheet 49 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	R9	GND	
VSS	T18	GND	
VSS	T24	GND	
VSS	T30	GND	
VSS	T34	GND	
VSS	T50	GND	
VSS	T54	GND	
VSS	T8	GND	
VSS	U15	GND	
VSS	U19	GND	
VSS	U23	GND	
VSS	U29	GND	
VSS	U35	GND	
VSS	U37	GND	
VSS	U39	GND	
VSS	U41	GND	
VSS	U43	GND	
VSS	U45	GND	
VSS	U47	GND	
VSS	U5	GND	
VSS	U9	GND	
VSS	V12	GND	
VSS	V18	GND	
VSS	V24	GND	
VSS	V30	GND	
VSS	V34	GND	
VSS	V38	GND	
VSS	V40	GND	
VSS	V50	GND	
VSS	V8	GND	
VSS	W15	GND	
VSS	W19	GND	
VSS	W23	GND	
VSS	W29	GND	
VSS	W5	GND	

Table 7-1. Land Name (Sheet 50 of 50)

Land Name	Land No.	Buffer Type	Direction
VSS	W51	GND	
VSS	Y12	GND	
VSS	Y18	GND	
VSS	Y24	GND	
VSS	Y30	GND	
VSS	Y34	GND	
VSS	Y54	GND	
VSS_VCC_SENSE	AE43		O
VSS_VTT_SENSE	L51		O
VSS_VSA_SENSE	BH6		O
VVMSE01	CD54	PWR	
VVMSE01	CF42	PWR	
VVMSE01	CJ35	PWR	
VVMSE01	CJ47	PWR	
VVMSE01	CR29	PWR	
VVMSE01	CT52	PWR	
VVMSE01	CV40	PWR	
VVMSE01	DB46	PWR	
VVMSE23	CF12	PWR	
VVMSE23	CF24	PWR	
VVMSE23	CJ5	PWR	
VVMSE23	CN17	PWR	
VVMSE23	CP24	PWR	
VVMSE23	CY6	PWR	
VVMSE23	DB12	PWR	
VVMSE23	DC25	PWR	

7.2 Listing by Land Number

Table 7-2. Land Number (Sheet 1 of 50)

Land No.	Land Name	Buffer Type	Direction
A11	PE1_RX_N[13]	PCIEX3	I
A13	VTTA	PWR	
A15	VSS	GND	
A17	PE1_TX_N[9]	PCIEX3	O
A19	VCC	PWR	
A21	VCC	PWR	
A23	VCC	PWR	
A33	VCC	PWR	
A35	QPI0_DRX_DN[3]	QPI	I
A37	QPI0_DRX_DN[5]	QPI	I
A39	QPI0_DRX_DN[7]	QPI	I
A41	QPI0_DRX_DN[9]	QPI	I
A43	QPI0_CLKRX_DN	QPI	I
A45	QPI0_DRX_DN[11]	QPI	I
A47	QPI0_DRX_DN[13]	QPI	I
A49	QPI0_DRX_DN[15]	QPI	I
A5	RSVD		
A51	VSS	GND	
A53	BPM_N[5]	CMOS	I/O
A7	RSVD		
A9	PE1_RX_N[15]	PCIEX3	I
AA11	PE1_RX_N[0]	PCIEX3	I
AA13	PE1_TX_P[11]	PCIEX3	O
AA15	VTTA	PWR	
AA17	PE1_TX_N[0]	PCIEX3	O
AA19	VSS	GND	
AA21	VCC	PWR	
AA23	VSS	GND	
AA25	VCC	PWR	
AA27	VCC	PWR	
AA29	VSS	GND	
AA3	QPI2_DRX_DP[8]	QPI	I
AA31	VCC	PWR	
AA33	VCC	PWR	
AA35	PE0_RX_P[0]	PCIEX3	O
AA37	PE0_RX_P[2]	PCIEX3	I
AA39	PE0_RX_P[4]	PCIEX3	I
AA41	PE0_RX_P[6]	PCIEX3	I
AA43	PE0_RX_P[12]	PCIEX3	I

Table 7-2. Land Number (Sheet 2 of 50)

Land No.	Land Name	Buffer Type	Direction
AA45	PE0_RX_P[15]	PCIEX3	I
AA47	VSS	GND	
AA49	QPI1_DTX_DN[15]	QPI	O
AA5	VSS	GND	
AA51	VSS	GND	
AA53	QPI0_DTX_DN[8]	QPI	O
AA55	QPI1_DRX_DP[12]	QPI	I
AA7	QPI2_DTX_DN[8]	QPI	O
AA9	VSS	GND	
AB10	PE1_RX_P[0]	PCIEX3	I
AB12	VTTA	PWR	
AB14	RSVD		
AB16	PE1_TX_P[0]	PCIEX3	O
AB18	VSS	GND	
AB20	VCC	PWR	
AB22	VCC	PWR	
AB24	VSS	GND	
AB26	VCC	PWR	
AB28	VCC	PWR	
AB30	VSS	GND	
AB32	VCC	PWR	
AB34	VSS	GND	
AB36	PE0_RX_P[1]	PCIEX3	I
AB38	PE0_RX_P[3]	PCIEX3	I
AB4	QPI2_DRX_DN[9]	QPI	I
AB40	PE0_RX_P[5]	PCIEX3	I
AB42	PE0_RX_P[7]	PCIEX3	I
AB44	PE0_RX_P[13]	PCIEX3	I
AB46	PE0_RX_P[14]	PCIEX3	I
AB48	QPI1_DTX_DP[15]	QPI	O
AB50	VSS	GND	
AB52	QPI0_DTX_DP[8]	QPI	O
AB54	SOCKET_ID[1]	CMOS	I
AB56	QPI1_DRX_DN[11]	QPI	I
AB6	QPI2_DTX_DP[8]	QPI	O
AB8	VSS	GND	
AC11	VSS	GND	
AC13	RSVD		
AC15	VSS	GND	
AC17	VSS	GND	

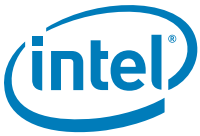

Table 7-2. Land Number (Sheet 3 of 50)

Land No.	Land Name	Buffer Type	Direction
AC19	VSS	GND	
AC21	VCC	PWR	
AC23	VSS	GND	
AC25	VCC	PWR	
AC27	VCC	PWR	
AC29	VSS	GND	
AC3	QPI2_DRX_DP[9]	QPI	I
AC31	VCC	PWR	
AC33	VCC	PWR	
AC35	VSS	GND	
AC37	VSS	GND	
AC39	VSS	GND	
AC41	VSS	GND	
AC43	VSS	GND	
AC45	VSS	GND	
AC47	VTTA	PWR	
AC49	QPI1_DTX_DN[14]	QPI	O
AC5	VSS	GND	
AC51	RSVD		
AC53	QPI0_DTX_DN[9]	QPI	O
AC55	QPI1_DRX_DP[11]	QPI	I
AC7	QPI2_DTX_DN[9]	QPI	O
AC9	VTTQ	PWR	
AD10	VCCPECI	PWR	
AD12	VSS	GND	
AD14	VSS	GND	
AD16	VSS	GND	
AD18	VSS	GND	
AD20	VCC	PWR	
AD22	VCC	PWR	
AD24	VSS	GND	
AD26	VCC	PWR	
AD28	VCC	PWR	
AD30	VSS	GND	
AD32	VCC	PWR	
AD34	VSS	GND	
AD36	VSS	GND	
AD38	VSS	GND	
AD4	VSS	GND	
AD40	VSS	GND	
AD42	VSS	GND	

Table 7-2. Land Number (Sheet 4 of 50)

Land No.	Land Name	Buffer Type	Direction
AD44	RSVD		
AD46	VSS	GND	
AD48	QPI1_DTX_DP[14]	QPI	O
AD50	FRMAGENT	CMOS	I
AD52	QPI0_DTX_DP[9]	QPI	O
AD54	VSS	GND	
AD56	QPI1_DRX_DN[10]	QPI	I
AD6	QPI2_DTX_DP[9]	QPI	O
AD8	VSS	GND	
AE11	NMI	GTL	I
AE13	VCC	PWR	
AE15	VCC	PWR	
AE17	VCC	PWR	
AE19	VSS	GND	
AE21	VCC	PWR	
AE23	VSS	GND	
AE25	VCC	PWR	
AE27	VCC	PWR	
AE29	VSS	GND	
AE3	VSS	GND	
AE31	VCC	PWR	
AE33	VCC	PWR	
AE35	PREQ_N	CMOS	I
AE37	RSVD		
AE39	PRDY_N	CMOS	O
AE41	PECI	PECI	I/O
AE43	VSS_VCC_SENSE		O
AE45	PMSYNC	CMOS	I
AE47	VSS	GND	
AE49	QPI1_DTX_DN[13]	QPI	O
AE5	VSS	GND	
AE51	VSS	GND	
AE53	QPI0_CLKTX_DN	QPI	O
AE55	QPI1_DRX_DP[10]	QPI	I
AE57	VSS	GND	
AE7	QPI2_CLKTX_DP	QPI	O
AE9	BCLK1_DN	CMOS	I
AF10	BCLK1_DP	CMOS	I
AF12	VCC	PWR	
AF14	VCC	PWR	
AF16	VCC	PWR	

Table 7-2. Land Number (Sheet 5 of 50)

Land No.	Land Name	Buffer Type	Direction
AF18	VSS	GND	
AF2	QPI2_CLKRX_DN	QPI	I
AF20	VCC	PWR	
AF22	VCC	PWR	
AF24	VSS	GND	
AF26	VCC	PWR	
AF28	VCC	PWR	
AF30	VSS	GND	
AF32	VCC	PWR	
AF34	VSS	GND	
AF36	FIVR_FAULT	CMOS	O
AF38	RESET_N	CMOS	I
AF4	VSS	GND	
AF40	TEST_8		
AF42	VCC_SENSE		O
AF44	RSVD		
AF46	BCLK0_DN	CMOS	I
AF48	QPI1_DTX_DP[13]	QPI	O
AF50	VSS	GND	
AF52	QPI0_CLKTX_DP	QPI	O
AF54	VSS	GND	
AF56	VSS	GND	
AF58	QPI1_CLKRX_DN	QPI	I
AF6	QPI2_CLKTX_DN	QPI	O
AF8	VSS	GND	
AG1	QPI2_CLKRX_DP	QPI	I
AG11	PM_FAST_WAKE_N	CMOS	I/O
AG13	VCC	PWR	
AG15	VCC	PWR	
AG17	VCC	PWR	
AG19	VSS	GND	
AG21	VCC	PWR	
AG23	VSS	GND	
AG25	VCC	PWR	
AG27	VCC	PWR	
AG29	VSS	GND	
AG3	VSS	GND	
AG31	VCC	PWR	
AG33	VCC	PWR	
AG35	CATERR_N	CMOS	I/O
AG37	VCC	PWR	

Table 7-2. Land Number (Sheet 6 of 50)

Land No.	Land Name	Buffer Type	Direction
AG39	VCC	PWR	
AG41	VCC	PWR	
AG43	VSS	GND	
AG45	VSS	GND	
AG47	VSS	GND	
AG49	QPI1_DTX_DN[12]	QPI	O
AG5	QPI2_DTX_DN[10]	QPI	O
AG51	TEST_9		
AG53	VSS	GND	
AG55	VSS	GND	
AG57	QPI1_CLKRX_DP	QPI	I
AG7	VSS	GND	
AG9	PROC_ID[1]		O
AH10	VSS	GND	
AH12	VCC	PWR	
AH14	VCC	PWR	
AH16	VCC	PWR	
AH2	QPI2_DRX_DN[10]	QPI	I
AH4	QPI2_DTX_DP[10]	QPI	O
AH42	VCC	PWR	
AH44	VCC	PWR	
AH46	BCLK0_DP	CMOS	I
AH48	QPI1_DTX_DP[12]	QPI	O
AH50	TMS	CMOS	I
AH52	VSS	GND	
AH54	VSS	GND	
AH56	VTTQ	PWR	
AH58	QPI1_DRX_DN[9]	QPI	I
AH6	VSS	GND	
AH8	PROC_ID[0]		O
AJ1	QPI2_DRX_DP[10]	QPI	I
AJ11	VSS	GND	
AJ13	VCC	PWR	
AJ15	VCC	PWR	
AJ17	VCC	PWR	
AJ3	VSA	PWR	
AJ43	VCC	PWR	
AJ45	VCC	PWR	
AJ47	TDO	Open Drain	O
AJ49	QPI1_DTX_DN[11]	QPI	O
AJ5	QPI2_DTX_DN[11]	QPI	O

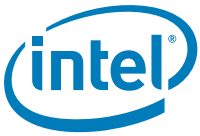

Table 7-2. Land Number (Sheet 7 of 50)

Land No.	Land Name	Buffer Type	Direction
AJ51	VSS	GND	
AJ53	VTTQ	PWR	
AJ55	QPI0_DTX_DN[10]	QPI	O
AJ57	QPI1_DRX_DP[9]	QPI	I
AJ7	VSA	PWR	
AJ9	TXT_PLTEN	CMOS	I
AK10	TXT_AGENT	CMOS	I
AK12	VCC	PWR	
AK14	VCC	PWR	
AK16	VCC	PWR	
AK2	QPI2_DRX_DN[11]	QPI	I
AK4	QPI2_DTX_DP[11]	QPI	O
AK42	VCC	PWR	
AK44	VCC	PWR	
AK46	TRST_N	CMOS	I
AK48	QPI1_DTX_DP[11]	QPI	O
AK50	VSS	GND	
AK52	QPI1_CLKTX_DN	QPI	O
AK54	QPI0_DTX_DP[10]	QPI	O
AK56	SOCKET_ID[0]	CMOS	I
AK58	QPI1_DRX_DN[8]	QPI	I
AK6	VSA	PWR	
AK8	DMI_TX_N[0]	CMOS	O
AL1	QPI2_DRX_DP[11]	QPI	I
AL11	SMBCLK		I/O
AL13	VSS	GND	
AL15	VSS	GND	
AL17	VSS	GND	
AL3	VSS	GND	
AL43	VCC	PWR	
AL45	VCC	PWR	
AL47	VSS	GND	
AL49	QPI1_DTX_DN[10]	QPI	O
AL5	QPI2_DTX_DN[12]	QPI	O
AL51	QPI1_CLKTX_DP	QPI	O
AL53	VSS	GND	
AL55	QPI0_DTX_DN[11]	QPI	O
AL57	QPI1_DRX_DP[8]	QPI	I
AL7	DMI_TX_P[0]	CMOS	O
AL9	VSS	GND	
AM10	SMBDAT		I/O

Table 7-2. Land Number (Sheet 8 of 50)

Land No.	Land Name	Buffer Type	Direction
AM12	VSS	GND	
AM14	VSS	GND	
AM16	VSS	GND	
AM2	QPI2_DRX_DN[12]	QPI	I
AM4	QPI2_DTX_DP[12]	QPI	O
AM42	VCC	PWR	
AM44	VCC	PWR	
AM46	RSVD		
AM48	QPI1_DTX_DP[10]	QPI	O
AM50	VSS	GND	
AM52	QPI1_DTX_DN[9]	QPI	O
AM54	QPI0_DTX_DP[11]	QPI	O
AM56	VSS	GND	
AM58	QPI1_DRX_DN[7]	QPI	I
AM6	VSS	GND	
AM8	DMI_TX_N[1]	CMOS	O
AN1	QPI2_DRX_DP[12]	QPI	I
AN11	ERROR_N[2]	Open Drain	O
AN13	VCC	PWR	
AN15	VCC	PWR	
AN17	VCC	PWR	
AN3	VSS	GND	
AN43	VSS	GND	
AN45	VSS	GND	
AN47	VSS	GND	
AN49	VSS	GND	
AN5	QPI2_DTX_DN[13]	QPI	O
AN51	QPI1_DTX_DP[9]	QPI	O
AN53	VSS	GND	
AN55	QPI0_DTX_DN[12]	QPI	O
AN57	QPI1_DRX_DP[7]	QPI	I
AN7	DMI_TX_P[1]	CMOS	O
AN9	VCCIO_IN		
AP10	SM_WP		I
AP12	VCC	PWR	
AP14	VCC	PWR	
AP16	VCC	PWR	
AP2	QPI2_DRX_DN[13]	QPI	I
AP4	QPI2_DTX_DP[13]	QPI	O
AP42	VSS	GND	
AP44	VSS	GND	

Table 7-2. Land Number (Sheet 9 of 50)

Land No.	Land Name	Buffer Type	Direction
AP46	RSVD		
AP48	VSS	GND	
AP50	BMCINIT	CMOS	I
AP52	QPI1_DTX_DN[8]	QPI	O
AP54	QPI0_DTX_DP[12]	QPI	O
AP56	VSS	GND	
AP58	QPI1_DRX_DN[6]	QPI	I
AP6	TEST_11		
AP8	DMI_TX_N[2]	CMOS	O
AR1	QPI2_DRX_DP[13]	QPI	I
AR11	ERROR_N[0]	Open Drain	O
AR13	VCC	PWR	
AR15	VCC	PWR	
AR17	VCC	PWR	
AR3	VSS	GND	
AR43	VCC	PWR	
AR45	VCC	PWR	
AR47	RSVD		
AR49	RSVD		
AR5	QPI2_DTX_DN[14]	QPI	O
AR51	QPI1_DTX_DP[8]	QPI	O
AR53	VSS	GND	
AR55	QPI0_DTX_DN[13]	QPI	O
AR57	QPI1_DRX_DP[6]	QPI	I
AR7	DMI_TX_P[2]	CMOS	O
AR9	VSS	GND	
AT10	ERROR_N[1]	Open Drain	O
AT12	VCC	PWR	
AT14	VCC	PWR	
AT16	VCC	PWR	
AT2	QPI2_DRX_DN[14]	QPI	I
AT4	QPI2_DTX_DP[14]	QPI	O
AT42	VCC	PWR	
AT44	VCC	PWR	
AT46	RSVD		
AT48	RSVD		
AT50	VSS	GND	
AT52	QPI1_DTX_DN[7]	QPI	O
AT54	QPI0_DTX_DP[13]	QPI	O
AT56	VSS	GND	
AT58	QPI1_DRX_DN[5]	QPI	I

Table 7-2. Land Number (Sheet 10 of 50)

Land No.	Land Name	Buffer Type	Direction
AT6	VSS	GND	
AT8	DMI_TX_N[3]	CMOS	O
AU1	QPI2_DRX_DP[14]	QPI	I
AU11	SVIDALERT_N	CMOS	I
AU13	VCC	PWR	
AU15	VCC	PWR	
AU17	VCC	PWR	
AU3	VSA	PWR	
AU43	VCC	PWR	
AU45	VCC	PWR	
AU47	VSS	GND	
AU49	RSVD		
AU5	QPI2_DTX_DN[15]	QPI	O
AU51	QPI1_DTX_DP[7]	QPI	O
AU53	VTTQ	PWR	
AU55	QPI0_DTX_DN[14]	QPI	O
AU57	QPI1_DRX_DP[5]	QPI	I
AU7	DMI_TX_P[3]	CMOS	O
AU9	VSS	GND	
AV10	SVIDCLK	Open Drain	O
AV12	VCC	PWR	
AV14	VCC	PWR	
AV16	VCC	PWR	
AV2	QPI2_DRX_DN[15]	QPI	I
AV4	QPI2_DTX_DP[15]	QPI	O
AV42	VCC	PWR	
AV44	VCC	PWR	
AV46	RSVD		
AV48	RSVD		
AV50	VSS	GND	
AV52	QPI1_DTX_DN[6]	QPI	O
AV54	QPI0_DTX_DP[14]	QPI	O
AV56	PROCHOT_N	Open Drain	I/O
AV58	QPI1_DRX_DN[4]	QPI	I
AV6	VSS	GND	
AV8	VSA	PWR	
AW1	QPI2_DRX_DP[15]	QPI	I
AW11	SVIDDATA	Open Drain	I/O
AW13	VSS	GND	
AW15	VSS	GND	
AW17	VSS	GND	

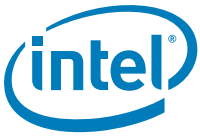

Table 7-2. Land Number (Sheet 11 of 50)

Land No.	Land Name	Buffer Type	Direction
AW3	VSS	GND	
AW43	VCC	PWR	
AW45	VCC	PWR	
AW47	RSVD		
AW49	RSVD		
AW5	QPI2_DTX_DN[16]	QPI	O
AW51	QPI1_DTX_DP[6]	QPI	O
AW53	VSS	GND	
AW55	QPI0_DTX_DN[15]	QPI	O
AW57	QPI1_DRX_DP[4]	QPI	I
AW7	VSS	GND	
AW9	VSA	PWR	
AY10	VSA	PWR	
AY12	VSS	GND	
AY14	VSS	GND	
AY16	VSS	GND	
AY2	QPI2_DRX_DN[16]	QPI	I
AY4	QPI2_DTX_DP[16]	QPI	O
AY42	VSS	GND	
AY44	VSS	GND	
AY46	VSS	GND	
AY48	VSS	GND	
AY50	BIST_ENABLE	CMOS	I
AY52	QPI1_DTX_DN[5]	QPI	O
AY54	QPI0_DTX_DP[15]	QPI	O
AY56	VSS	GND	
AY58	QPI1_DRX_DN[3]	QPI	I
AY6	VSA	PWR	
AY8	DMI_RX_N[0]	CMOS	I
B10	PE1_RX_P[13]	PCIEX3	I
B12	VSS	GND	
B14	PE1_RX_N[10]	PCIEX3	I
B16	PE1_TX_P[9]	PCIEX3	O
B18	VSS	GND	
B20	VCC	PWR	
B22	VCC	PWR	
B24	VCC	PWR	
B32	VCC	PWR	
B34	VSS	GND	
B36	QPI0_DRX_DN[4]	QPI	I
B38	QPI0_DRX_DN[6]	QPI	I

Table 7-2. Land Number (Sheet 12 of 50)

Land No.	Land Name	Buffer Type	Direction
B40	QPI0_DRX_DN[8]	QPI	I
B42	VSS	GND	
B44	QPI0_DRX_DN[10]	QPI	I
B46	QPI0_DRX_DN[12]	QPI	I
B48	QPI0_DRX_DN[14]	QPI	I
B50	QPI0_DRX_DN[16]	QPI	I
B52	RSVD		
B54	BPM_N[4]	CMOS	I/O
B6	RSVD		
B8	PE1_RX_P[15]	PCIEX3	I
BA1	QPI2_DRX_DP[16]	QPI	I
BA11	VSS	GND	
BA13	VCC	PWR	
BA15	VCC	PWR	
BA17	VCC	PWR	
BA3	TEST_13		
BA43	VSS	GND	
BA45	VSS	GND	
BA47	RSVD		
BA49	RSVD		
BA5	QPI2_DTX_DN[17]	QPI	O
BA51	QPI1_DTX_DP[5]	QPI	O
BA53	VSS	GND	
BA55	QPI0_DTX_DN[16]	QPI	O
BA57	QPI1_DRX_DP[3]	QPI	I
BA7	DMI_RX_P[0]	CMOS	I
BA9	VSS	GND	
BB10	VPP_SDA	CMOS	I/O
BB12	VCC	PWR	
BB14	VCC	PWR	
BB16	VCC	PWR	
BB2	QPI2_DRX_DN[17]	QPI	I
BB4	QPI2_DTX_DP[17]	QPI	O
BB42	VCC	PWR	
BB44	VCC	PWR	
BB46	RSVD		
BB48	RSVD		
BB50	VSS	GND	
BB52	QPI1_DTX_DN[4]	QPI	O
BB54	QPI0_DTX_DP[16]	QPI	O
BB56	VSS	GND	

Table 7-2. Land Number (Sheet 13 of 50)

Land No.	Land Name	Buffer Type	Direction
BB58	QPI1_DRX_DN[2]	QPI	I
BB6	VSS	GND	
BB8	DMI_RX_N[1]	CMOS	I
BC1	QPI2_DRX_DP[17]	QPI	I
BC11	VPP_SCL	CMOS	I/O
BC13	VCC	PWR	
BC15	VCC	PWR	
BC17	VCC	PWR	
BC3	VSS	GND	
BC43	VCC	PWR	
BC45	VCC	PWR	
BC47	VSS	GND	
BC49	VSS	GND	
BC5	QPI2_DTX_DN[18]	QPI	O
BC51	QPI1_DTX_DP[4]	QPI	O
BC53	VSS	GND	
BC55	QPI0_DTX_DN[17]	QPI	O
BC57	QPI1_DRX_DP[2]	QPI	I
BC7	DMI_RX_P[1]	CMOS	I
BC9	VSS	GND	
BD10	DEBUG_EN_N		
BD12	VCC	PWR	
BD14	VCC	PWR	
BD16	VCC	PWR	
BD2	QPI2_DRX_DN[18]	QPI	I
BD4	QPI2_DTX_DP[18]	QPI	O
BD42	VCC	PWR	
BD44	VCC	PWR	
BD46	RSVD		
BD48	RSVD		
BD50	VSS	GND	
BD52	QPI1_DTX_DN[3]	QPI	O
BD54	QPI0_DTX_DP[17]	QPI	O
BD56	VSS	GND	
BD58	QPI1_DRX_DN[1]	QPI	I
BD6	TEST_12		
BD8	DMI_RX_N[2]	CMOS	I
BE1	QPI2_DRX_DP[18]	QPI	I
BE11	VCC33	PWR	
BE13	VCC	PWR	
BE15	VCC	PWR	

Table 7-2. Land Number (Sheet 14 of 50)

Land No.	Land Name	Buffer Type	Direction
BE17	VCC	PWR	
BE3	VSA	PWR	
BE43	VCC	PWR	
BE45	VCC	PWR	
BE47	RSVD		
BE49	RSVD		
BE5	QPI2_DTX_DN[19]	QPI	O
BE51	QPI1_DTX_DP[3]	QPI	O
BE53	MSMI_N	CMOS	I/O
BE55	QPI0_DTX_DN[18]	QPI	O
BE57	QPI1_DRX_DP[1]	QPI	I
BE7	DMI_RX_P[2]	CMOS	I
BE9	VSS	GND	
BF10	VCCPLL	PWR	
BF12	VCC	PWR	
BF14	VCC	PWR	
BF16	VCC	PWR	
BF2	QPI2_DRX_DN[19]	QPI	I
BF4	QPI2_DTX_DP[19]	QPI	O
BF42	VCC	PWR	
BF44	VCC	PWR	
BF46	THERMTRIP_N	CMOS	O
BF48	RSVD		
BF50	TDI	CMOS	I
BF52	QPI1_DTX_DN[2]	QPI	O
BF54	QPI0_DTX_DP[18]	QPI	O
BF56	SAFE_MODE_BOOT	CMOS	I
BF58	QPI1_DRX_DN[0]	QPI	I
BF6	VSS	GND	
BF8	DMI_RX_N[3]	CMOS	I
BG1	QPI2_DRX_DP[19]	QPI	I
BG11	VCCPLL	PWR	
BG13	VSS	GND	
BG15	VSS	GND	
BG17	VSS	GND	
BG3	VSS	GND	
BG43	VSS	GND	
BG45	VSS	GND	
BG47	VSS	GND	
BG49	TCK	CMOS	I
BG5	VSA_SENSE		O

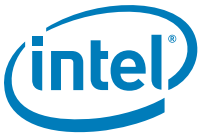

Table 7-2. Land Number (Sheet 15 of 50)

Land No.	Land Name	Buffer Type	Direction
BG51	QPI1_DTX_DP[2]	QPI	O
BG53	VSS	GND	
BG55	QPI0_DTX_DN[19]	QPI	O
BG57	QPI1_DRX_DP[0]	QPI	I
BG7	DMI_RX_P[3]	CMOS	I
BG9	VSS	GND	
BH10	VCCPLL	PWR	
BH12	VSS	GND	
BH14	VMSE3_CMD[4]	SMI2	O
BH16	VSS	GND	
BH2	VSS	GND	
BH4	VSS	GND	
BH42	VSS	GND	
BH44	VMSE0_CMD[0]	SMI2	O
BH46	VMSE0_CMD[15]	SMI2	O
BH48	VSS	GND	
BH50	VSS	GND	
BH52	QPI1_DTX_DN[1]	QPI	O
BH54	QPI0_DTX_DP[19]	QPI	O
BH56	VSS	GND	
BH58	VSS	GND	
BH6	VSS_VSA_SENSE		O
BH8	VSS	GND	
BJ1	VSS	GND	
BJ11	VSS	GND	
BJ13	VMSE3_CMD[8]	SMI2	O
BJ15	VMSE3_CMD[0]	SMI2	O
BJ17	VSA	PWR	
BJ3	SKTOCC_N		O
BJ43	VMSE0_CMD[4]	SMI2	O
BJ45	VMSE0_CMD[3]	SMI2	O
BJ47	VMSE0_CMD[16]	SMI2	O
BJ49	VMSE0_CMD[12]	SMI2	O
BJ5	VSS	GND	
BJ51	QPI1_DTX_DP[1]	QPI	O
BJ53	VSS	GND	
BJ55	VSS	GND	
BJ57	VSS	GND	
BJ7	VSS	GND	
BJ9	PWR_DEBUG_N	CMOS	I
BK10	VMSE3_DQ[0]	SMI2	I/O

Table 7-2. Land Number (Sheet 16 of 50)

Land No.	Land Name	Buffer Type	Direction
BK12	MEM_SDA_C3	Open Drain	I/O
BK14	VMSE3_CLK_N	SMI2	O
BK16	VSS	GND	
BK2	VMSE3_DQ[12]	SMI2	I/O
BK4	VMSE3_DQ[8]	SMI2	I/O
BK42	VSS	GND	
BK44	VSS	GND	
BK46	VSS	GND	
BK48	VSS	GND	
BK50	VSS	GND	
BK52	QPI1_DTX_DN[0]	QPI	O
BK54	VSS	GND	
BK56	VSS	GND	
BK58	VMSE0_DQ[59]	SMI2	I/O
BK6	VSS	GND	
BK8	VMSE3_DQ[4]	SMI2	I/O
BL1	VMSE3_DQ[9]	SMI2	I/O
BL11	VMSE3_DQ[5]	SMI2	I/O
BL13	VSS	GND	
BL15	VSS	GND	
BL17	VSA	PWR	
BL3	VMSE3_DQS_N[1]	SMI2	I/O
BL43	VMSE0_CMD[8]	SMI2	O
BL45	VMSE0_CMD[9]	SMI2	O
BL47	VMSE0_CMD[11]	SMI2	O
BL49	VMSE0_CMD[14]	SMI2	O
BL5	VMSE3_DQ[13]	SMI2	I/O
BL51	QPI1_DTX_DP[0]	QPI	O
BL53	VSS	GND	
BL55	PWRGOOD	CMOS	I
BL57	VMSE0_DQ[62]	SMI2	I/O
BL7	VMSE3_DQ[1]	SMI2	I/O
BL9	VMSE3_DQS_P[0]	SMI2	I/O
BM10	VSS	GND	
BM12	VSS	GND	
BM14	VMSE3_CLK_P	SMI2	O
BM16	VSS	GND	
BM2	VSS	GND	
BM4	VSS	GND	
BM42	VSS	GND	
BM44	VMSE0_CLK_N	SMI2	O

Table 7-2. Land Number (Sheet 17 of 50)

Land No.	Land Name	Buffer Type	Direction
BM46	VMSE0_CMD[13]	SMI2	O
BM48	VMSE0_CMD[10]	SMI2	O
BM50	RSVD		
BM52	VSS	GND	
BM54	VMSE0_DQ[57]	SMI2	I/O
BM56	VMSE0_DQS_P[7]	SMI2	I/O
BM58	VSS	GND	
BM6	VSS	GND	
BM8	VSS	GND	
BN1	VMSE3_DQ[15]	SMI2	I/O
BN11	VMSE3_DQ[6]	SMI2	I/O
BN13	VMSE3_CMD[3]	SMI2	O
BN15	VMSE3_CMD[9]	SMI2	O
BN17	VSA	PWR	
BN3	VMSE3_DQS_P[1]	SMI2	I/O
BN43	VSS	GND	
BN45	VMSE0_CLK_P	SMI2	O
BN47	VSS	GND	
BN49	VSS	GND	
BN5	VMSE3_DQ[14]	SMI2	I/O
BN51	VSS	GND	
BN53	VMSE0_DQ[60]	SMI2	I/O
BN55	VSS	GND	
BN57	VMSE0_DQ[58]	SMI2	I/O
BN7	VMSE3_DQ[7]	SMI2	I/O
BN9	VMSE3_DQS_N[0]	SMI2	I/O
BP10	VMSE3_DQ[3]	SMI2	I/O
BP12	VSS	GND	
BP14	VSS	GND	
BP16	VSS	GND	
BP2	VMSE3_DQ[10]	SMI2	I/O
BP4	VMSE3_DQ[11]	SMI2	I/O
BP42	VTTA	PWR	
BP44	VSS	GND	
BP46	VSS	GND	
BP48	VSS	GND	
BP50	VSS	GND	
BP52	VSS	GND	
BP54	VSS	GND	
BP56	VMSE0_DQS_N[7]	SMI2	I/O
BP58	VMSE0_DQ[63]	SMI2	I/O

Table 7-2. Land Number (Sheet 18 of 50)

Land No.	Land Name	Buffer Type	Direction
BP6	VSS	GND	
BP8	VMSE3_DQ[2]	SMI2	I/O
BR1	VSS	GND	
BR11	VSS	GND	
BR13	VMSE3_CMD[6]	SMI2	O
BR15	VMSE3_CMD[13]	SMI2	O
BR17	VSS	GND	
BR3	VSS	GND	
BR43	VSS	GND	
BR45	RSVD		
BR47	MEM_SDA_C0	Open Drain	I/O
BR49	VMSE0_DQ[49]	SMI2	I/O
BR5	VSS	GND	
BR51	VMSE0_DQ[51]	SMI2	I/O
BR53	VSS	GND	
BR55	VMSE0_DQ[61]	SMI2	I/O
BR57	VSS	GND	
BR7	VSS	GND	
BR9	VSS	GND	
BT10	VSS	GND	
BT12	VMSE3_ERR_N	SMI2	I/O
BT14	TEST_5		
BT16	VMSE3_CMD[14]	SMI2	O
BT2	VSS	GND	
BT4	VSS	GND	
BT42	VTTA	PWR	
BT44	VMSE0_CMD[6]	SMI2	O
BT46	VMSE0_CMD[5]	SMI2	O
BT48	VMSE0_DQ[53]	SMI2	I/O
BT50	VMSE0_DQS_N[6]	SMI2	I/O
BT52	VMSE0_DQ[54]	SMI2	I/O
BT54	VMSE0_DQ[56]	SMI2	I/O
BT56	VSS	GND	
BT58	VSS	GND	
BT6	VMSE3_DQ[20]	SMI2	I/O
BT8	VSS	GND	
BU1	VMSE3_DQ[23]	SMI2	I/O
BU11	VMSE3_CMD[1]	SMI2	O
BU13	VSS	GND	
BU15	VSS	GND	
BU17	VSS	GND	

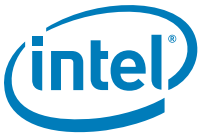

Table 7-2. Land Number (Sheet 19 of 50)

Land No.	Land Name	Buffer Type	Direction
BU3	VMSE3_DQ[17]	SMI2	I/O
BU43	VSS	GND	
BU45	VSS	GND	
BU47	VSS	GND	
BU49	VSS	GND	
BU5	VMSE3_DQS_N[2]	SMI2	I/O
BU51	VSS	GND	
BU53	VSS	GND	
BU55	VSS	GND	
BU57	VMSE0_ECC[3]	SMI2	I/O
BU7	VMSE3_DQ[16]	SMI2	I/O
BU9	VMSE3_CMD[2]	SMI2	O
BV10	TEST_4		
BV12	VSS	GND	
BV14	VMSE3_CMD[11]	SMI2	O
BV16	VMSE3_CMD[12]	SMI2	O
BV2	VSS	GND	
BV4	VSS	GND	
BV42	VTTA	PWR	
BV44	VMSE0_CMD[2]	SMI2	O
BV46	VMSE0_CMD[1]	SMI2	O
BV48	VMSE0_DQ[48]	SMI2	I/O
BV50	VMSE0_DQS_P[6]	SMI2	I/O
BV52	VMSE0_DQ[50]	SMI2	I/O
BV54	VSS	GND	
BV56	VMSE0_DQS_N[8]	SMI2	I/O
BV58	VMSE0_ECC[6]	SMI2	I/O
BV6	VSS	GND	
BV8	VSS	GND	
BW1	VSS	GND	
BW11	VMSE3_CMD[5]	SMI2	O
BW13	VMSE3_CMD[15]	SMI2	O
BW15	VMSE3_CMD[10]	SMI2	O
BW17	VSS	GND	
BW3	VMSE3_DQ[18]	SMI2	I/O
BW43	VSS	GND	
BW45	VMSE0_CMD[7]	SMI2	O
BW47	VSS	GND	
BW49	VMSE0_DQ[52]	SMI2	I/O
BW5	VMSE3_DQS_P[2]	SMI2	I/O
BW51	VMSE0_DQ[55]	SMI2	I/O

Table 7-2. Land Number (Sheet 20 of 50)

Land No.	Land Name	Buffer Type	Direction
BW53	TEST_2		
BW55	VMSE0_ECC[1]	SMI2	I/O
BW57	VSS	GND	
BW7	VMSE3_DQ[21]	SMI2	I/O
BW9	VMSE3_CMD[7]	SMI2	O
BY10	VSS	GND	
BY12	VMSE3_CMD[16]	SMI2	O
BY14	VSS	GND	
BY16	VSS	GND	
BY18	VSS	GND	
BY2	TEST_6		
BY20	VSS	GND	
BY22	VSS	GND	
BY24	VTTA	PWR	
BY26	VSS	GND	
BY28	VSS	GND	
BY30	VTTQ	PWR	
BY32	VSS	GND	
BY34	VSS	GND	
BY36	VTTQ	PWR	
BY38	VSS	GND	
BY4	VMSE3_DQ[19]	SMI2	I/O
BY40	VSS	GND	
BY42	VTTQ	PWR	
BY44	RSVD		
BY46	VSS	GND	
BY48	VMSE0_ERR_N	SMI2	I/O
BY50	VSS	GND	
BY52	VSS	GND	
BY54	VMSE0_ECC[4]	SMI2	I/O
BY56	VMSE0_DQS_P[8]	SMI2	I/O
BY58	VMSE0_ECC[2]	SMI2	I/O
BY6	VMSE3_DQ[22]	SMI2	I/O
BY8	VSS	GND	
C11	PE1_RX_N[14]	PCIEX3	I
C13	PE1_RX_P[10]	PCIEX3	I
C15	VTTA	PWR	
C17	PE1_TX_N[10]	PCIEX3	O
C19	VCC	PWR	
C21	VCC	PWR	
C23	VSS	GND	

Table 7-2. Land Number (Sheet 21 of 50)

Land No.	Land Name	Buffer Type	Direction
C25	VCC	PWR	
C3	RSVD		
C33	VCC	PWR	
C35	QPI0_DRX_DP[3]	QPI	I
C37	QPI0_DRX_DP[5]	QPI	I
C39	QPI0_DRX_DP[7]	QPI	I
C41	QPI0_DRX_DP[9]	QPI	I
C43	QPI0_CLKRX_DP	QPI	I
C45	QPI0_DRX_DP[11]	QPI	I
C47	QPI0_DRX_DP[13]	QPI	I
C49	QPI0_DRX_DP[15]	QPI	I
C5	RSVD		
C51	QPI0_DRX_DN[17]	QPI	I
C53	VSS	GND	
C55	BPM_N[3]	CMOS	I/O
C7	VSS	GND	
C9	VSS	GND	
CA1	VMSE3_DQ[40]	SMI2	I/O
CA11	VSS	GND	
CA13	VSS	GND	
CA15	VSS	GND	
CA17	VSS	GND	
CA19	VSS	GND	
CA21	VSS	GND	
CA23	VSS	GND	
CA25	VSS	GND	
CA27	VSS	GND	
CA29	VSS	GND	
CA3	VSS	GND	
CA31	VSS	GND	
CA33	VSS	GND	
CA35	VSS	GND	
CA37	VSS	GND	
CA39	VSS	GND	
CA41	VSS	GND	
CA43	VSS	GND	
CA45	VSS	GND	
CA47	VSS	GND	
CA49	VSS	GND	
CA5	VSS	GND	
CA51	VSS	GND	

Table 7-2. Land Number (Sheet 22 of 50)

Land No.	Land Name	Buffer Type	Direction
CA53	VSS	GND	
CA55	VSS	GND	
CA57	VMSE0_ECC[7]	SMI2	I/O
CA7	VSS	GND	
CA9	VSS	GND	
CB10	VMSE3_ECC[7]	SMI2	I/O
CB12	VSS	GND	
CB14	VMSE3_DQ[28]	SMI2	I/O
CB16	VMSE3_DQ[24]	SMI2	I/O
CB18	MEM_SCL_C2	Open Drain	I/O
CB2	VMSE3_DQ[45]	SMI2	I/O
CB20	VMSE2_DQ[41]	SMI2	I/O
CB22	VMSE2_DQ[46]	SMI2	I/O
CB24	VSS	GND	
CB26	VMSE2_DQ[37]	SMI2	I/O
CB28	VMSE2_DQ[39]	SMI2	I/O
CB30	VSS	GND	
CB32	VMSE1_DQ[5]	SMI2	I/O
CB34	VMSE1_DQ[7]	SMI2	I/O
CB36	VSS	GND	
CB38	VMSE1_DQ[45]	SMI2	I/O
CB4	VSS	GND	
CB40	VMSE1_DQ[47]	SMI2	I/O
CB42	VSS	GND	
CB44	VMSE1_DQ[57]	SMI2	I/O
CB46	VMSE1_DQ[62]	SMI2	I/O
CB48	MEM_HOT_C01_N	Open Drain	I/O
CB50	VMSE0_DQ[43]	SMI2	I/O
CB52	VMSE0_DQ[42]	SMI2	I/O
CB54	VSS	GND	
CB56	VSS	GND	
CB6	VSS	GND	
CB8	VMSE3_ECC[5]	SMI2	I/O
CC11	VMSE3_ECC[2]	SMI2	I/O
CC13	VMSE3_DQ[25]	SMI2	I/O
CC15	VMSE3_DQS_N[3]	SMI2	I/O
CC17	VMSE3_DQ[29]	SMI2	I/O
CC19	VMSE2_DQ[44]	SMI2	I/O
CC21	VMSE2_DQS_P[5]	SMI2	I/O
CC23	VMSE2_DQ[43]	SMI2	I/O
CC25	VMSE2_DQ[32]	SMI2	I/O

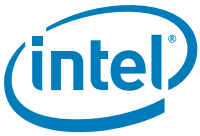

Table 7-2. Land Number (Sheet 23 of 50)

Land No.	Land Name	Buffer Type	Direction
CC27	VMSE2_DQS_N[4]	SMI2	I/O
CC29	VMSE2_DQ[38]	SMI2	I/O
CC3	VMSE3_DQ[41]	SMI2	I/O
CC31	VMSE1_DQ[0]	SMI2	I/O
CC33	VMSE1_DQS_P[0]	SMI2	I/O
CC35	VMSE1_DQ[2]	SMI2	I/O
CC37	VMSE1_DQ[40]	SMI2	I/O
CC39	VMSE1_DQS_N[5]	SMI2	I/O
CC41	VMSE1_DQ[42]	SMI2	I/O
CC43	VMSE1_DQ[60]	SMI2	I/O
CC45	VMSE1_DQS_P[7]	SMI2	I/O
CC47	VMSE1_DQ[59]	SMI2	I/O
CC49	VMSE0_DQ[46]	SMI2	I/O
CC5	VMSE3_DQ[44]	SMI2	I/O
CC51	VMSE0_DQS_P[5]	SMI2	I/O
CC53	VMSE0_DQ[47]	SMI2	I/O
CC55	VMSE0_ECC[5]	SMI2	I/O
CC7	VMSE3_ECC[0]	SMI2	I/O
CC9	VMSE3_DQS_P[8]	SMI2	I/O
CD10	VSS	GND	
CD12	VSS	GND	
CD14	VSS	GND	
CD16	VSS	GND	
CD18	VSS	GND	
CD20	VSS	GND	
CD22	VSS	GND	
CD24	VSS	GND	
CD26	VSS	GND	
CD28	VSS	GND	
CD30	VSS	GND	
CD32	VSS	GND	
CD34	VSS	GND	
CD36	VSS	GND	
CD38	VSS	GND	
CD4	VMSE3_DQS_N[5]	SMI2	I/O
CD40	VSS	GND	
CD42	VSS	GND	
CD44	VSS	GND	
CD46	VSS	GND	
CD48	VSS	GND	
CD50	VSS	GND	

Table 7-2. Land Number (Sheet 24 of 50)

Land No.	Land Name	Buffer Type	Direction
CD52	VSS	GND	
CD54	VVMSE01	PWR	
CD56	VMSE0_ECC[0]	SMI2	I/O
CD6	VSS	GND	
CD8	VSS	GND	
CE11	VMSE3_ECC[3]	SMI2	I/O
CE13	VMSE3_DQ[31]	SMI2	I/O
CE15	VMSE3_DQS_P[3]	SMI2	I/O
CE17	VMSE3_DQ[30]	SMI2	I/O
CE19	VMSE2_DQ[40]	SMI2	I/O
CE21	VMSE2_DQS_N[5]	SMI2	I/O
CE23	VMSE2_DQ[42]	SMI2	I/O
CE25	VMSE2_DQ[36]	SMI2	I/O
CE27	VMSE2_DQS_P[4]	SMI2	I/O
CE29	VMSE2_DQ[35]	SMI2	I/O
CE3	VMSE3_DQS_P[5]	SMI2	I/O
CE31	VMSE1_DQ[4]	SMI2	I/O
CE33	VMSE1_DQS_N[0]	SMI2	I/O
CE35	VMSE1_DQ[3]	SMI2	I/O
CE37	VMSE1_DQ[44]	SMI2	I/O
CE39	VMSE1_DQS_P[5]	SMI2	I/O
CE41	VMSE1_DQ[43]	SMI2	I/O
CE43	VMSE1_DQ[56]	SMI2	I/O
CE45	VMSE1_DQS_N[7]	SMI2	I/O
CE47	VMSE1_DQ[58]	SMI2	I/O
CE49	VMSE0_DQ[45]	SMI2	I/O
CE5	VMSE3_DQ[47]	SMI2	I/O
CE51	VMSE0_DQS_N[5]	SMI2	I/O
CE53	VMSE0_DQ[41]	SMI2	I/O
CE55	VSS	GND	
CE7	VMSE3_ECC[4]	SMI2	I/O
CE9	VMSE3_DQS_N[8]	SMI2	I/O
CF10	VMSE3_ECC[6]	SMI2	I/O
CF12	VVMSE23	PWR	
CF14	VMSE3_DQ[26]	SMI2	I/O
CF16	VMSE3_DQ[27]	SMI2	I/O
CF18	VSS	GND	
CF20	VMSE2_DQ[45]	SMI2	I/O
CF22	VMSE2_DQ[47]	SMI2	I/O
CF24	VVMSE23	PWR	
CF26	VMSE2_DQ[33]	SMI2	I/O

Table 7-2. Land Number (Sheet 25 of 50)

Land No.	Land Name	Buffer Type	Direction
CF28	VMSE2_DQ[34]	SMI2	I/O
CF30	VSS	GND	
CF32	VMSE1_DQ[1]	SMI2	I/O
CF34	VMSE1_DQ[6]	SMI2	I/O
CF36	SVID_IDLE_N	CMOS	O
CF38	VMSE1_DQ[41]	SMI2	I/O
CF4	VSS	GND	
CF40	VMSE1_DQ[46]	SMI2	I/O
CF42	VVMSE01	PWR	
CF44	VMSE1_DQ[61]	SMI2	I/O
CF46	VMSE1_DQ[63]	SMI2	I/O
CF48	VSS	GND	
CF50	VMSE0_DQ[40]	SMI2	I/O
CF52	VMSE0_DQ[44]	SMI2	I/O
CF54	VSS	GND	
CF56	VSS	GND	
CF6	MEM_SCL_C3	Open Drain	I/O
CF8	VMSE3_ECC[1]	SMI2	I/O
CG11	VSS	GND	
CG13	VSS	GND	
CG15	VSS	GND	
CG17	VSS	GND	
CG19	VSS	GND	
CG21	VSS	GND	
CG23	VSS	GND	
CG25	VSS	GND	
CG27	VSS	GND	
CG29	VSS	GND	
CG3	VMSE3_DQ[42]	SMI2	I/O
CG31	VSS	GND	
CG33	VSS	GND	
CG35	VSS	GND	
CG37	VSS	GND	
CG39	VSS	GND	
CG41	VSS	GND	
CG43	VSS	GND	
CG45	VSS	GND	
CG47	VSS	GND	
CG49	VSS	GND	
CG5	VSS	GND	
CG51	VSS	GND	

Table 7-2. Land Number (Sheet 26 of 50)

Land No.	Land Name	Buffer Type	Direction
CG53	VSS	GND	
CG55	VMSE0_DQ[28]	SMI2	I/O
CG7	VSS	GND	
CG9	VSS	GND	
CH10	VSS	GND	
CH12	VSS	GND	
CH14	VSS	GND	
CH16	VSS	GND	
CH18	VSS	GND	
CH20	VSS	GND	
CH22	VSS	GND	
CH24	VSS	GND	
CH26	VSS	GND	
CH28	VSS	GND	
CH30	VSS	GND	
CH32	VSS	GND	
CH34	VSS	GND	
CH36	VSS	GND	
CH38	VSS	GND	
CH4	VMSE3_DQ[46]	SMI2	I/O
CH40	VSS	GND	
CH42	VSS	GND	
CH44	VSS	GND	
CH46	VSS	GND	
CH48	VSS	GND	
CH50	VSS	GND	
CH52	VSS	GND	
CH54	VMSE0_DQ[24]	SMI2	I/O
CH56	VMSE0_DQ[25]	SMI2	I/O
CH6	VSS	GND	
CH8	VSS	GND	
CJ11	MEM_SDA_C2	Open Drain	I/O
CJ13	VMSE2_DQ[5]	SMI2	I/O
CJ15	VMSE2_DQ[7]	SMI2	I/O
CJ17	VSS	GND	
CJ19	VMSE2_DQ[21]	SMI2	I/O
CJ21	VMSE2_DQ[23]	SMI2	I/O
CJ23	VSS	GND	
CJ25	VMSE2_DQ[49]	SMI2	I/O
CJ27	VMSE2_DQ[54]	SMI2	I/O
CJ29	VSS	GND	

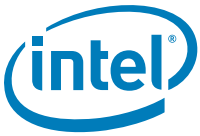

Table 7-2. Land Number (Sheet 27 of 50)

Land No.	Land Name	Buffer Type	Direction
CJ3	VMSE3_DQ[43]	SMI2	I/O
CJ31	VMSE1_DQ[9]	SMI2	I/O
CJ33	VMSE1_DQ[10]	SMI2	I/O
CJ35	VVMSE01	PWR	
CJ37	VMSE1_DQ[37]	SMI2	I/O
CJ39	VMSE1_DQ[39]	SMI2	I/O
CJ41	VSS	GND	
CJ43	VMSE1_DQ[53]	SMI2	I/O
CJ45	VMSE1_DQ[55]	SMI2	I/O
CJ47	VVMSE01	PWR	
CJ49	VMSE0_DQ[35]	SMI2	I/O
CJ5	VVMSE23	PWR	
CJ51	VMSE0_DQ[38]	SMI2	I/O
CJ53	VSS	GND	
CJ55	VSS	GND	
CJ7	VMSE3_DQ[36]	SMI2	I/O
CJ9	VMSE3_DQ[32]	SMI2	I/O
CK10	VMSE3_DQ[37]	SMI2	I/O
CK12	VMSE2_DQ[0]	SMI2	I/O
CK14	VMSE2_DQS_P[0]	SMI2	I/O
CK16	VMSE2_DQ[2]	SMI2	I/O
CK18	VMSE2_DQ[16]	SMI2	I/O
CK20	VMSE2_DQS_N[2]	SMI2	I/O
CK22	VMSE2_DQ[18]	SMI2	I/O
CK24	VMSE2_DQ[52]	SMI2	I/O
CK26	VMSE2_DQS_N[6]	SMI2	I/O
CK28	VMSE2_DQ[51]	SMI2	I/O
CK30	VMSE1_DQ[13]	SMI2	I/O
CK32	VMSE1_DQS_P[1]	SMI2	I/O
CK34	VMSE1_DQ[11]	SMI2	I/O
CK36	VMSE1_DQ[32]	SMI2	I/O
CK38	VMSE1_DQS_N[4]	SMI2	I/O
CK4	VSS	GND	
CK40	VMSE1_DQ[34]	SMI2	I/O
CK42	VMSE1_DQ[48]	SMI2	I/O
CK44	VMSE1_DQS_P[6]	SMI2	I/O
CK46	VMSE1_DQ[50]	SMI2	I/O
CK48	VMSE0_DQ[34]	SMI2	I/O
CK50	VMSE0_DQS_P[4]	SMI2	I/O
CK52	VMSE0_DQ[39]	SMI2	I/O
CK54	VMSE0_DQ[29]	SMI2	I/O

Table 7-2. Land Number (Sheet 28 of 50)

Land No.	Land Name	Buffer Type	Direction
CK56	VSS	GND	
CK6	VMSE3_DQ[33]	SMI2	I/O
CK8	VMSE3_DQS_N[4]	SMI2	I/O
CL11	VSS	GND	
CL13	VSS	GND	
CL15	VSS	GND	
CL17	VSS	GND	
CL19	VSS	GND	
CL21	VSS	GND	
CL23	VSS	GND	
CL25	VSS	GND	
CL27	VSS	GND	
CL29	VSS	GND	
CL3	VSS	GND	
CL31	VSS	GND	
CL33	VSS	GND	
CL35	VSS	GND	
CL37	VSS	GND	
CL39	VSS	GND	
CL41	VSS	GND	
CL43	VSS	GND	
CL45	VSS	GND	
CL47	VSS	GND	
CL49	VSS	GND	
CL5	VSS	GND	
CL51	VSS	GND	
CL53	VSS	GND	
CL55	VMSE0_DQS_P[3]	SMI2	I/O
CL7	VSS	GND	
CL9	VSS	GND	
CM10	VMSE3_DQ[38]	SMI2	I/O
CM12	VMSE2_DQ[4]	SMI2	I/O
CM14	VMSE2_DQS_N[0]	SMI2	I/O
CM16	VMSE2_DQ[3]	SMI2	I/O
CM18	VMSE2_DQ[20]	SMI2	I/O
CM20	VMSE2_DQS_P[2]	SMI2	I/O
CM22	VMSE2_DQ[19]	SMI2	I/O
CM24	VMSE2_DQ[48]	SMI2	I/O
CM26	VMSE2_DQS_P[6]	SMI2	I/O
CM28	VMSE2_DQ[50]	SMI2	I/O
CM30	VMSE1_DQ[8]	SMI2	I/O

Table 7-2. Land Number (Sheet 29 of 50)

Land No.	Land Name	Buffer Type	Direction
CM32	VMSE1_DQS_N[1]	SMI2	I/O
CM34	VMSE1_DQ[14]	SMI2	I/O
CM36	VMSE1_DQ[36]	SMI2	I/O
CM38	VMSE1_DQS_P[4]	SMI2	I/O
CM4	VMSE3_DQ[58]	SMI2	I/O
CM40	VMSE1_DQ[35]	SMI2	I/O
CM42	VMSE1_DQ[52]	SMI2	I/O
CM44	VMSE1_DQS_N[6]	SMI2	I/O
CM46	VMSE1_DQ[51]	SMI2	I/O
CM48	VMSE0_DQ[37]	SMI2	I/O
CM50	VMSE0_DQS_N[4]	SMI2	I/O
CM52	VMSE0_DQ[33]	SMI2	I/O
CM54	VMSE0_DQS_N[3]	SMI2	I/O
CM56	VMSE0_DQ[26]	SMI2	I/O
CM6	VMSE3_DQ[39]	SMI2	I/O
CM8	VMSE3_DQS_P[4]	SMI2	I/O
CN11	VSS	GND	
CN13	VMSE2_DQ[1]	SMI2	I/O
CN15	VMSE2_DQ[6]	SMI2	I/O
CN17	VVMSE23	PWR	
CN19	VMSE2_DQ[17]	SMI2	I/O
CN21	VMSE2_DQ[22]	SMI2	I/O
CN23	VSS	GND	
CN25	VMSE2_DQ[53]	SMI2	I/O
CN27	VMSE2_DQ[55]	SMI2	I/O
CN29	VSS	GND	
CN3	VMSE3_DQ[60]	SMI2	I/O
CN31	VMSE1_DQ[12]	SMI2	I/O
CN33	VMSE1_DQ[15]	SMI2	I/O
CN35	VSS	GND	
CN37	VMSE1_DQ[33]	SMI2	I/O
CN39	VMSE1_DQ[38]	SMI2	I/O
CN41	MEM_SDA_C1	Open Drain	I/O
CN43	VMSE1_DQ[49]	SMI2	I/O
CN45	VMSE1_DQ[54]	SMI2	I/O
CN47	VSS	GND	
CN49	VMSE0_DQ[32]	SMI2	I/O
CN5	VSS	GND	
CN51	VMSE0_DQ[36]	SMI2	I/O
CN53	MEM_SCL_C0	Open Drain	I/O
CN55	VMSE0_DQ[31]	SMI2	I/O

Table 7-2. Land Number (Sheet 30 of 50)

Land No.	Land Name	Buffer Type	Direction
CN57	VMSE0_DQ[30]	SMI2	I/O
CN7	VMSE3_DQ[34]	SMI2	I/O
CN9	VMSE3_DQ[35]	SMI2	I/O
CP10	VSS	GND	
CP12	VSS	GND	
CP14	VSS	GND	
CP16	VSS	GND	
CP18	VSS	GND	
CP2	VSS	GND	
CP20	VSS	GND	
CP22	VSS	GND	
CP24	VVMSE23	PWR	
CP26	VSS	GND	
CP28	VSS	GND	
CP30	VSS	GND	
CP32	VSS	GND	
CP34	VSS	GND	
CP36	VSS	GND	
CP38	VSS	GND	
CP4	VSS	GND	
CP40	VSS	GND	
CP42	VSS	GND	
CP44	VSS	GND	
CP46	VSS	GND	
CP48	VSS	GND	
CP50	VSS	GND	
CP52	VSS	GND	
CP54	VSS	GND	
CP56	VSS	GND	
CP58	VMSE0_DQ[27]	SMI2	I/O
CP6	VSS	GND	
CP8	VSS	GND	
CR1	VMSE3_DQ[56]	SMI2	I/O
CR11	VMSE2_DQ[11]	SMI2	I/O
CR13	VSS	GND	
CR15	VSS	GND	
CR17	VMSE2_CMD[3]	SMI2	O
CR19	VSS	GND	
CR21	VSS	GND	
CR23	VMSE2_CMD[12]	SMI2	O
CR25	VSS	GND	

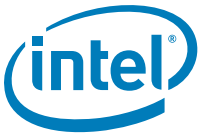

Table 7-2. Land Number (Sheet 31 of 50)

Land No.	Land Name	Buffer Type	Direction
CR27	VSS	GND	
CR29	VVMSE01	PWR	
CR3	VMSE3_DQS_N[7]	SMI2	I/O
CR31	VSS	GND	
CR33	VSS	GND	
CR35	VMSE1_ERR_N	SMI2	I/O
CR37	VSS	GND	
CR39	VSS	GND	
CR41	VMSE1_CMD[9]	SMI2	O
CR43	VSS	GND	
CR45	VSS	GND	
CR47	VSS	GND	
CR49	VSS	GND	
CR5	VMSE3_DQ[59]	SMI2	I/O
CR51	VSS	GND	
CR53	VSS	GND	
CR55	VSS	GND	
CR57	VSS	GND	
CR7	VSS	GND	
CR9	VSS	GND	
CT10	VMSE2_DQ[14]	SMI2	I/O
CT12	VSS	GND	
CT14	VMSE2_CMD[1]	SMI2	O
CT16	VMSE2_CMD[4]	SMI2	O
CT18	VMSE2_CMD[6]	SMI2	O
CT2	VMSE3_DQ[61]	SMI2	I/O
CT20	VMSE2_CMD[16]	SMI2	O
CT22	VMSE2_CMD[10]	SMI2	O
CT24	VSS	GND	
CT26	VSS	GND	
CT28	VSS	GND	
CT30	VSS	GND	
CT32	VSS	GND	
CT34	VSS	GND	
CT36	VMSE1_CMD[2]	SMI2	O
CT38	VMSE1_CMD[4]	SMI2	O
CT4	VMSE3_DQS_P[7]	SMI2	I/O
CT40	VMSE1_CMD[6]	SMI2	O
CT42	VMSE1_CMD[13]	SMI2	O
CT44	VMSE1_CMD[11]	SMI2	O
CT46	RSVD		

Table 7-2. Land Number (Sheet 32 of 50)

Land No.	Land Name	Buffer Type	Direction
CT48	VMSE0_DQ[9]	SMI2	I/O
CT50	VMSE0_DQ[14]	SMI2	I/O
CT52	VVMSE01	PWR	
CT54	VMSE0_DQ[21]	SMI2	I/O
CT56	VMSE0_DQ[23]	SMI2	I/O
CT58	VSS	GND	
CT6	VSS	GND	
CT8	VMSE2_DQ[9]	SMI2	I/O
CU1	RSVD		
CU11	VSS	GND	
CU13	VMSE2_ERR_N	SMI2	I/O
CU15	VMSE2_CMD[5]	SMI2	O
CU17	VSS	GND	
CU19	VMSE2_CMD[13]	SMI2	O
CU21	VMSE2_CMD[11]	SMI2	O
CU23	VSS	GND	
CU25	VMSE2_DQ[57]	SMI2	I/O
CU27	VMSE2_DQ[58]	SMI2	I/O
CU29	VSS	GND	
CU3	VSS	GND	
CU31	VMSE1_DQ[21]	SMI2	I/O
CU33	VMSE1_DQ[23]	SMI2	I/O
CU35	TEST_0		
CU37	VMSE1_CMD[5]	SMI2	O
CU39	VMSE1_CMD[3]	SMI2	O
CU41	VSS	GND	
CU43	VSS	GND	
CU45	VMSE1_CMD[14]	SMI2	O
CU47	VMSE0_DQ[12]	SMI2	I/O
CU49	VMSE0_DQS_P[1]	SMI2	I/O
CU5	VMSE3_DQ[62]	SMI2	I/O
CU51	VMSE0_DQ[11]	SMI2	I/O
CU53	VMSE0_DQ[16]	SMI2	I/O
CU55	VMSE0_DQS_N[2]	SMI2	I/O
CU57	VMSE0_DQ[18]	SMI2	I/O
CU7	VMSE2_DQ[12]	SMI2	I/O
CU9	VMSE2_DQS_P[1]	SMI2	I/O
CV10	VMSE2_DQ[15]	SMI2	I/O
CV12	MEM_HOT_C23_N	Open Drain	I/O
CV14	VSS	GND	
CV16	VSS	GND	

Table 7-2. Land Number (Sheet 33 of 50)

Land No.	Land Name	Buffer Type	Direction
CV18	VMSE2_CLK_P	SMI2	O
CV2	VSS	GND	
CV20	VSS	GND	
CV22	VSS	GND	
CV24	VMSE2_DQ[61]	SMI2	I/O
CV26	VMSE2_DQS_P[7]	SMI2	I/O
CV28	VMSE2_DQ[59]	SMI2	I/O
CV30	VMSE1_DQ[16]	SMI2	I/O
CV32	VMSE1_DQS_N[2]	SMI2	I/O
CV34	VMSE1_DQ[18]	SMI2	I/O
CV36	VSS	GND	
CV38	VSS	GND	
CV4	VMSE3_DQ[63]	SMI2	I/O
CV40	VVMSE01	PWR	
CV42	VSS	GND	
CV44	VSS	GND	
CV46	VSS	GND	
CV48	VSS	GND	
CV50	VSS	GND	
CV52	VSS	GND	
CV54	VSS	GND	
CV56	VSS	GND	
CV58	TEST_7		
CV6	VSS	GND	
CV8	VSS	GND	
CW1	RSVD		
CW11	VMSE2_DQ[10]	SMI2	I/O
CW13	VMSE2_CMD[2]	SMI2	O
CW15	TEST_3		
CW17	VMSE2_CMD[0]	SMI2	O
CW19	VSS	GND	
CW21	VSS	GND	
CW23	VSS	GND	
CW25	VSS	GND	
CW27	VSS	GND	
CW29	VSS	GND	
CW3	VMSE3_DQ[57]	SMI2	I/O
CW31	VSS	GND	
CW33	VSS	GND	
CW35	VSS	GND	
CW37	VMSE1_CMD[1]	SMI2	O

Table 7-2. Land Number (Sheet 34 of 50)

Land No.	Land Name	Buffer Type	Direction
CW39	VSS	GND	
CW41	VMSE1_CLK_P	SMI2	O
CW43	VMSE1_CMD[16]	SMI2	O
CW45	VMSE1_CMD[12]	SMI2	O
CW47	VMSE0_DQ[8]	SMI2	I/O
CW49	VMSE0_DQS_N[1]	SMI2	I/O
CW5	VSS	GND	
CW51	VMSE0_DQ[10]	SMI2	I/O
CW53	VMSE0_DQ[20]	SMI2	I/O
CW55	VMSE0_DQS_P[2]	SMI2	I/O
CW57	VMSE0_DQ[19]	SMI2	I/O
CW7	VMSE2_DQ[8]	SMI2	I/O
CW9	VMSE2_DQS_N[1]	SMI2	I/O
CY10	VSS	GND	
CY12	VSS	GND	
CY14	VMSE2_CMD[7]	SMI2	O
CY16	VMSE2_CMD[8]	SMI2	O
CY18	VMSE2_CLK_N	SMI2	O
CY2	VSS	GND	
CY20	VMSE2_CMD[15]	SMI2	O
CY22	VMSE2_CMD[14]	SMI2	O
CY24	VMSE2_DQ[56]	SMI2	I/O
CY26	VMSE2_DQS_N[7]	SMI2	I/O
CY28	VMSE2_DQ[62]	SMI2	I/O
CY30	VMSE1_DQ[20]	SMI2	I/O
CY32	VMSE1_DQS_P[2]	SMI2	I/O
CY34	VMSE1_DQ[19]	SMI2	I/O
CY36	VMSE1_CMD[7]	SMI2	O
CY38	VMSE1_CMD[8]	SMI2	O
CY4	VSS	GND	
CY40	VMSE1_CLK_N	SMI2	O
CY42	VMSE1_CMD[15]	SMI2	O
CY44	VMSE1_CMD[10]	SMI2	O
CY46	VSS	GND	
CY48	VMSE0_DQ[13]	SMI2	I/O
CY50	VMSE0_DQ[15]	SMI2	I/O
CY52	VSS	GND	
CY54	VMSE0_DQ[17]	SMI2	I/O
CY56	VMSE0_DQ[22]	SMI2	I/O
CY58	EAR_N	CMOS	I/O
CY6	VVMSE23	PWR	

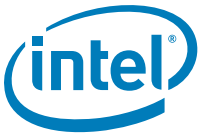

Table 7-2. Land Number (Sheet 35 of 50)

Land No.	Land Name	Buffer Type	Direction
CY8	VMSE2_DQ[13]	SMI2	I/O
D10	PE1_RX_P[14]	PCIEX3	I
D12	VSS	GND	
D14	PE1_RX_N[11]	PCIEX3	I
D16	PE1_TX_P[10]	PCIEX3	O
D18	VSS	GND	
D2	RSVD		
D20	VCC	PWR	
D22	VCC	PWR	
D24	VSS	GND	
D26	VCC	PWR	
D32	VCC	PWR	
D34	VSS	GND	
D36	QPI0_DRX_DP[4]	QPI	I
D38	QPI0_DRX_DP[6]	QPI	I
D4	RSVD		
D40	QPI0_DRX_DP[8]	QPI	I
D42	VTTA	PWR	
D44	QPI0_DRX_DP[10]	QPI	I
D46	QPI0_DRX_DP[12]	QPI	I
D48	QPI0_DRX_DP[14]	QPI	I
D50	QPI0_DRX_DP[16]	QPI	I
D52	QPI0_DRX_DN[18]	QPI	I
D54	BPM_N[6]	CMOS	I/O
D56	BPM_N[7]	CMOS	I/O
D6	VSS	GND	
D8	VSS	GND	
DA11	VSS	GND	
DA13	VSS	GND	
DA15	VSS	GND	
DA17	VSS	GND	
DA19	VMSE2_CMD[9]	SMI2	O
DA21	VSS	GND	
DA23	VSS	GND	
DA25	VMSE2_DQ[60]	SMI2	I/O
DA27	VMSE2_DQ[63]	SMI2	I/O
DA29	MEM_SCL_C1	Open Drain	I/O
DA3	RSVD		
DA31	VMSE1_DQ[17]	SMI2	I/O
DA33	VMSE1_DQ[22]	SMI2	I/O
DA35	VSS	GND	

Table 7-2. Land Number (Sheet 36 of 50)

Land No.	Land Name	Buffer Type	Direction
DA37	VSS	GND	
DA39	VMSE1_CMD[0]	SMI2	O
DA41	VSS	GND	
DA43	VSS	GND	
DA45	VSS	GND	
DA47	VSS	GND	
DA49	VSS	GND	
DA5	VMSE3_DQ[48]	SMI2	I/O
DA51	VSS	GND	
DA53	VSS	GND	
DA55	VSS	GND	
DA57	RSVD		
DA7	VSS	GND	
DA9	VSS	GND	
DB10	VMSE3_DQ[54]	SMI2	I/O
DB12	VVMSE23	PWR	
DB14	VSS	GND	
DB16	VSS	GND	
DB18	VSS	GND	
DB2	RSVD		
DB20	VSS	GND	
DB22	VSS	GND	
DB24	VSS	GND	
DB26	VSS	GND	
DB28	VSS	GND	
DB30	VSS	GND	
DB32	VSS	GND	
DB34	VSS	GND	
DB36	VSS	GND	
DB38	VSS	GND	
DB4	RSVD		
DB40	VSS	GND	
DB42	VSS	GND	
DB44	VSS	GND	
DB46	VVMSE01	PWR	
DB48	VSS	GND	
DB50	VSS	GND	
DB52	VSS	GND	
DB54	TEST_10		
DB56	RSVD		
DB58	VSS	GND	

Table 7-2. Land Number (Sheet 37 of 50)

Land No.	Land Name	Buffer Type	Direction
DB6	VMSE3_DQ[53]	SMI2	I/O
DB8	VSS	GND	
DC11	VMSE3_DQ[51]	SMI2	I/O
DC13	VMSE2_DQ[29]	SMI2	I/O
DC15	VMSE2_DQ[25]	SMI2	I/O
DC17	VMSE2_DQ[26]	SMI2	I/O
DC19	VMSE_PWR_OK	SMI2	I
DC21	VMSE2_ECC[4]	SMI2	I/O
DC23	VMSE2_ECC[7]	SMI2	I/O
DC25	VVMSE23	PWR	
DC3	RSVD		
DC33	VSS	GND	
DC35	VMSE1_DQ[25]	SMI2	I/O
DC37	VMSE1_DQ[26]	SMI2	I/O
DC39	RSVD		
DC41	VMSE1_ECC[4]	SMI2	I/O
DC43	VMSE1_ECC[7]	SMI2	I/O
DC45	VMSE1_ECC[6]	SMI2	I/O
DC47	VMSE0_DQ[5]	SMI2	I/O
DC49	VMSE0_DQ[1]	SMI2	I/O
DC5	RSVD		
DC51	VMSE0_DQ[2]	SMI2	I/O
DC53	VMSE0_DQ[3]	SMI2	I/O
DC55	RSVD		
DC7	VMSE3_DQ[52]	SMI2	I/O
DC9	VMSE3_DQS_N[6]	SMI2	I/O
DD10	VSS	GND	
DD12	VSS	GND	
DD14	VSS	GND	
DD16	VMSE2_DQS_P[3]	SMI2	I/O
DD18	VMSE2_DQ[30]	SMI2	I/O
DD20	VMSE2_ECC[5]	SMI2	I/O
DD22	VMSE2_DQS_P[8]	SMI2	I/O
DD24	VSS	GND	
DD26	VMSE2_ECC[3]	SMI2	I/O
DD32	VMSE1_DQ[24]	SMI2	I/O
DD34	VSS	GND	
DD36	VMSE1_DQS_P[3]	SMI2	I/O
DD38	VMSE1_DQ[30]	SMI2	I/O
DD40	VMSE1_ECC[5]	SMI2	I/O
DD42	VMSE1_DQS_P[8]	SMI2	I/O

Table 7-2. Land Number (Sheet 38 of 50)

Land No.	Land Name	Buffer Type	Direction
DD44	VSS	GND	
DD46	VSS	GND	
DD48	VSS	GND	
DD50	VMSE0_DQS_N[0]	SMI2	I/O
DD52	VMSE0_DQ[6]	SMI2	I/O
DD54	VSS	GND	
DD6	RSVD		
DD8	VMSE3_DQ[49]	SMI2	I/O
DE11	VMSE3_DQ[50]	SMI2	I/O
DE13	VMSE2_DQ[24]	SMI2	I/O
DE15	VMSE2_DQS_N[3]	SMI2	I/O
DE17	VSS	GND	
DE19	VSS	GND	
DE21	VSS	GND	
DE23	VMSE2_DQS_N[8]	SMI2	I/O
DE25	VMSE2_ECC[6]	SMI2	I/O
DE33	VMSE1_DQ[29]	SMI2	I/O
DE35	VMSE1_DQS_N[3]	SMI2	I/O
DE37	VSS	GND	
DE39	VSS	GND	
DE41	VSS	GND	
DE43	VMSE1_DQS_N[8]	SMI2	I/O
DE45	VMSE1_ECC[3]	SMI2	I/O
DE47	VMSE0_DQ[0]	SMI2	I/O
DE49	VMSE0_DQS_P[0]	SMI2	I/O
DE51	VSS	GND	
DE53	RSVD		
DE55	TEST_1		
DE7	VSS	GND	
DE9	VMSE3_DQS_P[6]	SMI2	I/O
DF10	VMSE3_DQ[55]	SMI2	I/O
DF12	VSS	GND	
DF14	VMSE2_DQ[28]	SMI2	I/O
DF16	VMSE2_DQ[31]	SMI2	I/O
DF18	VMSE2_DQ[27]	SMI2	I/O
DF20	VMSE2_ECC[0]	SMI2	I/O
DF22	VMSE2_ECC[1]	SMI2	I/O
DF24	VMSE2_ECC[2]	SMI2	I/O
DF26	VSS	GND	
DF34	VMSE1_DQ[28]	SMI2	I/O
DF36	VMSE1_DQ[31]	SMI2	I/O

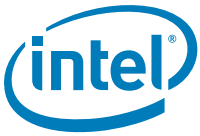

Table 7-2. Land Number (Sheet 39 of 50)

Land No.	Land Name	Buffer Type	Direction
DF38	VMSE1_DQ[27]	SMI2	I/O
DF40	VMSE1_ECC[0]	SMI2	I/O
DF42	VMSE1_ECC[1]	SMI2	I/O
DF44	VMSE1_ECC[2]	SMI2	I/O
DF46	VSS	GND	
DF48	VMSE0_DQ[4]	SMI2	I/O
DF50	VMSE0_DQ[7]	SMI2	I/O
DF52	RSVD		
DF8	VSS	GND	
E1	VSS	GND	
E11	PE1_RX_N[12]	PCIEX3	I
E13	PE1_RX_P[11]	PCIEX3	I
E15	VSS	GND	
E17	PE1_TX_N[8]	PCIEX3	O
E19	VSS	GND	
E21	VCC	PWR	
E23	VSS	GND	
E25	VCC	PWR	
E27	VCC	PWR	
E29	VSS	GND	
E3	RSVD		
E31	VCC	PWR	
E33	VCC	PWR	
E35	VSS	GND	
E37	VSS	GND	
E39	VSS	GND	
E41	VSS	GND	
E43	VSS	GND	
E45	VSS	GND	
E47	VSS	GND	
E49	VSS	GND	
E5	VSS	GND	
E51	QPI0_DRX_DP[17]	QPI	I
E53	QPI0_DRX_DN[19]	QPI	I
E55	VSS	GND	
E57	BPM_N[2]	CMOS	I/O
E7	QPI2_DTX_DN[0]	QPI	O
E9	VTTA	PWR	
F10	PE1_RX_P[12]	PCIEX3	I
F12	VTTA	PWR	
F14	PE1_RX_N[9]	PCIEX3	I

Table 7-2. Land Number (Sheet 40 of 50)

Land No.	Land Name	Buffer Type	Direction
F16	PE1_TX_P[8]	PCIEX3	O
F18	VSS	GND	
F2	RSVD		
F20	VCC	PWR	
F22	VCC	PWR	
F24	VSS	GND	
F26	VCC	PWR	
F28	VCC	PWR	
F30	VSS	GND	
F32	VCC	PWR	
F34	QPI0_DRX_DN[0]	QPI	I
F36	VTTA	PWR	
F38	VTTA	PWR	
F4	QPI2_DRX_DN[0]	QPI	I
F40	VSS	GND	
F42	VTTA	PWR	
F44	VSS	GND	
F46	VSS	GND	
F48	VSS	GND	
F50	VSS	GND	
F52	QPI0_DRX_DP[18]	QPI	I
F54	VSS	GND	
F56	QPI1_DRX_DN[19]	QPI	I
F58	RSVD		
F6	QPI2_DTX_DP[0]	QPI	O
F8	VSS	GND	
G1	VSS	GND	
G11	PE1_RX_N[7]	PCIEX3	I
G13	PE1_RX_P[9]	PCIEX3	I
G15	VSS	GND	
G17	PE1_TX_N[7]	PCIEX3	O
G19	VSS	GND	
G21	VCC	PWR	
G23	VSS	GND	
G25	VCC	PWR	
G27	VCC	PWR	
G29	VSS	GND	
G3	QPI2_DRX_DP[0]	QPI	I
G31	VCC	PWR	
G33	VCC	PWR	
G35	QPI0_DRX_DN[1]	QPI	I

Table 7-2. Land Number (Sheet 41 of 50)

Land No.	Land Name	Buffer Type	Direction
G37	RSVD		
G39	PE0_TX_N[8]	PCIEX3	O
G41	PE0_TX_N[10]	PCIEX3	O
G43	PE0_RX_N[8]	PCIEX3	I
G45	PE0_RX_N[10]	PCIEX3	I
G47	VTTA	PWR	
G49	QPI0_DTX_DN[0]	QPI	O
G5	VSS	GND	
G51	VSS	GND	
G53	QPI0_DRX_DP[19]	QPI	I
G55	QPI1_DRX_DP[19]	QPI	I
G57	VSS	GND	
G7	QPI2_DTX_DN[1]	QPI	O
G9	VSS	GND	
H10	PE1_RX_P[7]	PCIEX3	I
H12	VSS	GND	
H14	PE1_RX_N[8]	PCIEX3	I
H16	PE1_TX_P[7]	PCIEX3	O
H18	VSS	GND	
H2	QPI2_DRX_DN[2]	QPI	I
H20	VCC	PWR	
H22	VCC	PWR	
H24	VSS	GND	
H26	VCC	PWR	
H28	VCC	PWR	
H30	VSS	GND	
H32	VCC	PWR	
H34	QPI0_DRX_DP[0]	QPI	I
H36	QPI0_DRX_DN[2]	QPI	I
H38	PE0_TX_N[7]	PCIEX3	O
H4	QPI2_DRX_DN[1]	QPI	I
H40	PE0_TX_N[9]	PCIEX3	O
H42	VSS	GND	
H44	PE0_RX_N[9]	PCIEX3	I
H46	PE0_RX_N[11]	PCIEX3	I
H48	QPI0_DTX_DP[0]	QPI	O
H50	VTTA	PWR	
H52	VSS	GND	
H54	VTTA	PWR	
H56	QPI1_DRX_DN[18]	QPI	I
H58	RSVD		

Table 7-2. Land Number (Sheet 42 of 50)

Land No.	Land Name	Buffer Type	Direction
H6	QPI2_DTX_DP[1]	QPI	O
H8	EX_LEGACY_SKT	CMOS	I
J1	QPI2_DRX_DP[2]	QPI	I
J11	PE1_RX_N[6]	PCIEX3	I
J13	PE1_RX_P[8]	PCIEX3	I
J15	VTTQ	PWR	
J17	PE1_TX_N[6]	PCIEX3	O
J19	VSS	GND	
J21	VCC	PWR	
J23	VSS	GND	
J25	VCC	PWR	
J27	VCC	PWR	
J29	VSS	GND	
J3	QPI2_DRX_DP[1]	QPI	I
J31	VCC	PWR	
J33	VCC	PWR	
J35	QPI0_DRX_DP[1]	QPI	I
J37	RSVD		
J39	PE0_TX_P[8]	PCIEX3	O
J41	PE0_TX_P[10]	PCIEX3	O
J43	PE0_RX_P[8]	PCIEX3	I
J45	PE0_RX_P[10]	PCIEX3	I
J47	VTTA	PWR	
J49	QPI0_DTX_DN[1]	QPI	O
J5	VSS	GND	
J51	VTT_SENSE		O
J53	RSVD		
J55	QPI1_DRX_DP[18]	QPI	I
J57	VSS	GND	
J7	QPI2_DTX_DN[2]	QPI	O
J9	VTTQ	PWR	
K10	PE1_RX_P[6]	PCIEX3	I
K12	VSS	GND	
K14	VTTQ	PWR	
K16	PE1_TX_P[6]	PCIEX3	O
K18	VSS	GND	
K2	VSS	GND	
K20	VCC	PWR	
K22	VCC	PWR	
K24	VSS	GND	
K26	VCC	PWR	

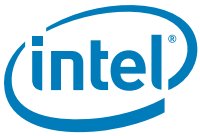

Table 7-2. Land Number (Sheet 43 of 50)

Land No.	Land Name	Buffer Type	Direction
K28	VCC	PWR	
K30	VSS	GND	
K32	VCC	PWR	
K34	VSS	GND	
K36	QPI0_DRX_DP[2]	QPI	I
K38	PE0_TX_P[7]	PCIEX3	O
K4	QPI2_DRX_DN[3]	QPI	I
K40	PE0_TX_P[9]	PCIEX3	O
K42	VSS	GND	
K44	PE0_RX_P[9]	PCIEX3	I
K46	PE0_RX_P[11]	PCIEX3	I
K48	QPI0_DTX_DP[1]	QPI	O
K50	VSS	GND	
K52	RSVD		
K54	VSS	GND	
K56	QPI1_DRX_DN[17]	QPI	I
K58	BPM_N[0]	CMOS	I/O
K6	QPI2_DTX_DP[2]	QPI	O
K8	VSS	GND	
L1	VSS	GND	
L11	PE1_RX_N[5]	PCIEX3	I
L13	VSS	GND	
L15	VSS	GND	
L17	PE1_TX_N[5]	PCIEX3	O
L19	VSS	GND	
L21	VCC	PWR	
L23	VSS	GND	
L25	VCC	PWR	
L27	VCC	PWR	
L29	VSS	GND	
L3	QPI2_DRX_DP[3]	QPI	I
L31	VCC	PWR	
L33	VCC	PWR	
L35	VSS	GND	
L37	VSS	GND	
L39	VSS	GND	
L41	VSS	GND	
L43	VSS	GND	
L45	VSS	GND	
L47	VSS	GND	
L49	QPI0_DTX_DN[2]	QPI	O

Table 7-2. Land Number (Sheet 44 of 50)

Land No.	Land Name	Buffer Type	Direction
L5	PIROM_ADDR[1]		I/O
L51	VSS_VTT_SENSE		O
L53	QPI0_DTX_DN[3]	QPI	O
L55	QPI1_DRX_DP[17]	QPI	I
L57	BPM_N[1]	CMOS	I/O
L7	QPI2_DTX_DN[3]	QPI	O
L9	VSS	GND	
M10	PE1_RX_P[5]	PCIEX3	I
M12	VTTA	PWR	
M14	PE1_TX_N[13]	PCIEX3	O
M16	PE1_TX_P[5]	PCIEX3	O
M18	VSS	GND	
M2	VSS	GND	
M20	VCC	PWR	
M22	VCC	PWR	
M24	VSS	GND	
M26	VCC	PWR	
M28	VCC	PWR	
M30	VSS	GND	
M32	VCC	PWR	
M34	VSS	GND	
M36	VSS	GND	
M38	VSS	GND	
M4	QPI2_DRX_DN[4]	QPI	I
M40	VSS	GND	
M42	VTTA	PWR	
M44	VSS	GND	
M46	VSS	GND	
M48	QPI0_DTX_DP[2]	QPI	O
M50	VSS	GND	
M52	QPI0_DTX_DP[3]	QPI	O
M54	TSC_SYNC	Open Drain	I/O
M56	QPI1_DRX_DN[16]	QPI	I
M6	QPI2_DTX_DP[3]	QPI	O
M8	VSS	GND	
N11	PE1_RX_N[4]	PCIEX3	I
N13	PE1_TX_P[13]	PCIEX3	O
N15	VTTA	PWR	
N17	PE1_TX_N[4]	PCIEX3	O
N19	VSS	GND	
N21	VCC	PWR	

Table 7-2. Land Number (Sheet 45 of 50)

Land No.	Land Name	Buffer Type	Direction
N23	VSS	GND	
N25	VCC	PWR	
N27	VCC	PWR	
N29	VSS	GND	
N3	QPI2_DRX_DP[4]	QPI	I
N31	VCC	PWR	
N33	VCC	PWR	
N35	PE0_TX_N[3]	PCIEX3	O
N37	PE0_TX_N[5]	PCIEX3	O
N39	PE0_TX_N[2]	PCIEX3	O
N41	PE0_TX_N[0]	PCIEX3	O
N43	PE0_TX_N[12]	PCIEX3	O
N45	PE0_TX_N[14]	PCIEX3	O
N47	VTTA	PWR	
N49	QPI1_DTX_DN[19]	QPI	O
N5	VSS	GND	
N51	VSS	GND	
N53	QPI0_DTX_DN[4]	QPI	O
N55	QPI1_DRX_DP[16]	QPI	I
N7	QPI2_DTX_DN[4]	QPI	O
N9	VTTQ	PWR	
P10	PE1_RX_P[4]	PCIEX3	I
P12	VSS	GND	
P14	PE1_TX_N[14]	PCIEX3	O
P16	PE1_TX_P[4]	PCIEX3	O
P18	VSS	GND	
P20	VCC	PWR	
P22	VCC	PWR	
P24	VSS	GND	
P26	VCC	PWR	
P28	VCC	PWR	
P30	VSS	GND	
P32	VCC	PWR	
P34	VSS	GND	
P36	PE0_TX_N[4]	PCIEX3	O
P38	PE0_TX_N[6]	PCIEX3	O
P4	QPI2_DRX_DN[5]	QPI	I
P40	PE0_TX_N[1]	PCIEX3	O
P42	PE0_TX_N[11]	PCIEX3	O
P44	PE0_TX_N[13]	PCIEX3	O
P46	PE0_TX_N[15]	PCIEX3	O

Table 7-2. Land Number (Sheet 46 of 50)

Land No.	Land Name	Buffer Type	Direction
P48	QPI1_DTX_DP[19]	QPI	O
P50	VTTA	PWR	
P52	QPI0_DTX_DP[4]	QPI	O
P54	VSS	GND	
P56	QPI1_DRX_DN[15]	QPI	I
P6	QPI2_DTX_DP[4]	QPI	O
P8	PIROM_ADDR[2]		I/O
R11	PE1_RX_N[3]	PCIEX3	I
R13	PE1_TX_P[14]	PCIEX3	O
R15	VSS	GND	
R17	PE1_TX_N[3]	PCIEX3	O
R19	VSS	GND	
R21	VCC	PWR	
R23	VSS	GND	
R25	VCC	PWR	
R27	VCC	PWR	
R29	VSS	GND	
R3	QPI2_DRX_DP[5]	QPI	I
R31	VCC	PWR	
R33	VCC	PWR	
R35	PE0_TX_P[3]	PCIEX3	O
R37	PE0_TX_P[5]	PCIEX3	O
R39	PE0_TX_P[2]	PCIEX3	O
R41	PE0_TX_P[0]	PCIEX3	O
R43	PE0_TX_P[12]	PCIEX3	O
R45	PE0_TX_P[14]	PCIEX3	O
R47	VSS	GND	
R49	QPI1_DTX_DN[18]	QPI	O
R5	VSS	GND	
R51	VSS	GND	
R53	QPI0_DTX_DN[5]	QPI	O
R55	QPI1_DRX_DP[15]	QPI	I
R7	QPI2_DTX_DN[5]	QPI	O
R9	VSS	GND	
T10	PE1_RX_P[3]	PCIEX3	I
T12	VTTA	PWR	
T14	PE1_TX_N[15]	PCIEX3	O
T16	PE1_TX_P[3]	PCIEX3	O
T18	VSS	GND	
T20	VCC	PWR	
T22	VCC	PWR	

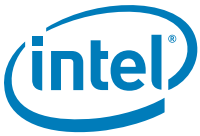

Table 7-2. Land Number (Sheet 47 of 50)

Land No.	Land Name	Buffer Type	Direction
T24	VSS	GND	
T26	VCC	PWR	
T28	VCC	PWR	
T30	VSS	GND	
T32	VCC	PWR	
T34	VSS	GND	
T36	PE0_TX_P[4]	PCIEX3	O
T38	PE0_TX_P[6]	PCIEX3	O
T4	QPI2_DRX_DN[6]	QPI	I
T40	PE0_TX_P[1]	PCIEX3	O
T42	PE0_TX_P[11]	PCIEX3	O
T44	PE0_TX_P[13]	PCIEX3	O
T46	PE0_TX_P[15]	PCIEX3	O
T48	QPI1_DTX_DP[18]	QPI	O
T50	VSS	GND	
T52	QPI0_DTX_DP[5]	QPI	O
T54	VSS	GND	
T56	QPI1_DRX_DN[14]	QPI	I
T6	QPI2_DTX_DP[5]	QPI	O
T8	VSS	GND	
U11	PE1_RX_N[2]	PCIEX3	I
U13	PE1_TX_P[15]	PCIEX3	O
U15	VSS	GND	
U17	PE1_TX_N[2]	PCIEX3	O
U19	VSS	GND	
U21	VCC	PWR	
U23	VSS	GND	
U25	VCC	PWR	
U27	VCC	PWR	
U29	VSS	GND	
U3	QPI2_DRX_DP[6]	QPI	I
U31	VCC	PWR	
U33	VCC	PWR	
U35	VSS	GND	
U37	VSS	GND	
U39	VSS	GND	
U41	VSS	GND	
U43	VSS	GND	
U45	VSS	GND	
U47	VSS	GND	
U49	QPI1_DTX_DN[17]	QPI	O

Table 7-2. Land Number (Sheet 48 of 50)

Land No.	Land Name	Buffer Type	Direction
U5	VSS	GND	
U51	VTTA	PWR	
U53	QPI0_DTX_DN[6]	QPI	O
U55	QPI1_DRX_DP[14]	QPI	I
U7	QPI2_DTX_DN[6]	QPI	O
U9	VSS	GND	
V10	PE1_RX_P[2]	PCIEX3	I
V12	VSS	GND	
V14	PE1_TX_N[12]	PCIEX3	O
V16	PE1_TX_P[2]	PCIEX3	O
V18	VSS	GND	
V20	VCC	PWR	
V22	VCC	PWR	
V24	VSS	GND	
V26	VCC	PWR	
V28	VCC	PWR	
V30	VSS	GND	
V32	VCC	PWR	
V34	VSS	GND	
V36	VTTA	PWR	
V38	VSS	GND	
V4	QPI2_DRX_DN[7]	QPI	I
V40	VSS	GND	
V42	VTTA	PWR	
V44	VTTA	PWR	
V46	VTTA	PWR	
V48	QPI1_DTX_DP[17]	QPI	O
V50	VSS	GND	
V52	QPI0_DTX_DP[6]	QPI	O
V54	SOCKET_ID[2]	CMOS	I
V56	QPI1_DRX_DN[13]	QPI	I
V6	QPI2_DTX_DP[6]	QPI	O
V8	VSS	GND	
W11	PE1_RX_N[1]	PCIEX3	I
W13	PE1_TX_P[12]	PCIEX3	O
W15	VSS	GND	
W17	PE1_TX_N[1]	PCIEX3	O
W19	VSS	GND	
W21	VCC	PWR	
W23	VSS	GND	
W25	VCC	PWR	

Table 7-2. Land Number (Sheet 49 of 50)

Land No.	Land Name	Buffer Type	Direction
W27	VCC	PWR	
W29	VSS	GND	
W3	QPI2_DRX_DP[7]	QPI	I
W31	VCC	PWR	
W33	VCC	PWR	
W35	PE0_RX_N[0]	PCIEX3	I
W37	PE0_RX_N[2]	PCIEX3	I
W39	PE0_RX_N[4]	PCIEX3	I
W41	PE0_RX_N[6]	PCIEX3	I
W43	PE0_RX_N[12]	PCIEX3	I
W45	PE0_RX_N[15]	PCIEX3	I
W47	RSVD		
W49	QPI1_DTX_DN[16]	QPI	O
W5	VSS	GND	
W51	VSS	GND	
W53	QPI0_DTX_DN[7]	QPI	O
W55	QPI1_DRX_DP[13]	QPI	I
W7	QPI2_DTX_DN[7]	QPI	O
W9	VTTQ	PWR	
Y10	PE1_RX_P[1]	PCIEX3	I
Y12	VSS	GND	
Y14	PE1_TX_N[11]	PCIEX3	O
Y16	PE1_TX_P[1]	PCIEX3	O
Y18	VSS	GND	
Y20	VCC	PWR	
Y22	VCC	PWR	
Y24	VSS	GND	

Table 7-2. Land Number (Sheet 50 of 50)

Land No.	Land Name	Buffer Type	Direction
Y26	VCC	PWR	
Y28	VCC	PWR	
Y30	VSS	GND	
Y32	VCC	PWR	
Y34	VSS	GND	
Y36	PE0_RX_N[1]	PCIEX3	I
Y38	PE0_RX_N[3]	PCIEX3	I
Y4	QPI2_DRX_DN[8]	QPI	I
Y40	PE0_RX_N[5]	PCIEX3	I
Y42	PE0_RX_N[7]	PCIEX3	I
Y44	PE0_RX_N[13]	PCIEX3	I
Y46	PE0_RX_N[14]	PCIEX3	I
Y48	QPI1_DTX_DP[16]	QPI	O
Y50	VTTA	PWR	
Y52	QPI0_DTX_DP[7]	QPI	O
Y54	VSS	GND	
Y56	QPI1_DRX_DN[12]	QPI	I
Y6	QPI2_DTX_DP[7]	QPI	O
Y8	PIROM_ADDR[0]		I/O

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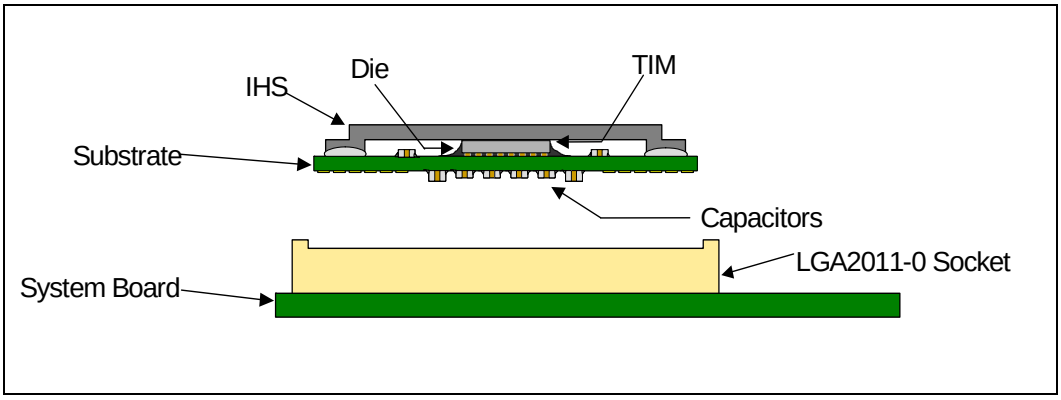
8 Package Mechanical Specifications

The Intel® Xeon® E7v2 processor is packaged in a Flip-Chip Land Grid Array (FCLGA10) package that interfaces with the baseboard via an LGA2011-1 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 8-1 shows a sketch of the processor package components and how they are assembled together. Refer to the *Intel® Xeon® Processor E7-2800/4800/8800 v2 Processor Family Thermal/Mechanical Design Guide* for complete details on the LGA2011-1 socket.

The package components shown in Figure 8-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor core (die)
4. Package substrate
5. Capacitors

Figure 8-1. Processor Package Assembly Sketch

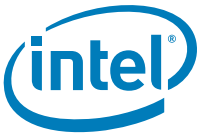


Note:
1. Socket and baseboard are included for reference and are not part of processor package.

8.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 8-2 and Figure 8-3. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference with tolerances (total height, length, width, and so forth)
2. IHS parallelism and tilt
3. Land dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums



6. All drawing dimensions are in mm.
7. Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the *Intel® Xeon® Processor E7-2800/4800/8800 v2 Processor Family Thermal/Mechanical Design Guide*.

Figure 8-2. Processor Package Drawing Sheet 1 of 2

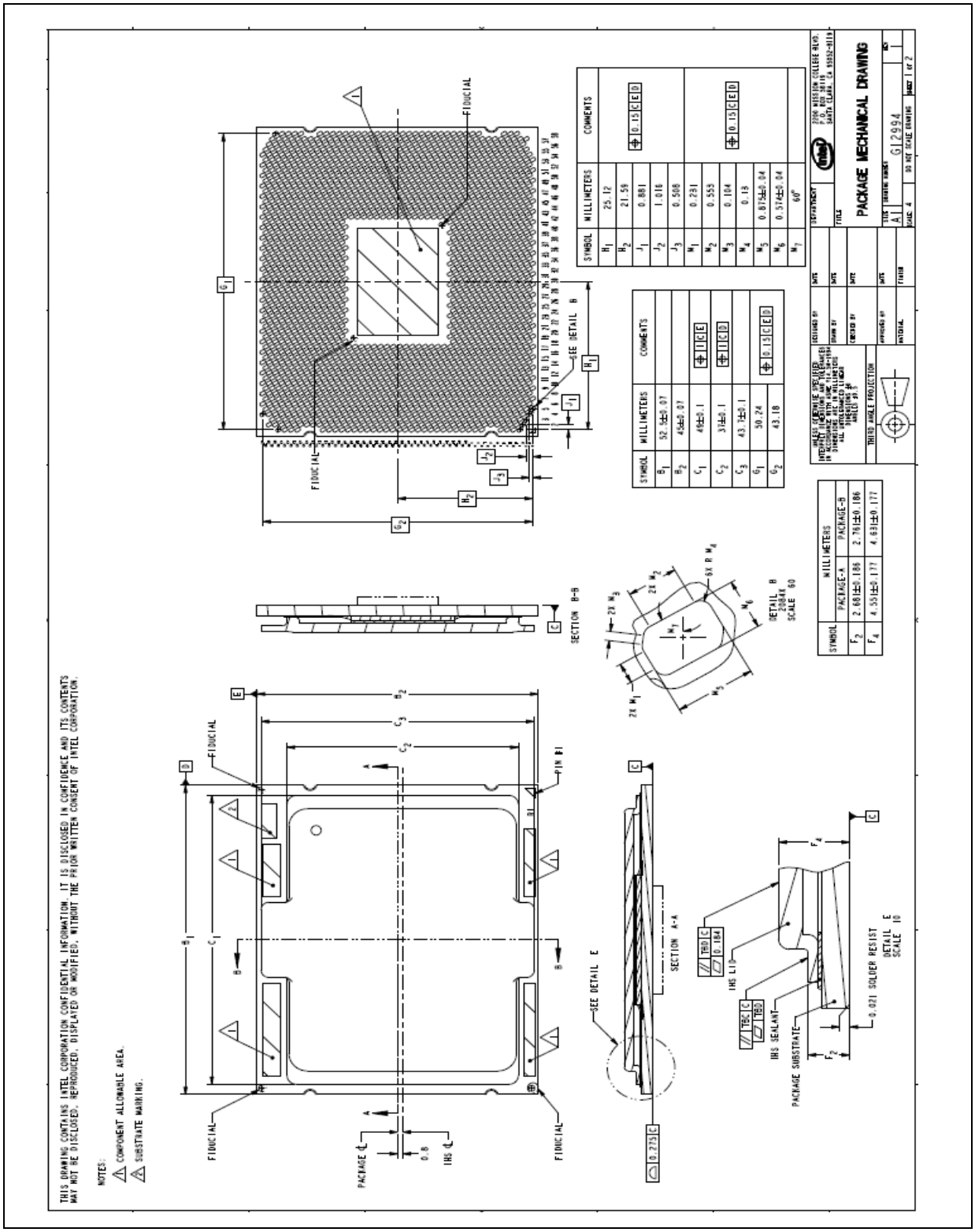
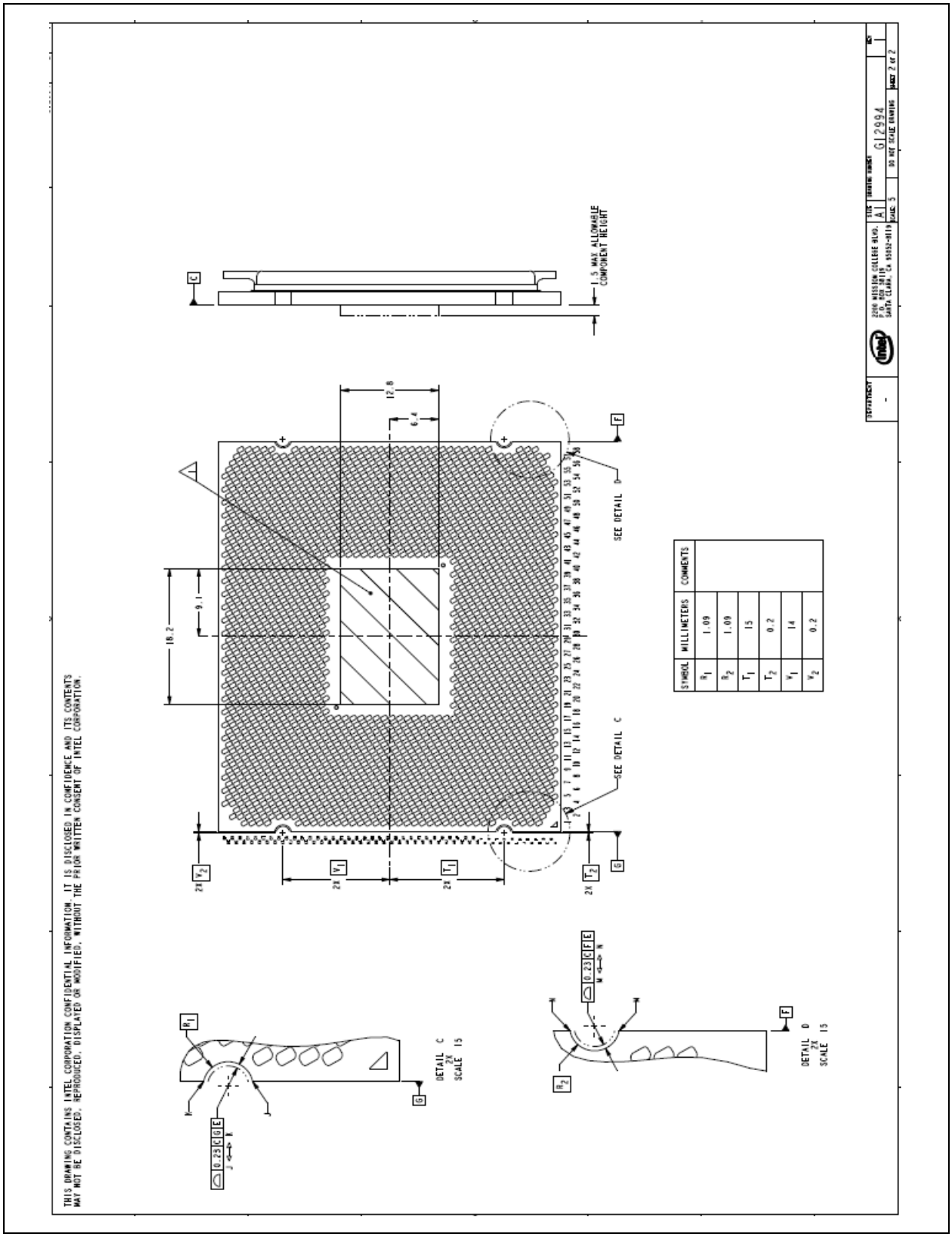
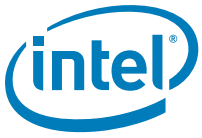


Figure 8-3. Processor Package Drawing Sheet 2 of 2





8.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Do not contact the Test Pad Area with conductive material. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 8-2 and Figure 8-3 for keep-out zones. The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

8.3 Package Loading Specifications

Table 8-1 provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load-bearing surface for thermal solutions. These values are preliminary, and expected variance is ±10%.

Table 8-1. Processor Loading Specifications

Parameter	Maximum	Notes
Static Compressive Load	1068 N [240 lbf]	1, 2, 3, 5
Dynamic Load	540 N [121 lbf]	1, 3, 4, 5

Notes:
1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum static force that can be applied by the heatsink and Independent Loading Mechanism (ILM).
3. These specifications are based on limited testing for design characterization. Loading limits are for the package constrained by the limits of the processor socket.
4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
5. See *Intel® Xeon® Processor E7-2800/4800/8800 v2 Processor Family Thermal/Mechanical Design Guide* for minimum socket load to engage processor within socket.

8.4 Package Handling Guidelines

Table 8-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal. These values are preliminary, and expected variance is ±10%.

Table 8-2. Package Handling Guidelines

Parameter	Maximum	Notes
Shear	36.287 kg [80 lbs]	
Tensile	15.875 kg [35 lbs]	
Torque	15.875 kg-cm [35 in.lbs]	

8.5 Package Insertion Specifications

The processor can be inserted into and removed from an LGA2011-1 socket 15 times. The socket should meet the LGA2011-1 requirements detailed in the *Intel® Xeon® Processor E7-2800/4800/8800 v2 Processor Family Thermal/Mechanical Design Guide*.

8.6 Processor Mass Specification

The typical mass of the processor is currently up to 50 grams. This mass [weight] includes all the components that are included in the package.

8.7 Processor Materials

Table 8-3 lists some of the package components and associated materials.

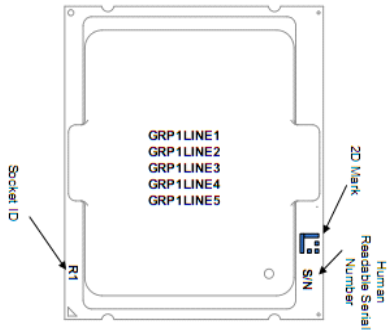
Table 8-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

8.8 Processor Markings

Figure 8-4 shows the topside markings on the processor. This diagram is to aid in the identification of the processor.

Figure 8-4. Processor Top-Side Markings



Legend:	Mark Text (Engineering Mark):
GRP1LINE1:	i{M}{C}YY
GRP1LINE2:	INTEL CONFIDENTIAL
GRP1LINE3:	QDF ES SPEED
GRP1LINE4:	XXXXX
GRP1LINE5:	{FPO} {e4}

Legend:	Mark Text (Production Mark):
GRP1LINE1:	i{M}{C}YY
GRP1LINE2:	SUB-BRAND PROC#
GRP1LINE3:	SSPEC SPEED
GRP1LINE4:	XXXXX
GRP1LINE5:	{FPO} {e4}

Note: XXXXX = Country of Origin

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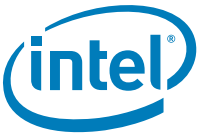


9 PIROM

9.1 Processor Information ROM

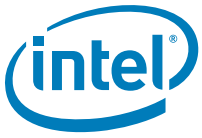
The Processor Information ROM (PIROM) is a memory device located on the processor and is accessible via the System Management Bus (SMBus) which contains information regarding the processor's features. These features are listed in table 10.1.1 below.

The PIROM resides in the lower half of the memory component (addresses 00 - 7Fh), which is permanently write-protected by Intel. The upper half comprises the Scratch EEPROM (addresses 80 - FFh).

9.1.1 Processor Information ROM Table

Offset / Section	# of Bits	Function	Notes	Examples
Header				
00h	8	Data Format Revision	Two 4-bit hex digits	Start with 00h
01-02h	16	PIROM Size	Size in bytes (MSB first)	Use a decimal to hex transfer; 128 bytes = 0080h:
03h	8	Processor Data Address	Byte pointer, 00h if not present	0Eh
04h	8	Processor Core Data Address	Byte pointer, 00h if not present	1Bh
05h	8	Processor Uncore Data Address	Byte pointer, 00h if not present	2A
06h	8	Package Data Address	Byte pointer, 00h if not present	4Ch
07h	8	Part Number Data Address	Byte pointer, 00h if not present	54h
08h	8	Thermal Reference Data Address	Byte pointer, 00h if not present	66h
09h	8	Feature Data Address	Byte pointer, 00h if not present	6Ch
0Ah	8	Other Data Address	Byte pointer, 00h if not present	77h
0B-0Dh	16	Reserved	Reserved for future use	000000h
Processor Data				
0E-13h	48	S-spec/QDF Number	Six 8-bit ASCII characters	QFJP = 20, 20, 51, 46, 4A, 50
14h	7/1	Sample/Production	First seven bits reserved	0b = Sample, 1b = Production 00000001 = production
15	6 2	Number of Cores Number of Threads	[7:2] = Number of cores [1:0] = Threads per core	00111110 = 15 cores with 2 threads each
16-17h	16	System Clock Speed	Four 4-bit hex digits (Mhz)	0100h = 100MHz[1]
18-1A	16	Reserved	Reserved for future use	000000h
Processor Core Data				
1B-1Ch	16	CPUID	Four 4-bit hex digits	06E2h = 06E2
1D-1Eh	16	Reserved	Reserved for future use	0000h
1F-20h	16	Maximum P1 Core Frequency	Non-Turbo Boost (MHz) Four 4-bit hex digits (MHz)	2500h = 2500 MHz[1]
21-22h	16	Maximum P0 Core Frequency	Turbo Boost (MHz) Four 4-bit hex digits (MHz)	2800h = 2800 MHz[1]
23-24h	16	Maximum Core Voltage ID	Four 4-bit hex digits (mV)	1350h = 1350 mV[1]
25-26h	16	Minimum Core Voltage ID	Four 4-bit hex digits (mV)	0800h = 800 mV[1]
27h	8	Core Voltage Tolerance, High	Allowable positive DC shift Two 4-bit hex digits (mV)	15h = 15mV[1]

Offset / Section	# of Bits	Function	Notes	Examples
28h	8	Core Voltage Tolerance, Low	Allowable negative DC shift Two 4-bit hex digits (mV)	15h = 15mV[1]
29h	8	Reserved	Reserved for future use	00h
Processor Uncore Data				
2A-2Bh	16	Maximum Intel QPI Link Transfer Rate	Four 4-bit hex digits (in MT/s)	8000h = 8.000 GT/s[1]
2C-2Dh	16	Maximum PCIe Link Transfer Rate	Four 4-bit hex digits (in MT/s)	8000h = 8.000 GT/s[1]
2E-31h	32	Intel QPI Version Number	Four 8-bit ASCII Characters	01.1
32h	7/1	TXT	First seven bits reserved	00000001 = supported 00000000 = unsupported
33-34h	16	Maximum Intel SMI2 Performance Transfer Rate	Four 4-bit hex digits (in MT/s)	2666h = 2.666GT/s[1]
35-36h	16	Maximum Intel SMI2 Lock Step Transfer Rate	Four 4-bit hex digits (in MT/s)	1600h = 1.600GT/s[1]
37-38h	16	Maximum VSA VID	Four 4-bit hex digits (mV)	1200h = 1200 mV[1]
39-3Ah	16	Minimum VSA VID	Four 4-bit hex digits (mV)	0600h = 600 mV[1]
3B-3Eh	32	Reserved	Reserved for future use	00000000h
3F-40h	16	L2 Cache Size	Decimal (Kb) Per CPU Core	0100h = 256Kb
41-42h	16	L3 Cache Size	Decimal (Kb)	6000h = 24576Kb, 4800h = 18432Kb, 3000h = 12288Kb
43-44	16	VVMSE Nominal Voltage	Four 4-bit hex digits (mV)	1350h = 1350 mV[1]
45-46h	16	VTT Nominal Voltage	Four 4-bit hex digits (mV)	1000h = 1000 mV[1]
47-4Bh	40	Reserved	Reserved for future use	0000000000h
Package				
4C-4Fh	32	Package Revision	Four 8-bit ASCII characters	01.0
50h	6/2	Substrate Revision Software ID	First 6 bits reserved	000000**
51-53h	24	Reserved	Reserved for future use	000000h
Part Numbers				
54-5Ah	56	Processor Family Number	Seven 8-bit ASCII characters	CM80636
5B-62h	64	Processor SKU Number	Seven 8-bit ASCII characters	1272834
63-65h	24	Reserved	Reserved for future use	000000h
Thermal Reference				
66h	8	Recommended THERMALERT_N assertion threshold value	MSB is Reserved	0h = 0C[1]
67h	8	Thermal calibration offset value	MSB is Reserved	0h = 0C[1]
68h	8	T_{CASE} Maximum	Maximum case temperature Two 4-bit hex digits (mV)	69h = 69°C[1]
69-6Ah	16	Thermal Design Power	Four 4-bit hex digits (in Watts)	0130h = 130 Watts[1]
6Bh	8	Reserved	Reserved for future use	00h
Features				
6C-6Fh	32	Processor Core Feature Flags	From CPUID function 1, EDX contents	4387FBFFh
70h	8	Processor Feature Flags	Eight features - Binary 1 indicates functional feature	10001101
71h	8	Additional Processor Feature Flags	Eight additional features - Binary 1 indicates functional feature	01110101
72	6/2	Multiprocessor Support	00b = 2S, 01b = S2S, 10b = S4S, 11b = S8S	00000011 = MP/SMS
73h	4/4	Number of Devices in TAP Chain	Two 4-bit hex digit - Bits	16h[1]
74-75h	16	Reserved	Reserved for future use	0000h



Offset / Section	# of Bits	Function	Notes	Examples
76h	8	Static Checksum	1 byte checksum	Add up by byte and take 2's complement.
Other				
77-7Eh	64	Electronic Signature	Coded binary	N/A
7Fh	8	Electronic Signature Checksum	1 byte checksum	Add up by byte and take 2's complement.

1. Uses Binary Coded Decimal (BCD) translation.

9.1.2 Scratch EEPROM

Also available in the memory component on the processor SMBus is an EEPROM which may be used for other data at the system or processor vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM_WP signal. This signal has a weak pull-down (10 kΩ) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (addresses 00 - 7Fh), which is permanently write-protected by Intel.

9.1.3 PIROM and Scratch EEPROM Supported SMBus Transactions

The PIROM responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignore the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. Table 9-1 illustrates the Read Byte command. Table 9-2 illustrates the Write Byte command.

In the tables, 'S' represents a SMBus start bit, 'P' represents a stop bit, 'A' represents an acknowledge (ACK), and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the PIROM or Scratch EEPROM, and the bits that aren't shaded are transmitted by the SMBus host controller. In the tables, the data addresses indicate 8 bits.

The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the PIROM (MSB = 0) or the Scratch EEPROM (MSB = 1).

Table 9-1. Read Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	S	Slave Address	Read	A	Data	///	P
1	7-bits	1	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

Table 9-2. Write Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	Data	A	P
1	7-bits	1	1	8-bits	1	8-bits	1	1

9.2 SMBus Memory Component Addressing

Of the addresses broadcast across the SMBus, the memory component claims those of the form “10100XXZb”. The “XX” bits are defined by pull-up and pull-down of the SKTID[1:0] pins. Note that SKTID[2] does not affect the SMBus address for the memory component. These address pins are pulled down weakly (10 k) on the processor substrate to ensure that the memory components are in a known state in systems which do not support the SMBus (or only support a partial implementation). The “Z” bit is the read/write bit for the serial bus transaction.

Note that addresses of the form “0000XXXXb” are Reserved and should not be generated by an SMBus master.

Table 9-3 describes the address pin connections and how they affect the addressing of the memory component.

Table 9-3. Memory Device SMBus Addressing

Address (Hex)	Upper Address[1]	Device Select			R/W
	Bits 7-4	SKTID[2]	SKTID[1] Bit 2	SKTID[0] Bit 1	Bit 0
A0h/A1h	10100	10100	0	0	X
A2h/A3h	10100	10100	0	1	X
A4h/A5h	10100	10100	1	0	X
A6h/A7h	10100	10100	1	1	X

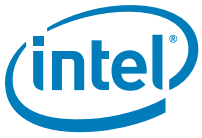
Note:
1. This addressing scheme will support up to 4 processors on a single SMBus.

9.3 Managing Data in the PIROM

The PIROM consists of the following sections:

- Header
- Processor Data
- Processor Core Data
- Processor Uncore Data
- Cache Data
- Package Data
- Part Number Data
- Thermal Reference Data
- Feature Data
- Other Data

Details on each of these sections are described below.



Note: Reserved fields or bits SHOULD be programmed to zeros. However, OEMs should not rely on this model.

9.3.1 Header

To maintain backward compatibility, the Header defines the starting address for each subsequent section of the PIROM. Software should check for the offset before reading data from a particular section of the ROM.

Example: Code looking for the processor uncore data of a processor would read offset 05h to find a value of 29. 29 is the first address within the 'Processor Uncore Data' section of the PIROM.

9.3.1.1 DFR: Data Format Revision

This location identifies the data format revision of the PIROM data structure. Writes to this register have no effect.

Offset: 00h	
Bit	**Description**
7:0	**Data Format Revision** The data format revision is used whenever fields within the PIROM are redefined. The initial definition will begin at a value of 1. If a field, or bit assignment within a field, is changed such that software needs to discern between the old and new definition, then the data format revision field will be incremented. 00h: Reserved 01h: Initial definition 02h: Second revision 03h: Third revision 04h: Fourth revision 05h:Fifth revision *(Defined by this document)* 06h-FFh: Reserved

9.3.1.2 PISIZE: PIROM Size

This location identifies the PIROM size. Writes to this register have no effect.

Offset: 01h-02h	
Bit	**Description**
15:0	**PIROM Size** The PIROM size provides the size of the device in hex bytes. The MSB is at location 01h; the LSB is at location 02h. 0000h - 007Fh: Reserved 0080h: 128 byte PIROM size 0081- FFFFh: Reserved

9.3.1.3 PDA: Processor Data Address

This location provides the offset to the Processor Data Section. Writes to this register have no effect.

Offset: 03h	
Bit	**Description**
7:0	**Processor Data Address** Byte pointer to the Processor Data section 00h: Processor Data section not present 01h - 0Dh: Reserved 0Eh: Processor Data section pointer value 0Fh-FFh: Reserved

9.3.1.4 PCDA: Processor Core Data Address

This location provides the offset to the Processor Core Data Section. Writes to this register have no effect.

Offset: 04h	
Bit	**Description**
7:0	**Processor Core Data Address** Byte pointer to the Processor Core Data section 00h: Processor Core Data section not present 01h - 09h: Reserved 1Ah: Processor Core Data section pointer value 1Bh-FFh: Reserved

9.3.1.5 PUDA: Processor Uncore Data Address

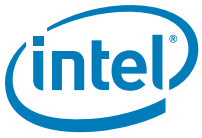
This location provides the offset to the Processor Uncore Data Section. Writes to this register have no effect.

Offset: 05h	
Bit	**Description**
7:0	**Processor Uncore Data Address** Byte pointer to the Processor Uncore Data section 00h: Processor Uncore Data section not present 01h - 28h: Reserved 29h: Processor Uncore Data section pointer value 2Ah-FFh: Reserved

9.3.1.6 PDA: Package Data Address

This location provides the offset to the Package Data Section. Writes to this register have no effect.

Offset: 06h	
Bit	**Description**
7:0	**Package Data Address** Byte pointer to the Package Data section 00h: Package Data section not present 01h - 4Ah: Reserved 4Bh: Package Data section pointer value 4Ch-FFh: Reserved



9.3.1.7 PNDA: Part Number Data Address

This location provides the offset to the Part Number Data Section. Writes to this register have no effect.

Offset: 07h	
Bit	**Description**
7:0	**Part Number Data Address** Byte pointer to the Part Number Data section 00h: Part Number Data section not present 01h - 52h: Reserved 53h: Part Number Data section pointer value 54h-FFh: Reserved

9.3.1.8 TRDA: Thermal Reference Data Address

This location provides the offset to the Thermal Reference Data Section. Writes to this register have no effect.

Offset: 08h	
Bit	**Description**
7:0	**Thermal Reference Data Address** Byte pointer to the Thermal Reference Data section 00h: Thermal Reference Data section not present 01h - 64h: Reserved 65h: Thermal Reference Data section pointer value 66h-FFh: Reserved

9.3.1.9 FDA: Feature Data Address

This location provides the offset to the Feature Data Section. Writes to this register have no effect.

Offset: 09h	
Bit	**Description**
7:0	**Feature Data Address** Byte pointer to the Feature Data section 00h: Feature Data section not present 01h - 6Ah: Reserved 6Bh: Feature Data section pointer value 6Ch-FFh: Reserved

9.3.1.10 ODA: Other Data Address

This location provides the offset to the Other Data Section. Writes to this register have no effect.

Offset: 0Ah	
Bit	**Description**
7:0	**Other Data Address** Byte pointer to the Other Data section 00h: Other Data section not present 01h - 78h: Reserved 79h: Other Data section pointer value 7Ah- FFh: Reserved

9.3.1.11 RES1: Reserved 1

This location is reserved. Writes to this register have no effect.

Offset: 0Bh-0Dh	
Bit	**Description**
23:0	**RESERVED** 000000h-FFFFFFh: Reserved

9.3.2 Processor Data

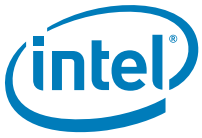
This section contains three pieces of data:

- The S-spec/QDF of the part in ASCII format.
- (1) 2-bit field to declare if the part is a pre-production sample or a production unit.
- The system bus speed in BCD format

9.3.2.1 SQNUM: S-Spec QDF Number

This location provides the S-Spec or QDF number of the processor. The S-spec/QDF field is six ASCII characters wide and is programmed with the same S-spec/QDF value as marked on the processor. If the value is less than six characters in length, leading spaces (20h) are programmed in this field. Writes to this register have no effect.

Example: A processor with a QDF mark of QWFZ contains the following in field 0E-13h: 20h, 20h, 51h, 57h, 46h, 5Ah. This data consists of two blanks at 0Eh and 0Fh followed by the ASCII codes for QEU5 in locations 10 - 13h.



Offset: 0Eh-13h	
Bit	**Description**
47:40	**Character 6** S-Spec or QDF character or 20h 00h-0FFh: ASCII character
39:32	**Character 5** S-Spec or QDF character or 20h 00h-0FFh: ASCII character
31:24	**Character 4** S-Spec or QDF character 00h-0FFh: ASCII character
23:16	**Character 3** S-Spec or QDF character 00h-0FFh: ASCII character
15:8	**Character 2** S-Spec or QDF character 00h-0FFh: ASCII character
7:0	**Character 1** S-Spec or QDF character 00h-0FFh: ASCII character

9.3.2.2 SAMPROD: Sample/Production

This location contains the sample/production field, which is a two-bit field and is LSB aligned. All Q-spec material will use a value of 00b. All S-spec material will use a value of 01b. All other values0 are reserved. Writes to this register have no effect.

Example: A processor with a Qxxx mark (engineering sample) will have offset 14h set to 00h. A processor with an Sxxxx mark (production unit) will use 01h at offset 14h.

Offset: 14h	
Bit	**Description**
7:2	**RESERVED** 000000b-111111b: Reserved
1:0	**Sample/Production** Sample or Production indictor 00b: Sample 01b: Production 10b-11b: Reserved

9.3.2.3 Processor Thread and Core Information

This location contains information regarding the number of cores and threads on the processor. Writes to this register have no effect. Data format is binary.

Example: The Intel® Xeon® E7 v2 processor has up to 15 cores and two threads per core.

Offset: 15h	
Bit	**Description**
7:2	Number of cores
1:0	Number of threads per core

9.3.2.4 SCS: System Clock Speed

This location contains the system clock frequency information. Systems may need to read this offset to decide if all installed processors support the same system clock speed. The data provided is the speed, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: A processor with system bus speed of 100 MHz will have a value of 0100h.

Offset: 16h-17h	
Bit	**Description**
15:0	**System Bus Speed** 0000h-FFFFh: MHz

9.3.2.5 RES2: Reserved 2

This location is reserved. Writes to this register have no effect.

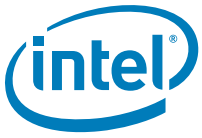
Offset: 18h-2Ah	
Bit	**Description**
23:0	**RESERVED** 000000h-FFFFFFh: Reserved

9.3.3 Processor Core Data

This section contains silicon-related data relevant to the processor cores.

9.3.3.1 CPUID: CPUID

This location contains the CPUID, Processor Type, Family, Model and Stepping. The CPUID field is a copy of the results in EAX[15:0] from Function 1 of the CPUID instruction. Writes to this register have no effect. Data format is hexidecimal.



Offset: 1Bh-1Ch	
Bit	**Description**
15:13	**Reserved** 00b-11b: Reserved
12:12	**Processor Type** 0b-1b: Processor Type
11:8	**Processor Family** 0h-Fh: Processor Family
7:4	**Processor Model** 0h-Fh: Processor Model
3:0	**Processor Stepping** 0h-Fh: Processor Stepping

9.3.3.2 RES3: Reserved 3

This locations are reserved. Writes to this register have no effect.

Offset: 1Dh-1Eh	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

9.3.3.3 MP1CF: Maximum P1 Core Frequency

This location contains the maximum non-Turbo Boost core frequency for the processor. The frequency should equate to the markings on the processor and/or the QDF/S-spec speed even if the parts are not limited or locked to the intended speed. Format of this field is in MHz, rounded to a whole number, and encoded in binary coded decimal. Writes to this register have no effect.

Example: A 2.666 GHz processor will have a value of 2666h.

Offset: 1F-20h	
Bit	**Description**
15:0	**Maximum P1 Core Frequency** 0000h-FFFFh: MHz

9.3.3.4 MP0CF: Maximum P0 Core Frequency

This location contains the maximum Turbo Boost core frequency for the processor. This is the maximum intended speed for the part under any functional conditions. Format of this field is in MHz, rounded to a whole number, and encoded in binary coded decimal. Writes to this register have no effect.

Example: A processor with a maximum Turbo Boost frequency of 2.666 GHz will have a value of 2666h.

Offset: 21h-22h	
Bit	**Description**
15:0	**Maximum P0 Core Frequency** 0000h-FFFFh: MHz

9.3.3.5 MAXVID: Maximum Core VID

This location contains the maximum Core VID (Voltage Identification) voltage that may be requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect.

Example: A voltage of 1.350 V maximum core VID would contain 1350h.

Offset: 23h-24h	
Bit	**Description**
15:0	**Maximum Core VID** 0000h-FFFFh: mV

9.3.3.6 MINVID: Minimum Core VID

This location contains the Minimum Core VID (Voltage Identification) voltage that may be requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect.

Example: A voltage of 1.000 V maximum core VID would contain 1000h.

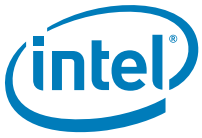
Offset: 25h-26h	
Bit	**Description**
15:0	**Maximum Core VID** 0000h-FFFFh: mV

9.3.3.7 VTH: Core Voltage Tolerance, High

This location contains the maximum Core Voltage Tolerance DC offset high. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: 15 mV tolerance would be saved as 15h.

Offset: 27h	
Bit	**Description**
7:0	**Core Voltage Tolerance, High** 00h-FFh: mV



9.3.3.8 VTL: Core Voltage Tolerance, Low

This location contains the maximum Core Voltage Tolerance DC offset low. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Writes to this register have no effect. A value of FF indicates that this value is undetermined. Writes to this register have no effect.

Example: 15 mV tolerance would be saved as 15h.

Offset: 28h	
Bit	**Description**
7:0	**Core Voltage Tolerance, Low** 00h-FFh: mV

9.3.3.9 RES3: Reserved 3a

This locations are reserved. Writes to this register have no effect.

Offset: 29h	
Bit	**Description**
7:0	**RESERVED** 00h-FFh: Reserved

9.3.4 Processor Uncore Data

This section contains silicon-related data relevant to the processor Uncore.

9.3.4.1 MAXQPI: Maximum Intel QPI Transfer Rate

Systems may need to read this offset to decide if all installed processors support the same Intel QPI Link Transfer Rate. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel® Xeon® E7 v2 processor supports a maximum Intel QPI link transfer rate of 8.0 GT/s. Therefore, offset 2Ah-2Bh has a value of 8000.

Offset: 2Ah-2Bh	
Bit	**Description**
15:0	**Maximum Intel QPI Transfer Rate** 0000h-FFFFh: MHz

9.3.4.2 MAXPCI: Maximum PCIe Transfer Rate

Systems may need to read this offset to decide if all installed processors support the same PCIe Link Transfer Rate. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel® Xeon® E7 v2 processor supports a maximum PCIe link transfer rate of 8.0 GT/s. Therefore, offset 2Ah-2Bh has a value of 8000.

Offset: 2Ch-2Dh	
Bit	**Description**
15:0	**Minimum Intel QPI Transfer Rate** 0000h-FFFFh: MHz

9.3.4.3 QPIVN: Intel QPI Version Number

The Intel QPI Version Number is provided as four 8-bit ASCII characters. Writes to this register have no effect.

Example: The Intel® Xeon® E7 v2 processor supports Intel QPI Version Number 1.1. Therefore, offset 2Eh-31h has an ASCII value of “01.1”, which is 30, 31, 2E, 31.

Offset: 2Eh-31h	
Bit	**Description**
31:0	**Intel QPI Version Number** 00000000h-FFFFFFFFh: MHz

9.3.4.4 TXT: TXT

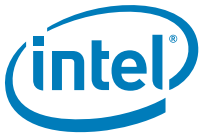
This location contains the Intel TXT location, which is a two-bit field and is LSB aligned. A value of 00b indicates Intel TXT is not supported. A value of 01b indicates Intel TXT is supported. Writes to this register have no effect.

Example: A processor supporting Intel TXT will have offset 32h set to 01h.

Offset: 32h	
Bit	**Description**
7:2	**RESERVED** 000000b-111111b: Reserved
1:0	**TXT** TXT support indicator 00b: Not supported 01b: Supported 10b-11b: Reserved

9.3.4.5 MAXSMP: Maximum Intel SMI2 Performance Transfer Rate

Systems may need to read this offset to decide on compatible processors and Intel C102/C104 Scalable Memory Buffer capabilities. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.



Example: The Intel® Xeon® E7 v2 processor supports a maximum Intel SMI2 performance transfer rate of 2.666 GT/s. Therefore, offset 33h-34h has a value of 2666h.

Offset: 33h-34h	
Bit	**Description**
15:0	**Maximum Intel SMI Transfer Rate** 0000h-FFFFh: MHz

9.3.4.6 MAXSML: Maximum Intel SMI2 Lock Step Transfer Rate

Systems may need to read this offset to decide on compatible processors and Intel C102/C104 Scalable Memory Buffer capabilities. The data provided is the transfer rate, rounded to a whole number, and reflected in binary coded decimal. Writes to this register have no effect.

Example: The Intel® Xeon® E7 v2 processor supports a maximum Intel SMI 2 lock step transfer rate of 1.600 GT/s. Therefore, offset 33h-34h has a value of 1600h.

Offset: 35h-36h	
Bit	**Description**
15:0	**Minimum Intel SMI Transfer Rate** 0000h-FFFFh: MHz

9.3.4.7 MXSAVD: MAX VSA VID

Offset 37h-38h is the Processor Vsa maximum VID (Voltage Identification) field and contains the maximum voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

Example: A voltage of 1.200 V maximum core VID would contain 1200h in Offset 36- 37h.

Offset: 37h-38h	
Bit	**Description**
15:0	**MAX VSA VID** 0000h-FFFFh: mV

9.3.4.8 MNSAVD: MIN VSA VID

Offset 39h-4Ah is the Processor Vsa minimum VID (Voltage Identification) field and contains the minimum voltage requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in binary coded decimal. Some systems read this offset to determine if all processors support the same default VID setting. Writes to this register have no effect.

Example: A voltage of 0.600 V maximum core VID would contain 600h in Offset 39- 4Ah.

Offset: 39-4Ah	
Bit	**Description**
15:0	**MIN VSA VID** 0000h-FFFFh: mV

9.3.4.9 RES4: Reserved 4

This location is reserved. Writes to this register have no effect.

Offset: 3Bh-3Eh	
Bit	**Description**
31:0	**RESERVED** 00000000h-FFFFFFFFh: Reserved

9.3.4.10 L2SIZE: L2 Cache Size

This location contains the size of the level-two cache in kilobytes. Writes to this register have no effect. Data format is decimal.

Example: The Intel® Xeon® E7 v2 processor has a 256K L2 cache. Thus, offset 3Fh-40h will contain a value of 0100h.

Offset: 3Fh-40h	
Bit	**Description**
15:0	**L2 Cache Size** 0000h-FFFFh: KB

9.3.4.11 L3SIZE: L3 Cache Size

This location contains the size of the level-three cache in kilobytes. Writes to this register have no effect. Data format is decimal.

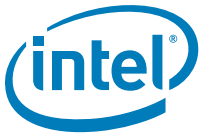
Example: The Intel® Xeon® E7 v2 processor has up to a 37.5 MB L3 cache. Thus, offset 41h-42h will contain a value of 9600h.

Offset: 41h-42h	
Bit	**Description**
15:0	**L3 Cache Size** 0000h-FFFFh: KB

9.3.4.12 VVMSE: VVMSE

This field contains the voltage requested for the VVMSE pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default VMSE settings. Writes to this register have no effect.

Example: A voltage of 1.350 VVMSE would contain an Offset 43-44h value of 1350h.



Offset: 43h-44h	
Bit	**Description**
15:0	**Cache Voltage ID** 0000h-FFFFh: mV

9.3.4.13 VTT: VTT

This field contains the voltage requested for the Vtt pins. This field is in mV and is reflected in hex. Some systems read this offset to determine if all processors support the same default Vtt settings. Writes to this register have no effect.

Example: A voltage of 1.000 VTT would contain an Offset 43-44h value of 1000h.

Offset: 45-46h	
Bit	**Description**
15:0	**Cache Voltage Tolerance, High** 0000h-FFFFh: mV

9.3.4.14 RES5: Reserved 5

This location is reserved. Writes to this register have no effect.

Offset: 47h-4Bh	
Bit	**Description**
39:0	**RESERVED** 0000000000h-FFFFFFFFFFh: Reserved

9.3.5 Package Data

This section contains substrate and other package related data.

9.3.5.1 PREV: Package Revision

This location tracks the highest level package revision. It is provided in an ASCII format of four characters (8 bits x 4 characters = 32 bits). The package is documented as 1.0, 2.0, and so forth. If only three ASCII characters are consumed, a leading space is provided in the data field. Writes to this register have no effect.

Example: The Intel® Xeon® E7 v2 processor utilizes the second revision of the LGA-2011 package. Thus, at offset 4C-4F-35h, the data is a space followed by 2.0. In hex, this would be 20h, 32h, 2Eh, 30h.

Offset: 4Ch-4Fh	
Bit	**Description**
31:24	**Character 4** ASCII character or 20h 00h-0FFh: ASCII character
23:16	**Character 3** ASCII character 00h-0FFh: ASCII character
15:8	**Character 2** ASCII character 00h-0FFh: ASCII character
7:0	**Character 1** ASCII character 00h-0FFh: ASCII character

9.3.5.2 Substrate Revision Software ID

This location is a place holder for the Substrate Revision Software ID. Writes to this register have no effect.

Offset: 50h	
Bit	**Description**
7:0	**Substrate Revision Software ID** 00h-FFh: Reserved

9.3.5.3 RES6: Reserved 6

This location is reserved. Writes to this register have no effect.

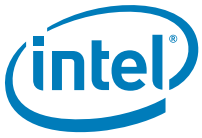
Offset: 51h-53h	
Bit	**Description**
23:0	**RESERVED** 000000h-FFFFFFh: Reserved

9.3.6 Part Number Data

This section provides device traceability.

9.3.6.1 PFN: Processor Family Number

This location contains seven ASCII characters reflecting the Intel® family number for the processor. This number is the same on all Intel® Xeon® E7 v2 processors. Combined with the Processor SKU Number below, this is the complete processor part number. This information is typically marked on the outside of the processor. If the part number is less than 15 total characters, a leading space is inserted into the value. The part number should match the information found in the marking specification. Writes to this register have no effect.



Example: A processor with a part number of AT80604******** will have the following data found at offset 38-3Eh: 41h, 54h, 38h, 30h, 36h, 30h, 34h.

Offset: 54h-5Ah	
Bit	**Description**
55:48	**Character 7** ASCII character or 20h 00h-0FFh: ASCII character
47:40	**Character 6** ASCII character or 20h 00h-0FFh: ASCII character
39:32	**Character 5** ASCII character or 20h 00h-0FFh: ASCII character
31:24	**Character 4** ASCII character 00h-0FFh: ASCII character
23:16	**Character 3** ASCII character 00h-0FFh: ASCII character
15:8	**Character 2** ASCII character 00h-0FFh: ASCII character
7:0	**Character 1** ASCII character 00h-0FFh: ASCII character

9.3.6.2 PSN: Processor SKU Number

This location contains eight ASCII characters reflecting the Intel® SKU number for the processor. Added to the end of the Processor Family Number above, this is the complete processor part number. This information is typically marked on the outside of the processor. If the part number is less than 15 total characters, a leading space is inserted into the value. The part number should match the information found in the marking specification. Writes to this register have no effect.

Example: A processor with a part number of *******003771AA will have the following data found at offset 58-62h: 30h, 30h, 33h, 37h, 37h, 31h, 41h, 41h.

Offset: 5Bh=62h	
Bit	**Description**
63:56	**Character 8** 00h-0FFh: ASCII character
55:48	**Character 7** ASCII character or 20h 00h-0FFh: ASCII character
47:40	**Character 6** ASCII character or 20h 00h-0FFh: ASCII character

Offset: 5Bh=62h	
Bit	**Description**
39:32	**Character 5** ASCII character or 20h 00h-0FFh: ASCII character
31:24	**Character 4** ASCII character 00h-0FFh: ASCII character
23:16	**Character 3** ASCII character 00h-0FFh: ASCII character
15:8	**Character 2** ASCII character 00h-0FFh: ASCII character
7:0	**Character 1** ASCII character 00h-0FFh: ASCII character

9.3.6.3 RES7: Reserved 7

This location is reserved. Writes to this register have no effect.

Offset: 63h-65h	
Bit	**Description**
23:0	**RESERVED** 000000h-FFFFFFh: Reserved

9.3.7 Thermal Reference Data

9.3.7.1 TUT: Thermalert Upper Threshold

This location is a place holder for the Thermalert Upper Threshold Byte. Writes to this register have no effect.

Offset: 66h	
Bit	**Description**
7:0	**Thermalert Upper Threshold** 0000h-FFFFh: Reserved

9.3.7.2 TCO: Thermal Calibration Offset

This location is a place holder for the Thermal Calibration Offset Byte. Writes to this register have no effect.

Offset: 67h	
Bit	**Description**
7:0	**Thermal Calibration Offset** 0000h-FFFFh: Reserved

9.3.7.3 TCASE: T_{CASE} Maximum

This location provides the maximum T_{CASE} for the processor. The field reflects temperature in degrees Celsius in binary coded decimal format. The thermal specifications are specified at the case Integrated Heat Spreader (IHS). Writes to this register have no effect.

Example: A temperature of 66 degrees C would contain a value of 66h.

Offset: 68h	
Bit	**Description**
7:0	**T_{CASE} Maximum** 00h-FFh: Degrees Celsius

9.3.7.4 TDP: Thermal Design Power

This location contains the maximum Thermal Design Power for the part. The field reflects power in watts in binary coded decimal format. Writes to this register have no effect. A zero value means that the value was not programmed.

Example: A 130W TDP would be saved as 0130h.

Offset: 69h-6Ah	
Bit	**Description**
15:0	**Thermal Design Power** 0000h-FFFFh: Watts

9.3.7.5 RES7: Reserved 8

This location is reserved. Writes to this register have no effect.

Offset: 6Bh	
Bit	**Description**
7:0	**RESERVED** 00h-FFh: Reserved

9.3.8 Feature Data

This section provides information on key features that the platform may need to understand without powering on the processor.

9.3.8.1 PCFF: Processor Core Feature Flags

This location contains a copy of results in EDX[31:0] from Function 1 of the CPUID instruction. These details provide instruction and feature support by product family. Writes to this register have no effect.

Example: A value of BFEBFBFFh can be found at offset 6C - 6Fh.

Offset: 6Ch-6Fh	
Bit	**Description**
31:0	**Processor Core Feature Flags** 00000000h-FFFFFFFFF: Feature Flags

9.3.8.2 PFF: Processor Feature Flags

This location contains additional feature information from the processor. Writes to this register have no effect.

Note: Bit 5 and Bit 6 are mutually exclusive (only one bit will be set).

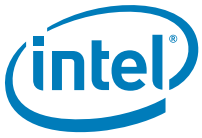
Offset: 70h	
Bit	**Description**
7	Multi-Core (set if the processor is a multi-core processor)
6	Serial signature (set if there is a serial signature at offset 5B- 62h)
5	Electronic signature present (set if there is a electronic signature at 5B- 62h)
4	Thermal Sense Device present (set if an SMBus thermal sensor is on package)
3	Reserved
2	OEM EEPROM present (set if there is a scratch ROM at offset 80 - FFh)
1	Core VID present (set if there is a VID provided by the processor)
0	L3 Cache present (set if there is a level-3 cache on the processor)

Bits are set when a feature is present, and cleared when they are not.

9.3.8.3 APFF: Additional Processor Feature Flags

This location contains additional feature information from the processor. Writes to this register have no effect.

Offset: 71h	
Bit	**Description**
7	Reserved
6	Intel® Cache Safe Technology
5	Extended Halt State (C1E)
4	Intel Virtualization Technology
3	Execute Disable
2	Intel® 64
1	Intel® Thermal Monitor 2
0	Enhanced Intel SpeedStep Technology



Bits are set when a feature is present, and cleared when they are not.

9.3.8.4 MPSUP: Multiprocessor Support

This location contains 2 bits for representing the supported number of physical processors on the bus. These two bits are LSB aligned where 00b equates to non-scalable 2 socket (2S) operation, 01b to scalable 2 socket (S2S), 10 to scalable 4 socket (S4S), and scalable 8 socket (S8S). The Intel® Xeon® E7 v2 processor is a S2S, S4S, or S8S processor. The first six bits in this field are reserved for future use. Writes to this register have no effect.

Example: A scalable 8 socket processor will have a value of 03h at offset 71h.

Offset: 72h	
Bit	**Description**
7:2	**RESERVED** 000000b-111111b: Reserved
1:0	**Multiprocessor Support** 2S, S2S, S4S or S8S indicator 00b: Non-Scalable 2 Socket 01b: Scalable 2 Socket 10b: Scalable 4 Socket 11b: Scalable 8 Socket

9.3.8.5 TCDC: Tap Chain Device Count

At offset 73, a 4-bit hex digit is used to tell how many devices are in the TAP Chain. Because the Intel® Xeon® E7 v2 processor has ten cores, this field would be set to Ah.

Offset: 73h	
Bit	**Description**
7:0	**TAP Chain Device Count** 0000h-FFFFh: Reserved

9.3.8.6 RES9: Reserved 9

This location is reserved. Writes to this register have no effect.

Offset: 74h-75h	
Bit	**Description**
15:0	**RESERVED** 0000h-FFFFh: Reserved

9.3.8.7 STTCKS: Static Checksum

This location provides the checksum of the static values per SKU. Writes to this register have no effect.

Offset: 76h	
Bit	**Description**
7:0	**Static Checksum** One-byte checksum of the Static Checksum 00h- FFh: See Section 9.3.10 for calculation of this value.

9.3.9 Electronic Signature

This section contains a large reserved area, and items added after the original format for the Intel® Xeon® E7 v2 processor PIROM was set.

9.3.9.1 ESIG: Electronic Signature

This location contains a 64-bit identification number. The value in this field is either an electronic signature. Writes to this register have no effect.

Offset: 77h-7Eh	
Bit	**Description**
63:0	**Electronic Signature** 0000000000000000h-FFFFFFFFFFFFFFFFh: Electronic Signature

9.3.9.2 ESCKS: Electronic Signature Checksum

This location provides the checksum for the Other Data Section. Writes to this register have no effect.

Offset: 7Fh	
Bit	**Description**
7:0	**Other Data Checksum** One-byte checksum of the Other Data Checksum 00h- FFh: See Section 9.3.10 for calculation of this value.

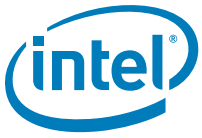
9.3.10 Checksums

The PIROM includes multiple checksums. Table 9-4 includes the checksum values for each section defined in the 128-byte ROM.

Table 9-4. 128-Byte ROM Checksum Values

Section	Checksum Address
Static Features	76h
Electronic Signature	7Fh

Checksums are automatically calculated and programmed by Intel®. The first step in calculating the checksum is to add each byte from the field to the next subsequent byte. This result is then negated to provide the checksum.



Example: For a byte string of AA445Ch, the resulting checksum will be B6h.

AA = 10101010 44 = 01000100 5C = 01011100

AA + 44 + 5C = 01001010

Negate the sum: 10110101 +1 = **10110110 (B6h)**

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