MPC8308-NSG

Reference Design Platform User's Guide

MPC8308NSGUG
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04/2011

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Federal Communications Commission Radio Frequency Interference Statement

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference and

(2) this device must accept any interference received, including interference that might cause undesired operation. Changes or modifications to this equipment not expressly approved by Freescale could void the user’s authority to operate the equipment. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

Reminding

1. The installed antennas must not be located in a manner that allows exposure of the general population at a distance of less than 23cm.
2. Mount the antennas in a manner that prevents any personnel from entering the area within 23cm from the central position of the antenna.

This device has been designed to operate with the attached antennas, and having a maximum gain of 2.5dBi. Antennas not identical as that or having a gain greater than 2.5dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms.
To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that permitted for successful communication.

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About This Book

This document presents system architecture, board-level functions, and external connections for the MPC8308-NSG board. It provides guidance of how to operate this product, making it easy for the user to connect with the outside world.

Audience

It is assumed that the reader understands operating systems, microprocessor system design, and the basic principles of RISC processing.

Organization

Following is a summary and a brief description of the major parts of this user's guide:

- Chapter 1, Introduction, provides a high-level description of features and block diagram of the MPC8308-NSG board.
- Chapter 2, MPC8308-NSG Board, describes the board in terms of its hardware: board-level functions, connectors, configurations, and board mechanical data.
- Chapter 3, Board Bootup, describes the board settings and physical connections needed to boot the MPC8308-NSG board.
- Chapter 4, Zigbee Module, describes the Zigbee module used in the product
- Chapter 5, Wi-Fi Card, introduces the Wi-Fi card used in the product.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

Related Documentation

The following sources were referenced to produce this book:

- *MPC8308 PowerQUICC™ II Pro Integrated Host Processor Reference Manual* (MPC8308RM)
- *MPC8308 PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (MPC8308EC)
- *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582)

Acronyms and Abbreviations

Table i contains acronyms and abbreviations used in this document.

Table i. Acronyms and Abbreviated Terms

Term	Meaning
CPU	Central Processing Unit
DDR2 SDRAM	Double-Data-Rate Two Synchronous Dynamic Random Access Memory

Table i. Acronyms and Abbreviated Terms (continued)

Term	Meaning
NOR Flash	Nor Gate Flash
eTSEC	Enhanced Three-Speed Ethernet Controller
RGMII	Reduced Gigabit Media Independent Interface
WAN	Wide Area Network
LAN	Local Area Network
USB	Univeral Serial Bus
ULPI	USB Low-Pin Count Interface
PCI-E	Peripheral Component Interconnect Express (Computer Bus)
SDHC	Secure Digital High Capacity (SD 2.0 Memory Card)
I^2C	Inter-Integrated Circuit (Computer Bus)
EEPROM	Electrically Erasable Programmable Read-Only Memory
JTAG	Joint Test Action Group
UART	Universal asynchronous receiver/transmitter
GPIO	General-purpose I/O

Chapter 1
Introduction

This chapter presents the features and block diagram for the MPC8308-NSG board.

This document is organized as follows:

- Section 1.1, Overview. This section gives a brief introduction of MPC8308-NSG board.
- Section 1.2, Features. This section presents the main features of MPC8308-NSG board.

1.1 Overview

The MPC8308-NSG is a reference design based on the MPC8308 PowerQUICC™II Pro processor. It supports applications of Wi-Fi Router, DMS (Digital Media Server), or Office in BOX, etc. The documentation for manufacturing the MPC8308-NSG—including schematic, Gerber files, reference software, Bill Of Material (BOM)—is on the product CD. With the documentation, original equipment manufacturers (OEMs) and original design manufacturers (ODMs) can accelerate the development process and speed time-to-market for their real product.

1.2 Features

This section presents the features, specification, and block diagram of the MPC8308-NSG board.

The features are as follows:

- CPU
  - Freescale MPC8308 up to 400 MHz
- Power
  - 12 V DC input
- Memory subsystem
  - On-board 128-MByte DDR2 unbuffered SDRAM
  - 8-MByte NOR Flash
  - 32-MByte NAND Flash
  - 256Kbit EEPROM
- 10/100/1000 BaseT Ethernet ports
  - eTSEC1: RGMII interface: WAN, 1 x 10/100/1000 BaseT with RJ-45 interface, using Atheros™ AR8035 single port 10/100/1000 BaseT PHY
  - eTSEC2: RGMII interface: LAN, 1 x 10/100/1000 BaseT with RJ-45 interface, using Atheros™ AR8035 single port 10/100/1000 BaseT PHY
- USB 2.0 Host

  - ULPI interface: 2x USB 2.0 Type A Receptacle interface, using SMSC™ USB3300 Hi-Speed USB PHY and Genesys Logic's GL850A USB 2.0 HUB Controller with 4 downstream ports
- PCI Express
  - One mini PCI Express Connector supports half size mini PCIe card
- SDHC
  - One SD/MMC Card Connector
- I^2C
  - ATMEL AT88SC0104CA Secure EEPROM on I^2C1
  - mini PCI Express connector on I^2C1
  - ST M2456 256Kbit EEPROM on I^2C2
  - Zigbee Module on I^2C2
- UART
  - UART1: 3-pin serial connector for 2-wire (RxD, TxD)
  - UART2: communication interface between MPC8308 and Zigbee module
- Board Connectors
  - One DC power jack
  - JTAG / COP for MPC8308 debugging
  - JTAG for Zigbee module development tool
- 6-layer PCB (4 layers signals and separate power and ground layers)
- Certification
  - FCC
  - Lead-Free (RoHS)

Figure 1-1 shows the MPC8308-NSG board block diagram.

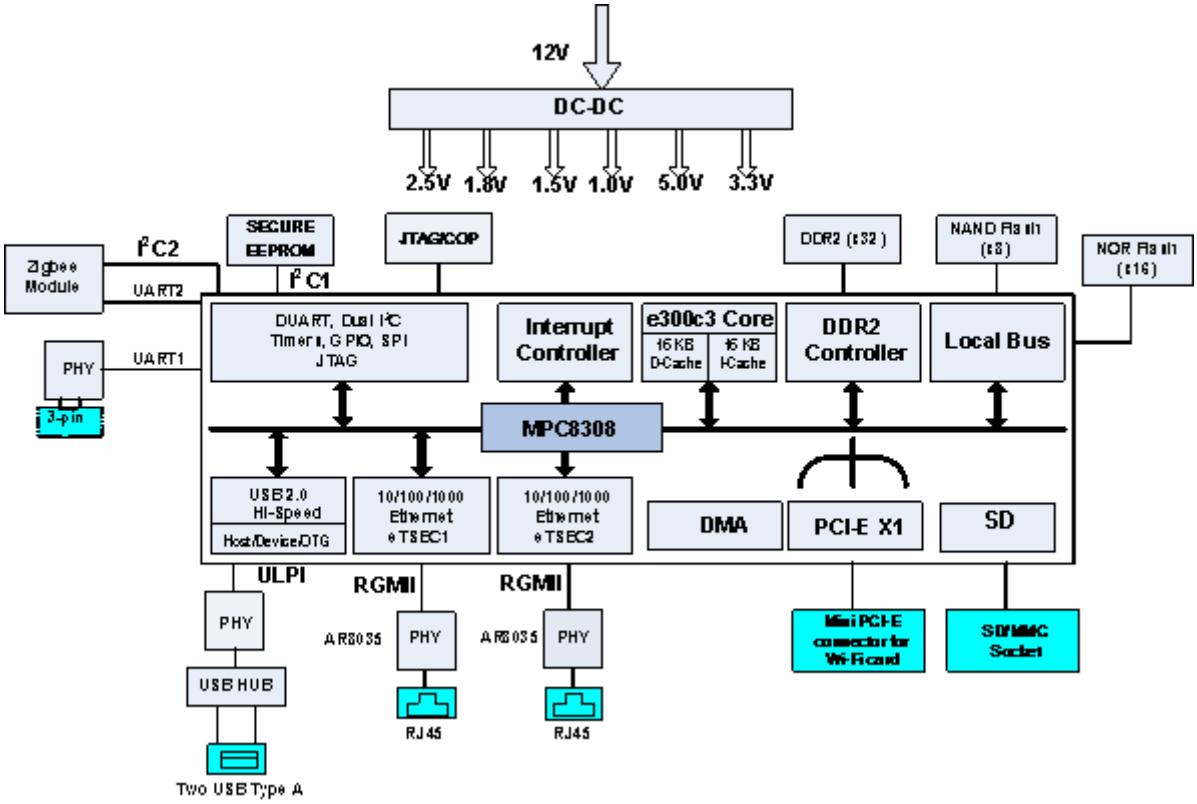

Figure 1-1. MPC8308-NSG Board Block Diagram

Chapter 2
MPC8308-NSG Board

This chapter presents the board-level functions, specifications, and mechanical data for the MPC8308-NSG board.

This document is organized as follows:

- Section 2.1, Board-Level Functions. This section includes reset, interrupts, clock distribution, and interface specification description.
- Section 2.2, MPC8308-NSG Assembly. This section shows top view of MPC8308-NSG board.
- Section 2.3, Connectors, describes pin assignment of all connectors on the board.
- Section 2.4, LEDs, shows LED indicators on the front panel.
- Section 2.5, MPC8308-NSG Board Configuration, describes the operational mode and configuration options of the MPC8308-NSG board.
- Section 2.6, Electric Characteristics, lists the electric characteristics of the MPC8308-NSG board.
- Section 2.7, Mechanical Data, shows MPC8308-NSG board dimensions.

2.1 Board-Level Functions

The board-level functions discussed in this section are reset, interrupts, clock distribution, and interface specification.

2.1.1 Reset and Reset Configurations

The MPC8308-NSG reset module generates a single reset to reset the MPC8308 and other peripherals on the board. The reset unit provides power-on reset, hard reset, and soft reset signals in compliance with the MPC8308 hardware specification. Figure 2-1 shows the reset circuitry.

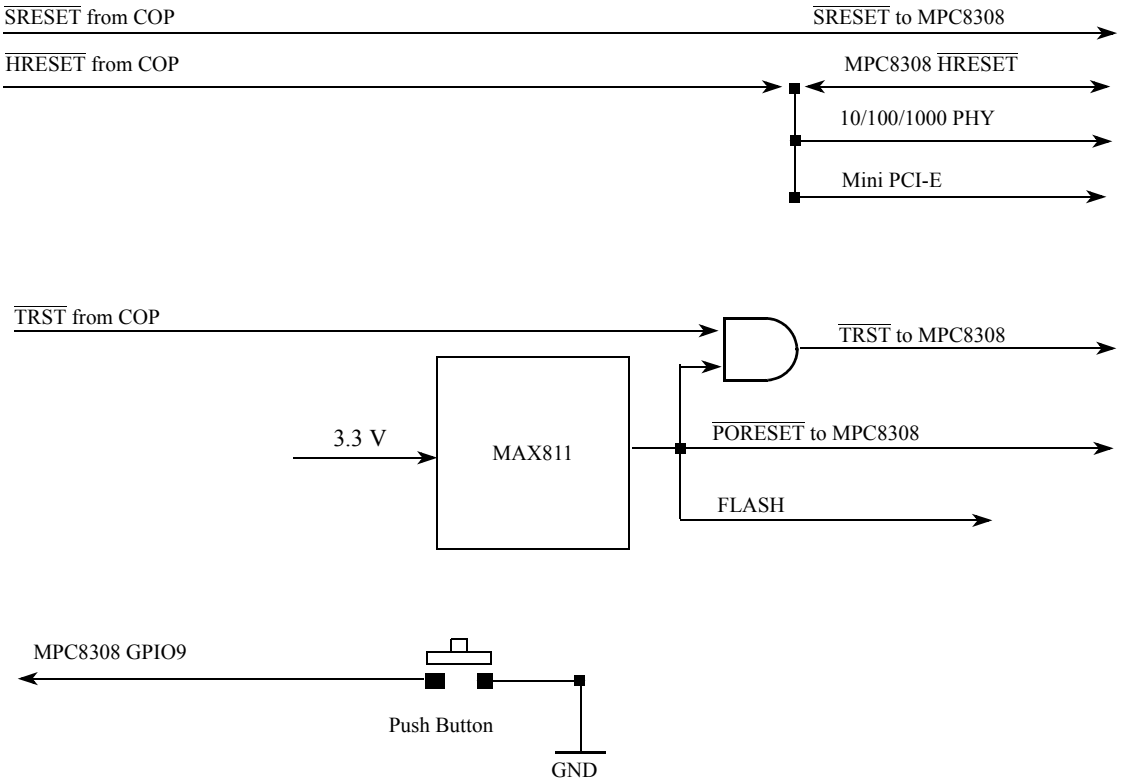

Figure 2-1. Reset Circuitry of the MPC8308-NSG Board

- The COP/JTAG port or the MPC8308 generates the signal for hard reset.
- The COP/JTAG port reset provides convenient hard-reset capability for a COP/JTAG controller. The RESET line is available at the COP/JTAG port connector. The COP/JTAG controller can directly generate the hard-reset signal by asserting this line low.
- The Maxim MAX811 device generates the power-on reset. When 3.3 V is ready, the MAX811 internal timeout guarantees a minimum reset active time of 140 ms before PORESET is de-asserted. This circuitry guarantees a 140 ms PORESET pulse width after 3.3 V reaches the right voltage level, and this meets the specification of the PORESET input of MPC8308.
- The Push Button reset interfaces GPIO9 of MPC8308 with a debounce capability to produce a manual reset controlled by software.
- The COP/JTAG port also generates the soft reset for the system. Assertion of SRESET causes the MPC8308 to abort all current internal and external transactions and set most registers to their default values.

2.1.2 External Interrupts

No external interrupt signals are used on MPC8308-NSG board.

2.1.3 Clock Distribution

Figure 2-2 and Table 2-1 show the clock distribution on the MPC8308-NSG board.

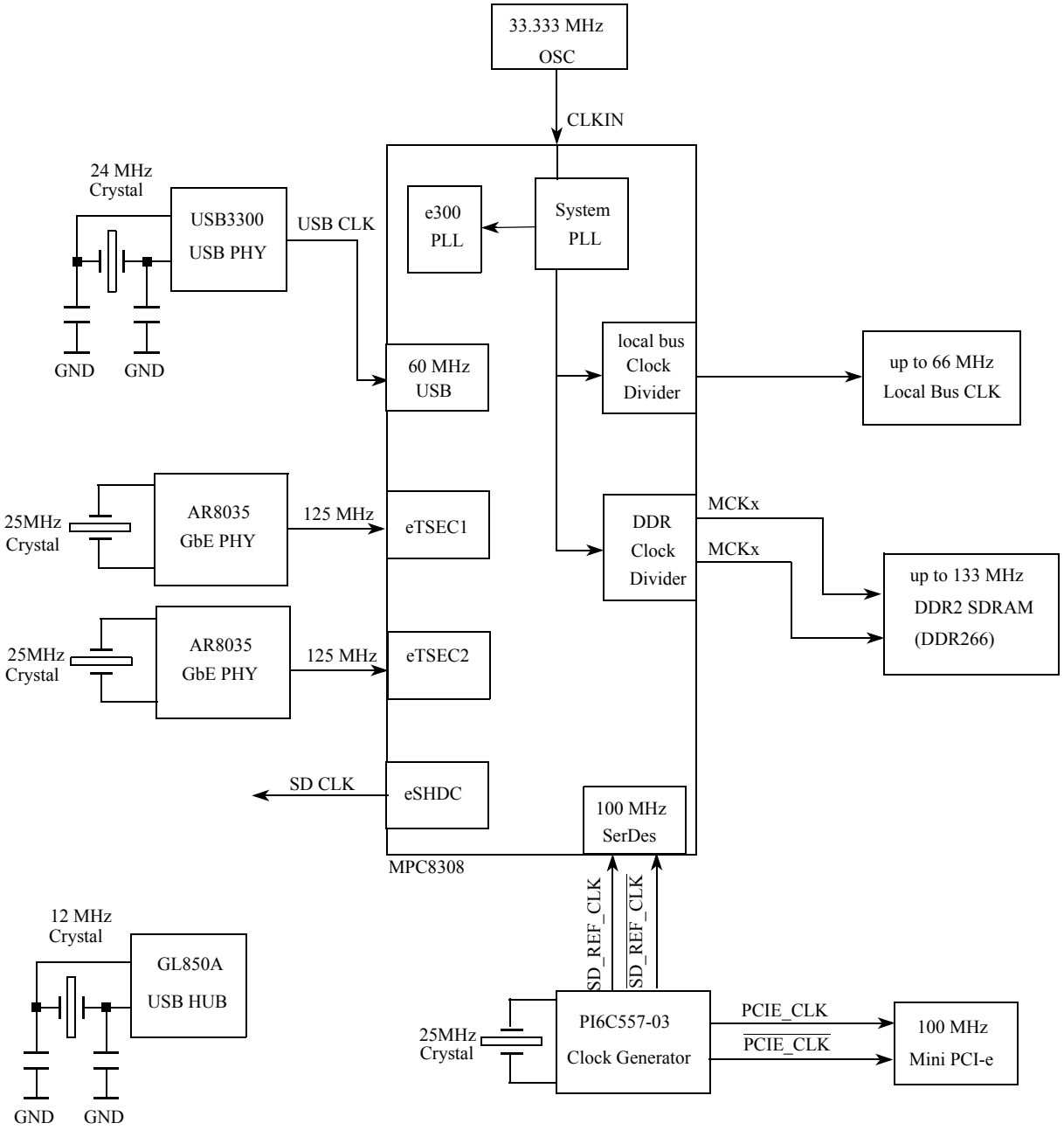

Figure 2-2. MPC8308-NSG Clock Distribution Diagram

Table 2-1. Clock Distribution

Clock Frequency	Module	Generated by	Description
33.333 MHz	MPC8308 CLKIN	33.333 MHz oscillator	The MPC8308 uses CLKIN as the reference clock to system PLL. From the power-on reset configuration, the internal PLL generates the CSB clock, which is fed to the e300 core PLL for generating the e300 core clock. The internal PLL also generates DDR clock for DDR controller and LBC clock for local bus.
125 MHz	MPC8308 eTSEC	AR8035	The gigabit Ethernet PHY (AR8035) provides a 125-MHZ clock for eTSEC operation.
133 MHz	DDR2 SDRAM	MPC8308	The DDR memory controller operates at twice the frequency of CSB clock.
66 MHz	Local Bus	MPC8308	The local bus memory controller operates with a frequency equal to CSB clock.
25 MHz	GBE PHY (AR8035)	25 MHz Crystal	The 25 MHz crystal generates the clock for GbE PHY.
60 MHz	MPC8308 USB	USB3300 USB PHY	60 MHz reference clock for MPC8308 USB module.
24 MHz	USB PHY (USB3300)	24 MHz crystal	
12 MHz	USB HUB Controller (GL850A)	12 MHz crystal	
100 MHz	SerDes Interface	25 MHz crystal and PI6C557-03 clock generator	100 MHz for SerDes reference clock.
100 MHz	Mini PCI-e Interface	25 MHz crystal and PI6C557-03 clock generator	100 MHz for Mini PCI-e card reference clock.
25/50 MHz	SD/MMC Interface	MPC8308	Reference clock for SD/MMC card.

2.1.4 DDR2 SDRAM Controller

MPC8308 uses DDR2 SDRAM as the system memory. The DDR2 interface uses the SSTL2 driver/receiver and 1.8 V power. A VREF 1.8V/2 is needed for all SSTL2 receivers in the DDR2 interface. For details on DDR timing design and termination, refer to the Freescale application note entitled

Hardware and Layout Design Considerations for DDR Memory Interfaces (AN2582). Figure 2-3 shows the DDR SDRAM controller connection.

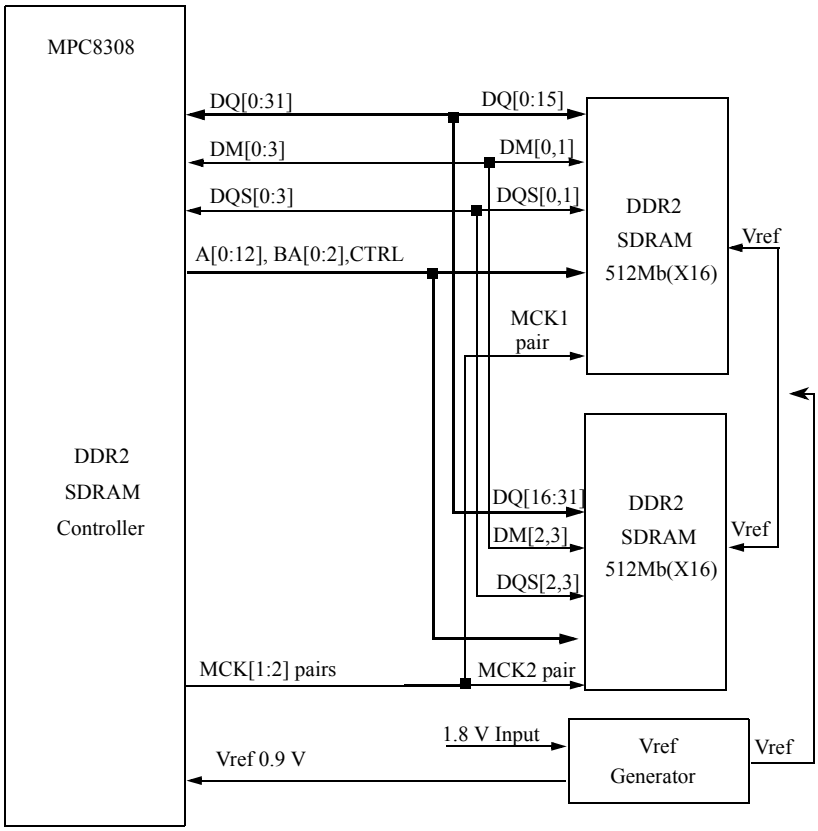

Figure 2-3. DDR2 SDRAM Connection

2.1.5 Local Bus Controller

The MPC8308 local bus controller has non-multiplexed 16-bit LD[0–15] data bus and 26-bit LA[0–25] address bus. The local bus speed is up to 66 MHz. The local bus drives one 8MB NOR Flash menory and one 32MB NAND Flash on the MPC8308-NSG board.

Figure 2-4 shows the block diagram and connections for the local bus.

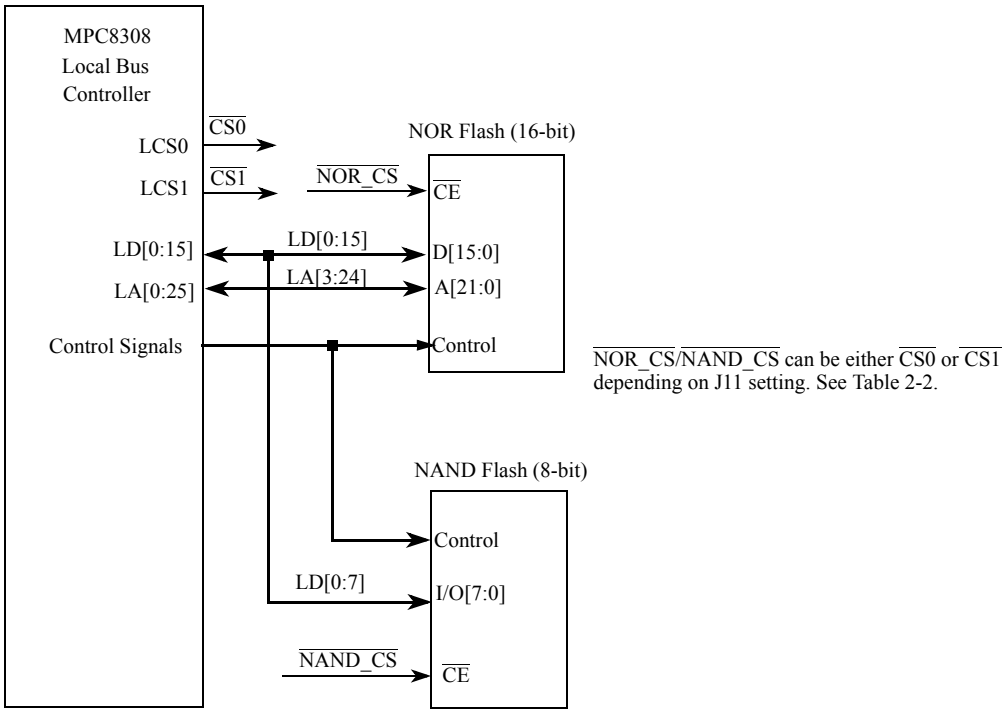

Figure 2-4. Local Bus Connections

2.1.6 Flash Memory

MPC8308-NSG provides 8Mbytes NOR Flash memory using general-purpose chip-select machine (GPCM). The NOR Flash is 16-bit port size in the system. One 32Mbytes 8-bit NAND Flash also connects to the local bus using NAND Flash control machine (FCM). The CS0, CS1 settings for NOR, NAND Flash and boot memory selecting is shown in below Table 2-2.

Table 2-2. Flash Memory Chip Selects and Boot ROM

J11	J6	J5	Description
Pin 1 & 3 short Pin 2 & 4 short	Pin 2 & 3 short	Open	NOR Flash CS0, NAND Flash CS1 Booting from NOR Flash.
Pin 1 & 2 short Pin 3 & 4 short	Pin 2 & 3 short	Short	NAND Flash CS0, NOR Flash CS1 Booting from NAND Flash.
Pin 1 & 3 short Pin 2 & 4 short	Pin 1& 2 short	Open	NOR Flash CS0, NAND Flash CS1 For CodeWarrior Operation

2.1.7 I^2C

The MPC8308 has two I^2C interfaces. On the MPC8308-NSG board, the MPC8308 serves as I^2C master for both I^2C buses (I2C1 and I2C2). I2C1 is connected to the following:

- Secure EEPROM AT88SC0104CA
- mini PCI-E socket

I2C2 is connected to the following:

- Serial EEPROM M24256 at address 0x50
- Zigbee module 0x00

2.1.8 PCI Express Interface (Mini PCI-E)

MPC8308 supports one PCI Express (PCI-E) interface. It is connected to one mini PCI-E connector as shown in Figure 2-5. It requires a 100-MHz reference clock, which is provided by the clock generator.

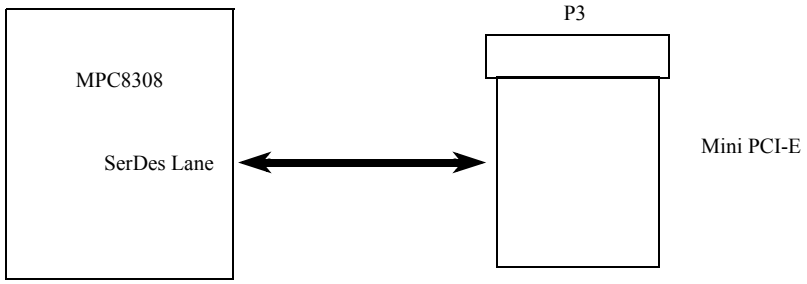

Figure 2-5. Mini PCI-E Connection

2.1.9 10/100/1000 BaseT Interface

On the MPC8308-NSG board, eTSEC1 and eTSEC2 use RGMII mode. The eTSEC1 and eTSEC2 drive two on-board 10/100/1000 PHYs (Atheros AR8035), respectively. The I/O voltage is set to 2.5 V RGMII. The RGMII (1000 BaseT) is a source synchronous bus. For a transmit bus connection, it is synchronous to GTX_CLK from the eTSEC module. The receive bus connection is synchronous to RX_CLK generated

from the PHY device. The MPC8308 MII management interface also connects to the RR8035. Figure 2-6 shows the connection between the MPC8308 eTSEC1 and eTSEC2 to the AR8035.

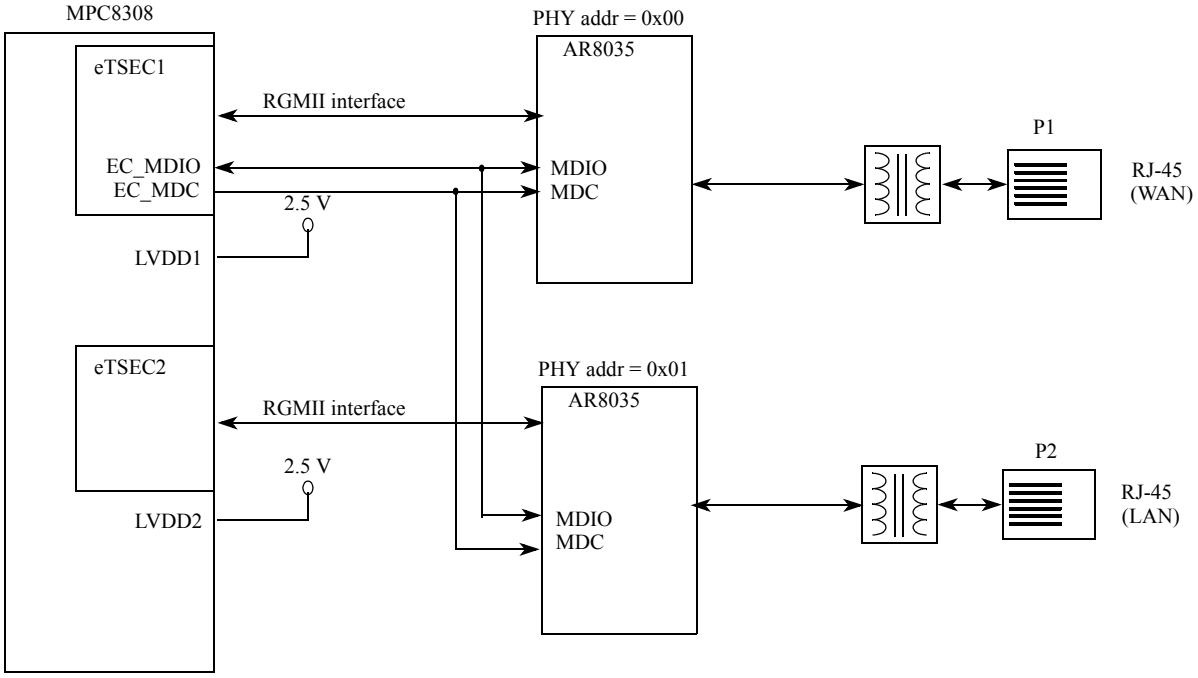

Figure 2-6. RGMII Interface Connection for 10/100/1000 BaseT Ethernet

2.1.10 UART Port

Figure 2-7 illustrates the serial port connection using a SP3232 3.3 V RS-232 driver to interface with a 3-pin right angle header available on the chassis. This serial connection runs at up to 115.2 Kbps.

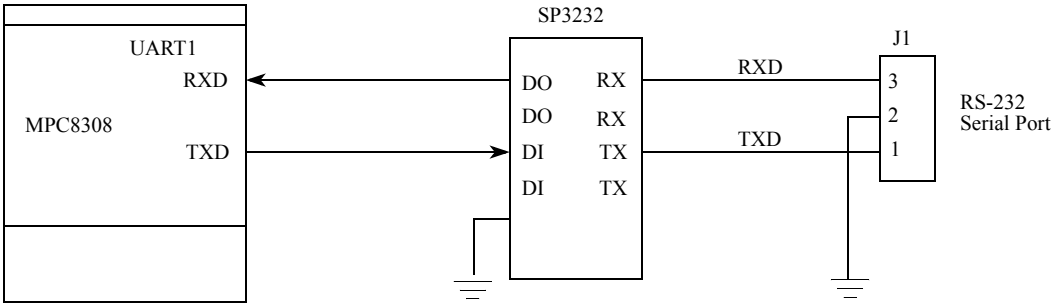

Figure 2-7. UART Debug Port Connection

2.1.11 USB 2.0 Interface

The MPC8308 has a internal USB modules (dual-role (DR) module). On the MPC8308-NSG board, it connects to the USB PHY (USB3300) through the 8-bit UTMI low-pin-count interface (ULPI). The USB3300 connects to one USB 2.0 HUB Controller GL850A with 4 downstream ports. Port 3 and 4 of the

USB HUB serve as USB host interfaces with USB Type A Receptacle. Figure 2-8 shows the connection of USB.

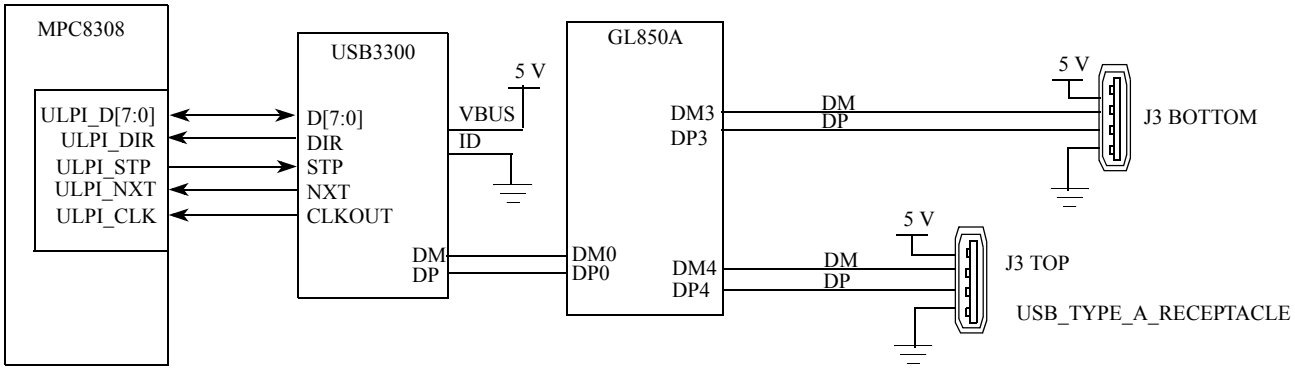

Figure 2-8. USB Port Connections

2.1.12 Zigbee Module

Zigbee Module ZFSM-201-2 from CEL is populated on the board. It is based on the Freescale™ chip MC13226V. UART2 or I2C2 of MPC8308 can be the interfaces for data exchange between MPC8308 and Zigbee Module. Header J8 selects which interface is used as shown in Table 2-3:

Table 2-3. Zigbee Module Interface Selection

J8	Description
Open	I2C interface is active, and UART is disabled
Short	UART interface is active, and I2C is disabled (default)

2.1.13 COP/JTAG Port

The common on-chip processor (COP) is part of the MPC8308 JTAG module and is implemented as a set of additional instructions and logic. This port can connect to a dedicated emulator for extensive system debugging. Several third-party emulators in the market can connect to the host computer through the

Ethernet port, USB port, parallel port, RS-232, etc. Figure 2-9 shows a typical setup using a USB port emulator.

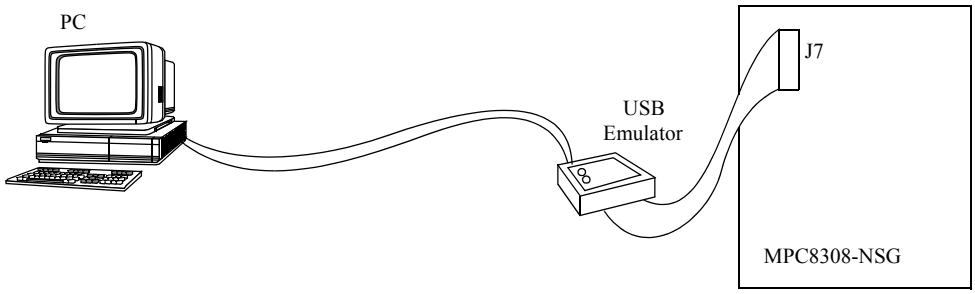

Figure 2-9. Connecting the MPC8308-NSG Board to a USB Emulator

The 16-pin generic header connector J7 carries the COP/JTAG signals and the additional signals for MPC8308 system debugging. Figure 2-10 shows the connector pinout.

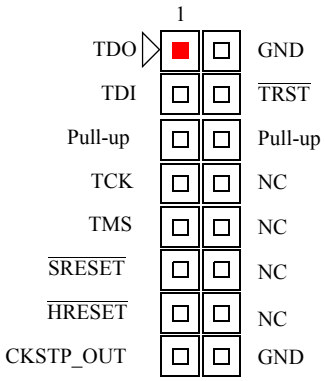

Figure 2-10. MPC8308-NSG Board COP Connector

2.1.14 GPIOs

MPC8308-NSG board uses GPIOs mutiplexed with IEEE1588 and GTM signals. System I/O Configuration Register High (SICRH) controls the multiplexing of GPIOs and the position of the GPIOs. The GPIO[0:15] of MPC8308 is provided at two places. Table 2-4 shows how the SICRH register is set:

Table 2-4. SICRH Bit Settings

Group	GPIO	Multiplexed with	SICRH Bits	Value	Description	GPIO Used for

IEEE1588_B	GPIO1	TSEC2_TMR_RX_ESFD	16-17	11	Select GPIO pin functionality for this signal group.	Zigbee Reset, not implemented yet
	GPIO2	TSEC2_TMR_TX_ESFD				Drive ERROR LED
	GPIO3	TSEC1_TMR_RX_ESFD				Drive RUN LED
	GPIO4	TSEC1_TMR_TX_ESFD				Drive Wi-Fi LED
GTM	GPIO9	$\overline{\text{GTM1\_TOUT3}}$	14-15	11	Select GPIO pin functionality for this signal group..	Manul Reset Button, not implemented by software yet
	GPIO10	$\overline{\text{GTM1\_TOUT4}}$				Drive Zigbee LED, not implemented yet
IEEE1588_A	GPIO11	TSEC_TMR_TRIG1	10-11	11	Select GPIO pin functionality for this signal group.	eTSEC1 GbE PHY INT
	GPIO12	TSEC_TMR_TRIG2				eTSEC2 GbE PHY INT
			23	1	GPIO[0:15] provided in function-3, selectable through GTM, IEEE1588_A, IEEE1588_B, and eTSEC2.	

2.2 MPC8308-NSG Assembly

Figure 2-11 shows the MPC8308-NSG board top view, with the references of LEDs, jumpers, headers, and switches.

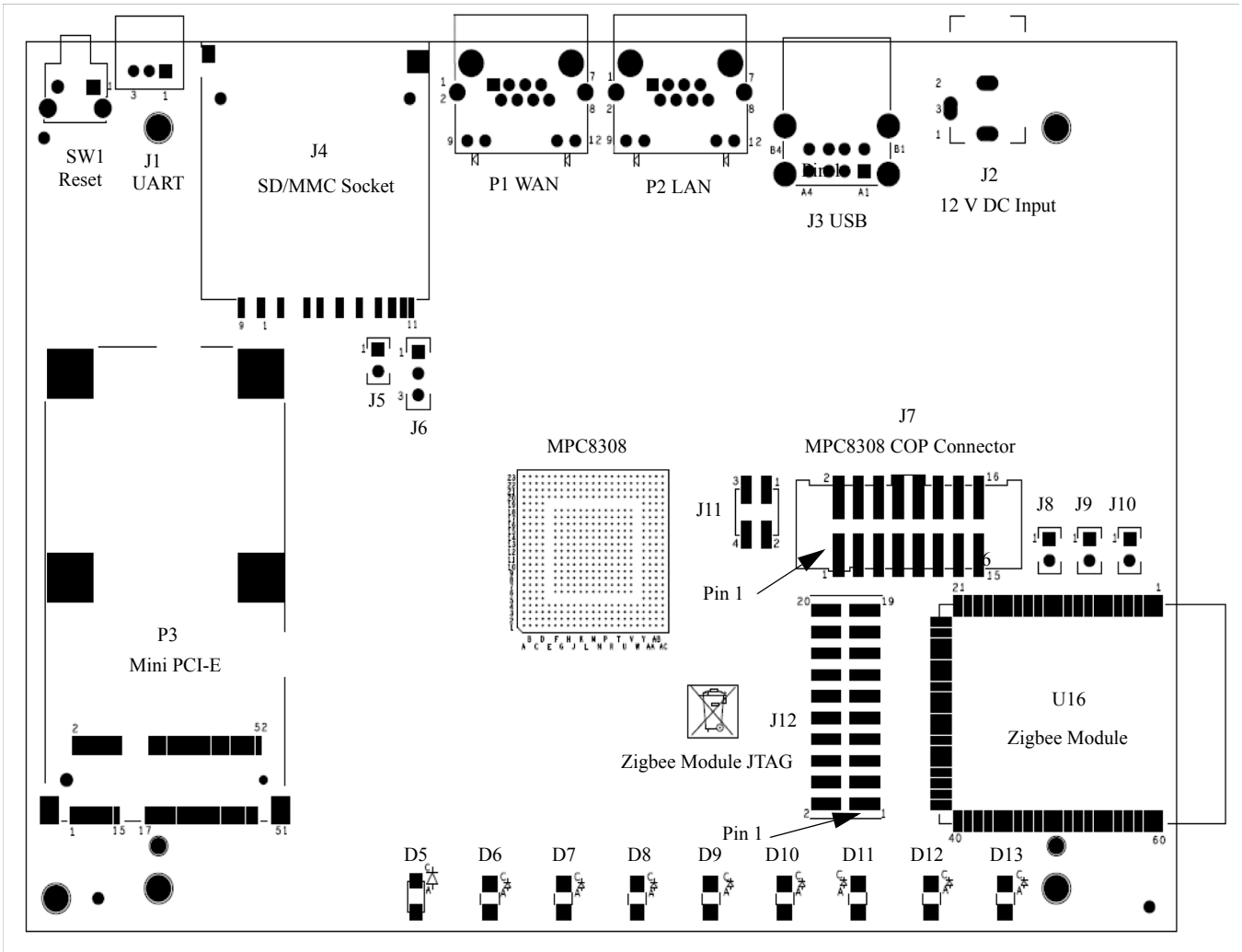

Figure 2-11. MPC8308-NSG Top View

CAUTION

Power down before mini PCI-e card insertion or removal.

Table 2-5 shows references and descriptions of LEDs, jumpers, headers, and switches.

Table 2-5. Lists of Connectors, Jumpers, Switches, and LEDs

Reference	Description
Connectors	
J7	16-pin MPC8308 COP/JTAG connector

Table 2-5. Lists of Connectors, Jumpers, Switches, and LEDs (continued)

Reference	Description
J12	20-pin Zigbee module JTAG connector
J3	Dual USB Type A receptacles (for USB high-speed external device)
J2	12 V DC power jack (external power adapter input)
J1	Serial port terminal connector (UART1) for MPC8308
P3	Mini PCI-E connector
P1	RJ-45 connector eTSEC1, WAN
P2	RJ-45 connector eTSEC2, LAN
J4	SD Card socket
Jumpers (Refer to Table 3-1)	
Switches	
SW1	System reset button. Resets the MPC8308-NSG board.
LEDs (See also Section 2.4, LEDs)	
D5	3.3 V Active (Power is on if lit, and 3.3 V power is good.)
D6 D7	Status LEDs controled by GPIOs of MPC8308 D6: RUN (GPIO3) D7: ERROR (GPIO2)
D8	Wi-Fi LED controlled by GPIO4 of MPC8308
D9	Zigbee LED controlled by Zigbee module
D10 D11	D10: WAN D11: LAN
D12 D13	Controlled by USB HUB GL850A D12: USB1 D13: USB2

2.3 Connectors

This section describes the MPC8308-NSG connectors and their pin assignments.

2.3.1 MPC8308 COP Connector

The COP connector (J7) allows the user to connect a COP/JTAG-based debugger to the MPC8308-NSG board for debugging. Table 2-6 lists the pin assignments of the COP connector.

Table 2-6. COP Connector Pin Assignments

Pin	Signal	Pin	Signal
1	TDO	2	GND
3	TDI	4	$\overline{\text{TRST}}$

Table 2-6. COP Connector Pin Assignments

Pin	Signal	Pin	Signal
5	$\overline{\text{QREQ}}$	6	VDD_SENSE
7	TCK	8	$\overline{\text{CHKSTOP\_IN}}$
9	TMS	10	NC
11	$\overline{\text{SRESET}}$	12	NC
13	$\overline{\text{HRESET}}$	14	NC
15	$\overline{\text{CHKSTOP\_OUT}}$	16	GND

2.3.2 UART Connector

Serial interface UART1 is available at connector (J1) with pin assignments as shown in Table 2-7.

Table 2-7. UART Connector Pins

Pin	Signal
1	TXD
2	GND
3	RXD

2.3.3 Zigbee Module JTAG Connector

The 2x10 header J12 is JTAG connector for Zigbee module development tool. Table 2-8 lists the pin assignments of the JTAG connector.

Table 2-8. Zigbee Module JTAG Connector Pin Assignments

Pin	Signal	Pin	Signal
1	VTREF	2	VSUPPLY
3	$\overline{\text{TRST}}$	4	GND
5	TDI	6	GND
7	TMS	8	GND
9	TCK	10	GND
11	RTCK	12	GND
13	TDO	14	GND
15	$\overline{\text{SRESET}}$	16	GND
17	DBGRQ	18	GND
19	DBGACK	20	GND

2.3.4 Power Connector

J2 is a DC jack for a 12 V power supply to the MPC8308-NSG board.

2.4 LEDs

Figure 2-12 shows 9 LED indicators on the front panel of MPC8308-NSG.

Figure 2-12. LED Indicators on the Front Panel of MPC8308-NSG

2.4.1 Power-on LED

Yellow Power LED (D5) indicates the system is power-on if lit.

2.4.2 Programmable LEDs

RUN, ERROR, WIFI and ZIGBEE LEDs are all software controlled LEDs. GPIOs of MPC8308 and Zigbee module drive these LEDs. Writing 0 turns on them, and writing 1 turns off them.

Green RUN LED (D6) and Red ERROR LED (D7) indicate the status of diagnostics for MPC8308-NSG board. The RUN LED is lit when system goes through the diagnostics successfully (SW not implemented yet). The ERROR LED is on if the system finds some problems during the diagnostics (SW not implemented yet). GPIO3 drives LED RUN, and GPIO2 drives LED ERROR.

Blue Wi-Fi LED (D8) indicates whether the WiFi Card is inserted and activated (SW not implemented yet). GPIO4 controls this LED.

Blue Zigbee LED (D9) indicates whether the Zigbee module is activated. Zigbee module drives this LED.

2.4.3 Ethernet LEDs

Blue WAN LED (D10) indicates the link and activity of WAN (eTSEC1)

Blue LAN LED (D11) indicates the link and activity of LAN (eTSEC2)

2.4.4 USB LEDs

Blue USB1 LED (D12) indicates if there is a USB device is working (USB connector BOTTOM)

Blue USB2 LED (D13) indicates if there is a USB device is working (USB connector TOP)

2.5 MPC8308-NSG Board Configuration

This section describes the operational mode and configuration options of the MPC8308-NSG board.

2.5.1 Reset Configuration Word

The reset configuration word (RCW) controls the clock ratios and other basic device functions, such as boot location, TSEC modes, and endian mode. The reset configuration word is divided into reset configuration word lower (RCWL) and reset configuration word higher (RCWH) and is loaded from the local bus during the power-on or hard reset flow. On the MPC8308-NSG board, the RCW low-bit setting is 0x4406_0000, and RCW high-bit setting is 0xA060_6C00.

The RCW is located at the lowest 64 bits of the boot Flash memory, which is 0xFE00_0000 on this board.

Figure 2-13 and Figure 2-14 show the RCW definitions.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	LBIUCM	DDRCM	SVCOD			SPMF			—	COREPLL						
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	—															

Figure 2-13. Reset Configuration Word Low (RCWL) Bit Settings

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Field	—				COREDIS	BMS	BOOTSEQ		SWEN	ROMLOC			RLEXT		—	—
	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Field	TSEC1M				TSEC2M				—				TLE		—	

Figure 2-14. Reset Configuration Word High (RCWH) Bit Settings

Table 2-9. RCWL Bit Descriptions

Bits	Name	Meaning	Description	
0	LBIUCM	Local bus memory controller clock mode	Local Bus Controller Clock : CSB_CLK	
			0: Default	ratio 1:1
			Note: This bit should always be set to 0.	
1	DDRCM	DDR SDRAM memory controller clock mode	DDR Controller Clock : CSB_CLK	
			1: Default	ratio 2:1
			Note: This bit should always be set to 1.	
2–3	SVCOD[0-1]	System PLL VCO division	00 (Default)	2
			01	4
			10	8
			11	Reserved
			Note: For the frequency of operation for MPC8308, 00 si the only applicable value of SVCOD.	

Table 2-9. RCWL Bit Descriptions (continued)

Bits	Name	Meaning	Description	
4–7	SPMF[0–3]	System PLL multiplication factor	CSB_CLK : SYS_CLK_IN	
			0000	Reserved
			0001	Reserved
			0010	2:1
			0011	3:1
			0100 (default)	4:1
			0101	5:1
			0110	6:1
			0111-1111	Reserved, should not be set
8	—	Reserved	Should be cleared.	
9–15	COREPLL [0–6]	Value	coreclk: csb_clk	VCO divider
		nn 0000 0	PLL bypassed	PLL bypassed
		11 nnnn n	n/a	n/a
		00 0001 0	1:1	2
		01 0001 0	1:1	4
		10 0001 0	1:1	8
		00 0001 1	1.5:1	2
		01 0001 1	1.5:1	4
		10 0001 1	1.5:1	8
		00 0010 0	2:1	2
		01 0010 0: Default	2:1	4
		10 0010 0	2:1	8
		00 0010 1	2.5:1	2
		01 0010 1	2.5:1	4
		10 0010 1	2.5:1	8
		00 0011 0	3:1	2
		01 0011 0	3:1	4
		10 0011 0	3:1	8
16–31	—	Reserved.	Should be cleared.	

Table 2-10. RCWH Bit Descriptions

Bits	Name	Meaning	Detailed Description	
0-3	—	Reserved	Should be cleared	
4	COREDIS	Core disable mode	0: Default	e300 enabled
			1	e300 disabled

Table 2-10. RCWH Bit Descriptions (continued)

Bits	Name	Meaning	Detailed Description	
5	BMS	Boot memory space	0: Default	0x0000_0000–0x007F_FFFF
			1	0xFF80_0000–0xFFFF_FFFF
6–7	BOOTSEQ	Boot sequencer configuration	00: Default	Boot sequencer is disabled
			01	Boot sequencer load configuration from I^2C in normal I^2C addressing mode.
			10	Boot sequencer load configuration from I^2C in extended I^2C addressing mode.
			11	Reserved
8	SWEN	Software watchdog enable	0: Default	Disabled
			1	Enabled
9–11	ROMLOC	Boot ROM interface location	000	RLEXT= 00: DDR SDRAM RLEXT= 01: Reserved
			001	RLEXT= 00: Reserved RLEXT= 01: Local bus NAND Flash, 8 bit smal page ROM
			010	Reserved
			011	Reserved
			100	Reserved
			101	RLEXT= 00: Local bus GPCM, 8 bits RLEXT= 01: Local bus NAND Flash, 8 bit large page ROM
			110: Default	RLEXT= 00: Local bus GPCM, 16 bits RLEXT= 01: Reserved
			111	Reserved
12–13	RLEXT	Boot ROM location extension	00: Default	Legacy mode
			01	NAND Flash mode
			10	Reserved
			11	Reserved
14–15	—	Reserved	Should be cleared	

Table 2-10. RCWH Bit Descriptions (continued)

Bits	Name	Meaning	Detailed Description	
16–18	TSEC1M	TSEC1 Mode	000	MII
			001	Reserved
			010	Reserved
			011: Default	RGMII
			100	Reserved
			101	Reserved
			110	ReservedI
			110	Reserved
19–21	TSEC2M	TSEC2 Mode	000	MII
			001	Reserved
			010	Reserved
			011: Default	RGMII
			100	Reserved
			101	Reserved
			110	Reserved
			110	Reserved
22–27	—	Reserved	Should be cleared	
28	TLE	True little endian	0: Default	Big-endian mode
			1	True little endian mode
29-31	—	Reserved	Should be cleared	

2.5.2 Power Supply

The MPC8308 requires a 12 V power supply from the DC power jack for normal operation. Low voltage 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V and 1.0 V are all generated from 12 V by switching regulators. The 1.0 V power is for a CPU core. The 1.5 V is for mini PCI-E connector. The 1.8 V power is for the DDR controller. The 5 V power is for USB interface. The 2.5 V is for RGMII interface.

2.5.3 Chip-Select Assignments and Memory Map

Table 2-11 shows an example memory map on the MPC8308 that is used for u-boot in the Flash memory.

Table 2-11. Example Memory Map, Local Access Window, and Chip-Select Assignments

Address Range	Target Interface	Chip-Select Line	Device Name	Port Size (Bits)
0x0000_0000–0x07FF_FFFF	DDR	MCS0	DDR2 SDRAM (128 Mbyte)	32
0xA000_0000–0xAFFF_FFFF	PCI-E	Nil	PCI-E memory space (256 Mbyte)	—
0xB100_0000–0xB17F_FFFF	PCI-E	Nil	PCI-E I/O space (8 Mbyte)	—
0xE000_0000–0xE00F_FFFF	Internal bus	Nil	IMMR (1 Mbyte)	—
0xFE00_0000–0xFE7F_FFFF	Local bus	LCS0	NOR Flash memory (8 Mbyte)	16
0xE060_0000–0xE060_7FFF	Local bus	LCS1	NAND Flash memory (32 Kbyte)	8

2.6 Electric Characteristics

Table 2-12 lists the electric characteristics of the MPC8308-NSG board.

Table 2-12. MPC8308-NSG Board Characteristics

Characteristics	Specifications
Power input:	12.0 V DC 2.0 A
Communication processor	MPC8308 running @ up to 400 MHz
Flash memory (local bus) DDR SDRAM	8 Mbyte NOR Flash 32 Mbyte NAND Flash 128 Mbyte DDR2 SDRAM at DDR266
Operating temperature	0°C to 70°C (room temperature)
Storage temperature	–25°C to 85°C
Relative humidity	5% to 90% (noncondensing)
PCB dimensions: Length Width Thickness	 5748 mil 4133 mil 67 mil

2.7 Mechanical Data

Figure 2-15 shows the MPC8308-NSG dimensions (in inch). The board dimensions are 105 mm × 146 mm (4.133 inches × 5.748 inches).

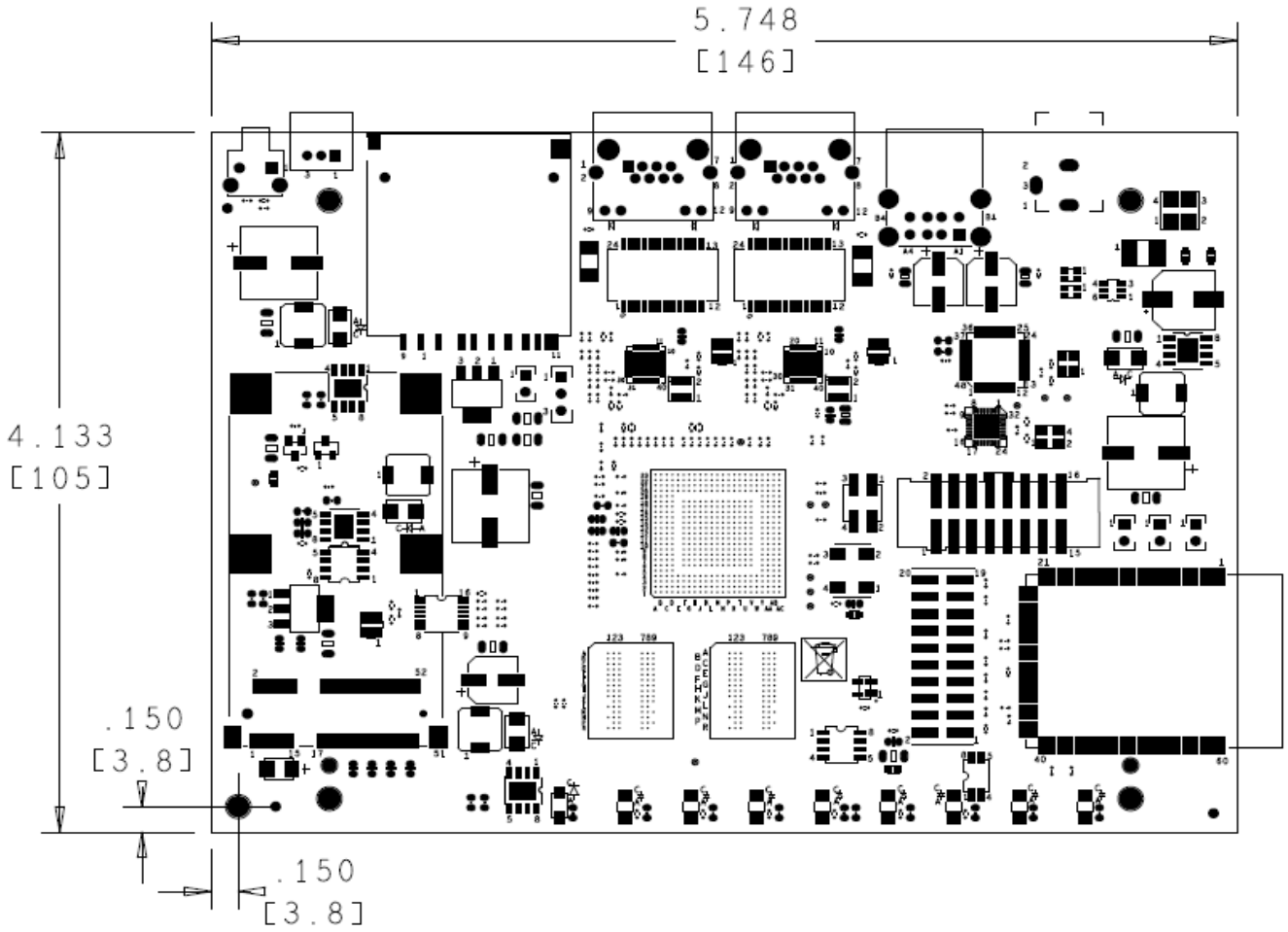

Figure 2-15. Dimensions of the MPC8308-NSG Board

Chapter 3
Board Bootup

This chapter describes how to boot up the MPC8308-NSG board. The factory has preloaded a Flash image onto the on-board Flash memory. Before powering up the board, set the on-board jumpers according to the settings listed in Section 3.1, Board Jumper Settings.

This document is organized as follows:

- Section 3.1, Board Jumper Settings. This section shows default jumper settings for board bootup.
- Section 3.2, External Connections. This section illustrates all available external connections of the MPC8308-NSG board.

CAUTION

Avoid touching areas of circuitry and connectors; static discharge can damage circuits.

3.1 Board Jumper Settings

Figure 3-1 shows jumpers on top of the MPC8308-NSG with red outlines at jumper designators J5, J6, J8, J9, J10 and J11. A square pad indicates pin 1 of the part. Table 3-1 shows the default jumper settings.

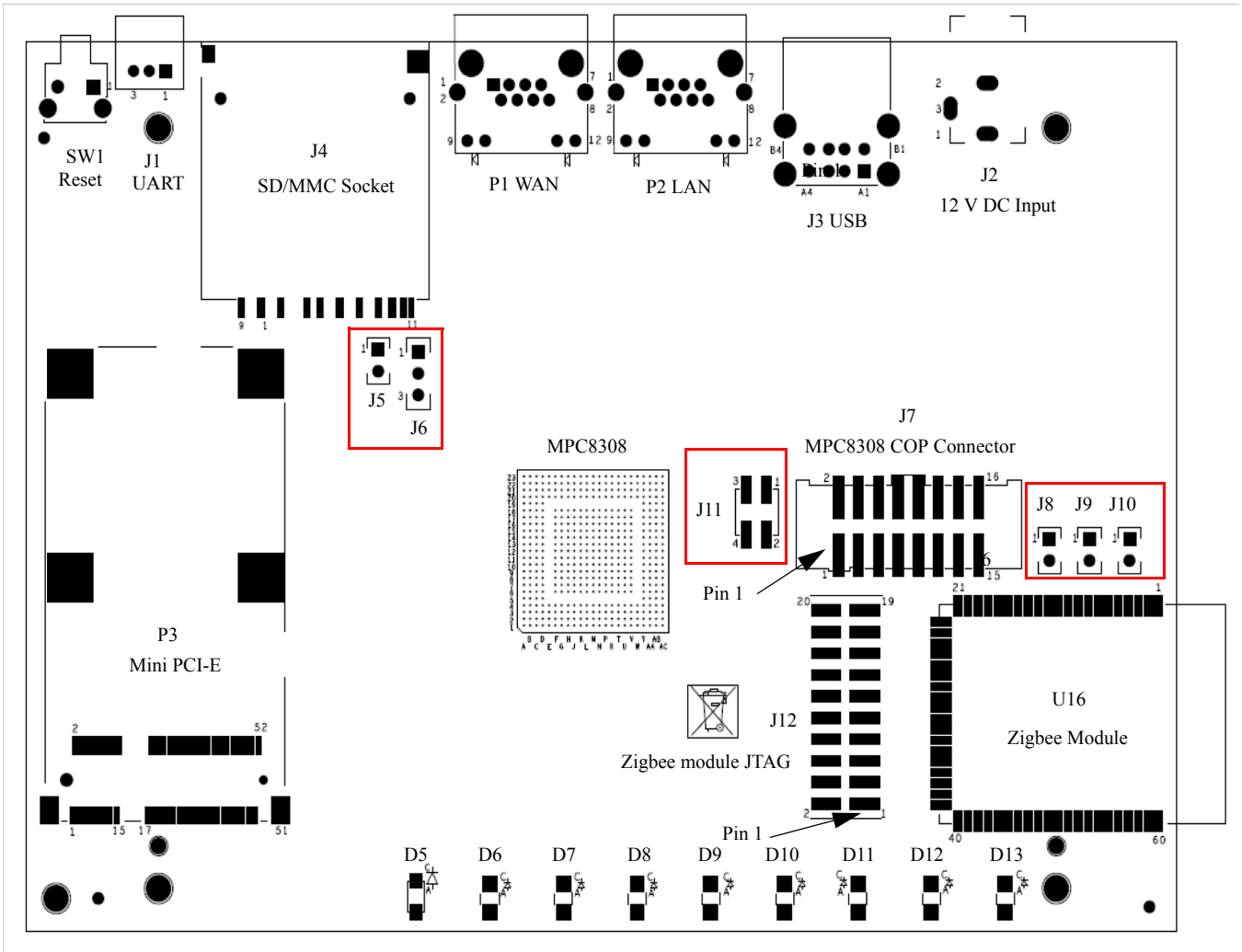

Figure 3-1. Jumpers on MPC8308-NSG Top View

Table 3-1. Default Jumper Settings

Reference	Default Jumper Setting	√ = Jumper × = No Jumper	Description
J5		×	Jumper 1-2: boot from NAND Flash (small page). Default is no jumper.
J6	2–3	√	Select the reset configuration source (RST-CFG-SRC) for the MPC8308. Jumper 2-3 (default): 0000 Reset configuration word is loaded from NOR Flash. Jumper 1-2: 1011 Hard-coded option 3. Reset configuration word is not loaded (for CodeWarrior connection).

Table 3-1. Default Jumper Settings (continued)

Reference	Default Jumper Setting	√ = Jumper × = No Jumper	Description
J8	1-2	√	Jumper 1-2 (default): active UART2 to communicate with Zigbee module. No Jumper: disable UART2 and active I^2C2 to communicate with Zigbee module.
J9		×	Select the Zigbee module on-board flash erase mode. J9, J10 both no Jumpers (default): not erase the FLASH on Zigbee module through the boot process J9, J10 both Jumpers: erase the FLASH on Zigbee module through the boot process
J10		×	
J11	1-3 2-4	√ √	Jumper 1-3 & 2-4: NOR Flash CS0, NAND Flash CS1 Jumper 1-2 & 3-4: NAND Flash CS0, NOR Flash CS1

3.2 External Connections

Figure 3-2 shows the external connections.

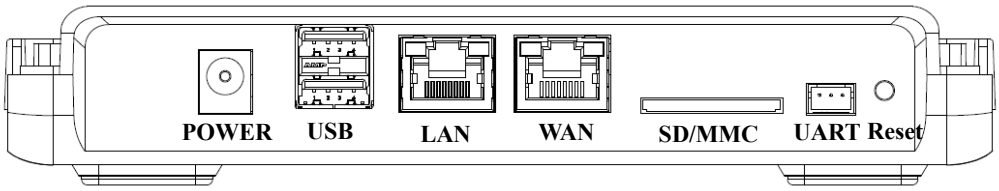

Figure 3-2. External Connections

NOTE

Strong electromagnetic interference might disturb the normal function of the product. If so, simply reset the product to resume normal operation by following the steps in the software user guide. If normal function does not return, please move the product to another location.

Chapter 4
Zigbee Module

This chapter introduces the specifications of CEL™ Zigbee module ZFSM-201-2 used on MPC8308-NSG board.

ZFSM-201-2 Zigbee module is based on the Freescale™ MC13226 transceiver platform. It is ideal for remote sensing, AMR/AMI, home and building automation, industrial control, and security applications.

This document is organized as follows:

- Section 4.1, Features of Zigbee Module. This section lists features of the Zigbee module.
- Section 4.2, Communication Interface and JTAG Port. This section shows Zigbee module connections

4.1 Features of Zigbee Module

- Powerful 32-bit ARM7TDMI based microprocessor, up to 26MHz
- Extensive on-board memory resources
  - 128Kbyte serial FLASH memory (can be mirrored into RAM)
  - 96Kbyte SRAM
  - 80Kbyte ROM
- Up to 100mW output power
- Miniature footprint: 1” x 1.4” (25.4 mm x 36.5 mm)
- Integrated PCB trace antenna
- 15 RF channels
- Over 4000 feet of range
- AES 128-bit encryption
- Low power consumption
- FCC, CE and IC certified
- RoHS compliant

4.2 Communication Interface and JTAG Port

Both UART and I2C interfaces are connected to Zigbee module. The interfaces on MPC8308 chip are UART2 and I2C2. UART is the default data communication interface.

Figure 4-1 shows the Zigbee module connection.

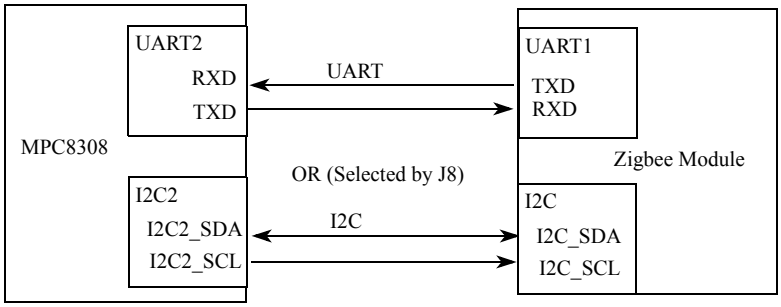

Figure 4-1. Zigbee Module Connection

Table 4-1 shows how to change the communication interfaces between Zigbee module and MPC8308.

Table 4-1. Communication Interface Selection

J8	Communication Interface
Pin 1-2: Short (default)	UART
Pin 1-2: Open	I2C

The 20-pin header connector J12 carries the JTAG signals of Zigbee module. Figure 4-2 shows the connector pinout.

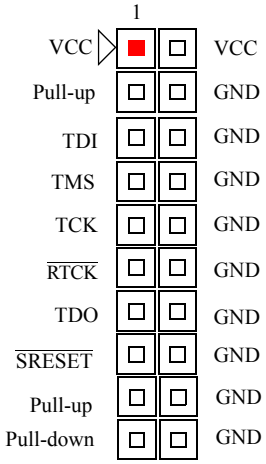

Figure 4-2. Zigbee Module JTAG Connector

The Zigbee module on-board flash can be erased through the boot process. Table 4-2 shows how to select the flash mode in Zigbee module boot process

Table 4-2. Zigbee Module on-board Flash Erase Mode

Mode	J9	J10	Mode of Operation
Recovery Mode	Pin 1-2: Short	Pin 1-2: Short	Erase the FLASH on Zigbee module through the boot process

Mode	J9	J10	Mode of Operation
Non-recovery Mode (default)	Pin 1-2: Open	Pin 1-2: Open	Not erase the FLASH on Zigbee module through the boot process

Chapter 5
Wi-Fi Card

This chapter introduces the specifications of SparkLAN's Wi-Fi card WPER-120GN used on MPC8308-NSG board.

This document is organized as follows:

- Section 5.1, Electric Specifications of Wi-Fi Card. This section lists the key specifications of Wi-Fi card.

5.1 Electric Specifications of Wi-Fi Card

Table 5-1 lists the electric specifications of WPER-120GN.

Table 5-1. Electric Specifications of WPER-120GN

Category	Key Specifications
Main Chipset	Ralink® RT3092, 2T2R, transmission rates up tp 300Mbps
Standard Conformance	802.11b, 802.11g, and 802.11n
Operating Frequency	b/g/n ISM Band: 2.412~2.472 GHz
Interface	Half Mini PCI Express Card
Operation Voltage	3.3V ±5%
Modulation Technique	•802.11b: CCK, DQPSK, DBPSK •802.11g: OFDM •802.11g/n: 64-QAM, 16-QAM, QPSK, BPSK
Output Power	•802.11b: 18dBm +/- 1.5dBm •802.11g: 15dBm +/- 1.5dBm •802.11n: 15dBm +/- 1.5dBm
Receive Sensitivity	•802.11b: -85dBm +/- 2dBm @ 11Mbps •802.11g: -72dBm +/- 2dBm @ 54Mbps •802.11n HT20: -70dBm +/- 2dBm @ 150Mbps •802.11n HT40: -67dBm +/- 2dBm @ 300Mbps
Power Consumption	•Continue TX: Max 510mA •Continue RX: Max 260mA
Operation System Supported	Driver: Windows 2000/XP/Vista, Win7, Linux2.6 above Security: 64/128bits WEP, WPA, WPA2
Dimension	30mm x 26.8mm x 3.5mm
Operation Temperature Range	0°C ~ +60°C
Storage Temperature Range	-10°C ~ +85°C

Table 5-1. Electric Specifications of WPER-120GN (continued)

Operating Humidity	5% ~ 90%, non-condensing
Storage Humidity	5% ~ 95%, non-condensing