Section 55. DDR SDRAM Controller

This section of the manual contains the following major topics:

Note:	This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32 devices. Please consult the note at the beginning of the **"DDR SDRAM Controller"** chapter in the current device data sheet to determine whether this document supports the device you are using. Device data sheets and family reference manual sections are available for download from the Microchip Web site at: http://www.microchip.com

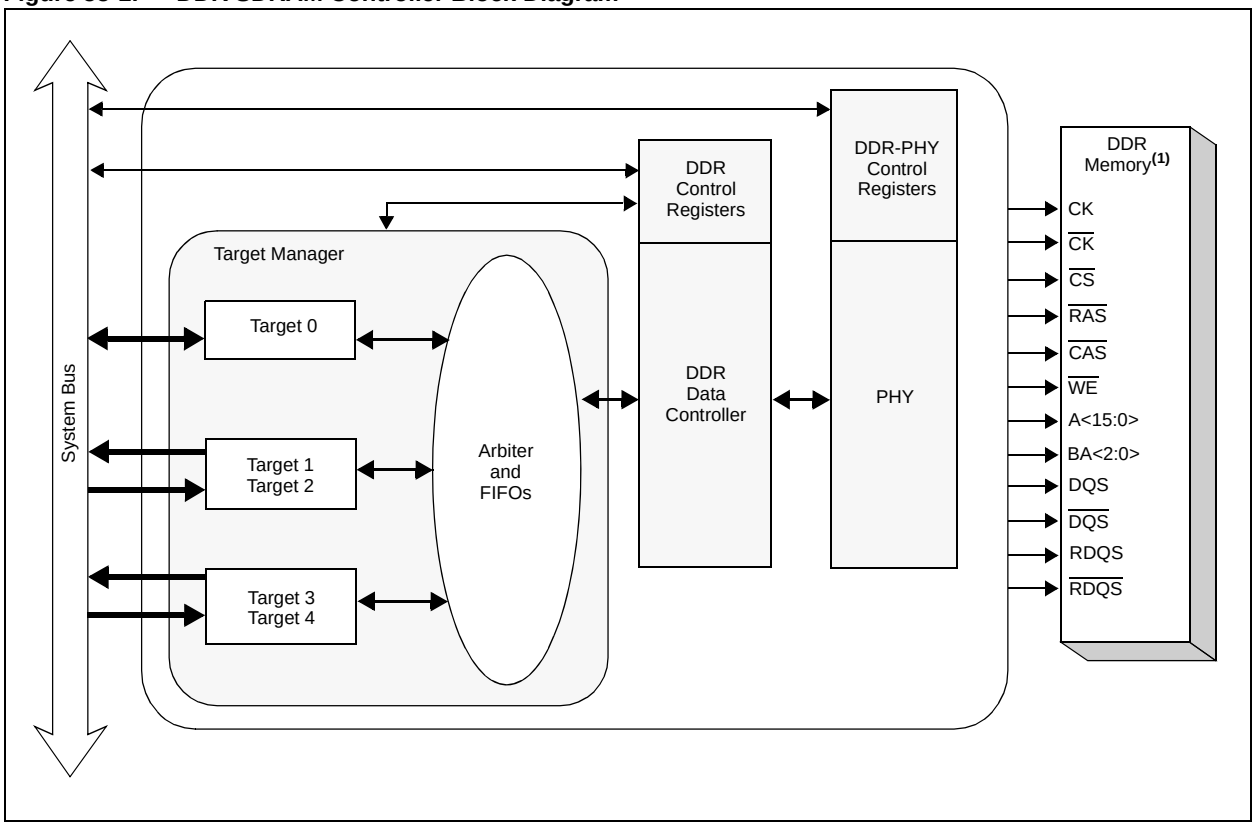
55.1 INTRODUCTION

The DDR Synchronous Dynamic Random Access Memory (SDRAM) Controller implements the controls for an external memory bus interface using the Dual Data Rate (DDR) Version 2 protocol and electrical interface that adheres to the JEDEC Standard JESD79-2F (Nov. 2009).

The component consists of a DDR SDRAM Controller Core with configurable options and a DDR Physical Interface.

A block diagram showing how these components are interfaced is illustrated in Figure 55-1.

Figure 55-1: DDR SDRAM Controller Block Diagram



55.2 CONTROL REGISTERS

The DDR SDRAM Controller has the following Special Function Registers (SFRs):

- **DDRTSEL: DDR Target Select Register**

  This register selects the target for which the arbitration parameters are to be programmed.

- **DDRMINLIM: DDR Minimum Burst Limit Register**

  This register sets the number of bursts that a target must have access to without interruption from another target.

- **DDRRQPER: DDR Request Period Register**

  This register, in conjunction with the DDRMINCMD register, sets the percentage of total bandwidth allocated to the target.

- **DDRMINCMD: DDR Minimum Command Register**

  This register, in conjunction with the DDRRQPER register, sets the percentage of total bandwidth allocated to the target.

- **DDRMEMCON: DDR Memory Control Register**

  This register enables the delivery of initialization commands to the DDR memory.

- **DDRMEMCFG0: DDR Memory Configuration Register 0**

  This register sets address parameters for the DDR memory.

- **DDRMEMCFG1: DDR Memory Configuration Register 1**

  This register sets the row address mask for the DDR memory.

- **DDRMEMCFG2: DDR Memory Configuration Register 2**

  This register sets the column address (high) mask for the DDR memory.

- **DDRMEMCFG3: DDR Memory Configuration Register 3**

  This register sets the column address (low) mask for the DDR memory.

- **DDRMEMCFG4: DDR Memory Configuration Register 4**

  This register sets the Chip Select and bank address masks for the DDR memory.

- **DDRREFCFG: DDR Refresh Configuration Register**

  This register sets the refresh parameters for the DDR memory.

- **DDRPWRCFG: DDR Power Configuration Register**

  This register sets the ECC and low-power parameters for the controller.

- **DDRDLYCFG0: DDR Delay Configuration Register 0**

  This register sets the timing parameters for the DDR memory.

- **DDRDLYCFG1: DDR Delay Configuration Register 1**

  This register sets the timing parameters for the DDR memory.

- **DDRDLYCFG2: DDR Delay Configuration Register 2**

  This register sets the timing parameters for the DDR memory.

- **DDRDLYCFG3: DDR Delay Configuration Register 3**

  This register sets the timing parameters for the DDR memory.

- **DDRODTCFG: DDR On-Die Termination Configuration Register**

  This register sets the timing parameters for enabling on-die termination.

- **DDRXFERCFG: DDR Transfer Configuration Register**

  This register sets the timing parameters for data transfer.

- **DDRCMDISSUE: DDR Command Issue Register**

  This register sets the number of initialization commands to be issued to the DDR memory.

- **DDRODTENCFG: DDR On-Die Termination Enable Configuration Register**

  This register selects the active Chip Select for the on-die termination timings in the DDROT-DCFG register.
- **DDRMEMWIDTH: DDR Memory Width Register**

  This register sets the DDR memory width in the controller.
- **DDRCMD1x: DDR Host Command 1 Register 'x' ('x' = 0 through 15)**

  This register holds the lower 32 bits of a DDR memory initialization command.
- **DDRCMD2x: DDR Host Command 2 Register 'x' ('x' = 0 through 15)**

  This register holds the upper 20 bits of a DDR memory initialization command.
- **DDRSCLSTART: DDL Self-Calibration Logic Start Register**

  This register is used to initialize the Self-Configuring Logic of the DDR PHY.
- **DDRSCLLAT: DDL Self-Calibration Logic Latency Register**

  This register is used to set the timing parameters for the DDR PHY Self-Configuring Logic.
- **DDRSCLCFG0: DDR SCL Configuration Register 0**

  This register sets PHY Self-Configuring Logic parameters.
- **DDRSCLCFG1: DDR SCL Configuration Register 1**

  This register sets PHY Self-Configuring Logic parameters.
- **DDRPHYPADCON: DDR PHY Pad Control Register**

  This register sets pad drive parameters for the PHY.
- **DDRPHYDLLR: DDR PHY DLL Recalibrate Register**

  This register controls the recalibration of the Delay Lock Loop (DLL).
- **DDRPHYCLKDLY: DDR PHY Clock Delta Delay Register**

  This register controls additional SCL latency settings.

Table 55-1 provides a summary of all DDR SDRAM Controller SFRs. Corresponding registers appear after the summaries, which include a detailed description of each bit.

Table 55-1: DDRC Register Summary

Register Name	Bit Range	Bits															
		31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
DDR TSEL	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	TSEL<7:0>							
DDR MINLIM	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	MINLIMIT<4:0>				
DDR RQPER	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	RQPER<7:0>							
DDR MINCMD	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	MINCMD<7:0>							
DDR MEMCON	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INITDN	STINIT
DDR MEMCFG0	31:16	—	APCHRGEN	—	CLHADDR<4:0>					—	—	—	CSADDR<4:0>				
	15:0	—	—	—	BNKADDR<4:0>					—	—	—	RWADDR<4:0>				
DDR MEMCFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	RWADDRMSK<12:0>												
DDR MEMCFG2	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	CLADDRHMSK<12:0>												
DDR MEMCFG3	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	CLADDRLMSK<12:0>												
DDR MEMCFG4	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	CSADDRMSK<2:0>			—	—	—	BNKADDRMSK<2:0>		
DDR REFCFG	31:16	—	—	—	—	—	MAXREFS<2:0>			REFDLY<7:0>							
	15:0	REFCNT<15:0>															
DDR PWRCFG	31:16	—	—	—	—	—	—	—	—	—	PCHRG PWRDN	SLFREFDLY<9:4>					
	15:0	SLFREFDLY<3:0>				PWRDNDLY<7:0>								ASLFREFEN	APWRDNEN	—	—
DDR DLYCFG0	31:16	RMWDLY<3:0>				R2WDLY>3:0>				W2WCSDLY<3:0>				W2WDLY<3:0>			
	15:0	R2RCSDLY<3:0>				R2RDLY<3:0>				W2RCSDLY<3:0>				W2RDLY<3:0>			
DDR DLYCFG1	31:16	—	SLFREF EXDLY<8>	NXTDAT AVDLY<4>	W2R CSDLY<4>	W2R DLY<4>	W2PCHRG DLY<4>	PWRDNEXDLY<5:0>						PWRDNMINDLY<3:0>			
	15:0	SLFREFEXDLY<7:0>								SLFREFMINDLY<7:0>							
DDR DLYCFG2	31:16	RBENDDLY<3:0>				PCHRG2RASDLY<3:0>				RAS2CASDLY<3:0>				RAS2RASDLY<3:0>			
	15:0	W2PCHRGDLY<3:0>				R2PCHRGDLY<3:0>				—	—	—	—	PCHRGALLDLY<3:0>			
DDR DLYCFG3	31:16	—	—	—	—	—	—	—	—	—	—	FAWTDLY<5:0>					
	15:0	—	—	RAS2RASSBNKDLY<5:0>						—	—	—	RAS2PCHRGDLY<4:0>				
DDR ODTCFG	31:16	—	—	—	—	—	—	—	—	—	ODTWLEN<2:0>			—	ODTRLEN<2:0>		
	15:0	ODTWDLY<3:0>				ODTRDLY<3:0>				ODTCSEN<7:0>							
DDR XFERCFG	31:16	BIGENDIAN	—	—	—	MAXBURST<3:0>				—	—	—	—	RDATENDLY<3:0>			
	15:0	—	—	—	—	—	—	—	—	NXTDATAVDLY<3:0>				NXTDATRQDLY<3:0>			
DDR CMDISSUE	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	VALID	NUMHOSTCMDS<3:0>			
DDR ODTENCFG	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODTWEN
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODTREN
DDR MEMWIDTH	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	HALFRATE	—	—	—

Table 55-1: DDRC Register Summary (Continued)

Register Name	Bit Range	Bits															
		31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
DDR CMD10	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD11	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD12	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD13	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD14	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD15	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD16	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD<27:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD17	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD18	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD19	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD110	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD111	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD112	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD113	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD114	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD<27:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD115	31:16	MDALCMD<7:0>								WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
	15:0	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7:0>								CLKENCMD1
DDR CMD20	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD21	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD22	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD23	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD24	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD25	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD26	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD27	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							

Table 55-1: DDRC Register Summary (Continued)

Register Name	Bit Range	Bits															
		31/15	30/14	29/13	28/12	27/11	26/10	25/9	24/8	23/7	22/6	21/5	20/4	19/3	18/2	17/1	16/0
DDR CMD28	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD29	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD210	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD211	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD212	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD213	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD214	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR CMD215	31:16	—	—	—	—	—	—	—	—	—	—	—	—	WAIT<8:5>			
	15:0	WAIT<4:0>					BNKADDRCMD<2:0>			MDADDRHCMD<7:0>							
DDR SCLSTART	31:16	—	—	—	SCLSTART	—	SCLEN	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLU BPASS	SCLL BPASS
DDR SCLLAT	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	DDRCLKDLY<3:0>				CAPCLKDLY<3:0>			
DDR SCLCFG0	31:16	—	—	—	—	—	—	—	ODTCSW	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	RCASLAT<3:0>				—	—	DDR	BURST8
DDR SCLCFG1	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	DBLREFDLY	WCASLAT<3:0>				—	—	—	—	—	—	—	SCLSEN
DDR PHYPADCON	31:16	—	PREAMBDLY<1:0>		RCVREN	—	—	—	—	DRVSTRPFET<3:0>				DRVSTRNFET<3:0>			
	15:0	—	HALFRATE	WR CMDDLY	—	—	—	NOEXTDLL	EOEN CLKCYC	ODTPUCAL<1:0>		ODTPDCAL<1:0>		ADDC DRVSEL	DATAD RVSEL	ODTEN	ODTSEL
DDR PHYDLLR	31:16	DLYSTVAL<3:0>				—	DISRECALIB	RECALIBCNT<17:8>									
	15:0	RECALIBCNT<7:0>								—	—	—	—	—	—	—	—
DDR PHYCLKDLY	31:16	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	15:0	—	—	—	—	—	—	—	—	—	—	SCLUB PASS	SCLLB PASS	—	CLKDLYDELTA<2:0>		

Register 55-1: DDRTSEL: DDR Target Select Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	TSEL<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **TSEL<7:0>:** Target Select bits

These bits select the target to program arbitration parameters and must be set before an arbitration parameter is programmed for a target. The value represents the target number (0-4) multiplied by the field size of the arbitration parameter.

Register 55-2: DDRMINLIM: DDR Minimum Burst Limit Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	—	—	—	MINLIMIT<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4-0 **MINLIMIT<4:0>:** Minimum Burst Limit bits

These bits determine the minimum number of DDR bursts (two cycles per burst) that a target must have uninterrupted access to without interference from another target.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the MINLIMIT field (5) before this register is used to program the minimum burst limit for that target.

Register 55-3: DDRRQPER: DDR Request Period Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RQPER<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **RQPER<7:0>:** Request Period bits

These bits, which are used in conjunction with the MINCMD<7:0> bits (DDRMINCMD<7:0>), determine the percentage of total bandwidth that is allocated to the target. If the number of DDR bursts specified by MINCMD<7:0> are not serviced for the target when it has been requesting access for (RQPER<7:0> * 4) number of clocks, the target's requests are treated with high priority until this condition becomes satisfied.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the RQPER field (8) before this register is used to program the minimum burst limit for that target.

Register 55-4: DDRMINCMD: DDR Minimum Command Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	MINCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-0 **MINCMD<7:0>:** Minimum Command bits

These bits, which are used in conjunction with the RQPER<7:0> bits (DDRRQPER<7:0>), determine the percentage of total bandwidth that is allocated to the target. If the number of DDR bursts specified by MINCMD<7:0> are not serviced for the target when it has been requesting access for (RQPER<7:0> * 4) number of clocks, then the target's requests are treated with high priority until this condition becomes satisfied.

Note: The TSEL<7:0> bits (DDRTSEL<7:0>) must be programmed with the target number multiplied by the size of the MINCMD field (8) before this register is used to program the minimum burst limit for that target.

Register 55-5: DDRMEMCON: DDR Memory Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	—	—	—	—	—	INITDN	STINIT

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-2 **Unimplemented:** Read as '0'

bit 1 **INITDN:** Memory Initialize Done bit

Set by software after memory initialization is completed to enable controller for regular operation.

1 = All commands have been issued; the controller is enabled for regular operation
0 = Controller is not enabled for regular operation

bit 0 **STINIT:** Memory Initialize Start bit

Set by software after the memory initialization commands are loaded into the DDRCMD registers to start memory initialization.

1 = Start memory initialization
0 = Do not start memory initialization

Register 55-6: DDRMEMCFG0: DDR Memory Configuration Register 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	APCHRGEN	—	CLHADDR<4:0>				
23:16	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CSADDR<4:0>				
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	BNKADDR<4:0>				
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RWADDR<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30 **APCHRGEN:** Automatic Precharge Enable bit

When set, this bit issues an Auto-precharge command to close the bank at the end of every user command. If the command accesses more than one bank before completing, all banks accessed are auto-precharged.

1 = Issue an auto-precharged command

0 = Do not issue an auto-precharged command

bit 29 **Unimplemented:** Read as '0'

bit 28-24 **CLHADDR<4:0>:** Column Address Shift bits

These bits specify how many bits the controller address must be right-shifted to put the high part of the column address to the immediate left of the low part of the column address. Used in conjunction with CLADDRHMSK (DDRMEMCFG2<26:0>) and CLADDRLMASK (DDRMEMCFG3<26:0>).

bit 23-21 **Unimplemented:** Read as '0'

bit 20-16 **CSADDR<4:0>:** Chip Select Shift bits

These bits specify which bits of user address space are used to derive the Chip Select address for the DDR memory. Used in conjunction with CSADDRMASK (DDRMEMCFG4<10:8>).

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **BNKADDR<4:0>:** Bank Address Select Shift bits

These bits specify which bits of user address space are used to derive the bank address for the DDR memory. Used in conjunction with BNKADDRMASK (DDRMEMCFG4<2:0>).

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RWADDR<4:0>:** Row Address Select Shift bits

These bits specify which bits of user address space are used to derive the row address for the DDR memory. Used in conjunction with RWADDRMSK (DDRMEMCFG1<12:0>).

Register 55-7: DDRMEMCFG1: DDR Memory Configuration Register 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RWADDRMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RWADDRMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **RWADDRMSK<12:0>:** Row Address Mask bits

These bits, which are used in conjunction with the RWADDR<4:0> bits (DDRMEMCFG0<4:0>), specify which bits of user address space are used to derive the row address for the DDR memory.

Register 55-8: DDRMEMCFG2: DDR Memory Configuration Register 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CLADDRHMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLADDRHMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **CLADDRHMSK<12:0>:** Column Address High Mask bits

These bits, which are used in conjunction with the CLADDR<4:0> bits (DDRMEMCFG0<28:24>) and the CLADDRLMASK<12:0> bits (DDRMEMCFG3<12:0>), specify which bits of user address space are used to derive the column address for the DDR memory.

Register 55-9: DDRMEMCFG3: DDR Memory Configuration Register 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	CLADDRLMSK<12:8>				
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CLADDRLMSK<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12-0 **CLADDRLMSK<12:0>:** Column Address Low Mask bits

These bits, which are used in conjunction with the CLADDR<4:0> bits (DDRMEMCFG0<28:24>) and the CLADDRHMASK<12:0> bits (DDRMEMCFG2<12:0>), specify which bits of user address space are used to derive the column address for the DDR memory.

Register 55-10: DDRMEMCFG4: DDR Memory Configuration Register 4

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	CSADDRMSK<2>
7:0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	CSADDRMSK<1:0>		—	—	—	BNKADDRMSK<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-9 **Unimplemented:** Read as '0'

bit 8-6 **CSADDRMSK<2:0>:** Chip Select Address Mask bits

These bits, which are used in conjunction with the CSADDR<4:0> bits (DDRMEMCFG0<20:16>), determine which bits of user address space are used to derive the Chip Select address for the DDR memory.

bit 5-3 **Unimplemented:** Read as '0'

bit 2-0 **BNKADDRMSK<2:0>:** Bank Address Mask bits

These bits, which are used in conjunction with the BNKADDR<4:0> bits (DDRMEMCFG0<12:8>), determine which bits of user address space are used to derive the bank address for the DDR memory.

Register 55-11: DDRREFCFG: DDR Refresh Configuration Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	—	MAXREFS<2:0>		
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFDLY<7:0>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFCNT<15:8>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	REFCNT<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-27 **Unimplemented:** Read as '0'

bit 26-24 **MAXREFS<2:0>:** Maximum Pending Refreshes bits

These bits specify the maximum number of refreshes that may be pending at any time. If there is any idle time when one or more refreshes are pending, the pending refreshes are issued continuously until a new request is received. If there is no idle time while MAXREFS <2:0> refreshes are pending, subsequent requests are stopped until at least one burst of pending refreshes can be issued.

bit 23-16 **REFDLY<7:0>:** Minimum Refresh-to-Refresh Delay bits

These bits specify the minimum number of clocks required between refreshes.

bit 15-0 **REFCNT<15:0>:** Refresh Count bits

These bits specify the number of clock cycles corresponding to the average periodic refresh interval.

Register 55-12: DDRPWRCFG: DDR Power Configuration Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	PCHRGPWRDN	SLFREFDLY<9:4>					
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFDLY<3:0>				PWDNDLY<7:4>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
	PWDNDLY<3:0>				ASLFREFEN	APWRDNEN	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22 **PCHRGPWRDN:** Precharge Power-Down Only bit

Allow automatic entry into Precharge Power-Down mode but not into active Power-Down mode. If any rows are open they will be Precharged before DDR SDRAM is put into Precharge Power-Down mode.
1 = Allow automatic entry into Precharge Power-Down mode.
0 = Do not allow automatic entry into Precharge Power-Down mode.

bit 21-12 **SLFREFDLY<9:0>:** Self-Refresh Delay bits

Specifies the minimum number of clock cycles of idle time the controller needs to wait before automatic entry into Self-Refresh mode. Value represents number of clocks multiplied by 1024.
111111111 = 2,111,452 clocks
•
•
•
000000001 = 1,024 clocks

bit 11-4 **PWDNDLY<7:0>:** Refresh Count bits

Specifies the minimum number of clock cycles of idle time the controller needs to wait before automatic entry into Power-Down mode (Active or Precharge). Value represents number of clocks multiplied by 4.
11111111 = 1,020 clocks
•
•
•
00000001 = 4 clocks

bit 3 **ASLFREFEN:** Automatic Self-Refresh Enable bit

1 = Allow automatic entry into Self-Refresh mode.
0 = Do not allow automatic entry into Self-Refresh mode.

bit 2 **APWRDNEN:** Automatic Power-Down Enable bit

1 = Allow automatic entry into Power-Down mode.
0 = Do not allow automatic entry into Power-Down mode.

bit 1-0 **Unimplemented:** Read as '0'

Register 55-13: DDRDLYCFG0: DDR Delay Configuration Register 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RMWDLY<3:0>				R2WDLY<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2WCSDLY<3:0>				W2WDLY<3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	R2RCSDLY<3:0>				R2RDLY<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2RCSDLY<3:0>				W2RDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **RMWDLY<3:0>:** Read-Modify-Write Delay bits

These bits specify the minimum number of clocks required between the Read and Write command issued for a read-modify-write operation.

bit 27-24 **R2WDLY<3:0>:** Read-to-Write Delay bits

These bits specify the minimum number of clocks required between a Read command and Write command. Commands may be to the same or different Chip Selects.

bit 23-20 **W2WCSDLY<3:0>:** Write-to-Write Chip Select Delay bits

These bits specify the minimum number of clocks required between two Write command to different Chip Selects.

bit 19-16 **W2WDLY<3:0>:** Write-to-Write Delay bits

These bits specify the minimum number of clocks required between two Write command to the same Chip Select.

bit 15-12 **R2RCSDLY<3:0>:** Read-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between two Read commands to different Chip Selects.

bit 11-8 **R2RDLY<3:0>:** Read-to-Read Delay bits

These bits specify the minimum number of clocks required between two Read commands to the same Chip Select.

bit 7-4 **W2RCSDLY<3:0>:** Write-to-Read Chip Select Delay bits

These bits specify the minimum number of clocks required between a Write command and a Read command to different Chip Selects.

bit 3-0 **W2RDLY<3:0>:** Write-to-Read Delay bits

These bits specify the minimum number of clocks required between a Write command and a Read command to the same Chip Select.

Register 55-14: DDRDLYCFG1: DDR Delay Configuration Register 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	SLFREF EXDLY<8>	NXTDAT AVDLY<4>	W2RCS DLY<4>	W2RDLY<4>	W2PCHRG DLY<4>	PWRDNEXDLY<5:4>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	PWRDNEXDLY<3:0>				PWRDNMINDLY <3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFEXDLY<7:0>							
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	SLFREFMINDLY<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30 **SLFREFEXDLY:** Self-Refresh Exit Delay bit 8

This bit specifies the minimum number of clocks required before normal operation after exiting Self-Refresh mode.

bit 29 **NXTDATAVDLY:** Next Data Available Delay bit 4

These bits specify the minimum number of clock cycles required between a Write command and the write data transfer handshake signal "next data request". Also, see the NXTDATAVDLY<3:0> bits (DDRXFERCFG<7:4>) in Register 55-18.

bit 28 **W2RCSDLY:** Write-to-Read Chip Select Delay bit 4

This bit specify the minimum number of clocks required between a Write command and a Read command to different Chip Selects. Also, see the W2RCSDLY<3:0> bits (DDRDLYCFG0<7:4>) in Register 55-13.

bit 27 **W2RDLY:** Write-to-Read Delay bit 4

This bit specifies the minimum number of clocks required between a Write command and a Read command to the same Chip Select. Also, see the W2RDLY<3:0> bits (DDRDLYCFG0<3:0>) in Register 55-13.

bit 26 **W2PCHRGDLY:** Write to Precharge Delay bit 4

These bits specify the minimum number of clocks required from a Write command to a Precharge command to the same bank as the write. Also, see WPCHRGDLY<3:0> bits (DDRDLYCFG2<15:12>) Register 55-15.

bit 25-20 **PWRDNEXDLY<5:0>:** Power-Down Exit Delay bits

These bits specify the minimum number of clocks required before normal operation after exiting Power-Down mode.

bit 19-16 **PWRDNMINDLY<3:0>:** Power-Down Minimum Delay bits

These bits specify the minimum number of clocks to stay in Power-Down mode after entering it.

bit 15-8 **SLFREFEXDLY<7:0>:** Self-Refresh Exit Delay bits

These bits specify the minimum number of clocks required before normal operation after exiting Self-Refresh mode.

bit 7-0 **SLFREFMINDLY<7:0>:** Self-Refresh Minimum Delay bits

These bits specify the minimum number of clocks to stay in Self-Refresh mode after entering it.

Register 55-15: DDRDLYCFG2: DDR Delay Configuration Register 2

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RBENDDLY<3:0>				PCHRG2RASDLY<3:0>			
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RAS2CASDLY<3:0>				RAS2RASDLY <3:0>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	W2PCHRGDLY<3:0>				R2PCHRGDLY<3:0>			
7:0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	PCHRGALLDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **RBENDDLY<3:0>:** Read Burst End Delay bits

These bits specify the minimum number of clocks required from issue of a Read command to the read data burst completion.

bit 27-24 **PCHRG2RASDLY<3:0>:** Precharge-to-RAS Delay bits

These bits specify the minimum number of clocks required from a Precharge command to a RAS command to the same bank.

bit 23-20 **RAS2CASDLY<3:0>:** RAS-to-CAS Delay bits

These bits specify the minimum number of clocks required from a RAS command to a CAS command to the same bank.

bit 19-16 **RAS2RASDLY<3:0>:** RAS-to-RAS Delay bits

These bits specify the minimum number of clocks required from a RAS command to a RAS command to a different bank on the same Chip Select.

bit 15-12 **W2PCHRGDLY<3:0>:** Write-to-Precharge Delay bits 3-0

These bits specify the minimum number of clocks required from a Write command to a Precharge command to the same bank as the write.

An overflow bit (DDRDLYCFG1<26>) is provided for delays greater than 15 clock cycles.

bit 11-8 **R2PCHRGDLY<3:0>:** Read-to-Precharge Delay bits

These bits specify the minimum number of clocks required from a Read command to a Precharge command to the same bank as the read.

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **PCHRGALLDLY<3:0>:** Precharge All Delay bits

These bits specify the minimum number of clocks required from a Precharge all banks command to an Activate or Refresh command.

Register 55-16: DDRDLYCFG3: DDR Delay Configuration Register 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	FAWTDLY<5:0>					
15:8	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	RAS2RASSBNKDLY<5:0>					
7:0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	RAS2PCHRGDLY<4:0>				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-22 **Unimplemented:** Read as '0'

bit 21-16 **FAWTDLY<5:0>:** Four Activate Window Time Delay bits
These bits specify the minimum number of clocks within which only four banks may be opened.

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RAS2RASSBNKDLY<5:0>:** RAS-to-RAS Same Bank Delay bits
These bits specify the minimum number of clocks required between RAS commands to the same bank.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RAS2PCHRGDLY<4:0>:** RAS-to-Precharge Delay bits
These bits specify the minimum number of clocks required from a RAS command to a Precharge command to the same bank.

Register 55-17: DDRODTCFG: DDR On-Die Termination Configuration Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	ODTWLEN<2:0>			—	ODTRLEN<2:0>		
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ODTWDLY<3:0>				ODTRDLY<3:0>			
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	ODTCSEN<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-23 **Unimplemented:** Read as '0'

bit 22-20 **ODTWLEN<2:0>:** On-Die Termination Write Length bits
These bits specify the number of clocks ODT is turned on for writes.

bit 19 **Unimplemented:** Read as '0'

bit 18-16 **ODTRLEN<2:0>:** On-Die Termination Read Length bits
These bits specify the number of clocks ODT is turned on for reads.

bit 15-12 **ODTWDLY<3:0>:** On-Die Termination Write Delay bits
These bits specify the number of clocks after a Write command before turning on ODT to the DDR.

bit 11-8 **ODTRDLY<3:0>:** On-Die Termination Read Delay bits
These bits specify the number of clocks after a Read command before turning on ODT to the DDR.

bit 7-0 **ODTCSEN<7:0>:** On-Die Termination Chip Select Enable bits
These bits are used with the DDRODTENCFG register (Register 55-20) to program the ODT control for each Chip Select. The value in this field represents the number of Chip Selects multiplied by the Chip Select number to be programmed.

Register 55-18: DDRXFERCFG: DDR Transfer Configuration Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0
	BIGENDIAN	—	—	—	MAXBURST<3:0>			
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	RDATENDLY<3:0>			
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	NXTDATAVDLY<3:0>				NXTDATRQDLY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **BIGENDIAN:** Big Endian bit

1 = Data is big-endian format
0 = Data is little-endian format

bit 30-28 **Unimplemented:** Read as '0'

bit 27-24 **MAXBURST<3:0>:** Maximum Command Burst Count bits

These bits specify the maximum number of commands that can be written to the DDR Controller in Burst mode.

bit 23-20 **Unimplemented:** Read as '0'

bit 19-16 **RDATENDLY<3:0>:** PHY Read Data Enable Delay bits

These bits specify the minimum number of clocks required between issuing a Read command to the PHY and when the "read data enable" signal to the PHY is asserted.

bit 15-8 **Unimplemented:** Read as '0'

bit 7-4 **NXTDATAVDLY<3:0>:** Next Data Available Delay bits

These bits specify the minimum number of clock cycles required between issuing a Read command and the read data being received.

bit 3-0 **NXTDATRQDLY<3:0>:** Next Data Request Delay bits

These bits specify the minimum number of clock cycles required between issuing a Write command and the write data transfer handshake signal "next data request".

Register 55-19: DDRCMDISSUE: DDR Command Issue Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R/W-0, HC	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	VALID	NUMHOSTCMDS<3:0>			

Legend:	HC = Cleared by hardware		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-5 **Unimplemented:** Read as '0'

bit 4 **VALID:** Host Command Valid bit

When written with a '1', this bit indicates to the controller that the data in the host command registers are valid, and should be transmitted to the SDRAM. This bit is cleared by hardware when all data has been transmitted.

bit 3-0 **NUMHOSTCMDS<3:0>:** Number of Host Commands bits

The number of host commands to be transmitted to the SDRAM.

Register 55-20: DDRODTENCFG: DDR On-Die Termination Enable Configuration Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ODTWEN
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
	—	—	—	—	—	—	—	ODTREN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-17 **Unimplemented:** Read as '0'

bit 16 **ODTWEN:** On-Die Termination Write Enable bit

1 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) in Register 55-17 has ODT enabled for data reads

0 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT disabled for data reads

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **ODTREN:** On-Die Termination Read Enable bit

1 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT enabled for data writes

0 = The Chip Select represented by the OTDCSEN<7:0> bits (DDRODTCFG<7:0>) has ODT disabled for data writes

Register 55-21: DDRMEMWIDTH: DDR Memory Width Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	—	—	—	—	HALFRATE	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-4 **Unimplemented:** Read as '0'

bit 3 **HALFRATE:** Half-rate Mode bit

The PIC32 device always operates in Half-rate mode. This bit must be set during initialization.

1 = Half-rate mode

0 = Full-rate mode

bit 2-0 **Unimplemented:** Read as '0'

Register 55-22: DDRCMD1x: DDR Host Command 1 Register 'x' ('x' = 0 through 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MDALCMD<7:0>							
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WENCMD2	CASCMD2	RASCMD2	CSCMD2<7:3>				
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSCMD2<2:0>			CLKENCMD2	WENCMD1	CASCMD1	RASCMD1	CSCMD1<7>
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CSCMD1<6:0>							CLKENCMD1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-24 **MDALCMD<7:0>:** Mode Address Low Command bits
These bits specify the value to be driven on the SDRAM address bits 7 through 0 when issuing the command.

bit 23 **WENCMD2:** Write Enable Command 2 bit
This bit specifies the value to be driven on WE_N on the second and subsequent cycles of issuing the command.

bit 22 **CASCMD2:** Column Address Strobe Command 2 bit
This bit specifies the value to be driven on CAS_N on the second and subsequent cycles of issuing the command

bit 21 **RASCMD2:** Row Address Strobe Command 2 bit
This bit specifies the value to be driven on RAS_N on the second and subsequent cycles of issuing the command.

bit 20-13 **CSCMD2<7:0>:** Chip Select Command 2 bits
These bits specify the value to be driven on the CS_N signals (maximum of 8) on the second and subsequent cycles of issuing the command.

bit 12 **CLKENCMD2:** Clock Enable Command 2 bit
This bit specifies the value to be driven on CKE on the second and subsequent cycles of issuing the command.

bit 11 **WENCMD1:** Write Enable Command 1 bit
This bit specifies the value to be driven on the WE_N on the first cycle of issuing the command.

bit 10 **CASCMD1:** Column Address Strobe Command 1 bit
This bit specifies the value to be driven on the CAS_N on the first cycle of issuing the command.

bit 9 **RASCMD1:** Row Address Strobe Command 1 bit
This bit specifies the value to be driven on the RAS_N on the first cycle of issuing the command.

bit 8-1 **CSCMD1<7:0>:** Chip Select Command 1 bit
These bits specify the value to be driven on the CS_N signals (maximum of 8) on the first cycle of issuing the command.

bit 0 **CLKENCMD1:** Clock Enable Command 1 bit
This bit specifies the value to be driven on CKE on the first cycle of issuing the command.

Register 55-23: DDRCMD2*x*: DDR Host Command 2 Register 'x' ('x' = 0 through 15)

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	—	—	WAIT<8:5>			
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	WAIT<4:0>					BNKADDRCMD<2:0>		
7:0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	MDADDRHCMD<7:0>							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-20 **Unimplemented:** Read as '0'

bit 19-11 **WAIT<8:0>:** Wait Command bits

These bits specify the number of clock cycles to wait after issuing a command before issuing the next command.

bit 10-8 **BNKADDRCMD<2:0>:** Bank Address Command bit

These bits specify the value to be driven on the bank address bits when issuing the command.

bit 7-0 **MDADDRHCMD<7:0>:** Mode Address High Command bits

These bits specify the value to be driven on the SDRAM address bits 15 through 8 when issuing the command.

Register 55-24: DDRSCLSTART: DDL Self-Calibration Logic Start Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	R/W-0	U-0	R/W-0	U-0	U-0
	—	—	—	SCLSTART(1)	—	SCLEN	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	R-0	R-0
	—	—	—	—	—	—	SCLUBPASS	SCLLBPASS

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-29 **Unimplemented:** Read as '0'

bit 28 **SCLSTART:** Start Self-Calibration Logic bit(1)
- 1 = Start self-calibration
- 0 = Do not start self-calibration

bit 27 **Unimplemented:** Read as '0'

bit 26 **SCLEN:** Start Self-Calibration Logic Enable bit
- 1 = Enable dynamic self-calibration logic
- 0 = Disable dynamic self-calibration logic

bit 25-2 **Unimplemented:** Read as '0'

bit 1 **SCLUBPASS:** Self-Calibration Logic Upper Data Byte Status bit
- 1 = Self-calibration logic for upper data byte has passed
- 0 = Self-calibration logic for upper date byte has failed

bit 0 **SCLLBPASS:** Self-Calibration Logic Lower Data Byte Status bit
- 1 = Self-calibration logic for lower data byte has passed
- 0 = Self-calibration logic for lower date byte has failed

Note 1: This bit is set by hardware when the SCL process is complete.

Register 55-25: DDRSCLLAT: DDL Self-Calibration Logic Latency Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
	DDRCLKDY<3:0>				CAPCLKDY<3:0>			

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-8 **Unimplemented:** Read as '0'

bit 7-4 **DDRCLKDLY<3:0>:** DDR Clock Delay bits
The recommended value is 4.

bit 3-0 **CAPCLKDLY<3:0>:** Capture Clock Delay bits
The recommended value is 3.

Register 55-26: DDRSCLCFG0: DDR SCL Configuration Register 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	—	—	—	—	—	—	—	ODTCSW
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	R/W-1	R/W-0	R/W-1	R/W-1	U-0	U-0	R/W-0	R/W-1
	RCASLAT<3:0>				—	—	DDR	BURST8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-25 **Unimplemented:** Read as '0'

bit 24 **ODTCSW:** On-Die Termination Chip Select Write bit
1 = ODT is turned on to the DRAM on CS0 during writes performed by the SCL
0 = ODT is turned off to the DRAM on CS0 during writes performed by the SCL.

bit 23-8 **Unimplemented:** Read as '0'

bit 7-4 **RCASLAT<3:0>:** Read CAS Latency bits
DRAM read CAS latency in clock cycles.

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **DDR:** DDR bit
1 = DDR is connected
0 = DDR is not connected

bit 0 **BURST8:** PHY Burst 8 bit
1 = DRAM is in Burst 8 mode while running a SCL test
0 = DRAM is in Burst 4 mode while running a SCL test. This bit should always be set for devices operating in Half-rate mode.

Register 55-27: DDRSCLCFG1: DDR SCL Configuration Register 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
	—	—	—	DBLREFDLY	WCASLAT<3:0>			
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-1
	—	—	—	—	—	—	—	SCLCSEN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-13 **Unimplemented:** Read as '0'

bit 12 **DBLREFDLY:** Double Reference Delay bit

Determines whether the PHY will delay a SCL operation following an acknowledge by one or two time intervals. The time interval is a function of the hardware design.

1 = SCL operation delay is doubled
0 = SCL operation delay is not doubled

bit 11-8 **WCASLAT<3:0>:** Write CAS Latency bits

DRAM write CAS latency in clock cycles.

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SCLCSEN:** SCL Chip Select Enable bit

1 = Run SCL on Chip Select 0
0 = Do not run SCL on Chip Select 0

Register 55-28: DDRPHYPADCON: DDR PHY Pad Control Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	R/W-1	R/W-0	R/W-1	U-0	U-0	U-0	U-0
	—	PREAMBDLY<1:0>		RCVREN	—	—	—	—
23:16	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
	DRVSTRPFET<3:0>				DRVSTRNFET<3:0>			
15:8	U-0	R/W-1	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
	—	HALFRATE	WR CMDDLY	—	—	—	NOEXTDLL	EOEN CLKCYC
7:0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
	ODTPUCAL<1:0>		ODTPDCAL<1:0>		ADDC DRVSEL	DAT DRVSEL	ODTEN	ODTSEL

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Unimplemented:** Read as '0'

bit 30-29 **PREAMBDLY<1:0>:** Preamble Delay bits

Controls the length of the preamble for writes.

11 = Reserved
10 = 1 cycle preamble
01 = 1.5 cycle preamble
00 = 2 cycle preamble

bit 28 **RCVREN:** Receiver Enable bit

1 = Pad receivers on bidirectional I/Os are turned ON
0 = Pad receivers on bidirectional I/Os are turned OFF

bit 27-24 **Unimplemented:** Read as '0'

bit 23-20 **DRVSTRPFET<3:0>:** PFET Drive Strength bits

Pad PFET driver output impedance adjustment control
1111 = Maximum drive strength
•
•
•
0000 = Minimum drive strength.

bit 19-16 **DRVSTRNFET<3:0>:** NFET Drive Strength bits

Pad NFET driver output impedance adjustment control
1111 = Maximum drive strength
•
•
•
0000 = Minimum drive strength.

bit 15 **Unimplemented:** Read as '0'

bit 14 **HALFRATE:** Half Rate bit

1 = Controller clock is running at half rate with respect to PHY
0 = Controller clock is running at full rate with respect to PHY

bit 13 **WRCMDDLY:** Write Command Delay bit

This bit should be set to '1' if write latency (WL) is an even number.

1 = Write command delay
0 = No Write command delay

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **NOEXTDLL:** No External DLL bit

1 = Use internal digital DLL.
0 = Use external DLL.

Register 55-28: DDRPHYPADCON: DDR PHY Pad Control Register (Continued)

bit 8 **EOENCLKCYC:** Extra Output Enable bit
1 = Drive pad output enabled for an extra clock cycle after a write burst
0 = Drive pad output is not enabled for an extra clock cycle after a write burst

bit 7-6 **ODTPUCAL<1:0>:** On-Die Termination Pull-up Calibration bits
11 = Maximum ODT impedance
•
•
•
00 = Minimum ODT impedance

bit 5-4 **ODTPDCAL<1:0>:** On-Die Termination Pull-down Calibration bits
11 = Maximum ODT impedance
•
•
•
00 = Minimum ODT impedance

bit 3 **ADDCDRVSEL:** Address and Control Pads Drive Strength Select bit
1 = Full Drive Strength
0 = 60% Drive Strength

bit 2 **DATDRVSEL:** Data Pads Drive Strength Select bit
1 = Full Drive Strength
0 = 60% Drive Strength

bit 1 **ODTEN:** On-Die Termination Enable bit
1 = ODT Enabled
0 = ODT Disabled

bit 0 **ODTSEL:** On-Die Termination Select bit
1 = 150 ohm On-Die Termination
0 = 75 ohm On-Die Termination

Register 55-29: DDRPHYDLLR: DDR PHY DLL Recalibrate Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-1	R/W-0	R/W-0
	DLYSTVAL<3:0>				—	DISRECALIB	RECALIBCNT<17:16>	
23:16	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RECALIBCNT<15:8>							
15:8	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	RECALIBCNT<7:0>							
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-28 **DLYSTVAL<3:0>:** Delay Start Value bits
The start value of the digital DLL master delay line. The recommended value is '0011'.

bit 27 **Unimplemented:** Read as '0'

bit 26 **DISRECALIB:** Disable Recalibration bit
1 = Do not recalibrate the digital DLL after the first time
0 = Recalibrate the digital DLL in accordance with the value of the RECALIBCNT<17:0> bits

bit 25-8 **RECALIBCNT<17:0>:** Recalibration Count bits
Determines the period of recalibration of the digital DLL in units of (256 * PHY clock cycles).

bit 7-0 **Unimplemented:** Read as '0'

Register 55-30: DDRPHYCLKDLY: DDR PHY Clock Delta Delay Register

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
	—	—	SCLUBPASS(1)	SCLLBPASS(1)	—	CLKDLYDELTA<2:0>		

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-6 **Unimplemented:** Read as '0'

bit 5 **SCLUBPASS:** Self-calibration Logic Upper Data Byte Status bit(1)
1 = Self-calibration logic for upper data byte is passed
0 = Self-calibration logic for upper data byte is failed

bit 4 **SCLLBPASS:** Self-calibration Logic Lower Data Byte Status bit(1)
1 = Self-calibration logic for lower data byte is passed
0 = Self-calibration logic for lower data byte is failed

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **CLKDLYDELTA<2:0>:** DDR Clock Delay Delta bits
These bits indicate the SCL latency setting programmed per byte lane. These bits are automatically programmed by SCL logic and can also be programmed by the user. This bit is specifically useful in case of SCL retires.
111 = 7 DDR clocks
110 = 6 DDR clocks
•
•
•
000 = 6 DDR clocks

Note 1: These bits indicate the same status as the SCLLBPASS (DDRSCLSTART<0>) and SCUBPASS (DDRSCLSTART<0>) bits.

55.3 MODES OF OPERATION

The Dual Data Rate (DDR) Controller and Physical Interface (PHY) implement the necessary controls for an external memory bus interface using DDR SDRAM.

The DDR Controller operates in Half-rate mode, providing internal 32-bit wide buffered data in its read queue when connected to 16-bit SDRAM devices. Half-rate mode means that the clock between the controller and the PHY is half the rate of the clock between the PHY and the SDRAM.

DDR Controller and PHY features:

- Controller: Compatible with the DDR PHY Interface (DFI) Version 2.1 Specification
- PHY: Compatible with the DFI Version 3.0 Specification
- Self-Calibration Logic (SCL)
- Half-rate mode operation
- 16-bit memory interface, 32-bit bus interface
- Programmable On-Die Termination (ODT)
- Self-Refresh

The DDR Controller is organized in the form of target interfaces that handle transactions to and from the system bus. The target interfaces share access to the memory controller through an arbiter. The arbitration parameters for each target can be programmed separately (see **Figure 55-1: "DDR SDRAM Controller Block Diagram"**).

55.3.1 Arbiter Configuration

The arbiter shares access to the memory controller across all targets. Each command from a target to the arbiter is for one SDRAM burst. Target bandwidth allocation and the number of consecutive bursts from a target are controlled by the programmed arbitration parameters for each target.

The arbitration parameters are controlled by the registers listed in Table 55-2:

Table 55-2: Arbiter Configuration Registers

Register	See...	Function
DDRTSEL	Register 55-1	Target for which the arbitration parameter is to be programmed
DDRMINLIM	Register 55-2	Minimum number of DDR (2-cycle) consecutive bursts for that target
DDRREQPER	Register 55-3	Time-out before raising priority of target if MINCMD bursts have not been serviced
DDRMINCMD	Register 55-4	Number of target bursts not serviced by arbiter within (REQPER * 4) clocks needed to raise target priority

To program an arbitration parameter for a target, the TSEL <7:0> bits (DDRTSEL<7:0>) must first be programmed with the target number multiplied by the size of the field being programmed. For example, the size of the MINLIM field (DDRMINLIM<4:0>) is five; therefore, to program MINLIM for Target 0, TSEL should be programmed to 0; for Target 1, TSEL should be programmed to 5; for Target 2, TSEL should be programmed to 10, and so on.

The unit of each data transfer is one burst. For controller initialization, the burst length can be specified in bytes or cycles. The burst length is fixed, depending on the mode (Full or Half) of the controller. In Half-rate mode, the burst length is always eight. The size in bytes of each burst is the SDRAM data path width times the burst length. For the PIC32 device, the burst size in bytes is 16, and the burst length in cycles is two. These values are used during controller initialization:

- Burst length = 8
- BS (burst size in bytes) = 16
- BL (burst length in cycles) = 2

The MINLIM value controls the number of consecutive bursts for a target that will be transferred before switching to another target. For example, to guarantee 64-byte continuous accesses for a target, MINLIM value for that target should be programmed to 4.

The arbiter attempts to optimize bandwidth utilization by giving high priority to open row accesses and by rotating accesses across banks. These optimization considerations are applied when more than one target is requesting data transfer at a time and none of the targets must be given higher priority than others because of a request period timeout. A request period timeout occurs when a target has requested access for longer than the number of clocks defined by REQPER and MINCMD. If the target has been requesting access for (REQPER * 4) clocks and MINCMD bursts have not been serviced for that target, then that target's requests are treated with high priority until those conditions are satisfied.

The user can use the arbitration parameters to tune performance based on the amount of data needed to be transferred by each target. General formulas for calculating the arbitration parameters:

- MINCMD = BT / (BS * EF)
- REQPER = (CT/4) * (DDR_controller_clk_freq / (cpu_clk_freq * EF))
- BT = bytes needing to be transferred
- BS = burst size in bytes of each DDR read or write burst
- CT = Target clock cycles in which BT bytes need to be transferred
- EF = efficiency factor ($\geq$ 1)

For example, a target must transfer 2000 bytes in 1000 target clock cycles, the DDR burst size is 16 bytes, the DDR Controller clock frequency is 200 MHZ, and the target clock frequency is 200 MHz. Using an efficiency factor of 1.5:

- MINCMD = 2000 / (16 * 1.5), which is approximately 83
- REQPER = (1000/4) * (200/(200 * 1.5)), which is approximately 167

The efficiency factor can be the same for the two values or they may differ. Adjustment can be made to the efficiency factors until the desired performance is achieved.

55.4 DDR CONTROLLER CONFIGURATION AND TIMING

The DDR controller has registers to configure the controller, control the timing between commands issued to the SDRAM, and control the timing of data transfers. The register values are determined by the clock speed and the characteristics of the SDRAM.

55.4.1 Address Configuration

To the user, the address space of the SDRAM is one contiguous, byte-accessible block of memory. Internally, the SDRAM controller accesses the SDRAM in terms of Chip Selects, columns, rows, and banks.

Note:	The least significant address bit of the controller is dependent on the width of the SDRAM. For example, if the SDRAM is 16 bits wide, the LSB of the memory controller is bit 1 of the user address, as calculated in the following formula: controller_address = user_address/(sdram_data_width in bytes).

The translation between user address space and SDRAM accesses is controlled by the Memory Configuration registers. The controller address can be organized by any sequence of the four fields. For example, the address may be specified as:

- {CS, ROW, BA, COL}
- {ROW, CS, BA, COL}, etc.,

where,

- CS = Chip Select bits
- BA = Bank address bits
- ROW = Row address bits
- COL= Column address bits

The column address may be split into two fields, COL_ADDR_HI and COL_ADDR_LO, where COL_ADDR_HI are the MSBs of the column address and COL_ADDR_LO are the LSBs of the column address.

Splitting the column address into two fields may be useful if the user wants to place the bank address and/or the Chip Select address bits in the middle of the column address bits. This may help performance in a system where data accesses are random and it is helpful to increase the probability that consecutive commands go to different banks.

The controller address is formed by programming the address shift and mask of each field into the memory configuration registers. The position is derived from the number of bits of each field and the sequence of the fields that make up the address. The mask is used to mask off the bits not corresponding to the related field.

The number of Chip Selects is a function of the design of the controller, and can be obtained from the specific PIC32 device data sheet. The memory controller recognizes that banks on different Chip Selects are different, and therefore, combines the Chip Select address and bank address into one effective field. There are no Chip Select address bits if there is only one Chip Select in the system.

The size of BA, ROW, and COL must be obtained from the data sheet of the DRAM in use.

To program the memory configuration address shift and mask bits correctly, the address organization and DRAM geometry must be known. Example 55-1 uses a controller with one Chip Select and the Winbond W972516KG DDR SDRAM.

Example 55-1: Memory Configuration Setup

Function	Value	Units
CS	1	bit
BA	2	bits
ROW	13	bits
COL	9	bits
sdram_data_width	2	bytes

Address organization = {CS, ROW, BA, COL}

The column address field is the least significant field in the sequence. It is specified by programming the upper address right-shift, and a mask for both the upper and lower portions of the address. The upper address right-shift specifies how many bits the controller address should be right-shifted to put the high part of the column address in position to the immediate left of the low part of the column address. The masks specify the number of bits in each part of the address.

column address = ((controller address >>COLHADDR) & (COLADDRHMASK)) | (controller address & COLADDRLMASK)

For this example, the column address is not split, therefore COLHADDR is 0. The entire address is contained in the low field, and the mask is the number of bits in the entire address.

CLHADDR (DDRMEMCFG0<28:24>) = 0x00

CLADDRLMASK (DDRMEMCFG3<12:0>) = 0x1FF

CLADDRHMASK (DDRMEMCFG2<12:0>) = 0x00

In this example, the bank address is shifted by the number of bits in the column address, to bring the bank address to the right most bit position. The mask corresponds to the number of bits in the bank address.

BNKADDR (DDRMEMCFG0<12:8>) = 0x09

BNKADDRMASK (DDRMEMCFG4<2:0>) = 0x03

The row address field must be shifted by the sum of the number of bits in the column and bank addresses. The mask corresponds to the number of bits in the row address.

RWADDR (DDRMEMCFG0<4:0>) = 0x0B

RWADDRMSK (DDRMEMCFG1<12:0>) = 0x1FFF

The Chip Select address field is shifted by the sum of the previous fields (COL, BA, ROW). Because this device has only one Chip Select, the address mask is zero.

CSADDR (DDRMEMCFG0<19:16>) = 0x18

CSADDRMASK (DDRMEMCFG4<8:6>) = 0x00

55.4.2 Timing Configuration

To operate reliably, SDRAM requires time delays between various events. Those delays are programmed into the controller as part of the initialization process. Minimum delay times are specified by the SDRAM manufacturer, and are included in the data sheet for the SDRAM device. Delay times are specified in units of time, but because the SDRAM controller clock speed may vary between implementations, the delays are programmed in units of clock pulses.

SDRAM delay parameters are standardized across controllers and devices. Table 55-3 lists the SDRAM parameters required to calculate delay configuration register values for the DDR Controller. The formulas used to convert SDRAM parameters into register values are provided in Table 55-4.

Note:	All fractional results are rounded up to the nearest number of clocks.

Table 55-3: SDRAM Timing Parameters

Parameter	Description	Units
tRFC	Auto-refresh Cycle Time	ns
tWR	Write Recovery Time	ns
tRP	Precharge-to-Active Command Delay Time	ns
tRCD	Active-to-Read/Write Command Delay Time	ns
tRRD	Row-to-Row (RAS to RAS) Command Delay Time	ns
tWTR	Write-to-Read Command Delay Time	ns
tRTP	Read-to-Precharge Command Delay Time	ns
tDLLK	DLL Lock Delay Time	nClk
tRAS	Active-to-Precharge Minimum Command Delay Time	ns
tRC	Row Cycle Time	ns
tFAW	Four Bank Activation Window	ns
tMRD	Mode Register Set Command Cycle Delay	nClk
tXP	Power-Down Exit Delay	nClk
tCKE	Power-Down Minimum Delay	nClk
tCKESR	Self-Refresh Minimum Delay	nClk
RL	CAS Latency	nClk
tRFI	Average Periodic Refresh Interval	µs
WL	Write Latency	nClk
BL	Burst Length (in cycles)	nClk

Legend: nClk = Number of clocks

Table 55-4: DRAM Controller Timing

Delay Configuration Register Bits	Description	Formula	Units
REFDLY (DDRREFCFG<23:16>)	Minimum Refresh-to-Refresh Delay	tRFC/CTL_CLK_PER - 1	nClk
W2PCHRGDLY<3:0> (DDRDLYCFG2<15:12>) W2PCHRGDLY<4> (DDRDLYCFG1<26>)	Write Recovery Time	(tWR/CTL_CLK_PER) + WL + BL	nClk
PCHRGALLDLY (DDRDLYCFG2<3:0>)	Precharge-to-Active Command Delay Time	tRP/CTL_CLK_PER	nClk
PCHRG2RASDLY (DDRDLYCFG2<27:24>)	Precharge-to-Active Command Delay Time	(tRP/CTL_CLK_PER) - 1	nClk
RAS2CASDLY (DDRDLYCFG2<23:20>)	Active-to-Read/Write Command Delay Time	(tRCD/CTL_CLK_PER) - 1	nClk
RAS2RASDLY (DDRDLYCFG2<19:16>)	Row-to-Row (RAS to RAS) Command Delay Time	((tRRD/CTL_CLK_PER) – 1)	nClk
W2RDLY<3:0> (DDRDLYCFG0<3:0>) W2RDLY<4> (DDRDLYCFG1<27>)	Write-to-Read Command Delay Time	(tWTR/CTL_CLK_PER) + WL + BL	nClk
W2RCSDLY<3:0> (DDRDLYCFG0<7:4>) W2RCSDLY<4> (DDRDLYCFG1<28>)	Write-to-Read Chip Select Command Delay Time	(W2RDLY -1) or 3, whichever is greater	nClk
R2PCHRGDLY (DDRDLYCFG2<11:8>)	Read-to-Precharge Command Delay Time	(tRTP/CTL_CLK_PER) + BL - 2	nClk
SLFREFEXDLY<7:0> (DDRDLYCFG1<15:8>) SLFREFEXDLY<8> (DDRDLYCFG1<30>)	DLL Lock Delay Time	tDLLK/2 - 2	nClk
RAS2PCHRGDLY (DDRDLYCFG3<3:0>)	Active-to-Precharge Minimum Command Delay Time	(tRAS/CTL_CLK_PER) - 1	nClk
RAS2RASSBNKDLY (DDRDLYCFG3<13:8>)	Row Cycle Time	(tRC/CTL_CLK_PER) - 1	nClk
FAWTDLY (DDRDLYCFG3<21:16>)	Four Bank Activation Window	(tFAW/CTL_CLK_PER) - 1	nClk
DDRCMD2x<19:11>	Mode Register Set Command Cycle Delay	tMRD * CLK_PER	nClk
PWRDNEXDLY (DDRDLYCFG1<25:20>)	Power-Down Exit Delay	tXP - 1 or tCKE - 1 whichever is greater	nClk
SLFREFMINDLY (DDRDLYCFG1<7:0>)	Self-Refresh Minimum Delay	tCKE - 1	nClk
PWRDNMINDLY (DDRDLYCFG1<19:16>)	Power-Down Minimum Delay	(tCKE/CTL_CLK_PER) - 1	nClk
RMWDLY (DDRDLYCFG0<31:28>)	Read-Modify-Write Delay	RL – WL + 3	nClk
REFCNT (DDRREFCFG<15:0>)	Average Refresh Count	(tRFI/CTL_CLK_PER) - 2	nClk
R2WDLY (DDRDLYCFG0<27:24>)	Read-to-Write Delay	BL + 2	nClk
W2WCSDLY<3:0> (DDRDLYCFG0<23:20>)	Write-to-Write Chip Select Delay	BL - 1	nClk
W2WDLY (DDRDLYCFG0<19:16>)	Write-to-Write Delay	BL - 1	nClk
R2RCSDLY (DDRDLYCFG0<15:12>)	Read-to-Read Chip Select Delay	BL	nClk
R2RDLY (DDRDLYCFG0<11:8>)	Read-to-Read Delay	BL - 1	nClk
RBENDDLY (DDRDLYCFG3<31:28>)	Read Burst End Delay	RL + 3	nClk
NXTDATRQDLY (DDRXFERCFG<3:0)	Next Data Request Delay	WL - 2	nClk
NXTDATAVDLY<3:0> (DDRXFERCFG<7:4>) NXTDATAVDLY<4> (DDRDLYCFG1<28>)	Next Data Available Delay	RL + 4	nClk
RDATAENDLY<3:0> (DDRXFERCFG<19:16>)	Read Data Enable Delay	RL - 2	nClk

Legend: CTL_CLK_PER = Controller Clock Period (DRAM clock period * 2); nClk = Number of Clocks

Note: All fractional results are rounded up to the nearest number of clocks.

55.4.3 On-Die Termination (ODT) Configuration

On-Die Termination (ODT) is used for impedance matching of the SDRAM transmission lines. Properly matched transmission lines reduce signal reflection and noise. Having the termination resistors on the silicon die eliminates impedance discontinuity to external resistors, reduces component count and simplifies board layout.

ODT is enabled and controlled at both the controller and PHY level. This section discusses the controller settings. ODT settings can be enabled individually for each supported Chip Select. ODT enable/disable for a given Chip Select is a two-step process:

1. Program the ODTCSEN<7:0> bits (DDRODTCFG<7:0>) with the total number of Chip Selects multiplied by the Chip Select number to be enabled or disabled.
2. Program the ODTREN bit (DDRODTENCFG<0>) and the ODTWEN bit (DDRODTENCFG<16>) to enable or disable ODT for that Chip Select.

Note: The PIC32 device has only one SDRAM Chip Select; therefore, the ODTCSEN<7:0> bits should always be programmed to zero.

The start and duration of ODT for both read and write can be individually controlled. Refer to the DDR On-Die Termination Configuration register (Register 55-17) for details.

55.5 SDRAM INITIALIZATION

DDR SDRAMs must be initialized prior to use. Initialization is performed by writing a sequence of commands to the SDRAM. The DDR SDRAM controller provides host command registers for this purpose.

The Host command registers used to initialize the SDRAM are listed in Table 55-5.

Table 55-5: Host Command Registers

Register	See...	Function
DDRMEMCON	Register 55-5	DDR Memory Control Register
DDRCMDISSUE	Register 55-19	DDR Command Issue Register
DDRCMD1x (‘x’ = 0-15)	Register 55-22	DDR Command 1 Register ‘x’
DDRCMD2x (‘x’ = 0-15)	Register 55-23	DDR Command 1 Register ‘x’

The DDR command registers are two sets of 16 registers each. These registers hold the initialization commands that are transmitted to the SDRAM. The DDRCMDISSUE register is programmed with the number of initialization commands to be transmitted, and the VALID bit is set when the commands are loaded into the command registers. Once the commands are loaded and the DDRCMDISSUE register is programmed, the initialization is started by writing to the STINIT bit (<DDRMEMCON<0>). The VALID bit is cleared by hardware when all of the commands have been transmitted. Once the VALID bit is cleared, the memory controller is enabled by setting the INITDN bit (DDRMEMCON<0>).

The bit fields in the DDRCMD1*x* and DDRCMD2*x* registers correspond to the signals between the controller and the DRAM. The CKE, CS, RAS, CAS, and WE signals are decoded by the DRAM and interpreted as commands. Each of the command signals may have different states on the first and subsequent clock cycles of the command, so each signal has a separate bit field for the first and subsequent clock cycles. The four commands required for DRAM initialization are shown in Table 55-6. The plus sign following the signal name indicates the value that corresponds to the second and subsequent clock cycles of issuing the command. These are a subset of the commands available. Refer to the SDRAM data sheet for a complete list of commands supported for that device.

Table 55-6: SDRAM Initialization Commands

Command	Description	WE+	CAS+	RAS+	CS+	CKE+	WE	CAS	RAS	CS	CKE
DSELECT	Deselect device	1	1	1	1	1	1	1	1	1	1
PCALL	Precharge all banks	1	1	1	1	1	0	1	0	0	1
LDM	Load mode register(s)	1	1	1	1	1	0	0	0	0	1
REF	Refresh	1	1	1	1	1	1	0	0	0	1

When writing a mode register using the LDM command, the bank address registers are decoded to determine the Mode Register Set, and the address bits are mapped to various SDRAM parameters. Each of these bits must be defined appropriately. Refer to the SDRAM data sheet for the address bit mapping for that particular device.

55.5.1 DRAM Initialization Sequence

The following steps are required to perform DDR SDRAM initialization:

1. Power up and start the DDR clock. The DDR clock must be stable for a minimum of 200 µs before transmitting initialization commands.
2. Program the DDRCMD1x and DDRCMD2x registers with the following sequence of commands:
   a) Bring CKE high after Reset, and then wait 400 ns using a NOP or DESELECT command.
   b) Issue a Precharge All Banks command.
   c) Initialize Extended Mode Register 2 (EMR2).
   d) Initialize Extended Mode Register 3 (EMR3).
   e) Enable the DLL by writing to the Extended Mode Register (EMR).
   f) Reset the DLL by writing to the Mode Register (MR).
   g) Issue a Precharge All Banks command.
   h) Issue two Auto-refresh commands.
   i) Reprogram the MR without resetting the DLL.
   j) Reprogram the EMR with the OCD default.
   k) Reprogram the EMR with a OCD exit.
3. Write the number of commands to NUMHOSTCMDS (DDRCMDISSUE<3:0>).
4. Set the VALID bit (DDRCMDISSUE<4>).
5. Set the STINIT bit (DDRMEMCON<0>).
6. Wait for the VALID bit (DDRCMDISSUE<4>) to be cleared by hardware.
7. Set the INITDN bit (DDRMEMCON<1>) to enable the controller.
8. The DDR SDRAM is now ready for normal operation.

55.6 DDR PHY INITIALIZATION

The DDR PHY is the physical interface between the DDR Controller and the SDRAM. Both the controller and PHY conform to the DFI specification, which defines the interface protocol between the controller and PHY.

55.6.1 PHY Self-calibrating Logic

The DDR PHY contains Self-Calibrating Logic (SCL) that helps eliminate DDR timing problems. Read data capture timing and write alignment timing are set up automatically during PHY initialization by SCL. SCL is largely automatic, with only a few parameters configurable by the user, as listed in Table 55-7.

Table 55-7: SCL Recommended Settings

Parameter	Description	Register Field	Recommended Setting
ODT on a SCL Write	ODT enabled/disabled during a SCL write	ODTCSWR (DDRSCLCFG0<24>)	Enabled
SCL Burst Size	DRAM in Burst 8 or Burst 4 mode during SCL	BURST8 (DDRSCLCFG0<24>)	Burst 8 Mode
SCL Delay	SCL delay following acknowledge. This parameter is a function of hardware design.	DBLREFDLY(DDRSCLCFG1<12>)	Single Delay
SCL Enabled	Enable SCL on Chip Select 0.	SCLTESTCS (DDRSCLCFG1<0>)	Enabled

55.6.2 PHY I/O Pad ODT Resistor Calibration

Programmable ODT provides selectable 75 or 150 ohm termination. The termination is enabled and selected via the PHY pad control register. ODT is implemented using a Thevenin Equivalent Circuit of equal resistances to VDD and VSS. Calibration inputs are provided to fine-tune ODT resistance. The recommended settings are listed in Table 55-8.

Table 55-8: ODT Resistance Calibration Recommended Settings

Parameter	Description	Register Field	Recommended Setting
ODT Enable	ODT Enable/Disable	ODTEN (DDRPHYPADCON<1>)	Enabled
ODT Term Select	Select 75 or 150 ohm ODT	ODTSEL (DDRPHYPADCON <0>)	150 ohm
ODT Pull-up Calibration	ODT Pull-up Calibration	ODTPUCAL (DDRPHYPADCON<7:6>)	0'b10
ODT Pull-down Calibration	ODT Pull-down Calibration	ODTPDCAL (DDRPHYPADCON<5:4>)	0'b10

55.6.3 PHY Pad Drive Strength

DDR memories support two drive strengths, full and reduced (60%). The drive strength configuration is set by the PHY Pad Control register bit, DATDRVSEL (DDRPHYPADCON<3>). Driver output impedance is optimized around 30 ohms for full drive and 55 ohms for reduced drive. The output impedance may be fine-tuned using the PHY Pad Control register bits, DRVSTRNFET<3:0> (DDRPHYPADCON<23:20>) and DRVSTRPFET<3:0> (DDRPHYPADCON<19:16>).

55.7 DLL CALIBRATION

The DDR PHY contains an internal digital DLL to align data and data strobes with the PHY clock. The DLL is self-calibrating, but the calibration interval must be programmed during initialization. The recommended start value and recalibration interval are shown in Table 55-9.

Table 55-9: Start Value and Recalibration Interval Recommended Settings

Parameter	Description	Register Bits	Recommended Setting
DLL Recalibrate Enable	DLL Recalibration Enable	DISRECALIB (DDRPHYDLLR<26>)	Enabled
DLL Delay Start Value	DLL Master Delay Line Start Value	DLYSTARTVAL (DDRPHYDLLR<31-28>)	3
Recalibration Count	Number of clocks between requests to the controller for DLL recalibration	RECALIBCNT (DDRPHYDLLR <25:8>)	0x10

55.8 INTERRUPTS

There are no interrupts associated with the DDR Controller.

55.9 OPERATION IN POWER-SAVING MODES

55.9.1 DDR Operation in Sleep Mode

As the device enters Sleep mode, the system clock (SYSCLK) to the CPU is disabled, but the clock to the DDR Controller is maintained by the MPLL. The DDR Controller will continue to refresh the SDRAM, but the CPU will be unable to read or write to the SDRAM. Therefore, it is possible to maintain the contents of the SDRAM while in Sleep mode.

To further reduce power in Sleep mode, the user may disable the clock by removing power from the MPLL and disabling the DDR Controller and PHY. This can be done by setting the PDMPLL bit (CFGAPP2<30>) and the DDRMD bit (PMD7<28>).

Note: Issuing a read or write to the DDR Controller when the clock is not ready could result in undefined device behavior.

55.9.2 DDR Operation in Deep Sleep Mode

PIC32 devices with DDR can be placed into a Self-Refresh mode. The user should adhere to the entry and exit descriptions for Self-Refresh mode provided by the vendor of the DDR device being used. To achieve this, the DDRCKE pin is held low when the core logic power is removed. The other signals to the DDR are placed in a Hi-Z state. Further, the DDRVREF signal must be valid at all times during self-refresh.

If Deep Sleep mode is entered while the DDR2 device is in Self-Refresh mode, the core voltage will be turned off, but the enable for the VREF circuit will continue to be driven per the last settings of the INTVREFCON <1:0> bits (CFGMPLL<7:6>), even when the core voltage is not valid.

When Deep Sleep mode is exited and the core voltage is again valid, the user must reload the INTVREFCON<1:0> bits with the desired settings before exiting the Deep Sleep mode handler. The Reset sequence that is executed upon leaving Deep Sleep mode then resumes using the values from the INTVREFCON<1:0> bits.

Note: Refer to the **"Special Features"** chapter in the specific device data sheet for information on the INTVREFCON<1:0> bits in the CFGMPLL register.

55.10 EFFECTS OF RESET

All forms of reset force the DDR Controller and PHY registers to the default state. The controller, PHY and SDRAM must be reinitialized before use.

55.11 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to DDR SDRAM Controller include the following:

Title	Application Note #
No related application notes at this time.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32 family of devices.

55.12 REVISION HISTORY

Revision A (February 2016)

This is the initial released version of this document.

Revision B (May 2017)

This revision includes the following updates:

- The POR values for the RQPER<7:0> bits in the DDRRQPER register were updated (see Register 55-3)
- The POR values for the MINCMD<7:0> bits in the DDRMINCMD register were updated (see Register 55-4)
- The POR values for the MAXBURST<3:0> bits in the DDRXFERCFG register were updated (see Register 55-18)
- The bit type for the SCLEN, SCLUBPASS, and SCLLBPASS bits in the DDRSCLSTART register were changed from U-0 to R/W-0 (see Register 55-24)
- The POR values for the DDRCLKDY<3:0> and CAPCLKDY<3:0> bits in the DDRSCLLAT register were updated (see Register 55-25)
- The following changes were made to the DDRSCLCFG0 register (see Register 55-26):
  - The POR values for the ODTCSW, RCASLAT<3:0>, and BURST8 bits were updated
  - The DDR3 bit was removed
  - The DDR2 bit was renamed to: DDR
- The following changes were made to the DDRPHYPADCON register (see Register 55-28)
  - The POR values for the PREAMBDLY<1:0>, DRVSTRNFET<3:0>, DRVSTRPFET<3:0>, HALFRATE, ODTPUCAL<1:0>, ODTEN, and ODTSEL bits were updated
  - The WRMCMDDLY bit was added
  - The ADDCDRVSEL bit was added
  - The DRVSEL bit was renamed to: DATDRVSEL
- The DDRPHYDLLRECALIB register was renamed to: DDRPHYDLLR (see Register 55-29)
- The DDRPHYCLKDLY register was added (see Register 55-30)
- **55.9.2 “DDR Operation in Deep Sleep Mode”** was updated
- In addition minor updates to text and formatting were incorporated throughout the document

NOTES:

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