ADC081S051,ADC081S101,ADC101S051, ADC101S101,ADC121S051,ADC121S101, LMP2011,LMP2012,LMP7711,LMP7712

Amplifier Closed-Loop Bandwidth Considerations in High Resolution A/D Converter Applications

Literature Number: SNOA829

ANALOG edge℠

Expert tips, tricks, and techniques for analog designs

Vol. IV, Issue 10

DESIGN idea

Amplifier Closed-Loop Bandwidth Considerations in High Resolution A/D Converter Applications

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Amplifier Bandwidth Limitations

Amplifier closed-loop bandwidth-limited accuracy considerations are critical when driving high resolution A/D Converters (ADCs). It is useful to be able to predict, for any closed loop gain, the required gain-bandwidth (GBW) product of an op amp to achieve a specified level of accuracy in terms of the minimum ADC resolution. Other sources of error include offset, noise, and distortion, which are beyond the scope of this article. A simple equation will be developed below that relates the minimum closed-loop bandwidth of an op amp to the resolution requirements of a given ADC.

Amplifier Response

Assuming a single pole roll-off, the frequency dependence of an amplifier's closed-loop gain, A_{CL}, is given by:

$$A_{CL} = \frac{A_{CLDC}}{\sqrt{1+\left(\frac{f}{f_{-3\,dB}}\right)^2}} \qquad \textit{Equation 1}$$

where A_{CLDC} is the amplifier's DC gain, and $f_{-3\,dB}$ is its corner frequency.

This equation describes the op amp's closed-loop gain at frequency ***f***, in terms of the amplifier's corner frequency.

The vast majority of op amps employ internal lag compensation with a single dominant pole that rolls off the open-loop gain, from its cut-off frequency, to unity gain (zero dB) at a 20 dB per decade rate. The frequency response of such an amplifier with feedback is therefore also the same as for an RC low-pass filter. The frequency where the open-loop gain crosses unity gain is routinely called the GBW product in op amp datasheets. The GBW product for an amplifier is the product of its open loop gain (constant for a given amplifier) and its -3 dB bandwidth (GBW product = gain x -3 dB bandwidth). Given the GBW product and the open-loop gain roll-off of -20 dB per decade, the -3 dB bandwidth for any closed loop gain can be easily calculated, from

$$BW = GBW / A_{CL} \qquad \textit{Equation 2}$$

For example, the LMP2011 with a GBW product of 3 MHz will have a bandwidth of 300 kHz when configured with an A_{CL} of 10 V/V. However, at -3 dB the closed-loop gain has a 29.3% gain error. In reality, the gain expression starts rolling off long before the -3 dB pole frequency is reached. It is important to determine the frequency at which the closed-loop gain error increases above the maximum error allowed for a given data error. The maximum error in data

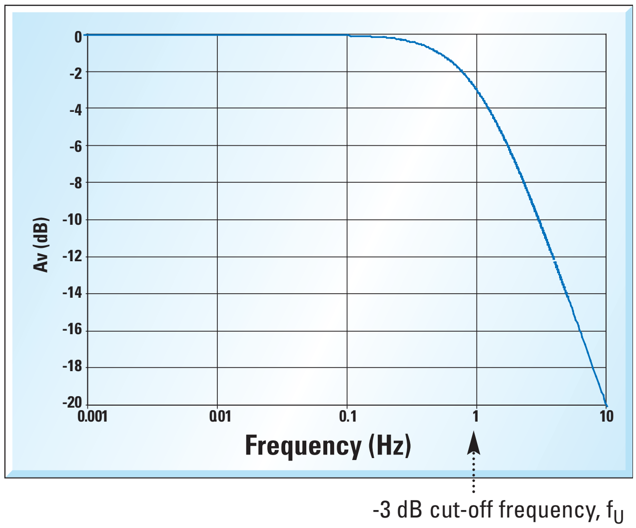

Figure 1. Normalized bandwidth curve for an op amp in unity gain (Curve assumes an open loop gain with a single pole roll-off.)

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Dithered Switching Frequency

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Single/Dual, High Precision, Rail-to-Rail Output Operational Amplifier

The LMP2011/12/14 (single/dual/quad) are part of the LMP™ family of precision amplifiers that offer an industry leading gain bandwidth of 3 MHz, while maintaining high precision and low drift over time. These amplifiers deliver excellent CMRR (130 dB) and PSRR (120 dB) ratings without frequency related noise (no 1/f). The high CMRR allows for high accuracy across voltages.

The LMP2011/12/14 deliver a very low input offset voltage which offers high accuracy measurements with continued accuracy over temperature. The low voltage noise increases signal accuracy during low frequency measurements. No external capacitors are required.

Features

- Low guaranteed V_{OS} over temperature 60 µV
- Low noise with no 1/f , 35 nV/$\sqrt{Hz}$
- High CMRR 130 dB
- High PSRR 120 dB
- High A_{VOL} 130 dB
- Wide gain-bandwidth product 3 MHz
- High slew rate 4 V/µs
- Low supply current 930 µA
- Rail-to-rail output 30 mV from rails

The extended temperature range of -40ºC to 125ºC allows for operation in demanding industrial and automotive applications, as well as in precision instrumentation amplifiers, thermocouple amplifiers, and strain gauge bridge amplifiers. The LMP2011 is offered in SOIC-8 and SOT23-5 packaging. The LMP2012 is offered in SOIC-8 and mini SOIC-8 packaging. The LMP2014 is offered in TSSOP-14 packaging.

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Low Power, 200 kSPS to 500 kSPS, 8/10/12-Bit A/D Converters

The ADC081S051, ADC101S051, and ADC121S051 are low-power, single channel, CMOS 8/10/12-bit Analog-to-Digital Converters (ADCs) with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, these ADCs are fully specified over a sample rate range of 200 kSPS to 500 kSPS.

Operation with a single supply can range from +2.7V to +5.25V. Normal power consumption for the ADC121S051 using a +3.6V or +5.25V supply is 1.7 mW and 8.7 mW, respectively. The power-down feature reduces the power consumption to as low as 2.6 µW using a +5.25V supply.

Features

- Speed range: 200 kSPS to 500 kSPS
- Integral Non-Linearity (INL):
  - +0.45, -0.40 LSB (ADC121S051)
  - +0.15, -0.09 LSB (ADC101S051)
  - +0.06, -0.05 LSB (ADC081S051)
- Differential Non-Linearity (DNL):
  - +0.5, -0.25 LSB (ADC121S051)
  - +0.15, -0.11 LSB (ADC101S051
  - +0.06, -0.045 LSB (ADC081S051)
- Signal-to-Noise Ratio (SNR):
  - 72.0 dB (ADC121S051)
  - 61.6 dB (ADC101S051)
  - 49.6 dB (ADC081S051)

The ADC081S051, ADC101S051, and ADC121S051 are ideal for use in applications including portable systems, remote data acquisitions, and instrumentation and control systems. These low power ADCs are offered in LLP-6 and SOT23-6 packaging.

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Amplifier Closed-Loop Bandwidth Considerations in High Resolution A/D Converter Applications

converters is usually expressed in terms of the Least Significant Bit (LSB). Ideally, all error sources should be well below this level. An LSB of an ADC is defined as the finest resolution of which the ADC is capable. Quantitatively this is equal to the full scale voltage divided by the resolution of the ADC ($V_{FS}/2^N$) for one LSB, were N is the number of bits. Thus for an 8-bit converter, the error would be $V_{FS}/256$. If ½ LSB is set as the required system accuracy, the acceptable accuracy limit would be:

Accuracy (δ) = 100% - gain error (%),

where gain error = 1/2 ($1/2^N$) *100%, *Equation 3*

which gives δ **= 100% - 1/2 ($1/2^N$) *100%,** or 99.8%

The accuracy is calculated based on the -3 dB cut-off frequency at a particular close-loop gain. Approximating the frequency response of an op amp to that of a single pole filter, we get the frequency vs gain curve of such a system as shown in ***Figure 1.***

Because the curve is normalized to 1 for a frequency f_U (-3 dB at unity gain), the expression for this curve, for any ***f***, from ***Equation 1*** is

$$A_{CL} = \frac{1}{\sqrt{1+(f)^2}} \qquad \textit{Equation 4}$$

Solving for f gives

$$f = \sqrt{\frac{1}{(A_{CL})^2} - 1} \qquad \textit{Equation 5}$$

The question is now, for any ACL, what is the maximum signal frequency that does not exceed the specified error? From ***Equation 1, Equation 3,*** and ***Equation 5***, and the example for 8-bit accuracy, the normalized frequency, f_{MAX}, for an amplifier requiring 99.8% accuracy, is the frequency where the gain roll off is less than ½ LSB is expressed as

$$f_{max} = \sqrt{\frac{1}{(0.998)^2} - 1} \times f_U = 0.062 \times f_U \qquad \textit{Equation 6}$$

for the case of unity gain.

Thus, the maximum frequency at which it is still possible to get at least 99.8% (½ LSB) accuracy in an 8-bit system, is 0.062 of the op amp's -3 dB frequency. In the case of the LMP2011 example, the available bandwidth for 99.8% accuracy is

$$0.062 \times f_{-3\,dB}\ \text{kHz} = 0.062 \times 300\ \text{kHz} = 18.6\ \text{kHz}$$

In general, the normalized f_{MAX} for ½ LSB error for ADCs of various resolutions can be calculated as

$$\text{Normalized } f_{MAX} = \sqrt{\frac{1}{\left(1-\frac{1}{2^{n+1}}\right)^2} - 1} \qquad \textit{Equation 7}$$

Using this equation, a list of normalized bandwidths for system resolutions up to 16 bits have been calculated *(Table 1)*.

System Resolution	Normalized Bandwidth for <1/2 LSB Error
8-bit	0.062592
9-bit	0.044227
10-bit	0.031261
11-bit	0.022101
12-bit	0.015626
13-bit	0.011049
14-bit	0.007813
15-bit	0.005524
16-bit	0.003906

Table 1. Calculated maximum frequency with an error less than ½ LSB at the specified resolution

Conclusion

Obtaining dynamic performance compatibility between an amplifier and an ADC in data acquisition designs requires careful analysis of the amplifier's bandwidth capability. Choosing an amplifier that satisfies the bandwidth requirements of the system on the basis of its GBW product specification can introduce an excessive amount of error into the system. The amplifier must be chosen such that its closed-loop bandwidth matches the resolution needs of the ADC. This dictates the need for a much wider bandwidth amplifier than would be suggested by the specified signal bandwidth in the amplifier's datasheet. ■

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Low Power, High Precision 8/10/12-Bit, 1 MSPS A/D Converters

The ADC081S101, ADC101S101, and ADC121S101 are low-power, single channel, CMOS 8/10/12-bit Analog-to-Digital Converters (ADCs) with a high-speed serial interface. Operation with a single supply can range from +2.7V to +5.25V. Normal power consumption using a +3V or +5V supply is 2 mW and 10 mW, respectively. The power-down feature reduces the power consumption to as low as 2.5 μW using a +5V supply.

Features

- Speed range: 500 kSPS to 1 MSPS
- Integral Non-Linearity (INL):
  - ±0.4 LSB (ADC121S101)
  - ±0.2 LSB (ADC101S101)
  - ±0.05 LSB (ADC081S101)
- Differential Non-Linearity (DNL):
  - +0.5, -0.3 LSB (ADC121S101)
  - +0.3, -0.2 LSB (ADC101S101
  - ±0.07 LSB (ADC081S101)
- Signal-to-Noise Ratio (SNR):
  - 72.5 dB (ADC121S101)
  - 62 dB (ADC101S101)
  - 49.7 dB (ADC081S101)

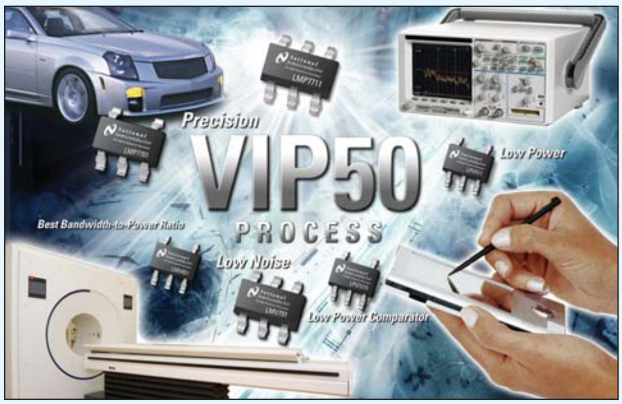
The ADC081S101, ADC101S101, and ADC121S101 are ideal for use in applications including portable systems, remote data acquisitions, instrumentation, and control systems. These ADCs are offered LLP-6 and SOT23-6 packaging.

For FREE samples, datasheets, and more, visit
www.national.com/pf/DC/ADC081S101.html
www.national.com/pf/DC/ADC101S101.html
www.national.com/pf/DC/ADC121S101.html

Precision, 17 MHz, Low Noise, CMOS Input Op Amps

The LMP7711/12 (single/dual) are low-noise, low offset, CMOS input, rail-to-rail output precision amplifiers with a high gain bandwidth and an enable pin. These precision amplifiers achieve an input bias current of 100 fA, an input referred voltage noise of 5.8 $nV/\sqrt{Hz}$ and an input offset voltage of less than ±150 μV, using a CMOS input stage.

These features make the LMP7711/12 superior choices for precision applications. Consuming only 1.15 mA of supply current, the LMP7711 offers a high gain bandwidth product of 17 MHz, enabling accurate amplification at high closed loop gains. The high PSRR (100 dB) and CMRR (100 dB) ensure high accuracy with noisy supplies, and high accuracy over a wide input range.



Features

- ±150 μV (max) input offset voltage
- 100 fA input bias current
- 5.8 $nV/\sqrt{Hz}$ input voltage noise
- 17 MHz gain bandwidth product
- 1.15 mA supply current (LMP7711)
- 1.30 mA supply current (LMP7712)
- 0.001% THD+N at f = 1 kHz
- Rail-to-rail output swing

Operating at -40°C to +125°C, these precision amplifiers are ideal for use in sensor interface applications, transimpedance amplifiers, and active filters and buffers. The LMP7711 is offered in Thin SOT23-6 packaging and the LMP7712 is offered in a MSOP-10 packaging.

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