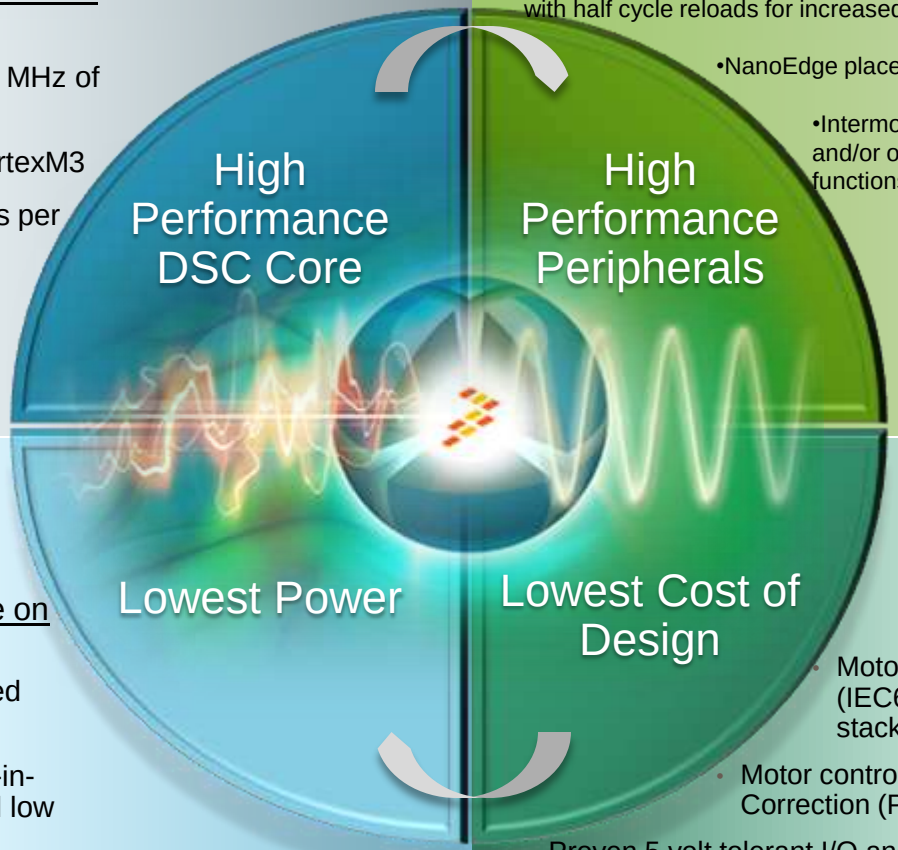
Freescale Digital Signal Controllers (DSC) Introduction

AMF-IND-T0794

Mark Houston / Ron Lowman
Industrial Solutions Team
Microcontroller Solutions Group

September 2013

…C56F827x – Half the Power, Twice the Performance (100MHz in a 5x5 32pin QFN!)



100MHz DSP 32-BIT 56800EX Hawk V3 core

- Fastest DSC in its class with 100 MHz of performance
- FIR Filter 6x faster than ARM CortexM3
- The highest number of operations per cycle of any MCU in its class
- Fractional arithmetic
- Nested looping
- Superfast interrupt

- eFlexPWM – Freescale's most advance timer for Digtial Power Conversion with up to 8ch and 312pico-sec resolution, supported by 4 independent time bases, with half cycle reloads for increased flexibility and best in class performance
- NanoEdge placer to implement fractional delays
- Intermodule Cross-Bar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)
- DAC with hardware Waveform generation support
- Very high speed ADCs capture events real time.

The lowest power DSC available on the market

- Less than 0.4mA/Mhz at full speed run
- Concurrent operations offer best-in-class execution times and overall low power run rates.

Advanced Integration & development speed

- A high level of on-chip integration lowers external Op Amp and capacitor costs.
- Motor Control, Power Control, Safety (IEC60730) Libraries, PMBus software stack, PLC software stack.
- Motor control with integrated Power Factor Correction (PFC) reducing chip count.
- Proven 5 volt tolerant I/O and Peripheral Crossbar enable greater flexibility and system cost reduction.
- Development tools, including FREEMaster, enable real-time debug monitoring, data visualization, advanced modeling, rapid application design, and more.

Freescale DSC Roadmap

Microcontrollers Based on 32-bit Hawk 56800EX core in Freescale's 90nm TFS

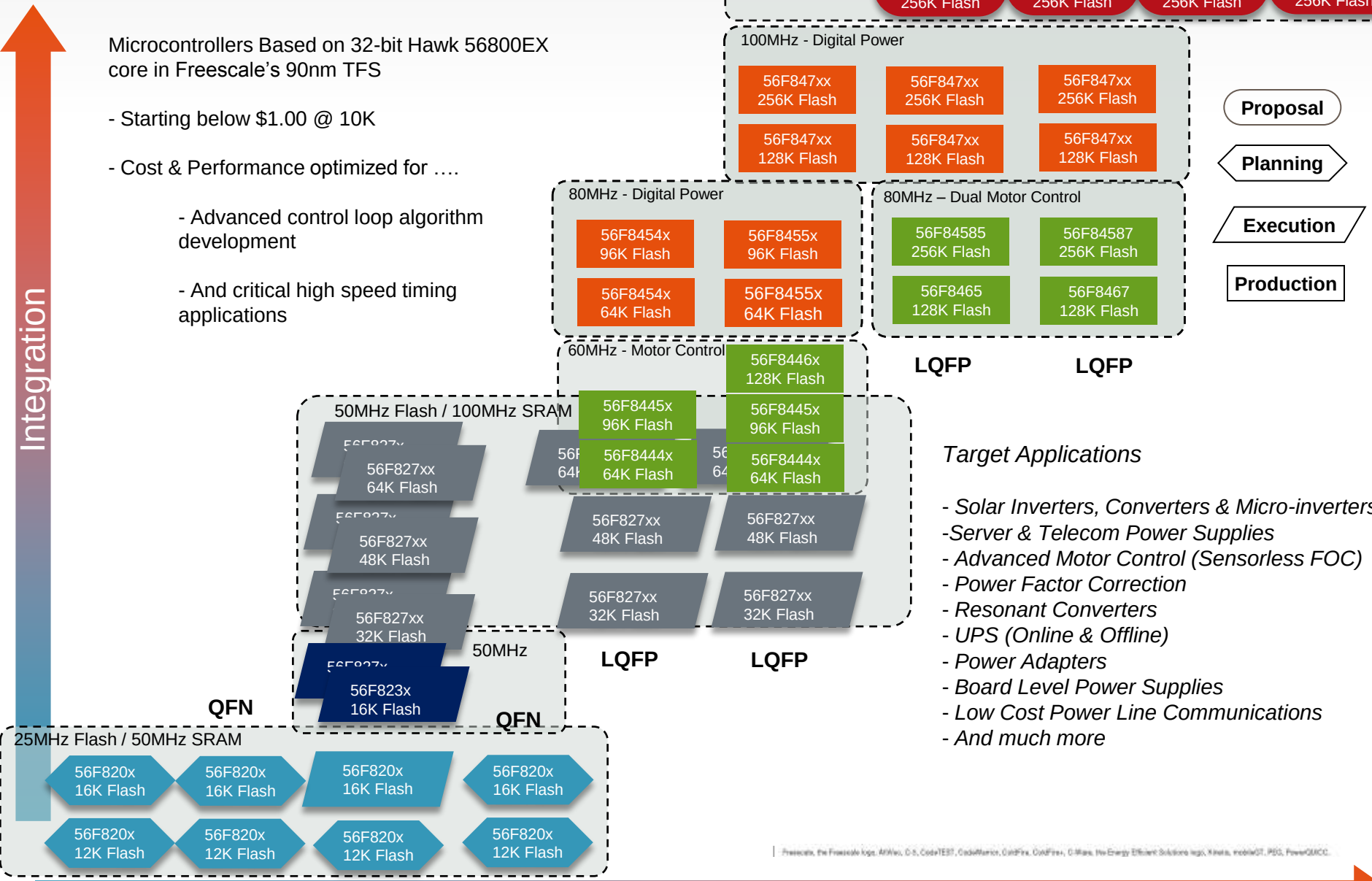
- Starting below $1.00 @ 10K

- Cost & Performance optimized for ….

  - Advanced control loop algorithm development

  - And critical high speed timing applications

Integration



Target Applications

- Solar Inverters, Converters & Micro-inverters
-Server & Telecom Power Supplies
- Advanced Motor Control (Sensorless FOC)
- Power Factor Correction
- Resonant Converters
- UPS (Online & Offline)
- Power Adapters
- Board Level Power Supplies
- Low Cost Power Line Communications
- And much more

MC56F827xx (64kB Flash, 50/100MHz)

Key Features:

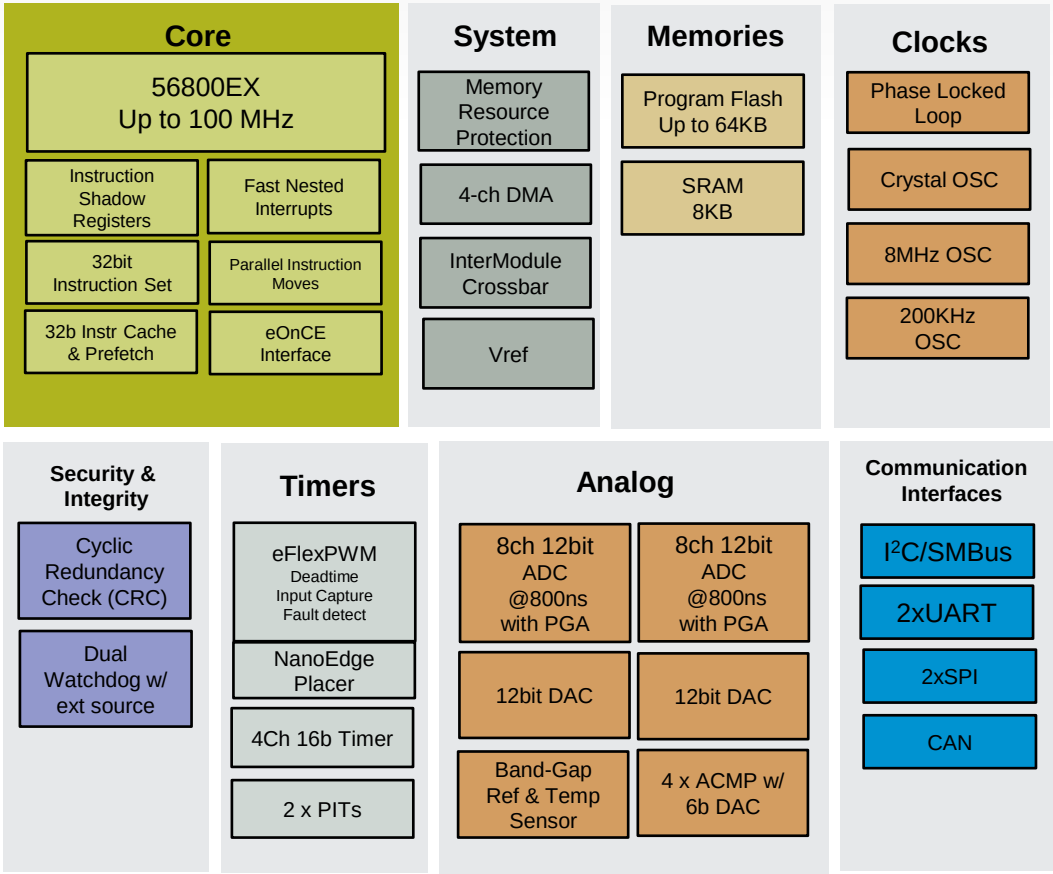
Core
• 56800EX @ 50/100MHz supporting fractional arithmetic with 4 accumulators, 8 cycle pipeline, separate program and data memory maps for parallel moves, single cycle math instructions, nested looping, and superfast interrupts that far outpace any competitive core on the market.

System
• Inter-module crossbar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)
• DMA controller for reduced core intervention when shifting data from peripherals
• Memory resource protection unit to ease safety certification

Timers
• eFlexPWM – Freescale's most advance timer for Digtial Power Conversion, up to 8ch and 312 pico-sec resolution, 4 independent time bases, with half cycle reloads for increased flexibility, automatic complimentary mode for ease of use and best in class performance

Analog
- 2x12-bit high-speed ADCs each with 800ns conversion rates
- 4 analog comparators with integrated 6-bit DACs that can enable emergency shutdown of the PWMs
- Integrated PGAs to increase the accuracy of ADC conversions on small voltages and currents

Power Consumption:
- Best in class Power Consumption – 50% better than nearest competitor



Others: 5-volt tolerant I/O for cost-effective board design

Packages: 32QFN (5x5), 32LQFP, 48LQFP, 64LQFP

Temperature: -40 to +105C across all packages, with -40 to +125C option on 64LQFP

MC56F823xx (32kB Flash, 50MHz)

Key Features:

Core

• 56800EX @ 50MHz supporting fractional arithmetic with 4 accumulators, 8 cycle pipeline, separate program and data memory maps for parallel moves, single cycle math instructions, nested looping, and superfast interrupts that far outpace any competitive core on the market.

System

• Inter-module crossbar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)

• DMA controller for reduced core intervention when shifting data from peripherals

• Memory resource protection unit to ease safety certification

Timers

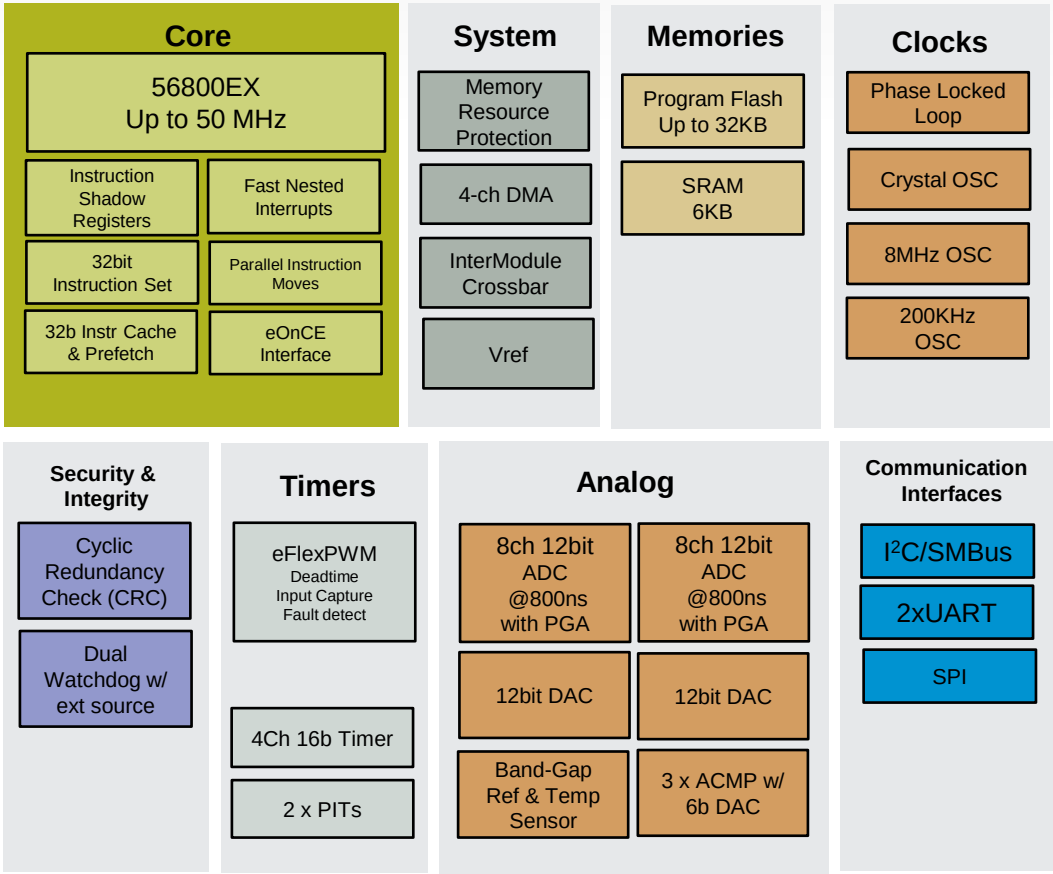
• eFlexPWM – Freescale's most advance timer for Digtial Power Conversion, up to 8ch and 312 pico-sec resolution, 4 independent time bases, with half cycle reloads for increased flexibility, automatic complimentary mode for ease of use and best in class performance

Analog

- 2x12-bit high-speed ADCs each with 800ns conversion rates
- 4 analog comparators with integrated 6-bit DACs that can enable emergency shutdown of the PWMs
- Integrated PGAs to increase the accuracy of ADC conversions on small voltages and currents

Power Consumption:

- Best in class Power Consumption – 50% better than nearest competitor



Others: 5-volt tolerant I/O for cost-effective board design

Packages: 32QFN (5x5), 32LQFP, 48LQFP

Temperature: -40 to +105C across all packages

MC56F84xxx (256kB Flash, 100MHz)

Key Features:

Core

• 56800EX @ 100MHz supporting fractional arithmetic with 4 accumulators, 8 cycle pipeline, separate program and data memory maps for parallel moves, single cycle math instructions, nested looping, and superfast interrupts that far outpace any competitive core on the market.

System

• Inter-module crossbar directly connecting any input and/or output with flexibility for additional logic functions (AND/OR/XOR/NOR)

• DMA controller for reduced core intervention when shifting data from peripherals

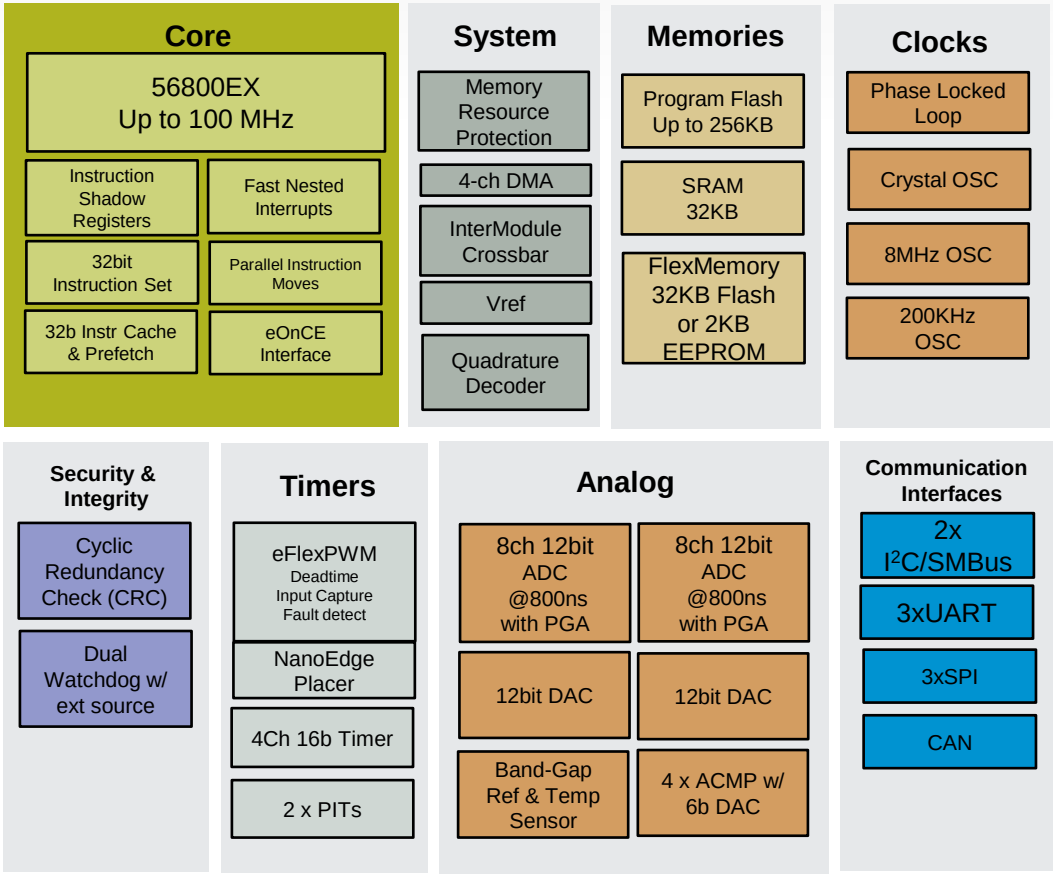
• Memory resource protection unit to ease safety certification

Timers

• eFlexPWM – Freescale's most advance timer for Digtial Power Conversion, up to 8ch and 312 pico-sec resolution, 4 independent time bases, with half cycle reloads for increased flexibility, automatic complimentary mode for ease of use and best in class performance

Analog

- 2x12-bit high-speed ADCs each with 800ns conversion rates
- 16 ch 16b SAR ADC that enables external sensors inputs and accurate system measurements
- 4 analog comparators with integrated 6-bit DACs that can enable emergency shutdown of the PWMs
- Integrated PGAs to increase the accuracy of ADC conversions on small voltages and currents



Others: 5-volt tolerant I/O for cost-effective board design
Freescale FlexMemory for simplified data storage

Packages: 48LQFP, 64LQFP, 80LQFP, 100LQFP

Temperature: -40 to +105C across all packages

Tools and Software

- Tower Development Kit TWR-56F8400
- High Voltage and Low Voltage Motor Control & Power Conversion Boards

FreeMASTER

Real-Time Debug, Monitoring and Visualization GUI development Tool

CodeWarrior

Comprehensive IDE that provides a highly visual, automated framework to accelerate development of some of the most complex embedded applications

Run Time Software

Digital Power Library
Motor Control Library
Filter Library
Safety Library
PMBUS Stack
CAN Stack & more……

QEDesign Lite

Complimentary graphical filtering tool used to auto-generate coefficients that drop into any project. Ideal for designing any type of filter

Processor Expert & QuickStart Init Tools

Rapid Init Code Generation as well as more advanced design tool features that combines easy-to-use component-based application creation with an expert knowledge system

Reference Designs

Complimentary code and schematics for :

- FOC PMSM motor control
- LLC resonant converter
- Solar power conversion
- Wireless Charging
- Lighting

SFIO

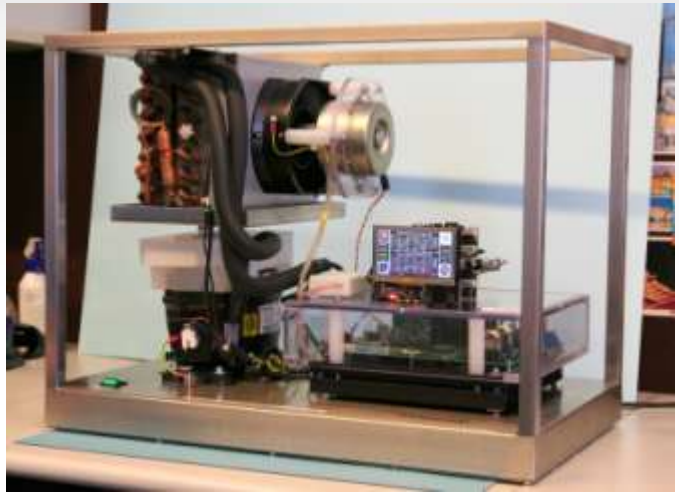
Matlab Plugin via FreeMaster

S-Function Input Output (SFIO) Toolbox
-smart simulation using the Matlab/Simulink tool for in-the-loop simulation & automatic testing tool

freescale™

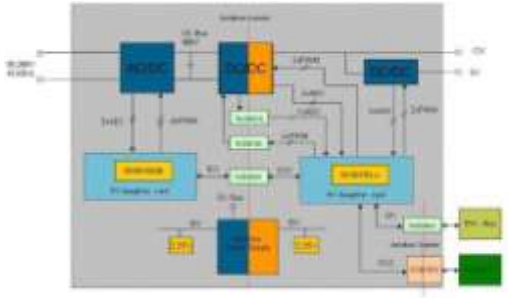
Dual Sensorless VOC PMSM with PFC usingMC56F84xxx

- Dual PMSM Vector Control Demo with PFC
- Application based on C-callable library functions (GFLIB, MCLIB, GDFLIB, ACLIB)
- Application software in C (CodeWarrior®)
- FreeMASTER visualization tool
- 3-in-1 high voltage power stage
- Kinetis K70 Touch Graphic LCD Tower
- Reference design manual



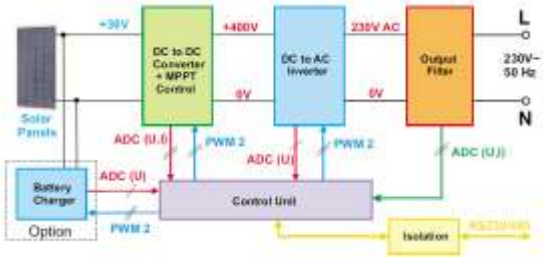
Switch Mode Power Supply

- AC/DC SMPS using 56F825x and 56F800x
  - Interleaved Power Factor Correction and AC/DC conversion are implemented by the 56F8006
  - LLC resonant half-bridge converter together with synchronous rectifier converts high voltage DC bus voltage to low voltage DC (12V)
  - Buck Converter lowers DC voltage to 12v and 5v
- LLC resonant half-bridge converter, synchronous rectifier and buck converter are controlled by the 56F8247 DSC



Solar Inverter

- DC to AC inverter consists of main power parts:
  - MPP Tracking for solar panel output – software implemented
  - DC low voltage to DC high voltage converter
  - DC high voltage to AC sine output voltage inverter
  - Output filter
  - Isolated RS-485 line
- Associated control and fault detection circuits
- Both DC-DC converter and DC-AC inverter is controlled by one DSC MC56F8023



Tools
CodeWarrior Development Tools for MCUs (Eclipse IDE)
USB TAP for ONCE DSC
P&E USB Multilink Universal (P&E DSC product support)
P&E Cyclone MAX
Processor Expert Software
FreeMASTER – Debug Monitor and Data Visualization Tool for application development and information management – (Training Overview)
Quick Start – Initialization and Development Tool
DSC Development Boards
http://www.freescale.com/TWR-56F8400
http://www.freescale.com/TWR-56F827x
TWR-MC-LV3PH: Low-Voltage, 3-Phase Motor Control Tower System Module
RTOS Support
MQX
FreeRTOS
uCOS II / Micrium
Software
56800E_FSLESL_R2.0 : 56800E Freescale Embedded Software Libraries
PMBUS – Freescale Power Management Bus (PMBus) Library
Embedded Component: FreescaleCAN - DLP-568-FLXCN-CX support for MC56F84xxx
Embedded Component: FreescaleCAN - DLP-568-MSCAN-CX support for MC56F827xx
Services enabling Telephony Feature Library (DLP-568-FPHON-CX)
Implementation of G.723.1A speech codec (DLP-568-G723-CX)
Implementation of G.729AB speech codec (DLP-568-G729A-CX)
Services to support Voice Recognition (DLP-568-VRLIT-CX)

Application Notes
ANxxxx -Using eFlexPWM with MC56F82xx DSC
AN4675 - eFlexPWM Module for ADC Synchronization for MC56F84xxx and MC56F82xxx
AN4656 - PMSM FOC of Industrial Drives using the 56F84789
AN4642 - Motor Control Application Tuning Tool for 3-Phase PMSM
AN4625 - DSC MC56F84xxx in Motor Control Applications
AN4615 – Freescale DSC in PV Solar Inverter Applications
AN4612 - Sensorless Sinusoidal Vector Control of BLDC Ceiling Fan on MC56F8006
AN4611 - Freescale Embedded Software and Motor Control Libraries
AN4608 - PWM and ADC on MC56F84789 to Drive Dual PMS Motor FOC
AN4598 - Using DMA Transfers with Enhanced Flexible PWM on MC56F84xxx
AN4583 - MC56F84789 Peripherals Synchronization for Interleaved PFC Control
AN4485 - Using eFlexPWM with MC56F82xx DSC
AN4429 - Using Motor Control eFlexPWM for BLDC Motors
AN4413 “BLDC Motor Control with Hall Sensors Driven by DSC (using TWR-56F8257 and TWR-MC-LV3PH Boards) (AN4413SW)
AN4386 – Single Phase Two Channel Interleaved Critical Conduction Mode
AN4381 - Configuring the FlexTimer for Position and Speed Measurement with an Encoder
AN4275 : Serial Bootloader for 56F82xx
AN3843 : Single Phase Two-Channel Interleaved PFC Converter Using MC56F8006
AN3815 : Implementing a Modular High Brightness RGB LED Network
AN3814 : Static Serial Bootloader for MC56F800x/801x/802x/803x
AN3118 : Production Flash Programming for the 56F8000 Family
AN3115 - Implementing a Digital AC-DC SMPS using 56F8300 DSC
AN3113 : Network-Enabled high Performance Triple Conversion UPS
AN1965 : AN1965 Design of Indirect Power Factor Correction
White Papers and User Guides
56800E754FPL04UG : 56800E Family IEEE-754 Compliant Floating-Point Library
WP8000 : Benefits and Applications Enabled by 56F8000 Digital Signal Controllers
LVMCDBLDCPMSMUG : 3-Phase BLDC/PMSM Low-Voltage Motor Control Drive

Reference Designs
DRM137 - Low Power Wireless Transmitter User's Guide
DRM126 - Inverter for the Solar Panel Using an MC56F8023
DRM119 - LLC Resonant ACDC SMPS using the MC56F8013 and MC56F8257
DRM110 - Sensorless PMSM Control for an H-axis Washing Machine Drive
DRM108 : BLDC Sensorless Reference Design Using MC56F8006
DRM102 : PMSM Vector Control with Single-Shunt Current-Sensing Using MC56F8013/23
DRM100 - Sensorless High Speed SR Motor Drive for Vacuum Cleaners using an MC56F8013
DRM099 : Sensorless PMSM Vector Control with Sliding Mode Observer for Compressors
DRM098 - Direct PFC Using the MC56F8013
DRM092 - 3Ph AC Induction Vector Control Drive with Single Shunt Current Sensing
DRM087 - Spread FSK Power Line Modem for CENELEC Band-A
DRM078 - 3-Phase BLDC Drive Using Variable DC Link Six-Step Inverter
DRM075 - Design of an ACIM Vector Control Drive using the 56F8013 Device
DRM077 - Design of PMSM and BLDC Sensorless Motor Control using the 56F8013 Device
DRM074 - Design of a Digital AC/DC SMPS Using the 56F8323 Device
DRM070 - Three-Phase BLDC Motor Sensorless Control Using MC56F8013/23
DRM069 - Online UPS using the 56F8300

Freescale DSC Performance vs. Competitors

Freescale Value Proposition

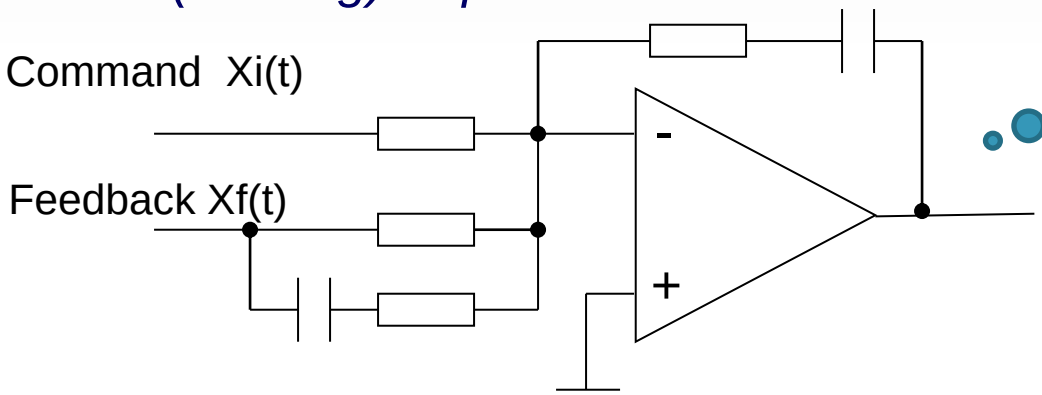
- Dynamic Performance - The greatest number of operations per cycle of any MCU in it's class

Attribute	Freescale DSC	TI Piccolo	Microchip dsPIC	STMicro STM32
Core / Speed	**56800EX Up to 100MHz**	C28x Up to 80MHz	dsPIC33F/E Up to 70MHz	**CortexM4 Up to 168MHz**
Data Types	**Integer & Fractional**	Integer	**Integer & Fractional**	Integer
Buses	3 address / 4 data	3 address / 3 data	3 address / 4 data	3 (I-bus/D-bus/S-bus)
Memory Maps	**Separate program & data**	Unified program and data	**Separate program & data**	Unified program and data
Pipeline Depth	**8**	**8**	3	3
Math Operations per Instruction	**6**	4	**6**	5
Accumulators	**4 ACCs (36 bits)**	1 ACC (32 bits)	2 ACCs (40 bits)	**N/A (0-8 reg)**
DMA	Up to 4-ch	Up to 6-ch	Up to 15-ch	Up to 16-ch
Interrupt Controller	Hardware Priority **Fast ISR**	**No Hardware Priority**	Hardware Priority	Hardware Priority
Architecture Advantages	**Intermodule Crossbar Switch, Nested Interrupts (no need for CLA)**	**CLA, VCU, FPU**	**Peripheral Pin Select (PPS) for pin function remap**	**ART Accelerator, FPU, Multi-level AHB bus matrix**
Flash	Up to 288KB TFS 90nm	**Up to 256KB + 2KB OTP Requires Paging**	Up to 536KB	Up to 1MB +512B OTP Multiple Incompatible Technology Nodes
Cache	**Yes**	No	No	**Yes (ART Accelerator)**
RAM	**Dual Port**	Single Port	Single Port	Single Port
EEPROM	**Yes, up to 2KB**	No	No	No
Memory Corruption Protection	**Yes – memory resource protection**	No	No	**Yes – memory protection unit**

Control Law Processor - PID Controller

(Proportional-Integral-Derivative)

- *Continuous (Analog) Expression*



No Flexibility to respond to different loads

Competitors can copy

$$e(t) = Xi(t) - Xf(t) \quad \text{----- (1)}$$

$$M(t) = Kp*e(t) + Ki*\int e(t)dt + Kd * \frac{d}{dt} e(t) \quad \text{----- (2)}$$

Where -- e(t): Error signal; Kp: Proportional Gain; Ki: Integral Gain; Derivative Gain

- *Difference (digital) Expression*

$$m(n) = Kp \times e(n) + Ki \times \sum_{i=0}^{n} e(i) \times \Delta t + Kd \times \frac{e(n) - e(n-1)}{\Delta t} \quad \text{- (3)}$$

Software Flexibility

Not easy to copy

$$m(n) = m(n-1) + Kp \times [e(n)-e(n-1)] + Ki \times e(n) \times \Delta t + Kd \times \left[\frac{e(n) - e(n-1)}{\Delta t} - \frac{e(n-1) - e(n-2)}{\Delta t}\right] \quad (4)$$

Math required includes 5 Mul/Acum – Freescale DSC can accomplish in 5 cycles
CortexM4 takes 30 cycles - 6 times slower

Freescale DSC Measure & Control vs. Competitors

Freescale Value Proposition

- High Performance on-chip Peripherals - A high level of on-chip integration to reduce software overhead and total BOM cost.

Attribute	Freescale DSC	TI Piccolo	Microchip dsPIC	STMicro STM32
Analog CMP response time	25ns	30ns	20ns	**None**
CMP	4 w/6-bit DAC	3	4	**None**
DAC	**Up to 2x12-bit w/ Hardware Slope Compensation**	3x10-bit	4x10-bit	2x12-bit
ADC Blocks	2 (w/ one S&H for each ADC) 1 w/ **High Input Impedance (enabling lower cost ext. Op Amp & Cap)**	1 (w/dual S&H)	2 (w/up to five S&H for one SAR, one S&H for another SAR)	3 (w/ dual S&H for regular group and injected group in each ADC)
ADC conversion	Up to 300ns @ 12-bit	Up to 217ns @ 12-bit	Up to 500ns @ 10-bit 2,000ns @ 12-bit	417ns @ 12-bit
ADC channels	16-ch 12-bit 8ch 16-bit	16-ch 12-bit	32-ch 10-/12-bit	24-ch 12-bit
Temp Sensor	Yes	Yes	**No**	Yes
PWM	**Total 16-ch / 8-ch with 312.5ps resolution**	**Total 19-ch / 8-ch with 150ps resolution**	Total 18-ch with1.04ns resolution	Total 14-ch with 5.95ns resolution
PWM Features	**Multiple time base, enhanced capture functionality** **Edge locked loop for stable PWM edge control** **Fractional clock calculation and tracking, effectively reducing the software workloads.** **submodule to submodule synchronization has no delay**	Multiple time base, PWM chopper Open loop delay, no stable edge over temp Fractional clock calculation is handled manually 2 clock delay to sync modules	Multiple time base, capture and chopper functionality	Capture functionality
Timer	8-ch 16-bit QTimer / 2-ch 16-bit PIT / 2-ch 16-bit PDB	3-ch 32-bit CPU timer	9-ch 16-bit timer / 1-ch RTCC	12-ch 16-bit Timer / 1-ch RTC
I/O	**5V Tolerance on all I/O**	**Only 3v**	5V Tolerance on digital I/O	**5V Tolerance on all I/O**

Freescale DSC Power Consumption vs. Competitors

Freescale Value Proposition

- Low Power - The most compelling uA/MHz performance available today for applications requiring arithmetic functions. Low power similar to CortexM0 & MSP430, Higher performance than the CortexM4 and C2000.

Attribute	Freescale DSC MC56F82748 (100Mhz, 32bit)		Attribute	TI Piccolo TMS320F28069 (90Mhz, 32bit)		TI Piccolo TMS320F28035 (60Mhz, 32bit)		Attribute	Microchip dsPIC dsPIC33FJ16GS504 (40Mhz, 16bit)		Microchip dsPIC dsPIC33EP64MC206 (60Mhz, 16bit)	
	IDD	IDDA		IDD	IDDA	IDD	IDDA		IDD	IDDA	IDD	IDDA
Full Run Mode With MAC operation in while loop	25.18mA	8.9mA	Full RUN Mode With MAC operation in while loop	174mA	15.5mA	114mA	12.7mA	Full Run Mode With MAC operation in while loop	100mA	38mA	38mA	2.5mA
WAIT mode	17.3mA	0.4uA	IDLE mode	6.16mA	8.2uA	5.09mA	8.2uA	Idle mode	57mA	20mA	17mA	2.5mA
STOP mode	4.94mA	0.04uA	STANDBY mode	3.36mA	8.2uA	2.69mA	8uA					
VLSTOP	500uA	0.01uA	HALT mode	473uA	8.2uA	1.15mA	8uA	Power Down mode	300uA		100uA	
ADC	12bit		ADC	12bit		12bit		ADC	10bit		10bit/12bit	
PWM resolution	320psec		PWM resolution	150psec		150psec		PWM resolution	1.04nsec		7.14nsec	
RUN, WAIT, STOP, LPSTOP,VLPSTOP, LPWAIT, VLPWAIT			RUN, IDLE, STANDBY, HALT					RUN, IDLE, DOZE, SLEEP				

Example code:

```
0x00000000  0xE584          move.w    #4,Y0

0x00000001  0xF754          move.w    X:(R0)+N,Y1
0x00000002  0xF457          move.w    X:(R3)+N,X0
0x00000003  0x7618          macr      Y1,X0,A      X:(R0)+,Y1      X:(R3)+,X0
0x00000004  0x7476          lsrac     Y1,Y0,A
0x00000005  0xD0C10003      move.w    A,X:(R1+3)
0x00000007  0xE700          nop
0x00000008  0xE1540001      jmp       0x000001
```

DSC 56800EX Hawk V3 Core

DSP56800E Core Features

CPU	MIPS	# Interrupt Priorities	Registers	Data Types	Program Memory Adr Space	Data Memory Adr Space	Technology
DSP56800E	Up to 200MIPS	5	7 Data 8 Address	8-bit, 16-bit 32-bit	4 MB	32 MB	Fully Synthesizable and Scanable

56800/E MCU Functionality

True Software
Stack and Pointer

16-bit Program Word

20 Addressing Modes and Atomic
Read-Modify-Write Instructions

General Purpose Register Files and Orthogonal
Instructions to Data and Address Register Files

Full Set of Bit and Bitfield Manipulation
Instructions and 16- and 32-bit Shifting

Superfast Interrupt

56800/E DSP Functionality

Multiplier - Accumulator (MAC)
Single And Dual Parallel Move Instructions

No Overhead Hardware Looping
Nested Looping Capability

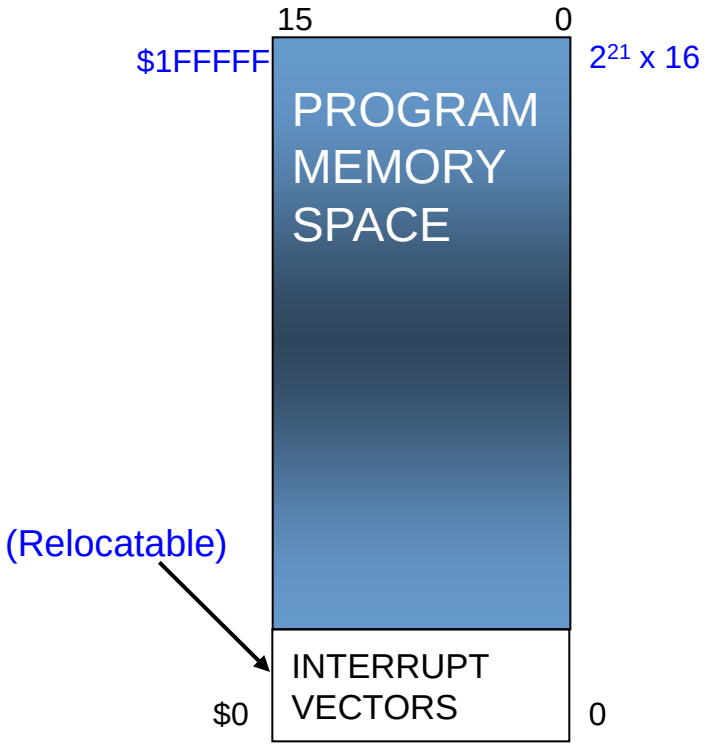
Modulo arithmetic (For Circular Buffers)
Integer and Fractional Arithmetic Support

Nested Interrupt with HW priority
Fast Interrupt Support

Program and Data Memories

Program (4 MB)

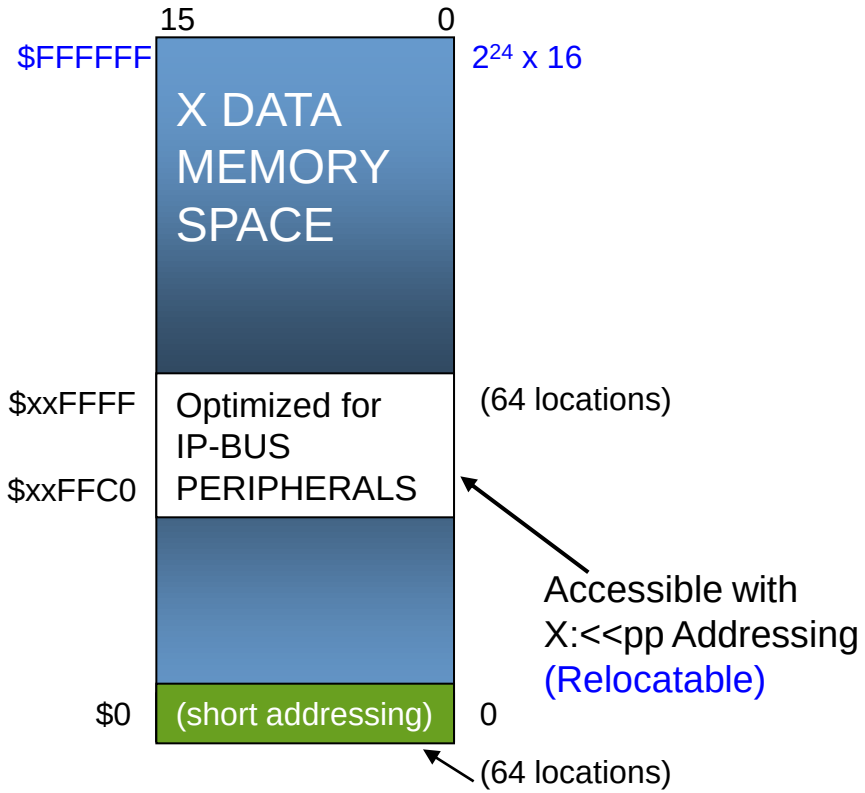
"P:"



=> 16-Bit Accesses Only

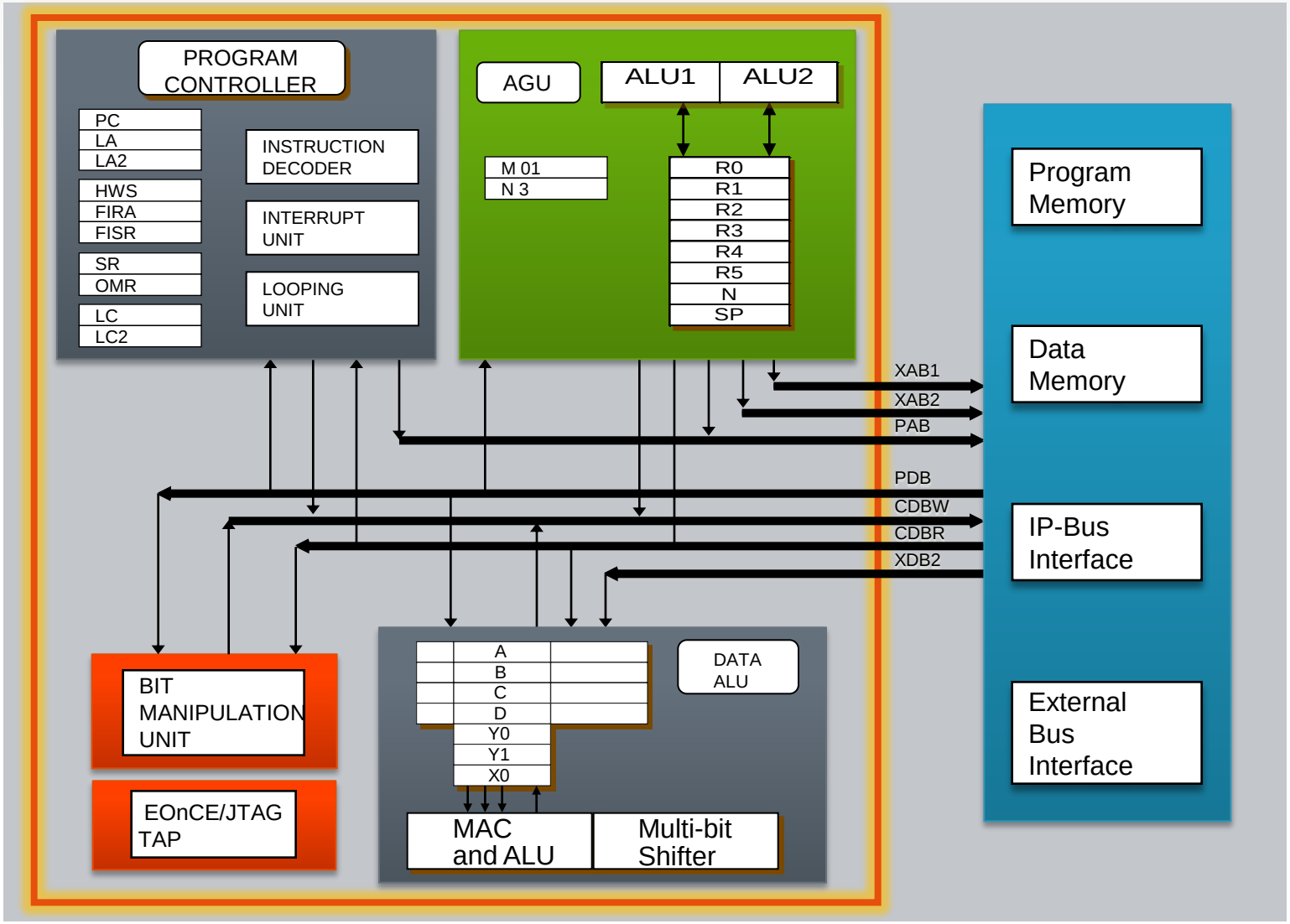
Data (32 MB)

"X:"



=> 8, 16, 32-Bit Accesses

DSP56800E Core Architecture



Instruction Fetch:

PAB - 21 bits
PDB - 16 bits

1st Data Access:

XAB1 - 24 bits
CDBR - 32 bits
CDBW - 32 bits

2nd Data Access:

XAB2 - 24 bits
XDB2 - 16 bits

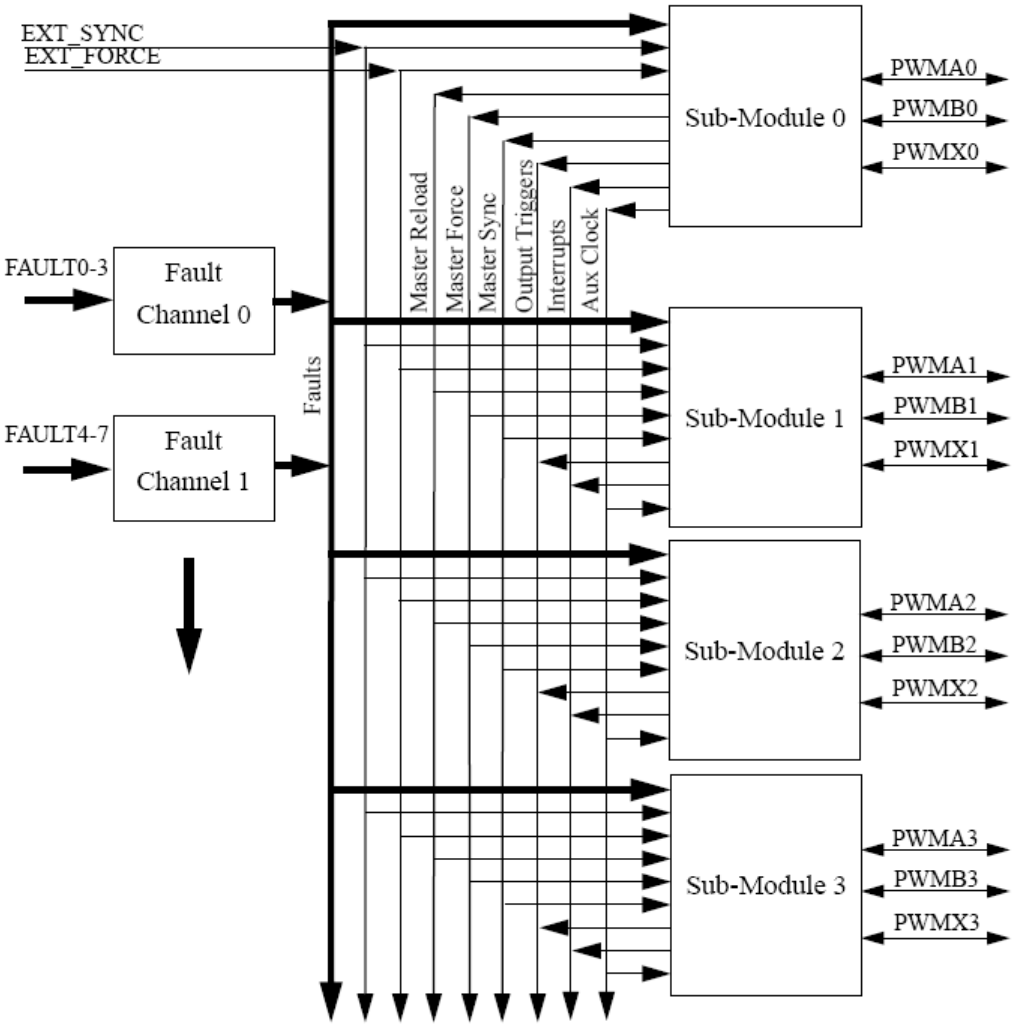
Operations Performed:

1st - PAB / PDB
2nd - XAB1 / CDBR-CDBW
3rd - XAB2 / XDB2

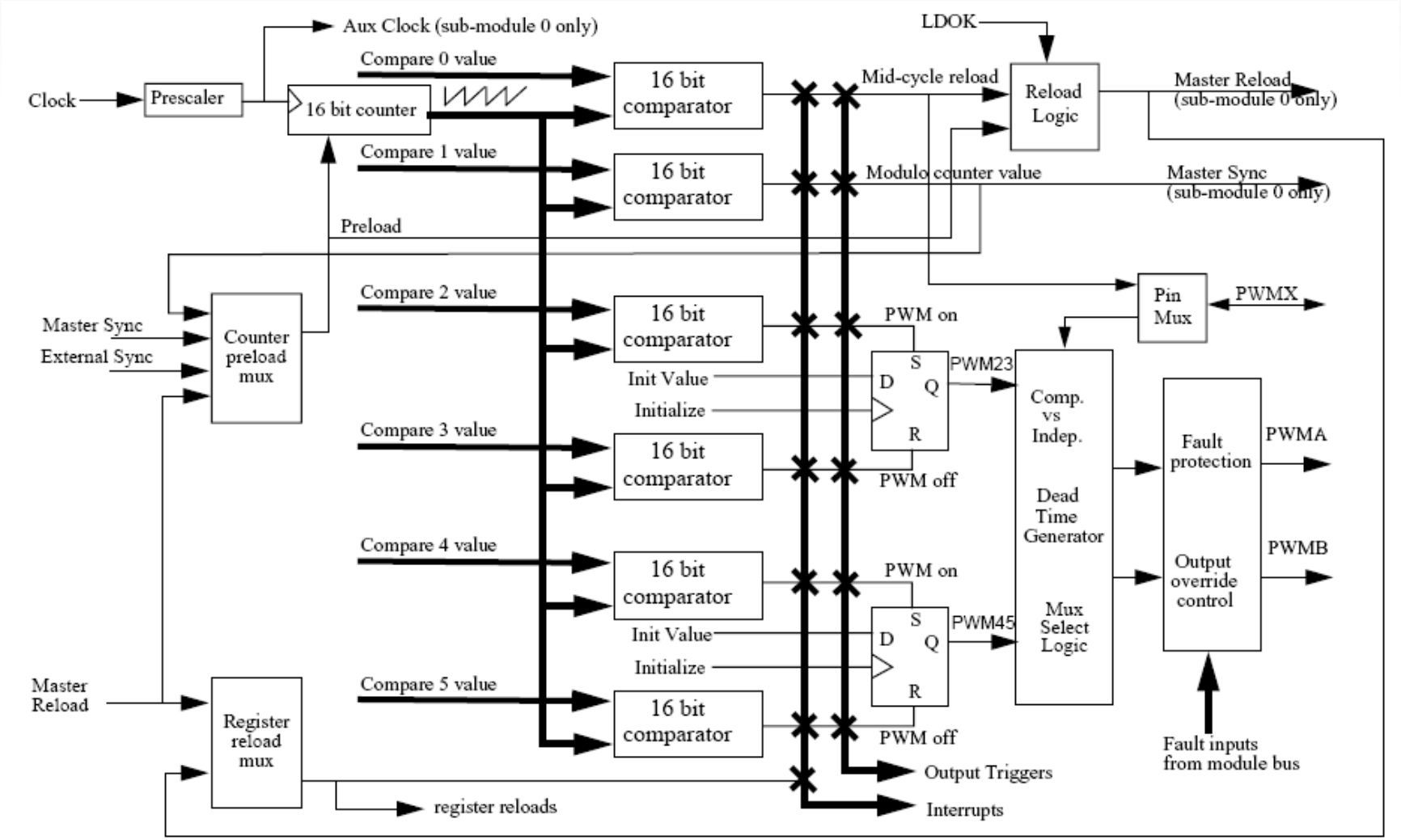
Pulse Width Modulator (PWM)

enhanced FlexPWM Module

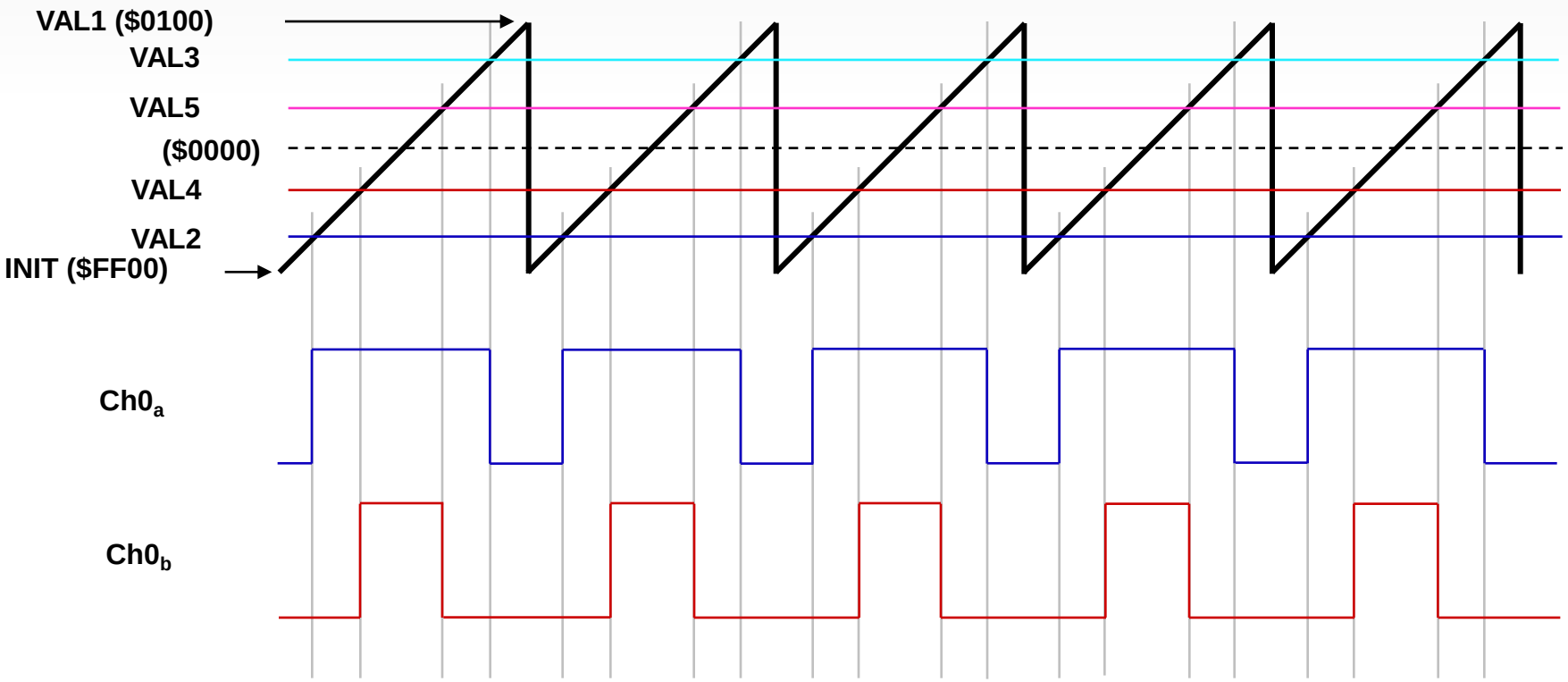
The eFlexPWM architecture is configurable, up to 4 sub-modules (shown)



eFlexPWM Sub-Module Detail

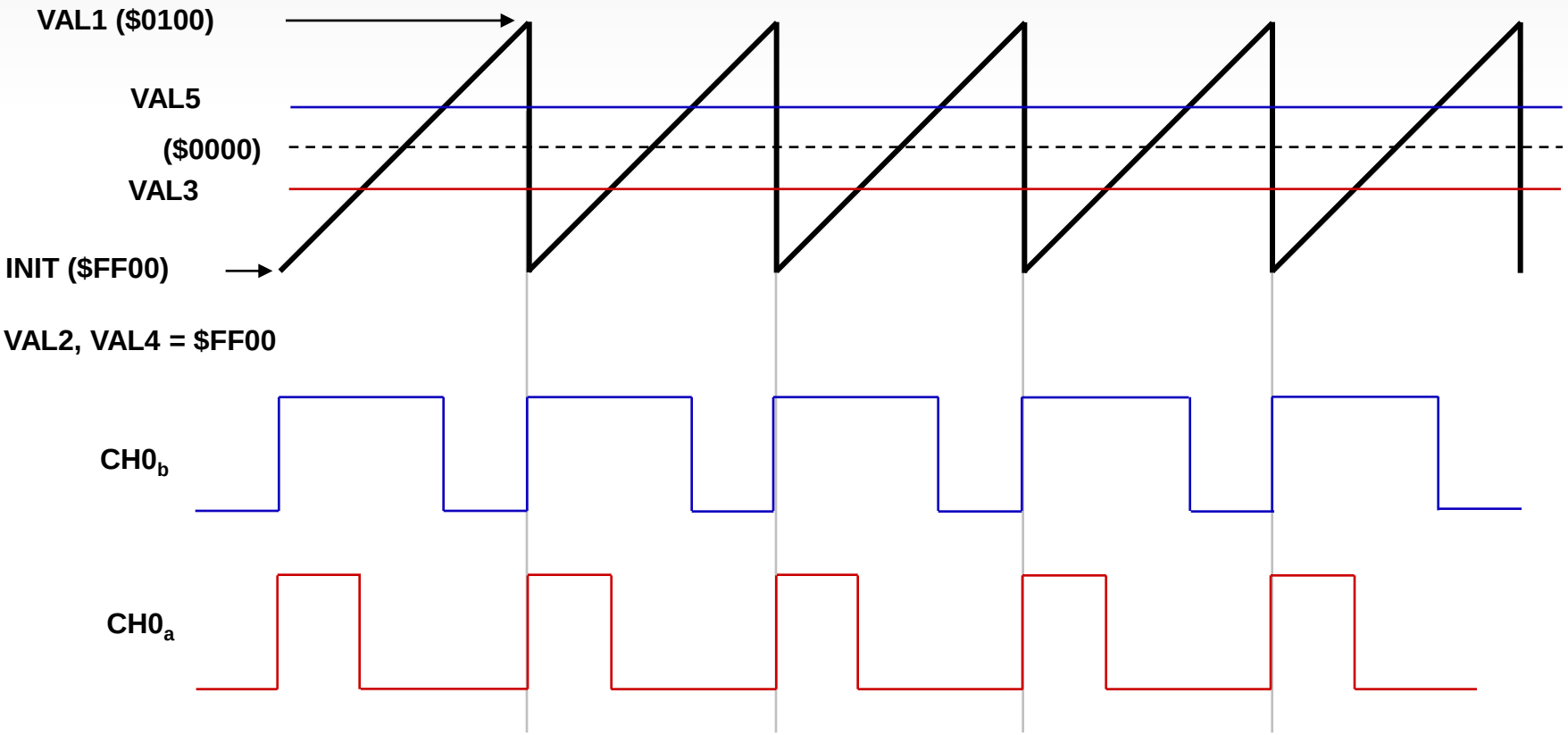


Center Aligned Example



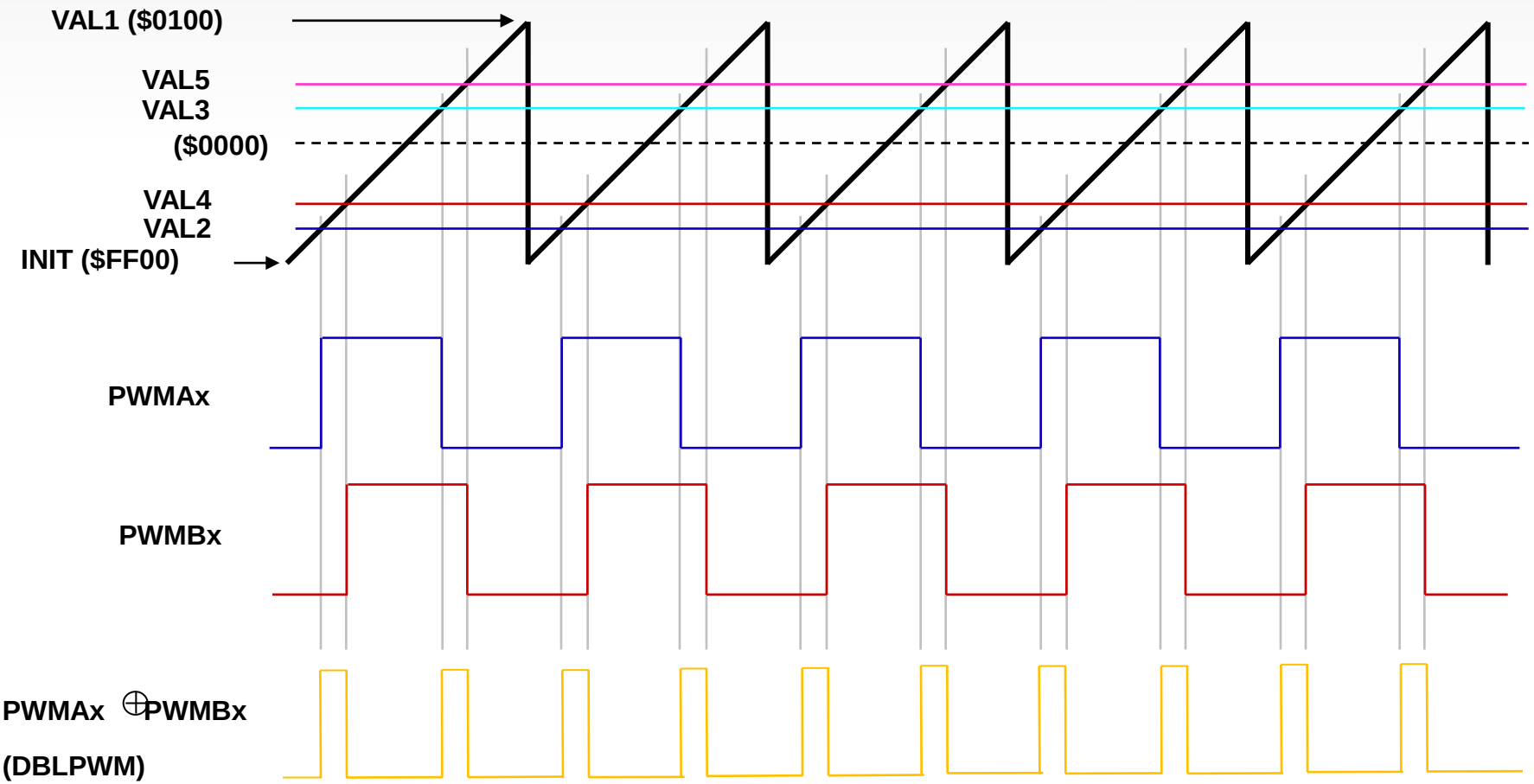
When the Init value is the signed negative of the Modulus value, the PWM module works in signed mode. Center-aligned operation is achieved when the turn-on and turn-off values are the same number, but just different signs.

Edge Aligned Signed Mode Example



All PWM-on values are set to the init value, and never changed again.
Positive PWM-off values generate pulse widths above 50% duty cycle.
Negative PWM-off values generate pulse widths below 50% duty cycle.
This works well for bipolar waveform generation.

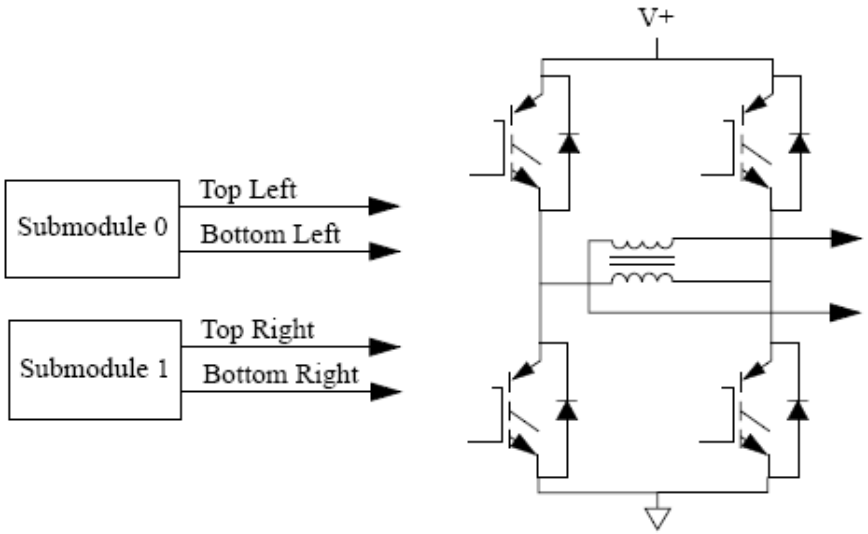
Phase Shifted & Double Switching PWMs

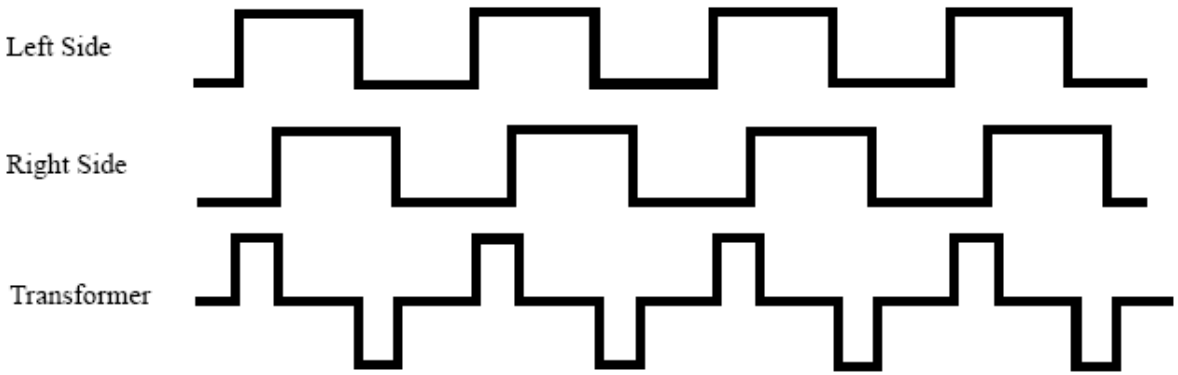


In this example, both PWMs have the same duty-cycle. However, the edges are shifted relative to each other by simply biasing the compare values of one waveform relative to the other.

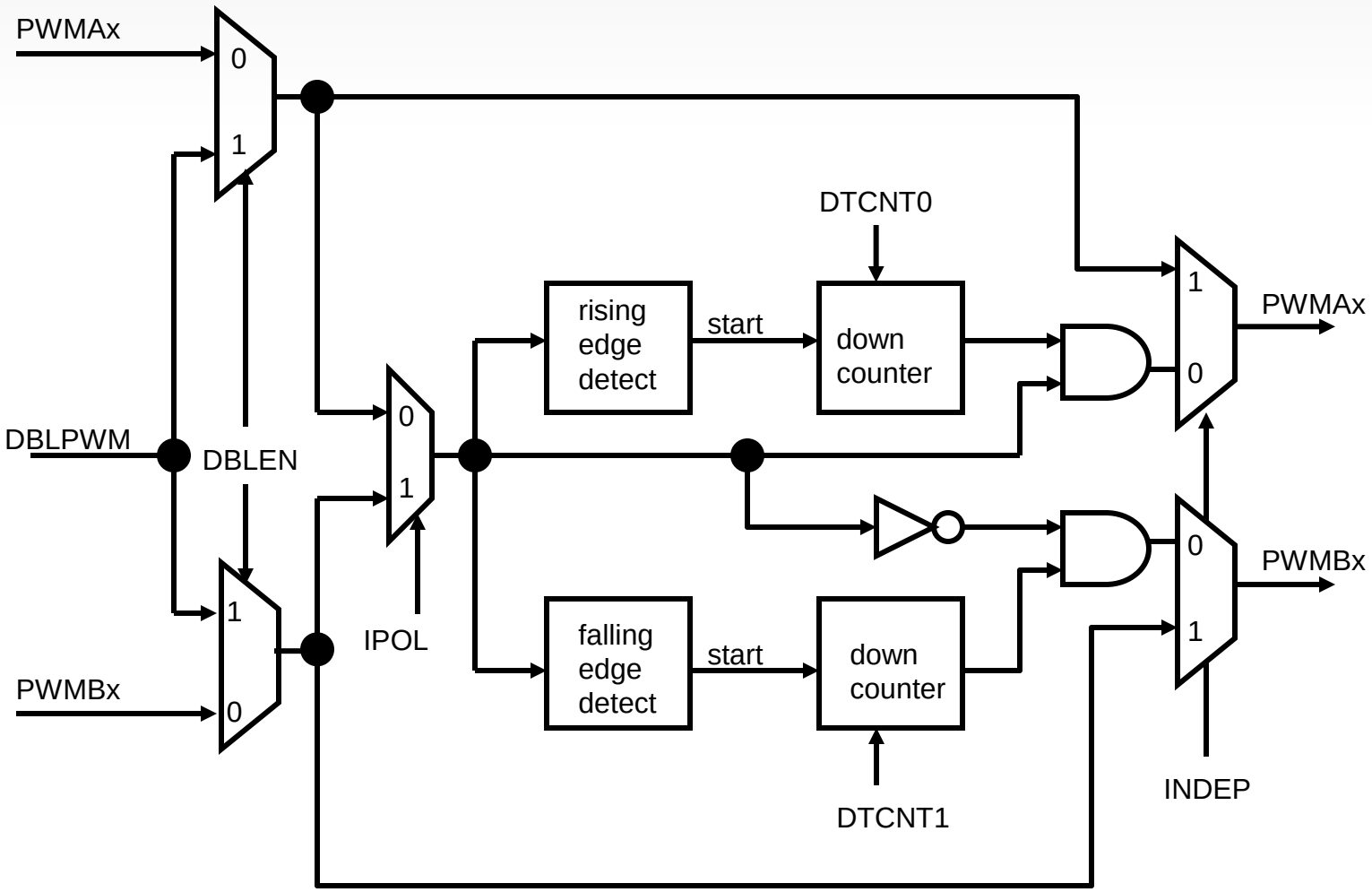
Alternatively, if the waveforms are generated by different sub-modules, the waveforms can be shifted by simply changing the Init value of one sub-module relative to the other.

Application of Phase Shifted & Double Switching PWMs





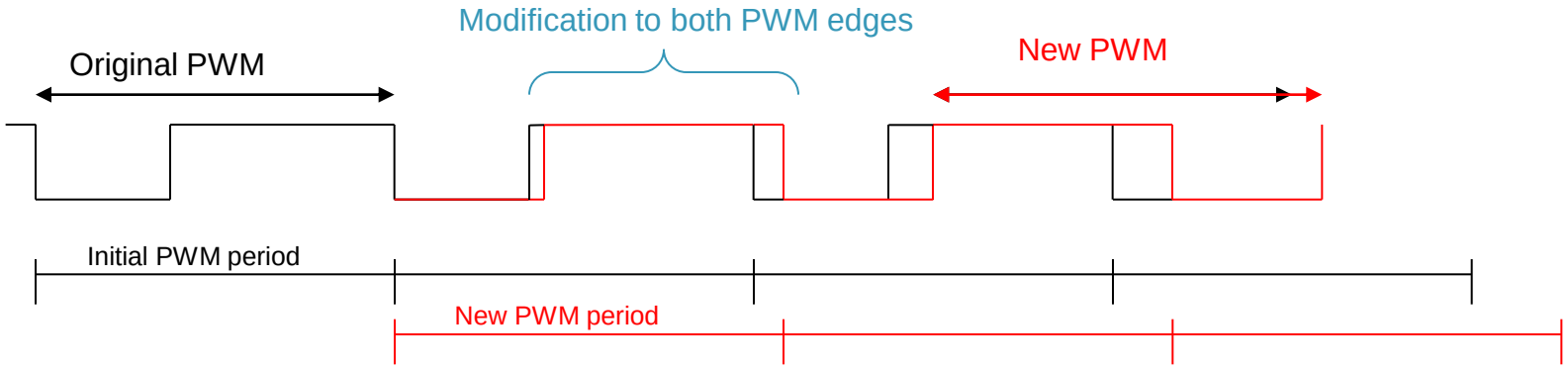
Dead Time Insertion



Challenge of Controlling Resonate Converter

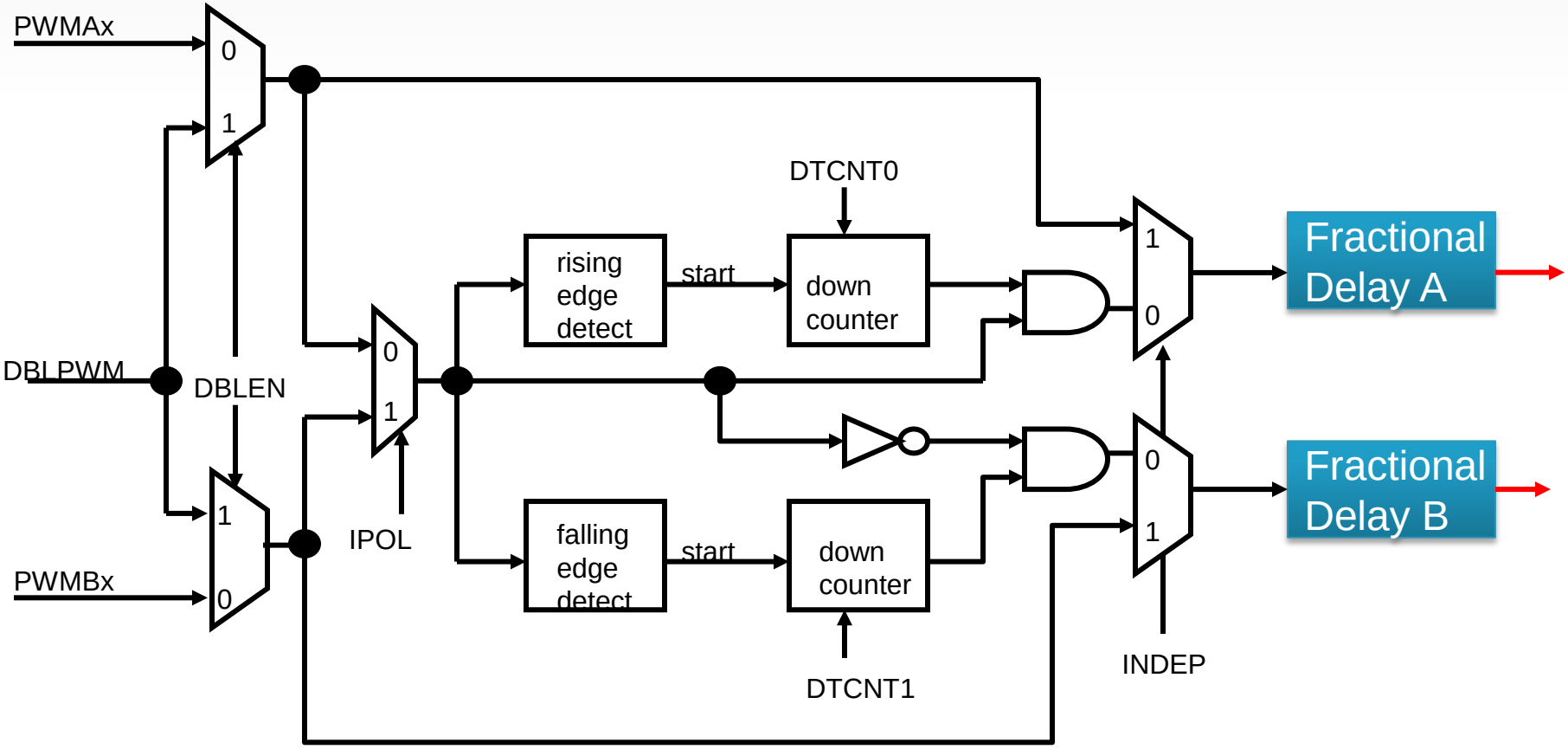
- **Challenge:**
  - Wide range of PWM switching frequency from 100KHz up to 1Mhz
  - Need to make a change to the PWM period without changing the duty cycle for up to 4 channels of PWM within one period of the existing PWM
  - PWM period change must be in a few nanosecond

- **Solution:**
  - High speed digital PWM plus Analog edge delay
  - PWM duty cycles are calculated by high speed controller
  - Special circuit is used to automatically increment the PWM period by repositioning edges



PWM period requires small incremental adjustment

FlexPWM Detail Showing Inclusion of Fractional Delays



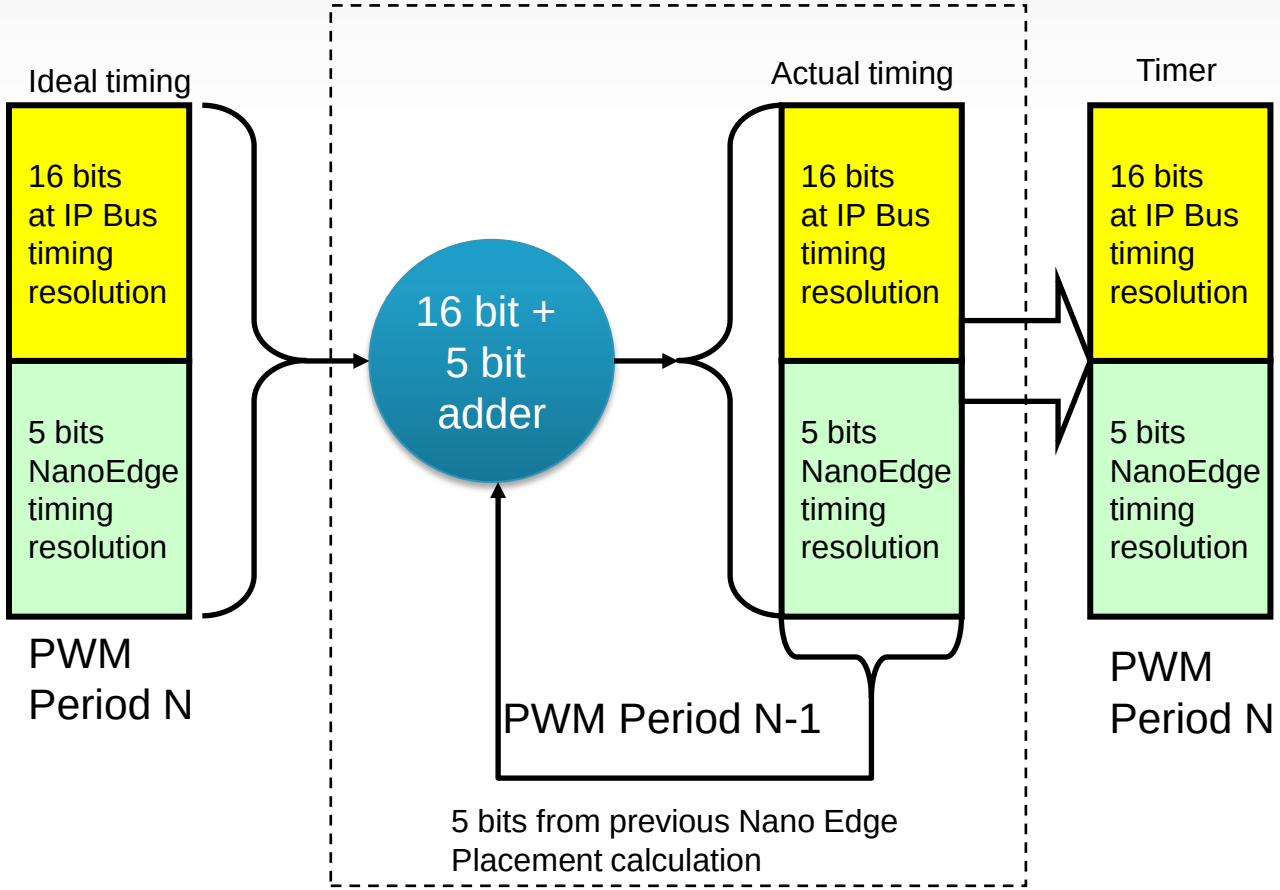
INDEP=1: Fractional Delays A & B are separate

INDEP=0 & IPOL=0: Delay B (dependent variable) = Inverse Delay A (controlling) => $T_{FB} = T_{RA}$ AND $T_{RB} = T_{FA}$

INDEP=0 & IPOL=1: Delay A (dependent variable) = Inverse Delay B (controlling) => $T_{FA} = T_{RB}$ AND $T_{RA} = T_{FB}$

Digital Adder for Frequency Control

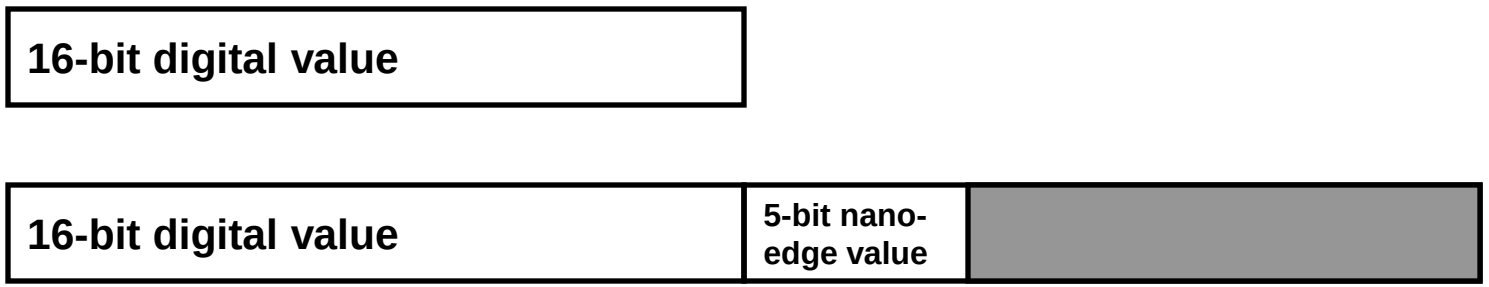
- Need to calculate the next edge position for rising and falling edges within very short period.
- Software not fast enough so need hardware adder
- Diagram shows 21 bit adder to control both edges automatically setting new comparator values after each edge has been triggered



PWM reload times are restricted to 16-bit IP Bus timing (truncation of 21 bit value). Any residual left over from PWM period N-1 needs to be added back to period N.

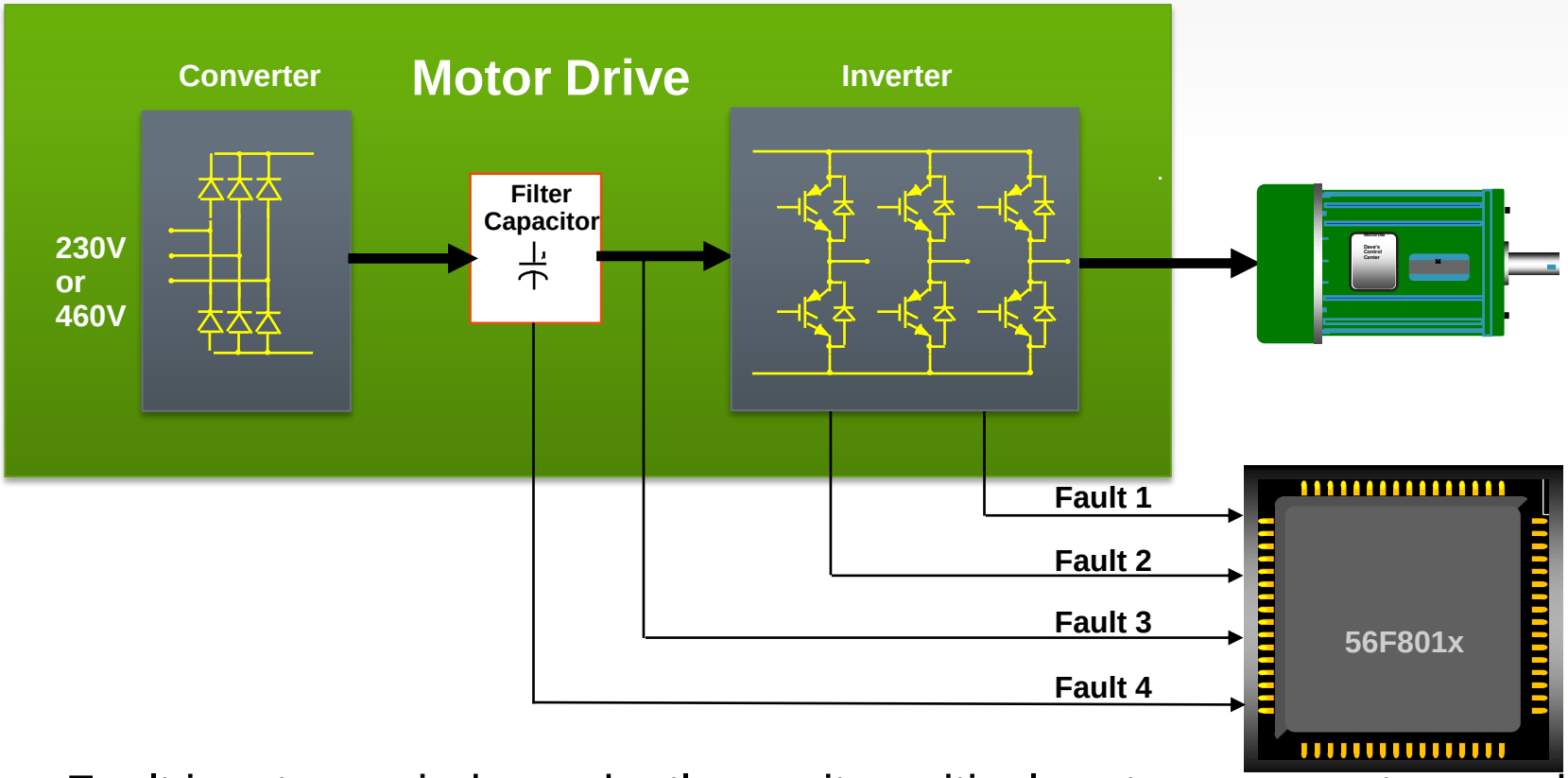
Nano-Edge Placer

- The Nano-Edge Placer allows us to control edge placement to sub-nanosecond resolution.
- The actual block is based uses a dual-slope method to calibrate individual time slices to fractions of a digital clock period.
- U.S. Patent # 7288977: High resolution pulse width modulator
- *<include reference to Martin & Pavels patent application>*
- When using the nano-edge placer, delay values change from 16-bit resolution to 21-bit resolution or better:



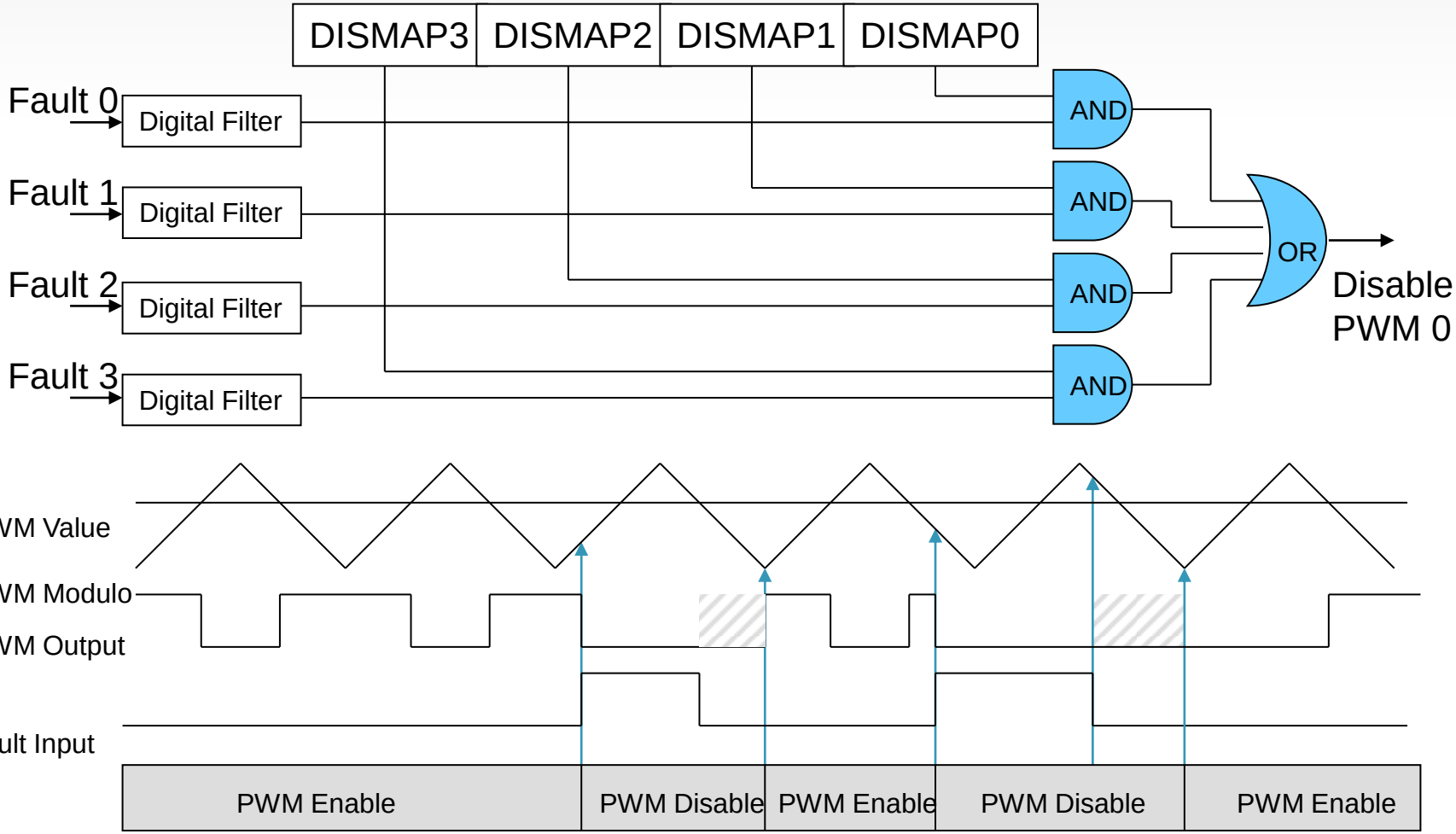
Include patent app from Roznov.

PWM – Multiple Fault Inputs



- Fault inputs can independently monitor critical system parameters, and generate an interrupt when asserted.
- Each input is mappable to immediately disable any or all PWMs
- Each input is programmable to allow Automatic or Manual PWM restart

PWM Fault Decode and Automatic Clearing

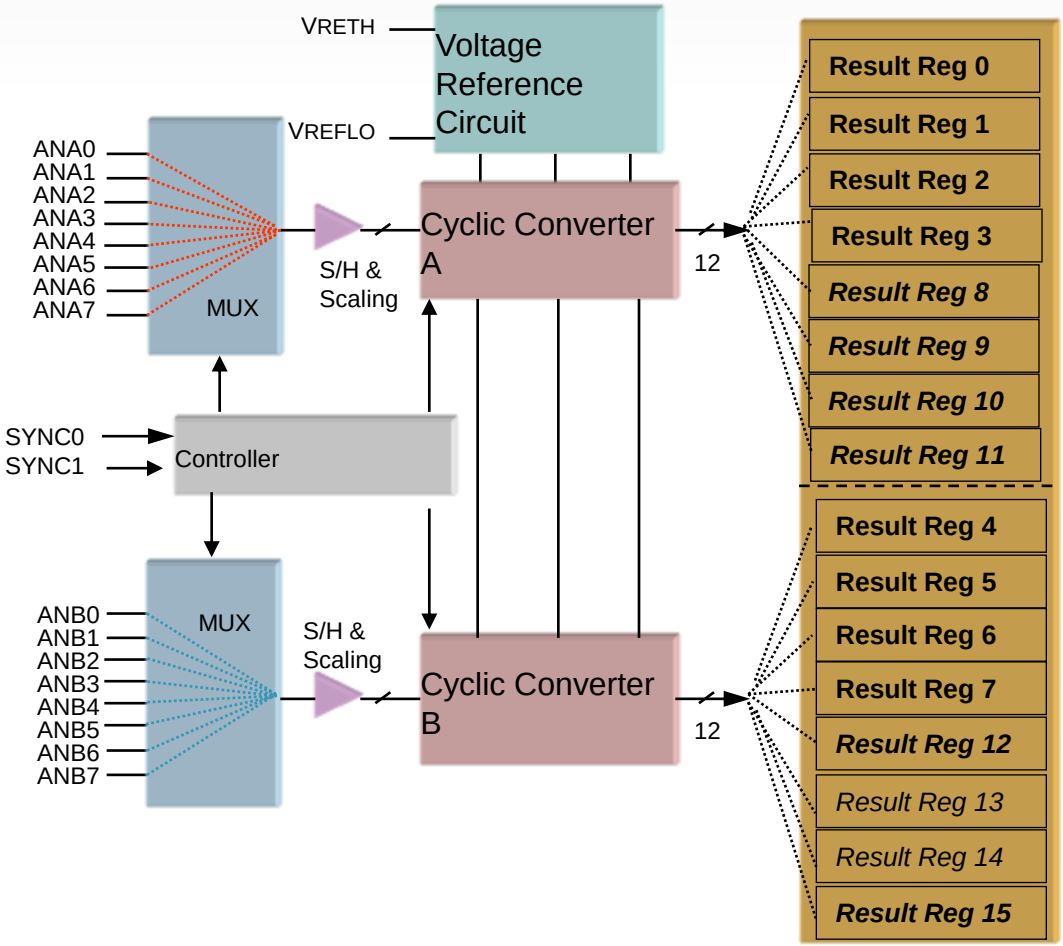


*When Fault logic returns to logic 0, the PWM restart at beginning of the next half cycle.

Peripheral Summary: High Speed ADCs

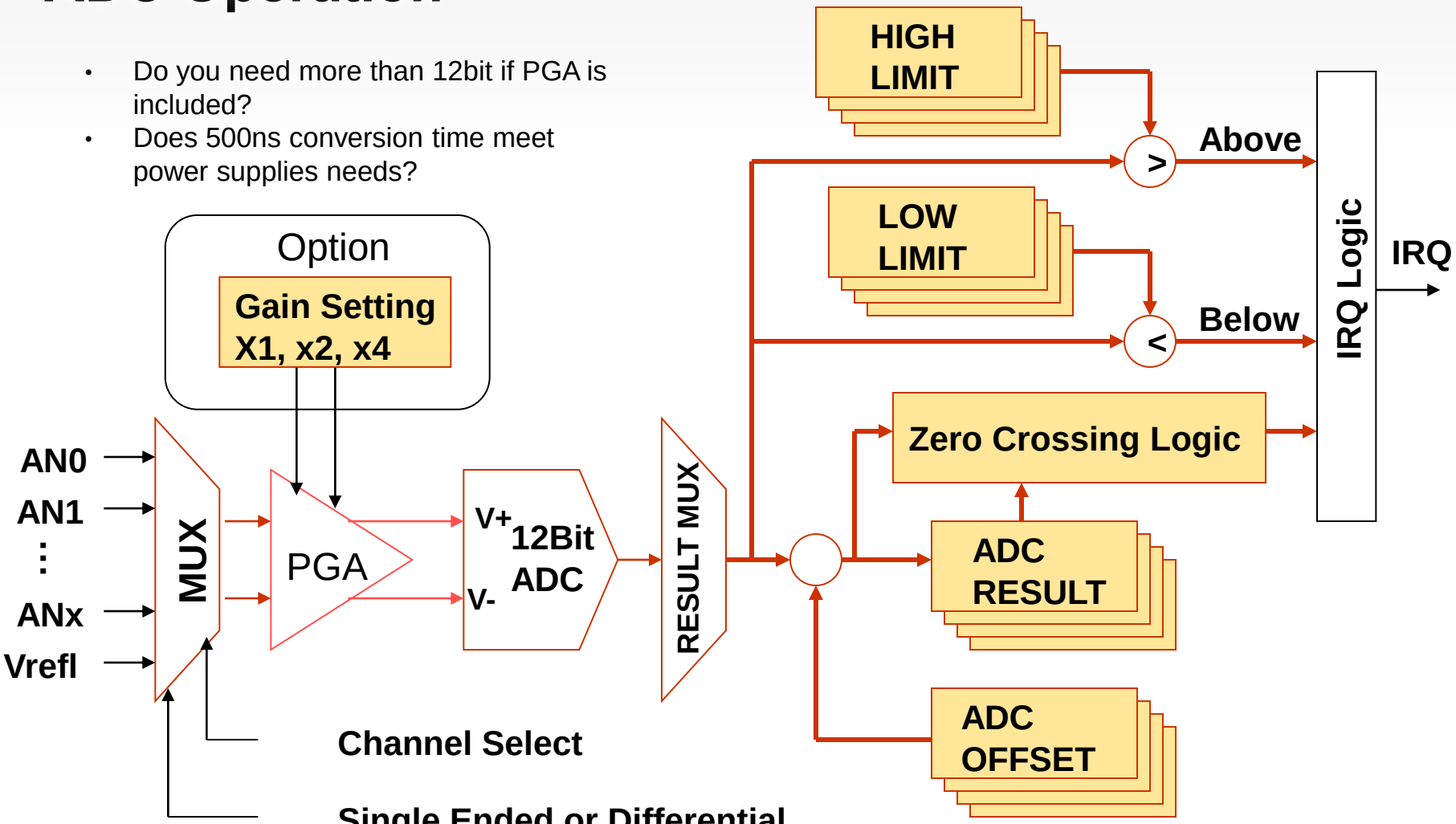
ADC Channel Scan Modes

- **Once**
  - The ADC starts to sample just one time whether you use the START bit or by a sync pulse. This mode must be re-armed by writing to the ADCR1 register again if you want to go capture another scan
- **Triggered**
  - Sampling begins with every recognized START command or sync pulse
- **Loop**
  - The ADC continuously take samples as long as power is on and the STOP bit has not been set
- **Sequential Mode**
  - Sequential will sample SampleN one after another. Channel ANAx are sampled by ADCA and Channel ANBx are sampled by ADCB
- **Parallel Mode**
  - Simultaneous: Parallel can sample SampleN from Group1 and SampleN
  - Independent:: ADCA and ADCB can operate independently. At end of scan of each ADC, they generate separate interrupt request.

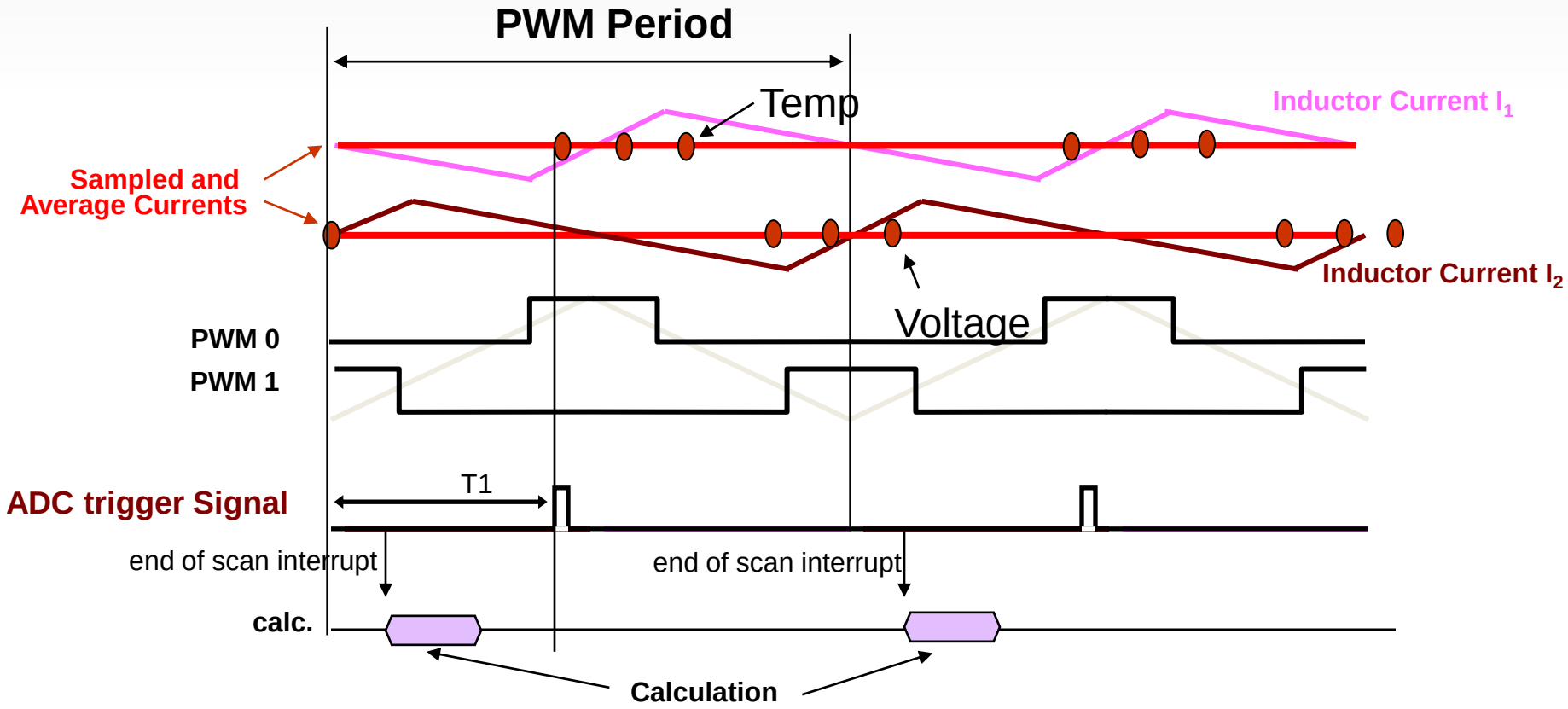


ADC Operation

- Do you need more than 12bit if PGA is included?
- Does 500ns conversion time meet power supplies needs?

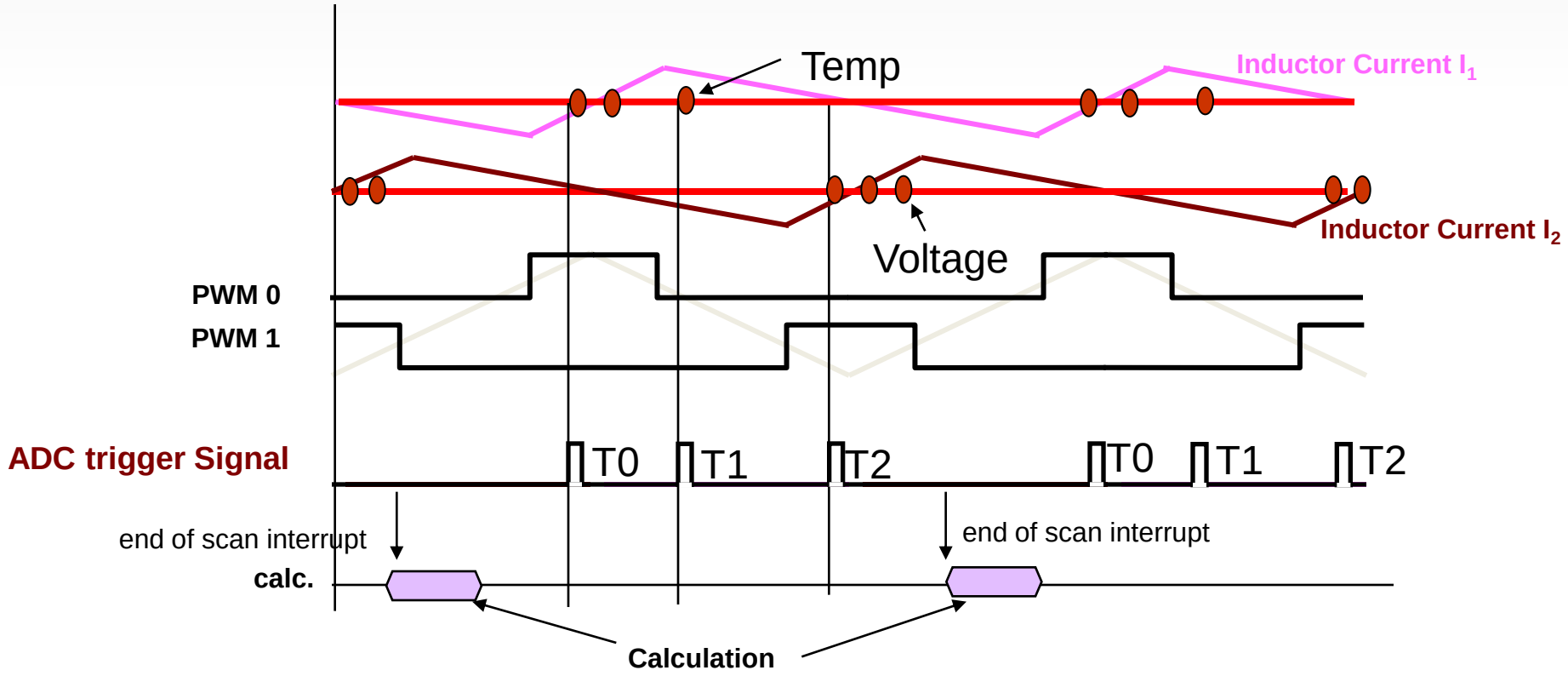


A/D Converters
PWM Synchronization Benefits



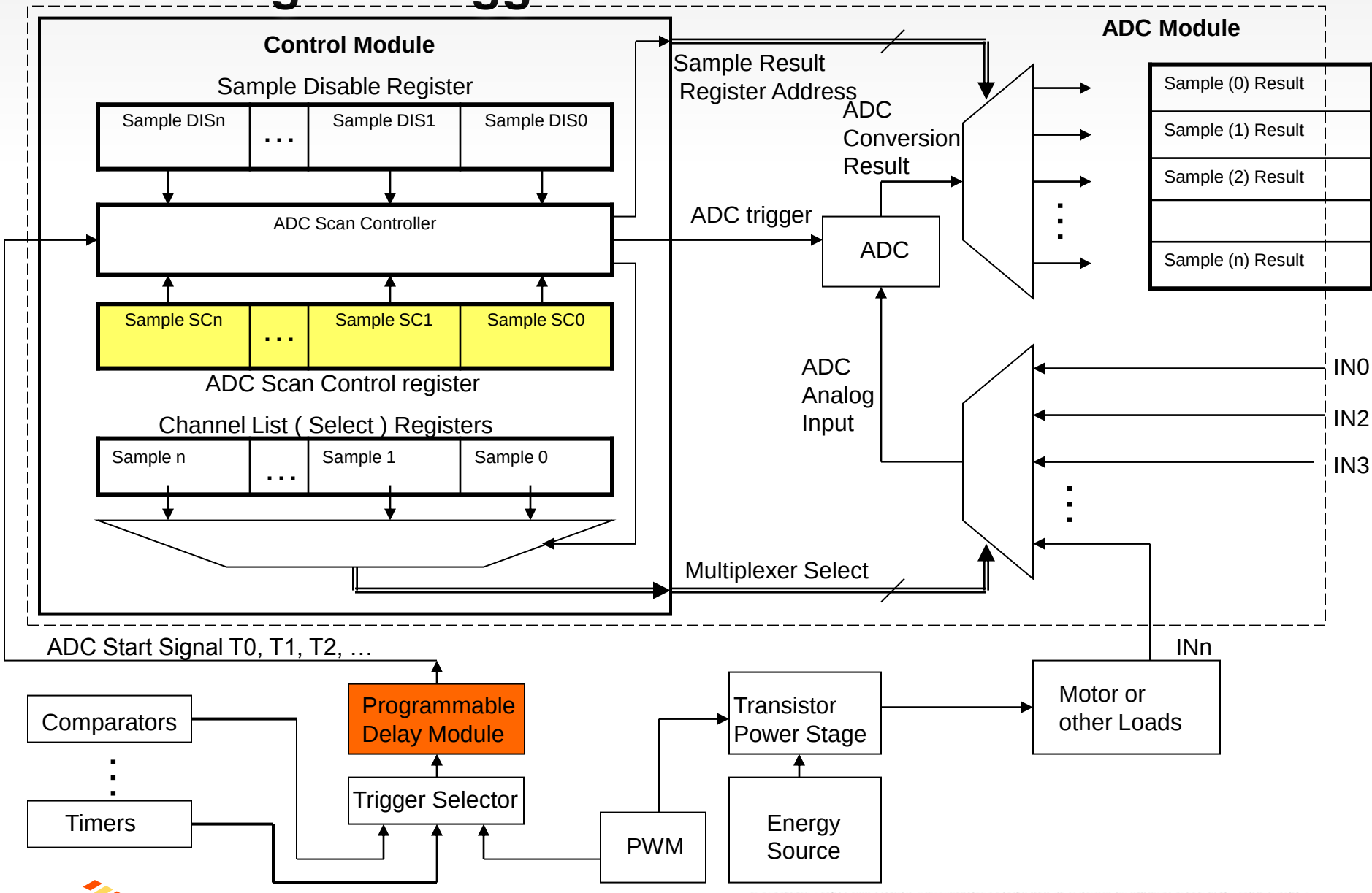
- ✓ ADC Sampling helps to filtering the measured current - antialiasing.
- ✓ Noise free ADC sampling when the power switch is not acting
- ✓ ADC sample is taken at middle of PWM pulse which is equal to average Current
  - But second phase samples are difficult to be located in middle of PWM Pulse

A/D Converters
Example Irregular Triggers

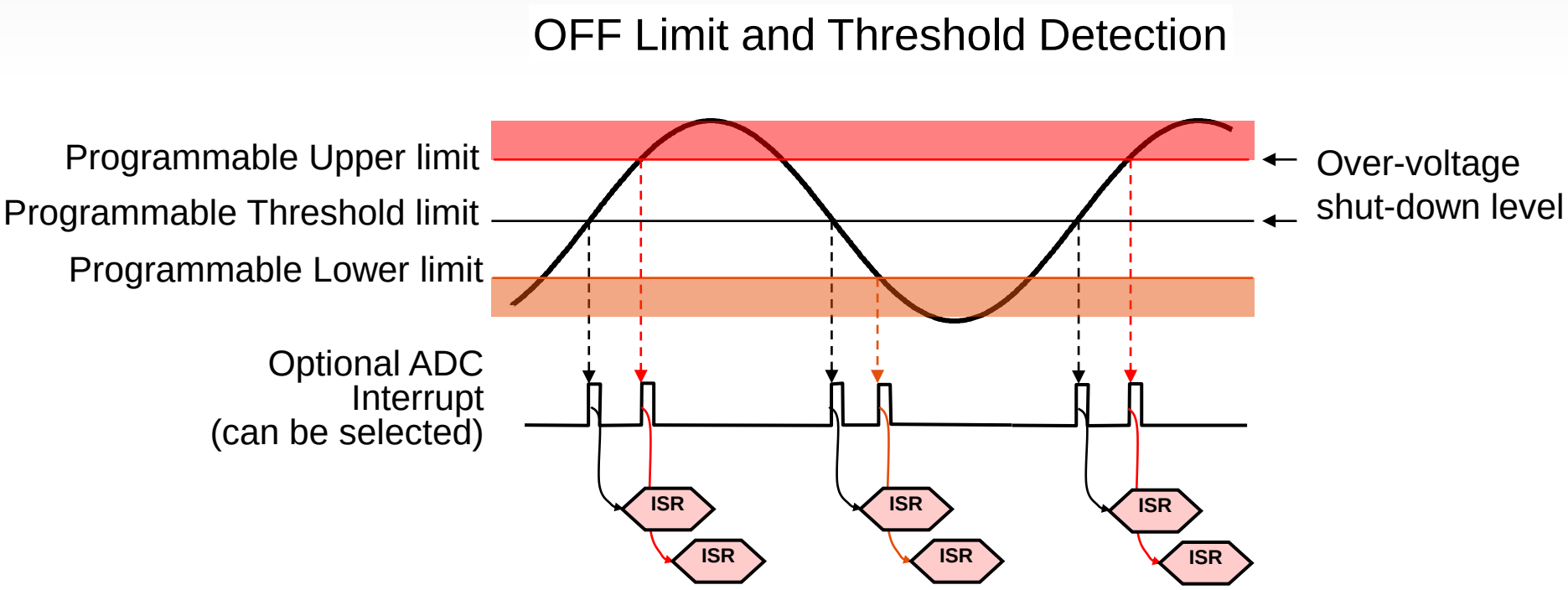


- ✓ Trigger 0 (T0) starts 1st conversion which ADC takes two conversions then wait next trigger
- ✓ Trigger 1 (T1) starts 2nd conversion which ADC takes one conversion then wait next trigger
- ✓ Trigger 2 (T2) starts 3rd conversion which ADC takes three conversions then generates INT

ADC Irregular Triggers

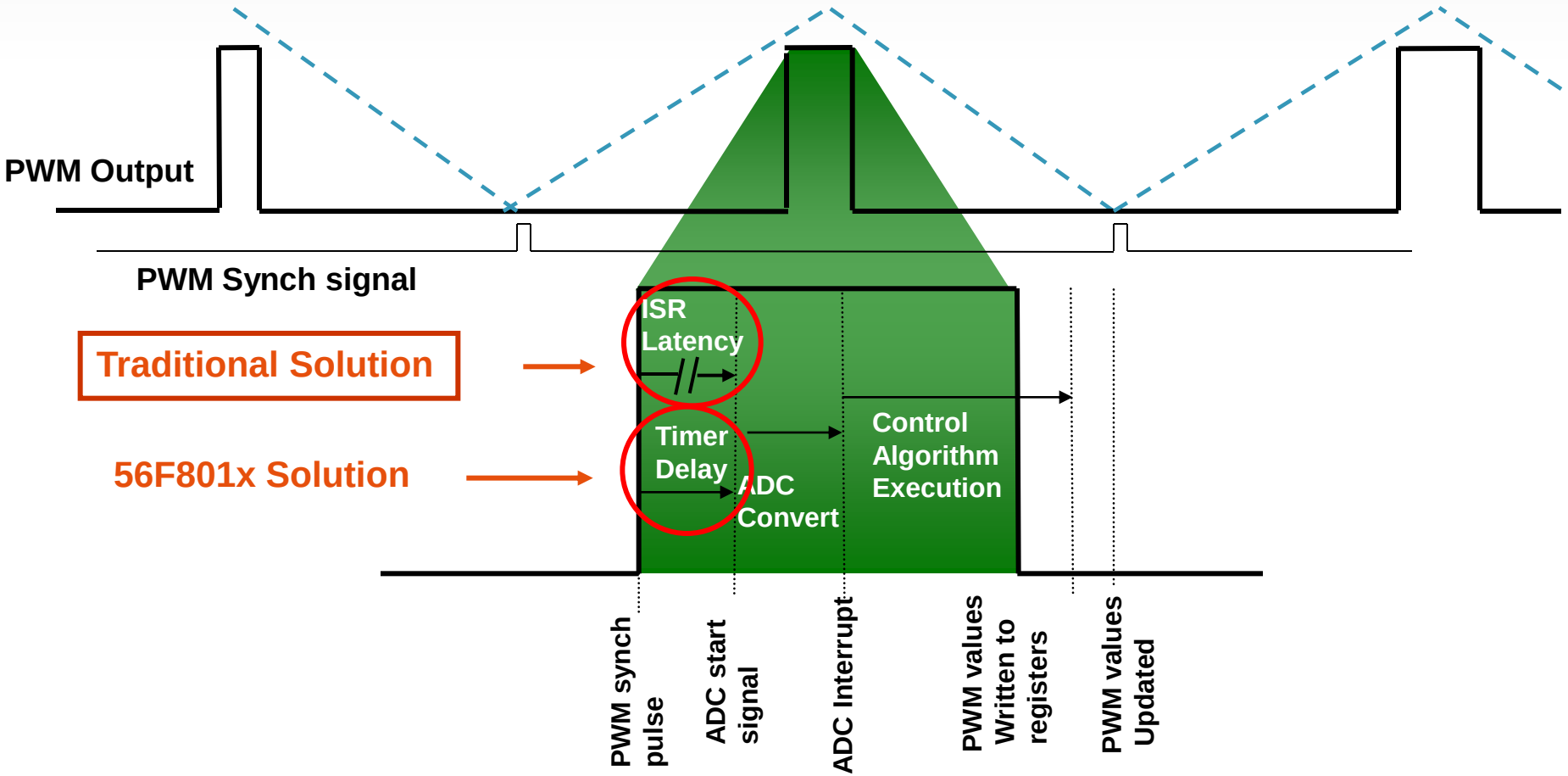


ADC Sampling Process

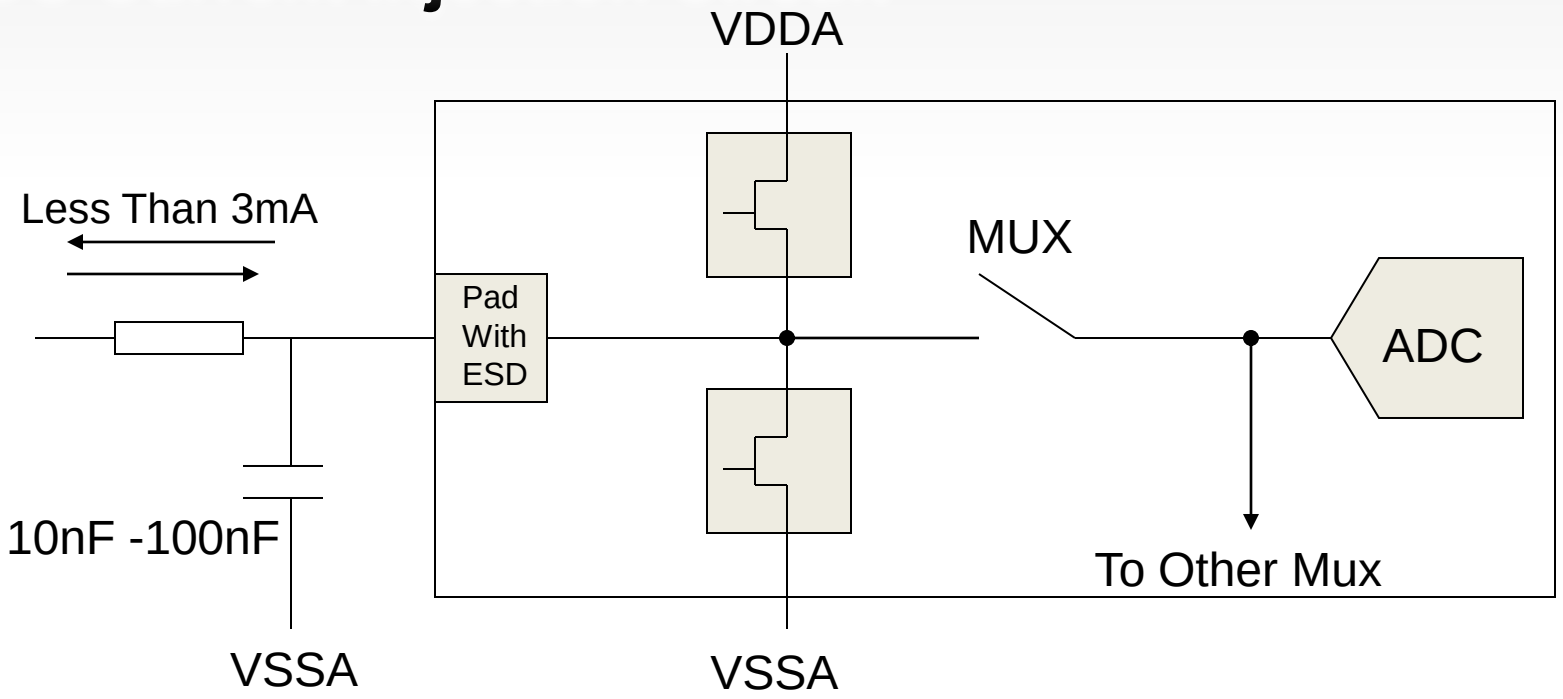


- The ADC can perform limit checking and zero crossing detection with NO CPU intervention.
- Each channel has its own upper, lower, and threshold comparators.

ADC Synchronization With The PWM

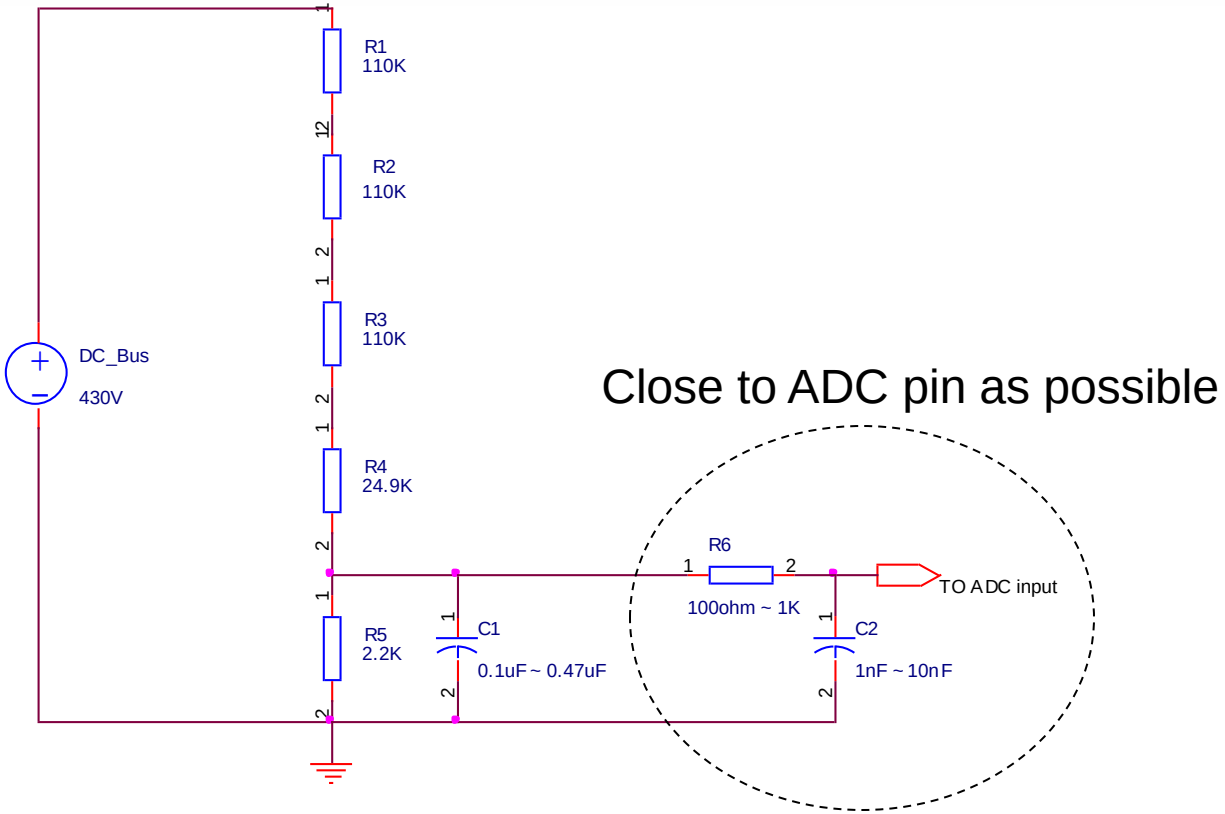


ADC Current Injection Circuit



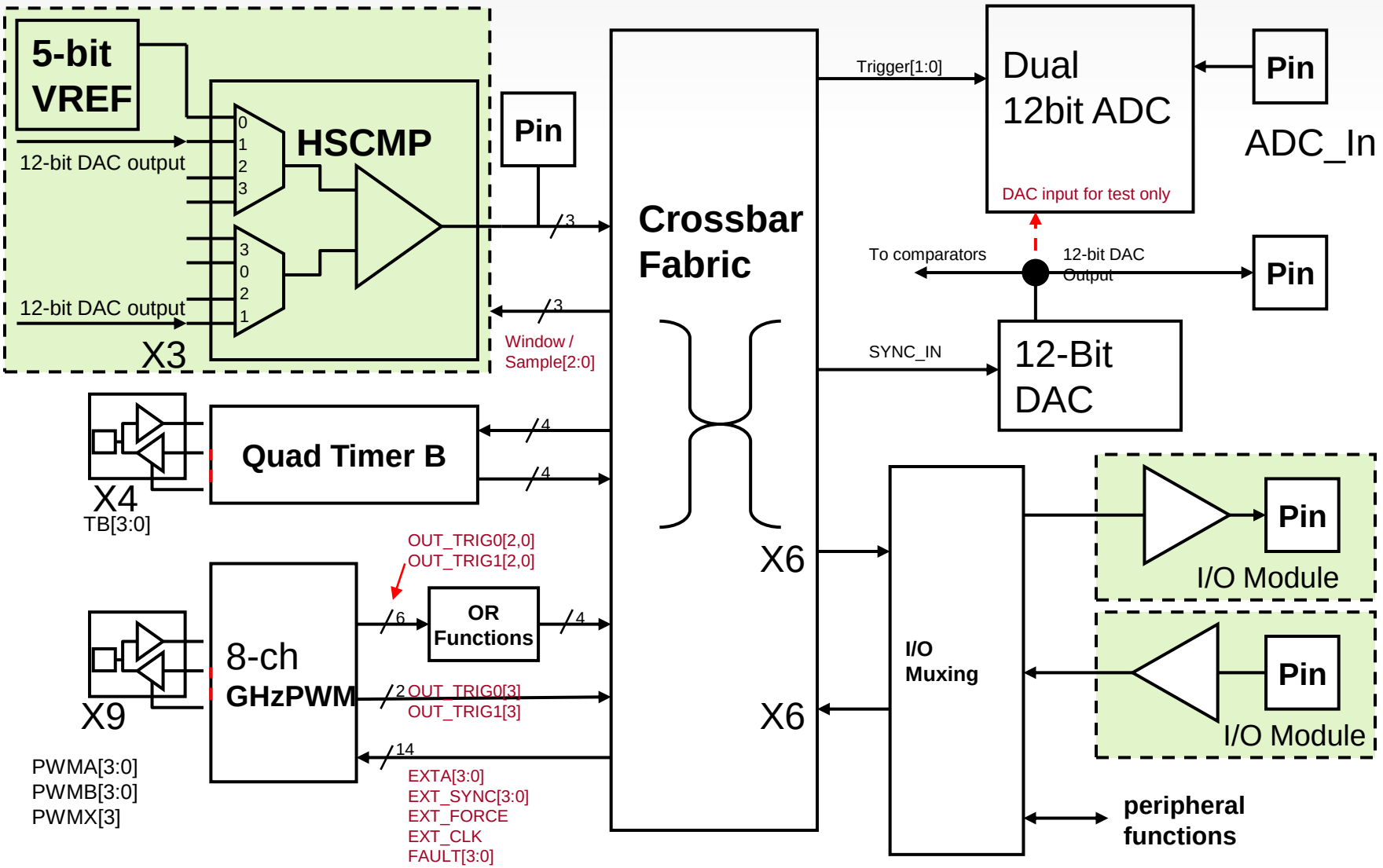
ADC Inputs[6] (Pin Group 3)					
Input voltage (external reference)	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Input voltage (internal reference)	V_{ADIN}	V_{SSA}	—	V_{DDA}	V
Input leakage[7]	I_{IA}	—	0	+/- 2	µA
V_{REFH} current	I_{VREFH}	—	0	—	µA
Input injection current[8], per pin	I_{ADI}	—	—	3	mA
Input capacitance	C_{ADI}	—	See **Figure 10-17**	—	pF
Input impedance	X_{IN}	—	See **Figure 10-17**	—	Ohms

DC -Bus Voltage Sampling Circuit

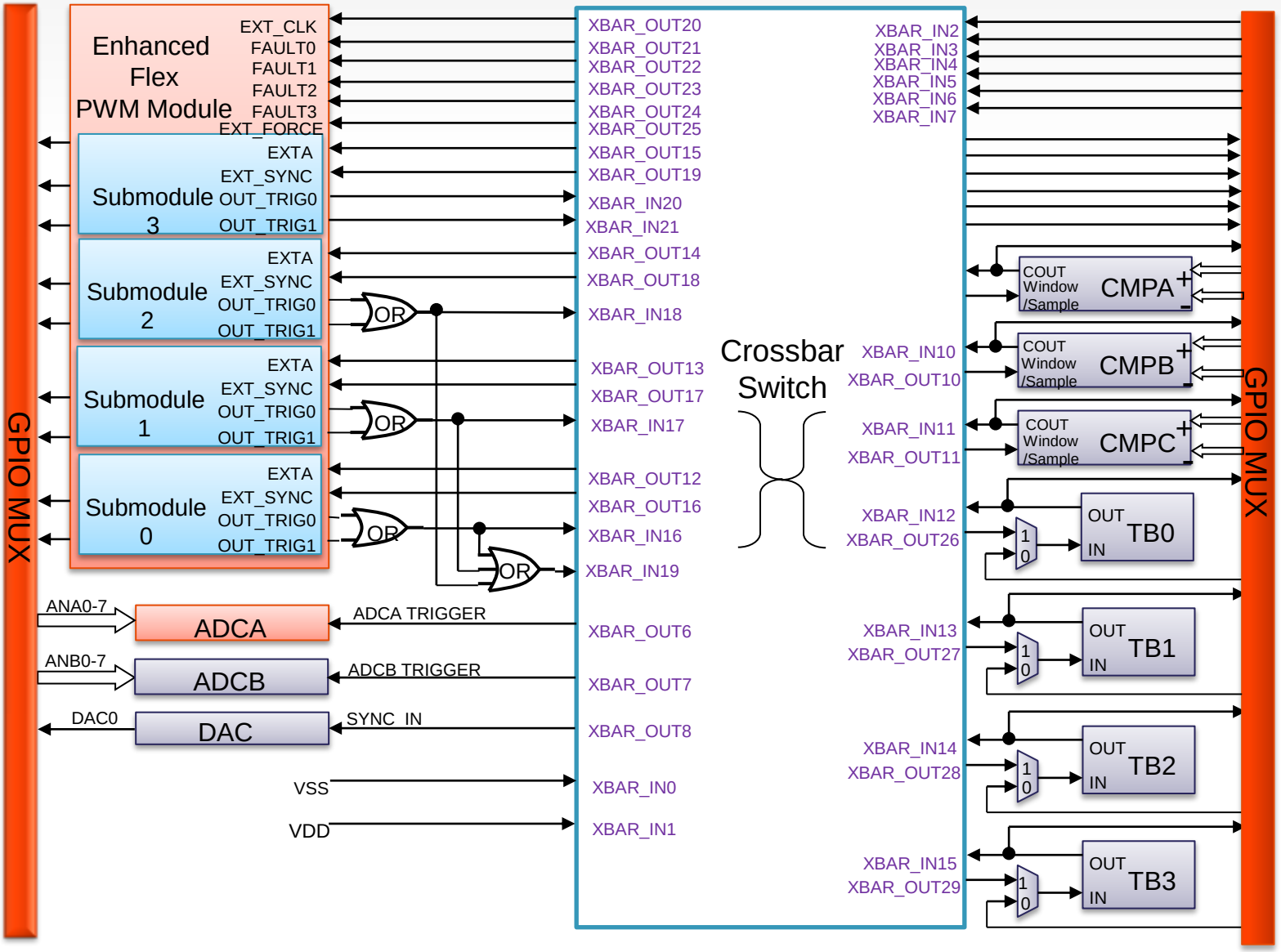


Peripheral Summary: Crossbar

…C56F824x/5x Crossbar Inter-module Connection



Crossbar Detail

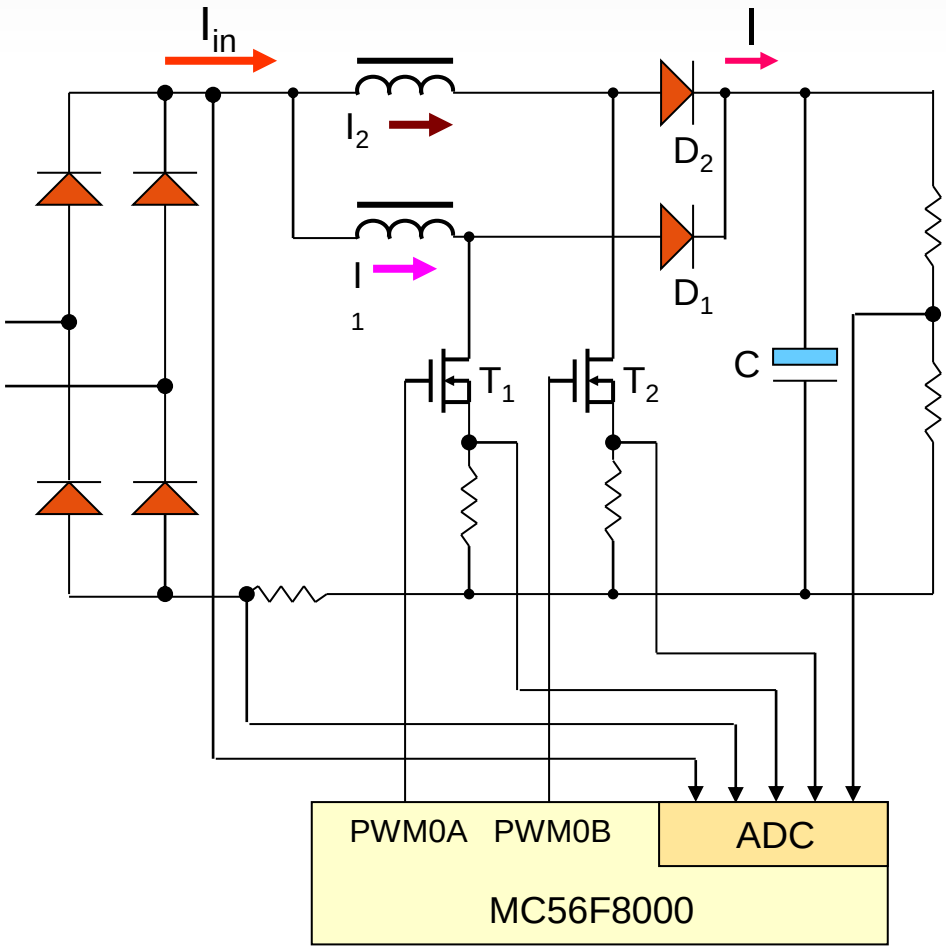


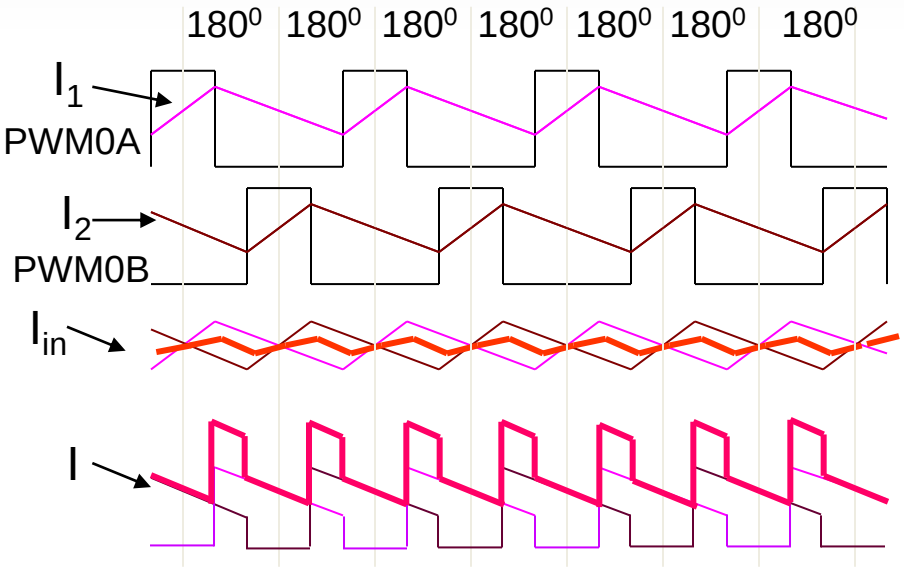
Resonant Converter Introduction

- Continuous demand for high power density and low profile in power converters leads to increasing switching frequency
- The higher switching frequency ensures smaller power transformer include all passive components at given output power
- On the other hand the higher switching frequency brings higher switching losses
- To solve this issue several resonant converter topologies have been introduced
- The resonant converter topology allows to use switching frequency above 1MHz

PFC Implementation in Freescale DSC

Single-phase interleaved PFC





Application Notes

AN1919 - Design of Indirect Power Factor Correction Using DSP56F80X
AN1965 - Design of Indirect Power factor Correction Using the 56F800/E
AN3115 - Implementing a Digital AC/DC Switched-Mode Power Supply using a 56F8300 Digital Signal Controller
AN3843 - Single Phase Two-Channel Interleaved PFC Converter Using MC56F8006

Reference Design

DRM069 - Online UPS using the 56F8300
DRM074 - Design of a Digital AC/DC SMPS using the 56F8323 Device
DRM098 - Direct PFC Using the MC56F8013

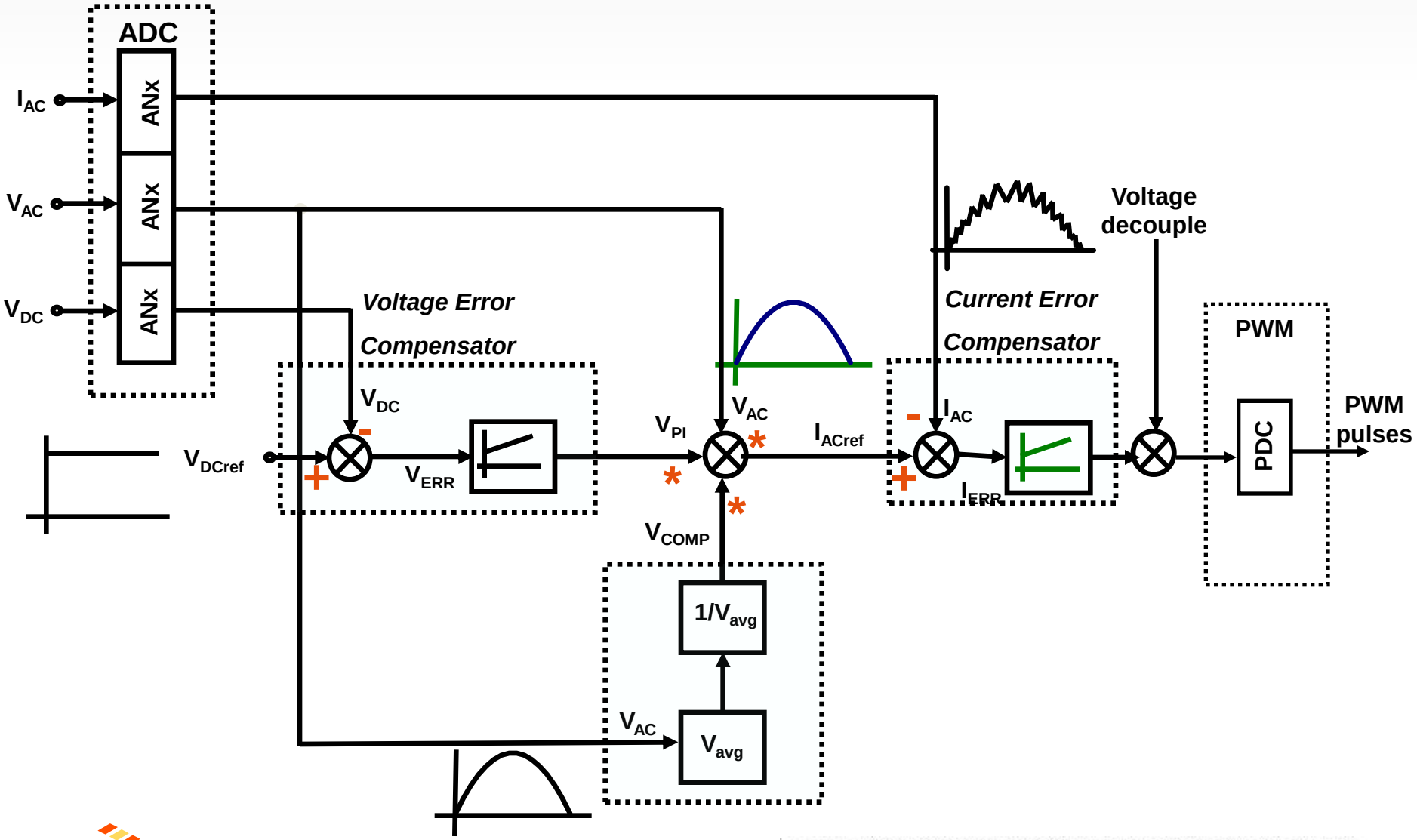
Recommended Devices

MC56F800x, MC56F80xx, MC56F82xx, MC56F83xx , MC82F84xx

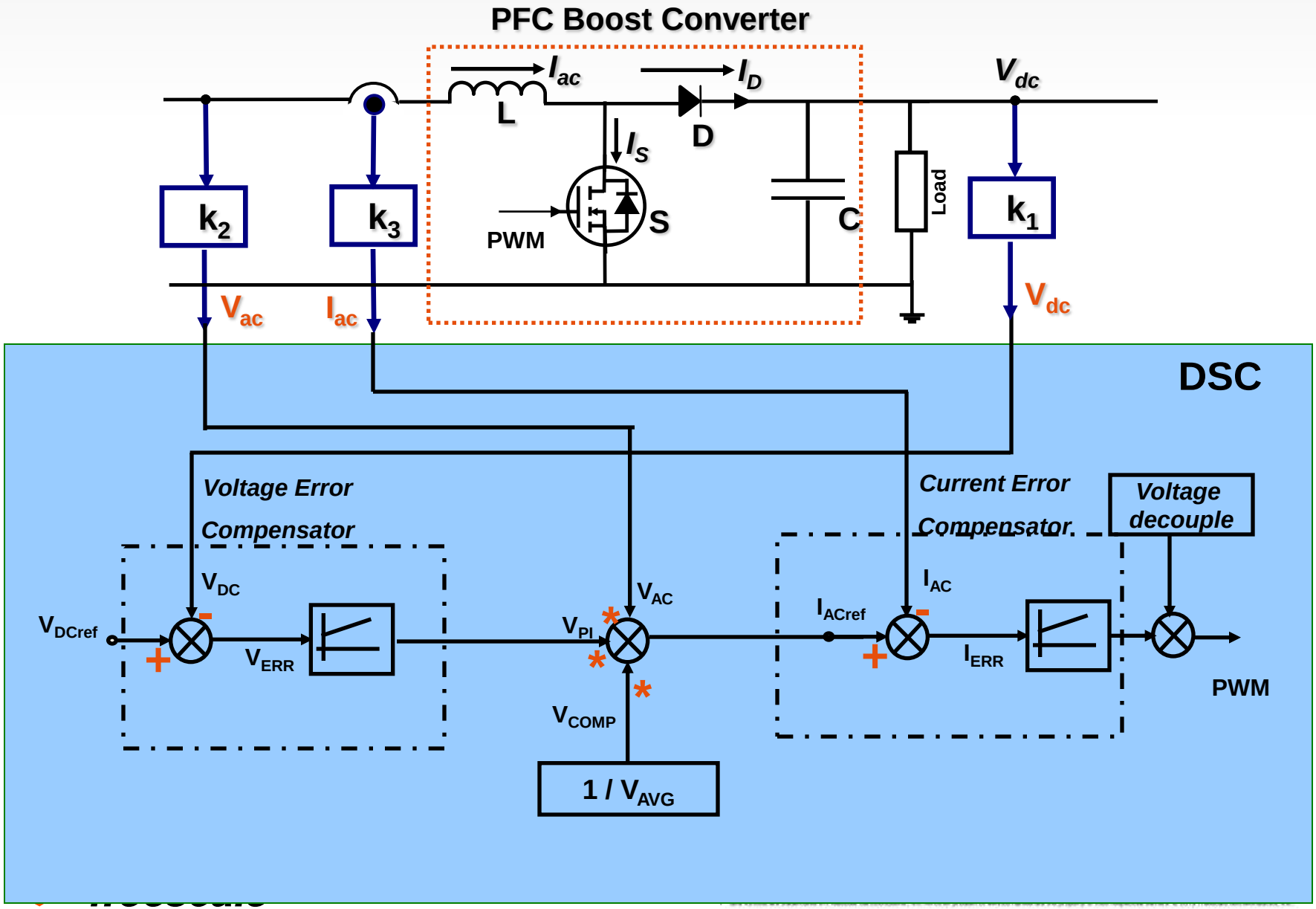
DSC peripherals for Integrated PFC

Description	Peripheral Resources
Gate drive for MOSFETS	PWM0A, PWM0B
Line current	ADC
Line voltage	ADC
Output voltage	ADC
T1 current	ADC
T2 current	ADC

Digital Implementation



Complete PFC Integration



MC56F827xx (Anguilla Silver) Key Messages

Half the power, twice the performance

The MC56F827xx digital signal microcontroller uses half the power and achieves twice the performance as the competition in a compact 5x5 mm package.

For *real* engineers doing *real* work.

Unrivalled Low Power

The lowest power DSC available on the market

- Power consumption is minimized while servicing advanced mathematical algorithms with minimal cycles.
- Ultra low power ADC block reduces overall run-time power consumption by over 40% when compared to existing solutions.
- Concurrent operations offer best-in-class execution times and overall low power run rates.
- Switches from high performance code at100MHz to background code at 50Mhz, lowering power consumption.

Dynamic Performance

Fastest DSC in its class with 100 MHz of performance

- The highest number of operations per cycle of any MCU in its class
- Low load efficiencies are able to easily meet new power conversion regulations.
- High resolution PWMs with precise and stable control across a wide range of loads and temperatures.
- PWM automatically synchronizes complimentary channels with no delay on independent time bases
- Improved real-time control, accuracy and power consumption with dual 12-bit ADCs sampling up to 1.25 mega samples per second (Msps).
- Peripheral Crossbar increases signal integrity, adds additional HW logic flexibility and eliminates unnecessary core intervention.

Lowest Cost of Design

Advanced integration with invaluable tools and software speed development and lower BOM costs

- Achieves motor control with integrated Power Factor Correction (PFC) reducing chip count.
- Motor and Power Control Libraries, PMBus software stack, and application-focused reference designs reduce development time and provide market-focused building blocks.
- A high level of on-chip integration lowers external Op Amp and capacitor costs.
- Proven 5 volt tolerant I/O and Peripheral Crossbar enable greater flexibility and system cost reduction.
- Development tools, including FREEMaster, enable real-time debug monitoring, data visualization, advanced modeling, rapid application design, and more.

Find your Z-Domain

Freescale DSC

$$A = \begin{bmatrix} a_{11} & a_{12} & \cdots & a_{1k} \\ a_{21} & a_{22} & \cdots & a_{2k} \\ \vdots & \vdots & & \vdots \\ a_{n1} & a_{n2} & \cdots & a_{nk} \end{bmatrix}$$

$$B = \begin{bmatrix} b_{11} & b_{12} & \cdots & \\ b_{21} & b_{22} & \cdots & b_{2k} \\ \vdots & \vdots & & \vdots \\ b_{n1} & b_{n2} & \cdots & b_{nk} \end{bmatrix}$$

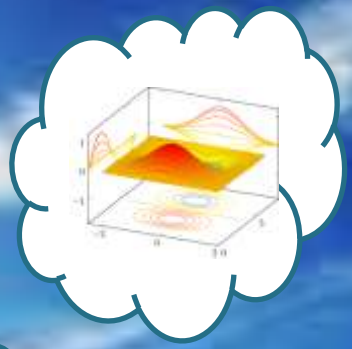
$$y(k) = 2b(a^k)\left(\frac{\cos(k\theta + \phi) + \cos(k\theta)}{2}\right)u(k)$$

$$y(k) = 2b \cdot a^k \cdot \cos(k\theta + \phi) \cdot u(k)$$

$$A + B = \begin{bmatrix} a_{11} + b_{11} & a_{12} + b_{12} & \cdots & a_{1k} + b_{1} \\ a_{21} + b_{21} & a_{22} + b_{22} & \cdots & a_{2k} + b_{2k} \\ \vdots & \vdots & & \vdots \\ a_{n1} + b_{n1} & a_{n2} + b_{n2} & \cdots & a_{nk} + b_{nk} \end{bmatrix}$$

$$cA = \begin{bmatrix} ca_{11} & ca_{12} & \cdots & ca_{1k} \\ \vdots & \vdots & & \vdots \\ ca_{n1} & ca_{n2} & \cdots & ca_{nk} \end{bmatrix}$$

$$y(k) = \left((b\angle\phi)(a\angle\theta)^k + (b\angle -\phi)(a\angle -\theta)^k\right)u(k)$$



$$Y(z) = \left(\frac{(b\angle\phi)z}{z-(a\angle\theta)}\right) + \left(\frac{(b\angle -\phi)z}{z-(a\angle -\theta)}\right)$$


freescale™