ISL70321SEH

Total Dose Testing

TR053
Rev.0.00
Sep 7, 2017

Introduction

This report documents the results of low dose rate (LDR) and high dose rate (HDR) total dose testing and subsequent anneals of the ISL70321SEH radiation hardened quad power supply sequencer. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of dose rate or bias sensitivity. Parts were irradiated under bias and with all pins grounded at LDR and at HDR. The ISL70321SEH is acceptance tested on a wafer by wafer basis to 100krad(Si) at HDR (50 – 300rad(Si)/s) and to 75krad(Si) at LDR (0.01rad(Si)/s).

Related Literature

- For a full list of related documents, visit our website
  - ISL70321SEH product page

Product Description

The ISL70321SEH is a radiation hardened and SEE mitigated power supply sequencer designed to control Point-of-Load (POL) regulators with enable pins. Up to four power supplies can be sequenced by a single device, or multiple devices can be easily cascaded to sequence an unlimited number of power supplies for dense RF applications in EW, radar, and SIGINT platforms. The sequencer requires only two feedback resistors per power supply and a single resistor to set the rising and falling delay. The device features precision input comparators with an input threshold voltage of 600mV ±1.5% for the highest possible accuracy when monitoring the power supply voltages.

The ISL70321SEH is offered in an 18 Ld 10mmx12mm CDFP package or in die form, and is fully specified across the military ambient temperature range of -55°C to +125°C. With minimal external component count, precision voltage monitoring, and SET mitigation, the ISL70321SEH is the ideal choice to control many of today's spaceborne power systems.

1. Test Description

1.1 Irradiation Facilities

HDR testing was performed at 187rad(Si)/s using a Gammacell 220 ^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. LDR testing was performed at 0.01rad(Si)/s using the Intersil Palm Bay Hopewell Designs N40 panoramic ^{60}Co irradiator. Biased irradiation and annealing were performed using the bias configuration listed in "Appendix" on page 13 at 100ºC for 168 hours using a small temperature chamber.

1.2 Test Fixturing

The "Appendix" on page 13 shows the configuration used for biased irradiation at both dose rates.

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with datalogging at each downpoint.

1.4 Experimental Matrix

Total dose irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of four samples irradiated at LDR under bias, four samples irradiated at LDR with all pins grounded, four samples irradiated at HDR under bias, and four samples irradiated at HDR with all pins grounded. Three control units were used to ensure high-quality data.

The LDR ISL70321SEH samples were drawn from preproduction wafer lot 5STWB. The HDR samples were drawn from preproduction wafer lots 5STWB and 5STWB01. All samples were packaged in the hermetic 18-pin solder-sealed production flatpack (package code K18.B). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the LDR tests were 0, 10, 30, 50, and 75krad(Si). Downpoints for the HDR tests were 0, 30, 50, 100, and 150krad(Si). All irradiations were followed by a high temperature anneal at 100ºC under bias.

2. Test Results

2.1 Attributes Data

Part	Dose Rate, Rad(Si)/s	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
ISL70321SEH	0.01	Refer to "Appendix" on page 13	4	Pre-irradiation	4	
				10krad(Si)	4	0
				30krad(Si)	4	0
				50krad(Si)	4	0
				75krad(Si)	4	0
				Anneal	4	0
ISL70321SEH	0.01	Grounded	4	Pre-irradiation	4	
				10krad(Si)	4	0
				30krad(Si)	4	0
				50krad(Si)	4	0
				75krad(Si)	4	0
				Anneal	4	0
ISL70321SEH	187	Refer to "Appendix" on page 13	4	Pre-irradiation	4	
				30krad(Si)	4	0
				50krad(Si)	4	0
				100krad(Si)	4	0
				150krad(Si)	4	0
				Anneal	4	0
ISL70321SEH	187	Grounded	4	Pre-irradiation	4	
				30krad(Si)	4	0
				50krad(Si)	4	0
				100krad(Si)	4	0
				150krad(Si)	4	0
				Anneal	4	0

Note:
1. 'Pass' indicates a sample that passes all SMD Group A limits.

2.2 Critical Parameters

The table below lists 13 critical parameters that are considered indicative of part performance. These parameters are discussed in detail below and are plotted in Figures 1 through 13. All limits are SMD Group A values.

Fig	Parameter	Limit, low	Limit, high	Units	Notes
1	Quiescent power supply current	-	6	mA	3V supply
	Quiescent power supply current	-	8	mA	13.2V supply
2	Average comparator rising threshold voltage	0.591	0.609	V	3V supply
3	Average comparator rising threshold voltage	0.591	0.609	V	13.2V supply
4	Average comparator input leakage current	-50	50	nA	3V supply
5	Average comparator input leakage current	-50	50	nA	13.2V supply

Fig	Parameter	Limit, low	Limit, high	Units	Notes
6	Average comparator hysteresis current	-28	-20	µA	3V supply
7	Average comparator hysteresis current	-28	-20	µA	13.2V supply
8	Delay timer delay	1.8	2.2	ms	RSET = 10K, 13.2V supply
9	Delay timer delay	18	22	ms	RSET = 100K, 13.2V supply
10	Power Good (PGOOD) timer delay	3.6	4.4	ms	RSET = 10K, 13.2V supply
11	Power Good (PGOOD) timer delay	36	44	ms	RSET = 100K, 13.2V supply
12	Rising undervoltage lockout level	2.8	2.95	V	13.2V supply
13	Undervoltage lockout hysteresis	30	100	mV	13.2V supply

Note:
2. All limits are SMD Group A values.

Figure 1 on page 5 plots the quiescent power supply current for the 3V supply and 13.2V supply cases.

Figure 2 on page 6 and Figure 3 on page 6 plot the average comparator rising threshold voltage for the six comparator-type inputs. We also show minimum/maximum error bars. The six comparator-type inputs are:

- The Sequence INITIATE input (Pin 7), which is connected to the UP pin when the device is in a standalone application or is the first in a cascade configuration. For the subsequent parts in a cascade configuration the Sequence INITIATE input is driven by the DONE output pin of the previous ISL70321SEH.
- The UP input (Pin 2), which commands the ISL70321SEH to start the power-up sequence.
- The VM1 through VM4 inputs (Pins 3, 4, 5 and 6), which are voltage monitor inputs indicating the sequenced power supply has reached the desired power-on voltage or has reached the desired power-off voltage.

Figure 4 on page 7 and Figure 5 on page 7 plot the average comparator input leakage current for the above six comparator-type inputs. We also show minimum/maximum error bars.

Figure 6 on page 8 and Figure 7 on page 8 plot the average comparator hysteresis current for the above six comparator-type inputs. We also show minimum/maximum error bars.

Figure 8 on page 9 and Figure 9 on page 9 plot the rising and falling time delay between a supply ON/OFF signal (UP or VMx) and the enabling or disabling of the next power supply in the sequence. This delay is set by an external 10kΩ to 100kΩ resistor. Figure 8 shows the 10kΩ case (2ms delay), and Figure 9 shows the 100kΩ case (20ms delay).

Figure 10 on page 10 and Figure 11 on page 10 plot the ramp time for a power supply to reach a power-good state after being enabled with ENx. A 10kΩ to 100kΩ resistor connected between PGTMR to GND sets the Power-good (PGOOD) timer delay. Figure 10 shows the 10kΩ case (4ms), and Figure 11 shows the 100kΩ case (40ms).

Figure 12 on page 11 plots the rising undervoltage lockout (UVLO) level. The UVLO function monitors the output voltage (VCC5) of the internal linear regulator. When this voltage rises above ~2.8V, the ISL70321SEH initializes by turning on the 600mV bandgap reference voltage and the internal PGOOD and delay timer oscillators. If the voltage on VCC5 falls below 2.8V, the UVLO shuts off both oscillators and the band-gap reference. It also holds the open-drain ENx outputs low until VCC5 drops below 1.2V.

Figure 13 on page 11 plots the UVLO hysteresis. This circuit allows the level of the sequenced power supply output voltage to precisely gate the turn-on/turn-off of the next regulator. The internal IHYS current source has a typical value of 24µA and adds hysteresis between the turn-on and turn-off levels.

Refer to the ISL70321SEH data sheet for further details.

2.3 Critical Parameter Variables Data

The plots in Figures 1 through 13 show the TID response of the critical parameters outlined in "Critical Parameters" on page 3. The input comparator threshold, input leakage current and hysteresis current (Figures 2 through 7) include minimum/maximum error bars. The remaining figures plot the median only.

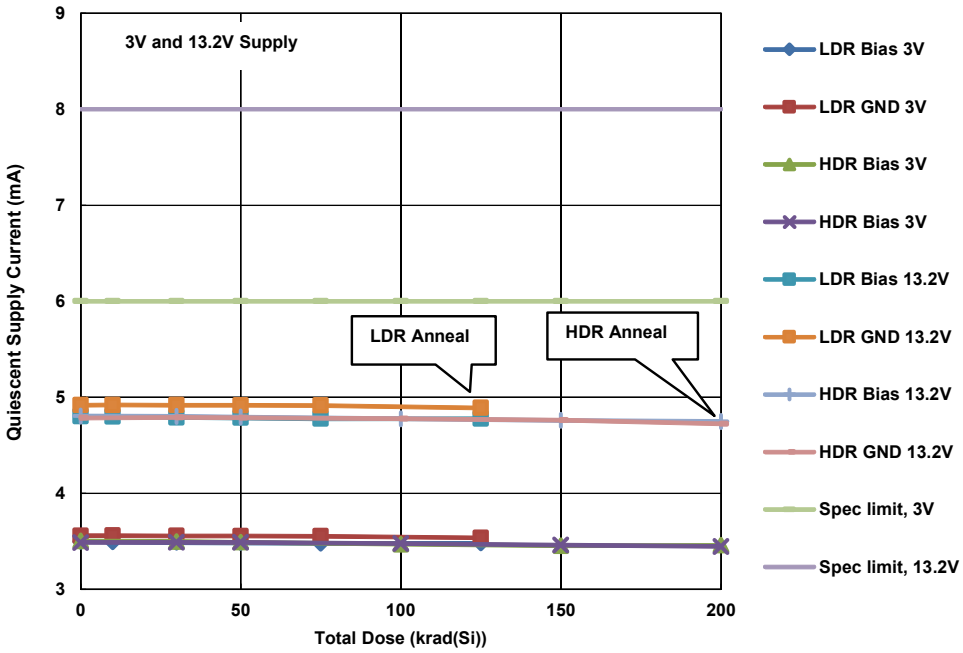


Figure 1. ISL70321SEH quiescent power supply current, 3V and 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median as well as minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 6mA maximum (3V supply) and 8mA maximum (13.2V).

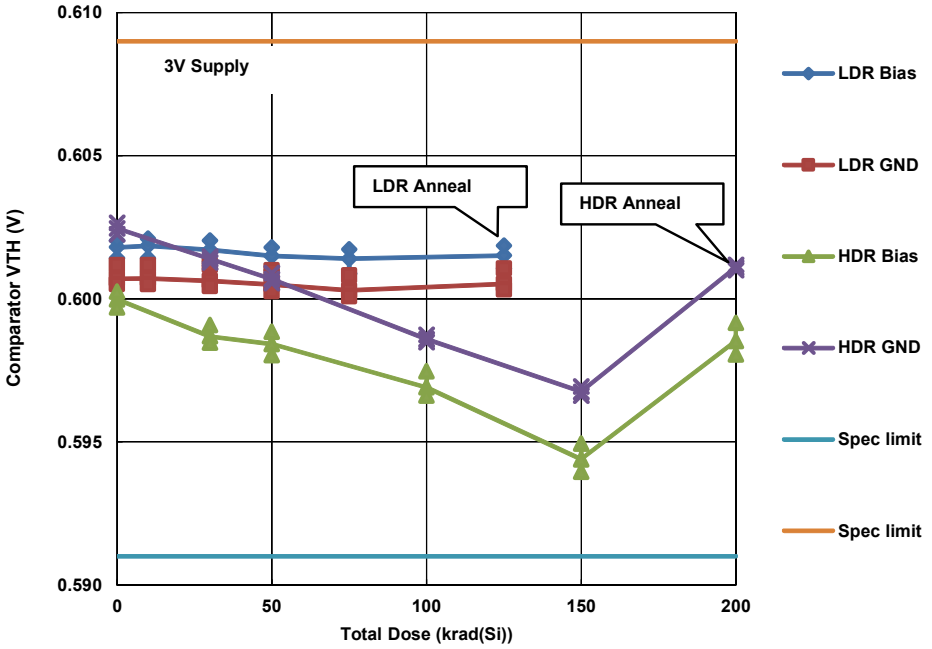


Figure 2. ISL70321SEH comparator rising threshold voltage, 3V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median and minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 0.591V to 0.609V.

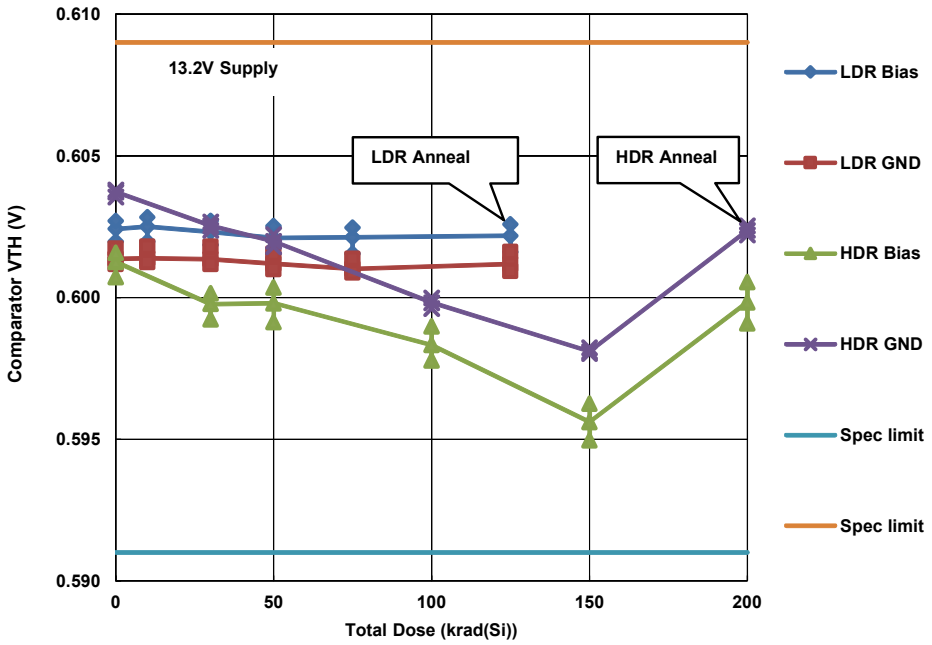


Figure 3. ISL70321SEH comparator rising threshold voltage, 13.2V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median and minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 0.591V to 0.609V.

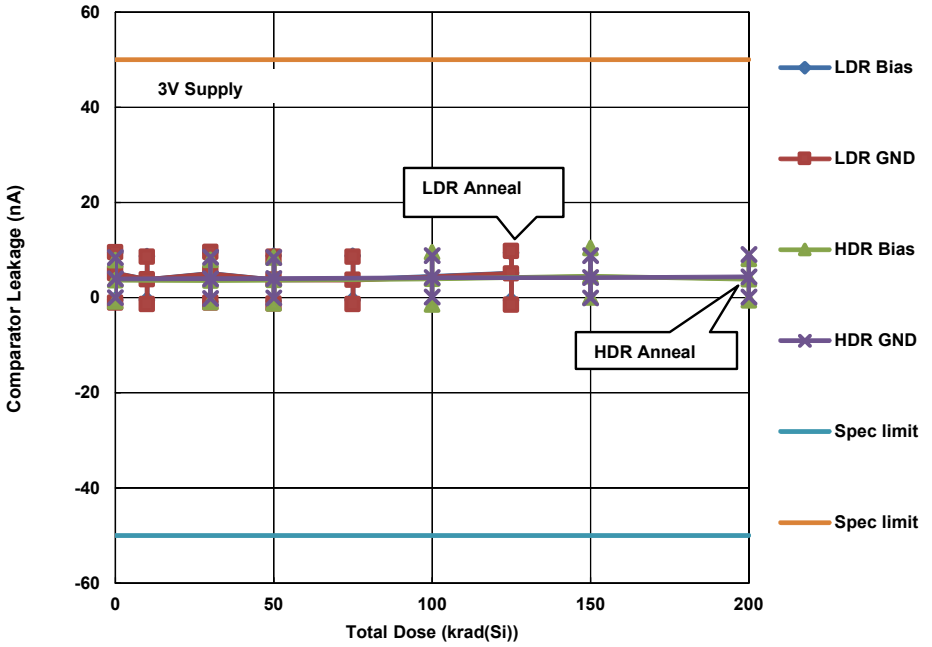


Figure 4. ISL70321SEH comparator input leakage current, 3V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median and minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are -50nA to 50nA.

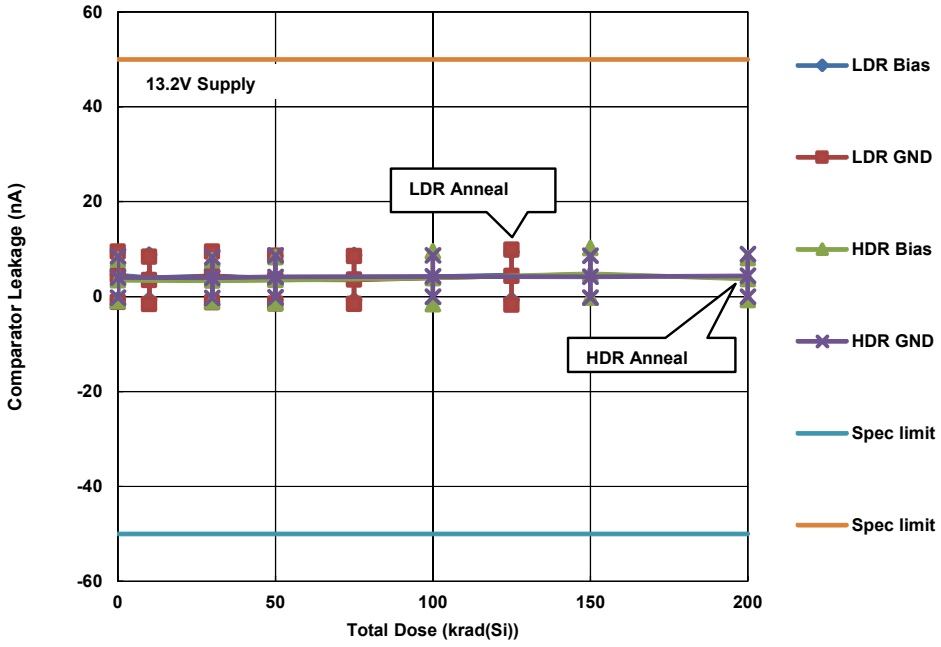


Figure 5. ISL70321SEH comparator input leakage current, 13.2V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median and minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are -50nA to 50nA.

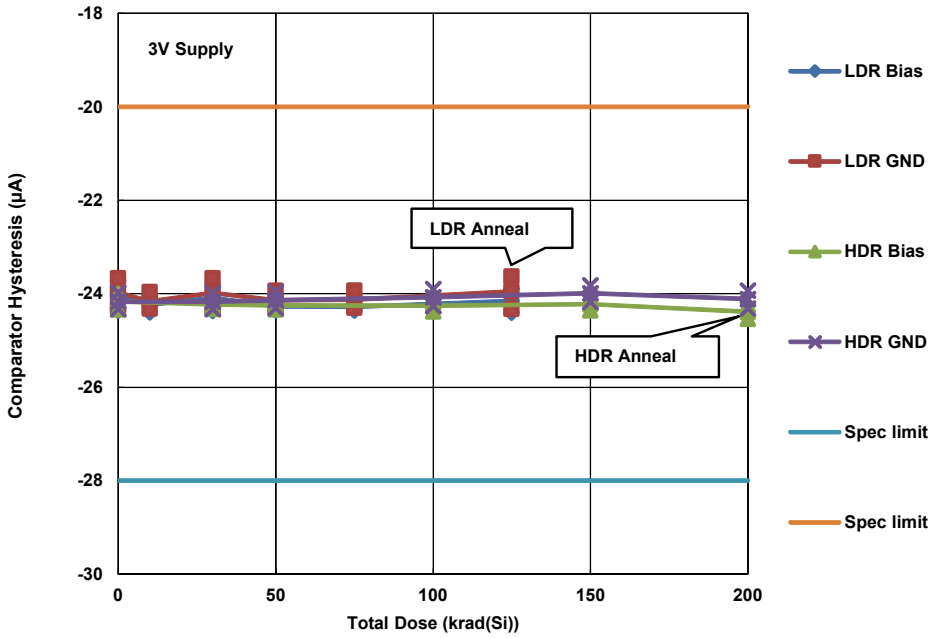


Figure 6. ISL70321SEH comparator hysteresis current, 3V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median and minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are -28µA to -20µA.

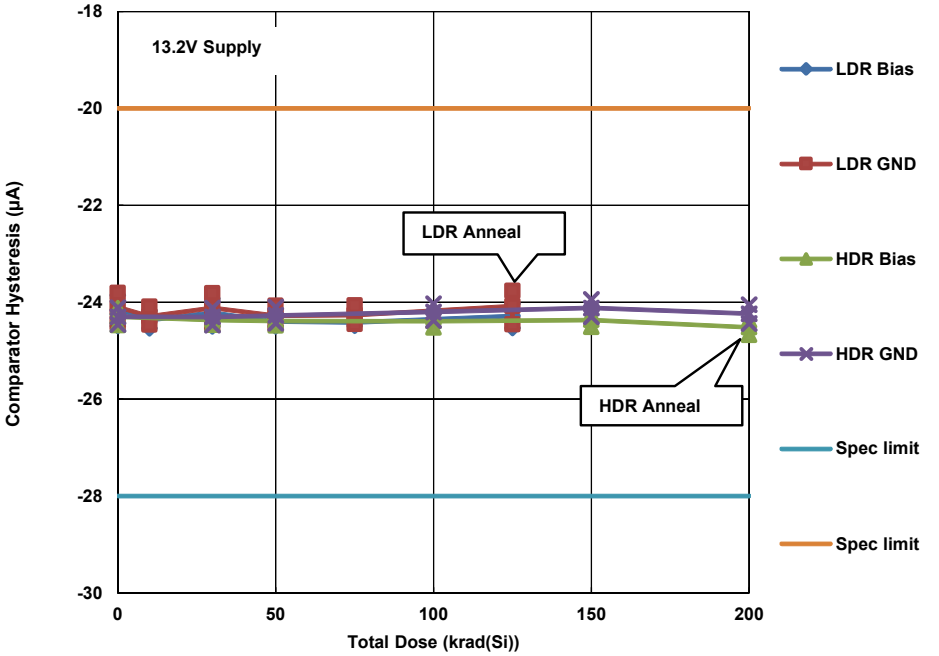


Figure 7. ISL70321SEH comparator hysteresis current, 13.2V supply, average of INIT, UP, VM1, VM2, VM3, and VM4 inputs, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median and minimum/maximum error bars. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are -28µA to -20µA.

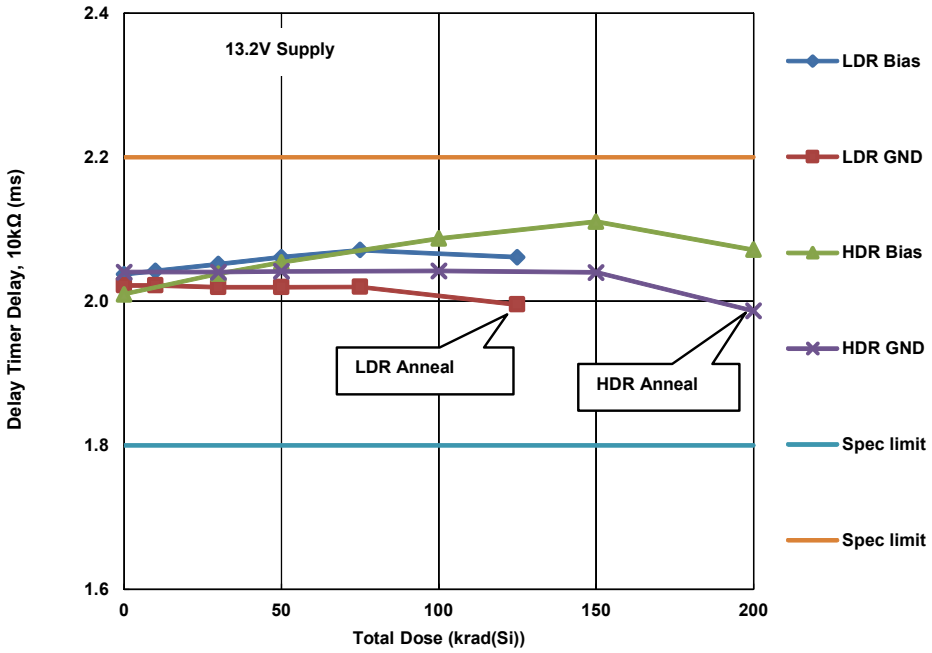


Figure 8. ISL70321SEH delay timer delay with a timer delay resistor value of 10kΩ, 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 1.8ms to 2.2ms.

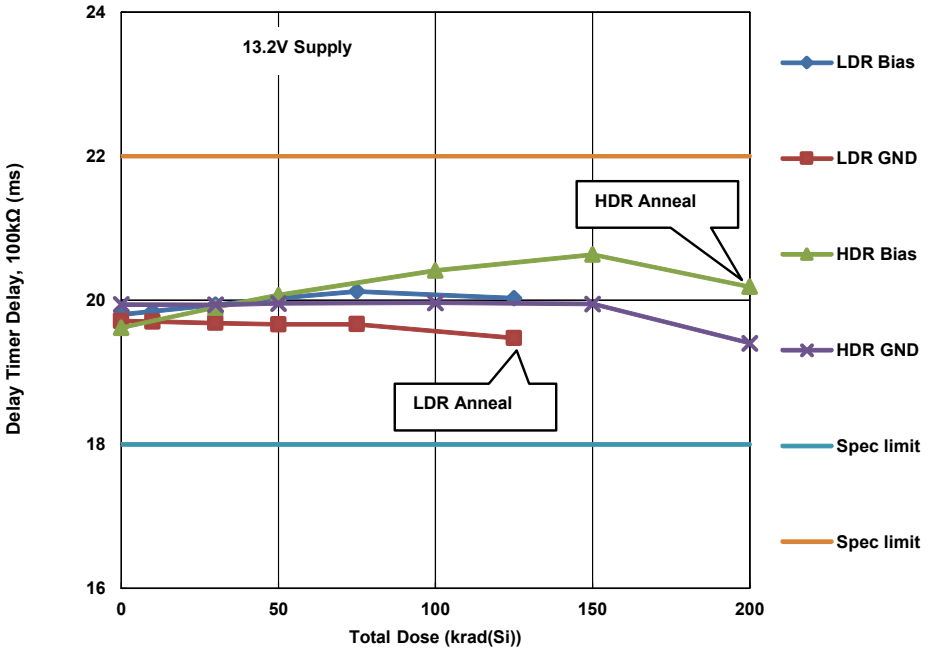


Figure 9. ISL70321SEH delay timer delay with a timer delay resistor value of 100kΩ, 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 18ms to 22ms.

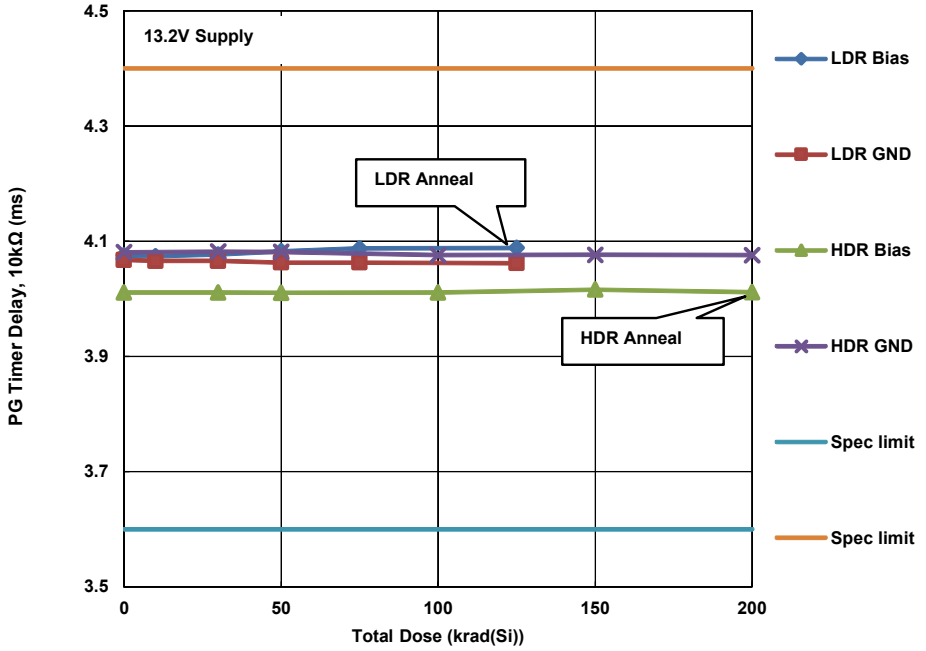


Figure 10. ISL70321SEH Power Good (PGOOD) timer delay with a timer delay resistor value of 10kΩ, 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 3.6ms to 4.4ms.

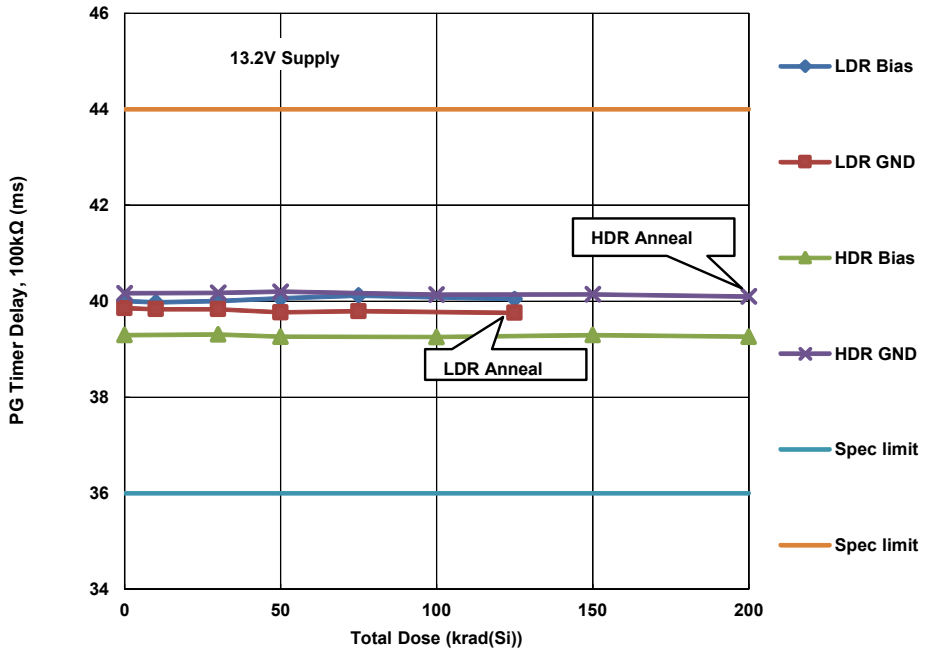


Figure 11. ISL70321SEH Power Good (PGOOD) timer delay with a timer delay resistor value of 100kΩ, 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100°C 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 36ms to 44ms.

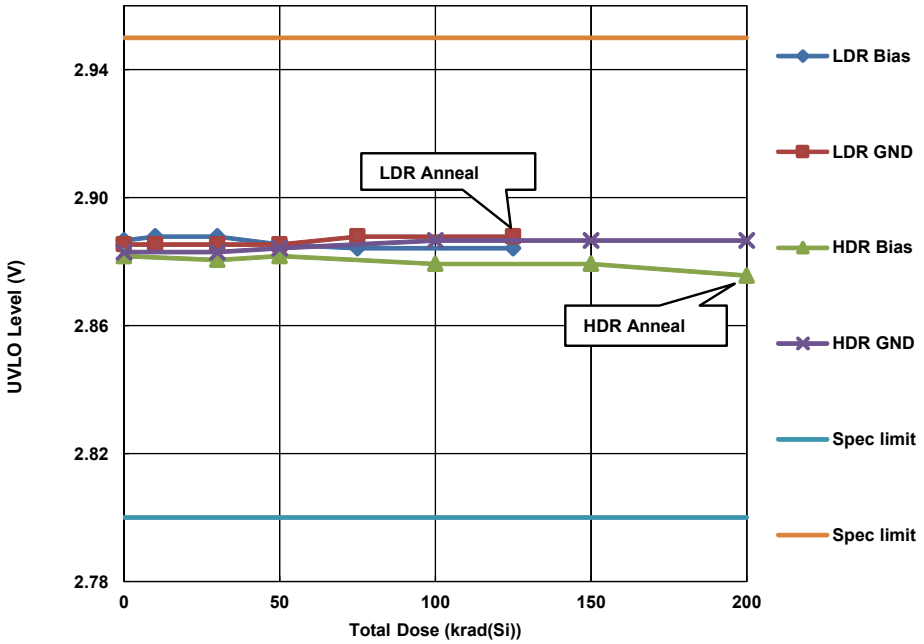


Figure 12. ISL70321SEH rising undervoltage lockout level, 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100ºC 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 2.8V to 2.95V.

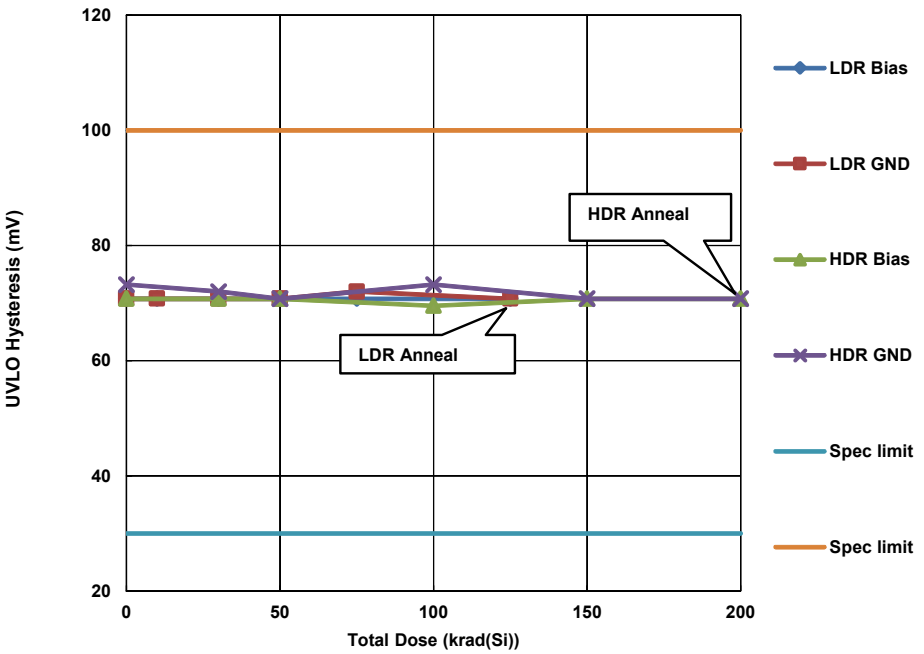


Figure 13. ISL70321SEH undervoltage lockout hysteresis, 13.2V supply, as a function of total dose irradiation at LDR and at HDR for the biased (per "Appendix" on page 13) and unbiased (all pins grounded) cases, plotting the median. The LDR was 0.01rad(Si)/s and the HDR was 187rad(Si)/s. Irradiations were followed by a 100ºC 168-hour biased anneal; the LDR anneal was performed after 75krad(Si) at LDR while the HDR anneal was performed after 150krad(Si) at HDR. The sample size of all cells was four. The SMD Group A limits are 30mV to 100mV.

3. Discussion and Conclusion

We report the results of a low and HDR total dose test of the ISL70321SEH radiation hardened quad power supply sequencer. All irradiations were followed by a 168-hour anneal at 100ºC under bias.

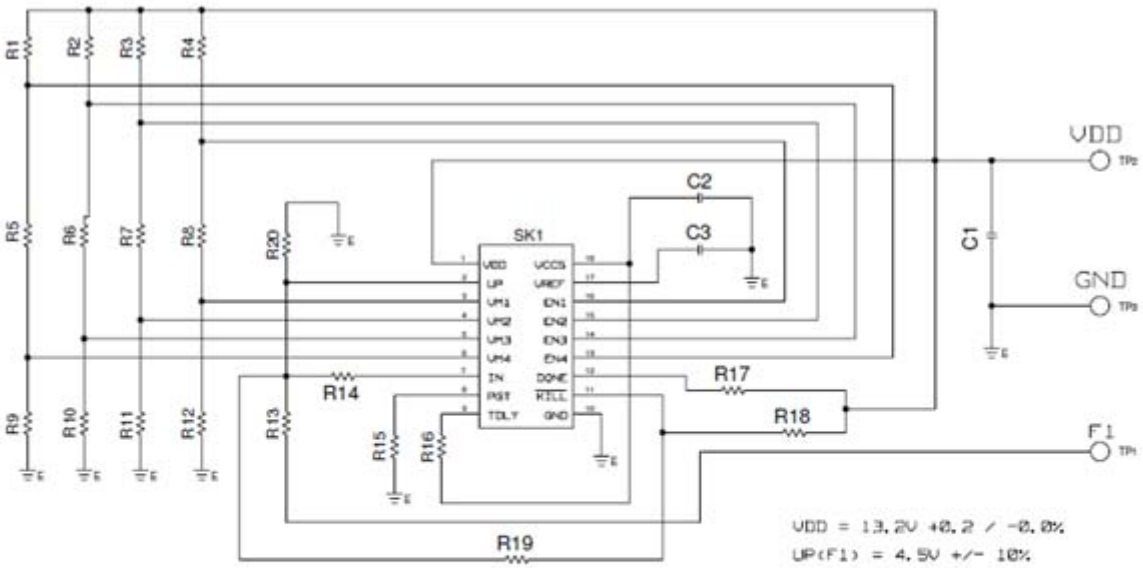
"Attributes Data" on page 3 summarizes the attributes data for the test. "Critical Parameters" on page 3 summarizes the critical parameters for the part. Finally, "Critical Parameter Variables Data" on page 5 provides plots of the total dose and anneal response for these critical parameters.

All parameters remained well within the SMD Group A limits at all downpoints. The comparator rising threshold voltage for the 3V supply and 13.2V supply cases (Figure 2 on page 6 and Figure 3 on page 6, respectively) showed significant change over HDR irradiation. The parameter plotted in Figures 2 and 3 is the average of the comparator threshold voltage for the INIT, UP, VM1, VM2, VM3, and VM4 inputs; we plotted the median as well as minimum/maximum error bars for these averages. The parameters recovered to very near the pre-irradiation value after the high temperature biased anneal. These behaviors are often observed in all-CMOS or largely CMOS parts. All other parameters showed no differences in total dose response between low and HDR. Referring to Figure 2 on page 6 and Figure 3 on page 6, we note that all parameter values remained well within the SMD Group A limits, which leads to the conclusion that the part is not considered dose rate sensitive.

Similarly, no differences in total dose response between biased and grounded irradiation were noted at either dose rate, and the part is not considered bias sensitive.

4. Appendix

ISL70321SEH irradiation and anneal bias configuration.



PARTS:

R1-R4 = 1.78K OHMS, 1%, 1/4 WATT RESISTOR
R5-R8 = 24.3K OHMS, 1%, 1/4 WATT RESISTOR
R9-R12 = 15.8K OHMS, 1%, 1/4 WATT RESISTOR
R13 = 6.8K OHMS, 1%, 1/4 WATT RESISTOR
R14-R18 = 20K OHMS, 1%, 1/4 WATT RESISTOR
R19 = 1.6K OHMS, 1% 1/4 WATT RESISTOR
R20 = 1K OHMS, 1% 1/4 WATT RESISTOR
C1 = 0.47UF, 10%, 25V, CAPACITOR
C2 = 470NF, 10%, 25V, CAPACITOR
C3 = 220NF, 10%, 25V, CAPACITOR
SK1= SENSATA (621-0182315-011)
WITH "SPECIAL LATCH"(002-015-000)

VDD = 13.2V +0.2 / -0.0%
UP(F1) = 4.5V +/- 10%

POWER ON SEQUENCE:
1.) POWER ON VDD (13.2V)
2.) POWER ON F1 (4.5V)

POWER OFF SEQUENCE:
1.)TURN OFF F1 THEN VDD

5. Revision History

Revision	Date	Description
0.00	Sep 7, 2017	Initial release