Tektronix

Application Note

TDR Tools in Modeling Interconnects and Packages

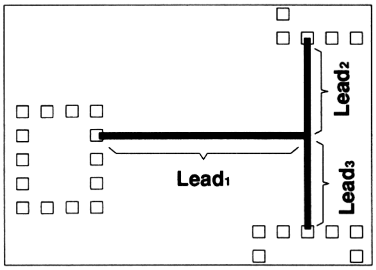


Figure 1. (a) Interconnect leads can branch between several points in a circuit. We shall measure the parameters of individual leads and the coupling parameters to other leads.

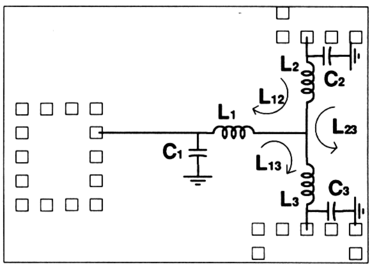


Figure 1. (b) One of many ways to represent an interconnect with a model. Each lead is characterized by its total inductance.

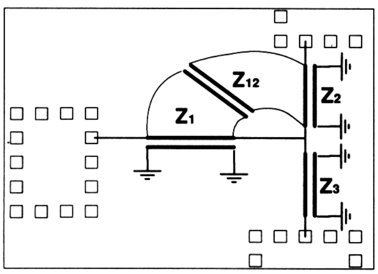


Figure 1. (c) Another way to represent an interconnect. Each lead is represented with a transmission line having characteristic impedance Z. Lines can be coupled, as shown between the leads 1 and 2.

Interconnects, signal paths, and their models

Electrical interconnects are paths that transmit signals between two or more points in a circuit, most often between active devices. Circuit boards are interconnects, semiconductor device packages are interconnects, etc. An interconnect system can have many branches, which are, ultimately, made of single leads. This application note will explore how to measure model parameters of single leads in a complex interconnect. The model parameters we derive will help us determine how leads effect transmission of electrical signals and how each lead interacts with other leads.

Figure 1 (a) is an example of an interconnect between three points in a circuit. To model such interconnect, we will first segment it into three individual leads. Now we can use a variety of models to represent the electrical behavior. The type of a model is determined by the choice a user makes. One type of model is illustrated in Figure 1 (b). Here, we represent each lead with a single inductance, single capacitance and with mutual inductances and capacitances to other leads. This is called single lump modeling, in which all the inductances and capacitances along one lead are lumped into one value. Typical single lump model parameters will be the lead inductance L, the mutual inductance to another lead L_m, the lead capacitance C and the mutual capacitance between two leads C_m. Instead of an LC pair, a transmission line section can also be used. In modeling semiconductor packages, single lump models are employed very often, since they work efficiently in simulators like SPICE and usually represent an interconnect adequately in bandwidths under 100 MHz. As with most models, a single lump model is just an approximation, which gives adequate results simulating the circuit for a given range of electrical signals.

Another type of model for our interconnect is illustrated in Figure 1 (c). Here, each lead is represented with a transmission line with some delay and characteristic impedance Z_i. Two lines can be coupled through another characteristic impedance, Z_{12}, as shown between lines 1 and 2. In more sophisticated models, the characteristic impedance can be changing along the signal path. Such changing impedance is called an impedance profile. Impedance profile can be a powerful means for extracting a variety of model parameters.

The focus of this paper will be on the measurement of electrical model parameters for semiconductor packages, such as inductance, capacitance or impedance values for different portions of leads.

For packages, the two most useful models will be the *distributed line model* and the *lumped parameter model.*

Impedance models

Consider a lead in a semiconductor package, as illustrated in Figure 2 (a). Such a lead can be viewed as composed from several sections, each acting as a transmission line, having some delay and characteristic impedance. This delay and impedance will depend on several factors, including the length of section, proximity to metal surfaces and dielectric properties. The sections can thus be represented with a string of transmission lines of varying impedance, as shown in Figure 2 (b). The impedance along the lead as a function of delay time is called the impedance profile, shown in Figure 2 (c). Individual impedance segments can be approximated with low-pass LC filter sections, Figure 2 (d). We get lumped models by combining the inductances and capacitances into fewer sections. Figure 2 (e) shows the result of combining all the inductance sections into one inductance and all the capacitance sections into two capacitances.

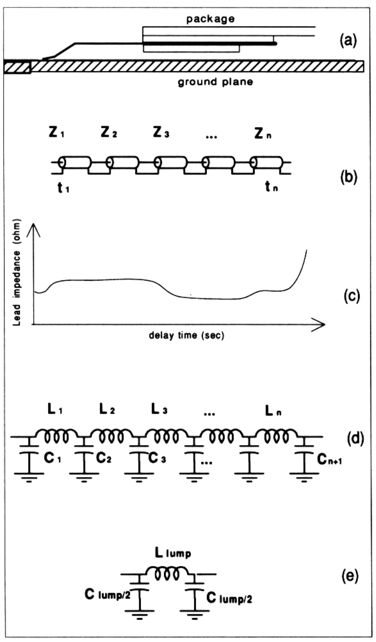


Figure 2. An interconnect lead (a) suspended over a ground plane can be represented with sections of transmission line of varying impedance (b). Plotting the impedance of transmission line sections as a function of time we get the impedance profile, shown in (c).

Each impedance section can be approximated with a low-pass LC element (d). For low frequency applications, all inductances and capacitances can be combined (lumped) into one or two sections (e).

Types of semiconductor packages

Most semiconductor packages widely in use belong to one of two basic categories: multilayer packages and leadframe packages.

Multilayer packages (Figure 3.) resemble circuit boards. Inside the package body, leads run within layers and they cross the layers through vias. There usually are several layers of conducting planes, such as ground planes, power planes, etc. The signal leads often have defined characteristic impedance. They can also be configured to minimize the coupling to neighboring leads. The connection to the outside world is made either through pins along the periphery (i.e., quad-flatpack style) or as a matrix of pins on one surface (pin-grid array style). Ground planes and power planes typically connect through several pins in parallel, to minimize the inductance between a plane and the outside world.

Leadframe packages, on the other hand, have a system of leads stamped out of one sheet of metal (Figure 4.). Their leads form a dense planar array, converging toward the active device which resides in the center. The pins are formed by bending the leads as they emerge from the plastic body. Leadframe style packages characteristically have very high coupling between neighboring leads and they interact weakly with ground planes in the world outside the package.

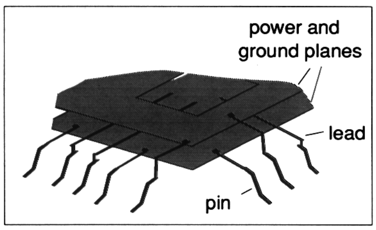


Figure 3. In a multilayer package, leads often run between conductive planes and have relatively constant impedance. Only the metalized portion of the package is shown, the dielectric body is omitted for clarity.

We shall employ different models for multilayer and leadframe packages and different techniques for measurements of these models.

Multilayer package measurement and distributed model

There is a powerful technique which can be applied in cases where the leads are relatively well isolated from each other (low crosstalk), as is often the case with multilayer ceramic packages. This is the technique employing impedance profile [1]. Here, a lead is regarded as a transmission line with a characteristic impedance which varies depending on the location, just as described in Figure 2.

We show in Appendix 1 that, for leads with negligible losses and with negligible crosstalk, the

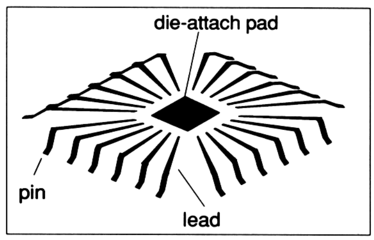


Figure 4. Leadframe packages are usually etched from a single sheet of metal. There are no internal ground planes and the coupling between leads is relatively strong.

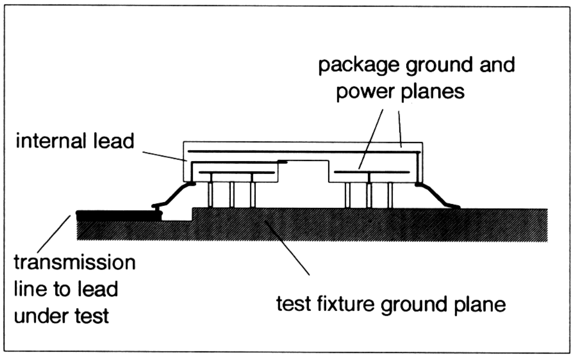


Figure 5. Package mounted on the test fixture. Power and ground planes have multiple leads contacting the fixture ground plane.

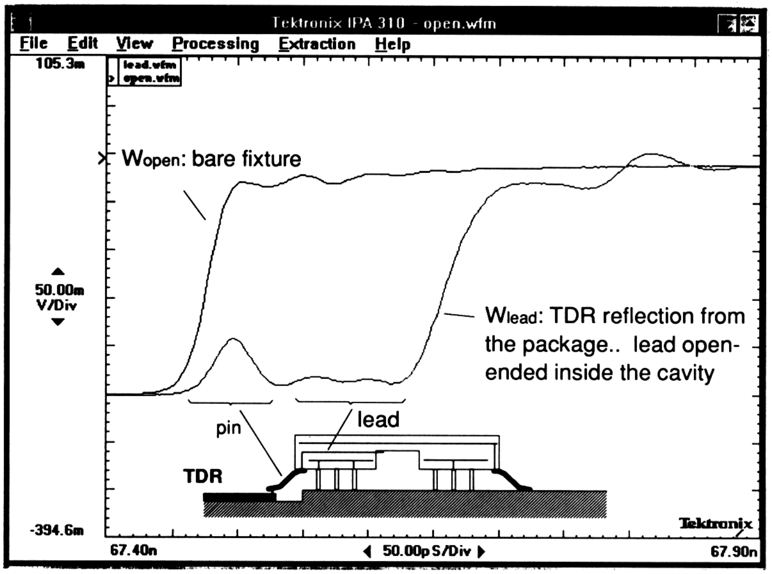


Figure 6. The TDR waveform from one package lead. The inductance of the package pin will cause an impedance mismatch in a 50 ohm system, but the lead impedance inside the package looks nice and uniform.

inductance between any two points of the interconnect is given by [2]

$$L = \frac{1}{2}\int_{t2}^{t1} Z(t)dt$$

and the capacitance is

$$C = \frac{1}{2}\int_{t2}^{t1} \frac{1}{Z(t)}dt$$

The impedance profile Z(t) is derived from the Time Domain Reflectometer (TDR) waveform, as described in Appendix 1. The points t_1 and t_2 correspond to the beginning and the end of the interval over which L and C are measured. These points can be determined by comparing the shape of the Z(t) curve with physical features of the structure under test.

We shall illustrate the method with an example using an empty multilayer ceramic package. The first step in the measurement process is to mount our package (our Device Under Test or DUT), on a test fixture which mimics the environment the package will experience in the end-user's application.

The test fixture should have a conductive surface (fixture ground plane) corresponding to the application circuit ground plane and the signal should be applied through an electrode mimicing the pad to which the package will be soldered. The package mounted on the test fixture is shown in Figure 5.

The test fixture brings the 50 ohm TDR line to the point where it can connect to the DUT. We shall observe the signal reflected from this end of transmission line before we mount our package on the fixture. The TDR reflection from here will reproduce the incoming signal (Figure 6, W_{open}). When we now mount our package, the signal will propagate through the attached lead reflecting off different features inside (Figure 6, W_{lead}). Ultimately, the signal reflects off the end of the lead (open end in our case, since the package is empty) which again generates the "open end" step. This reflection off the open end of the lead inside the package looks different from the waveform W_{open} we observed previously. The reason is that the signal underwent changes from multiple reflections as it traversed different impedance sections of the lead.

We need to acquire the waveform W_{lead} (transfer it from the TDR instrument into our computer) for further processing.

To get to the distributed impedance, we shall also acquire another waveform, W_{short}. To do this we remove the package under test from the fixture and connect the signal launching tip to fixture ground using the shortest possible lead. This can usually be achieved by pressing a piece of flexible copper tape against both the tip and the ground surface, shorting the tip to ground. The waveform W_{short} thus obtained is a much more accurate representation than W_{step} of the TDR signal entering the DUT. We will use W_{short} in impedance profile extraction.

When we extract the impedance profile using W_{short} and W_{lead} (see Appendix 1), we obtain the function Z(t), shown in Figure 7. This function looks somewhat similar to the waveform W_{lead}, but its features will be better defined. Z(t) corresponds directly to physical features of the lead, since the multiple signal reflections which can plague the TDR signal W_{lead} are removed.

The shape of the impedance profile curve Z(t) suggests several choices for the interconnect model [3]. The simplest choice is the single-lump LC model, shown in Figure 7 (a). We obtain the total L and total C for the lead by integrating between the points on Z(t) corresponding to the beginning and the end of the lead. (These points are marked by cursors in Figure 7 and the values obtained by integration for total L and C are shown in the area to the left of the curve.)

Another way to model our interconnect is chown in Figure 7 (b). Here, we divide our model into two sections. The first section is associated with the peak at the beginning of the impedance profile Z(t), which obviously corresponds to the input pin with relatively high inductance. The second section approximates the relatively flat portion of Z(t) with a segment of transmission line. Indeed, this package has a lead of relatively constant impedance running toward the cavity where the active device will be bonded. Yet another model in Figure 7 (c) approximates this second section with an LC lump.

Which of these models to chose depends on the judgment of the user. In general, as the speed of signals in the final application increases, a larger number of sections will be required to make the results of circuit simulation correspond to reality.

An item of high interest in fast digital circuit design is the ground bounce (or, ΔI noise), related to the inductance of package ground leads. To measure the inductance of one ground lead, we acquire the TDR waveforms W_{short} and W_{lead} of one package ground lead (just as we did before for a signal lead), and derive the

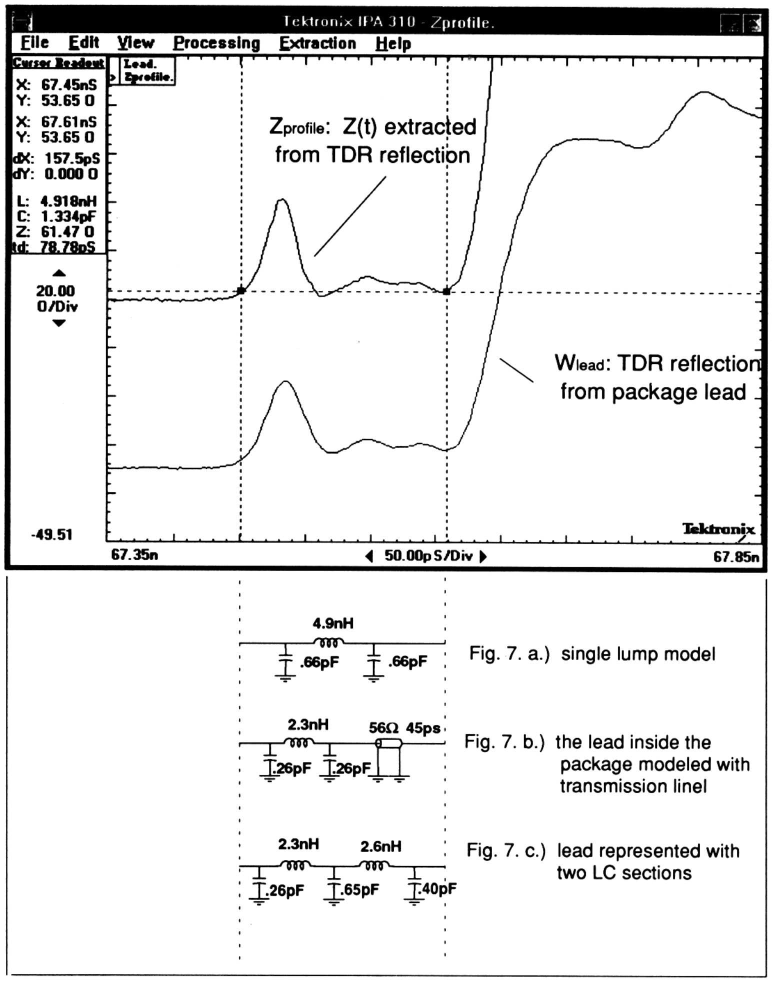


Figure 7. The impedance profile extracted from the packageTDR reflection (top) used to generate parameter values for various model configurations (bottom). Which model configuration to choose depends on simulation needs.With appropriate tools, the inductance, capacitance, etc. can be read directly with cursors from the Z(t) waveform.

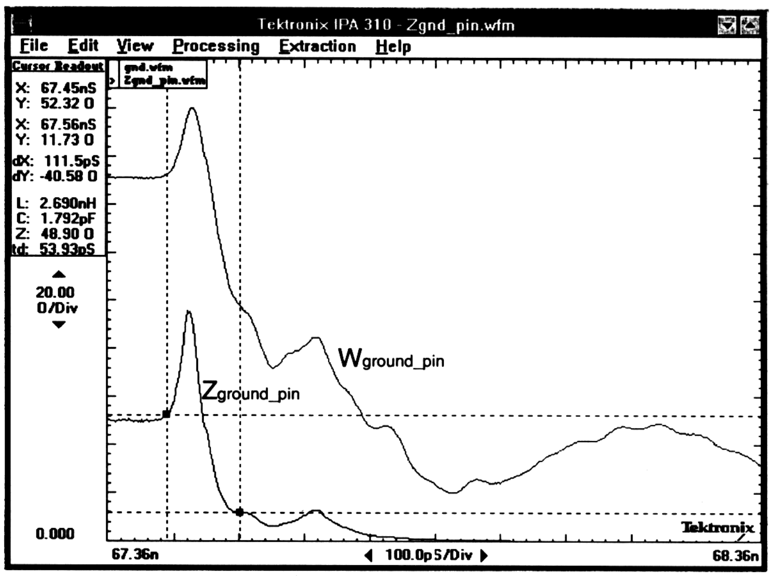


Figure 8. The TDR reflection waveform from the pin leading to internal ground plane is degraded by multiple reflections (top waveform). The extracted impedance profile (bottom waveform) clearly shows the pin inductance region (between cursors) followed by very low impedance of the internal ground plane. Cursor readout shows the ground pin inductance to be 2.69 nH.

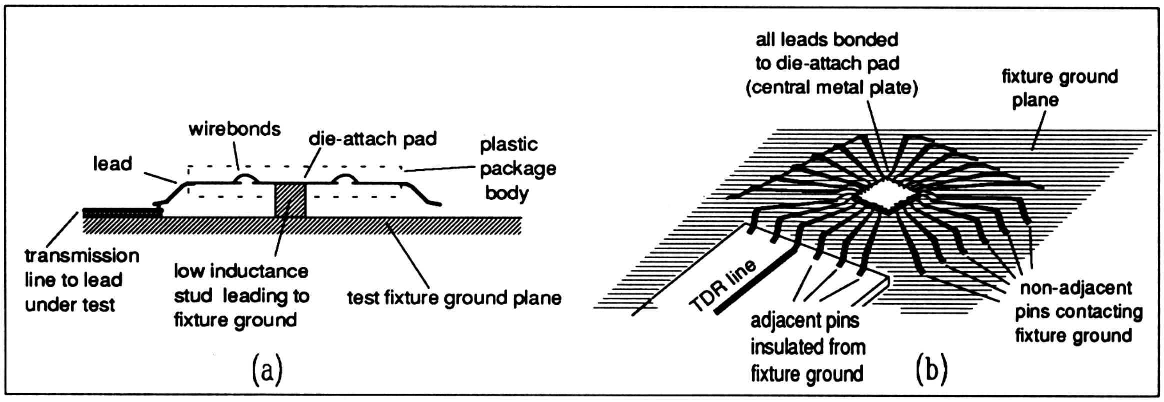


Figure 9. Two different ways of creating the ground return path for leadframe package inductance measurements. At left (a), the low inductance path is made by physically adding a low inductance connection to fixture ground plane. At right (b), the majority of the package pins are grounded, providing low inductance return path. In both cases, all the leads inside the package are connected to central metal plate.

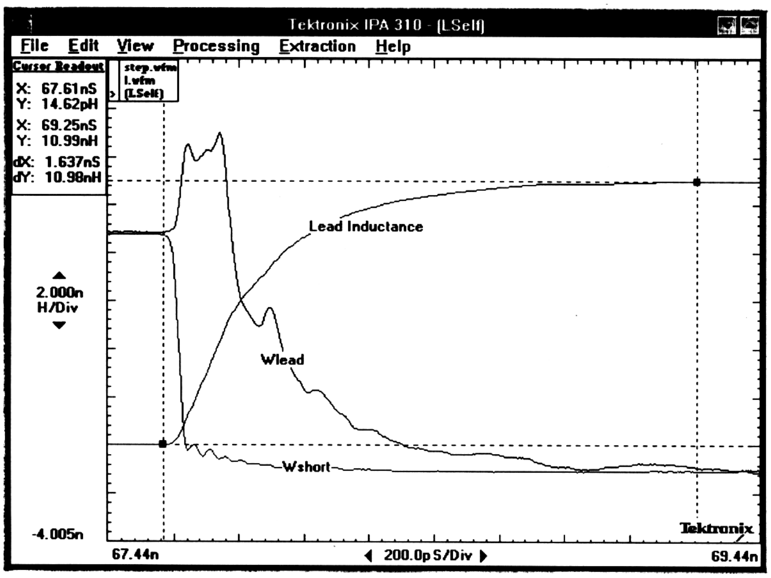


Figure 10. Lead inductance measurement with Coupled Lump method. Two waveforms are used: one obtained by shorting the test fixture end to ground, the other with the package lead grounded inside. The lead inductance curve is read asymptotically, intermediate inductance values on the curve have no meaning. The lead inductance in this case is 10.98 nH.

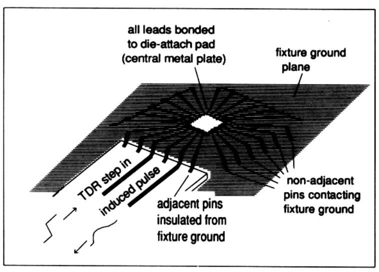


Figure 11. Measuring mutual inductance between two package leads. The mutual inductance is calculated from the induced pulse waveform. Adjacent pins should be insulated to avoid creating adjacent shunt loops which would alter inductances.

impedance profile function Z(t), shown in Figure 8. The ground lead inductance is obtained by integrating the Z(t) between the entrance to the package and the point where the impedance drops as the lead connects to the internal package ground plane (points marked with cursors in Figure 8, which also shows the value for the inductance). Note, again, how the impedance profile function Z(t) outlines lead features much more sharply than the TDR waveform W_{lead}, because the later is obscured by multiple reflections. Measurements like this can be a useful tool for analyzing power semiconductor interconnects [4].

Leadframe package model measurements

Leadframe packages, such as one shown in Figure 4, usually have leads which have strong inductive coupling to their neighbors, so the simple model extraction using distributed impedance won't work well. Remember, to extract the distributed impedance, the whole signal sent into a lead must be returned back, we cannot lose portions of the signal through coupling to other leads. However, when single-lump models provide adequate accuracy for simulation, there is a very good method to measure single-lump model parameters L and C using TDR. This is the Coupled Lump method (Appendix 2). Using this method, we can measure the self-inductance L of a lead, the mutual inductance Lm between any two leads, the total capacitance C of a lead and the mutual capacitance Cm between any two leads.

The lead inductance L:

To measure the lead inductance, we will apply the TDR signal to one end of the lead and ground the other end (Figure 9.). We will leave the neighboring leads open ended on one side (having them connected to passive 50 ohm transmission lines is permissible), so that coupled inductances do not interfere with the measurement. Like with the distributed impedance method described previously, we will acquire W_{lead} and W_{short} TDR waveforms, shown in Figure 10. The waveform W_{short} looks just like it did

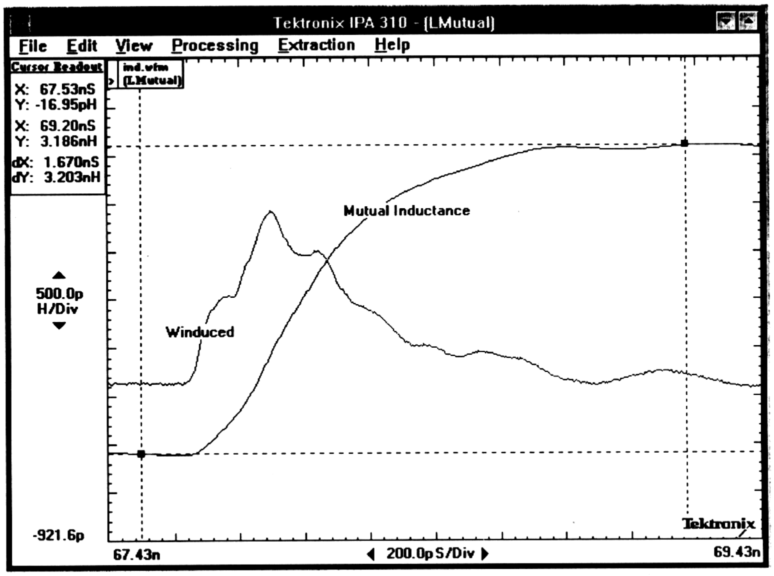


Figure 12. Mutual inductance is calculated from the area under the Winduced waveform. In this case, the mutual inductance was 3.2 nH. In these measurements, we always place the right hand cursor on the flat portion on the curve, where it has asymptotically converged.

before, but W_{lead} looks much different from W_{lead} in Figure 6. The reason for this is that the ground plane is relatively distant from the lead when the package is mounted in a fashion similar to that in which an end-user would mount the device in the circuit. Nevertheless, according to the Coupled Lump theory in Appendix 2, the inductance of the package is given by

$$L = \frac{Z_0}{2V_{step}} \int_0^{\infty} (W_{lead} - W_{short})dt$$

Here, V_{step} is the absolute value of amplitude of the reflected step determined from W_{short} (i.e., approximately 250 mV) Z_0 is the impedance of the TDR fixture lead (50 ohm). The integration above is carried from the beginning of waveforms to the point where the waveform W_{lead} has asymptotically reached the ground level. The waveforms W_{lead} and W_{short} should refer to the same time origin. If there is any drift present in the system, such as drift associated with instrument warm-up, these waveforms have to be acquired within a short time interval, before the drift had time to effect the measurement.

The critical aspect of this method is connecting one end of the lead to ground, which we casually mentioned before. With the test fixture which injects a TDR signal into package pins, this means grounding the inside end of the package lead. One way to conveniently prepare the package for doing this is to bond all the inside lead ends to the central metal plate in the package (the die attach plate). Then, we either drill a hole in the package body and connect the central plate to fixture ground with a low inductance metal post (Figure 10 (a)), or we can connect the majority of package leads to the fixture ground (Figure 10 (b)) (i.e., this includes all leads except for those adjacent to the lead under test. The adjacent leads have to remain open ended.). This latter way is very convenient to implement in practice and will produce adequate accuracy of measured values in most cases. Note that with this method of grounding leads, one bondwire will be in the inductance measuring loop so that bondwire inductance will be included in the single-lump inductance L.

Mutual inductance L_m:

To measure the mutual inductance L_m between any two leads of a package (the leads don't have to be adjacent), we, again, ground all the inside ends of package leads as described before. Then, we connect the TDR signal to one of the two leads and connect the other lead to the oscilloscope, using a 50 ohm transmission line, such as we use for TDR signals. We acquire the signal induced in the other lead $W_{induced}$ and determine the mutual inductance between the two leads as:

$$L_m = \frac{Z_0}{2V_{step}} \int_0^{\infty} (W_{induced})dt$$

Again, the leads adjacent to these measured should be open ended

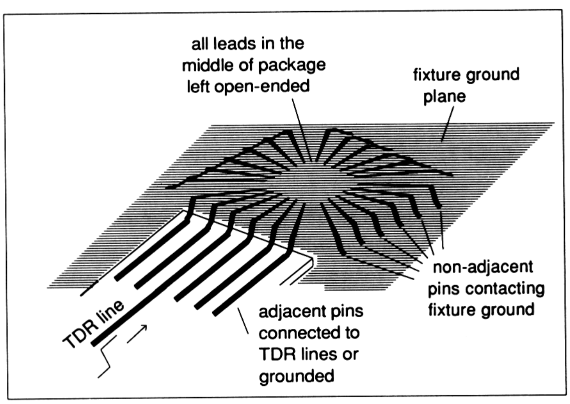


Figure 13. Measuring the capacitance of one lead to all others (including the capacitance to ground).

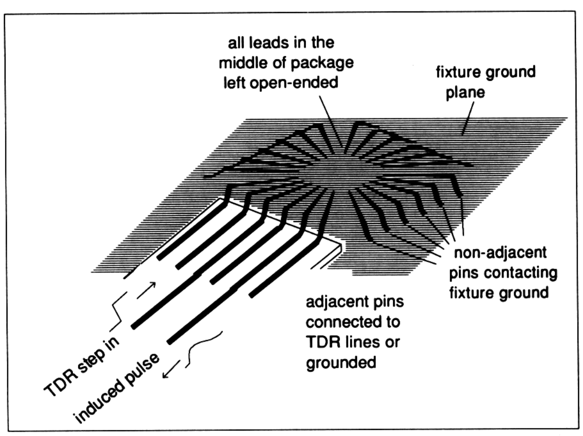


Figure 14. Mutual capacitance measurement between the two leads. All leads are open in the middle of the package, grounded or connected to TDR line around the periphery.

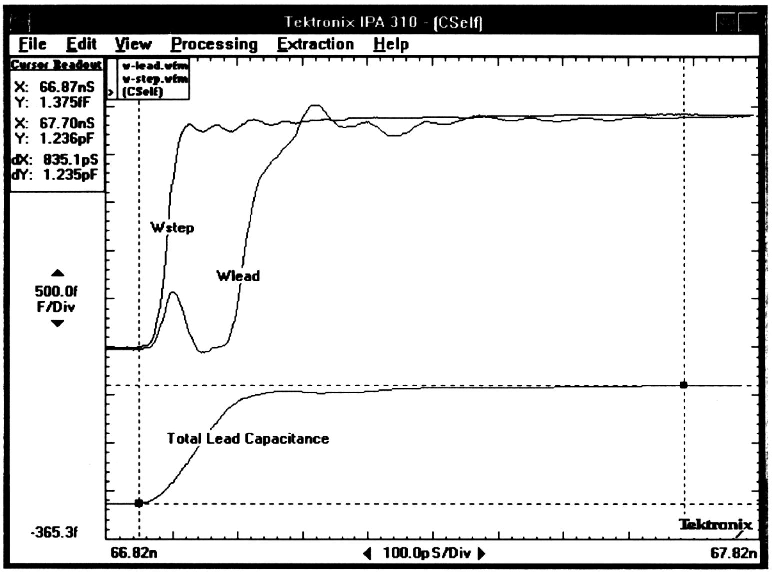


Figure 15. Capacitance of one lead to ground and all other leads. In capacitance measurements, the lead ends inside the package are open ended. All lead ends outside the package are either grounded or connected to 50 ohm transmission lines. Here, the capacitance is 1.235 pF.

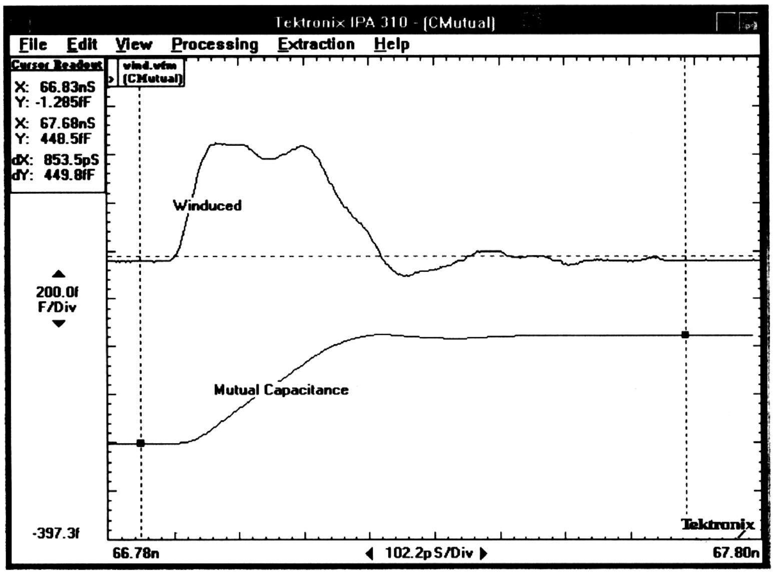


Figure 16. Mutual capacitance measurement between one lead and another lead. It is calculated from the area under the induced waveform. In this case, the mutual capacitance was 449 fF.

or connected to 50 ohm transmission lines, while all the other leads should contact the fixture ground plate so as to provide the low inductance current return path.

Total lead capacitance C:

For this measurement, we use a package which has all the leads open ended on the inside, as in Figure 13, (as compared to all the leads connected together on the inside for inductance measurements). The package should be positioned on the fixture so that the fixture ground plane is roughly in the same location the ground plane will be when the package is mounted in the circuit.

All the ends of leads outside the package, except for the lead under test, should be contact the fixture ground or to 50 ohm transmission line end. We acquire two waveforms, one with the lead under test connected to the TDR lead on the fixture, W_{lead}, and the other with the package removed from the fixture, W_{step}. The total lead capacitance will be:

$$C = \frac{1}{2Z_0 V_{step}} \int_0^{\infty} (W_{step} - W_{lead})\,dt$$

Mutual capacitance C_m:

This is the simplest measurement in the group. With the leads inside the package open ended, connect the TDR signal to one lead and acquire the induced signal $W_{induced}$ in the other lead. The mutual capacitance between the two leads is then:

$$C_m = \frac{1}{2Z_0 V_{step}} \int_0^{\infty} W_{induced}\,dt$$

The model we can construct for two coupled leads in a package can look like the one shown in Figure 17. It is important to note that the C_g in this model is not the capacitance of one electrode to all others found above, but C with all the mutual capacitances to other leads C_m subtracted.

One lead in Figure 17 will have mutual capacitance to the adjacent lead C_m of 0.449 (dY in Figure 16). The value for C_g is 0.33 pF, which is obtained from the total capacitance of 1.235 pF (dY in Figure 15) less two capacitances C_m of 0.449 pF from leads on each side. The lead inductance of 11 nH is obtained as dY in Figure 10, and the mutual inductance of 3.2 nH is obtained from Figure 13.

The two coupled lines model

This model is more complicated than the coupled lump model for L, L_m, C, C_m described above. We can use the coupled lines model when we wish to see how the mutual impedance is distributed along the lead length in a leadframe package. An example of this would be when we wish to know what portion of total inductance is contributed by the package pin, or what is the mutual inductance between pins (useful information for simulating ground bounce behavior). The assumptions making this model valid are

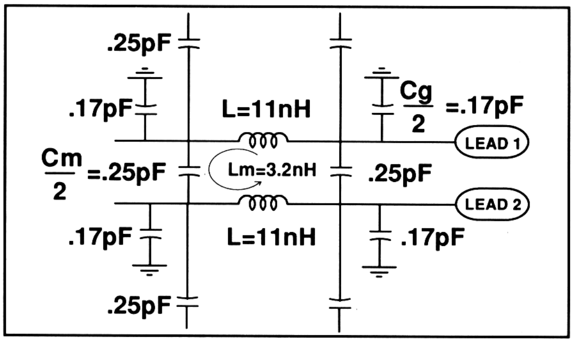


Figure 17. The equivalent model for leads in a leadframe package we can compose from the measurements. Just two leads out of the array are shown.

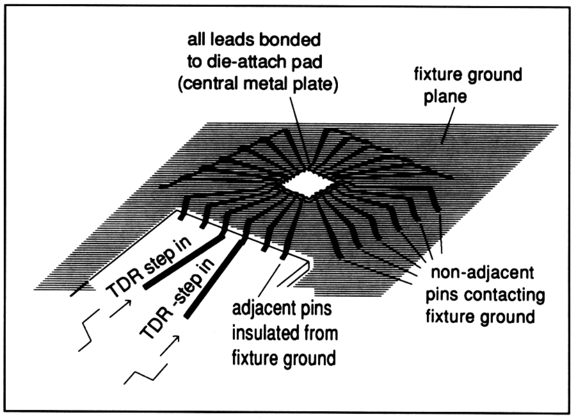


Figure 18. Arrangement to measure inductance variation in a lead using odd-even mode techniques. The odd-mode impedance is the impedance of one lead while the symmetrical lead is fed the opposite polarity pulse. Feeding the same polarity pulse yields even-mode impedance.

that the leads are mutually symmetrical and that neighboring leads' influence on measured model parameters is minimal. This latter assumption will be approximately valid when adjacent leads are left open-ended.

We will use the even and odd mode impedance concept [5] in the coupled lines model. The even mode impedance $Z_e(t)$ is the impedance of one line when the other line is supplied with an identical TDR signal of same polarity. The odd mode impedance $Z_o(t)$ is the impedance of one line when the other line is supplied with an identical signal of opposite polarity. To obtain $Z_e(t)$ and $Z_o(t)$, we acquire the waveforms W_{even}, W_{odd} and W_{short}, and use the algorithm for distributed impedance extraction we used before. The even and odd mode will, in general, propagate with slightly different velocities. To the extent that these velocities can be considered equal (again an approximation), the expressions for L, L_m, C, C_m along the pair of coupled transmission lines will be given by equations similar to equations used to extract lumped model parameters from distributed impedance:

$$L = \frac{1}{2}\int_{t2}^{t1} (Ze(t) + Zo(t))dt$$

$$Lm = \frac{1}{2}\int_{t2}^{t1} \left(Ze(t) - Zo(t)\right)dt$$

$$C = \frac{1}{2}\int_{t2}^{t1} \frac{1}{Ze(t)}dt$$

$$Cm = \frac{1}{2}\int_{t2}^{t1} \left(\frac{1}{Zo(t)} - \frac{1}{Ze(t)}\right)dt$$

Again, if we are interested in inductance, lead ends inside the package should be grounded and, if we are extracting capacitance, they should be open-ended.

An example where we separate the inductances of pins and the leads inside the package for a leadframe is shown in Figures 19 and 20. We found the even and odd impedance distribution using the process described above and then constructed the function $(Z_e(t)+Z_o(t)/2)$. In this function we can identify different zones corresponding to the pin and the reminder of the lead. The pin inductance can be found by integrating the function $(Z_e(t)+Z_o(t))/2$ in the region of the pin. The mutual inductance between the pins can be found by integrating $(Z_e(t)-Z_o(t))/2$.

The question arises: Why derive lumped models if a more accurate description of lead behavior (such as its distributed impedance) is known? The answer is that most simulators will readily handle lumped elements (such as L, L_m, C, C_m), while they have varying degrees of difficulty simulating circuits with coupled transmission lines.

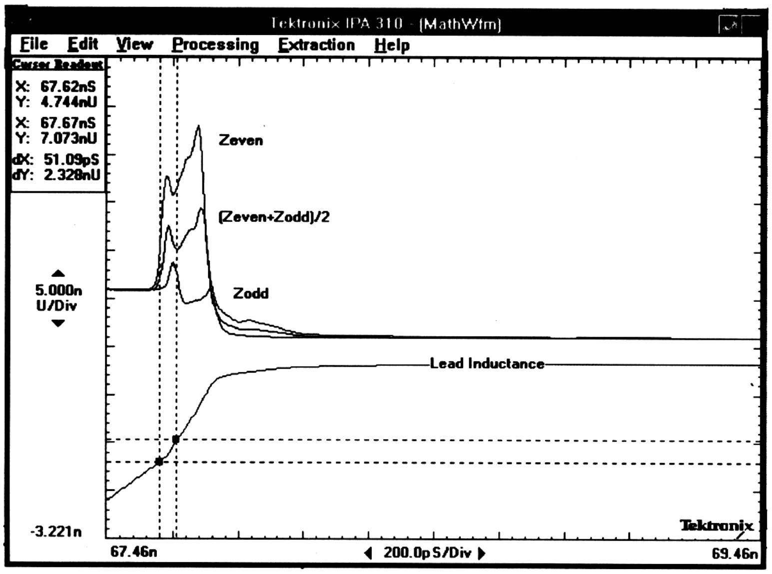


Figure 19. Finding the inductance of a lead segment inside the package using the odd and even impedance method. Integrating the average of Zeven and Zodd gives the inductance (lower curve). In this case, the package pin zone is selected with cursors, the inductance we can attribute to the pin is 2.3 nH.

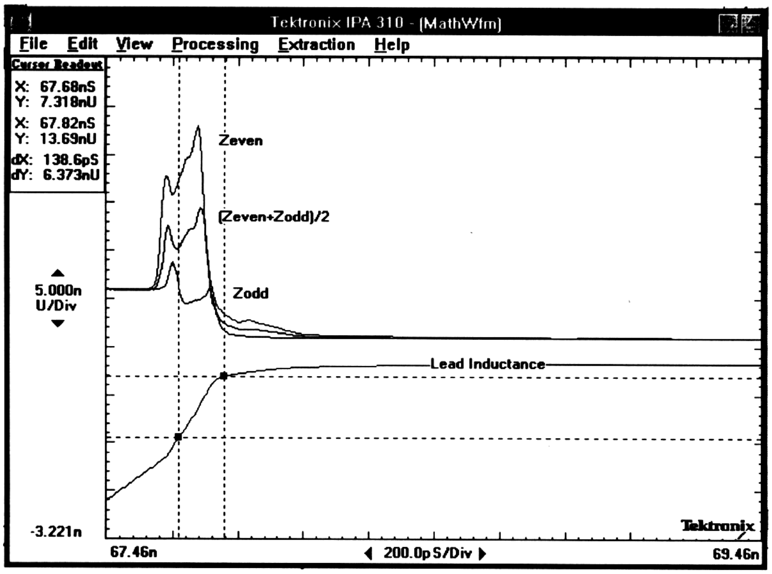


Figure 20. Here we are measuring with cursors the inductance between the package pin and the end of the lead inside the package. The average impedance curve shows that the impedance is climbing in this region, because the lead in this package is tapering as it approaches the center. The leads were connected to the ground in the middle, so the impedance there drops. The measured inductance of the tapered lead section is 6.3 nH.

References

[1] A. Buckstein, T. Kailath, "An Inverse Scattering Framework for Several Problems in Signal Processing", IEEE ASSP Magazine, pp. 6-20, Jan. 1987.

[2] L.A. Hayden, J.M. Jong, J.B. Rettig and V.K. Tripathi, "Measurement and Characterization of Multiple Coupled Interconnection Lines in Hybrid and Monolithic Integrated Circuits", SPIE Proceedings of International Symposium on Advances in Interconnects and Packaging, vol. 1389, pp. 205-214, Nov. 1989.

[3] J.M. Jong, V.K. Tripathi and B. Janko, "Equivalent Circuit Modeling of Interconnects from Time Domain Measurements", Proceedings of 42nd Electronic Components and Technology Conference, San Diego, May 1992.

[4] B. Janko and P. Decher, "Measuring Package and Interconnect Model Parameters Using Distributed Impedance", Proc. 40th ARFTG Conference, Orlando, Fla., Dec. 1992.

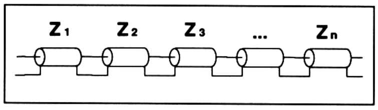
[5] R. Lewallen, "Establishing the Basis for Differential TDR Measurements with the 11800 Series Oscilloscopes", Tektronix Handshake, Spring 1990.

Appendix 1

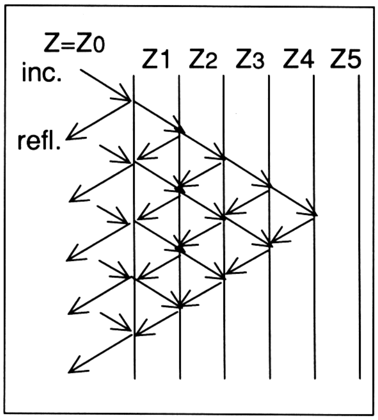
Impedance Profile and LCZ Extraction

Notation

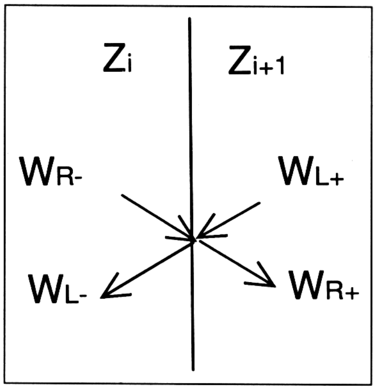
Let's consider a multisection DUT. We shall divide the DUT impedance into n sections of equal length, as shown below.



Our assumption is that a TDR instrument is connected to the DUT via lossless transmission line, so no multiple reflections take place between the TDR cable and the DUT. The signal propagation through our structure can then be depicted in the lattice diagram below:



The layer peeling algorithm breaks the incoming and the outgoing waveform into impulse trains and reconstructs the impedance profile from propagation of these trains across impedance section boundaries. For each boundary i, there is one impedance section Z_i on the left and one section Z_{i+1} on the right. On the left of the boundary, there is a signal W_{R-} traveling to the right and a signal W_{L-} traveling to the left. There are also corresponding signals W_{R+} and W_{L+} on the right side of the boundary. In general, we shall denote the signals with direction traveling to the left by index L and those traveling to the right by index R. We shall denote the signals found on the left side of the boundary with index –, and signals found on the right hand side by index +. This is illustrated in the following diagram:



Employing the reflection coefficients for impedance boundaries

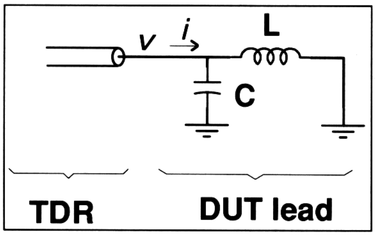
$$\rho = \frac{Z_{i+1} - Z_i}{Z_{i+1} + Z_i}$$

and applying the diagram successively for each boundary, we obtain the sequence of impedance segments Z_1, Z_2, Z_3, Z_4, which, for uniform time increment for all segments define the impedance profile Z(t). (For details how this is done see Tektronix Application Note: "Z-profile Algorithm".)

Coupled Lumps

L measurements

For inductance measurements of an interconnect lead attached to a TDR line, the lead is connected to ground at one end. The single-lump LC model of this can be depicted as shown below.



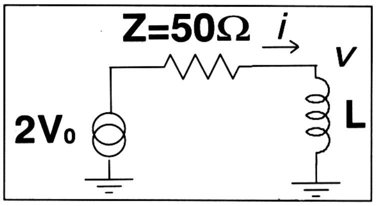
The voltage υ , caused by current i flowing through the DUT lead will be

$$i = \upsilon\left(j\omega C + \frac{1}{j\omega L}\right)$$

As the frequency ω decreases, the term jωC will become negligible and, in the limit, the current will be determined solely by the inductance

$$i = \upsilon\frac{1}{j\omega L}$$

Solving the equivalent circuit



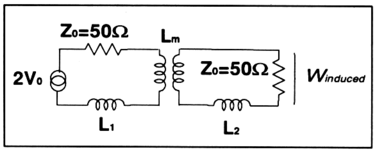
for TDR, we obtain for L

$$L = \frac{Z_0}{2V_{step}}\int_0^{\infty}(W_{lead} - W_{short})dt$$

where W_{lead} is the TDR reflection from the DUT and W_{short} is the reflection from the TDR line shorted.

Mutual inductance

The equivalent circuit for coupled lumps looks like this:



Solving the circuit equations, we get for mutual inductance

$$L_m = \frac{Z_0}{2V_{step}}\int_0^{\infty}(W_{induced})dt$$

C and Cm

Applying reasoning similar to that used above, we get the expressions for capacitances in the limit

$$C = \frac{1}{2Z_0V_{step}}\int_0^{\infty}(W_{step} - W_{lead})dt$$

$$C_m = \frac{1}{2Z_0V_{step}}\int_0^{\infty}W_{induced}dt$$

W_{step} above is the reflection from the open end of the fixture.

For further information, contact:

U.S.A., Africa, Asia, Australia, Central & South America, Japan
Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077-0001
For additional literature, or the address and phone number of the Tektronix Sales Office or Representative nearest you, contact: (800) 426-2200

Belgium: Brussels
Phone: 32(2) 725 96 10
FAX: 32(2) 725 99 53

Canada: Barrie
Phone: (705) 737-2700
FAX: (705) 737-5588

Denmark: Copenhagen
Phone: 45 44 53 54 55
FAX: 45 44 53 07 55

Eastern Europe, Middle East, and Austria
Tektronix Ges.m.b.H.
Doerenkampgasse 7
A-1100 Vienna, Austria
Phone: 43(222) 68-66-02-0
FAX: 43(222) 68-66-00

Finland: Helsinki
Phone: 358(0) 7282 400
FAX: 358(0) 7520033

France and North Africa
Tektronix S.A.
ZAC Courtaboeuf, 4 Av du Canada
B.P.13
91941 Les Ulis Cedex, France
Phone: 33(1) 69 86 81 81
FAX: 33(1) 69 07 09 37

Germany: Koeln
Phone: 49 (221) 96969-0
FAX: 49 (221) 96969-362

Italy: Milan
Phone: 39(2) 84441
FAX: 39(2) 8950-0665

Japan: Tokyo
Phone: 81(3) 3448-4611
FAX: 81(3) 3444-0318

The Netherlands: Hoofddorp
Phone: 31(2503) 13300
FAX: 31(2503) 37271

Norway: Oslo
Phone: 47(2) 165050
FAX: 47(2) 165052

Spain: Madrid
Phone: 34 (1) 404.1011
FAX: 34 (1) 404.0997

Sweden: Stockholm
Phone: 46(8) 29 21 10
FAX: 46(8) 98 61 05

Switzerland: Zug
Phone: 41(42) 219192
FAX: 41(42) 217784

U.K.: Marlow
Phone: 44 (0628) 486000
FAX: 44 (0628) 47 4799

Tektronix sales and service offices around the world: Algeria, Argentina, Australia, Austria, Bahrain, Bangladesh, Belgium, Bolivia, Brazil, Bulgaria, Canada, Chile, People's Republic of China, Colombia, Costa Rica, Cyprus, Czechoslovakia, Denmark, Ecuador, Egypt, Finland, France, Germany, Greece, Hong Kong, Iceland, India, Indonesia, Ireland, Israel, Italy, Ivory Coast, Japan, Jordan, Korea, Kuwait, Lebanon, Malaysia, Mexico, The Netherlands, New Zealand, Nigeria, Norway, Oman, Pakistan, Panama, Peru, Philippines, Poland, Portugal, Saudi Arabia, South Africa, Singapore, Spain, Sri Lanka, Sweden, Switzerland, Taiwan, Thailand, Tunisia, Turkey, United Arab Emirates, United Kingdom, Uruguay, Venezuela, Zimbabwe.

5/93 XBS 10M 85W-8885-0

Tektronix