CHAPTER 9: POWER MANAGEMENT

SECTION 9.3: SWITCHED CAPACITOR VOLTAGE CONVERTERS

CHAPTER 9: POWER MANAGEMENT

Introduction

All electronic systems require power supplies to operate. This part of the system design is often overlooked. But, as discussed in the amplifier section on PSRR (Power Supply Rejection Ratio), the AC component of the power supply (noise) may add to the output of the amplifier. And the PSRR has a strong frequency dependence, falling as frequency increases. The supply voltage(s) must be kept as quiet as possible for optimum performance of high performance circuits. Local decoupling helps—but it is not sufficient.

Power management broadly refers to the generation and control of regulated voltages required to operate an electronic system. It encompasses much more than just power supply design. Today's systems require power supply design be integrated with the system design in order to maintain high efficiency. In addition, distributed power supply systems require localized regulators at the PC board level, thereby requiring the design engineer to master at least the basics of both switching and linear regulators.

Integrated circuit components such as switching regulators, linear regulators, switched capacitor voltage converters, and voltage references are typical elements of power management.

Historically, the standard for supply voltages was ±15 V. In recent years the trend is towards lower supply voltages. This is partially due to the processes used to manufacture integrated circuits. Circuit speeds have increased. One of the enabling technologies of this increase is the reduction of size of the transistors used in the process. These smaller feature sizes imply lower breakdown voltages, which, in turn, indicate lower supply voltages.

Another trend in power management is the often misguided attempt to operate the analog and digital circuitry on the same supply, eliminating one of the supplies. While the supply voltages may be the same, the low noise requirement is at odds with the often very noisy digital supply.

While reducing the supply voltage has the very desirable effect of reducing the power dissipation of digital circuits, lowering the supply of linear circuits limits the dynamic range of the signal. And, unfortunately, lowering the signal swing (the upper end of the dynamic range) by lowering the supply voltage does not imply that the noise level (the lower end of the signal dynamic range) will be reduced by a like amount.

Another trend in power management is the adoption of unipolar (single) supplies. This is often done in the attempt to eliminate the negative supply. Often, a negative supply is cheaper and provides better performance. This is due to the extra circuitry required for level shifting and ac coupling required by a single supply.

Notes:

SECTION 1: LINEAR VOLTAGE REGULATORS

Linear Regulator Basics

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5 V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from less than 1 V to 24 V, handling output currents from as low as 25 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. One reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. Because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required an unregulated input 2 V or more above the regulated output voltage, making them lossy in power terms. Typical maximum efficiency for a 5 V supply is 71%, meaning 29% of the power is dissipated in the regulator.

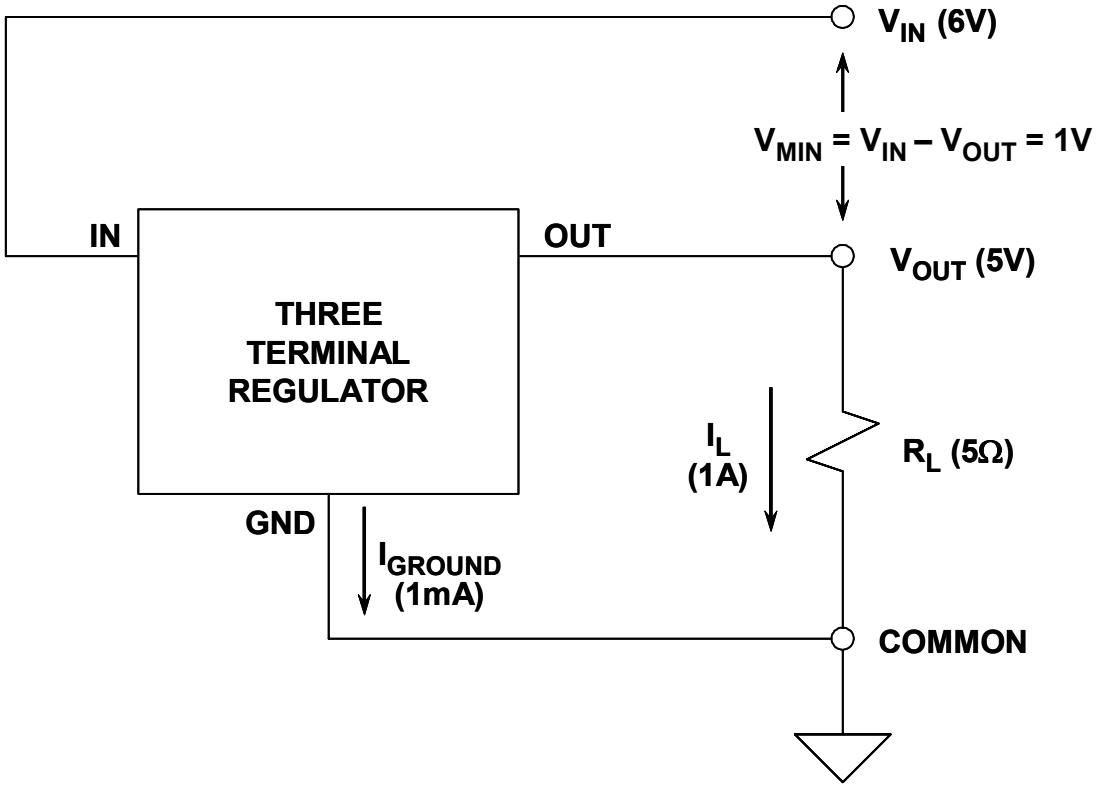

Figure 9.1: *A Basic Three Terminal Voltage Regulator*

Figure 9.1 also allows a more detailed analysis of power losses in the regulator. There are two components to power which are dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second which is a function of V_{IN} and Iground. If we call the total power P_D, this then becomes:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(\text{Iground}). \qquad \text{Eq. 9-1}$$

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 9.2.

In this diagram virtually all of the elements shown are fundamentally necessary, the exceptions being the shutdown control and saturation sensor functions (shown dotted). While these are present on many current regulators, the shutdown feature is relatively new as a standard function, and certainly isn't part of standard three-terminal regulators. When present, shutdown control is a logic level controllable input. The optional error output, $\overline{ERR}$, is useful within a system to detect regulator overload, such as saturation of the pass device, thermal overload, etc. The remaining functions shown are always part of an IC power regulator. While this diagram shows the blocks in a conceptual way, actual implementation may vary.

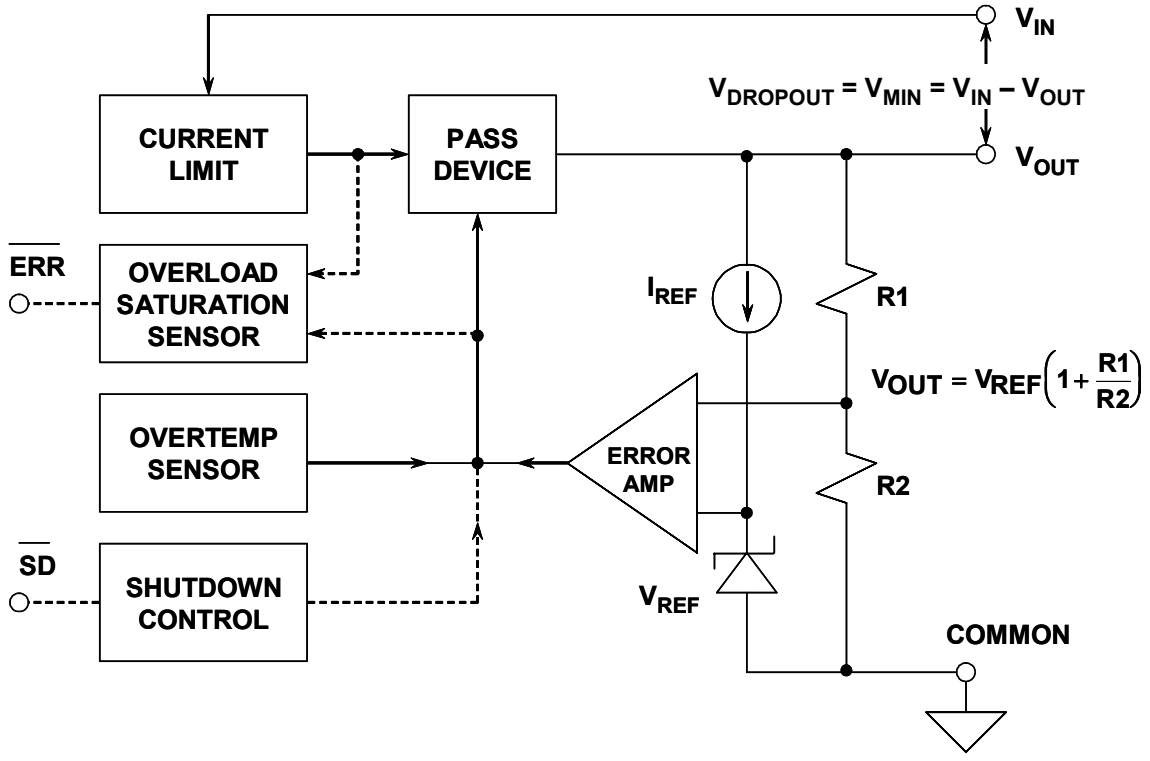

Figure 9.2: *Block Diagram of a Voltage Regulator*

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a band gap based voltage, typically ~1.2 V. This voltage is presented to one input of an error amplifier, with the other input connected to the V_{OUT} sensing divider, R1 & R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right). \qquad \text{Eq. 9-2}$$

When standby power is critical, several design steps will be taken. The resistor values of the divider will be high, the error amplifier and pass device driver will be low power, and the reference current I_{REF} will also be low. By these means the regulator's unloaded standby current can be reduced to a mA or less using bipolar technology, and to only a few μA in CMOS parts. In regulators which offer a shutdown mode, the shutdown state standby current may be reduced to 1 μA or less.

Nearly all regulators will have some means of current limiting and over temperature sensing, to protect the pass device against failure. Current limiting is usually implemented by a series sensing resistor for high current parts, or alternately by a more simple drive current limit to a controlled β pass device (which achieves the same end). For higher voltage circuits, this current limiting may also be combined with voltage limiting, to provide complete load line control for the pass device. All power regulator devices will also have some means of sensing excessive temperature, usually by means of a fixed reference voltage and a V_{BE}-based sensor monitoring chip temperature. When the die temperature exceeds a dangerous level (above ~150°C), this can be used to shutdown the chip, by removing the drive to the pass device. In some cases an error flag output may be provided to warn of this shutdown (and also loss of regulation from some other means).

Pass Devices and Their Associated Trade-offs

The discussion thus far has not treated the pass device in any detail. In practice, this major part of the regulator can actually take on quite a number of alternate forms. Precisely which type of pass device is chosen has a major influence on almost all major regulator performance issues. Most notable among these is the dropout voltage, V_{MIN}.

It is difficult to fully compare all of the devices from their schematic representations, since they differ in so many ways beyond their applicable dropout voltages. For this reason, the chart of Figure 9.4 is useful.

This chart compares the various pass elements in greater detail, allowing easy comparison between the device types, dependent upon which criteria is most important. Note that columns A to E correspond to the schematics of Figure 9.3a to 9.3e. Note also that the pro/con comparison items are in *relative* terms, as opposed to a hard specification limit for any particular pass device type.

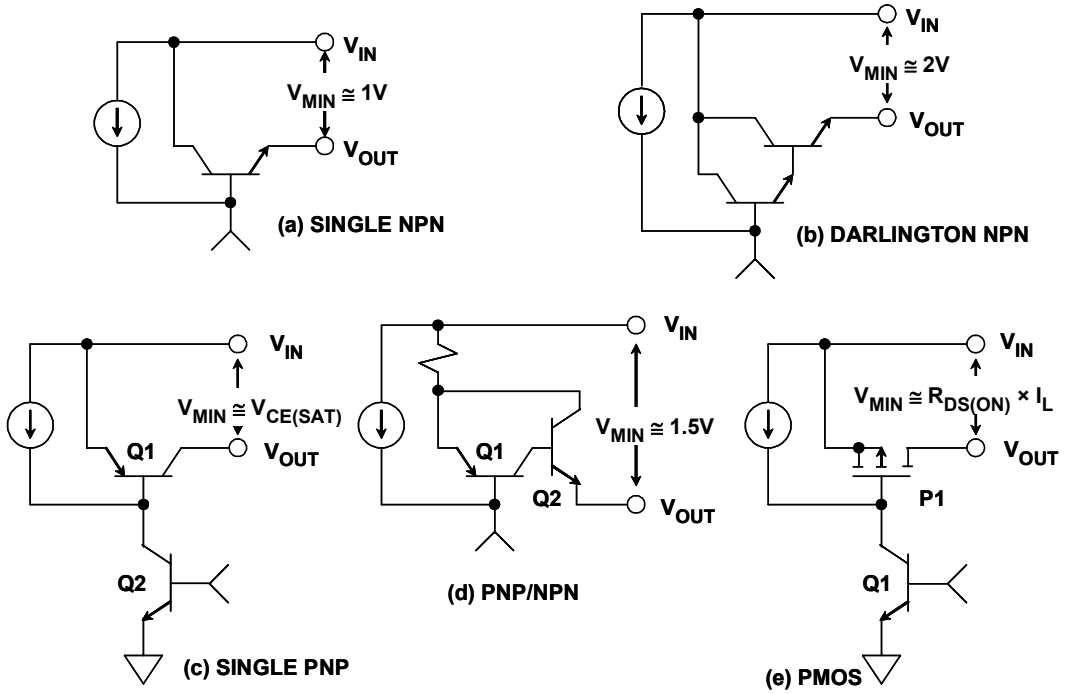

Figure 9.3: *Pass Devices Useful in Voltage Regulators*

A SINGLE NPN	B DARLINGTON NPN	C SINGLE PNP	D PNP/NPN	E PMOS
V_{MIN} ~ 1V	V_{MIN} ~ 2V	V_{MIN} ~ 0.1V	V_{MIN} ~ 1.5V	V_{MIN} ~ $R_{DS(ON)}$× I_L
I_L < 1A	I_L > 1A	I_L < 1A	I_L > 1A	I_L > 1A
Follower	Follower	Inverter	Inverter	Inverter
Low Z_{OUT}	Low Z_{OUT}	High Z_{OUT}	High Z_{OUT}	High Z_{OUT}
Wide BW	Wide BW	Narrow BW	Narrow BW	Narrow BW
C_L Immune	C_L Immune	C_L Sensitive	C_L Sensitive	C_L Sensitive

Figure 9.4: *Pros and Cons of Voltage Regulator Pass Devices*

For example, it can be seen that the all NPN pass devices of columns A and B have the attributes of a follower circuit, which allows high bandwidth and provides relative immunity to cap loading because of the characteristic low Z_{OUT}.

All of the three connections C/D/E have the characteristic of high output impedance, and require an output capacitor for stability. The fact that the output cap is part of the regulator frequency compensation is a most basic application point, and one which needs to be clearly understood by the regulator user. This factor, denoted by "C_L sensitive", makes regulators using them generally critical as to the exact C_L value, as well as its ESR (equivalent series resistance). Typically this type of regulator must be used only with a specific size as well as type of output capacitor, where the ESR is stable and predictable with respect to both time and temperature to fully guarantee regulator stability. Some recent Analog Devices LDO IC circuit developments have eased this burden on the part of the regulator user a great deal, and will be discussed below in further detail.

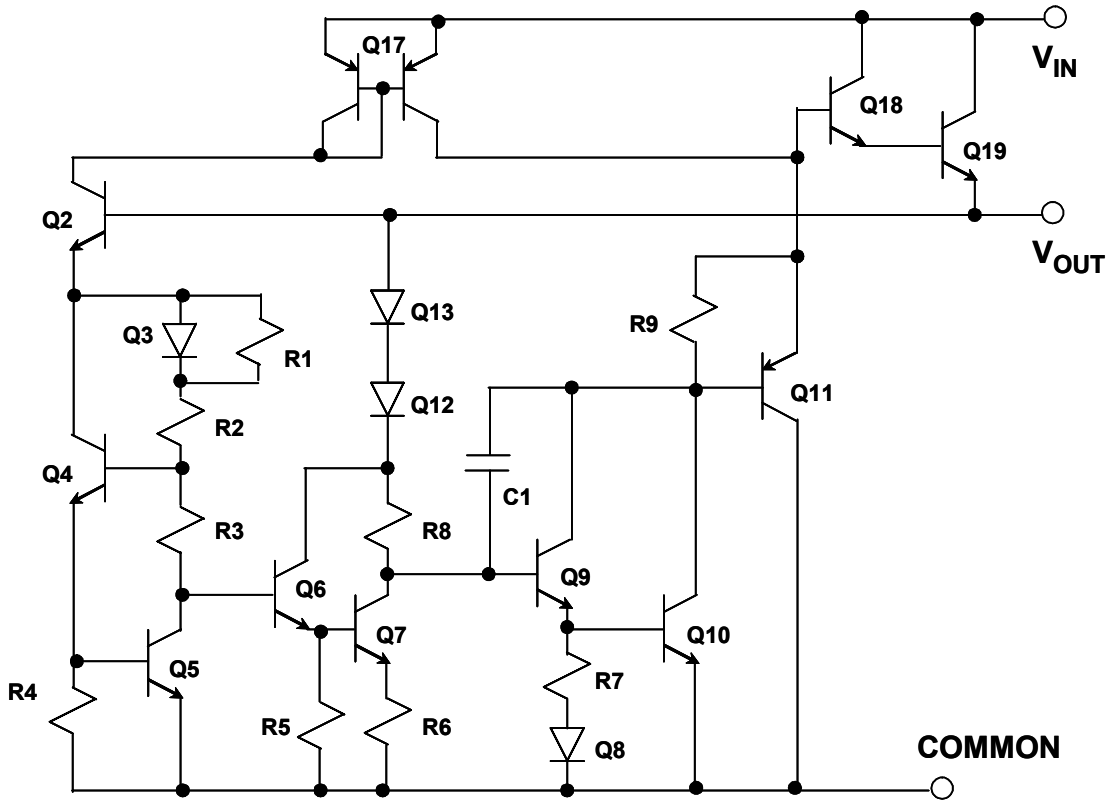

Figure 9.5: *Simplified Schematic of a LM309 Fixed 5 V/1 A Three Terminal Regulator*

The classic LM309 5 V /1 A three-terminal regulator (see Reference 1) was the originator in a long procession of linear regulators. This circuit is shown in much simplified form in Figure 9.5, with current limiting and over temperature details omitted. This IC type is still in standard production today, not just in original form, but in family derivatives such as the 7805, 7815 etc., and their various low and medium current alternates. Using a Darlington pass connection for Q18 to Q19, the design does not have low dropout characteristics (~1.5 V typical minimum), or for low quiescent current (~5 mA). It is

however relatively immune to instability issues, due to the internal compensation of C1, and the buffering of the emitter follower output. This helps make it easy to apply.

Later developments in references and three-terminal regulation techniques led to the development of the voltage adjustable regulator. The original IC to employ this concept was the LM317 (see Reference 2), which is shown in simplified schematic form in Figure 9.6. Note that this design does not use the same ΔV_{BE} form of reference as in the LM309. Instead, Q17 to Q19, etc. are employed as a form of a Brokaw band gap reference cell (Reference 3).

This adjustable regulator bootstraps the reference cell transistors Q17 to Q19 and the error amplifier transistors Q16 to Q18. The output of the error amplifier drives Darlington pass transistors Q25 to Q26, through buffer Q12. The basic reference cell produces a fixed voltage of 1.25 V, which appears between the V_{OUT} and ADJ pins of the IC as shown. External scaling resistors R1 and R2 set up the desired output voltage, which is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + 50\mu A \times R2 \,. \qquad \text{Eq. 9-3}$$

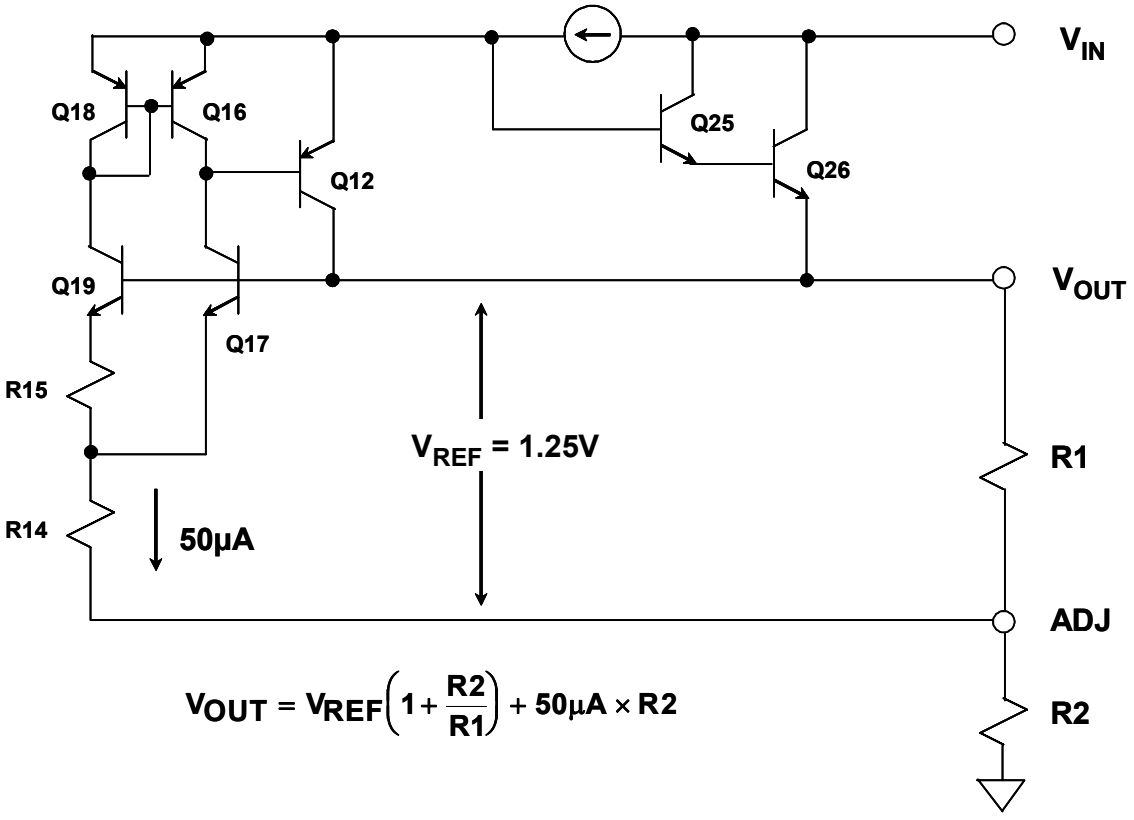

Figure 9.6: *Simplified Schematic of a LM317 Adjustable Three terminal Regulator*

As can be noted, the voltage output is a scaling of V_{REF} with R2 and R1, plus a small voltage component which is a function of the 50 μA reference cell current. Typically, the R1 and R2 values are chosen to draw > 5 mA, making the offset current term relatively small by comparison. The design is internally compensated, and in many applications will not necessarily need an output bypass capacitor to insure stability. But in most cases you will still want to use one—see the section on decoupling.

Like the LM309 fixed voltage regulator, the LM317 series has relatively high dropout voltage, due to the use of Darlington pass transistors. It is also not a low power IC (quiescent current typically 3.5 mA). The strength of this regulator lies in the wide range of user voltage adaptability it allows.

Low Dropout Regulator Architectures

In many systems it is desirable to have a linear regulator with low input—output differential. This allows for reduced power dissipation. It also allows for declining input voltage (such as a discharging battery). This is known as a low dropout regulator (LDO). As has been shown thus far, all LDO pass devices have the fundamental characteristics of operating in an inverting mode. This allows the regulator circuit to regulate down to the pass device saturation (but if saturation is reached, the circuit is no longer a regulator), and thus low dropout. A by-product of this mode of operation is that this type of topology will necessarily be more susceptible to stability issues. This is due to the higher output impedance of the inverting pass devices, relative to the follower configurations. This higher impedance, combined with the impedance of the output capacitor can move the second pole of the system too far in, causing instability and possible oscillations. These basic points give rise to some of the more difficult issues with regard to LDO performance. In fact, these points influence both the design and the application of LDOs to a very large degree, and in the end, determine how they are differentiated in the performance arena.

A traditional LDO architecture is shown in Figure 9.7, and is generally representative of actual parts employing either a PNP pass device as shown, or alternately, a PMOS device. There are both dc and ac design and application issues to be resolved with this architecture, which are now discussed.

In dc terms, perhaps the major issue is the type of pass device used, which influences dropout voltage and ground current. If a lateral PNP device is used for Q1, the β will be low, sometimes only on the order of 10 or so. Since Q1 is driven from the collector of Q2, the relatively high base current demanded by a lateral PNP results in relatively high emitter current in Q2, or a high Iground. For a typical lateral PNP based regulator operating with a 5 V / 150 mA output, Iground will be typically ~18 mA, and can be as high as 40 mA. To compound the problem of high Iground in PNP LDOs, there is also the “spike” in Iground, as the regulator tries to regulate down to the dropout region. Under such conditions, the output voltage is out of tolerance, and the regulation loop requires higher drive to the pass device, in an unsuccessful attempt to maintain loop regulation. This results in a substantial spike upward in Iground, which is typically internally limited by the regulator’s saturation control circuits.

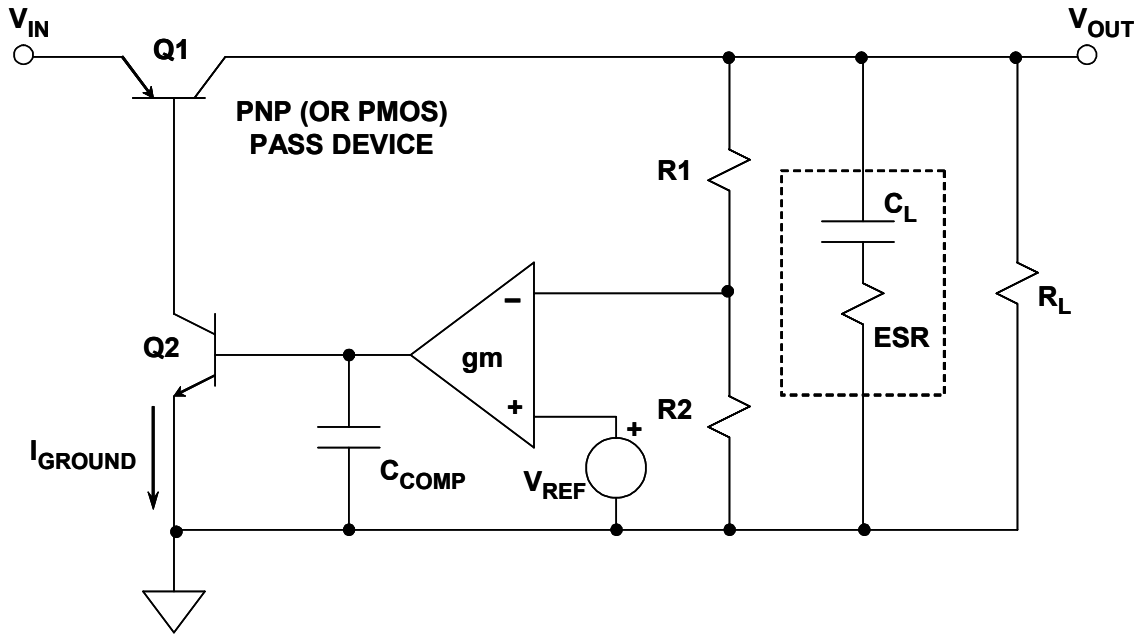

Figure 9.7: *Traditional LDO Architecture*

PMOS pass devices do not demonstrate a similar current spike in Iground, since they are voltage controlled. But, while devoid of the Iground spike, PMOS pass devices do have some problems of their own. Problem number one is that high quality, low R_{ON}, low threshold PMOS devices generally aren't compatible with many IC processes. This makes the best technical choice for a PMOS pass device an external part, driven from the collector of Q2 in the figure. This introduces the term "LDO controller", where the LDO architecture is completed by an external pass device. While in theory NMOS pass devices would offer lower R_{ON} choice options, they also demand a boosted voltage supply to turn on, making them impractical for a simple LDO. PMOS pass devices are widely available in both low R_{ON} and low threshold forms, with current levels up to several amperes. They offer the potential of the lowest dropout of any device, since dropout can always be lowered by picking a lower R_{ON} part.

The dropout voltage of lateral PNP pass devices is typically around 300 mV at 150 mA, with a maximum of 600 mV. These performance levels are considerably bettered in regulators using vertical PNPs, which have a typical β of ~150 at currents of 200 mA. This corresponds to an Iground of 1.3 mA at the 200 mA output current. The dropout voltage of vertical PNPs is also an improvement vis-à-vis that of the lateral PNP regulator, and is typically 180 mV at 200 mA, with a maximum of 400 mV.

There are also major ac performance issues to be dealt with in the LDO architecture of Figure 9.7. This topology has an inherently high output impedance, due to the operation of the PNP pass device in a common-emitter (or common-source with a PMOS device) mode. In either case, this factor causes the regulator to appear as a high source impedance to the load.

The internal compensation capacitor of the regulator, C_{COMP}, forms a fixed frequency pole, in conjunction with the g_m of the error amplifier. In addition, load capacitance C_L forms an output pole, in conjunction with R_L. This particular pole, because it is a second (and sometimes variable) pole of a two-pole system, is the source of a major LDO application problem. The C_L pole can strongly influence the overall frequency response of the regulator, in ways that are both useful as well as detrimental. Depending upon the relative positioning of the two poles in the frequency domain, along with the relative value of the ESR of capacitor C_L, it is quite possible that the stability of the system can be compromised for certain combinations of C_L and ESR. Note that C_L is shown here as a real capacitor, which is actually composed of a pure capacitance plus the series parasitic resistance ESR.

If the two poles of such a system are widely separated in terms of frequency, stability may not be a serious problem. The emitter-follower output of a classic regulator like the LM309 is an example with widely separated pole frequencies, as the very low Z_{OUT} of the NPN follower pushes the output pole due to load capacitance far out in frequency, where it does little harm. The internal compensation capacitance (C1 of Figure 9.5) then forms part of a *dominant pole*, which reduces loop gain to below unity at the much higher frequencies where the second (output) pole does occur. Thus stability is not necessarily compromised by load capacitance in this type of regulator.

By their nature however, LDOs simply can't afford the luxury of emitter follower outputs, they must instead operate with pass devices capable of saturation. Thus, given the existence of two or more poles (one or more internal and another formed by external capacitance) there is the potential for the cumulative phase shift to exceed 180° before the gain drops to unity, thus causing oscillations. The potential for instability under certain output loading conditions is, for better or worse, a fact-of-life for most LDO topologies.

However, the very output capacitor which gives rise to the instability can, in certain circumstances, also be the solution to the same instability. This seemingly paradoxical situation can be appreciated by realizing that all practical capacitors are actually a series combination of the capacitance C_L and the parasitic resistance, ESR. While load resistance R_L and C_L do form a pole, C_L and its ESR also form a zero. The effect of the zero is to mitigate the de-stabilizing effect of C_L for certain conditions. For example, if the pole and zero in question are appropriately placed in frequency relative to the internal regulator poles, some of the deleterious effects can be made to essentially cancel. The basic challenge with this approach to stability is simply that the capacitor's ESR, being a parasitic term, is not well controlled. As a result, LDOs which depend upon output pole-zero compensation schemes must very carefully limit the capacitor ESR to certain *zones*, such as shown by Figure 9.8.

A zoned ESR chart such as this is meant to guide the user of an LDO in picking an output capacitor which confines ESR to the stable region, i.e., the central zone, for all operating conditions. Note that this generic chart is not intended to portray any specific device, just the general pattern. Finding a capacitor that guarantees min and max ESR (especially over temperature). This effectively means that general purpose aluminum electrolytic are

prohibited from use, since they deteriorate (increase) in terms of ESR at cold temperatures. Very low ESR types such as OS-CON or multilayer ceramic units have ESRs which are too low for use. While they could in theory be padded up into the stable zone with external resistance, this would hardly be a practical solution. This leaves tantalum types as the best all around choice for LDO output use. Finally, since a large capacitor value is likely to be used to maximize stability, this effectively means that the solution for an LDO such as Figure 9.8 must use a more expensive and physically large tantalum capacitor. This is not desirable if small size is a major design criteria.

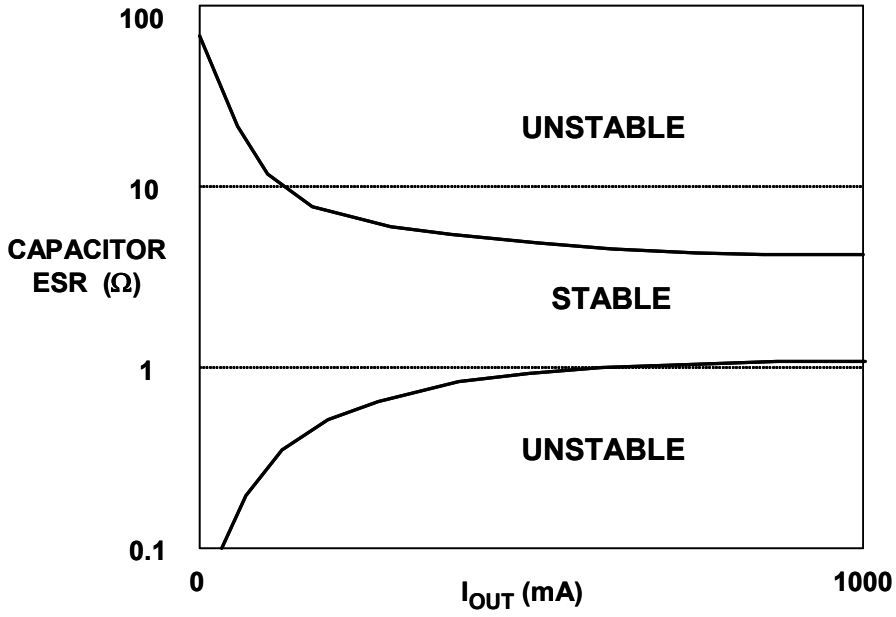

Figure 9.8: *Zoned Load Capacitor ESR Can Make LDO Applications a Nightmare*

The anyCAP Low Dropout Regulator Family

Some novel modifications to the basic LDO architecture of Figure 9.7 allow major improvements in terms of both dc and ac performance. These developments are shown schematically in Figure 9.9, which is a simplified diagram of the Analog Devices ADP330X series LDO regulator family. These regulators are also known as the anyCAP® family, so named for their relative insensitivity to the output capacitor in terms of both size and ESR. They are available in power efficient packages such as the Thermal Coastline (discussed below), in both stand-alone LDO and LDO controller forms, and also in a wide span of output voltage options.

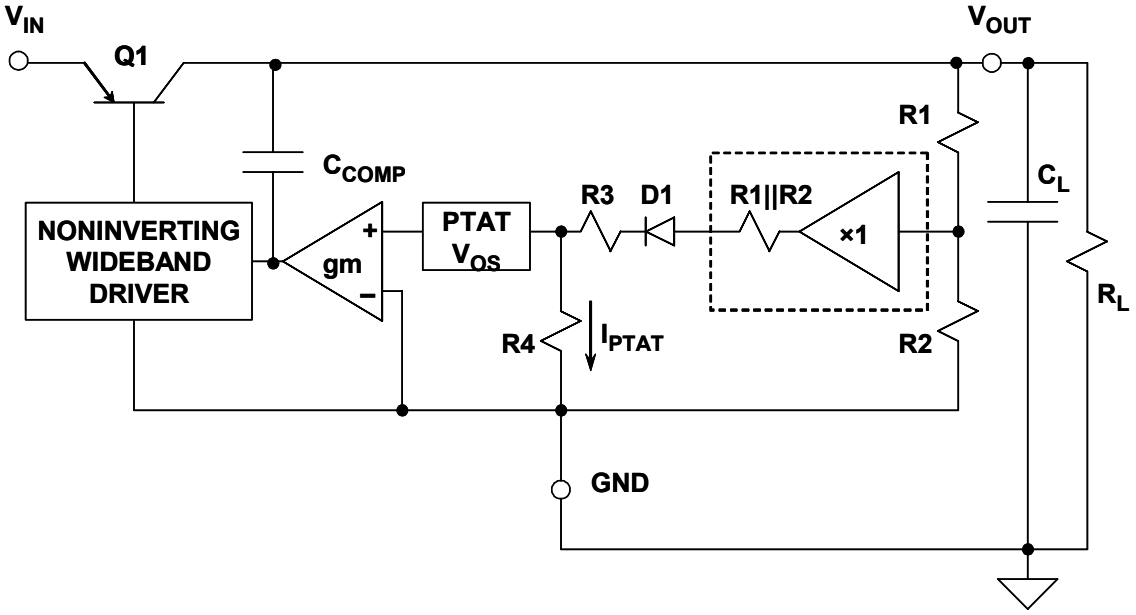

Figure 9.9: *ADP330X anyCAP Topology Features Improved DC and AC Performance over Traditional LDOs*

Design Features Related to DC Performance

One of the key differences in the ADP330X series is the use of a high gain vertical PNP pass device, with all of the advantages described above with Figs. 9.7 (Reference 6). This allows the typical dropout voltages for the series to be on the order of 1 mV/mA for currents of 200 mA or less.

It is important to note that the topology of this LDO is distinctly different from that of the generic form in Figure 9.7, as there is no obvious V_{REF} block. The reason for this is the fact that the ADP330X series uses what is termed a "merged" amplifier-reference design. The operation of the integral amplifier and reference scheme illustrated in Figure 9.9 can be described as follows.

BASIC LINEAR DESIGN

In this circuit, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1 and R2. In the figure, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1 and R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1 and R2, then actual components D1, R3, R4, etc.

The error amplifier, shown here as a gm stage, is actually a PNP input differential stage with the two transistors of the pair operated at different current densities, so as to produce a predictable PTAT offset voltage. Although shown here as a separate block V_{OS}, this offset voltage is inherent to a bipolar pair for such operating conditions. The PTAT V_{OS} causes a current I_{PTAT} to flow in R4, which is simply:

$$I_{PTAT} = \frac{V_{OS}}{R4}. \qquad \text{Eq. 9-4}$$

Note that this current also flows in series connected R4, R3, and the Thevenin resistance of the divider, R1||R2, so:

$$V_{PTAT} = I_{PTAT}\left(R3 + R4 + R1||R2\right). \qquad \text{Eq. 9-5}$$

The *total* voltage defined as V_{REF} is the sum of two component voltages:

$$V_{REF} = V_{PTAT} + V_{D1}, \qquad \text{Eq. 9-6}$$

where the I_{PTAT} scaled voltages across R3, R4, and R1||R2 produce a net PTAT voltage V_{PTAT}, and the diode voltage V_{D1} is a CTAT voltage. As in a standard band gap reference, the PTAT and CTAT components add up to a temperature stable reference voltage of 1.25 V. In this case however, the reference voltage is not directly accessible, but instead it exists in the virtual form described above. It acts as it would be seen at the output of a zero impedance divider of a numeric ratio of R1/R2, which is then fed into the R3-D1 series string through a Thevenin resistance of R1||R2 in series with D1.

With the closed loop regulator at equilibrium, the voltage at the virtual reference node will be:

$$V_{REF} = V_{OUT}\left(\frac{R2}{R1+R2}\right). \qquad \text{Eq. 9-7}$$

With minor re-arrangement, this can be put into the standard form to describe the regulator output voltage, as:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right). \qquad \text{Eq. 9-8}$$

In the various devices of the ADP330X series, the R1-R2 divider is adjusted to produce standard output voltages of 2.7 V, 3.0 V, 3.2 V, 3.3 V, and 5.0 V.

As can be noted from this discussion, unlike a conventional reference setup, there is no power wasting reference current such as used in a conventional regulator topology (I_{REF} of Figure 9.2). In fact, the Figure 9.9 regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

Design Features Related to AC Performance

While the above described dc performance enhancements of the ADP330X series are worthwhile, the most dramatic improvements come in areas of ac related performance. These improvements are in fact the genesis of the anyCAP series name.

Capacitive loading and the potential instability it brings is a major deterrent to easily applying LDOs. While low dropout goals prevent the use of emitter follower type outputs, and so preclude their desirable buffering effect against cap loading, there is an alternative technique of providing load immunity. One method of reducing susceptibility against variation in a particular amplifier response pole is called *pole splitting* (see Reference 8). It refers to an amplifier compensation method whereby two response poles are shifted in such a way so as to make one a dominant, lower frequency pole. In this manner the secondary pole (which in this case is the C_L related output pole) becomes much less of a major contributor to the net ac response. This has the desirable effect of greatly desensitizing the amplifier to variations in the output pole.

The anyCAP Pole-Splitting Topology

Returning to the anyCAP series topology, (Figure 9.9) it can be noted that in this case C_{COMP} is isolated from the pass device's base (and thus input ripple variations), by the wideband noninverting driver. But insofar as frequency compensation is concerned, because of this buffer's isolation, C_{COMP} still functions as a modified pole splitting capacitor (see Reference 9), and it does provide the benefits of a buffered, C_L independent single-pole response. The regulator's frequency response is dominated by the internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L. Thus the name anyCAP for the series is apt, as the design is tolerant of virtually any output capacitor type. C_L can be as low as 0.47 μF, and it can also be a multi-layer ceramic capacitor (MLCC) type. This allows a very small physical size for the entire regulation function, such as when a SOT-23 packaged anyCAP LDO is used, for example the ADP3300 device.

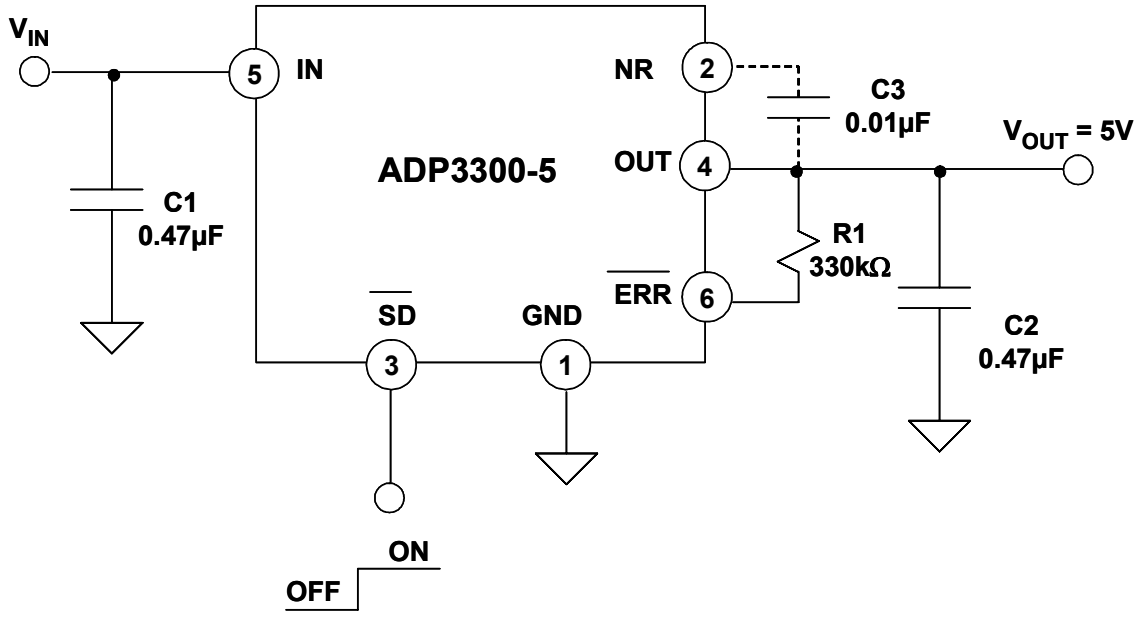

Figure 9.10: *A Basic ADP3000 50 mA LDO Regulator*

The ADP3300 and other anyCAP series devices maintain regulation over a wide range of load, input voltage, and temperature conditions. However, when the regulator is overloaded or entering the dropout region (for example, by a reduction in the input voltage) the open collector $\overline{\text{ERR}}$ pin becomes active, by going to a LOW or conducting state. Once set, the $\overline{\text{ERR}}$ pin's internal hysteresis keeps the output low, until some margin of operating range is restored. In the circuit of Figure 9.10, R1 is a pull-up resistor for the $\overline{\text{ERR}}$ output, E_{OUT}. This resistor can be eliminated if the load being driven provides a pull-up current.

The $\overline{\text{ERR}}$ function can also be activated by the regulator's over temperature protection circuit, which trips at 165°C. These internal current and thermal limits are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited by means of heat sinking, air flow, etc. so that junction temperatures will not exceed 125°C.

A capacitor, C3, connected between pins 2 and 4, can be used for an optional noise reduction (NR) feature. This is accomplished by ac-bypassing a portion of the regulator's internal scaling divider, which has the effect of reducing the output noise ~10 dB. When this option is exercised, only low leakage 10 nF - 100 nF capacitors should be used. Also, input and output capacitors should be changed to 1 µF and 4.7 µF values respectively, for lowest noise and the best overall performance. Note that the noise reduction pin is internally connected to a high impedance node, so connections to it should be carefully done to avoid noise. PC traces and pads connected to this pin should be as short and small as possible.

LDO Regulator Thermal Considerations

To determine a regulator's power dissipation, calculate it as follows:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(\text{Iground}), \qquad \text{Eq. 9-9}$$

where I_L and Iground are load and ground current, and V_{IN} and V_{OUT} are the input and output voltages respectively. Assuming I_L= 50 mA, Iground = 0.5 mA, V_{IN} = 8 V, and V_{OUT} = 5 V, the device power dissipation is:

$$P_D = (8 - 5)(0.05) + (8)(0.0005) = 0.150 + .004 = 0.154 \text{ W}. \qquad \text{Eq. 9-10}$$

To determine the regulator's temperature rise, ΔT, calculate it as follows:

$$\Delta T = T_J - T_A = P_D \times \theta_{JA} = 0.154 \text{ W} \times 165°\text{C/W} = 25.4°\text{C}. \qquad \text{Eq. 9-11}$$

With a maximum junction temperature of 125°C, this yields a calculated maximum safe ambient operating temperature of 125°C – 25.4°C, or just under 100°C. Since this temperature is in excess of the device's rated temperature range of 85°C, the device will then be operated conservatively at an 85°C (or less) maximum ambient temperature.

These general procedures can be used for other devices in the series, substituting the appropriate θ_{JA} for the applicable package, and applying the remaining operating conditions.

In addition, layout and PCB design can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads, to transfer heat away from the package. Appropriate PC layout techniques should then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance in SOT-23 and SO-8 packages:

1. *PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the uppermost side of the PCB.*

2. *Electrically connect dual V_{IN} and V_{OUT} pins in parallel, as well as to the corresponding V_{IN} and V_{OUT} large area PCB lands.*

3. *In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.*

4. *Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).*

5. *Do* not *use solder mask or silkscreen on the heat dissipating traces, as they increase the net thermal resistance of the mounted IC package.*

A real life example visually illustrates a number of the above points far better than words can. It is shown in Figure 9.11, a photo of the ADP3300 1.5" square evaluation PCB. The boxed area on the board represents the actual active circuit area.

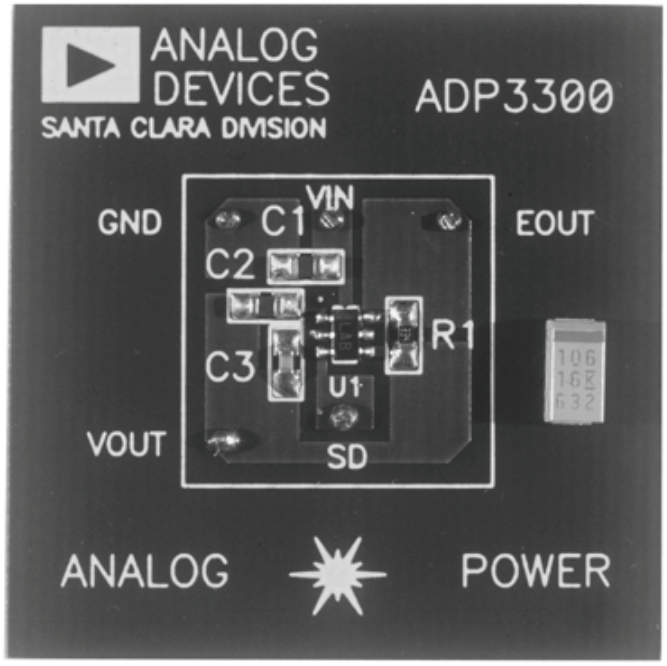

Figure 9.11: *Size Does Make a Difference*
ADP3300 Evaluation Board

Recent developments in packaging have led to much improved thermal performance for power management ICs. The anyCAP LDO regulator family capitalizes on this most effectively, using a thermally improved lead frame as the basis for all 8-pin devices. This package is called a "Thermal Coastline" design, and is shown in Figure. 2.39. The foundation of the improvement in heat transfer is related to two key parameters of the lead frame design, distance and width. The payoff comes in the reduced thermal resistance of the lead frame based on the Thermal Coastline, only 90°C/W versus 160°C/W for a standard SO-8 package. The increased dissipation of the Thermal Coastline allows the anyCAP series of SO-8 regulators to support more than one watt of dissipation at 25°C.

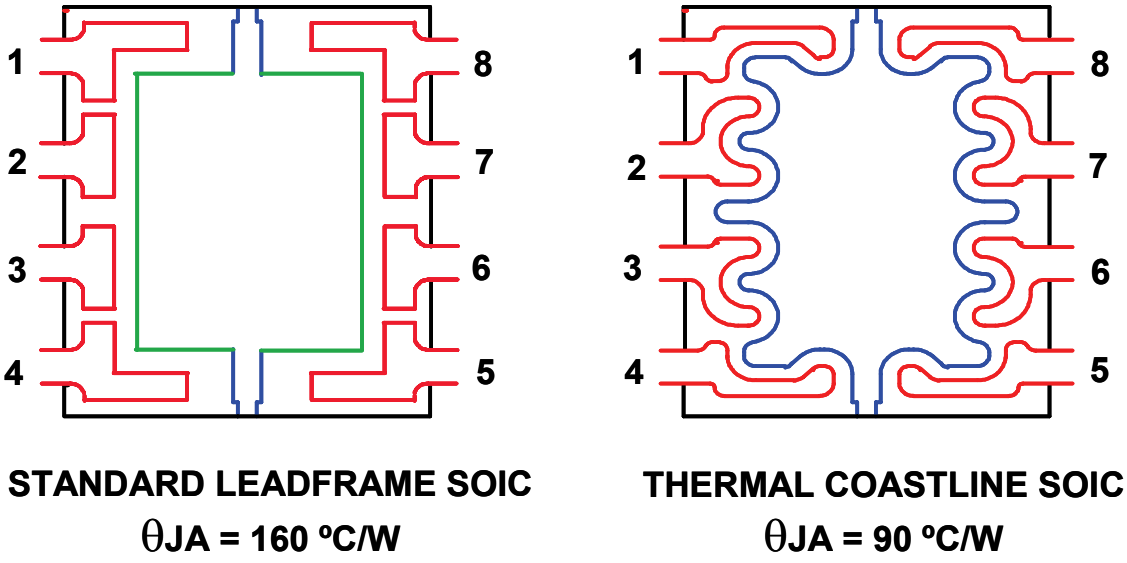

Figure 9.12: *anyCAP SERIES REGULATORS IN SO-8 USE THERMAL COASTLINE PACKAGES*

Additional insight into how the new lead frame increases heat transfer can be appreciated by Figure. 2.40. In this figure, it can be noted how the spacing of the Thermal Coastline paddle and leads shown on the right is reduced, while the width of the lead ends are increased, versus the standard lead frame, on the left.

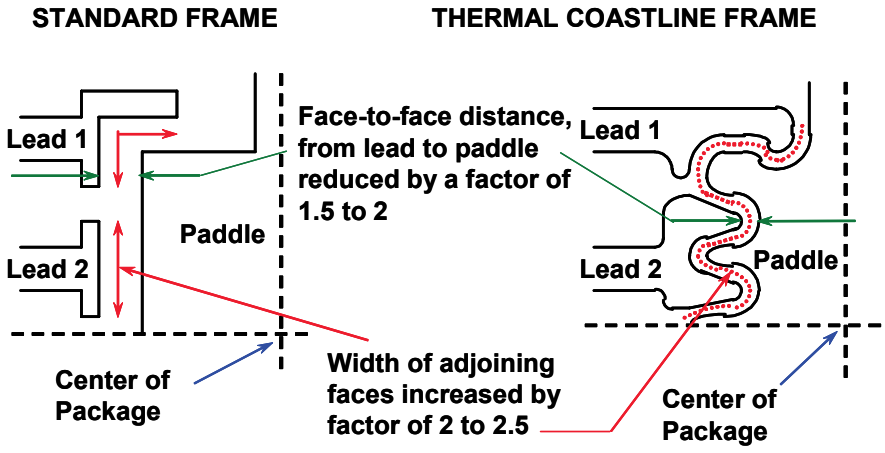

Figure 9.13: *Details of the Thermal Coastline Package*

Regulator Controller Differences

A basic difference between the regulator controller and a stand alone regulator is the removal of the pass device from the regulator chip. This design step has both advantages and disadvantages. A positive is that the external PMOS pass device can be chosen for the exact size, package, current rating, and power handling which is most useful to the application. This approach allows the same basic controller IC to be useful for currents of several hundred mA to more than 10 A, simply by choice of the FET. Also, since the regulator controller IC's Iground of 800 μA results in very little power dissipation, its thermal drift will be enhanced. On the downside, there are two packages now used to make up the regulator function. And, current limiting (which can be made completely integral to a standalone IC LDO regulator) is now a function which must be split between the regulator controller IC and an external sense resistor. This step also increases the dropout voltage of the LDO regulator controller somewhat, by about 50 mV.

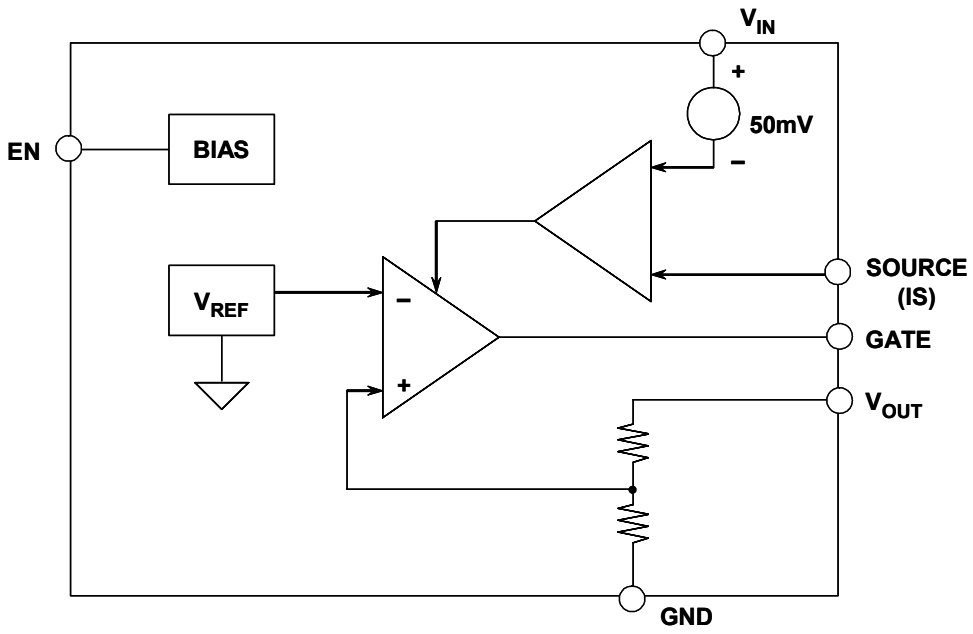

Figure 9.14: *Functional Block Diagram of anyCAP Series LDO Regulator Controller*

A functional diagram of the ADP3310 regulator controller is shown in Figure 9.14. The basic error amplifier, reference and scaling divider of this circuit are similar to the standalone anyCAP regulator, and will not be described in detail. The regulator controller version does share the same cap load immunity of the standalone versions, and also has a shutdown function, similarly controlled by the EN (enable) pin.

The main difference in the regulator controller IC architecture is the buffered output of the amplifier, which is brought out on the GATE pin, to drive the external PMOS FET. In addition, the current limit sense amplifier has a built in 50 mV threshold voltage, and is designed to compare the voltage between the V_{IN} and IS pins. When this voltage exceeds

50 mV, the current limit sense amplifier takes over control of the loop, by shutting down the error amplifier and limiting output current to the preset level.

A Basic 5 V/1 A LDO Regulator Controller

An LDO regulator controller is easy to use, since a PMOS FET, a resistor and two relatively small capacitors (one at the input, one at the output) is all that is needed to form an LDO regulator. The general configuration is shown by Figure 9.15 LDO suitable as a 5 V/1A regulator operating from a V_{IN} of 6 V, using the ADP3310-5 controller IC.

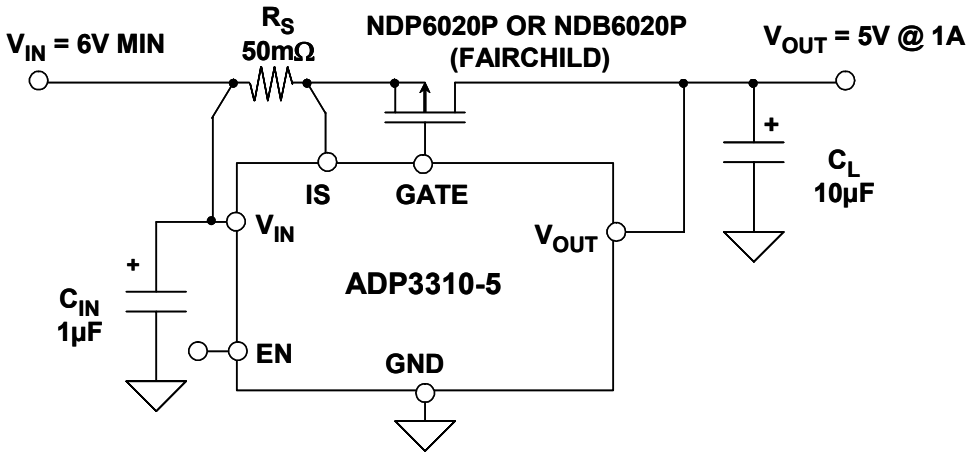

Figure 9.15: *A Basic ADP3310 PMOS FET 1 A LDO Regulator Controller*

This regulator is stable with virtually any good quality output capacitor used for C_L (as is true with the other anyCAP devices). The actual C_L value required and its associated ESR depends on the gm and capacitance of the external PMOS device. In general, a 10 µF capacitor at the output is sufficient to ensure stability for load currents up to 10 A. Larger capacitors can also be used, if high output surge currents are present. In such cases, low ESR capacitors such as OS-CON electrolytics are preferred, because they offer lowest ripple on the output. For less demanding requirements, a standard tantalum or aluminum electrolytic can be adequate. When an aluminum electrolytic is used, it should be qualified for adequate performance over temperature. The input capacitor, C_{IN}, is only necessary when the regulator is several inches or more distant from the raw dc filter capacitor. However, since it is small physically, it is usually prudent to use it in most instances. It should be located close to the V_{IN} pin of the regulator. Note also the current sensing resistor, R_S. This will be discussed in a following section.

Selecting the Pass Device

The type and size of the pass transistor are determined by a set of requirements for threshold voltage, input-output voltage differential, load current, power dissipation, and thermal resistance. An actual PMOS pass device selected must satisfy all of these electrical requirements, plus physical and thermal parameters. There are a number of manufacturers offering suitable devices in packages ranging from SO-8 up through TO-220 in size.

To ensure that the maximum available drive from the controller will adequately drive the FET under worst-case conditions of temperature range and manufacturing tolerances, the maximum drive from the controller ($V_{GS(DRIVE)}$) to the pass device must be determined. This voltage is calculated as follows:

$$V_{GS(DRIVE)} = V_{IN} - V_{BE} - \left(I_{L(MAX)}\right)\left(R_S\right), \qquad \text{Eq. 9-12}$$

where V_{IN} is the minimum input voltage, $I_{L(MAX)}$ is the maximum load current, R_S the sense resistor, and V_{BE} is a voltage internal to the ADP3310 (~ 0.5 @ high temp, 0.9 cold, and 0.7 V at room temp). Note that since $I_{L(MAX)} \times R_S$ will be no more than 75mV, and V_{BE} at cold temperature ≅0.9 V, this equation can be further simplified to:

$$V_{GS(DRIVE)} \cong V_{IN} - 1V. \qquad \text{Eq. 9-13}$$

In the Figure 2.43 example, V_{IN} = 6 V and V_{OUT} = 5 V, so $V_{GS(DRIVE)}$ is 6 – 1 = 5 V.

It should be noted that the above two equations apply to FET drive voltages which are *less* than the typical gate-to-source clamp voltage of 8 V (built into the ADP3310, for the purposes of FET protection).

An overall goal of the design is to then select an FET which will have an $R_{DS(ON)}$ sufficiently low so that the resulting dropout voltage will be less than $V_{IN} - V_{OUT}$, which in this case is 1 V. For the NDP6020P used in Figure 2.43 (see Reference 10), this device achieves an $R_{DS(ON)}$ of 70 milliohms (max) with a V_{GS} of 2.7 V, a voltage drive appreciably less than the ADP3310's $V_{GS(DRIVE)}$ of 5 V. The dropout voltage V_{MIN} of this regulator configuration is the sum of two series voltage drops, the FET's drop plus the drop across R_S, or:

$$V_{MIN} = I_{L(MAX)}\left(R_{DS(ON)} + R_S\right). \qquad \text{Eq. 9-14}$$

In the design here, the two resistances are roughly comparable to one another, so the net V_{MIN} will be 1 A × (50 milliohms + 70 milliohms) = 120 mV.

Thermal Design

The maximum allowable thermal resistance between the FET junction and the highest expected ambient temperature must be taken into account, to determine the type of FET package and heat sink used (if any).

Using 2 oz. copper PCB material and one square inch of copper PCB land area as a heatsink, it is possible to achieve a net thermal resistance, θ_{JA}, for mounted SO-8 devices on the order of 60°C/W or less. Such data is available for SO-8 power FETs (see Reference 11). There are also a variety of larger packages with lower thermal resistance than the SO-8, but still useful with surface mount techniques. Examples are the DPAK and D^2PAK, etc.

For higher power dissipation applications, corresponding to thermal resistance of 50°C/W or less, a bolt-on external heat sink is required to satisfy the θ_{JA} requirement. Compatible package examples would be the TO-220 family, which is used with the NDP6020P example of Figure 2.43.

Sensing Resistors for LDO Controllers

Current limiting in the ADP3310 controller is achieved by choosing an appropriate external current sense resistor, R_S, which is connected between the controller's V_{IN} and IS (source) pins. An internally derived 50 mV current limit threshold voltage appears between these pins, to establish a comparison threshold for current limiting. This 50 mV determines the threshold where current limiting begins. For a continuous current limiting, a foldback mode is established, with dissipation controlled by reducing the gate drive. The net effect is that the ultimate current limit level is a factor of 2/3 of maximum. The foldback limiting reduces the power dissipated in the pass transistor substantially.

To choose a sense resistor for a maximum output current I_L, R_S is calculated as follows:

$$R_S = \frac{0.05}{K_F \cdot I_L}. \qquad 9\text{-}15$$

In this expression, the nominal 50 mV current limit threshold voltage appears in the numerator. In the denominator appears a scaling factor K_F, which can be either 1.0 or 1.5, plus the maximum load current, I_L. For example, if a scaling factor of 1.0 is to be used for a 1 A I_L, the R_S calculation is straightforward, and 50 milliohms is the correct R_S value.

However, to account for uncertainties in the threshold voltage and to provide a more conservative output current margin, a scaling factor of $K_F = 1.5$ can alternately be used. When this approach is used, the same 1 A I_L load conditions will result in a 33 milliohm

R_S value. In essence, the use of the 1.5 scaling factor takes into account the foldback scheme's reduction in output current, allowing higher current in the limit mode.

The simplest and least expensive sense resistor for high current applications such as Figure 9.15 is a copper PCB trace controlled in both thickness and width. Both the temperature dependence of copper and the relative size of the trace must be taken into account in the resistor design. The temperature coefficient of resistivity for copper has a positive temperature coefficient of +0.39%/°C. This natural copper TC, in conjunction with the controller's PTAT based current limit threshold voltage, can provide for a current limit characteristic which is simple and effective over temperature.

The table of Figure 9.16 provides resistance data for designing PCB copper traces with various PCB copper thickness (or weight), in ounces of copper per square foot area. To use this information, note that the center column contains a resistance coefficient, which is the conductor resistance in milliohms/inch, divided by the trace width, W. For example, the first entry, for 1/2 ounce copper is 0.983 milliohms/inch/W. So, for a reference trace width of 0.1", the resistance would be 9.83 milliohms/inch. Since these are all linear relationships, everything scales for wider/skinnier traces, or for differing copper weights. As an example, to design a 50 milliohm R_S for the circuit of Figure 9.15 using 1/2 ounce copper, a 2.54" length of a 0.05" wide PCB trace could be used.

Copper Thickness	Resistance Coefficient, Milliohms / inch/ W (trace width W in inches)	Reference 0.1 Inch wide trace, Milliohms / inch
1/2 oz / ft^2	0.983 / W	9.83
1 oz / ft^2	0.491 / W	4.91
2 oz / ft^2	0.246 / W	2.46
3 oz / ft^2	0.163 / W	1.63

Figure 9.16: *Printed Circuit Copper Resistance*

To minimize current limit sense voltage errors, the two connections to R_S should be made four-terminal style, as is noted in Figure 9.15. It is not absolutely necessary to actually use four-terminal style resistors, except for the highest current levels. However, as a minimum, the heavy currents flowing in the source circuit of the pass device should not be allowed to flow in the ADP3310 sense pin traces. To minimize such errors, the V_{IN} connection trace to the ADP3310 should connect close to the body of R_S (or the resistor's input sense terminal), and the I_S connection trace should also connect close to the resistor body (or the resistor's output sense terminal). Four-terminal wiring is increasingly important for output currents of 1 A or more.

Alternately, an appropriate selected sense resistor such as surface mount sense devices available from resistor vendors can be used (see Reference 13). Sense resistor R_S may not be needed in all applications, if a current limiting function is provided by the circuit feeding the regulator. For circuits that don't require current limiting, the IS and V_{IN} pins of the ADP3310 must be tied together.

PCB Layout Issues

For best voltage regulation, place the load as close as possible to the controller device's V_{OUT} and GND pins. Where the best regulation is required, the V_{OUT} trace from the ADP3310 and the pass device's drain connection should connect to the positive load terminal via separate traces. This step (Kelvin sensing) will keep the heavy load currents in the pass device's drain out of the feedback sensing path, and thus maximize output accuracy. Similarly, the unregulated input common should connect to the common side of the load via a separate trace from the ADP3310 GND pin.

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SECTION 2: SWITCH MODE REGULATORS

Introduction

The trend toward lower power, lower weight, and portable equipment has driven the technology and the requirement for converting power efficiently. Switch mode power converters, often referred to simply as "switchers," offer a versatile way of achieving this goal. Modern IC switching regulators are small, flexible, and allow either step-up (boost) or step-down (buck) operation. Some topologies operate in both modes.

The most basic switcher topologies require only one transistor which is essentially used as a switch, one diode, one inductor, a capacitor across the output, and for practical but not fundamental reasons, another one across the input. A practical converter, however, requires a control section comprised of several additional elements, such as a voltage reference, error amplifier, comparator, oscillator, and switch driver, and may also include optional features like current limiting and shutdown capability.

Depending on the power level, modern IC switching regulators may integrate the entire converter except for the main magnetic element(s) (usually a single inductor) and the input/output capacitors. Often, a diode, the one which is an essential element of basic switcher topologies, cannot be integrated either. In any case, the complete power conversion for a switcher cannot be as integrated as a linear regulator. The requirement of a magnetic element means that system designers should not be inclined to think of switching regulators as simply “drop in” solutions. This presents a challenge to switching regulator manufacturers to provide careful design guidelines, commonly-used application circuits (using off the shelf components where possible), and plenty of design assistance. As the power levels increase, ICs tend to grow in complexity because it becomes more critical to optimize the control flexibility and precision. Also, since the switches begin to dominate the size of the die, it becomes more cost effective to remove them and integrate only the controller.

The primary limitations of switching regulators, as compared to linear regulators, are the generation of input and output voltage noise, EMI/RFI emissions, and the comparatively stringent requirements of the external support components. Although switching regulators do not necessarily require transformers, they do use inductors, and magnetic theory is not generally well understood by design engineers. However, manufacturers of switching regulators generally offer applications support in this area by offering design software and complete data sheets with recommended parts lists for the external inductor as well as capacitors and switching elements.

One unique advantage of switching regulators lies in their ability to convert a given supply voltage with a known voltage range to virtually any desired output voltage, with no “first order” limitations on efficiency. This is true regardless of whether the output voltage is higher or lower than the input voltage—the same or the opposite polarity. Consider the basic components of a switcher, as stated above. The inductor and capacitor are, ideally, reactive elements which dissipate no power. The transistor is effectively,

ideally, a switch in that it is either "on," thus having no voltage dropped across it while current flows through it, or "off," thus having no current flowing through it while there is voltage across it. Since either voltage or current are always zero, the power dissipation is zero, thus, ideally, the switch dissipates no power. Finally, there is the diode, which has a finite voltage drop while current flows through it, and thus dissipates *some* power. But even that can be substituted for by a synchronized switch, called a "synchronous rectifier," so that it ideally dissipates no power. Practical efficiencies can exceed 90%.

Switchers also offer the advantage that, since they inherently require a magnetic element, it is often a simple matter to "tap" an extra winding onto that element and, often with just a diode and capacitor, generate a reasonably well regulated additional output. If more outputs are needed, more such taps can be used. Since the tap winding requires no electrical connection, it can be isolated from other circuitry, or made to "float" atop other voltages. Note that only one of the outputs would be "regulated." The others track according to the ratio of the taps.

Of course, real components create inefficiencies. Inductors have resistance, and their magnetic cores are not ideal either, so they dissipate power. Capacitors have resistance, and as current flows in and out of them, they dissipate power, as well. Transistors, bipolar or field-effect, are not ideal switches, and have a voltage drop when they are turned on, plus they cannot be switched instantly, and thus dissipate power while they are turning on or off.

As we shall soon see, switchers create ripple currents in their input and output capacitors. Those ripple currents create voltage ripple and noise on the converter's input and output due to the resistance, inductance, and finite capacitance of the capacitors used. That is the *conducted* part of the noise. Then there are often ringing voltages in the converter, parasitic inductances in components and PCB traces, and an inductor which creates a magnetic field which it cannot perfectly contain within its core—all contributors to *radiated* noise. Noise is an inherent by-product of a switcher and must be controlled by proper component selection, PCB layout, and, if that is not sufficient, additional input or output filtering or shielding.

Inductor and Capacitor Fundamentals

In order to understand switching regulators, the fundamental energy storage capabilities of inductors and capacitors must be fully understood. When a voltage is applied to an ideal inductor (see Figure 9.17), the current builds up linearly over time at a rate equal to V/L, where V is the applied voltage, and L is the value of the inductance. This energy is stored in the inductor's magnetic field, and if the switch is opened quickly, the magnetic field collapses, and the inductor voltage goes to a large instantaneous value until the field has fully collapsed.

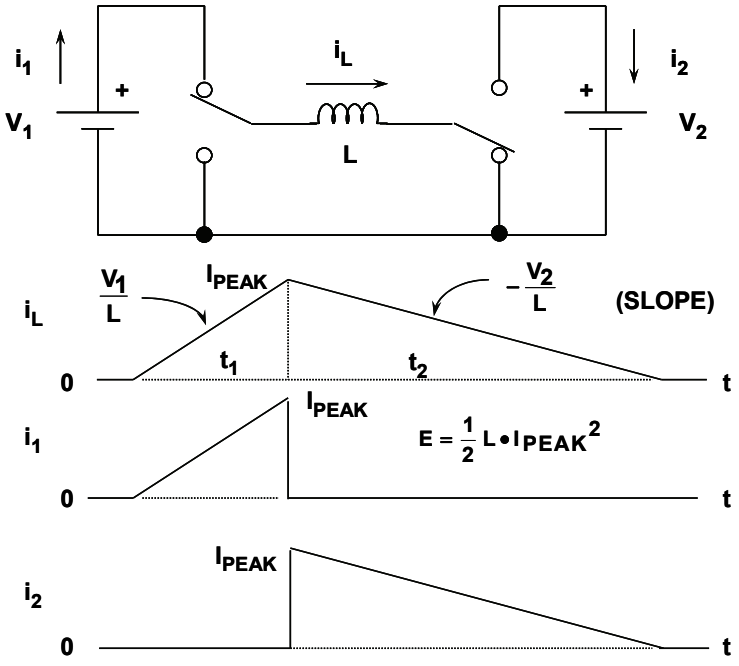


Figure 9.17: *Inductor and Capacitor Fundamentals*

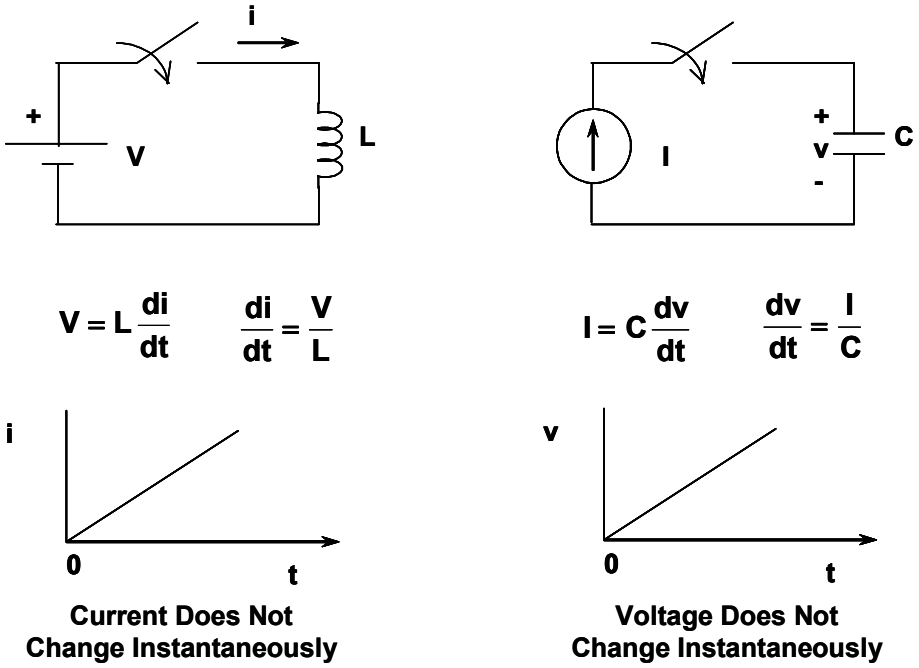


Figure 9.18: *Energy Transfer Using an Inductor*

When a current is applied to an ideal capacitor, the capacitor is gradually charged, and the voltage builds up linearly over time at a rate equal to I/C, where I is the applied current, and C is the value of the capacitance. Note that the voltage across an ideal capacitor cannot change instantaneously.

Of course, there is no such thing as an ideal inductor or capacitor. Real inductors have stray winding capacitance, series resistance, and can saturate for large currents. Real capacitors have series resistance and inductance and may break down under large voltages. Nevertheless, the fundamentals of the ideal inductor and capacitor are fundamental in understanding the operation of switching regulators.

An inductor can be used to transfer energy between two voltage sources as shown in Figure 9.18. While energy transfer could occur between two voltage sources with a resistor connected between them, the energy transfer would be inefficient due to the power loss in the resistor, and the energy could only be transferred from the higher to the lower value source. In contrast, an inductor ideally returns all the energy that is stored in it, and with the use of properly configured switches the energy can flow from any one source to another, regardless of their respective values and polarities.

When the switches are initially placed in the position shown, the voltage V_1 is applied to the inductor, and the inductor current builds up at a rate equal to V_1/L. The peak value of the inductor current at the end of the interval t_1 is:

$$I_{PEAK} = \frac{V_1}{L} \bullet t_1 . \qquad \text{Eq. 9-16}$$

The average power transferred to the inductor during the interval t_1 is

$$P_{AVG} = \frac{1}{2} I_{PEAK} \bullet V_1 . \qquad \text{Eq. 9-17}$$

The energy transferred during the interval t_1 is:

$$E = P_{AVG} \bullet t_1 = \frac{1}{2} I_{PEAK} \bullet V_1 \bullet t_1 . \qquad \text{Eq. 9-18}$$

Solving the first equation for t_1 and substituting into the last equation yields:

$$E = \frac{1}{2} L \bullet I_{PEAK}^{\,2} . \qquad \text{Eq. 9-19}$$

When the switch positions are reversed, the inductor current continues to flow into the load voltage V_2, and the inductor current decreases at a rate $-V_{OUT} + V_F/L$. At the end of the interval t_2, defined by when the inductor current has decreased to zero, and all of the energy previously stored in the inductor has been transferred into the load. The figure shows the current waveforms for the inductor, the input current i_1, and the output current i_2. The ideal inductor dissipates no power, so there is no power loss in this transfer, assuming ideal circuit elements. This fundamental method of energy transfer forms the basis for all switching regulators.

Ideal Step-Down (Buck) Converter

The basic topology of an ideal step-down (buck) converter is shown in Figure 9-19. The actual integrated circuit switching regulator contains the switch control circuit and may or may not include the switch (depending upon the output current requirement). The inductor, diode, and load bypass capacitor are external.

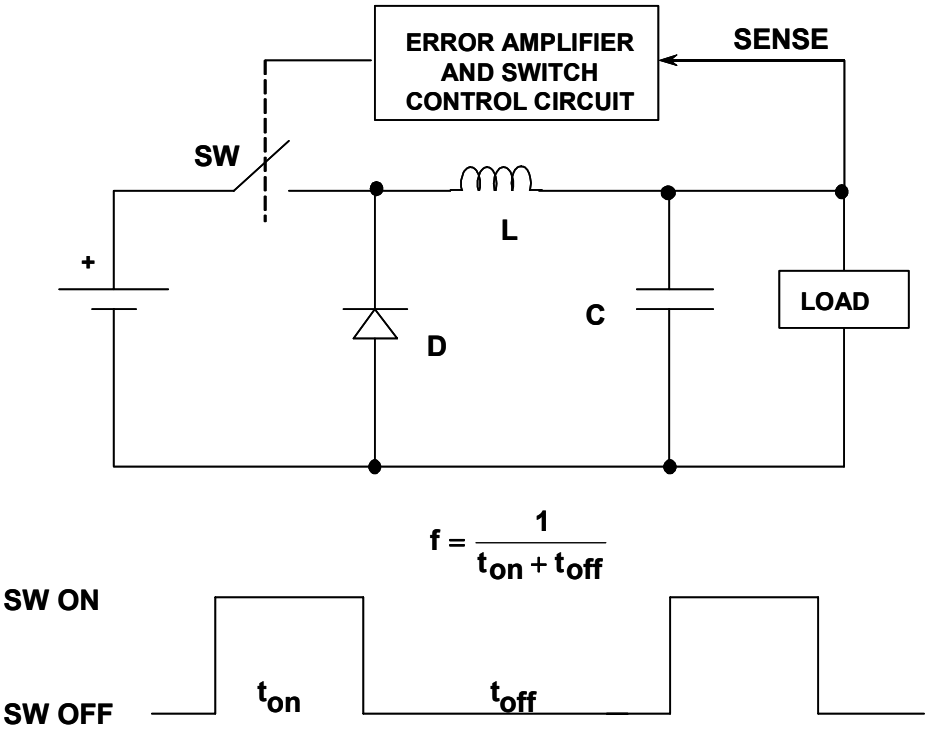


Figure 9.19: *Basic Step-down (Buck) Converter*

The output voltage is sensed and then regulated by the switch control circuit. There are several methods for controlling the switch, but for now assume that the switch is controlled by a pulse width modulator (PWM) operating at a fixed frequency, f.

The actual waveforms associated with the buck converter are shown in Figure 9.20. When the switch is on, the voltage $V_{IN}-V_{OUT}$ appears across the inductor (neglecting the voltage drop across the inductor), and the inductor current increases with a slope of $(V_{IN}-V_{OUT})/L$ (see Figure 9-20B). When the switch turns off, current continues to flow through the inductor in the same direction and into the load (remember that the current cannot change instantaneously in an inductor). The diode providing the return current path, called a "freewheeling" diode in this application, completes the current path broken by opening the switch. It also clamps the V_D as the inductor tries to pull current out of the node. The voltage across the inductor is now $V_{OUT} + V_F$, but the polarity has reversed. Therefore, the inductor current decreases with a slope equal to $- V_{OUT}/L$. Note that the inductor current is equal to the output current in a buck converter.

The diode and switch currents are shown in Figure 9-20C and 9.20D, respectively, and the inductor current is the sum of these waveforms. Also note by inspection that the instantaneous input current equals the switch current. Note, however, that the average input current is less than the average output current. In a practical regulator, both the switch and the diode have voltage drops across them during their conduction which creates internal power dissipation and a loss of efficiency, but these voltages will be neglected for now. It is also assumed that the output capacitor, C, is large enough so that the output voltage does not change significantly during the switch on or off times.

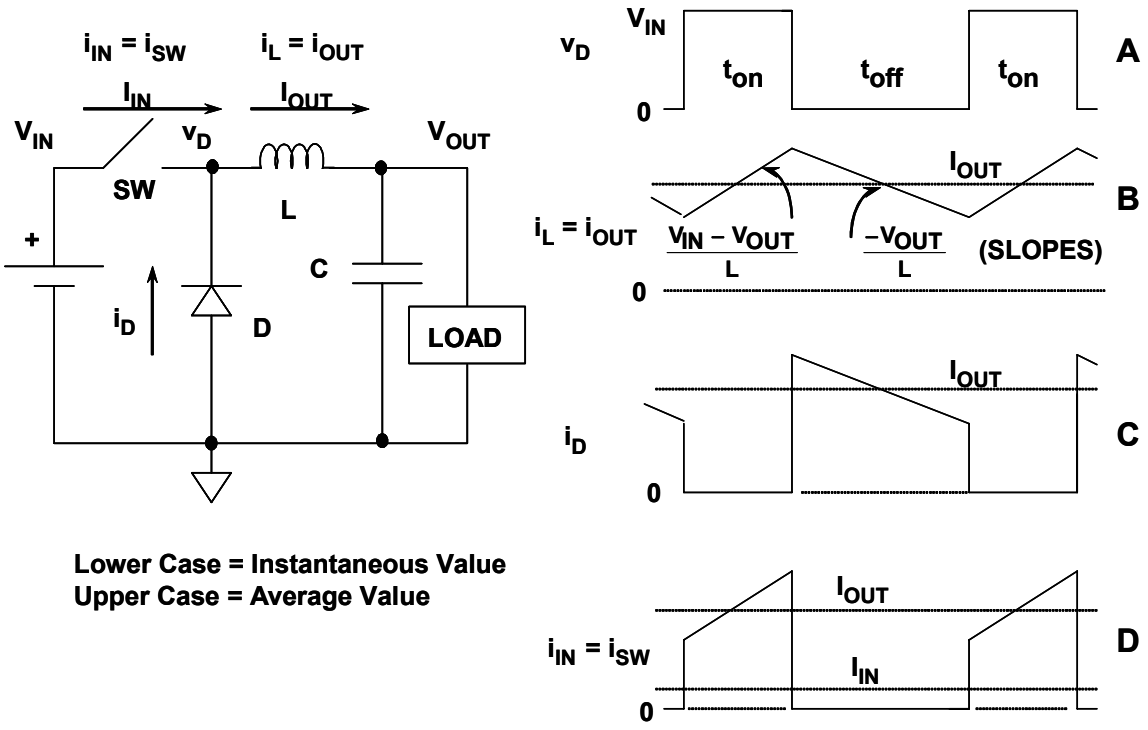


Figure 9.20: *Basic Step-Down (Buck) Converter Waveforms*

There are several important things to note about these waveforms. First is that ideal components have been assumed, i.e., the input voltage source has zero impedance, the switch has zero on-resistance and zero turn-on and turn-off times. It is also assumed that the inductor does not saturate and that the diode is ideal with no forward drop.

Also note that the output current is continuous, while the input current is pulsating. Obviously, this has implications regarding input and output filtering. If one is concerned about the voltage ripple created on the power source which supplies a buck converter, the input filter capacitor (not shown) is generally more critical that the output capacitor with respect to ESR/ESL.

If a steady-state condition exists (see Figure 9-21), the basic relationship between the input and output voltage may be derived by inspecting the inductor current waveform and writing:

$$\frac{V_{IN} - V_{OUT}}{L} \bullet t_{on} = \frac{V_{OUT}}{L} \bullet t_{off}. \qquad \text{Eq. 9-20}$$

Solving for V_{OUT}:

$$V_{OUT} = V_{IN} \bullet \frac{t_{on}}{t_{on} + t_{off}} = V_{IN} \bullet D, \qquad \text{Eq. 9-21}$$

where D is the switch *duty ratio* (more commonly called *duty cycle*), defined as the ratio of the switch on-time (t_{on}) to the total switch cycle time ($t_{on} + t_{off}$).

This is the classic equation relating input and output voltage in a buck converter which is operating with *continuous* inductor current, defined by the fact that the inductor current never goes to zero.

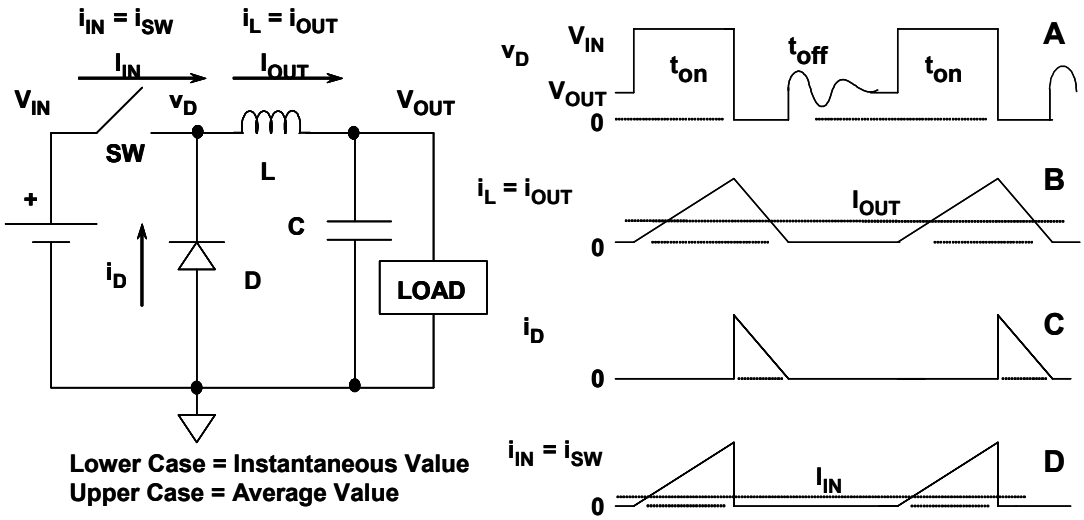


Figure 9.21: *Input/Output Relationships for a Buck Converter*

Notice that this relationship is independent of the inductor value L as well as the switching frequency $1/(t_{on} + t_{off})$ and the load current. Decreasing the inductor value, however, will result in a larger peak-to-peak output ripple current, while increasing the value results in smaller ripple. There are many other trade-offs involved in selecting the inductor, and these will be discussed in a later section.

In this simple model, line and load regulation (of the output voltage) is achieved by varying the duty cycle using a pulse width modulator (PWM) operating at a fixed frequency, f. The PWM is in turn controlled by an error amplifier—an amplifier which

amplifies the "error" between the measured output voltage and a reference voltage. As the input voltage increases, the duty cycle decreases; and as the input voltage decreases, the duty cycle increases. Note that while the average inductor current changes proportionally to the output current, the duty cycle does not change. Only dynamic changes in the duty cycle are required to modulate the inductor current to the desired level; then the duty cycle returns to its steady state value. In a practical converter, the duty cycle might increase slightly with load current to counter the increase in voltage drops in the circuit, but would otherwise follow the ideal model.

This discussion so far has assumed the regulator is in the *continuous-mode* of operation, defined by the fact that the inductor current never goes to zero. If, however, the output load current is decreased, there comes a point where the inductor current will go to zero between cycles, and the inductor current is said to be *discontinuous*. It is necessary to understand the implications of this operating mode as well, since many switchers must supply a wide dynamic range of output current, where this phenomenon is unavoidable. Waveforms for discontinuous operation are shown in Figure 9-22.

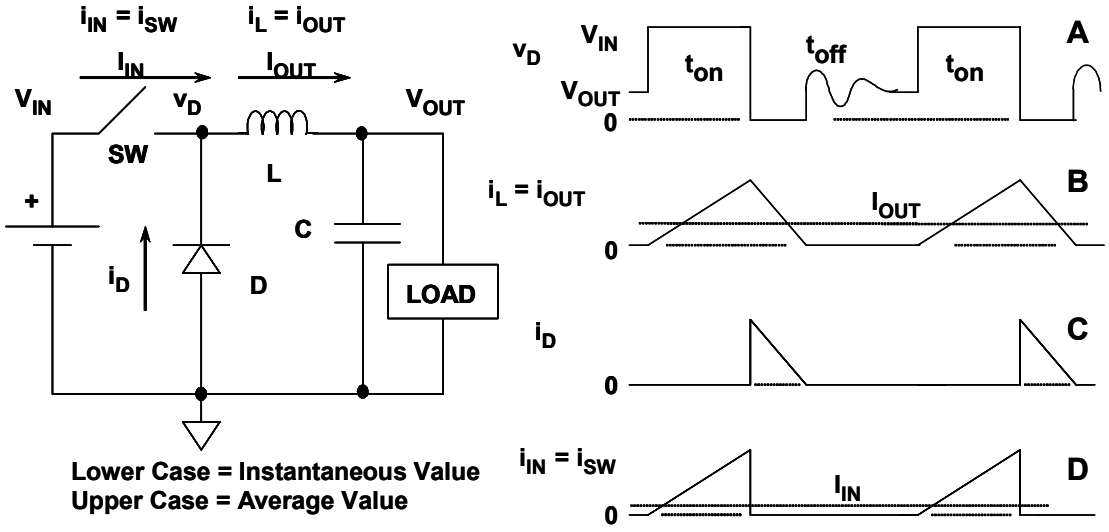


Figure 9.22: *Buck Converter Waveforms— Discontinuous Mode*

Behavior during the switch on-time is identical to that of the continuous mode of operation. However, during the switch off-time, there are two regions of unique behavior. First, the inductor current ramps down at the same rate as it does during continuous mode, but then the inductor current goes to zero. When it reaches zero, the current tries to reverse but cannot find a path through the diode any longer. So the voltage on the input side of the inductor (same as the diode and switch junction) jumps up to V_{OUT} such that the inductor has no voltage across it, and the current can remain at zero.

Because the impedance at diode node (v_D) is high, ringing occurs due to the inductor, L, resonating with the stray capacitance which is the sum of the diode capacitance, C_D, and

the switch capacitance, C_{SW}. The oscillation is damped by stray resistances in the circuit, and occurs at a frequency given by:

$$f_o = \frac{1}{2\pi\sqrt{L(C_D + C_{SW})}}. \qquad \text{Eq. 9.22}$$

A circuit devoted simply to dampening resonances via power dissipation is called a *snubber*. If the ringing generates EMI/RFI problems, it may be damped with a suitable RC snubber. However, this will cause additional power dissipation and reduced efficiency.

If the load current of a standard buck converter is low enough, the inductor current becomes discontinuous. The current at which this occurs can be calculated by inspection of the waveform shown in Figure 9.23. This waveform is drawn showing the inductor current going to exactly zero at the end of the switch off-time. Under these conditions, the average output current is:

$$I_{OUT} = I_{PEAK}/2. \qquad \text{Eq. 9-23}$$

We have already shown that the peak inductor current is:

$$I_{PEAK} = \frac{V_{IN} - V_{OUT}}{L} \bullet t_{on}. \qquad \text{Eq. 9-24}$$

Thus, discontinuous operation will occur if:

$$I_{OUT} < \frac{V_{IN} - V_{OUT}}{2L} \bullet t_{on}. \qquad \text{Eq. 9-25}$$

However, V_{OUT} and V_{IN} are related by:

$$V_{OUT} = V_{IN} \bullet D = V_{IN} \bullet \frac{t_{on}}{t_{on} + t_{off}}. \qquad \text{Eq. 9-26}$$

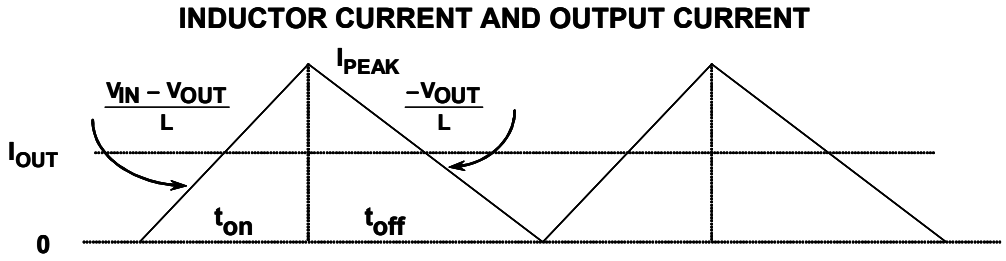
Solving for t_{on}:

$$t_{on} = \frac{V_{OUT}}{V_{IN}} \bullet (t_{on} + t_{off}) = \frac{V_{OUT}}{V_{IN}} \bullet \frac{1}{f}. \qquad \text{Eq. 9.27}$$

Substituting this value for t_{on} into the previous equation for I_{OUT}:

$$I_{OUT} < \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2Lf} \quad \text{Eq. 9-28}$$

(Criteria for discontinuous operation—buck converter)



DISCONTINUOUS MODE IF:

$$I_{OUT} < \frac{1}{2} I_{PEAK} = \frac{V_{IN} - V_{OUT}}{2L} \bullet t_{on}$$

$$I_{OUT} < \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2Lf}, \quad f = \frac{1}{t_{on} + t_{off}}$$

Figure 9.23: *Buck Converter Point of Discontinuous Operation*

Ideal Step-Up (Boost) Converter

The basic step-up (boost) converter circuit is shown in Figure 9.24. During the switch on-time, the current builds up in the inductor. When the switch is opened, the energy stored in the inductor is transferred to the load through the diode.

The actual waveforms associated with the boost converter are shown in Figure 9.25. When the switch is on, the voltage V_{IN} appears across the inductor, and the inductor current increases at a rate equal to V_{IN}/L. When the switch is opened, a voltage equal to $V_{OUT} - V_{IN}$ appears across the inductor, current is supplied to the load, and the current decays at a rate equal to $(V_{OUT} - V_{IN})/L$. The inductor current waveform is shown in Figure 9.25B.

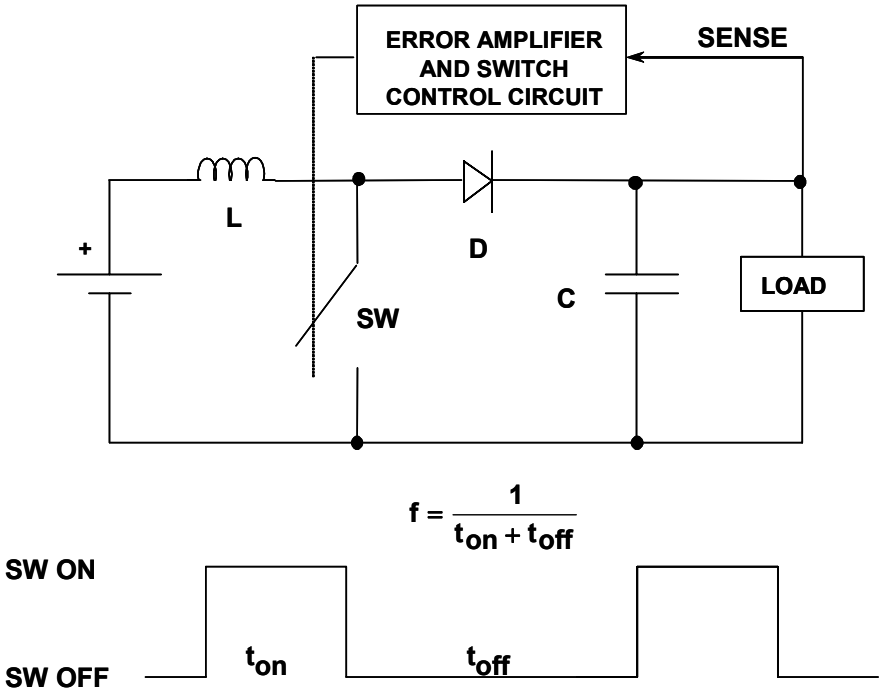


Figure 9.24: *Basic Step-Up (Boost) Converter*

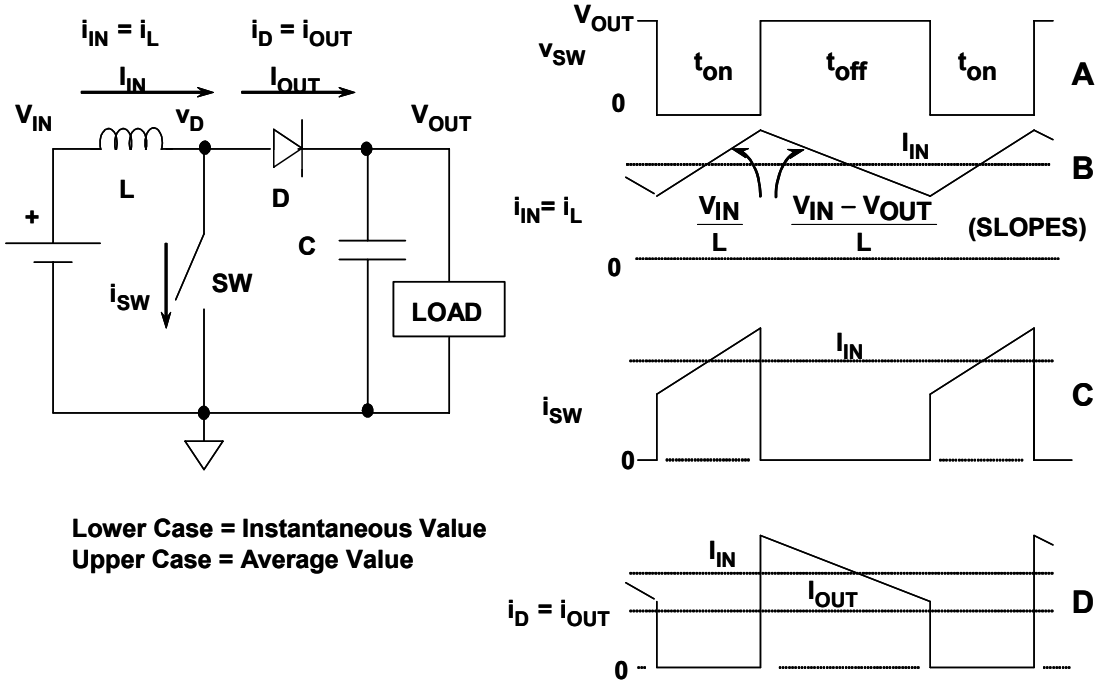


Figure 9.25: *Basic Step-Up Converter Waveforms*

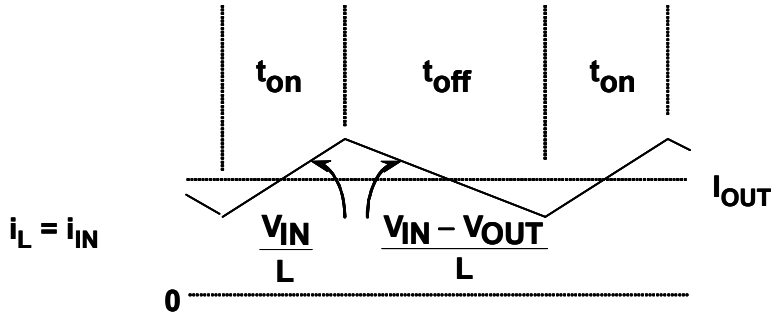
Note that in the boost converter, the input current is continuous, while the output current (Figure 9.15D) is pulsating. This implies that filtering the output of a boost converter is more difficult than that of a buck converter. (Refer back to the previous discussion of buck converters). Also note that the input current is the sum of the switch and diode current.

If a steady-state condition exists (see Figure 9.26), the basic relationship between the input and output voltage may be derived by inspecting the inductor current waveform and writing:

$$\frac{V_{IN}}{L} \bullet t_{on} = \frac{V_{OUT} - V_{IN}}{L} \bullet t_{off}. \qquad \text{Eq. 9-29}$$

Solving for V_{OUT}:

$$V_{OUT} = V_{IN} \bullet \frac{t_{on} + t_{off}}{t_{off}} = V_{IN} \bullet \frac{1}{1 - D}. \qquad \text{Eq. 9-30}$$



$$\frac{V_{IN}}{L} \bullet t_{on} = \frac{V_{OUT} - V_{IN}}{L} \bullet t_{off}$$

$$V_{OUT} = V_{IN} \bullet \frac{t_{on} + t_{off}}{t_{off}} = V_{IN} \bullet \frac{1}{1 - D}$$

Figure 9.26: *Input/Output Relationship for a Boost Converter*

This discussion so far has assumed the boost converter is in the *continuous-mode* of operation, defined by the condition that the inductor current never goes to zero. If, however, the output load current is decreased, there comes a point where the inductor current will go to zero between cycles, and the inductor current is said to be

discontinuous. It is necessary to understand this operating mode as well, since many switchers must supply a wide dynamic range of output current, where this phenomenon is unavoidable.

Discontinuous operation for the boost converter is similar to that of the buck converter. Figure 9.27 shows the waveforms. Note that when the inductor current goes to zero, ringing occurs at the switch node at a frequency f_o given by:

$$f_o = \frac{1}{2\pi\sqrt{L(C_D + C_{SW})}}. \qquad \text{Eq. 9-31}$$

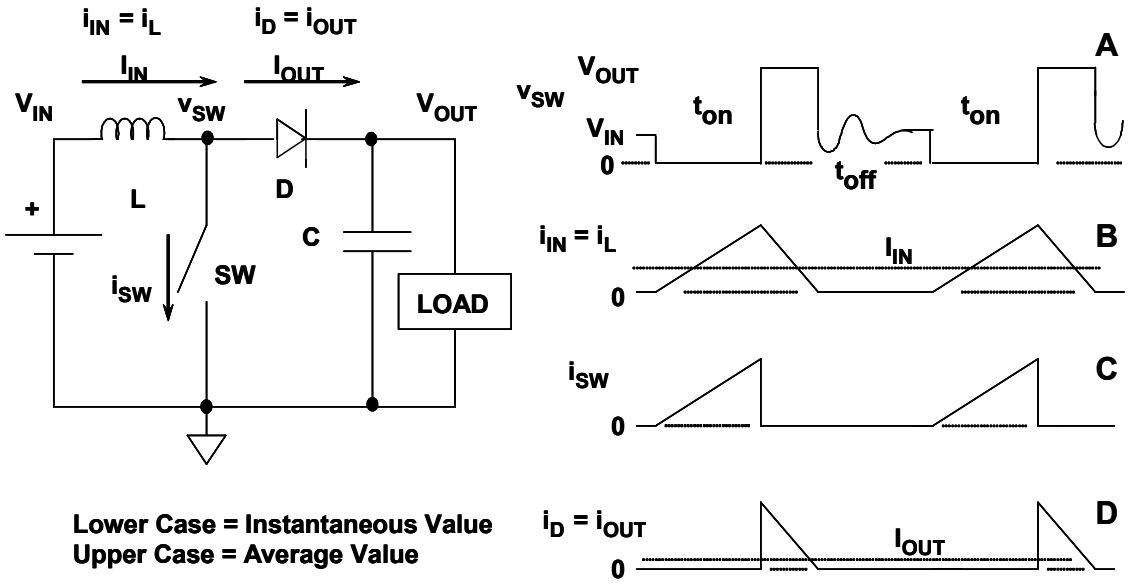


Figure 9.27: *Boost Converter Waveform—Discontinuous Mode*

The inductor, L, resonates with the stray switch capacitance and diode capacitance, $C_{SW} + C_D$ as in the case of the buck converter. The ringing is dampened by circuit resistances, and, if needed, a snubber.

The current at which a boost converter becomes discontinuous can be derived by inspecting the inductor current (same as input current) waveform of Figure 9.28.

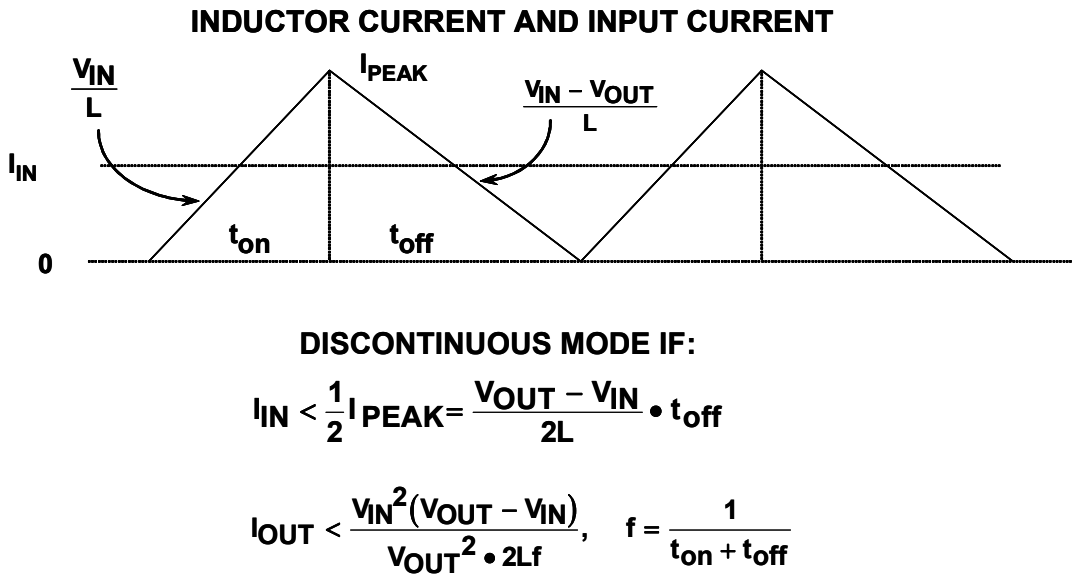


Figure 9.28: *Boost Converter Point of Discontinuous Operation*

The average input current at the point of discontinuous operation is:

$$I_{IN} = I_{PEAK}/2. \qquad \text{Eq. 9-32}$$

Discontinuous operation will occur if:

$$I_{IN} < I_{PEAK}/2. \qquad \text{Eq. 9-33}$$

However,

$$I_{IN} = \frac{I_{PEAK}}{2} = \frac{V_{OUT} - V_{IN}}{2L} \bullet t_{off}. \qquad \text{Eq. 9-34}$$

Also,

$$V_{IN} \bullet I_{IN} = V_{OUT} \bullet I_{OUT}, \qquad \text{Eq. 9-35}$$

and therefore:

$$I_{OUT} = \frac{V_{IN}}{V_{OUT}} \bullet I_{IN} = \frac{V_{IN}}{V_{OUT}} \bullet \frac{(V_{OUT} - V_{IN})}{2L} \bullet t_{off}. \qquad \text{Eq. 9-36}$$

However,

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} = \frac{1}{1-\dfrac{t_{on}}{t_{on}+t_{off}}} = \frac{t_{on}+t_{off}}{t_{off}}. \qquad \text{Eq, 9-37}$$

Solving for t_{off}:

$$t_{off} = \frac{V_{IN}}{V_{OUT}}\left(t_{on}+t_{off}\right) = \frac{V_{IN}}{f \bullet V_{OUT}}. \qquad \text{Eq. 9-38}$$

Substituting this value for t_{off} into the previous expression for I_{OUT}, the criteria for discontinuous operation of a boost converter is established:

$$I_{OUT} < \frac{V_{IN}{}^2(V_{OUT}-V_{IN})}{V_{OUT}{}^2 \bullet 2Lf}. \qquad \text{Eq. 9-39}$$

(Criteria for discontinuous operation—boost converter).

The basic buck and boost converter circuits can work equally well for negative inputs and outputs as shown in Figure 9.29. Note that the only difference is that the polarities of the input voltage and the diode have been reversed. In practice, however, not many IC buck and boost regulators or controllers will work with negative inputs. In some cases, external circuitry can be added in order to handle negative inputs and outputs. Rarely are regulators or controllers designed specifically for negative inputs or outputs. In any case, data sheets for the specific ICs will indicate the degree of flexibility allowed.

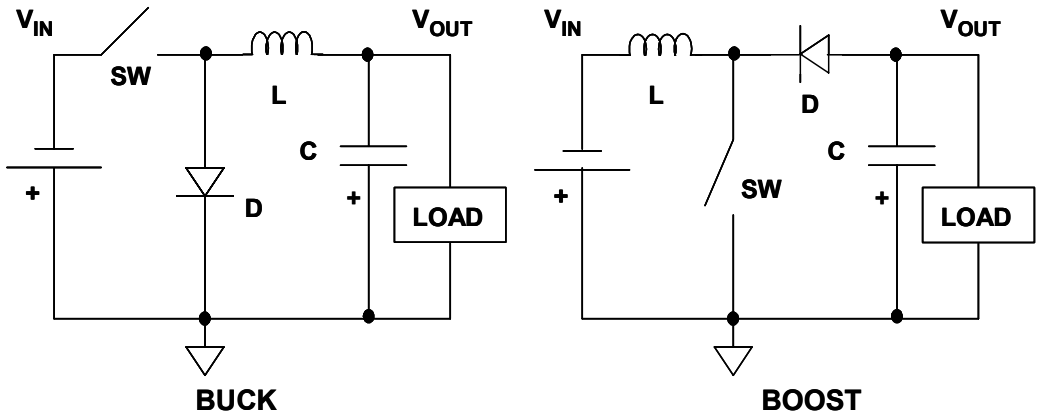
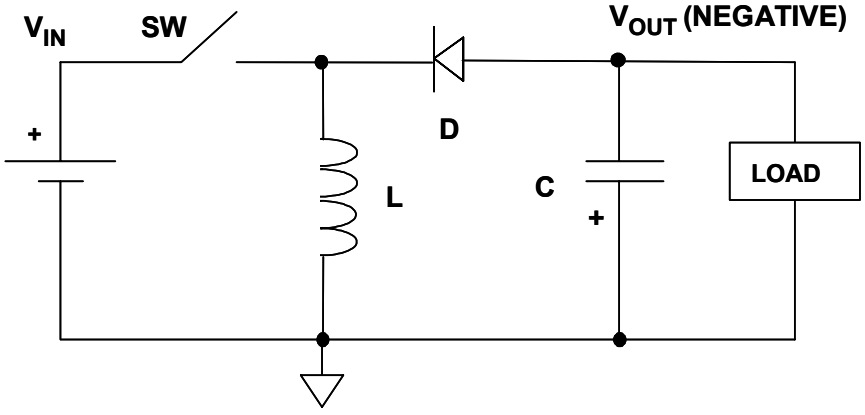


Figure 9.29: *Negative In, Negative Out Buck and Boost Converter*

Buck-Boost Topologies

The simple buck converter can only produce an output voltage which is less than the input voltage, while the simple boost converter can only produce an output voltage greater than the input voltage. There are many applications where more flexibility is required. This is especially true in battery powered applications, where the fully charged battery voltage starts out greater than the desired output (the converter must operate in the buck mode), but as the battery discharges, its voltage becomes less than the desired output (the converter must then operate in the boost mode).

A *buck-boost* converter is capable of producing an output voltage which is either greater than or less than the absolute value of the input voltage. A simple buck-boost converter topology is shown in Figure 9.30. The input voltage is positive, and the output voltage is negative. When the switch is on, the inductor current builds up. When the switch is opened, the inductor supplies current to the load through the diode. Obviously, this circuit can be modified for a negative input and a positive output by reversing the polarity of the diode.



The Absolute Value of the Output Can Be Less Than Or Greater Than the Absolute Value of the Input

Figure 9.30: *Buck-Boost Converter #1 $+V_{IN}$, $-V_{OUT}$*

A second buck-boost converter topology is shown in Figure 9.31. This circuit allows both the input and output voltage to be positive. When the switches are closed, the inductor current builds up. When the switches open, the inductor current is supplied to the load through the current path provided by D1 and D2. A fundamental disadvantage to this circuit is that it requires two switches and two diodes. As in the previous circuits, the polarities of the diodes may be reversed to handle negative input and output voltages.

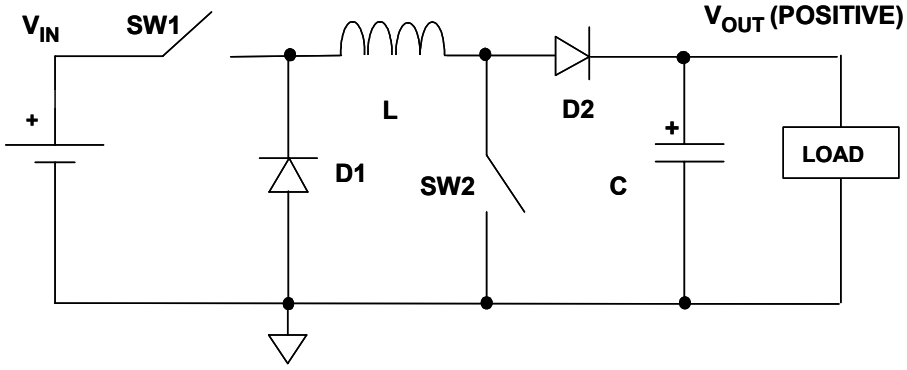


Figure 9.31: *Buck-Boost Converter #2*
$+V_{IN}$, $-V_{OUT}$

Another way to accomplish the buck-boost function is to cascade two switching regulators; a boost regulator followed by a buck regulator as shown in Figure 9.32. The example shows some practical voltages in a battery-operated system. The input from the four AA cells can range from 6 V (charged) to about 3.5 V (discharged). The intermediate voltage output of the boost converter is 8 V, which is always greater than the input voltage. The buck regulator generates the desired 5 V from the 8 V intermediate voltage. The total efficiency of the combination is the product of the individual efficiencies of each regulator, and can be greater than 85% with careful design.

An alternate topology is use a buck regulator followed by a boost regulator. This approach, however, has the disadvantage of pulsating currents on both the input and output and a higher current at the intermediate voltage output.

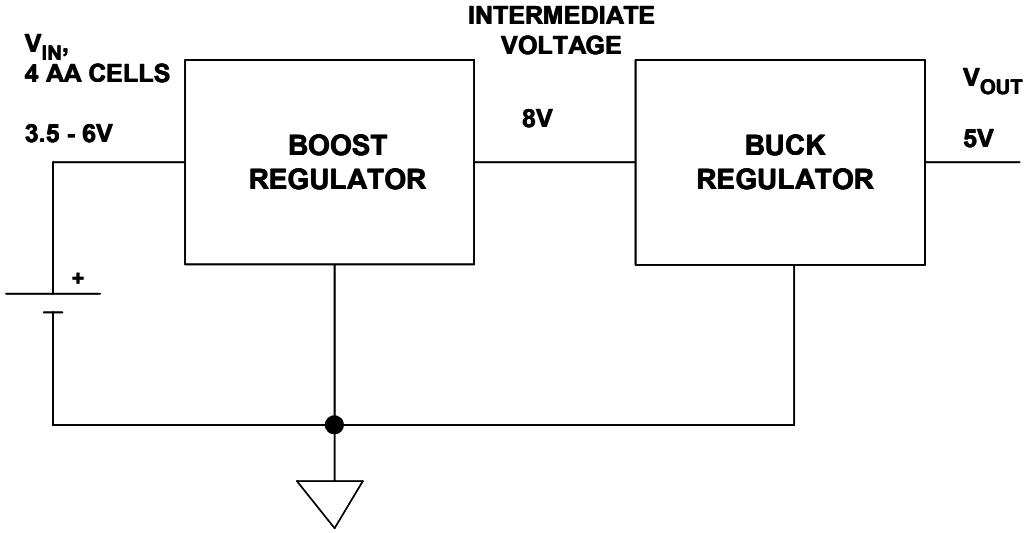


Figure 9.32: *Cascaded Buck Boost Regulators*
(Example Voltages)

Other Nonisolated Switcher Topologies

The coupled-inductor single-ended primary inductance converter (SEPIC) topology is shown in Figure 9.33. This converter uses a transformer with the addition of capacitor C_C which couples additional energy to the load. If the turns ratio (N = the ratio of the number of primary turns to the number of secondary turns) of the transformer in the SEPIC converter is 1:1, the capacitor serves only to recover the energy in the leakage inductance (i.e., that energy which is not perfectly coupled between the windings) and delivering it to the load. In that case, the relationship between input and output voltage is given by

$$V_{OUT} = V_{IN} \bullet \frac{D}{1 - D}. \qquad \text{Eq. 9-40}$$

For nonunity turns ratios the input/output relationship is highly nonlinear due to transfer of energy occurring via both the coupling between the windings and the capacitor C_C. For that reason, it is not analyzed here.

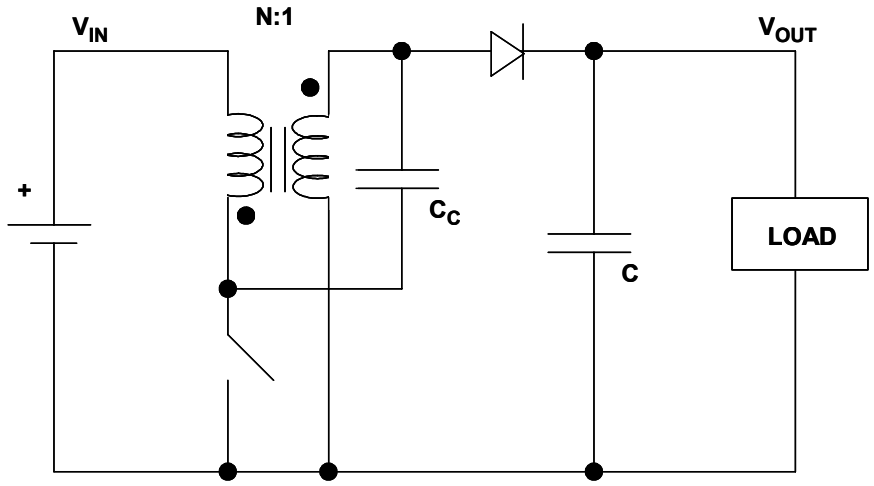


Figure 9.33: *Single-Ended Primary Inductance Converter (SEPIC)*

This converter topology often makes an excellent choice in nonisolated battery-powered systems for providing both the ability to step up or down the voltage, and, unlike the boost converter, the ability to have zero voltage at the output when desired.

The Zeta and Cük converters, not shown, are two examples of nonisolated converters which require capacitors to deliver energy from input to output, i.e., rather than just to store energy or deliver only recovered leakage energy, as the SEPIC can be configured via a 1:1 turns ratio. Because capacitors capable of delivering energy efficiently in such converters tend to be bulky and expensive, these converters are not frequently used.

Isolated Switching Regulator Topologies

The switching regulators discussed so far have direct galvanic connections between the input and output. Transformers can be used to supply galvanic isolation as well as allowing the buck-boost function to be easily performed. However, adding a transformer to the circuit creates a more complicated and expensive design as well as increasing the physical size.

The basic *flyback* buck-boost converter circuit is shown in Figure 9.34. It is derived from the buck-boost converter topology. When the switch is on, the current builds up in the primary of the transformer and energy is stored in the magnetic core. When the switch is opened, the current reverts to the secondary winding and flows through the diode delivering the stored energy into the load. The relationship between the input and output voltage is determined by the turns ratio, N, and the duty cycle, D, per the following equation:

$$V_{OUT} = \frac{V_{IN}}{N} \bullet \frac{D}{1 - D}. \qquad \text{Eq. 9-41}$$

One advantage of the flyback topology is that the transformer provides galvanic isolation as well as acting like an inductor (the transformer is more appropriately referred to as a coupled inductor in this application). A disadvantage of the flyback converter is the high energy which must be stored in the transformer in the form of dc current in the windings. This requires larger cores than would be necessary if the transformer just passed energy (instead of also acting as an inductor).

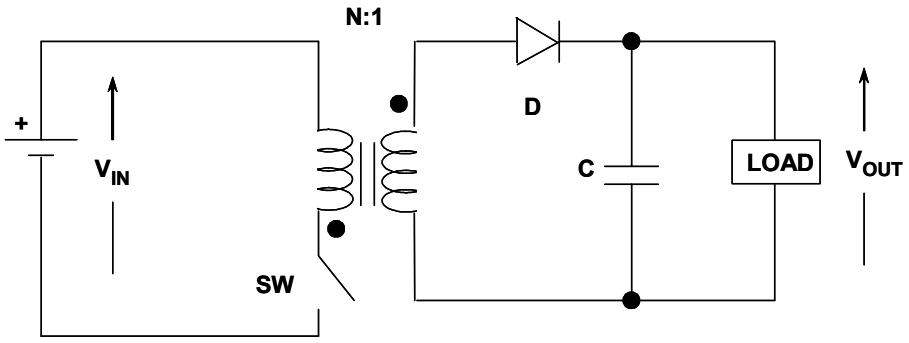
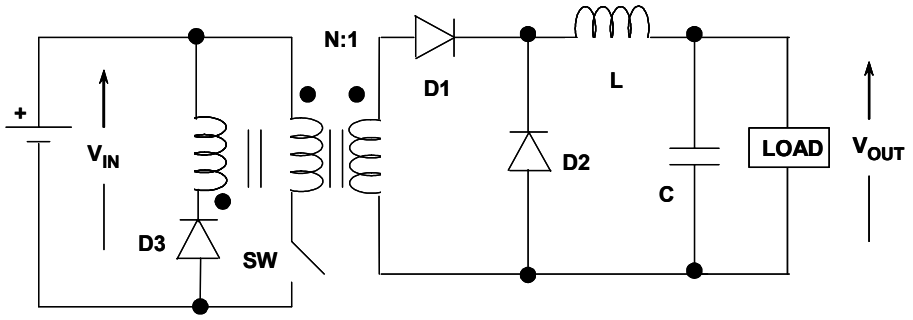


Figure 9.34: *Isolated Topology: Flyback Converter*

The basic *forward* converter topology is shown in Figure 9.35. It is derived from the buck converter. This topology avoids the problem of having to store large amounts of energy in the transformer core. However, the circuit is more complex and requires an additional magnetic element (a transformer), an inductor, an additional transformer winding, plus three diodes. When the switch is on, current builds up in the primary winding and also in the secondary winding, where it is transferred to the load through diode D1. When the switch is on, the current in the inductor flows out of D1 from the transformer and is reflected back to the primary winding according to the turns ratio. Additionally, a current (called a *magnetization current*) builds up in the primary due to the input voltage applied across the primary inductance, called the *magnetizing inductance*, flows in the primary winding. When the switch is opened, the current in the inductor continues to flow through the load via the return path provided by diode D2. The load current is no longer reflected into the transformer, but the magnetizing current induced in the primary still requires a return path so that the transformer can be *reset*. Hence the extra *reset* winding and diode are needed.

The relationship between the input and output voltage is given by:

$$V_{OUT} = \frac{V_{IN}}{N} \bullet D . \qquad \text{Eq. 9-42}$$



(BUCK DERIVED)

$$V_{OUT} = \frac{V_{IN}}{N} \bullet D$$

D = Duty Cycle

Figure 9.35: *Isolated Topology: Forward Converter*

There are many other possible isolated switching regulator topologies which use transformers, however, the balance of this section will focus on nonisolated topologies because of their wider application in portable and distributed power systems.

Switch Modulation Techniques

Important keys to understanding switching regulators are the various methods used to control the switch. For simplicity of analysis, the examples previously discussed used a simple fixed-frequency pulse width modulation (PWM) technique. There can be two other standard variations of the PWM technique: variable frequency constant on-time, and variable frequency constant off-time.

In the case of a buck converter, using a fixed off-time ensures that the peak-to-peak output ripple current in the inductor current remains constant as the input voltage varies. This is illustrated in Figure 9.36, where the output current is shown for two conditions of input voltage. Note that as the input voltage increases, the slope during the on-time increases, but the on-time decreases, thereby causing the frequency to increase. Fixed off-time control techniques are popular for buck converters where a wide input voltage range must be accommodated. The ADP1147 family implements this switch modulation technique.

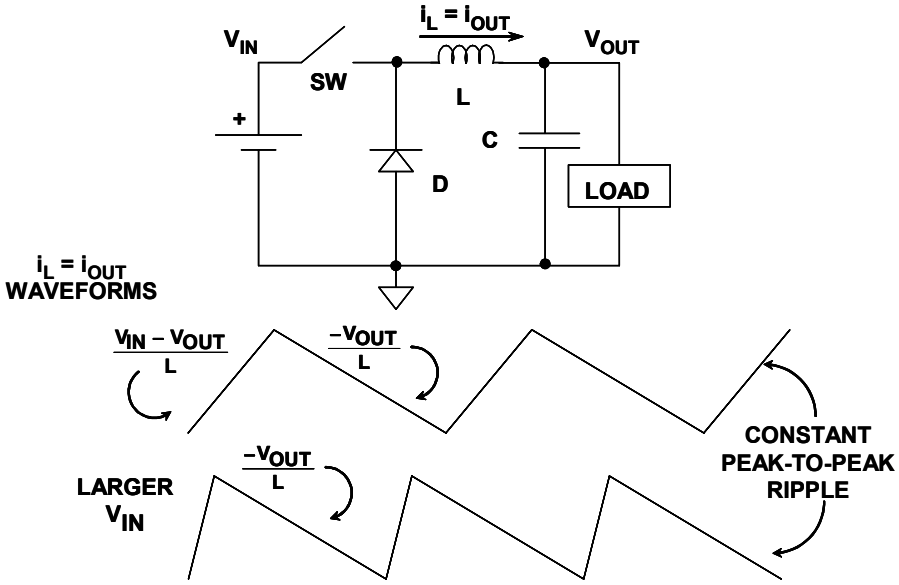


Figure 9.36: *Control of a Buck Converter using Fixed Off-Time, Variable Frequency PWM*

In the case of a boost converter, however, neither input ramp slopes nor output ramp slopes are solely a function of the output voltage (see Figure 9.35), so there is no inherent advantage in the variable frequency constant off-time modulation method with respect to maintaining constant output ripple current. Still, that modulation method tends to allow for less ripple current variation than does fixed frequency, so it is sometimes used.

In the case where very low duty cycles are needed, e.g., under short-circuit conditions, sometimes the limitation of a minimum achievable duty cycle is encountered. In such

cases, in order to maintain a steady-state condition and prevent runaway of the switch current, a pulse skipping function must be implemented to reduce effective duty cycle. This might take the form of a current monitoring circuit which detects that the switch current is excessive. So either a fixed frequency cycle is skipped without turning on the switch, or the off-time is extended in some way to delay the turn-on.

The pulse skipping technique for a fixed frequency controller can be applied even to operation at *normal* duty cycles. Such a switch modulation technique is then referred to as *pulse burst modulation* (PBM). At its simplest, this technique simply gates a fixed frequency, fixed duty cycle oscillator to be applied to the switch or not. The duty cycle of the oscillator sets the maximum achievable duty cycle for the converter, and smaller duty cycles are achieved over an average of a multiplicity of pulses by skipping oscillator cycles. This switch modulation method accompanies a simple control method of using a hysteretic comparator to monitor the output voltage versus a reference and decide whether to use the oscillator to turn on the switch for that cycle or not. The hysteresis of the comparator tends to give rise to several cycles of switching followed by several cycles of not switching. Hence, the resulting switching signal is characterized by pulses which tend to come in bursts—hence the name for the modulation technique.

There are at least two inherent fundamental drawbacks of the PBM switch modulation technique. First, the constant variation of the duty cycle between zero and maximum produces high ripple currents and accompanying losses. Second, there is an inherent generation of subharmonic frequencies with respect to the oscillator frequency. This means that the noise spectrum is not well controlled, and often audible frequencies can be produced. This is often apparent in higher power converters which use pulse skipping to maintain short-circuit current control. An audible noise can often be heard under such a condition, due to the large magnetic elements acting like speaker voice coils. For these reasons, PBM is seldom used at power levels above ~10 Watts, but for its simplicity, it is often preferred below that power level, but above a power level or with a power conversion requirement where charge pumps are not well suited.

Control Techniques

Though often confused with or used in conjunction with discussing the switch modulation technique, the control technique refers to what parameters of operation are monitored and how they are processed to control the modulation of the switch. The specific way in which the switch is modulated can be thought of separately, and was just presented in the previous section.

In circuits using PBM for switch modulation, the control technique typically used is a voltage-mode hysteretic control. In this implementation the switch is controlled by monitoring the output voltage and modulating the switch such that the output voltage oscillates between two hysteretic limits. The ADP3000 switching regulator is an example of a regulator which combines these modulation and control techniques.

Figure 9.37 shows the most basic control technique for use with PWM is *voltage-mode (VM) control*. Here, the output voltage is the only parameter used to determine how the

switch will be modulated. An error amplifier (first mentioned in the Buck Converter section) monitors the output voltage, its error is amplified with the required frequency compensation for maintaining stability of the control loop, and the switch is modulated directly in proportion to that amplifier output.

The output voltage is divided down by a ratio-matched resistor divider and drives one input of an amplifier, G. A precision reference voltage (V_{REF}) is applied to the other input of the amplifier. The output of the amplifier in turn controls the duty cycle of the PWM. It is important to note that the resistor divider, amplifier, and reference are actually part of the switching regulator IC, but are shown externally in the diagram for clarity. The output voltage is set by the resistor divider ratio and the reference voltage:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right). \qquad \text{Eq. 9-43}$$

The internal resistor ratios and the reference voltage are set to produce standard output voltage options such as 12 V, 5 V, 3.3 V, or 3 V. In some regulators, the resistor divider can be external, allowing the output voltage to be adjusted.

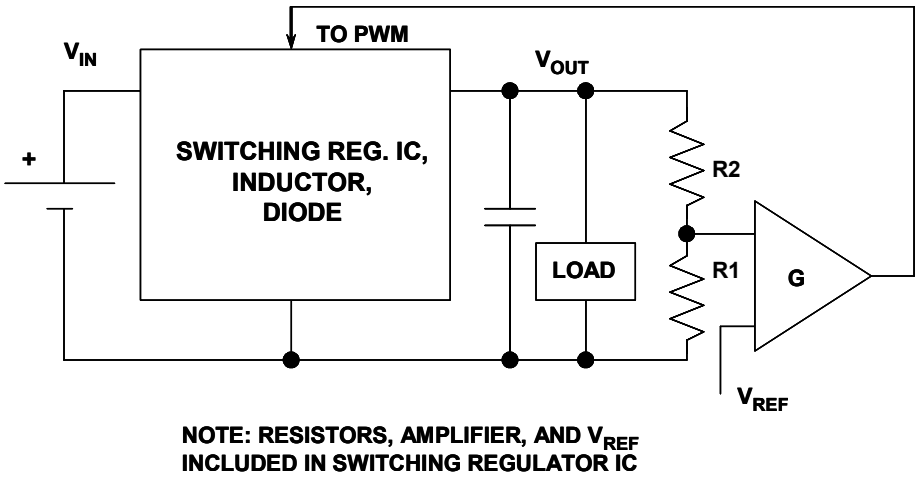


Figure 9.37: *Voltage Feedback for PWM Control*

A simple modification of VM control is voltage *feedforward*. This technique adjusts the duty cycle automatically as the input voltage changes so that the feedback loop does not have to make an adjustment (or as much of an adjustment). Voltage feedforward can even be used in the simple PBM regulators. Feedforward is especially useful in applications where the input voltage can change suddenly or, perhaps due to current limit protection limitations, it is desirable to limit the maximum duty cycle to lower levels when the input voltage is higher.

In switchers, the VM control loop needs to be compensated to provide stability, considering that the voltage being controlled by the modulator is the average voltage

produced at the switched node, whereas the actual output voltage is filtered through the switcher's LC filter. The phase shift produced by the filter can make it difficult to produce a control loop with a fast response time.

A popular way to circumvent the problem produced by the LC filter phase shift is to use current-mode (CM) control as shown in Figure 9.38. In current-mode control, it is still desirable, of course, to regulate the output voltage. Thus, an error amplifier (G1) is still required. However, the switch modulation is no longer controlled directly by the error amplifier. Instead, the inductor current is sensed, amplified by G2, and used to modulate the switch in accordance with the command signal from the [output voltage] error amplifier. It should be noted that the divider network, V_{REF}, G1 and G2 are usually part of the IC switching regulator itself, rather than external as shown in the simplified diagram.

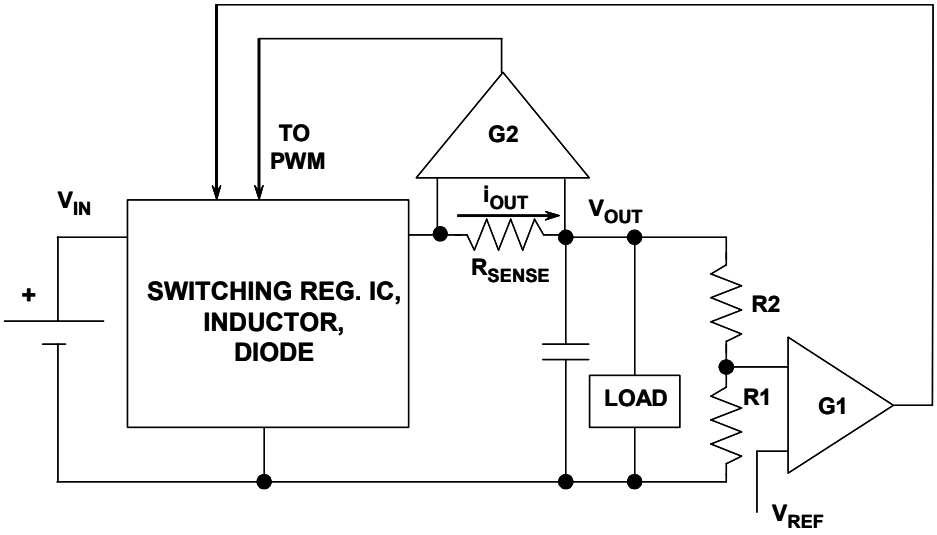


Figure 9.38: *Current Feedback for PWM Control*

The CM control system uses feedback from both the output voltage and output current. Recall that at the beginning of each PWM cycle, the switch turns on, and the inductor current begins to rise. The inductor current develops a voltage across the small sense resistor, R_{SENSE}, which is amplified by G2 and fed back to the PWM controller to turn off the switch. The output voltage, sensed by amplifier G1 and also fed back to the PWM controller, sets the level at which the peak inductor current will terminate the switch on-time. Since it is inductor current that turns off the switch (and thereby sets the duty cycle) this method is commonly referred to as *current-mode* control, even though there are actually two feedback control loops: the fast responding current loop, and the slower responding output voltage loop. Note that inductor current is being controlled on a pulse-by-pulse basis, which simplifies protection against switch over-current and inductor saturation conditions.

In essence, then, in CM control, rather than controlling the average voltage which is applied to the LC filter as in VM control, the inductor current is controlled directly on a cycle-by-cycle basis. The only phase shift remaining between the inductor current and the output voltage is that produced by the impedance of the output capacitor(s). The correspondingly lower phase shift in the output filter allows the loop response to be faster while still remaining stable. Also, instantaneous changes in input voltage are immediately reflected in the inductor current, which provides excellent line transient response. The obvious disadvantage of CM control is the requirement of sensing current and, if needed, an additional amplifier. With increasingly higher performance requirements in modern electronic equipment, the performance advantage of CM control typically outweighs the cost of implementation. Also, some sort of current limit protection is often required, whatever the control technique. Thus it tends to be necessary to implement some sort of current sensing even in VM-controlled systems.

Now even though we speak of a CM controller as essentially controlling the inductor current, more often than not the switch current is controlled instead, since it is more easily sensed (especially in a switching regulator) and it is a representation of the inductor current for at least the on-time portion of the switching cycle. Rather than actually controlling the average switch current, which is not the same as the average inductor current anyway, it is often simpler to control the peak current - which is the same for both the switch and the inductor in all the basic topologies. The error between the average inductor current and the peak inductor current produces a non-linearity within the control loop. In most systems, that is not a problem. In other systems, a more precise current control is needed, and in such a case, the inductor current is sensed directly and amplified and frequency-compensated for the best response.

Other control variations are possible, including *valley* rather than peak control, *hysteretic current* control, and even *charge* control—a technique whereby the integral of the inductor current (i.e., charge) is controlled. That eliminates even the phase shift of the output capacitance from the loop, but presents the problem that instantaneous current is not controlled, and therefore short-circuit protection is not inherent in the system. All techniques offer various advantages and disadvantages. Usually the best tradeoff between performance and cost/simplicity is peak-current control - as used by the ADP1147 family. This family also uses the current-sense output to control a *sleep, or power saving mode* of operation to maintain high efficiency for low output currents.

Gated Oscillator (Pulse Burst Modulation) Control Example

All of the PWM techniques discussed thus far require some degree of feedback loop compensation. This can be especially tricky for boost converters, where there is more phase shift between the switch and the output voltage.

As previously mentioned, a technique which requires no feedback compensation uses a fixed frequency gated oscillator as the switch control (see Figure 9.39). This method is often (incorrectly) referred to as the Pulse Frequency Modulation (PFM) mode, but is more correctly called *pulse burst modulation (PBM)* or *gated-oscillator* control.

The output voltage (V_{OUT}) is divided by the resistive divider (R1 and R2) and compared against a reference voltage, V_{REF}. The comparator hysteresis is required for stability and also affects the output voltage ripple. When the resistor divider output voltage drops below the comparator threshold (V_{REF} minus the hysteresis voltage), the comparator starts the gated oscillator. The switcher begins switching again which then causes the output voltage to increase until the comparator threshold is reached (V_{REF} plus the hysteresis voltage), at which time the oscillator is turned off. When the oscillator is off, quiescent current drops to a very low value (for example, 95 μA in the ADP1073) making PBM controllers very suitable for battery-powered applications.

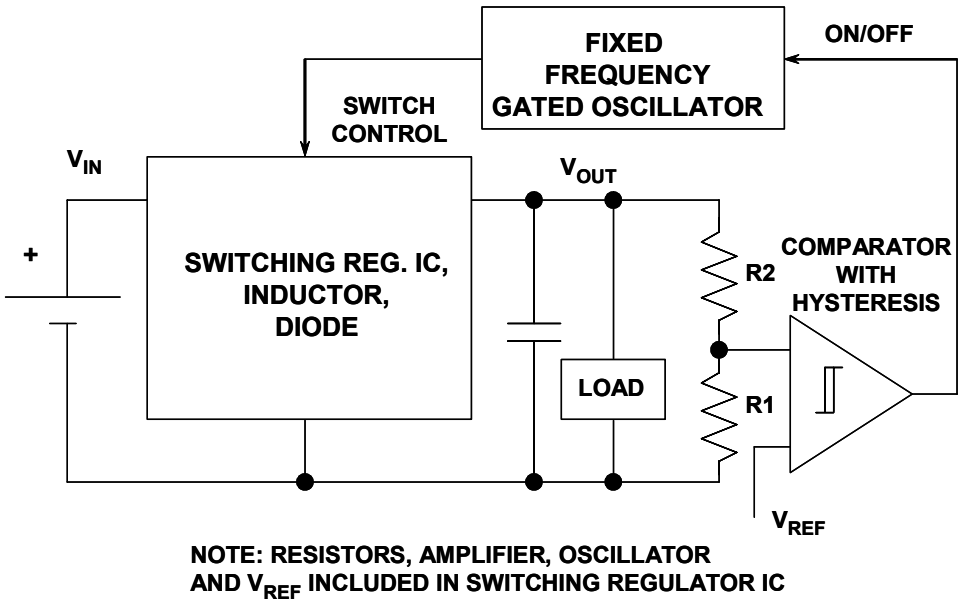


Figure 9.39: *Switch Control Using Gated Oscillator (Pulse Burst Modulation, PBM)*

A simplified output voltage waveform is shown in Figure 9.40 for a PBM buck converter. Note that the comparator hysteresis voltage multiplied by the reciprocal of the attenuation factor primarily determines the peak-to-peak output voltage ripple (typically between 50 mV and 100 mV). It should be noted that the actual output voltage ripple waveform can look quite different from that shown in Figure 3.30 depending on the design and whether the converter is a buck or boost.

A practical switching regulator IC using the PBM approach is the ADP3000, which has a fixed switching frequency of 400 kHz and a fixed duty cycle of 80%. This device is a versatile step-up/step-down converter. It can deliver an output current of 100 mA in a 5 V to 3 V step-down configuration and 180 mA in a 2 V to 3.3 V step-up configuration. Input supply voltage can range between 2 V and 12 V in the boost mode, and up to 30 V

in the buck mode. It should be noted that when the oscillator is turned off, the internal switch is opened so that the inductor current does not continue to increase.

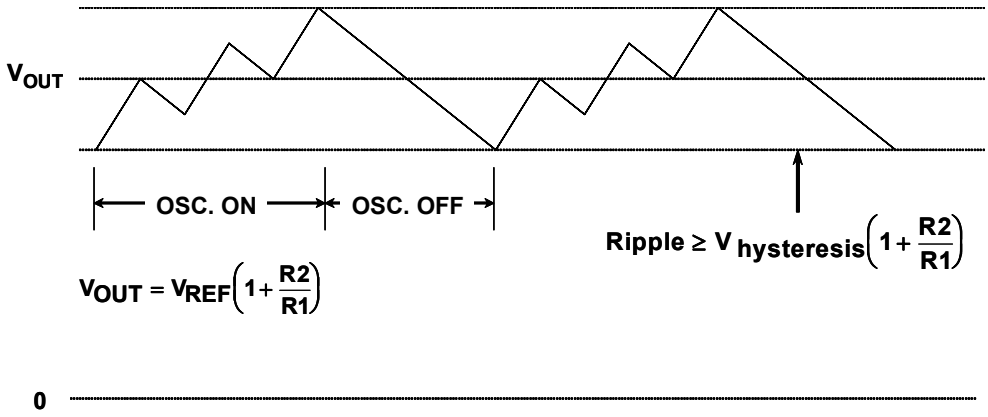


Figure 9.40: *Representative Output Voltage Waveform for Gated Oscillator Controlled (PBM) Buck Regulators*

In the gated-oscillator method, the comparator hysteresis serves to stabilize the feedback loop making the designs relatively simple. The disadvantage, of course, is that the peak-to-peak output voltage ripple can never be less than the comparator hysteresis multiplied by the reciprocal of the attenuation factor:

$$\text{Output Ripple} \geq V_{hysteresis}\left(\frac{R2}{R1}\right). \qquad \text{Eq. 9-44}$$

Because the gated-oscillator (PBM) controlled switching regulator operates with a fixed duty cycle, output regulation is achieved by changing the number of "skipped pulses" as a function of load current and voltage. From this perspective, PBM controlled switchers tend to operate in the "discontinuous" mode under light load conditions. Also, the maximum average duty cycle is limited by the built-in duty cycle of the oscillator. Once the required duty cycle exceeds that limit, no pulse skipping occurs, and the device will lose regulation.

One disadvantage of the PBM switching regulator is that the frequency spectrum of the output ripple is "fuzzy" because of the burst-mode of operation. Frequency components may fall into the audio band, so proper filtering of the output of such a regulator is mandatory.

Selection of the inductor value is also more critical in PBM regulators. Because the regulation is accomplished with a burst of fixed duty cycle pulses (i.e., higher than needed on average) followed by an extended off time, the energy stored in the inductor during the burst of pulses must be sufficient to supply the required energy to the load. If the inductor value is too large, the regulator may never start up, or may have poor transient response and inadequate line and load regulation. On the other hand, if the inductor value is too small, the inductor may saturate during the charging time, or the

peak inductor current may exceed the maximum rated switch current. However, devices such as the ADP3000 incorporate on-chip overcurrent protection for the switch. An additional feature allows the maximum peak switch current to be set with an external resistor, thereby preventing inductor saturation. Techniques for selecting the proper inductor value will be discussed in a following section.

Diode and Switch Considerations

So far, we have based our discussions around an ideal lossless switching regulator having ideal circuit elements. In practice, the diode, switch, and inductor all dissipate power which leads to less than 100% efficiency.

Figure 9.41 shows typical buck and boost converters, where the switch is part of the IC. The process is bipolar, and this type of transistor is used as the switching element. The ADP3000 and its relatives (ADP1108, ADP1109, ADP1110, ADP1111, ADP1073, and ADP1173) use this type of internal switch.

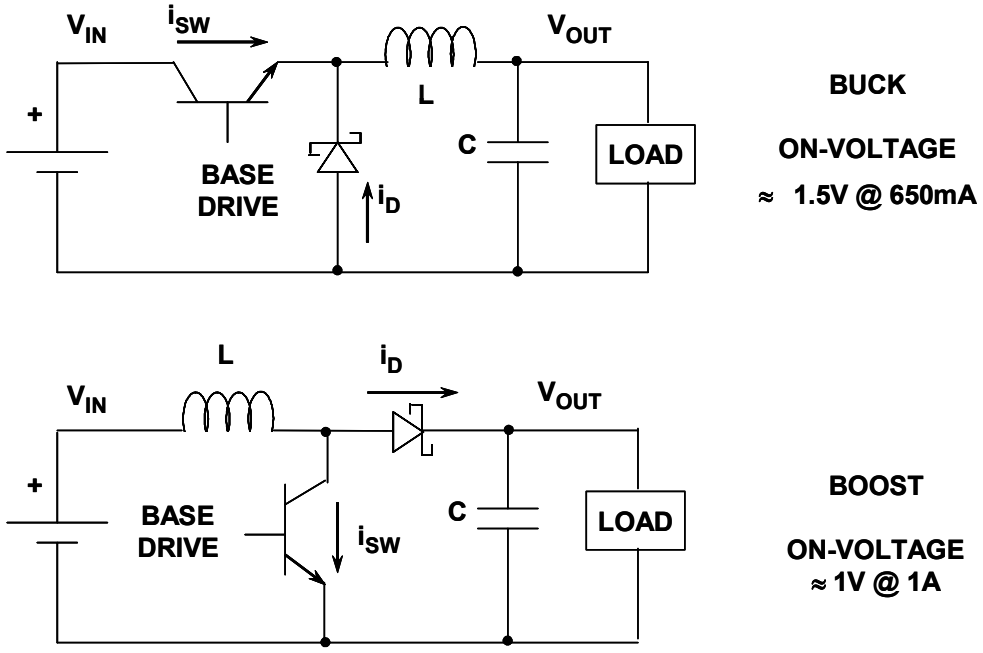


Figure 9.41: *NPN Switches in IC Regulators*

The diode is external to the IC and must be chosen carefully. Current flows through the diode during the off-time of the switching cycle. This translates into an average current which causes power dissipation because of the diode forward voltage drop. The power dissipation can be minimized by selecting a Schottky diode with a low forward drop (0.5 V), such as the 1N5818-type. It is also important that the diode capacitance and recovery time be low to prevent additional power loss due to charging current, and this is

also afforded by the Schottky diode. Power dissipation can be approximated by multiplying the average diode current by the forward voltage drop.

The drop across the NPN switch also contributes to internal power dissipation. The power (neglecting switching losses) is equal to the average switch current multiplied by the collector-emitter on-state voltage. In the case of the ADP3000 series, it is 1.5 V at the maximum rated switch current of 650 mA (when operating in the buck mode).

In the boost mode, the NPN switch can be driven into saturation, so the on-state voltage is reduced, and thus, so is the power dissipation. Note that in the case of the ADP3000, the saturation voltage is about 1V at the maximum rated switch current of 1 A.

In examining the two configurations, it would be logical to use a PNP switching transistor in the buck converter and an NPN transistor in the boost converter in order to minimize switch voltage drop. However, the PNP transistors available on processes which are suitable for IC switching regulators generally have poor performance, so the NPN transistor must be used for both topologies.

In addition to lowering efficiency by their power dissipation, the switching transistors and the diode also affect the relationship between the input and output voltage. The equations previously developed assumed zero switch and diode voltage drops. Rather than re-deriving all the equations to account for these drops, we will examine their effects on the inductor current for a simple buck and boost converter operating in the continuous mode as shown in Figure. 9.42.

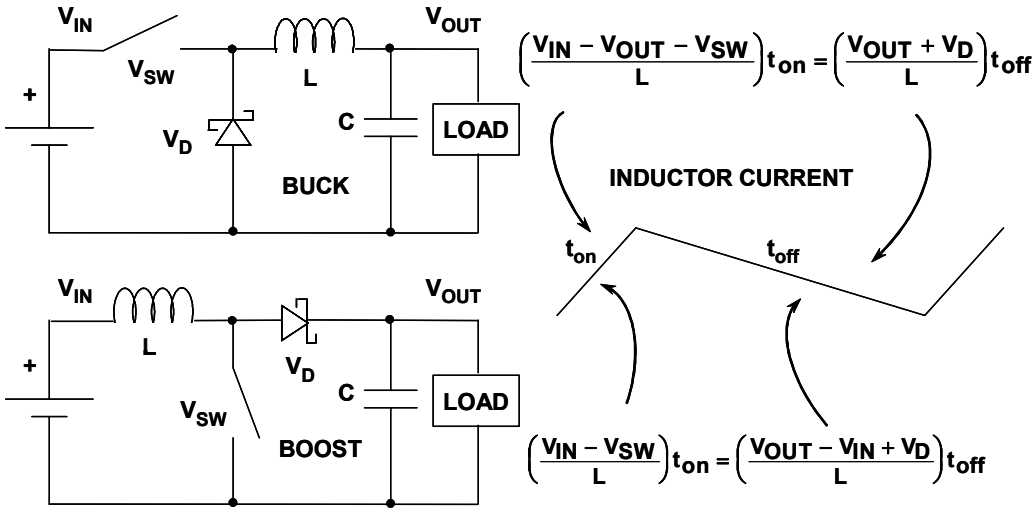


Figure 9.42: *Effects of Switch and Diode Voltage on Inductor Current Equations*

In the buck converter, the voltage applied to the inductor when the switch is on is equal to $V_{IN} - V_{OUT} - V_{SW}$, where V_{SW} is the approximate average voltage drop across the switch. When the switch is off, the inductor current is discharged into a voltage equal to

$V_{OUT} + V_D$, where V_D is the approximate average forward drop across the diode. The basic inductor equation used to derive the relationship between the input and output voltage becomes:

$$\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right)t_{on} = \left(\frac{V_{OUT} + V_D}{L}\right)t_{off}. \qquad \text{Eq. 9-45}$$

In the actual regulator circuit, negative feedback will force the duty cycle to maintain the correct output voltage, but the duty cycle will also be affected by the switch and the diode drops to a lesser degree.

When the switch is on in a boost converter, the voltage applied to the inductor is equal to $V_{IN} - V_{SW}$. When the switch is off, the inductor current discharges into a voltage equal to $V_{OUT} - V_{IN} + V_D$. The basic inductor current equation becomes:

$$\left(\frac{V_{IN} - V_{SW}}{L}\right)t_{on} = \left(\frac{V_{OUT} - V_{IN} + V_D}{L}\right)t_{off}. \qquad \text{Eq. 9-46}$$

From the above equations, the basic relationships between input voltage, output voltage, duty cycle, switch, and diode drops can be derived for the buck and boost converters.

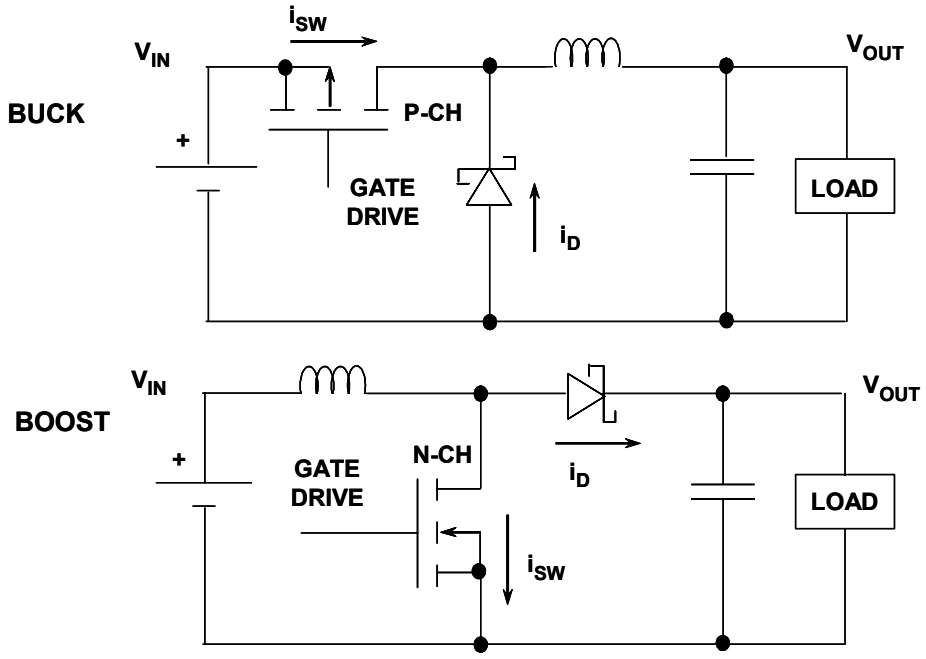


Figure 9.43: *Power MOSFET Switches*

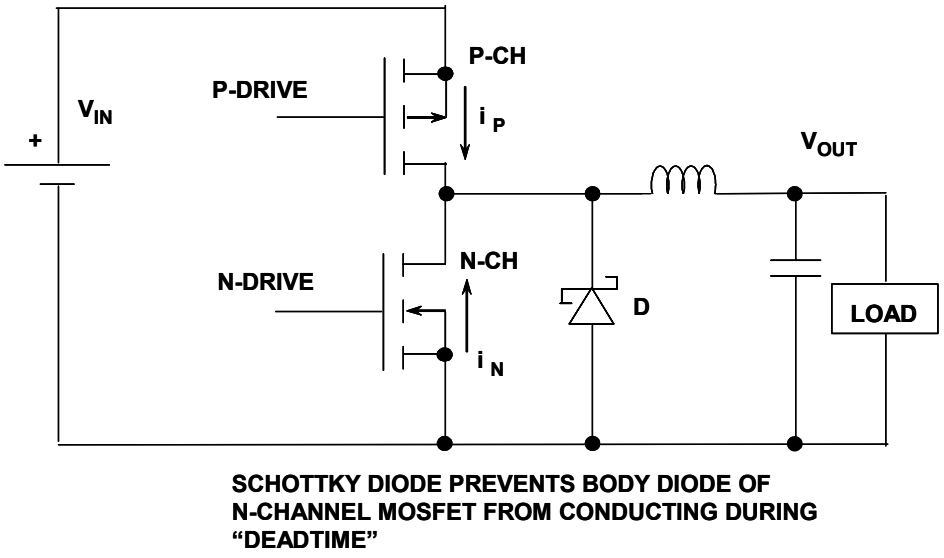


Figure 9.44: *Buck Converter with Synchronous Switch Using P- and N-Channel MOSFETS*

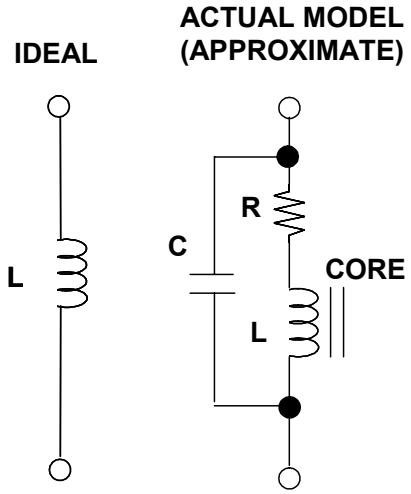
Inductor Considerations

The selection of the inductor used in a switching regulator is probably the most difficult part of the design. Fortunately, manufacturers of switching regulators supply a wealth of applications information, and standard off-the-shelf inductors from well-known and reliable manufacturers are quite often recommended on the switching regulator data sheet. However, it is important for the design engineer to understand at least some of the fundamental issues relating to inductors. This discussion, while by no means complete, will give some insight into the relevant magnetics issues.

Selecting the actual value for the inductor in a switching regulator is a function of many parameters. Fortunately, in a given application the exact value is generally not all that critical, and equations supplied on the data sheets allow the designer to calculate a minimum and maximum acceptable value. That's the easy part.

Unfortunately, there is more to a simple inductor than its inductance! Figure 9.45 shows an equivalent circuit of a real inductor and also some of the many considerations that go into the selection process. To further complicate the issue, most of these parameters interact, thereby making the design of an inductor truly more of an art than a science.

Probably the easiest inductor problem to solve is selecting the proper value. In most switching regulator applications, the exact value is not very critical, so approximations can be used with a high degree of confidence.



- Inductance Value, L
- Saturation Current
- Inductor Losses:
  - Hysteresis Loss
  - Eddy Current Loss
  - Winding Loss
- Heating
- EMI/RFI
- Self-Resonant Frequency

- Core Material
- Form Factor, Core Volume
- Number of Turns
- Wire Size, Spacing
- Temperature
- Operating Current
- Operating Frequency

Figure 9.45: *Inductor Considerations*

The heart of a switching regulator analysis involves a thorough understanding of the inductor current waveform. Figure 9.46 shows an assumed inductor current waveform (which is also the output current) for a buck converter, such as the ADP3000, which uses the gated-oscillator PBM switch modulation technique. Note that this waveform represents a worst case condition from the standpoint of storing energy in the inductor, where the inductor current starts from zero on each cycle. In high output current applications, the inductor current does not return to zero, but ramps up until the output voltage comparator senses that the oscillator should be turned off, at which time the current ramps down until the comparator turns the oscillator on again. This assumption about the worst case waveform is necessary because in a simple PBM regulator, the oscillator duty cycle remains constant regardless of input voltage or output load current. Selecting the inductor value using this assumption will always ensure that there is enough energy stored in the inductor to maintain regulation.

It should be emphasized that the following inductance calculations for the PBM buck and boost regulators should be used only as a starting point, and larger or smaller values may actually be required depending on the specific regulator and the input/output conditions.

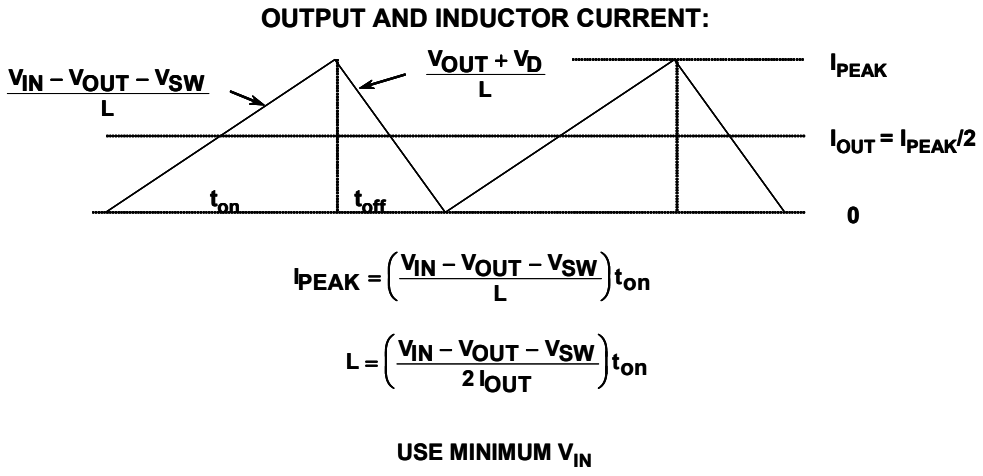


Figure 9.46: *Calculating L for a Buck Converter: Gated Oscillator (PBM) Type*

The peak current is easily calculated from the slope of the positive-going portion of the ramp:

$$I_{PEAK} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right) t_{on} . \qquad \text{Eq. 9-47}$$

This equation can then be solved for L:

$$L = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{I_{PEAK}}\right) t_{on} . \qquad \text{Eq. 9-48}$$

However, the average output current, I_{OUT} is equal to $I_{PEAK}/2$, and therefore $I_{PEAK}=2I_{OUT}$. Substituting this value for I_{PEAK} into the previous equation yields:

$$L = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{2I_{OUT}}\right) t_{on} . \qquad \text{Eq. 9.49}$$

[L for buck PBM Converter]

The minimum expected value of V_{IN} should be used in order to minimize the inductor value and maximize its stored energy. If V_{IN} is expected to vary widely, an external resistor can be added to the ADP3000 to limit peak current and prevent inductor saturation at maximum V_{IN}.

A similar analysis can be carried out for a boost PBM regulator as shown in Figure 9.47.

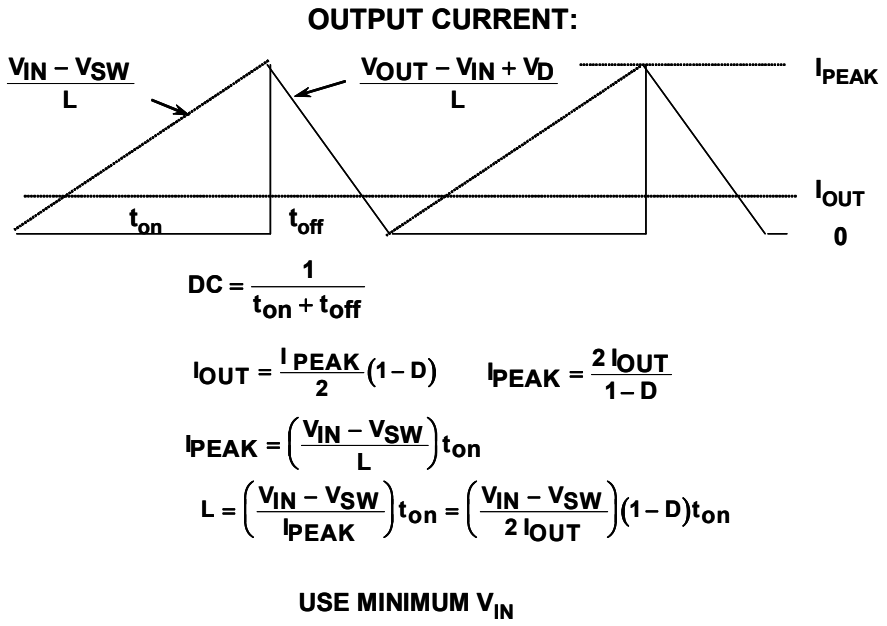


Figure 9.47: *Calculating L for a Boost Converter: Gated Oscillator (PBM) Type*

We make the same assumptions about the inductor current, but note that the output current shown on the diagram is pulsating and not continuous. The output current, I_{OUT}, can be expressed in terms of the peak current, I_{PEAK}, and the duty cycle, D, as:

$$I_{OUT} = \frac{I_{PEAK}}{2}(1 - D). \qquad \text{Eq. 9-50}$$

Solving for I_{PEAK} yields:

$$I_{PEAK} = \frac{2I_{OUT}}{1 - D}. \qquad \text{Eq. 9-51}$$

However, I_{PEAK} can also be expressed in terms of V_{IN}, V_{SW}, L, and t_{on}:

$$I_{PEAK} = \left(\frac{V_{IN} - V_{SW}}{L}\right) t_{on}, \qquad \text{Eq. 9-52}$$

which can be solved for L:

$$L = \left(\frac{V_{IN} - V_{SW}}{I_{PEAK}}\right) t_{on}. \qquad \text{Eq. 9-53}$$

Substituting the previous expression for I_{PEAK} yields:

$$L = \left(\frac{V_{IN} - V_{SW}}{2I_{OUT}}\right)(1 - D)t_{on}. \qquad \text{Eq. 9-54}$$

[L for boost PBM Converter]

The minimum expected value of V_{IN} should be used in order to ensure sufficient inductor energy storage under all conditions. If V_{IN} is expected to vary widely, an external resistor can be added to the ADP3000 to limit peak current and prevent inductor saturation at maximum V_{IN}.

The above equations will only yield approximations to the proper inductor value for the PBM-type regulators and should be used only as a starting point. An exact analysis is difficult and highly dependent on the regulator and input/output conditions. However, there is considerable latitude with this type of regulator, and other analyses may yield different results but still fall within the allowable range for proper regulator operation.

Calculating the proper inductor value for PWM regulators is more straightforward. Figure 9.48 shows the output and inductor current waveform for a buck PWM regulator operating in the continuous mode. It is accepted design practice to design for a peak-to-peak ripple current, I_{pp}, which is between 10% and 30% of the output current, I_{OUT}. We will assume that $I_{pp} = 0.2*I_{OUT}$.

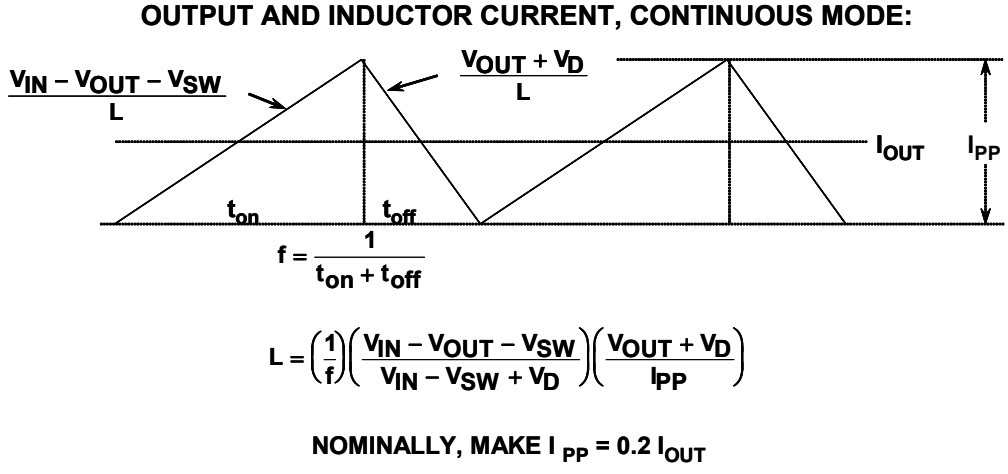


Figure 9.48: *Calculating L for a Buck Converter: Constant Frequency PWM Type*

By inspection, we can write:

$$\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right)t_{on} = \left(\frac{V_{OUT} + V_D}{L}\right)t_{off}, \quad \text{Eq. 9-55}$$

or

$$t_{off} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{V_{OUT} + V_D}\right)t_{on}. \quad \text{Eq. 9-56}$$

However, the switching frequency, f, is given by:

$$f = \frac{1}{t_{on} + t_{off}}, \quad \text{Eq. 9-57}$$

or:

$$t_{off} = \frac{1}{f} - t_{on}. \quad \text{Eq. 9-58}$$

Substituting this expression for t_{off} in the previous equation for t_{off} and solving for t_{on} yields:

$$t_{on} = \frac{1}{f}\left(\frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right). \quad \text{Eq. 9-59}$$

However,

$$I_{pp} = \left(\frac{V_{IN} - V_{OUT} - V_{SW}}{L}\right)t_{on}. \quad \text{Eq. 9-60}$$

Combining the last two equations and solving for L yields:

$$L = \left(\frac{1}{f}\right)\left(\frac{V_{IN} - V_{OUT} - V_{SW}}{V_{IN} - V_{SW} + V_D}\right)\left(\frac{V_{OUT} + V_D}{I_{pp}}\right). \quad \text{Eq. 9-61}$$

[L for buck PWM converter, constant frequency]

As indicated earlier, choose I_{pp} to be nominally $0.2*I_{OUT}$ and solve the equation for L. Calculate L for the minimum and maximum expected value of V_{IN} and choose a value halfway between. System requirements may dictate a larger or smaller value of I_{pp}, which will inversely affect the inductor value.

A variation of the buck PWM constant frequency regulator is the buck PWM regulator with variable frequency and constant off-time (e.g. ADP1148).

A diagram of the output and inductor current waveform is shown in Figure 9.49 for the continuous mode.

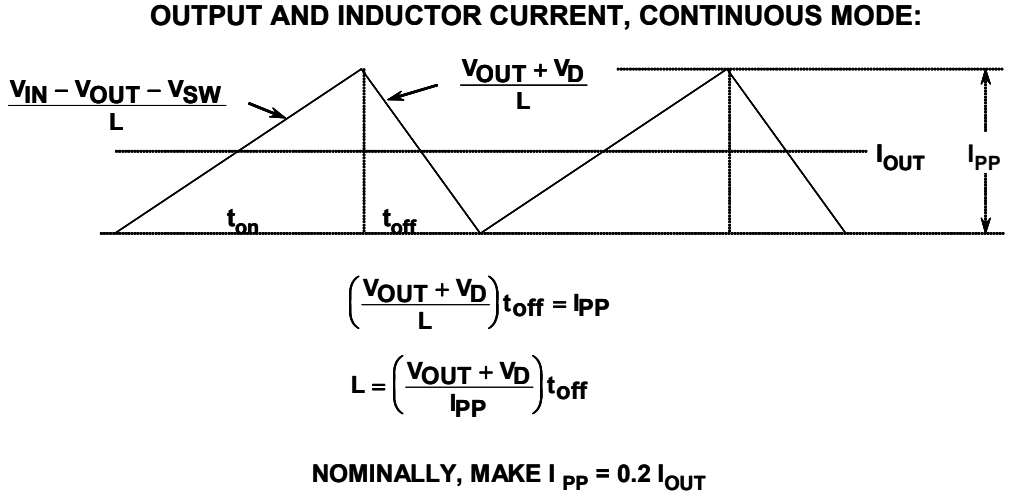


Figure 9.49: *Calculating L for a Buck Converter: Constant Off-Time, Variable Frequency PWM Type*

The calculations are very straightforward, since the peak-to-peak amplitude of the ripple current is constant:

$$I_{pp} = \left(\frac{V_{OUT} + V_D}{L}\right) t_{off}. \qquad \text{Eq. 9-62}$$

Solving for L:

$$L = \left(\frac{V_{OUT} + V_D}{I_{pp}}\right) t_{off}. \qquad \text{Eq. 9-63}$$

[L for buck PWM constant off-time, variable frequency converter]

Again, choose $I_{pp} = 0.2*I_{OUT}$, or whatever the system requires.

The final example showing the inductance calculation is for the boost PWM constant frequency regulator. The inductor (and input) current waveform is shown in Figure 9.50.

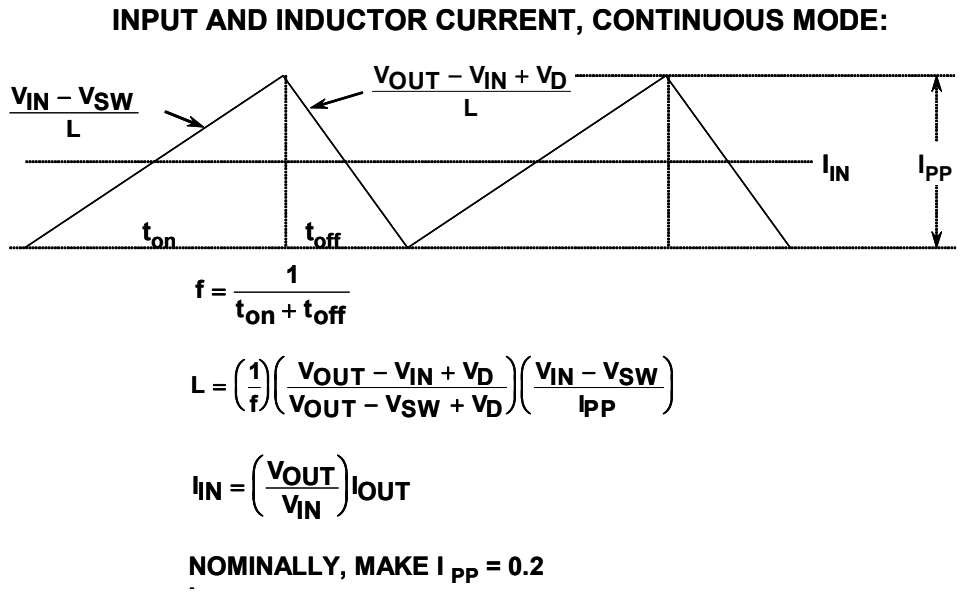


Figure 9.50: *Calculating L for a Boost Converter: Constant Frequency PWM Type*

The analysis is similar to that of the constant frequency buck PWM regulator.

By inspection of the inductor current, we can write:

$$\left(\frac{V_{IN} - V_{SW}}{L}\right) t_{on} = \left(\frac{V_{OUT} - V_{IN} + V_D}{L}\right) t_{off}, \qquad \text{Eq. 9-64}$$

or

$$t_{off} = \left(\frac{V_{IN} - V_{SW}}{V_{OUT} - V_{IN} + V_D}\right) t_{on}. \qquad \text{Eq. 9-65}$$

However, the switching frequency, f, is given by

$$f = \frac{1}{t_{on} + t_{off}}, \qquad \text{Eq. 9-66}$$

or

$$t_{off} = \frac{1}{f} - t_{on}. \qquad \text{Eq. 9-67}$$

Substituting this expression for t_{off} in the previous equation for t_{off} and solving for t_{on} yields:

$$t_{on} = \frac{1}{f}\left(\frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} - V_{SW} + V_D}\right). \qquad \text{Eq. 9-68}$$

However,

$$I_{pp} = \left(\frac{V_{IN} - V_{SW}}{L}\right) t_{on} . \qquad \text{Eq. 9-69}$$

Combining the last two equations and solving for L yields:

$$L = \left(\frac{1}{f}\right)\left(\frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} - V_{SW} + V_D}\right)\left(\frac{V_{IN} - V_{SW}}{I_{pp}}\right) . \qquad \text{Eq. 9-70}$$

[L for boost PWM, constant frequency converter]

For the boost converter, the inductor (input) current, I_{IN}, can be related to the output current, I_{OUT}, by:

$$I_{IN} = \left(\frac{V_{OUT}}{V_{IN}}\right) I_{OUT} . \qquad \text{Eq. 9-71}$$

Nominally, make $I_{pp} = 0.2 I_{IN}$.

Note that for the boost PWM, even though the input current is continuous, while the output current pulsates, we still base the inductance calculation on the peak-to-peak inductor ripple current.

As was previously suggested, the actual selection of the inductor value in a switching regulator is probably the easiest part of the design process. Choosing the proper type of inductor is much more complicated as the following discussions will indicate.

Fundamental magnetic theory says that if a current passes through a wire, a magnetic field will be generated around the wire (right-hand rule). The strength of this field is measured in ampere-turns per meter, or *oersteds* and is proportional to the current flowing in the wire. The magnetic field strength produces a *magnetic flux density* (B, measured in webers per square meter, or *gauss*).

Using a number of turns of wire to form a coil increases the magnetic flux density for a given current. The effective inductance of the coil is proportional to the ratio of the magnetic flux density to the field strength.

This simple air core inductor is not very practical for the values of inductance required in switching regulators because of wiring resistance, interwinding capacitance, sheer physical size, and other factors. Therefore, in order to make a reasonable inductor, the wire is wound around some type of ferromagnetic core having a high *permeability*. Core permeability is often specified as a relative permeability which is basically the increase in inductance which is obtained when the inductor is wound on a core instead of just air. A relative permeability of 1000, for instance, will increase inductance by 1000:1 above that of an equivalent air core.

Figure 9.51 shows magnetic flux density (B) versus inductor current for the air core and also ferromagnetic cores. Note that B is linear with respect to H for the air core inductor, i.e., the inductance remains constant regardless of current.

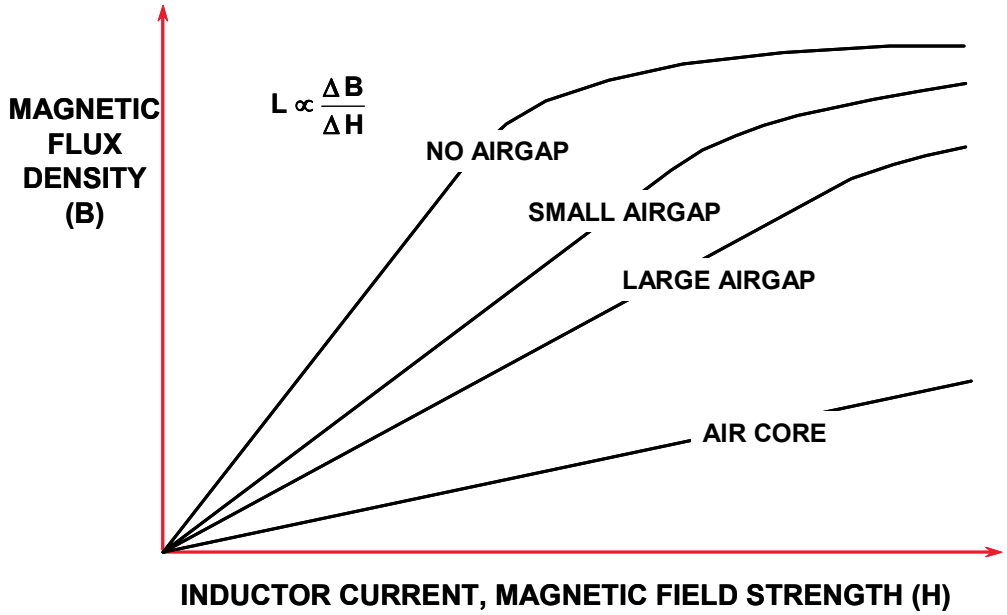


Figure 9.51: *Magnetic Flux Density vs. Inductor Current*

The addition of a ferromagnetic core increases the slope of the curve and increases the effective inductance, but at some current level, the inductor core will saturate (i.e., the inductance is drastically reduced). It is obvious that inductor saturation can wreck havoc in a switching regulator, and can even burn out the switch if it is not current-limited.

This effect can be reduced somewhat while still maintaining higher inductance than an air core by the addition of an air gap in the ferromagnetic core. The air gap reduces the slope of the curve, but provides a wider linear operating range of inductor current. Air gaps do have their problems, however, and one of them is the tendency of the air-gapped inductor to radiate high frequency energy more than a non-gapped inductor. Proper design and manufacturing techniques, however, can be used to minimize this EMI problem, so air-gapped cores are popular in many applications.

The effects of inductor core saturation in a switcher can be disastrous to the switching elements as well as lowering efficiency and increasing noise. Figure 9.52 shows a normal inductor current waveform in a switching regulator as well as a superimposed waveform showing the effects of core saturation. Under normal conditions the slope is linear for both the charge and discharge cycle. If saturation occurs, however, the inductor current increases exponentially, corresponding to the drop in effective inductance. It is therefore important in all switching regulator designs to determine the peak inductor current

expected under the worst case conditions of input voltage, load current, duty cycle, etc. This worst case peak current must be less than the peak-current rating of the inductor. Notice that when inductor literature does not have a "dc-current" rating, or shows only an "ac amps" rating, such inductors are often prone to saturation.

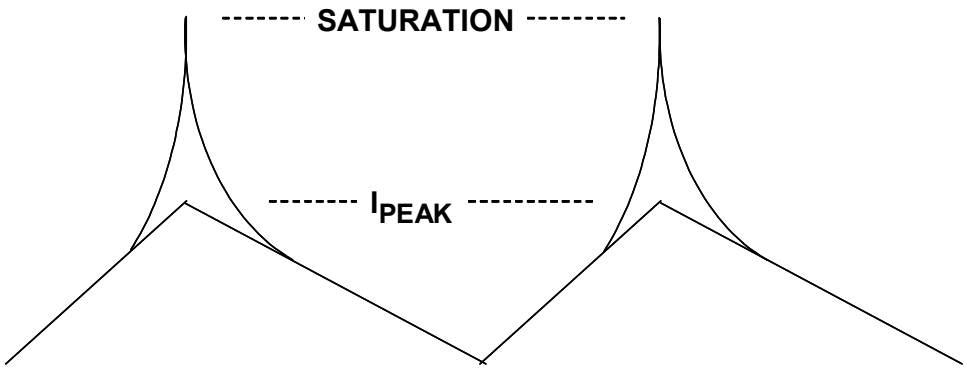


Figure 9.52: *Effects of Saturation on Inductor Current*

From a simplified design standpoint, the effects or presence of inductor saturation can best be observed with a scope and a current probe. If a current probe is not available, a less direct but still effective method is to measure the voltage across a small sense resistor in series with the inductor. The resistor value should be 1 Ω or less (depending on the inductor current), and the resistor must be sized to dissipate the power. In most cases, a 1 Ω, 1 W resistor will work for currents up to a few hundred mA, and a 0.1 Ω, 10 W resistor is good for currents up to 10 A.

Another inductor consideration is its loss. Ideally, an inductor should dissipate no power. However, in a practical inductor, power is dissipated in the form of hysteresis loss, eddy-current loss, and winding loss. Figure 9.53 shows a typical B/H curve for an inductor. The enclosed area swept out by the B/H curve during one complete operating cycle is the hysteresis loss exhibited by the core during that cycle. Hysteresis loss is a function of core material, core volume, operating frequency, and the maximum flux density during each cycle. The second major loss within the core is eddy-current loss. This loss is caused by the flow of circulating magnetic currents within the core material caused by rapid transitions in the magnetic flux density. It is also dependent on the core material, core volume, operating frequency, and flux density.

In addition to core loss, there is winding loss, the power dissipated in the dc resistance of the winding. This loss is a function of the wire size, core volume, and the number of turns.

In a switching regulator application, excessive loss will result in a loss of efficiency and high inductor operating temperatures.

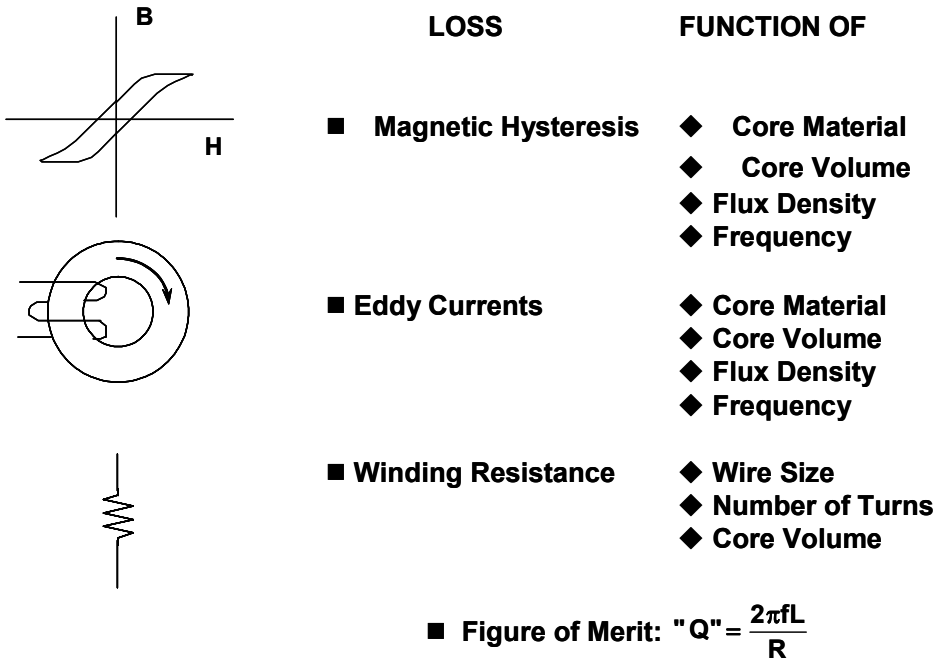


Figure 9.53: *Inductor Power Losses*

Fortunately, inductor manufacturers have simplified the design process by specifying maximum peak current, maximum continuous current, and operating frequency range and temperature for their inductors. If the designer derates the maximum peak and continuous current levels by a factor of 20% or so, the inductor should be satisfactory for the application. If these simple guidelines are observed, then the designer can be reasonably confident that the major sources of efficiency losses will be due to other parts of the regulator, i.e., the switch (I^2R®, gate charge, on-voltage), the diode (on-voltage), and the quiescent power dissipation of the regulator itself.

One method to ensure that the inductor losses do not significantly degrade the regulator performance is to measure the Q of the inductor at the switching frequency. If the Q is greater than about 25, then the losses should be insignificant.

There are many possible choices in inductor core materials: ferrite, molypermalloy (MPP) ferrite, powdered iron, etc. High efficiency converters generally cannot accommodate the core loss found in the low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy (MPP), or "Kool Mμ"® cores.

Ferrite core material saturates "hard," which causes the inductance to collapse abruptly when the peak current is exceeded. This results in a sharp increase in inductor ripple current.

Molypermalloy from Magnetics, Inc., is a very good, low loss core material for toroids, but is more expensive than ferrite. A reasonable compromise from the same manufacturer is "Kool Mμ."

The final consideration is the inductor self-resonant frequency. A practical example would be an inductor of 10 μH which has an equivalent distributed capacitance of 5 pF. The self-resonant frequency can be calculated as follows:

$$f_{resonance} = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} = 22 \text{ MHz.} \qquad \text{Eq. 9-72}$$

The switching frequency of the regulator should be at least ten times less than the resonant frequency. In most practical designs with switching frequencies less than 1 MHz this will always be the case, but a quick calculation is a good idea.

Capacitor Considerations

Capacitors play a critical role in switching regulators by acting as storage elements for the pulsating currents produced by the switching action. Although not shown on the diagrams previously, all switching regulators need capacitors on their inputs as well as their outputs for proper operation. The capacitors must have very low impedance at the switching frequency as well as the high frequencies produced by the pulsating current waveforms.

Recall the input and output current waveforms for the simple buck converter shown in Figure 9.54. Note that the input current to the buck converter is pulsating, while the output is continuous. Obviously, the input capacitor C_{IN} is critical for proper operation of the regulator. It must maintain the input at a constant voltage during the switching spikes. This says that the impedance of the capacitor must be very low at high frequencies, much above the regulator switching frequency. The load capacitor is also critical in that its impedance will determine the peak-to-peak output voltage ripple, but its impedance at high frequencies is not as critical due to the continuous nature of the output current waveform.

The situation is reversed in the case of the boost converter shown in Figure 9.55. Here the input waveform is continuous, while the output waveform is pulsating. The output capacitor must have good low and high frequency characteristics in order to minimize the output voltage ripple. Boost converters are often followed by a post filter to remove the high frequency switching noise.

Switching regulator capacitors are generally of the electrolytic type because of the relatively large values required. An equivalent circuit for an electrolytic capacitor is shown in Figure 9.56. In addition to the capacitance value itself, the capacitor has some equivalent series resistance (ESR) and equivalent series inductance (ESL). It is useful to make a few assumptions and examine the approximate response of the capacitor to a fast current step input. For the sake of the discussion, assume the input current switches from 0 A to 1 A in 100 ns. Also, assume that the ESR is 0.2 Ω and that the ESL is 20 nH. ESR and ESL vary widely between manufacturers and are also dependent upon body style (through-hole versus surface mount), but these values will serve to illustrate the point.

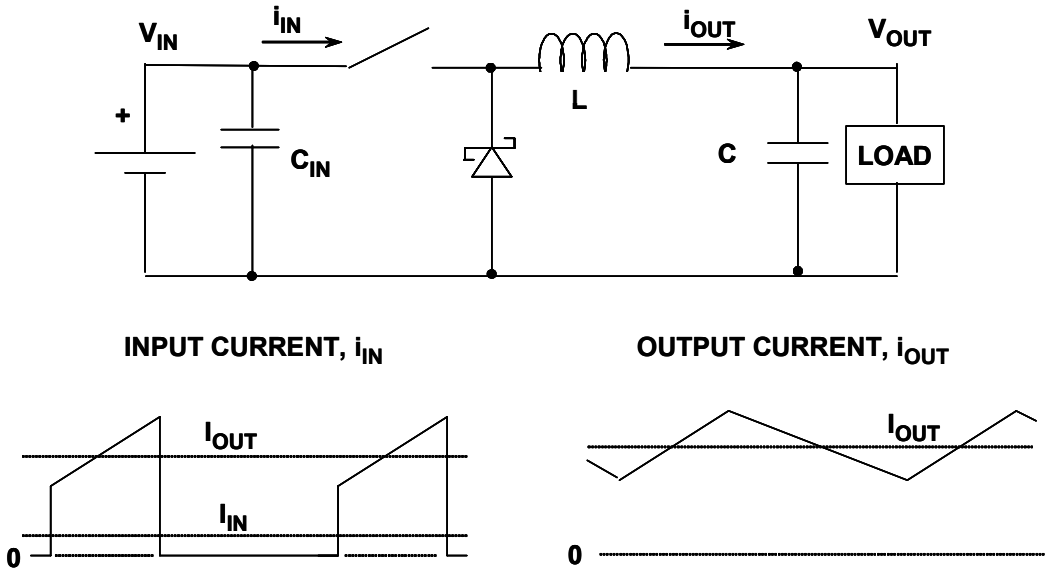


Figure 9.54: *Buck Converter Input and Output Current Waveforms*

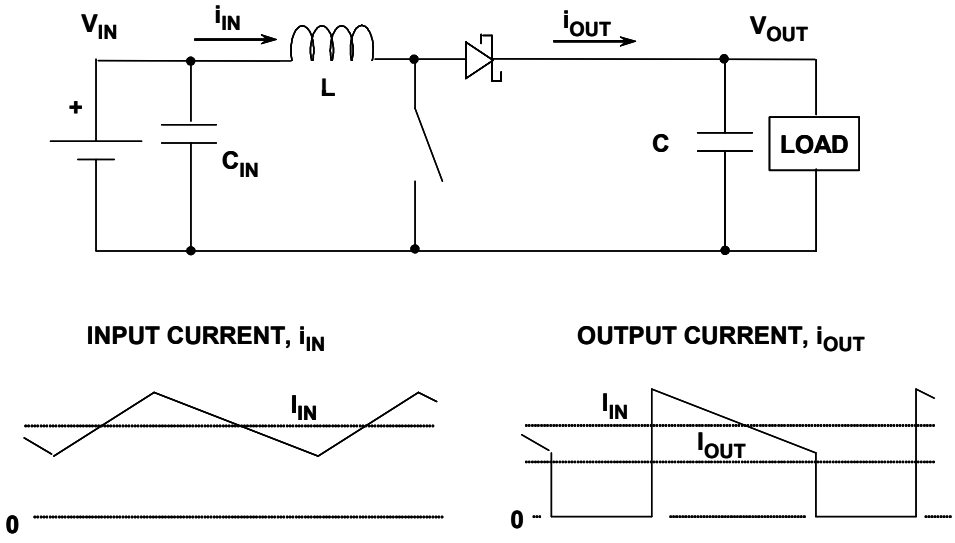


Figure 9.55: *Boost Converter Input and Output Current Waveforms*

Assume that the actual value of the capacitor is large enough so that its reactance is essentially a short circuit with respect to the step function input. For example, 100 μF at 3.5 MHz (the equivalent frequency of a 100 ns risetime pulse) has a reactance of $1/2\pi fC = 0.0005\ \Omega$. In this case, the output voltage ripple is determined exclusively by the ESR and ESL of the capacitor, not the actual capacitor value itself.

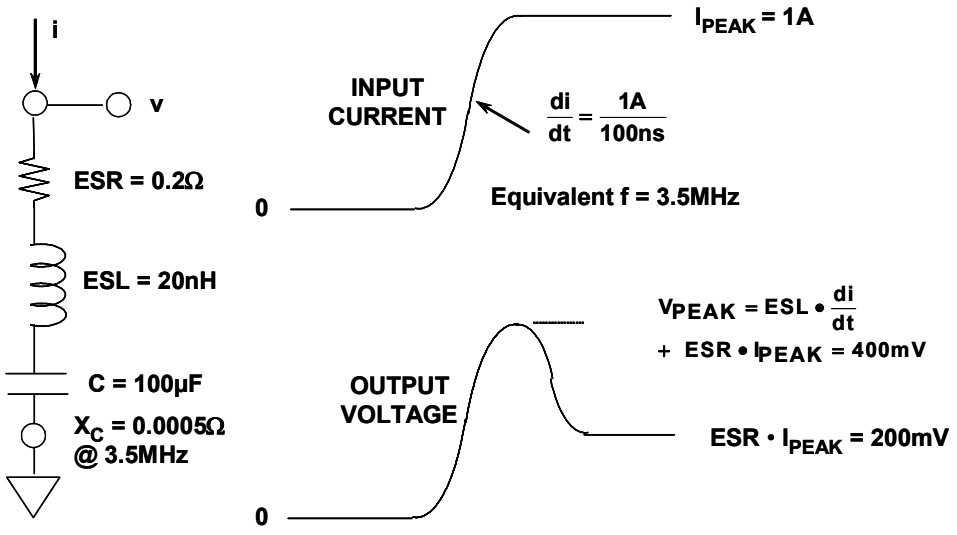


Figure 9.56: *Response of a Capacitor to a Current Step*

These waveforms show the inherent limitations of electrolytic capacitors used to absorb high frequency switching pulses. In a practical system, the high frequency components must be attenuated by low inductance ceramic capacitors with low ESL or by the addition of an LC filter.

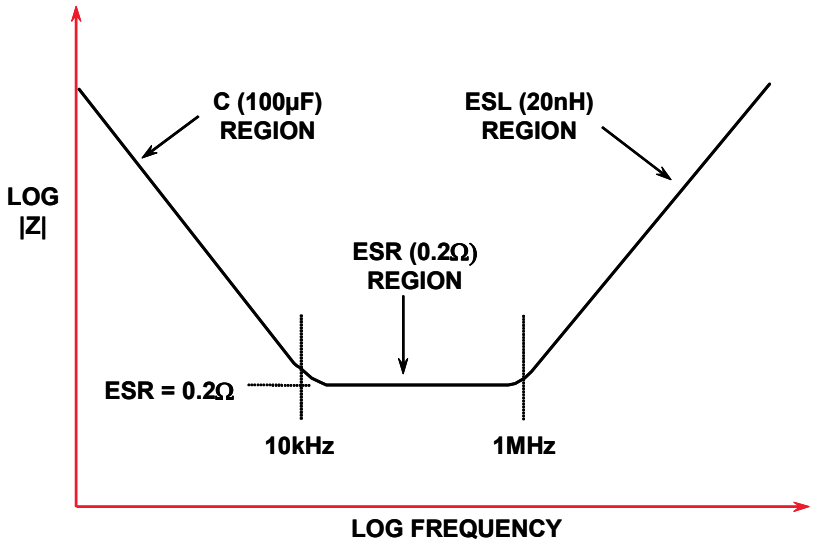


Figure 9.57: *Typical Electrolytic Capacitor Impedance vs. Frequency*

Figure 9.57 shows the impedance versus frequency for a typical 100 µF electrolytic capacitor having an ESR of 0.2 Ω and an ESL of 20 nH. At frequencies below about 10 kHz, the capacitor is nearly ideal. Between 10 kHz and 1 MHz (the range of switching frequencies for most IC switching regulators!) the impedance is limited by the ESR to 0.2 Ω. Above about 1 MHz the capacitor behaves like an inductor due to the ESL of

20 nH. These values, although they may vary somewhat depending upon the actual type of electrolytic capacitor (aluminum general purpose, aluminum switching type, tantalum, or organic semiconductor), are representative and illustrate the importance of understanding the limitations of capacitors in switching regulators.

From the electrolytic capacitor impedance characteristic, it is clear that the ESR and ESL of the output capacitor will determine the peak-to-peak output voltage ripple caused by the switching regulator output ripple current.

In most electrolytic capacitors, ESR degrades noticeably at low temperature, by as much as a factor of 4 to 6 times at –55°C versus the room temperature value. For circuits where ESR is critical to performance, this can lead to problems. Some specific electrolytic types do address this problem, for example within the HFQ switching types, the –10°C ESR at 100 kHz is no more than 2× that at room temperature. The OS-CON electrolytics have a ESR versus temperature characteristic which is relatively flat.

There are generally three classes of capacitors useful in 10 kHz to 100 MHz frequency range, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These can, in turn, be further subdivided. A thumbnail sketch of capacitor characteristics is shown in the chart of Figure 9.58.

	Aluminum Electrolytic (General Purpose)	Aluminum Electrolytic (Switching Type)	Tantalum Electrolytic	OS-CON Electrolytic	Polyester (Stacked Film)	Ceramic (Multilayer)
Size	100 µF	120 µF	120 µF	100 µF	1 µF	0.1 µF
Rated Voltage	25 V	25 V	20 V	20 V	400 V	50 V
ESR	0.6 Ω @ 100 kHz	0.18 Ω @ 100 kHz	0.12 Ω @ 100 kHz	0.02 Ω @ 100 kHz	0.11 Ω @ 1 MHz	0.12 Ω @ 1 MHz
Operating Frequency (*)	≅ 100 kHz	≅ 500 kHz	≅ 1 MHz	≅ 1 MHz	≅ 10 MHz	≅ 1 GHz

(*) Upper frequency strongly size and package dependent

Figure 9.58: Capacitor Selection Guide

The *electrolytic* family provides an excellent, cost effective low frequency component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general-purpose aluminum electrolytic* types, available in working voltages from below 10 V up to about 500 V, and in size from 1 to several thousand µF (with proportional case sizes). All electrolytic capacitors are polarized, and thus cannot withstand more than a volt or so of reverse bias without

damage. They also have relatively high leakage currents (up to tens of μA, and strongly dependent upon design specifics).

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100 V or less, with capacitance of 500 μF or less [Reference 8]. In a given size, tantalums exhibit a higher capacitance-to-volume ratio than do general-purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses [Reference 9]. This capacitor type competes directly with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte [Reference 10]. The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of low low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and different dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10 μF/50 V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50 V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10 mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

Typically using a wound layer-type construction, film capacitors can be inductive, which can limit their effectiveness for high frequency filtering. Obviously, only noninductively made film caps are useful for switching regulator filters. One specific style which is noninductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads [see References 9, 10, 11]. Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL [Reference 12].

Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to well above 10 MHz. At the highest frequencies, only stacked film types should be considered. Some manufacturers are now supplying film types in leadless surface mount packages, which eliminates the lead length inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200 V [see ceramic families of Reference 8]. NP0 (also called COG) types use a lower dielectric constant formulation, and have nominally zero TC, plus a low voltage coefficient (unlike the less stable high-K types). NP0 types are limited to values of 0.1 μF or less, with 0.01 μF representing a more practical upper limit.

Multilayer ceramic "chip caps" are very popular for bypassing/filtering at 10 MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1 GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

The *ripple-current* rating of electrolytic capacitors must not be ignored in switching regulator applications because, unlike linear regulators, switching regulators subject capacitors to large ac currents. AC currents can cause heating in the dielectric material and change the temperature-dependent characteristics of the capacitor. Also, the capacitor is more likely to fail at the higher temperatures produced by the ripple current. Fortunately, most manufacturers provide ripple-current ratings, and this problem can be averted if understood.

Calculating the exact ripple current can be tedious, especially with complex switching regulator waveforms. Simple approximations can be made, however, which are sufficiently accurate. Consider first the buck converter input and output currents (refer to Figure 9.61). The rms input capacitor ripple current can be approximated by a square wave having a peak-to-peak amplitude equal to I_{OUT}. The rms value of this square wave is therefore $I_{OUT}/2$. The output capacitor current waveform can be approximated by a sawtooth waveform having a peak-to-peak amplitude of $0.2*I_{OUT}$. The rms value of this sawtooth is therefore approximately $0.2*I_{OUT}/\sqrt{12}$, or $0.06*I_{OUT}$.

Similarly for a boost converter (see waveforms shown in Figure 9.62), the input capacitor rms ripple current is $0.06*I_{IN}$, and the rms output current ripple is $0.5*I_{IN}$. These boost converter expressions can also be expressed in terms of the output current, I_{OUT}, using the relationship, $I_{IN} = I_{OUT}(V_{OUT}/V_{IN})$. In any case, the minimum expected value of input voltage should be used which will result in the largest value of input current.

In practice, a safety factor of 25% should be added to the above approximations for further derating. In practical applications, especially those using surface mount components, it may be impossible to meet the capacitance value, ESR, and ripple current requirement using a single capacitor. Paralleling a number of equal value capacitors is a viable option which will increase the effective capacitance and reduce ESR, ESL. In addition, the ripple current is divided between the individual capacitors.

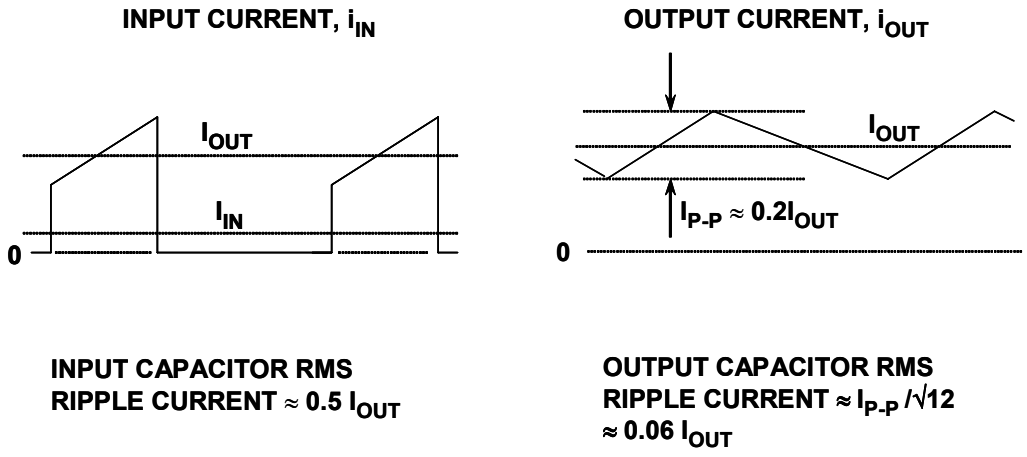


Figure 9.59: *Buck Converter Input and Output Capacitors RMS Ripple Current Approximations*

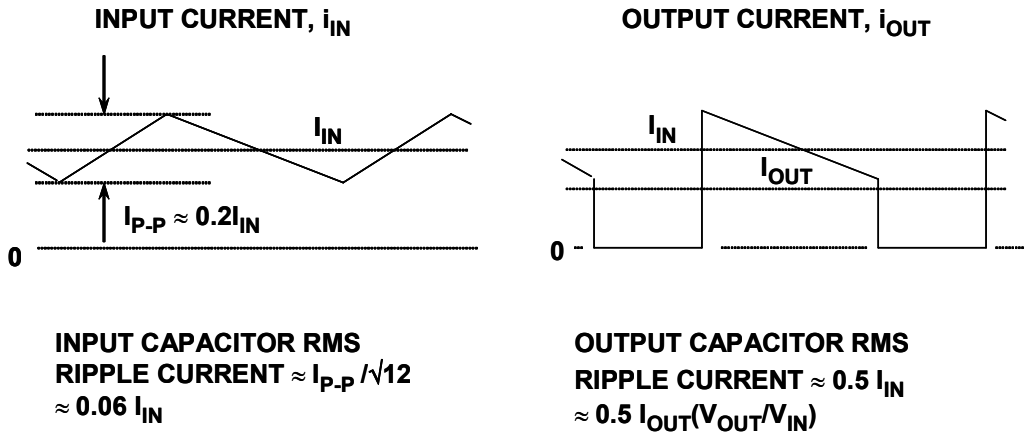


Figure 9.60: *Boost Converter Input and Output Capacitor RMS Ripple Current Approximations*

Several electrolytic capacitor manufacturers offer low ESR surface-mount devices including the AVX TPS-series [Reference 14], and the Sprague 595D-series [Reference 15]. Low ESR through-hole electrolytic capacitors are the HFQ-series from Panasonic [Reference 16] and the OS-CON-series from Sanyo [Reference 17].

Switching Regulator Output Filtering

In order to minimize switching regulator output voltage ripple it is often necessary to add additional filtering. In many cases, this is more efficient than simply adding parallel capacitors to the main output capacitor to reduce ESR.

Output ripple current in a boost converter is pulsating, while that of a buck converter is a sawtooth. In any event, the high frequency components in the output ripple current can be removed with a small inductor (2 μH to 10 μH or so followed by a low ESR capacitor). Figure 9.61 shows a simple LC filter on the output of a switching regulator whose switching frequency is f. Generally the actual value of the filter capacitor is not as important as its ESR when filtering the switching frequency ripple. For instance, the reactance of a 100 μF capacitor at 100 kHz is approximately 0.016 Ω, which is much less than available ESRs.

The capacitor ESR and the inductor reactance attenuate the ripple voltage by a factor of approximately $2\pi fL/ESR$. The example shown in Figure 9.61 uses a 10 μH inductor and a capacitor with an ESR of 0.2 Ω. This combination attenuates the output ripple by a factor of about 32.

The inductor core material is not critical, but it should be rated to handle the load current. Also, its dc resistance should be low enough so that the load current does not cause a significant voltage drop across it.

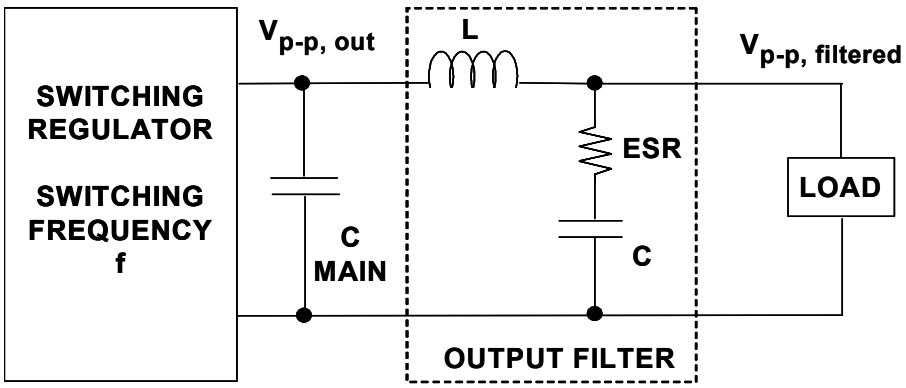
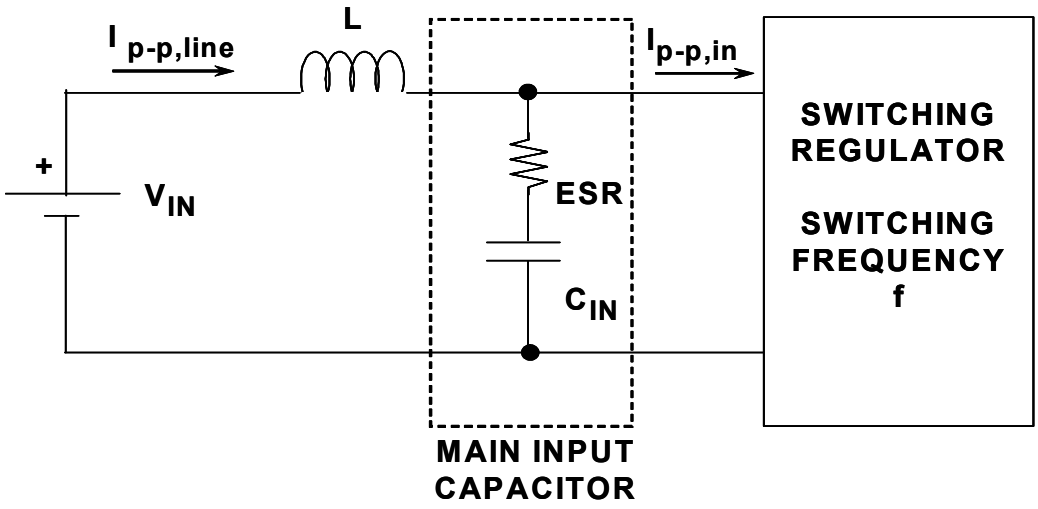


Figure 9.61: *Switching Regulator Output Filtering*

Switching Regulator Input Filtering

The input ripple current in a buck converter is pulsating, while that of a boost converter is a sawtooth. Additional filtering may be required to prevent the switching frequency and the other higher frequency components from affecting the main supply ripple current.

This is easily accomplished by the addition of a small inductor in series with the main input capacitor of the regulator as shown in Figure 9.62. The reactance of the inductor at the switching frequency forms a divider with the ESR of the input capacitor. The inductor will block both low and high frequency components from the main input voltage source. The attenuation of the ripple current at the switching frequency, f, is approximately $2\pi fL/ESR$.



$$\text{ATTENUATION} \approx \frac{2\pi fL}{ESR}$$

Figure 9.62: *Switching Regulator Input Filtering*

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14. AVX Corporation, 801 17th Ave. S., Myrtle Beach, SC 29577, 803-448-9411.

15. Sprague, 70 Pembroke Road, Concord, NH 03301, 603-224-1961.

16. Panasonic, 2 Panasonic Way, Secaucus, NJ 07094, 201-392-7000.

17. Sanyo Corporation, 2001 Sanyo Ave., San Diego, CA 92173, 619-661-6835

18. Kemet Electronics, Box 5828, Greenville, SC 29606, 803-963-6300

Inductor Manufacturers:

19. Coiltronics, 6000 Park of Commerce Blvd., Boca Raton, FL 33487, 407-241-7876.

20. Sumida, 5999 New Wilke Rd. Suite 110, Rolling Meadow, IL. 60008, 847-956-0666.

21. Pulse Engineering, 12220 World Trade Drive, San Diego, CA 92128, 619-674-8100.

22. Gowanda Electronics, 1 Industrial Place, Gowanda, NY 14070, 716-532-2234.

23. Coilcraft, 1102 Silver Lake Rd., Cary, IL 60013, 847-639-2361.

24. Dale Electronics, Inc., E. Highway 50, P.O. Box 180, Yankton, SD 57078, 605-665-9301.

25. Hurricane Electronics Lab, 331 N. 2260 West, P.O. Box 1280, Hurricane, UT 84737, 801-635-2003.

Core Manufacturers:

26. Magnetics, P.O. Box 391, Butler, PA 16003, 412-282-8282.

MOSFET Manufacturers:

27. International Rectifier, 233 Kansas Street, El Segundo, CA 90245, 310-322-3331.

28. Motorola Semiconductor, 3102 North 56th Street, MS56-126, Phoenix, AZ 85018, 800-521-6274.

29. Siliconix Inc., 2201 Laurelwood Road, P.O. Box 54951, Santa Clara, CA 95056, 408-988-8000.

Schottky Diode Manufacturers:

30. General Instrument, Power Semiconductor Division, 10 Melville Park Road, Melville, NY 11747, 516-847-3000.

31. International Rectifier, 233 Kansas Street, El Segundo, CA 90245, 310-322-3331.

32. Motorola Semiconductor, 3102 North 56th Street, MS56-126, Phoenix, AZ 85018, 800-521-6274.

Notes:

SECTION 9.3: SWITCHED CAPACITOR VOLTAGE CONVERTERS

Introduction

In the previous section, we saw how inductors can be used to transfer energy and perform voltage conversions. This section examines switched capacitor voltage converters which accomplish energy transfer and voltage conversion using capacitors.

The two most common switched capacitor voltage converters are the *voltage inverter* and the *voltage doubler* circuit shown in Figure 9.63. In the voltage inverter, the charge pump capacitor, C1, is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle, its voltage is inverted and applied to capacitor C2 and the load. The output voltage is the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle—defined as the ratio of charging time for C1 to the entire switching cycle time—is usually 50%, because that generally yields the optimal charge transfer efficiency.

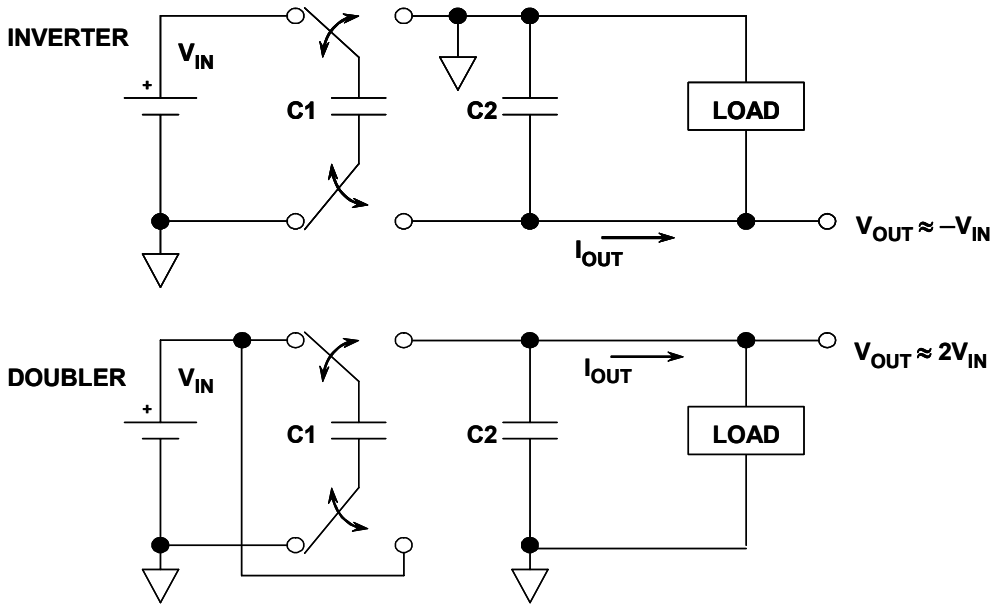


Figure 9.63: *Basic Switched Capacitor Voltage Inverter and Doubler*

After initial start-up transient conditions and when a steady-state condition is reached, the charge pump capacitor only has to supply a small amount of charge to the output capacitor on each switching cycle. The amount of charge transferred depends upon the load current and the switching frequency. During the time the pump capacitor is charged by the input voltage, the output capacitor C2 must supply the load current. The load current flowing out of C2 causes a droop in the output voltage which corresponds to a

component of output voltage ripple. Higher switching frequencies allow smaller capacitors for the same amount of droop. There are, however, practical limitations on the switching speeds and switching losses, and switching frequencies are generally limited to a few hundred kHz.

The voltage doubler works similarly to the inverter; however, the pump capacitor is placed in series with the input voltage during its discharge cycle, thereby accomplishing the voltage doubling function. In the voltage doubler, the average input current is approximately twice the average output current.

The basic inverter and doubler circuits provide no output voltage regulation, however, techniques exist to add regulated capability and have been implemented in the ADP3603/ADP3604/ADP3605/ADP3607.

There are certain advantages and disadvantages of using switched capacitor techniques rather than inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, these converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there is no need for an inductor, the final PCB component height can generally be made smaller than a comparable switching regulator. This is important in many applications such as display panels.

Switched capacitor inverters are low cost and compact and are capable of achieving efficiencies greater than 90%. Obviously, the current output is limited by the size of the capacitors and the current carrying capacity of the switches. Typical IC switched capacitor inverters have maximum output currents of about 150 mA maximum.

- **No Inductors!**
- **Minimal Radiated EMI**
- **Simple Implementation: Only 2 External Capacitors (Plus an Input Capacitor if Required)**
- **Efficiency > 90% Achievable**
- **Optimized for Doubling or Inverting Supply Voltage - Efficiency Degrades for Other Output Voltages**
- **Low Cost, Compact, Low Profile (Height)**

- **Parts with Voltage Regulation are Available:**

  ADP3603/ADP3604/ADP3605/ADP3607

Figure 9.64: *Advantages of Switched Capacitor Voltage Converters*

Switched capacitor voltage converters do not maintain high efficiency for a wide range of ratios of input to output voltages, unlike their switching regulator counterparts. Because the input to output current ratio is scaled according to the basic voltage conversion (i.e., doubled for a doubler, inverted for an inverter) regardless of whether or not regulation is

used to reduce the doubled or inverted voltage, any output voltage magnitude less than $2*V_{IN}$ for a doubler or less than $|V_{IN}|$ for an inverter will result in additional power dissipation within the converter, and efficiency will be degraded proportionally.

The voltage inverter is useful where a relatively low current negative voltage is required in addition to the primary positive voltage. This may occur in a single supply system where only a few high performance parts require the negative voltage. Similarly, voltage doublers are useful in low current applications where a voltage greater than the primary supply voltage is required.

Charge Transfer Using Capacitors

A fundamental understanding of capacitors (theoretical and real) is required in order to master the subtleties of switched capacitor voltage converters. Figure 9.65 shows the theoretical capacitor and its real-world counterpart. If the capacitor is charged to a voltage V, then the total charge stored in the capacitor, q, is given by q = CV. Real capacitors have equivalent series resistance (ESR) and inductance (ESL) as shown in the diagram, but these parasitics do not affect the ability of the capacitor to store charge. They can, however, have a large effect on the overall efficiency of the switched capacitor voltage converter.

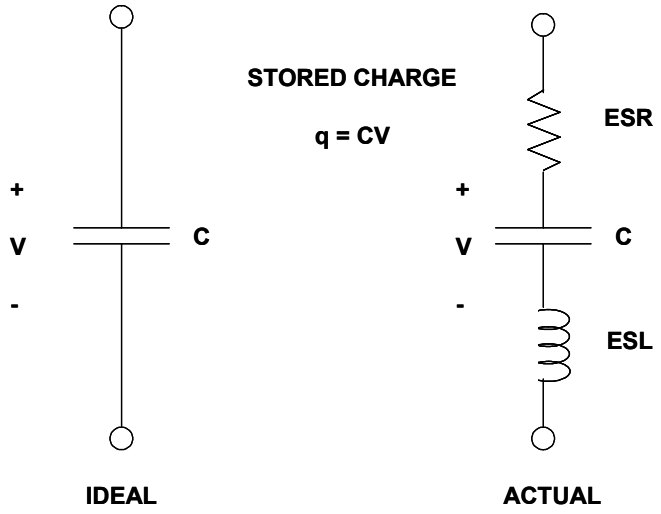


Figure 9.65: *Stored Charge in a Capacitor*

If an ideal capacitor is charged with an ideal voltage source as shown in Figure 9.66(A), the capacitor charge buildup occurs instantaneously, corresponding to a unit impulse of current. A practical circuit (Figure 9.66(B)) will have resistance in the switch (R_{SW}) as well as the equivalent series resistance (ESR) of the capacitor. In addition, the capacitor has an equivalent series inductance (ESL). The charging current path also has an effective series inductance which can be minimized with proper component layout techniques.

These parasitics serve to limit the peak current, and also increase the charge transfer time as shown in the diagram. Typical switch resistances can range from 1 Ω to 50 Ω, and ESRs between 50 mΩ and 200 mΩ. Typical capacitor values may range from about 0.1 µF to 10 µF, and typical ESL values 1 nH to 5 nH. Although the equivalent RLC circuit of the capacitor can be underdamped or overdamped, the relatively large switch resistance generally makes the final output voltage response overdamped.

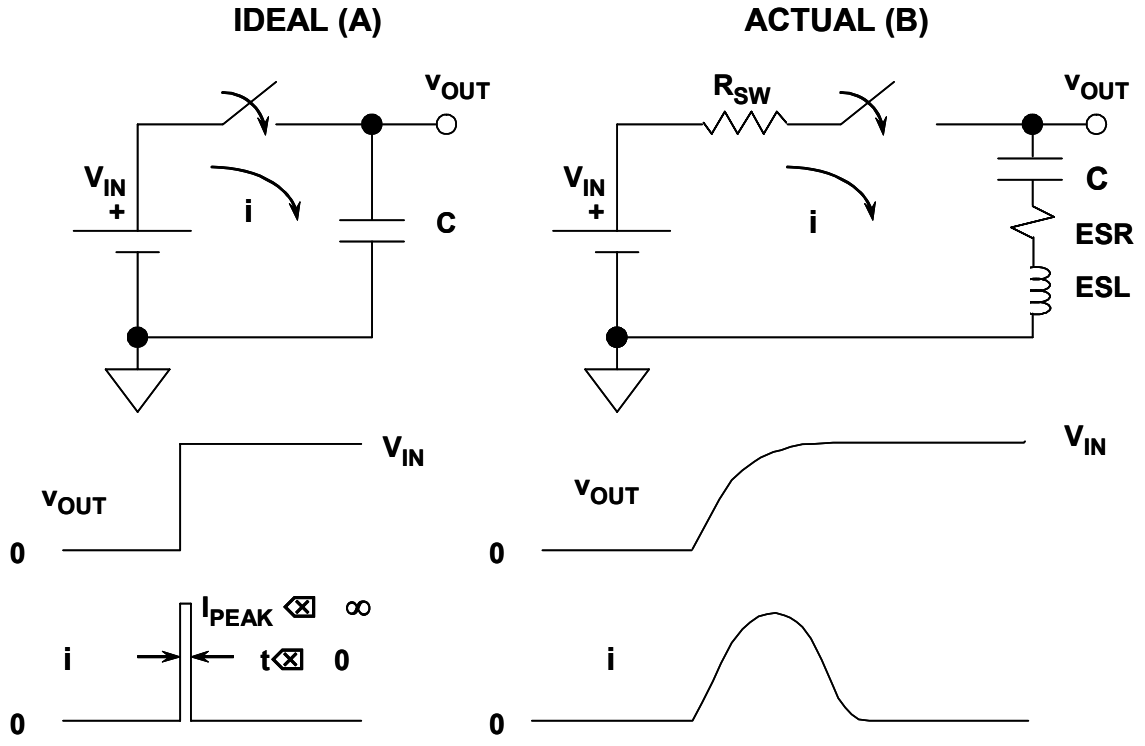


Figure 9.66: *Charging a Capacitor from a Voltage Source*

The law of conservation of charge states that if two capacitors are connected together, the total charge on the parallel combination is equal to the sum of the original charges on the capacitors. Figure 9.69 shows two capacitors, C1 and C2, each charged to voltages V1 and V2, respectively. When the switch is closed, an impulse of current flows, and the charge is redistributed. The total charge on the parallel combination of the two capacitors is $q_T = C1 \cdot V1 + C2 \cdot V2$. This charge is distributed between the two capacitors, so the new voltage, V_T, across the parallel combination is equal to qT/(C1 + C2), or

$$V_T = \frac{q_T}{C1 + C2} = \frac{C1 \cdot V1 + C2 \cdot V2}{C1 + C2} = \left(\frac{C1}{C1 + C2}\right) V1 + \left(\frac{C2}{C1 + C2}\right) V2 \,. \quad \text{Eq. 9-73}$$

This principle may be used in the simple charge pump circuit shown in Figure 9.68. Note that this circuit is neither a doubler nor inverter, but only a voltage replicator. The pump

capacitor is C1, and the initial charge on C2 is zero. The pump capacitor is initially charged to V_{IN}. When it is connected to C2, the charge is redistributed, and the output voltage is $V_{IN}/2$ (assuming C1 = C2). On the second transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4$. On the third transfer cycle, the output voltage is pumped to $V_{IN}/2 + V_{IN}/4 + V_{IN}/8$. The waveform shows how the output voltage exponentially approaches V_{IN}.

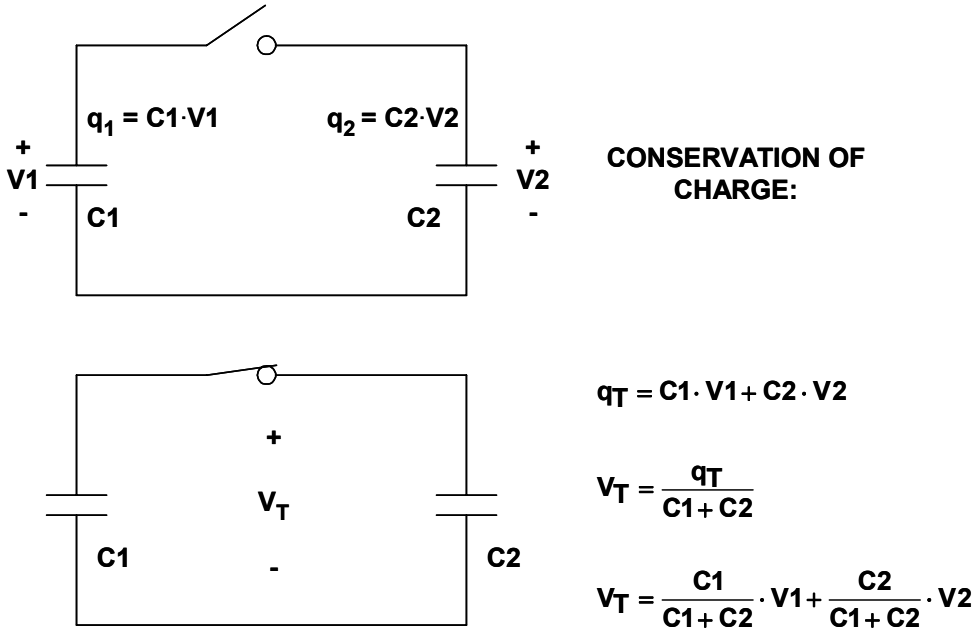


Figure 9.67: *Charge Redistribution Between Capacitors*

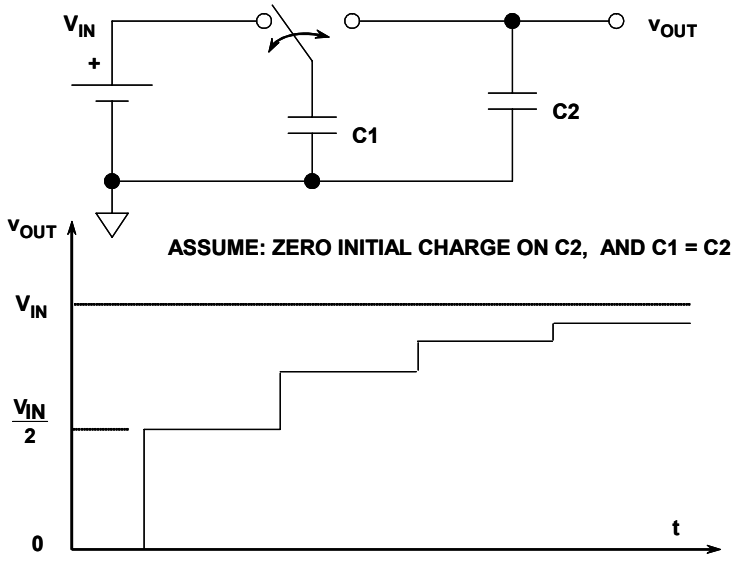


Figure 9.68: *Continuous Switching*

Figure 9.69 shows a pump capacitor, C1, switched continuously between the source, V1, and C2 in parallel with the load. The conditions shown are after a steady state condition has been reached. The charge transferred each cycle is $\Delta q = C1(V1 - V2)$. This charge is transferred at the switching frequency, f. This corresponds to an average current (current = charge transferred per unit time) of

$$I = f\,\Delta q = f \cdot C1(V1 - V2), \qquad \text{Eq. 9-74}$$

or

$$I = \frac{V1 - V2}{1/f \cdot C1}\ . \qquad \text{Eq. 9-75}$$

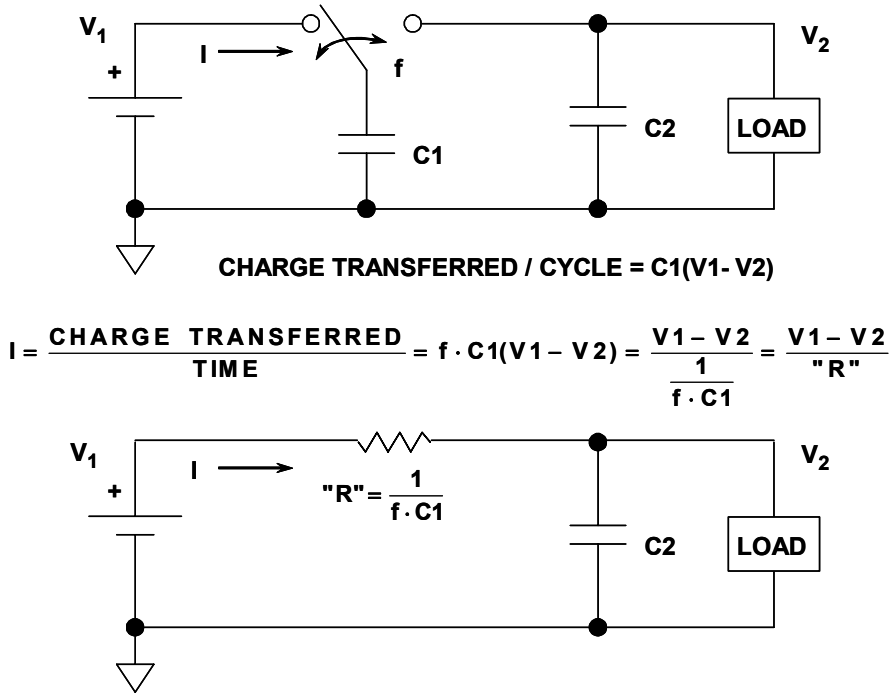


Figure 9.69: *Continuous Switching, Steady State*

Notice that the quantity, $1/f \cdot C1$, can be considered an equivalent resistance, "R," connected between the source and the load. The power dissipation associated with this virtual resistance, "R," is essentially forced to be dissipated in the switch on resistance and the capacitor ESR, regardless of how low those values are reduced. (It should be noted that capacitor ESR and the switch on-resistance cause additional power losses as will be discussed shortly.)

In a typical switched capacitor voltage inverter, a capacitance of 10 µF switched at 100 kHz corresponds to "R" = 1 Ω. Obviously, minimizing "R" by increasing the frequency minimizes power loss in the circuit. However, increasing switching frequency

tends to increase switching losses. The optimum switched capacitor operating frequency is therefore highly process and device dependent. Therefore, specific recommendations are given in the data sheet for each device.

Unregulated Switched Capacitor Inverter and Doubler Implementations

An unregulated switched capacitor inverter implementation is shown in Figure 9.70. Notice that the SPDT switches (shown in previous diagrams) actually comprise two SPST switches. The control circuit consists of an oscillator and the switch drive signal generators. Most IC switched capacitor inverters and doublers contain all the control circuits as well as the switches and the oscillator. The pump capacitor, C1, and the load capacitor, C2, are external. Not shown in the diagram is a capacitor on the input which is generally required to ensure low source impedance at the frequencies contained in the switching transients.

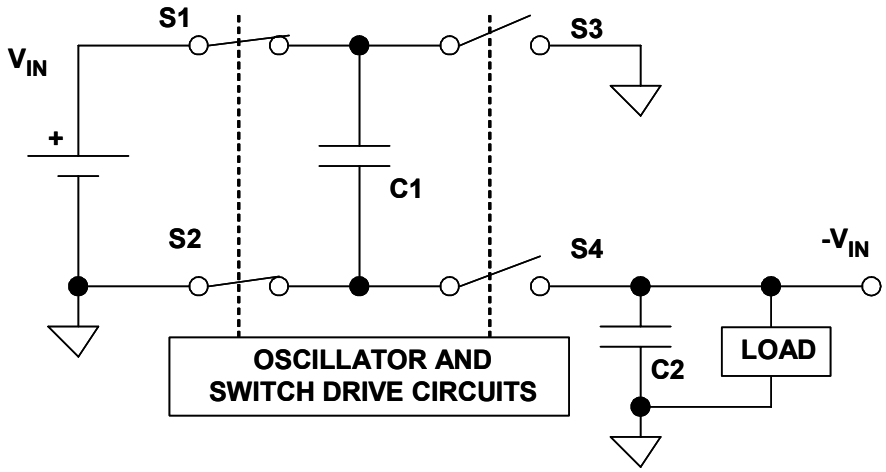


Figure 9.70: *Switched Capacitor Voltage Inverter*

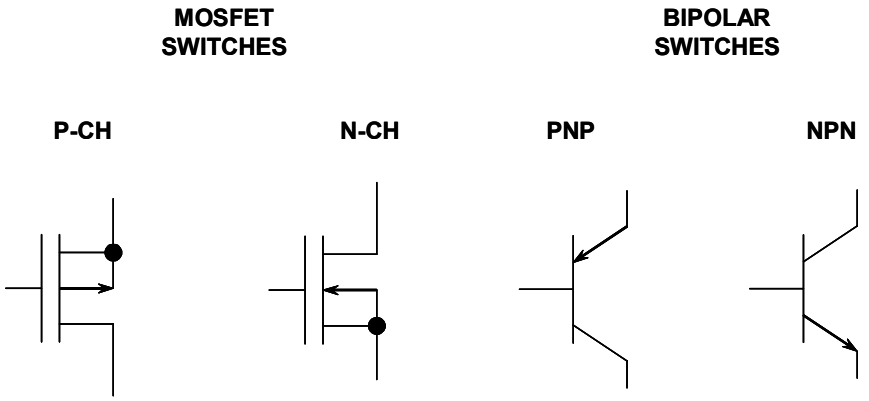


Figure 9.71: *Switches Used in Voltage Converters*

The switches used in IC switched capacitor voltage converters may be CMOS or bipolar as shown in Figure 9.71. Standard CMOS processes allow low on resistance MOSFET switches to be fabricated along with the oscillator and other necessary control circuits. Bipolar processes can also be used, but add cost and increase power dissipation.

Voltage Inverter and Doubler Dynamic Operation

The steady-state current and voltage waveforms for a switched capacitor voltage inverter are shown in Figure 9.72. The average value of the input current waveform (A) must be equal to I_{OUT}. When the pump capacitor is connected to the input, a charging current flows. The initial value of this charging current depends on the initial voltage across C1, the ESR of C1, and the resistance of the switches. The switching frequency, switch resistance, and the capacitor ESRs generally limit the peak amplitude of the charging current to less than $2.5*I_{OUT}$. The charging current then decays exponentially as C1 is charged. The waveforms in Figure 9.72 assume that the time constant due to capacitor C1, the switch resistance, and the ESR of C1 is several times greater than the switching period (1/f). Smaller time constants will cause the peak currents to increase as well as increase the slopes of the charge/discharge waveforms. Long time constants cause longer start-up times and require larger and more costly capacitors. For the conditions shown in Figure 9.72 (A), the peak value of the input current is only slightly greater than $2*I_{OUT}$.

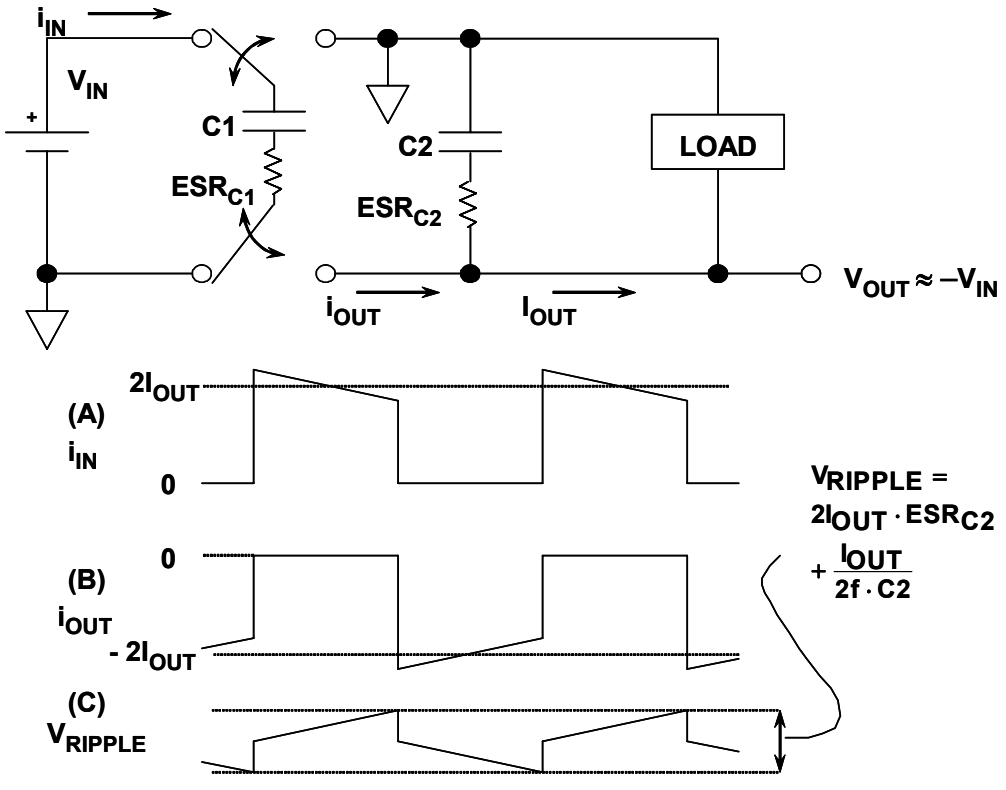


Figure 9.72: *Voltage Inverter Waveforms*

The output current waveform of C1 is shown in Figure 9.72(B). When C1 is connected to the output capacitor, the step change in the output capacitor current is approximately $2*I_{OUT}$. This current step therefore creates an output voltage step equal to $2*I_{OUT} * ESR_{C2}$ as shown in Figure 9.72(C). After the step change, C2 charges linearly by an amount equal to $I_{OUT}/2f \bullet C2$. When C1 is connected back to the input, the ripple waveform reverses direction as shown in the diagram. The total peak-to-peak output ripple voltage is therefore:

$$V_{RIPPLE} \approx 2I_{OUT} \cdot ESR_{C2} + \frac{I_{OUT}}{2f \cdot C2}. \qquad \text{Eq. 9-76}$$

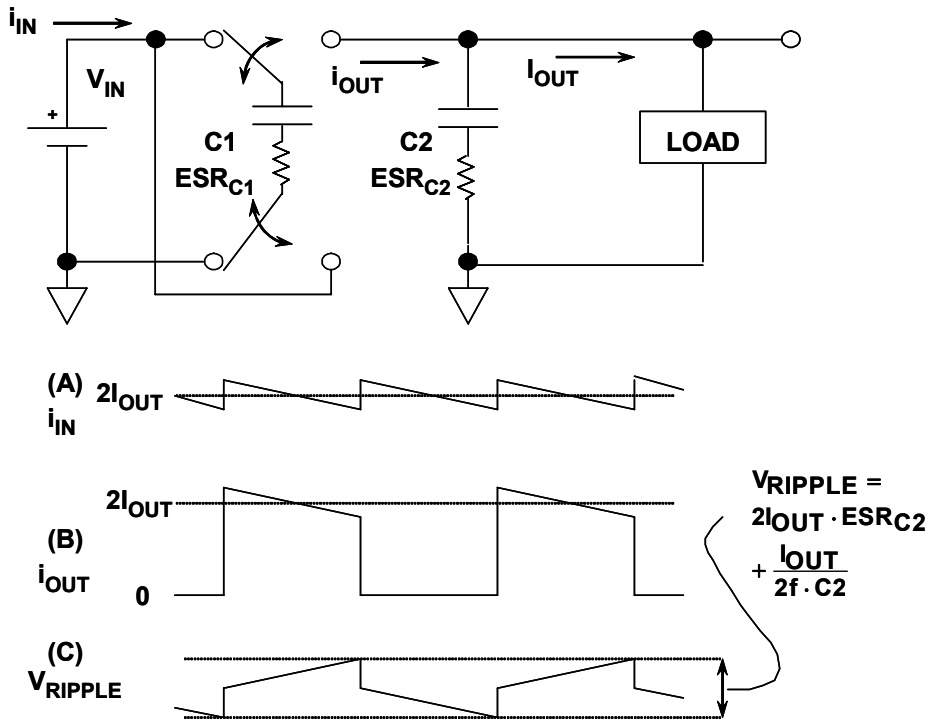


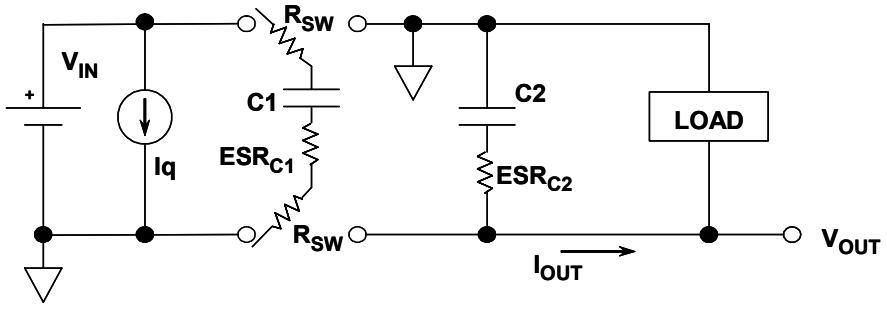
Figure 9.73: *Voltage Doubler Waveforms*

The current and voltage waveforms for a simple voltage doubler are shown in Figure 9.73 and are similar to those of the inverter. Typical voltage ripple for practical switched capacitor voltage inverter/doublers range from 25 mV to 100 mV, but can be reduced by filtering techniques.

Note that the input current waveform has an average value of $2*I_{OUT}$ because V_{IN} is connected to C1 during C1's charge cycle and to the load during C1's discharge cycle. The expression for the ripple voltage is identical to that of the voltage inverter.

Switched Capacitor Voltage Converter Power Losses

The various sources of power loss in a switched capacitor voltage inverter are shown in Figure 9.74. In addition to the inherent switched capacitor resistance, "R" = 1/f*C1, there are resistances associated with each switch, as well as the ESRs of the capacitors. The quiescent power dissipation, I_q*V_{IN}, must also be included, where I_q is the quiescent current drawn by the IC itself.



$$P_{LOSS} = I_{OUT}(V_{IN} - |V_{OUT}|) + I_q V_{IN}$$
$$= I_{OUT}^2 \cdot R_{OUT} + I_q V_{IN}$$

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + \frac{1}{f \cdot C1} + ESR_{C2}$$

Figure 9.74: *Voltage Inverter Power Losses*

The power dissipated in the switching arm is first calculated. When C1 is connected to V_{IN}, a current of $2*I_{OUT}$ flows through the switch resistances ($2R_{SW}$) and the ESR of C1, ESR_{C1}. When C1 is connected to the output, a current of $2*I_{OUT}$ continues to flow through C1, $2R_{SW}$, and ESR_{C1}. Therefore, there is always an rms current of $2*I_{OUT}$ flowing through these resistances, resulting in a power dissipation in the switching arm of:

$$P_{SW} = (2*I_{OUT})^2 \times (2*R_{SW} + ESR_{C1}) = I_{OUT}^2 \times (8R_{SW} + 4\&ESR_{C1}). \quad \text{Eq. 9-77}$$

In addition to these purely resistive losses, an rms current of I_{OUT} flows through the "resistance" of the switched capacitor, C1, yielding an additional loss of:

$$P_{C1} = I_{OUT}^2: \; R_{C1} = I_{OUT2} * \frac{1}{f*C1} \quad \text{Eq. 9-78}$$

The rms current flowing through ESR_{C2} is I_{OUT}, yielding a power dissipation of:

$$P_{ESR_{C2}} = I_{OUT}^2 \times ESR_{C2}. \quad \text{Eq. 9-79}$$

Adding all the resistive power dissipations to the quiescent power dissipation yields:

$$P_{LOSS} = I_{OUT}^2 \times \left(8R_{SW} + 4ESR_{C1} + ESR_{C2} + \frac{1}{f \cdot C1}\right) + I_q V_{IN} . \quad \text{Eq. 9-80}$$

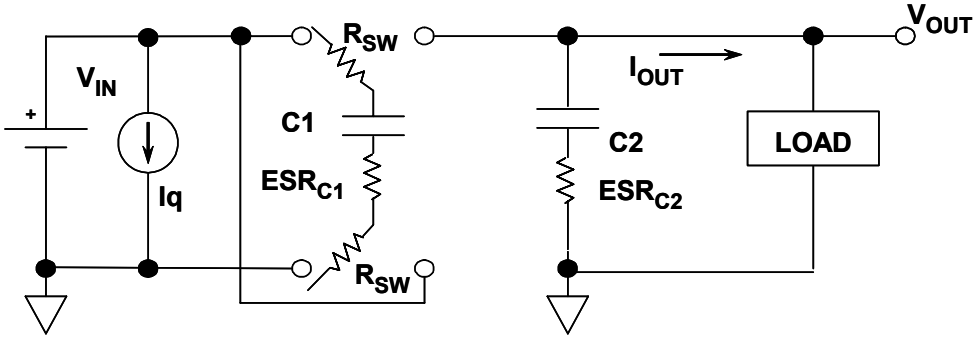
All of the resistive losses can be grouped into an equivalent R_{OUT} as shown in the diagram.

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + 1/f{\cdot}C1 + ESR_{C2}. \quad \text{Eq, 9-81}$$

Typical values for switch resistances are between 1 Ω and 20 Ω, and ESRs between 50 mΩ and 200 mΩ. The values of C1 and f are generally chosen such that the term, 1/f·C1, is less than 1 Ω. For instance, 10 µF @ 100 kHz yields "R" = 1 Ω. The dominant sources of power loss in most inverters are therefore the switch resistances and the ESRs of the pump capacitor and output capacitor.

The ADP3603/ADP3604/ADP3605/ADP3607 series regulators have a shutdown control pin which can be asserted when load current is not required. When activated, the shutdown feature reduces quiescent current to a few tens of microamperes.

Power losses in a voltage doubler circuit are shown in Figure 9.75, and the analysis is similar to that of the inverter.



$$P_{LOSS} = I_{OUT}(2V_{IN} - V_{OUT}) + I_q V_{IN}$$
$$= I_{OUT}^2 \cdot R_{OUT} + I_q V_{IN}$$

$$R_{OUT} \approx 8R_{SW} + 4ESR_{C1} + \frac{1}{f \cdot C1} + ESR_{C2}$$

Figure 9.75: *Voltage Doubler Power Losses*

Regulated Output Switched Capacitor Voltage Converters

Adding regulation to the simple switched capacitor voltage converter greatly enhances its usefulness in many applications. There are three general techniques for adding regulation to a switched capacitor converter. The most straightforward is to follow the switched capacitor inverter/doubler with a low dropout (LDO) linear regulator. The LDO provides the regulated output and also reduces the ripple of the switched capacitor converter. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO.

Another approach to regulation is to vary the duty cycle of the switch control signal with the output of an error amplifier which compares the output voltage with a reference. This technique is similar to that used in inductor-based switching regulators and requires the addition of a PWM and appropriate control circuitry. However, this approach is highly nonlinear and requires long time constants (i.e., lossy components) in order to maintain good regulation control.

By far the simplest and most effective method for achieving regulation in a switched capacitor voltage converter is to use an error amplifier to control the on resistance of one of the switches as shown in Figure 9.76, a block diagram of the ADP3603/ADP3604/ADP3605 voltage inverters. These devices offer a regulated –3 V output for an input voltage of +4.5 V to +6 V. The output is sensed and fed back into the device via the V_{SENSE} pin. Output regulation is accomplished by varying the on resistance of one of the MOSFET switches as shown by control signal labeled "R_{ON} CONTROL" in the diagram. This signal accomplishes the switching of the MOSFET as well as controlling the on resistance.

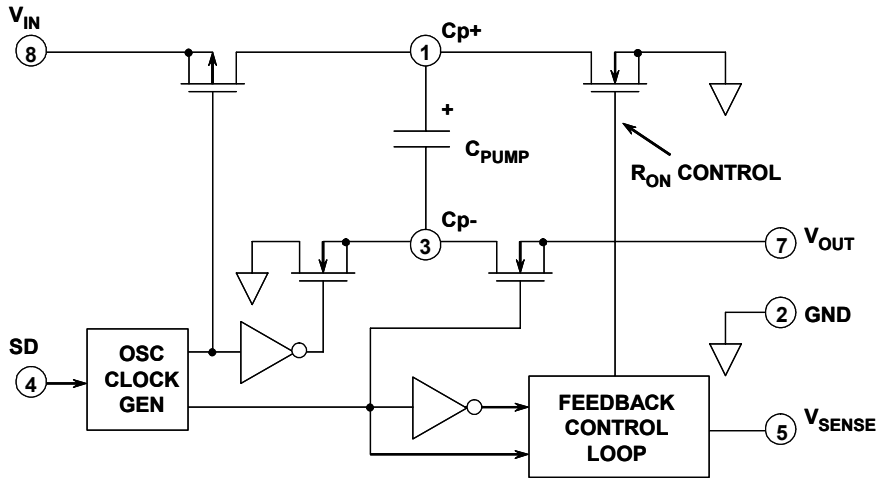


Figure 9.76: *ADP3603/ADP3604/ ADP3605 Regulated −3 V Output Voltage Inverters*

A typical application circuit for the ADP3603/ADP3604/ADP3605 series is shown in Figure 9.77. In the normal mode of operation, the SHUTDOWN pin should be connected to ground. The 10 µF capacitors should have ESRs of less than 150 mΩ, and values of 4.7 µF can be used at the expense of slightly higher output ripple voltage. The equations for ripple voltage shown in Figure 9.72 also apply to the ADP3603/ADP3604/ADP3605. Using the values shown, typical ripple voltage ranges from 25 mV to 60 mV as the output current varies over its allowable range.

The regulated output voltage of the ADP3603/ADP3604/ADP3605 series can varied between –3 V and $-V_{IN}$ by connecting a resistor between the output and the V_{SENSE} pin as shown in the diagram. Regulation will be maintained for output currents up to about 30 mA. The value of the resistor is calculated from the following equation:

$$V_{OUT} = -\left(\frac{R}{5k\Omega} + 3V\right). \qquad \text{Eq. 9-82}$$

The devices can be made to operate as standard inverters providing an unregulated output voltage if the V_{SENSE} pin is simply connected to ground

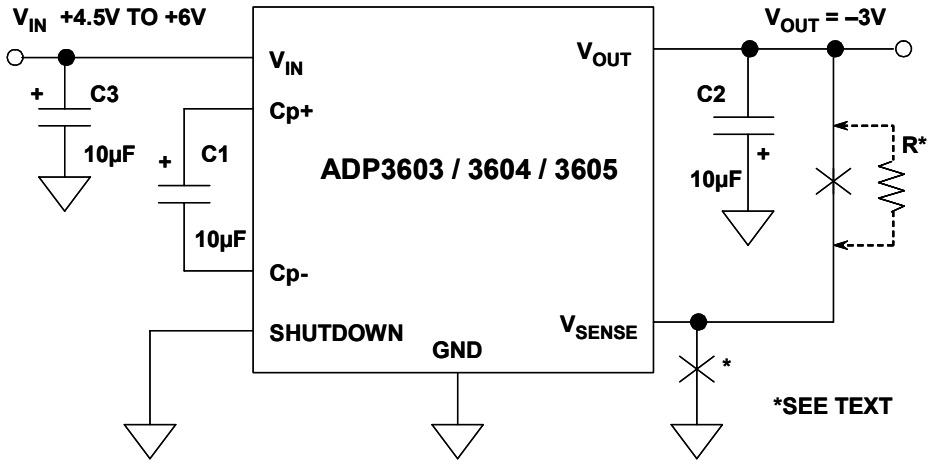


Figure 9.77: *ADP3603/ADP3604/ADP3605 Application Circuit for −3 V Operation*

A typical application circuit is shown in Figure 9.78. The Schottky diode connecting the input to the output is required for proper operation during start-up and shutdown. If V_{SENSE} is connected to ground, the devices operate as unregulated voltage doublers.

The output voltage of each device can be adjusted with an external resistor. The equation which relates output voltage to the resistor value for the ADP3607 is given by:

$$V_{OUT} = \frac{R}{9.5k\Omega} + 1V, \text{ for } V_{OUT} < 2V_{IN}. \qquad \text{Eq. 9-83}$$

The ADP3607 should be operated with an output voltage of at least 3 V in order to maintain regulation.

Although the ADP3607-5 is optimized for an output voltage of 5 V, its output voltage can be adjusted between 5 V and 2*V_{IN} with an external resistor using the equation:

$$V_{OUT} = \frac{2R}{9.5k\Omega} + 5V, \text{ for } V_{OUT} < 2V_{IN}. \qquad \text{Eq. 9-84}$$

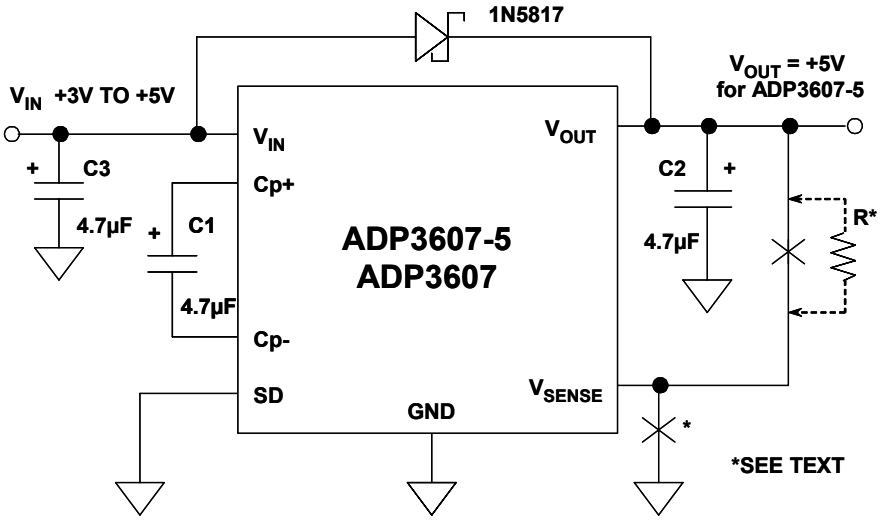


Figure 9.78: *ADP3607 Application Circuit*

When using either the ADP3607 or the ADP3607-5 in the adjustable mode, the output current should be no greater than 30 mA in order to maintain good regulation.

The circuit shown in Figure 9.79 generates a regulated 12 V output from a 5 V input using the ADP3607-5 in a voltage tripler application. Operation is as follows. First assume that the V_{SENSE} pin of the ADP3607-5 is grounded and that the resistor R is not connected. The output of the ADP3607-5 is an unregulated voltage equal to 2*V_{IN}. The voltage at the Cp+ pin of the ADP3607-5 is a square wave with a minimum value of V_{IN} and a maximum value of 2*V_{IN}. When the voltage at Cp+ is V_{IN}, capacitor C2 is charged to V_{IN} (less the D1 diode drop) from V_{OUT1} via diode D1. When the voltage at Cp+ is 2*V_{IN}, the output capacitor C4 is charged to a voltage 3*V_{IN} (less the diode

drops of D1 and D2). The final unregulated output voltage of the circuit, V_{OUT2}, is therefore approximately $3*V_{IN} - 2*V_D$, where V_D is the Schottky diode voltage drop.

The addition of the feedback resistor, R, ensures that the output is regulated for values of V_{OUT2} between $2*V_{IN} - 2*V_D$ and $3*V_{IN} - 2*V_D$. Choosing R = 33.2 kΩ yields an output voltage V_{OUT2} of +12 V for a nominal input voltage of +5 V. Regulation is maintained for output currents up to approximately 20 mA.

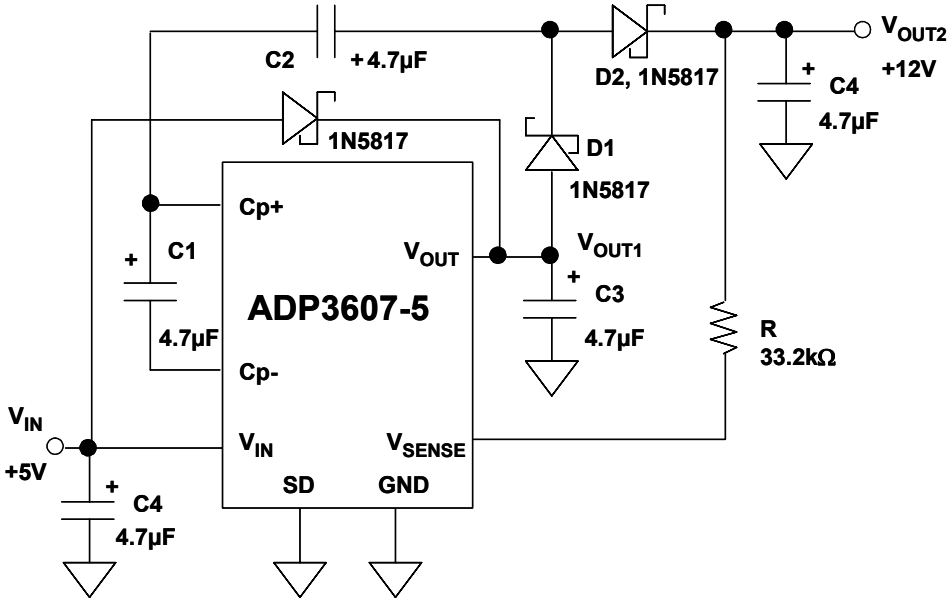


Figure 9.79: *Regulated +12 V from a +5 V Input*