ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

Find the *Wavecrest DTS-2070C* at our website: ***Click HERE***

WAVECREST Corporation

PLL JITTER CHARACTERIZATION AND DEBUGGING

Application Note No. 121

PLL Jitter Characterization and Debugging

Application Note 121

The first six sections of this application note give general knowledge on Phase Lock Loop behavior and how it fits into the overall high-speed digital design environment. The next six sections illustrate how the *WAVECREST* DTS-2070 instrument can be used to properly characterize PLL output jitter and locate the cause(s) of this jitter. When the DTS-2070 instrument is effectively utilized, it is a critical measurement tool for understanding your PLL design (if you are a PLL designer) or for optimizing the use of PLLs in your system (if you are a system designer).

Introduction

The primary purpose of this application note is to provide a solid foundation and background on the need to properly measure, characterize, and analyze the jitter performance of today's Phase Lock Loop (PLL) circuits using *WAVECREST's* precision DTS-2070 Digital Time System. PLL jitter characteristics are best measured since today's simulation tools[1,2] cannot adequately account for all the variables required for modeling PLL jitter behavior. In particular, four unique analysis features of the DTS-2070 are explained in the following document: spectrum, jitter, function and oscilloscope analysis.

Other parameters such as skew, time to lock and symmetrical duty cycle are also important for optimum PLL performance, but are not covered in this application note. PLL used in data communication (clock recovery devices) is also not discussed. Refer to Application Note No. 120, "Jitter Analysis of Clock Recovery Devices at 155.52Mbit/S" to see how the DTS-2070 can be used to analyze data communication circuits. In general, however, many of the issues and measurement techniques discussed in this application note can also be applied to data communication circuits.

The focal point of this work is to establish a baseline for the proper measurement of PLL jitter behavior and noise sensitivity of PLL in a benign environment (no fast transient or other system level induced noise). Proper PLL jitter data analysis may allow the designer to assess timing sensitivities to system level noise. Although jitter causes and jitter measurement issues are broad, this application note is one of several that is devoted to the area of PLL characterization and debugging. Currently, *WAVECREST* is exploring the idea of introducing a variety of external noises into the PLL fixture environment as a subject for a future application note.

General High Speed Trends

Clock distribution is a major topic in high-speed digital systems design on the device level as well as on a system level. For CPUs and CPU-based electronic systems, the clock frequency determines the rate of data processing. Consequently, digital system designers strive to maximize the clock frequency for high system performance. Although other attributes lead to higher system performance, such as multi- and parallel processing and compiler design, clock distribution design continues to be a critical design objective.

Figure 1 shows the clock frequency trend[4] for an Intel-based microprocessor. P5 is the popular Pentium chip which is used in 70% of PCs worldwide. Given the speed trend of microprocessors used in computers, super computers and workstations typically a generation ahead, one can easily expect 1 Giga Hertz computer systems by the year 2000. Therefore, jitter will become an even bigger consideration in a system timing budget.

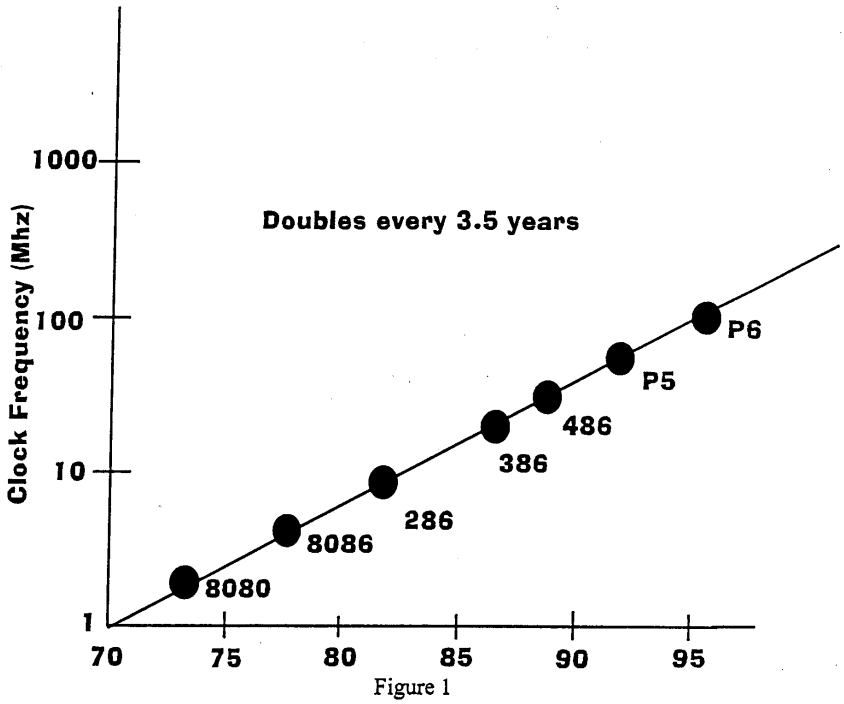


Figure 1

Benefits associated with designing a robust clock distribution network include:

- Shorter design cycle
- Design work the first time
- Performance advantage over the competition
- Satisfied customers (repeat business)
- Beating competitors to market
- Higher revenues from meeting window of opportunity.

If clock distribution designs are not managed properly with the above items taken into consideration, delays in product introduction could occur which could also have a severe impact on revenue.

General Clock Design Issues

In the typical computer system, the clock signals are faster than other signals. Not only are clocks the fastest signals, they tend to be the heaviest loaded. These two factors contribute to severe timing uncertainties. Because of this, clock signals deserve special attention and devices associated with clock distribution (PLL, etc.) should be thoroughly characterized and debugged. There are many excellent references[5,6,7] on the market that provide an in-depth treatment of clock timing, both on a device and system level. The following provides only a general overview. Readers interested in this subject matter should consider one of the references listed at the end of this application note.

The typical timing budget may include several or all of the items listed below.

- Gate delays
- Driver delays
- Set up times
- Hold times
- Clock skew
- Package delays
- Wiring delays
- Rise times
- Settling times
- Jitter

As system speeds continue to escalate, the above factors continue to play a vital role in timing margins. In addition, PLL jitter is also critical because there is a general lack of standards and familiarity with the causes and effects of PLL output jitter. Recently, the JEDEC Committee (JC42)[8] was formulated to address output skew and jitter standardization on off-the-shelf digital devices. Only recently, semiconductor suppliers have begun to define output jitter specifications on device data sheets.

Figure 2 shows the timing tolerance breakdown for a typical 66MHz Pentium system[9] application. The Pentium system specification dictates that the arrival times between the processor and any cache memory, and the cache controller and any cache memory, can never exceed 700ps. Working through the calculations gives the final constraint of 50ps of jitter for timing margins. This is very difficult to achieve.

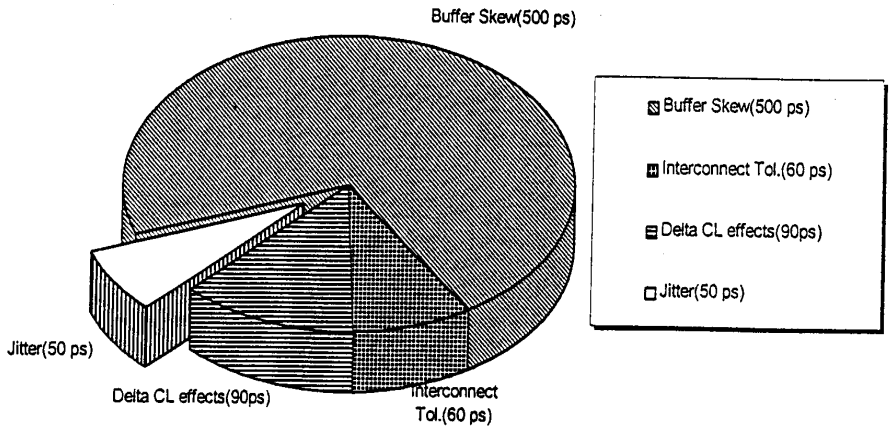


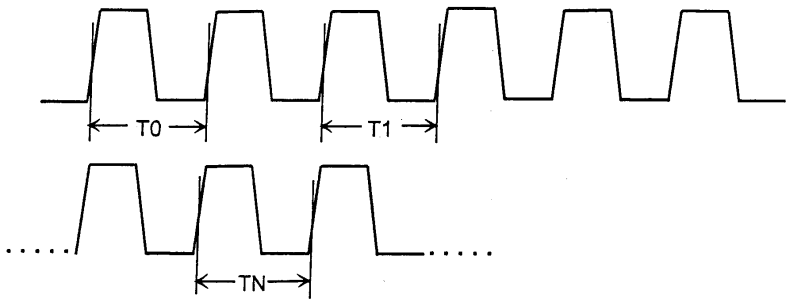
Figure 2

Timing uncertainties scale with shorter cycle times. As the frequency goes up, timing uncertainties become a significant portion of the cycle, resulting in less time for the designer to satisfy system timing requirements. A rule of thumb is to allow 10% of the clock period as a timing margin or clock tolerance. The timing margin is the slack time remaining in each clock cycle. A timing margin protects your circuit against signal degradation from crosstalk, reflections, and manufacturing deviations in your devices and board designs.

A 100MHz system (10ns period) allows 1ns of margins. However, for a 200MHz system (5ns period), this 1ns of margin becomes 20% of the clock period. As designs become more aggressive, timing margins may or may not include the effect of jitter. Consequently, unexpected jitter behavior may appear towards the end of a design and have an adverse impact on system performance. To avoid this pitfall and to insure the PLL functions properly in its intended application, PLL jitter behavior must be measured and understood.

For the purpose of this application note, jitter terminology on the following pages is used.

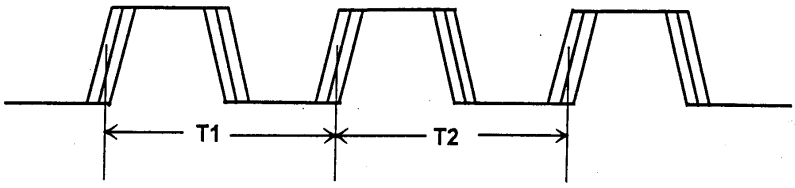
Period Jitter: Maximum period variation of any random cycle



Jitter period=T(i)max-T(i)min
i=0-N i=0-N

Figure 3

Cycle-to-cycle jitter deviation between periods of two adjacent cycles:



Jitter cycle to cycle=T1-T2

Figure 4

Benefits of Using PLL

There are three primary clock sources for use in most digital systems: clock drivers, stand alone PLLs, and embedded PLLs. As shown later in "General PLL Concerns," there are unique concerns when using a PLL. Given these disadvantages, one must ask why the interest and proliferation in the use of PLL.

In recent years, many articles[10-13] have appeared in the press announcing the availability of a variety of PLL-based clock drivers and clock synthesizer chips. These new devices incorporate features like programmable output skews and automatic output deskewing. In many cases, these new devices are single source. This places an enormous burden on the designer to assess the integrity of these products. Often, the device suppliers do not have the resources to evaluate their products in conditions resembling their customers' applications. The *WAVECREST* DTS-2070 is a leading edge instrument for characterizing these new devices.

Significant system benefits result when a PLL option is available. Because of these desirable PLL features, using a PLL can provide the most cost effective timing solution for a system, along with the following:

- Frequency synthesizer
- Clock skew control
- EMI control
- Frequency slow down for green PC
- Clock recovery (data communication).

General PLL Operation Theory

Before we discuss the general concerns with Phase Lock Loop (PLL), a brief discussion of a typical PLL operation is necessary. This background information includes underlying design and characterization issues when using PLLs. Additional references[14,15] are provided on the reference pages of this application note.

Most PLLs are designed to be clock generator and synchronizers consisting of both analog and digital building blocks. The basic PLL building blocks are shown in Figure 5. A digitally controlled PLL consists of a reference counter (N), feedback counter (M), post scaling counter (P), and the four core blocks listed after the block diagram. Counter blocks N, M, and P may not necessarily be included in all PLL designs. F output is proportional to Fref x M/NP.

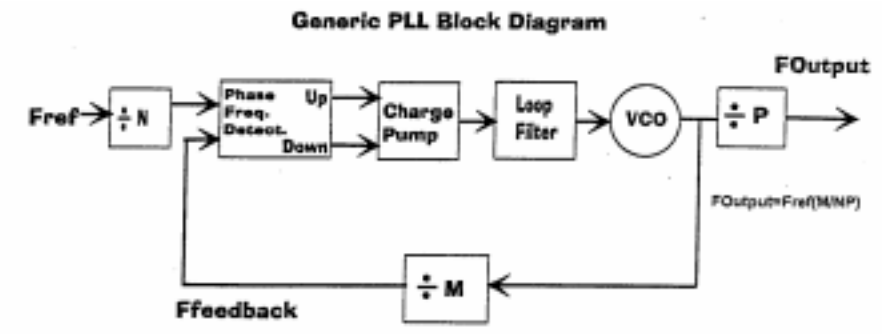


Figure 5

The four core PLL building blocks are (See Figure 5):

- PFD (Phase Frequency Detector)
- Charge Pump
- Loop Filter
- VCO (Voltage Controlled Oscillator)

The PFD detects any phase or frequency difference between the input clock (Fref) and the VCO clock (Ffeedback) and generates a control (error) signal proportional to the phase difference between Fref and Ffeedback. Two outputs at the PFD, UP and DOWN, cause the Charge Pump to modulate the amount of charge stored in the Low Pass Filter. The Low Pass Filter output controls the VCO frequency. If the Ffeedback is leading Fref (VCO output is leading), the VCO slows down somewhat. The DOWN signal is activated to slow down the VCO. If Ffeedback is lagging, Fref, the VCO speeds up somewhat. The UP signal is activated to speed up the VCO. When Fref and Ffeedback are in phase with each other, the PLL holds the control voltage at that potential and phase lock is achieved. Thus, through this negative feedback arrangement, the PLL causes the Ffeedback and Fref signals to be equal with minimum phase offset.

The Charge Pump converts the logic base signals from the PFD into an analog signal suitable for controlling the VCO. This is accomplished by adding or removing charges that are stored in the low pass filter. The Loop Filter's primary function is to integrate the charge pump output (reducing ripple) into a signal suitable for controlling the VCO. Loop Filters can be integrated on chip, or external to the device, like the devices evaluated for this application note. The Loop Filter bandwidth determines how fast the PLL can correct any phase error. Generally, a PLL with narrow bandwidth can reject the input jitter but cannot correct the VCO timing errors quickly. The resultant output jitter is VCO noise limited. A PLL with wider bandwidth can correct VCO errors. However, if the bandwidth is too wide, the resultant system is input jitter limited.[14]

The following dichotomy must be considered in all designs. Low bandwidth provides a more stable PLL design, but may not react fast enough to correct the VCO. If it's too fast (high bandwidth), gain peaking may occur, causing resonance which leads to higher jitter. In addition, the Loop Filter bandwidth has a direct influence in cascaded PLL applications. In general, a downstream PLL must have a loop filter bandwidth that is higher (faster) than the upstream PLL. One of the most difficult parts of the VCO design is to ensure the VCO can reject noise very effectively. A typical PLL generates a lot of switching noise on the power and ground buses which can introduce excessive jitter at the VCO output.

Simultaneous switching, or ground bounce noise, is another important topic in high speed design. Interested readers should consider other references[16] to obtain a better understanding of this subject. Needless to say, simultaneous switching continues to be a concern, since PLL clock drivers tend to incorporate many outputs. A higher number of switching outputs tends to increase ground bounce.

General PLL Concerns

Given the previous PLL operational description, it is not surprising that one of the biggest concerns when using PLL is output jitter. Also worth repeating is the lack of jitter specifications and test methodology for today's PLL devices. The effects of jitter can range from no effects to a complete system malfunction. The following categories cover most of the common causes of PLL output jitter.

- Power supply noise
- PLL deadband region
- Noise from input reference/feedback signal
- Internal switching noise
- Internal and external crosstalk/reflection noise

Many noise sources can disrupt the proper behavior of a PLL. In many cases, these noise sources directly cause the device input thresholds to have time fluctuations. Noise sources can be either internal to the device or external to the device. If the noise source is external, three typical noise entry points can affect PLL behavior. These include the input frequency reference, the power supply attachment point and the feedback point from the VCO. As shown later in "Vcc Noise Using the Oscilloscope Functions," this is the case with some of the devices characterized. In addition, the Loop Filter dynamics and Phase Detector deadband behavior may accentuate these noise source effects.

Various PLL output jitter issues have been reported in articles.[17] In fact, an embedded PLL was reported to have 4ns of jitter with 125mv of 1MHz injected into Vdd in "Electrical Design of the 200Mhz UltraSparc™ Module." This was later reduced to 100ps by the incorporation of an on-board voltage regulator. In this paper and others, noise via the power entry point is stressed because of the wide spectrum of noise that could exist, and because the most sensitive range of noise is between the loop filter bandwidth and the reference frequency. This is further aggregated by the high gain (MHz/V) of the VCO stage. As this application note shows, even without inducing external noise, a PLL can intrinsically have excessive output jitter which could lead to system timing violations. The DTS-2070 measures both synchronous and asynchronous causes of PLL output jitter.

Device Description

The PLL clock driver described here locks its output frequency and phase onto an input reference clock. This device is designed to provide clock distribution for high performance PCs and workstations. Like many PLL devices available on the market today, these PLLs do not have jitter specifications in the data sheets. Consequently, a pass/fail cannot be determined. However, as shown in the tests results section, the DTS-2070 uncovered some major PLL abnormalities that could cause some of these devices to malfunction in a system application.

Two suppliers and three unique PLL designs were evaluated for this note. One sample of each design was characterized using the DTS-2070. One design is from Supplier A. Two designs are from Supplier B. Supplier B discontinued one of the designs and recently introduced a new design. In this application note, the discontinued device is designated as "OLD" and the new is "NEW." In general, these three designs are pin out and functionally equivalent. This application note shows that this may not always be true.

The PLL device evaluated is a 28 pins PLCC low skew PLL clock driver. The device has eight outputs. Five "Q" outputs (QO-Q4) are provided with less than 500ps skew between their rising edges. The /Q5 output is inverted (180° phase shift) from the "Q" outputs. The 2XQ output runs at twice the "Q" output frequency, while Q/2 output runs at half the "Q" frequency. The device uses an external loop filter consisting of seven RC components. There are four digital VCC and five digital GND connections. The analog VCC and GND are isolated by the loop filter. Several output feedback configurations are possible. The one chosen for this work is the 1:1 input to "Q" output frequency relationship.

Test Fixture Setup

The general test setup is shown in Figure 6. Care was taken to use all surface mount components to reduce lead inductance. The PLL loop filter components were mounted within a ½" area of the PLL device pins. The PLL test board used controlled impedance (50 ohms) microstrip with multiple power and ground planes. PLL VCC pins had 0.00luf in parallel with 0.1uf for good decoupling. References for a good discussion on decoupling capacitor selection based on board layout effects can be found at the end of this application note.[18]

An HP8110A pulse generator was used for the input reference frequency to the PLL. The *WAVECREST* DSM-16 relay matrix unit was used in conjunction with the DTS-2070 system under a GPIB controlled from a Pentium grade PC. As shown in the Figure 6, both CH1and CH2 of the DTS-2070 are used. CH1 is used for measuring the input signal to the PLL. CH2 is used for measuring the PLL outputs. The DSM-16 has two channels (CH1 and CH2) with each channel routed to a 3GHz, 1 x 8 SPST switch. Only four cables were available for monitoring PLL outputs. Figure 6 shows four cables to CH2 of DSM-16. Four PLL outputs can be conveniently measured by manually switching the DSM-16 matrix relay. To measure the other four PLL outputs, the four cables were manually switched. The DSM-16 is also GPIB controllable, but was not set up that way for this work.

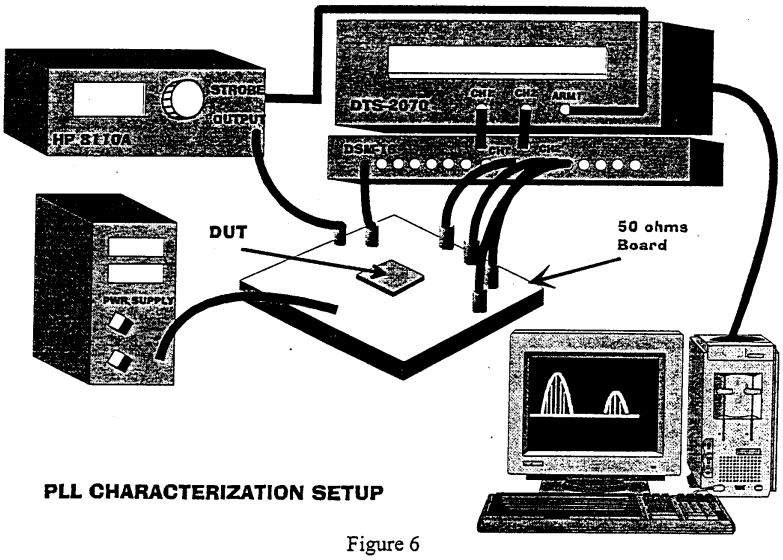


Figure 6

Repeatability is especially important for jitter measurements. A decision was made not to use a hand held probe which could be subject to the manual probing skills of the individual; instead, connections to the PLL input and outputs were made through 50-ohm, high bandwidth cables terminated to SMA connectors. The board fixture has the mating ends for the cable SMA. For providing a 10X attenuation (DTS-2070 is limited to ±1.1v), 450-ohm chip resistors were used on the fixture. Figure 7 provides a detailed block diagram. Outputs not used during the measurement were terminated into 500-ohms to ground (450 ohms on the board in series with 50 ohms from terminator to ground). So for a given measurement, all PLL outputs effectively saw 500 ohms to ground with minimal capacitive loading.

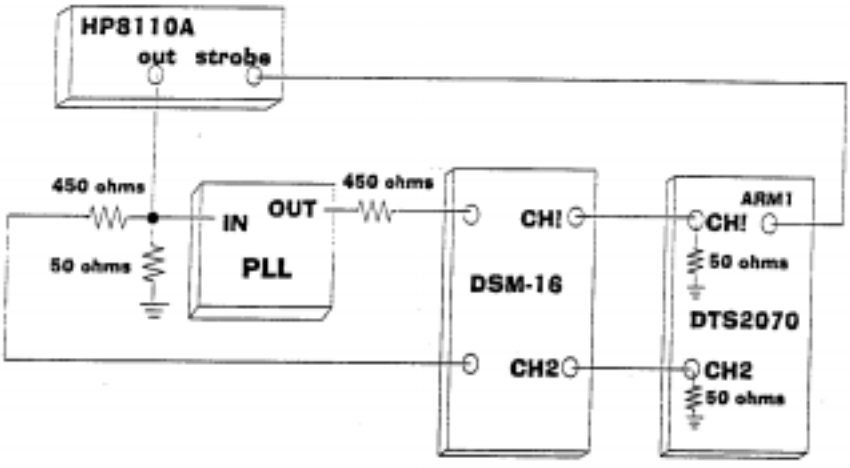


Figure 7

Test Methodology

The measurements for this application note used the following four analysis options available on the DTS-2070.

- Spectrum
- Jitter
- Function
- Oscilloscope

In general, spectrum and jitter analysis are used to look for asynchronous events; whereas, function and oscilloscope typically use an externally- generated sync signal to the DTS-2070 ARM input. [19] This signal is provided by the strobe signal from the HP8110A pulse generator in this application note. The period attribute of the PLL signal was chosen for measurements, although frequency, PW+, PW-, etc. could have been used. Results presented in this application note used room temperature to minimize setup time for each measurement. But in serious characterization work, a temperature controlled system is recommended.

One intent of this application note is to show how the DTS-2070 measurement results can be effectively used for analyzing PLL jitter behavior and for competitive PLL comparisons. In this regard, the results from the two supplier B designs, "OLD" and "NEW," are effectively compared against results from Supplier A. This helps illustrate the usefulness of the DTS-2070 for competitive performance comparisons.

DTS-2070 Test Results

Measurement details from the DTS-2070 are discussed and summarized in the following sections. The DTS-2070 plots referenced in these sections can be found in the Appendix.

Spectrum Analysis of Period (10Mhz/50Mhz)

Plots 1-6 in the Appendix are representative spectrum plots for Supplier A 2XQ, Q4, and Q/2 outputs. Plots 1-3 are for input frequency=50MHz, and plots 4-6 are for input frequency=10MHz. A measurement sample size of N=1000 was chosen. Vcc=5v and input duty cycle was set to 50%. These three outputs were chosen to illustrate the different period histogram modes possible with Supplier A. As clearly shown, Q/2 has a single Gaussian mode, Q4 is bimodal, and 2XQ has three histogram modes.

The number of modes also tracks with frequencies for Supplier A (e.g. Q4 was bimodal for both 10 MHz and 50 MHz inputs). Supplier B-designed output modes did not track in this fashion. What is also apparent when comparing the 10MHz and 50MHz plots is the center of the distribution converging with the lower input frequency. In general, the output jitter measurements for the 10MHz input condition is higher than for the 50MHz input condition.

Figure 8 that follows is a graphical summary of the 1 sigma jitter for all the outputs. It compares the Supplier A device with the Supplier B "NEW" device. Data was taken from spectrum analysis results (similar to Plots 1-6). When comparing Supplier A to Supplier B, notice a significantly higher jitter on 2XQ output for Supplier B, for a 10MHz input frequency condition.

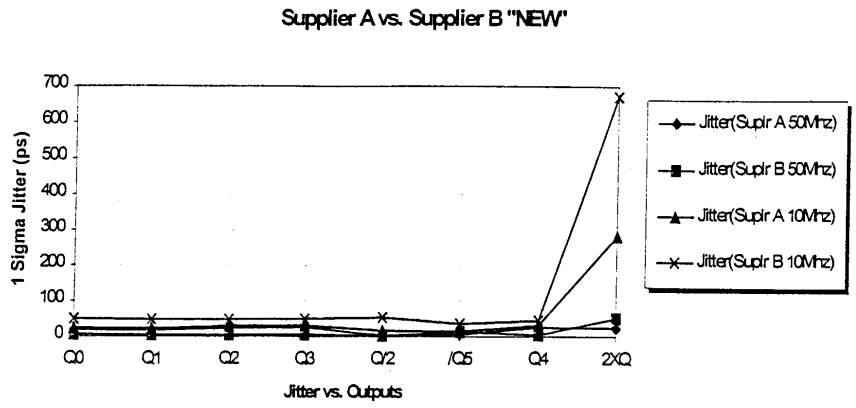


Figure 8

Figure 9 is similar to Figure 8, except 2XQ results were excluded. This allows better resolutions for comparing 10MHz and 50MHz data. Supplier A jitter delta between 10MHz and 50MHz was less than 10ps for most outputs. Supplier B's NEW device was over 40ps, a factor of 4X over supplier A. For the same test conditions, the Supplier A device provides higher timing margins. This is important, since there are no jitter specifications for these PLLs.

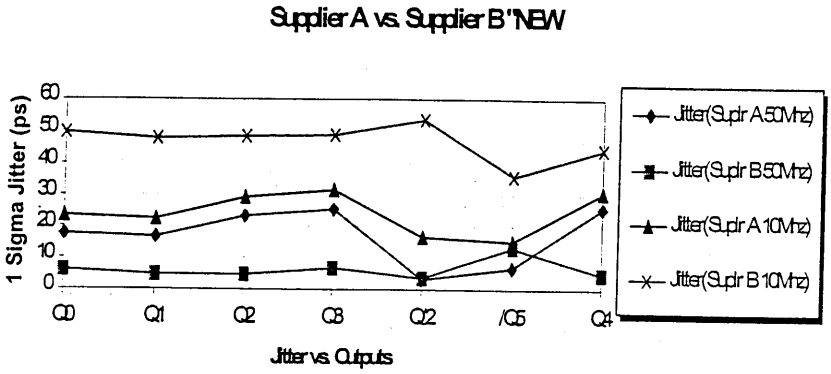


Figure 9

Figure 10 compares the Supplier B NEW design to the Supplier B OLD design. There's no significant difference between these designs, other than the NEW design appears to have 10ps higher jitter for the 10MHz input condition.

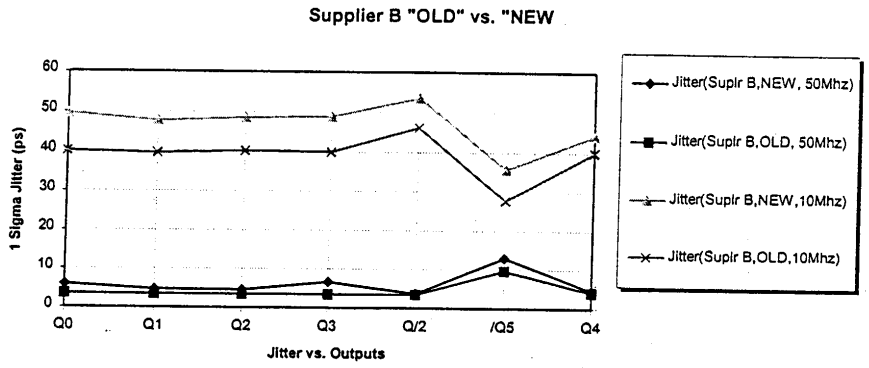


Figure 10

Function Analysis Tutorial

The DTS-2070 function analysis capability can be a very useful tool for analyzing jitter that is synchronized. It can be extremely helpful in explaining the different period modes that are typically evident from a spectrum analysis (as mentioned in the last section, “Spectrum Analysis of Period”). Function analysis is used to explain the cause of trimodal period histograms in the next section. However, a brief tutorial on using a known pattern from the HP8110A is beneficial before proceeding.

The pattern used is a PRBS=7 RZ (see Figure 11). The HP8110A strobe output was connected to the DTS-2070 ARM1 input. A 50MHz frequency (20ns period) was chosen. With an address selection of 20, this provides a total repeatable pattern length of 400ns (7x2Ons+140ns+120ns). The spectrum analysis for this pattern is shown in Plot 7 in the Appendix. Notice the three distinct period distributions shown by the arrows. They are one-to-one correspondences to the periods in the PRBS pattern. The three different period distributions can be considered very excessive period deviations. Keeping this in mind will help in understanding the results in the following section. The 20ns distribution has a higher number of counts compared to the 140ns and 120ns periods.

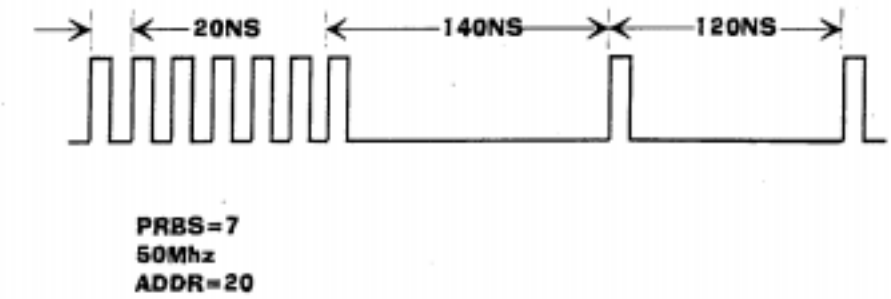


Figure 11

By using the digital filtering feature of the DTS-2070, one can isolate each period distribution for further analysis. Plot 8 in the Appendix appears when digital filtering is used to zoom in on the 20ns period distribution. As shown, the 20ns period is bimodal. Plot 9 is for the 120ns period. The number of data points is inadequate due to the 7:1 ratio of the 20ns periods. By using the accumulation mode (see Plot 10) to store more data, the 120ns period distribution is approximately Gaussian. A good rule of thumb to use when trying to determine whether a distribution is Gaussian or not is if the range value of the distribution is three times the 1 sigma or jitter value. Plot 11 shows the 140ns period result after using digital filtering and the accumulation mode.

Plot 12 shows the function analysis for the PRBS pattern. Shown on the X axis is the number of consecutive periods or counts. There are seven consecutive periods at 20ns followed by the 140ns and 120ns periods. Thus, the function analysis establishes the order of precedence for the different period modes evident in spectrum analysis. This becomes very useful in analyzing synchronous PLL output jitter as discussed in the next section.

Function Analysis and Pattern Sensitivity of Output Jitter

Oftentimes, using spectrum analysis and depending on the measurements that are made, results in multiple histograms displaying as stated previously. The following explains how function analysis can complement and enhance the understanding of PLL output jitter. For this example, the PLL output period is used. Plot 13 in the Appendix shows the period spectrum for 2XQ output for the Supplier B NEW design. The input to the PLL is 50MHz. Therefore, the basic 2XQ period should be 10ns. Plot 13 shows three distinct period distributions, each distribution labeled with a circled number. The first distribution (far left) is labeled with circled numbers 2 and 4. This will be explained shortly. With the help of Figure 12 and function analysis, the cause of the three period distributions is explained. Figure 12 shows the phase relationships of the four unique PLL output configurations. Remember, Q is really Q0-Q4. Function analysis for 2XQ output is shown in Plot 14 of the Appendix.

It is suggested that the three distributions identified in Plot 13 are caused by the order of PLL output switching activities. This leads to internal switching noise which translates to output jitter modulation. Each set of unique output rising and falling edges (Figure 12) can give rise to a specific mode of period jitter. With the help of Plot 14 (function analysis) and Figure 12, the circled period distributions in spectrum analysis (Plot 13) are correlated to the appropriate four different modes of edge switching.

Plot 14 shows that period deviations repeat every four cycles. Cycles 2 and 4 correspond to the lowest period numbers. Since they occur twice within four cycles, they produce the highest number of hits or counts in the far left spectrum analysis histogram. This corresponds to the switching activities on /Q, Q, and 2XQ (see Modes 2 and 4 of Figure 12). Plot 14 shows that cycle 1 and 3 have approximately the same period duration, with the cycle 3 period slightly higher. This corresponds to the distributions 1 and 3 of spectrum analysis and to switching activity Modes 1 and 3 of Figure 12.

Plot 14 displays consecutive periods of the measured signal. It shows how this information can be used to arrive at cycle-to-cycle jitter information.
Also, if an asynchronous signal was present, distinct distributions may not appear. Instead, a general overall spreading of the distributions may occur. If other output switching activities are occurring, function analysis can help determine the relationship of these occurrences to output jitter, and may provide some insight on how to position the outputs and feedback arrangements. Using the PLL as an example, one can see the influence of /Q edges on Modes 2 and 4. Moving /Q output to the side of the package where 0/2 is located (no switching activity Figure 12) may provide better overall jitter performance. Although, this is only a hypothetical solution, since many constraints are involved.

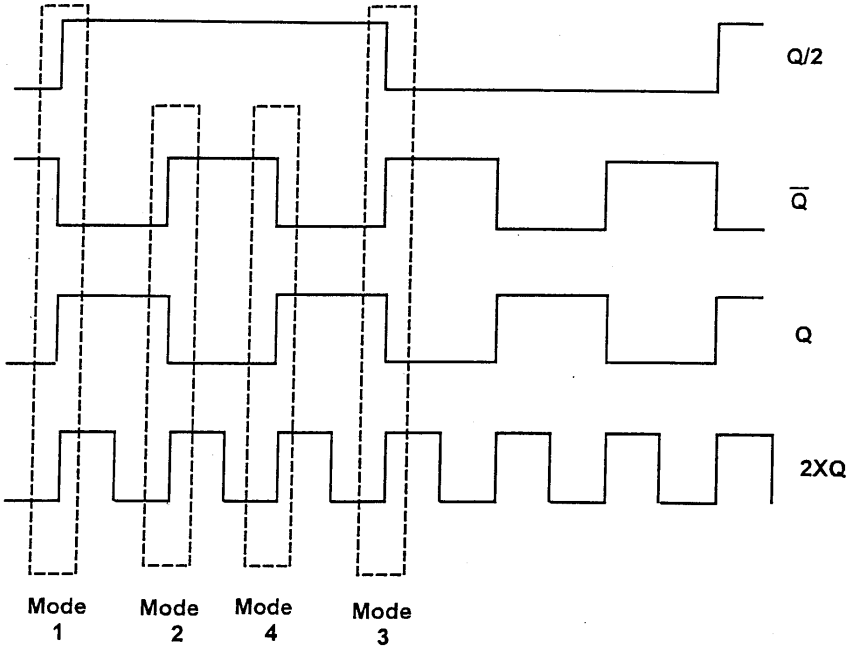


Figure 12

Spectrum Analysis and Input Frequency Sensitivities

Previously, we used spectrum analysis to look at the output period spectrum with 10MHz and 50MHz inputs (min./max. range from data sheet). However, experience has shown that PLL output jitter behavior may have “pockets” of input frequencies that may cause anomalous output behavior. Using the same technique described in “Spectrum Analysis of Period,” the 2XQ output period jitter was measured as the input PLL reference frequency swept from 8MHz to 50MHz. Results are summarized in Figure 13.

For 20MHz to 50MHz inputs, the output 1 sigma jitters were all below 200ps. However, below 20MHz, Supplier B has significantly more jitter than Supplier A. For system applications, Supplier A should be seriously considered over Supplier B for a more stable clock design. In addition, the Supplier B NEW design has significantly higher jitter over the OLD design below 10MHz. This may or may not be related to the external loop filter used in our test setup. The Supplier B NEW design recommends a loop filter that is slightly different than the filter recommended by Supplier A, which is also the filter used on our test fixture.

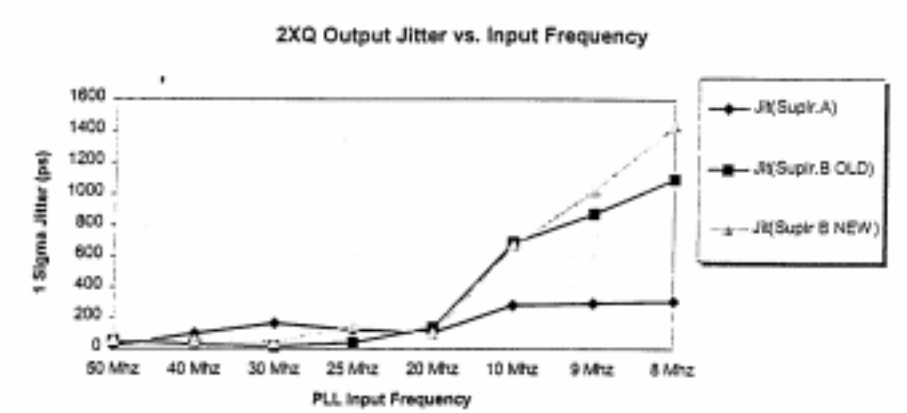


Figure 13

The above PLL output jitter behavior suggests that a finer frequency sweep (especially at lower input frequency) on the PLL input may be revealing. When this was performed on the Supplier B OLD design, a significant output jitter sensitivity was noticed when the input frequency was set to 19.5MHz. Not only was there an input frequency sensitivity, but the Vcc level also had a significant influence on output jitter behavior.

Plots 15-18 in the Appendix are typical spectrum analysis plots for 2XQ output with input at 19.5MHz with Vcc 4.5v to 5.25v. Ideally, a 19.5MHz input should provide a 2XQ output period of 25.6ns. Plots 15-18 show 2XQ period distributions going from bimodal at Vcc-4.5v to overlapping quad-modal at Vcc=4.75v, to overlapping bimodal at Vcc=5.0v, back to non-overlapping bimodal at Vcc=5.25v.

The same input frequency sweep was used on the Supplier A device, but no significant output jitter anomalies were evident. This data provides another reference point for choosing the Supplier A design over Supplier B design for better timing margins in a digital system design.

Overlapping period modes are a special concern, since they occur with an operating Vcc in a system environment. Plots 19 and 20 were made using the oscilloscope analysis capability of the DTS-2070. Notice the severe period distortion at both Vcc=4.75v and 5.00v. Since overlapping modes suggest some asynchronous cause and effect, jitter analysis is described next to provide full details and give a better understanding of this PLL output jitter behavior.

Using Jitter Analysis for Asynchronous Output Jitter Characterization

This section demonstrates how the DTS-2070 jitter analysis option can be used to analyze asynchronous effects on PLL output jitter. The overlapping period histograms in Plots 16 and 17 suggest that an asynchronous noise source is modulating the PLL. Plots 21 through 24 show the jitter analysis results for 2XQ output for the Supplier B OLD design.

Each Plot shows the accumulated period jitter over 200 consecutive cycles with 1000 measurements taken at each cycle. In all plots, there is evidence of output jitter modulation by a noise source. In fact, the modulation is repeated over the entire 200 cycles for Vcc=4.75v and 5.0v. A careful check on Plots 22 and 23 reveals that the modulation repeats every 28 cycles (30-2). Dividing the 2XQ output frequency of 39MHz (2 x 19.5MHz) by 28 cycles, gives a modulation frequency of 1.4MHz on the 2XQ output.

To further trace the cause of this output jitter modulation, jitter analysis was performed on the input to the PLL (input reference to PLL from HP generator). The results are shown in Plots 25-28. At Vcc=4.75v and 5.0v, one can see distinct input modulation. However, unlike 2XQ jitter analysis at Vcc=4.75v and 5.0v (Plots 22 and 23) which took 28 cycles for complete modulation, the results for the input shows approximately half of the 28 cycles or 14 cycles.

Since Q4 output is used as the feedback to the Phase Detector, jitter analysis was also performed on Q4. Plot 29 shows the results with a 1:1 match to the modulation profile of the input signal. Since Q4 output frequency is half that of 2XQ output, by dividing 19.5MHz by 14 cycles, we again arrive at the 1.4MHz modulation frequency. One possible explanation is that the PLL overall loop bandwidth may have some peaking around the 1.4MHz region and is sensitive to any noise source within this frequency spectrum.

With the help of jitter analysis, we determined that excessive 2XQ output jitter at 19.5MHz is caused by a modulation effect at the PLL input reference pin from the Q4 feedback signal to the PLL Phase Detector. However, only using spectrum analysis on the input signal does not show the modulation effects. (See Plots 30 and 31 in the Appendix). At Vcc=4.5v, there is no apparent input jitter modulation. But at Vcc=4.75, there is modulation. The spectrum analysis for both of these Vcc conditions displays a Gaussian distribution.

When the Supplier B NEW design was evaluated at a 19.5MHz input, no output jitter anomalies appeared, but a further input frequency sweep showed similar behavior at an input reference frequency of 23MHz. See Plots 32-33 for spectrum and jitter analysis results for 2XQ output. Plot 34 is the jitter analysis for the input to the PLL. It appears that both the OLD and NEW designs from Supplier B have “pockets” of input frequency sensitivities. The Supplier A design, over the same input frequency sweep, does not.

Vcc Noise Measurement Using the Oscilloscope Function

The DTS-2070 oscilloscope function option can effectively measure the Vcc noise on the device, instead of using a digital sampling oscilloscope. In addition, this section shows the importance of using the correct ground reference for measuring low amplitude noise signals.

A Tektronics P6204 FET single-ended probe (10 MEG, 1.7pf, 1Ghz) with external power supply was used. The HP8110A strobe signal was connected to ARM1 of the DTS-2070. To reduce any resonance effects from long ground leads, a spring ground (1/2") was connected to the probe tip outside barrel ground.

Two Vcc pins were measured on the Supplier A device. Pin 27 is to digital Vcc and pin 8 is to analog Vcc for the loop filter. The input to the PLL is a 50MHz (20ns period) square wave.

Plot 35 in the Appendix is the DTS-oscilloscope result for Pin 8 Vcc noise. The peak-to-peak noise amplitude is 200mv with the highest positive peaks occurring at 20ns intervals. Plots 36 and 37 show the Vcc noise on Pin 27. Both plots are using the same probe with probe ground connected to board (fixture) ground. Plot 36 indicates a peak-to-peak noise that is 40mv higher (110mv-70mv) than Plot 37. Plot 37 used the ground directly under the device; whereas measurement for Plot 36 used ground to the side, and therefore, the effective loop inductance is higher.

The above technique was used to measure the Supplier B OLD design for 19.5MHz and 50MHz input conditions to see if Vcc noise could help explain some of the jitter behavior. Plots 38 and 39 show the results for Pin 8. The results do not show any relationship to the PLL output jitter modulation with 19.5MHz input. The only obvious difference is that the positive Vcc noise peaks for the 19.5MHz input condition are significantly wider.

In the course of debugging output jitter, a common measurement is the power and ground noise at the various Vcc pin(s) on the device. Looking for any unexpected artifacts such as this measurement can help explain output jitter behavior. This section shows how the strobing voltmeter technique of the DTS-2070 oscilloscope analysis can be effectively used for this purpose. Using the DTS-2070 in this manner makes an oscilloscope unnecessary. In fact, a good application for the DTS-2070 is for ground bounce characterization of devices where both amplitude and the width of the around bounce pulse are a concern.

Jitter Caused by Unterminated Outputs

This section demonstrates the resolution and repeatability of the DTS-2070, and any effects of output jitter if neighboring outputs are left unterminated. Figure 14 shows the tabulated results from spectrum analysis on the Supplier B OLD design. Test conditions were Vcc=5.0v and 50MHz input reference frequency. Output 2XQ 1 sigma jitter was measured.

As Figure 14 clearly shows, an unterminated output has a direct impact on 2XQ jitter results. As more outputs are left unterminated 2XQ jitter increases. And with QO-Q4 outputs unterminated, 2XQ jitter doubles. By connecting the output terminators back in reverse sequence, the DTS-2070 obtained the same jitter values shown in Figure 14 within ±1ps.

This result implies that output termination must be strictly defined when small jitter measurements are made. Both the DC and AC loading aspect of the output load should be considered when assessing and discriminating small deviations in jitter.

2XQ Output Jitter vs.number of unterminated outputs

Output(s) Unterminated	2XQ Jitter
None	46ps
Q0	59ps
Q0-Q1	72ps
Q0-Q2	82ps
Q0-Q3	92ps
Q0-Q4	102ps

Figure 14

Conclusions

The trend for increasing performance through faster synchronous system designs will drive the requirements for high clocking rates into the 1GHz region by the year 2000. As faster clock rates are used, the characterization of timing accuracy and jitter becomes a critical success factor in creating an error free design for both suppliers of clocking devices and the users of these devices.

With enough processor horsepower, simulation tools like SPICE can do a very good job in predicting skews on a device and system level, but jitter is an attribute of the timing signal that needs to be measured in order to produce a statistically sound timing budget.

The *WAVECREST* DTS-2070 one-shot measurement instrument, along with easy to use software, provides a flexible and powerful tool to meet these stringent requirements. The results presented in this application note show that by using a combination of the spectrum, function, jitter, and oscilloscope DTS-2070 features, PLL output jitter behavior can be characterized, with the cause and effect on output jitter effectively analyzed. From a competitive standpoint, a better product can be distinguished from a marginal product. By using the DTS-2070, this note demonstrates that the Supplier A PLL design is superior to the Supplier B designs. The key points supporting this conclusion are:

- The Supplier A design had a significantly higher period jitter on the 2XQ output (1 sigma jitter was approximately 700ps).
- When compared with Supplier A, Supplier B exhibited 4X higher 1 sigma jitter, better 50MHz and 10MHz input conditions.
- Below 10MHz, Supplier B PLL output jitter increased, whereas Supplier A flattened out.
- Both Supplier B designs exhibited pockets of input frequency in which output jitter is modulated by the Q4 output. This pin is used as the feedback signal to the PLL input feedback pin. For the Supplier B OLD design, an input frequency of 19.5MHz was discovered; for the Supplier B NEW design, an input frequency of 23MHz was discovered. In addition, it was discovered that a small change in Vcc can have a significant effect on the PLL output jitter. The modulation rate using jitter analysis was found to be 1.4MHz for both designs. It was hypothesized that this modulation rate is possibly related to the PLL loop filter bandwidth peaking point.

In addition, using function analysis allows the relationship between different period distributions caused by output switching activities; this is common to all PLL-based clock drivers/synthesizers.

Repeatability of the DTS-2070 was indirectly demonstrated by measuring the small incremental changes in PLL output jitter, as neighboring output(s) were left unterminated and terminated again.

In spectrum analysis mode, the DTS-2070 is able to take 1000 one-shot measurements, calculate the statistical results, and transfer the results to a host PC or workstation in less than 70mS. This makes the DTS-2070 useful as both a characterization or production instrument for clock drivers with and without PLL.

The DTS-2070 Versus DSOs

As discussed in this application note, the DTS-2070 is a very effective instrument for PLL jitter characterization. However, since digital sampling oscilloscopes (DSOs) are also used for jitter measurement, some general observations and comments should be made that compare the two.

High end DSOs can provide a histogram view of timing events; however, there is a significant accuracy-speed trade off involved here. The typical step one takes is to use infinite persistence on the display and set up a “window” on an expanded edge of the waveforms for the DSO to take the measurements. The smaller the window, the more accurate the jitter measurement. But a smaller window takes much longer, since there are less data points or “hits” for the DSO to capture. Using a window size of only 20mv, results can take many seconds to appear on the screen.

The above steps cannot only be cumbersome, but make it difficult to correlate to measurements taken by others. Unless the exact window size, timing and voltage scales are used, the results may vary. Using the same timing scale is important since DSOs have timing error that is based on time/div. settings. Because a DSO may take several seconds before a timing histogram is displayed on the screen, the user cannot easily see the effects of small changes in real time as conditions in the test environment such as Vcc and input signal conditions are changed.

In the DTS-2070 spectrum analysis mode, the different histogram period modes can “dance” around as Vcc and input signal conditions are manually varied. This flexibility is very useful in the device bench characterization and debugging environment.

Another important point is that DSOs require a trigger for proper operation. Depending on the slew rate of your signal used for trigger, a trigger error factor must be accounted for when correlating to previous measurements. How often does one document the characteristics of the trigger source? The DTS-2070 does not require a trigger signal because of its auto arming feature.

Jitter specifications are slowly beginning to show up in PLL data sheets. Like output skews, which may or may not be tested for in a production environment, output jitter will initially follow the same path. Jitter is not considered an unimportant parameter, but simply difficult to measure in general ATEs. In the future, with the competitive nature of the electronic industry, and a growing quality awareness of six sigma designs, the electronic industry may require jitter tests and not rely on sample tests or design “guarantees.”

Although the aspects of integrating the DTS-2070 into a production ATE environment is not discussed in this application note, other *WAVECREST* application notes[20,21] are available on ATE testing.

About the DTS-2070

The DTS-2070 is a precise, high-speed time measurement instrument designed for use in automated lab and production environments where large amounts of accurate and repeatable data are required.

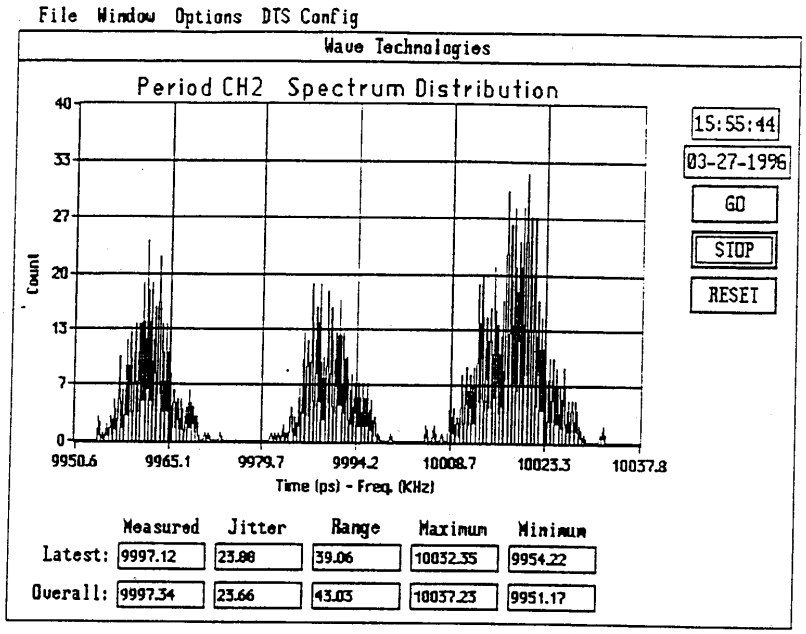
Because of the patented calibration technique used in the DTS design, the linearity and repeatability of all timing measurements can be guaranteed to tight tolerances. Calibration is based on a built-in standard with 0.1 femtoseconds of accuracy in 10.0 nanoseconds.

The single shot speed of the DTS enables it to take many measurements in a burst to verify jitter distributions or to simply verify good continuity on contacts in a production environment.

References

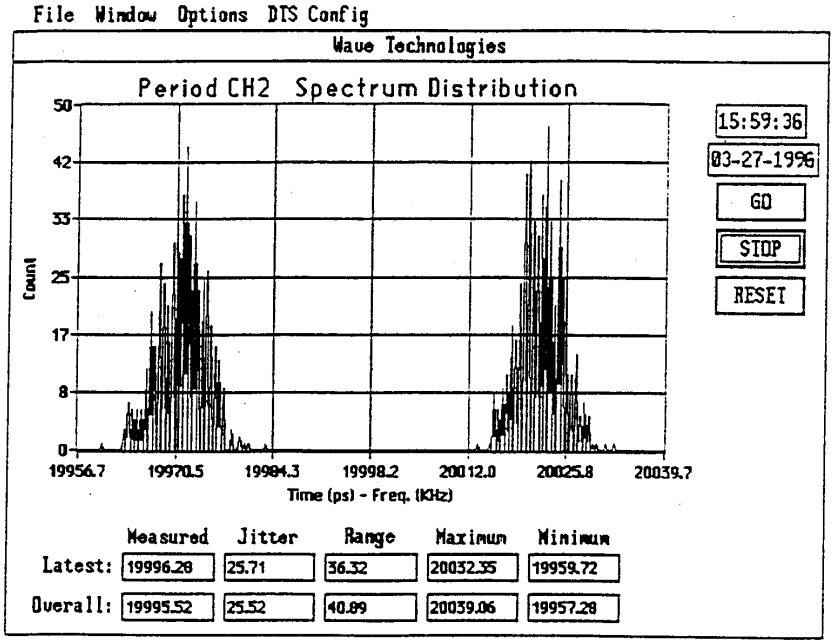
1. WE Thain, J.A. Connelly, *A Determination of the Best Macromodal Circuits for a Phase-Locked Loop*, Georgia Institute of Technology.
2. D. Chen, *Designing On-Chip Clock Generators*, IEEE Circuits & Devices, 1992.
3. *Jitter Analysis of Clock Recovery Devices at 155-52 MBIT/S*, *WAVECREST* Application Note No. 120.
4. Bogatin Enterprises, *High Speed System Design Methodology and Principles and Applications of Inductance*, 1994 notes.
5. E.G. Friedman, *Clock Distribution Networks in VLSI Circuits and Systems*, IEEE Press, 1995.
6. R.K. Poon, *Computer Circuits Electrical Design*, Prentice Hall, 1995.
7. H.W. Johnson, M. Graham, *High Speed Digital Design*,Prentice Hall, 1993.
8. JEDEC JC42 working committee minutes.
9. M.K. Williams, A.M.R. Pfaff, *Clock Design and Measurement Issues in Pentium Systems*, Hewlett Packard Journal, 1994.
10. R. Myrvaagnes, *A Smorgasbord of Clock Chip Solutions*, Electronic Products, February 1995.
11. F.G. Goodenough, *Analog Techniques Deskew Clocks, Multiply Sines*, Electronic Design, May 13, 1993.
12. G. Tharalson, *Low Skew Clock Drivers: Which Type is Best?*, Electronic Products, May 1992.
13. D. Bursky, *Unsurpassed Flexibility Heralds Clock Generator*, Electronic Design, November 12, 1992.
14. C. Vaidya, *Design and Application of High Speed Clock Generators*, National Semiconductor, On Chip Design Conference, 1995.
15. T. Pearson, T. Boar Motorola, *Successfully Implementing Phase Locked Loops into High Performance Clock Networks*, High Performance System Design Conference, 1996.
16. J.L. Prince, *Simultaneous Switching Noise of CMOS Devices and Systems*, Kluwer Academic Publishers, 1994.
17. C. Cheng, *Electrical Design of the 200 MHz UltraSparc Module*, High Performance System Design Conference, 1996.
18. T.V. Doren, J. Drewniak, T.Hubing, *Printed Circuit Board Response to the Addition of Decoupling Capacitors*, University of Missouri-Rolla EMC Lab.
19. *Arming the DTS-2070, WAVECREST* Application Note No. 115.
20. *DTS-2070 ATE Testing Applications Measuring One Shot Events, WAVECREST* Application Note No. 118.
21. *Achieving ±30ps Accuracy in the ATE Environment, WAVECREST* Application Note No. 114.

Appendix



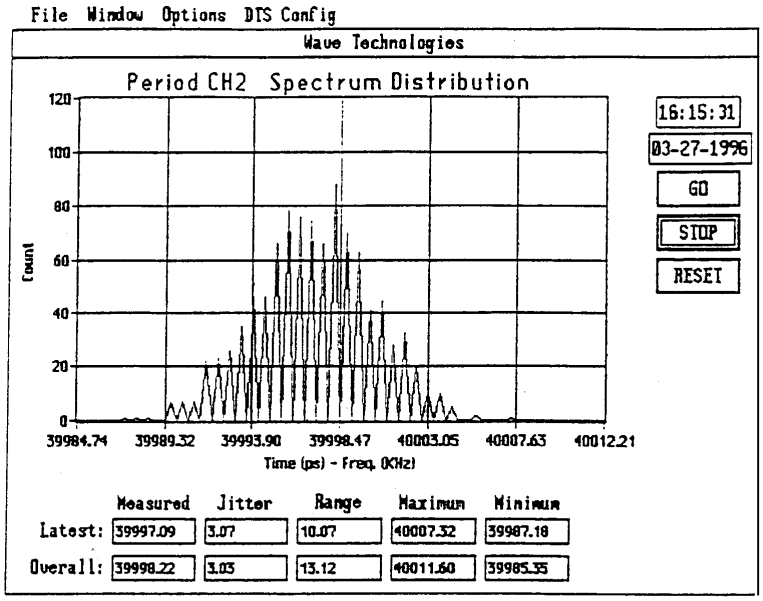
Spectrum Analysis--2XQ Period Jitter
(50 Mhz In, Vcc=5.00v, Supplier A)

PLOT 1



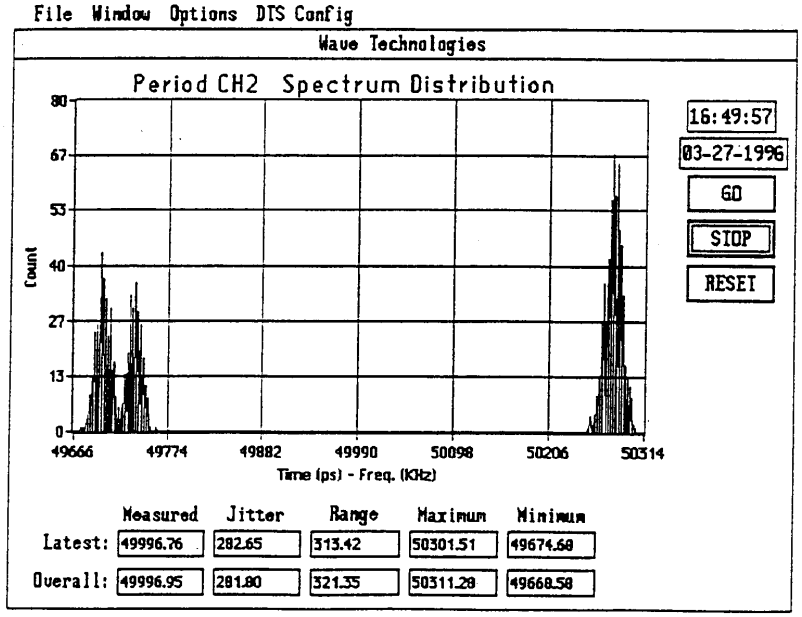
Spectrum Analysis--Q4 Period Jitter
(50 Mhz In, Vcc=5.00v, Supplier A)

PLOT 2



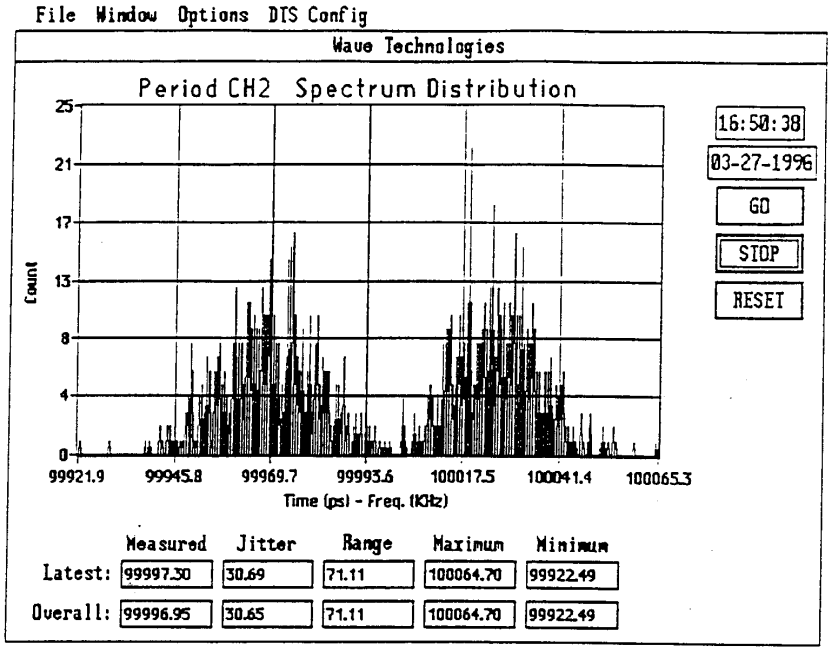
Spectrum Analysis–Q/2 Period Jitter
(50 Mhz In, Vcc=5.00v, Supplier A)

PLOT 3



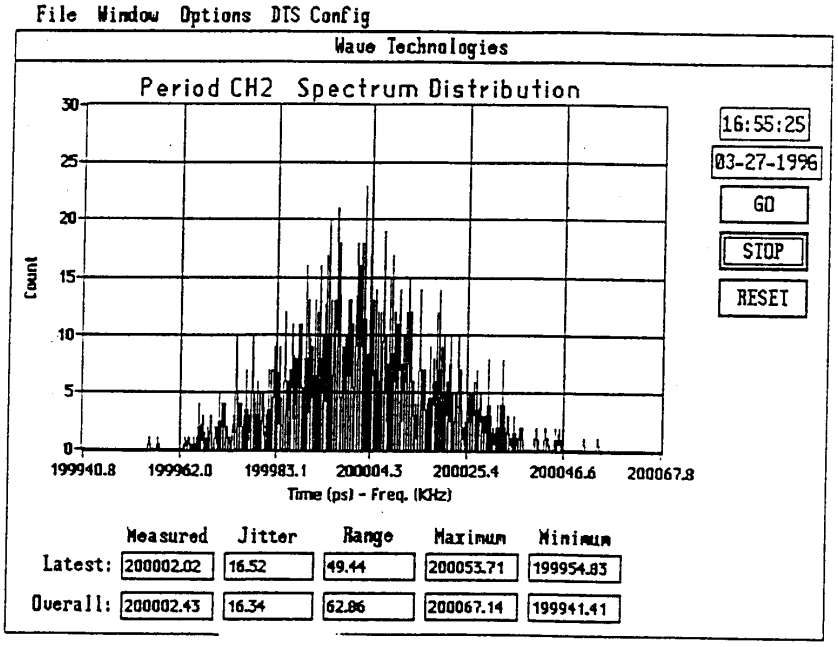
Spectrum Analysis–2XQ Period Jitter
(10 Mhz In, Vcc=5.00v, Supplier A)

PLOT 4



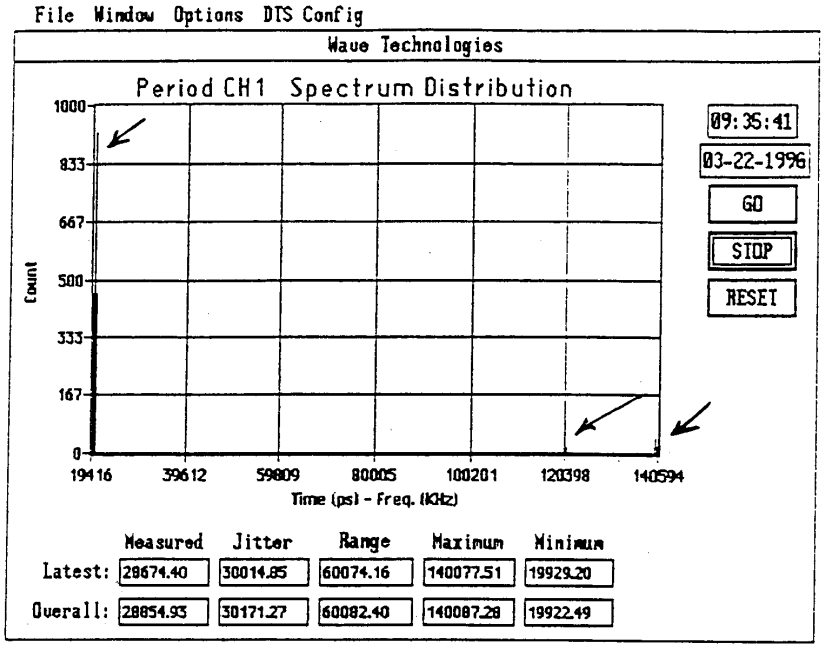
Spectrum Analysis--Q4 Period Jitter
(10 Mhz In, Vcc=5.00v, Supplier A)

PLOT 5



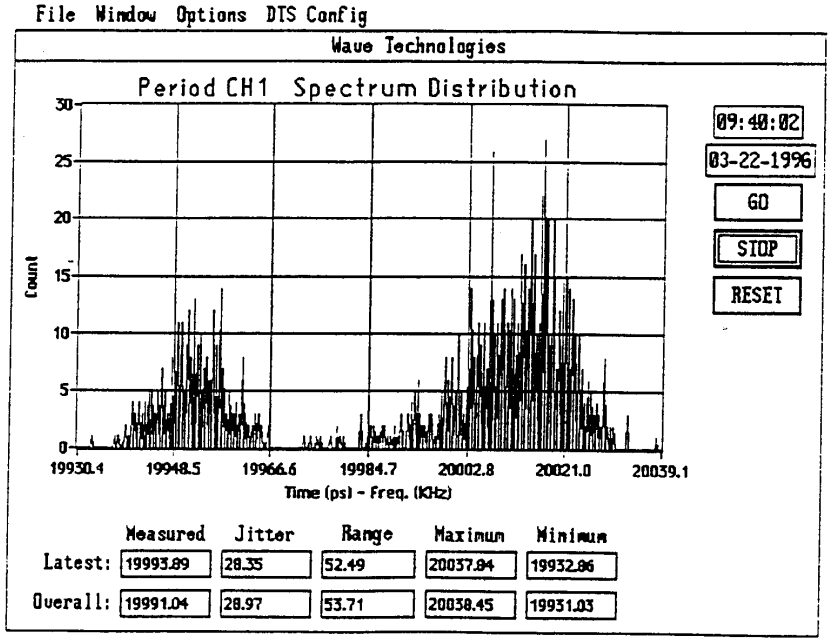
Spectrum Analysis--Q/2 Period Jitter
(10 Mhz In, Vcc=5.00v, Supplier A)

PLOT 6



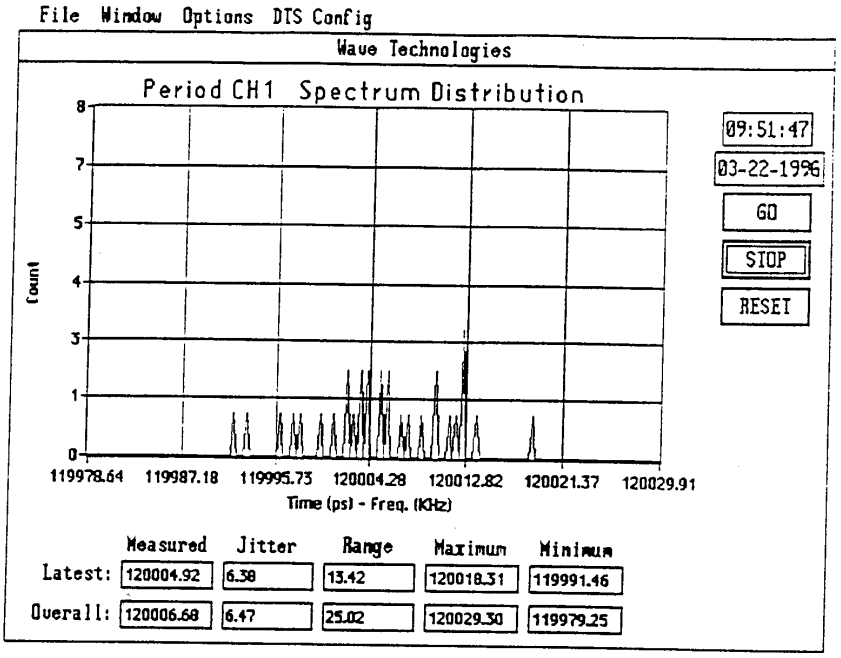
Spectrum Analysis--HP8110A PRBS=7 (20ns, 120ns, 140ns Periods)
(50 Mhz Output, No Filtering)

PLOT 7



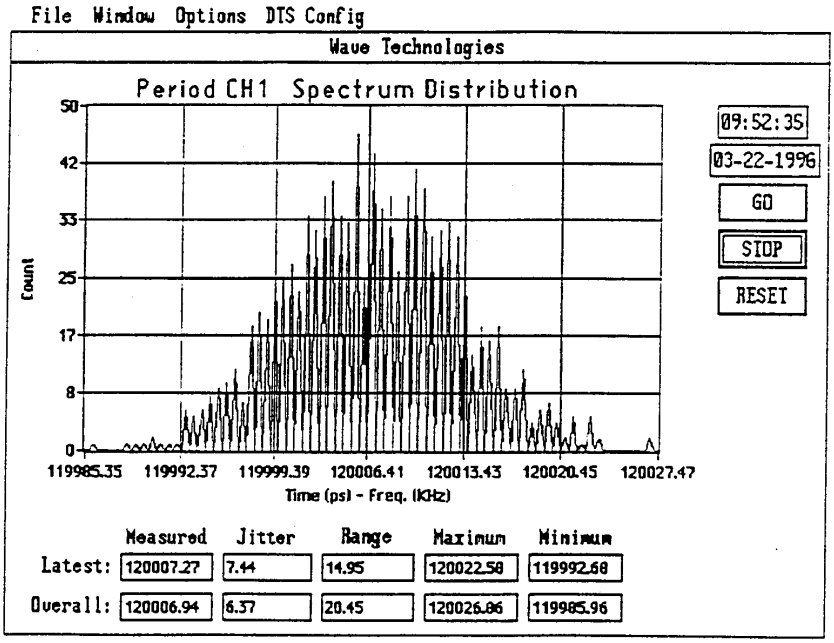
Spectrum Analysis--HP8110A PRBS=7
(50 Mhz Output, Filtering around 20ns period)

PLOT 8



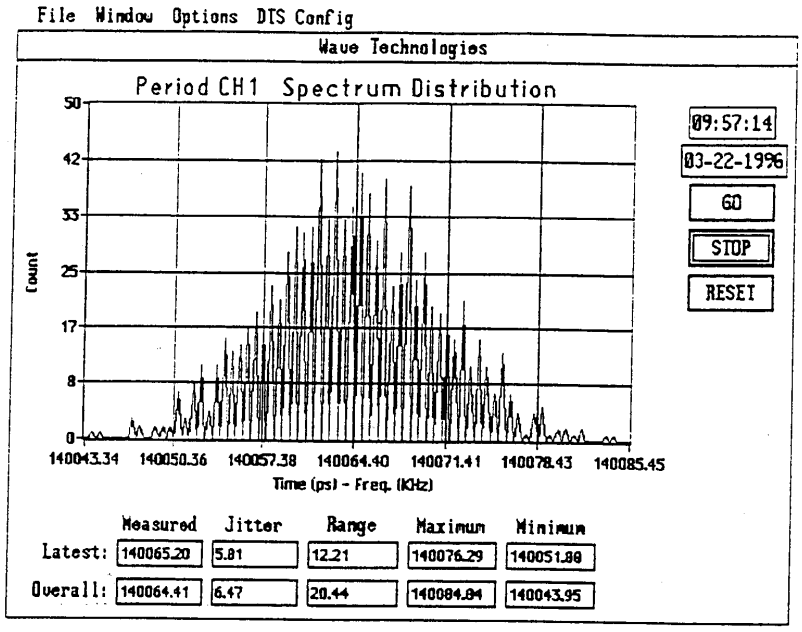
Spectrum Analysis--HP8110A PRBS=7
(50 Mhz Output, Filtering around 120ns Period, No Accumulation)

PLOT 9



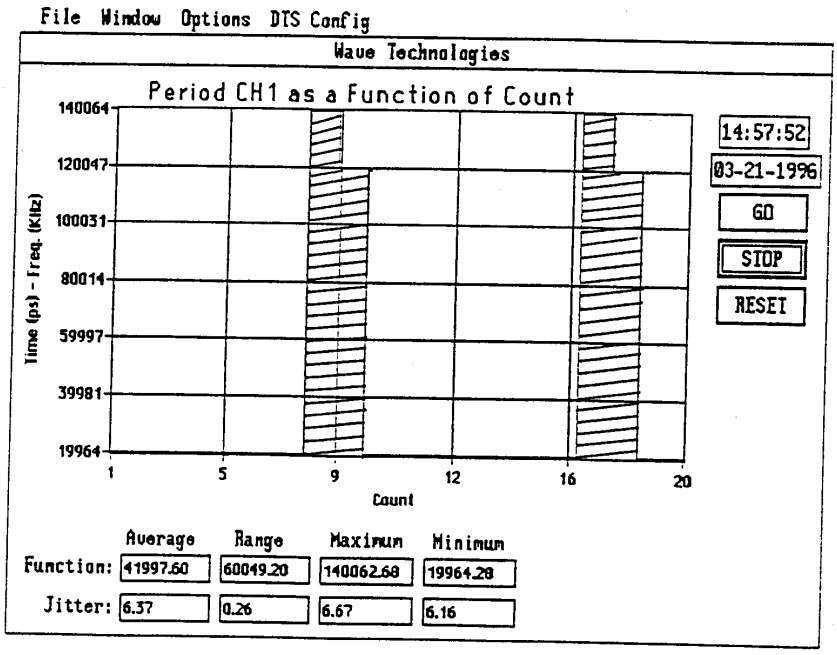
Spectrum Analysis--HP8110A PRBS=7
(50 Mhz Output, Filtering around 120ns period, With Accumulation)

PLOT 10



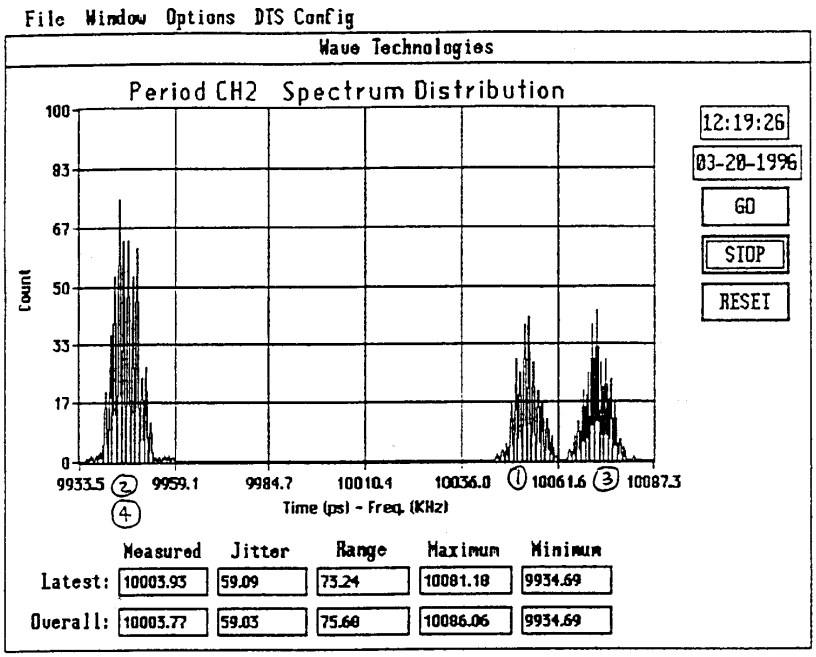
Spectrum Analysis--HP8110A PRBS=7
(50 Mhz Output, Filtering around 140ns Period, With Accumulation)

PLOT 11



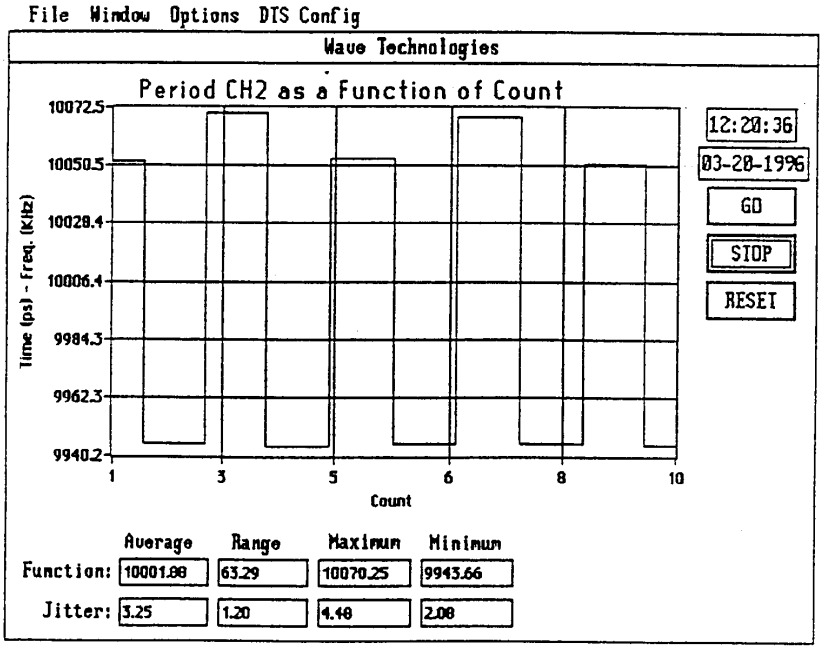
Function Analysis--Period vs.Counts HP8110A PRBS=7
(50 Mhz Output)

PLOT 12



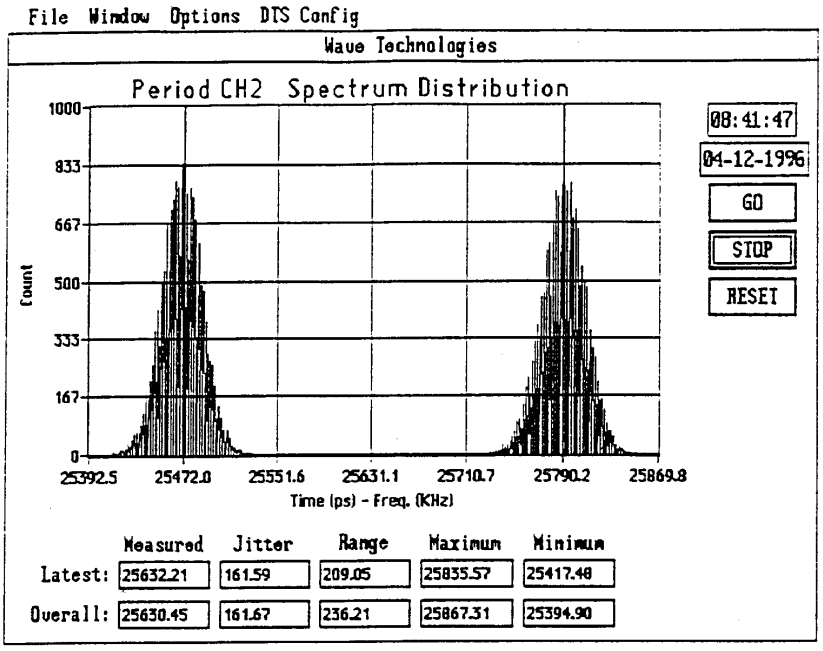
Spectrum Analysis--2XQ Period Jitter
(50 Mhz In, Vcc=5.00v, Supplier B NEW)

PLOT 13



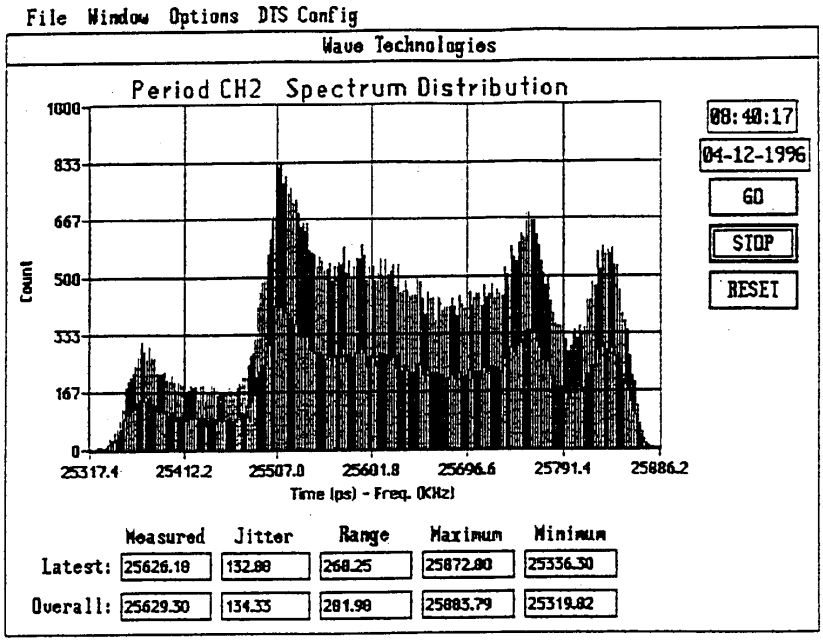
Function Analysis--2XQ Period vs. Counts
(50 Mhz In, Vcc=5.00v, Supplier B NEW)

PLOT 14



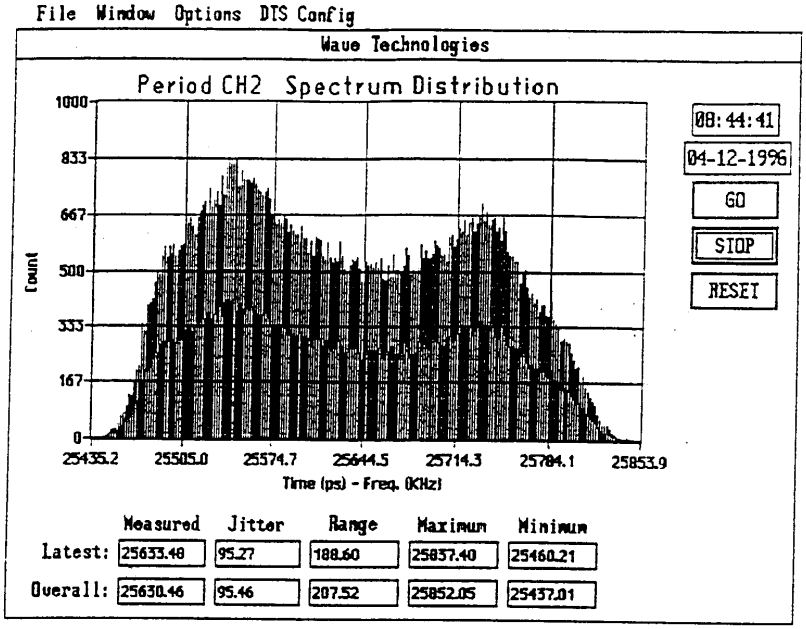
Spectrum Analysis--2XQ Period Jitter
(19.5 Mhz In, Vcc=4.50v, Supplier B OLD)

PLOT 15



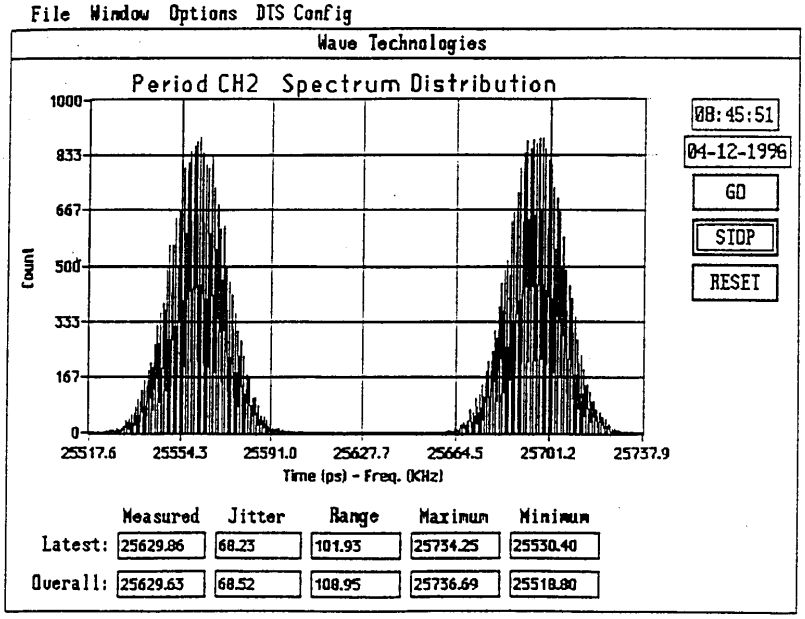
Spectrum Analysis--2XQ Period Jitter
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 16



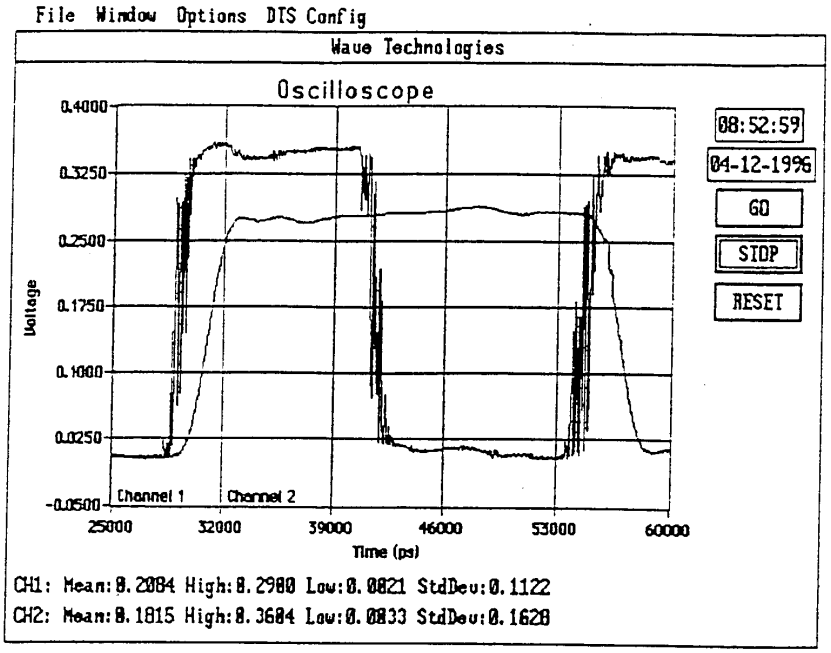
Spectrum Analysis--2XQ Period Jitter
(19.5 Mhz In, Vcc=5.00v, Supplier B OLD)

PLOT 17



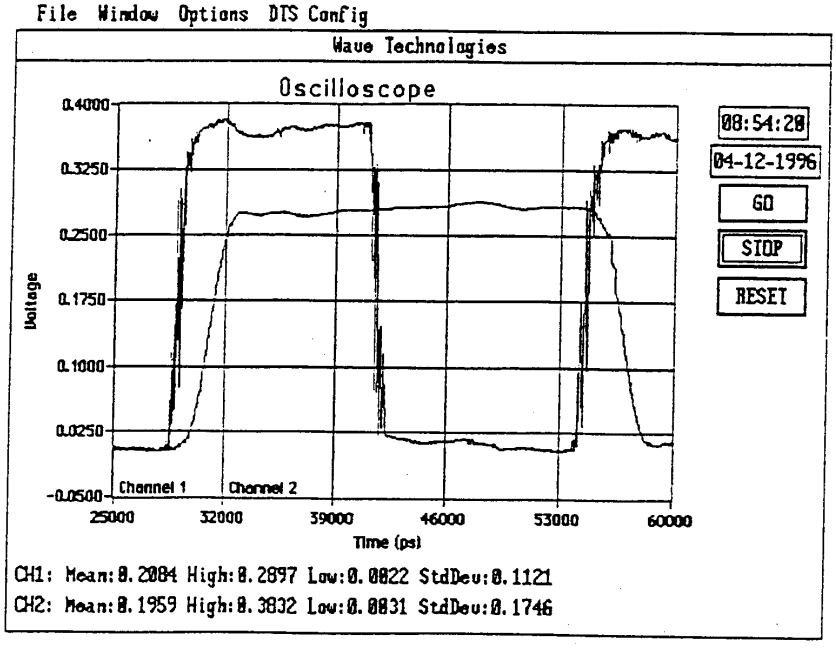
Spectrum Analysis--2XQ Period Jitter
(19.5 Mhz In, Vcc=5.25v, Supplier B OLD)

PLOT 18



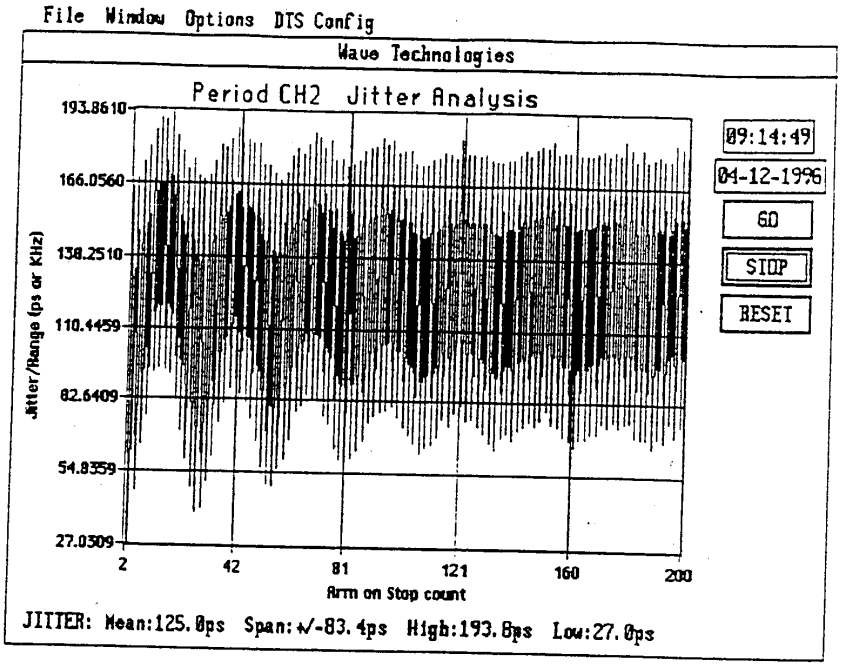
Oscilloscope Analysis--2XQ Period Jitter
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 19



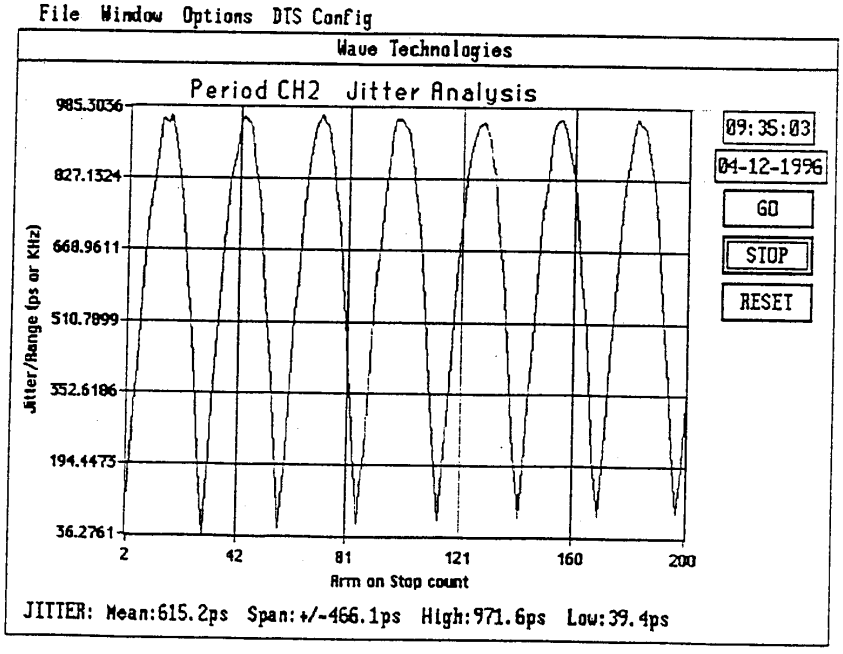
Oscilloscope Analysis--2XQ Period Jitter
(19.5 Mhz In, Vcc=5.00v, Supplier B OLD)

PLOT 20



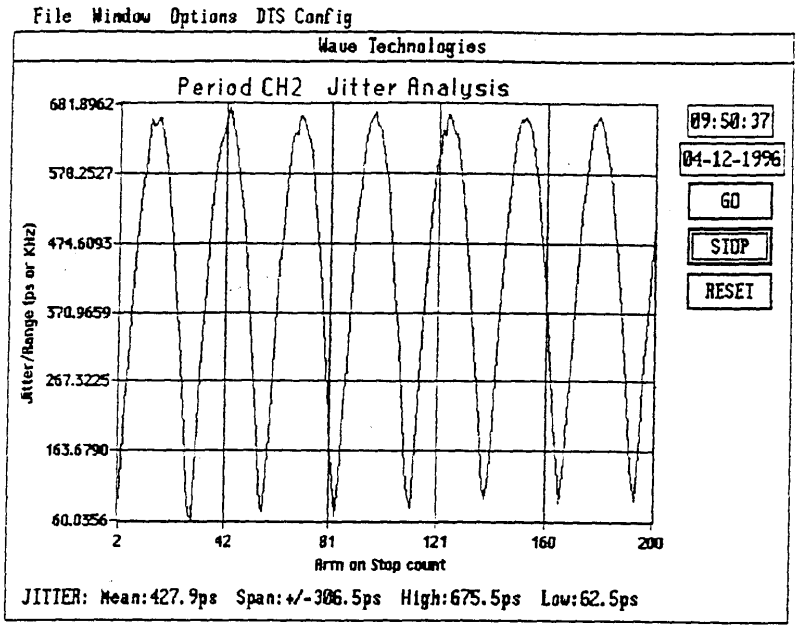
Jitter Analysis--2XQ Accumulated Period Jitter
(19.5 Mhz In, Vcc=4.50v, Supplier B OLD)

PLOT 21



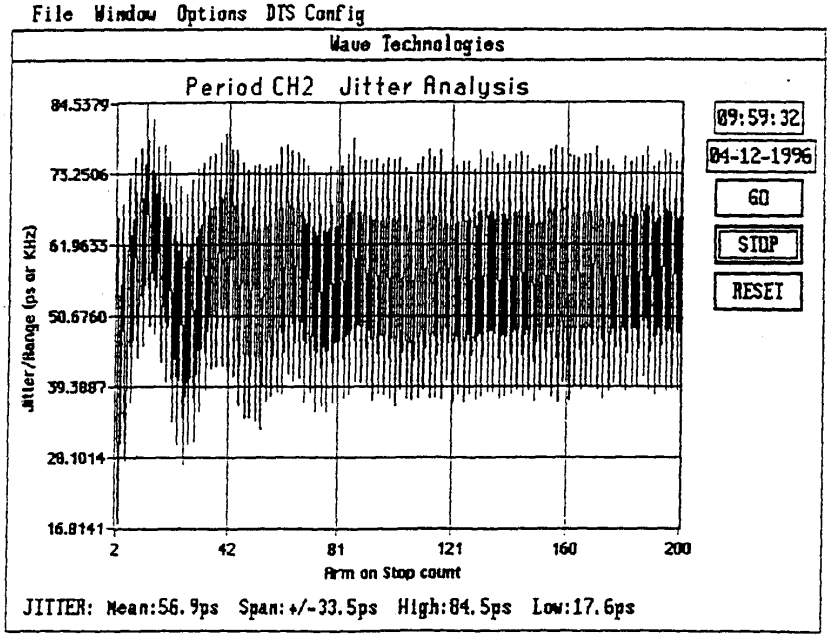
Jitter Analysis--2XQ Accumulated Period Jitter
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 22



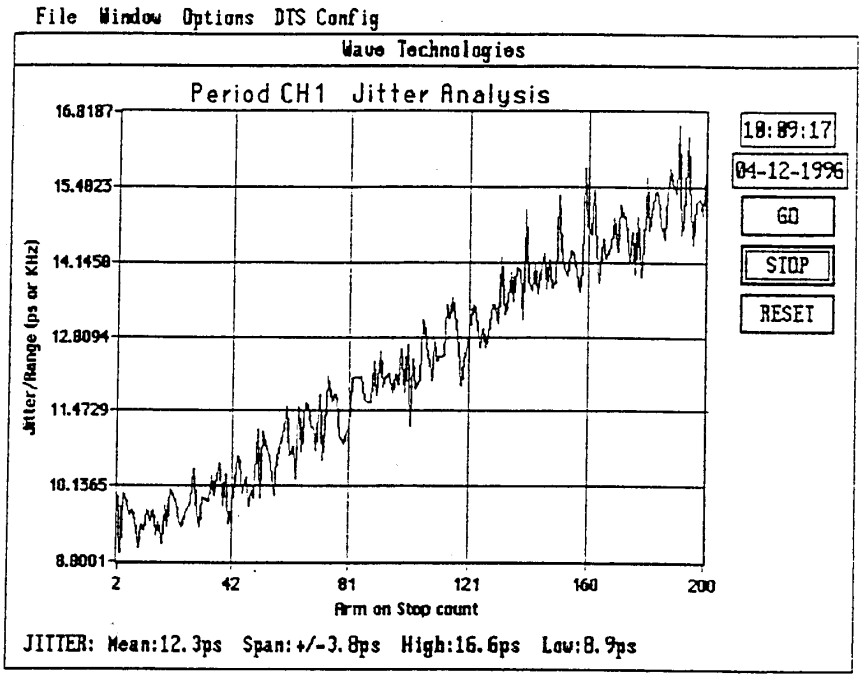
Jitter Analysis--2XQ Accumulated Period Jitter
(19.5 Mhz In, Vcc=5.00v, Supplier B OLD)

PLOT 23



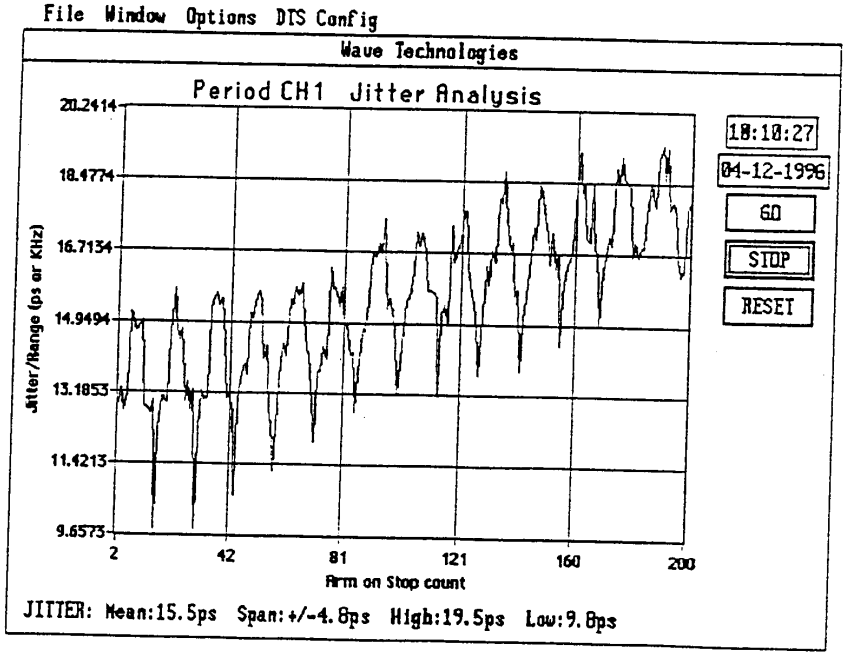
Jitter Analysis--2XQ Accumulated Period Jitter
(19.5 Mhz In, Vcc=5.25v, Supplier B OLD)

PLOT 24



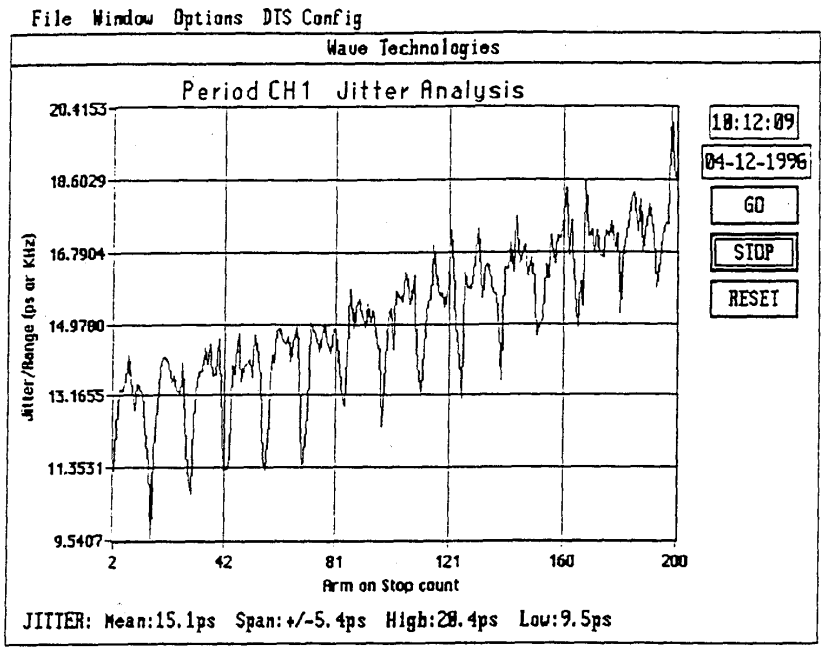
Jitter Analysis–Input Reference Accumulated Period Jitter
(19.5 Mhz In, Vcc=4.50v, Supplier B OLD)

PLOT 25



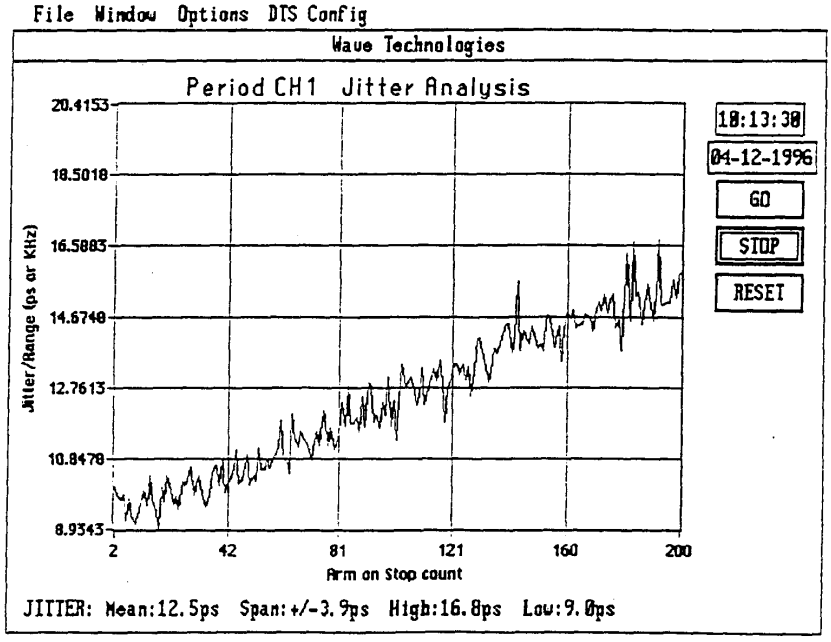
Jitter Analysis–Input Reference Accumulated Period Jitter
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 26



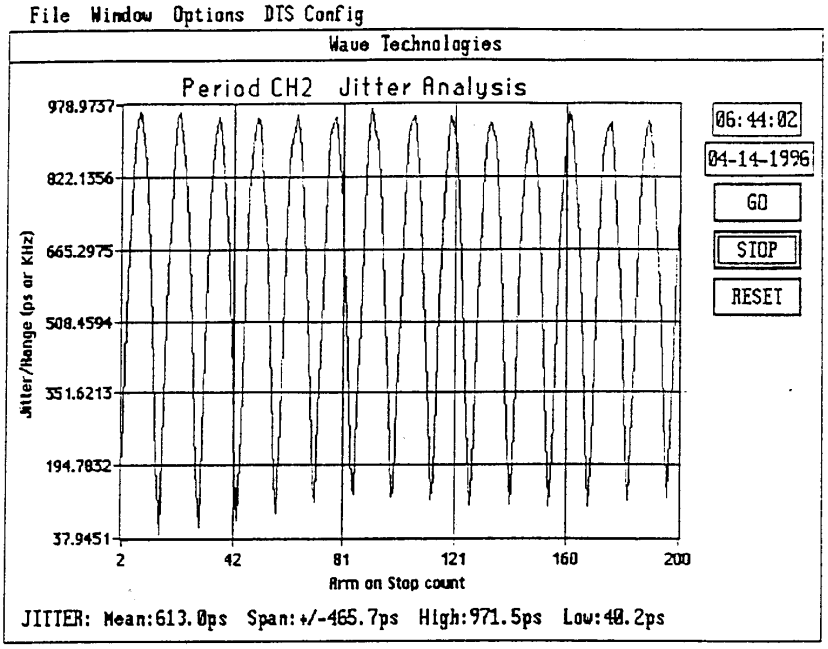
Jitter Analysis--Input Reference Accumulated Period Jitter
(19.5 Mhz In, Vcc=5.00v, Supplier B OLD)

PLOT 27



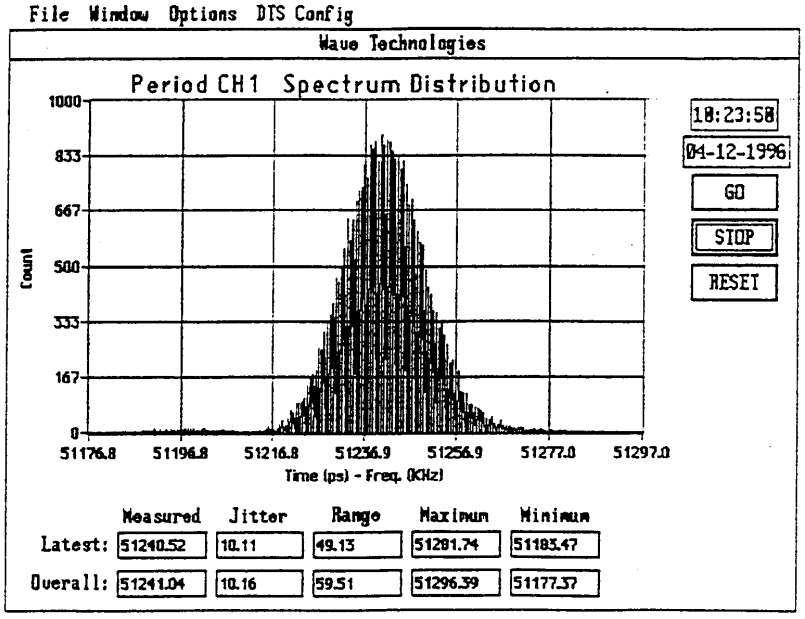
Jitter Analysis--Input Reference Accumulated Period Jitter
(19.5 Mhz In, Vcc=5.25v, Supplier B OLD)

PLOT 28



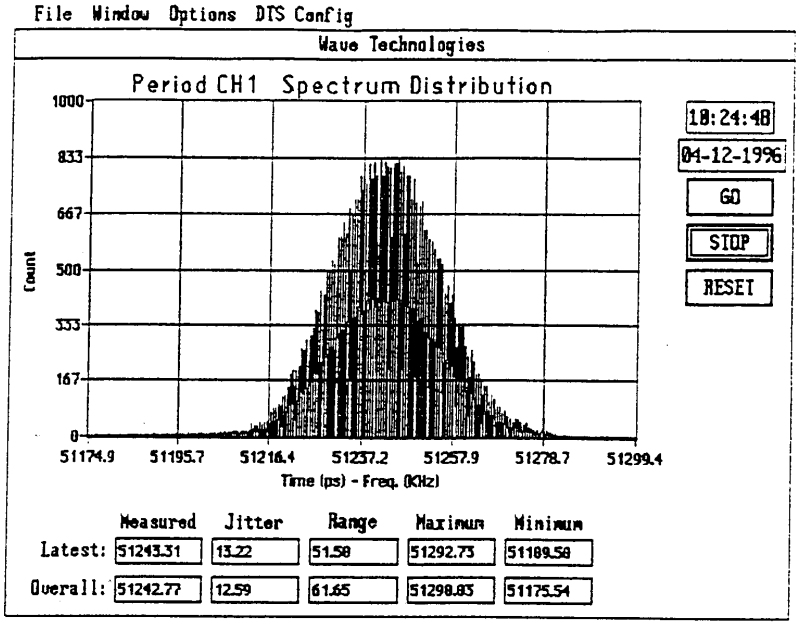
Jitter Analysis--Q4 Accumulated Period Jitter
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 29



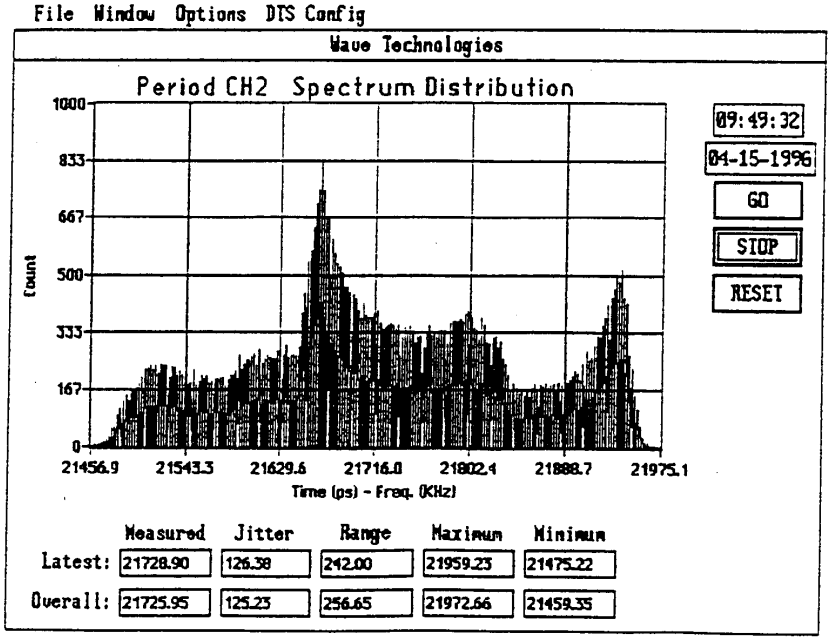
Spectrum Analysis--Input Reference Period Jitter
(19.5 Mhz In, Vcc=4.50v, Supplier B OLD)

PLOT 30



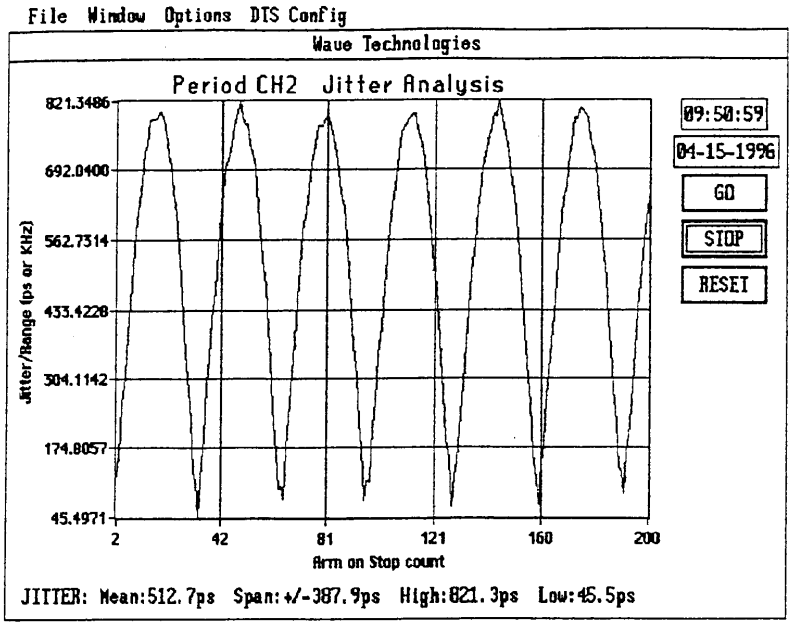
Spectrum Analysis--Input Reference Period Jitter
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 31



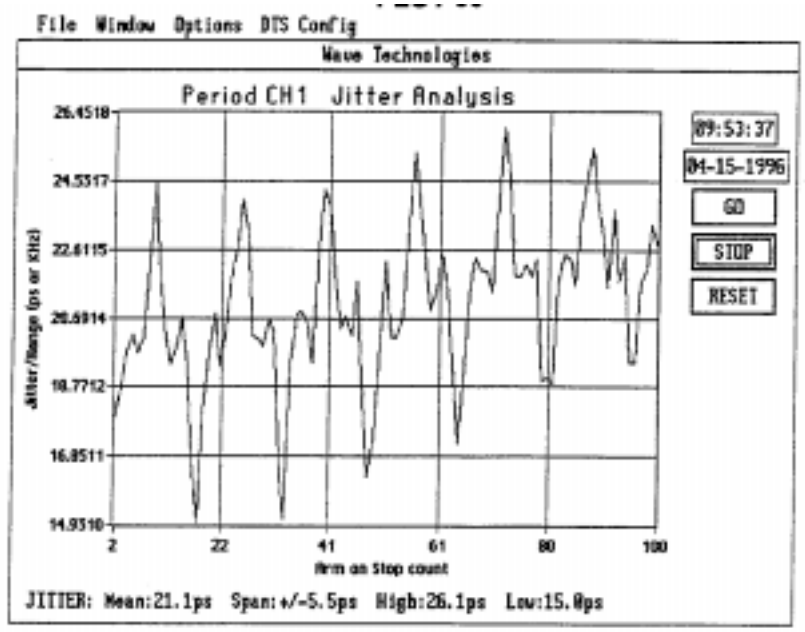
Spectrum Analysis--2XQ Period Jitter
(23 Mhz In, Vcc=5.00v, Supplier B NEW)

PLOT 32



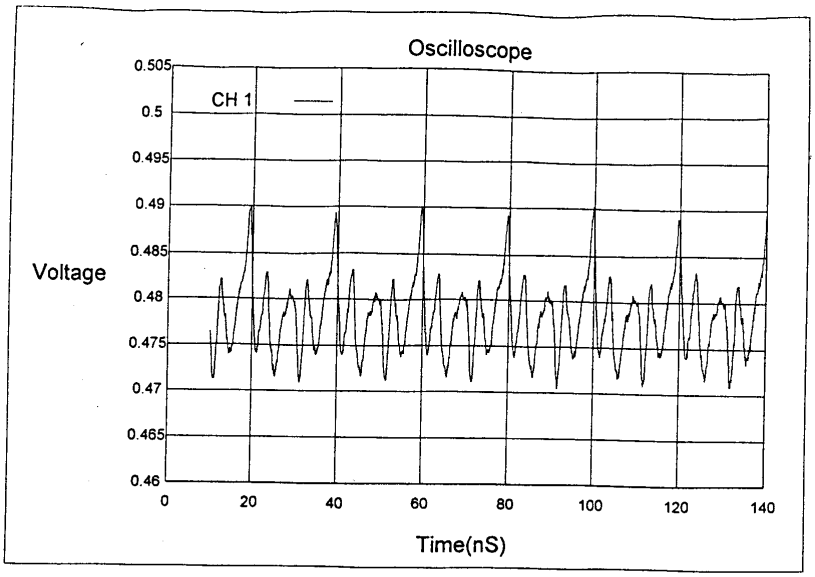
Jitter Analysis--2XQ Accumulated Period Jitter
(23 Mhz In, Vcc=5.00v, Supplier B NEW)

PLOT 33



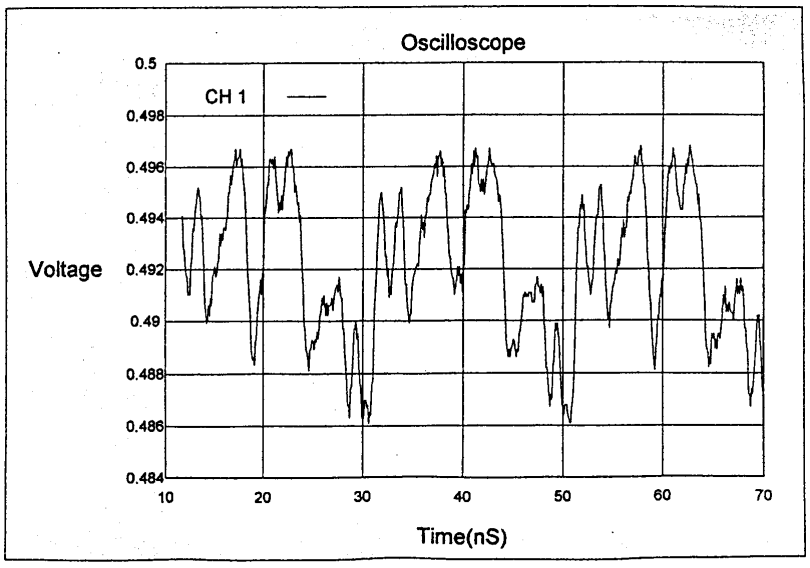
Jitter Analysis--Input Reference Accumulated Period Jitter
(23 Mhz In, Vcc=5.00v, Supplier B NEW)

PLOT 34



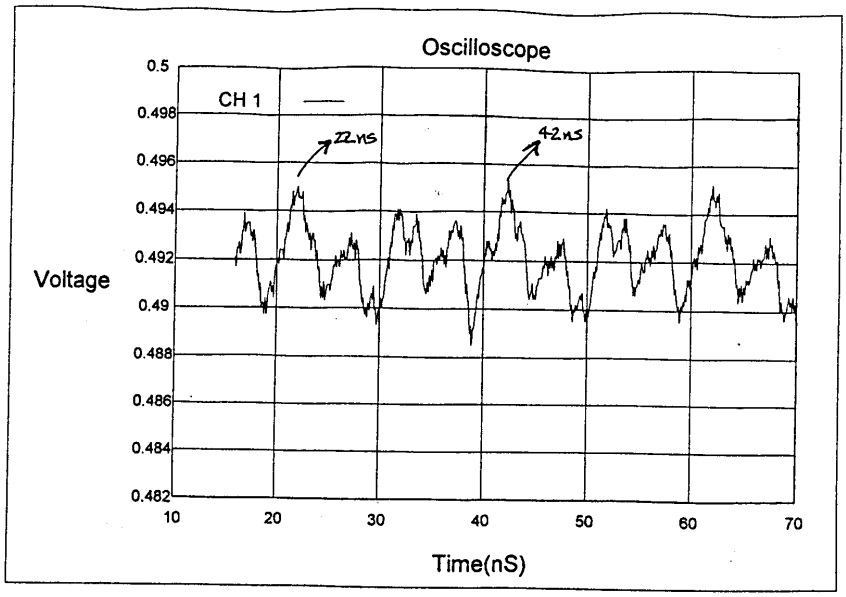
Oscilloscope Analysis--Pin 8 Vcc Noise
(50 Mhz In, Vcc=5.00v, Supplier A)

PLOT 35



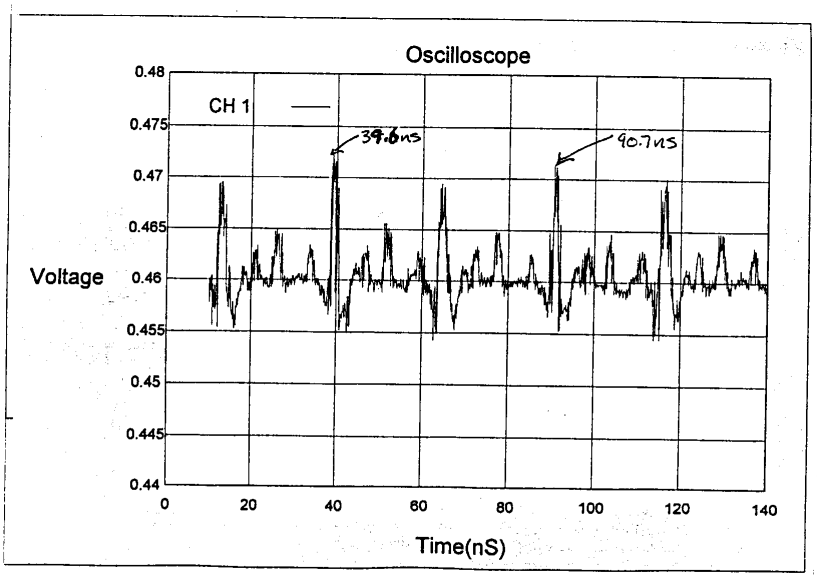
Oscilloscope Analysis--Pin 27 Vcc Noise, GND Position 1
(50 Mhz In, Vcc=5.00v, Supplier A)

PLOT 36



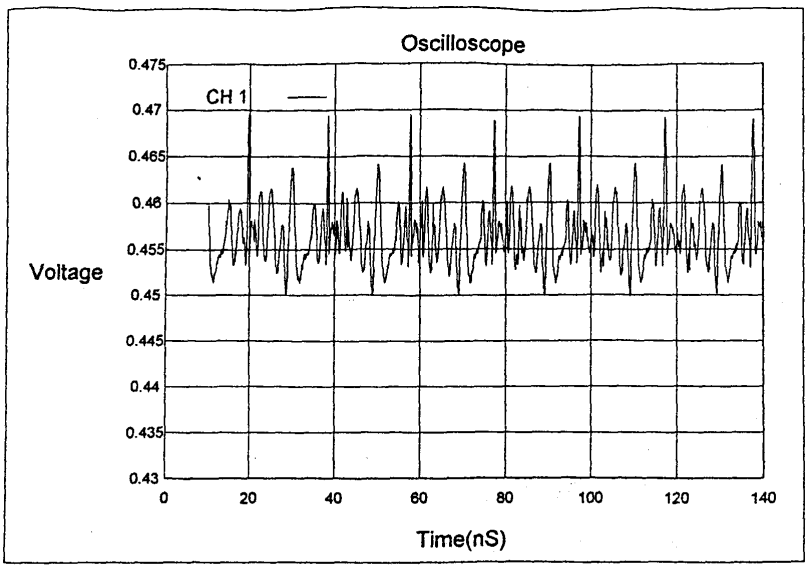
Oscilloscope Analysis--Pin 27 Vcc Noise. GND Position 2
(50 Mhz In, Vcc=5.00v, Supplier A)

PLOT 37



Oscilloscope Analysis--Pin 8 Vcc Noise
(19.5 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 38



Oscilloscope Analysis--Pin 8 Vcc Noise
(50 Mhz In, Vcc=4.75v, Supplier B OLD)

PLOT 39

WAVECREST Corporation
World Headquarters
7275 Bush Lake Road
Edina, MN 55439
(612) 831-0030
FAX: (612) 831-4474
Toll Free: 1-800-733-7128
www.wavecrestcorp.com

WAVECREST Corporation
West Coast Office:
1735 Technology Drive, Suite 400
San Jose, CA 95110
(408) 436-9000
FAX: (408) 436-9001
1-800-821-2272

200121-01 REV A