# Keysight Technologies
DDR4 Functional/Protocol Debug and Analysis Reference Solution

Solution Brochure

When DDR4 memory systems don't behave as expected, Keysight's DDR4 functional/protocol debug and analysis solution provides trace capture and analysis, enabling the insight needed to understand system behavior and get to the root cause of system issues.

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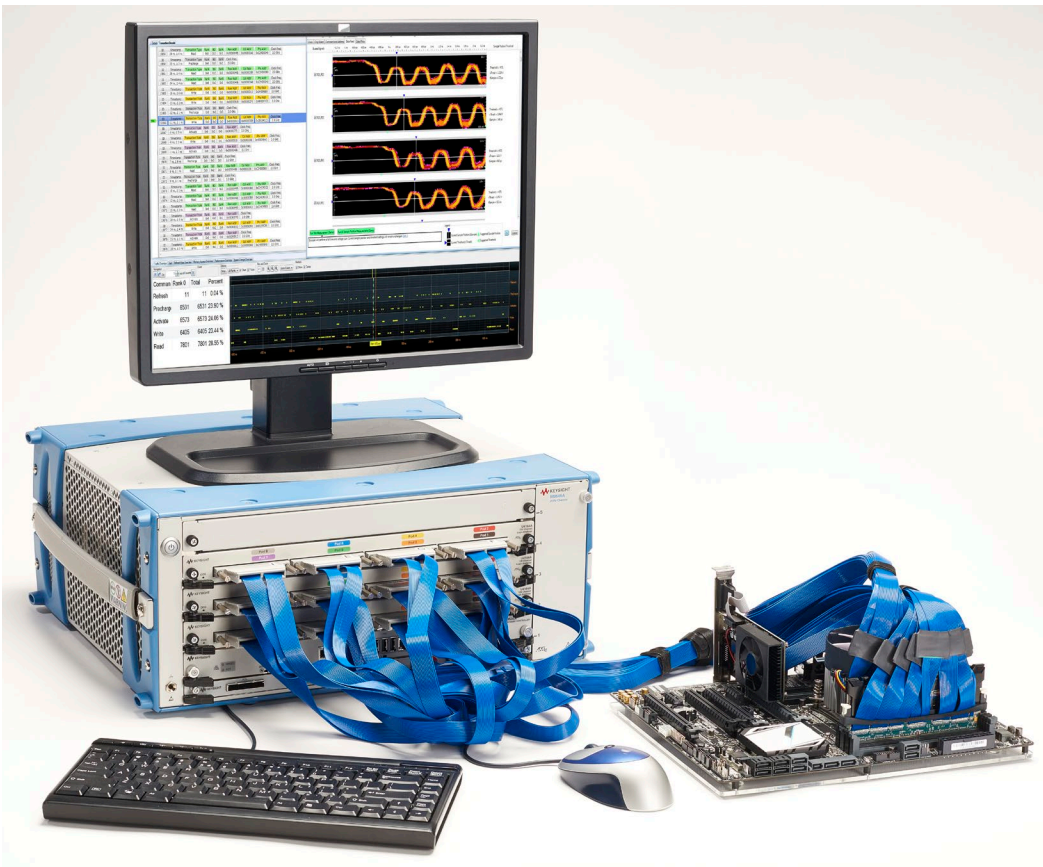
Unlocking Measurement Insights

Next-Generation DDR4 Test Challenges

System and memory designers implementing DDR4 are striving for innovations in performance, density and power efficiency in their systems. Reliable measurements and analysis enable market-changing innovations and rapid fault isolation by providing insight into actual system behavior.
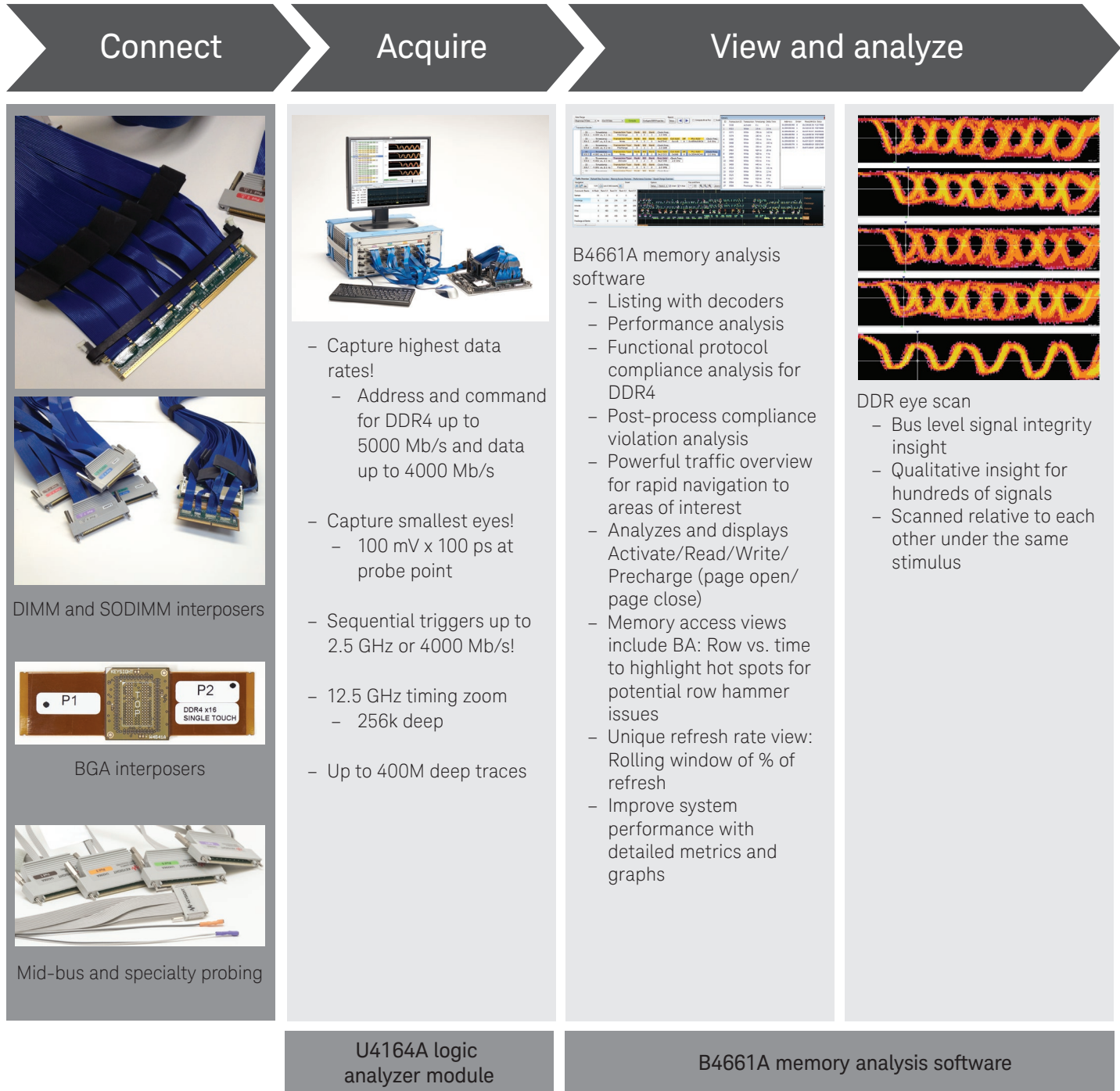
Using Keysight's DDR4 functional/protocol debug and analysis solution to address DDR4 test challenges

Keysight's DDR4 functional/protocol debug and analysis reference solution is the industry's only functional/protocol validation, debug, analysis and bus level signal integrity insight solution covering address/command and data for DDR4 systems operating at data rates up to and including 4000 Mb/s.

Solution feature	Benefit
Proven capture of DDR4 Read/ Write data at 4000 Mb/s	Follow the signal flow on DDR4 memory systems to isolate issues – Memory write back issues, initialization issues, system crashes, and system abnormalities – Visibility to all Address, Command and Data (Address/Command up to 5000 Mb/s data rates)
100 ps by 100 mV minimum eye requirement at probe point	Reliable capture on the smallest eye openings. No other logic analyzer can capture eyes this small
2.5 GHz trigger sequencer with burst trigger option	Capture sequential up to 2.5 GHz. Capture up to 32 sequential events using Keysight's exclusive burst trigger. Competition triggers at 750 MHz, which is inadequate for DDR/LPDDR above 1500 Mb/s
Exclusive quad sample mode (Option U4164A-02G)	Maximum signal access at highest data rates from one probe point
	Allows simultaneous capture of Read/Write data at two different thresholds at rates up to 4000 Mb/s from a single probe load
Extensive memory analysis software (B4661A) makes your job easier	Debug, improve performance, and validate protocol compliance
	DDR2/3/4 decoder/transaction viewer

	Functional protocol compliance analysis for DDR4
	  – Post-process compliance violation analysis
	    – Protocol compliance violation testing across speed changes
	    – Click to jump to worst violation or to mark violations
	    – Margin information on violations
	  – Real-time compliance violation analysis triggers on violations to identify elusive DDR4 system violations
	  – User-defined regression tests for any logic analyzer configuration on any bus

	Performance overview and analysis
	  – Powerful traffic overview for rapid navigation to areas of interest
	  – Analyzes and displays Activate/Read/Write/Precharge (page open/ page close)
	  – Memory access views include BA: Row vs. time to highlight hot spots for potential row hammer issues
	  – Unique refresh rate view: rolling window of % of refresh
	  – Improve system performance with detailed metrics and graphs

	Bus level signal insight – Qualitative eye scans (up to hundreds of signals) using DDR eye scan

	Ease-of-use to minimize set up and analysis time
	  – DDR setup assistant: Simplifies state mode measurement setup to minutes
	  – DDR configuration creator enables users to create custom mid-bus or BGA configurations in minutes using an interactive graphical interface

DIMM, SODIMM, universal footprint, and BGA probing	Allows you to connect to any DDR4 system under test for functional compliance validation, debug, and bus level signal integrity insight
Timing zoom	Provides 256k high-resolution (12.5 GHz) timing measurements simultaneous with full memory depth state or timing measurements from single probe point

Reference Solution Architecture

Accelerate DDR4 Insight using the U4164A

Connect	Acquire	View and analyze

DIMM and SODIMM interposers

BGA interposers

Mid-bus and specialty probing

– Capture highest data
  rates!
    – Address and command
      for DDR4 up to
      5000 Mb/s and data
      up to 4000 Mb/s

– Capture smallest eyes!
    – 100 mV x 100 ps at
      probe point

– Sequential triggers up to
  2.5 GHz or 4000 Mb/s!

– 12.5 GHz timing zoom
    – 256k deep

– Up to 400M deep traces

B4661A memory analysis
software
   – Listing with decoders
   – Performance analysis
   – Functional protocol
     compliance analysis for
     DDR4
   – Post-process compliance
     violation analysis
   – Powerful traffic overview
     for rapid navigation to
     areas of interest
   – Analyzes and displays
     Activate/Read/Write/
     Precharge (page open/
     page close)
   – Memory access views
     include BA: Row vs. time
     to highlight hot spots for
     potential row hammer
     issues
   – Unique refresh rate view:
     Rolling window of % of
     refresh
   – Improve system
     performance with
     detailed metrics and
     graphs

DDR eye scan
   – Bus level signal integrity
     insight
   – Qualitative insight for
     hundreds of signals
   – Scanned relative to each
     other under the same
     stimulus

U4164A logic analyzer module	B4661A memory analysis software

– Connect to your system by selecting probing specific to your device under test.
– Aquire trace captures using the U4164A module(s) in an M9502A/05A chassis with a host
  controller. The number of U4164A modules and options for the modules varies depending
  on the probing and data rate required.
– View and analyze the B4661A memory analysis software.

1. For a more complete set of configuration options and examples, please refer to the DDR4 Functional/
    Protocol Debug and Analysis Reference Solution Configuration Guide, literature number 5992-1539EN.

Hardware

Instruments

### U4164A logic analyzer module
www.keysight.com/find/u4164a

The U4164A logic analyzer system combines reliable data capture with powerful analysis and validation tools to enable you to quickly and confidently validate and debug high-speed digital designs operating at speeds up to 4 Gb/s. The U4164A logic analyzer module delivers unique capabilities that enable you to make measurements and achieve levels of insight not available with other logic analyzers.

M9502/05A AXIe 2-5 slot chassis
www.keysight.com/find/m9502a

The M9502/05A AXIe chassis is fully compatible with the AXIe 1.0 specification. It includes an embedded system module (ESM) that does not take up an instrument slot. This system module performs the chassis management functions contained in the AXIe specification. Additionally, it provides PCI and LAN interfaces for connection to an external computer, external clock and trigger connectors, and Keysight-exclusive, inter-chassis synchronization connectors. The local bus implemented in the M9502/05A provides the maximum 62 pairs allowed by the AXIe specification. Combine the M9502/05A with the M9048A PCIe desktop adaptor to achieve the highest system bandwidth.
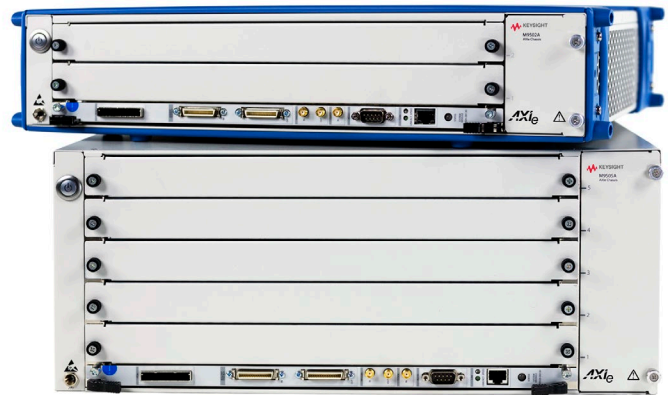
M9536A AXIe embedded controller
www.keysight.com/find/m9536a

The Keysight M9536A is the first AXIe embedded controller available on the market. It provides a high-performance PCIe Gen2 link to the AXIe backplane and is a powerful one-slot computer that can be used to build compact AXIe systems. It easily integrates into hybrid test systems using GP-IB, USB, and LAN due to the built-in front panel interfaces.

Hardware – Probing

DDR4 DIMM and SODIMM interposers are available through Keysight.

Contact your Keysight representative to order the interposer for your system under test. Visit: **www.keysight.com/find/contactus**.

FS2510AB DDR4 DIMM and FS2512 DDR4 SODIMM interposers offer:
– Ease of connection
– Direct connect to U4164A
– Low profile - Minimal loading
– Support of UDIMM or RDIMM
– Timing and state analysis
– Compatible with DDR setup assistant and DDR eye scan

W4640 Series BGA probes
www.keysight.com/find/w4641a
www.keysight.com/find/w4643a

The W4640A series DDR4 BGA interposers enable probing of embedded memory DRAM from the ball grid array with Keysight logic analyzers. The W4640A Series DDR4 BGA interposers are designed to take full advantage of quad sample state mode on U4164A modules with U4164A-02G option, requiring only a single probe point for up to four samples at two different thresholds.
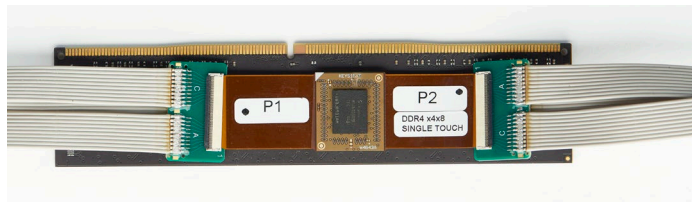
U4208/09A probe/cable, 61-pin ZIF, 160-pin direct connect
www.keysight.com/find/u4208a

The U4208A/09A probe/cables have a 61-pin ZIF probe connector on one end of the cable and two 160-pin connectors that connect into the front panel of a U4164A logic analyzer module on the other end of the cable. The U4208A/09A are designed to connect from the left/right wings of the W4640A Series DDR4 BGA interposer directly into the U4164A logic analyzer. The U4164A logic analyzer will be in normal state mode for the address and command signal capture and in quad sample state mode for the data signal capture. Default configurations for the W4640A Series DDR4 BGA interposers and U4208A/09A probe/cables are included at no charge in the standard download package of the B4661A memory analysis software.

For a more complete set of probing options, please refer to the DDR4 Functional/Protocol Debug and Analysis Reference Solution Configuration Guide, literature number 5992-1539EN and the Keysight Technologies Probing Solutions for Logic Analyzers Data Sheet, literature number 5968-4632E.

Software

Figure 1. B4661A Option 4FP/TP/NP, performance analysis option, performance overview graph.

The Keysight B4661A memory analysis software offers options that include the industry's first protocol compliance violation testing capability across speed changes, a condensed traffic overview for rapid navigation to areas of interest in the logic analyzer trace, powerful performance analysis graphics, and DDR and LPDDR decoders. With the B4661A memory analysis software and a Keysight logic analyzer, users can monitor DDR4 systems to debug, improve performance, and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.
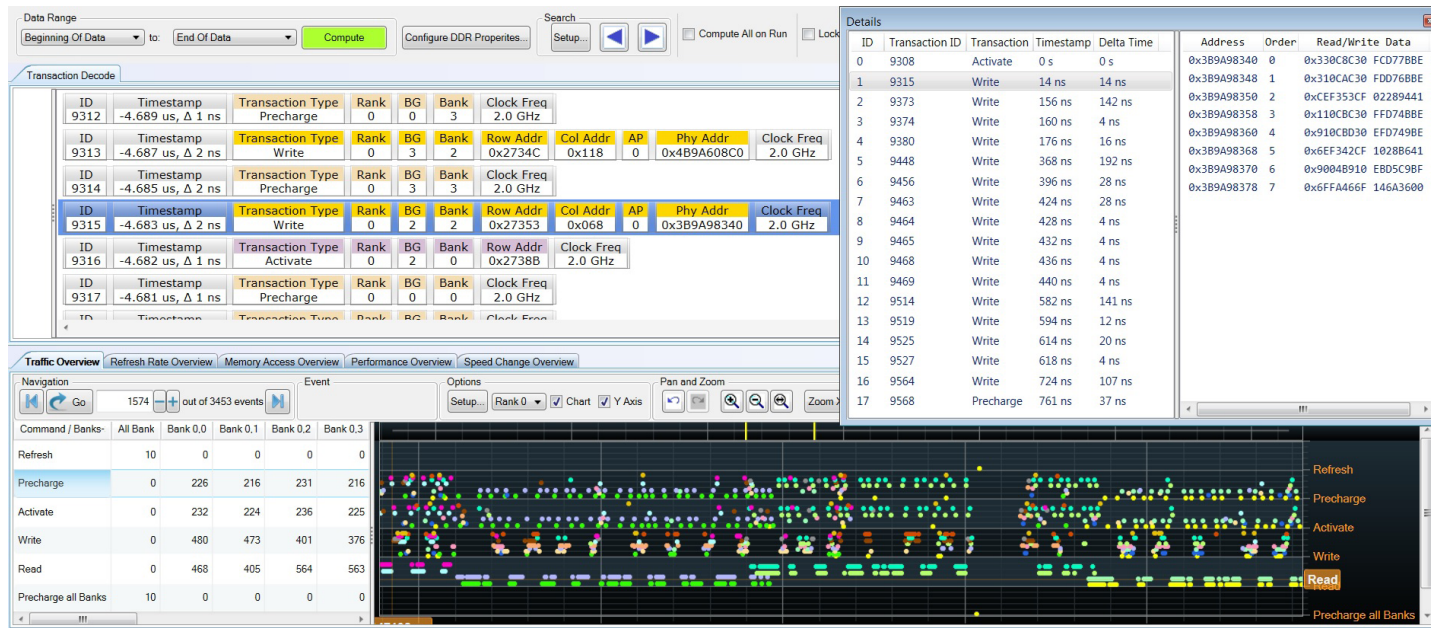

Figure 2. B4661A Option 4FP/TP/NP, performance analysis option, transaction decoder, details tab showing open/closed page commands with data for specific write command and traffic overview calculations and graph of command activity.

Software (Continued)

The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

Standard software features
  – Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers
  – DDR setup assistant
  – DDR eye finder/eye scan
 – DDR configuration creator

B4661A licensed software options:

Software capability	License type		
Determine the function(s) you need ↓ Determine the license type you need →	Node (-xFP)	Transportable (-xTP)	Server/floating (-xNP)
Intersection of row/column gives full option number ↘			
DDR decoder with physical address trigger tool (–1xx)	B4661A-1FP	B4661A-1TP	B4661A-1NP
LPDDR decoder (–2xx)	B4661A-2FP	B4661A-2TP	B4661A-2NP
DDR and LPDDR compliance violation analysis (–3xx)	B4661A-3FP	B4661A-3TP	B4661A-3NP
DDR3/4 and LPDDR2/3/4 performance analysis (–4xx)	B4661A-4FP	B4661A-4TP	B4661A-4NP

You can order any combination and/or quantity of the B4661A licensed options.

Recommended Reference Solution Configuration For: DDR4 DIMM System Under Test [2]

DDR4 DIMM Solution for DDR4 ADD/CMD/Data capture up to 4000 Mb/s
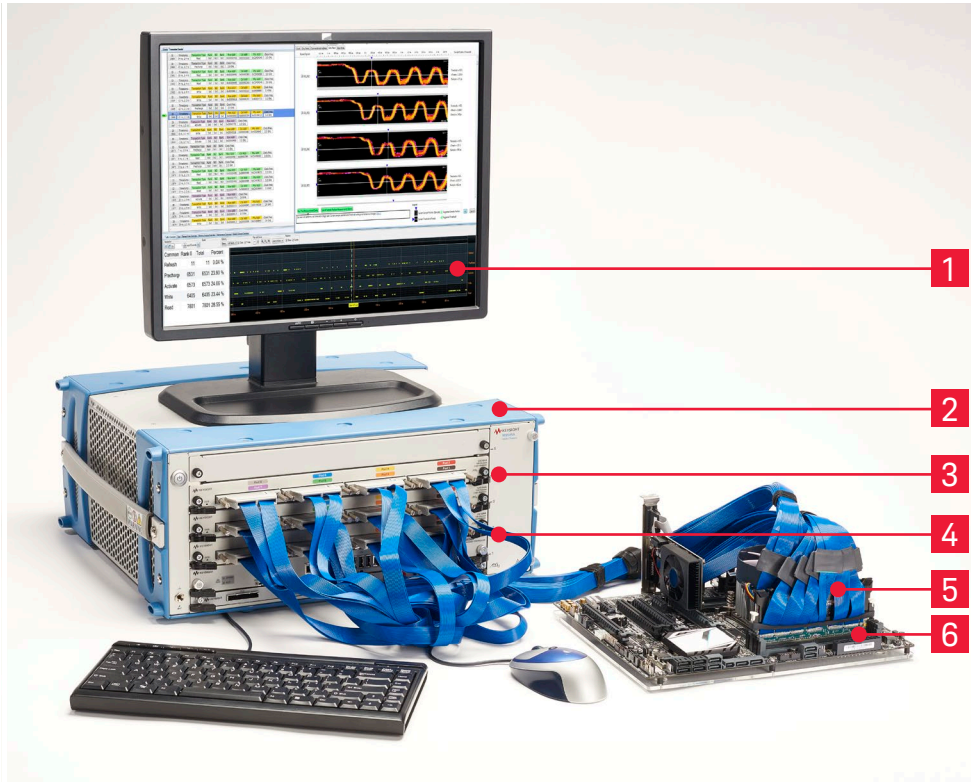
1. User-supplied monitor

2. M9505A five-slot chassis (qty 1)

3. U4164A logic analyzer module (qty 3)

4. M9536A embedded controller running logic analyzer and B4661A software (qty 1)

5. FS2510AB DDR4 DIMM interposer with FS1070 conversion for use with three modules (qty 1)

6. Device under test

Hardware

Model	Quantity	Description
U4164A	3	136-channel logic analyzer module
U4164A-02G	3	Speed grade option for 2.5 GHz clocking and 4 Gb/s data capture
U4164A-008	3	Increase acquisition memory depth to 8 Mb
PS-X10-750-3PH	1	Interposer FS2510AB DDR4 288-pin DIMM accessory for logic with FS1070 conversion kit for operation over 2500 Mb/s
M9505A	1	5-slot AXIe-based chassis
M9536A	1	Embedded controller

Software

Model	Quantity	Description
Version 6.20 or higher	1	Keysight's logic and protocol analyzer software (64-bit)
B4661A	1	Memory analysis software
B4661A-1FP	1	DDR decoder with physical address trigger tool, fixed perpetual license
B4661A-3FP	1	DDR and LPDDR compliance violation analysis, fixed perpetual license
B4661A-4FP	1	DDR3/4 and LPDDR2/3/4 performance analysis, fixed perpetual license

2. For a more complete set of configuration options, please refer to the DDR4 Functional/Protocol Debug and Analysis Reference Solution Configuration Guide, literature number 5992-1539EN.

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www.lxistandard.org

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