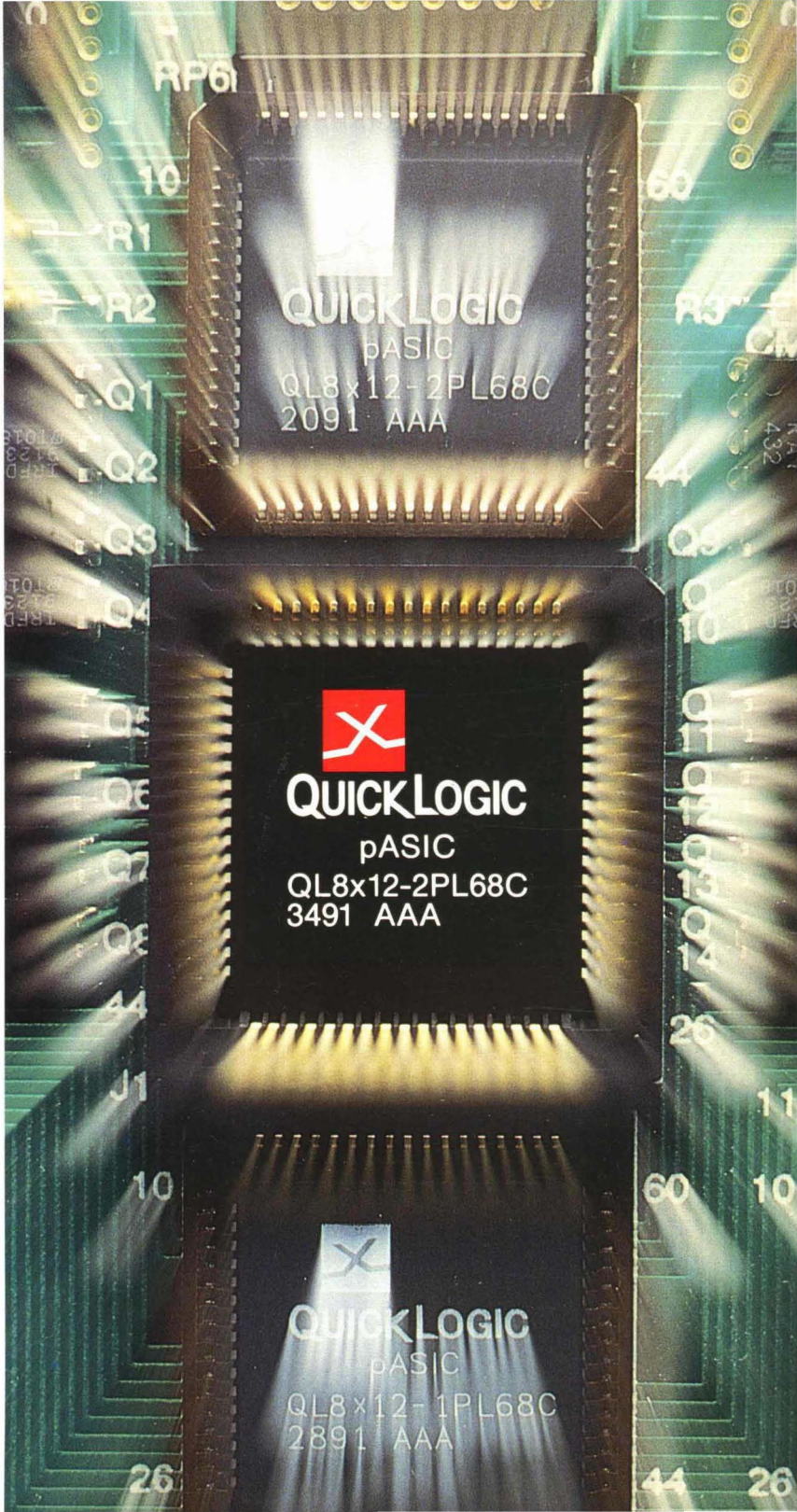
QUICKLOGIC

FPGA DATA BOOK

1992

VERY HIGH SPEED FPGAS

1992 DATA BOOK



QUICKLOGIC

Very-High-Speed FPGAs

General Information

FPGA Data Sheets

CAE Design Tools

Application Notes

Quality, Reliability, and Packaging Information

Sales Representatives and Distributors

QuickLogic Corporation
2933 Bunker Hill Lane
Santa Clara, CA 95054

General Information (408) 987-2000
Applications Hotline (408) 987-2037
FAX: (408) 987-2012

LIFE SUPPORT POLICY

QuickLogic's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and the President of QuickLogic.

1. Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or affect its safety or effectiveness.

QUICKLOGIC

QuickLogic Corporation
2933 Bunker Hill Lane
Santa Clara, CA 95054
Tel: 408-987-2000
Fax: 408-987-2012

USERS AGREE THAT QUICKLOGIC DELIVERS THE FASTEST FPGAs

"The entire industry has been waiting for an FPGA that delivers the speed QuickLogic claims. Plenty of start-ups have claimed to be fast, routable and predictable - and each one has disappointed me. But not this time. We've installed the QL8x12 in a real system, replacing several 7ns and 10ns PALs. The part works just as you would expect from the data sheet."

Jack Regula
Hardware Engineering Manager
Force Computers Inc.

"There is little doubt that this is the fastest FPGA on the market. You don't need to invest lots of training hours to get great functionality and amazing speed - and you get this without having to waste valuable design time on tedious manual intervention."

Michael Dini
Design Consultant
San Diego

"These people designed their tools as though they had to use them themselves....even the first time user has some fluency in navigating around the system. After some initial performance checking, I can see that the FPGAs will actually deliver the performance the company claims for itself."

George Morrow
VP Engineering
Intelligent Access Corp.

"I have found the tools to be powerful, easy to use and efficient to design with. I have also found QuickLogic's pASIC architecture to readily accommodate a wide variety of designs with surprising performance characteristics."

Roger C. Alford
Author
Programmable Logic Designer's Guide

"I did the entire design for four QuickLogic parts over a single weekend. We have other EPLD and FPGA tools in-house... the speed criteria eliminated most of the choices. QuickLogic is a great solution for people needing high speed and low power."

Stewart J. Dunn
VP Research and Development
Datacube Inc.

"Even without programming logic into the other FPGAs, getting on and off the daughter cards took 45 - 50 ns. With QuickLogic, the I/O delay fell to 9 ns, and we could preserve all the performance of the (previous) design."

John Thomas
Director of Sales and Marketing
Universal Computing

"QuickLogic offers a great way to implement very fast state machines in an easy-to-use part."

Brian Fenstermacher
Design Engineer
Performance Controls

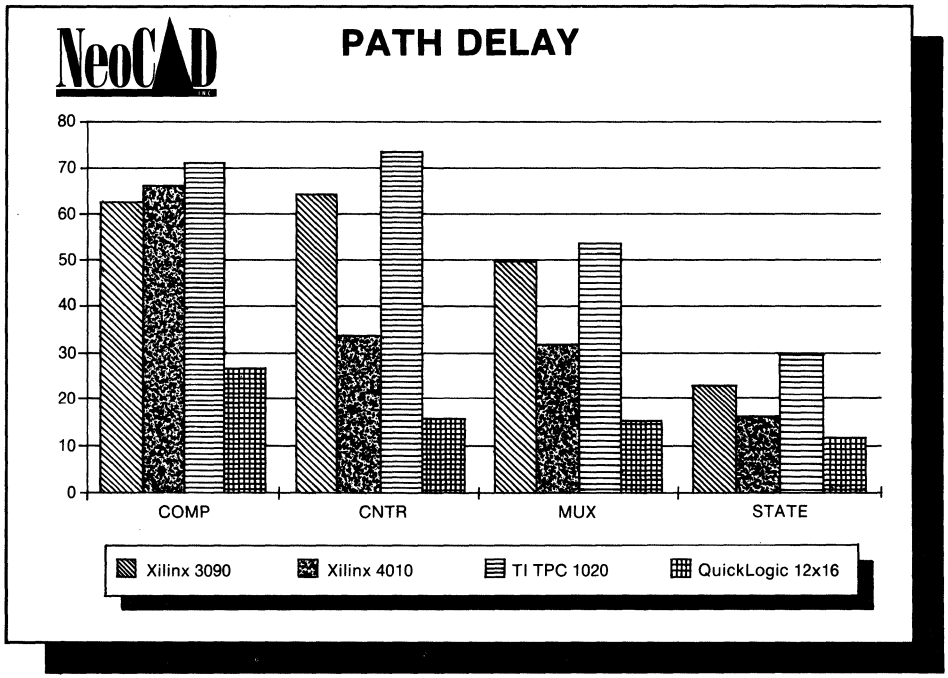
THIRD-PARTIES AGREE THAT QUICKLOGIC DELIVERS THE FASTEST FPGAs

Device Performance Evaluation

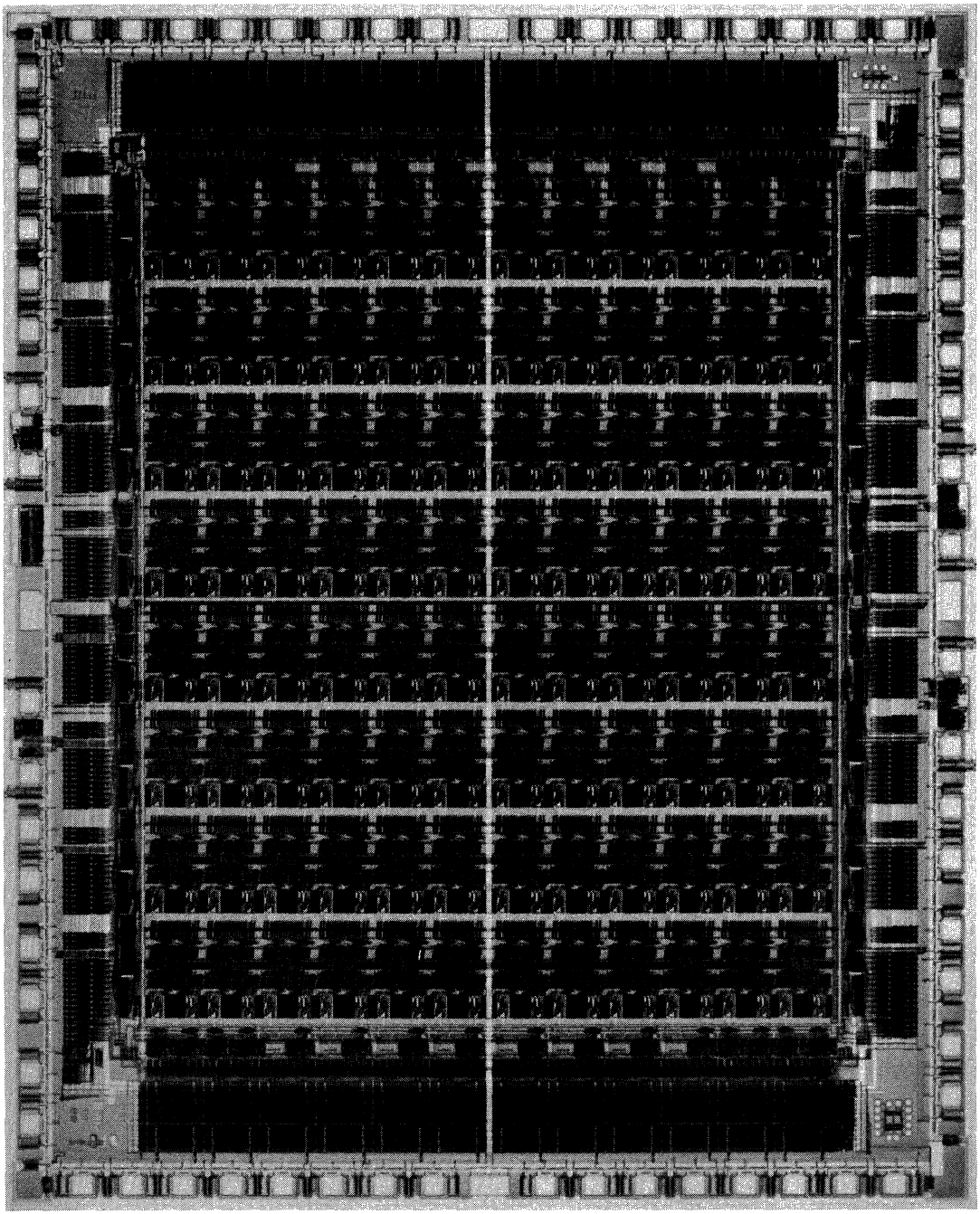
UART Design

Architecture	Area	Speed	Device
Actel Act2	160 logic	90 ns	1225
QuickLogic pASIC	122 "gates"	29 ns	QL8x12
Xilinx 4000	93 CLBs	6 levels	4005

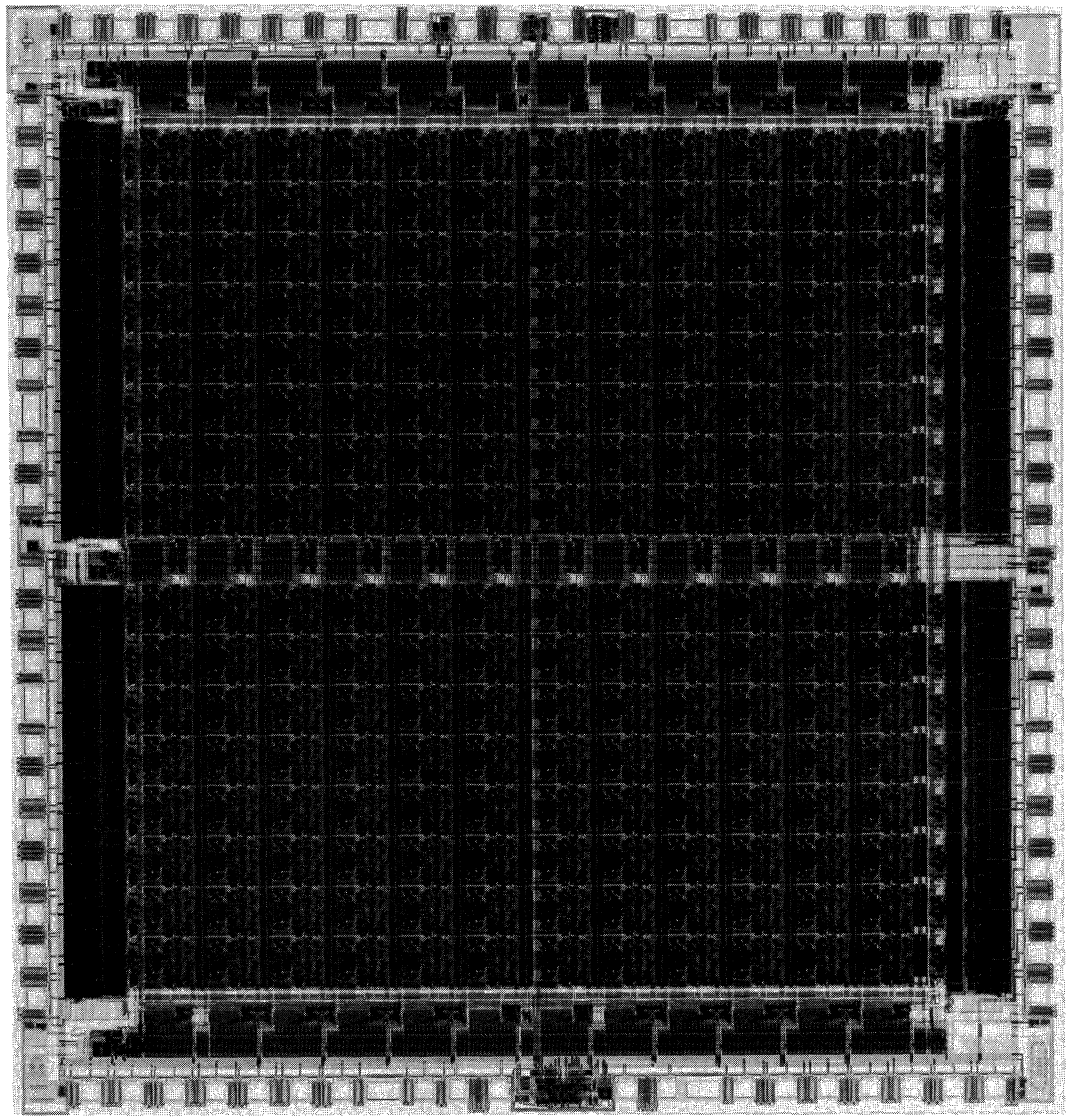
This data was presented by Exemplar Logic Inc. of Berkeley, CA for the 1992 PLD conference and shows that the QuickLogic QL8x12 is **3x** the speed of Actel's fastest ACT2 device. Xilinx will also be slow, but must be fully routed to generate precise results.



NeoCAD, Inc of Boulder, CO offers a generic FPGA place and route tool that supports QuickLogic, Actel, and Xilinx. NeoCAD showed the results of using their tool on 4 simple logic functions; comparator, counter, multiplexer, and state machine. The data was presented at the 1992 ASIC and EDA sponsored IDEA conference.



The QuickLogic QL8x12 - 1000 usable gate Very-High-Speed FPGA features 96 logic cells in an 8 by 12 matrix. It is equivalent in capacity to many so called 3000 gate EPLD and LCA™ devices.



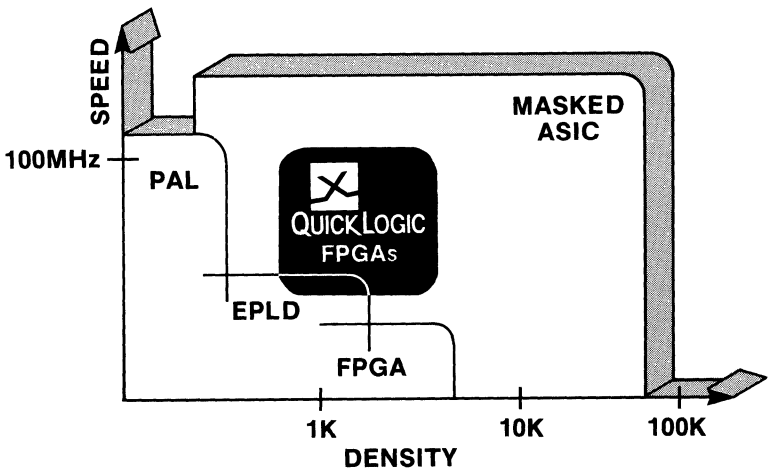
The QuickLogic QL12x16 - 2000 usable gate Very-High-Speed FPGA delivers "real-world" Operating Performance above 100 MHz.

Very-High-Speed FPGAs Through Technology, Architecture, and Tools

QuickLogic Corporation provides very-high-speed programmable ASIC solutions for designers of high-performance systems who must get their products to market quickly.

The company was founded by the engineers who invented the PAL device and PALASM software. By offering the ability to create high-speed custom logic circuits with standard off-the-shelf products, their invention revolutionized the world of logic design. First-generation FPGAs extended these benefits to higher levels of density, but at much lower speeds. QuickLogic was formed to create a single solution combining the fast speed of PAL devices with the high density, low power and logic flexibility of FPGAs.

FIGURE 1 Comparative Speed/Density Chart



QuickLogic pASIC 1 Family FPGAs operate at two to three times the usable system speed of first-generation devices.

...FPGAs operating two to three times faster

To achieve these goals, QuickLogic has created a CMOS antifuse technology, called the ViaLink™ element, which couples small size with high speed. It results in FPGAs operating two to three times faster than other technologies using the same process lithography. The small size also provides a technology migration path to 50,000 gates and beyond.

QUICKLOGIC

...can be used in applications with 33, 40 and 50 MHz microprocessors

The first product line from QuickLogic, the pASIC 1™ Family of Very-High-Speed CMOS FPGAs, delivers new levels of speed and density in an easy-to-use product. High-density programmable devices can now be used in data path applications with 33, 40 and 50 MHz microprocessors. And in designs with useful internal logic functions operating at over 100 MHz.

QuickLogic engineers achieve industry-leading performance by addressing the design task through the three aspects of Technology, Architecture, and Tools. In each area they combine a variety of techniques to yield the optimum solution.

Speed Through Technology

- ViaLink direct metal-to-metal antifuse
- Speed-critical links less than 50 ohms
- Standard high-speed CMOS logic process

These features yield both the smallest physical programming element size and fastest interconnect speed of all programmable technologies.

Speed Through Architecture

- Up to 14-input wide gates
- Highly tuned, dedicated register in every logic cell
- Regular and orthogonal interconnect wiring resources

These features provide an architecture optimized for a wide range of high-speed control, data path and general-purpose logic integration applications.

Speed Through Tools

...100% automatic place and route

- Architecture-optimized place and route tools
- Precise timing simulation using actual wire lengths, fanout, and loading
- Rapid design iterations permit design optimization

Users achieve high speed and fast design implementation through 100% automatic place and route tools even on functions using up to 100% of the available logic cells.

SPEED THROUGH TECHNOLOGY

At the heart of every programmable device is an electronic switch for user configuration of specific logic functions. It may be an active device, such as an EPROM cell or an SRAM bit. Or a passive fuse or antifuse element. Two basic electrical characteristics limit the maximum useful operating speed which can be achieved with each approach.

- The capacitance, C, of the programmable element in the OFF (OPEN) state. This determines the capacitive loading effect of unprogrammed elements on metal interconnect wires.
- The resistance, R, of the programmable element in the ON (CLOSED) state. This determines the series resistance of the programmed element when interconnecting wires and logic functions.

The technology with the lowest values of R and C delivers the fastest raw speed to the circuit designer.

Early CMOS programmable ASIC devices using EPROM and SRAM programming elements typically have high resistance values, above 1000 ohms, plus large physical size. Dielectric antifuses improve on both these factors but still cannot yield the performance demanded by today's systems.

ViaLink Antifuses

QuickLogic created the ViaLink antifuse to provide a low-resistance, low-capacitance programmable connection directly from one metal layer to another. The ViaLink element is formed by depositing a very high resistance layer of programmable silicon into a via between the two metal layers of a standard high-volume CMOS gate array process.

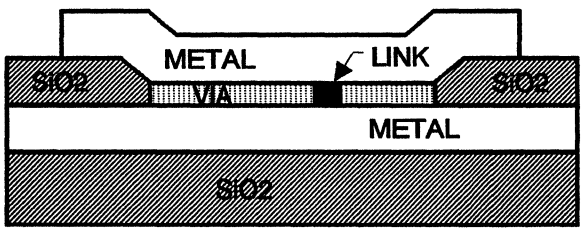


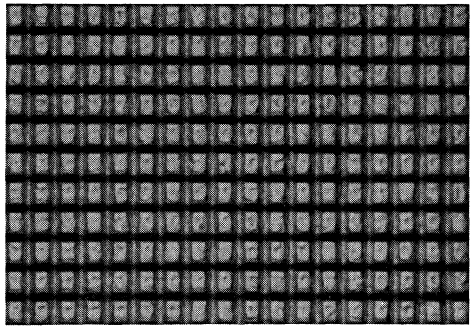
FIGURE 2
ViaLink
Cross Section

The ViaLink element provides a direct metal-to-metal connection.

Selected vias are addressed with a programming voltage. This creates a direct metal-to-metal link by permanently converting the silicon to a low resistance state. Typical resistance is less than 50 ohms.

In one micron process, the size of a ViaLink via is approximately one micron square; or orders of magnitude smaller than active elements. This, coupled with the high dielectric constant of the via material, ensures that unprogrammed ViaLink devices exhibit low capacitive loading (less than 1fF). As the size of the programmed link is physically much smaller than the via, the technology can potentially be scaled below 0.5 microns for future very-high-density applications.

FIGURE 3 Photomicrograph of an Array of ViaLink Elements



A ViaLink antifuse is located at the intersection of every horizontal and vertical wire. Array density is limited by the process lithography, not by the programmable element size.

EPLD AND FPGA TECHNOLOGY COMPARISONS

Programmable Element	SRAM	E/EEPROM	Dielectric Antifuse	ViaLink Antifuse
Typical ON Resistance R	~1000 ohm	~1000 ohm	~500 ohm	~50 ohm
Typical OFF Capacitance C	~50 fF	~15 fF	~5 fF	~1 fF
Physical Size	Very Large	Large	Medium	Small

The ViaLink element delivers the lowest ON resistance, lowest OFF capacitance and smallest physical size of any programmable technology. These characteristics open up a new spectrum of high-speed, high-density applications to programmable devices.

ViaLink Reliability

ViaLink elements have been subjected to accelerated stress testing in both programmed and unprogrammed states. Test results indicate that the ViaLink element has no measurable impact on the reliability of the underlying CMOS process. Product reliability levels in the system environment compare favorably with gate arrays and other FPGAs.

SPEED THROUGH ARCHITECTURE

A simple interconnect architecture, a performance-oriented logic cell, and optimized I/O circuitry maximize the fundamental speed advantage of the ViaLink technology.

Fast, Yet Regular Routing

Early FPGAs employ a variety of wiring types to limit the number of high-resistance connections in a net. For example, signals can be routed through a variety of short lines, long lines, switch boxes and other structures. These irregular routing resources cause unpredictable delay behavior and limit logic utilization.

The low impedance of the ViaLink antifuse allows a regular and orthogonal architecture. The pASIC structure features a matrix of logic cells interconnected by vertical and horizontal routing channels. A ViaLink element located at every wire intersection allows direct, metal-to-metal links between signal lines.

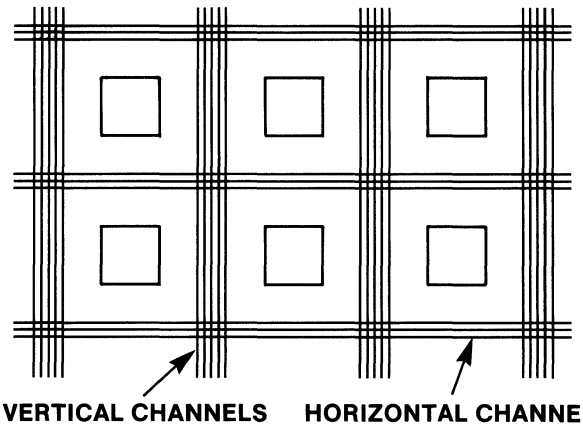


FIGURE 4
pASIC Architecture

A matrix of speed-optimized logic cells is set in a grid of vertical and horizontal wiring channels which can be selectively connected with metal-to-metal links.

According to users (*Computer Design*, 12/91, pg. 78), QuickLogic FPGAs are the closest to masked gate arrays both in predictability and in absolute levels of performance.

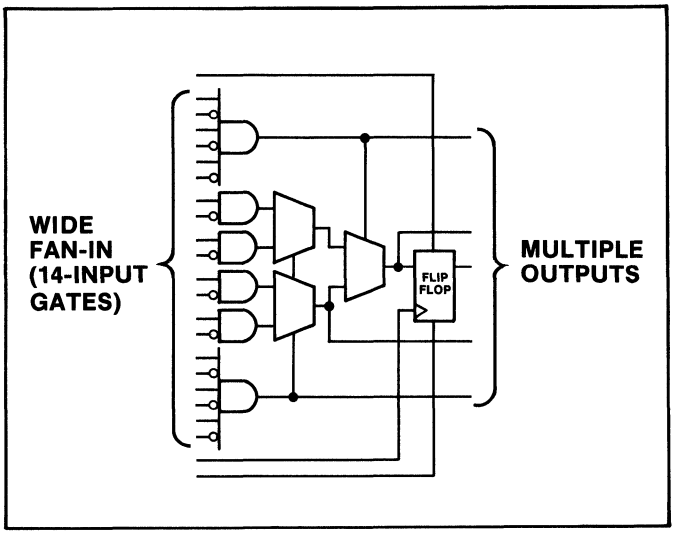
- Delays are "predictable no matter what the layout is."
- "Wire delays are shorter than logic delays."
- As net lengths increase, delays increase proportionally.
- Small design changes result only in small changes in speed.

All these characteristics allow rapid iteration towards the fastest possible solution.

High-Speed Logic Cell

The pASIC logic cell is optimized for high-speed applications. Gates up to 14 inputs wide, multiplexers, decoders and sum-of-products functions can be implemented in a single cell delay with worst case nominal t_{PD} of under 4 ns. Many logic functions therefore incur just half the propagation delay of traditional, narrow fan-in, FPGA logic cell structures.

FIGURE 5 pASIC Logic Cell



The wide fan-in and multiple outputs of the pASIC logic cell permit high-speed logic functions and efficient use of resources.

...16-bit loadable counters operate at over 100 MHz

Each cell includes a dedicated, highly-tuned register element. Flip-flop toggle rates are close to 200 MHz; simple Johnson counters run at 150 MHz. 16-bit loadable counters, capable of doing useful work, require one logic cell delay and operate at over 100 MHz.

Fast sum-of-product state machines require just two cell delays. Complex arithmetic functions using up to four levels of logic run faster than 40 MHz.

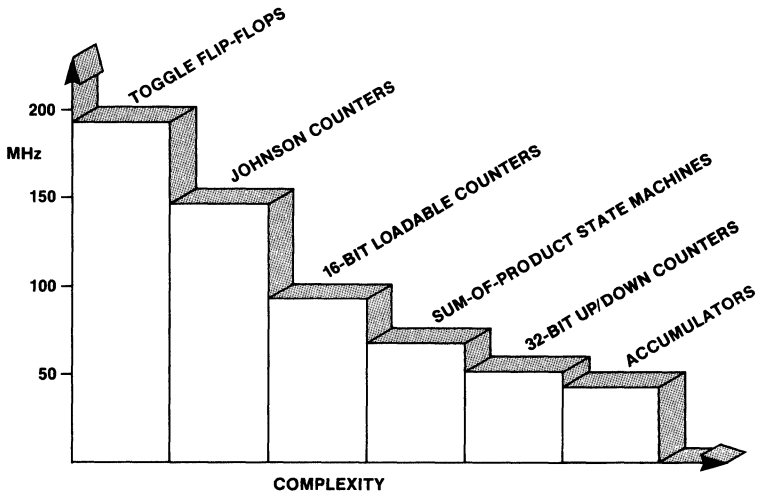


FIGURE 6
Real World Operating Speeds of 50 to 75 MHz

Typical examples of speed versus logic function complexity.

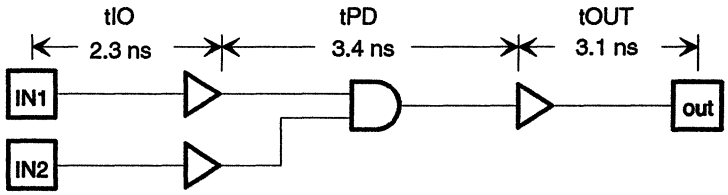
Fast I/O

These impressive on-chip specs are matched by fast I/O performance. Worst case nominal input pad to output pad delay through a 14-input AND gate, or a 4-input MUX, for example, is less than 10 ns.

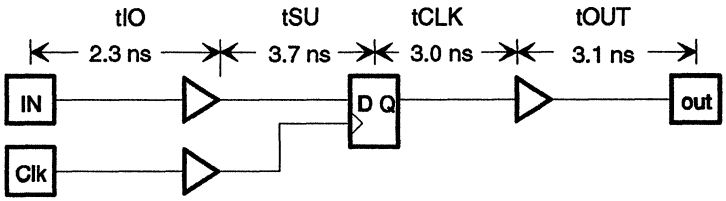
Fast I/O circuits allow logic functions in separate packages to operate together at over 60 MHz. This speed is achieved while preserving low output switching noise levels. Switching of up to 48 outputs simultaneously has been demonstrated with less than 1 volt of ground bounce.

FIGURE 7
Fast I/O Pads

QL12x16 Nominal I/O Delays



Input Delay + Combinatorial Delay + Output Delay = 8.8 ns

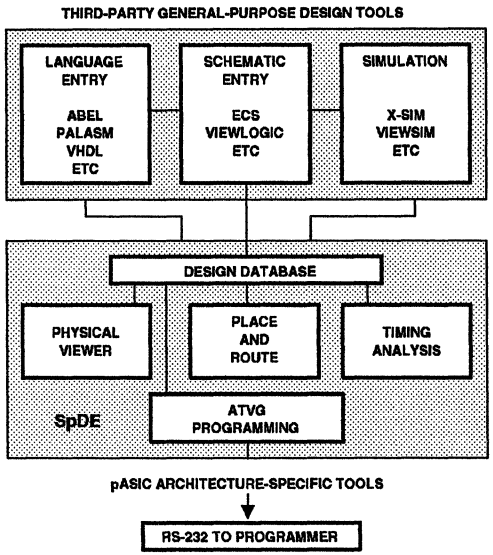


Input Delay + Reg Setup + Clock to Output + Output Delay = 12.1 ns

SPEED THROUGH TOOLS

Fast device operation and rapid design execution is achieved by combining the best third-party CAE tools with device-specific place and route and delay modeling software.

FIGURE 8
The pASIC Toolkit



QuickLogic tools communicate with third-party software through an object-oriented design database.

Third-Party Design Entry

Designs are created using general-purpose schematic, language entry and simulation packages on PC and Sun workstation platforms. These tools interface to the QuickLogic Seamless pASIC Design Environment (SpDE — pronounced "Speedy") for place and route, delay modeling, and other tasks best served by architecture specific code.

VHDL, state machine, and Boolean (ABEL, CUPL, MINC, PALASM, etc.) language entry is available through Exemplar and other logic synthesis packages.

A low-cost, fully integrated design solution, operating under Microsoft Windows on the PC, is available as the pASIC Toolkit 3.0. This includes ECS schematic capture from the CAD/CAM Group, and X-SIM simulation from SAS, plus SpDE software and device programming hardware.

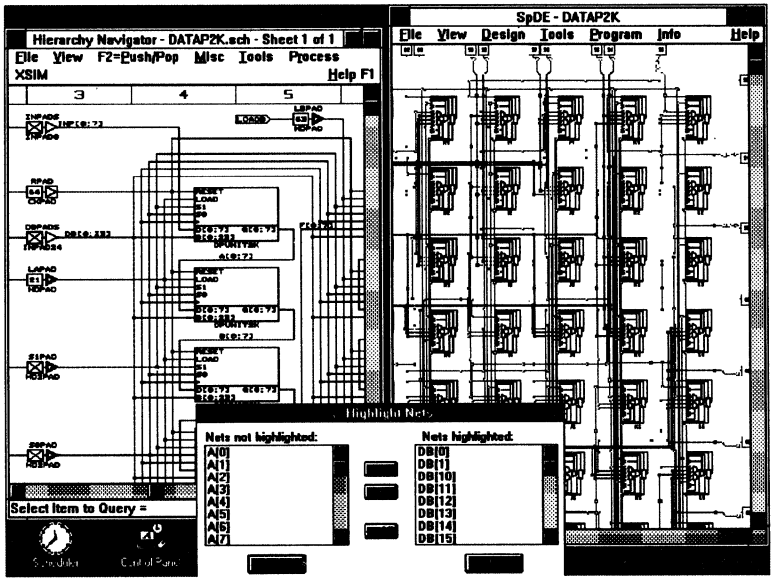
Optimized Place and Route

The regular gate array-like architecture, combined with ample wiring resources, enables 100% automatic placement and routing with high utilization. QL8x12 users report completing designs using 100% of the 96 logic cells, even with a large number of fixed pin locations.

A physical viewer shows how the automatic tools fit logic functions into the silicon resources.

Cross probing between applications allows for easy analysis of designs and fast debugging of problems. Click on a net in the schematic and it is instantly highlighted in the physical layout. Or vice versa. Similar interactive links exist to the simulator.

FIGURE 9 Windows Screen Shot



A net selected in the schematic is instantly highlighted in the physical viewer, and vice versa.

Precise Timing

Asymptotic Waveform Evaluation, AWE, techniques generate precise timing data, using actual circuit wire lengths, fanout and loading. This enhances speed by providing accurate delay models for back annotation into the simulator. It also identifies the most heavily loaded nets for selective programming to less than 50 ohms.

Testing and Programming

Scan path circuitry built into the pASIC flip-flops allows automatic generation of test vectors for post programming functional testing.

Programmers attach to the PC via the RS-232 port. No special-purpose programming cards occupy valuable expansion slots.

pASIC 1 FAMILY PRODUCTS

The pASIC 1 Family serves general-purpose, high-speed logic integration tasks in arithmetic, control, data path and RISC and CISC microprocessor support applications. Three basic devices cover a broad range of speed, package, density, and I/O options.

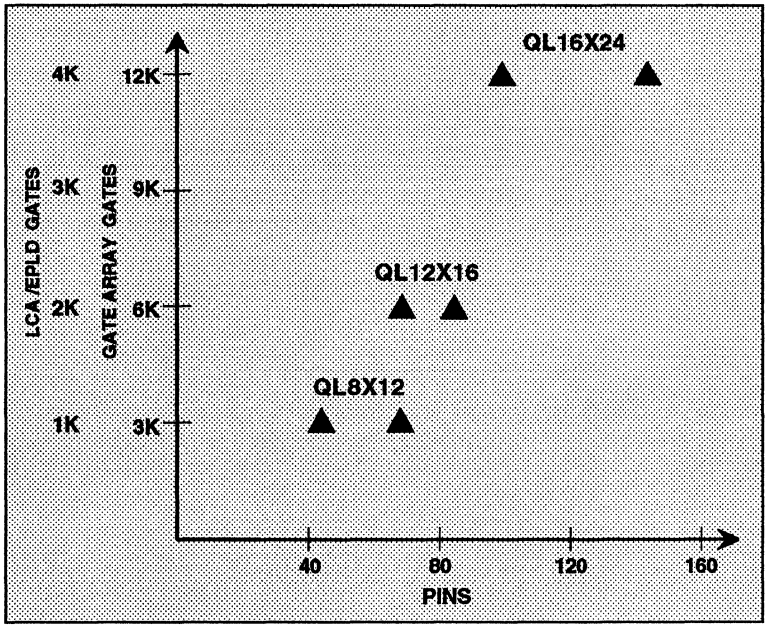


FIGURE 10 The pASIC 1 Product Family Family Features

The pASIC 1 family includes density and I/O options meeting the needs of most high-speed, high-density programmable device applications.

Family Features

Device part numbers describe the organization of logic cells. For example, the QL8x12 features 96 logic cells in an eight by twelve matrix. A fully utilized QL8x12 accommodates 800 to 1200 gates, for an average of ten gates per cell. QuickLogic describes this as a 1000 usable-gate FPGA. It is equivalent in capacity to many, so called "3000 to 4000 gate" EPLD and LCA devices.

As each logic cell contains a dedicated register function plus combinatorial logic sufficient to create two latches, the QL8x12 can contain up to 288 storage elements.

Part Number	Logic Cells	Storage Elements	Max I/O Cells	Dedicated Inputs	Package Pins	Usable Gates	EPLD/LCA Gates
QL8x12	96	288	56	8	44, 68	1000	3000
QL12x16	192	576	68	8	68, 84	2000	6000
QL16x24	384	1152	104	8	100, 144	4000	12000

Product Features

PLCC, PQFP, and other package styles are available. Multiple speed selections on each device allow the user to trade-off performance and cost.

- Input buffer plus logic cell plus output buffer delay of under 10 ns.
- Multiple-chip operating frequencies over 60 MHz.
- Logic function delays, up to two levels deep, in under 4 ns.
- Useful counter speeds up to 100 MHz.
- Low output switching noise. Less than 1 volt of ground bounce with 48 outputs switching simultaneously.
- Worst case clock skew less than 1 ns.
- Input hysteresis provides high reliability in noisy operating environments.
- Low CMOS power consumption; typically 2 mA standby current.

Future pASIC Families

Future pASIC products will use the small size of the ViaLink element to offer FPGA families with densities and I/O counts comparable to today's masked gate arrays. ViaLink technology will also be used to extend the flexibility and ease of use of user-configurable logic to new programmable ASIC architectures.

QuickLogic very-high-speed FPGAs are allowing users to extend the benefits of programmable solutions to new applications which could not be served before due to speed, density, power dissipation or time-to-market limitations of earlier products. The following five case studies demonstrate a variety of applications where pASIC™ 1 Family FPGAs offered significant advantages over alternative TTL, FPGA, PAL/GAL and gate array implementations.

Universal Computing
San Diego, CA

QuickLogic FPGAs help systems company to beat the competition to market with 40-MHz Intel i860-based small form factor multiprocessor system

Design Problem

Universal Computing designs and manufactures high-performance systems for a wide range of vertical market customers. One of Universal's designs is a multiprocessing VME board for signal processing applications in defense, medical imaging, seismology, image processing, molecular modeling and 3-D visualization. In addition to a motherboard supporting a VME bus and high-speed external interface, the system provides four "supercards," each containing a 40-MHz i860 XR microprocessor, up to 4 MB of high-speed DRAM, and high-speed interprocessor communications logic.

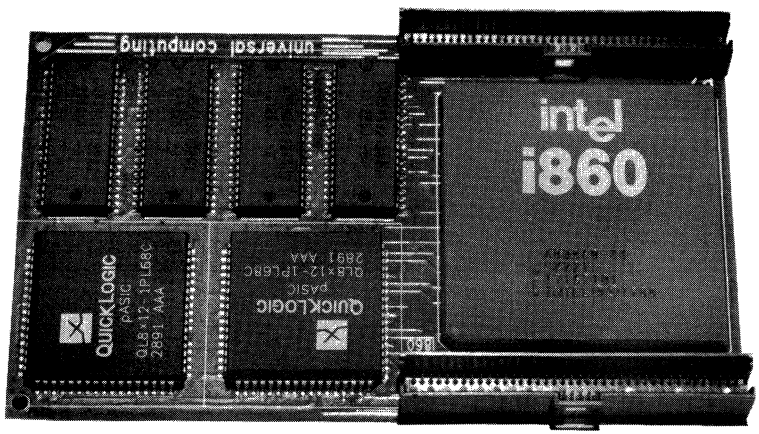


FIGURE 1
The MPi860 offers up to 320 MFLOPS of floating point performance in a single 6U VME slot

QUICKLOGIC

According to sales and marketing director John Thomas, several other companies offered similar products in the large 9-U VME form factor. However, the 9-U standard is considered by some potential customers to be unwieldy. The large form factor can create vibration problems, has loose power standards, and often suffers from inadequate cooling. While the 9-U product is a low-volume opportunity by nature, more compact 6-U products are far more popular and available. Thomas wanted Universal to become the first company on the market to offer such a powerful multiprocessing system in the 6-U form factor.

...to meet VME power specifications, PALs or EPLDs were out of the question.

The major challenge for Universal was redesigning each of the four supercards to create four highly compact daughtercards. In addition, while 9-U systems may use as much as 175W, Universal's 6-U system would need to draw less than 45W to meet VME power specifications. As a result, high-speed PALs or EPLDs were out of the question. A masked gate array could have been used, but the time needed to design and manufacture the part would shorten the period during which Universal would be the sole supplier of 6-U boards.

Design Solution

Universal recognized FPGAs as the solution. The company had used FPGAs from other vendors in several previous designs and considered them for the new design, along with the new pASIC FPGAs from QuickLogic. According to Thomas, "Even without programming logic into the other FPGAs, getting on and off the daughtercards took 45-50 ns. The only way to make the design work would be to drop the performance of the system from 40 MHz to as low as 25 MHz. With QuickLogic, the I/O delay fell to 9 ns, and we could preserve all of the high performance of the 9-U design."

Design Process

Universal used two QL8x12 FPGAs to provide the high-speed memory and bus interface logic required by each of the 40-MHz i860 XR microprocessors. Using the pASIC Toolkit development system, Universal's designers were able to create their logic quickly using high-level schematics. The design tools automatically routed the schematics into optimized gate-level designs that made efficient use of the FPGA logic cells and preserved the high performance needed. By cross probing between the schematic entry, timing simulator and physical viewer, the designers were able to easily debug and optimize the design to support the full potential of the i860 processors and the high-speed memories.

QuickLogic FPGA replaces Xilinx device on 88000-based VME board to boost system speed from 20 MHz to 33 MHz

Force Computers
Campbell, CA

Design Problem

Force Computers manufactures high-performance VME boards for its OEM customers worldwide. Engineering manager Jack Regula was responsible for the design of a VME board based on a 33 MHz version of the Motorola 88000 RISC microprocessor. Regula had chosen to implement the design with the help of programmable logic, selecting an LCA device from Xilinx. When the system design was complete, Regula realized that the system would not function properly beyond 20 MHz. A critical path in the design was a DRAM controller for the 88000 CPU, and although specified to run at high speeds, the SRAM-based FPGA proved too slow in the system. Regula sought a replacement solution that could provide the same pin functionality along with a 65 percent increase in speed.

Design Solution

Regula knew that QuickLogic's new pASIC FPGAs were designed to support high-speed RISC and CISC processors, but by this time, he was skeptical about vendor performance claims. "Each one of the FPGAs I've used has disappointed me," he stated. At the time, however, Force was a beta site for QuickLogic's pASIC Toolkit FPGA development system. Because the 68-pin QL8x12 provided virtually identical pin functionality, Regula decided to find out whether QuickLogic could be used to boost the board's speed to 33 MHz with a minimal redesign effort.

Design Process

Within days, Regula was able to reenter all of the design schematics into the easy-to-use QuickLogic environment. He programmed the QL8x12 to be virtually pin-compatible with the LCA device and easily achieved his 33 MHz speed objective. Regula decided that getting high performance from a Xilinx device requires more than just a synchronous design. "You have to tweak the design to fit the layout and to fit the board. How far apart the CLBs (configurable logic blocks) are affects the propagation delays between them. You don't know what the delay is 'til you route them."[1]

Regula found that QuickLogic delays are always larger than interconnect delays. "They're predictable, no matter what the layout is, very much like a masked gate array." According to Regula, "The entire industry has been waiting for an FPGA that delivers the speed needed to support high-performance designs. Plenty of start-ups have claimed to be fast, routable and predictable, but QuickLogic FPGAs are the first to actually work as you would expect from the data sheet."

"QuickLogic FPGAs are the first to work as you would expect from the data sheet."

[1] Source: *Computer Design*, December 1991

Datacube, Inc.
Dearborn, MA

QuickLogic FPGAs allow developer of powerful real-time video processing systems to complete custom logic design in one weekend

Design Problem

Datacube, Inc. develops extremely powerful computers designed to manipulate complex video data in real time. One Datacube product called the MaxVideo 20 provides 3,500 MIPS for compute-intensive video processing applications such as real-time correction of the geometric image distortion caused by a wide-angle lens. Datacube is a sophisticated user of all kinds of programmable logic, using 80 FPGAs and EPLDs in the MaxVideo 20 product to help integrate the functionality of 14 standard image processing boards onto one double-VME board.

R&D vice president J. Dunn was responsible for developing a new system for real-time pipeline processing of video data. A custom logic design was needed for data formatting and routing, and a critical path existed where 12 memory modules output 96 video data signals at 40 MHz. Here, custom logic was needed to format the data as 192 signals at 20 MHz and then route the data to other system components according to various board and operating mode specifications.

Design Solution

A masked gate array would solve Dunn's custom logic requirements, but time-to-market was a consideration, and the one masked gate array used on the MaxVideo 20 product proved to be the longest-lead component in the system. Dunn decided instead to evaluate all of the programmable logic alternatives in packages ranging from 28 pins to 160 pins, looking for the right high-speed partition for his 24-bit data path. Fast PALs or EPLDs might meet the 40 MHz data rates, but according to Dunn, "EPLDs use substantial power in the process — from 150 mA on up." FPGAs posed the ideal solution, but in Dunn's experience, "The speed criteria eliminated most of the choices. We have the Xilinx tools and the Actel tools in-house, but I didn't believe that I could make either of the architectures go fast enough." Dunn instead chose the 1,000-usable-gate QL8x12 from QuickLogic because the device easily met the 40 MHz data rate and low power requirements. "The 68-pin package was just right," Dunn added.

"We have the Xilinx and Actel tools in-house, but I didn't believe I could make either go fast enough."

Design Process

Dunn designed his logic on the pASIC Toolkit, which is designed to be easy to learn and use, even for first-time customers. According to Dunn, "I did the entire logic design for four QuickLogic parts over a single weekend." Added Dunn, "QuickLogic is a great solution for people needing high speed and low power. I hear other vendors trying to build excitement for their next-generation products. QuickLogic is already there with devices that I can use today."

QuickLogic FPGAs boost speed of servo control system to 40 MHz while integrating 25 TTL devices into a single component

Performance Controls
Horsham, PA

Design Problem

Performance Controls is a manufacturer of high-performance motion control systems. Digital design engineer Brian Fenstermacher was assigned to create a higher-speed implementation of an existing servo control system. The prior system logic implementation used about 25 TTL logic components, including LS-TTL, AS-TTL and F-TTL parts. Board space was an issue in the previous design and would be a problem in the redesign as well. More importantly, Fenstermacher predicted that the speed requirements of the redesign exceeded the capabilities of discrete logic parts. A new approach was inevitable.

Design Solution

Fenstermacher decided to try to integrate the functionality of the TTL devices into a single, high-speed FPGA. He considered all of the available FPGA solutions, looking for the one that could best meet the high-speed logic requirements of the new product specification. Fenstermacher decided to use the first member of QuickLogic's pASIC 1 family of FPGAs, the 1,000-usable-gate QL8x12.

Design Process

According to Fenstermacher, QuickLogic's Microsoft Windows-based pASIC Toolkit was easy to learn and more intuitive than competing FPGA development systems. He mastered the design tools in days, using schematic capture for design entry. Fenstermacher took advantage of cross probing between the schematic capture, simulation and physical viewer tools to quickly optimize and debug the design. The simulator provided precise results, and the programmed QL8x12 performed exactly as predicted. Within two weeks of receiving the QuickLogic tools, the pASIC FPGAs were programmed and ready for system installation. Fenstermacher was successful at integrating the functionality of two dozen MSI and LSI parts into the QL8x12 while comfortably meeting the 40 MHz speed requirements of the redesign.

...the programmed QL8x12 performed exactly as predicted.

According to Fenstermacher,"QuickLogic offers a great way to implement very fast, complex state machines in an easy-to-use part."

VLSI Technology
San Jose, CA

QuickLogic FPGAs enable 50-MHz memory controller for RISC processor evaluation board

Design Problem

VLSI Technology is a manufacturer of CMOS ASICs and ASSPs as well as the ARM family of RISC processors. When a new family of ARM6 processors was introduced last autumn, design engineer Art Sobel became responsible for designing an evaluation board that would allow engineers to adapt hardware and software to the new processors. Two functions were needed to complete a minimal system design. One function was a memory controller capable of driving DRAM, EPROM and I/O functions, and 50-MHz operating frequency was mandatory. The second function was a simple interrupt controller.

The logic requirements of each element could be met with high-speed PALs, but with much greater part count and some loss of flexibility. Moreover, a masked gate array solution was not appropriate because of the long lead time, and the possibility of design changes on the product.

Design Solution

In response to these requirements, Sobel decided to use the QuickLogic QL8x12 for both logic functions. For memory control, the QL8x12 had the capability of operating with the 50-MHz clock needed to craft the DRAM waveforms while providing a high enough drive capability to drive the DRAM address pins and the ARM600 clock pins. The QL8x12 was also very well suited to the design requirements of the interrupt controller. In addition, the solution greatly reduced the number of parts that Sobel needed to procure. Both designs used all 56 I/O pins and several of the input-only pins on the QL8x12 and utilized about 60 percent of the available logic cells. In both designs, all of the I/O pins were preassigned to simplify the PC board design.

Design Process

Sobel designed his logic using schematic capture, taking advantage of QuickLogic's macro library of more than 200 commonly used logic elements. The simulator was used to provide functional verification of the design even before the first pASIC device was programmed. Timing analysis ensured that the QL8x12 devices would meet the speed requirements of the RISC processor's memory interface, and both parts worked well on the board at the 50 MHz clock frequency. The memory controller function FPGA was revised once to correct for an unexpected logic signal and was fully functional once a second part was programmed. The interrupt controller FPGA was fully functional on the first attempt. According to Sobel, "I got completely over the learning curve in just a couple of weeks. After designing only two chips, I would feel comfortable taking on any design challenge with QuickLogic."

...the parts worked well on the board at the 50 MHz clock frequency.

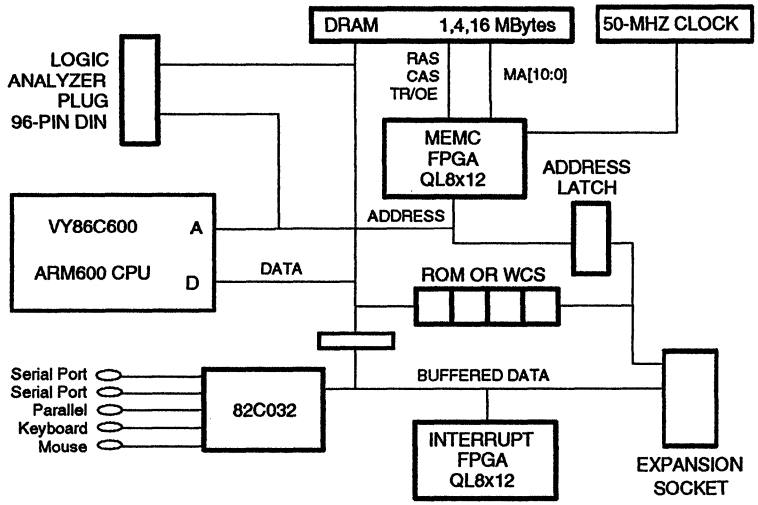


FIGURE 2
VY86XPID Development Board Block Diagram

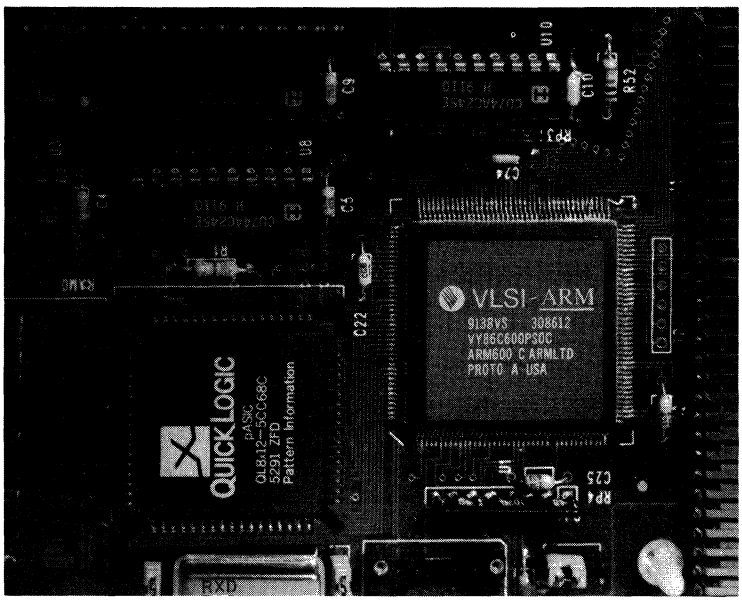
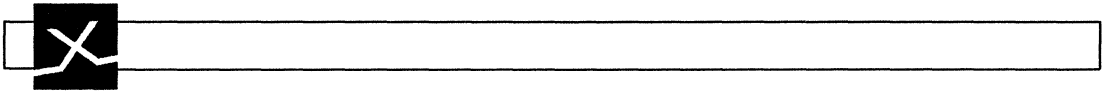


FIGURE 3
The VLSI Technology VY86C600 - ARM60D RISC processor with cache and memory management plus the QL8x12 used as a 50 MHz memory controller (MEMC PGA)



pASIC 1 FAMILY
ViaLink Technology
Very-High-Speed CMOS FPGAs

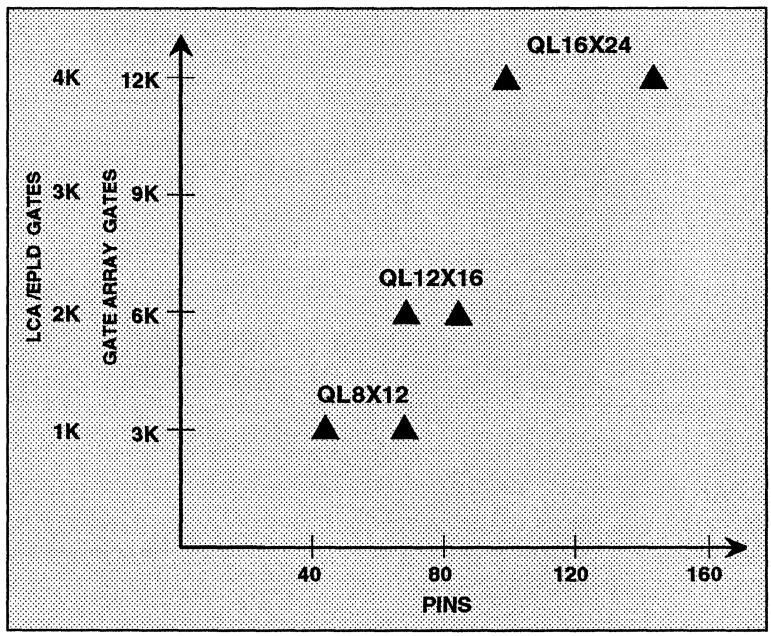
FAMILY HIGHLIGHTS

...migration path to 20,000 gates

- **Very High Speed** – ViaLink™ metal-to-metal, programmable-via antifuse technology ensures useful internal logic function speeds over 100 MHz, and logic cell delays of under 4 ns.
- **High Usable Density** – Up to 4,000 "gate array" gates, equivalent to 12,000 EPLD or LCA Gates. Technology migration path to 20,000 gates and above.
- **Low Power** – Stand-by current typically 2 mA. A 16-bit counter operating at 100 MHz consumes 50 mA.

  Flexible FPGA Architecture – The pASIC™ logic cell supports efficient, high-speed arithmetic, counter, data path, state machine and random logic applications with up to 14-input wide gates.
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using third-party CAE tools. Fast, fully automatic place and route on PC and workstation platforms.

FIGURE 1
pASIC 1 Family



QUICKLOGIC

FAMILY SUMMARY

The pASIC 1 Family of very-high-speed CMOS user-programmable ASIC (pASIC) devices is based on the first FPGA technology to combine high speed, high density and low power in a single architecture.

All pASIC 1 Family devices are based on an array of highly flexible logic cells which have been optimized for efficient implementation of high-speed arithmetic, counter, data path, state machine, random and glue logic functions. Logic cells are configured and interconnected by rows and columns of routing metal and ViaLink metal-to-metal programmable-via interconnect elements.

ViaLink technology provides a nonvolatile, permanently programmed custom logic function capable of operating at counter speeds of over 100 MHz. Internal logic cell nominal worst case delays are under 4 ns and total input to output combinatorial logic delays are under 10 ns. This permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors, while consuming a fraction of the power and board area of PAL, GAL and discrete logic solutions.

pASIC 1 Family devices range in density from 1000 "gate array" gates (3,000 EPLD/LCA gates) in a 44-pin package, to 4,000 (12,000) gates in high-pin-count packages. All devices share a common architecture and CAE design software to allow easy transfer of designs from one product to another. The small size of the ViaLink programming element ensures a technology migration path to devices of 20,000 gates and above.

Designs are entered into the pASIC Family devices on PC or workstation platforms using third-party, general-purpose design-entry and simulation CAE packages, together with QuickLogic device-specific place and route and programming software, called SpDE tools. Sufficient on-chip routing channels are provided to allow fully automatic place and route of designs using up to 100% of the available logic cells.

All the necessary hardware and software, required to complete a design, from entering a schematic to programming a device are included in pASIC Toolkits available from QuickLogic. The pASIC Toolkit 3.0, includes the CAD/CAM ECS™ Engineering Capture System together with a waveform-driven version of the X-SIM™ simulator from Silicon Automation Systems. All applications run on the PC under the Microsoft Windows 3.0 graphical user interface to ensure a highly productive and easy-to-use design environment. An open interface (QDIF) allows many other third-party tools (Exemplar, Viewlogic, etc.) to be used with QuickLogic software on both PC and workstation platforms.

VIALINK PROGRAMMING ELEMENT

Programmable devices implement customer-defined logic functions by interconnecting user-configurable logic cells through a variety of semiconductor switching elements. The maximum speed of operation is determined by the effective impedance of the switch in both programmed, ON, and unprogrammed, OFF, states.

In pASIC devices the switch is called a ViaLink element. The ViaLink element is an antifuse formed in a via between the two layers of metal of a standard CMOS gate array process. The direct metal-to-metal link created as a result of programming achieves a connection with resistance values below 50 ohms. This is less than 5 percent of the resistance of an EPROM or SRAM switch and 10 percent of that of a dielectric antifuse. The capacitance of an unprogrammed ViaLink site is also lower than these alternative approaches. The resulting low RC time constant provides speeds two to three times faster than older generation technologies.

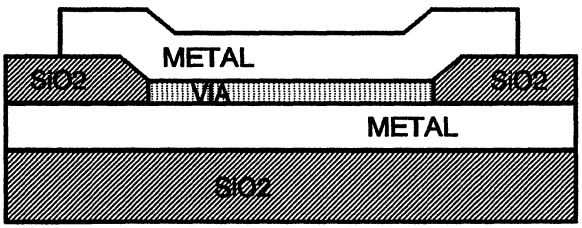


FIGURE 2a Unprogrammed ViaLink Element

Figure 2a shows an unprogrammed ViaLink site. In a custom metal masked ASIC, such as a gate array, the top and bottom layers of metal make direct contact through the via. In a ViaLink programmable ASIC device the two layers of metal are initially separated by an insulating silicon layer with resistance in excess of 1 gigaohm.

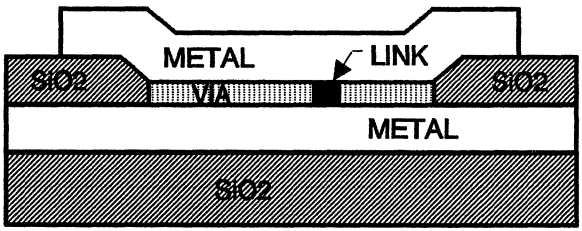
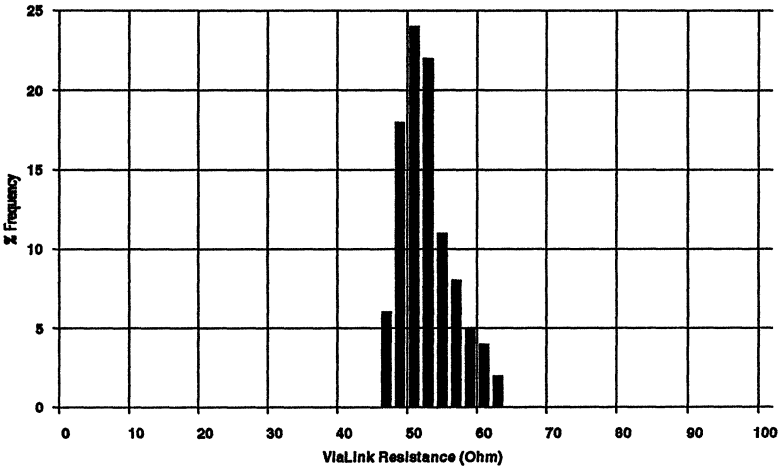


FIGURE 2b Programmed ViaLink Element

A programming pulse of 10 to 11 volts applied across the via forms a bidirectional conductive link connecting the top and bottom metal layers, Figure 2b. The tight distribution of link resistance is shown in Figure 3.

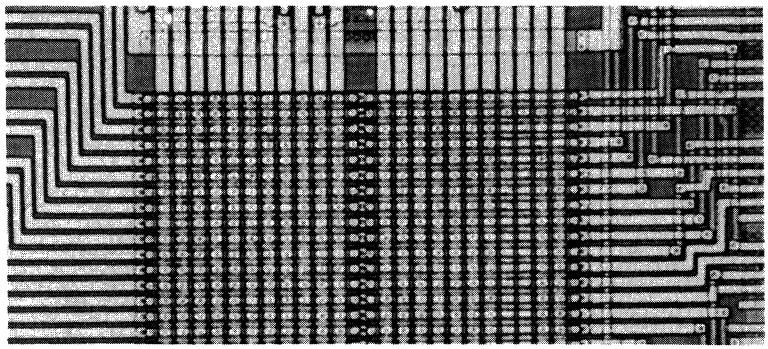
FIGURE 3
Distribution of Programmed Link Resistance



STANDARD CMOS PROCESS

QuickLogic pASIC devices are the first FPGA devices to be fabricated on a conventional high-volume CMOS gate array process. The base technology is a 1 micron, n-well CMOS technology with a single polysilicon layer and two layers of metal interconnect. The only deviation from the standard process flow occurs when the ViaLink module is inserted between the metal deposition steps.

FIGURE 4
An Array of ViaLink Elements



As the size of a ViaLink via is identical to that of a standard metal interconnect via, programmable elements can be packed very densely. The microphotograph of Figure 4 shows an array of ViaLink elements. The density is limited only by the minimum dimensions of the metal-line to metal-line pitch. Migration of the gate array process to submicron dimensions will allow the development of pASIC devices with tens of thousands of usable gates.

pASIC FAMILY ARCHITECTURE

The pASIC device architecture consists of an array of user-configurable logic building blocks, called logic cells, set in a grid of metal wiring channels similar to those of a gate array. Figure 5 shows a section of a pASIC device containing internal logic cells, input/output cells and dual-layer vertical and horizontal metal routing channels. Through ViaLink elements located at the wire intersections, the output of any cell may be programmed to connect to the input of any other cell.

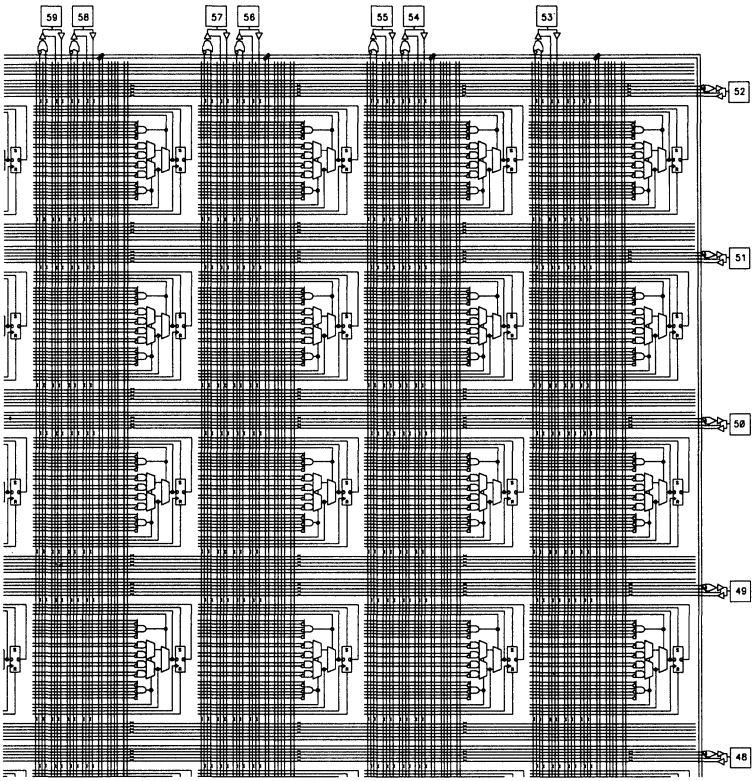


FIGURE 5
A Matrix of Logic Cells and Wiring Channels

This regular and orthogonal interconnect, makes the pASIC architecture similar in structure and performance to a metal masked gate array. It also makes system operating speed far less sensitive to partitioning and placement decisions, as minor revisions to a logic design result only in small changes in performance.

Adequate wiring resources permit 100% automatic placement and routing of designs using up to 100% of the logic cells. This has been demonstrated on designs that include a high percentage of fixed pin placements.

ORGANIZATION

The pASIC 1 Family of very-high-speed FPGAs contains devices covering a wide spectrum of I/O and density requirements. Three members ranging from 1,000 gates in a 44-lead package to 4000 gates in a 144-lead package are shown in Figure 6.

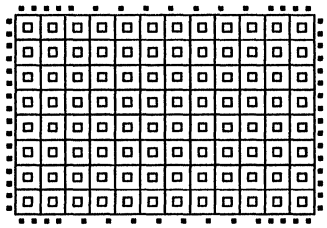
Device part numbers are derived from the organization of internal logic cells. For example, in Figure 6, the QL8x12 contains 96 logic cells in an 8-by-12 matrix. The single lines between logic cells represent channels containing up to twenty-two wires. Each of the internal logic cells has the logic capacity of up to 30 "gate array gates." As a typical application will use 10 to 12 gates from each logic cell, the QL8x12 is described as a 1000-usable-gate device. Based on the "available gate" gate counting approach of some programmable logic vendors, it would be called a 3000-gate part. The QL8x12 is available in a 68-lead package with 56 bidirectional I/O pins and 8 dedicated input/high drive clock pins and a 44-lead package with 32 I/O pins.

The key features of these three pASIC devices are as follows:

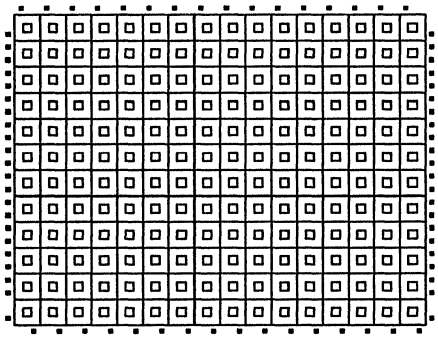
Device Cells	Logic Cells	Max I/O Inputs	Dedicated Pins	Package Pins	Usable Gates	EPLD/LCA Gates
QL8x12	96	56	8	44,68	1000	3000
QL12x16	192	68	8	68,84	2000	6000
QL16x24	384	104	8	100,144	4000	12000

See individual product data sheets for specific information on each device.

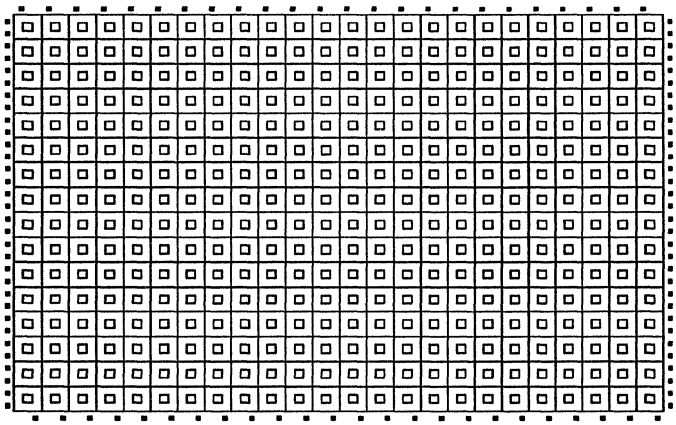
8x12



12x16



16x24



■ = I/O /High-drive Input/ Clock Cells
□ = Logic Cells
+ = Interconnect Wiring Channels

FIGURE 6
pASIC 1 Family Members

2

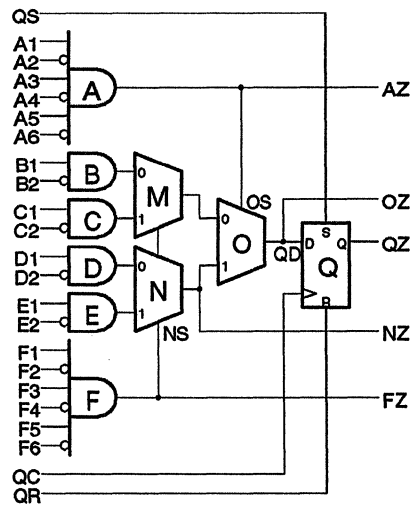
PASIC INTERNAL LOGIC CELL

The pASIC internal logic cell, shown in Figure 7, is a general-purpose building block that can implement most TTL and gate array macro library functions. It has been optimized to maintain the inherent speed advantage of the ViaLink technology while ensuring maximum logic flexibility.

The logic cell consists of two 6-input AND gates, four 2-input AND gates, three 2-to-1 multiplexers and a D flip-flop. In addition to the dedicated flip-flop, logic gates in each cell can be configured to provide two latches. As noted above, each cell represents approximately 30 gate-equivalents of logic capability. Multiple outputs from the logic cell allow the automatic place and route software to pack unrelated logic functions into a single cell to maximize silicon utilzation.

The pASIC logic cell is unique among FPGA architectures in that it offers up to 14-input-wide gating functions. This allows many logic functions to be accomplished in a single cell delay that require two or more delays with other architectures. It can implement all possible Boolean transfer functions of up to three variables as well as many functions of up to 14 variables.

FIGURE 7
pASIC Internal Logic Cell



Glitch-free switching of the multiplexer is ensured as the internal capacitance of the circuit maintains enough charge to hold the output in a steady state during input transitions. The multiplexer output feeds the D-type flip-flop which can also be configured to provide J-K, S-R, or T-type functions as well as count with carry-in. Two independent SET and RESET inputs can be used to asynchronously control the output condition. The combination of wide gating capability and a built-in sequential function makes the pASIC logic cell particularly well suited to the design of high-speed state machines, shift registers, encoders, decoders, arbitration and arithmetic logic, as well as a wide variety of counters.

The function of a logic cell is determined by the logic levels applied to the inputs of the AND gates. ViaLink sites located on signal wires tied to the gate inputs perform the dual role of configuring the logic function of a cell and establishing connections between cells.

The pASIC macro library contains more than 200 of the most frequently used logic functions optimized to fit the logic cell architecture. A detailed understanding of the logic cell is therefore not necessary to successfully design with pASIC devices. CAE tools will automatically translate a conventional logic schematic into a device and provide excellent performance and utilization.

Many useful hints on how to achieve optimum results are provided in The pASIC Users Guide supplied with the pASIC Toolkit. Application Notes QAN 1 and QAN 2 provide more details for users who wish to add special-purpose counter or register macros to the library.

INPUT AND OUTPUT CELLS

Three types of input and output structures are provided on pASIC devices to configure buffering functions at the external pads. They are the Bidirectional Input/Output (I/O) cell, the Dedicated Input (I) cell and the Clock Input cell (I/CLK).

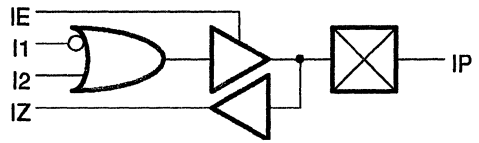
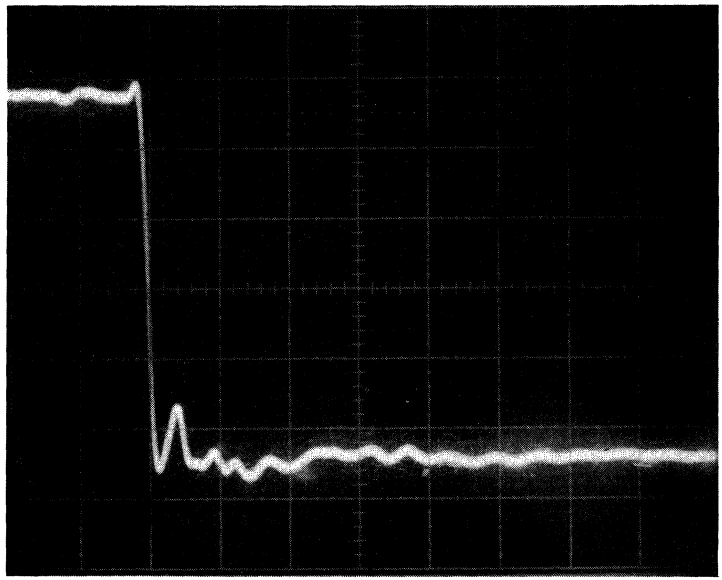


FIGURE 8 Bidirectional I/O Cell

The bidirectional I/O cell, shown in Figure 8, consists of a 2-input OR gate connected to a pin buffer driver. The buffer output is controlled by a three-state enable line to allow the pad to also act as an input. The output may be configured as active HIGH, active LOW, or as an open drain inverting buffer.

FIGURE 9
Scope photo of worst case output switching noise



The output buffers (IOL/IOH of 8 mA) are designed to ensure quiet switching characteristics while maintaining high speed. Measured results show up to 48 outputs switching simultaneously into a 10 pF load with less than ±1 volt of output switching noise.

FIGURE10a
Dedicated Input High-Drive Cell

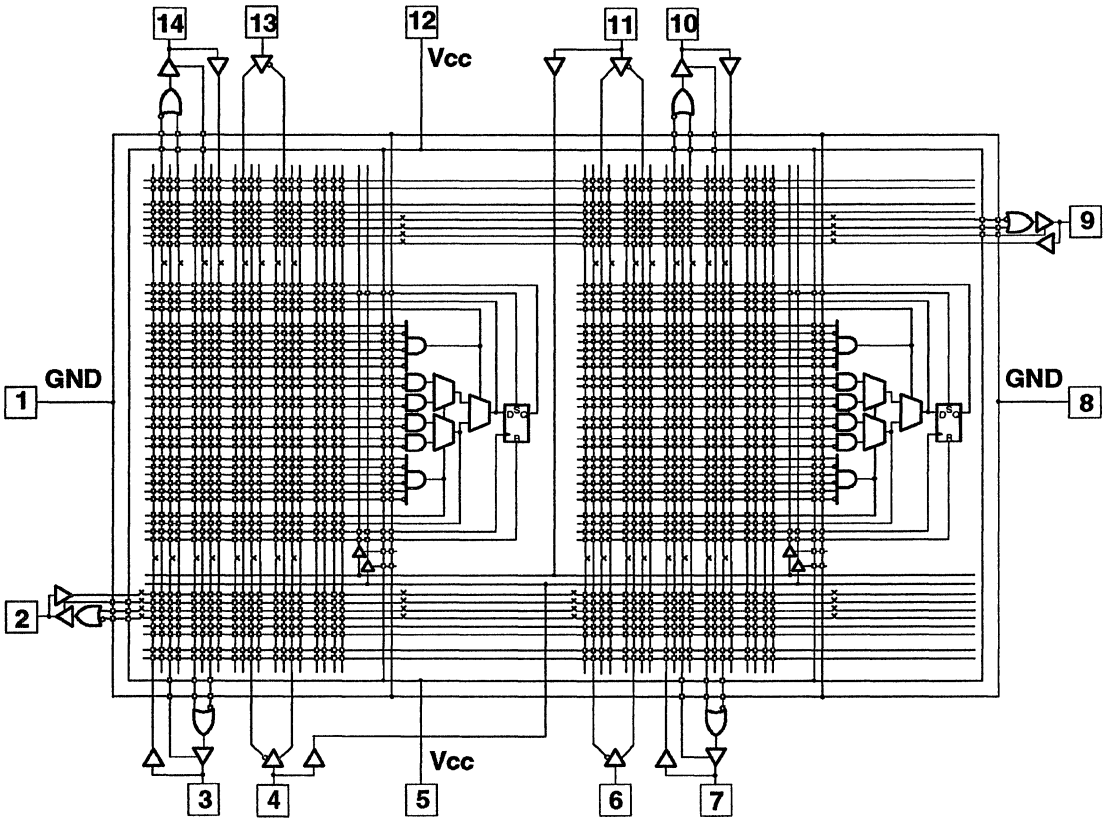
The Dedicated Input I cell, Figure 10a, conveys true and complement signals from the input pads into the array of logic cells. As these pads have nearly twice the current drive capability of the I/O pads, they are useful for distributing high fanout signals across the device. The Clock Input I/CLK cell (Figure 10b) drives a low-skew, fanout-independant clock tree that can connect to the clock, set, or reset inputs of the flip-flop. The QL12x16 device, for example, has 68 I/O cells, 6 I cells, and 2 I/CLK cells.

FIGURE10b
Clock Input Cell

pASIC INTERCONNECT STRUCTURE

Multiple logic cells can be programmed to form a complex logic function by interconnection through the routing channels. To describe the organization of these routing channels, a hypothetical 14-pin function consisting of two logic cells is shown in Figure 11. This device contains the same architectural features as the members of the pASIC 1 family.

FIGURE 11 pASIC Device Features



Active logic functions are performed by the internal logic cells, the I/O cells (pins 2, 3, 7, 9, 10 and 14) the I cells (pins 4, 6), and the I/CLK cells (pins 11 and 13). These cells are connected with vertical and horizontal wiring channels.

Three types of signal wires are employed; Segmented Wires, Express Wires, and Clock Wires. Segmented wires are predominantly used for local connections and have a ViaLink element, known as a Cross Link (denoted by the open box symbol) at every crossover point. They may also be connected to the segmented wires of cells above and below through ViaLink elements, called Pass Links (denoted by the X symbol). Express lines are similar to segmented wires except that they are not divided by pass links. Dedicated Clock wires are lightly loaded with only three links per cell to distribute high-speed clock edges to the flip-flop CLK, SET and RESET pins. Express wires may also be used to deliver clock signals into the multiplexer region of the cell for combinatorial gating. The automatic place and route software allocates signals to the appropriate wires to ensure the optimum speed/density combination.

Vertical VCC and GND wires are located close to the logic cell AND-gate inputs to allow any input that is not driven by the output of another cell to be automatically tied to either VCC or GND. All the vertical wires (segmented, express, clock and power) considered as a group are called vertical channels. These channels span the full height of the device and run to the left of each column of logic cells.

Horizontal wiring channels, called rows, provide connections, via cross links, to other columns of logic cells and to the periphery of the chip. Appropriate programming of ViaLink elements allows electrical connection to be made from any logic cell output to the input of any other logic or I/O cell. Ample wires are provided in the channels to permit automatic place and route of many designs using up to 100 percent of the device logic cells. Designs can be completed automatically even with a high percentage of fixed user placement of internal cells and pin locations.

This information is presented to provide the user with insight into how a logic function is implemented in pASIC devices. However it is not necessary to develop a detailed understanding of the architecture in order to achieve efficient designs. All routing tasks are fully automatic. No manual wire routing is necessary, nor is it permitted by the software. Fully automatic placement of logic fuctions is also offered. But if necessary to achieve a specific pin configuration or register alignment, for example, manual placement is supported.

DESIGN ENTRY

Designs are entered into pASIC devices using third-party schematic capture packages, Boolean equation (ABEL, PALASM, etc.), and high-level language descriptions (such as VHDL)

The basic macro library for use with schematic entry tools utilizes logic cells, I/O cells, high-drive I and clock input I/CLK cells to implement a broad selection of building blocks including gates, multiplexers, latches and flip-flops. Complex macros spanning multiple logic cells provide counters, multipliers and other arithmetic functions.

The flexibility of the pASIC logic cell will permit the generation of thousands of possible macro functions. For example, over 10,000 single-output gate configurations can be conceived. To keep the library to a manageable size, all configurations of up to 6-input gates are included together with all configurations of 14-input gates. The user can create any other desired function and store it for future use in a custom macro library.

MACRO LIBRARY

Macro cells available in the library include the following groups :

- AND Gates
- NOR Gates
- NAND Gates
- OR Gates
- Multiplexers
- Other Combinatorial Macros
- Flip Flops
- Latches
- I/O Pads
- Adders and Multipliers
- Registers
- Counters
- Shift Registers
- 7400-Series TTL Macros
- Master Cells

See the pASIC Macro Library Data Sheet for more details.

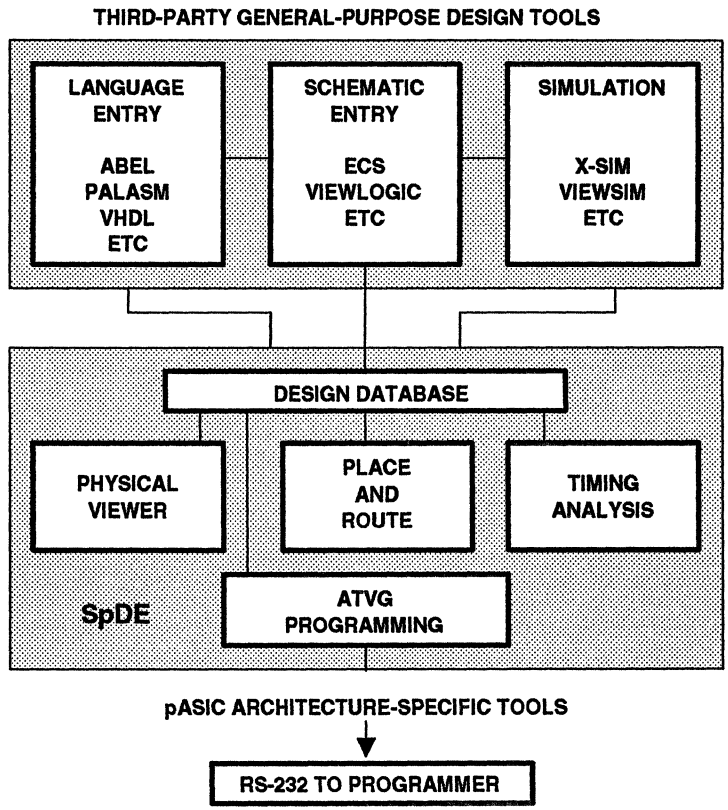
pASIC TOOLKIT

Macro libraries for popular schematic packages, including CAD/CAM ECS and VIEWlogic Viewdraw, are included in a series of pASIC Toolkits developed for designing, simulating, programming and testing of QuickLogic pASIC devices. The following applications are available:

- Schematic capture
- Logic Synthesis for Equation and VHDL entry
- Simulation
- Static Path Timing analysis
- Automatic Placement and Routing (APR)
- Physical View of the results of APR
- Post-layout delay modeling and back-annotation
- Device programming
- Automatic test vector generation
- Device testing

Communication between third-party tools and the pASIC-specific software, called the Seamless pASIC Design Environment (SpDE)— pronounced Speedy, is provided via an open QuickLogic Data Interface Format (QDIF). This allows tight integration with the object-oriented design database within SpDE. Figure 12 shows a typical configuration of a pASIC development system.

FIGURE 12
pASIC Toolkit 3.0
Block Diagram



Unique features of the SpDE tools include:

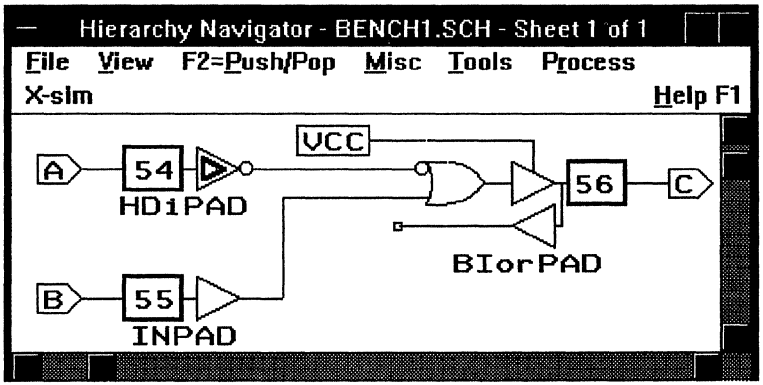
- An object-oriented design database for efficient interaction with third-party tools.
- Delay modeling based on Asymptotic Waveform Evaluation (AWE) RC timing analysis techniques for precise simulation results.
- An interactive physical viewer for visual inspection of the results of the place and route operation.
- The ability to cross probe between applications for efficient debugging and design optimization.

Full details are provided in the SpDE and pASIC Toolkit data sheets.

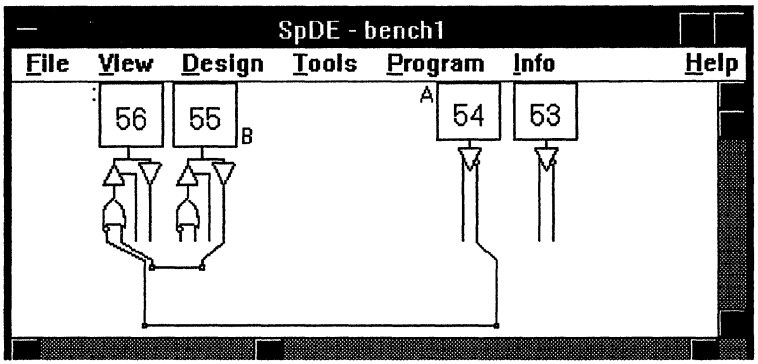
PERFORMANCE BENCHMARKS

The flexibility of the internal logic cell and interconnect structure allows pASIC devices to be used for a wide variety of high-performance logic applications. The following examples have been selected to provide a general overview of the performance of the devices in typical applications.

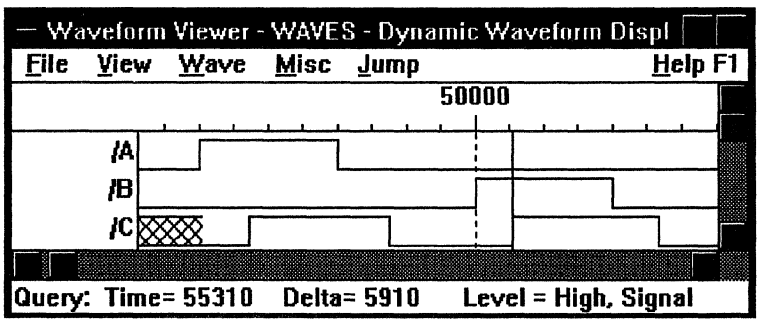
I/O Delays Schematic



Physical View

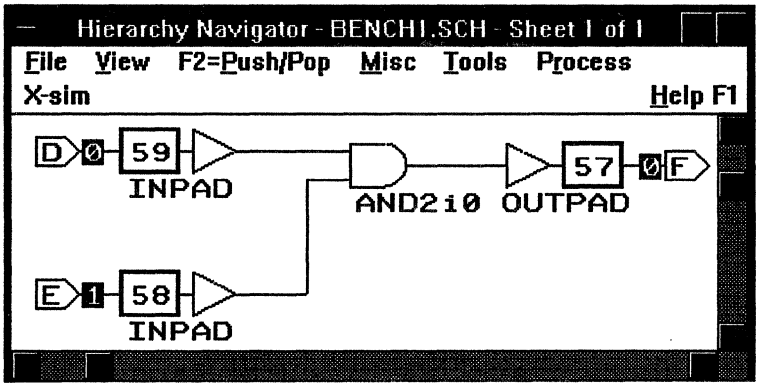


Simulator Analysis

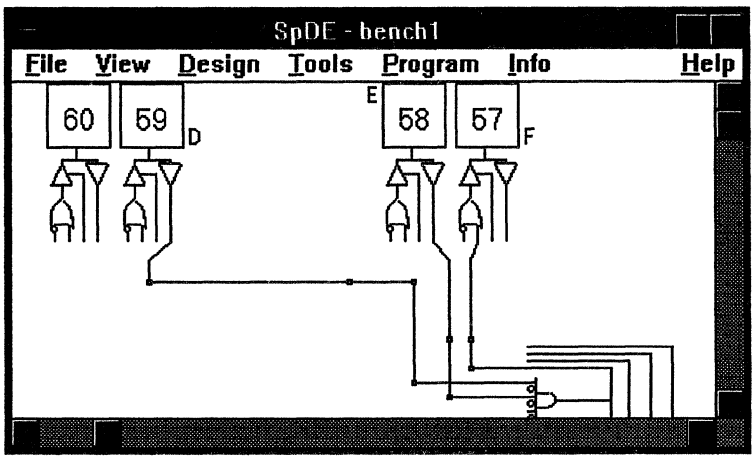


...nominal 5.9 ns input to output

Combinatorial Delay Benchmark Schematic

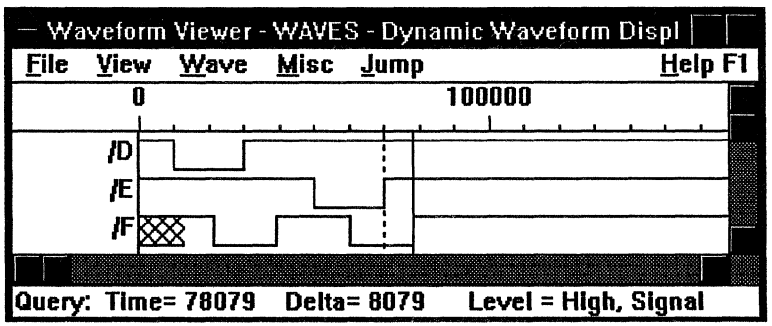


Physical View



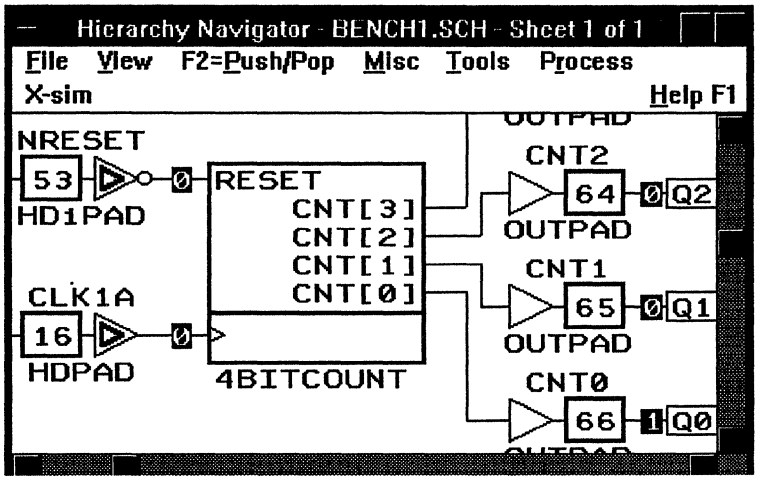
Simulator Analysis

...nominal 8.1 ns input to output

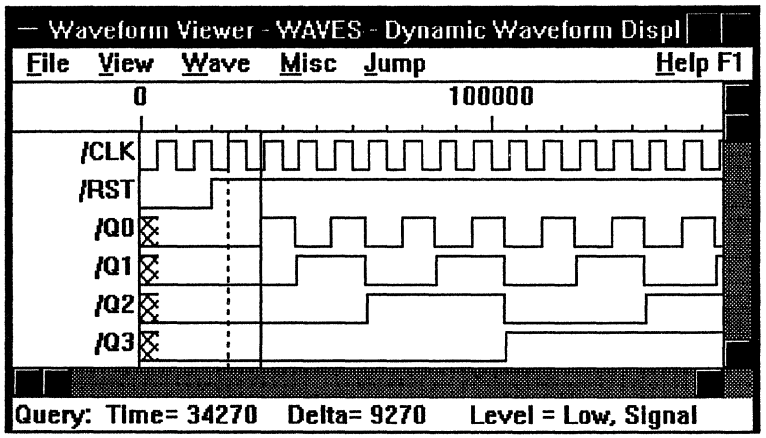


The 4-bit counter demonstrates the performance of small state machines operating at over 100 MHz.

4-Bit Counter Benchmark



...nominal clock to output of 9.3 ns

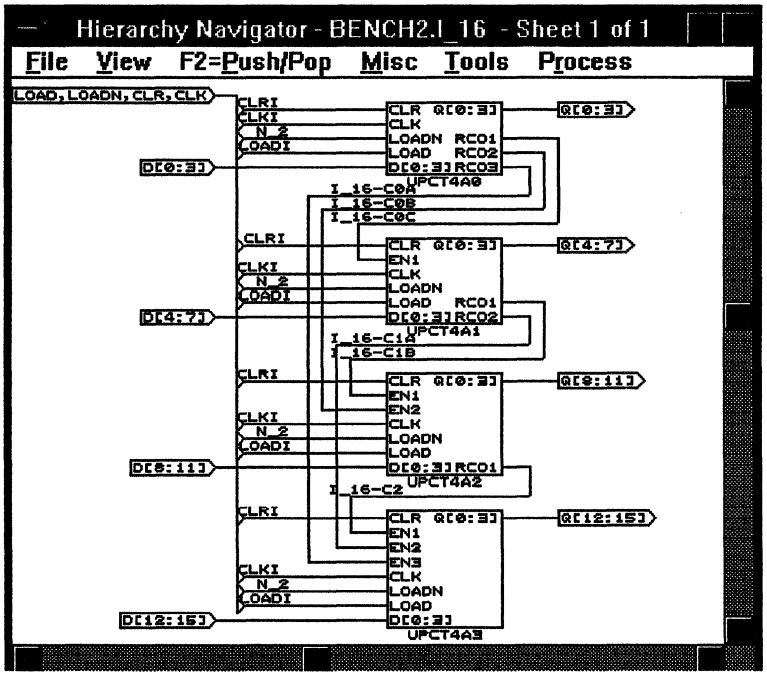


...Fmax >100 MHz

16-Bit Loadable Counter Benchmark

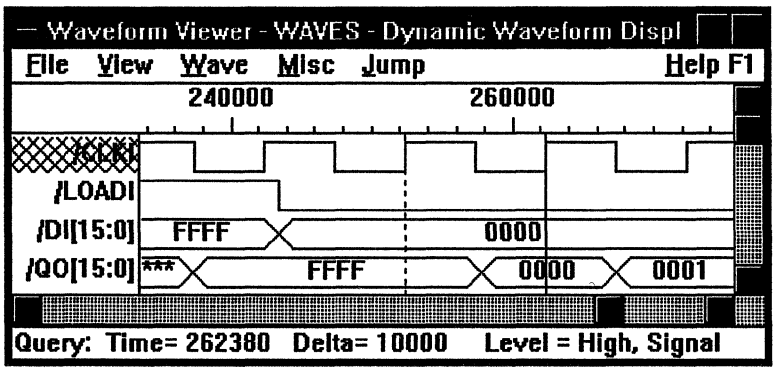
The 16-Bit Loadable Counter can operate at frequencies of greater than 100 MHz for both loading and counting. A count operation may take place in the next clock cycle following a load of any arbitrary data including the end conditions, FFFE and FFFF.

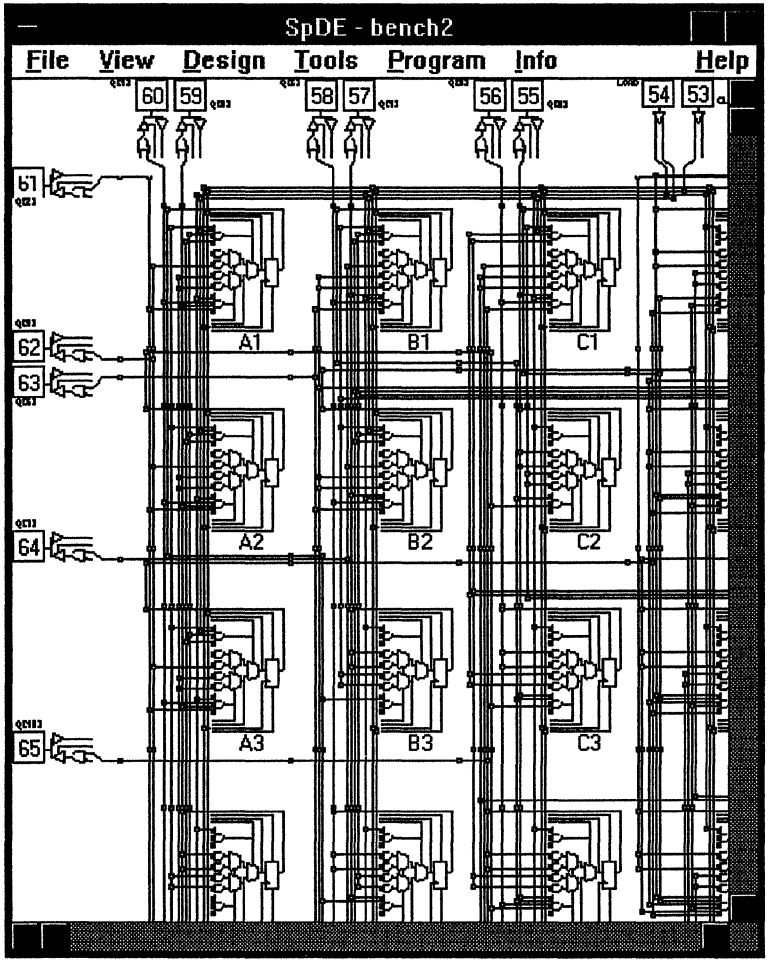
Schematic



Simulator Analysis

...>100 MHz Load and /or Count



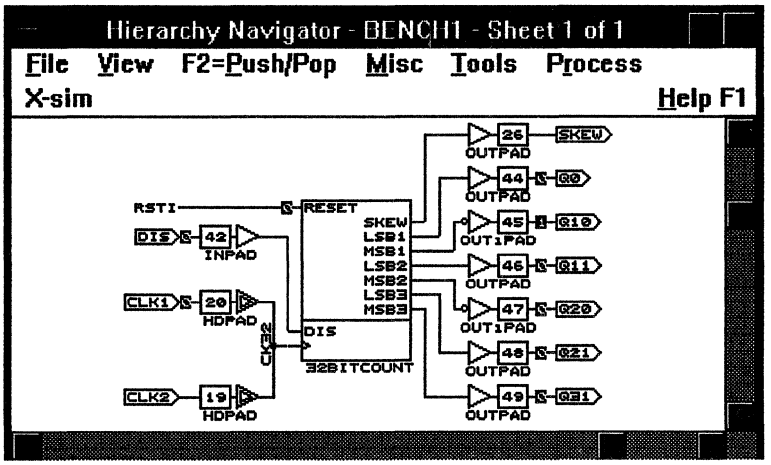


Physical Viewer

32-Bit Counter Benchmark

The 32-bit counter benchmark demonstrates large state machine performance utilizing 36 logic cells and express routing for clocks and carry signals.

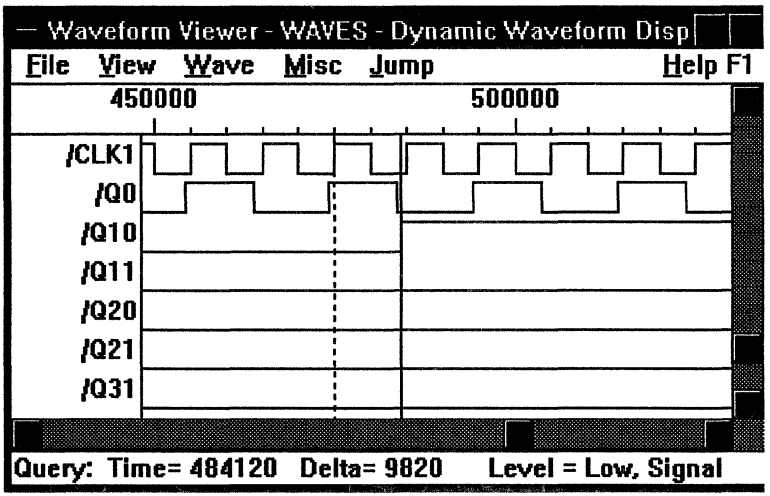
Schematic



Waveforms

...nominal 9.8ns clock to out

...>100 MHz clock rate



POWER CONSUMPTION

Typical stand-by power supply current consumption, ICC, of a pASIC device is 2 mA. The worst-case limit over the operating range for the QL8x12 is 10 mA. A formula for calculating ICC under AC conditions is provided on the device data sheets. The 16-bit counter shown in the previous benchmark design consumes under 50 mA at 100 MHz.

PROGRAMMING AND TESTING

pASIC devices may be programmed and functionally tested on the low-cost Designer Programmer (QP-PL84) supplied by QuickLogic. The unit is completely self contained. No add-in boards are required. Programming signals are downloaded from the PC over an RS-232 link. Third-party programmers are being qualified.

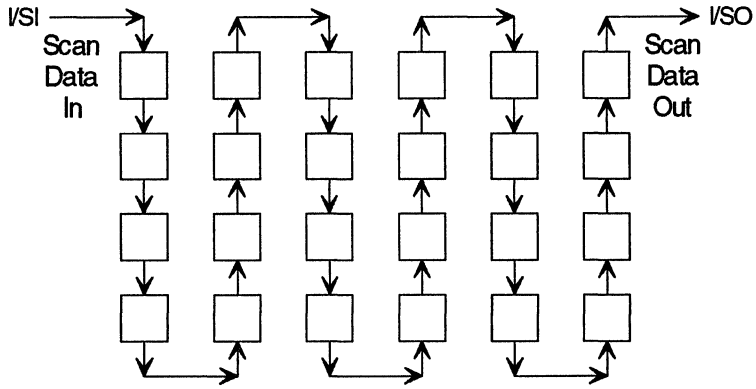


FIGURE 13 Internal Serial Scan Path

All pASIC devices have a built-in serial scan path linking the logic cell register functions (Figure 13). This is provided to improve factory test coverage and to permit testing by the user with automatically generated test vectors following programming. Automatic Test Vector Generation software is included in the pASIC toolkits. The Designer Programmer permits a high degree of test coverage to be achieved conveniently and rapidly using test vectors optimized for the pASIC architecture.

Pins used for scan testing also serve as dedicated logic inputs, see individual device data sheets. Certain logic uses of these pins may conflict with ATVG operation. The software will advise the user of these conditions.

RELIABILITY

The pASIC 1 Family is based on a 1 micron high-volume CMOS gate array fabrication process with the ViaLink programmable-via antifuse technology inserted between the metal deposition steps. The base CMOS process has been qualified to meet the requirements of MIL-STD-883B, Revision C.

The ViaLink element exists in one of two states; a highly resistive unprogrammed, OFF, state and the low impedance, conductive, ON, state. It is connected between the output of one logic cell and the inputs of other logic cells directly or through other links. No D.C. current flows through either a programmed or an unprogrammed link during operation as a logic device. An unprogrammed link sees a worst case voltage equal to VCC biased across its terminals. A programmed link carries A.C. current caused by charging and discharging of device and interconnect capacitances during switching.

Study of test structures and complete pASIC devices has shown that an unprogrammed link under VCC bias remains in the unprogrammed state over time. Similar tests on programmed links under current bias exhibit the same stability. These tests indicate that the long term reliability of the combined CMOS and ViaLink structure is similar to that of the base gate array process. For further details see the pASIC 1 Family Reliability Report.

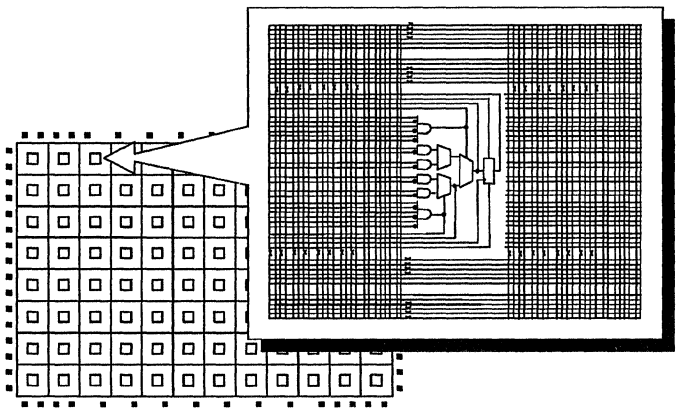
QL8x12
pASIC 1 FAMILY
Very-High-Speed 1K (3K) Gate CMOS FPGA

pASIC HIGHLIGHTS

- **Very High Speed** – ViaLink™ metal-to-metal programmable–via antifuse technology, allows counter speeds over 100 MHz, and logic cell delays of under 4 ns.
- **High Usable Density** – An 8-by-12 array of 96 logic cells provides 3000 total available, with 1000 typically usable "gate array" gates in 44- and 68-pin PLCC, and 100-pin Thin PQFP packages.
- **Low-Power, High-Output Drive** – Stand-by current typically 2 mA. A 16-bit counter operating at 100 MHz consumes 50 mA. Minimum IOL and IOH of 8 mA.
- **Flexible FPGA Architecture** – The pASIC™ logic cell supports efficient, high-speed arithmetic, counter, data path, state machine and random logic applications with up to 14-input gates.
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using third-party, CAE tools. Fast, fully automatic place and route on PC and workstation platforms.

...3000 total available gates

QL8x12 Block Diagram



96 Logic Cells

▪ = Up to 56 I/O cells, 6 Input high-drive cells, 2 Input/CLK (high-drive) cells.

QUICKLOGIC

PRODUCT SUMMARY

The QL8x12 is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC (pASIC) devices. The 96-logic cell field-programmable gate array (FPGA) offers up to 3000 total available, with 1000 typically usable "gate array" gates (equivalent to 3000 gate claims of EPLD or LCA vendors) of high-performance general-purpose logic in 44- and 68-pin plastic leaded chip carrier packages.

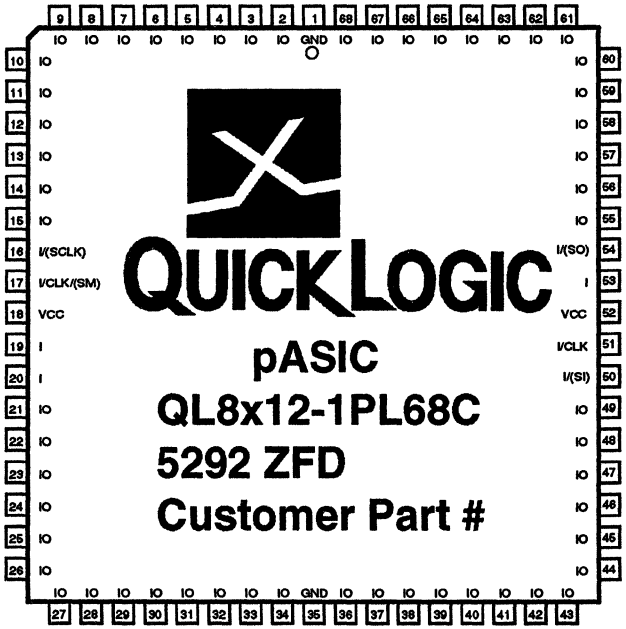
Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating at counter speeds above 100 MHz. Combined with input delays of 2 ns and output delays under 4 ns, this permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

Designs are entered into the QL8x12 using a pASIC Toolkit combining third-party general-purpose design entry and simulation tools with device-specific place and route and programming software. Ample on-chip routing channels are provided to allow fast, fully automatic place and route of high gate utilization designs.

FEATURES

- 56 Bidirectional Input/Output pins
- 8 Dedicated Input/High-Drive Clock pins
- Input + logic cell + output delays under 9 ns
- Chip-to-chip operating frequencies up to 85 MHz
- Internal state machine frequencies up to 100 MHz
- Clock skew <2 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing with Automatic Test Vector Generation (ATVG) software after programming
- Ample routing tracks permit fully automatic place and route of designs using up to 100% of internal logic cells
- 68-pin PLCC compatible with EPLD 1800 and LCA 2064 industry-standard pinouts
- 1μ CMOS gate array process with ViaLink programming technology

Pinout Diagram 44-pin PLCC



Pinout Diagram 68-pin PLCC

Pins identified I/SCLK, SM, SO, and SI are used during scan path testing operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... –0.5 to 7.0V
Input Voltage ..... –0.5 to VCC +0.5V
ESD Pad Protection ..... ± 2000V
DC Input Current ..... ± 20 mA
Latch-up Immunity ..... ±100 mA

Storage Temperature
Ceramic ..... –65°C to + 150°C
Plastic ..... –40°C to + 125°C
Lead Temperature ..... 300°C

OPERATING RANGE

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-0 Speed Grade	0.39	2.12	0.4	1.94	0.46	1.80	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade					0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage	IOH = -4 mA	3.7		V
		IOH = -8 mA	2.4		V
		IOH = -10 µA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 8 mA		0.4	V
		IOL = 10 µA		0.1	V
II	Input Leakage Current	VI = VCC or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	µA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current	VO = GND	-10	-80	mA
		VO = VCC	30	140	mA
ICC	Supply Current [2]	VI, VIO = VCC or GND		10	mA

Notes:

[1] CI = 20 pF Max on Pin 50

[2] For AC conditions use the formula described in Section 5 — Power vs Operating Frequency.

[3] Worst case Propagation Delay times over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range. All inputs are TTL with 3 ns linear transition time between 0 and 3 volts.

AC CHARACTERISTICS at VCC = 5V, TA = 25°C (K = 1.00)

Logic Cell

Symbol	Parameter	Propagation Delays (ns) [3] Fanout				
		1	2	3	4	8
tPD	Combinatorial Delay [4]	3.6	4.0	4.4	5.0	8.3
tSU	Setup Time [4]	3.9	3.9	3.9	3.9	3.9
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	3.0	3.3	3.8	4.3	4.9
tSET	Set Delay	2.7	3.1	3.5	4.1	7.4
tRESET	Reset Delay	2.9	3.2	3.6	4.2	7.5
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0
tCWLO	Clock Low Time	3.6	3.6	3.6	3.6	3.6
tSW	Set Width	2.1	2.1	2.1	2.1	2.1
tRW	Reset Width	1.9	1.9	1.9	1.9	1.9

Input Cells

Symbol	Parameter	Propagation Delays (ns) [3] Fanout				
		1	2	3	4	8
tIN	Input Delay (high drive)	3.7	3.8	4.2	4.6	6.4
tINI	Input, Inverting Delay (high drive)	3.5	3.6	4.0	4.4	6.2
tIO	Input Delay (bidirectional pad)	2.3	2.6	3.2	4.1	5.5

Output Cell

Symbol	Parameter	Propagation Delays (ns) [3] Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	3.1	3.8	4.6	5.5	7.2
tOUTHL	Output Delay High to Low	3.1	3.9	5.0	6.1	8.3
tPZH	Output Delay Tri-state to High	4.4	5.3	6.5	7.7	10.1
tPZL	Output Delay Tri-state to Low	4.0	4.6	5.4	6.2	7.7
tPHZ	Output Delay High to Tri-state [5]	3.3				
tPLZ	Output Delay Low to Tri-state [5]	3.7				

Notes:

[4] These limits are derived from worst case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.

[5] The following loads are used for tPXZ:

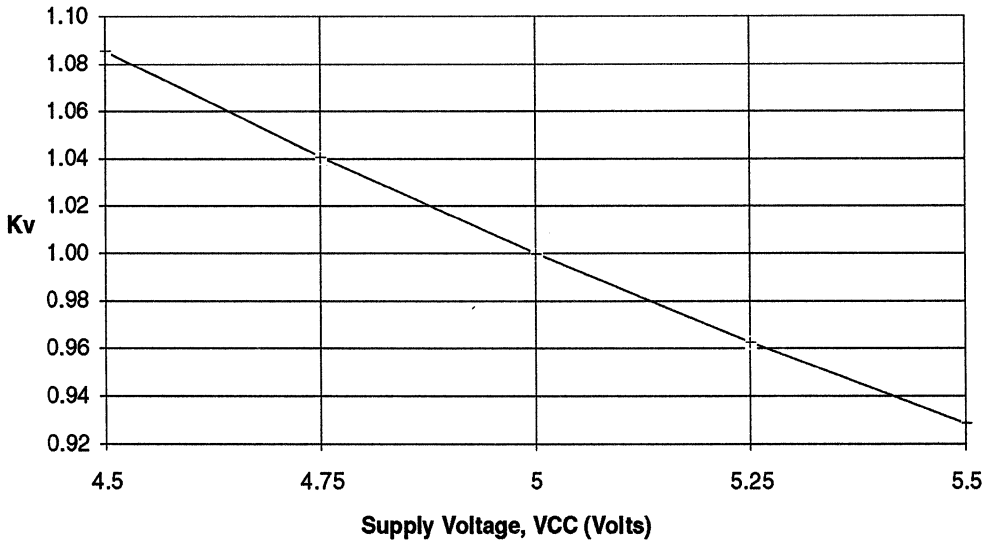
Clock Driver

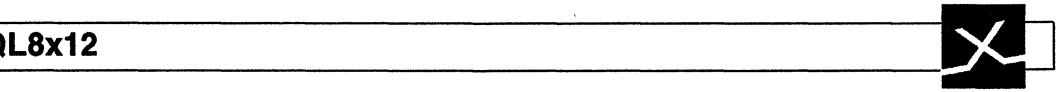
Symbol	Parameter	Clock Drivers Wired Together	Propagation Delays (ns) [3] Fanout				
			12	24	48	72	96
tCKD	Clock Driver Delay	1	4.8	6.8			
		2		4.8	6.1		
		3			5.4	6.4	7.5
		4				5.8	6.2
tCKDI	Clock Driver, Inverting Delay	1	5.2	7.2			
		2		5.1	6.4		
		3			5.7	6.7	7.3
		4				6.2	6.5

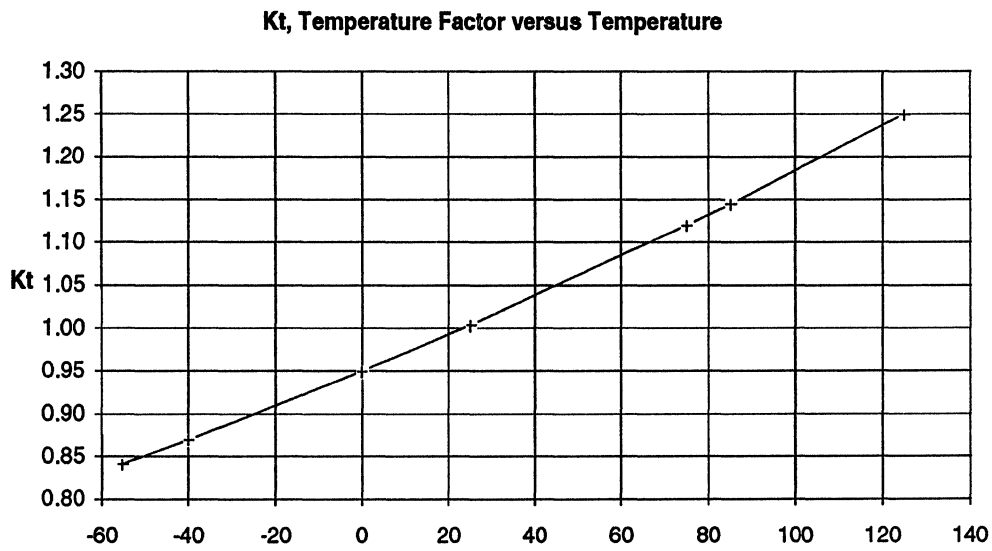
AC Performance

Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Operating Range. The effects of voltage and temperature variation are illustrated in the following graphs. The SpDE Toolkit incorporates data sheet AC Characteristics into the QDIF database for pre-place-and-route simulations. The SpDE Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

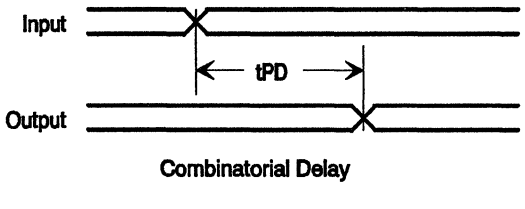
Kv, Voltage Factor versus Vcc, Supply Voltage

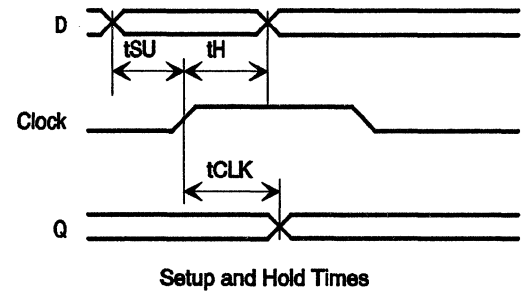


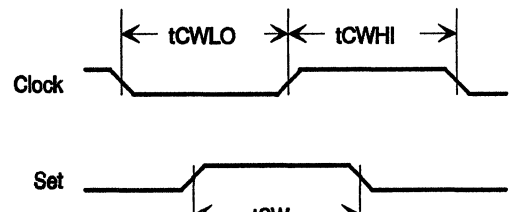


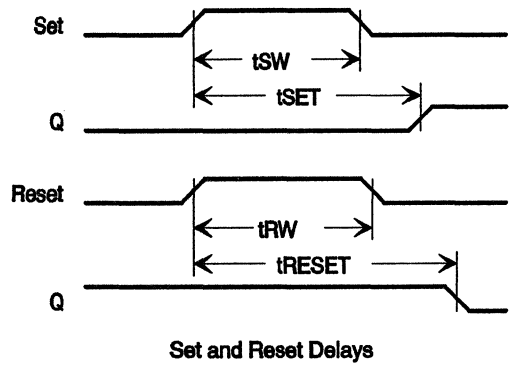


Timing Waveforms



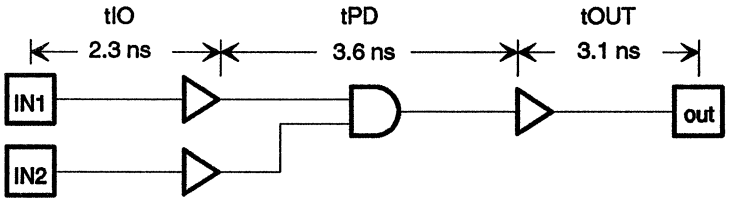






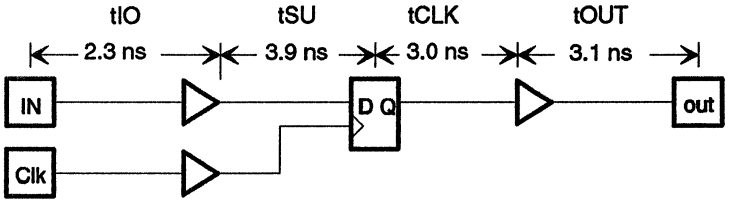
Combinatorial Delay Example

Nominal I/O Delays Load = 30 pF



Input Delay + Combinatorial Delay + Output Delay = 9.0 ns

Sequential Delay Example



Input Delay + Reg Setup + Clock to Output + Output Delay = 12.3 ns

ORDERING INFORMATION

QL 8x12 -1 PL68 C

- **QL** — QuickLogic pASIC device prefix
- **8x12** — pASIC device part number for 8 by 12 array of 96 logic cells
- **-1** — Speed Grade (see data sheet)
- **PL68** — Package Code
  - First Letter
    - P = Plastic
    - C = Ceramic
  - Second Letter
    - L = LCC
    - F = QFP
    - G = PGA
  - Number of Leads
    - 68 = 68 Leads
- **C** — Operating Range
  - C = Commercial
  - I = Industrial
  - M = Military

QL12x16
pASIC 1 FAMILY
Very-High-Speed 2K (6K) Gate CMOS FPGA

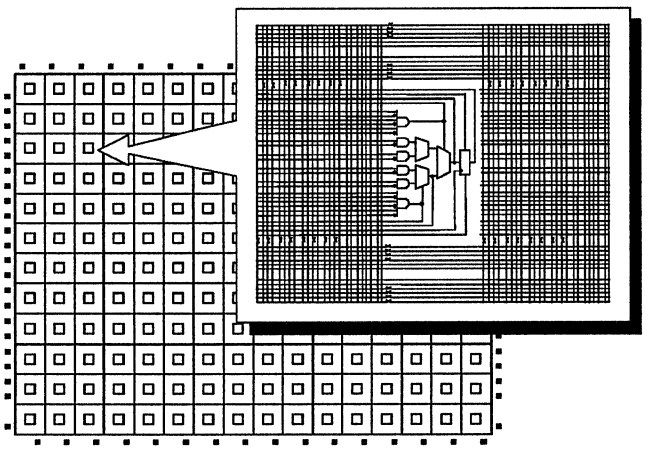
pASIC HIGHLIGHTS

- **Very High Speed** – ViaLink™ metal-to-metal programmable-via antifuse technology, allows counter speeds over 100 MHz, and logic cell delays of under 4 ns.
- **High Usable Density** – A 12-by-16 array of 192 logic cells provides 6000 total available, with 2000 typically usable "gate array" gates in 84- and 68-pin PLCC packages, and a 100-pin Thin PQFP package.
- **Low-Power, High-Output Drive** – Stand-by current typically 2 mA. A 16-bit counter operating at 100 MHz consumes 50 mA. Minimum IOL and IOH of 8 mA.
- **Flexible FPGA Architecture** – The pASIC™ logic cell supports efficient, high-speed arithmetic, counter, data path, state machine and random logic applications with up to 14-input gates.
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using third-party, CAE tools. Fast, fully automatic place and route on PC and workstation platforms.

...6000 total available gates

QL12x16 Block Diagram

192 logic cells



■ = Up to 68 I/O cells, 6 Input high-drive cells, 2 Input/CLK (high-drive) cells.

QUICKLOGIC

PRODUCT SUMMARY

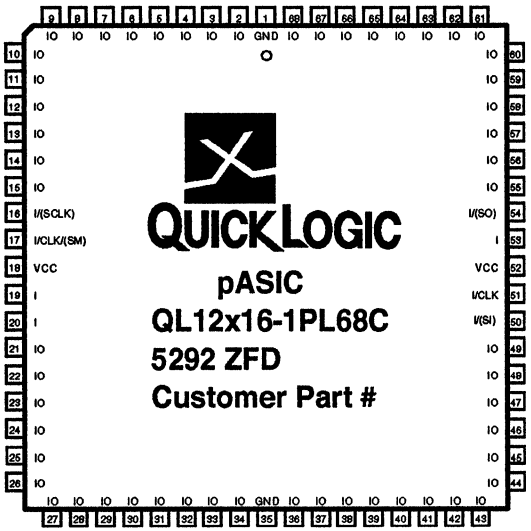
The QL12x16 is a member of the pASIC 1 Family of very-high-speed CMOS user-programmable ASIC (pASIC) devices. The 192 logic cell field-programmable gate array (FPGA) offers up to 6000 total available, with 2000 typically usable "gate array" gates (equivalent to 6000 gate claims of EPLD or LCA vendors) of high-performance general-purpose logic in 68- and 84-pin plastic leaded chip carrier packages.

Low-impedance, metal-to-metal, ViaLink interconnect technology provides nonvolatile custom logic capable of operating at counter speeds above 100 MHz. Combined with input delays of 2 ns and output delays under 4 ns, this permits high-density programmable devices to be used with today's fastest CISC and RISC microprocessors.

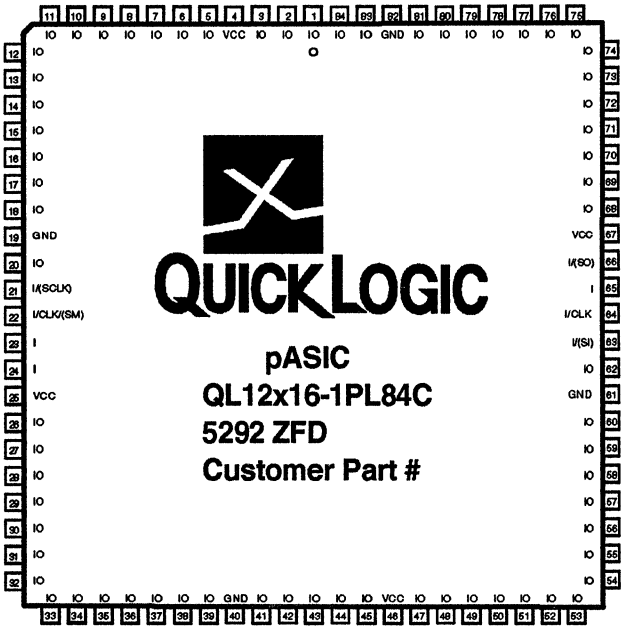
Designs are entered into the QL12x16 using a pASIC Toolkit combining third-party general-purpose design entry and simulation tools with device-specific place and route and programming software. Ample on-chip routing channels are provided to allow fast, fully automatic place and route of high gate utilization designs.

FEATURES

- 68 Bidirectional Input/Output pins
- 6 Dedicated Input/High-Drive pins
- 2 Clock/Dedicated input pins with fanout-independent, low-skew clock nets
- Input + logic cell + output delays under 9 ns
- Chip-to-chip operating frequencies up to 85 MHz
- Internal state machine frequencies up to 100 MHz
- Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells and functional testing with Automatic Test Vector Generation (ATVG) software after programming
- Ample routing tracks permit fully-automatic place and route of designs using up to 100% of internal logic cells
- 84-pin PLCC compatible with ACT1020 power supply and ground pinouts
- 68-pin PLCC compatible with QL8x12 footprint for easy upgrade of designs.
- 1µ CMOS gate array process with ViaLink programming technology



Pinout Diagram 68-pin PLCC



Pinout Diagram 84-pin PLCC

Pins identified I/SCLK, SM, SO and SI are used during scan path testing operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... –0.5 to 7.0V
Input Voltage ..... –0.5 to VCC +0.5V
ESD Pad Protection ..... ± 2000V
DC Input Current ..... ± 20 mA
Latch-up Immunity ..... ±100 mA

Storage Temperature
Ceramic ..... –65°C to +150°C
Plastic ..... –40°C to +125°C
Lead Temperature ..... 300°C

OPERATING RANGE

			Military		Industrial		Commercial		
Symbol	**Parameter**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
VCC	Supply Voltage		4.5	5.5	4.5	5.5	4.75	5.25	V
TA	Ambient Temperature		-55		-40	85	0	70	°C
TC	Case Temperature			125					°C
K	Delay Factor	-0 Speed Grade	0.39	2.12	0.4	1.94	0.46	1.80	
		-1 Speed Grade	0.39	1.56	0.4	1.43	0.46	1.33	
		-2 Speed Grade					0.46	1.25	

DC CHARACTERISTICS over operating range

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	Input HIGH Voltage		2.0		V
VIL	Input LOW Voltage			0.8	V
VOH	Output HIGH Voltage	IOH = -4 mA	3.7		V
		IOH = -8 mA	2.4		V
		IOH = -10 µA	VCC-0.1		V
VOL	Output LOW Voltage	IOL = 8 mA		0.4	V
		IOL = 10 µA		0.1	V
II	Input Leakage Current	VI = VCC or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCC or GND	-10	10	µA
CI	Input Capacitance [1]			10	pF
IOS	Output Short Circuit Current	VO = GND	-10	-80	mA
		VO = VCC	30	140	mA
ICC	Supply Current [2]	VI, VIO = VCC or GND		10	mA

Notes:

[1] CI = 20 pF Max on Pin 63

[2] For AC conditions use the formula described in Section 5 — Power vs Operating Frequency.

[3] Clock buffer fanout refers to the maximum number of flip flops per half column. The number of half columns used does not affect clock buffer delay.

[4] Worst case Propagation Delay times over process variation at VCC = 5.0V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range. All inputs are TTL with 3 ns linear transition time between 0 and 3 volts.

AC CHARACTERISTICS at VCC = 5V, TA = 25°C (K = 1.00)

Logic Cell

Symbol	Parameter	Propagation Delays (ns) [4] Fanout				
		1	2	3	4	8
tPD	Combinatorial Delay [5]	3.4	3.8	4.2	4.8	8.1
tSU	Setup Time [5]	3.7	3.7	3.7	3.7	3.7
tH	Hold Time	0.0	0.0	0.0	0.0	0.0
tCLK	Clock to Q Delay	3.0	3.3	3.8	4.3	4.9
tSET	Set Delay	2.7	3.1	3.5	4.1	7.4
tRESET	Reset Delay	2.9	3.2	3.6	4.2	7.5
tCWHI	Clock High Time	2.0	2.0	2.0	2.0	2.0
tCWLO	Clock Low Time	3.6	3.6	3.6	3.6	3.6
tSW	Set Width	2.1	2.1	2.1	2.1	2.1
tRW	Reset Width	1.9	1.9	1.9	1.9	1.9

Input Cells

Symbol	Parameter	Propagation Delays (ns) [4] Fanout				
		1	2	3	4	8
tIN	Input Delay (high drive)	3.7	3.8	4.2	4.6	6.4
tINI	Input, Inverting Delay (high drive)	3.5	3.6	4.0	4.4	6.2
tIO	Input Delay (bidirectional pad)	2.3	2.6	3.2	4.1	5.5
tGCK	Clock Buffer Delay [3]	4.4	4.5	4.6	4.6	5.0

Output Cell

Symbol	Parameter	Propagation Delays (ns) [4] Output Load Capacitance (pF)				
		30	50	75	100	150
tOUTLH	Output Delay Low to High	3.1	3.8	4.6	5.5	7.2
tOUTHL	Output Delay High to Low	3.1	3.9	5.0	6.1	8.3
tPZH	Output Delay Tri-state to High	4.4	5.3	6.5	7.7	10.1
tPZL	Output Delay Tri-state to Low	4.0	4.6	5.4	6.2	7.7
tPHZ	Output Delay High to Tri-state [6]	3.3				
tPLZ	Output Delay Low to Tri-state [6]	3.7				

Notes:

[5] These limits are derived from worst case values for a representative selection of the slowest paths through the pASIC logic cell including net delays. Guaranteed delay values for specific paths should be determined from simulation results.

[6] The following loads are used for tPXZ:

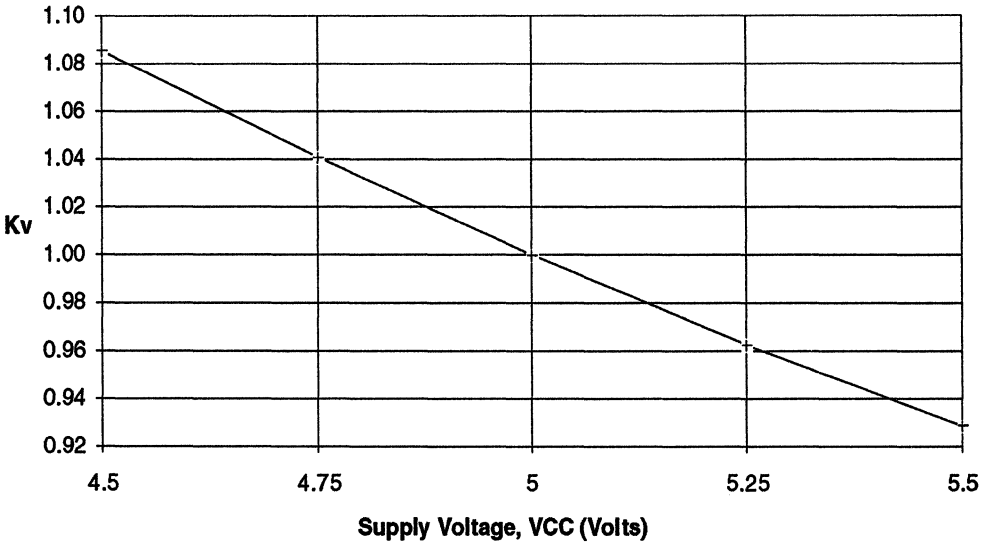
High Drive Buffer

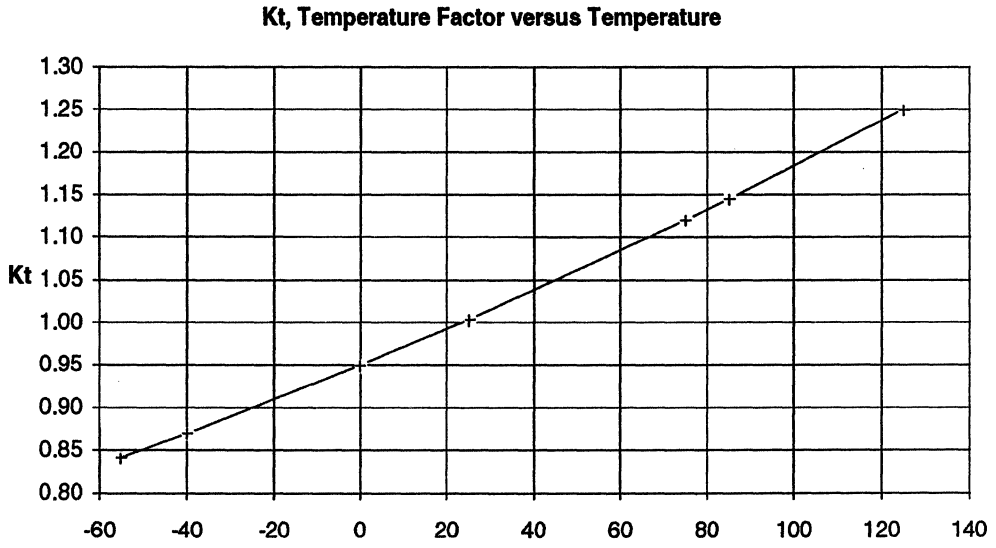
Symbol	Parameter	# High Drives Wired Together	Propagation Delays (ns) [4] Fanout				
			12	24	48	72	96
tIN	High Drive Input Delay	1	7.9	11.2			
		2		8.0	9.7		
		3			8.6	10.4	11.8
		4				9.4	10.8
tINI	High Drive Input, Inverting Delay	1	7.5	10.8			
		2		7.5	9.3		
		3			8.2	10.0	11.8
		4				9.0	10.8

AC Performance

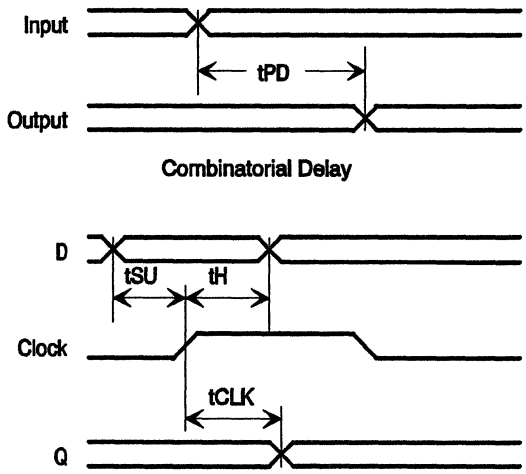
Propagation delays depend on routing, fanout, load capacitance, supply voltage, junction temperature, and process variation. The AC Characteristics are a design guide to provide initial timing estimates at nominal conditions. Worst case estimates are obtained when nominal propagation delays are multiplied by the appropriate Delay Factor, K, as specified in the Operating Range. The effects of voltage and temperature variation are illustrated in the graphs below. The SpDE Toolkit incorporates data sheet AC Characteristics into the QDIF database for pre-place-and-route simulations. The SpDE Delay Modeler extracts specific timing parameters for precise simulation results following place and route.

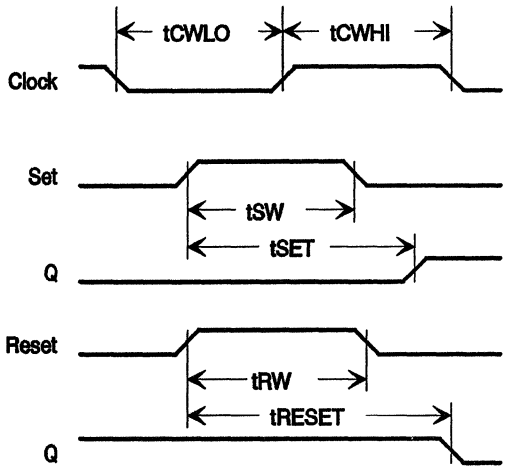
Kv, Voltage Factor versus Vcc, Supply Voltage





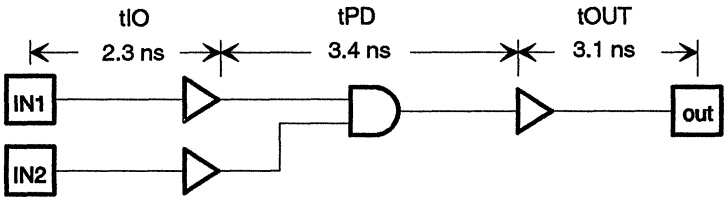
Timing Waveforms





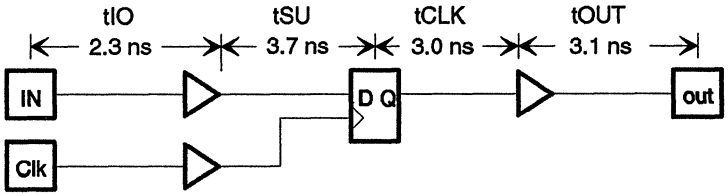
Combinatorial Delay Example

Nominal I/O Delays Load = 30 pF



Input Delay + Combinatorial Delay + Output Delay = 8.8 ns

Sequential Delay Example



Input Delay + Reg Setup + Clock to Output + Output Delay = 12.1 ns

ORDERING INFORMATION

QL 12x16 -1 PL84 C

- **QL** — QuickLogic pASIC device prefix
- **12x16** — pASIC device part number for 12 by 16 array of 192 logic cells
- **-1** — Speed Grade (see data sheet)
- **PL84** — Package Code
  - First Letter
    - P = Plastic
    - C = Ceramic
  - Second Letter
    - L = LCC
    - F = QFP
    - G = PGA
  - Number of Leads
    - 84 = 84 Leads
- **C** — Operating Range
  - C = Commercial
  - I = Industrial
  - M = Military

QL16x24
pASIC 1 FAMILY
Very-High-Speed 4K (12K) Gate CMOS FPGA

ADVANCE DATA

pASIC HIGHLIGHTS

- **Very High Speed** – ViaLink™ metal-to-metal programmable–via antifuse technology, allows counter speeds over 100 MHz, and logic cell delays of under 4 ns.
- **High Usable Density** – A 16-by-24 array of 384 logic cells provides 12,000 total available, with 4000 typically usable "gate array" gates.
- **Low-Power, High-Output Drive** – Stand-by current typically 2 mA. A 16-bit counter operating at 100 MHz consumes 50 mA. Minimum IOL and IOH of 8 mA.

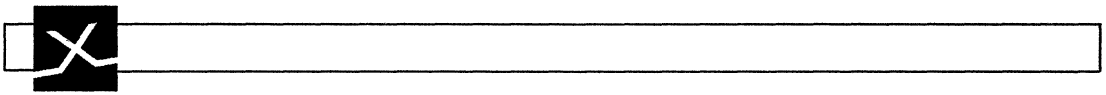
...4000 useable gates

- **Flexible FPGA Architecture** – The pASIC™ logic cell supports efficient, high-speed arithmetic, counter, data path, state machine and random logic applications with up to 14 input gates.
- **Low-Cost, Easy-to-Use Design Tools** – Designs entered and simulated using third-party, CAE tools. Fast, fully automatic place and route on PC and workstation platforms.

FEATURES

- 104 Bidirectional Input/Output pins
- 6 Dedicated Input/High-Drive pins
- 2 Clock/Dedicated input pins with fanout-independent low-skew clock rates
- Input + logic cell + output delays under 9 ns
- Clock skew <1 ns
- Input hysteresis provides high noise immunity
- Built-in scan path permits 100% factory testing of logic and I/O cells
- Ample routing tracks permit fully-automatic place and route of designs
- 100 and 144 PQFP
- 84-pin PLCC compatible with QL12x16 footprint for easy upgrade of designs

QUICKLOGIC



pASIC TOOLKIT 3.0
Windows Development System for Very-High-Speed FPGAs

HIGHLIGHTS

- **Third-party Design Entry and Simulation Tools** that are general purpose and can be used for the total system design task.
- **pASIC™ architecture-specific place and route algorithms** to optimize speed and density of the QuickLogic pASIC devices.
- **Microsoft Windows™ industry-standard user interface** that gives the user a consistent graphical interface across third-party and QuickLogic Applications.
- **Automatic Test Vector Generation** for fast, easy testing of programmed devices.
- **Everything included,** from the programmer to the wrist strap so you can get started immediately.

Everything included, down to the wrist strap

QUICKLOGIC

INTRODUCTION

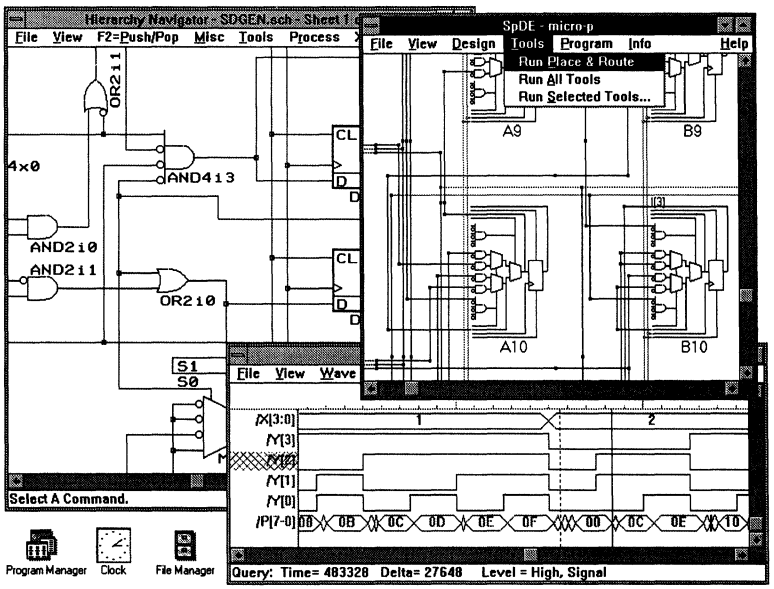
...Windows 3.0 on the PC

The pASIC Toolkit 3.0 is a fully integrated solution for the design and programming of QuickLogic FPGA devices. It combines the Engineering Capture System, (ECS™), from CAD/CAM Group and the X-SIM™ simulator from Silicon Automation Systems with the Seamless pASIC Design Environment (SpDE - pronounced Speedy) tools from QuickLogic. All tools operate efficiently and interactively under the Microsoft Windows™ graphical user interface on the PC. SpDE tools include automatic place and route (APR), delay modeling, and automatic test vector generation. Additional third-party simulation and synthesis, as well as schematic, equation, and language design entry tools are supported via the Open QuickLogic Design Interchange Format (QDIF) interface.

THE pASIC TOOLKIT 3.0

The pASIC Toolkit 3.0 is a comprehensive set of tools for designing, simulating, programming and testing QuickLogic programmable ASIC devices on the PC. The entire toolkit runs under Microsoft Windows for a consistent user interface and a unified design environment across all applications (Figure 1). While easy to learn, these are very powerful tools which ensure a highly efficient and productive development solution for the experienced designer.

FIGURE 1
A Windows view of the schematic, simulation and physical editor tools



Key Features and Benefits

Features	Benefits
Object-oriented database architecture.	Clean, efficient communication between QuickLogic and third-party tools.
Windows eliminates DOS memory limitations.	Complex simulation can be performed on the PC.
Windows hardware compatibility.	Wide variety of graphics cards, printers and plotters supported.
Cut and paste schematics, waveforms, etc. between applications.	Simplifies system documentation.
Advanced RC timing delay modeler based on AWE.	Accurate delay extraction and back annotation to simulator.
Post-layout physical viewer.	Visual display of results of place and route for design optimization.
Cross probing between schematic, simulation and physical viewer.	Nodes selected in one application are highlighted in another.

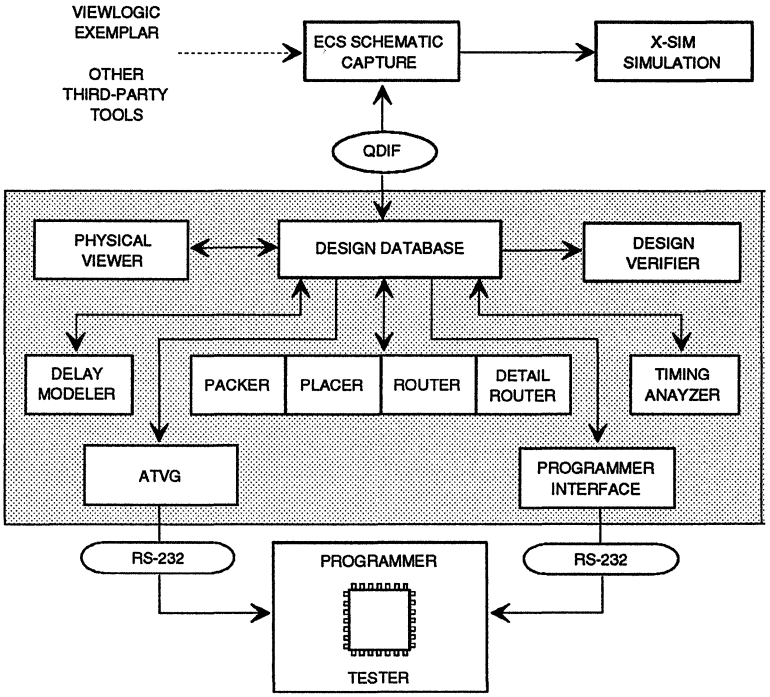
pASIC TOOLKIT 3.0 SOFTWARE AND HARDWARE TOOLS

The pASIC Toolkit 3.0 includes the following software and hardware tools:

- Schematic capture
- Support for language and equation entry
- Simulation
- Automatic placement and routing (APR)
- Post-layout delay extraction and back-annotation
- Path timing analysis
- Physical layout viewer
- Automatic test vector generation (ATVG)
- Device programmer/tester

All applications are tightly integrated within a high-performance design framework (Figure 2). An open database file format provides access to the framework for additional user or third-party tools. The pASIC Toolkit is the most modern and powerful development system available for designing FPGA devices today.

FIGURE 2
The pASIC Toolkit



THE pASIC TOOLKIT 3.0

The pASIC Toolkit 3.0 includes two of the most advanced third-party CAE packages for system design. The Engineering Capture System, ECS™, from CAD/CAM Group and X-SIM from Silicon Automation Systems.

Design Entry

ECS is the most widely used Windows-based schematic capture system in the industry. ECS includes a Schematic Editor, Symbol Editor and a Hierarchy Navigator. The Schematic Editor is a highly flexible design-entry tool capable of handling complex hierarchical designs. This package supports multisheet designs, and to prevent many common errors, the system maintains network connectivity as the schematic is entered. The Symbol Editor allows easy creation of symbols. The Hierarchy Navigator is a tool which loads the entire schematic database into memory. This enables the user to easily navigate the hierarchy of the entire design without having to repetitively load individual schematics. The Hierarchy Navigator also forms a bridge between the design database, the X-SIM Simulator and QuickLogic's device-optimized tools.

The pASIC Macro Library contains more than 200 logic elements, including 2-input to 14-input AND gates and high-complexity logic functions. The library includes a comprehensive selection of registers, counters, and arithmetic blocks as well as most of the familiar 7400 series TTL building blocks.

Design Simulation

The X-SIM functional and timing event-driven simulation engine has been integrated into the ECS Waves Tool. Originally developed for full system simulation on high-end workstations, its high-performance design provides rapid simulation with efficient memory utilization. The X-SIM simulator includes setup and hold violation reporting using completely back-annotated Asymptotic Waveform Evaluation (AWE) generated delay results. The ECS Waves Tool provides an interactive logic analyzer interface to X-SIM for stimulus entry and results interpretation.

Design Compilation

QuickLogic's architecture-specific design compilation tool set is comprised of pASIC architecture-specific modules, collectively called SpDE. These include the automatic place and route modules (Packer, Placer, and Router), the Physical Viewer, timing analysis modules (Delay Modeler and Timing Analyzer), Automatic Test Vector Generation (ATVG) and programming modules. See the QuickLogic SpDE Tools data sheet for a description of the SpDE modules.

The Physical Viewer is a unique tool that shows the user how the automatic place and route tools have mapped a logic design into the silicon resources. As all tools are based on a common design database structure, the user can take advantage of the ability to cross probe between applications. For example, a net on the physical layout displayed by the Physical Viewer can be selected within the viewer, and its logical counterpart will be highlighted within the ECS schematic tool. Alternatively, a net can be selected on the ECS schematic and its corresponding physical layout will be highlighted in the viewer. Similar tight coupling is supported between the ECS schematic and the X-SIM waveform driven simulator. This tight interaction between the logical and physical representations gives the user a high degree of control over the evaluation of critical speed paths.

Programming and Testing

A Programmer Interface translates the results of the APR process into the patterns required to program pASIC devices and transmits them, together with test vectors generated by the Automatic Test Vector Generator, over an RS-232 link to the programmer.

The Designer Programmer/Tester is a low-cost programming and testing unit for QuickLogic pASIC devices. The model DP-PL84 accepts 84-lead plastic PLCC devices directly. Other packages are supported by individual adapters.

pASIC TOOLKIT 3.0 CONTENTS PART NUMBER QT-3.0

The pASIC Toolkit 3.0 contains all the software and hardware required to produce complete custom designs in QuickLogic pASIC devices, minus the PC workstation. It includes important but usually overlooked accessories such as cables, connectors and wrist straps. A software only version is available for design stations not requiring direct device programming support. A complete list of contents of each system is as follows:

- CAD/CAM Group Engineering Capture System and Macro Library
- Silicon Automation Systems X-SIM Simulator
- QuickLogic SpDE tools
  - Place and Route
  - Delay Modeler
  - Static Path Timing Analyzer
  - Physical Layout Viewer
  - Automatic Test Vector Generator
  - Interface to Exemplar Logic Synthesis Tools
- Programming Hardware
  - Programmer/Tester with socket for 84-pin PLCC devices
  - Adapter for 68-pin PLCC devices
  - AC adapter and cord
  - RS-232 cable
  - 9- to 25-pin adapter
  - Antistatic wrist strap
- Two QL8x12 device samples

pASIC TOOLKIT 3.0 SOFTWARE ONLY CONTENTS PART NUMBER QS-3.0

- CAD/CAM Group Engineering Capture System and Macro Library
- Silicon Automation Systems XSIM Simulator
- QuickLogic SpDE Tools
  - Place and Route
  - Delay Modeler
  - Static Path Timing Analyzer
  - Physical Layout Viewer
  - Automatic Test Vector Generator
  - Interface to Exemplar Logic Synthesis Tools

ECS AND X-SIM FOR GENERAL-PURPOSE SYSTEM DESIGN APPLICATIONS

The ECS and X-SIM software included in the pASIC Toolkit are specifically designed for QuickLogic's pASIC design libraries. Software upgrades that allow these tools to be used in general-purpose system design are available from their manufacturers.

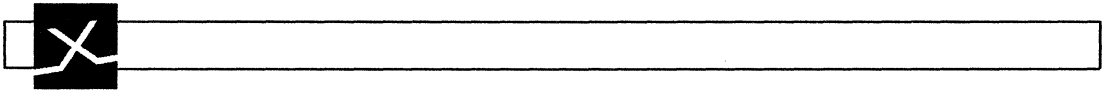
CAD/CAM Group's ECS software also supports Sun 3, Sun 4, and SPARCstations, as well as Macintosh II and SE/30 platforms. Industry-standard netlists to Verilog, Silos, Hilo, Futurenet, Cadnetix, VHDL, Spice, Racal-Redac and Pads are supported. Interfaces are also available to convert graphical and electrical data to ASCII and EDIF formats.

CAD/CAM also provides a general-purpose Windows-compatible version of X-SIM which is integrated with the ECS tool for the PC. X-SIM system level simulation software is available directly from Silicon Automation Systems for operation on Sun 3, Sun 4, IBM RISC 6000 series, and HP/Apollo DN2000, 3000, and 4000 series workstations.

PC SYSTEM REQUIREMENTS

The minimum software and hardware requirements for running the pASIC Toolkit are as follows:

- MS-DOS (or PC-DOS) version 3.1 or higher
- Microsoft Windows version 3.0 or higher
- 80386- or 80486-based personal computer
- 4 MBytes RAM
- Windows-supported monitor and graphics adapter (EGA, VGA)
- Windows-supported mouse
- 8 MBytes free hard disk space



pASIC Macro Library

HIGHLIGHTS

- More than 300 Architecturally Optimized Macros
- Includes Simple Gates and Advanced Soft Macros
- Includes Over 100 7400-Series TTL Building Blocks
- SpDE Packs as Many as 4 Macros Into a Single Logic Cell

INTRODUCTION

The pASIC™ Macro Library contains more than 300 macros. While these macros offer a wide range of functions and flexibility, they fall into familiar functional groups. The naming conventions employed in the library are easy to learn and remember—while 300 macros may seem like a daunting number at first, little experience is required to master the use of the library.

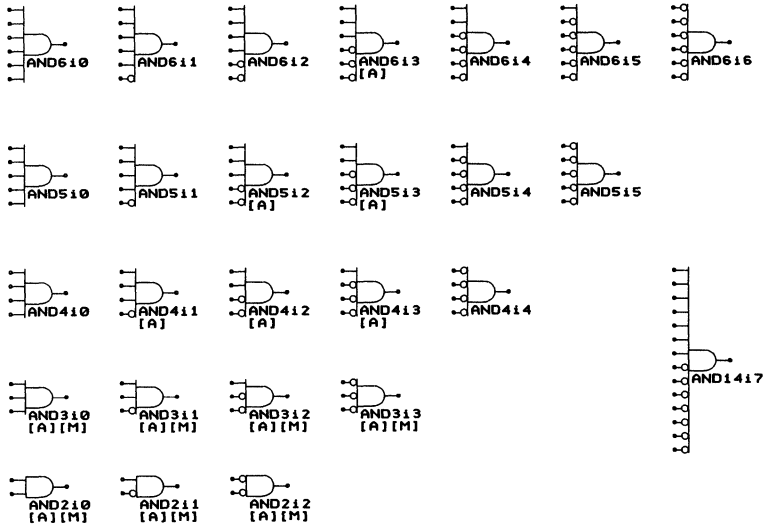
The remarkable flexibility of the pASIC logic cell allows literally millions of different hard macros to be created; not all of these are included in the macro library. Therefore, custom hard macros can be created easily using the pASIC logic cell. The logic cell represents the pASIC's basic building block—all macros are created out of logic cells at the lowest level. Although most designers will never need to design at the logic cell level, this option is available.

The pASIC Macro Library includes hard macros and soft macros. Hard macros provide simple functionality on a scale of two to twenty gates in complexity. Hard macros are implemented in one logic cell or a part of one logic cell. Soft macros provide more complex functionality, and are implemented in more than one logic cell.

Packing information is provided beneath many of the hard macros—an [A] or [M] or [Q] mark. Briefly, two [A]-type macros, one [M]-type macro, and one [Q]-type macro can be implemented in a single logic cell. The Packer (one of the SpDE tools included in the pASIC Toolkit) automatically performs this mapping of multiple macros into a single logic cell.

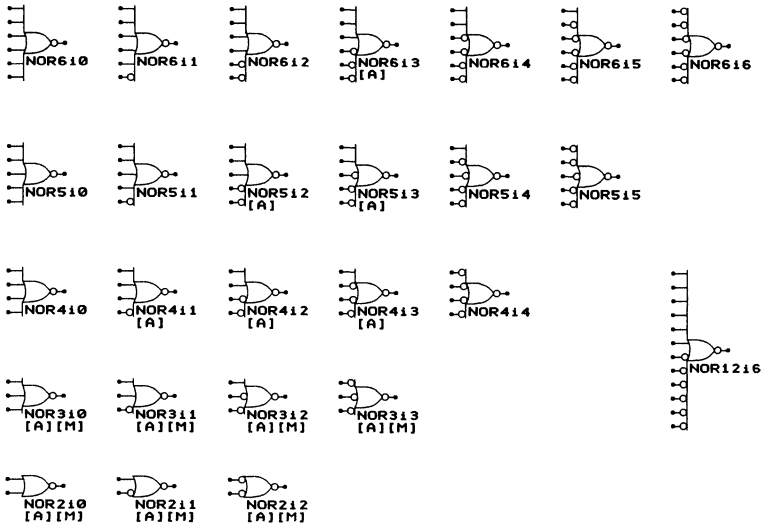
QUICKLOGIC

AND Gates

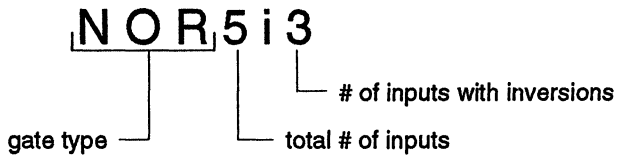


The pASIC Macro Library includes AND, NOR, NAND, and OR gates with two to six inputs. At each input count, all numbers of inversion bubbles are available (for example, 3-input gates are available with 0, 1, 2, and 3 inversion bubbles). The library also features the largest possible AND, NOR, NAND, and OR gates which can be implemented in a single logic cell (**AND14i7, NOR12i6, NAND13i6, OR12i6**).

NOR Gates

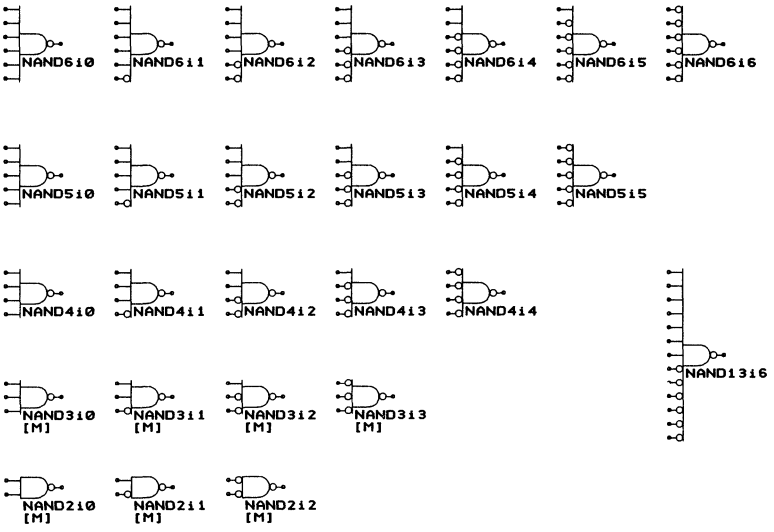


An easy-to-remember naming convention is employed to identify these gates.

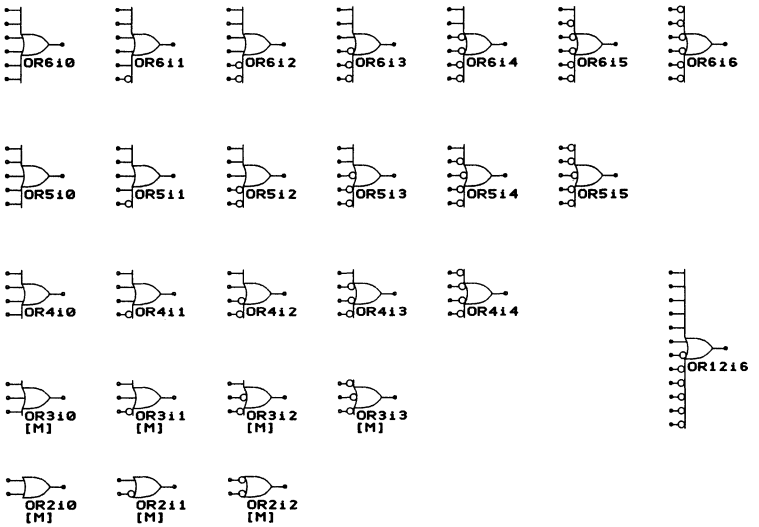


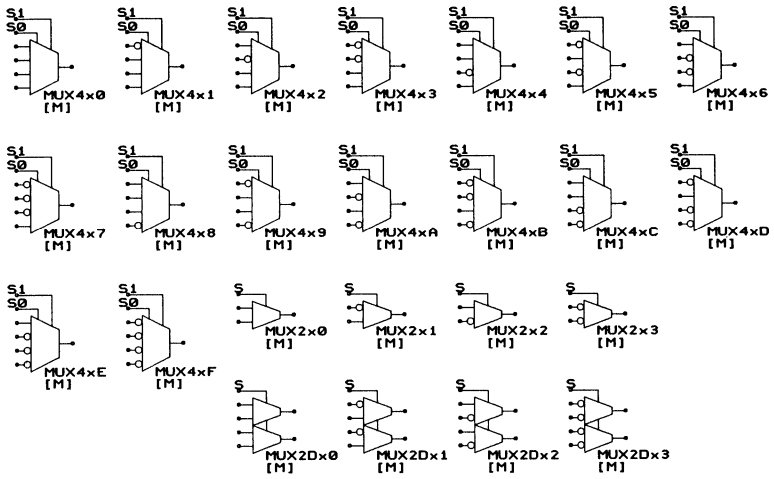
The first field identifies the type of gate—AND, NOR, NAND, OR. The second field specifies the total number of inputs. The 'i' character, which stands for "inverts," serves as a separator. The third field specifies the number of inputs with inversion bubbles.

NAND Gates



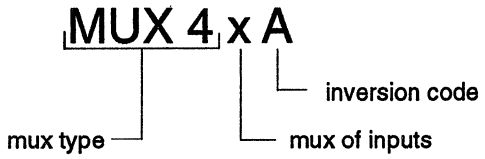
OR Gates





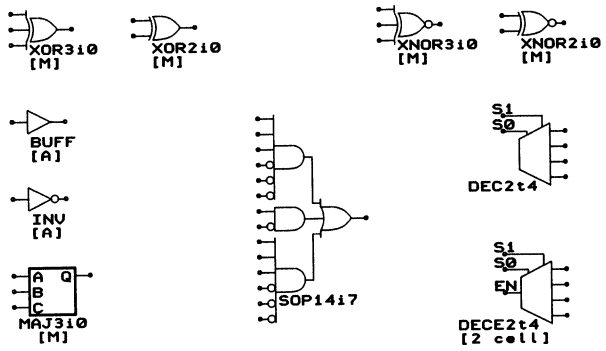
Multiplexers

The pASIC Macro Library includes sixteen 4-to-1 multiplexers, representing all possible combinations of inversion bubbles on the four inputs. The naming convention is similar to the AND, NOR, NAND, OR form explained above.



The first field, MUX, identifies this as a multiplexer. The second field specifies the number of inputs. The 'x' character serves as a separator. The third field specifies a hexadecimal code for the pattern of inversion bubbles.

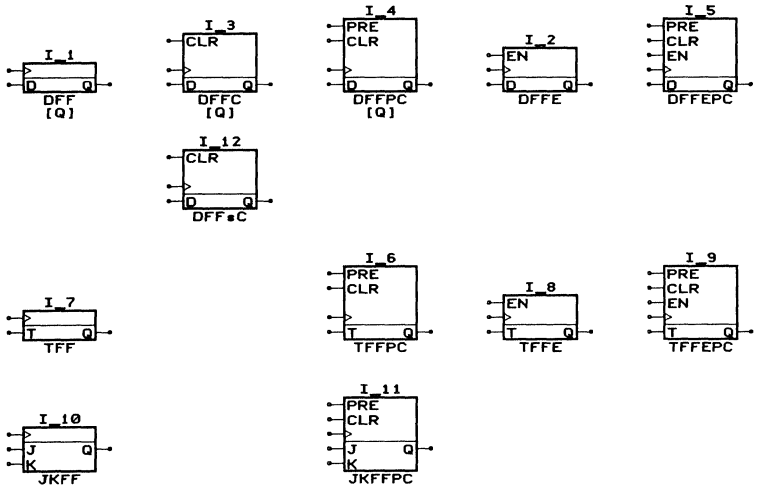
Other Combinational Macros



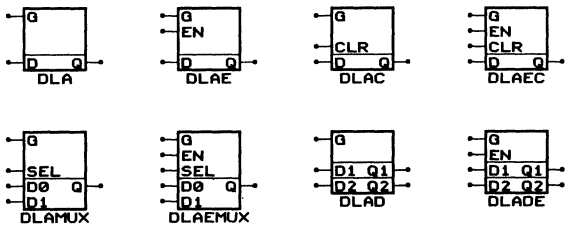
The pASIC Macro Library includes two and three input XOR (exclusive-or) and XNOR (exclusive-nor, also known as equivalence) gates. Their names use the same terminology as the AND, NOR, NAND, OR gates, although input inversion bubbles are not provided (Boolean algebra shows that an even number of input inversion bubbles is ignored, while an odd number of input inversion bubbles is transformed into an inversion bubble on the output).

The pASIC Macro Library does not include combination gates (AND-OR, OR-AND, AND-XOR, etc.) present in some macro libraries. There are literally thousands of possible combination gates which can be implemented in a single logic cell, which would make for a fairly large macro library. These combination gates are handled automatically by the Packer, as discussed earlier.

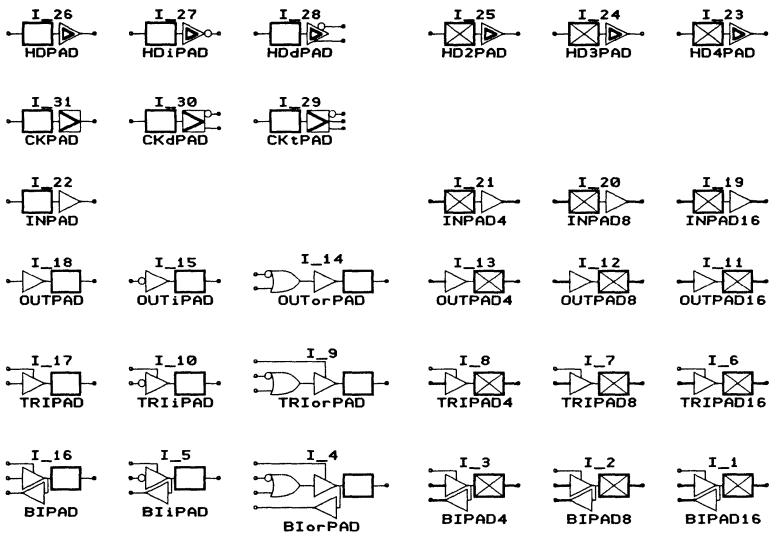
Flip Flops



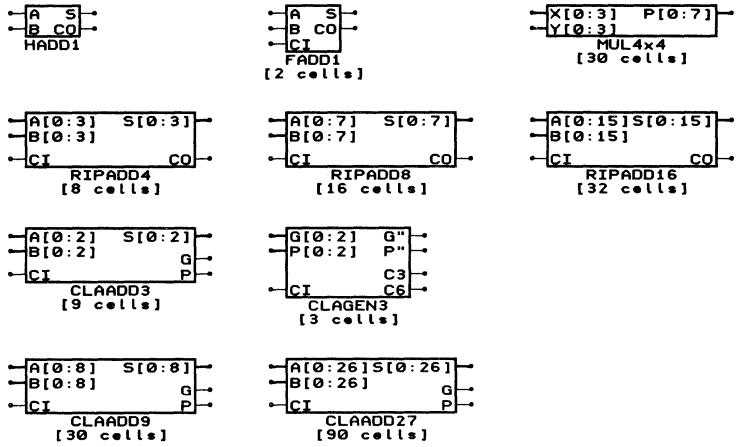
Latches



I/O Pads



Adders and Multipliers



The pASIC logic cell is well suited for high-speed arithmetic. It includes **HADD1**, a simple half-adder macro which can be implemented in less than one logic cell.

FADD1 is a full-adder which requires two logic cells. This soft macro contains one **XOR3i0** and one **MAJ3i0** macro.

RIPADD4, **RIPADD8**, and **RIPADD16** are ripple-carry adders of 4, 8, and 16 bits, respectively. Each utilizes the **FADD1** full-adder macro in a ripple-carry arrangement. This provides excellent density at the cost of additional logic delays, compared to the carry-look-ahead adders to be introduced shortly.

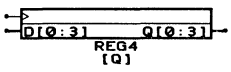
If high-speed addition is required, **CLAADD3** is a carry-look-ahead adder of three bits. The three-bit adder is designed in the spirit of the 7400-series '283—the control signals are identical, but the '283 is a four-bit device. As such, larger adders can be built with multiple **CLAADD3** macros and **CLAGEN3**, the latter being a carry-look-ahead generator similar to the 7400-series '282.

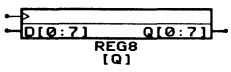
The nine-bit adder is built from three **CLAADD3** macros and one **CLAGEN3** macro. The following table illustrates the speed-density tradeoff between the ripple-carry adders and the carry-look-ahead adders.

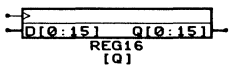
MUL4x4 is a four-by-four multiplier which offers excellent speed and excellent density. This macro's design takes advantage of the **XOR** utilization property mentioned above—two AND gates and a 3-input XOR gate can be packed into a single pASIC logic cell.

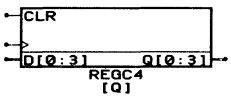
	Type	Levels	Cells
HADD1	half-adder	1	1
FADD1	full-adder	1	2
RIPADD4	4-bit ripple adder	4	8
RIPADD8	8-bit ripple adder	8	16
RIPADD16	16-bit ripple adder	16	32
CLAADD3	3-bit CLA adder	3	9
CLAGEN3	3-bit CLA generator	1	3
CLAADD9	9-bit CLA adder	4	30
CLAADD27	27-bit CLA adder	6	93
MUL4x4	4-by-4-bit multiplier	5	30

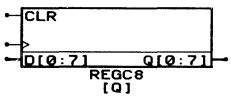
Registers

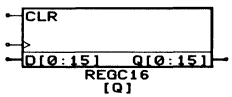


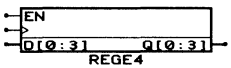


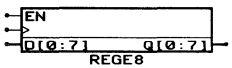


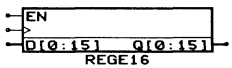


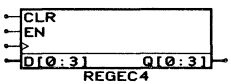


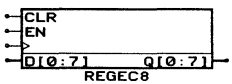


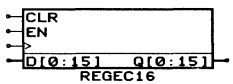




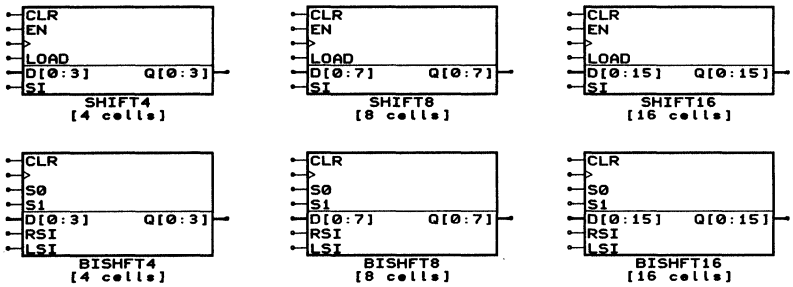






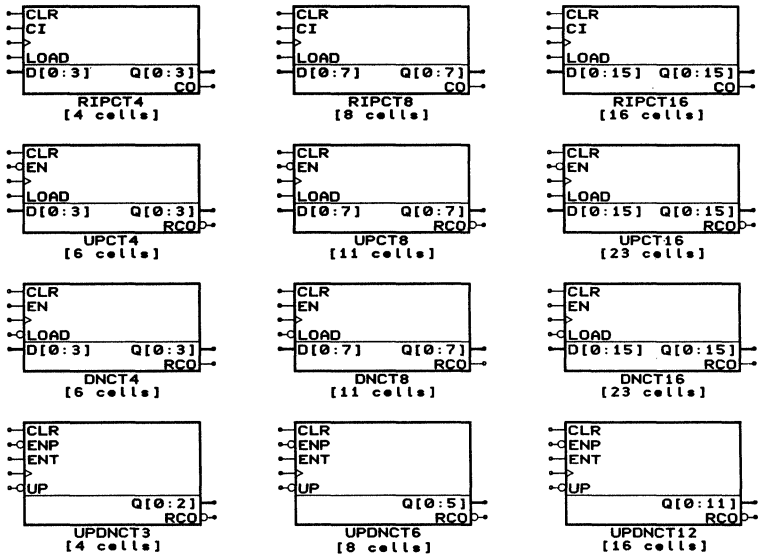


Shift Registers



The pASIC architecture can implement extremely fast shift registers. In fact, the shift registers included in the macro library can operate at the maximum logic cell toggle rate.

Counters



The pASIC architecture can produce extremely fast counters ("you can count on us"). Many of the counters in the macro library can operate near the maximum logic cell toggle rate.

The pASIC Macro Library includes ripple-carry counters (names starting with the prefix RIP) and parallel-carry counters. The following table illustrates the speed-density tradeoffs between these counters.

	Type	Bits	Levels	Cells
RIPCT4	up	4	4	4
RIPCT8	up	8	8	8
RIPCT16	up	16	16	16
UPCT4	up	4	1	6
UPCT8	up	8	1	11
UPCT16	up	16	1	23
DNCT4	down	4	1	6
DNCT8	down	8	1	11
DNCT16	down	16	1	23
UPDNCT3	up-down	3	1	4
UPDNCT6	up-down	6	2	8
UPDNCT12	up-down	12	2	16

The library includes up and down counters utilizing parallel carry designs. The 4-bit up counter UPCT4 is designed in the spirit of the 7400-series '161. The up and down counters have a common LOAD control signal, which causes the counter to be synchronously loaded from the D inputs when asserted. The 3-bit up-down counter UPDNCT3 is designed in the spirit of the 7400-series '169. There are two versions of this macro to allow them to be cascaded.

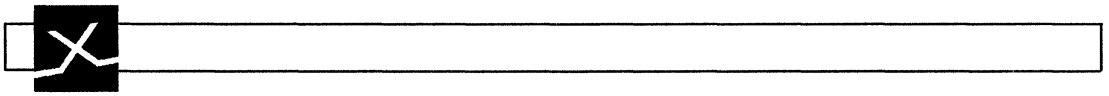
7400-Series TTL Macros

	Description
TTL02	quad 2-input NOR gates
TTL04	hex inverters
TTL08	quad 2-input AND gates
TTL11	triple 3-input AND gates
TTL21	dual 4-input AND gates
TTL27	triple 3-input NOR gates
TTL42q	4-to-10 decoder
TTL49	BCD to 7-segment decoder
TTL74q	dual D FFs with preset & clear
TTL77	4-bit D latch
TTL78q	dual J-K FFs with common clock & clear
TTL85	4-bit magnitude comparator
TTL86	quad 2-input XOR gates
TTL87	4-bit true/complement elements
TTL91	8-bit shift register
TTL98	4-bit data selector/storage register
TTL104q	gated J-K FF with preset & clear
TTL105q	gated J-K FF with preset & clear
TTL107q	dual J-K FFs with clear
TTL109q	dual J-K FFs with preset & clear
TTL116	dual 4-bit D latches with clear
TTL138q	3-to-8 decoder
TTL139q	dual 2-to-4 decoders
TTL145q	BCD to decimal decoder
TTL150	16-to-1 multiplexer
TTL152	8-to-1 multiplexer
TTL153	dual 4-to-1 multiplexers
TTL154q	4-to-16 decoder
TTL157	quad 2-to-1 multiplexers
TTL161	4-bit binary counter with asynchronous clear
TTL163	4-bit binary counter with synchronous clear
TTL164q	8-bit parallel-out shift register
TTL166q	8-bit parallel-load shift register
TTL169	4-bit binary up/down counter
TTL171q	quad D FFs with clear
TTL174q	hex D FFs with clear
TTL180	9-bit odd-even parity generator
TTL194q	4-bit bidirectional shift register
TTL240q	octal inverting tri-state drivers

7400-Series TTL Macros (continued)

	Description
TTL244q	octal noninverting tri-state drivers
TTL259	8-bit addressable latches
TTL261	2-bit by 4-bit binary multipliers
TTL268q	hex D latches
TTL273q	octal D FFs with clear
TTL278	4-bit cascadable priority register
TTL279	quad S-R latches
TTL295q	4-bit right-shift left-shift register
TTL365	hex tri-state drivers
TTL366	hex inverting tri-state drivers
TTL367	hex tri-state drivers, 4-bit/2- bit banks
TTL368	hex inverting tri-state drivers, 4-bit/2-bit banks
TTL373q	octal D latches
TTL374q	octal D FFs
TTL375	4-bit latches with dual polarity outputs
TTL376q	quad J-K FFs with clear
TTL395q	4-bit cascadable shift register with clear
TTL396	octal storage register
TTL465	octal tri-state buffers
TTL466	octal inverting tri-state buffers
TTL467	octal tri-state buffers, 4-bit/4-bit banks
TTL468	octal inverting tri-state buffers, 4-bit/4-bit banks
TTL518	8-bit identity comparator
TTL594q	8-bit shift register with output register with clear
TTL595q	8-bit shift register with output register
TTL604q	octal 2-input multiplexed latches
TTL684	8-bit magnitude/identity comparator
TTL686	8-bit magnitude/identity comparator with enable
TTL688	8-bit identity comparator
TTL821	10-bit FFs
TTL822	10-bit inverting FFs
TTL823q	10-bit FFs with enable
TTL841q	10-bit latches
TTL842q	10-bit inverting latches

Note: The q suffix indicates that the part is not an exact duplicate of the TTL device. The differences are described in the User's Guide.



SpDE TOOLS
Seamless pASIC Design Environment

HIGHLIGHTS

- **Microsoft Windows** – Standard easy-to-use graphical user interface on PC 386/486 platforms.
- **Object-oriented database** – Facilitates seamless integration of design entry, simulation, and automatic place and route tools.
- **Third-Party Design Entry** – Includes libraries for CAD/CAM ECS and VIEWlogic schematic and simulation products.
- **Logic Synthesis Interface** – Accepts design entry data from Exemplar Logic Synthesis System in broad range of formats:
  - PALASM, ABEL/CUPL/MINC via PALASM
  - Boolean/state machines
  - VHDL or Verilog via HDL Synthesizer
- **Automatic Place and Route (APR)** – 100% APR can be achieved on designs with up to 100% cell utilization.
- **Delay Modeler uses AWE (Asymptotic Waveform Evaluation) techniques** – The AWE methodology yields accuracy as precise as SPICE simulation without the long runtimes.
- **ATVG (Automatic Test Vector Generator)** – The ATVG uses pASIC™ internal register scan path to automatically generate an optimum set of test vectors.

Logic designs for pASIC 1 Family, very-high-speed FPGA devices are created using third-party schematic capture, language entry, logic synthesis and simulation CAE tools on PC and workstation platforms. These tools interface to the QuickLogic Seamless pASIC Design Environment (SpDE™ — pronounced "speedy") for automatic place and route (APR), delay modeling, timing analysis and other tasks best served by architecture-specific software.

SpDE tools are available as a complete design capability including third-party design entry and simulation software, or as a standalone package with macro libraries only (order code QS-SPDEPC) for integration into the user's own design entry environment. This data sheet describes the features of the SpDE standalone product.

QUICKLOGIC

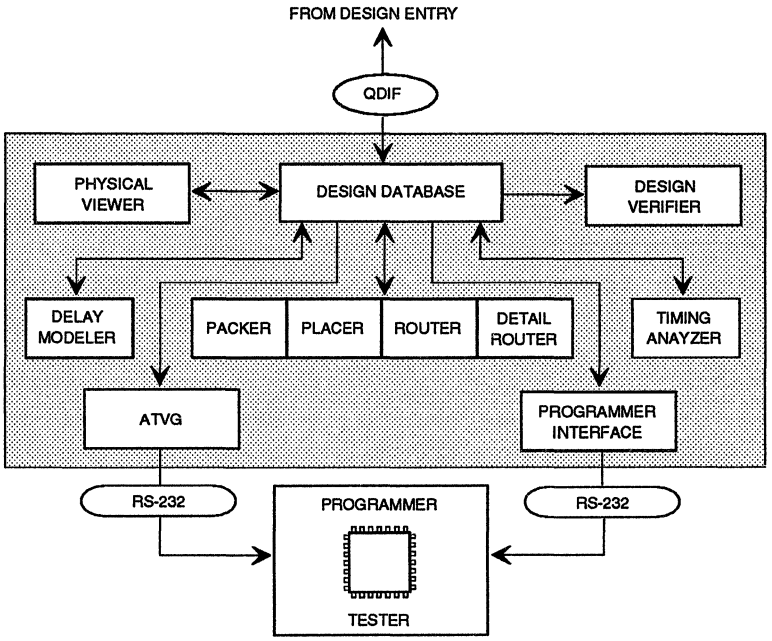


FIGURE 1
QuickLogic SpDE tools communicate with third-party software through a common design database

INTRODUCTION

FPGA architectures need sophisticated, yet low-cost and easy-to-use development tools to take full advantage of the available silicon speed. First-generation tools require the user to completely exit one design activity before beginning the next. The overall design process is slow and it is difficult to move interactively between design entry, simulation, and APR in the intuitive manner essential to optimize speed and functionality. Cumbersome interfaces between third-party and vendor tools further reduce designer efficiency.

QuickLogic has taken advantage of recent advances in CAE technology to offer an open system development environment which overcomes many of these limitations. These advances include the use of an object-oriented design database structure and the adoption of industry-standard graphical user interfaces, such as Microsoft Windows on the PC. This allows modern third-party design entry tools to interface in a seamless manner with QuickLogic SpDE software.

SpDE Tools

The QuickLogic architecture-specific tools include the major modules shown in Figure 1. These are:

- Design Database
- Design Verifier
- Automatic Place and Route (APR)
- Physical Layout Viewer
- Delay Modeler
- Static Path Timing Analyzer
- Automatic Test Vector Generator (ATVG)
- Programmer Interface

SpDE Tools also contain interface software to the Exemplar Logic synthesis package plus libraries for popular PC-based schematic and simulation tools, including the CAD/CAM Group and VIEWlogic products. See the Macro Library data sheet for the selection of available library elements.

Design Database

The QuickLogic design database contains all the information required to describe a complete pASIC design. A database architecture provides a user with the software analog of a computer backplane. It allows software modules to be easily plugged in and out of an application. Instead of being distributed across multiple files in different formats, design data is stored in a consistent format in a location directly accessible to all applications involved in the design process. For example, the QuickLogic design file includes information describing the netlist, timing, programming, ATVG data, etc.

Open access to the database is available via the QuickLogic Data Interchange Format (QDIF). Third-party tools can therefore be configured to communicate cleanly and efficiently with the functions of any, or all, of the QuickLogic SpDE tools.

Design Verifier

The Design Verifier analyzes a design for common errors, and architectural violations and warnings. In addition to catching errors prior to running place and route tools, the Design Verifier alerts the user to potential performance oriented problems such as excessive fanout.

Automatic Place and Route

The logic design is input to SpDE in the form of a QDIF file. This can originate directly from a schematic capture package, such as the CAD/CAM Group Electronic Capture System (ECS) or VIEWlogic VIEWdraw. Inputs from equation entry tools (ABEL, CUPL, MINC or PALASM), or high-level languages (VHDL, etc.) are accepted following processing by a logic synthesis package, such as the Exemplar Logic Synthesis System, to generate a QDIF file. Alternatively, a schematic generator can build symbols and schematics for the design, so that they can be integrated with other blocks in a higher-level schematic. In this manner, Boolean/HDL entry and schematic entry can be mixed and matched as desired.

The QDIF file is mapped into the physical pASIC silicon architecture by SpDE Automatic Place and Route tools. These tools consist of three key modules; the Packer, Placer, and Router.

The **Packer** maps logic symbols into pASIC logic cells. Five independent outputs on the pASIC logic cell allow multiple, unrelated logic functions to be automatically identified and packed into a partially used cell. This provides the most efficient use of silicon. The Packer is not an optimizer; it does not change the defined logic nor modify the netlist. Rather, it maps the user's macro symbols into logic cells in order to produce the fastest and densest possible implementation.

The **Placer** uses automatic placement technology to place I/O cells and internal logic cells in locations that provide optimum performance. The Placer takes the densest arrangement generated by the Packer and manipulates it to produce the fastest result. Fixed assignment of both internal and I/O cells is supported. This allows the user to fit pASIC devices into board designs with predetermined signal pin locations. It also permits a designer to iterate to the fastest possible solution by locating registers adjacent to selected output cells, or assigning priority to functions in a critical net.

While manual placement is optional, only fully automatic routing is permitted. The combination of the regular and orthogonal architecture permitted by the low impedance ViaLink interconnect technology, together with ample wire routing resources allows 100% automatic place and route of designs using up to 100% of the logic cells. Many designs have been completed successfully even with a high percentage of fixed user placement of internal cells and pin locations.

Consisting of Global and Detail Router stages, the **Router** connects logic cells together while minimizing the wiring delays and routing resources consumed. The Global Router assigns routability by making channel assignments. It includes an optimized Clock Router, which minimizes delay and skew on high-speed clock nets. It may also be used on resets and other wide fanout signals. The Detail Router completes the task by mapping the routes produced by the Global Router to specific wires in the pASIC device.

Physical Viewer

The Physical Viewer shows the user how the automatic place and route tools have mapped a logic design into the silicon resources. It is not a manual editor, but a tool that allows the designer to inspect the results of APR for placement efficiency and routing congestion. Timing critical paths can be identified and alternative placements evaluated.

In third-party tools with a database software structure, such as CAD/CAM's ECS, the Physical Viewer can be tightly coupled to allow cross probing between the schematic and the physical layout. For example, a wire on the physical layout can be selected within the viewer, and its logical counterpart will be highlighted within the schematic tool. Alternatively, a net can be selected on the schematic and its corresponding wire will be highlighted in the viewer. This tight interaction between the logical and physical representations gives the user a high degree of control over the design of critical speed paths.

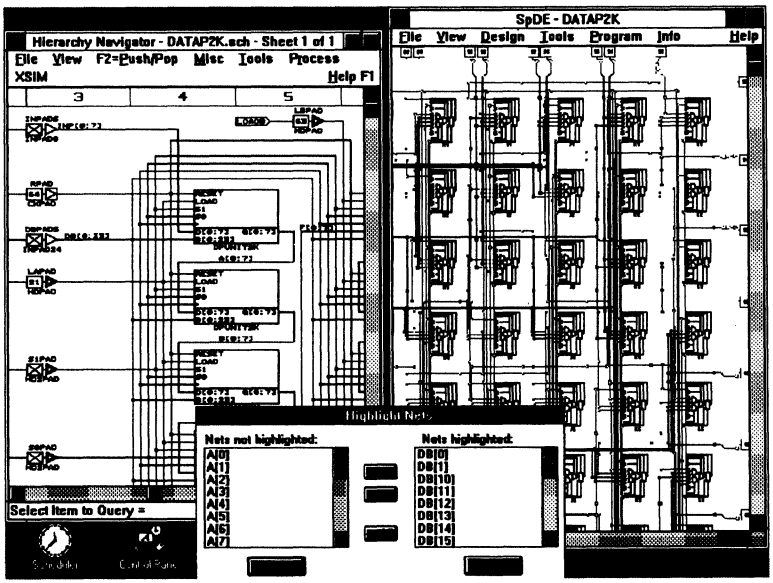


FIGURE 2
The user can cross probe between the physical layout and third-party schematic capture tools to highlight selected nets for debugging and iterative design improvement

3

Timing Analysis Tools

Timing analysis tools contained in SpDE include a Delay Modeler and a Static Path Timing Analyzer.

The Delay Modeler performs post-layout delay calculations using Advanced Waveform Evaluation (AWE) techniques. The AWE technique, developed by Professors Pillage of the University of Texas and Rohrer of Carnegie Mellon, uses moment matching approximations to evaluate the delays caused by distributed resistance and capacitance. It yields results that are as precise as SPICE simulations while reducing computing time by orders of magnitude, permitting highly accurate results using PC or workstation platforms. This work received the IEEE Transactions on CAD best paper award for 1990. By processing the complete results of APR, the Delay Modeler analyzes packing, placement, and routing to determine the intrinsic (active device) and wiring delays for the entire design. These precisely calculated delays are back-annotated into third-party simulators for timing-accurate results.

The Static Path Timing Analyzer performs path analysis of the circuit delay from the Delay Modeler. It offers automatic analysis of the complete design, as well as interactive analysis of user-specified portions of the design. Critical paths can be easily identified as the Path Timing Analyzer can be tightly coupled to both the schematic and the Physical Viewer.

Programming and Testing

The Programmer Interface translates the results of the APR process into the patterns required to program pASIC devices. These are transmitted, together with automatically generated test vectors, over an RS-232 link to the programmer.

The optimal programming procedure is determined by a function called the sequencer. By coupling the AWE calculations of the Delay Modeler with the results of the Detail Router, the sequencer optimizes the programming procedure to program ViaLink elements on the most heavily loaded nets to resistance values below 50 ohms. This ensures the shortest possible delays on these critical interconnects.

The flip-flops in the pASIC logic cells are connected by an internal scan path which allows device testing both prior to, and following, programming. Automatic Test Vector Generation (ATVG) software, included in the SpDE product, uses this feature to provide convenient and thorough test coverage of programmed pASIC devices by the user.

PROGRAMMING/ TESTING HARDWARE

The Designer Programmer/Tester is a low-cost programming and testing unit for QuickLogic pASIC devices. The model QP-PL84 accepts 84-lead plastic PLCC devices directly. Other packages are supported by individual adapters. This is included together with sample devices, cables, etc. in the pASIC Toolkit 3.0 (QT-3.0) and the SpDE PC Toolkit (QT-SPDEPC) or may be ordered separately (QP-DPPC).

SpDE Product Contents

The SpDE tools are available in the following configurations:

	Total Design Capability		SpDE Tools		Programming Capability
	QT-3.0	QS-3.0	QT-SPDEPC	QS-SPDEPC	QT-DPPC
Design Entry Tools					
ECS Schematic Capture	•	•			
X-SIM Simulator	•	•			
SpDE Tools					
Third-party Support					
Exemplar Interface	•	•	•	•	
CAD/CAM ECS Libraries	•	•	•	•	
Viewlogic Libraries	•	•	•	•	
Layout Tools					
Design Verifier	•	•	•	•	
Auto Place and Route	•	•	•	•	
Physical Viewer	•	•	•	•	
Timing Tools					
Delay Modeler	•	•	•	•	
Path Analyzer	•	•	•	•	
Programming Tools					
Programmer Interface	•	•	•	•	•
ATVG	•	•	•	•	•
Programming/Testing Hardware					
QP-PL84 Programmer	•		•		•
64-lead PLCC Adapter	•		•		•
Two QL8x12 Devices	•		•		•
Cables, connectors, etc.	•		•		•

SpDE Products Summary

Name	Order Code	Description
pASIC Toolkit	QT-3.0	ECS schematic capture X-SIM device simulator SpDE Tools Programming/Testing Unit
pASIC Tools – Software Only	QS-3.0	ECS schematic capture X-SIM device simulator SpDE Tools
SpDE Toolkit	QT-SPDEPC	SpDE Tools Programming/Testing Unit
SpDE Tools – Software Only	QS-SPDEPC	SpDE Tools
Programming/ Testing Toolkit	QT-DPPC	Automatic Test Vector Generator Programmer Interface Programming/Testing Unit

QT-DPPC
Programming/Testing Toolkit

HIGHLIGHTS

- **Combination programmer and tester** – All the hardware and software that is required to program pASIC devices from a 386/486 PC and execute ATVG test vectors to verify programming results.
- **Internal Device Scan Path** allows device testing of all registers following programming.
- **Programming/Testing Toolkit** includes sample devices, cables, adapter and even an antistatic wrist strap.
- **Intended for users of third-party place and route tools** who need to program QuickLogic devices. (NeoCAD Inc., for example, offers a device-independent APR package compatible with the QuickLogic Designer Programmer/Tester.)

Programming/ Testing Toolkit

QUICKLOGIC

Designer Programmer/ Tester

The Designer Programmer /Tester is a cost effective programming and testing unit for QuickLogic pASIC family devices. The model QP-PL84 directly accepts 84-lead PLCC devices; other packages are supported by individual socket adapters.

Programming and Testing

The Programmer Interface translates the results of the APR process into the patterns required to program pASIC devices. These are transmtited, together with automatically generated test vectors, over an RS-232 link to the programmer.

The optimal programming procedure is determined by a function called the sequencer. By coupling the AWE calculations of the Delay Modeler with the results of the Detail Router, the sequencer optimizes the programming procedure to program ViaLink elements on the most heavily loaded nets to resistance values below 50 ohms. This ensures the shortest possible delays on these critical interconnects.

Automatic Test Vector Generation (ATVG) software analyzes test coverage and generates the test vectors This allows convenient and thorough test coverage of programmed pASIC parts using the internal scan path included in the design of the pASIC devices. The degree of test coverage can be easily controlled, and user-specified test vectors generated in the X-SIM simulator can be included. The Programmer Interface downloads the programming element and test vector signals over an RS-232 connection to the pASIC Designer Programmer.

Contents and System Requirements

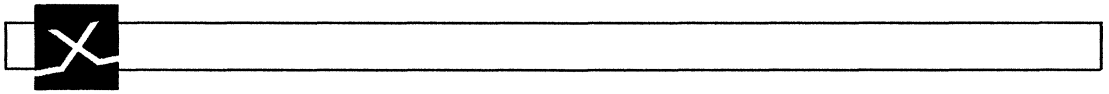
The Programming/Testing Toolkit contains all necessary hardware and software to program and test the pASIC device, minus the PC workstation.

- Model QP-PL84 Designer Programmer/Tester unit
- Automatic Test Vector Generator (ATVG)
- Programming interface software
- Two QL8X12 pASIC FPGA devices
- AC adapter and cord (Output 12 VAC, 800 mA. Plug ID 2.1 mm, OD 5.5 mm)
- 9-pin RS-232 cable
- Cable adapter, 25-pin to 9-pin
- 68-pin adapter
- ESD wrist strap
- All software supplied on 5.25-inch high-density disks, 3.5-inch versions available upon request.

The programming unit operates when connected serially to a PC station running Windows™ 3.0 or greater. The minimum sotware and hardware requirements for programming the device are as follows:

- MS-DOS (or PC-DOS) version 3.1 or higher
- Microsoft Windows version 3.0 or higher
- 80386/486-based PC
- 4 MBytes RAM
- Windows-supported mouse
- 8 MBytes free disk space
- Available serial port

Name	Order Code
Programming /Testing Toolkit	QT-DPPC



QAN1
Registers and Latches in the pASIC Architecture
QuickNote

INTRODUCTION

Quicklogic's pASIC™ 1 Family of high-performance FPGAs allows logic function speeds of over 100 MHz. The prime objective of the QuickLogic pASIC 1 Family logic cell is to maximize in-system device speed, while providing the flexibility to integrate both combinatorial and register-intensive designs. For sequential applications, each pASIC 1 logic cell can be configured for latched or registered operation. In fact, for some designs, it is possible to integrate two latches and a register into a single logic cell. Thus, the QL8X12, which offers 1000 usable gates in 96 logic cells, has a maximum potential capacity of 288 registers and latches. The pASIC logic cell is shown in Figure 1.

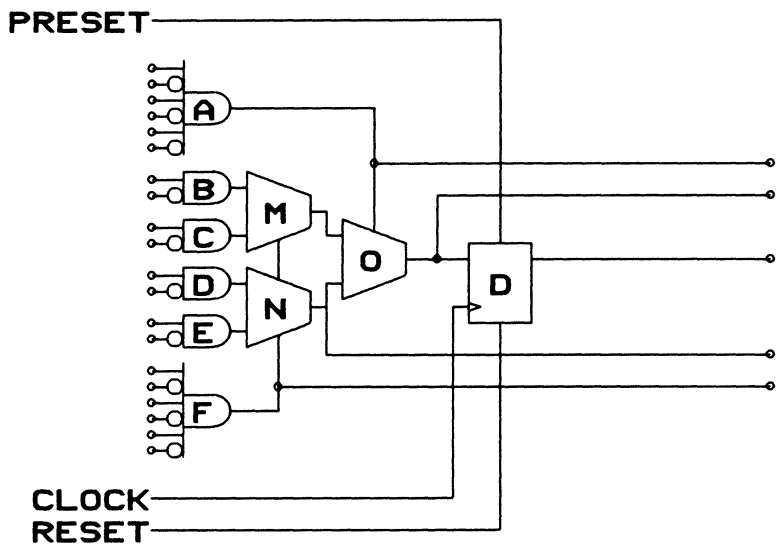


FIGURE 1
The pASIC 1 logic cell's 5 outputs offer a new level of flexibility in FPGA design, resulting in very high gate useage

QUICKLOGIC

Each logic cell has a dedicated register that has independent reset and preset functions. One of the unique features of the logic cell is the availability of multiple outputs, which may also be used as feedback paths. These feedback paths, combined with the combinatorial logic in each logic cell, allow it to be configured for a variety of registered and latched applications, while maintaining efficient gate utilization. This QuickNote will demonstrate a few of the many ways the pASIC 1 logic cell can be used to implement latches, registers, and combinations of the two functions.

The pASIC Toolkit is a fully integrated, Windows 3.0-based development environment for QuickLogic pASIC 1 FPGAs. The Engineering Capture System (ECS) from CAD/CAM Group allows for fast schematic entry of designs. To simplify design entry, the Toolkit comes with an extensive library of macrofunctions including over 50 register and latch functions. These include single and grouped functions, as well as many 7400 series equivalents. Figure 2a shows a few of the basic functions, while Figure 2b gives a listing of the 7400 series register and latch functions included in the library.

FIGURE 2a
Several of the over 50 register and latch macrofunctions included in the pASIC Toolkit 3.0

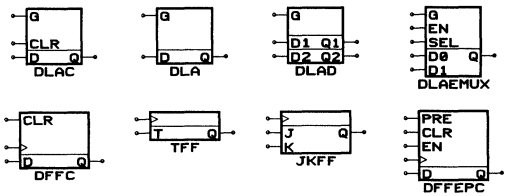


FIGURE 2b
The pASIC Toolkit 3.0 also offers an extensive library of 7400 series latch and register functions

7474	7477	7478	7491
7498	74104	74105	74107
7409	74116	74171	74174
74194	74268	74273	74278
74279	74373	74374	74376
74395	74396	74594	74604
74821	75822	74823	74841
74842			

For most cases, the macrofunction library will contain all of the functionality required by a particular design. The Toolkit includes a module called the Packer, which will scan a design for gates, registers, and latches that can be combined into a single logic cell. This not only offers the benefit of higher density, but higher speed as well. For a more detailed discussion of the Packer, consult Chapter 8 of the pASIC Toolkit User's Guide.

However, in some cases a customized element may be desired to achieve a specific function. The pASIC Toolkit 3.0 allows custom functions to be designed at the cell level, or by combining existing library elements. This gives the designer the best of both worlds—high-level functionality from the macro library and control at the gate level when desired.

The multiplexer-based pASIC 1 logic cell, is ideal for implementing latched functions. As shown in Figure 3, a D-type flow-through latch is easily implemented in a single 2-to-1 multiplexer. This function is available in the library as the element DLA.

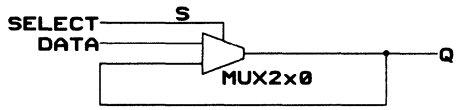


FIGURE 3
A 2-to-1 multiplexer is easily configured as a flow-through latch, taking a fraction of a logic cell

The multiplexer-based logic cell can implement two flow-through latches in a single cell (library element name DLAD). Thus, a function such as the 74373, an 8-bit latch, is implemented in only four logic cells.

Perhaps not so obvious are the benefits gained when the design requires pipelined latches. In this case, for which a logic cell design is shown in Figure 4, the output of the first latch (which is implemented in multiplexer N) feeds the input of the second latch (which is implemented in multiplexer O). This design is easily modified for common enables, true-complement enabling, or inverted data input.

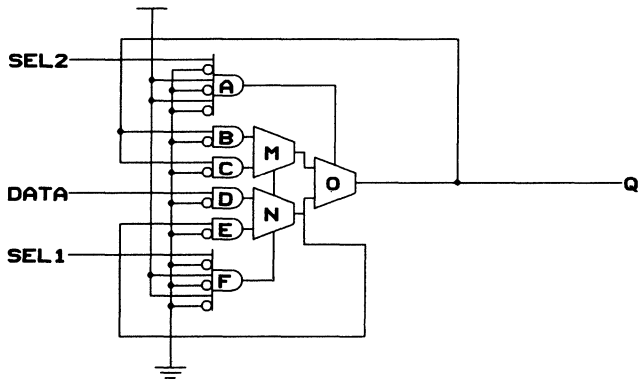


FIGURE 4
Using a cell design such as the one above, pipelined latches can be combined into a single logic cell to minimize the latch-to-latch delay

This type of design minimizes the delay path between latches for high operating frequency, while at the same time maximizing logic cell utilization.

The pASIC 1 Family is equally capable when it comes to integrating edge-triggered registers. As mentioned previously, each of the logic cells within a pASIC 1 FPGA comes equipped with a dedicated D-type register that can also be configured for J-K and Toggle operation. This register has dedicated preset and reset logic, and can be clocked from any of the express lines. These dedicated registers will typically satisfy the register requirements of most designs. However, some designs are register-intensive and will require more than the fixed number of registers within the pASIC device. In this case, it is often possible to put two registers into a single logic cell. An edge-triggered register can be easily constructed from the multiplexer logic in each logic cell. Figure 5 shows how two 2-to-1 multiplexers are connected to create an edge-triggered register.

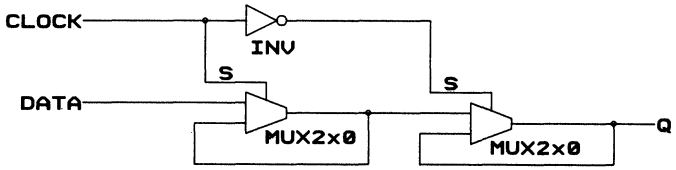


FIGURE 5
Two latches, implemented in multiplexers, are combined in a master/slave configuration to create an edge triggered flip-flop

This is the familiar master/slave latch implementation of an edge-triggered flip-flop. Note that this design can be easily modified for negative edge-trigger clocking, simply by moving the inverter such that the enable to the first mux is inverted, and the enable for the second is not. This configuration is essentially the pipelined latch configuration that was shown previously, and it is implemented in multiplexer logic, leaving the dedicated register still available. Thus, for cases where one register is feeding another, the pASIC logic cell is capable of integrating two registers into a single cell. Figure 6 shows a cell design for pipelined registers. The first register consists of multiplexer N and multiplexer O in a master/slave latch configuration. This is followed by the dedicated cell register.

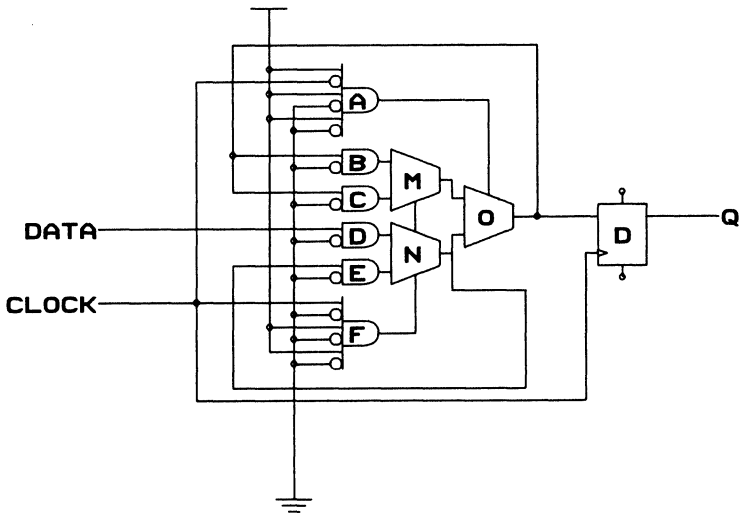
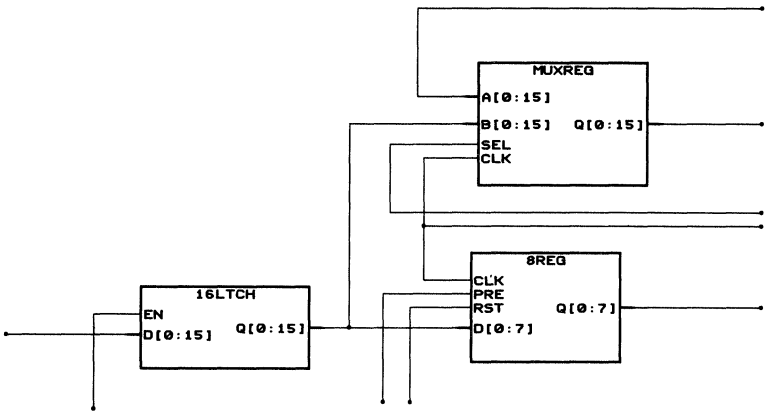


FIGURE 6
A cell design for two edge-triggered registers in a single cell. This allows an 8-bit shift register to be implemented in only 4 logic cells.

A typical example of how this function would be used is an 8-bit shift register. This function is implemented in only four logic cells, thus maximizing the overall gate utilization of the device.

Similarly, designs frequently call for a latch feeding a register. The pASIC Family of FPGAs is capable of integrating this logic into a single logic cell. Conversely, if needed, the logic cell is also capable of handling a design requiring a register feeding into a flow-through latch. Finally, for the designer wishing to take advantage of the full capability of the device, a logic cell can be configured as a pair of latches followed by a register. The register must be fed by one of the latches, but this is not unusual when latching data off a system bus where it is then registered for internal use.

FIGURE 7
A typical 16-bit bus interface, where the data is first latched, and then can be stored in one of two registers



The 16-bit latch plus the 8-bit register can fit into only 8 logic cells, for an average utilization of 22 gates per logic cell.

This QuickNote details a few of the many register and latch functions that can be implemented in the pASIC 1 Family of FPGAs. The flexibility of the logic cell architecture allows for easy integration of multiple latches and registers into a single logic cell, up to 288 in the pASIC QL8X12 1000-gate FPGA. It is this flexibility of the logic cell, combined with the powerful pASIC Toolkit, that allows rapid completion of designs that will operate over 100 MHz, with a fully automatic place and route.

QAN2
Counter Designs in the pASIC Device QuickNote

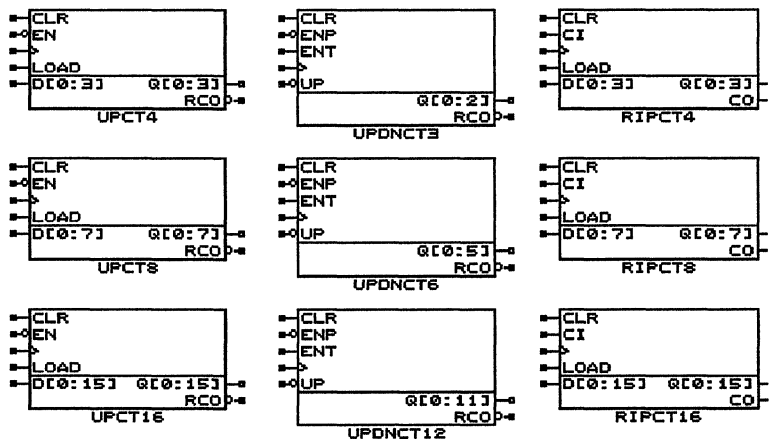
HIGHLIGHTS

- **Free running counters** – High-speed counters optimized for binary counting at frequencies in excess of 100 MHz.
- **Counters with added features** – Binary counters with LOAD for data inputs, COUNT ENABLE, UP/DOWN count capability, 3-State output control, synchronous and asynchronous clear inputs.
- **Counter Macro Library** – A comprehensive library of QuickLogic counters exists as ready-made designs for instant systems applications.
- **Counter Design Methodology for pASIC™ devices** – Introduction of techniques to enhance the performance of counter design. How to use look-ahead and pipelined carry to decrease propagation delay between counter modules.

INTRODUCTION

The low -impedance ViaLink™ interconnect element employed in the pASIC device architecture enables higher performance operation than any other FPGA family. This is particularly evident in the design of high-speed counters. The pASIC macro library contains a range of predesigned counters covering a wide variety of needs. Examples of nine of these are shown below. This QuickNote is intended as an overview of alternative approaches to the pASIC design methodology of functions that cannot be satisfied by these counter modules.

Counters from QuickLogic's Macro Library



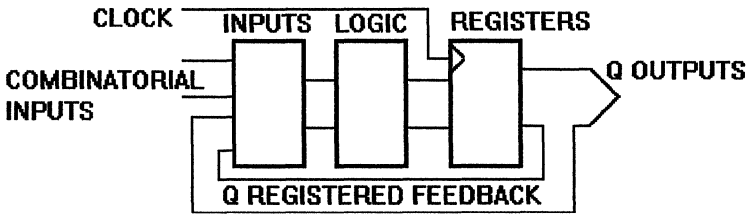
QUICKLOGIC

Designs in this application note were implemented with the QuickLogic pASIC Toolkit operating under Microsoft Windows™ 3.0 on the PC. This comprehensive set of CAE software includes third-party design entry (ECS from CAD/CAM Group, Inc.) and timing and functional simulation (X-SIM from SAS, Inc.). Both operate efficiently and interactively with QuickLogic SpDE place and route, delay modeling and physical viewer tools. The ability to enter and simulate in the same graphical environment provides the user with a quick and efficient way of generating and debugging counter designs.

After SpDE place and route of the pASIC device, timing values may be generated. Compiling net, gate and ViaLink propagation delays provides timing parameters that are a function of the layout and partitioning of the cells in the pASIC device. These timing values can be annotated back into the simulator. Having done this, the designer can evaluate the performance of his counter with regard to maximum count frequency, clock to output, input set up and hold times. If the counter's performance needs improvement the ECS schematic capture environment may be invoked to manually improve the placement of registers or clock input buffers. An optimum placement for counters would have registers placed in a column with clock inputs driven from a clock express line to minimize clock skew.

Figure 1 shows a block diagram of a Moore state machine. The next state of the registered Q outputs is a function of combinatorial inputs gated with the current state of the same Q outputs. A counter is a state machine that conforms to this structure. The state of the inputs combine with the Q registered feedback to provide the next output state. Depending on counter complexity, a design can have combinatorial inputs; CLEAR, HOLD, COUNT ENable, UP/DOWN control, and for loadable counters DATA inputs and a LOAD control.

FIGURE 1
Moore State Machine



...State machine design in the pASIC device

Implementation of this type of state machine is well suited to the pASIC device that has internal logic cells comprising logic gates, multiplexers and registers. Universal cell interconnect is possible through vertical and horizontal routing channels and programmable ViaLink sites. Logic and registers combine with interconnect to realize state machines and counters of varying complexity. Position constraints of the registered cells can be entered into the schematic along with the design itself, thus ensuring optimum placement of cell groups.

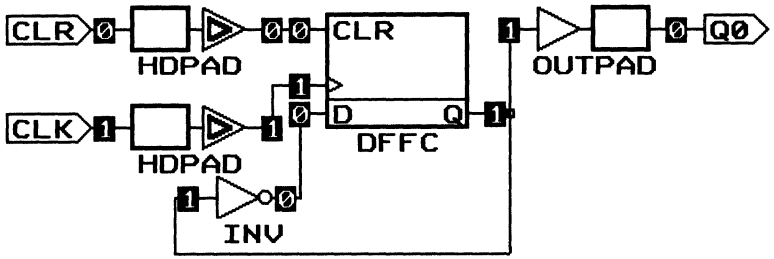


FIGURE 2
Binary Flip-flop

Figure 2 shows a binary flip-flop as entered in the ECS schematic capture system. It conforms to the Moore state machine of Figure 1. The CLR line is used as a direct input to reset the register and the Q0 output is inverted and fed back to drive the D input of the same register which causes it to toggle after each clock rising edge. This circuit forms the least significant bit of a free-running binary counter. To optimize a counter design for maximum performance the designer should take advantage of the high drive input buffer (HDPAD) which rapidly charges/discharges the low capacitance on the dedicated express clock lines. High current drive minimizes clock skew on these lines that cover the entire length and breadth of the pASIC device.

The X-SIM simulator allows logic ONEs and ZEROs to be displayed over the signal lines so the designer can trace the behavior of his system dynamically, as in Figure 2.

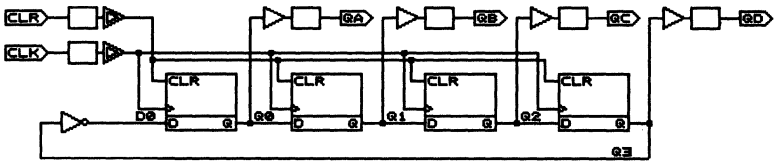
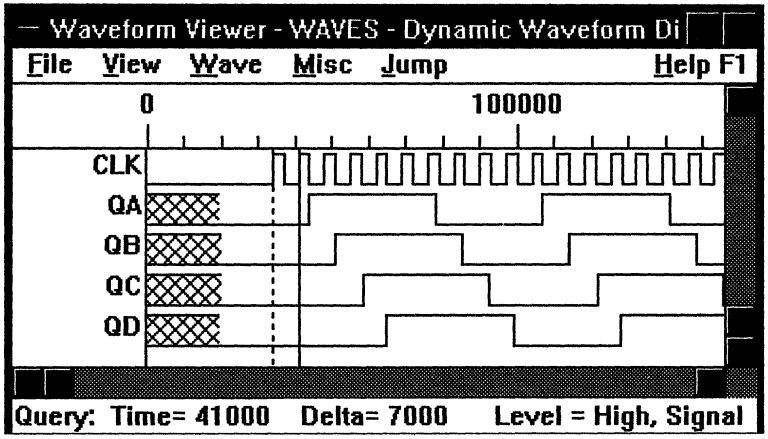


FIGURE 3
Four-bit Johnson counter design

The circuit shown in Figure 3 is a Johnson counter implemented in the pASIC device. It consists of four D-type registers linked as a shift register with an inverting feedback from Q3 into the D0 input of register Q0. After the registers have been cleared, the first clock pulse will strobe a logic HIGH into Q0 and a further three clock pulses will propagate that HIGH through the other registers. When Q3 goes HIGH the feedback to D0 will be inverted and a LOW will be clocked into Q0. The subsequent clock pulses will sequentially clock a LOW condition through the shift register as shown in the following simulation. This design comprises four registers and provides eight distinct states through which the counter can transition. With a clock input period of 7000 pico seconds (7 ns) the Johnson counter performed with a clock frequency of 143 MHz during simulation.

Simulation of the Johnson counter



The advantages of the Johnson counter are found in its simplicity and very high performance. The light capacitive loading on each register output and the lack of combinatorial logic delays in the feedback loop make this design capable of clocking at well over 100 MHz in the pASIC device. A disadvantage is in the number of states through which the counter can transition. If n represents the number of registers in the counter, then the Johnson counter can clock through 2n states as opposed to 2^n found in a binary counter with n registers.

FIGURE 4 Free-running four-bit binary counter with clear

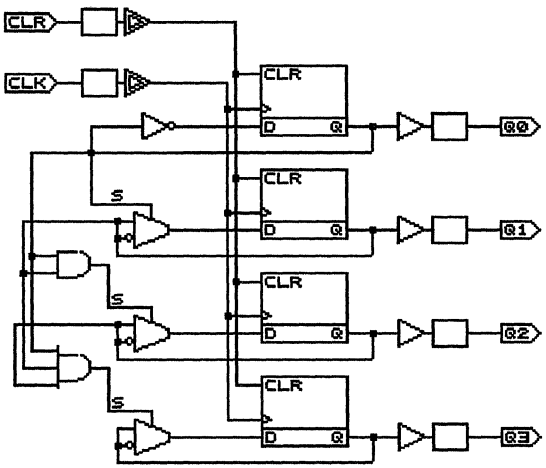
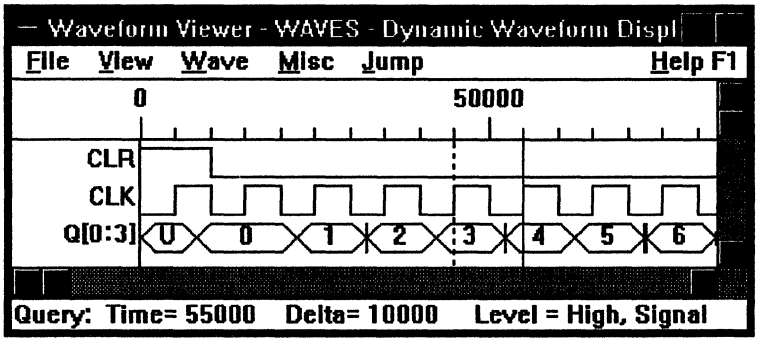


Figure 4 shows a binary counter with an asynchronous CLEAR input. In this design a register is required to maintain or HOLD its current contents until all the lesser significant registers become HIGH. Then the register is required to change its state or TOGGLE after the next clock edge. The least significant stage of this design features the binary flip-flop that is given in Figure 2 and provides the output for Q0.



Simulation waveforms of the four-bit free-running counter clocking at 100 MHz

The TOGGLE and HOLD functions for registered outputs Q1, Q2 and Q3 are achieved with a 2:1 multiplexer feedback. An AND gate control drives the S (Select) input of each multiplexer. When the AND gate output is HIGH, the inverting feedback path through the multiplexer is selected causing the register output to TOGGLE, otherwise a HOLD function is maintained through the noninverting route. This four-bit counter shows a very efficient use of the pASIC cell as only four of them are required to perform this function. The design when simulated with a clock input of period 10,000 pico seconds (10ns), showed 100 MHz counter performance.

Four-bit Gray code counter design

A Gray Code sequence allows only one bit in the pattern to change as one state proceeds to the next. This type of encoding can safeguard against simultaneous output driver transition. By definition only one bit can change so only one output buffer will transition after each clock pulse.

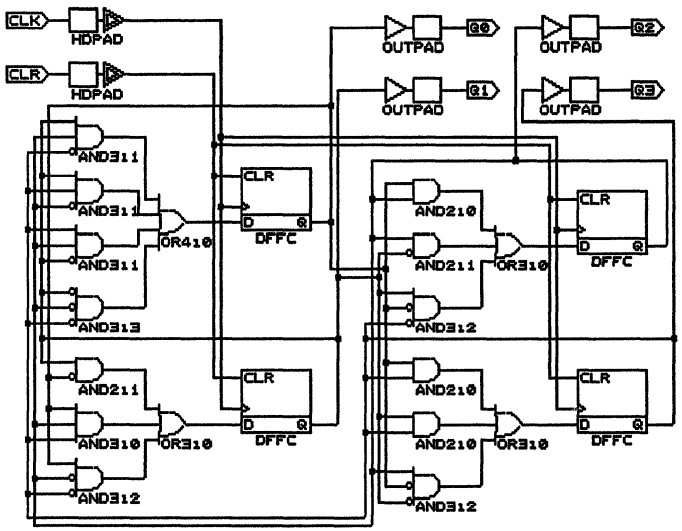


FIGURE 5

Four-bit Gray code counter in pASIC device

Figure 5 shows a Gray code counter as a state machine design. The conventional "sum of product terms" has been used to encode the registered feedback and provide the correct sequence states.

Four-bit Gray code counter simulation

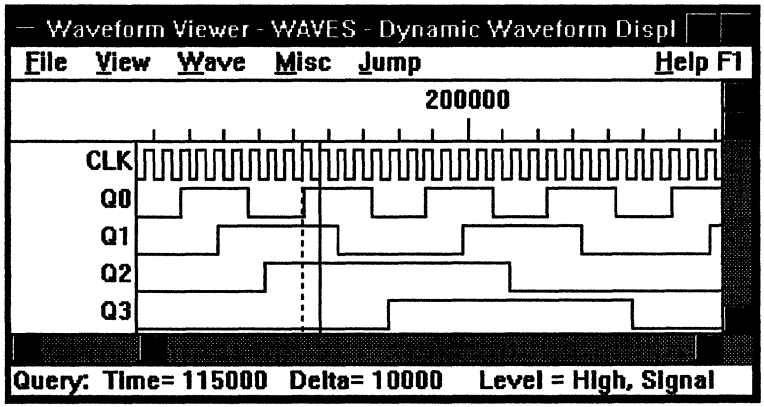


FIGURE 6
Loadable counter with count and output enable

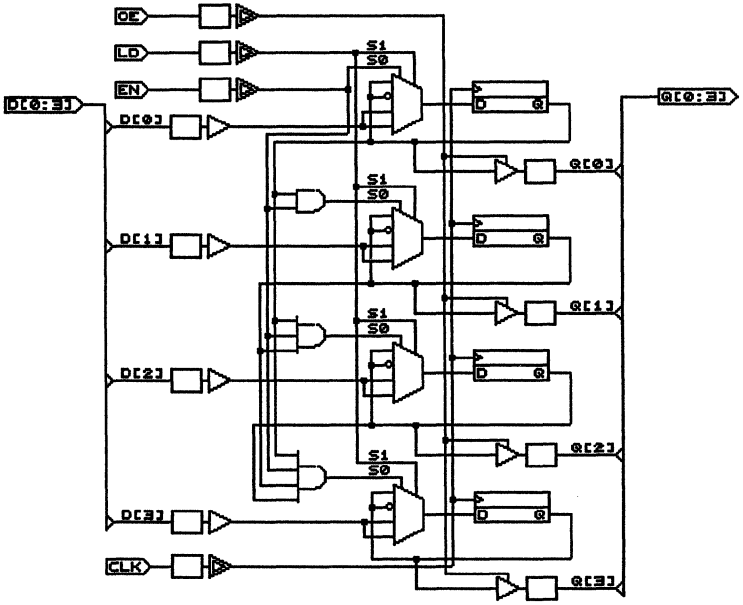
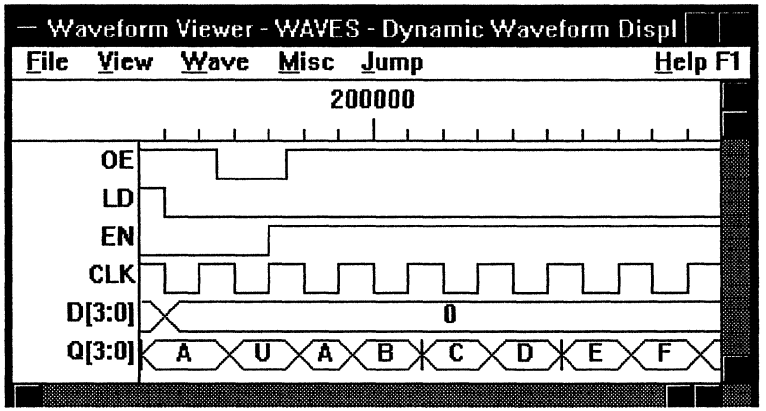


Figure 6 shows a counter having a LOAD/COUNT function selected through 4:1 multiplexers that drive each register in the counter. When the LOAD input is HIGH, the data on the D0:D3 input bus is selected through the multiplexers. The clock rising edge will synchronously load the registers Q0:Q3. To disable a LOAD function, the LD input must be LOW, enabling the COUNT function. The EN input allows the counter to increment or hold. Finally the OE input gives an active HIGH enable to the 3-State output buffers (TRIPAD) given in Figure 6.



Counter simulation load hold 3-State count

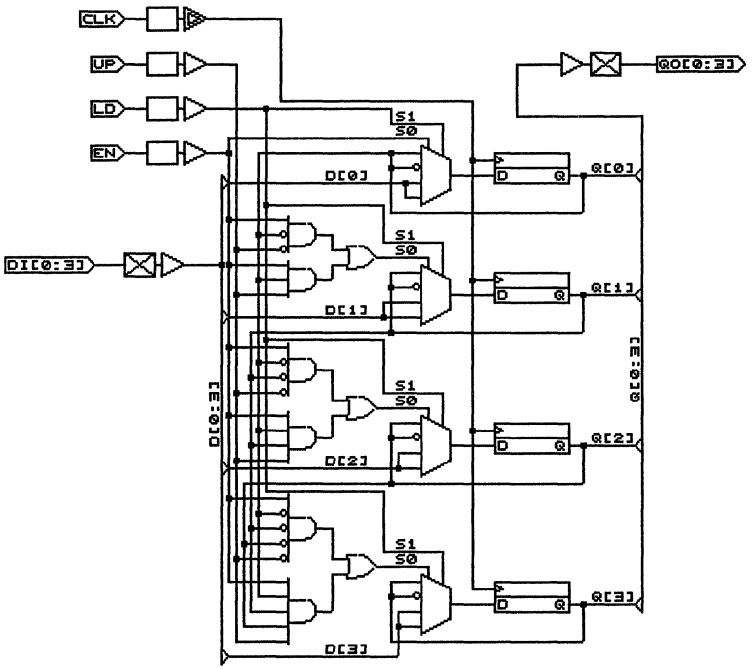


FIGURE 7
Loadable up/down counter

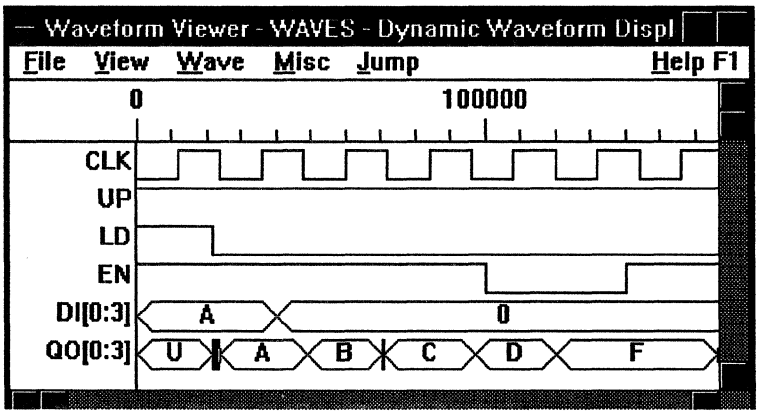
4

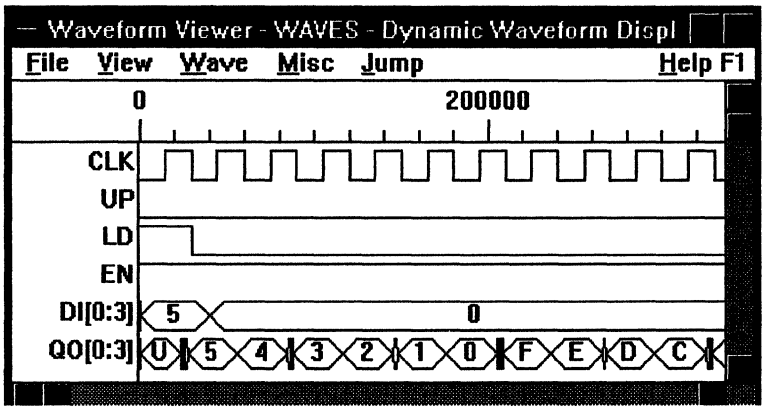
Synchronous loadable up/down counter

Figure 7 shows a binary four-bit loadable UP/DOWN counter with a count enable, EN, input. Data inputs DI[0:3] are tied to a bus and enter the pASIC device through a four-bit wide input buffer. Individual data lines D[0], D[1], D[2], and D[3] drive inputs 3 and 4 of the multiplexer circuits. The LD input, when HIGH, will select these data lines to drive the D-type register inputs. A synchronous clock loads D[0:3] Data inputs to the registered Q[0:3] outputs. When the registers are loaded, the LD input may be taken inactive LOW. To enable the count function, the EN input must be driven HIGH. This input provides an enabling HIGH to all the AND gates shown in Figure 7. When LOW, this signal maintains a HOLD condition on all four registers. In a binary counter a register is required to TOGGLE after all the less significant registers become HIGH, but this circuit can count either way, UP or DOWN. In a down count a register TOGGLES after all the less significant registers become LOW. The circuit controlling the TOGGLE function of each register comprises a sum of two product terms and drives the S0 input of each multiplexer. One of the two AND gates will be enabled by a logic HIGH on the UP control and the second AND gate enabled for the DOWN count. The UP input is a dual function pin, UP and NOT DOWN. When HIGH, this input selects the UP count and when LOW, selects the down count.

It should be noted that in both Figures 6 and 7, buses have been used for data inputs and register outputs. Combining signals on a bus and using components in a group can help simplify the schematic diagrams in complex circuits. For deeper counters such as eight bits, sixteen bits and above, it is recommended that the designer use buses to improve the clarity of the circuit design.

Simulation showing up count, load, count enable





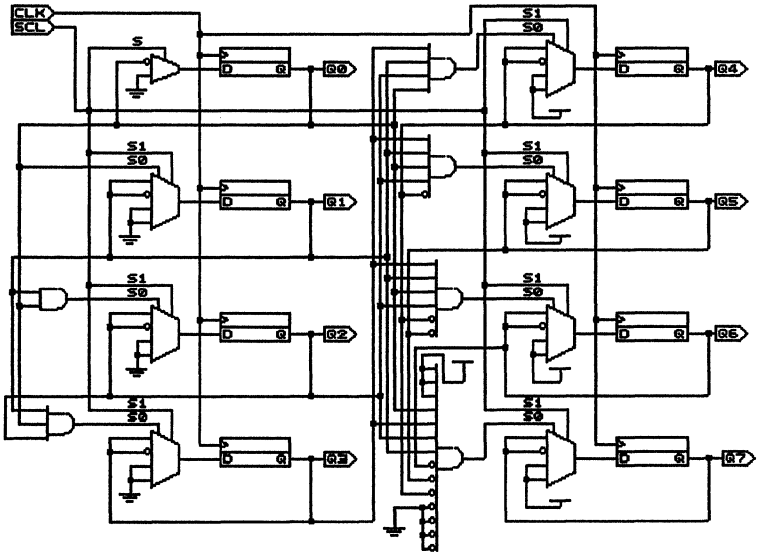
Simulation showing counter load, down count, wrap-around

Eight-bit binary counter with synchronous clear

The design methodology used for integrating deeper counters into the pASIC device employs a technique of interlacing internal registered HIGH and LOW conditions. The wider AND gates in the pASIC cell library have both true and complement inputs up to the widest AND gate which is the AND14i7. This gate has a total of fourteen inputs, seven inverting and seven noninverting. The counter shown in Figure 8 has outputs Q0:Q7 and has been designed such that Q0:Q3 function on LOW logic levels, and Q4:Q7 on HIGHs. When the SCL input is driven active HIGH it will select a logic LOW for registers Q0:Q3, and a HIGH for registers Q4:Q7 via the multiplexer inputs 3 and 4. If registered outputs Q4:Q7 drive inverting output buffers and Q0:Q3 noninverting buffers then all the buffer output pins will be driven LOW. To an external system, this counter is designed to function as a conventional binary counter, but internally the groups Q0:Q3 and Q4:Q7 function on interlaced LOW and HIGH logic group levels respectively.

During synchronous count operations, the AND gates controlling the TOGGLE function also require interlaced true and complement inputs. Just as Q4:Q7 require inverting output buffers, the same internal TOGGLE control AND gates invert Q4:Q7 signals. An example is given in the TOGGLE control gate for Q6 which combines Q0:Q3 and NOT Q4 and NOT Q5 as an AND gate function of all six input variables.

FIGURE 8
Eight-bit binary counter



...Tie unused logic inputs to Vcc or GND

The TOGGLE function to register Q7 uses the 14i7 AND gate. In any circuit design the unused inverting or noninverting inputs must always be tied to Vcc or GND. This is shown for the 14i7 AND gate in Figure 8. Any unused input to a logic cell can be tied to create a permanent HIGH or LOW enable condition for the other signal inputs. The way in which the designer interlaces the logic HIGH and LOW conditions in the counter design is also important. An obvious way would be to consider even outputs Q0, Q2, Q4 ... functioning on logic HIGH levels and odd outputs Q1, Q3, Q5 ... on logic LOWs. This way of interlacing a counter is on a bit-by-bit basis and could cause problems if there were a requirement for the registers to be bussed onto pin driver groups. Interlacing a four-bit-wide group, Q0:Q3, and Q4:Q7 allows a bus of four bits wide to drive a pin driver group four bits in width. Interlacing on alternate bits would prevent the designer taking advantage of the bus feature.

The circuit given in Figure 8 can be made into a symbol and used as an eight-bit counter module or block with CLK and SCL inputs. The design has no count ENable input and is a free-running counter toggling on each clock cycle. A designer can develop deeper counters, 16, 24 and 32 bits by combining eight-bit counter modules. If a 16-bit counter is created from two eight-bit modules, then the higher order eight-bit module must be prevented from incrementing until the lower order counter has reached its final count. An ENable input is an additional control that is required by the higher order byte counter. The counter shown in Figure 8 may be developed to incorporate an additional ENable input. If each TOGGLE AND gate has one additional

input to control the TOGGLE or HOLD function, then that control can be used as the ENable input. An AND gate will be required for the register and multiplexer combination driving Q1. The S0 input of the multiplexer will be selected by Q0 AND the ENable function. For Q0, a four-input multiplexer should be added with the ENable input driving its S0 input and the S1 input being driven by SCL. This multiplexer has the same connections as Q1, Q2 and Q3.

Pipelined carry generation

The way in which a carry output is generated, from the lower order eight-bit counter, and propagated to the ENable input of the next stage is crucial in determining the performance of the two stages. One method would be to detect the final count of the lower order counter and feed an enabling signal to the next stage. This requires one clock period for gating and propagation. A more subtle approach would be to detect the count value prior to the final count. This penultimate carry bit is generated one clock pulse before the last count, so a D-type register is required to delay its propagation to the next eight-bit stage. Carry generation and propagation can be extended over two clock cycles, effectively halving the delay path.

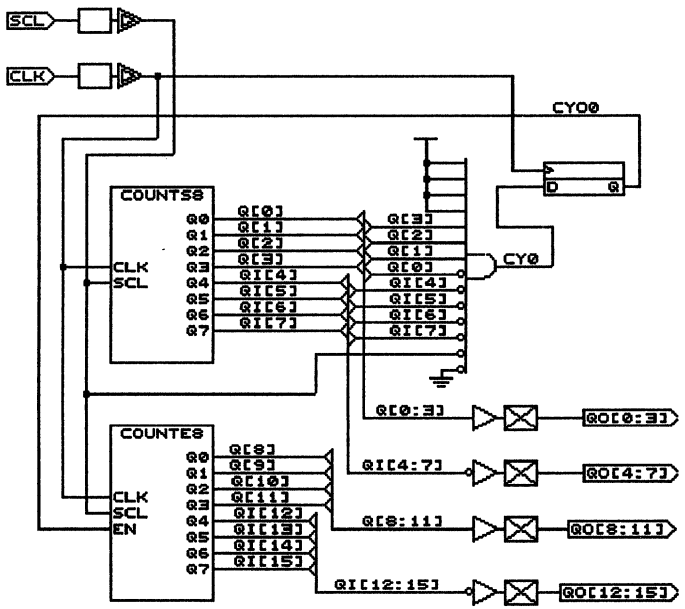


FIGURE 9
16-bit counter from two eight-bit modules and a pipelined look-ahead carry

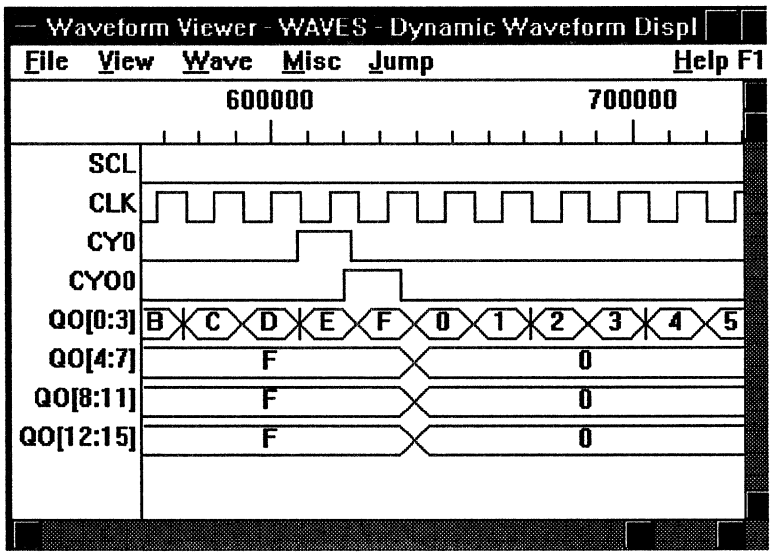
One AND gate and a D-type register combination is used to decode and generate and pipeline the carry CY0/CYO0. This is decoded from the least significant eight-bit counter output bus. The technique is also called 'carry anticipate' and its application is to reduce the carry propagation delay to the input of the next counter stage. The eight-bit counter module in Figure 8 is given in Figure 9 as a macro COUNTS8. An additional eight-bit counter has been added to provide outputs QO8-QO15. The macro COUNTS8 is identical to COUNTE8 apart from one additional input. The EN input is an active HIGH count enable input and is driven from the look-ahead pipeline carry register. This counter will HOLD its current contents when EN is LOW and increment when EN goes HIGH. From Figure 9 the bus nets Q[0:3] and Q[8:11] are non-inverted while QI[4:7] and QI[12:15] give inverted outputs. The output buffers correct the logic polarity to provide a conventional binary output code.

...Carry generation and propagation is critical in determining performance

When considering the performance of this counter design it should be noted that the internal set up time for the registered outputs Q[8:11] and QI[12:15], of module COUNTE8, is 256 clock cycles. The propagation of the carry bit then becomes the critical performance factor in the linking of the two counters.

The simulation shows the sixteen-bit counter outputs and the look-ahead carry CYO which decodes the hexadecimal count 'FFFE'. The D-type register delays this signal by one clock edge, so its output CYO0 goes HIGH when the counter reaches 'FFFF'. The counter outputs "roll over" to '0000' after the next clock transition and a logic zero is clocked into the carry register. So carry generation and propagation takes two clock cycles.

Simulation of the 16-bit counter showing the pipelined carry



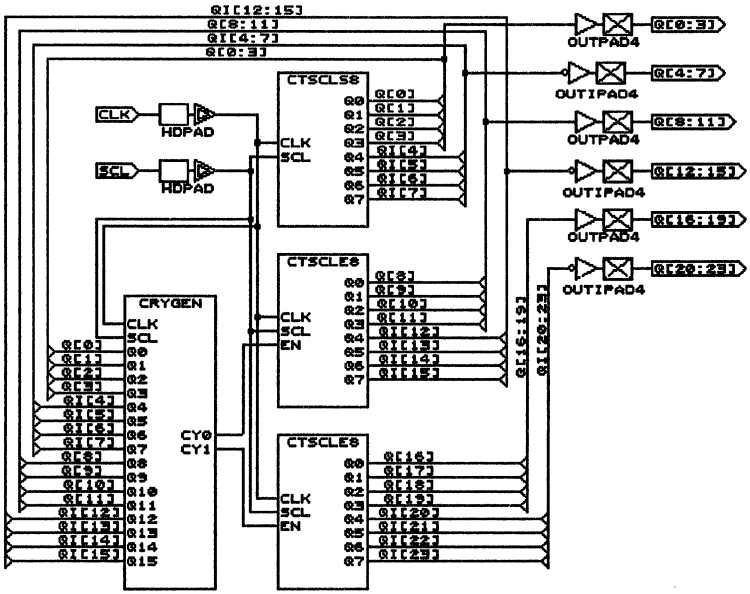


FIGURE 10
24-bit counter from three eight-bit modules

Figure 10 takes the counter depth to 24 bits using a similar look-ahead technique. In this example a carry generator macro CRYGEN has been created to decode the count before the penultimate count. If 'FD' hexadecimal is decoded from the least significant byte, as opposed to 'FE' then two registers are required to pipeline the early carry. Its propagation delay is then extended to three clock cycles increasing the time available to enable the higher order counters. The higher order byte counters in the chain have a set up time through internal feedback of 256 count periods. This makes the look-ahead carry generation propagation delay the significant determining factor in the counter's overall performance.

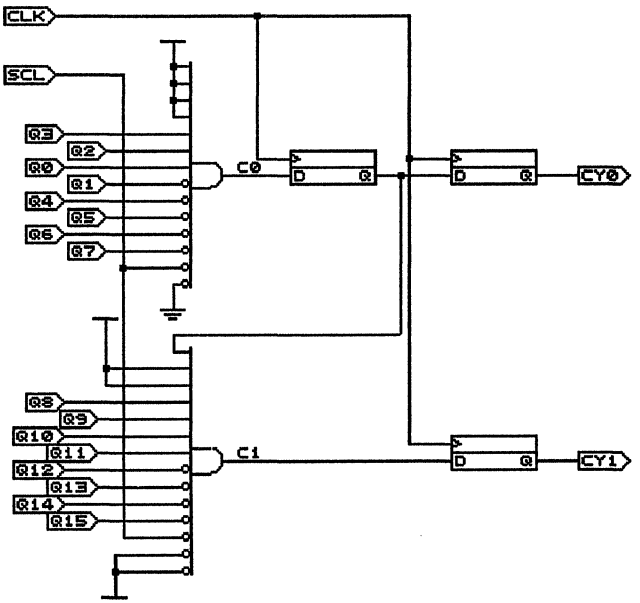
Look-ahead carry for a 24-bit counter

For a 32-bit design, the designer could decode 'FC' from the least significant eight-bit stage and pipeline the carry through three registered stages if it gives any benefit to the system performance. In a design that uses the technique of a pipelined carry it should be noted that a synchronous clear should flush the carry registers as well as the counter registers. The CRYGEN MACRO has a SCL (synchronous clear) input to perform this function, Figure 11.

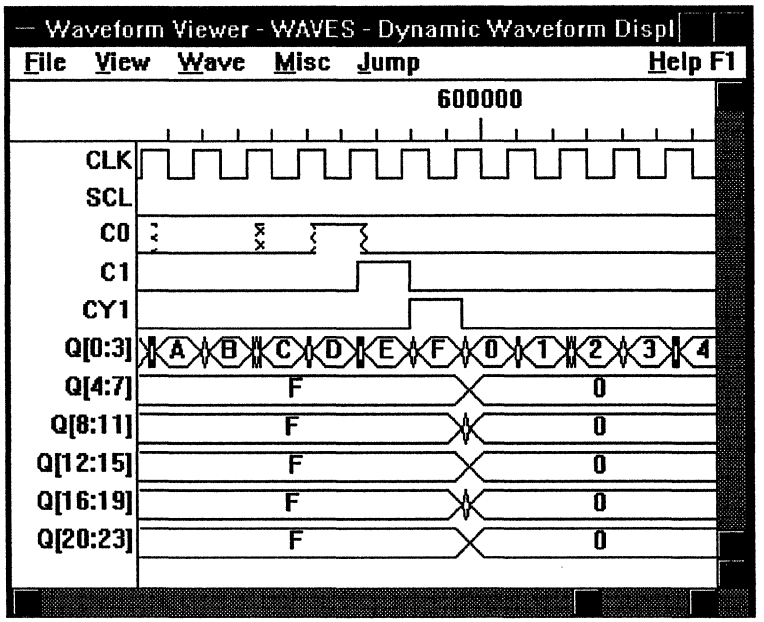
For deep loadable counters that use look-ahead carry, the design should distinguish between a count and a load function. When the count ENable is valid, the carry bit is generated from the look-ahead condition at the registered outputs. For a LOAD, the carry input is created from a HIGH condition on all the data inputs of the lesser significant stage.

Additional considerations

FIGURE 11
Pipelined look-ahead carry generator CRYGEN



Simulation of the 24-bit counter

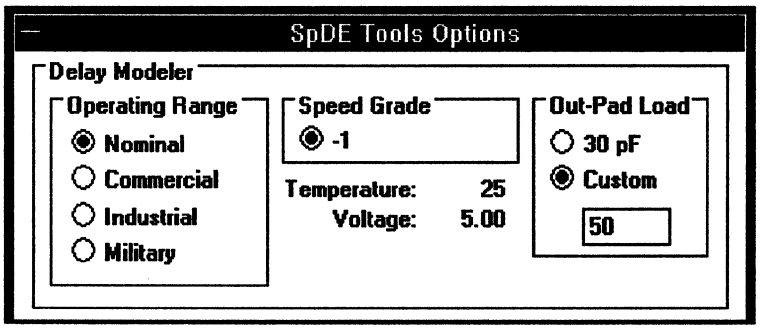


QAN3
JEDEC Gate Array Benchmark Set
QuickNote

CONTENTS

The pASIC™ Family of CMOS PFGA devices implements JEDEC Standard No. 12 using the pASIC Toolkit 3.0. Propagation Delays are calculated by the SpDE Delay Modeler with Operating Range set to nominal, Speed Grade set to –1 and Output Load Capacitance set to 50 pF. To obtain worst case conditions, multiply propagation delays by the appropriate K factor found in the datasheet OPERATING CONDITIONS, according to voltage, temperature and speed grade, e.g., for Commercial, –1 Speed Grade, multiply delays by 1.33.

SpDE Tools Options for Benchmark Tests



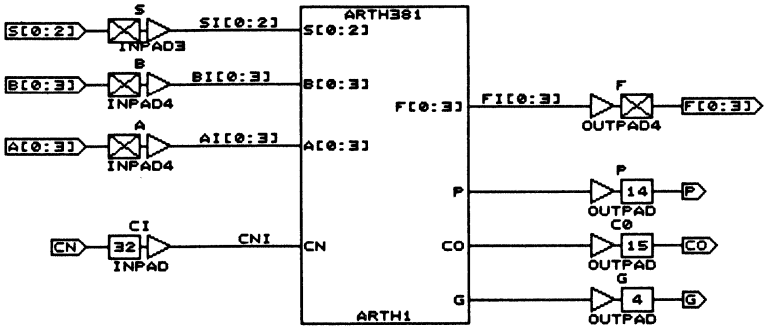
QUICKLOGIC

BENCHMARK 1

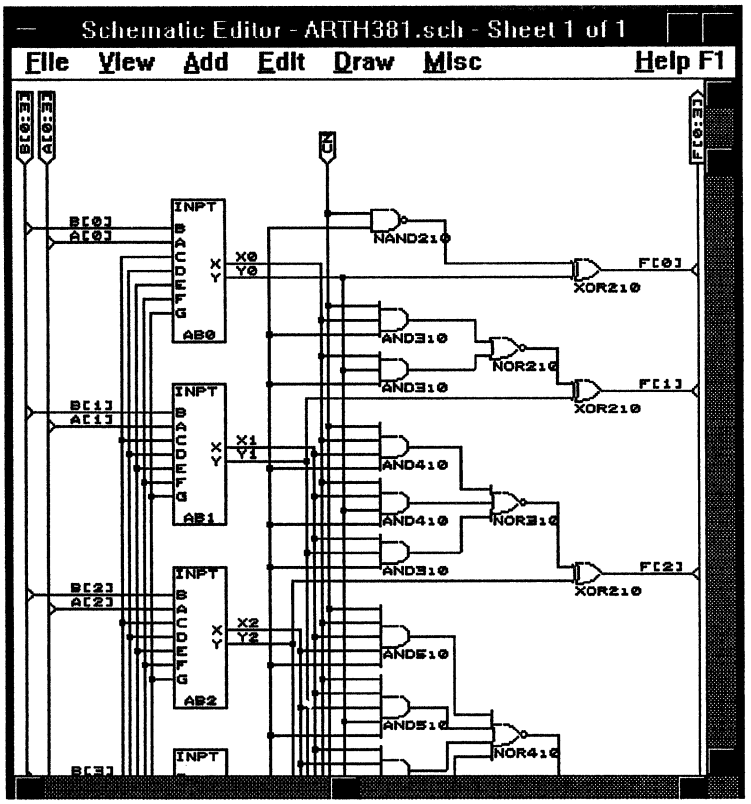
Performance Results

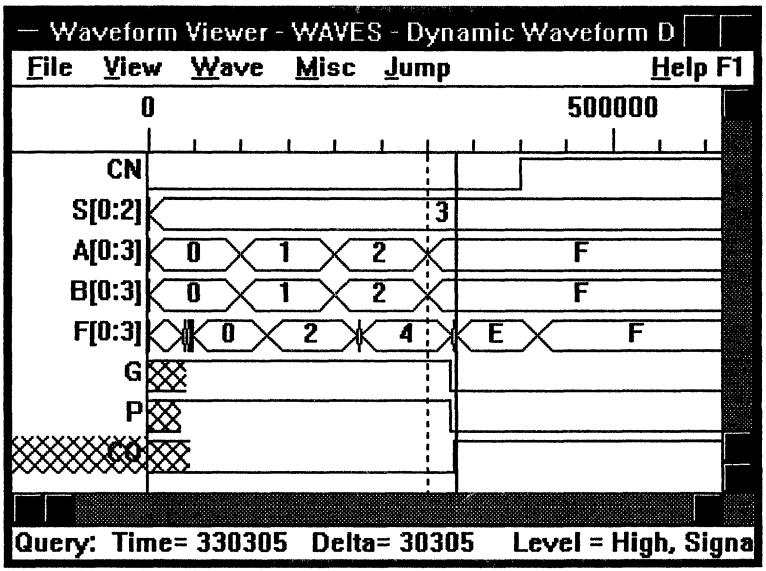
Max Delay	Any input to output	30.3 ns
Total logic cells used		42

4-bit ALU Symbol



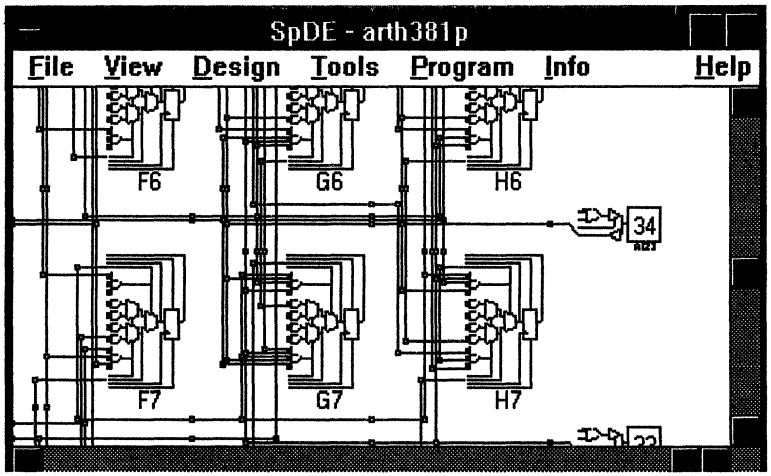
Schematic (partial)





Simulation Waveforms

...nominal 30.3 ns input-to-output delay



Physical View of A[2] Input

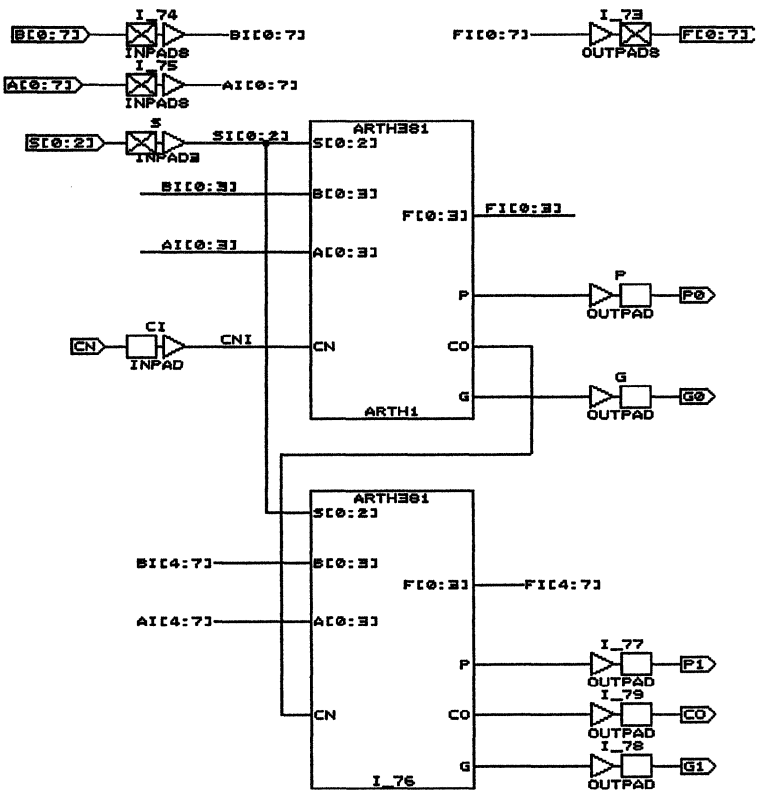
4

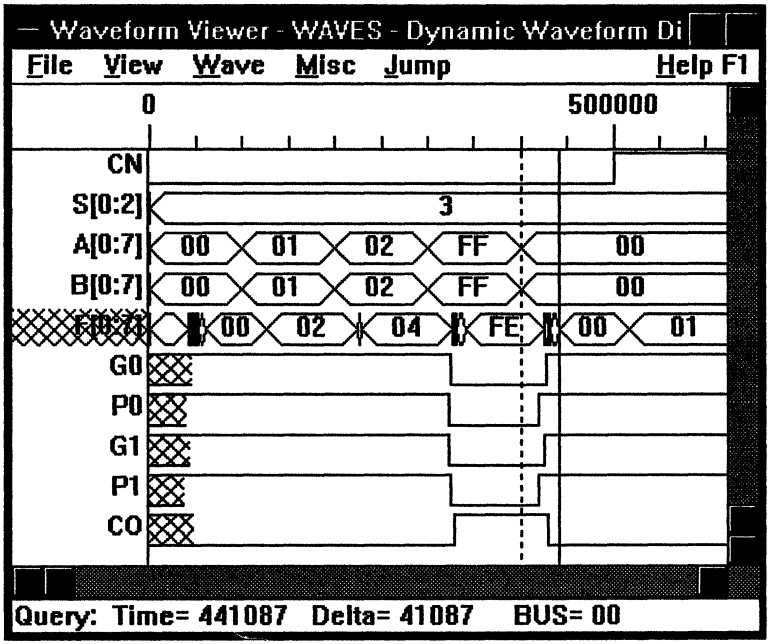
BENCHMARK 2

Performance Results

Max Delay	Any input to output	41.1 ns
Total logic cells used		83

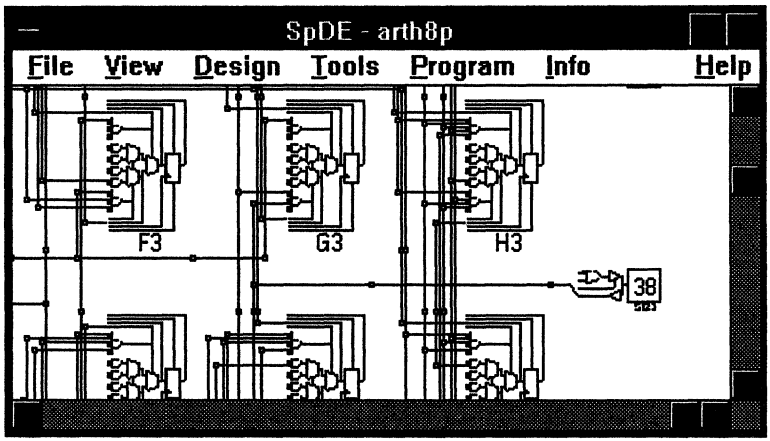
8-bit ALU Schematic





Simulation Waveforms

...nominal 41.1 ns input-to-output delay



Physical View of S[0] Input

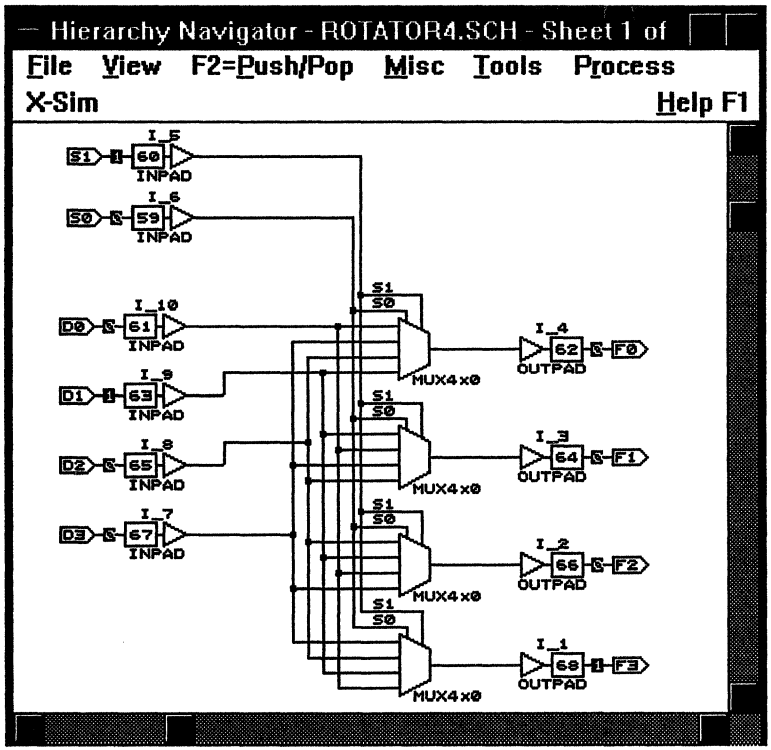
4

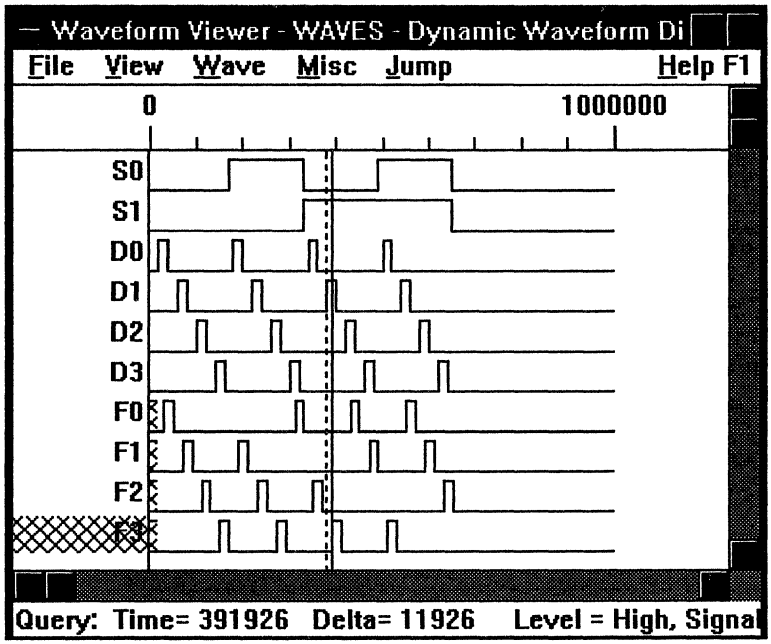
BENCHMARK 3

Performance Results

Max Delay	Any input to any output	11.9 ns
Total logic cells used		4

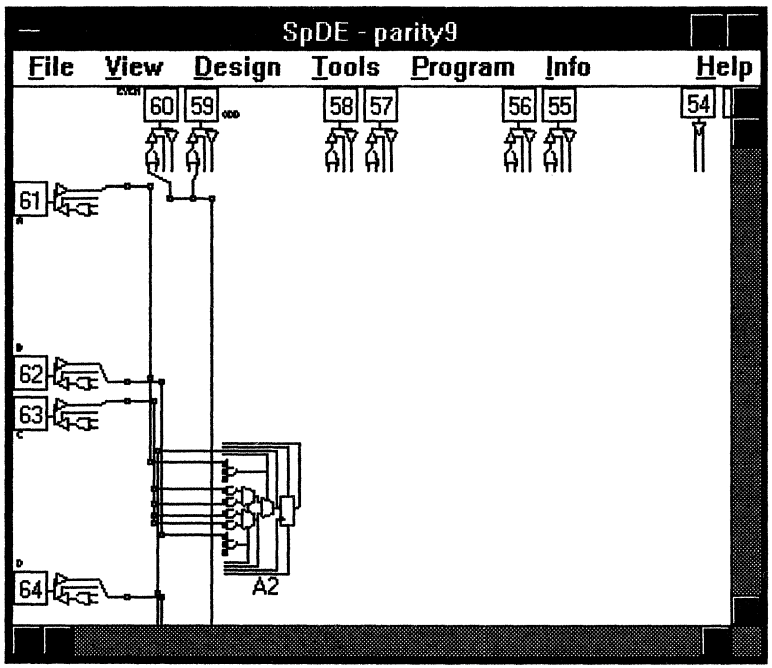
4-bit Rotator Schematic with Simulation Values





4-bit Rotator Simulation Waveforms

...nominal 11.9 ns input-to-output delay



Physical View of F0 Mux Logic Cell

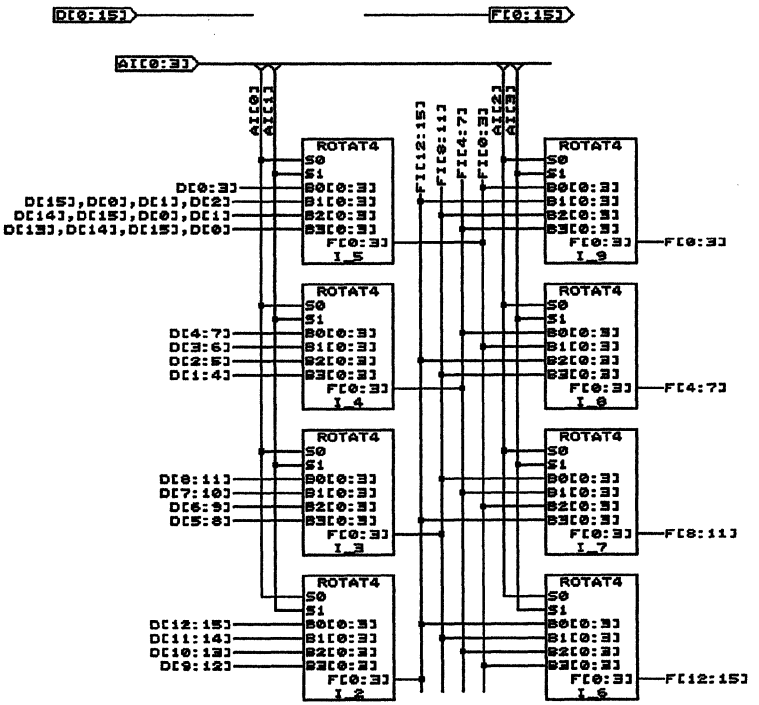
4

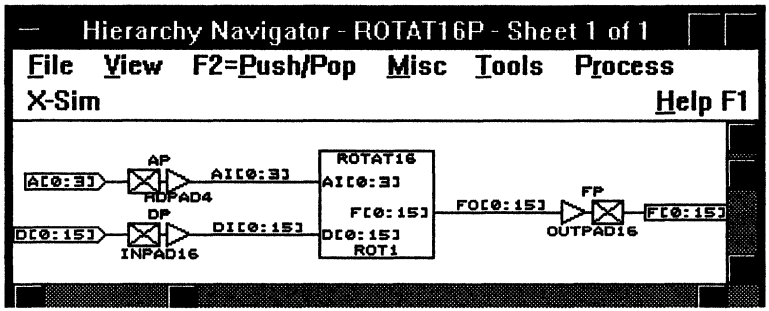
BENCHMARK 4

Performance Results

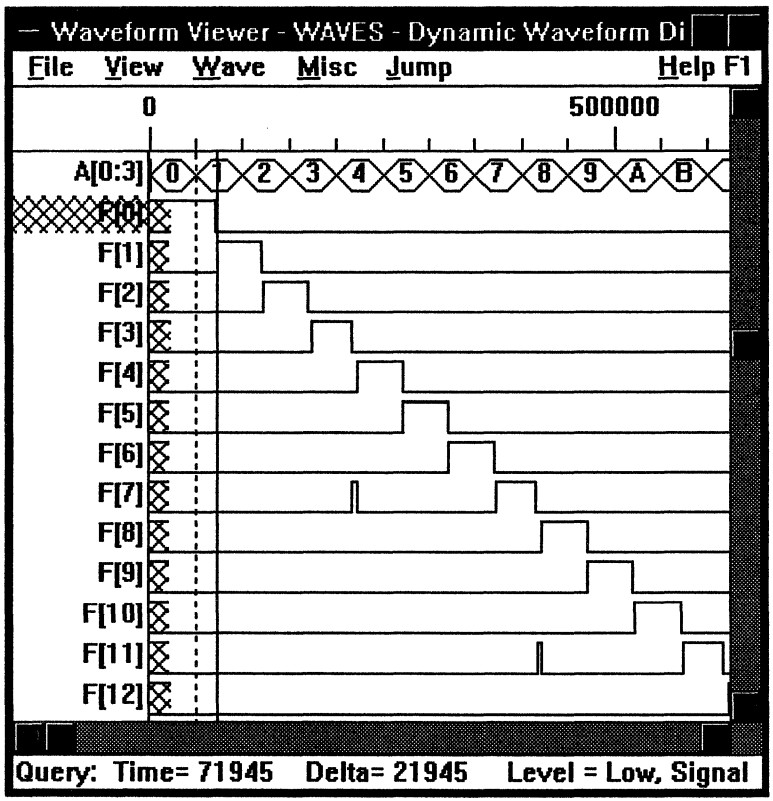
Max Delay	Any input to any output	21.9 ns
Total logic cells used		32

16-bit Rotator Schematic





16-bit Rotator Symbol



Simulation Waveforms

...nominal 21.9 ns input-to-output delay

4

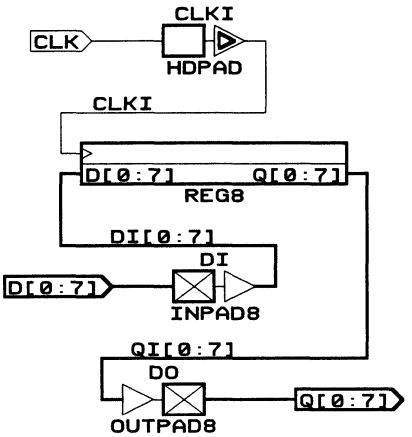
BENCHMARK 5
8-bit Register

Similar to a 74S374, the register benchmark demonstrates basic state machine operation from chip to chip.

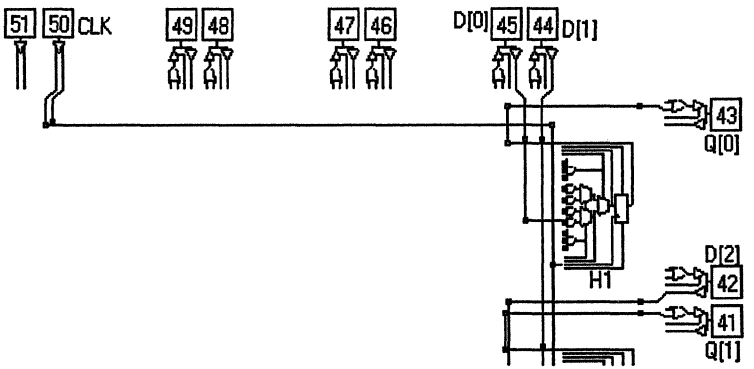
Performance Results

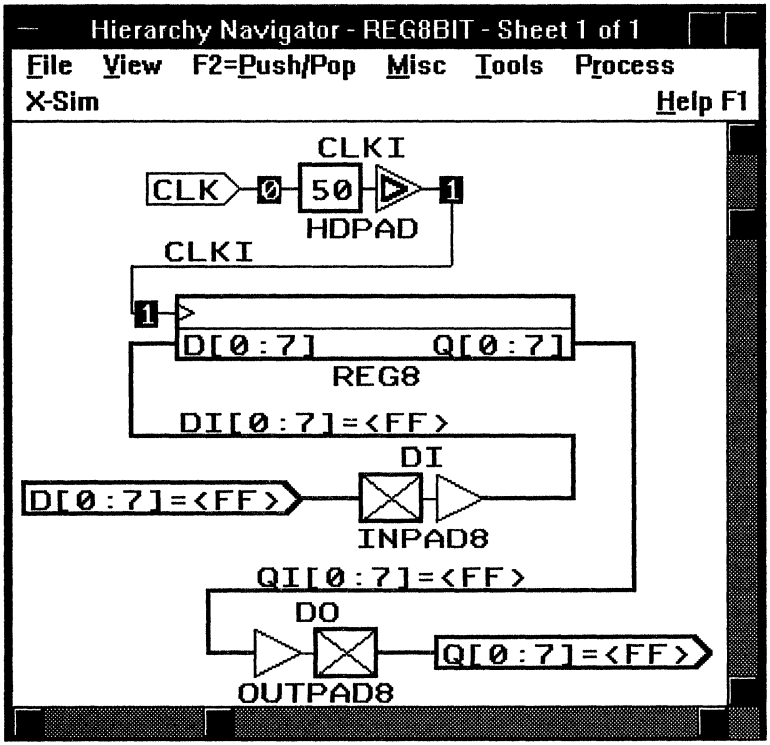
Min Setup at	Any D to Clock	5 ns
Min Hold for	Any D after Clock	–1 ns
Max Delay	Clock to any Q	10.3 ns
Total logic cells used		8

Schematic

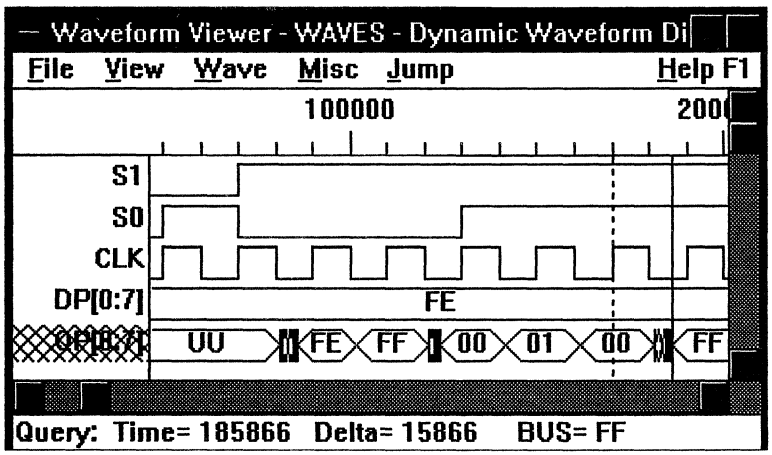


Physical View of Q0 Register and Clock Buffer





8-bit Register Schematic with Simulation Values



Simulation Waveforms

...nominal 10.3 ns clock to output

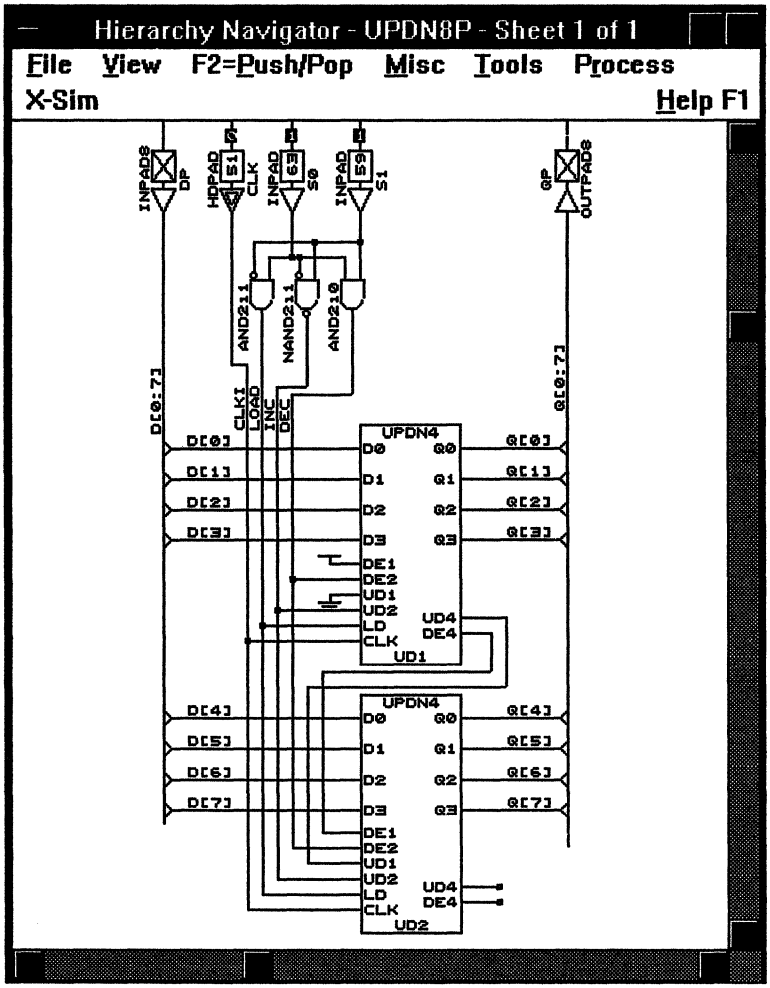
4

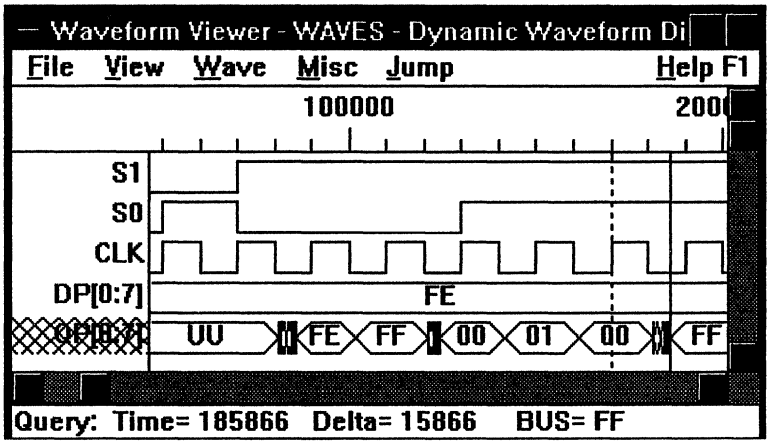
BENCHMARK 6

Performance Results

Max Delay	Clock to Q	15.9 ns
Max Frequency		50 MHz
Total logic cells used		15

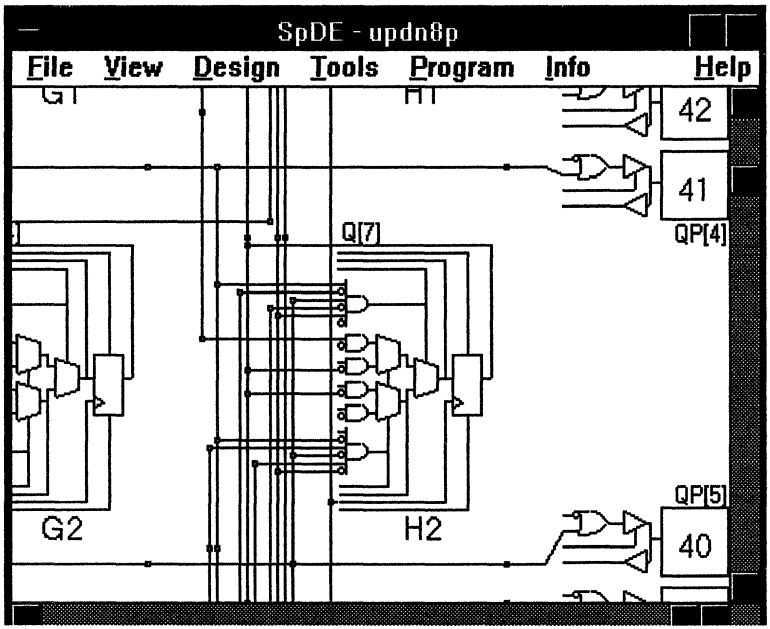
8-bit Up/Down Counter Schematic





Simulation Waveforms

...nominal 15.9 ns clock to out at 50 MHz



Physical View of Q7 Register

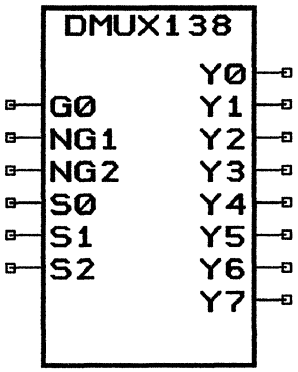
4

BENCHMARK 7

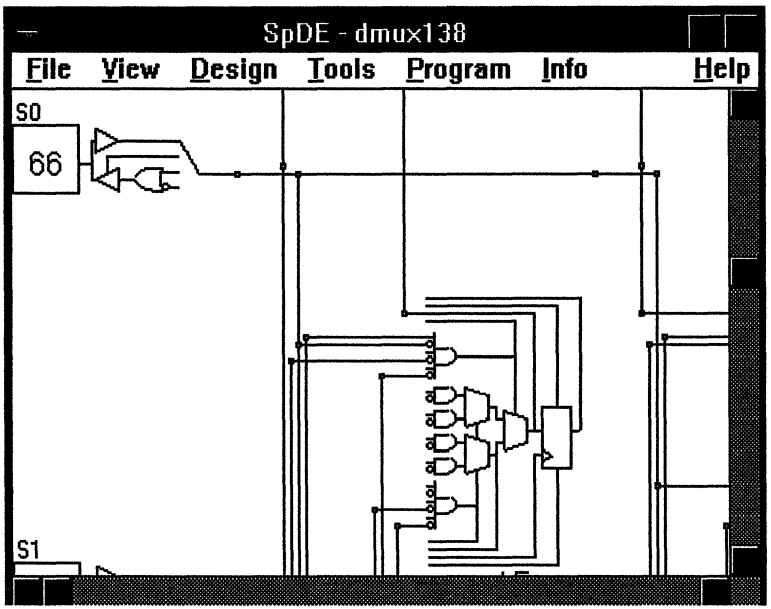
Performance Results

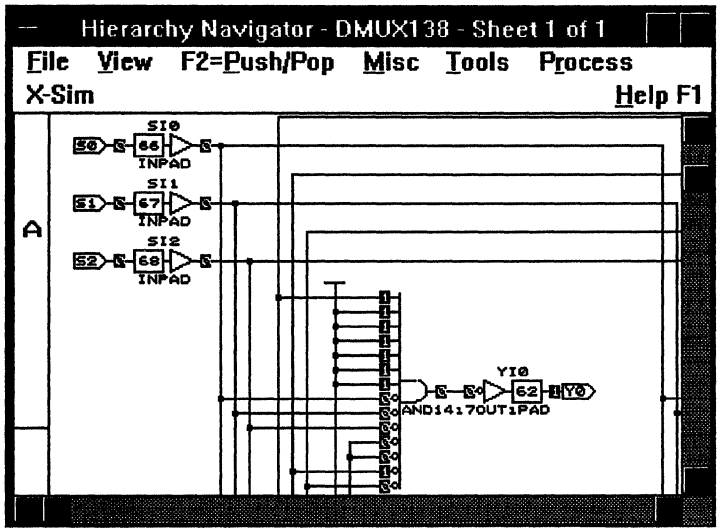
Max Delay	Any input to any output	18.7ns
Total logic cells used		8

3-to-8 Decoder Symbol

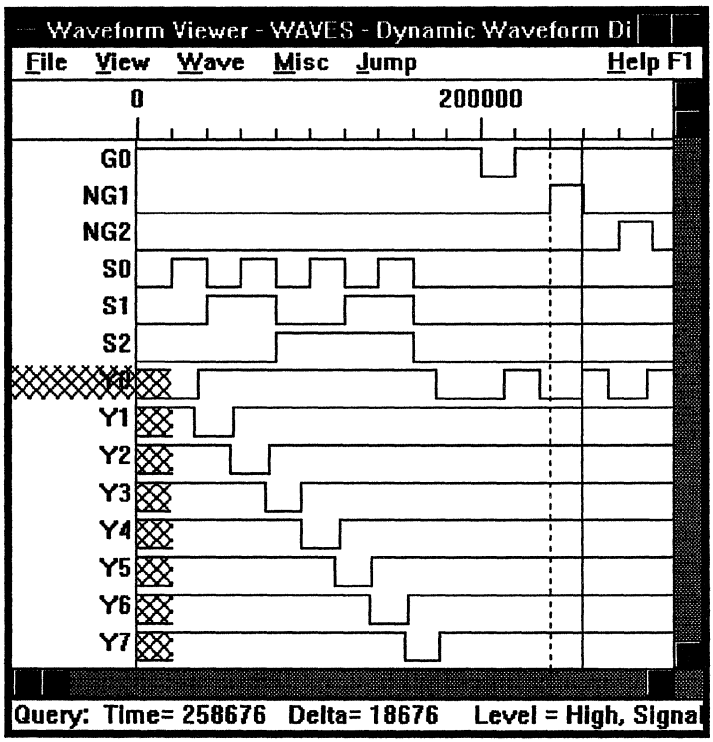


Physical View of Y0 Decode





3-to-8 Decoder Schematic with Simulation Values



Simulation Waveforms

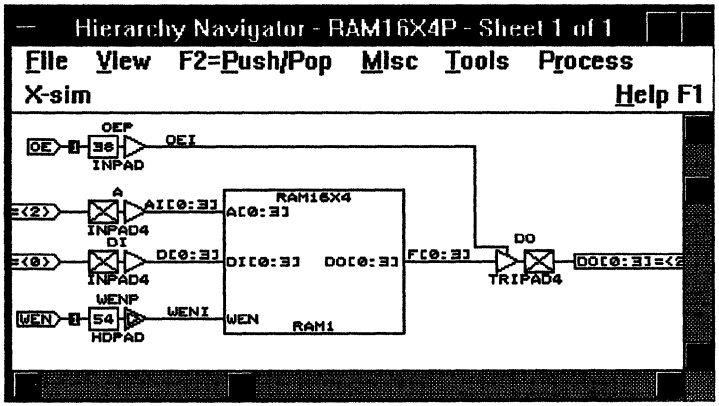
...nominal 18.7 ns in-to-out delay

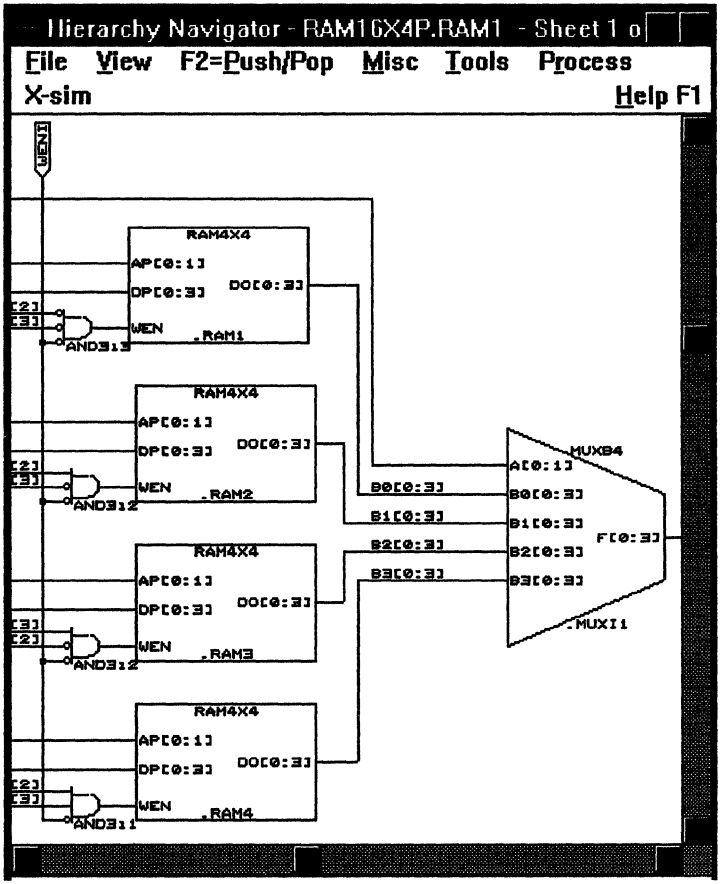
4

BENCHMARK 8
16x4 RAM
Performance Results

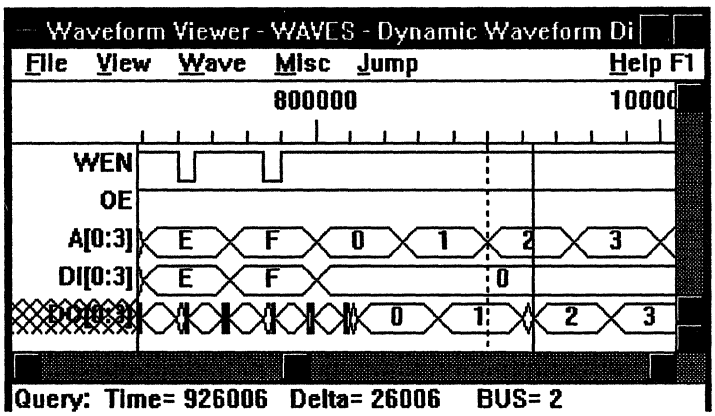
Max Delay	Any input to any output	26.0 ns
Total logic cells used		66

Schematic
Top Level with
Simulation Data





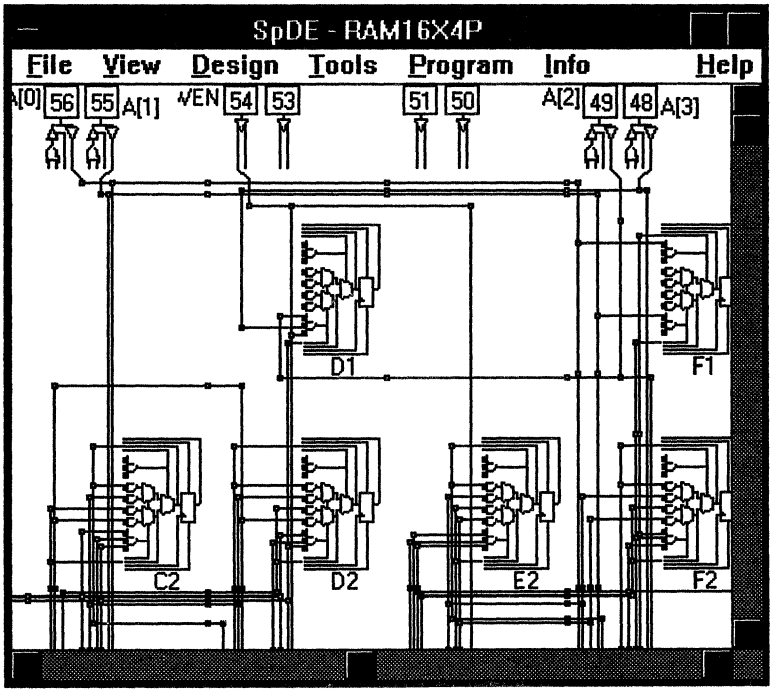
Schematic 2nd Level



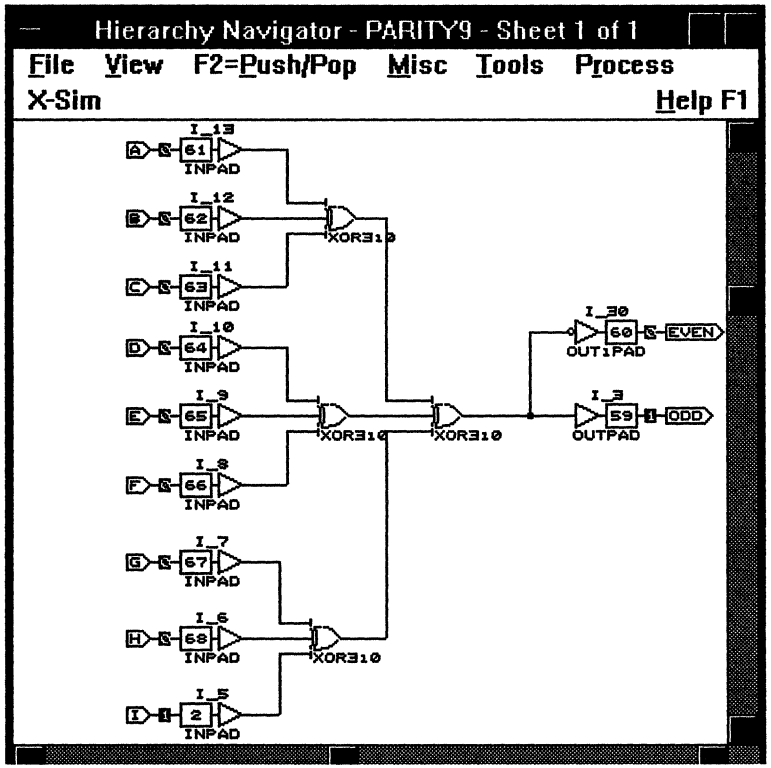
Simulation

...nominal 26 ns address-to-data access delay

Physical View
WEN and A[0..3]



Max Delay	Any input to output	16.8 ns
Total logic cells used		8



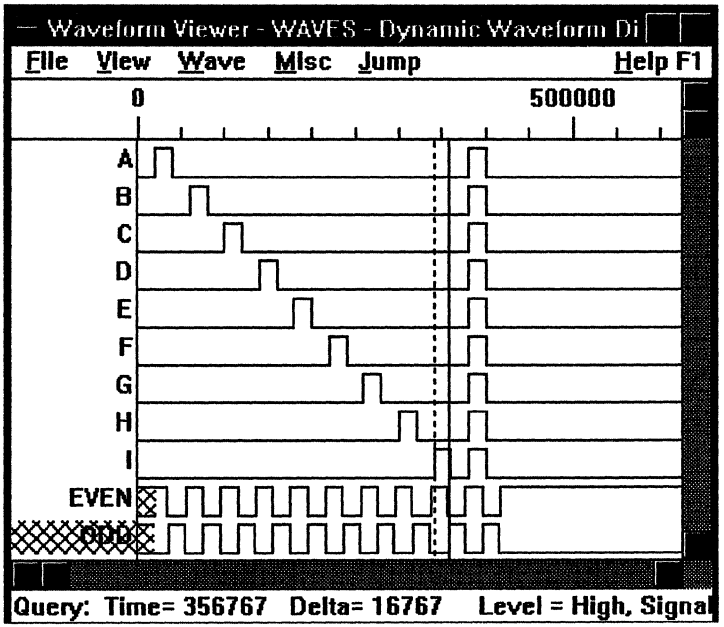
BENCHMARK 9

Performance Results

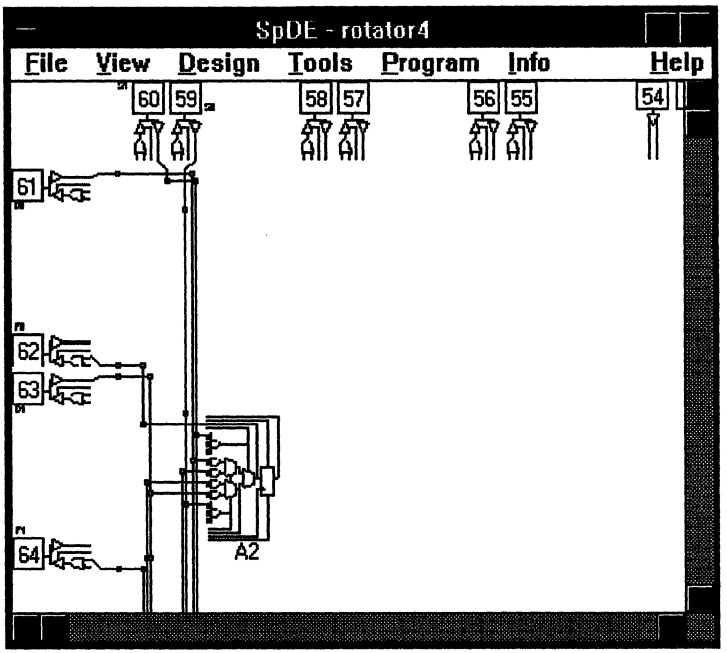
9-bit Parity Generator Schematic with Simulation Values

Parity Generator Simulation Waveforms

...nominal 16.8 ns input-to-output delay



Physical View of A, B, C, D & EVEN/ODD Pads



pASIC 1 FAMILY
Quality Program

OVERVIEW

The pASIC product quality program has the goal of achieving the highest quality as perceived by the customer. The program includes product acceptance inspection in the Standard Process Flow (see the following Standard Process Flow diagram). Electrical, visual, mechanical, solderability, and hermeticity inspection monitors check on the adequacy of the process controls. Inspection data defects, should they occur, are used as feedback to the operating departments for analysis and process improvement.

Designed for testability, the pASIC 1 Family incorporates many special test modes to verify circuit performance and array programmability. Test row and column patterns, specifically designed to detect array anomalies, are programmed at both the wafer sort and packaged product test stages. These test patterns and conditions represent the worst-case operating and programming conditions that will be encountered in the field. For example, the ViaLink element requires a 10- to 11-volt pulse to program. During wafer sort and final test, all devices are stressed near this voltage to eliminate products with potentially weak links.

The QL8x12 contains 76,000 ViaLink elements, including 1,336 test links. Half of the test links are programmed at wafer sort, the balance at final test. In a typical application, less than 5 percent of the links, approximately 3,400 are required to be programmed. Therefore, links representing one-third of the number which will be programmed at the customer site will have been checked on every device prior to shipment. A similar proportion of links are verified on all devices.

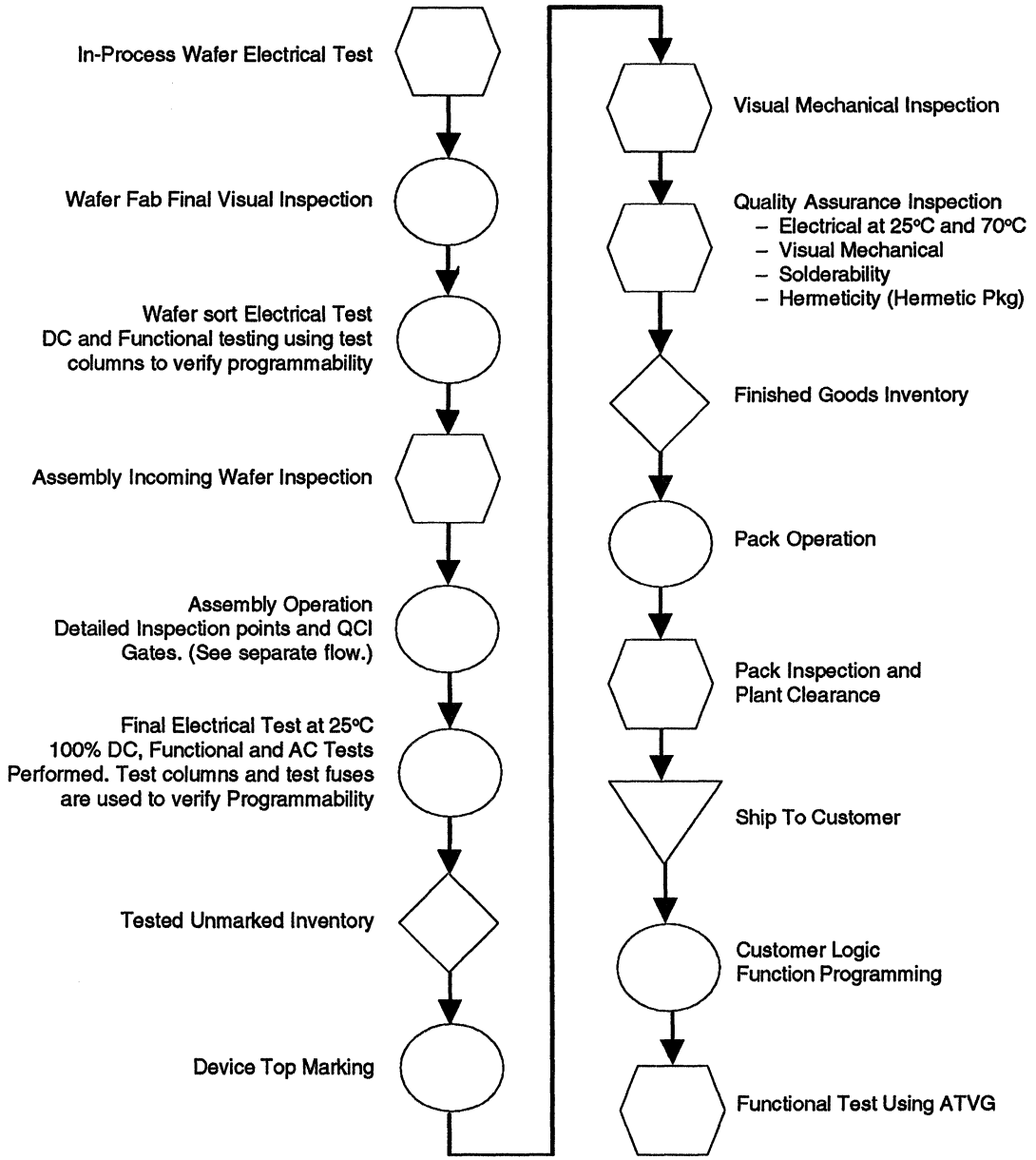
Another on-chip test feature is a silicon signature test column. The signature allows process sequence verification at each electrical test step. Devices not programmed with the proper signature for the sequence to be performed are rejected.

A serial scan path allows 100 percent functional testing of each logic cell and its interconnecting wiring channels. The channels are checked for inter and intra shorting under stress conditions. Dedicated input and I/O cells are fully tested to the guardband limit of data sheet D.C. specifications. A.C. performance is tested via an internal capability which chains all of the cells together. A chain of over 560 gates allows extremely accurate measurement without the traditional shortfalls encountered with high-resolution range measurements.

QUICKLOGIC

PRODUCT QUALITY ASSURANCE

Standard Process Flow



pASIC 1 FAMILY
Reliability Report

INTRODUCTION

The QuickLogic pASIC™ 1 family of very-high-speed FPGAs is built by integrating the QuickLogic ViaLink™ metal-to-metal antifuse programming element into a standard high-volume CMOS gate array process.

Reliability testing of pASIC devices is part of a continuous process to assure long-term reliability of the product. It consists of industry established accelerated life tests for basic CMOS devices plus additional stress tests for the ViaLink elements. The standard tests include high-temperature operating life, thermal shock, temperature cycle, biased 85/85, pressure pot, and high-temperature storage tests. The addition of two high-voltage life tests stresses the unprogrammed and programmed ViaLink elements beyond conventional CMOS reliability testing.

Results to date, from the evaluation of over 1700 pASIC devices from multiple wafer lots, indicate that the addition of the ViaLink element to a well-established CMOS process has no measurable effect on the reliability of the resulting product. There have been no failures in 31 million equivalent device hours of high temperature operating life. The observed failure rate is 0 FITs, and the failure rate at a 60% confidence level is 29 FITs.

PROCESS DESCRIPTION

The pASIC devices are fabricated using a standard, high-volume 1 μm CMOS gate array process with twin-well, single-poly, and double layer metal interconnect. This technology has been qualified to meet MIL-STD-883C. Over 1.1×10^9 equivalent device hours of operating life test have been accumulated since volume production began in 1989.

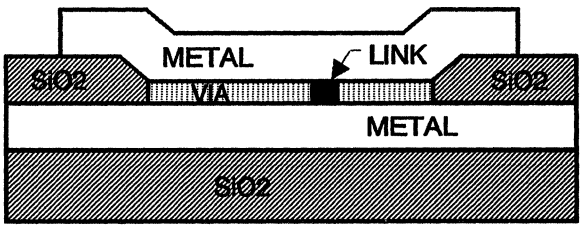
The technology employs a high-integrity TiW-Al+Cu-TiW metal system which offers very low contact resistance through the use of PtSi contacts, high resistance to electromigration, and freedom from stress-induced opens. [1]

The basic CMOS technology [2] features LDD-type transistors with a gate oxide thickness of 200Å. BPSG applied over the polysilicon lines is reflowed after contact formation giving a sloped entry for metal one. The interlevel dielectric is planarized with spin-on-glass. Vias are wet/dry etched giving sloped walls for good metal two step coverage. Interconnect metal lines contain layers of TiW on both sides of standard Al+Cu alloy.

QUICKLOGIC

The ViaLink element is located in an intermetal oxide via between the first and second layers of metal. It is created by depositing a very-high-resistance silicon film in a standard size metal one to metal two via. The silicon deposition is done at low temperature and causes no change to the properties of the CMOS transistors. When deposited at low temperatures, silicon forms an amorphous structure which can be electrically switched from a high-resistance state (≅ 1 G-Ω) to a low-resistance state (≅ 50Ω) for an off-to-on ratio of $2x10^7$. QuickLogic takes advantage of this property to create the ViaLink metal-to-metal antifuse programming element. See Figure 1.

FIGURE 1
Cross Section of a ViaLink Antifuse



The programming voltage of the ViaLink element varies with amorphous silicon thickness. For a desired programming voltage between 10-12 volts, the thickness of the amorphous silicon film is approximately 1000 Å. This is ideal for good process control and minimizes the capacitive coupling effect of an unprogrammed element located between the two layers of metal.

Amorphous silicon is deposited with standard semiconductor manufacturing equipment and processing techniques. In addition to antifuse elements, it is used in the high-volume fabrication of image sensors, decode and drive circuits for flat panel displays, and high efficiency solar cells.

FAILURE MECHANISMS IN THE pASIC DEVICE

A variety of failure mechanisms exists in CMOS integrated circuits. Since the overall failure rate is composed of various failure mechanisms, each having different temperature dependence and thus varying time-temperature relationships, it is important to understand the characteristics of each contributing failure mechanism. Table 1 lists nine key failure mechanisms that have been characterized for standard CMOS devices, plus the two mechanisms for the programmed and unprogrammed ViaLink elements.

Various accelerated life tests are used to detect the possible contribution of each mechanism to the overall failure rate of the device. Failure rate data taken at elevated temperature can be translated to a lower temperature through the Arrhenius equation. This equation, in the form of an acceleration factor, A_f, can be written as,

$$A_f = \exp[-E_a/k(1/T_s - 1/T_o)] \qquad (1)$$

where T_s is the stress temperature, T_o is the operating temperature of the device, E_a is the activation energy for that mechanism, and k is the Boltzmann constant.

TABLE 1 Failure Mechanisms Which May be Operative in pASIC Devices

Failure Mechanism	t_{50} dependence	Activation Energy (E_a)	Detection Tests
Insulator breakdown (leakage, opens)	exp(-β/E) value of β depends on the dielectric and may be temp. dependent.	Approx. 0.3 eV for SiO_2 and dependent on E	High voltage operating life test (HTOL)
Parameter shifts due to contamination (such as Na)	exp(E_a/kT) (Arrhenius)	1.0 eV	High temp. bias
Silicon defects (leakage, etc.)	Arrhenius	0.5 eV	High voltage and guard banded tests
Metal line opens from electromigration	$\frac{Wt}{J^2}$ exp(E_a/kT)	Approx. 0.7 eV for Al+Cu alloys	HTOL
Masking and assembly defects	Arrhenius	0.5 eV	High temp. storage and HTOL
Short channel charge trapping (V_T and g_m shifts)	$g_m \cong$ exp(-AE)	Appox. -0.06 eV	Low temp. high voltage oper. life test
Stress induced open metal (operative only on non-clad metal systems)	$W^m t^p$ exp (E_a/kT) (m and p range from 1.3 to 4.7)	0.6 to 1.4 eV (E_a difficult to reproduce)	Temp. cycling
Open metal from electrolytic corrosion	$(\%RH)^{-4.5}$exp(E_a/kT)	0.3 to 0.6	High temp./high humidity/ bias test
Wire bond failure from excessive gold-aluminum interdiffusion	$1/(Dt)^{1/2}$ where $D = D_0$exp(E_a/kT)	0.7 eV	HTOL
Unprogrammed ViaLink	exp(-BE)	0 eV	High V_{cc} static life test
Programmed ViaLink	exp(-PJ)	Approx. 0 eV	High V_{cc} operating life test

In Table 1, t_{50} is the mean time to failure, E is the electric field, E_a is the activation energy, k is the Boltzmann constant ($8.62X10^{-5}$eV/°K), W is the metal width, t is the metal thickness, J is current density, g_m is transconductance, V_T is the threshold voltage, A is a constant, m and p are constants, T is the absolute temperature, RH is the relative humidity, and D is the diffusion constant.

ACCELERATED LIFE TESTS ON QL8X12

The purpose of a life test is to predict the reliability and failure rate of a device. However, a device operating under normal operating conditions would require years of testing to determine its long-term reliability. Methods of accelerating failures developed in the industry allow accurate prediction of a device life time and failure rate in a much shorter time duration. Accelerated stress tests are run at high temperature, high voltages, or a combination of both. Table 2 contains the results of the tests performed on a programmed QL8X12, where approximately 3500 ViaLink elements were programmed and about 75,000 ViaLink elements were left unprogrammed. These numbers are typical for a fully utilized device.

TABLE 2 Results of Accelerated Life Tests on the QL 8X12

Test	Process Qual. Acceptance Requirements	Test Results
HTOL, 1000 hrs, 125°C, V_{cc}= 5.5V, MIL-STD-883C, Method 1005	≤100 FITs @ 55°C, E_a= 0.7eV, 60% confidence	0 observed FITs, 29 FITs at a 60% confidence. 400 units from 4 lots
High temp. storage, 1000 hrs., 150°C, unbiased	≤1% cum. failures per test	0% 105 units from 3 lots
THB, 1000 hrs., alternately biased, 85% R.H., 85°C, JEDEC STD 22-B Method A101	≤1% cum. failures per test	0% 300 units from 3 lots
Temp. cycle, 1000 cycles, -65°C to 150°C, MIL-STD-883C, Method 1010	≤1% cum. failures per test	0% 110 units from 4 lots
Thermal shock, 100 cycles, -65°C to 150°C, 883C, Method 1011	≤1% cum. failures per test	0% 105 units from 3 lots
Pressure Pot, 168 hrs., 121°C, 2.0 atm., no bias	≤1% cum. failures per test	0% 105 units from 3 lots
High Vcc Static Life 1000 hrs, 25°C, V_{cc} = 7.0V Static	< 20 FITs due to unprogrammed ViaLink element, A_f = 130	0 observed FITs. 363 units from 5 lots
High Vcc Dynamic Life, 1000 hrs, 25°C, Vcc = 6.0V, 15MHz	< 20 FITs due to programmed ViaLink element, A_f = 380	0 observed FITs. 300 units from 3 lots. 1 Failure not related to ViaLink element

A failure is defined as any change in the DC characteristic beyond the data sheet limits and any measurable change in the AC performance.

The overall reliability of the QL8X12 devices as indicated by the results of the tests shown in Table 2 is 29 FITs with a 60% confidence.

Details of each of the tests of Table 2 are given in the following sections. The failure mechanisms specific to the ViaLink antifuse element are described in detail. All tested devices were in the 68-lead plastic chip carrier (PLCC) package.

STANDARD CMOS TESTS AND RESULTS

High-Temperature Operating Life Test

HTOL is the life test which operates the device at a high Vcc and high temperature. This test is used to determine the long-term reliability and failure rate of the device in the customer environment. The specific condition of this test is defined by the MIL-STD-883C Quality Conformance Test. The devices are operated at 5.5v and 125°C for 1000 hours. The acceleration due to temperature can be calculated by using equation (1), assuming an average activation energy of 0.7eV and an operating temperature of 55°C. The observed failure rate in FITs is,

Failure Rate = (failures) x (10^9 device-hrs)/(total equivalent device-hrs) (2)

The generally reported failure rate is a 60% confidence level of the observed FITs. The failure rate at this confidence level is calculated using Poisson statistics since the distribution is valid for a low failure occurrence in a large sample.

The acceleration factor from equation (1), for 55°C and E_a = 0.7eV is 78. Therefore, from the results shown in Table 3, the QL8X12 has been operating for more than 31 million equivalent device hours without a failure. The observed failure rate is 0 FITs and the failure rate at a 60% confidence level is 29 FITs.

TABLE 3
Results of High-Temperature Operating Life Test

High-Temperature Operating Life Test
V_{cc} = 5.5V, Temp. = 125°C, f = 1MHz, 68-lead PLCC

Fab Lot	Quantity	Failures @ Hours		
		168	500	1000
18362	100	0	0	0
19194	100	0	0	0
19618	100	0	0	0
20454	100	0	0	0

High-Temperature Storage

High-temperature storage test is a 150°C, 1000 hour, unbiased bake. This test accelerates failures due to mobile charge, such as sodium. The results in Table 4 demonstrate the stability of the programmed and unprogrammed ViaLink element and the long-term shelf life of the QL8X12.

TABLE 4 Results of High-Temperature Storage Test

High-Temperature Storage Test
No bias, Temp. = 150°C, 68-lead PLCC

Fab Lot	Quantity	Failures @ Hours		
		168	500	1000
18362	35	0	0	0
19194	35	0	0	0
19390	35	0	0	0

Temperature, Humidity, and Bias (85/85)

The temperature, humidity, and bias test is performed under severe environmental conditions. The device is exposed to a temperature of 85°C and a relative humidity of 85% for 1000 hours, while the pins are alternately biased between 0 and 5.5 volts (JEDEC STD 22-B). This test is effective at detecting corrosion problems, while also stressing the package and bonding wires. Table 5 shows that the QL8X12 had no failures.

TABLE 5 Results of Temperature, Humidity, and Bias Test

Temperature, Humidity, and Bias Test
85% R.H., Temp. = 85°C, pins alternately biased at 5.5V, 68-lead PLCC

Fab Lot	Quantity	Failures @ Hours		
		168	500	1000
19194	100	0	0	0
19618	100	0	0	0
19454	100	0	0	0

Temperature Cycle Tests

The temperature cycle test stresses the packaged part from -65°C to 150°C for 1000 cycles. The air-to-air cycling follows the MIL-STD-883C Quality Conformance Test. This test checks for any problems due to the thermal expansion stresses. The plastic package, lead frame, silicon die, and die materials expand and contract at different rates. This mismatch can lead to cracking, peeling, or delamination of the high stress layers. The results in Table 6 show that the QL8X12 had no failures.

TABLE 6 Results of Temperature Cycle Test

Temperature Cycle Test
Air-to-air -65°C to 150°C, 68-lead PLCC

Fab Lot	Quantity	Failures @ Cycle		
		250	500	1000
16921	5	0	0	0
18362	35	0	0	0
19194	35	0	0	0
19618	35	0	0	0

Thermal Shock Tests

The thermal shock test cycles the packaged part through the same temperatures as the temperature cycle test except that the cycling is done from liquid to liquid. The temperature change is nearly instantaneous in this case. The rapid temperature change can result in higher stresses in the package and lead frame. The results in Table 7 show that the QL8X12 had no failures.

TABLE 7 Results of Thermal Shock Test

Thermal Shock Test
Liquid to liquid, -65°C to 150°C, 68-lead PLCC

Fab Lot	Quantity	Failures @ Cycle
		100
18362	35	0
19194	35	0
19618	35	0

Pressure Pot Tests

The pressure pot test is performed at 121°C at 2.0 atmospheres of saturated steam with devices in an unbiased state. This test forces moisture into the plastic package and tests for corrosion in the bonding pads and wires which are not protected by passivation. Corrosion can also occur in passivated areas where there are micro cracks or poor step coverage. QL8X12 had no failures as shown in Table 8.

TABLE 8
Results of Pressure Pot Test

Pressure Pot Test
Pressure = 2.0 atm., Temp. = 121°C, no bias, 68-lead PLCC

Fab Lot	Quantity	Failures @ Hours		
		48	96	168
18362	35	0	0	0
19194	35	0	0	0
19390	35	0	0	0

VIALINK ELEMENT RELIABILITY TESTS AND RESULTS

The ViaLink antifuse is a one time programmable device. In the unprogrammed state it has a resistance of greater than one gigaohm and capacitance of less than one femtofarad.

The application of a programming voltage across the antifuse structure, above a critical level causes the device to undergo a switching transition through a negative resistance region into a low-resistance state. The magnitude of the current allowed to flow in the low resistance state, the programming current, is predetermined by design. A link of tungsten, titanium, and silicon alloy is formed between metal one and metal two during the programming process.

The link has a metallic-like resistivity of the order of 500 micro-ohms-cm and is responsible for the low 50 ohm resistance that is a unique characteristic of the QuickLogic ViaLink antifuse.

The link forms a permanent, bidirectional connection between two metal lines. The size of the link, and hence, the resistance, depends on the magnitude of the programming current. Figure 2 shows the relationship between programming current and programmed link resistance. Figure 3 shows the distribution of link resistance for a fixed programming current.

FIGURE 2 Resistance vs 1 / Programming Current

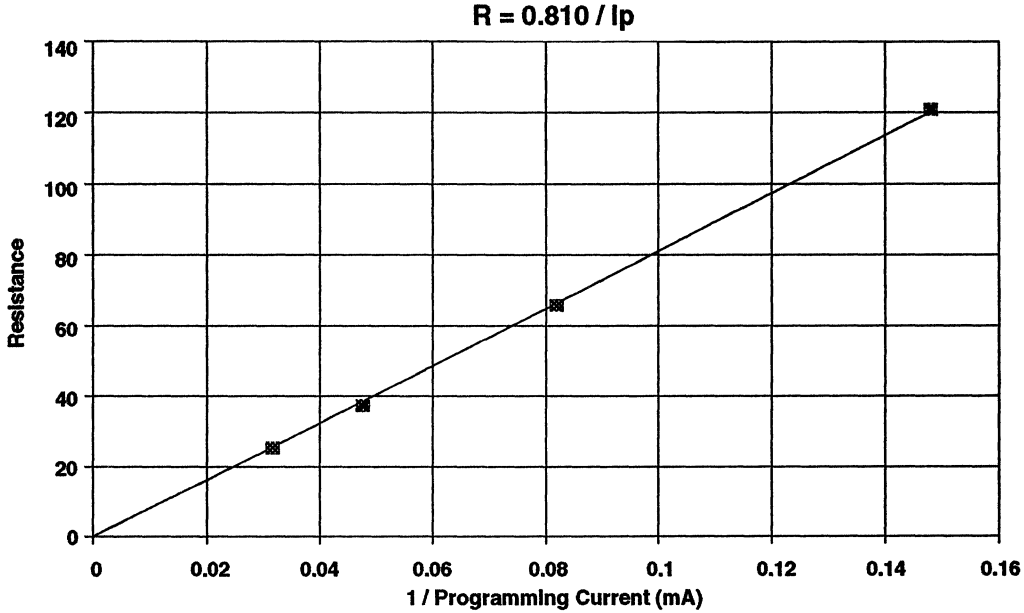
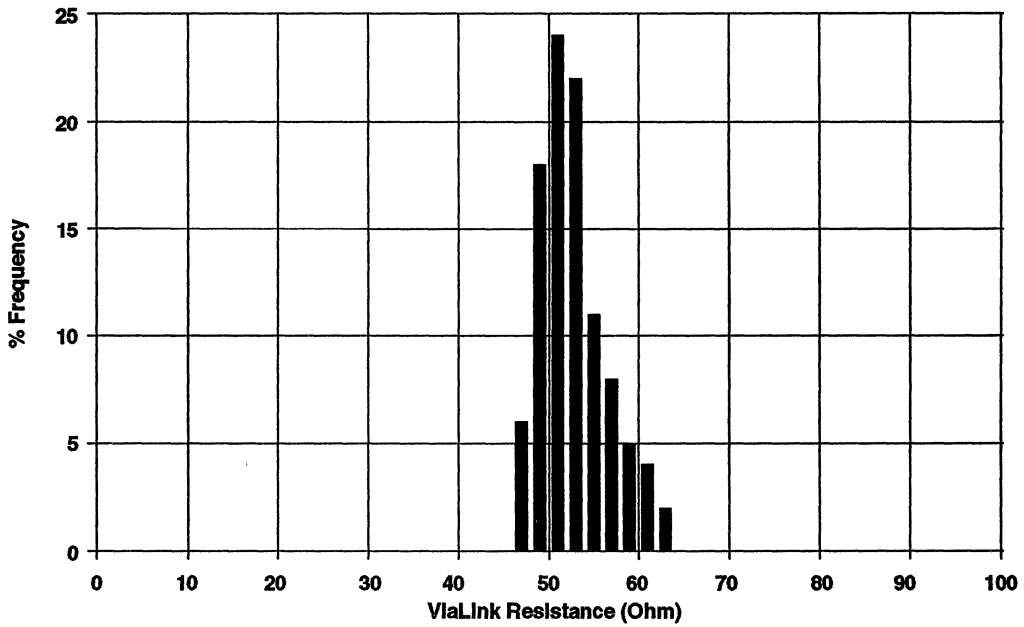


FIGURE 3 Distribution of ViaLink Resistance at Ip = 15 mA

Average = 52.3 Ohms Std Deviation = 3.69



5

Unprogrammed ViaLink Element Reliability

Reliability studies on an antifuse, that can exist in two stable resistance states, must focus on the ability of an unprogrammed and a programmed device under stress to remain in the desired state. In the context of standard IC testing, the antifuse should be stressed under conditions similar to those for a dielectric (in the unprogrammed state) and for a conductor (in the programmed state).

For ViaLink elements in the unprogrammed state, the tests must determine their ability to withstand applied voltages over the range of operating conditions without changing resistance or becoming programmed. Amorphous materials might be expected to show gradual changes in resistance as a result of relaxation or annealing. Reliability studies have been designed to explore these effects.

When a ViaLink element is stressed at high electric fields its resistance can decrease from the initial 1 G-Ω value. The reliability testing program examined the time for the resistance to reach 50 M-Ω at different stress fields. Figures 4 & 5 illustrate that because of time constraints (≅500 years), it is impossible to detect this effect at normal operating fields in systems.

The pASIC device is designed to operate with resistance of the unprogrammed ViaLink element from 50 M-Ω to greater than 1 G-Ω. Even with all unprogrammed ViaLink elements at 50 M-Ω, the pASIC product would remain within the guaranteed speed and standby Icc specifications.

Figure 4 shows the time required for a ViaLink element to reach 50 M-Ω under various applied electric fields at different temperatures. The time required for the change is not accelerated by temperature over the studied range of electric fields. The activation energy, E_a, for this process is zero.

Figure 5 shows the time required for a ViaLink element to reach 50 M-Ω under various electric field stresses. A range of amorphous silicon thicknesses have been included in this chart. The data can be modeled using the equation,

$$t_{50M\Omega} = t_0 \exp(-BE) \qquad (3)$$

where the time to 50 M-Ω decreases exponentially with increasing applied electric field. The constant t_0 is $3x10^{15}$ seconds and the field acceleration factor, B, is 20 cm/MV. The model is valid for electric fields, E, below 1.6 MV/cm. Above this field, programming occurs. The electric field for 5.0 volt Vcc operation with a typical amorphous silicon thickness is 0.61 MV/cm, which extrapolates $t_{50M\Omega}$ to $1.5x10^{10}$ seconds, or 500 years. The time to 50 M-Ω for the worst case amorphous silicon thickness and operating at worst case Vcc is in excess of 30 years.

The high field effect is both predicable and reproducible. This effect is inherent to the amorphous silicon in the ViaLink element [3]. The pASIC device has been designed to operate where the effect is minimized and has no impact on the reliability of the pASIC device.

FIGURE 4 Temperature Dependence of Time to 50 Megohms (Lot 617 Wafer 8)

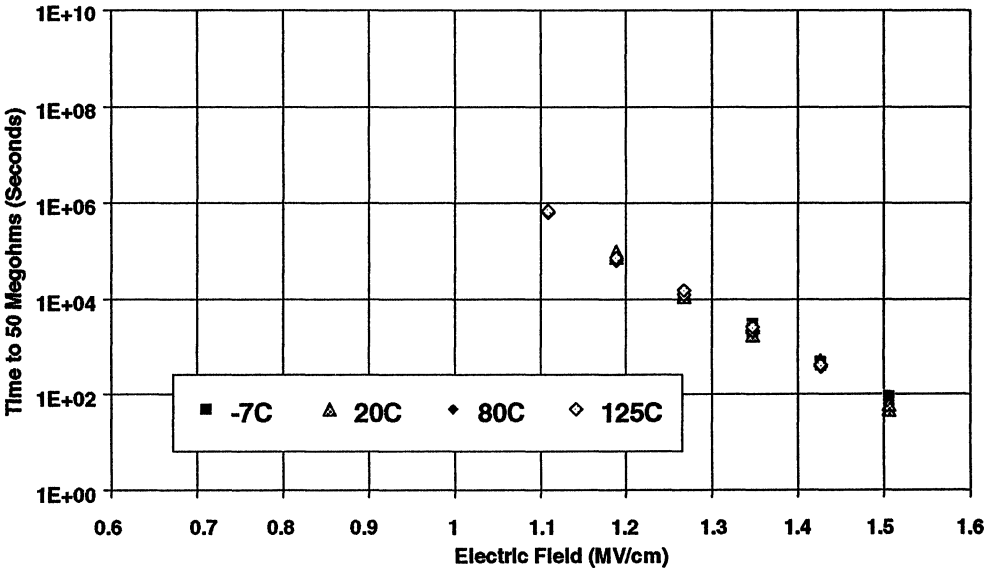
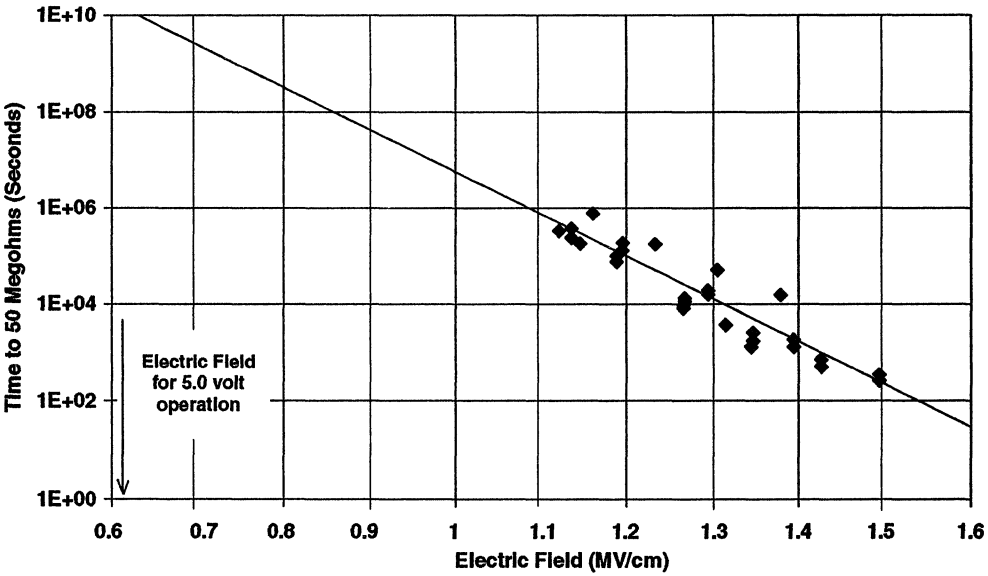


FIGURE 5 Electric Field Acceleration of Unprogrammed ViaLink Element



5

Accelerated Stress Tests for Unprogrammed ViaLink Elements

The high field effect is created in the packaged QL8X12 device through a high Vcc static life test. This test stresses the unprogrammed ViaLink element with a Vcc = 7.0 volts for 1000 hours. Over 360 QL8X12 devices from four lots have been tested. This condition stresses over 20,000 unprogrammed ViaLink elements in each QL8X12. The failure criteria for the pASIC device for this test is the same as that of the previous tests, with emphasis placed on the standby Icc, which increases as the resistance of the unprogrammed ViaLink element decreases. The acceleration factor for this stress is calculated by using equation (3) to find the ratio of the t_{50M} for E = 0.61 MV/cm at 5 volts and E = 0.85 MV/cm at 7 volts. This test has an acceleration factor = 130 for the unprogrammed ViaLink element. The test results in Table 9 show that no device has failed this stress in more than 73 million equivalent device hours. Life tests continue to run; two lots have reached 1500 hours, and one lot has exceeded 3500 hours.

TABLE 9
Results of High V_{cc} Static Life Test

High V_{cc} Static Life Test
V_{cc} = 7.0V static, Temp. = 25°C, 68-lead PLCC

Fab Lot	Quantity	Failures	Total Hours
16558	14	0	3650
18362	39	0	1907
19194	110	0	1756
19618	101	0	1456
20454	100	0	1000

Programmed ViaLink Element Reliability

The reliability tests on the programmed ViaLink element must demonstrate the stability of the link resistance in the programmed state. While an increase in resistance of the programmed device may not be catastrophic, a higher resistance can affect the device operating speed. Because the programmed ViaLink element has become part of the on-chip interconnect, reliability tests should be similar to those that are normally used to validate the integrity of metal interconnects.

In operation, the programmed ViaLink elements are subjected to capacitive switching current of the interconnect network. They do not experience any DC current or voltage. See Figure 6. Each switching pulse forces a capacitive charging current to flow through programmed ViaLink elements into the network on the rising edge, and an opposite, or discharging current, to flow on the falling edge. Each cycle is analogous to a read pulse for a memory device. A 10% change in resistance was set as the read disturb criteria for the

ViaLink element. The typical impedance of a network is about 500Ω with the programmed ViaLink element contributing 50Ω. A 10% increase in the ViaLink resistance will increase the network impedance by approximately 5Ω, or 1%. This increase in resistance will increase a network delay in the pASIC device by about the same proportion.

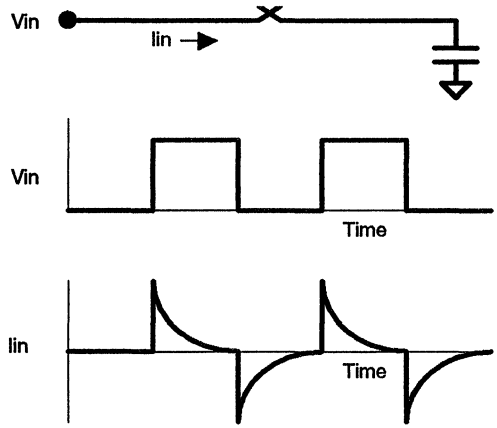


FIGURE 6 Switching of Programmed ViaLink Antifuse

Programmed ViaLink elements were stressed under severe capacitive currents. AC stresses rather than DC stresses were used to accelerate the failures for closer correlation with actual operation. The mean number of read cycles to disturb, N_{50}, for various temperatures were found to be identical. The absence of temperature dependence indicates an $E_a \cong 0$. Figure 7 shows the acceleration of the read disturb at high AC current densities through the programmed ViaLink element. Thus, the number of cycles to disturb can be modeled as,

$$N_{50} = N_0 \exp(-PJ) \qquad (4)$$

Where $N_0 = 7 \times 10^{41}$ cycles is a constant, $P = 1.2\ cm^2/MA$ is the current density acceleration factor, and J is the peak AC current density through the link.

The QL8X12 is designed to operate at worst case AC current density of $40 \times 10^6\ A/cm^2$. The N_{50} for this condition is 1×10^{21} cycles. The failure rate can be calculated using the cumulative density F(t),

$$F(t) = \Phi \ln [(N/N_{50})/\sigma] \qquad (5)$$

The failure distribution can be determined by plotting the data on a log normal probability scale versus the log of the number of cycles to failure. See Figure 8. The shape parameter, σ, is $\ln(N_{50}/N_{16}) = 2.5$.

FIGURE 7 Acceleration of Read Disturb for Programmed ViaLink Element

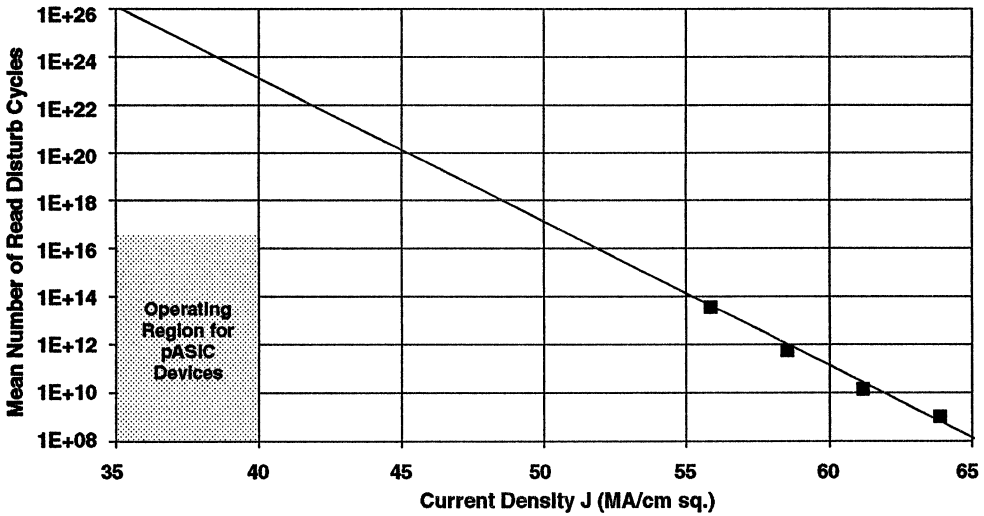
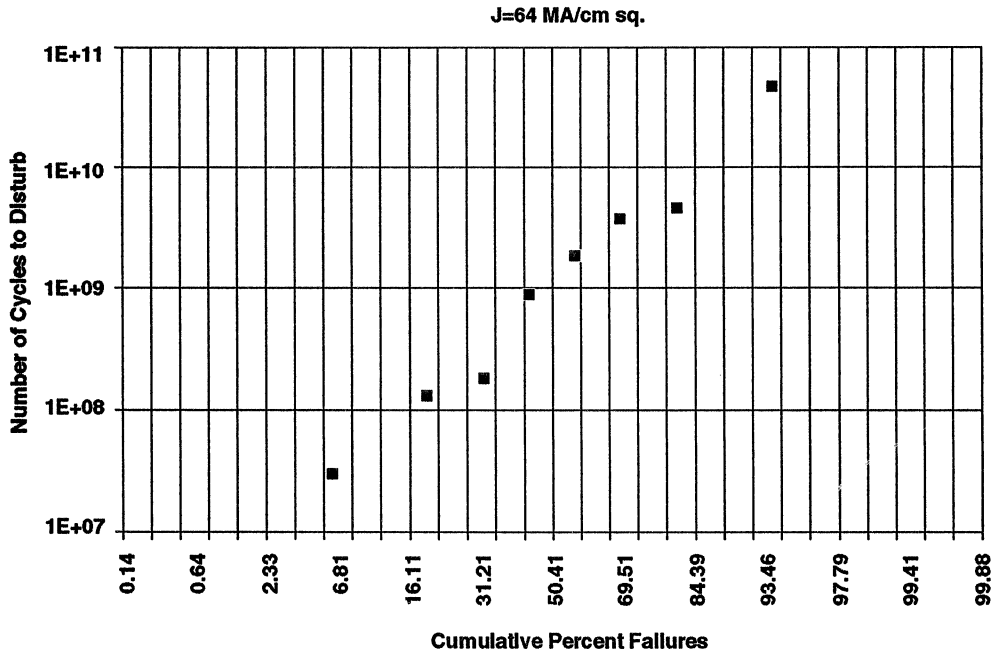


FIGURE 8 Distribution of Read Disturb on Programmed ViaLink Elements



High AC current density occurs at low frequencies where there is sufficient time for the network to be fully charged or discharged. At frequencies above 50 MHz, AC current through a ViaLink element decreases due to incomplete charging and discharging cycle. The worst case pattern in a programmed pASIC has less than 150 ViaLink elements operating at $40x10^6$ A/cm^2. Most of the programmed ViaLink elements operate at much lower current densities. Using equation (5), the cumulative failure rate for the ViaLink element operating at $40x10^6$ A/cm^2 for $1.6x10^{16}$ read cycles (equivalent to continuous operation at 50 MHz for 10 years) is 0.6 parts per million. This failure rate for the pASIC device is 90 parts per million operating under worst case condition for 10 years. The failure rate of the programmed ViaLink element would contribute 1 FIT to the overall failure rate of the pASIC device.

Accelerated Stress Tests for Programmed ViaLink Elements

The high Vcc dynamic life test stresses the QL8X12 with Vcc = 6.0 volts at 15 MHz for 1000 hours. This test stresses the programmed ViaLink elements at $45x10^6$ A/cm^2 for $5.4x10^{13}$ cycles. The acceleration factor, calculated from equation (4), is 380. This test is equivalent to $2.0x10^{16}$ switching cycles, or continuous operation under worst case condition at 50 MHz for 12 years. Three hundred QL8X12 devices from 3 lots have been stressed. The failure criteria is the same as previously described, with emphasis placed on careful monitoring of AC performance. Test results in Table 10 show that there have been no failures of the programmed ViaLink elements in over 34 million equivalent device hours.

TABLE 10
Results of High V_{cc} Dynamic Life Test

High V_{cc} Dynamic Life Test
V_{cc} = 6.0V, Temp. = 25°C, 15 MHz, 68-lead PLCC

Fab Lot	Quantity	Failures @ Hours		
		168	500	1000
19194	100	0	0	0
19618	100	1*	0	0
20454	100	0	0	0

* Icc failure. Not a ViaLink element related failure.
Failure Analysis revealed a particle under M2 causing a short

One failure, which was not associated with the ViaLink element, was observed during this test. Failure analysis on this part revealed a particle under the second metal that caused a short. This failure was due to an oxide defect and is highly accelerated by voltage stress. This device which failed at the 6.0 volt stress, may not have failed had it been subjected to the standard 5.5 volt HTOL stress.

Conclusion on Life Tests

The testing reported here establishes the reliability of the QL8X12. No failures have been observed in 31 million equivalent device hours of high temperature operating life. The observed failure rate is 0 FITs and the failure rate with a 60% confidence is 29 FITs. The acceleration factors that can lead to the degradation of the programmed and unprogrammed ViaLink elements were studied. The pASIC devices are designed to operate at voltages and currents where the failure rate of the ViaLink element does not measurably increase the failure rate of the pASIC device above that of normal CMOS products.

REFERENCES

[1] Jim Nulty, et al, *A High Reliability Metallization System for a Double Metal 1.5 μm CMOS Process*, Proc. Fifth IEEE VMIC, 1988, pp. 453-459.

[2] Dipankar Pramanik, et al, *A High Reliability Triple Metal Process for High Performance Application Specific Circuits*, Proc. Eighth IEEE VMIC, 1991, pp. 27-33.

[3] F. Yonezawa, *Fundamental Physics of Amorphous Semiconductors*, Proc of the Kyoto Summer Inst., 1981.

pASIC™ 1 FAMILY
Packaging Specifications

HIGHLIGHTS

QuickLogic offers surface mount packaging in both the standard PLCC and PQFP package types. The 100-pin Thin PQFP (TQFP) package has a nominal thickness of only 1.40 mm and is ideally suited for designs with severe height restrictions. Several hermetic packages are now in development; contact your QuickLogic sales representative for current information.

Plastic Assembly Materials

Component	PLCCs	PQFPs
Molding Compound	Epoxy Novalac	Epoxy Novalac
Lead Frame	Copper Alloy	Copper Alloy
Die Attach Area	Spot Ag	Spot Ag
Die Attach Material	Silver Filled Epoxy	Silver Filled Epoxy
Bond Wire	Au	Au
Lead Finish	Tin Lead Plate 80%/20% Sn/Pb	Tin Lead Plate 80%/20% Sn/Pb

Thermal Dissipation Data

Package (# Leads)	JC (typ)	JA
PLCC (44)	11° C/Watt	45° C/Watt
PLCC (68)	8° C/Watt	45° C/Watt
PLCC (84)	6° C/Watt	45° C/Watt
TQFP (100)	11° C/Watt	48° C/Watt

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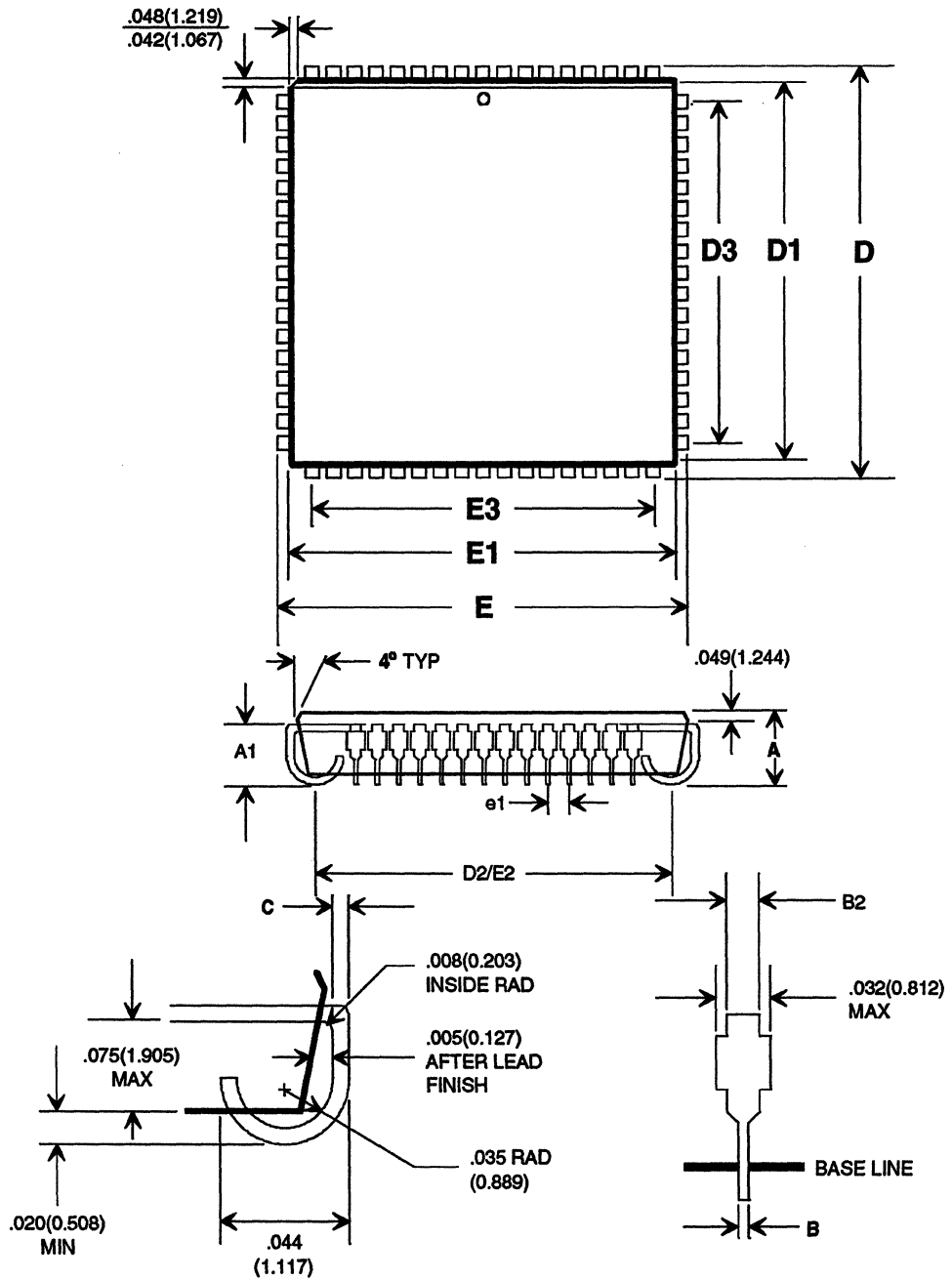
PLCC Package



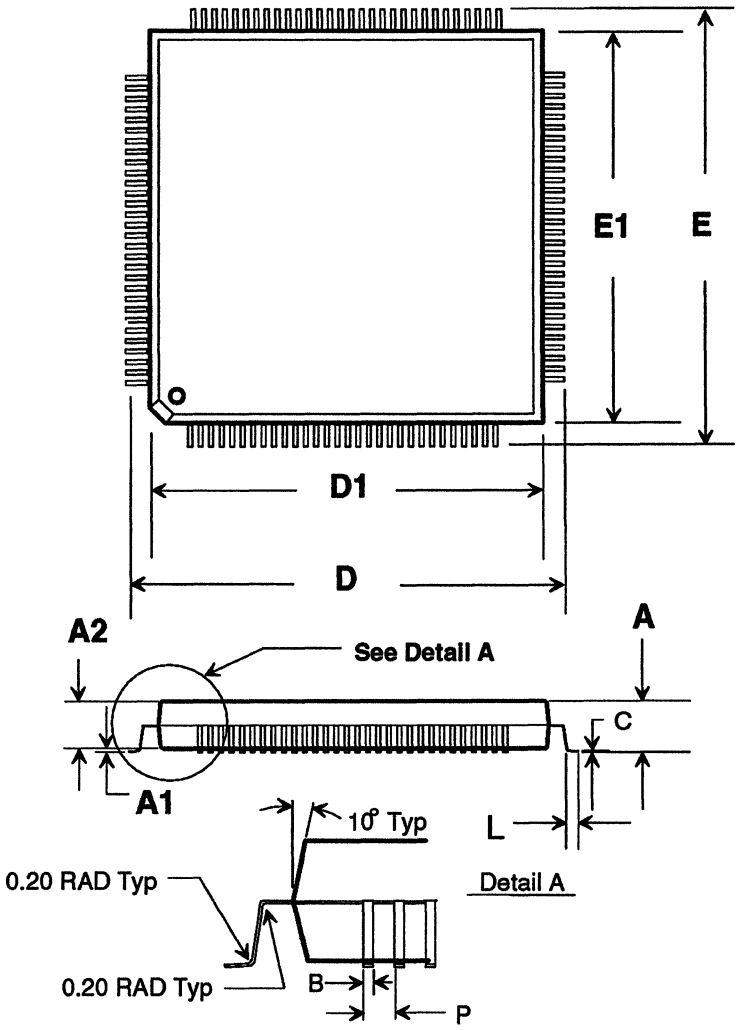
Plastic Leaded Chip Carriers

Symbol	44-Lead		68-Lead		84-Lead	
	Min	Max	Min	Max	Min	Max
A	.165 (4.19)	.180 (4.57)	.165 (4.19)	.200 (5.08)	.165 (4.19)	.200 (5.08)
A1	.090 (2.29)	.120 (3.05)	.090 (2.29)	.130 (3.30)	.090 (2.29)	.130 (3.30)
B	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)	.013 (.330)	.021 (.533)
B2	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)	.026 (.660)	.032 (.813)
C	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)	.008 (.203)	.010 (.254)
D	.685 (17.40)	.695 (17.65)	.985 (25.02)	.995 (25.27)	1.185 (30.10)	1.195 (30.35)
D1	.650 (16.51)	.656 (16.66)	.950 (24.13)	.958 (24.33)	1.150 (29.21)	1.158 (29.41)
D2	.590 (14.99)	.630 (16.00)	.890 (22.61)	.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D3 Ref only	.500 (12.70)		.800 (20.32)		1.00 (25.40)	
E	.685 (17.40)	.695 (17.65)	.985 (25.02)	.995 (25.27)	1.185 (30.10)	1.195 (30.35)
E1	.650 (16.51)	.656 (16.66)	.950 (24.13)	.958 (24.33)	1.150 (29.21)	1.158 (29.41)
E2	.590 (14.99)	.630 (16.00)	.890 (22.61)	.930 (23.62)	1.090 (27.69)	1.130 (28.70)
E3 Ref only	.500 (12.70)		.800 (20.32)		1.00 (25.40)	
e1 Typ only	.050 (1.27)		.050 (1.27)		0.50 (1.27)	
Theta JA(4) (°C/Watt)	45		45		45	

Notes:

1. All dimensions are in inches (mm).
2. Controlling dimension: inches
3. D1 and E1 do not include mold flash.
4. The Thermal Resistance, Theta JA, in °C/Watt, is for a 10,000 sq. mil die in still air with copper frame. Values are approximate.
5. Lead frame material: Copper
6. Lead finish: Matte Tin or Sn/Pb solder dip.

PQFP Package



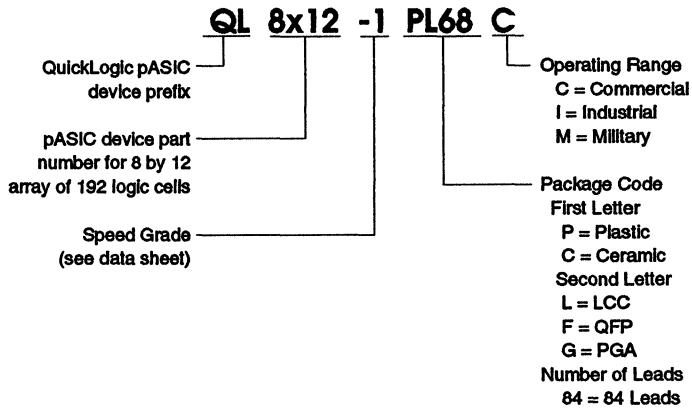
Plastic Quad Flat Package

Symbol	100-Lead		144-Lead		160-Lead	
	Min	Max	Min	Max	Min	Max
A		.063 (1.60)		.164 (4.17)		.164 (4.17)
A1	.002 (.05)	.006 (.15)	.010 (.25)	.017 (.43)	.010 (.25)	.017 (.43)
A2	.053 (1.35)	.057 (1.45)	.128 (3.24)	.147 (3.74)	.128 (3.24)	.147 (3.74)
D	.620 (15.75)	.640 (16.25)	1.22 (30.95)	1.24 (31.45)	1.22 (30.95)	1.24 (31.45)
D1	.547 (13.90)	.555 (14.10)	1.10 (27.90)	1.11 (28.10)	1.10 (27.90)	1.11 (28.10)
E	.620 (15.75)	.640 (16.25)	1.22 (30.95)	1.24 (31.45)	1.22 (30.95)	1.24 (31.45)
E1	.547 (13.90)	.555 (14.10)	1.10 (27.90)	1.11 (28.10)	1.10 (27.90)	1.11 (28.10)
B	.010 (.25 BSC)		.012 (.30 BSC)		.012 (.30 BSC)	
P	.020 (.50 BSC)		.026 (.65 BSC)		.026 (.65 BSC)	
c	.004 (.09)	.008 (.20)	.005 (.13)	.009 (.23)	.005 (.13)	.009 (.23)
L	.012 (.30)	.028 (.70)	.026 (.65)	.037 (.95)	.026 (.65)	.037 (.95)
Theta JA(4) (°C/Watt)	48		TBD		TBD	

Notes:
1. All dimensions are in inches (millimeters).
2. Controlling dimension: millimeters
3. D1 and E1 do not include mold flash.
4. The Thermal Resistance, Theta JA, in °C/Watt, is for a 10,000 sq. mil die in still air with copper frame. Values are approximate.
5. Lead frame material: Copper Alloy
6. Lead finish: Matte Tin Lead Plate or Sn/Pb solder dip.

ORDERING INFORMATION

pASIC device ordering part numbers are composed as follows:



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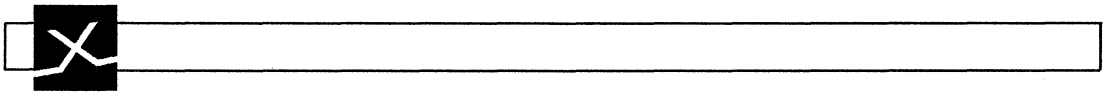

pASIC™ 1 FAMILY
Third-party Design Support

PRODUCT DESCRIPTION	VENDOR	PHONE	
	Design Entry		
PALASM, ABEL, CUPL, MINC to QDIF	Exemplar Logic	(510) 849-0937 33-140-200915	U.S. France
ECS – Engineering Capture System (schematic entry)	CAD/CAM Group	(408) 725-0204 44-(0)-483-750-149	U.S. U.K.
VIEWdraw	Viewlogic	(508) 480-0881	
	Simulation		
X-SIM pASIC Simulator	Silicon Automation Systems	(408) 437-9161	
VIEWsim	Viewlogic	(508) 480-0881	
Simulation Models	Logic Automation	(503) 690-6900	
	Place and Route		
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	Programming		
Call Factory			
	Design Services		
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FPGA Designs	Steve Golson Trilobyte Systems	(508) 369-9669	
FPGA Designs	Kash Johal ASIC Technical Solutions	(408) 943-1332	
FPGA Designs	Mike Dini FPGA Consultant	(619) 546-0229	
FPGA Designs	Chris Jay Essex Technology	(408) 226-6048	
FPGA Designs	Michael Kelley Cogent Computer Systems	(508) 624-6447	

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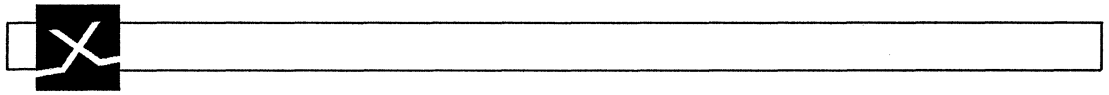

pASIC 1 FAMILY POWER CALCULATIONS

While bipolar devices draw similar amounts of current regardless of frequency, CMOS devices use power in relation to the switching frequency in addition to drawing a nominal amount of static Icc. CMOS power calculations are therefore based upon combining both static power and active power. Many of the power calculation models used for CMOS gate arrays can be applied to pASIC devices.

Static Power

The FPGA draws static current when in a quiescent state. QuickLogic FPGAs are rated at 10 mA worst case and are typically 2 mA.

Active Power

The FPGA draws active current dependent upon operating frequency. The active power calculation uses the following components:

- Macrocells
- Input Buffers
- Output Buffers
- High-Drive Buffers
- Clock Buffers

The active power can be calculated by using the guidelines in Figures 1 and 2 and Tables 1 and 2. These show the equivalent device capacitances as a function of frequency for both the QL8X12 and the QL12X16 for typical conditions.

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FIGURE 1 QL8x12 Ceq vs Operating Frequency

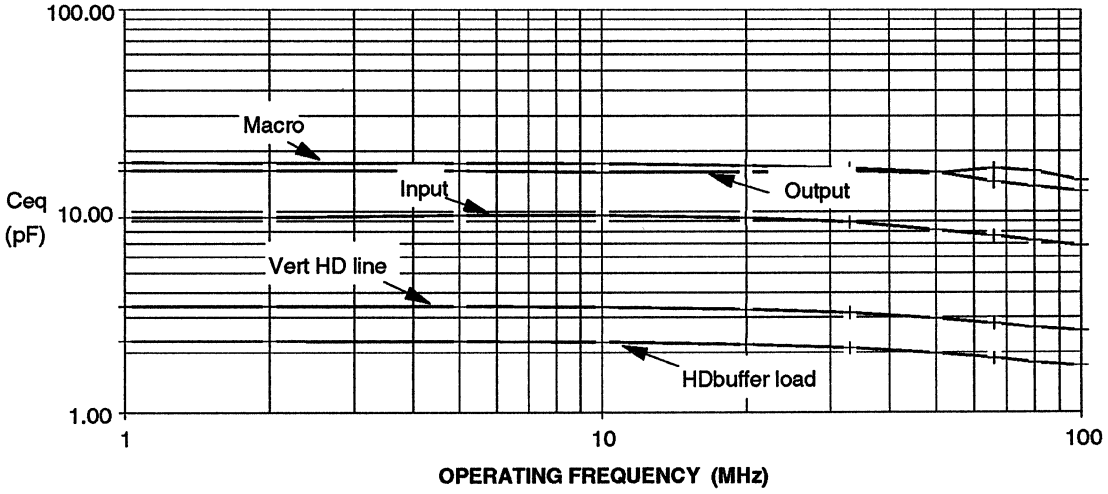


TABLE 1 QL8x12 Equivalent Capacitance

	MHz	10	20	33	50	66	80	100
Input	(pF)	9.60	9.30	8.89	8.13	7.62	7.23	6.83
Output	(pF)	15.73	15.83	16.04	15.55	16.60	16.04	14.39
Macro	(pF)	17.47	17.02	16.57	15.78	14.15	13.42	12.69
HDbuffer load	(pF)	2.25	2.19	2.10	1.98	1.87	1.77	1.71
Vert HD line	(pF)	3.38	3.29	3.16	2.97	2.80	2.66	2.57

FIGURE 2 QL12x16 Ceq vs Operating Frequency

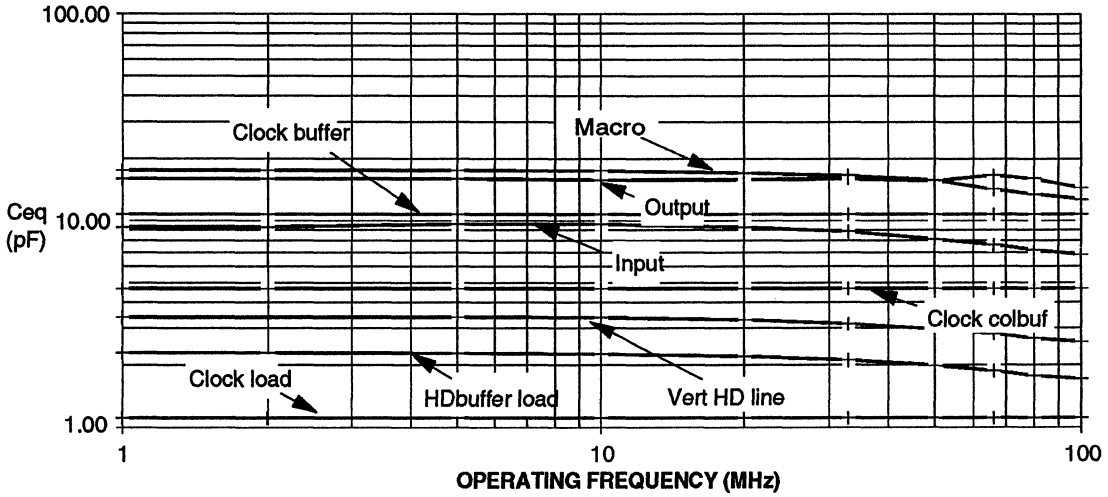


TABLE 2 QL12x16 Equivalent Capacitance

	MHz	10	20	33	50	66	80	100
Input	(pF)	9.60	9.30	8.89	8.13	7.62	7.23	6.83
Output	(pF)	15.73	15.83	16.04	15.55	16.60	16.04	14.39
Macro	(pF)	17.47	17.02	16.57	15.78	14.15	13.42	12.69
HDbuffer load	(pF)	2.25	2.19	2.10	1.98	1.87	1.77	1.71
Vert HD line	(pF)	3.38	3.29	3.16	2.97	2.80	2.66	2.57
Clock buffer	(pF)	10.75	10.75	10.75	10.75	10.75	10.75	10.75
Clock colbuf	(pF)	4.67	4.67	4.67	4.67	4.67	4.67	4.67
Clock load	(pF)	1.11	1.11	1.11	1.11	1.11	1.11	1.11

The equation for the power calculation for each individual component is:

$$P_{comp(mW)} = (\#Components)*(C_{equiv})*(F_{ave})*(V_{cc})^2*(1000)$$

The "#Components" is the number of components being used; "C_{equiv}" is the equivalent capacitance from Figure 1; "F_{ave}" is the average frequency of the components and "V_{cc}" is the operating voltage of the device.

The complexity in calculating power for CMOS arrays is in determining the average frequency of individual components in the system. For an example we use a 16-bit counter with 16 macrocells/outputs; Q0-Q15. All of these macrocells toggle at different frequencies and will draw different amounts of power. The frequency of each bit is as follows:

- Q0 will toggle at F/2 where F is the incoming clock frequency.
- Q1 will toggle at F/4
- Q2 will toggle at F/8
- .
- .
- Q15 will toggle at F/(65536)

With x representing the number of bits in the counter, this relationship can be simplified down to an average frequency for each individual flip flop:

$$F_{ave} = 1/16 \sum_{n=1}^{n=x} (1/2)^n \cong F/16$$

Example Using the Power Calculation

Our 16-bit counter is implemented in a QL8X12 and uses 16 macrocells. 16 outputs, and a high-drive clock pad that drives 4 vertical express columns. The incoming clock frequency is 33 MHz operating at 5 volts. We determine total device power by calculating the power of the individual components.

Macrocells

From Figure 1 or Table 1 we locate Cequiv for an individual macrocell. In this case C_{equiv} is 16 pf/MHz-Macrocells.

$$P_{macro(mW)} = (16)*(16)*(33/16)*(5)^2*(10^{-3}) = 13.20 \text{ mW}$$

Input Buffers

From Figure 1 or Table 1 we use C_{equiv} for an individual input running at 33 MHz or 8.9 pf/MHz-Input.

$$P_{inputs(mW)}=(1)*(8.9)*(33)*(5)^2*(10^{-3})=7.34 \text{ mW}$$

Output Buffers

The C_{equiv} for an individual output buffer is 16 pf/MHz-Output. Because the outputs of the device are the same as the outputs of the counter, we use F/16 for our average frequency of the outputs. Inserting the numbers we calculate:

$$P_{outputs(mW)}=(16)*(16)(33/16)*(5)^2*(10^{-3})=13.2 \text{ mW}$$

High-Drive Buffers

Calculations for the power for High-Drive Buffers and Clock Buffers are divided into two components consisting of (1) the number of columns and (2) the number of loads the High Drive/Clock Buffer drives. The appropriate equation is:

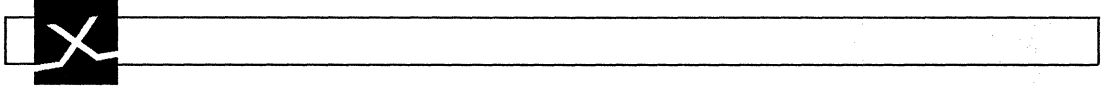
$$P_{HighDrive(mW)}=[(\#Columns)(C_{equivcol})+(\#Loads)(C_{equivloads})]*(Vcc)^2*(F)*(10^{-3})$$

$$P_{High\ Drive(mW)}=[(4)(3.16)+(16)(2.10)](5)^2(33)(1000)=38.15 \text{ mW}$$

Total Device Power

By adding both the static and active power components we determine that the typical total device power equals the following:

$$P_{sys}=(13.20mW)+(7.34mW)+(13.20mW)+(38.15mW)+(50mW)=121.89 \text{ mW}$$



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CMS Marketing
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(215) 834-6840
FAX: (215) 834-6848

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International Representatives/ Distributors

ENGLAND

Abacus Electronics Holdings Ltd
Abacus House, Bone Lane
Newbury Berks, RG14 5SF England
Telephone: 44-(0) 635 515701
FAX: 44-(0) 635 38670

FRANCE

SCIENTECH

Bordeaux
Zi du Phare – 16
ru Francois Arago
33700 Merignac
Telephone: 33-56 34 03 07
FAX: 33-56 47 74 73

Rennes
Techno Parc – 4
4 Avenue Des Peupliers – Bat E
35510 Cesson Sevigne
Telephone: 33-99 83 98 98
FAX: 33-99 83 48 04

Saint Etienne
Le Chatelet – 5
Place Carnot
42000 Saint-Etienne
Telephone: 33-77 79 79 70
FAX: 33-77 74 10 03

Toulouse
Minipark – BP232
Innopole Voie No 2
31677 Labege Cedex
Telephone: 33-61 39 19 77
FAX: 33-61 39 04 85

GERMANY

Scantec Mikroelektronik GmbH

Behringstrasse 10
8033 Planegg West Germany
Telephone: 49-89 859 80 21
FAX: 49-89 857 65 74

Tannenbergstrasse 103
7312 Kircheim/Teck West Germany
Telephone: 49-70 21 830 94

Topas electronic GmbH
Striehlstrasse 18
3000 Hannover 1, West Germany
49-5 11 13 12 17
FAX: 49-5 11 13 12 16

Max Weber Str. 16
2085 Quickborn
Telephone: 49-4106-73097
FAX: 49-4106-73378

ITALY

Claitron

Claitron S.p.A
Via Gallarate 211
20151 Milano – Italy
Telephone: 39 2 33404000
FAX: 39 2 38001414

Claitron Torino
Corso Francia 220
10093 Collegno (To) – Italy
Telephone: 39 11 4054100
FAX: 39 11 4053018

Claitron Padova
Via Nicolo' Tommaseo 15
35131 Padova – Italy
Telephone: 39 49 665636
FAX: 39 49 663558

Claitron Bologna
Via E. Collamarini 22
40138 Bologna – Italy
Telephone: 39 51 534883
FAX: 39 51 531217

Claitron Firenze
Via Masaccio 175
50132 Firenze – Italy
Telephone: 39 55 5001923
FAX: 39 55 5001921

Claitron Roma
Piazza Carduti della Montagnola 50
00142 Roma – Italy
Telephone: 39 6 5413279
FAX: 39 6 5402876

JAPAN

Nippon QuickLogic k.k.
2-34-16 Yoga
Setagaya-ku, Tokyo 158
Telephone: 03-5716-5930
FAX: 03-5716-5931