512K x 8 Bit Static Random Access Memory

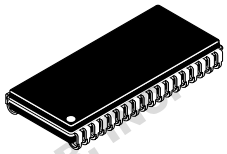
MCM6946
SCM6946

The MCM6946/SCM6946 is a 4,194,304–bit static random access memory organized as 524,288 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

The MCM6946/SCM6946 is equipped with chip enable ($\overline{E}$) and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Either input, when high, will force the outputs into high impedance.

The MCM6946 is available in a 400 mil, 36–lead surface–mount SOJ package.

- Single 3.3 V – 5%, + 10% Power Supply
- Fast Access Time: 8/10/12/15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Three–State Outputs
- Power Operation: 195/185/180/175 mA Maximum, Active AC
- Available in TSOP or SOJ Packages



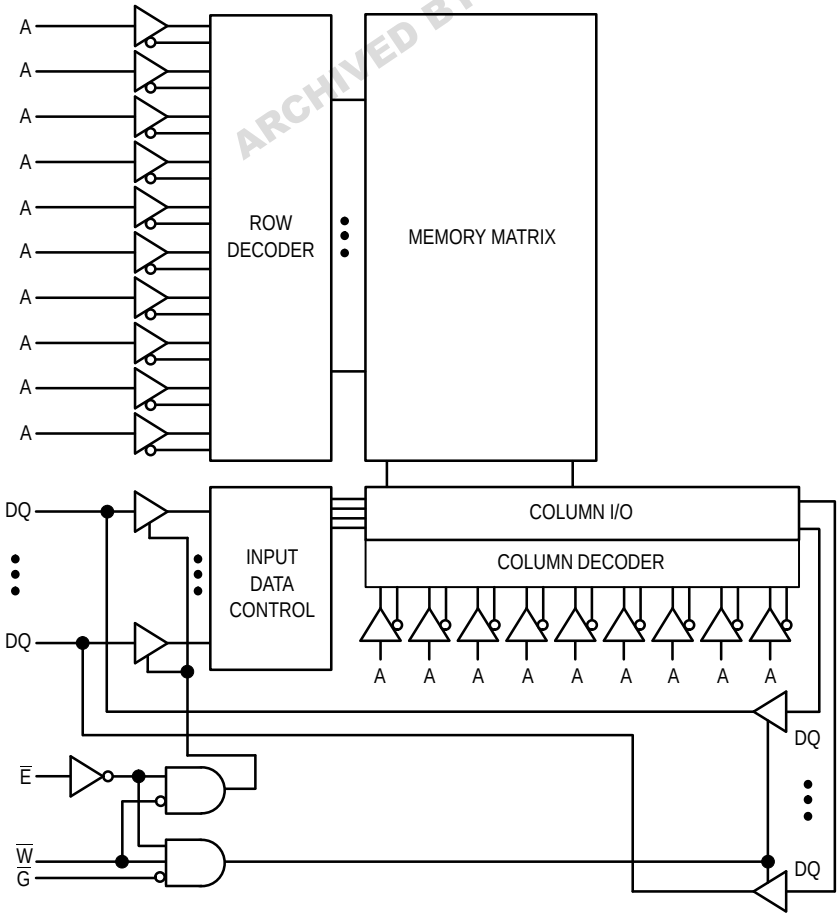
YJ PACKAGE
400 MIL SOJ
CASE 893–02

TS PACKAGE
44–LEAD
TSOP TYPE II
CASE 924A–02

PIN NAMES

A0 – A18	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
DQ	Data Input/Output
NC	No Connection
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



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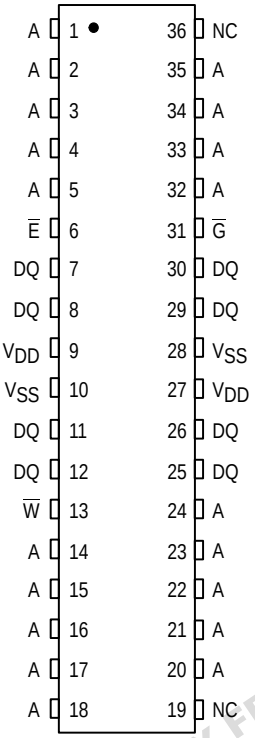
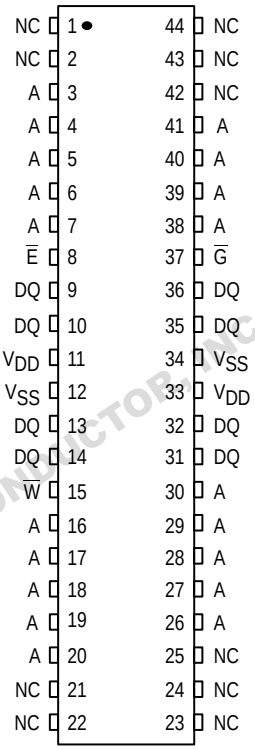
PIN ASSIGNMENTS

400 MIL SOJ



TSOP TYPE II



TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	I/O Pin	Cycle	Current
H	X	X	Not Selected	High–Z	—	I_{SB1}, I_{SB2}
L	H	H	Output Disabled	High–Z	—	I_{DDA}
L	L	H	Read	D_{out}	Read	I_{DDA}
L	X	L	Write	High–Z	Write	I_{DDA}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage Relative to V_{SS}	V_{DD}	– 0.5 to 5.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{DD}	V_{in}, V_{out}	– 0.5 to V_{DD} + 0.5	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{bias}	– 10 to 85	°C
Operating Temperature	T_A	0 to 70	°C
Storage Temperature — Plastic	T_{stg}	– 55 to 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V – 5%, + 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

*V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 2.0 ns).
**V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 2.0 ns).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})	$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter		Symbol	0 to 70°C	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{DD} = Max)	SCM6946–8: t_{AVAV} = 8 ns MCM6946–10: t_{AVAV} = 10 ns MCM6946–12: t_{AVAV} = 12 ns MCM6946–15: t_{AVAV} = 15 ns	I_{DD}	195 185 180 175	mA
AC Standby Current (V_{DD} = Max, $\overline{E}$ = V_{IH}, No Other Restrictions on Other Inputs)	SCM6946–8: t_{AVAV} = 8 ns MCM6946–10: t_{AVAV} = 10 ns MCM6946–12: t_{AVAV} = 12 ns MCM6946–15: t_{AVAV} = 15 ns	I_{SB1}	55 50 50 45	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{DD} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{DD} – 0.2 V) (V_{DD} = Max, f = 0 MHz)		I_{SB2}	20	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.3 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except Clocks and DQs $\overline{E}$, $\overline{G}$, $\overline{W}$	C_{in} C_{ck}	4 5	6 8	pF
Input/Output Capacitance	DQ	$C_{I/O}$	5	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

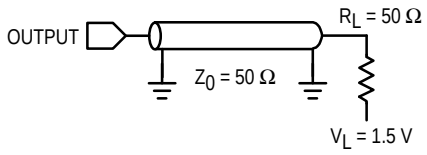
(V_{DD} = 3.3 V – 5%, + 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns
Input Timing Measurement Reference Level . . . . . 1.5 V
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	SCM6946–8		MCM6946–10		MCM6946–12		MCM6946–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	4
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	2	—	2	—	2	—	2	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	5, 6, 7
Enable High to Output High–Z	t_{EHQZ}	0	4	0	5	0	6	0	7	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	4	0	5	0	6	0	7	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. All read cycle timings are referenced from the last valid address to the first transitioning address.
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured ± 200 mV from steady–state voltage.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E} \le V_{IL}$, $\overline{G} \le V_{IL}$).

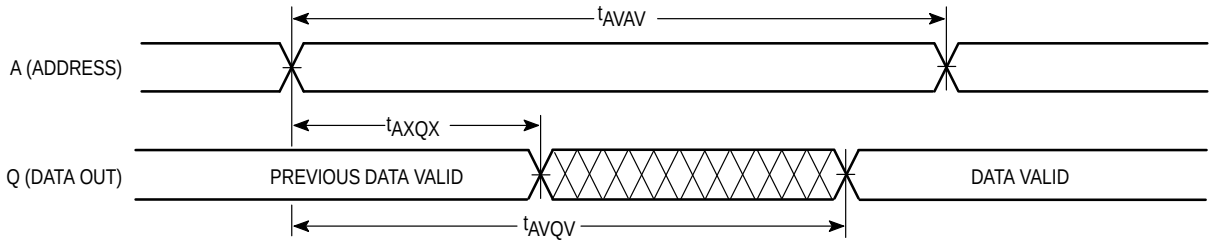


TIMING LIMITS

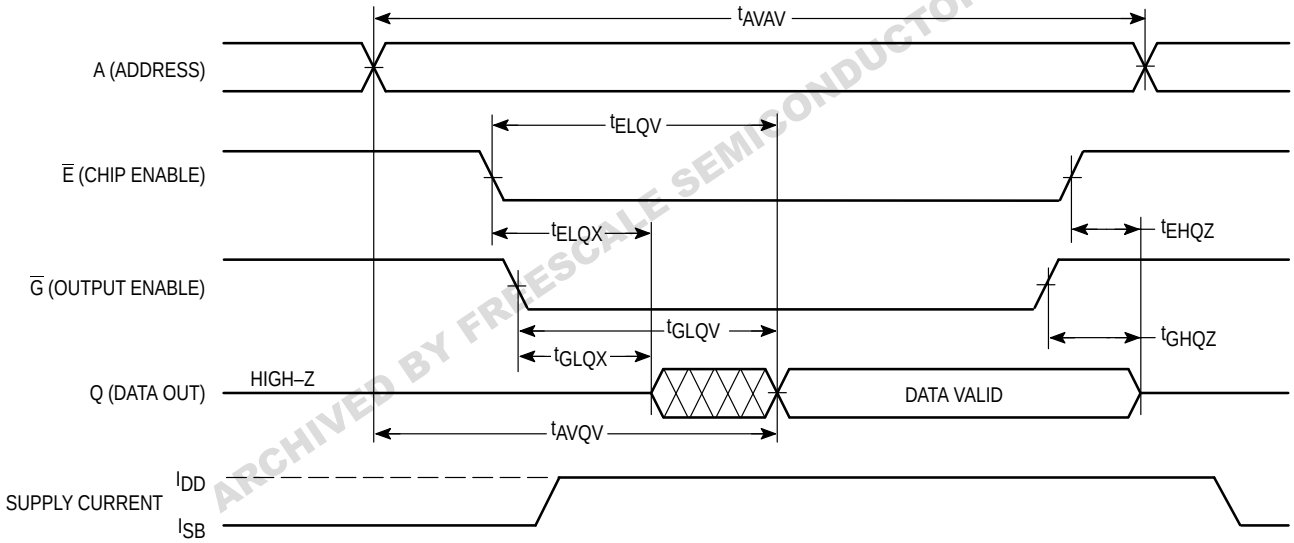
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

Figure 1. AC Test Load

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 4)

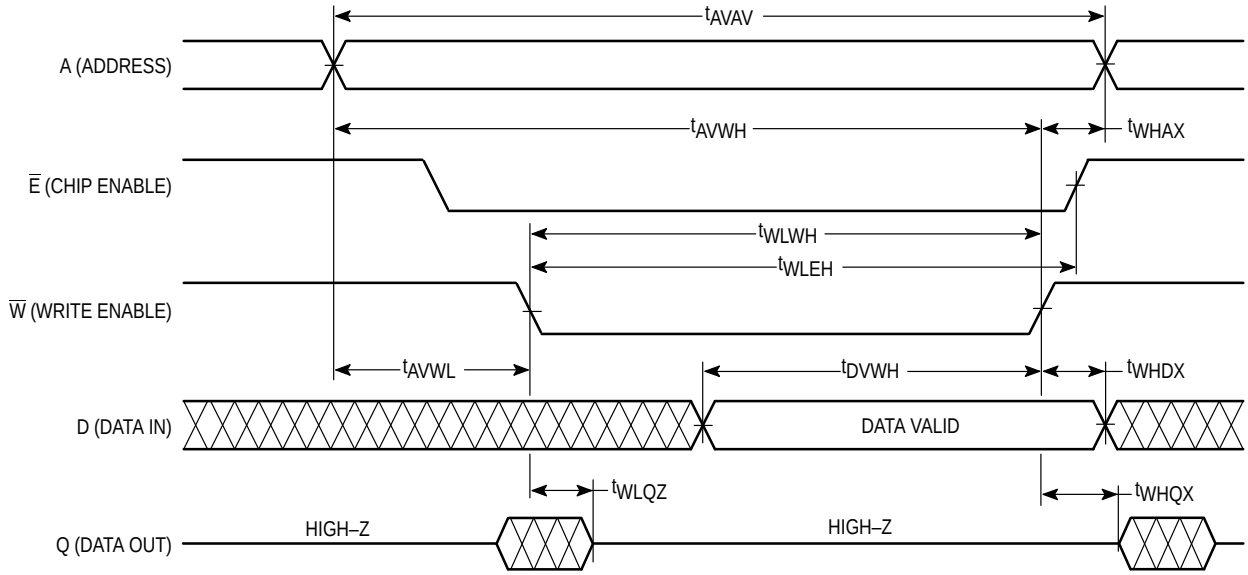


WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	SCM6946–8		MCM6946–10		MCM6946–12		MCM6946–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVWL}	0.5	—	0.5	—	0.5	—	0.5	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width ($\overline{G}$ High)	t_{WLWH} t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	6	—	6	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	0	7	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured ± 200 mV from steady–state voltage.
6. This parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min, both for a given device and from device to device.

WRITE CYCLE 1 ($\overline{W}$ Controlled; See Notes 1, 2, and 3)

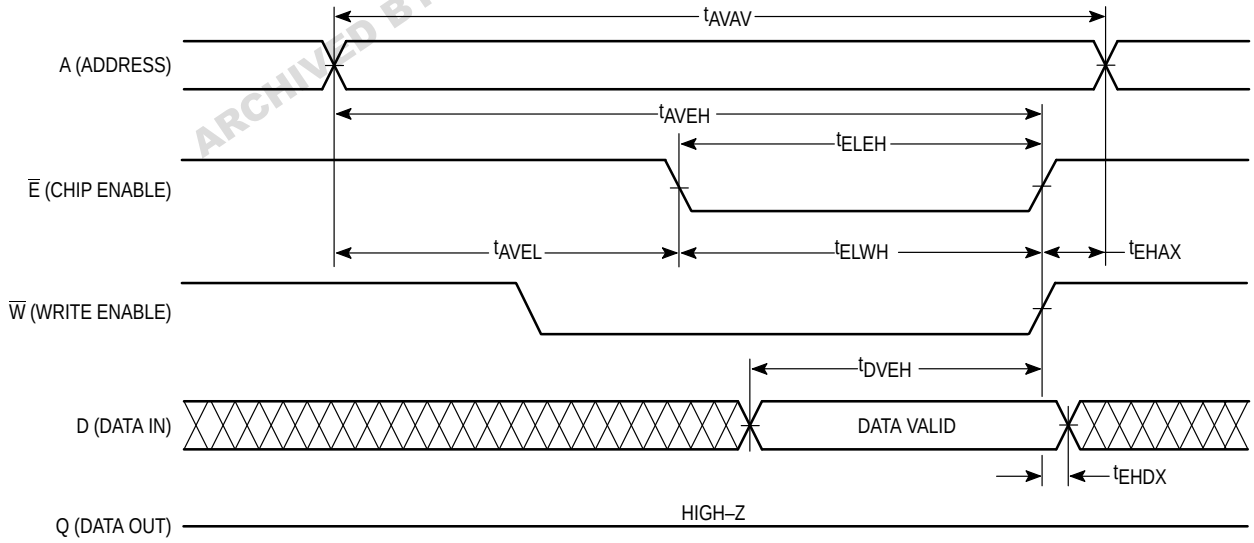


WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)

Parameter	Symbol	SCM6946–8		MCM6946–10		MCM6946–12		MCM6946–15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write ($\overline{G}$ High)	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable Pulse Width	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	12	—	ns	5, 6
Enable Pulse Width ($\overline{G}$ High)	t_{ELEH}, t_{ELWH}	7	—	8	—	9	—	10	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	6	—	6	—	6	—	7	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivities to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance state.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high–impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high–impedance condition.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1, 2, and 3)



ORDERING INFORMATION
(Order by Full Part Number)

XCM 6946 XX XX XX

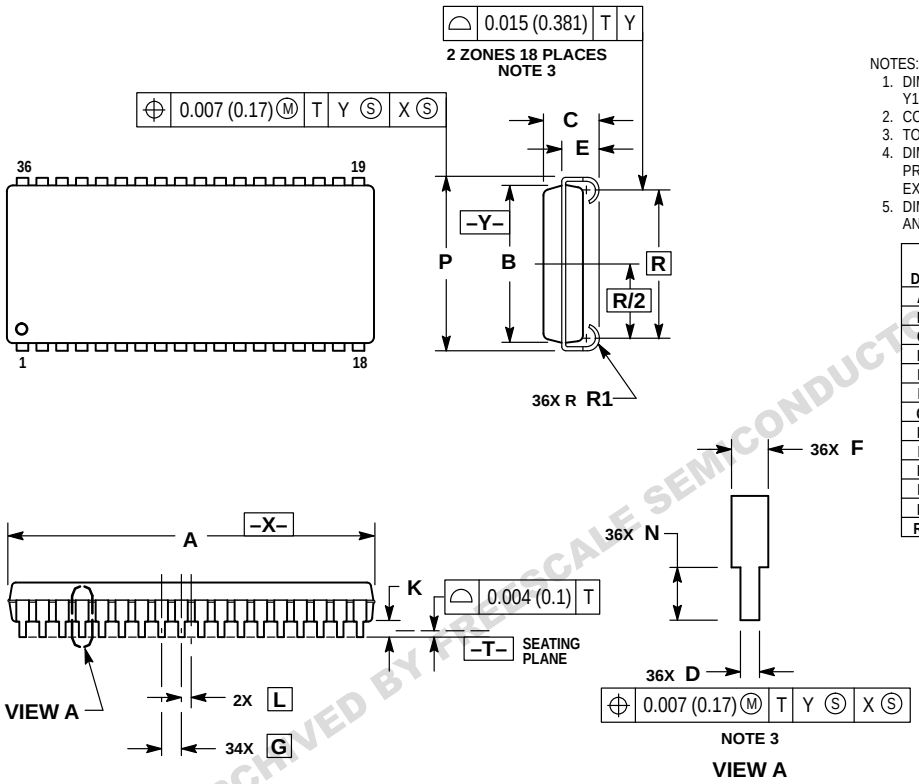
- XCM: Motorola Memory Prefix
- 6946: Part Number
- XX: Package (YJ = 400 mil SOJ, TS = 44–Lead TSOP Type II)
- XX: Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
- XX: Shipping Method (R = Tape and Reel, Blank = Rails)

Full Commercial Part Numbers —

SCM6946YJ8	MCM6946YJ10	MCM6946YJ12	MCM6946YJ15
SCM6946TS8	MCM6946YJ10R	MCM6946YJ12R	MCM6946YJ15R
	MCM6946TS10	MCM6946TS12	MCM6946TS15
	MCM6946TS10R	MCM6946TS12R	MCM6946TS15R

PACKAGE DIMENSIONS

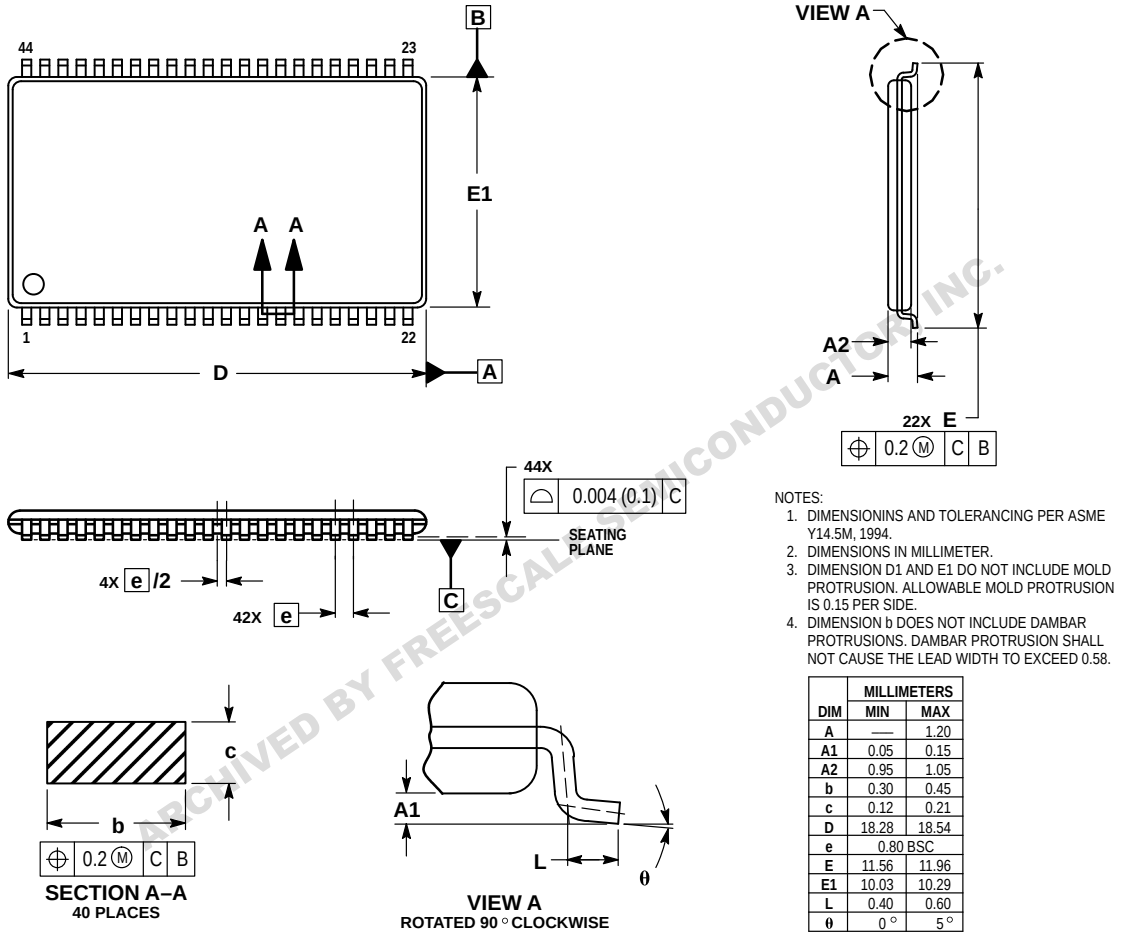
YJ PACKAGE
400 MIL SOJ
CASE 893–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE –T–.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.15) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.920	0.930	23.37	23.62
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.25	3.76
D	0.015	0.020	0.38	0.51
E	0.082	—	2.08	—
F	0.026	0.032	0.66	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.55	0.90	1.40
L	0.025 BSC		0.64 BSC	
N	0.035	0.045	0.90	1.14
P	0.435	0.445	11.05	11.30
R	0.370 BSC		9.40 BSC	
R1	0.030	0.040	0.76	1.02

TS PACKAGE
44–LEAD
TSOP TYPE II
CASE 924A–02



NOTES:
1. DIMENSIONINS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.58.

	MILLIMETERS	
DIM	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.30	0.45
c	0.12	0.21
D	18.28	18.54
e	0.80 BSC	
E	11.56	11.96
E1	10.03	10.29
L	0.40	0.60
θ	0 °	5 °

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