PUNCHED CARD EQUIPMENT TRAINING MANUAL

FIRST EDITION

FOR TRAINING PURPOSES ONLY

This manual was compiled and written by members of the instructional staff of

CONTROL DATA INSTITUTE
CONTROL DATA CORPORATION

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FOREWORD

The Punched Card Equipment Training Manual provides information on punched card technology and equipments found in modern computer systems. The equipments considered in this manual, though products of Control Data Corporation, are representative of those used in the computer industry.

This manual contains five discrete subjects. Chapter I provides information fundamental to punched cards. Chapter II explains the CONTROL DATA 405 Card Reader. Chapter III contains information concerning the CONTROL DATA 3248 Card Reader Controller. Chapter IV explains the CONTROL DATA 415 Card Punch. Chapter V provides information regarding the CONTROL DATA 3245 Card Punch Controller.

To aid the reader, study questions are located at the end of each chapter and should be completed before continuing to subsequent chapters. Answers to the questions are located in Appendix A.

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CHAPTER I

STANDARD DATA CARDS

CHAPTER I

STANDARD DATA CARDS

INTRODUCTION

The use of punch cards for storing data or information goes back to the early 19th century. In New England a form of the punched card was used in the textile industry to control the weaving looms to weave different patterns in the material from cotton and wool fibers. Later in the 19th century men of advance education began experimenting with forms of mechanical machines that could add and subtract numbers, but the rate of entering data into the machines was very slow until Hollerith devised a coding system. This Hollerith system allowed data to be punched on cards to provide a higher entry rate of information into these types of machines. The data card as we know today was standardized by IBM, since they were essentially the first company to enter the computer field.

The standard data card is used in computer systems as a means of inputting data for programs or storing information outputted by the computer after the computations are completed. The computer interprets the information as a logical one or zero and processes it accordingly.

The standard data card is 7.3 inches in length and 3.25 inches in width and contains 80 columns of information. Each column contains 12 bits of information with one or more columns making up a computer word. As the card is fed through the card reader, each column of data is tranferred to the computer. The computer will use the information as the computer program directs.

Data stored on the card is indicated by the presence or absence of punched holes in each column on the card. The holes punched in each column can be in the format of several coding systems such as Hollerith, Binary, and Binary Coded Decimal. These coding systems allow a variety of data to be used in computer systems for varied applications.

The Binary coding system can represent numbers (based on the powers of 2) in numerical applications or it can represent the contents of a card memory "dumped" on punched cards. Cards using the binary format will contain a 12 bit word in each column on the card and each card will be identified by a 7 and 9 punch in column 1.

The Hollerith system is considered to be the standard coding system for the computer industry. The Hollerith coding system has a wide application, since it represents alphanumeric characters and punctuation marks. Cards using the Hollerith format will contain a 12-bit word (representing a character) in each column on the card and each card will be identified by not having a "7 and 9" punch in column 1.

It should be pointed out that Control Data computer systems have logic components wired to recognize the identification codes used in column 1 of each card and will process it accordingly. Binary data will be transferred directly to the computer. Hollerith data must first be converted to another coding format called Binary Coded Decimal before it can be transferred to the computer.

The Binary Coded Decimal (BCD) system was devised by IBM to replace the Hollerith system for use of data transfer on higher speed computer systems. The BCD system is equivalent to the Hollerith system except it uses a 6 bit word per character instead of a 12 bit word and it has no identification code in Column 1. Cards using the BCD format are used with a computer instruction called "Negate Translation" to transfer the data directly to the computer.

Regardless of the type of coding system used data cards are grouped together to make a program deck. Each card is considered to be a record of information. Records of information are combined to make a file of information, called the program deck, which can be divided in control cards, data cards, and an End of File card. The control cards contain the computer instructions which will be used to execute the program. The data cards contain the information to be processed. The End of File card, identified by a 7 and 8 punch in column 1, indicates the last card of the program deck is present and can be used to transfer program control elsewhere in memory.

Standard data cards have a limited, usable life, but this can be extended by proper care of the cards when not being used. Cards are normally stored at room temperature in a humidity range of 35% - 65%. Excessive temperature or humidity changes should be avoided, since it can cause the cards to warp or increase in size. These changes can also cause incorrect feeding of cards through card readers or punches.

Data cards provide an inexpensive means of storing information for computer programs, allow easy revision of programs when being updated or debugged, and can be used repeatedly to input information into the computer.

PUNCHED CARDS

HANDLING

Punched cards may be adversely affected by extreme climate changes or by careless handling. However a few precautions in storage and handling will assure that the cards always give top performance.

ENVIRONMENT

Relative humidity affects the size and weight of punched cards. As humidity rises the card stock absorbs moisture and tends to expand, causing warpage if cards are not tightly clamped in their containers. As humidity falls the card stock loses moisture and shrinks, causing card buckling. The recommended relative humidity in the equipment and storage areas should be stable and within the range of 35% - 65%. The lower humidity is preferred. When the relative humidity is under 35% or over 65% for a long time, permanent warp may develop.

Temperature changes also affect punched cards. When cards are moved from a cold area to a warm area, moisture condenses on them and temporary warping occurs.

CORRECTING WARP DUE TO HUMIDITY

Cards warped by exposure to abrupt changes in humidity usually regain their shape when they achieve equilibrium with the room humidity. If 30% relative humidity differential exists between storage room and machine room, the acclimatization period should be two to three weeks. If the differential is 20%, the period is from 1 to 1½ weeks. A differential of 10% or less normally does not require a waiting period. If storage facilities are available in the machine room, it is good practice to process all incoming cards for a week.

HANDLING

Keep cards in their original containers until they are used. When the quantity of card permits, stack the boxes so that the cards lie flat. Pressure block cards in partially filled boxes and do not stack these boxes. Also pressure block cards when they are in a card tray.

If the cards appear curved, carefully flex them back and forth a few times. Prior to feeding cards into the 405 align them with a joggle plate. If static electricity makes joggle plate alignment difficult, fan the cards after each card pass. Newly punched cards or cards that have been stored for a long time (1 year or more) should be thoroughly fanned before feeding.

CORRECTING WARP DUE TO INPROPER HANDLING OR STORAGE

Warping caused by stacking half-filled boxes of cards, by storing cards under very humid conditions, etc., is more serious than that due to changes in climate. Such warping is recognizable by the uneven nature of the card warp.

If the warp is not severe or of long duration, it may be corrected by storing the cards under pressure at a constant humidity. The relative humidity in the area should be from 35% - 65%.

Card dust should be removed from newly punched cards by fanning the deck before reading.

EXPLANATION OF HOLLERITH AND BCD FORMATS

HOLLERITH

The Hollerith System is a numeric code by which data can be stored on a punched card. There are 12 Rows on a punch card. Rows 1 to 9 are called the numeric portion of the card and are used in an incrementing manner. Rows 12, 11, and 0 are called the zone portion of the card. Identical punches in rows 1 to 9 can have the meaning changed by selecting a different zone.

Alpha characters can be represented by utilizing different combinations of zones and numerics as can special characters such as the comma, slash, cent, etc.

Alpha characters A to I are represented by selecting Row 12 and incrementing Rows 1-9.

Example: A = Rows 12 and 1 punched
B = Rows 12 and 2 punched
Etc. to
I = Rows 12 and 9 punched

Alpha characters J to R are represented by selecting Row 11 and incrementing Rows 1-9.

Example: J = Rows 11 and 1 punched
K = Rows 11 and 2 punched
Etc. to
R = Rows 11 and 9 punched

Alpha characters S to Z are represented by selecting Row 0 and incrementing Rows 2-9.

Example: S = Rows 0 and 2 punched
T = Rows 0 and 3 punched
Etc. to
Z = Rows 0 and 9 punched

Numerals are represented by punching Rows 0 to 9 without using a zone.

Example: 0 = Row 0 punched
1 = Row 1 punched
Etc. to
9 = Row 9 punched

Except for the slash (/) which is represented by a Row 0 and 1 punch, the rest of the special characters are represented by a combination of one zone and two numeric punches.

EXTERNAL BCD

Since the Hollerith System is only compatible with punched card equipment, it must be converted to a code which will be compatible with other input/output equipment as well as computers. This code is called BCD (Binary-Coded Decimal) and is in a 6-bit format with bit position "0" the least significant and bit position "B" the most significant. Following is the format for a BCD word:

B A 8 4 2 1

The "1" is bit position "0", the "2" is bit position "1", etc. on through the "B" being bit position "5". Bits 0 to 3 are assigned binary values of 2^0 at bit position "0", 2^1 at bit position "1", 2^2 at bit position "2" and 2^3 at bit position "3". Bit position "4" is labeled "A" and bit position "5" is labeled "B". Bit positions 0 to 3 represent the numeric portion of the punched card and bit positions "A" and "B" represent the zone portion of the card.
A punch in zone 12 of the card will be represented by "1" bits in both the A and B positions of the BCD word.
A punch in zone 11 of the card will be represented by a "1" bit only in the "B" position of the BCD word.
A punch in zone 0 of the card will be represented by a "1" bit only in the "A" position of the BCD word.

Numerals do not have bits in the zones. A value of one has a "1" bit in position "0" of the BCD word. Two = position "1", three = positions 0 and 1, four = position 2, five = positions 0 and 2, six = positions 1 and 2, seven = positions 0, 1, and 2 , eight = position 3, and nine = positions 0 and 3.

Example: B A 8 4 2 1

0 0 0 0 0 1 = 1
0 0 0 0 1 0 = 2
0 0 0 0 1 1 = 3
0 0 0 1 0 0 = 4
Etc. to 0 0 1 0 0 1 = 9

Alpha characters A to I, which are zone 12 characters, will have "1" bits present in the B and A positions of the BCD word and will increment bit positions 0 to 3.

Example: B A 8 4 2 1

1 1 0 0 0 1 = A = 12,1 punch = 61_8
1 1 0 0 1 0 = B = 12,2 punch = 62_8
Etc. to 1 1 1 0 0 1 = I = 12,9 punch = 71_8

Alpha characters J to R, which are zone 11 characters, will have "1" bits present in the B position of the BCD word and will increment bit positions 0 to 3.

Example: B A 8 4 2 1

1 0 0 0 0 1 = J = 11,1 punch = 41_8
1 0 0 0 1 0 = K = 11,2 punch = 42_8
Etc. to 1 0 1 0 0 1 = R = 11,9 punch = 51_8

Alpha characters S to Z, which are zone 0 characters, will have "1" bits present in the A position of the BCD word and will increment bit positions 0 to 3.

Example: B A 8 4 2 1

0 1 0 0 1 0 = S = 0,2 punch = 22_8
0 1 0 0 1 1 = T = 0,3 punch = 23_8
Etc. to 0 1 1 0 0 1 = Z = 0,9 punch = 31_8

INTERNAL BCD

Analyzing the above BCD codes the following is found to be true:

1. Numerals are represented by a straight Decimal to Binary conversion
2. Letters A through I are equivalent to 61_8 to 71_8
3. Letters J through R are equivalent to 41_8 to 51_8
4. Letters S through Z are equivalent to 22_8 to 31_8

These alpha codes make sorting operations difficult within computer systems. For this reason, another coding system, called Internal BCD, was developed and is used by some computer systems including Control Data.

The character codes were re-arranged so the numerical progression would coincide with the alpha character progression. J through R codes remained unchanged while the other two groups were reversed. The numeric value for A through I, then, went below 41 to 51 and the numeric value for S through Z went above 41 to 51. It was found that this reversal could be accomplished by complementing the upper most bit (bit 5) of groups A to I and S to Z. However, this complement must not affect the 41 to 51 codes. Upon close examination of the codes, it was found that bit position 4 is only present (a "1") in groups A to I and S to Z. From this resulted the rule for converting from Internal BCD to External BCD or vice-versa:

"When bit 4 is a "1" complement bit 5; when bit 4 is a "0" leave bit 5 alone".

Thus, the resultant Internal BCD Codes are:

1. A to I = 21 to 31
2. J to R = 41 to 51
3. S to Z = 62 to 71

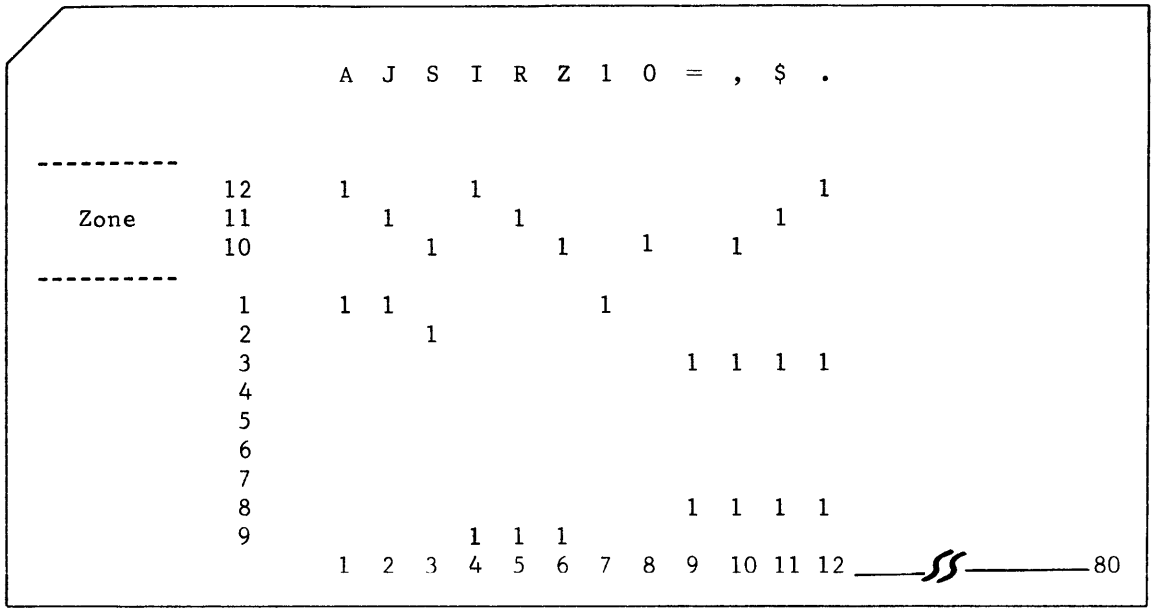
TABLE OF CODES

CHARACTER	HOLLERITH CODE	EXTERNAL CODE	INTERNAL CODE	CHARACTER	HOLLERITH CODE	EXTERNAL CODE	INTERNAL CODE
0	0	12	00	-	11	40	40
1	1	01	01	J	11,1	41	41
2	2	02	02	K	11,2	42	42
3	3	03	03	L	11,3	43	43
4	4	04	04	M	11,4	44	44
5	5	05	05	N	11,5	45	45
6	6	06	06	O	11,6	46	46
7	7	07	07	P	11,7	47	47
8	8	10	10	Q	11,8	50	50
9	9	11	11	R	11,9	51	51
=	8,3	13	13	%	11,0	52	52
≠	8,4	14	14	$	11,3,8	53	53
≤	8,5	15	15	*	11,4,8	54	54
¬	8,6	16	16	↑	11,5,8	55	55
[	8,7	17	17	↓	11,6,8	56	56
blank	unpunched	20	60	>	11,7,8	57	57
/	0,1	21	61	+	12	60	20
S	0,2	22	62	A	12,1	61	21
T	0,3	23	63	B	12,2	62	22
U	0,4	24	64	C	12,3	63	23
V	0,5	25	65	D	12,4	64	24
W	0,6	26	66	E	12,5	65	25
X	0,7	27	67	F	12,6	66	26
Y	0,8	30	70	G	12,7	67	27
Z	0,9	31	71	H	12,8	70	30
]	0,2,8	32	72	I	12,9	71	31
,	0,3,8	33	73	<	12,0	72	32
(	0,4,8	34	74	.	12,3,8	73	33
→	0,5,8	35	75	)	12,4,8	74	34
≡	0,6,8	36	76	≥	12,5,8	75	35
≈	0,7,8	37	77	?	12,6,8	76	36
:	illegal	00	12	;	12,7,8	77	37

HOLLERITH TO BCD CONVERSION ON PUNCHED CARDS

Hollerith codes are made from a combination of "1"s and "0"s in one column on a card (12 bits). BCD codes consist of 6 bits allowing two codes to be put into each column. On the following pages are three cards; a Hollerith, card, an External BCD card and an Internal BCD card.

HOLLERITH CARD

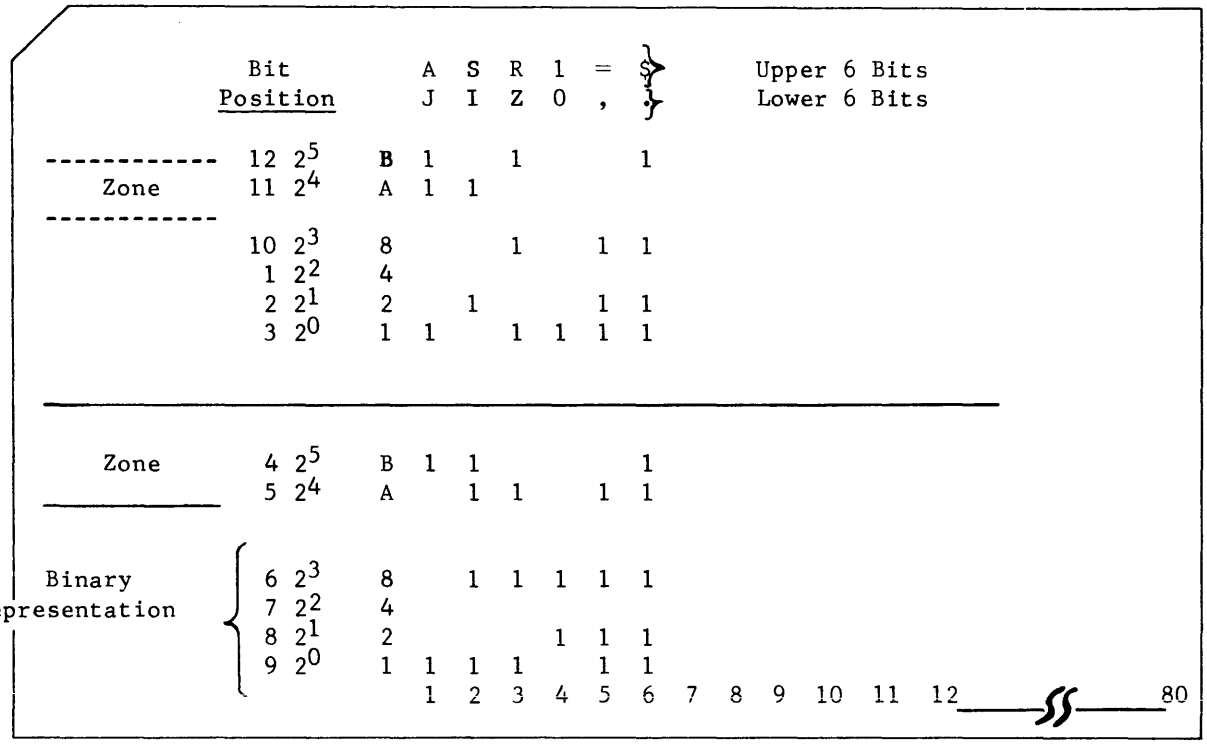


In a column a hole punched in row

12 signifies characters A-I
11 signifies characters J-R
10 signifies characters S-Z

An A =	punch in 12	and a punch in 1
J =	11	1
S =	10	2
I =	12	9
R =	11	9
Z =	10	9

EXTERNAL BCD CARD

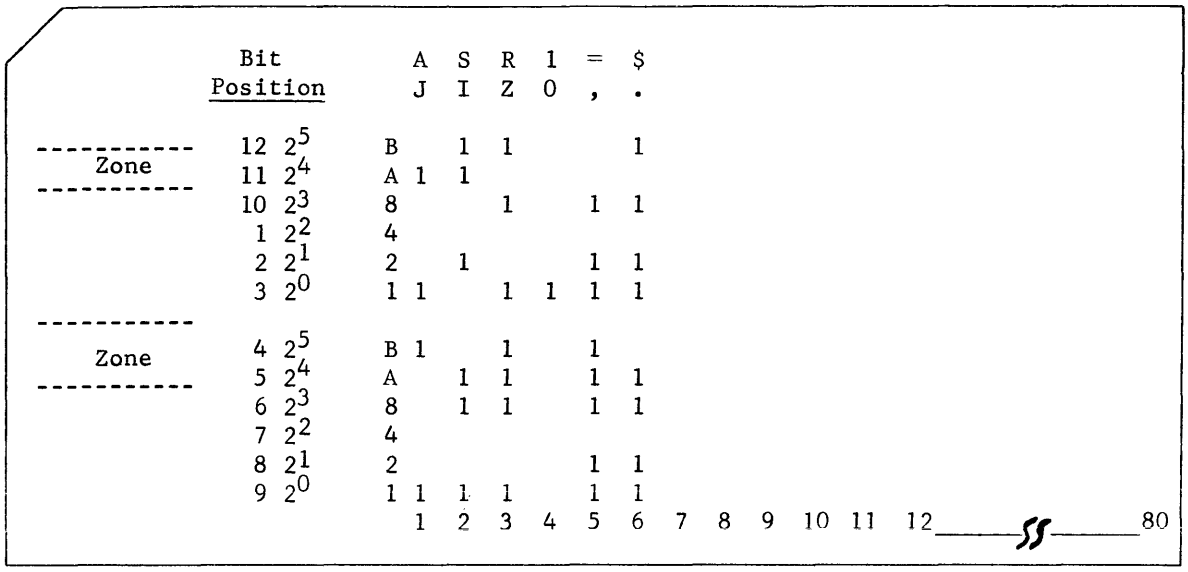


Hollerith 12 bit = A & B BCD
Hollerith 11 bit = B BCD
Hollerith 10 bit = A BCD

Hollerith 1-9 = BCD 1 2 4 8

An A = punch in A & B & 2^0
J = B & 2^0
S = A & "2^1"
I = A & B & 2^3 & 2^0
R = B & 2^3 & 2^0
Z = A & 2^3 & 2^0

INTERNAL BCD CARD



Hollerith 12 bit = A BCD
11 bit = B BCD
10 bit = A & B BCD

Hollerith 1-9 = BCD 1 2 4 8

An A = punch in A & 2^0
J = B & 2^0
S = A & B & 2^1
I = A & 2^3 & 2^0
R = B & 2^3 & 2^0
Z = A & B & 2^3 & 2^0

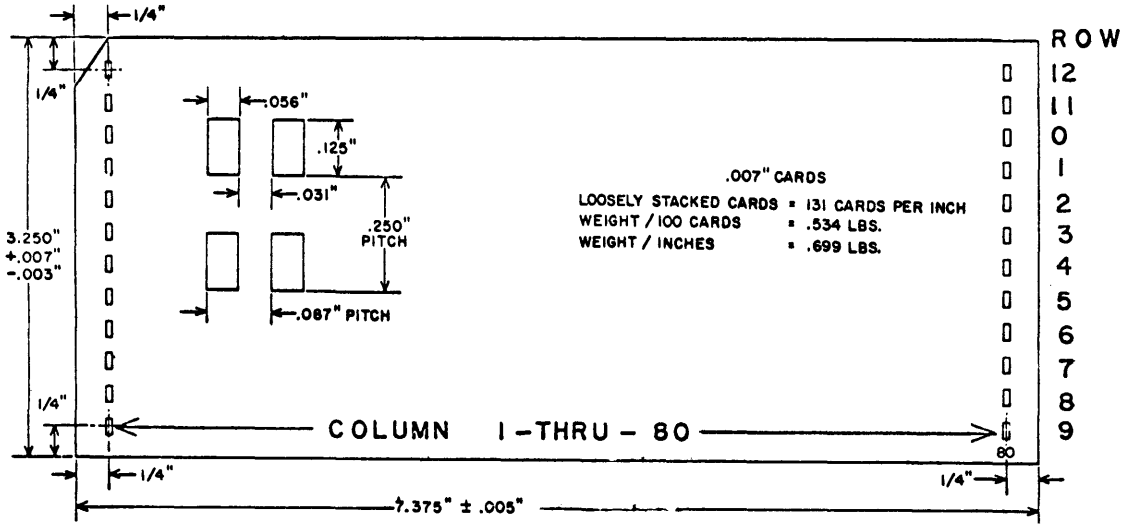
When converting Internal BCD to External BCD a very simple explanation will explain how it is done.

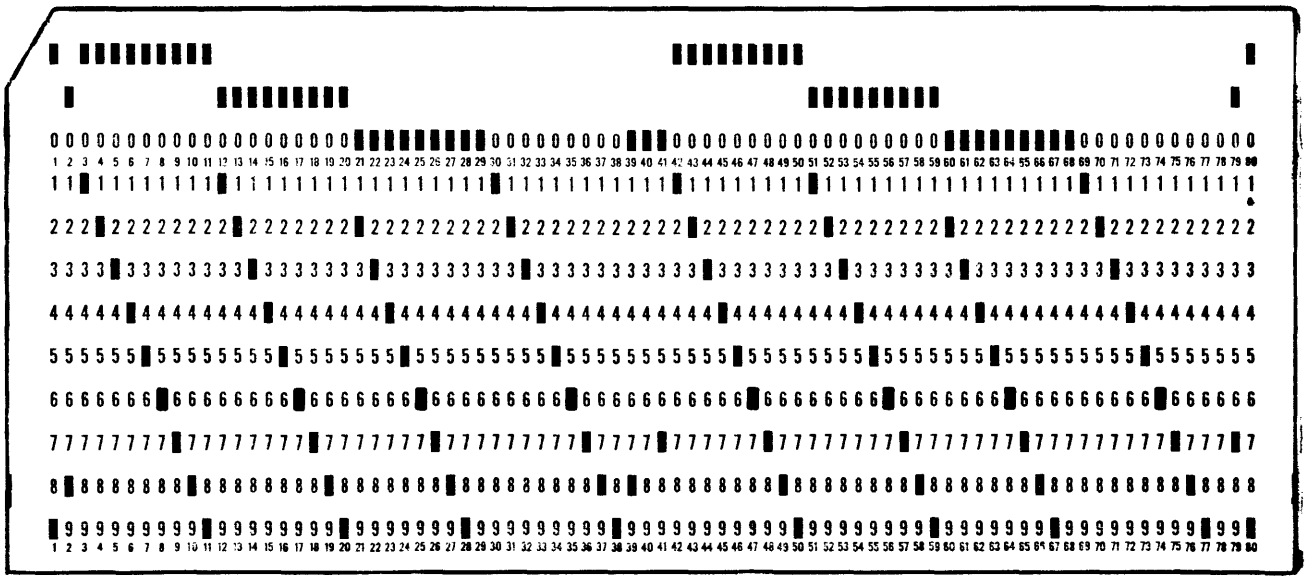
If bit 2^4 is a one toggle bit 2^5.
If bit 2^4 is a zero leave bit 2^5 alone.

Int A	Ext A	Int M	Ext M
21	61	44	44
010001	110001	100100	100100

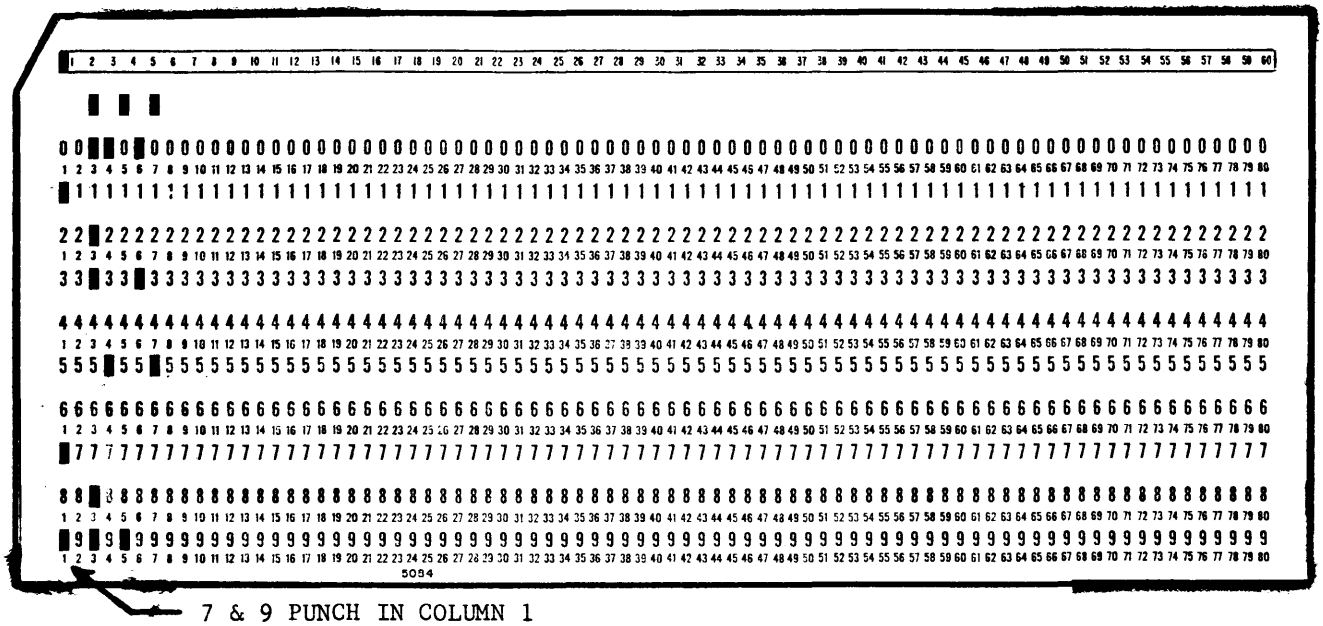
CARD SPECIFICATIONS

Standard thickness of a punched card is .007" (±.0004"). The following card dimensions are specified at 50% relative humidity. The corner cut indicates the top of the card. It may be found at the column 1 or 80 corner.

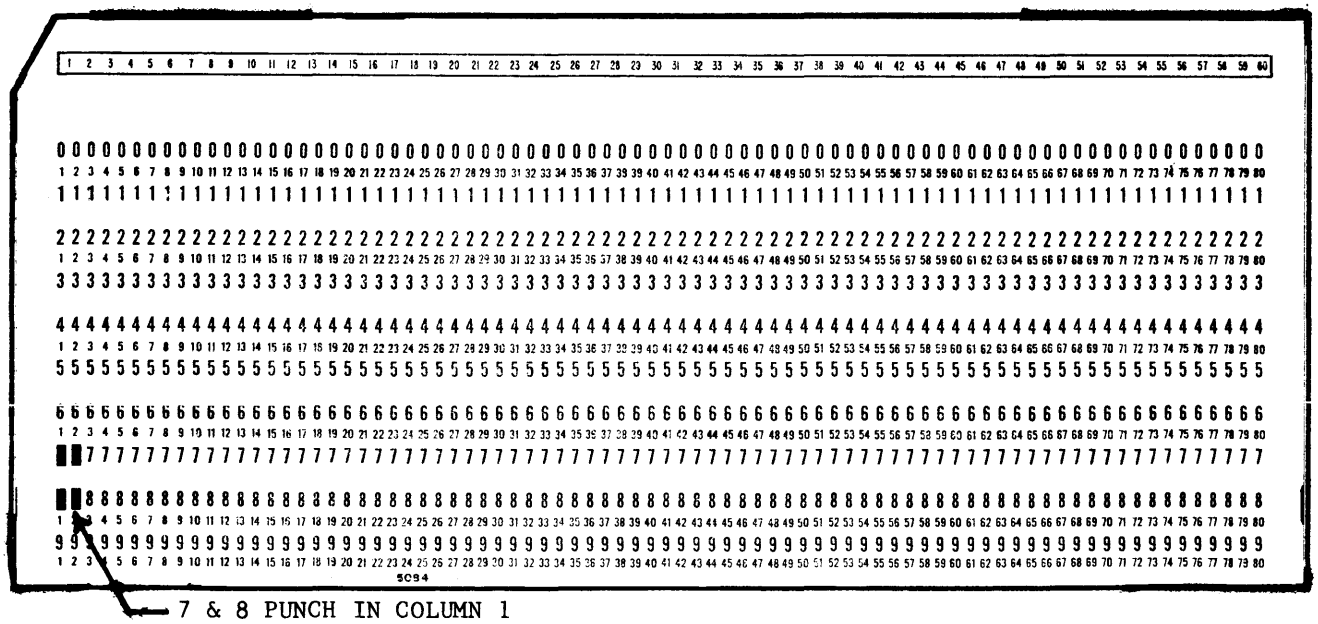




Hollerith Card



BINARY CARD



END OF FILE CARD

STUDY QUESTIONS

1. The best humidity range of data cards is?

   a. 35 - 65%

   b. 30 - 50%

   c. 20 - 30%

   d. 50%

2. If the differential of storage area and machine room humidity is 20% the maximum acclimatization of data cards should be:

   a. overnight

   b. 48 hours

   c. one and a half weeks

   d. no time

3. An oil stained paper card would probably:

   a. Present no problem on any machine

   b. Never read correctly

   c. Present extraneous data pick up on photo electric readers

   d. Would shrink the card size too much

4. To correct the curve due to warping found in stored cards what would be done before using them?

   a. Condition them for a longer period at machine humidity conditions

   b. Turn them over before placing them in the machine

   c. Fan them gently several times before placing them in the machine

   d. Flex them carefully back and forth a few times

5. Data cards stored in half-filled storage containers:

   a. Presents no problem no matter how they are handled

   b. Must be pressure blocked in partially filled containers and must not be stacked

   c. Present no problem provided they are used again within four to six weeks

   d. Present no problem if humidity is controlled at 20%

6. The space between column punched holes is:

   a. .125"

   b. .250"

   c. .056"

   d. .031"

7. The standard thickness of a paper punched card is:

   a. .009" ($\pm$.0004")

   b. .007" ($\pm$.0004")

   c. .0004" ($\pm$.007)

   d. .003" (no tolerance)

8. A loosely packed deck of cards measuring ten inches would have approximately how many cards in it?

   a. 1000 cards

   b. 131 cards

   c. 699 cards

   d. 1310 cards

9. The weight of the cards in the previous problem is approximately:

   a. 10.68 lbs.

   b. 1.068 lbs.

   c. 6.99 lbs.

   d. .699 lbs.

10. Data bits to be stored on standard 80 column cards are indicated by:

   a. Blank areas left in the row positions in each column on the card

   b. Holes punched in the row positions in each column on the card

   c. Data bits are not punched on 80 column cards

   d. Holes punched in between the row positions in each column on the card

11. Data bit positions in a word punched on the card are arranged:

   a. With 2^{0} bit position in Row 12 through 2^{11} bit position in Row 9 in Column Binary Word

   b. With 2^{11} bit position in Column 1 through 2^{0} bit position in column 12 in Row Binary Word

   c. With 2^{11} bit position in Row 12 through 2^{0} bit position in Row 9 in a Column Binary Word

   d. None of the above answers are **correct**

12. An End of File Card is identified by:

   a. A 7 and 9 punch in Column #1 of each card

   b. A 7, 8, and 9 punch in Column #1 of each card

   c. No 7 or 9 punch in Column #1 of each card

   d. A 7 and 8 punch in Column #1 of each card

   e. No identification is required for an End of File Card

13. Translate the following external BCD code statement

61 63-46-44-47-24-23-65-51 33
26-71-23-70-46-24-23 61 47-51-46-67-
51-61-44 33 71-22 61 70-71-67-70
22-47-65-65-64 44-46-51-46-45

14. The first data card, in a program deck of cards punched in the Binary format, is the only card that is required to have an identification code.

a. True

b. False

CHAPTER II

405 CARD READER

CHAPTER II

405 CARD READER

INTRODUCTION

During a Read operation, cards are transported from the Input (supply) Tray past the dual read station to the main receiving tray. Each tray accommodates up to 4000 punched cards of either the 80 column or 51 column type.

While the cards are being transported, both trays vibrate to overcome friction between cards and tray. The backup arm applies force to the end of the card supply and moves the stack toward the capstan. Air under pressure is injected at the lower left end of the input tray to provide positive separation between cards as they approach the capstan. Pressure is also provided at the left wall of the input tray to insure minimum friction drag on the card when being picked from the stack.

Punched cards are propelled from the supply tray past the read station to the receiving tray by a pneumatic capstan and a series of pinch rollers. The perforated capstan rotates continually. When vacuum is applied to the inner core of the capstan, a card is pulled against the capstan and moved through the card channel. Pinch rollers then move the card past the read station to the receiving tray.

An electromechanical brake assembly serves as a gate in the card channel. If the card read operation has not been initiated, the braking force overcomes the pulling force being applied to the card at the capstan and the card remains stationary. Once released, either manually or via the control unit, the braking shoe is pulled back to permit the card to pass to the dual read station.

The Read Station consists of two vertical columns of twelve photodiodes each, which sense information holes in the punched cards. Holes punched in each card column are read in parallel mode. The same column is then read by the second row of photodiodes and the results of the two read operations are compared. If the two information groups do not compare, the card is routed to a small secondary bin, in the manual mode of operation. In the automatic mode a "not compare" sends a signal to the adapter for use in external programming.

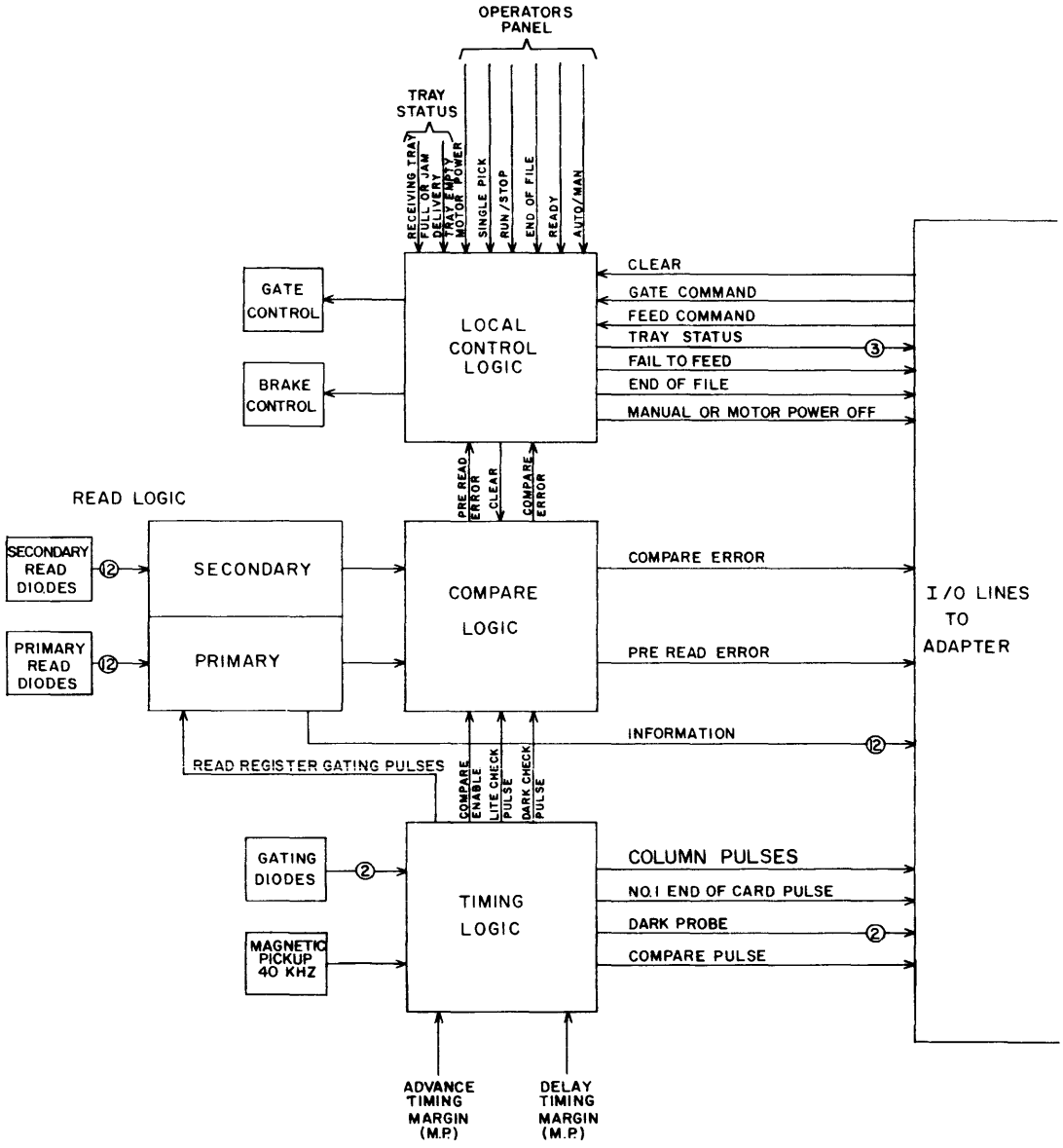
If no error was detected, the card continues into the primary receiving tray. The original orientation and sequence of the deck is preserved except those cards sorted to the secondary bin.

Information readout is executed by a clock pulse generated within the reader itself and occurs only when holes of the card column are centered on the read diodes. Clock pulses are resynchronized along the length of the card to compensate for poor card registration or card expansion due to temperature or humidity.

DETAILED SPECIFICATIONS

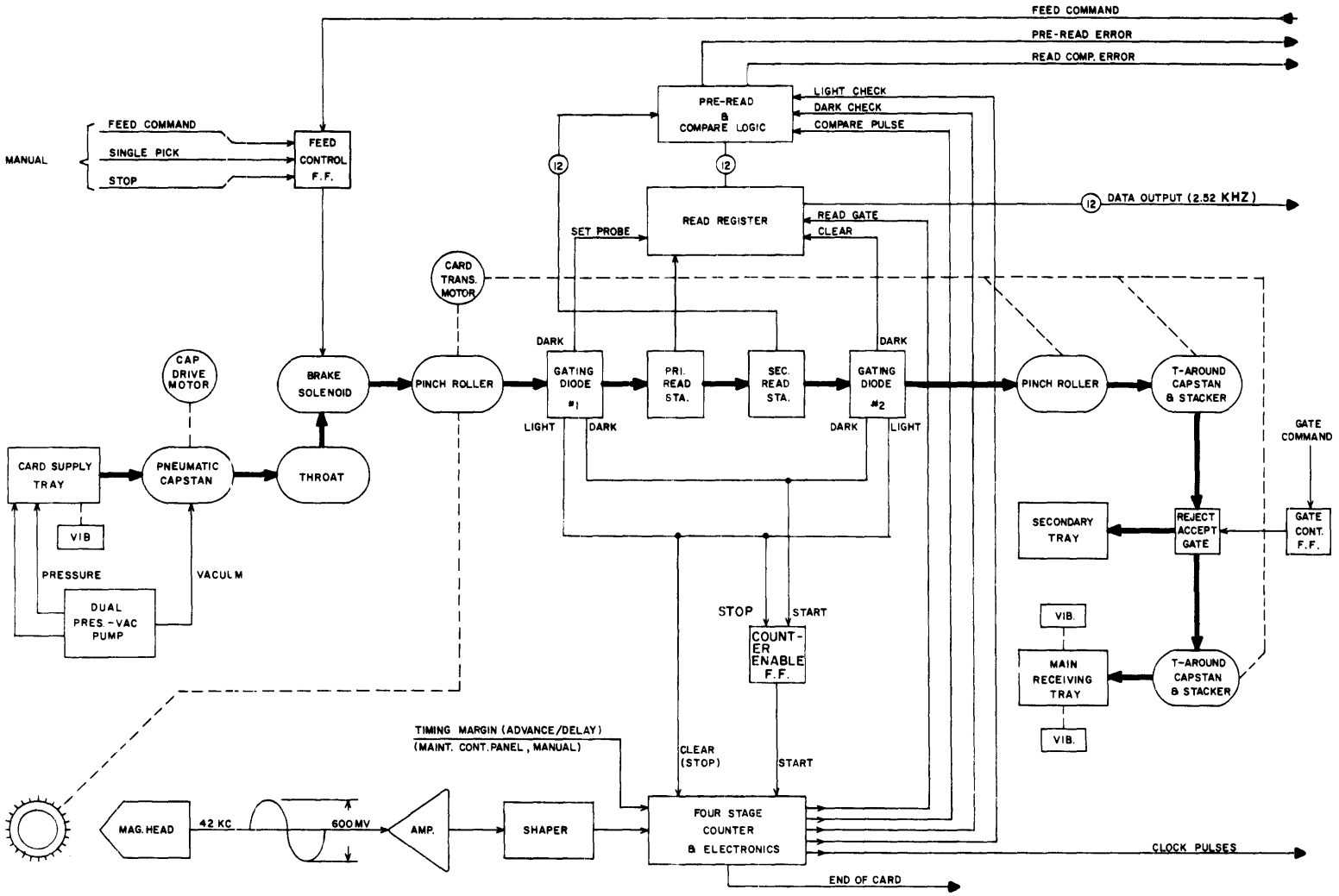
CARD READING	Method	Two rows of 12 photodiodes read and check punched cards column by column
	Dual Read Station	One column (0.087 in.) separation between read stations
	Preread Checks	Primary and secondary read station outputs compared. Automatic card rejection if comparison error exists in off-line mode. When on-line, the program controls rejection.
	Rate	1200--80 column cards read per minute 1600--51 column cards read per minute
CARD FEEDING	Input Tray	4000 card capacity Vibrating tray and pneumatic card separation for low friction card feeding
	Card Picking	Asynchronous (i.e. no waiting period between card selections)
	Method	Vacuum capstan applies ½ pound pull between horizontal rows of card punches. Card reaches capstan velocity within 2 ms.
	Card Drive	Pinch rollers at each side of read station receive card from capstan and move card past read station
	Card Speed	At capstan -- 130 ips At pinch rollers -- 218 ips At read station -- 218 ips
	Card Channel	Card input throat (0.0095 to 0.011 in.) permits passage of only a single card. Beveled upper and lower corners of card throat permit passage of cards with frayed or bent corners
	Card Brake	Solenoid controlled Stop time 3 milliseconds maximum Start time 14 milliseconds maximum
CARD DELIVERY	Receiving Trays	Original card orientation maintained in receiving trays 4000 card primary receiving tray 240 card secondary receiving tray Vibrating trays for low friction card receiving

FRONT CONTROL PANEL	Operator Controls with Indicators	Main Power Motor Power Auto/Man End of File	Ready Single Pick Run/Stop
ELECTRICAL	Power Source	208V $\pm$ 10%, 60 cycle (Mod A)*, three phase, 8 amps per phase	
	Input/Output	All input and output signals are digital as represented by nominal -3 and -0.5 voltage levels. Signal voltages are presented and received via connectors B40 through B42	
WEIGHT	1060 LBS.		



Block Diagram

For purposes of discussion, the 405 logic is divided into four general Control sections: read, timing, compare and local. The Block Diagram shows the relationship of these sections to the adapter (control unit).



System Block Diagram

FUNCTIONAL DESCRIPTION

Functional sections of the 405 Card Reader may be divided into the following categories: The card transport mechanism, dual read station, pneumatic system and cabinet cooling system. This chapter discusses each equipment section in detail, explaining construction characteristics and their function in the overall equipment.

CARD TRANSPORT MECHANISM (Refer to system block diagram)

The basic card transport channel is formed by a cast aluminum structure which guides the card from the input throat assembly to one of two output positions. The pneumatic capstan, pinch rollers and assist rollers propel the card (edgewise) along its route in the transport channel.

Bold lines indicate the route of card travel and the various components that act upon the card during its travel. Solid lines indicate paths of information flow as well as the source and destination of control signals; dotted lines indicate areas of mechanical coupling.

Supply Tray and Receiving Tray -- The card supply tray and receiving tray are constructed in a similar manner. Each stainless steel tray is mounted on a base structure comprised of laminated birch wood, which forms a solid platform for the individual tray. The platform, in turn, is mounted on four shock absorbers. The steel trays are constructed such that they form two parallel halves. When the narrow half is removed, turned end-for-end and remounted, the raised metal strip forms a marginal guide for the type of punched card being used (80-column or 51-column). The broad half of each tray is fixed to the laminated platform.

A single electromagnetic vibrator unit is fixed to the bottom side of the supply tray. Because the receiving tray must stack as well as accommodate large numbers of cards, two vibrator units are employed in this assembly (the only significant difference between the two card trays). The vibrator receives pulsating current at the rate of 60 Hertz, causing vibrations to be induced into the card tray assembly. Hence, the vibrating action reduces friction forces between cards and the tray surface, requiring minimum mechanical force in feeding cards to the pneumatic capstan and in assembling cards in the receiving tray.

Each card tray contains a backup arm which supports the cards at the right end of the stack and travels over the entire length of the tray. This arm has a dual function; to hold the card stack in an upright position, and to apply a slight pressure to the entire stack as cards move across the tray. In the supply tray, the backup pressure is greatest when a large number of cards are being carried toward the capstan, and pressure decreases as the card supply is reduced. Pressure is applied to the backup arm by a coil spring element, which is contained within a circular housing and connected to the arm by a cable and pulley arrangement.

When the last card has been pulled from the supply tray, the condition is sensed by a switch plunger which protrudes from the feed wall of the tray. As long as a single card is contained in the tray, the plunger is depressed. When removed, however, the switch plunger passes through a hole in the backup arm and a circuit is closed. The empty tray signal is transmitted to the computer (via adapter circuits) when the leading edge of the last card covers gating diode No. 2. A pneumatic switch is employed in detecting a supply tray empty condition. This switch is located in the pneumatic circuit which applies vacuum to the feed capstan. When the supply tray is empty, vacuum to the capstan drops from its normal level of 15 inches of mercury to one inch, and the switch is activated to produce the desired signal.

Pneumatic Capstan -- With vibration of the card supply deck and mechanical force being applied at the right end of the card stack, the cards move toward the capstan area. Air under pressure is injected at the bottom of the card stack, near the left end of the tray, insuring positive separation between cards. Distribution of air from below is via a series of 26 holes, arranged in two columns across the width of the card tray. Air is also injected from the forward, or left wall of the tray, in a direction perpendicular to the cards. This combination of air pressure tends to form a pneumatic cushion which "floats" the first card as it nears the capstan.

The capstan consists of a perforated drum which is driven continuously by a direct-coupled motor. A fixed graphite block is located inside the capstan drum, which extends over the entire length of the drum and contains a 3/8 inch cutout or opening at one side. This block is held to the inner surface of the rotating capstan by spring tension. Vacuum equal to 15 inches of mercury is applied to the graphite block element via flexible tubing. The circular capstan contains a total of 1080 holes of 1/16 inch diameter and are located such that vacuum is always applied to the solid portions of the card (areas between horizontal rows of punched holes).

When the first card moves into position, the capstan exerts a pulling force of approximately 1/2 pound on the forward end of the card, and the card reaches capstan velocity (130 inches per second) within 2 milliseconds. Picking action of the capstan is asynchronous; i.e., there is no "pick cycle" or waiting period between card selections. Rather, picking action is continuous as long as the brake unit permits the card to pass through the input throat. When initiating the card transport operation (first card of group), approximately 40 milliseconds are required between receipt of the pick card command and reading of the first card column. Following transport of the first card, this interval is reduced.

Card Input Throat -- The capstan forms one half of the throat; a fixed member forms the other half. The front edge of the throat contains a slight bevel which assists the card in being pulled into the narrow opening (0.0095 to 0.0115 inch). The thickness of a single card is approximately 0.007 inch, hence the throat permits the passage of only a single card at a time. The left wall of the supply tray, through which

the slotted capstan protrudes, tends to peel the card from the capstan as the vacuum force pulls the card into the throat.

The throat gap extends over the entire 3 1/4-inch vertical dimension of the card. Upper and lower corners of the throat are beveled such that frayed or bent card corners cannot jam or hang up as they enter the narrow opening. Vacuum is applied to the capstan continuously; therefore, when one card passes through the throat, the next card is immediately pulled from the supply stack and advanced behind the previous card.

Brake Unit -- An electromagnetic card brake assembly is located just inside of the input throat and acts to control the passage of cards through the transport channel. The brake magnet contains a U-shaped core with coils mounted on each leg. A hinged armature is driven by a relatively heavy spring which provides the necessary card-braking force. Hence, when the magnet coils are de-energized, the braking shoe extends into the transport channel to prevent card movement. When the coils are energized, the brake shoe retracts to allow cards to pass through the machine. Since the card braking operation is not dependent upon current flow through the magnet coils, a card "jam" condition is avoided in the case of power failure.

The brake is approximately 1/4 inch wide, 2 3/4 inches long and fabricated from hard-coated aluminum. The shoe is fixed to a flat spring plate which, in turn, is mounted on the main transport casting.

Initially, when cards have been loaded in the supply tray and the capstan energized, the first card is picked, inserted into the throat, and has passed approximately one-third of its length into the throat when it strikes the brake shoe. The card remains in this position, the capstan slipping on the card, until the card transport operation is initiated. If braking force is applied while cards are being transported, the card motion is arrested by pinching action between the brake shoe and the transport channel wall. The brake shoe is grooved such that braking force applied to the moving card is always applied to the solid areas between card rows.

Pinch Rollers, Read Station -- Pinch rollers are located at each side of the read station. The purpose of these rollers is to assure positive transport action as the card is carried past the read station, and to avoid possible skew or misalignment of the card while being read. Both pinch rollers are belted together to insure uniform rate of card transfer during the read operation.

Each pinch roller assembly consists of a steel roll (the driven member) and an idler roller which is made of a rubber-like material. Peripheral velocity of the pinch rollers is 218 inches per second. Because the rotational rate of the pinch rollers is considerably greater than that of the capstan, spacing between cards is greatest in this area. From the read station on, however, a fixed spacing of approximately 3 3/4 inches is maintained between cards.

There is an exact correlation between the diameter of the steel roller contained in the first pinch roller assembly and the hole pattern of the

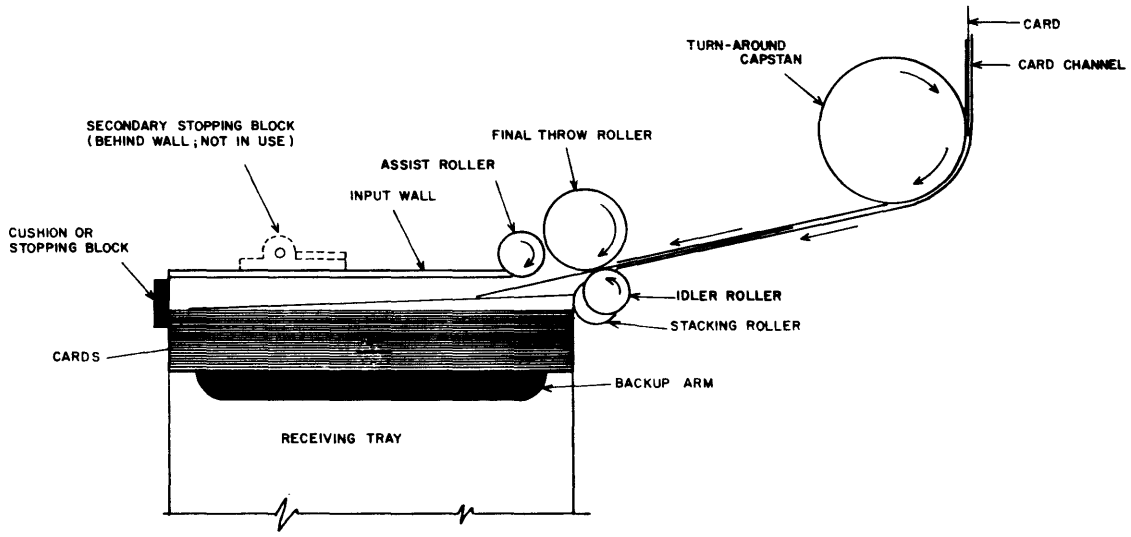
punched card. The roller diameter is such that 54 vertical columns of the punched card are traversed with one revolution of the roller. The drive shaft of this roller also mounts a timing gear, or toothed wheel, which is used in generating internal clock pulses. This component serves as the heart of the internal clock system, which acts to coordinate overall operation of the Card Reader and transmits timing pulses to the adapter. One such timing function is to insure that the read operation occurs only when the card holes are centered on the read diodes.

Accept/Reject Gate -- This electromechanical gating unit is located between the two turn-around capstan wheels and acts to channel the punched card to either the secondary tray or regular receiving tray. This assembly employs a U-shaped core and dual core configuration as previously described for the card brake. The armature structure differs, however, in that it controls the position of card-gating fingers. When the magnet is de-energized, the gating fingers are not extended and the card travels to the main receiving tray. When energized, the gating fingers move into the card channel, causing the card to make a full 180-degree turn at the first turn-around capstan and is carried into the secondary receiving tray.

If a given card is to be rejected and channeled into the secondary tray, the gate command pulse must be received within 1.5 milliseconds after the last column of the card has been read.

Stacker Assemblies -- Before the card is deposited in either the secondary tray or main receiving tray, it must pass through a stacker assembly which is located at the entrance of each of these final positions. The primary function of both stacker assemblies is to deposit the card into the chosen output position. The first turn-around capstan forms part of the secondary bin stacker; the second is part of the receiving tray stacker. When a card has passed through the stacker assembly, it has been turned 180 degrees from its original position. Because of construction similarities, the following description is directed toward the stacker assembly serving the main receiving tray.

The card is assisted by the turn-around capstan and enters a pair of final throw pinch rollers. From here, the card is boosted by the assist roller which drives the card into the tray. As the card enters the receiving tray, the leading edge strikes a stopping block which is faced with a polyurathane material. The speed at which the card enters the tray causes a slight rebound as it strikes the stopping block, but the throat area at the entrance to the receiving tray prevents the card from bouncing back into the card channel. Also, a slow-speed stacking roller moves the trailing edge of the card aside to permit unhampered entrance of the next card.



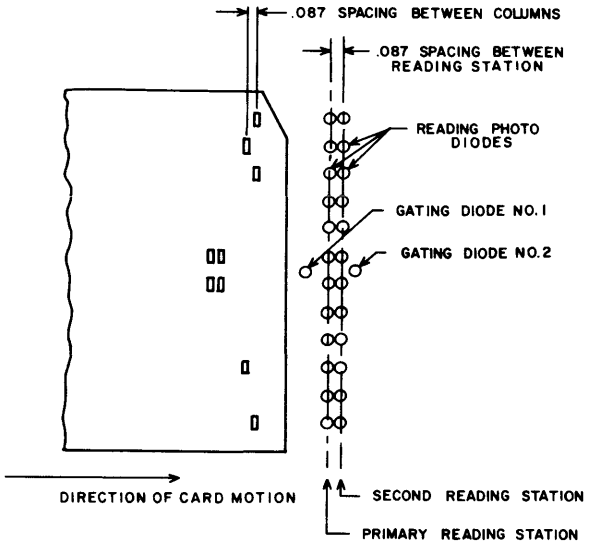
STACKER ASSEMBLY

Jam-Detecting Devices -- Switches perform a jam detection function at the throat entrances of each output tray. The switch plunger is located behind a hinged sensing plate, which moves to actuate the switch if a card should fold or become crumpled. A second detection device is located at the entrance of the receiving tray. This consists of a photoelectric circuit which transmits a light beam from the floor of the tray to the photocell above. When cards are being handled in normal manner light cannot reach the photocell; a crumpled card opens this area to permit light transmission and the error condition is sensed. These sensing devices produce an error signal which de-energizes the card brake and operation is halted.

DUAL READ STATION

The read station consists of two vertical columns of twelve photodiodes each and two gating diodes, located at each side of the read diode columns. Spacing between read diode columns is equal to that of one card column, i.e., the space between punched holes on the card (0.087 inch). Vertical spacing between diodes is 1/4 inch and the diodes span twelve information rows of the card.

Gating Diodes Nos. 1 and 2 -- Gating diode elements are located between the horizontal rows of read diodes such that they always see the solid portions of the punched card. Hence, these diodes are triggered only by the leading edge or trailing edge of the card.



DIODE CONFIGURATION OF READ STATION

Because the gating diodes are slightly offset from the vertical alignment of the read diode columns, presence of the punched card at the read station is sensed by gating diode No. 1. The leading edge of the card covers this diode and a signal is generated which initiates a preread photocell and read logic check. This condition initiates an examination of all read diodes and logic circuits before the read operation begins.

At this time, all diodes must indicate "light", or that light is striking each of the 24 read diodes. When the leading edge of the card moves on to cover gating diode No. 2, another pulse is generated which checks the "dark" state of all diodes (card covering both gating diodes). If a discrepancy is sensed in either of these tests, a signal is transmitted to the computer, via adapter circuits, which indicates an error condition at the Card Reader.

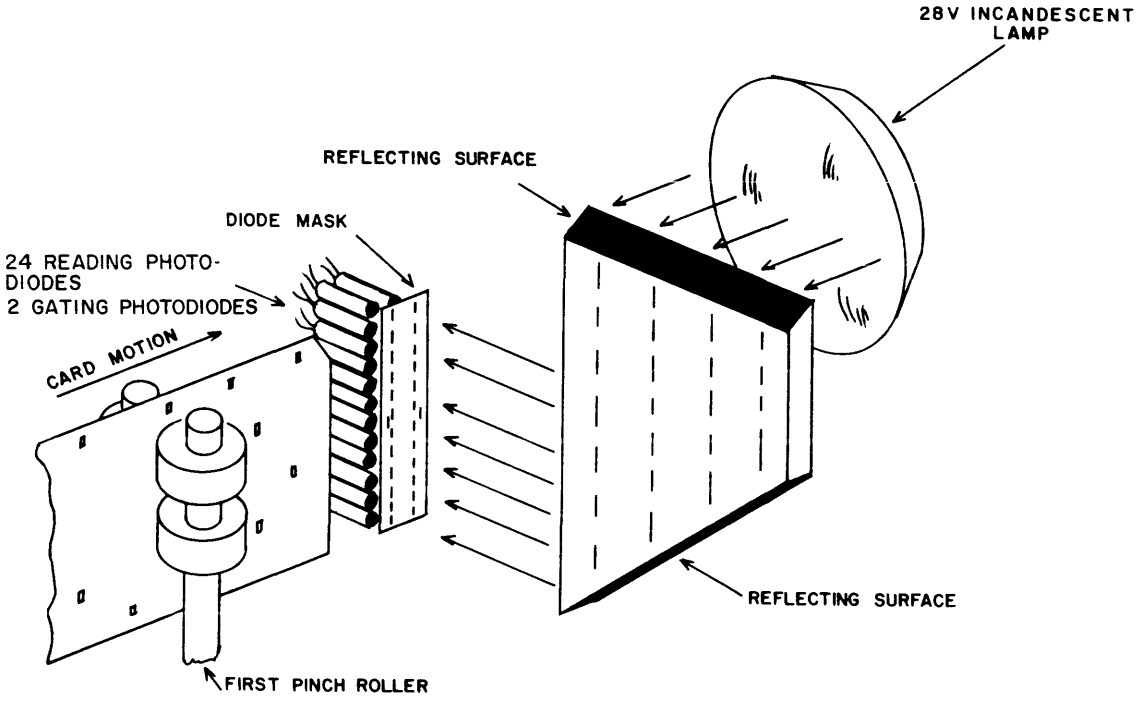
The Diode Mask -- All read station photodiodes are covered by a mask which contains rectangular holes that are slightly narrower than the width of the punched card hole. The length of these slots is equal to the punched card hole. Masking slots covering gating diodes No. 1 and No. 2 are smaller in length than those used for the read diodes. The smaller dimension allows for minute card skew or the possibility of slight misorientation between information holes contained in the punched card.

The read station assembly provides a choice of three possible locations for each of the gating diodes. The lower-most location places the diode nearest the vertical read diode column, and each succeeding location represents horizontal displacement of 0.012 inch.

A glass cover is fitted over the masking plate of the read station to form a flush wall in the card transport channel. This cover also avoids maintenance problems by preventing the accumulation of dust and foreign particles at the read station.

Excitor Light Assembly -- The photodiode excitor light source consists of a 28-volt, incandescent lamp. Light rays from the lamp are directed toward a periscopic mirror element, where the reflective surface at the upper end directs light rays downward, through the optical glass, to strike the second reflective surface at the lower end. Parallel light rays are emitted from the edge of the glass and mirror element. The periscopic system distributes the light evenly, over the three-inch read station area, and isolates the photodiodes from the heat being radiated by the lamp. This configuration provides no horizontal surfaces which might accumulate dust and hamper light transfer. Light enters the optical element at a vertical surface and exists at a vertical surface.

Operation of the excitor lamp is normally at 20 volts, rather than the rated 28-volt level. This greatly extends the operational life of the lamp and reduces ambient temperatures within the light source housing. Louvers contained in the cover of this housing permit convection currents to carry the lamp heat from the enclosure.



EXCITOR LAMP ASSEMBLY

When the punched card reaches the dual read station, parallel light rays pass through the information holes of the card and strike the corresponding read diodes. At the peak of light transmission, timing circuits transmit a read gate probe, which permits information contained in the first card column to be recorded in the primary read register. Hence, each 12-bit column of the punched card is read in character-serial manner. Once read and recorded, the first card column is read again by the second group of read diodes. This operation is performed in sequence for each column of the card. If any two information groups do not correspond, in the automatic mode of operation, a compare error signal is transmitted to the computer and the computer may return a gate command signal to channel the card into the secondary tray. In the manual mode of operation, the compare error signal acts as a gate command to channel the card into the secondary receiving tray.

Clock Assembly System -- The timing gear is being driven by the card transport motor. Mechanically, this gear element is mounted on the drive shaft of the first pinch roller (at the left of read station) and contains a total of 864, 120-pitch, metallic projections. This wheel is never used as a gear, however, but is mounted in close proximity to a magnetic pickup head. As the gear rotates, the teeth change the reluctance sensed by the pickup head. Output from the pickup is a sinewave voltage with peak-to-peak amplitude of approximately 600 millivolts at a frequency of 40 kilohertz. This signal is amplified, shaped and fed to a four-stage counter.

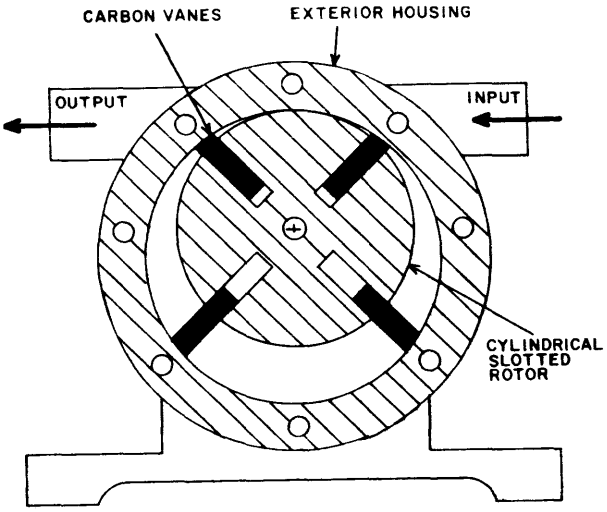
PNEUMATIC SYSTEM

The pump unit provides a source of low-volume pressure and vacuum required in picking cards at the capstan. This system also aids in the separation of cards at the supply tray.

Dual Pump Unit -- The system employes a dual rotary pump, consisting of two pump assemblies within a common exterior housing but separated from one another within. A common shaft serves both units and is belt-coupled to a drive motor.

A cross-sectional view of a single pump unit is illustrated. The physical configuration includes the outer housing with intake and exhaust ports and a slotted rotor containing vane inserts. Except for the intake and exhaust ports provided in the upper area of the housing, the inner side consists of a smooth, polished surface. The central rotor is bearing-mounted and located off center toward the upper side of the housing. Four vanes ride freely in the slots provided in the cylindrical rotor. When the drive motor is energized, centrifugal force causes the vanes to move outward in a radial direction and follow the surface of the housing.

Pneumatic Circuits and Components -- As shown, the dual pump assembly forms two independent pneumatic circuits; one pressure, the other vacuum. The pressure pump draws atmospheric air through an intake muffler, which serves to limit operating sound and to filter dust and foreign particles

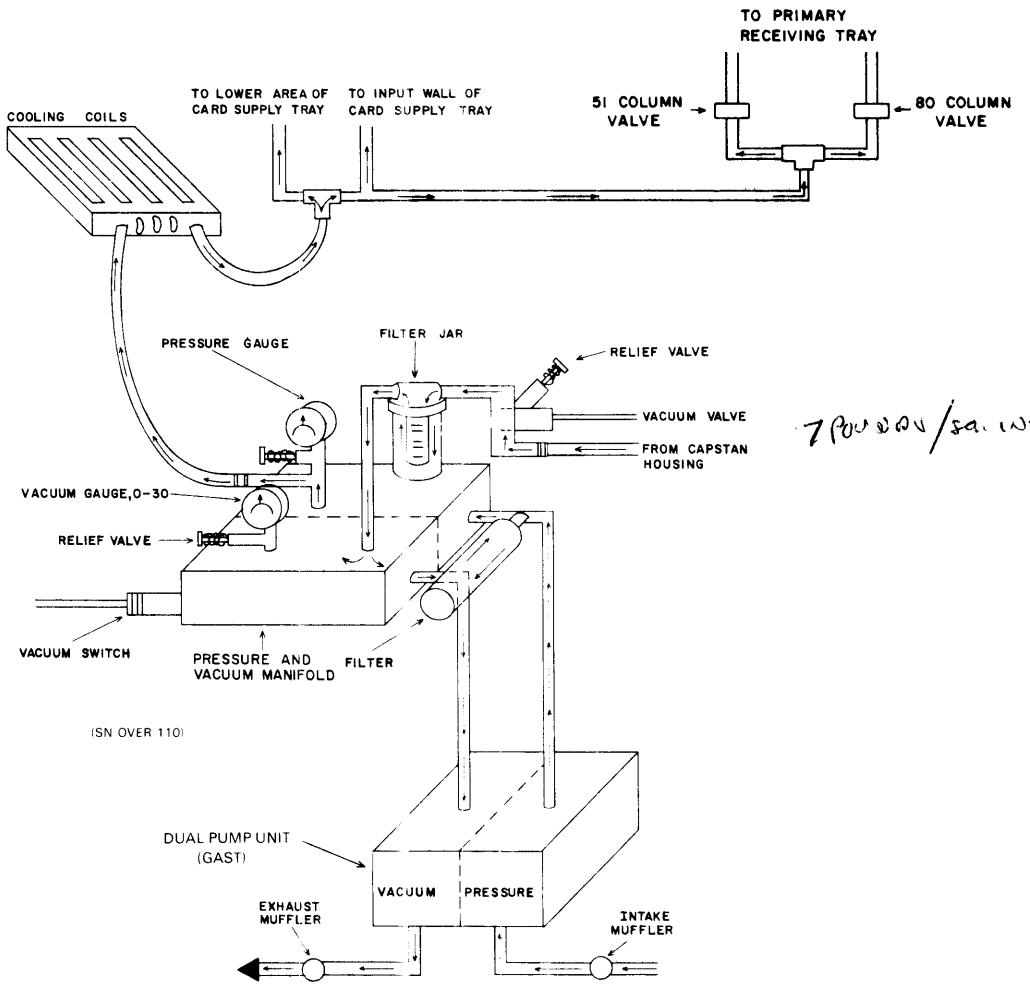


CROSS SECTION OF DUAL PUMP UNIT

from the incoming air. Compressed air enters the pressure line where it is subjected to a second filtering process. The filter contains a corrugated filtering element made of a special paper which removes all carbon particles 1.0 microns and larger. Compressed air is forced through the filter paper and on to a drilled assembly block. The relief valve provides adjustment of the air pressure in the circuit which may be read directly at the pressure gauge. The cooling coils absorb existing heat from the air, which has been generated as a result of high compression, and dissipates the heat via radiation fins. Cooled air is then distributed to the upper and lower areas of the card supply and receiving trays.

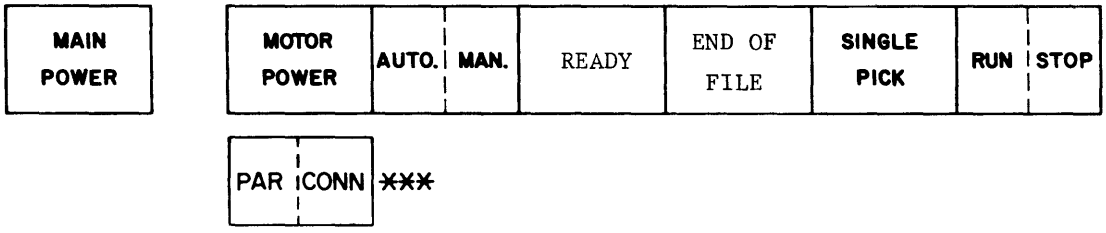
The vacuum circuit functions in similar manner, except that vacuum is pulled on the circuit and pump exhaust is via an output muffler. The upper filtering unit consists of a cloth and glass jar combination which extracts bits of paper and dust from the vacuum circuit. The vacuum switch detects drastic changes in vacuum level, such as occurs when all cards have been picked from the supply tray and cards are no longer in contact with the capstan. When this condition exists, the switch is activated and the signal is used in generating the end-of-card pulse.

In units above serial number 110 the basic pressure and vacuum routing is the same as in units 110 and below. However in later units the pressure and vacuum manifolds are combined into one and an additional vacuum valve has been added. The vacuum valve reduces the vacuum to the capstan when card feeding is interrupted for more than 1.3 seconds.



VACUUM & PRESSURE COMPONENTS OF THE
PNEUMATIC SYSTEM

MANUAL CONTROLS AND INDICATORS

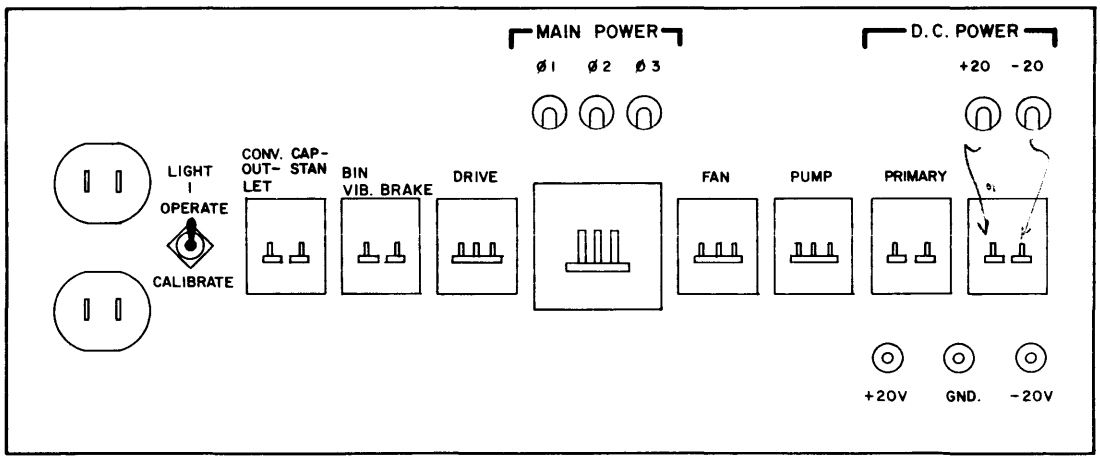


NAME		FUNCTION
MAIN POWER	S**	Applies power to cabinet cooling fans and d-c power supplies and exciter lamp.
	I**	Lighted while power is on
MOTOR POWER	S	Applies power to the capstan motor, card transport motor, card tray vibrator units and rotary pump motor
	I	Lighted while power is on
AUTO-MAN	S	Toggles the mode of equipment operation between automatic and manual
	I	When Auto is lighted equipment is under external control. When Man is lighted equipment is under manual control
END OF FILE	S	Switch may be pressed when the last group of cards (of a given number to be read) has been placed in the input tray
	I	When on, light indicates that an end of file signal is being sent to the adapter
READY	S	Places card reader in ready to operate state
	I	Turned on only when all of the following conditions are met: Card supply tray is not empty No error conditions exist throughout the unit Receiving tray is not full Secondary tray is not full Primary power is applied to unit If any of the above conditions occur during operation of card reader, indicator will be turned off. Condition must be corrected and switch pressed to re-establish ready state. In auto mode, a clear signal must be received from adapter or Ready switch pressed before operation may be resumed.

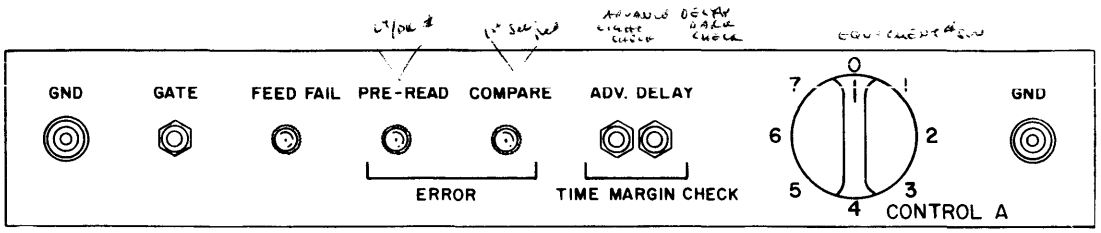
NAME		FUNCTION
SINGLE PICK	S	Momentarily releases card brake and permits a single card to be read. One card is read each time switch is pressed when in manual mode
RUN-STOP	S	In manual mode of operation, this switch starts or stops the card transport operation
	I	Corresponding half of this switch is lighted when card reader is in run or stop state. In auto mode neither half is lighted

*Switch
**Indicator
***Controller indicators

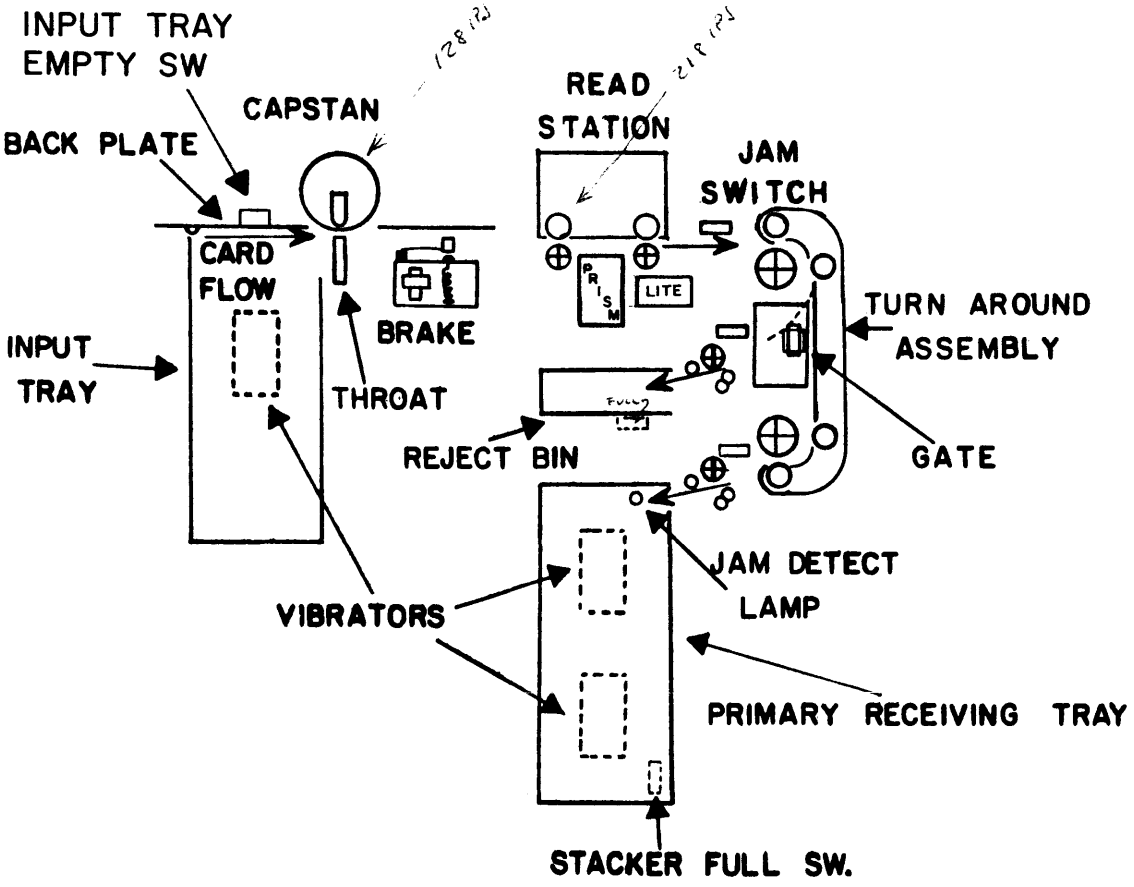
POWER CONTROL PANEL



POWER CONTROL PANEL



MAINTENANCE PANEL



405 CARD FLOW

1200 80 col. cd/m
1600 51 col. cd/m

-50 ms/80 col. cd.
-32 ms Actual read time.
400ms/cd.

LOGIC DESCRIPTION

READ CONTROL

This portion of the logic detects information punched in cards and routes the information to the adapter in binary form. The read logic is divided into two sections; primary read circuits and secondary read circuits.

Primary Read Circuits

The 12 primary read circuits detect and route information from the punched card to the adapter. A typical circuit is shown in figure 1.

When a card moves through the read station, each vertical column of information passes between the exciter lamp and the photodiodes. Light from the excitor lamp passes through each punch in the column and illuminates the corresponding photodiode.

The signal from the photodiode is amplified, converted to standard logic voltage levels by MOXX and gated to the associated Read Register FF by signals from the Read register gating circuit. If the photodiode is illuminated (punch in that column position) the Read Register FF is set and a "1" bit is sent to the adapter. If no punch is detected the FF is cleared and a "0" bit is sent to the adapter.

After the column is read the adapter is informed that information is on the line by a 10 usec. pulse from the clock counter circuit. When the next column is detected and the gating pulse is received the new information is placed on the lines for sampling by the adapter. Note that the information bits are also sent to the compare circuit for checking purposes.

Secondary Read Circuits

Approximately 400 usec. after a column of information is read by the primary read circuits, the same column is read by the secondary read circuits (figure 2). The information bits are, as before, amplified, converted to logic voltage levels and immediately routed to the compare circuit for verification with the outputs from the Read register. Note that the results of the secondary read are not temporarily stored in a register or sent to the adapter.

3.75 inch gap conv. feed

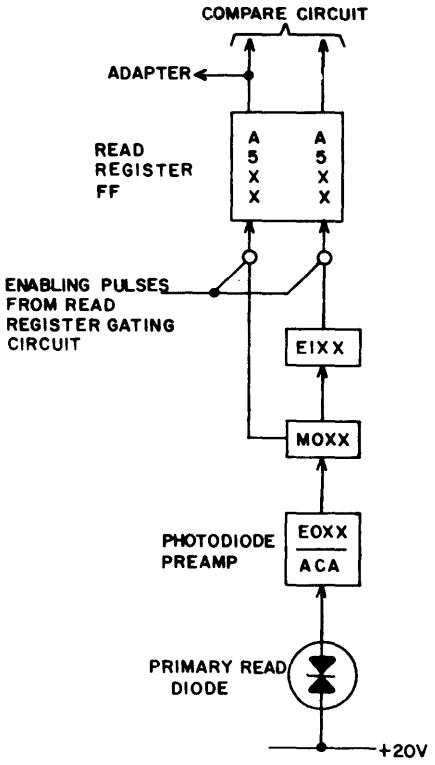


Figure 1 TYPICAL PRIMARY READ CIRCUIT

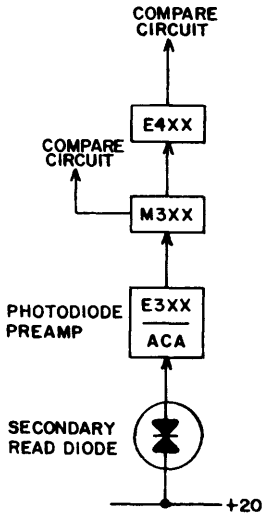


Figure 2 TYPICAL SECONDARY READ CIRCUIT

TIMING CONTROL

The timing control logic provides enabling signals to the card reader logic circuits and timing pulses to the adapter. The basic circuits of this section are the clock counter circuit, read register enable circuit, resync circuit and the compare pulse timing circuit.

Clock Counter Circuit

The clock counter is the heart of the timing logic. Counter output pulses are presented to other timing logic circuits and are arranged so that associated circuits are enabled only when the counter is at a specific count.

A timing gear and magnetic pick-up generates a 40KHZ sinewave with a peak-to-peak voltage of approximately 600 millivolts. This signal is amplified and shaped by the EFA card (B000). B000 outputs two square wave pulses which are 180 degrees out of phase. One output is called the advance pulse, the other output is called the transfer pulse (figure 3).

The output from B001 provides an advance pulse to Rank I (RI) of the clock counter. The advance pulse increases the count in RI by increments of one with each pulse. The output from B002 enables the AND gates between RI and RII thereby transferring the contents of RI to RII. This transfer pulse is the equivalent of a half count; that is, when the count of 7 in RI is transferred to RII the equivalent count stored in the counter is 7 1/2. The next advance pulse then sets the counter to 8. Table 3 briefly outlines how the counter advances and stores counts.

State of RI FF's

A000/001	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
A010/011	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A020/021	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A030/031	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
Equivalent Decimal Count	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

0 = cleared; 1 = set

Table 3

Note that 0/0/0/0 appears as the equivalent of both 0 and 16. When there is no card in the read station, the counter is held with all FF's clear and the equivalent count is 0.

When all FF's of the counter (RI and RII) are set, the count is 15 1/2. The next advance pulse clears all FF's of RI, setting the counter to 16, and enabling a 10 usec. "0" to the adapter. The subsequent transfer pulse clears all FF's of RII, and the counter begins at one with the next advance pulse. A complete counter cycle requires approximately 400 usec.

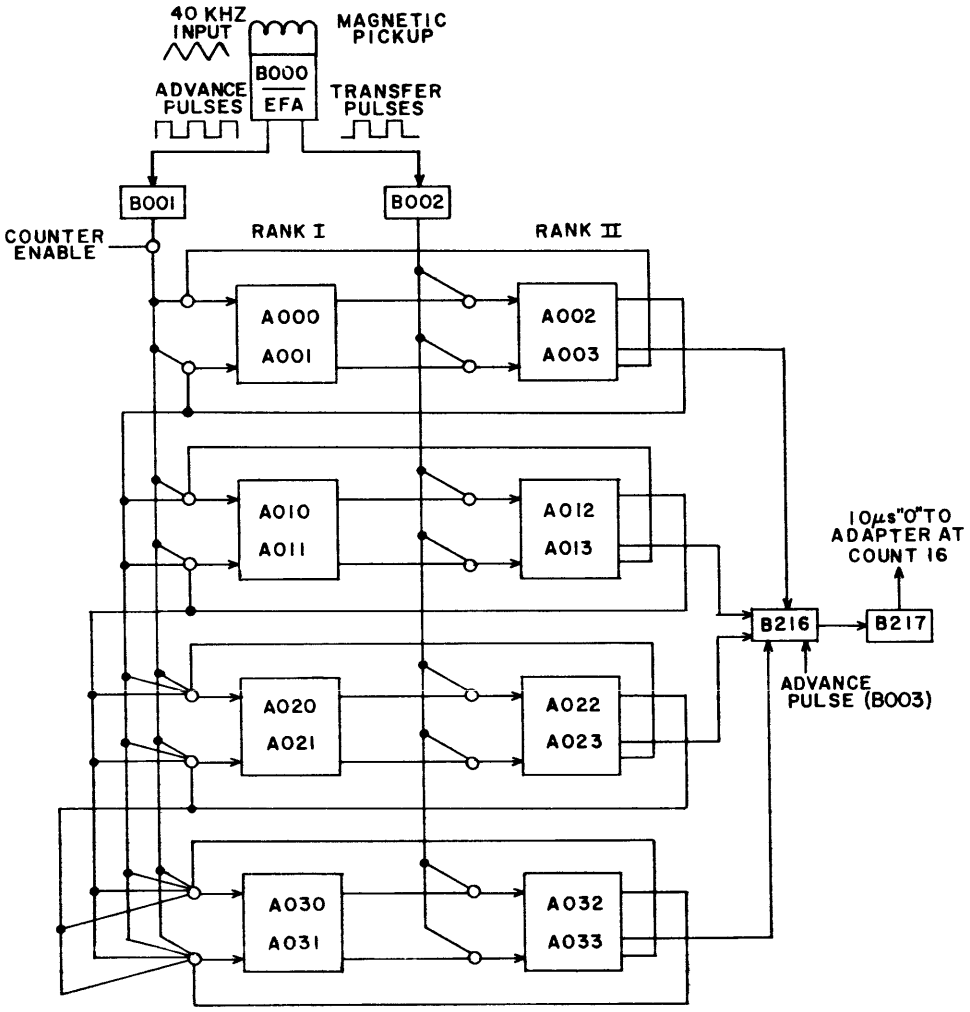


Figure 3 CLOCK COUNTER

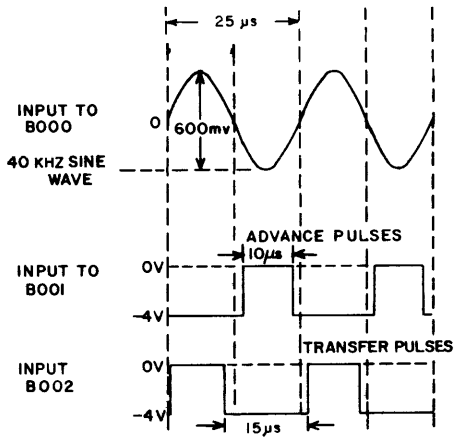


Figure 4 CLOCK ADVANCE AND TRANSFER PULSES

As a general rule, the clock counter makes as many complete cycles as there are columns on the card, plus a final count of 13 1/2. Thus, an 80-column card advances the counter to 16, 80 times, plus a final count of 13 1/2. Throughout this section the clock count will be referred to by counter cycle and count. Thus, counter cycle 4 count 13 is written T4-13.

Counter Enable

The Counter Enable consists of two gating diodes, the Counter-Enable FF and associated inverters. The main function of this circuit is to enable advance pulses to the counter. Advance pulses are enabled as the card enters the reading station and are disabled when the last column passes the read station.

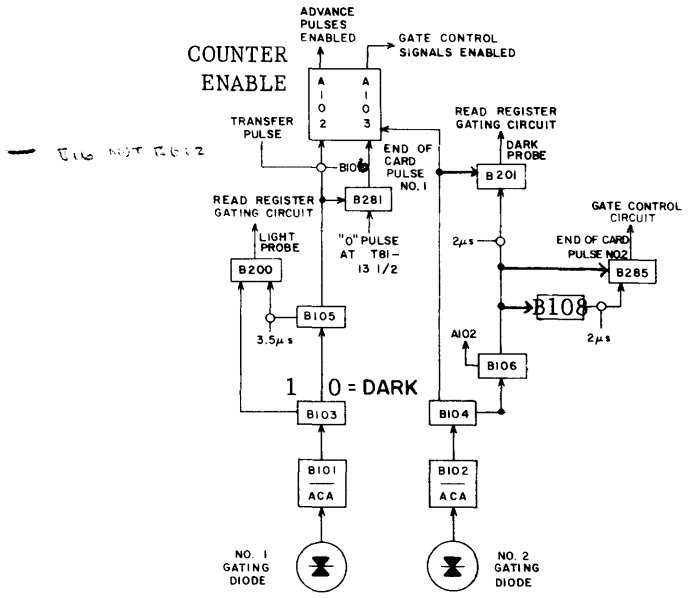


Figure 5 Counter Enable

Two gating diodes (one on each side of the read station between horizontal card rows) detect cards entering and leaving the read station. When a gating diode is lit (card not covering it) the equivalent of a logical "0" is forced from the associated ACA card. As a card enters the read station the output of first one ACA card and then the other is changed from "0" to "1". The output of both ACA cards is "1" while a card is in the read station. As the card leaves the read station the outputs of the gating diodes are changed from "1's" to "0's".

Signals which originate from the two gating diodes and the counter enable circuit are, the light probe, dark probe, advance pulses enabled signal, end of card pulse No. 1 and end of card pulse No. 2.

Read Register Gating Circuit

The Read register gating circuit (Figure 6) enables information to be gated to the Read register only if signals from the read diodes and the gating circuit coincide.

The enable signal is sent to the Read register if any one of the following conditions exist:

1. Light Probe -- A 3.5 usec. enable pulse is sent to the Read register when the leading edge of a card covers gating diode No. 1. All the primary read diodes will detect light at this time, therefore this enable pulse allows all Primary Read FF's to be set.
2. Dark Probe -- A 2 usec. enable pulse is sent to the Read register when the leading edge of a card covers gating diode No. 2. The Primary Read diodes will detect dark at this time, therefore the enable pulse allows all Primary Read FF's to be cleared.
3. Read Register Gating Pulses -- (Delay Timing Margin Switch Normal Position) 8 usec. enabling pulses at each clock count of 13 1/2 (TI-13 1/2 through T81-13 1/2)
(Delay Timing Margin Switch Test Position) -- Delays enabling pulses to clock count 15 1/2. The test position of the Delay Timing Margin switch is usually used in conjunction with the Advance Timing Margin switch.

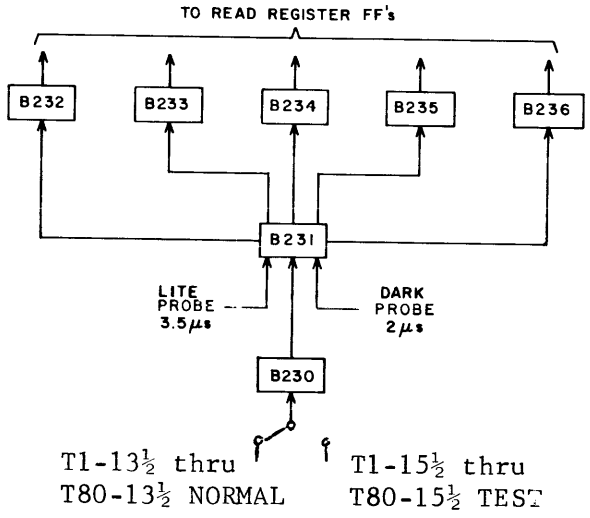


Figure 6 Read Register Gating Circuit

Compare Pulse Timing Circuit

The compare pulse timing circuit (figure 7) performs an enabling function to the preread error and compare error circuits.

If a preread or compare error is detected the appropriate FF will be set when the gating signal from the compare pulse timing circuit is received. The gating signal, therefore, serves a timing function. The times at which the signals exist are governed by the gating diode and counter inputs to the compare pulse timing circuit.

The timing and functions of the gating pulses are given on the following page.

1. Light Check Pulse - 1.5 usec pulse resulting from ANDing the light probe from the read register enable circuit, the output of the No. 1 gating diode and a delay capacitor. At this time both the Read register, which was set by the light probe, and the secondary read diodes should indicate light is detected.

2. Dark Check Pulse - a 10 us pulse at T1-13 from the clock counter: at this time both the Read register, which was cleared by the dark probe, and the secondary read station, which is covered by the card border, should indicate dark is detected.

3. Compare Enable Pulses (Advance Timing Margin Switch Normal Position) - 10 us pulses at each clock count of 13 (T2-13 thru T81-13). At this time the card column stored in the Read register is centered over the secondary read diodes. Outputs from the secondary read diodes are compared with the information stored in the Read register. If the outputs do not compare, the compare enable pulses allow the Compare Error FF to be set.

(Advance Timing Margin Switch test position)

- The Advance Timing Margin switch test position is usually used in conjunction with the Delay Timing Margin Switch as part of a maintenance procedure.

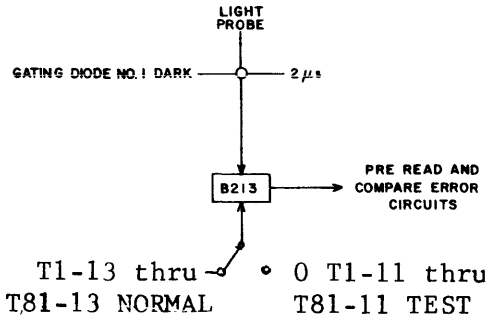


Figure 7 Compare Pulse Timing Circuit

COMPARE LOGIC

Preread error and compare error circuits compare outputs from the primary and secondary read stations. The preread error circuit is enabled until the counter reaches T1-13 1/2, and compares the outputs of the two read stations during the light and dark check pulses. The compare error circuit is enabled when the counter reaches T1-13 1/2 and compares the outputs of the two read stations at clock counts T2-13 through T81-13. The selection of the pre-read or compare error logic is performed by the select error f.f. (A100/101).

The preread error and compare error circuits share a common comparison circuit (figure 8). The set output of a Primary Read FF is ANDed with the output of the inverter of the corresponding secondary read diode. The clear output of the FF is ANDed with the M card of the corresponding secondary read diode. If any one of the AND gates in the comparison circuit are enabled at the time of a light check, dark check or compare pulse the preread error or compare error FF will be set.

Preread Error Circuit

The preread error circuit (figure 8) tests the read logic for light and dark detecting capability prior to reading each card. The Preread Error FF is set only when three conditions exist simultaneously:

1. The Select Error FF (A100/101) is cleared.

2. A light check pulse (1.5 us) or dark check pulse (10 us) is present.

3. A comparison error is present.

The Select Error FF is cleared when gating diode #2 is uncovered and is set at clock count T1-13 1/2. The Select Error FF disables the preread error circuit at T1-13 1/2.

The light and dark check pulses occur when all outputs from the comparison circuitry should indicate light or dark. The light check pulse takes place 2 μs after the leading edge of the card covers gating diode No. 1. The Read Register FF's should have been set by the light probe and all secondary read diodes should indicate light at this time. The dark check pulse occurs when the Read Register FF's have been cleared by the dark probe and the secondary read diodes are covered by the card margin. If all outputs do not indicate light or dark during the light and dark probes respectively the Preread Error FF will be set.

Setting the Preread Error FF in the manual mode stops all card feeding via a signal from the ready circuit and directs the card in the read station to the secondary receiving tray. The Preread Error light on the maintenance panel is lit. In the auto. mode a preread error results in a logical "0" to the adapter. A master clear signal clears the Preread Error FF and turns off the Preread Error light.

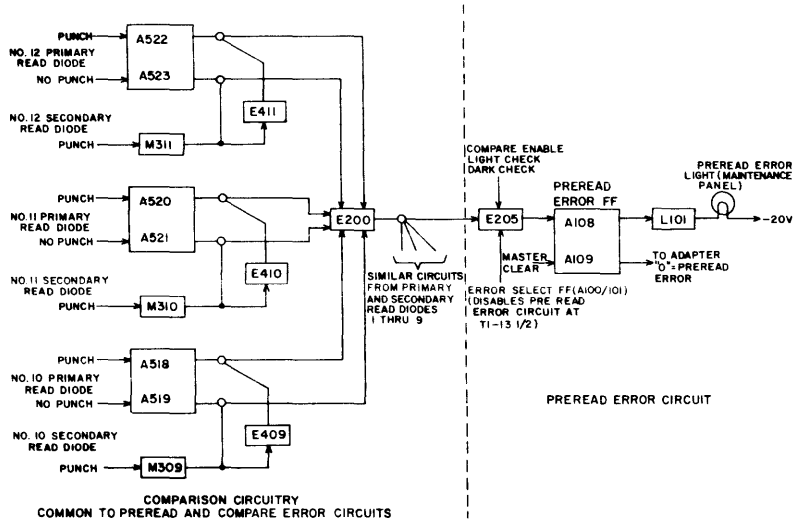


Figure 8 Comparison Circuitry and Preread Error Circuit

Compare Error Circuit

The compare error circuit (figure 9) is analogous to the preread error circuit in that it compares the outputs of the primary and secondary read diodes. This circuit however, is operative during card reading. At T2-13 through T81-13 10 us "0" pulses from the compare pulse timing circuit to E204 will result in a "1" to the Compare Error FF if a comparison error exists.

When the Compare Error FF is set in the auto. mode of operation a "0" to the adapter informs it of the error condition. In the manual mode setting the Compare Error FF results in:

1. A signal to the gate control circuit which directs the card to the secondary receiving tray.
2. A signal to the ready circuit which turns off the Ready light and disables all manual feed commands.
3. A signal to the brake control circuit to activate the card brake.

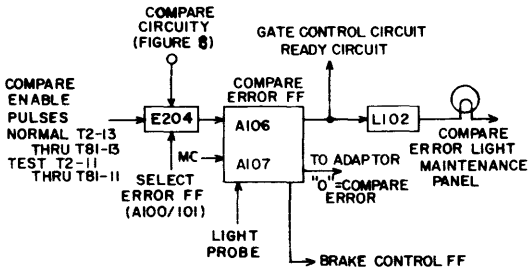


Figure 9 Compare Error Circuit

Resync Circuit

The resync circuit (figure 10) resynchronizes the clock counter for each column of holes punched in the card. This ensures that each card column (where at least one punch exists) will be centered over the primary read diodes at clock count 13 1/2.

The Resync FF is set only when three conditions exist simultaneously:

1. Any of the primary read diodes detect light.
2. The Counter Enable FF is set. This assures that the resync circuit is disabled between cards.
3. A transfer pulse is present. The transfer pulse enables the AND gate to the FF for 2 us.

Setting the Resync FF results in a 2 us pulse to RI of the counter which sets the count to seven. The contents in RI are immediately transferred to RII by the same transfer pulse which enabled the Resync FF. Therefore, the counter is set to a count of 7 1/2. Setting the counter at 7 1/2 when a column moves into the read station insures that at the time of the Read register enable pulses (count 13 1/2) the column will be centered over the primary read diodes.

The Resync FF is cleared between each card column when the primary read diodes are dark. All 12 primary read diodes must indicate dark simultaneously between resync pulses.

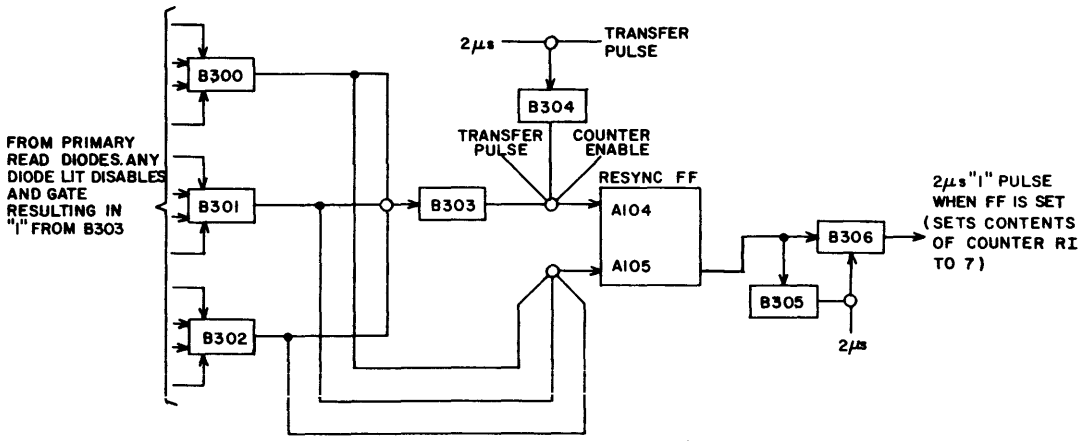


Figure 10 Resync Circuit

LOCAL CONTROL LOGIC

The Local Control Logic is divided into 4 sections:

A. Ready and Master Clear Circuit - informs the operator when a fault is detected and clears the Fault Detecting FF's by a signal received from the operator panel or the controller
B. Motion Control Circuits

    1. Feed Control Circuit - Receives manual or automatic feed commands to regulate the card brake which stops or starts card feed, and informs the operator of a fail-to-feed condition.
    2. The Gate Control Circuit - Receives manual or automatic gate commands and determines whether a card will be directed to the primary or secondary receiving tray.

C. Tray Status Circuits

    1. Jam or Receiving Tray Full Circuit - Detects a full condition in either of the receiving trays or a jammed card in the primary receiving tray.
    2. Input Tray Empty Circuit - In the automatic mode, this circuit informs the adapter when the last card has been taken from the input tray; in the MAN. mode, it disables all manual feed commands.
    3. End of File Circuit

D. Motor Power Status Circuit

Ready and Master Clear Circuit

The Ready and master clear circuit (figure 11) performs the following functions:

1. Signals the operator that a fault has been detected by one of the fault detecting circuits (compare error, preread error, jam or receiving tray full, input tray empty, or fail to feed).
2. Master clears all fault detecting FF's.
3. Disables all feed commands when a fault is detected in the manual mode.
4. Disables all internal gate commands and manual feed commands in the auto mode. In the manual mode the circuit enables all manual feed commands and internal gate commands.

When the unit is placed in the manual mode a 2 us "1" from D118 sets the Ready Inhibit FF (A200/201) and turns off the Ready Light on the operator panel. The "1" from D108 enables internal gate commands, partially enables all manual feed commands and forces a "0" from D109. The "0" from D109 informs the adapter that the unit is under manual control.

After the unit is placed in manual control the Ready switch must be pressed to fully enable manual feed commands. When the Ready switch is pressed "1's" from D116 and D111 clear the fault detecting FF's and the Ready Inhibit FF.

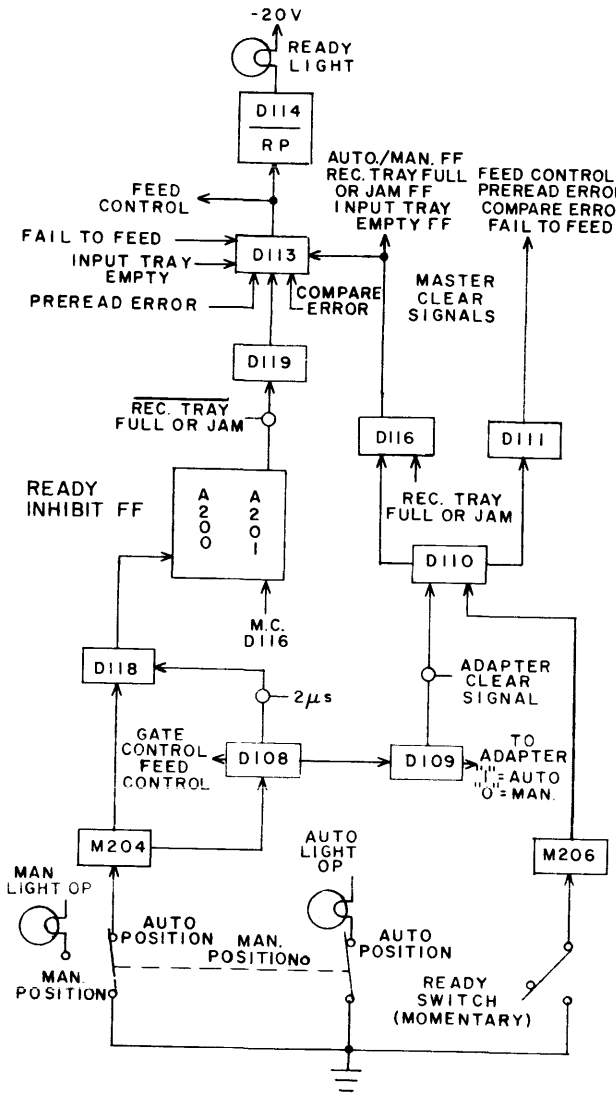


Figure 11 Ready and Master Clear Circuit

When the Ready switch is released the clear output from the Ready Inhibit FF fully enables all manual feed commands and lights the Ready light. If any of the fault detecting FF's are subsequently set, a "0" from D113 disables the feed commands and turns off the Ready light. The fault must then be corrected and the Ready switch pressed to continue card feeding.

In the auto mode the output of D108 is a steady "0", which disables internal gate commands and manual feed commands and puts these circuits under the control of the adapter. The "1" signal from D109 informs the adapter the unit is under automatic control and partially enables the AND gate at D110. An adapter clear signal fully enables the AND gate and clears the fault detecting FF's.

Motion Control Circuits

Feed Control Circuit. The feed control circuit (Figure 12) receives manual or automatic feed commands to regulate the card brake and start or stop card feeding. A 500 millisecond delay in card feeding sets the Fail to Feed FF and informs the controller of the feed failure.

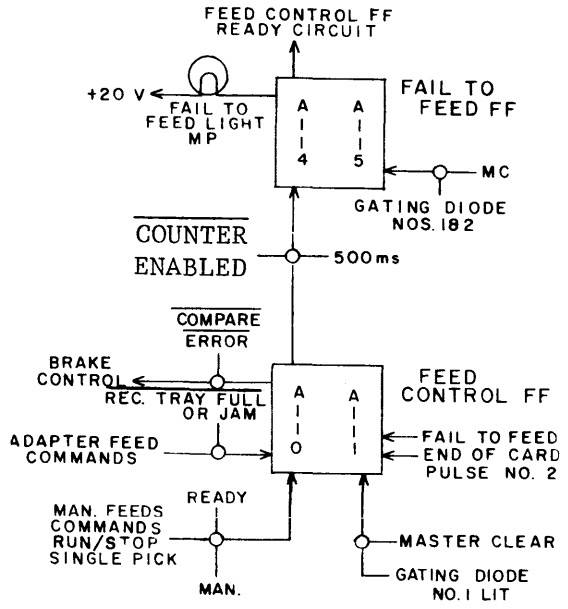


Figure 12 Feed Control Circuit

In the manual mode the feed commands may originate from either the Run/Stop switch or the Single Pick switch on the maintenance panel. When the Run/Stop switch is in the Run position and no faults are present the Feed Control FF is set. The resultant "1" to the brake control solenoid pulls the card brake from the card channel and allows a card to be fed. If the ready signal is dropped or the unit is placed in the automatic mode the set signal to the Feed Control FF is dropped and the FF is cleared by end of card pulse No. 2. When the FF is cleared the card brake solenoid is released and card feeding is stopped.

When the Single Pick switch is pressed, capacitor discharge sends a "1" pulse to the set side of the Feed Control FF. The FF is then cleared by end of card pulse No. 2 after one card has been read.

The Feed command from the adapter holds the Feed Control FF in the set state until the Feed command is dropped or the input is disabled from the receiving tray full or jam circuit. A compare error disables the input to the brake control circuitry and immediately stops card feeding.

When the Feed Control FF is set and no card is in the read station a capacitor is charged in the fail-to-feed circuit. A card entering the read station discharges the capacitor. A 500 millisecond interval between cards entering the read station allows the capacitor to charge to a level which allows the Fail-to-Feed FF to be set. Setting the Fail-to-Feed FF results in a "0" signal to the adapter informing it of the fail to feed condition. The "1"s from the Fail-to-Feed FF disable the manual feed commands via the ready circuit and clear the Feed Control FF. Thus in the manual mode a fail-to-feed condition releases the card brake and stops any subsequent card-feeding until the fault is corrected and the ready condition is reestablished.

Note that the manual feed commands are disabled from the ready circuit by any of a number of possible fault conditions. The auto-feed commands are disabled only by a jam condition at the primary receiving tray or when this tray is full.

Card readers above serial 110 have an additional output from the Feed Control FF which controls the vacuum level at the capstan. When card feeding is interrupted and the Feed Control FF is cleared a capacitor is charged. If card feeding is not resumed for 1.3 seconds the capacitor charges to a level which enables a solenoid to be activated. Activating the solenoid reduces the vacuum to the card capstan.

Gate Control Circuit. The gate control circuit (Figure 13) directs cards to the primary or secondary receiving tray. Normally the Gate Control FF is cleared and cards are directed to the primary receiving tray. When the Gate Control FF is set a solenoid is activated and the card is directed to the secondary stacker.

Both inputs to the Gate Control FF are partially enabled for 2 usec after each card by end of card pulse no.2. A "1" input to D103 at this time will set the FF and the card will be sent to the secondary receiving tray. The following conditions will set the Gate Control FF:

In the manual mode of operation:

1. A pre-read error
2. A compare error
3. The Gate switch on the maintenance panel is pressed.

In the automatic mode of operation:

1. The adapter sends a "1" gate signal
2. The Gate switch on the maintenance panel is pressed.

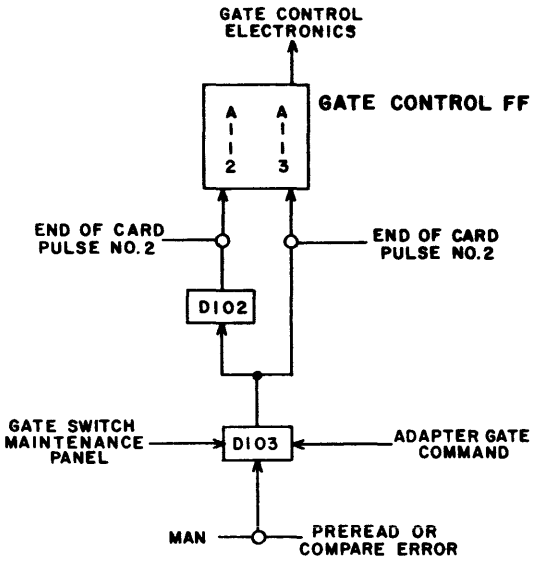


Figure 13 Gate Control Circuit

Tray Status Circuits

Input Tray Empty Circuit. The input tray empty circuit (Figure 14) disables all manual feed commands and informs the controller when the last card has been taken from the input tray.

A mechanical and a vacuum switch detect the input tray empty condition. The mechanical switch is actuated when the last card is pulled from the

input tray. The vacuum switch is actuated when the trailing edge of the card leaves the delivery capstan, causing vacuum to drop to approximately 1 inch of mercury.

The Input Tray Empty FF may be set in two ways:

1. When both the vacuum and mechanical switches are actuated.
2. When the mechanical switch is actuated and the leading edge of the last card covers gating diode No. 2.

With the first method it is not necessary for any cards to be read before an input tray empty condition is sensed. The second method insures that the FF will be set before reading the first column of the last card, although capstan vacuum has not dropped to one inch of mercury at this time.

When the Input Tray Empty FF is set, the Ready indicator on the operator panel is extinguished and all manual feed commands are disabled. The clear side outputs of the Input Tray Empty FF tell the adapter that the input tray is empty.

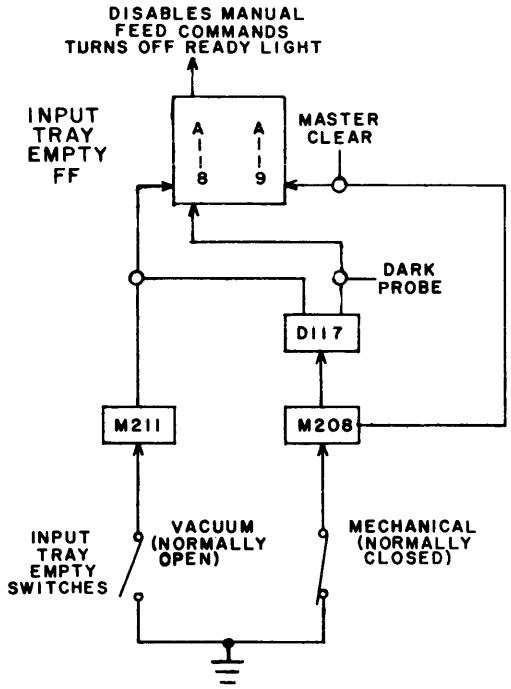


Figure 14 Input Tray Empty Circuit

Jam or Receiving Tray Full Circuit. This circuit (Figure 15) detects a full condition in either of the receiving trays or a jammed card in the primary receiving tray. Any one of these conditions sets the Jam or Receiving Tray Full FF. One output informs the controller of the existing condition. The other two outputs disable automatic feed commands and turn off the Ready light.

When either of the receiving trays is full, a mechanical switch within the tray is toggled, forcing a "1" from M209. The output from M209 partially enables the AND gate to the set side of the FF.

A card jam in the receiving tray is detected by a photo voltiac cell, located above the entrance to the tray. Light is directed to the diode from the floor of the receiving tray. Normally, light cannot reach the photocell. However, a crumpled card allows the photocell to be illuminated and a "1" is forced from M209 which partially enables the input to the set side of the Jam or Receiving Tray Full FF. The Jam or Receiving Tray Full FF will be set when a card enters the read station and the output of M209 is a "1".

The Jam or Receiving Tray Full FF, when set:

1. Sends a "0" to the adapter, informing it that the card in the read station will be the last one delivered.
2. Disables the AUTO feed command to the Feed Control FF.
3. Forces a "0" from D113 (ready circuit) which turns off the Ready indicator on the operators panel and disables all automatic feed commands.

Note that motion is stopped after the card in the read station is read.

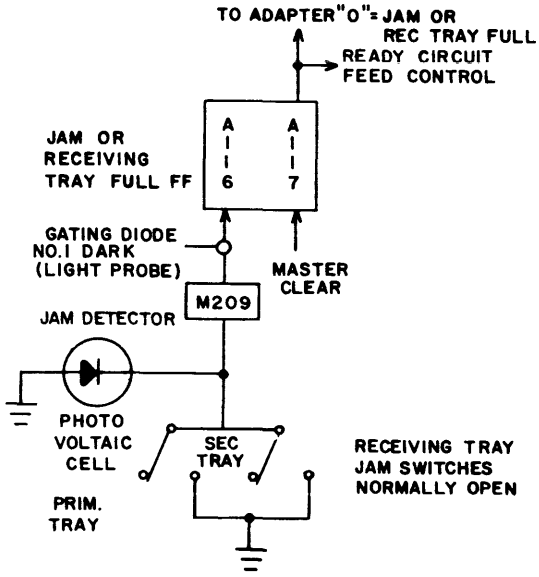


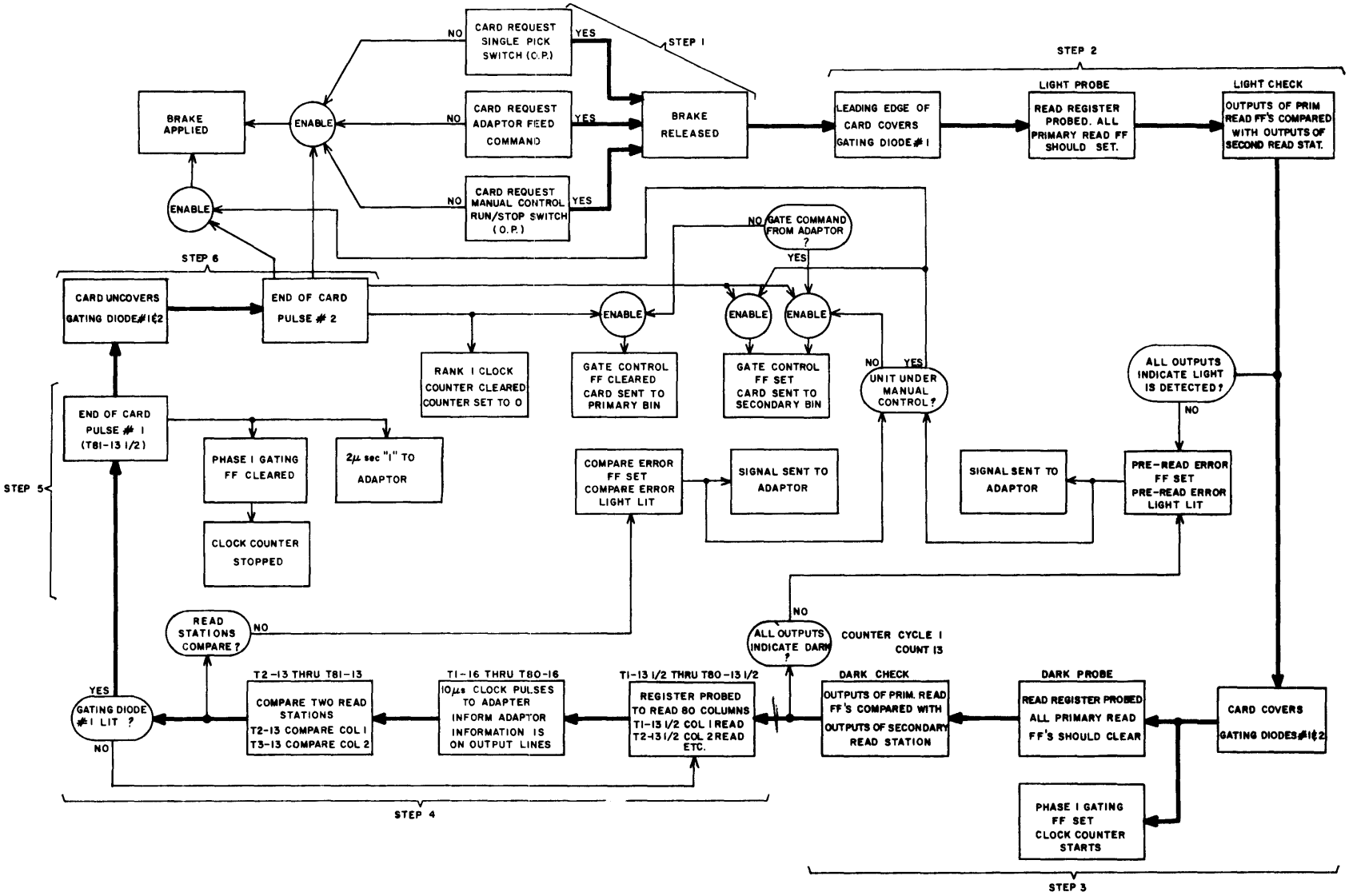
Figure 15 Jam or Receiving Tray Full Circuit

End of File Circuit. When the End of File switch on the operators panel is depressed the End of File indicator is lit and a logical "0" is sent to the controller. This signal remains present until the switch is again depressed.

Normally, the end of file circuit is used to indicate when the last group of cards in a file are being run or when the last card of a file has been fed through the machine. This circuit sends a signal to the controller for use in external programming.

Motor Power Status Circuit

The motor power status circuit sets the Fail to Feed FF and the Compare Error FF when motor power is off. When the unit is in the automatic mode of operation, the controller is informed by a logical "0" that motor power is off.



FLOW CHART OF CARD MOVEMENT

POWER SUPPLY AND DISTRIBUTION

The power supply chassis is located immediately behind the left front cabinet door and requires 208 volts, 3-phase primary power from a 10-amp service line. Full wave rectifier circuits provide -21, -20, +20 and miscellaneous DC operating voltages required for Reader operation. AC power required by the various motors and card tray vibrators (as well as many DC voltages) are applied via relay contacts to provide sequenced distribution. The front panel of this chassis contains 12 circuit breakers, a toggle switch, power indicator lamps and test points, and a dual convenience outlet (see power supply schematic in the maintenance aids manual).

Main circuit breaker CB06 (Main Power) is used in closing the 3-phase service lines to the chassis. When primary power is present, indicators DS505, DS504 and DS503 (Phases 1, 2 and 3) become illuminated. One hundred-ten VAC also becomes available at the dual convenience outlet, which provides operating power for auxiliary lighting facilities, test equipment, etc.

Assuming that all other circuit breakers at the power panel are in the up or closed position, the following power distribution sequence is initiated:

1. 110 VAC applied to convenience outlet.

2. Primary winding of transformer TO2 energized (Minus 21 volt supply).

3. Minus 21 volt power applied to one pole of Main Power switch via closed contacts of CB01A, CB02A and CB05C.

MAIN POWER SWITCHPLATE PRESSED:

1. Relay K01 becomes energized, holds in through toggle action of Main Power switch.

2. Contacts of K01 close to apply power to primary winding of T01 (plus and minus 20-volt supply).

   a. Read station excitor lamp illuminated.

   b. Jam detector excitor lamp illuminated.

   c. Plus and minus 20-volt operating power applied to logic chassis.

   d. Contacts close to energize fan motors of cabinet cooling system, through contacts of circuit breaker CB05.

MOTOR POWER SWITCHPLATE PRESSED (ON).

1. Relay K02 energizes through series circuit formed by the jam detector switches and closed contacts of relay K501. Relay K02 remains energized through holding contacts.

2. Contacts of relay K02 close in -21 volt power circuit.

   a. RC circuit of K501 charges.

   b. Motor Power indicator becomes illuminated.

   c. Minus 21 volts applied to card gate and brake coil circuits.

   d. Vibrator units energized.

   e. Relay K03 energized.

      (1) Contacts close to apply three phase operating power to pump motor.

      (2) Single phase power applied to capstan motor, running time meter, and spring bias motor.

      (3) Contacts close in relay K04 coil circuit.

   f. Relay K04 energized.

      (1) Contacts close to apply 3-phase operating power to drive motor.

      (2) Contacts open which removes the constant set condition from the Fail to Feed and the Compare Error FF's.

MOTOR POWER SWITCHPLATE PRESSED (OFF)

1. Relay K501 energized and held through its own contacts.

   a. Contacts open to break continuity in relay K02 circuit - relay de-energized.

      (1) Contacts close which sets Fail to Feed & Compare Error FF's.

      (2) Contacts open to remove power from vibrator circuits.

      (3) Contacts open in -21 volt supply line.

         (a) Motor Power indicator becomes extinguished.

         (b) RC circuit used with K501 discharges through bleeder resistor.

         (c) Power removed from card gate and brake coil circuits.

         (d) Relay K03 de-energized:
         Contacts open to remove power from pump motor, capstan motor, running time meter, and spring bias motor.

         (e) Relay K04 de-energized:
         Contacts open to remove power from drive motor.

MAIN POWER SWITCHPLATE PRESSED (OFF)

1. Relay K01 de-energized.

    a. Contacts open to remove primary power from the plus and minus 20-volt power circuit.

    b. Contacts open to remove operating power from blower motors of cabinet cooling system.

In order to better understand the logical operation of the 405 Card Reader the following sequence will consider a single card read operation. It will be assumed that the manual control switches on the operator panel will be in the following condition:

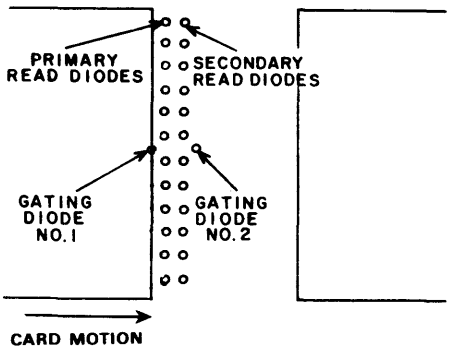
A. Main Power - On
B. Motor Power - On
C. Auto./Manual-Manual Position
D. End of File - Off
E. Ready - On
F. Single Pick - Pressed and released
G. Run/Stop - Stop Position

Cards are loaded into the Input Hopper with the first card of the deck resting against the brake.

Single Pick Operation (Manual Made)

1. 405 is in the Ready condition
2. Press and release the Single Pick switch
3. Set the Feed Control F/F
4. Brake solenoid is energized by D101
5. Card is now in motion
6. Card enters the read station covering GD#1:

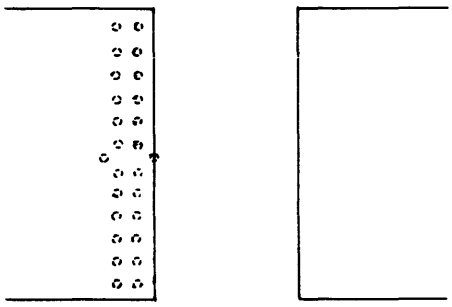
Gating Diode No. 1 Covered



a. 3.5 usec pulse from B200 (Lite Probe) -- Initiates a preread check of read logic, preamps and primary and secondary diodes
   1. Primary Read Register will set
   2. Secondary read station is compared with the primary read register (lite check)
b. The input AND gate to the Counter Enable FF is partially enabled

7. Both read stations and G.D.#2 are covered:

Gating Diode No. 2 Covered.

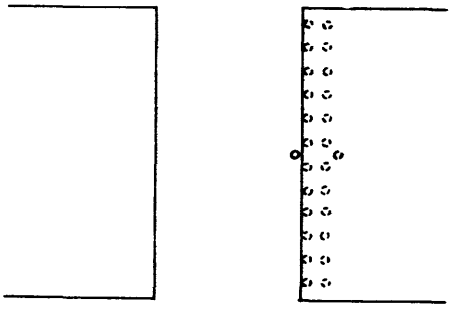


a. 2 usec pulse from B201 (Dark Probe) -- Initiates a check of the dark detecting ability of the photo diodes and preamps.
   1. Primary Read Register will clear.
   2. Counter Enable FF will set by the first transfer pulse from the Clock Counter circuit. This enables the Clock Counter to count Advance and Transfer pulses.
   3. Clear is dropped to the Rank I Clock Counter FF's.
   4. Disable Fail to Feed delay.

8. T1-7·5 Resync - Counter will be forced to a count of 7·5 if Column 1 contains data.
9. T1-13 Compare Time - Dark check will compare the secondary read station with the primary read register. If an error is detected the Pre-Read Error F/F will set causing the 405 to go Ready.
10. T1-13·5 Read - Probe
    a. Set Select Error F/F disabling Pre-Read Error Circuit and enabling the Compare Error Circuit.
    b. Column #1 is gated into the Primary Read Register.
11. T1-16 Column Pulse - Data word is transferred to the computer via the 3248 controller.
12. T2-0 Counter Recycles.
13. T2-7·5 Resync - Counter is forced to 7·5 if column 2 contains data.
14. T2-13 Compare Time - column 1 data is compared. If an error occurs the Compare Error F/F is set and the 405 goes Ready.
15. T2-13·5 Read Time - Column 2 is gated to the Primary Read Register.
16. T2-16 Column Pulse - Data word is transferred to the computer via the 3248 controller.
17. Repeat steps 12-16 to read the remaining columns on the card.
18. T81-0 Counter Recycles.
19. T81-7·5 Counter does not resync because the margin at the end of the card is now covering the Primary Read Station.

20. Gating Diode#1 is uncovered as the card moves off the read station:

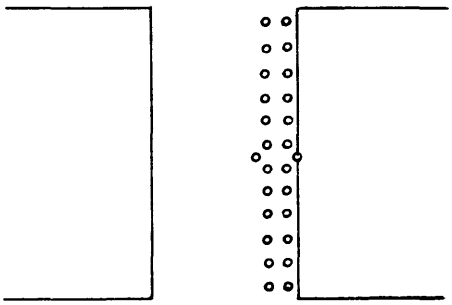
    Gating Diode No. 1 Uncovered.



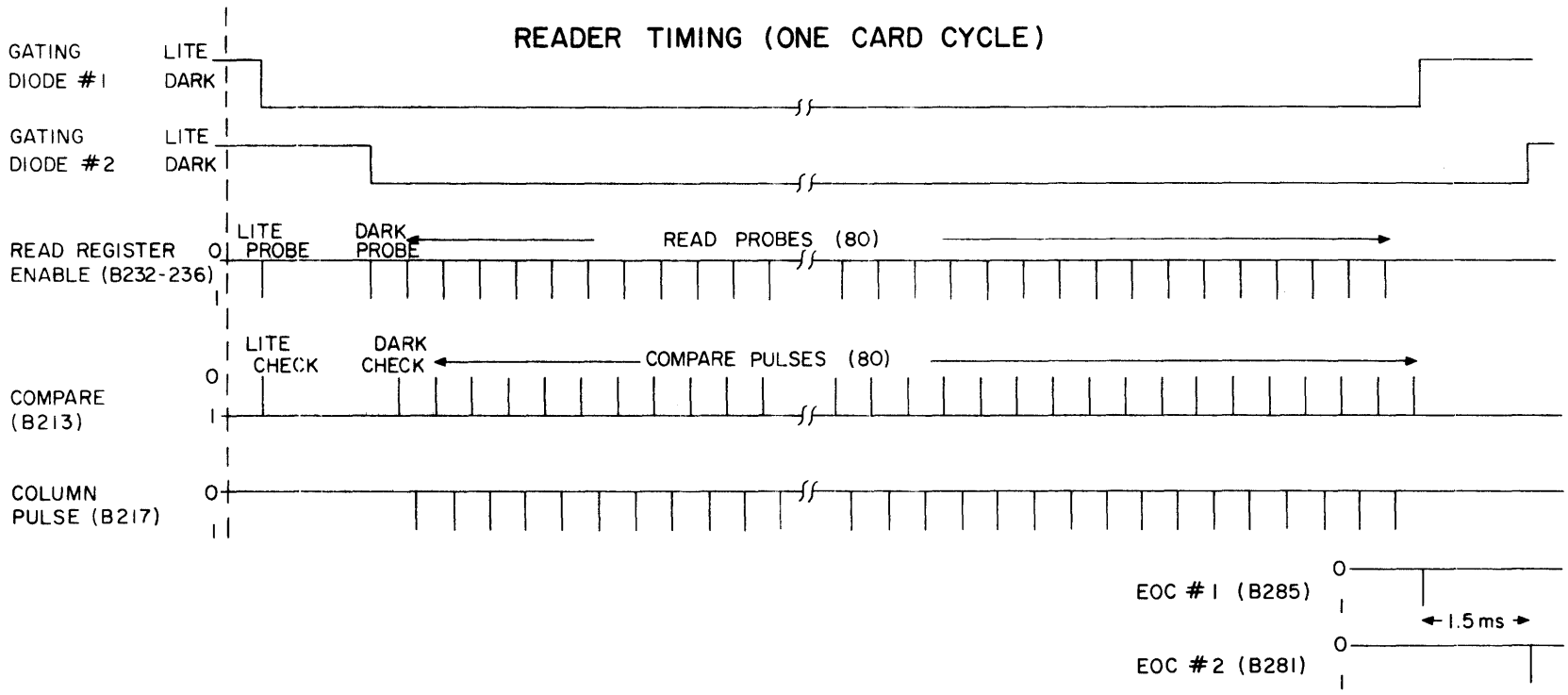
21. T81-13 Compare Time - 80th column of data is compared.
22. T81-13.5 Read Time:
    a. Clear Primary Read Register.
    b. End of Card Pulse#1 (B281):
        1. Clears Counter Enable FF which stops the Clock Counter.
        2. 2 usec "1" to the controller informing it that the card is out of the read station.

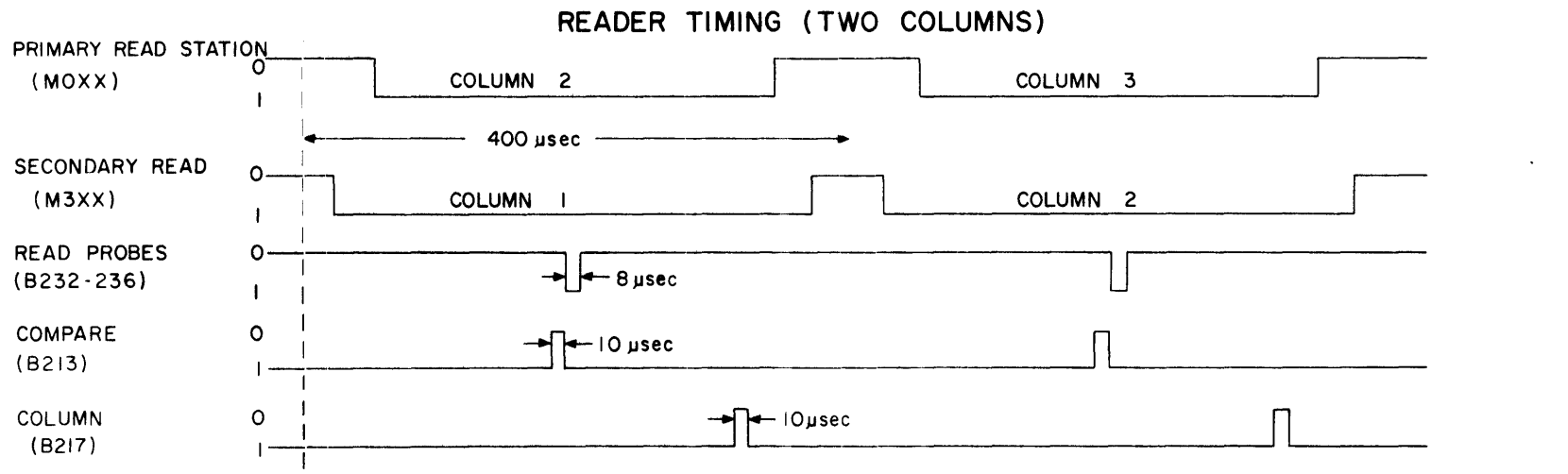
23. Gating Diode#2 is uncovered 1.5 milliseconds after the 80th column is read.

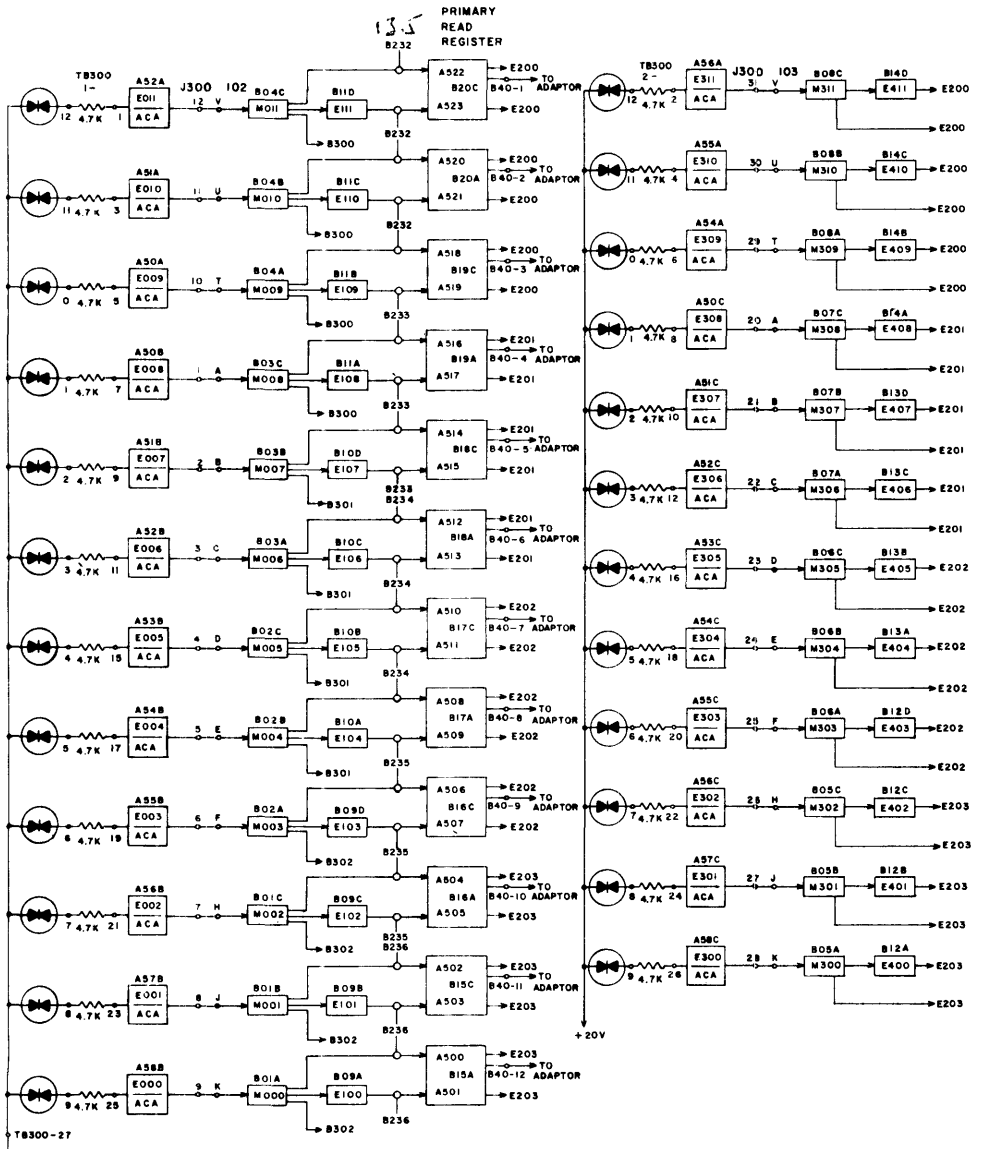
    Gating Diode No. 2 Uncovered.



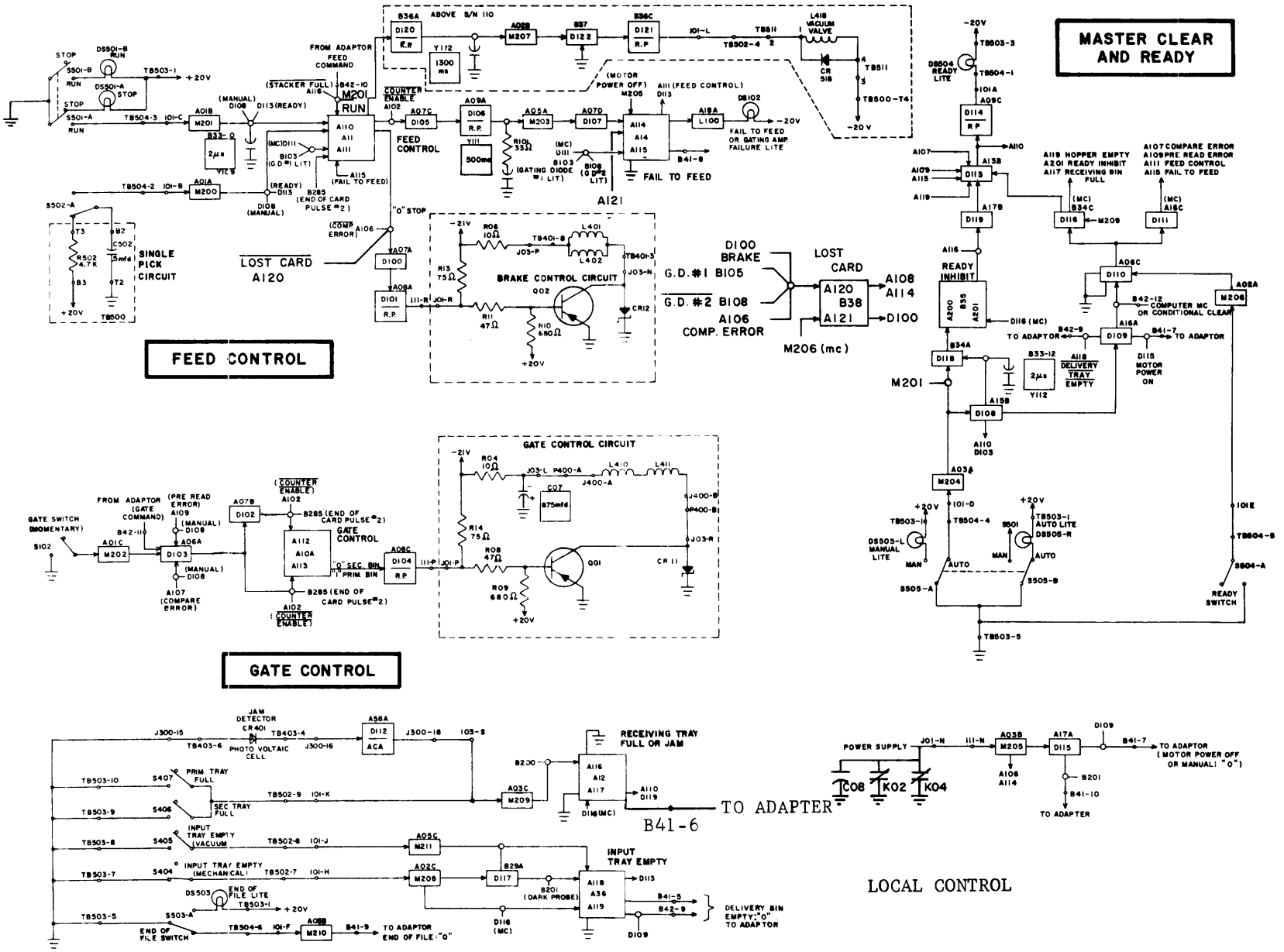
    a. Counter Enable FF is held clear.
    b. Rank I Clock Counter FF's are cleared (Rank II will clear on the next transfer pulse).
    c. End of Card Pulse#2 (B285 - 2usec "1"):
        1. Clears Feed Control FF.
        2. Enables Gate Control circuit to activate the gate if it is selected.

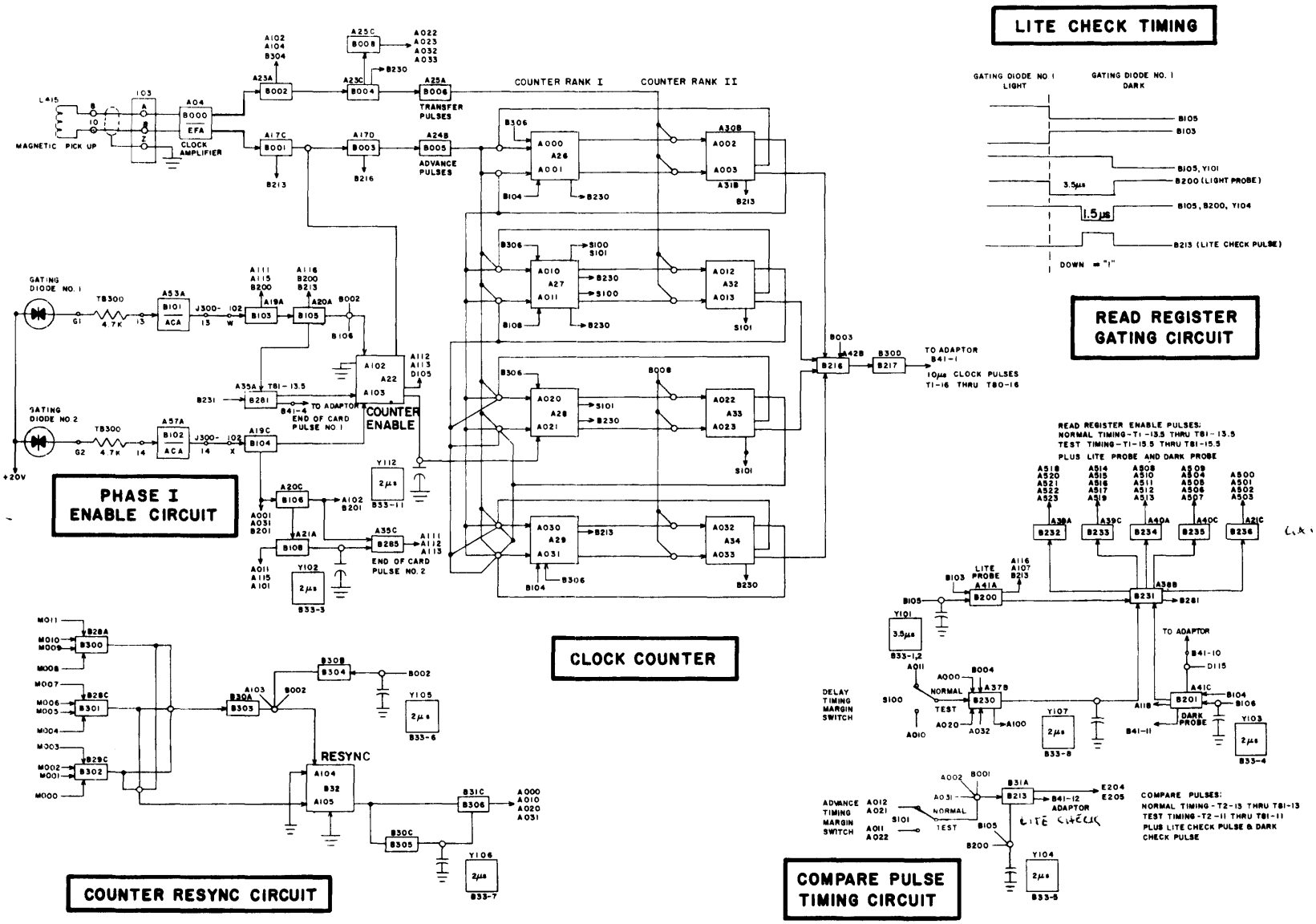

READER TIMING (ONE CARD CYCLE)
GATING DIODE #1
LITE
DARK
GATING DIODE #2
LITE
DARK
READ REGISTER ENABLE (B232-236)
0
LITE PROBE
DARK PROBE
READ PROBES (80)
COMPARE (B213)
0
1
LITE CHECK
DARK CHECK
COMPARE PULSES (80)
COLUMN PULSE (B217)
0
EOC #1 (B285)
0
1.5 ms
EOC #2 (B281)
0


READER TIMING (TWO COLUMNS)
PRIMARY READ STATION (MOXX)
0
COLUMN 2
COLUMN 3
400 µsec
SECONDARY READ (M3XX)
0
COLUMN 1
COLUMN 2
READ PROBES (B232-236)
0
8 µsec
COMPARE (B213)
0
10 µsec
COLUMN (B217)
0
10µsec

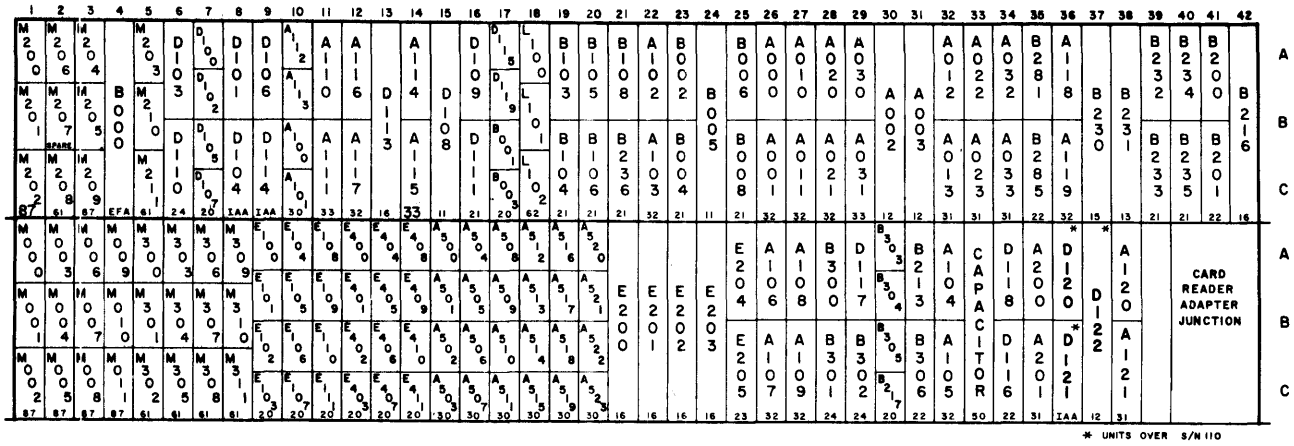


READ AND COMPARE

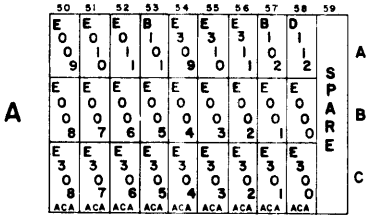

FEED CONTROL
MASTER CLEAR AND READY
GATE CONTROL
LOCAL CONTROL
SINGLE PICK CIRCUIT
LOST CARD A120
BRAKE CONTROL CIRCUIT
GATE CONTROL CIRCUIT
FEED CONTROL
FAIL TO FEED
READY INHIBIT
M206 (mc)
TO ADAPTOR
RECEIVING TRAY FULL OR JAM
INPUT TRAY EMPTY
DELIVERY BIN EMPTY: "0" TO ADAPTOR
END OF FILE SWITCH
POWER SUPPLY
READY SWITCH



TIMING LOGIC



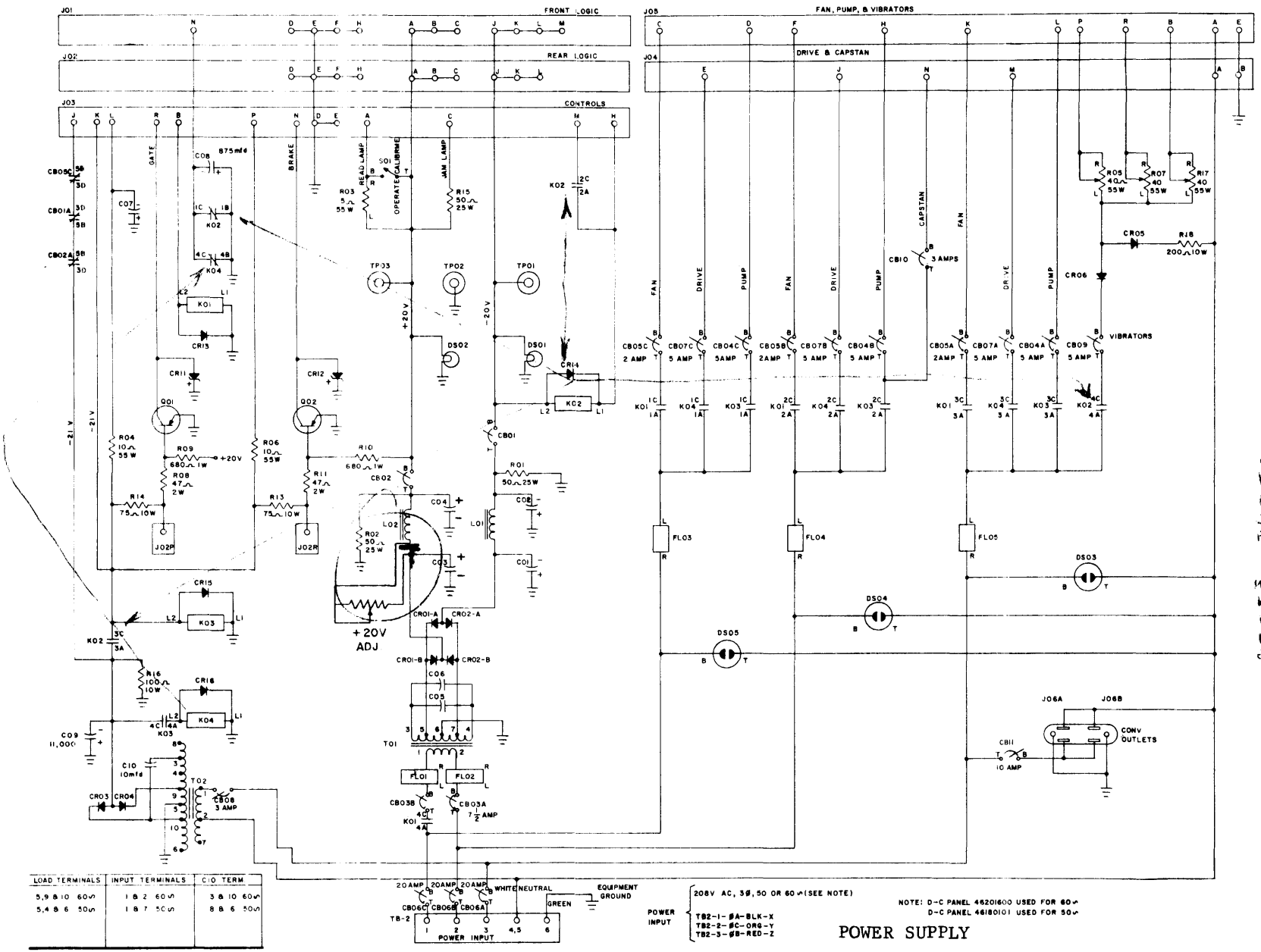
READ STATION



TYPE	QUANTITY	TYPE	QUANTITY	TYPE	QUANTITY
11	2	30	7	IAA	3
12	3	31	5	13	1
15	1	32	9	ACA	9
16	6	33	2	TOTAL	88
20	9	50	1		
21	8	61	7		
22	4	62	1		
23	1	87	5		
24	3	EFA	1		

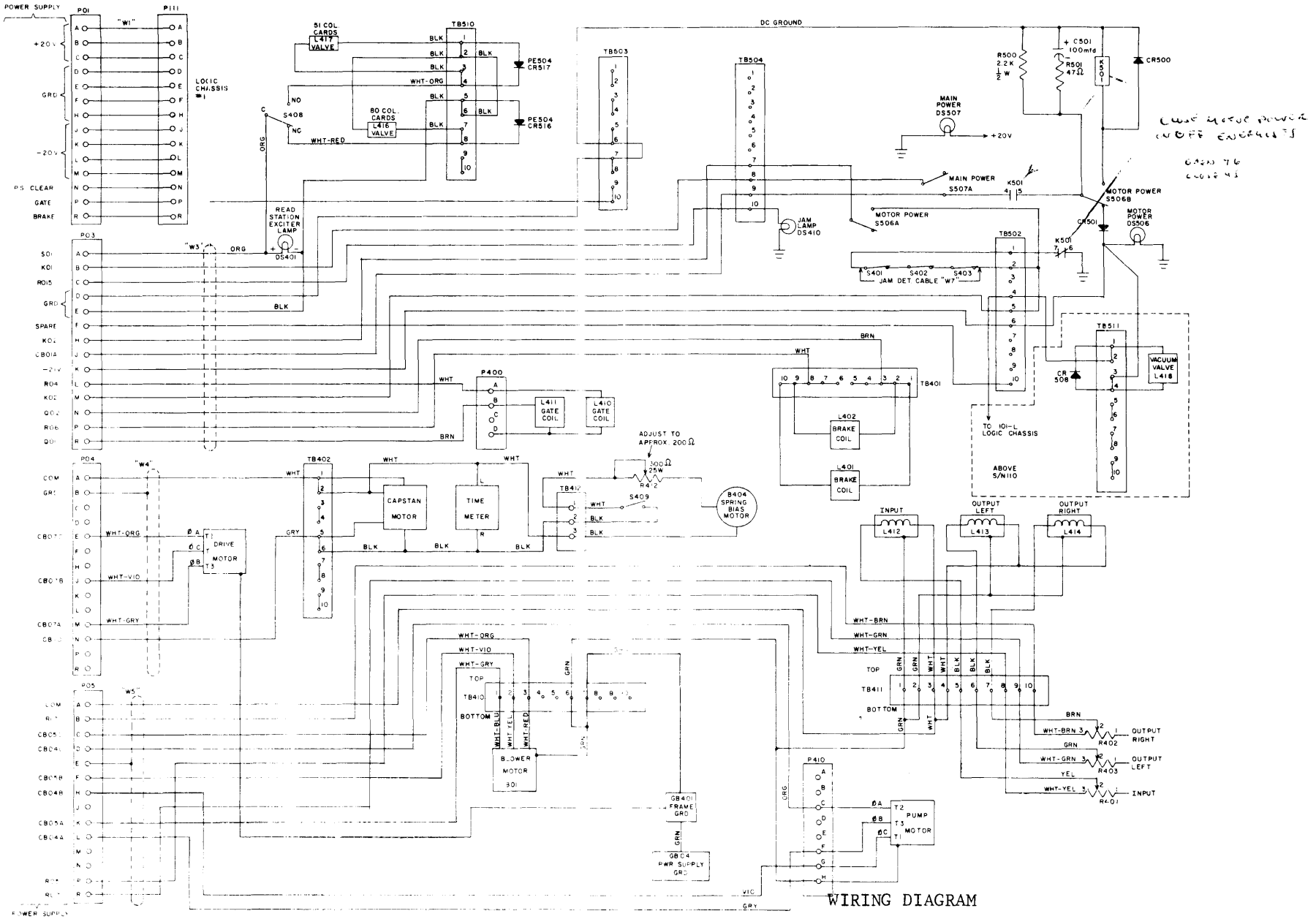
CARD PLACEMENT CHART

7. RESYNCH
13. CHECK
12. STATE
16. READ NEXT
0.

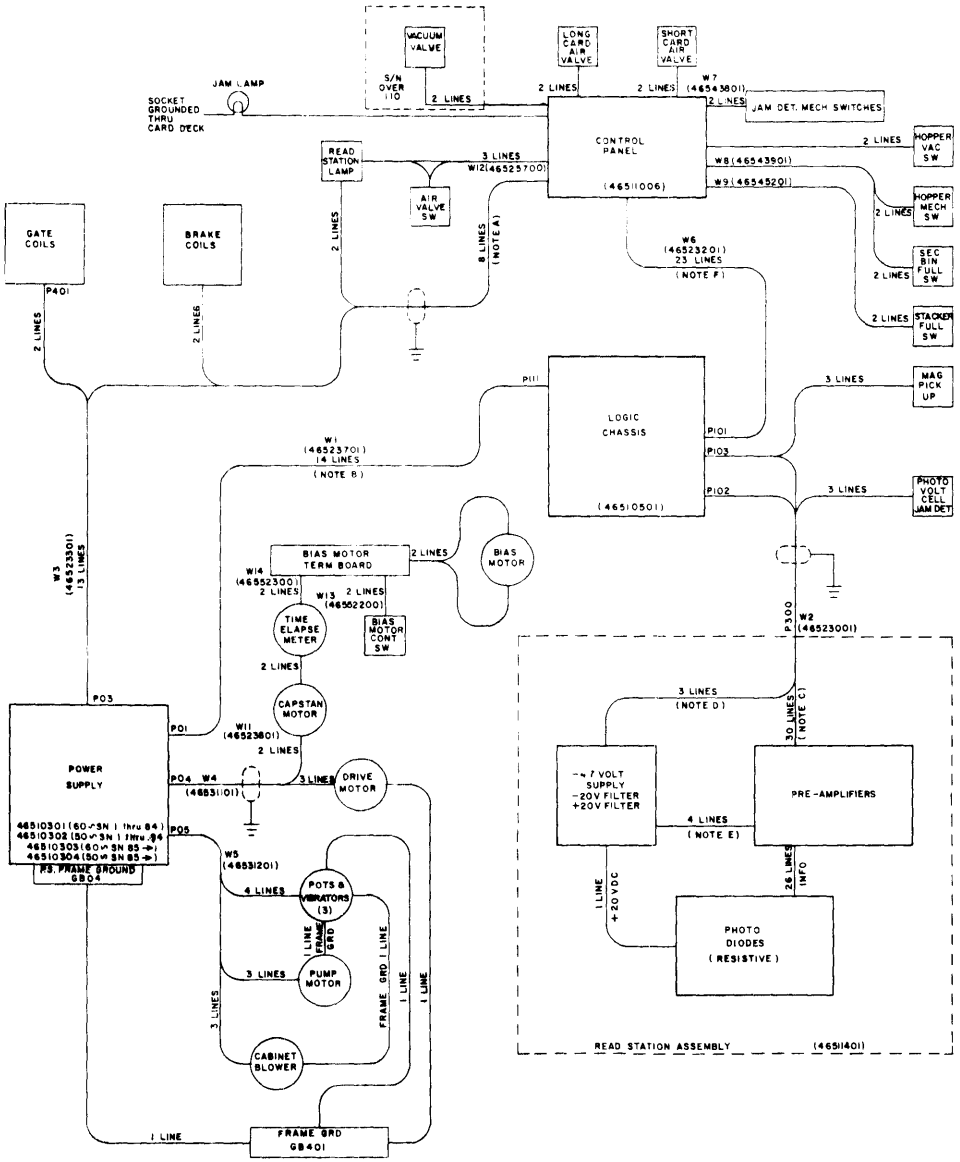


LOAD TERMINALS	INPUT TERMINALS	C10 TERM
5,9 & 10 60 ~	1 & 2 60 ~	3 & 10 60 ~
5,4 & 6 50 ~	1 & 7 50 ~	8 & 6 50 ~

POWER SUPPLY



WIRING DIAGRAM



A: 1 LINE FOR JAM LAMP VOLTAGE (2.3 V)
2 LINES FOR POWER ON OFF SWITCH
1 LINE FOR -21V IN MOTOR POWER ON OFF CIRCUIT
2 LINES FOR MOTOR POWER ON OFF
1 LINE FOR CABLE SHIELD
1 LINE FOR SHIELD & SENSING SW GRD
8 LINES TOTAL

B: 3 LINES +20V
4 LINES GRD
4 LINES -20V
1 LINE MASTER CLEAR
1 LINE GATE SIGNAL
1 LINE BRAKE SIGNAL
14 LINES TOTAL

C: 2 LINES JAM DETECTOR INPUT
1 LINE JAM DETECTOR OUTPUT
24 LINES INFORMATION
2 LINES GATING DIODES
1 LINE JAM DETECTOR SHIELD GRD
30 LINES TOTAL

D: 1 LINE -20V
1 LINE GRD
1 LINE +20V
3 LINES TOTAL

E: 1 LINE - 20V
1 LINE +20V
1 LINE GRD
1 LINE BIAS VOLTAGE (-4.7V)
4 LINES TOTAL

F: 11 LINES SPARE
1 LINE MECH HOPPER SWITCH
1 LINE VACUUM HOPPER SWITCH
1 LINE STACKER SWITCHS
1 LINE -20V
1 LINE +20V
1 LINE GRD
1 LINE READY LITE
1 LINE SINGLE PICK
1 LINE RUN/STOP
1 LINE MAN / AUTO
1 LINE CLEAR
1 LINE END OF FILE
23 LINES TOTAL

CABLING DIAGRAM

PRACTICAL APPLICATION EXERCISES

EXERCISE I: COMPONENT LOCATION

1. Reference: Punched Card Equipment Training Manual

2. Equipment: 405 Card Reader

3. Procedure: Remove the top and side covers from the machine. After removal, make a thorough study of the general construction of the machine.

Component	Location	Function
Main Power Switch		
Motor Power Switch		
Auto/Manual Switch		
End of File Switch		
Ready Switch		
Single Pick Switch		
Run/Stop Switch		
Advance Switch (Logic Chassis)		
Delay Switch (Logic Chassis)		
Operate/Calibrate Switch (Power Supply)		
Vacuum Capstan		
Input Tray Empty Switch (Mechanical)		
Input Tray Empty Switch (Vacuum)		
Card Throat		
Electro-Magnetic Brake Assembly		
Read Station Assembly		
Accept/Reject Gate		
Turn Around Assembly		
Vibrators		

Component	Location	Function
Vibrator Rheostats		
Voltage Test Points (Power Supply)		
Vacuum Relief Valves		
Pump Motor		
Carbon Vane Pump		
Cabinet Cooling Fan		
Bias Motor & Control Switch		
Bias Motor Adjustment		
Input Tray Back-Up Arm Drum Adjustment		
Air Pressure Valves for 51 & 80 Column Cards		
Switch for 51 and 80 Column Card Air Pressure Valves		
Magnetic Pick-up Assembly		
Relay K501		
Pressure Gauge		
Power Supply		
Cable Connections		
Main Drive Motor		
Drive Belt Assembly		
Drive Clutch		
Pinch Roller & Timing Wheel		
Capstan		

b. Set up the machine to read 51 column cards:

1. Unfasten the lock screws on the supply and receiving trays and turn so that the lip edge is positioned on the inside of the tray.
2. Open the 51 column stops in the Primary and Secondary Stacker Trays.
3. Observe the action of the machine:
    a. In Continuous (Free Run) Mode. At random, depress the Gate Switch on the Maintenance Panel and observe the gating action on card movement.
    b. In Single Pick Mode.

c. Set up the machine to read 80 column cards:

1. Unfasten the lock screws on the supply and receiving trays and turn so that the lip edge is positioned on the outside of the tray.
2. Close the 51 column stops in the Primary and Secondary Stacker Trays.
3. Observe the action of the machine:
    a. In Continuous (Free Run) Mode. At random, depress the Gate Switch on the Maintenance Panel and observe the gating action on card movement.
    b. In Single Pick Mode.

EXERCISE II: WAVEFORM ANALYSIS

1. Reference: 405 Reference Manual

2. Equipment: 405 Card Reader and Oscilloscope

3. Procedure: Connect scope leads to the appropriate location in the logic rack and observe the waveforms on the scope.

   a. Read Register Probe.

      1. Sync on M011 (B04C) and look at M011 on Channel A.

      2. Look at B231 (A38B) on Channel B.

      3. Mode: Alternate.

      4. The Read Register Probe should fall within 50 usec of the center of Read Diode #12. Depress the Delay Margin Switch and note the direction that the Probe pulse moves.

      5. Sync and look at M000 and repeat the above step.

   b. Magnetic Pick-up (It is not necessary to feed cards).

      1. Sync on B000 (A04B) and look at the same on Channel A.

      2. Look at B000 (A04D).

      3. Mode: Alternate.

   c. End of Card Pulse #1 (Free Run read the test cards).

      1. Sync and look at B281 (A35A) on Channel A.

      2. How long is the pulse? Why?

   d. End of Card Pulse #2 (Free Run read the test cards).

      1. Sync and look at B281 (A35A) on Channel A.

      2. Look at B285 (A35C) on Channel B.

      3. End of Card Pulse #2 (Channel B) should occur approximately 1.7 msec after End of Card Pulse #1 (Channel A).

e. Light Probe Pulse (Free Run read the test cards).

1. Sync and look at B200 (A41A) on Channel A.
2. Look at B231 (A38B) on Channel B.
3. B231 should output a 3.5 usec "0". Why?

f. Light Check Pulse (Free Run read the test cards).

1. Sync and look at B200 (A41A) on Channel A.
2. Look at B213 (B31A) on Channel B.
3. B213 should output a 1.5 usec "0". Why?

g. Dark Probe Pulse (Free Run read the test cards).

1. Sync and look at B201 (A41C) on Channel A.
2. Look at B231 (A38B) on Channel B.
3. B231 should output a 2 usec "0". Why?

h. Dark Check Pulse and Compare Pulse (Free Run read).

1. Sync and look at B213 (B31A).
2. B213 should output a 10 usec "0". Why?

i. Read Probe (Free Run read)

1. Sync and look at B230 (A37B) on Channel A.
2. Look at B231 (A38B) on Channel B.
3. B231 should output an 8 usec "0". Why?

j. Column Pulse (Free Run read).

1. Sync and look at B217 (B30D)
2. Each pulse should be a 10 usec "0". Why?

k. Resync Pulse (Free Run read).

1. Sync and look at B306 (B31C) on Channel A
2. Look at B002 (A23A) on Channel B.
3. Note 16 pulses on Channel B to one pulse on Channel A.

EXERCISE III: MAINTENANCE PROCEDURES

1. Reference: 405 Reference Manual

2. Equipment: 405 Card Reader and Basic 405 Tool Kit

3. Procedure: The following electronic/mechanical adjustments are to familiarize trainees with the 405 card reader operation and allow them to gain enough experience to provide reliable maintenance of the 405 in the field. Reference to the maintenance procedures in the 405 Reference Manual will be made at the end of each adjustment to provide additional information

a. Position of Brake Assembly

1. With power off remove Feed Control FF at A11.
2. Loosen three mounting bolts on brake assembly and two screws on throat plate.
3. Remove upper card guide.
4. Turn on power and press ready to energize brake solenoid.
5. Insert .016 inch feeler gauge between brake shoe and card plate. (Fine adjustment will be made in step 10)
6. Set one inch (15/16 for machines below S.N. 163 without ENC 135) between the throat plate and left end of capstan slots. Insure that the throat plate is at 90° to the card plate.
7. While holding the brake assembly in place, tighten the mounting bolts and re-check steps 5 and 6.
8. Using special tool #84-0512, set the throat plate up for a .010 inch gap.
9. While manually rotating the capstan, check that the minimum

gap is .0095 inches and maximum gap is .0115 inches.

10. Loosen the lock nut at the front of the brake shoe tension spring and turn the adjusting screw to obtain .016 (+.002 inch) gap.

NOTE: The purpose of the following steps is to adjust the brake release time so that it is a maximum of 3ms.

b. Brake Start/Stop Time

1. Tape input tray empty switch closed to simulate ready condition.
2. Loosen lock nut on tension spring adjustment shaft on brake and adjust until brake shoe can no longer be pulled back. To monitor this, engage SINGLE PICK and READY.
3. Back off tension adjusting screw 2-3 turns.
4. To check adjustment, place 405 in MANUAL and RUN. After cycling several cards, engage STOP and look between read station assembly and capstan assembly. The card should be stopped with columns 4-9 visible (only 3 columns will be visible, but the card should not stop with less than column 4 or more than column 9 visible). Repeat cycling to insure consistent brake operation. If not, adjust tension spring accordingly.
5. Mark card stopped in step 4 and leave MOTOR POWER on for 2-5 minutes and check to see that the mark has not moved.

c. Input Card Guide

1. Attach upper card guide. Do not seat screws at this time.
2. Insert special tool #87-1068 into place between card guide and manifold.
3. Press upper card guide downward against special tool and seat screws.

d. Capstan Vacuum

1. With a 50 percent punched card placed in front of the capstan, the capstan should exert a force of .55 pounds on the card. If the force is less, the vacuum valve should be adjusted for an indication of 11 to 15 inches of vacuum by using the following adjustment procedure:
2. Remove the IAA card (D120) from location B36.
3. Adjust the Vacuum Valve (next to the Vacuum Gauge) for 15 inches of vacuum.
4. Replace the IAA card.
5. Adjust the Vacuum Gate Valve (located behind the filter jar) for 7 inches of vacuum as measured on the same Vacuum Gauge as used in the above step.
6. Single Pick cards at approximately 5 second intervals while observing the Vacuum Gauge. The reading should fluctuate between 7 and 15 inches of vacuum for each card fed.

e. Position of Gate Solenoid

1. With the solenoid de-energized, the gap between the back surface of the gate and the turn-around roller should be .010 inches.
2. Refer to Turn-Around and Gating Assembly.

f. Pinch Roller Adjustments

1. Place a stainless steel shim stock (.005") between the elastomer (Idler) rollers and the steel (Drive) rollers. Hold the steel roller stationary and pull the shim out slowly with an inch/pound gauge. The read station rollers and stacker rollers should exert a pressure of $2 \pm .2$ pounds with a steady pull.

2. Refer to Read Station Replacement

g. Back-up Arm Force

1. Input Back-up Arm: With Motor Power ON and no cards in the machine, the force gauge should read .1 to .2 pounds to start initial motion of back-up arm away from the stop. Over 3 inches away, the force should be from .4 to .45 pounds. If not, adjust the Input Back-up Arm Spring Drum.

2. Primary Receiving Tray Arm: With Motor Power ON and no cards in the tray, the force gauge should read from .175 to .2 pounds to start initial motion of the back-up arm away from the stop. Over 3 inches away, it should read .4 to .6 pounds for 80 column cards. If not, adjust the associated Spring Drum.

   For 51 column cards, the force gauge should read .275 $\pm$ .05 pounds. If not, R412 should be adjusted to provide the necessary current to the Spring Bias Motor.

h. Photo Diode Adjustment (NOTE: Adjustment should be done after about one-half hour warm-up time to allow the diodes to stabilize.

1. Gating Diode Adjustment

a. Gating Diode #1: With the Operate/Calibrate Switch in the Calibrate position, observe the output of B105 (A20A) and adjust the control on the associated ACA card (A53A) until the output begins to oscillate.

b. Gating Diode #2: Proceed as for the adjustment of Gating Diode #1 with one exception; Observe the output of B106 (A20C) and adjust the control on the ACA card at A57A.

c. Refer to Gating Diode Adjustment.

NOTE: The Operate/Calibrate Switch must be in the Operate position at all times except when making the Gating Diode Adjustments.

2. Primary Read Station: Sync scope negative on B105 (A20A) and look at M000 through M011, one at a time, on Channel A. While feeding the test cards (preferably cards with consecutive punches in each row) adjust the scope to look at two columns from each M card. While observing the photo diode output at the M card, adjust the control on the associated ACA card until the average OFF time ("0") between holes is 50 to 90 usec.

Refer to Photo Diode Bias Adjustments, Read Station #1.

3. Secondary Read Station: Follow the same procedure as that of the Primary Read Station Diode Adjustment with one exception; The OFF time between holes should be 20 to 40 usec.

Refer to Photo Diode Bias Adjustments, Read Station #2.

i. Read Skew Check

1. Observe the photo diode output of rows 9 and 12 at the associated M cards. As cards are read that have all rows punched in columns 1, 40, and 80 the two outputs should switch within 25 usec of each other.
2. Perform step 1 using different row combinations.
3. Perform steps 1 and 2 on both read stations.

j. Final Check After Adjustments Are Made

1. Read 4000 cards without error without using the Advance and Delay switches.
2. Read 4000 cards with no more than one error while the Advance and Delay switches are held depressed.

STUDY QUESTIONS

1. At what speed will the 405 read 80 column cards?

   a. 650 cpm

   b. 1200 cpm

   c. 1600 cpm

   d. 1000 cpm

2. At what speed does the 405 read 51 column cards?

   a. 200 cpm

   b. 1200 cpm

   c. 1600 cpm

   d. 2400 cpm

3. What is the card capacity of the input tray?

   a. 2500

   b. 4000

   c. 2000

   d. 6000

4. How are the cards read in the 405 reader?

   a. row by row, 12 edge first

   b. column by column, column 1 first

   c. column by column, column 80 first

   d. none of the above

5. What type of mechanism is used to initially pick cards from the input tray?

   a. picker knife

   b. pinch roller

   c. pneumatic capstan

   d. more than one of the above

6. During free run read how is the interval between cards developed as they travel along the card path?

   a. on-off action of the brake

   b. electronic delay network

   c. speed difference between capstan and pinch rollers

   d. blank spot on capstan

7. Is positive air pressure used in the 405 reader,if so, for what purpose?

   a. no

   b. yes, it is used to drive capstan.

   c. yes, it is used to separate cards.

   d. no, unless you consider the cooling fan.

8. The same motor that drives the capstan drives the Pinch Rollers.

   a. true

   b. false

9. The Timing Gear is driven by:

   a. the same motor that drives the capstan.

   b. the same motor that drives the vacuum pump.

   c. the same motor that drives the Pinch Rollers.

   d. its own separate motor.

10. If the +20 VDC circuit breaker is turned off, power up sequence would be normal but the read station lamp, jam lamp, and +20 VDC to the logic chassis would be out.

    a. true

    b. false

11. The brake is normally:

    a. spring controlled when reading cards.

    b. pulled by a solenoid when reading cards.

    c. pulled by a solenoid when not reading cards.

    d. controlled off-line only.

12. The Single Pick Switch will allow card feed:

    a. as long as the switch is made.

    b. just long enough to feed one card.

    c. just long enough to feed cards that happen to be in the input tray.

    d. the Single Pick Switch will not feed cards.

13. Listed below are control switches. Which ones must be active (on) in order to perform a single pick operation?

    a. 1, 3, 4

    b. 1, 4

    c. 6, 3, 4, 1

    d. 1, 4, 6

    e. 1, 3, 6

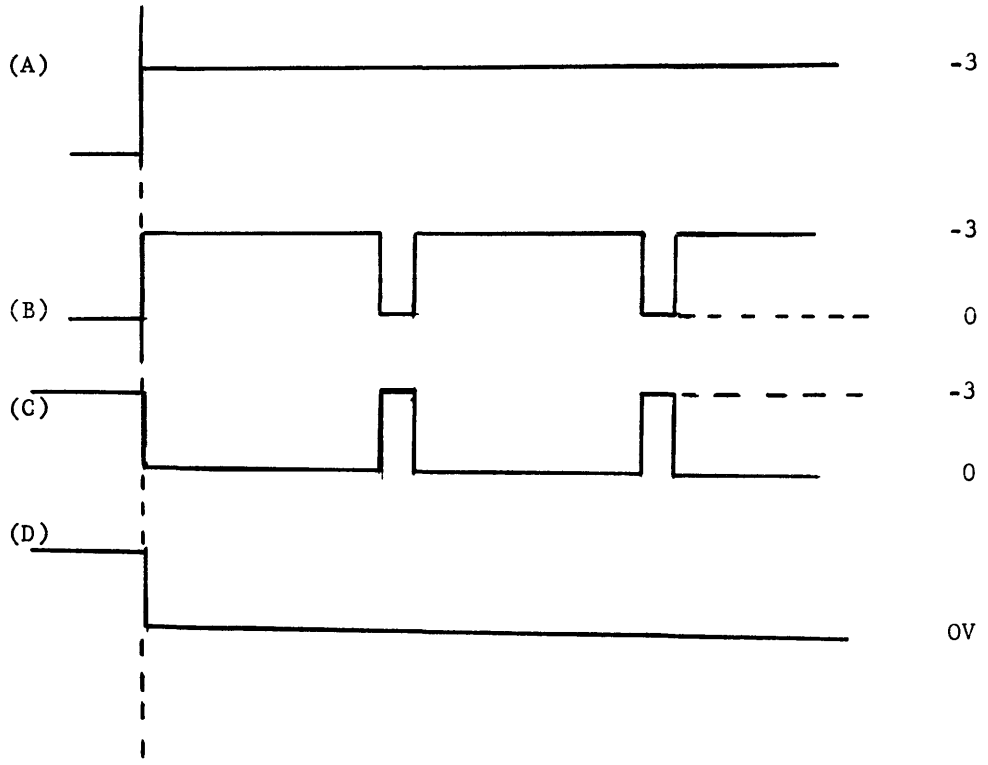
    1. Ready
    2. Run
    3. Single Pick
    4. Manual
    5. End of File
    6. Stop
    7. Auto

14. Cards will always be gated to the Secondary Stacker if a compare or pre-read error occurs:

    a. true

    b. false

15. Choose the correct waveshape from below for the <u>set output</u> of the Feed Control Flip Flop during a free run read.



16. How many cycles from the Magnetic Pick-up correspond to one card column?

    a. 42

    b. 16

    c. 8

    d. 1

17. What kind of counter is used for timing in the 405?

    a. Decrementing Binary

    b. Incrementing Binary

    c. Decrementing Gray Code

    d. Incrementing Gray Code

18. How do we start the counter that is used for timing?

    a. cover gating diode 1

    b. uncover gating diode 2

    c. cover both gating diodes

    d. the counter is always running

19. The counter used for timing never stops during a free run read.

    a. true

    b. false

20. What is the approximate duration of the Advance and Transfer Pulses used to cause the counter to run?

    a. 24 us

    b. 10 us

    c. 2 us

    d. somewhere between 20 us and 28 us

21. How many complete cycles will the counter make during the reading of one 80 column card?

    a. 80

    b. 40

    c. 81

    d. 49

22. Pre-Read checks are executed:

    a. before each card column is read.

    b. before each card is read.

    c. only when programmed.

    d. once before the first card in the input tray is read.

23. The pulse used for Pre-Read lite check is: (output of B213)

    a. a 3.5 us logical 1.

    b. a 3.5 us logical 0.

    c. a 1.5 us logical 0.

    d. a 1.5 us logical 1.

24. How do we control whether we will do a pre-read error check or a compare error check?

    a. two completely different check networks are used.

    b. set flip-flop A100/A101.

    c. clear flip-flop A100/A101.

    d. both B and C are correct.

25. A compare error could be detected from T1-13 to T80-13.

    a. true

    b. false

26. Data read from a card is not compare checked before being sent to the computer.

    a. true

    b. false

27. The purpose of the Resync Circuit is:

    a. to keep the counter in time with the speed of the card being read and/or offset punches.

    b. to sync data transfer to computer timing.

    c. to insure that the mechanics of the machine resync to the counter time.

    d. to insure proper spacing of clock pulses.

28. When reading a card that has a punch in every column, the resync F/F A104/A105 would:

    a. never set.

    b. never clear.

    c. clear and set for every column.

    d. set only on the last column.

29. The output of the Resync Circuit sets the Timing Counter to what time:

    a. 7.5

    b. 13.5

    c. 16.0

    d. 0

    e. none of the above

30. The Main Power Switch controls:

    a. the fans only.

    b. all power to logic and drive motor.

    c. power to fans logic chassis and exciter lamps

    d. chassis power and exciter lamp only.

31. The vibrators are being fed by:

    a. a full wave rectifier.

    b. a half wave rectifier.

    c. unrectified 110 vac 3 phase power.

    d. unrectified 110 vac 1 phase power.

32. The Photo Cell Exciter Lamp would be brighter if the calibrate switch was in the calibrate position.

    a. true

    b. false

33. The Advance Switch causes our compare circuit to compare primary and secondary photo-cell outputs:

    a. sooner than usual.

    b. later than usual.

    c. the Advance Switch has nothing to do with the Compare Circuit.

    d. none of the above are correct.

34. If both the Delay and Advance Switches are active at the same time, the card reader should be able to read cards without generating a pre-read or compare error.

    a. true

    b. false

35. The Compare Error Light can be seen on the Maintenance Panel only.

    a. true

    b. false

CHAPTER III

3248 CARD READER CONTROLLER

CHAPTER III

3248 CARD READER CONTROLLER

INTRODUCTION

The 3248 Card Reader Controller is a single access channel device providing interface between the 3200 Computer and the 405 Card Reader. The logic circuitry is contained in the lower four (4) rows of the same chassis that contains the 405 logic circuitry.

Data read from punched cards is transferred to the 3200 data channel in the 12 bit byte parallel form. Binary data, identified by a 7 and 9 punch in column 1 of each card, is transferred directly to the data channel. Hollerith data, identified by no 7 and 9 punch in column 1 of each card is converted to internal BCD before being transferred. After two (2) Hollerith columns are converted, they are automatically packed into a 12 bit byte. Total data transfer from a punched card will be 80 bytes from a Binary card or 40 bytes from a Hollerith card.

Card motion is initiated upon receiving the Read, Data, and Channel Busy signals from the computer data channel. After being read the card can be diverted into the secondary hopper by using the gate function or allowed to enter the primary stacker tray.

The current status of the 405 and controller can be sensed at any time after the connect has been completed. Included in the status response will be certain interrupt conditions, if they have been selected and the interrupt condition is present.

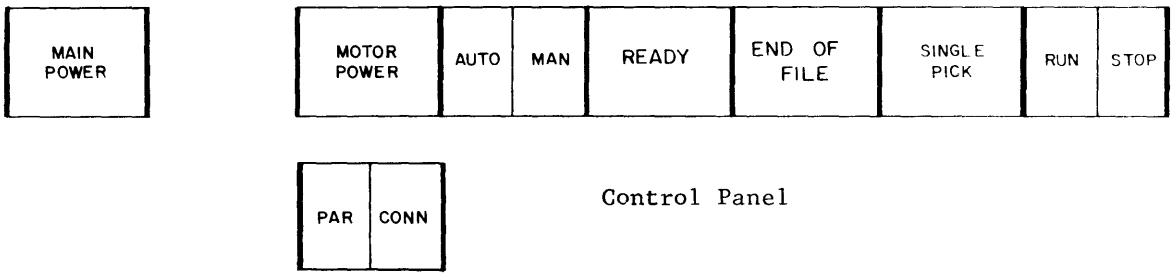
Although the data input is relatively slow compared to other peripheral devices, proper programming will allow the data to be assembled as it is being inputted rather than use additional computer time to assemble.

After the data input is complete,detection of the last card of the deck, the End of File Card, transfers program control to continue the computer operation.

CHARACTERISTICS

1.	Reading Speed:	
	a. 80 column cards	1200 cards per minute
	b. 51 column cards	1600 cards per minute
2.	Card Cycle Time:	
	a. 80 column cards	50 milliseconds (average)
	b. 51 column cards	38 milliseconds (average)
3.	Read Capability:	Binary data and Hollerith to internal BCD data
4.	Data Transfer Rate:	2.52 KC

Name	Function
MAIN POWER	Controls all primary power and turns on the photocell light source.
MOTOR POWER	Controls power to the drive motors, the vacuum-pressure system and the input tray-stacker vibrators.
AUTO/MAN	Selects manual or program controlled modes of operation. Changing switch position automatically drops Ready signal.
END OF FILE	Indicates last card in input tray will complete a file. Must be selected manually.
READY	Indicates reader is ready to read. Performs a MC when the Auto/Man switch is in the MAN position.
SINGLE PICK	Allows a single card to be cycled through the reader when the Auto/Man switch is in the MAN position.
RUN/STOP	Allows manual control of the 3248 when the Auto/Man switch is set to either mode.
PAR/CONN	PAR indicates a transmission parity error has occurred. CONN indicates the 3248 is connected to the data channel.



Control Panel

CARD READER PREPARATION

The following steps must be followed to prepare the 3248 Card Reader Controller for external (computer) control:

1. Place cards in input tray
2. Depress Main Power switch
3. Depress Motor Power switch
4. Set the Auto/Man switch to the AUTO position
5. Set Run/Stop switch to the RUN position
6. Turn End of File switch off unless the input tray contains a complete file
7. Issue a MC or EF Clear from the computer
8. Ready indicator must be lit indicating that the card reader is ready to read cards

CODES

CONNECT CODE

The Connect code, accompanied by a Connect signal, connects the reader to the data channel. A Reply is returned when the 3248 is connected. Bits 9, 10, and 11 (N) in the Connect code (NXXX) must match the Equipment Number switch setting on the 3248 logic chassis. Any Connect code that does not match the Equipment switch setting or does not have correct parity will cause the Connect flip flop to be cleared.

FUNCTION	CODE
RELEASE AND DISCONNECT	0000
NEGATE HOLLERITH to INTERNAL BCD CONVERSION	0001
RELEASE NEGATE HOLLERITH to INTERNAL BCD CONVERSION	0002
GATE CARD	0004
CLEAR	0005
INTERRUPT ON READY AND NOT BUSY	0020
RELEASE INTERRUPT ON READY AND NOT BUSY	0021
INTERRUPT ON END OF OPERATION	0022
RELEASE INTERRUPT ON END OF OPERATION	0023
INTERRUPT ON ABNORMAL END OF OPERATION	0024
RELEASE INTERRUPT ON ABNORMAL END OF OPERATION	0025

FUNCTION CODES

Release and Disconnect (0000)

This code master clears the 3248 Card Reader, and disconnects it from the Data Channel.

Negate Hollerith to Internal BCD Conversion (0001)
Release Negate Hollerith to Internal BCD Conversion (0002)

This code allows cards without the 7 and 9 punch to be read as binary. In normal operation, the 3248 checks column one of each card for a 7 and 9 punch. If a 7 and 9 punch exists, the card is read as a binary card. If the 7 and 9 punch does not exist, the card is considered Hollerith and the data is translated into BCD.

Gate Card (0004)

This code allows a limited card sorting operation. The selected cards are directed to the secondary stacker. A Gate Card instruction must be issued for each card to be gated. The instruction must arrive within 1.5 ms after the last column of the selected card has been read.

Clear (0005)

This code clears any Interrupt selection, Interrupt response or Negate selection in the 3248 logic.

Interrupt on Ready and Not Busy (0020)
Release Interrupt on Ready and Not Busy (0021)

This Interrupt code informs the computer when it can start an operation due to the completion of a manual intervention. The equipment is ready if the Ready switch has been pressed, cards are in the input tray and the primary and secondary stackers are not full. The Interrupt response for this condition is cleared by a Release (0021), Function Clear (0005) or Reselection (0020).

Interrupt on End of Operation (0022)
Release Interrupt on End of Operation (0023)

This Interrupt occurs in the following conditions:

1) All information has been transferred.
2) The Channel Active is down and the current record has been completely read.
3) If information transfer cannot continue.

The Interrupt response may be cleared by any of the following codes: 0022, 0023 or 0005.

Interrupt on Abnormal End of Operation (0024)
Release Interrupt on Abnormal End of Operation (0025)

This Interrupt occurs when the information transfer, requested by the Channel Active and Read line, cannot continue. The Interrupt is caused by any or all of the following conditions:

1) Fail to feed.
2) Read compare error or pre-read error.
3) Stacker full or jammed.
4) Input tray empty.
5) Manual intervention.
6) Illegal suppress assembly/disassembly.
7) A file card has been read 33

The Interrupt response may be cleared by either of the following codes: 0024, 0025.

STATUS RESPONSE CODES

STATUS	CODE
READER READY	XXX1
READER BUSY	XXX2
BINARY CARD	XXX4
FILE CARD	XX1X
FAIL TO FEED OR STACKER FULL OR JAM	XX2X
INPUT TRAY EMPTY	XX4X
END OF FILE	X1XX
INTERRUPT - READY AND NOT BUSY	X2XX
INTERRUPT - END OF OPERATION	X4XX
INTERRUPT - ABNORMAL END OF OPERATION	1XXX
READ COMPARE OR PRE-READ ERROR	2XXX

Reader Ready (XXX1)

If bit 0 of the Status code is present the reader is operationally ready. This condition exists if cards are in the input tray, the primary and secondary stackers are not full and the reader has been cleared. The following abnormal conditions cause the Ready to drop:

1) Fail to feed.
2) Read compare error or pre-read error.
3) Stacker full or jammed.
4) Input tray empty.
5) Manual intervention.
6) Illegal suppress assembly/disassembly.

Reader Busy (XXX2)

The Reader Busy status (bit 1 of the Status code) occurs when the Channel Busy and Reader Ready signals are present. The Reader Busy signal remains up until the Channel Busy drops or the completed card cycle causes the Reader Ready to drop.

Binary Card (XXX4)

The presence of a 7 and 9 punch in the first column of a card flags it as a binary card if negation has not been requested. Bit 2, the status bit for this condition, is present after the first column is read and is dropped approximately 1 ms prior to reading the next card.

File Card (XX1X)

This condition exists when a card containing punches in rows 7 and 8 only of the first column of a Hollerith card is detected. It cannot be generated when reading binary cards. All information on a File Card is read and delivered to the data channel if desired. An interrupt on Abnormal End of Operation (if selected) will occur after detecting

a File Card if the Read signal drops during the reading of the card or at the end of the card. The File Card indication remains on the status lines until cleared by a Function Clear or Master Clear signal, or until a new operation is initiated by the next rising of Channel Busy.

Fail to Feed or Stacker Full or Jam (XX2X)
Input Tray Empty (XX4X)

These status responses are self-explanatory and are all abnormal conditions.

End of File (X1XX)

This condition exists when the End of File switch is ON and the input tray is empty. When the input tray does not contain the last card of a file, the switch should be placed in the OFF position. The switch does not override abnormal conditions.

Interrupt - Ready and Not Busy (X2XX)

This interrupt status is present when the (XX20) EF code is generated and indicates to the computer that the card reader can initiate an operation.

Interrupt - End of Operation (X4XX)

This interrupt status is present at the completion of either a normal or abnormal operation and the XX22 EF code has been generated.

Interrupt - Abnormal End of Operation (1XXX)

This interrupt status indicates that the (XX24) EF code was generated due to the abnormal completion of an operation.

Read Compare or Pre-read Error (2XXX)

Bit 10 indicates that either a comparison error was detected during the transfer of card information to the computer or a read amplifier was not functioning properly prior to reading the information from the card.

PROGRAM CONCEPTS

Programming the 405/3248 Card Reading equipment can be made as simple or as complex as the programmer desires. Regardless of the complexity the program must follow certain rules to ensure proper operation of this portion of the computer I/O equipment.

The following is an example program used to show how computer instructions can be used to complete a Single Card Read cycle.

CONNECT

Location 0 770 CH 5000

The equipment switch on the 3248 is set to number 5. Bit positions 9-10-11 of the Connect code must match the setting of the equipment switch. If the match occurs the Connect signal is enabled to set the Connect F/F. A Reply will be returned to the data channel. At the completion of the connect operation the status lines are enabled to the data channel. If none of the controllers connected to the data channel have the proper switch setting, or a parity error occurs in the Connect code, an Internal Reject is generated by the computer clearing the data channel. The next instruction will be read at P+2.

Location 1 01000000

The Reject instruction, read at P+1, is used to cause the Connect to wait until the channel becomes $\overline{\text{Busy}}$ in the event another operation is in process.

Location 2 772 CH 0001

The Sense External Status instruction is used to sense the 3248 status lines to determine the operating condition of the 405. The lower 12 bits of the status instruction are programmed to sense a Reader Ready condition. If the card reader is ready the next instruction will be read at P+2, otherwise P+1.

Location 3 01000002

The Reject instruction will cause the computer in this case to "loop" on the status instruction until the ready condition is sensed.

FUNCTION

Location 4 771 CH 0024

Since the 3248 controller is connected to the data channel we can now function for an Abnormal End of Operation Interrupt condition. The Function code (XX24) accompanied by the Function signal are sent via the data channel. The 3248 will translate the Function code (XX24) and set the Interrupt ABEOP Select F/F. The Function code will set the Function F/F. If the function can be completed a Reply signal is returned to the data channel. If the 405 is busy reading a card a Reject signal is returned to the data channel causing the Reject instruction at P+1 to be executed. A Function which does not receive a Reply signal within 100 u/s will be cleared by an Internal Reject in the data channel. When the abnormal condition occurs in the 405 the 3248 will interrupt the computer.

Location 5 01000004

The Reject instruction causes the Function instruction to "loop" until the 405 goes $\overline{\text{Busy}}$, then it can be executed.

CARD INPUT

Location 6 74000101

The Input Word instruction causes the Read, Data, and Channel Busy signals from the data channel to be sent to the 3248. The 3248 will send a feed command to the 405 to move a card onto the read stations for a data transfer. A 12 bit column word will be transferred, with a Reply signal, to the data channel after each data signal comes up. Location 100 will be the Last Word Address for the data input.

The End of Record Signal, sent on the Data signal following the last column transferred, will cause the data input to be terminated. The Read, Data, and Channel Busy signals will be cleared.

Location 7 CH 0000050

The First Word Address for the data input will begin at location 50. The data is received in 12 bit bytes from the 3248, then is stored in memory (a 24 bit word containing 2 bytes of data). It will be noted that only 40 locations in memory are used to store 80 columns of data from a binary card. Only 20 locations in memory are used to store an 80 column Hollerith card.

Location 10 01000006

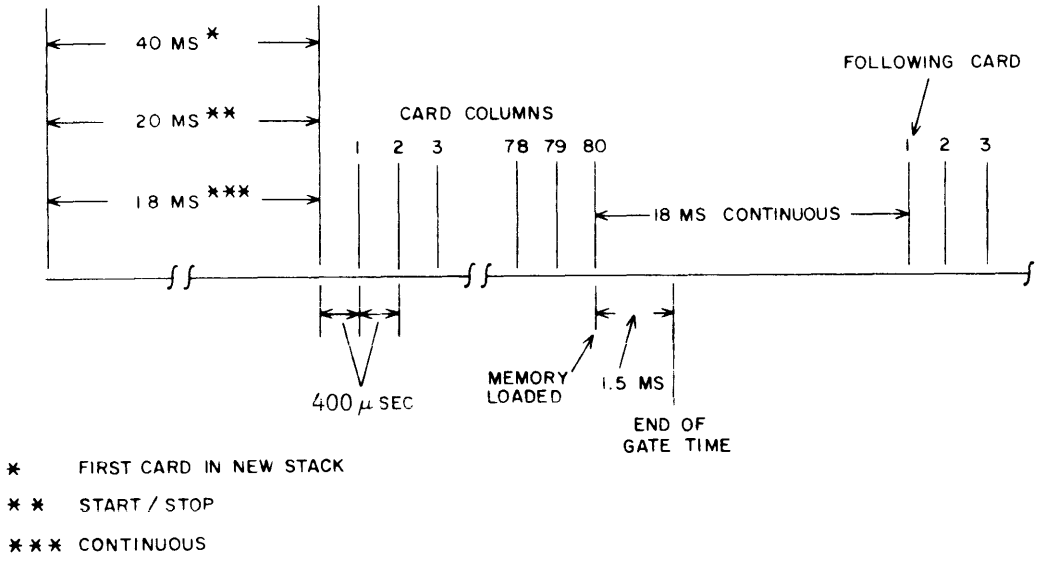
The Reject instruction causes the Read operation to wait until the previous Function instruction has been completed.

Location 11 77770000

The Halt instruction causes the program to stop. No more instructions will be executed but the data input will continue until the last byte is stored.

PROGRAM TIMING

The reader may send up to 40 translated and packed or 80 untranslated 12-bit bytes to the computer from each card. The timing chart shows the timing for each card cycle. This chart enables a programmer to make full use of the computer between card columns and to reselect the reader at a time that will insure full speed on-line operation.



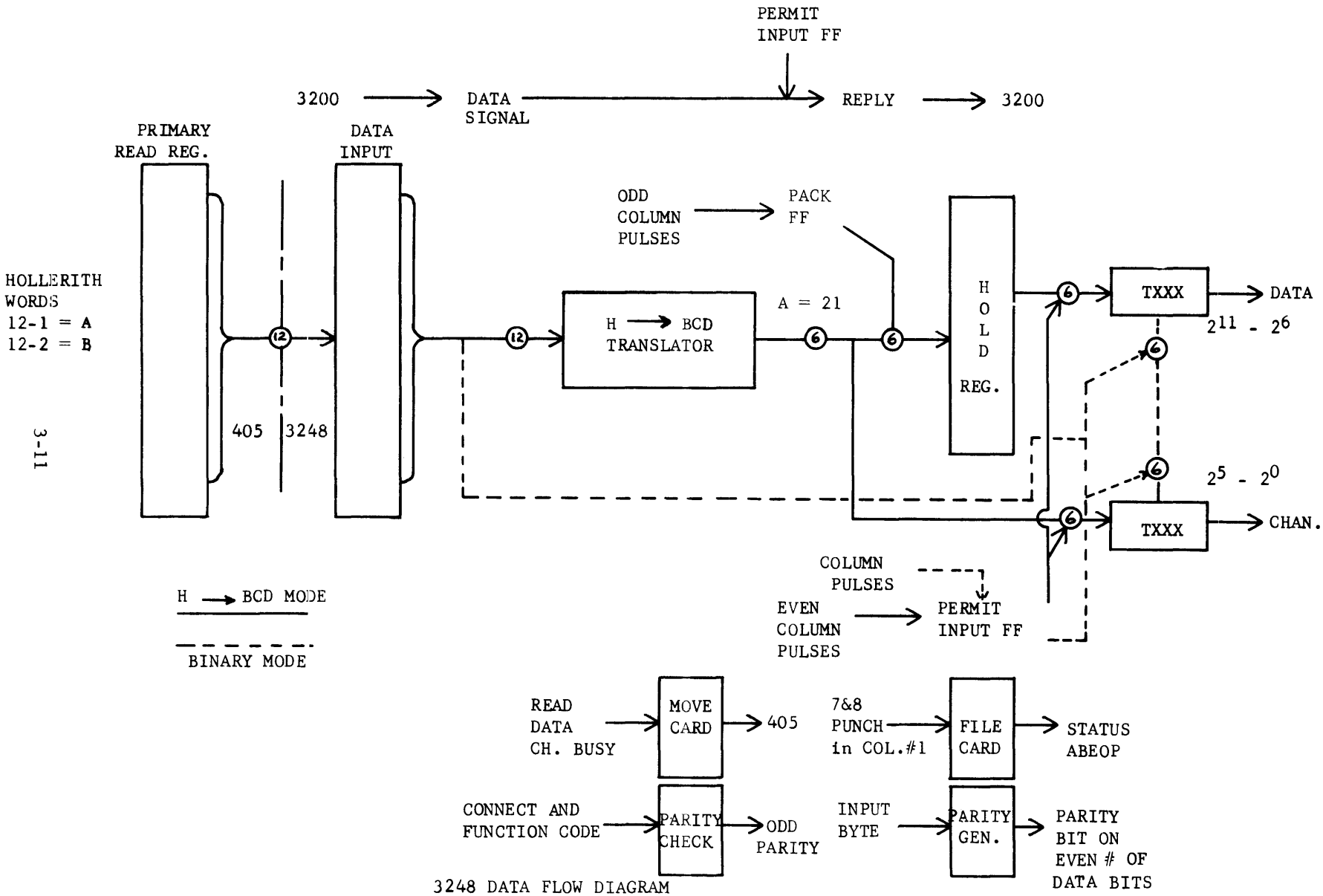
Program Timing

SUPPRESS ASSEMBLY MODE (6-BIT CHARACTER INPUT)

The Suppress Assembly Mode is automatically established when using the 73 (character input) or 73.4 (character input to A) instructions in the 3200 computer. As each column of a Hollerith card is read it is converted to a 6-bit BCD character. Normally, to provide maximum transfer of data between the reader and the data channel, two adjacent columns are read and packed into one 12-bit byte. However, for Suppress Assembly mode, only one column is read, and the translation is gated to the lower 6-bits of each byte, the upper 6-bits being zeros. Suppress Assembly Mode is valid only when reading Hollerith cards. If a binary card is detected during this operation (7 and 9 punch in column 1), or if the Negate Hollerith to BCD function is in effect, an abnormal EOP will ensue. In addition, an Interrupt signal will be transmitted to the computer, if Interrupt on abnormal EOP had been previously selected.

Internal BCD Code	Char	Card	Internal BCD Code	Char	Card
00	0	0	40	(minus) -	11
01	1	1	41	J	11, 1
02	2	2	42	K	11, 2
03	3	3	43	L	11, 3
04	4	4	44	M	11, 4
05	5	5	45	N	11, 5
06	6	6	46	O	11, 6
07	7	7	47	P	11, 7
10	8	8	50	Q	11, 8
11	9	9	51	R	11, 9
12		8, 2	52	-0	11, 0
13	=	8, 3	53	$	11, 8, 3
14	(dash) -	8, 4	54	*	11, 8, 4
15		8, 5	55		11, 8, 5
16		8, 6	56		11, 8, 6
17		8, 7	57		11, 8, 7
20	+	12	60	(Space)	Blank
21	A	12, 1	61	/	0, 1
22	B	12, 2	62	S	0, 2
23	C	12, 3	63	T	0, 3
24	D	12, 4	64	U	0, 4
25	E	12, 5	65	V	0, 5
26	F	12, 6	66	W	0, 6
27	G	12, 7	67	X	0, 7
30	H	12, 8	70	Y	0, 8
31	I	12, 9	71	Z	0, 9
32	+0	12, 0	72		0, 8, 2
33	.	12, 8, 3	73	,	0, 8, 3
34	)	12, 8, 4	74	(	0, 8, 4
35		12, 8, 5	75		0, 8, 5
36		12, 8, 6	76		0, 8, 6
37		12, 8, 7	77		0, 8, 7

BCD/HOLLERITH/CODES



3248 DATA FLOW DIAGRAM

SEQUENCE OF OPERATION

CONNECT

1. Connect Signal and connect code to 3248.

    a. R015 = 1
    b. R000 to R011, Connect code
    c. R012 has parity bit

2. Do a parity check

    a. If Parity OK set "K020/021"
       NOTE: Parity OK F/F cannot set if parity error on a connect operation.

3. Bits 9-10-11 go to select switch in 405 for comparison.

    a. If compare, J041 = 1.

4. Set "Connect FF", K010/011. } Enables status, etc. back to the channel.

    a. If parity is OK

5. After 2.5 u/s set "Reply FF", K014/015.

    a. Send reply via T013.

    Channel drops Connect Sig & Code.

6. R015 = 0.

    a. J040 = 1.

        1. Clear "Reply FF", K014/015
        2. Clear "Parity OK FF".

    NOTE: "Ready FF" K300/301, Sets when:

    a. Connect FF sets
    b. If no abnormal condition

FUNCTION

1. Function Signal and Function code to 3248.

    a. R016 = 1
    b. R012 parity bit
    c. R000 to R011 Function code

2. Do a parity check.

   a. If good, set K020/021
   b. If bad, set K018/019

3. Set "Function FF", K012/013.

   a. Set the selected function FF. (as J051 = 1)

4. After .5 u/s set "Reply FF" and send Reply to channel.

5. Channel drops function signal and code

   a. J040 = 1.

      1. Clear K012/013, "Function FF"
      2. Clear "Reply FF"
      3. Clear "Reject FF"
      4. Clear "Parity OK FF".

   NOTE: If Parity Error and not busy:

      a. Set"Parity Error FF", send Parity Error signal to channel
      b. Cannot set "Function FF" K012/013
      c. Cannot send Reply or Reject

   NOTE: If "Busy FF" K302/303 set

      a. Cannot set Function
      b. Set "Reject FF" K016/016 and send External Reject.

READ (BINARY CARD WITH 7 AND 9 PUNCH IN COLUMN ONE)

1. Read Signal (R013 = 1), Channel Busy (R020 = 1) and Data Signal (R017 = 1)

   a. JC40 = 0.

   b. Set "Card Feed FF" P530/531. (Sets A110/111 in 405 causing brake to be pulled back).

      1. Set "Busy FF"

2. The 405 executes the light and dark check. Pre-read error checks.

3. Dark Probe comes up when GD #2 is covered.

   a. Clear "Card Feed FF" P530/531.
   b. Set "Read Card FF" P500/501. The Column Pulse is enabled to enter P510.
   c. Set "In Operation FF" P560/561.
   d. Clear Translate FF, Translate Test FF, and File Card FF.

4. Read column #1 of card in 405, T_1 - T13.5

   a. Data available at J120 to J131.
   b. P516 = 1 and P518 = 1 as Translate FF is clear.

      1. J120 - J131 are enabled into J200 - J211.

   c. J056 = 1 and J055 = 1 enabling J200 - J211 to enter data in the transmitter cards and send it to the data channel. (NOTE: The channel <u>needs</u> a reply to accept the data).
   d. J200 and J300 terms feed the Parity Generator. (If the data word has an even number of bits J416 will output a "1") J416 feeds T012.

5. Column pulse from 405 at T_1 - 16, 10 us "0" into P510.

   a. P510 and P511 = 2.5 u/s "1" setting "Translate Test FF" P502/503
   b. P503 and P512 = 2.5 u/s "1" setting "Translate FF" P504/505 <u>only</u> if there is no 7 and 9 punch
   c. If "Translate FF" does <u>not</u> set, "Pack FF" <u>won't</u> set

      1. After .5 u/s set "Permit Input FF" P508/509.
      2. Set "Reply FF" and send reply via T013.

6. Data Signal drops

   a. Clear "Permit Input FF" P508/509
   b. J040 = 1, clear "Reply FF"

7. Steps 5 through 7 repeat for the remaining 79 columns.

8. T_{81} - 13.5 (GD #1 uncovered)

   a. End of Card Pulse #1 generated
   b. P535 = 1 for 2 u/s

      1. Set "End of Record FF". End of Record signal is sent to data channel on T016.
      2. Clear "In Operation FF" P560/561.
      3. After .5 u/s clr "Read Card FF".

      NOTE: End of Record Signal will cause the Channel to drop the Data signal, Read signal and Channel Busy.

9. Clear "Busy FF".

10. If "Abnormal End of Operation" clear "Ready FF".

READ HOLLERITH CARD (WITH NO 7 AND 9 PUNCH IN COLUMN ONE)

1. Read, Channel Busy and Data signals arrive.

   a. Set "Card Feed FF" causing the brake to be pulled back in the 405.
   b. Set "Busy FF".

2. Dark Probe from 405, P533 = 1, P538 = 1.

   a. Set "Read Card FF" and "In Operation FF".
   b. Clear "Card Feed FF" "Translate Test FF", "Translate FF", and "File Card FF."

3. Read column #1 at T_1 - 13.5. (Data available at J120 to J131)

   a. P516 and P518 = 1.

      1. J120 - J131 are enabled into J200 - J211.

   b. J056 = 1 and J055 = 1.

      1. Enables J200 - J211 to the transmitters feeding the channel data lines.

   c. J200 and J300 terms feed the Parity Generator and J416 feeds the Parity Bit into T012.

4. Column pulse from 405 at T_1 - 16, 10 u/s "0" into P510.

   a. P510 and P511 = 2.5 u/s "1" setting "Translate Test FF".
   b. P503 and P512 = 2.5 u/s "1" setting "Translate FF."

      1. Set "Pack FF."

   c. P510 and P507 and P513 = 1, driving P514 to a "0".

      1. Enables H100 - H105 into the "Hold Register".

      NOTE: The first 12 bit word for column #1 has been converted to a 6 bit "INT BCD CODE" and stored in the "Hold Register".

      NOTE: The "Permit Input FF" cannot be set at this time to return a reply.

Reasons: 1. The "Translate FF" is set breaking the lower "and" input to the set side of P508/509.
2. The output of P507 is delayed 30 u/s by Y100.

But. P510 and P511 = 1 for only 2.5 u/s breaking the top "and" gate into the set side of P508/509

5. Read column #2, T_2 - 13.5.

   a. Column #2 is now fed to the Hollerith to BCD converter.

6. Column Pulse #2, T_2 - 16.

   a. P510 and P511 = 1 for 2.5 u/s.

      1. Set "Permit Input" FF.

   NOTE: Translate Test FF, Translate FF and Pack FF still set from Column #1.

      2. P514 has a "0" input as Y100 = 1 and P513 = 0. Thus the 2nd column is <u>not</u> gated into the "Hold Register".
         At this time the "Hold Register" output goes on the upper 6 bits of the Data Lines (Col. #1) and the "H" inverters are applied to the lower 6 bits of the Data Lines (Col. #2).

      3. Set "Reply FF" and send Reply to channel via T013.

7. The channel will drop the Data Signal.

   a. J040 = 1 clear "Reply FF".
   b. Clear "Permit Input FF".
   C. Clear "Pack FF" if not Suppress Assembly/Disassembly.

      1. P520 = 1 clearing the "Hold Register"

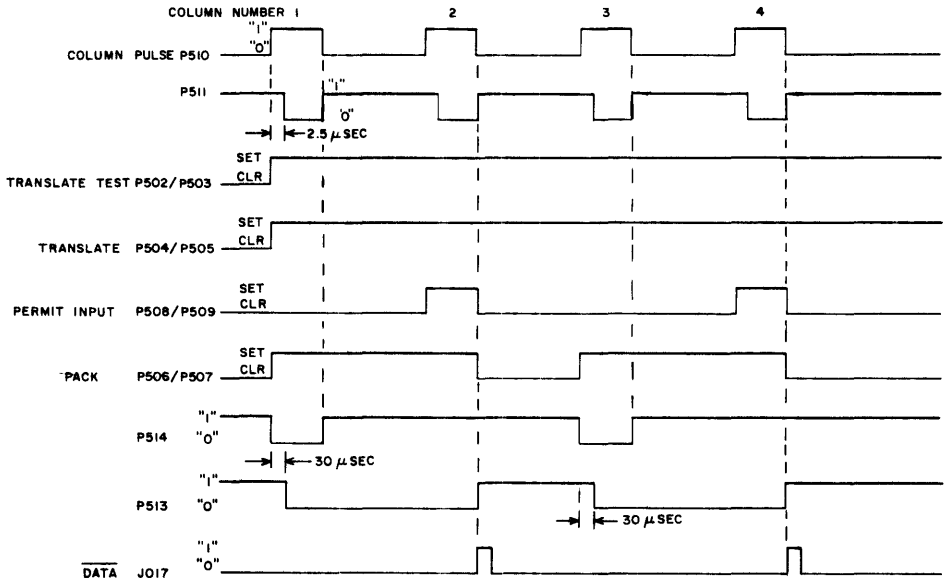
8. Steps 3 through 7 will be repeated for the remaining 78 columns.

   NOTE: 40 Data Transfers are needed during the reading of all 80 columns.

   When GD #1 uncovers and End of Card Pulse #1 is sent P535 = 1.

   a. Clear P560-561, set "EOR FF" sending EOR to channel.
   b. Clear "Read Card FF" after .5 u/s.

      Translate FF and Translate Test FF won't clear until the next dark probe.



NOTE: TIME IS NOT IN TRUE PROPORTION

TIMING FOR PACK MODE

BLOCK DIAGRAM

The CONTROL DATA* 3248-A Card Reader Controller Transmits columnar information read by a CONTROL DATA 405 Card Reader to a 3000 Series data channel in 12-bit bytes.

The 3248-A consists of the basic 405 reader logic plus approximately 120 additional cards which perform the following functions:

1) Connect.

2) Parity generation.

3) Parity checking.

4) Function control and translation.

5) Card reader control.

6) Data preparation.

7) Status.

READ BINARY

One of two conditions indicate that the information on a card is to be interpreted as binary:

1) column 1 of the card contains punches in rows 7 and 9, or

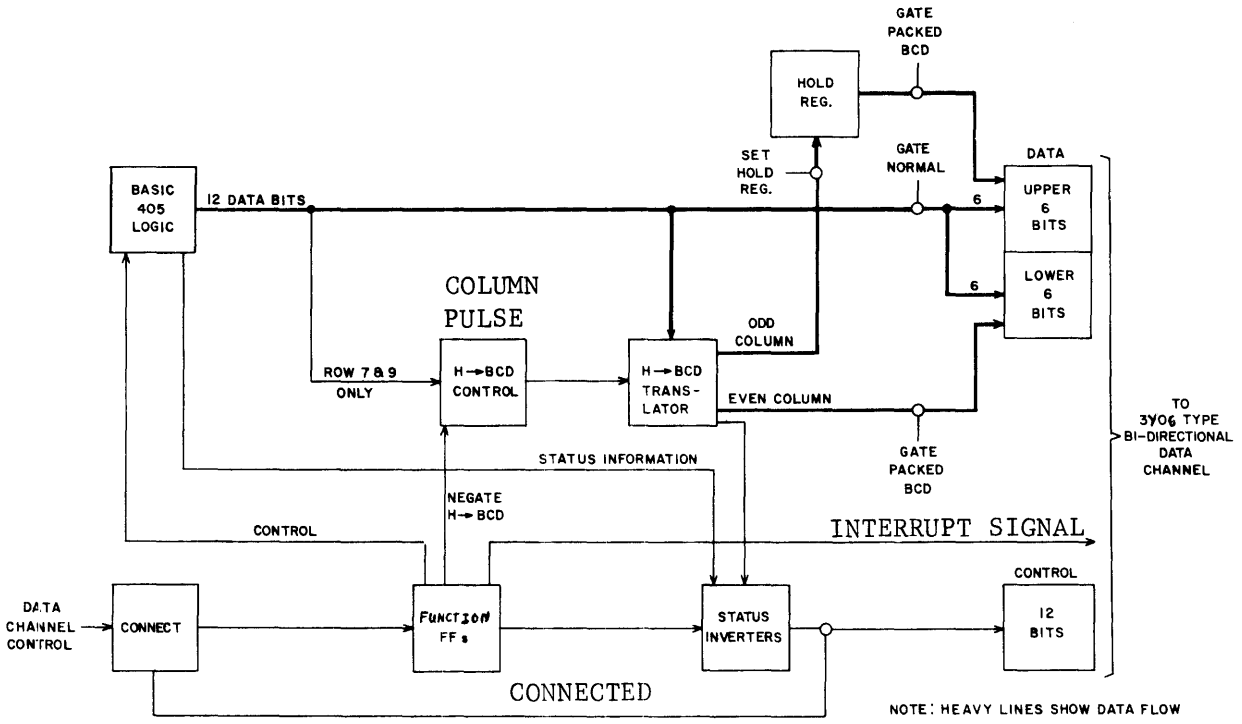
2) a Negate H→BCD function has been selected prior to the reading of the card.

The 12 bits of data read by the 405 are passed directly to the data lines (Gate Normal), then to the data channel.

READ HOLLERITH

Hollerith-coded cards (no 7 and 9 punches in column 1, or Negate H→BCD not selected) are handled as follows: The data read from the first (odd) column is passed through a H→BCD Translator. The translator converts the data into a 6-bit BCD character which is stored in a Hold register. Then the second (even) column is read and translated. This second character is gated to the lower six data lines, and simultaneously the character in the Hold register is gated to the upper six data lines. Successive odd and even columns are processed in the same manner with the information from two columns being "packed" into one 12-bit byte. When reading 51-column cards, Column 51 cannot be read by this controller unless an input character operation is performed.

*Registered trademark of Control Data Corporation



BLOCK DIAGRAM

CONNECT

The Connect signal and Connect code are received through R000-R011 and R015. The code is routed through the Equipment Number switch and the parity network. If the setting of the switch agrees with the code and there is no parity error, the Connect FF sets, turning on the Connect (CONN) light. After 2.5 usec the Reply FF (K014/015) sets, gating a reply to the data channel. If there is a parity error (K018=0), the Connect FF is cleared, the Parity Error (PAR) light on the controller is turned on, and the Parity Error line to the data channel is energized.

FUNCTION

The Function signal and Function code are received through R000-R011 and R016. If there is no parity error (K021=1) the Function FF is set, enabling the translated function code to set one of the three Interrupt FFs, Negate H⟶BCD, or Gate Card. After 0.5 usec a reply is sent to the data channel. If a parity error is recognized, the Function FF is not set and the Parity Error line (and light) is energized.

If the data channel should issue a function code while the controller is busy (K302=0), the resultant "0" from J036 would prevent setting the Function FF; instead a Reject signal (K016/017) would be returned to the data channel.

INTERRUPT

When an interrupt condition has been selected and that condition occurs, J060 energizes T015, which sends an Interrupt signal back to the data channel. The interrupt line through which this signal travels is determined by sections 4 and 5 of the Equipment Number switch The conditions generating the interrupts are shown on page 3-21. These are:

Ready and Not Busy

Self-evident

Abnormal End of Operation

An Interrupt on Abnormal End of Operation is generated whenever the controller goes from Ready to Not Ready. These conditions (see page 3-21) are:

1) Input Tray Empty
2) Compare or Pre-read Error
3) Stacker Full or Card Jam
4) Fail to Feed
5) Illegal Suppress Assembly/Disassembly
6) Reader in Manual mode

In addition, an Abnormal End of Operation interrupt is generated when the Read signal drops after a file card has been read.

End of Operation

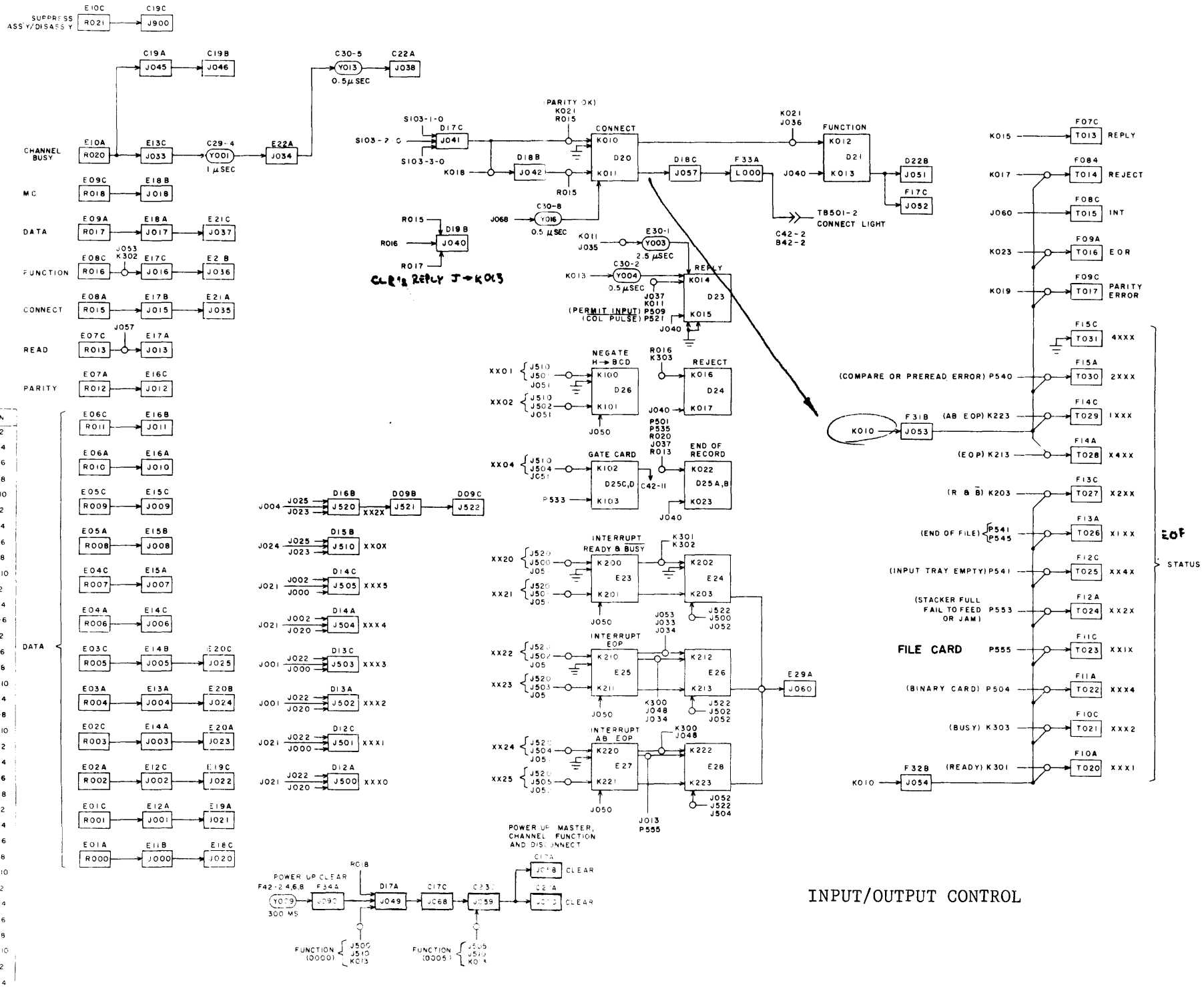
An Interrupt on End of Operation is generated whenever the data channel goes Not Busy or, if as a result of any of the abnormal conditions mentioned above, the controller goes Not Ready while the Channel Busy signal is still up.

GATE CARD

The Gate Card FF is set by a XX04 function code, and sends a signal to the 405 which directs the card just read into the secondary stacker.

END OF RECORD

If the Read signal from the data channel remains up after the last column of a card has been read, then at the rise of the next Data Signal, the EOR FF will set, returning an EOR signal to the data channel.



TERM	JACK	PIN
RC00	A3J	A1-2
RC01	A3J	A3-4
R002	A3J	A5-6
R003	A3J1	A7-8
R004	A3J1	A9-10
R005	A3J1	B1-2
R006	A3J1	B3-4
R007	A3J	B5-6
R008	A3J	B7-8
R009	A3J1	B9-10
R010	A3J1	C1-2
R011	A3J1	C3-4
R012	A3J1	C5-6
R013	A3J1	D1-2
R015	A3J1	D5-6
R016	A3J1	D7-8
R017	A3J1	D9-10
R018	A3J1, J2	F3-4
R020	A3J1, J2	C7-8
R021	A3J3, J4	C9-10
T013	A3J2	E1-2
T014	A3J2	E3-4
T016	A3J2	E5-6
TO 7	A3J2	E7-8
T020	A3J3, J4	A1-2
T021	A3J3, J4	A3-4
T022	A3J3, J4	A5-6
T023	A3J3, J4	A7-8
T024	A3J3, J4	A9-10
T025	A3J3, J4	B1-2
T026	A3J3, J4	B3-4
T027	A3J3, J4	B5-6
T028	A3J3, J4	B7-8
T029	A3J3, J4	B9-10
T030	A3J3, J4	C1-2
T031	A3J3, J4	C3-4

CARD FEED

If a Full Connect (J057) has been established, and the Read, Channel Busy, & Data signals indicate the data channel wishes some information, the Card Feed FF is set, energizing the Reader brake. As the leading edge of the card passes under the read station, a Dark Probe signal (P533) is generated. This clears the Card Feed FF, and at the same time sets the Read Card FF.

TRANSLATE

Hollerith

When a ground level signal appears at C41-1, indicating the first card column is in the read station, a 2.5 usec pulse sets the Translate Test FF, and another 2.5 usec pulse checks the first column for a 7 and 9 punch. If these punches are absent, the Translate FF sets. Because the switching time of the Translate Test and Translate FFs is considerably below 2.5 usec, P510 AND P511 may now set the Pack FF. This drops P514 to a "0", and the first column data is translated and loaded into the Hold register. When P510 returns to a "0" the H⟶Hold register transfer is terminated.

After 30 usec, Y100 times out, and P513 returns to a "0", further inhibiting the Hold register inputs. When the column pulse appears for column 2, the information is translated, put on the data lines, and after 0.5 usec, Y014 allows Permit Input (P508/509) to be set. When the reply signal drops the data signal, J017 clears Permit Input. Translate and Translate Test FFs are cleared by the Dark Probe at the start of another card cycle.

Binary

If the first column contains a 7 and 9 punch, the Translate FF cannot be set. The information in column 1 is transferred to the 12 data lines, and 0.5 usec later Permit Input is set.

ABNORMAL CONDITIONS

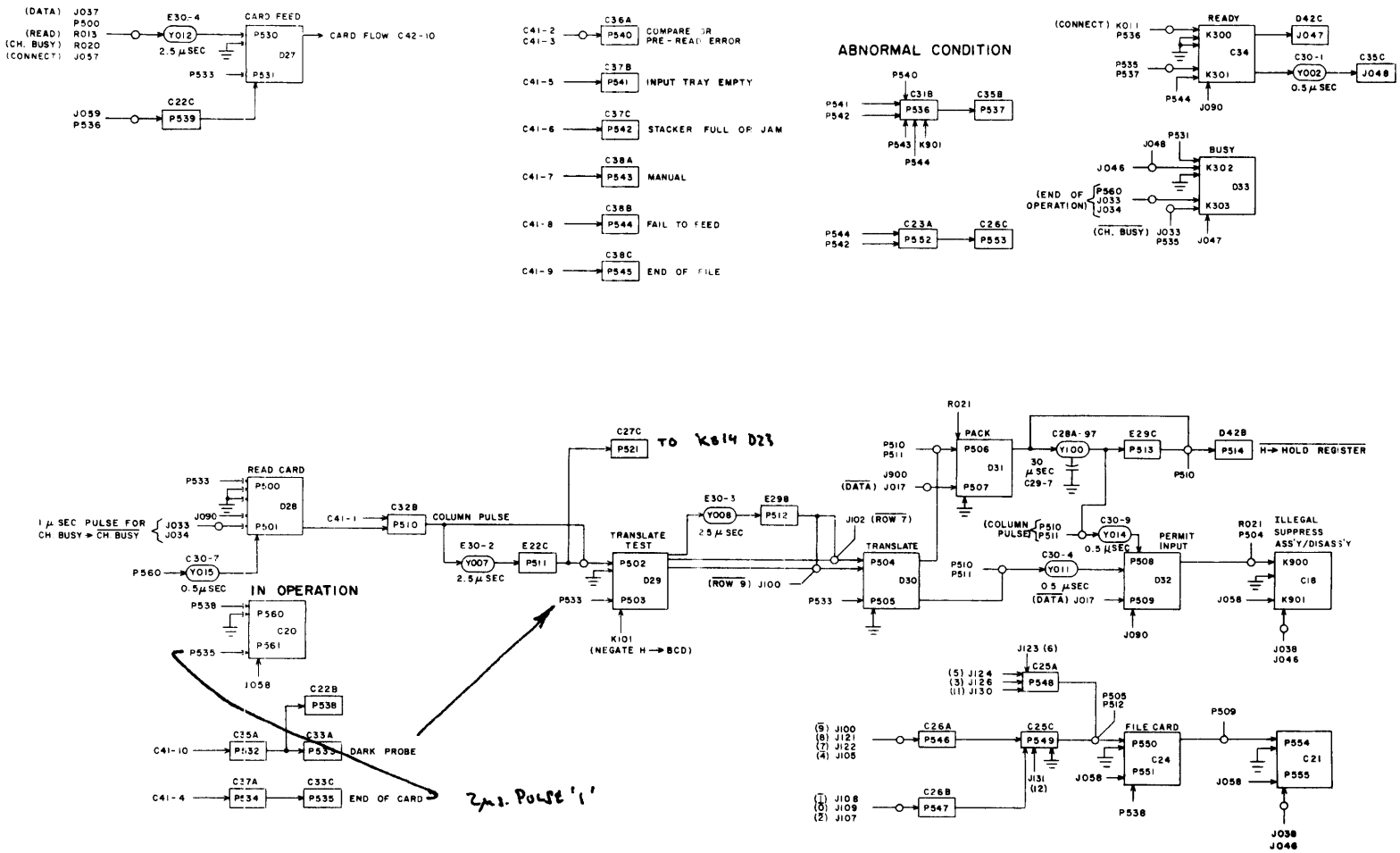
If a transfer of binary information is attempted during a Character Input instruction, the Suppress Assembly/Disassembly signal (R021), which comes up during Character instructions will set K900/901. This will indicate an Abnormal Condition. The card data will be transmitted but when the End of Card Pulse (P535) comes up, the Ready FF will be cleared. This will send a 0.5 usec pulse to set the Interrupt on Abnormal End of Operation FF (page 3), providing that class of interrupt had been selected. If there were no interrupt selection, the information would be transmitted with no indication of abnormality. Other abnormal conditions, all of which operate in the same manner, are shown as additional inputs to P536.

FILE CARD

If a 7 and 8 punch is recognized during the first column pulse, the File Card FF will be set. Then, with the setting of Permit Input, P554/555 will set. When the data line falls after the transfer of the first byte, the Interrupt on Abnormal End of Operation FF will be set, providing that class of interrupt had been selected.

CHARACTER INPUT

During a Character Input instruction (3100 and 3200 Computer Systems) each column on the card is translated into a 6-bit BCD character and transmitted to the data channel as the lower six bits of a byte, the upper six bits being zeros. In this case the Suppress Assembly/Disassembly signal (R021) comes up with the first Data signal. Thus, by the time the column pulse for column 1 appears (which ordinarily sets the Pack FF), the prior R021 input to P506/507 has already caused Y100 to time out, and Permit Input is set after a delay of only 0.5 usec (Y014). The R021 forced set input to the Pack FF remains throughout the entire data transfer, thereby allowing Permit Input to be set for every column pulse.



READER CONTROL

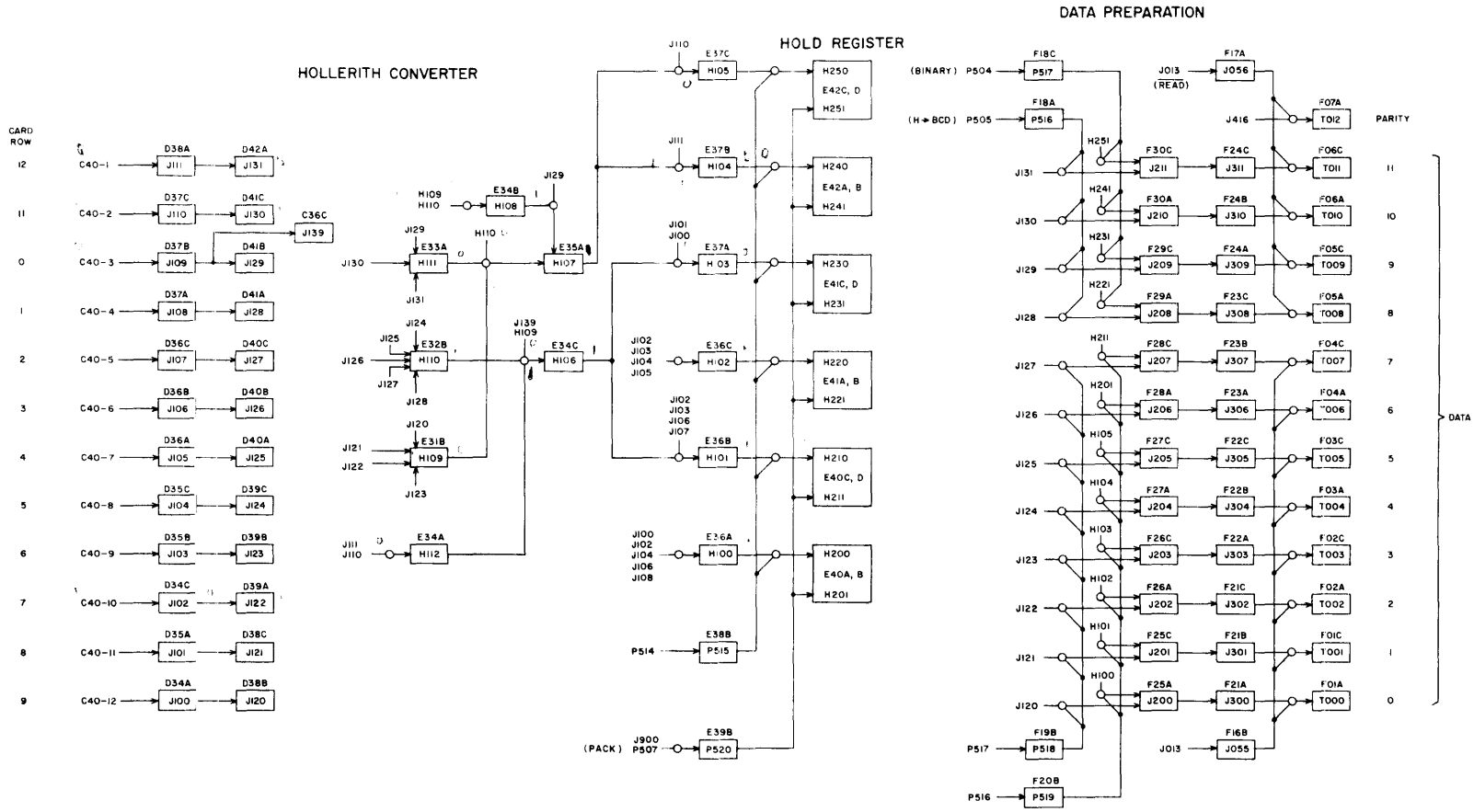
NIC/IR DROBE GATES INFORMATION?

BINARY

With a binary input the translate FF (P505) is clear, so the outputs from P516 and P518 enable the binary gates to the data lines. All incoming data is fed through the Hollerith converter, but the resultant translations are meaningless for binary data because the Hollerith gates to the data lines are not enabled.

HOLLERITH

The sequence for Hollerith data was explained on page 3-18. Note that every translated character appears at the gates to the lower six data lines. This is important during Character Input instructions (3100 and 3200 Computer Systems), since each BCD character must be transmitted as the lower six bits of a separate 12-bit byte. During normal Hollerith input, however, the Permit Input FF will be set only when even-column characters appear at the lower six data line gates.



DATA PREPARATION

TERM	JACK	PIN
T000	A3J2	A1-2
T001	A3J2	A3-4
T002	A3J2	A5-6
T003	A3J2	A7-8
T004	A3J2	A9-10
T005	A3J2	B1-2
T006	A3J2	B3-4
T007	A3J2	B5-6
T008	A3J2	B7-8
T009	A3J2	B9-10
T010	A3J2	C1-2
T011	A3J2	C3-4
T012	A3J2	C5-6

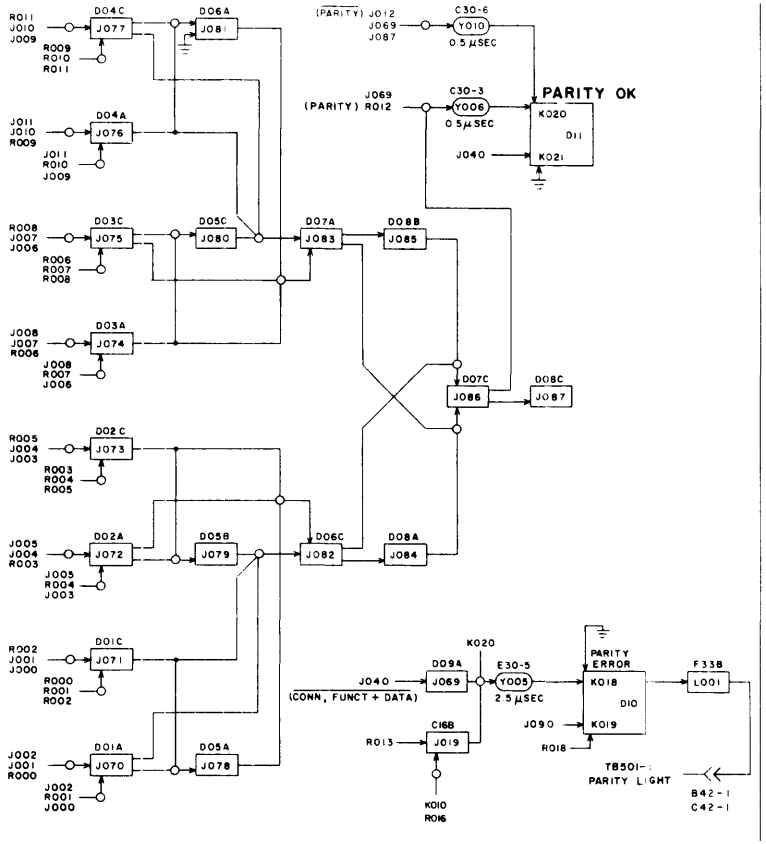
PARITY CHECK

This network determines whether or not a parity error was encountered during the transmission of information (Connect and Function codes) from the data channel. The logic provides for setting the Parity OK FF whenever correct parity has been realized. The state of that FF is then used to sample (test) for the setting of the Parity Error FF. Note that the Parity Error FF cannot be set during a Read operation (R013=1), since there will not be any incoming data for the controller to examine, or during a Function instruction if the controller is not connected. The Parity Error FF is cleared by a Master Clear signal (R018), or when power is turned on (J090).

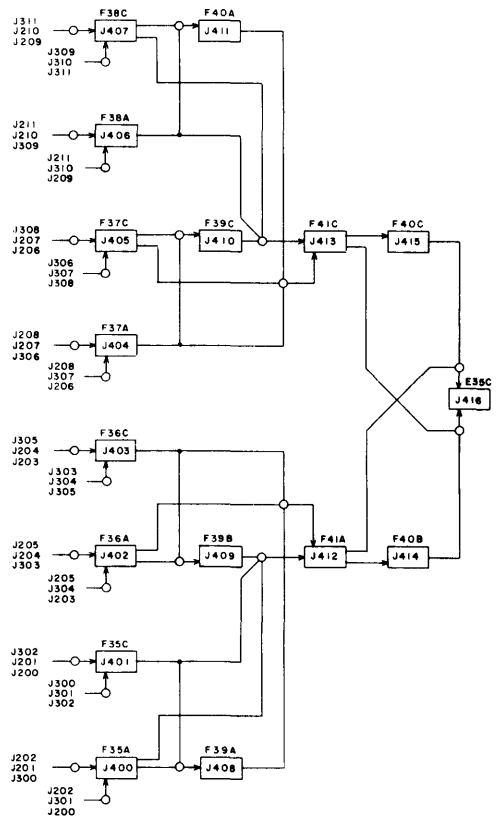
PARITY GENERATOR

Odd parity is maintained on all data transmissions from the controller to the data channel. If the number of bits in the 12-bit byte is even, J416 energizes T012, which puts a parity bit on the data lines. The method of handling this parity bit in the data channel varies in each of the 3000 Series computers. Refer to specific C.E. manuals for more information.

PARITY CHECK

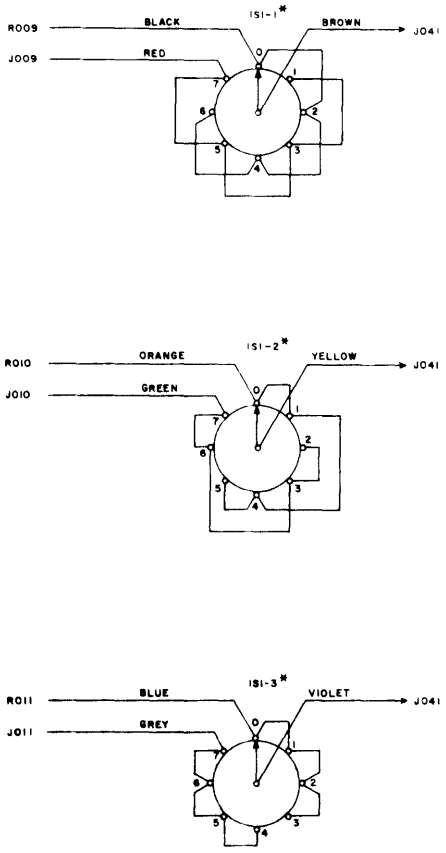


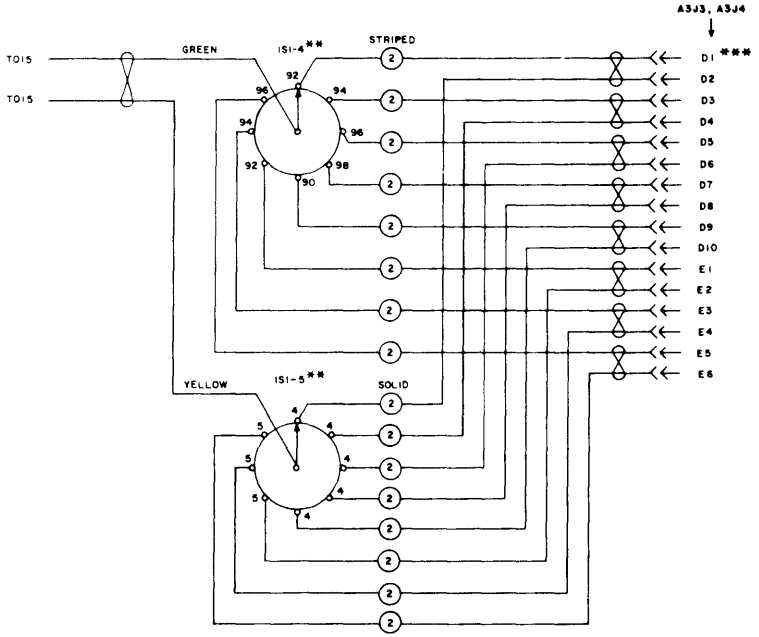
PARITY GENERATOR



PARITY

CONTROL A



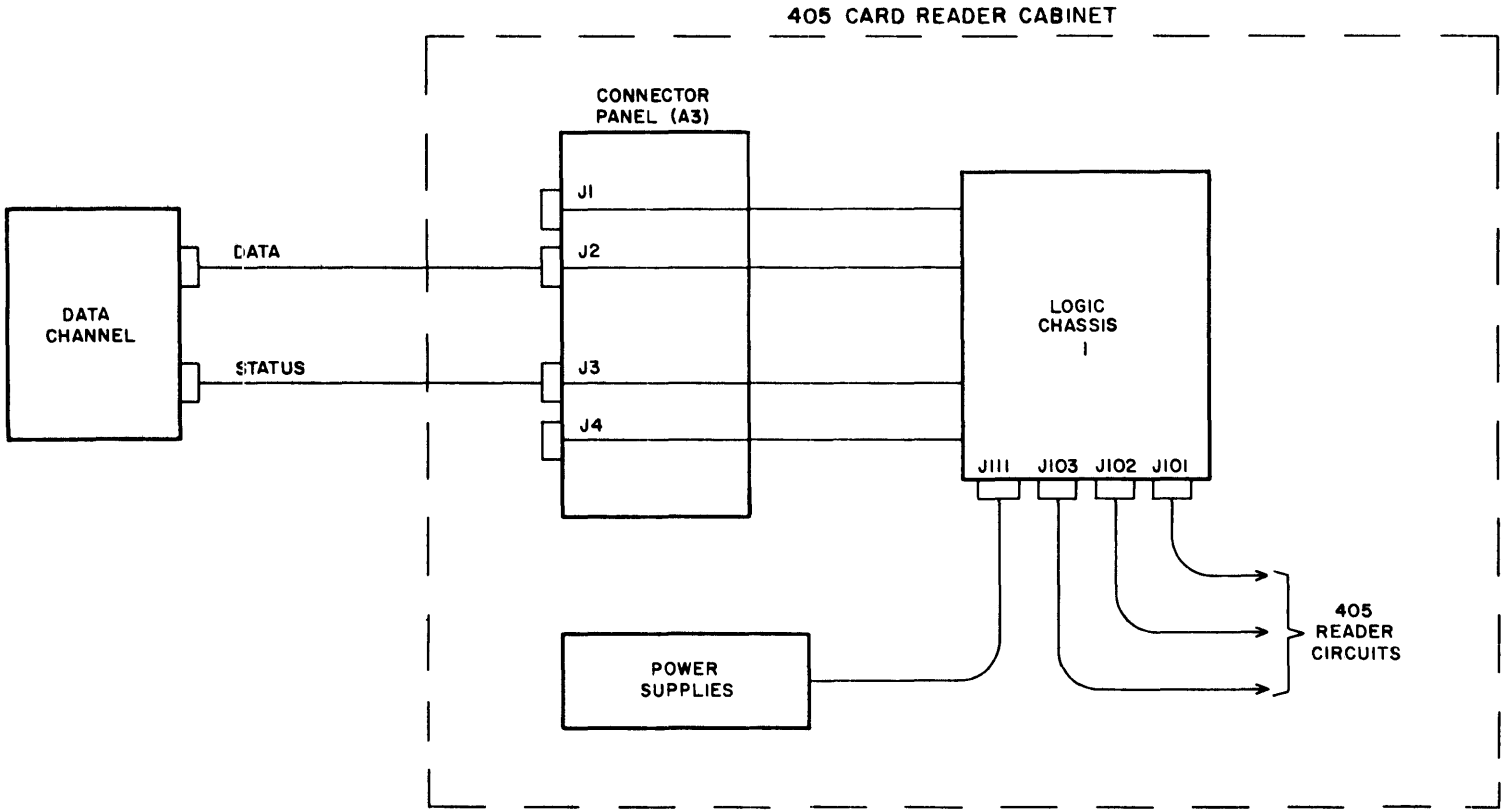


* ON SWITCH SECTIONS 1, 2, AND 3, NUMBERING REFERS TO SWITCH POSITION, NOT PIN NUMBERS.

** ON SWITCH SECTIONS 4 AND 5, NUMBERING REFERS TO COLOR CODE OF WIRES.

*** INTERRUPT LINES (USING TWISTED PAIR WIRES) FEED I/O CABLE CONNECTORS.

EQUIPMENT NUMBER SWITCH



CABLING DIAGRAM

STUDY QUESTIONS

1. Is it possible to negate H→BCD translation after a card has started to read? Why or why not.

2. Status may be checked at any time during the reading of a card.

   > a. true

   b. false

3. How much time is allowed a programmer to decide whether a card just read will be gated to secondary hopper if an error occurs in the 80th column?

   a. 20 ms

   > b. 1.5 ms

   c. 2.0 ms

   d. 15 us

   e. 1.1 ms

4. When reading cards binary, the information first goes to the Hold Register?

   a. true

   > b. false

5. It is possible to read any card and have its data translated to BCD by correct programming of the 405.

   a. true

   > b. false

6. The lack of a 7 and 9 punch in column one of a card tells the controller the card should be read Hollerith, and translated.

   > a. true

   b. false

7. What would the output of the H⟶BCD translator be if the input was a Row 0 and Row 3 punch?

   a. 6300

   b. 63

   >c. 23

   d. 24

8. After receiving a packed BCD word in the Data channel what bits correspond to the first column read?

   a. 2^5 through 2^0

   b. 2^{11} through 2^0

   > c. 2^{11} through 2^6

   d. always the lower bits since the upper bits are used to match the equipment switch number.

9. What is the purpose of the Holding Register during a H - BCD & Pack operation?

   > a. to help assemble one twelve bit word from two columns read

   b. not used during H⟶BCD and Pack operation

   > c. allow us to remember the output of the H⟶BCD translator

   > d. more than one of the above is correct

10. An End of Record signal is sent back to the Data channel along with the reply for the 80th column read to indicate the card read cycle is complete.

    a. true

    > b. false

11. For one card read that has no 7 and 9 punch:

    a. an interrupt will unconditionally be sent to the Data channel after the card is read.

    > b. An End of Record is sent on the Data signal following the 40th word transfer.

    c. same as (b) except the number of Data signals must exceed 80.

    d. more than one of the above is correct.

12. An Interrupt condition can be generated at any time during the reading of a card and sent to the Data channel.

    a. true

    > b. false

13. The delay Y100, located on the set side output of the Pack F/F, could be 5 us in duration and still provide reliable operation of the 3248.

    > a. true

    b. false

14. Malfunction condition: open input pin into P533 (Dark Probe). The probable result would be:

    a. Ready F/F is cleared, but the information transferred to the data channel will continue until the last card has been read.

    b. Ready F/F is cleared, card motion in the 405 will stop.

    c. Card motion continues and the data transfer remains unaffected.

    > d. Card motion will continue in the 405, no information will be transferred to the data channel. Card motion will stop on an abnormal condition.

15. Malfunction condition: The translate F/F P504/505 is always in the set condition. A probable result would be:

    a. Binary read operation would be normal, Hollerith to BCD read operation would be incorrect.

    b. Suppress assy./Dis. assy. operation would send BCD data words over the data lines in the upper 6 bit positions rather than the lower 6 bit positions.

> c. Hollerith to BCD read operation would be normal, Binary read operation would send the incorrect data to the computer.

d. File Card logic circuit would be unable to detect the 7 and 8 punch in Column #1.

16. When an End of File card (7 & 8 punch in Column #1) is sensed, an _____ Interrupt is enabled to be sent to the computer.

a. End of Operation

b. Ready and $\overline{\text{Busy}}$

c. End of Record

> d. Abnormal End of Operation

17. When a Suppress A/D Operation is requested by the Data Channel:

a. each column of Binary data is transferred in the lower six bit positions of the data lines.

b. columns of Hollerith data are translated to BCD and packed into 12 bit bytes to be transferred to the Data Channel.

> c. each column of Hollerith data is translated into BCD data and transferred to the Data Channel in the lower six bit positions of the data lines.

d. the data transferred from the card reader is ignored.

18. When a Function for a Negate H$\longrightarrow$BCD is completed, data

> a. will be transferred to the Data Channel as it appeared on the data card.

b. will be blocked from being transferred to the Data Channel.

c. will be transferred to the Data Channel with even parity.

d. will be transferred to the Data Channel as a gated & packed Binary word.

CHAPTER IV

415 CARD PUNCH

CHAPTER IV

415 CARD PUNCH

INTRODUCTION

The Control Data 415 Card Punch is designed to provide high speed punching of data for permanent storage. The 415 Card Punch contains a high speed transport and punch head capable of punching any combination of punches, up to a fully laced pattern of 960 holes. It can punch, and check-read on demand, at rates up to 250 cards per minute. Included with the high speed transport are the logic circuitry, logic power supply, interlock circuitry, and blowers.

The input hopper has a capacity of 1200 cards and the output stacker has a capacity of 1500 cards. The punch mechanism is designed for punching and check-reading cards, row by row, at demand rates up to 250 cards per minute. Two ready stations along the card path allow for efficient card processing on demand. The first ready station is used to hold a card in readiness for punching. The second ready station is used to hold a card in readiness for check-reading. On a punch demand, simultaneous punching of one card and check-reading of another occurs during the same card cycle with timing pulses controlling each function. At the completion of the punch operation another card will have fed from the input hopper to the first ready station, the newly punched card will have advanced to the check-read ready station, and the card that was just read will have advanced to the output stacker.

Data from the check read station is sent to the punch controller for punch verification. If a comparison error is detected, the off set mechanism can be selected by the programmer to off set the card horizontally so it will enter the output stacker in an off set position from the other cards.

All timing pulses are generated by magnetic pickups. Card tracking and jam detection switches are located along the card path to provide an indication if a card fails to feed properly. Switches on the punch allow various on-line operations to be duplicated for ease of maintenance.

Components in the 415 are protected from over heating by a thermostat interlock located in the cabinet.

Characteristics

1.	Processing Speed	250 cpm
2.	Punch Cycle	240 ms
3.	Punching method	80 bits per row - row at a time for 12 rows
4.	Hopper capacity	1200 cards
5.	Stacker capacity	1500 cards
6.	Power requirements	115 vac, 60 cycle, 1Ø, 6.4 amps
7.	Dimensions	Height 45" Width 21" Depth 39"
8.	Weight	550 lbs.
9.	Punch Cycle/Row	7.1 ms every 15 ms

10. Read timing pulse/row — 2 ms every 15 ms
11. Maintenance aids
    - A. Run cards at 250 cpm
    - B. Punch check
    - C. Read strobe check
    - D. Off set check

FUNCTIONAL DESCRIPTION

The following functional description describes the motion of one card from the input hopper through the card punch to the output stacker. Each of the mechanical assemblies which act on the card as it is transported are located and described as major assemblies of the card punch.

INPUT HOPPER

A card is picked from the bottom of the card stack in the input hopper by a pair of picker knives which grip the rear edge of the card and pass the card through the input hopper throat to the first set of pinch rollers. The throat knife in the input hopper is adjusted to allow only one card of a specific thickness to be picked.

DRIVE ROLLERS

The five sets of drive rollers are spring loaded and adjusted to a gap somewhat less then one card thickness. The bottom roller of each set of drive rollers is driven by a spur gear engaging the main drive shaft on the left side of the unit. The first set of rollers grip the card and pull it through the input hopper throat to the second set of drive rollers.

PUNCH READY (CARD READY 1) STATION

The second set of rollers move the card into the punch ready station, also called the card ready I (CRI) station. When the trailing edge of the card is released by the rollers it drops below the level of a pair of spring loaded lift levers which project above the level of the card path. While moving into the punch ready station (still driven by the second set of pinch rollers) the right and left edges of the card move under guide plates and the leading edge of the card depresses a read switch (CRI). The signal from the CRI switch sends a signal to the punch controller that a card has entered the punch ready station. The rollers continue driving the card until the leading edge of the card is about one half way across the punch die. At this time the trailing edge of the card drops below the level of the lift levers and card motion stops. The card will remain in this position until another feed command is received from the punch controller.

ANTI-JAM MECHANISM

The first card entering the punch ready station raises the bail of the anti-jam mechanism and pivots the trip arm down behind the card. Therefore, if a card is jammed in the punch ready station and a second card is picked, the second card will be shunted up out of the card path by the trip arm. This action of the anti-jam mechanism prevents more than one card jamming in the punch ready station. As the card is moved out of the punch ready

station the bail drops back into the card path and the trip arm is raised.

ALIGNER MECHANISM

When a card feed command is received, the card in the punch ready station is aligned against the 80 column guide on the right side of the card by the aligner mechanism patter on the left side and the card lift lever solenoids are energized for 184 msec by a signal timed and generated by the card punch internal logic. As soon as the card lift levers are depressed the row indexing mechanism starts moving the card through the punch station.

ROW INDEXING MECHANISM

The row indexing mechanism is mounted in the upper housing above the punch ready station. The row indexing shuttles, containing twelve pairs of spring loaded pawls, are constantly driven by an eccentric rotating at 4000 rpm. As the shuttles move toward the input hopper, the pawls move over the surface of the card until behind the card edge. Once behind the card-edge, the pawls drop below the card and, as the shuttle moves toward the output stacker, push the card forward one-quarter inch into position on the punch die. This process recurs 12 times on each card cycle to position each of the 12 rows for punching. Average card speed through the punch station is 1000 inches per minute. Notice that the card is stationary during the time it is punched.

The row indexing mechanism is designed to nudge the card slightly to the right each time the card is moved. This nudging action maintains card contact against the 80 column guide to insure proper punch registration.

The quarter inch stepping motion of the row indexing mechanism continues until all twelve card rows have been punched and the card has been moved across the punch die. At this time the short drive surface of the third set of pinch rollers grips the leading edge of the card and moves the card completely across the punch die and into the read ready station (also called the card ready II (CRII) station).

PUNCH STATION

Punch Head Assembly

The punch station consists of a punch die mounted in the card path and a punch head assembly containing the punch guide, punches, upper and lower toggles, the punch ram and punch ram eccentric, solenoid banks, and the side frames. The punch head is located in relation to the punch die by two large dowel pins press fitted into the ends of the punch die which fit into corresponding holes in the punch guide. The punch guide and punch die are a matched set.

The punch eccentric shaft at the top of the punch head assembly is constantly driven by the punch timing belt at 4000 rpm. The punch eccentric shaft drives the punch ram. Each of the eighty punch pins are connected to the punch ram by a two part linkage consisting of the upper and lower toggle.

The toggle link, which is an extension of the upper toggle, is held up or released by one of the solenoid activated interposers. When a punch command is received from the card punch controller, the interposer solenoid is energized and the interposer is withdrawn from beneath the toggle link. The toggle spring prevents the toggle from pivoting when the punch pin is driven through the card by the punch ram. In the "no punch" condition, the interposer remains beneath the toggle link and the upper toggle pivots rather than driving the punch pin through the card. Twelve punch cycles occur as the card passes through the punch station.

The interposer solenoids and interposers are arranged in four banks (two on each side of the punch eccentric). Each interposer solenoid may be individually activated on command from the punch controller. The interposers ride in an interposer guide at the end nearest the upper toggle links. The interposers are held beneath their associated toggle links by a spring on the solenoid clapper.

PUNCH TIMING

A punch command is received from the punch controller when the punch ram is at bottom dead center (BDC). As the interposer solenoid magnetic field is building up, the punch eccentric is rotating toward top dead center (TDC). As the punch eccentric approaches TDC the toggle link lifts from the interposer and the interposer is withdrawn from beneath the toggle link. At TDC the toggle linkage is held straight by the toggle spring. The punch now begins it downward motion and the current to the solenoid is terminated. The interposer is held back by residual magnetism in the solenoid. As the punch continues downward the interposer starts forward motion at a time where the toggle link gap is closed and the interposer may not be reinserted beneath the link. The punch pin penetrates the card before the punch reaches BDC and continues through into the guide.

If the next row is to be punched the interposer solenoid is again pulsed and the process described above is repeated. If the next row is not to be punched the interposer solenoid is not pulsed and, as the punch eccentric approaches TDC, the interposer is reinserted beneath the toggle link by the force of the interposer return spring. As the punch eccentric passes TDC and starts its downward travel the toggle link contacts the interposer and the upper toggle pivots. This prevents the punch from contacting the card as the ram moves downward on the punch stroke.

READ READY (CARD READY II) STATION

After punching, the card remains in the read ready station until another card feed command is received from the punch controller. The upper roller of the third set of drive rollers is held up and out of contact with the card by a pair of follower arms which rest on cam lobes on the right and left sides. The bottom roller is continuously driven but card motion is halted until the upper roller is lowered. When a feed command is received, a solenoid in the read ready clutch mechanism (located on the left side) is activated and the cam is allowed to revolve. As the cam revolves the follower arms drop off the cam lobes and the third upper drive roller moves

down in position to drive the card across the segmented plate of the read station. The upper roller is dropped at a time when the leading edge of the larger drive surface of the lower roller is just approaching top dead center.

READ STATION

The read station consists of a read brush assembly mounted in the upper housing and a segmented plate mounted in the card path. The read brush assembly consists of 80 read brushes wired in common. The segmented plate consists of 81 beryllium copper segments insulated from one another. Eighty of the segments are wired to an output cable to the punch controller. The eighty-first segment is no longer used.

As a card passes through the read station, the brushes ride across the card (one brush for each card column). The 80 read brushes receive 2 millisecond ground level pulses at the time when the brushes are approximately in the center of the holes punched on the row being read. When a punch is present the segmented plate picks up the ground pulses and sends them to the controller through the output cable. This is repeated 12 times until all 12 rows are read. The card does not stop as it is being read.

OFFSET STATION

As the card passes out of the read station it is driven into the offset station. At this point a mechanism similar to the aligner mechanism will push the card to the right if a signal is received from the controller. A relieved portion of the final drive roller allows the card to be pushed to the side before it is gripped by the final drive rollers.

STACKER DISK ASSEMBLY

The final (fifth) drive roller carries the card out of the offset station and moves it forward to the stacker disk assembly.

The stacker disk assembly consists of two disks which are driven by the main drive motor and revolve between guards on the assembly. The stacker disks have 5 sets of cam actuated, spring loaded, steel clamps, which each set opens and closes at the correct time to grip the card from number 5 drive roller and releases it in the output stacker.

OUTPUT STACKER

The output stacker receives the cards from the stacker disk assembly. The cards are received at the bottom of the stack as the stacker disks revolve between the guards. Maximum capacity of the output stack is approximately 1500 cards. A toggle switch at the top of the stacker provides an output stacker full signal to the controller and stops card feeding when the card weight reaches the top of the stacker.

CABINET COOLING SYSTEM

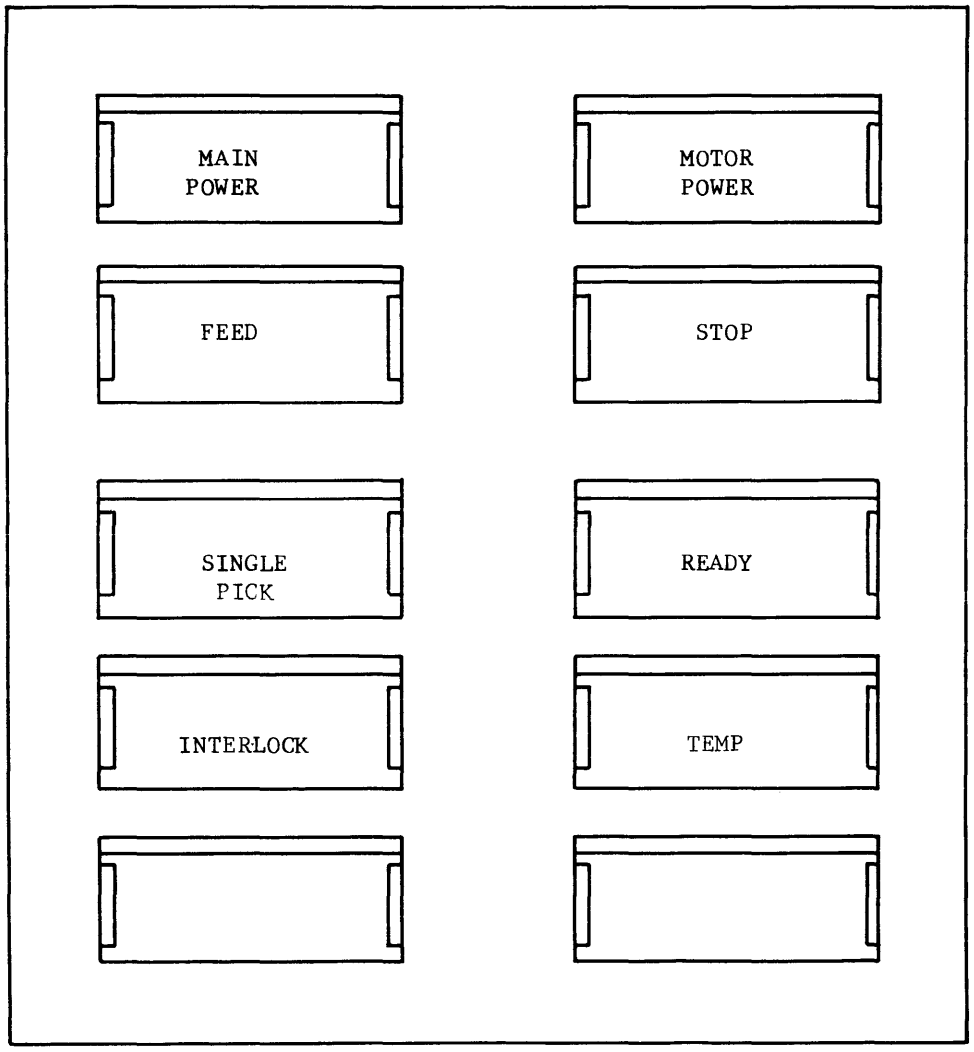
A forced air cooling system circulates room temperature air throughout the card punch cabinet. Air is drawn into the plenum through a filter at the

front base of the cabinet. The blower unit distributes the filtered air up along the logic chassis and by a duct to the power supply at the rear of the cabinet. The air is exhausted through a grill on the back side of the cabinet.

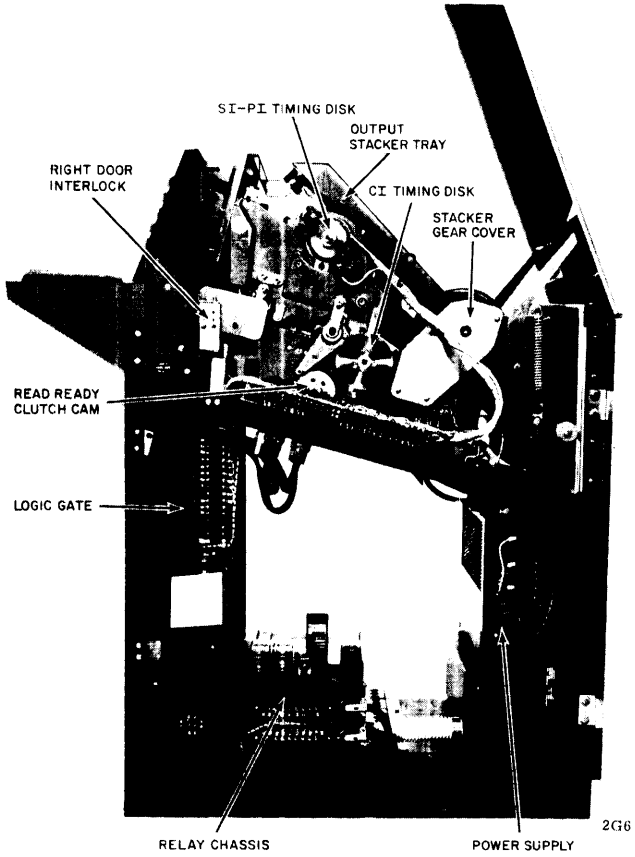
CONTROLS AND INDICATORS

All controls and indicators required for operating the card punch are mounted on the operator control panel, shown in figure 3-1, which is located to the right of the input hopper.

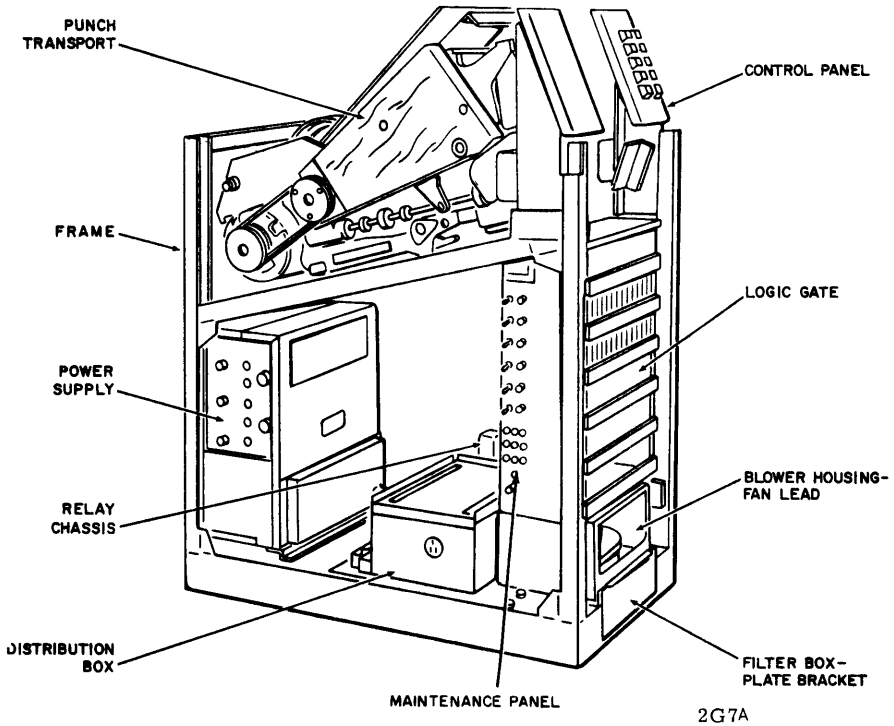
CONTROL AND/OR INDICATOR	FUNCTION
Main Power indicator lamp/ pushbutton	Power is applied to the cooling fans and d-c power supplies when the Main Power pushbutton is depressed. The indicator lamp indicates that the power is on.
Motor Power indicator lamp/ pushbutton	One of the conditions for starting the 1/3 hp motor is met when the Motor Power pushbutton is depressed. The indicator lamp indicates that this condition has been met.
Feed indicator lamp	The Feed indicator lamp lights when a card jam exists.
Stop indicator lamp/ pushbutton	The card punch provides the controller with a not ready signal when the stop pushbutton is depressed and stops feeding cards. The indicator lamp goes out when the Ready pushbutton is depressed.
Single Pick indicator lamp/ pushbutton	Cards are advanced one cycle when the Single Pick pushbutton is released. The indicator lamp lights when the pushbutton is depressed and remains lit until the cards have advanced one cycle.
Ready indicator lamp/ pushbutton	The card punch logic is cleared when the Ready pushbutton is depressed. The indicator lamp lights after the logic is cleared and the card punch is ready for on-line operation.
Interlock indicator lamp	The Interlock indicator lamp lights when the head, hood or right door is open.
Temp indicator lamp	The Temp indicator lamp lights when the card punch temperature exceeds 110° F. The motor and power supply are shut down.



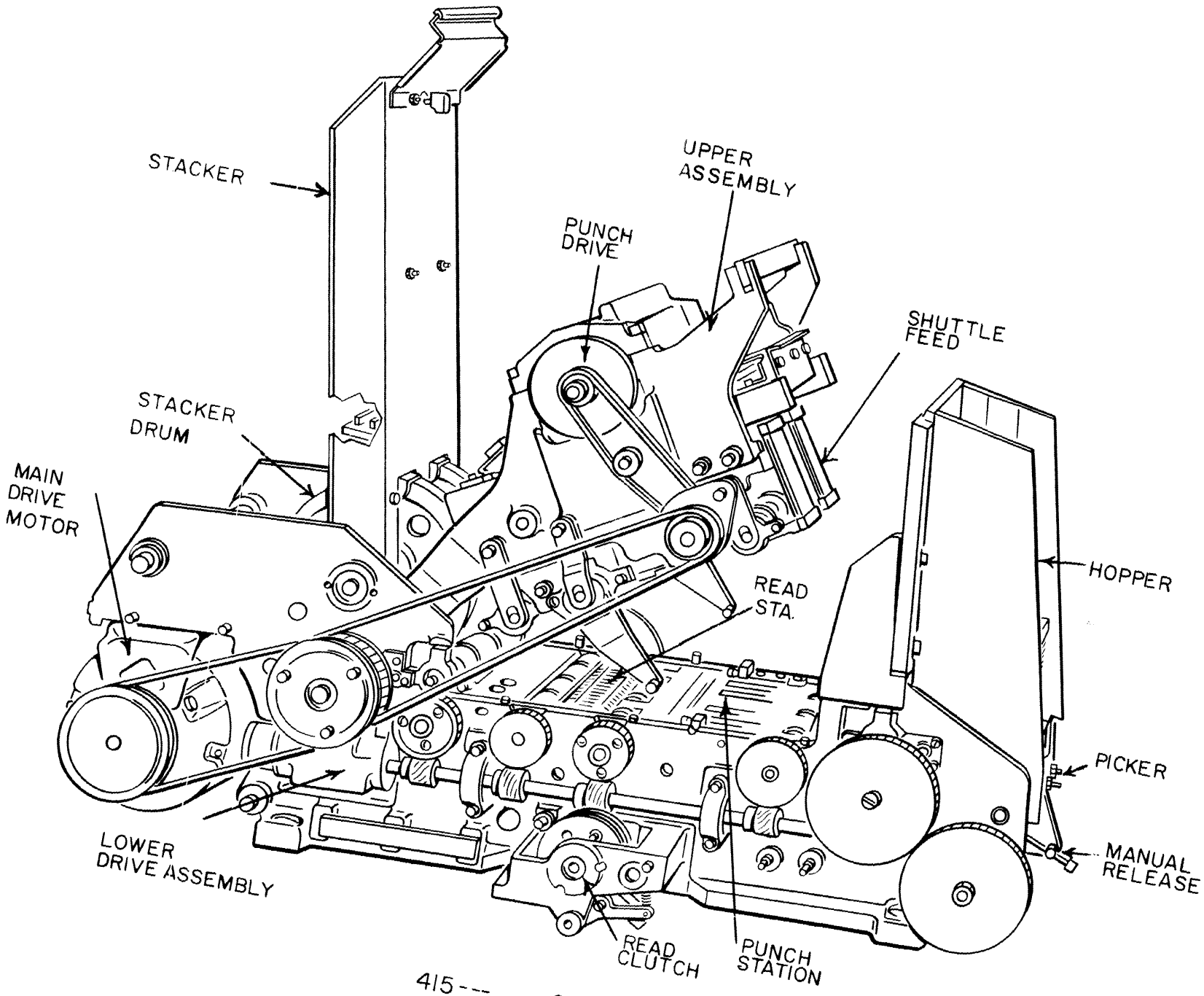
OPERATOR CONTROL PANEL



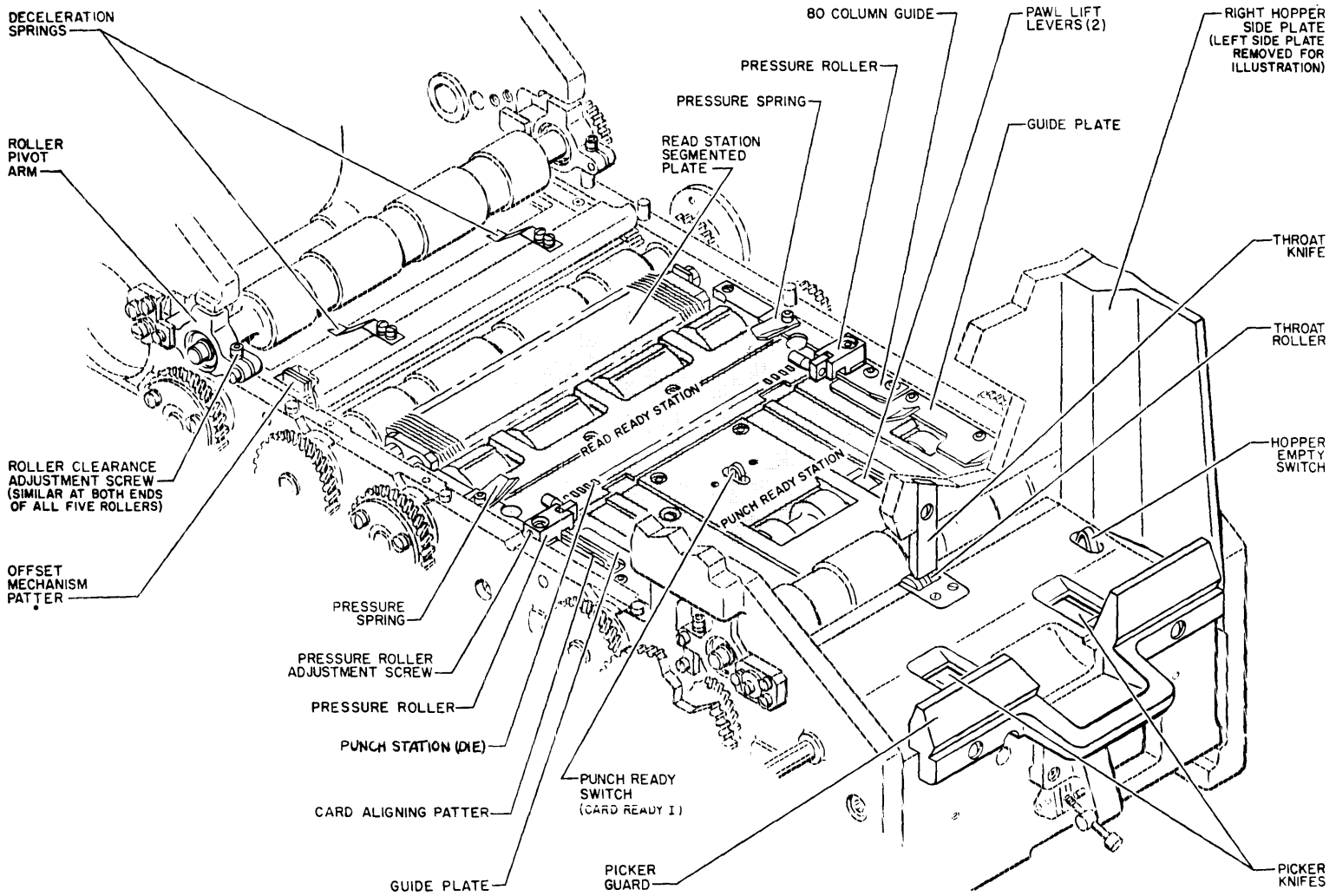
Card Punch (Right side)



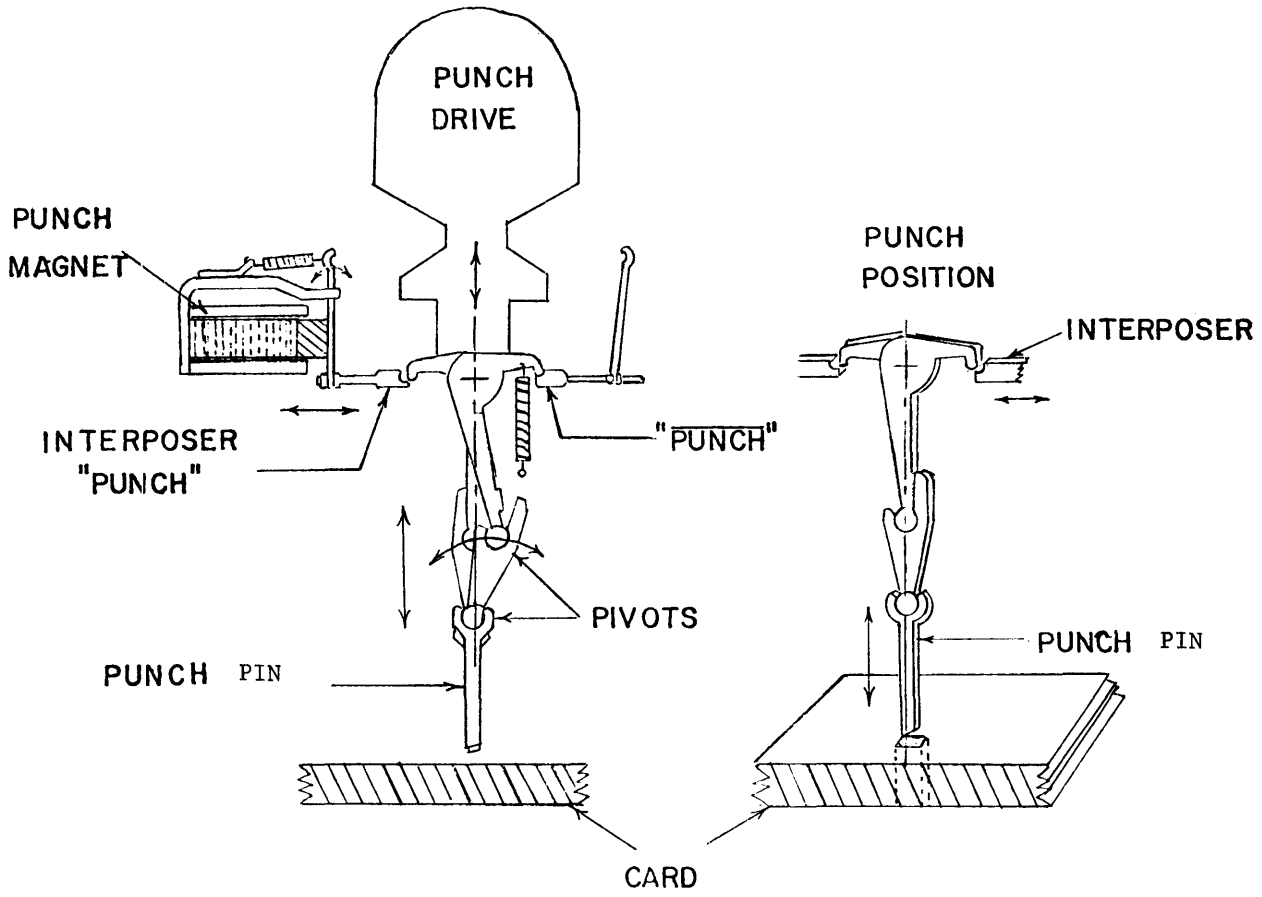
Card Punch (Left side)



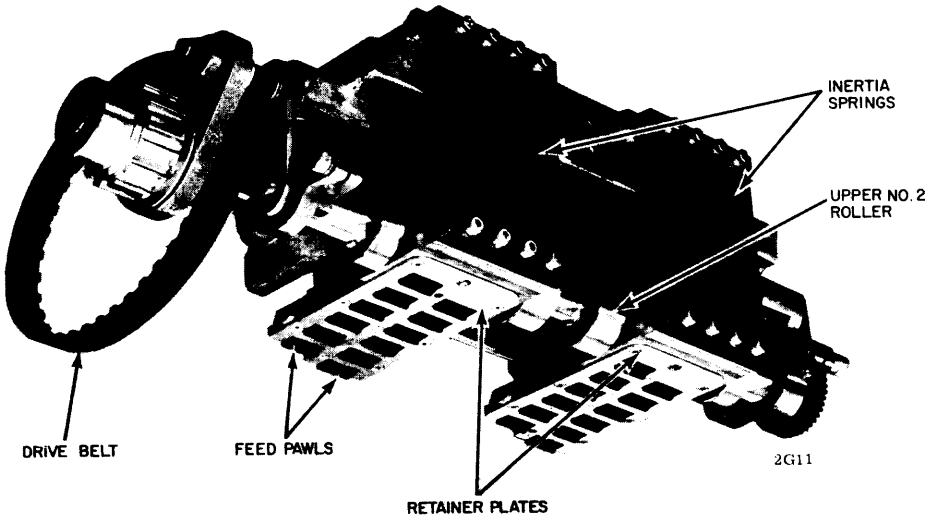
415 --- --OPEN VIEW



CARD PATH - - - - LOWER ASSEMBLY



PUNCH LINKAGE DIAGRAM



Row Indexing Mechanism

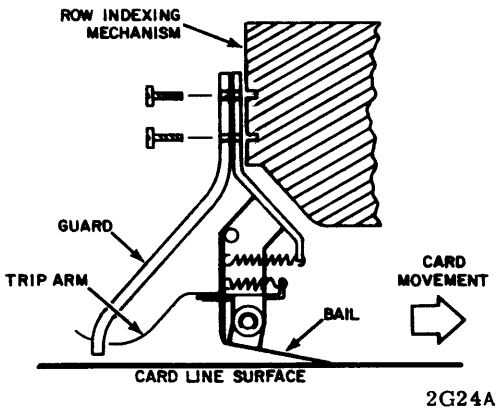
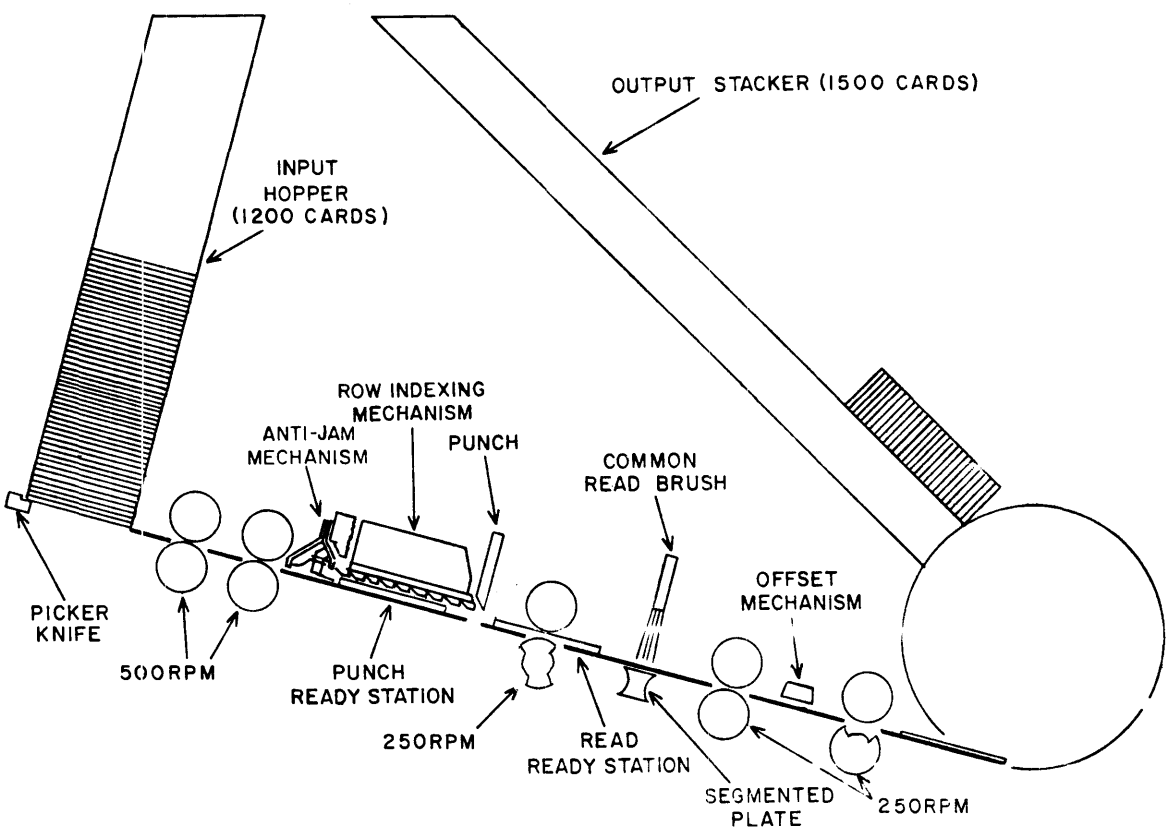
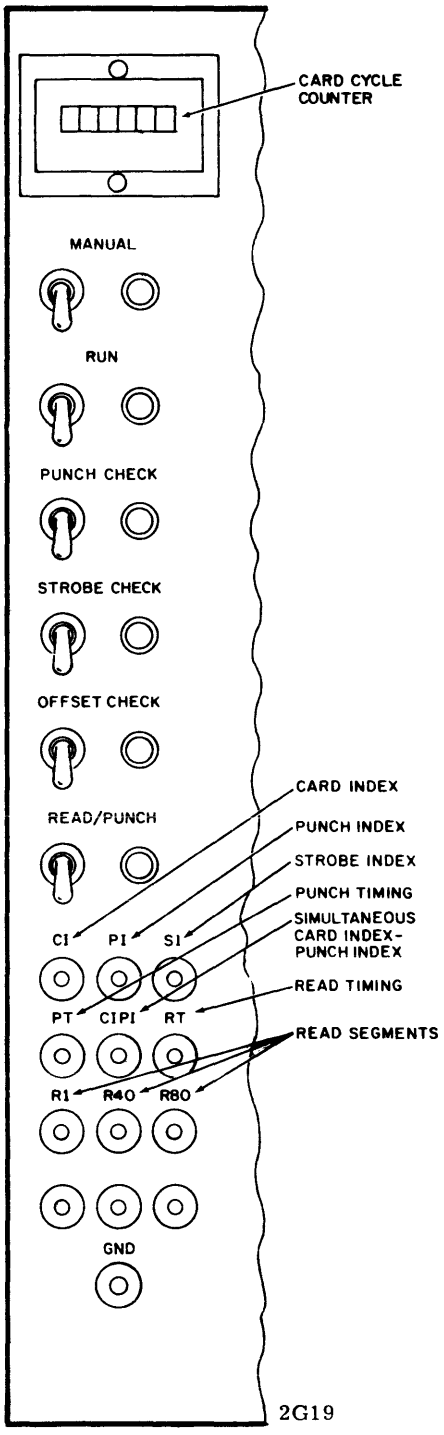


Figure 6-4. Anti-Jam Mechanism Removal



BLOCK DIAGRAM 415 CARD PUNCH

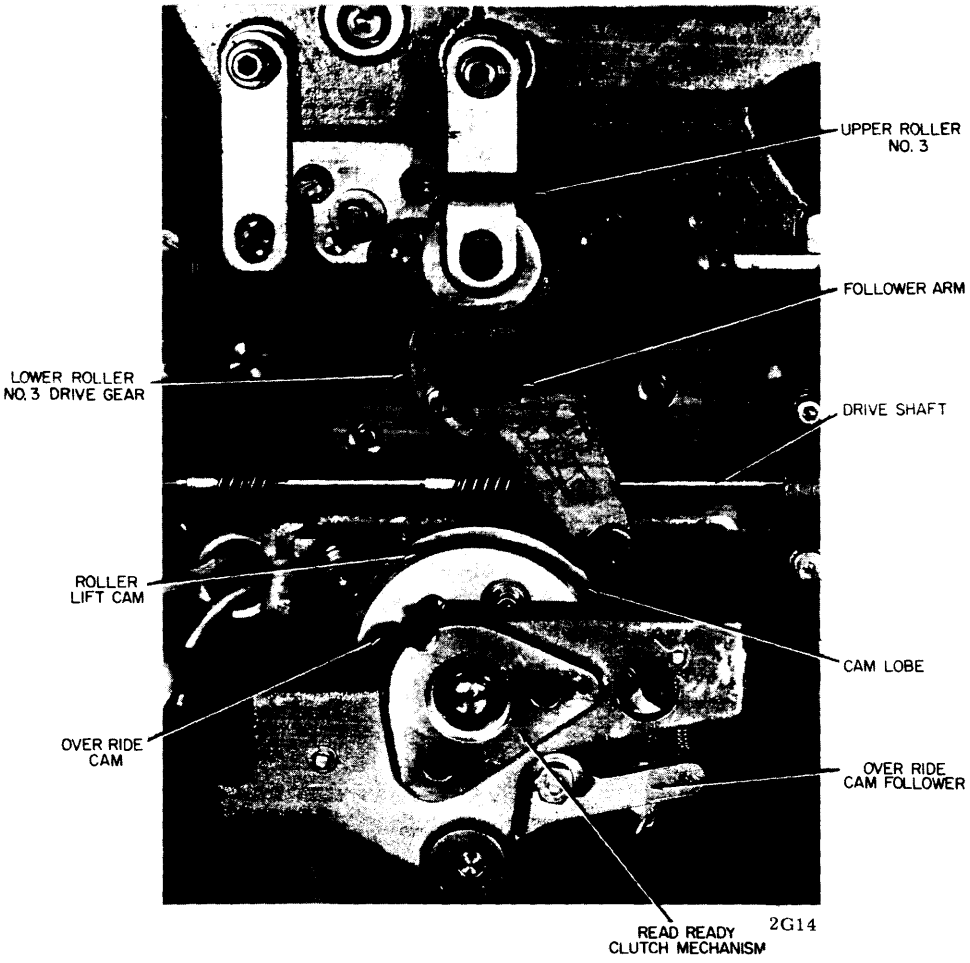


Maintenance Panel

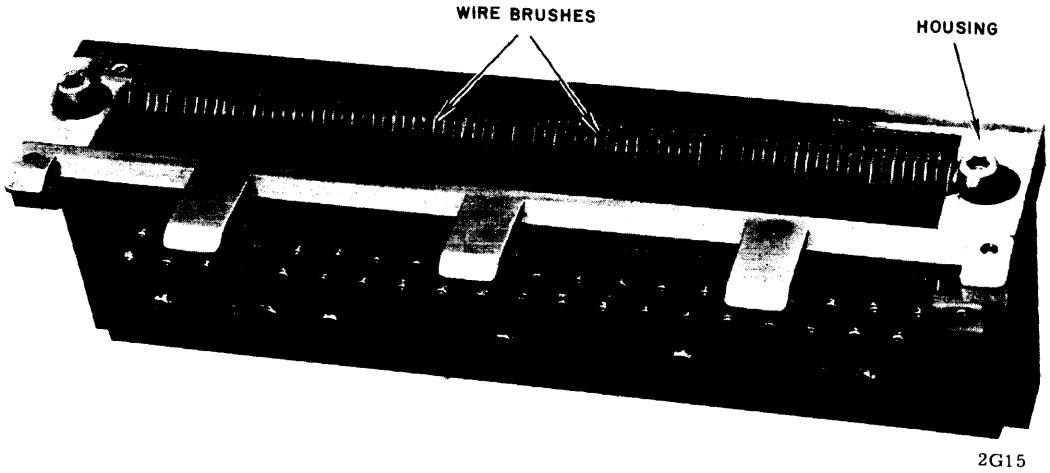
Maintenance Panel Controls and Indicators

CONTROL AND/OR INDICATOR		FUNCTION
Card Cycle Counter	I*	Counts picker cycles (cards picked).
Manual	S**	On (up) - Removes the unit from punch controller control. The unit may now be run from the maintenance panel. Off (down) - Returns the unit to the control of the punch controller.
	I	The indicator is lit when the Manual switch is on.
Run	S	This switch is used in conjunction with the Manual switch. The Manual switch must be on to enable the Run switch. On (up) - Cards are run at the rate of 250 cards per minute.
	I	Cards are being run at the maximum demand rate.
Punch Check	S	The left cabinet door must be open to enable the switch. On (up) - All 12 row positions in columns 1, 40, and 80 are punched.
	I	Cards are punched in columns 1, 40, and 80.
Strobe Check	S	The left cabinet door must be open to enable the switch. On (up) - Grounds the read brushes. Off (down) - Removes the ground signal from the read brush.
Offset Check	S	The left cabinet door must be open to enable the switch. On (up) - Activates the offset mechanism to offset cards in the output stacker.
Read/Punch	S	The Read/Punch toggle switch does not have a special function at this time. The Read/Punch toggle switch should be left in the Off (down) position.
CI	TP***	Card index timing pulses may be read from this point with an oscilloscope.
PI	TP	Punch index timing pulses may be read from this point with an oscilloscope.
SI	TP	Strobe index timing pulses may be read from this point with an oscilloscope.
PT	TP	The punch timing pulses to the controller may be viewed with an oscilloscope at this point.
CIPI	TP	The card index/punch index timing pulse may be viewed with an oscilloscope from this point.
RT	TP	The read timing pulses to the controller may be viewed with an oscilloscope at this point.
R1, R40, R80	TP(s)	The read signal on segments 1, 40, and 80 of the read station may be viewed with an oscilloscope at this point.
Gnd	TP	Provides an access to ground for meter usage.

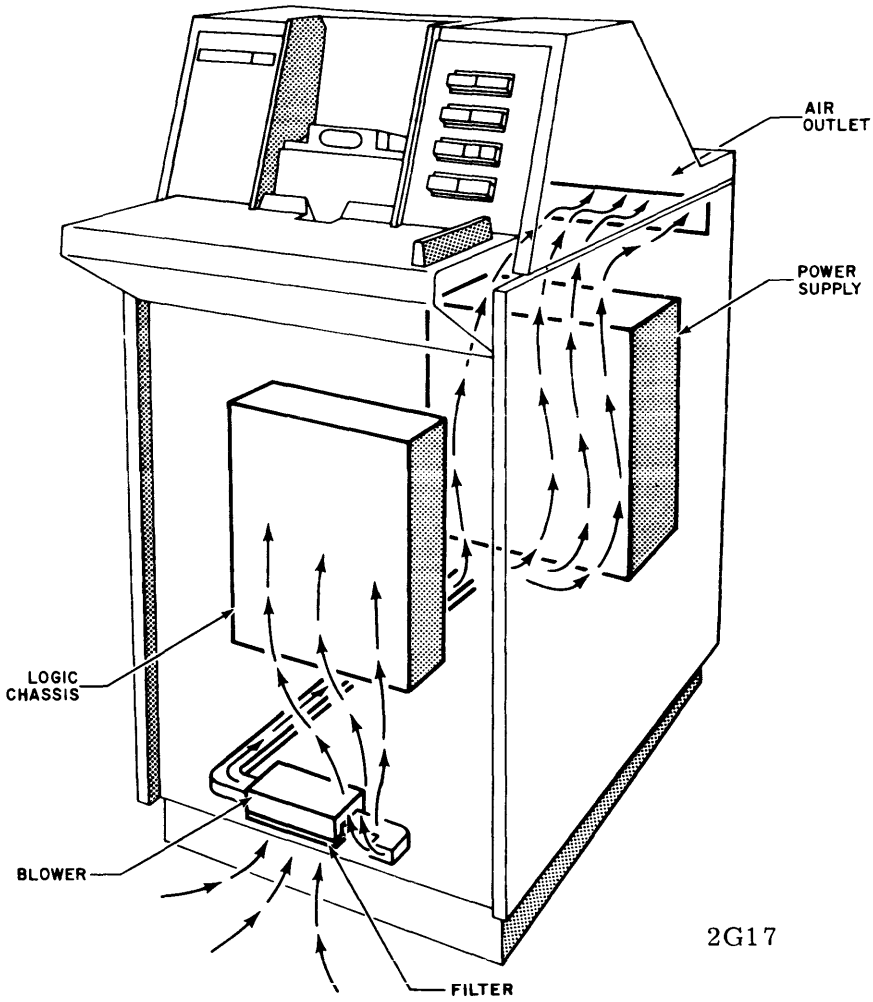
*Indicator
**Switch
***Test Point



Read Ready Clutch Mechanism



Read Station Wire Brush Assembly (Shown Inverted)

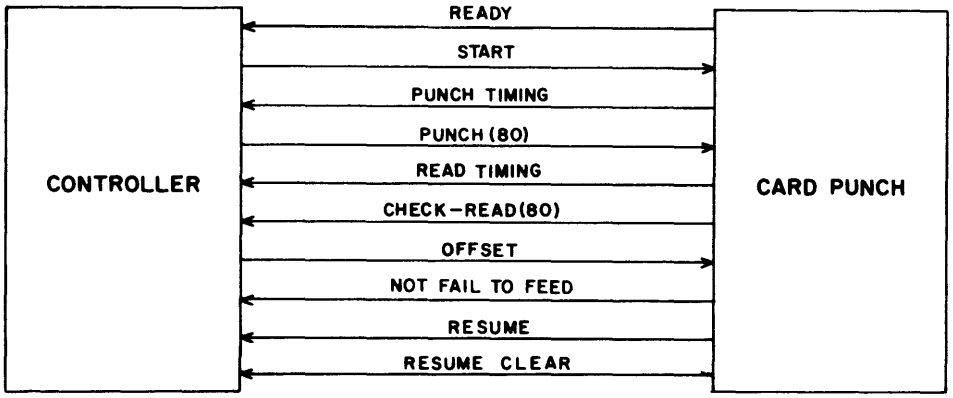


Cabinet Cooling System

LOGIC DESCRIPTION

For purposes of discussion, the logic is presented in two major sections: ready logic and timing logic. All logic circuits are directly related to one, or both, of these sections.

Refer to the simplified block diagram showing all demand and response lines between the card punch and associated controller. The controller is not part of the card punch.



Card Punch and Controller Demand and Response Lines

READY LOGIC

A card is fed through each station in the card punch each time a start signal is received from the controller. The controller cannot send a start signal until it receives a ready signal from the card punch. The ready signal is developed by the ready logic shown in Figure 1. The Ready FF is set when all of the following conditions are met:

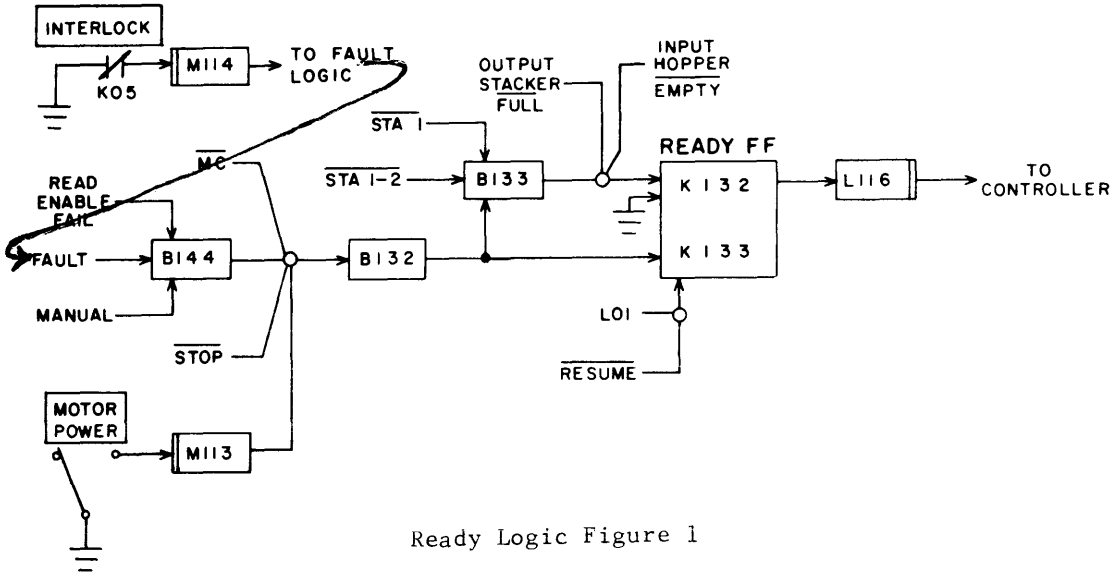
1. The input hopper contains cards
2. The output stacker is not full
3. The ready station 1 and 1-2 FF's are set
4. The output from B132 is a "0"

The Ready FF is cleared at the end of each punch cycle by the L01 and $\overline{\text{Resume}}$ pulses, or when any of the following conditions exist:

1. The Fault FF is set
2. The Manual toggle switch on the maintenance panel is On
3. The Stop FF is set
4. The Ready pushbutton on the operator control panel is depressed

5. The Read Enable Failure FF is set
6. The Motor Power switch is Off
7. The Interlock circuit is open

The output from the Ready FF is applied to output card L116 which converts the standard logic voltages into suitable potentials for transmission of the Ready signal, via an input/output cable, to an input card in the controller.

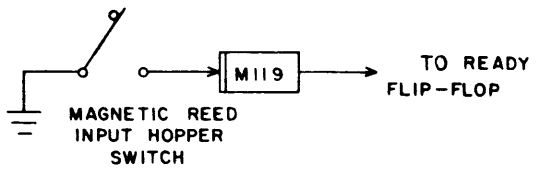


Ready Logic Figure 1

Input Hopper Logic

A magnetic reed switch, located in the bed of the input hopper, provides an input hopper indication to the Ready FF and causes the card punch to go Ready after the last card is fed from the input hopper.

The Input Hopper switch, shown in Figure 2, is closed when the input hopper contains cards and a ground signal is applied to M119. M119 outputs a "1" when the ground input is present and it will output a "0" when the ground input is absent (open). The "1" output resulting from the closed input hopper switch is applied to the Ready FF (K132) and must be present for the card punch to have a "Ready" condition.

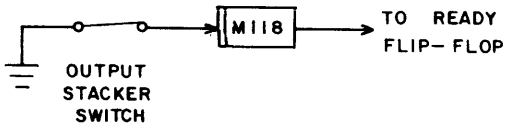


Input Hopper Logic Figure 2

Output Stacker Logic

An output stacker switch, located on the back of the output stacker tray, provides an output stacker full indication to the ready logic when the tray reaches maximum card capacity.

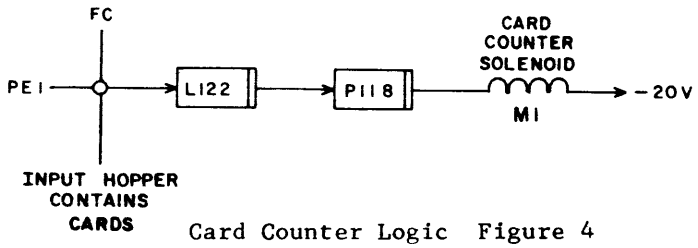
The output stacker switch, shown in figure 3, opens when the tray is full and the ground input signal is removed from circuit card M118. Circuit card M118 switches to a "1" when a ground input signal is present and to a "0" when the ground signal is not present. The "0" output resulting from the open output stacker switch disables the ready flip-flip (K132) and the card punch has a not-ready indication.



Output Stacker Logic Figure 3

Card Counter Logic

The card counter display is located on the maintenance panel and provides an accurate count of the number of cards punched. The L122 card pulses the puller card, P118, on each card cycle when cards are being fed. The card counter solenoid is energized by the -20 volt d-c potential each time P118 conducts to ground (once for each card fed).



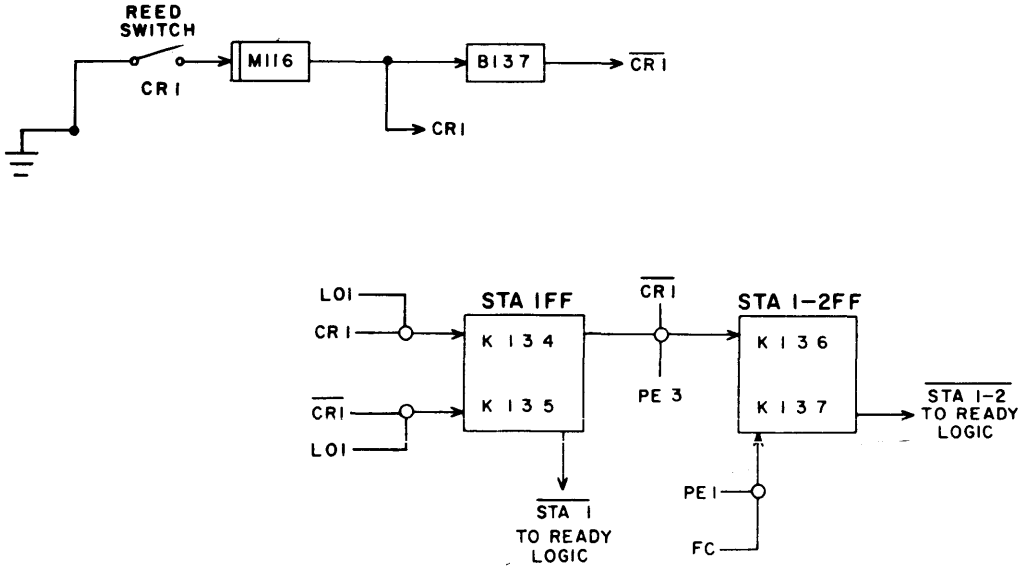
Card Counter Logic Figure 4

Ready Station Logic

The ready stations provide indications when a card enters the punch ready station (STA-1 F/F) and when a card leaves the punch ready station and proceeds to the read ready station (STA 1-2 F/F). The CR1 magnetic reed switch contacts are shown in figure 5 with no card in the punch ready station.

When a card is in ready station 1 and ready to pass through the die station, the CR1 switch is closed, causing the M116 output to switch from "0" to "1". The STA 1 flip flop is set when the CR1 switch is closed and the lockout 1 flip flop is set (at the end of each card cycle). The STA 1 flip flop is cleared only if another card does not close CR1 in the next cycle. Since the lockout 1 flip flop is set at the end and at the beginning of each cycle, the STA 1 flip flop is always set when a card is in Ready Station 1.

The STA 1-2 flip flop is cleared at the beginning of each punch cycle and must be set again (on the same cycle) if the card punch is to remain ready. The STA 1-2 flip flop is set when the card leaves ready station 1. The STA 1 and STA 1-2 flip flops must be set in order to partially enable the ready logic.

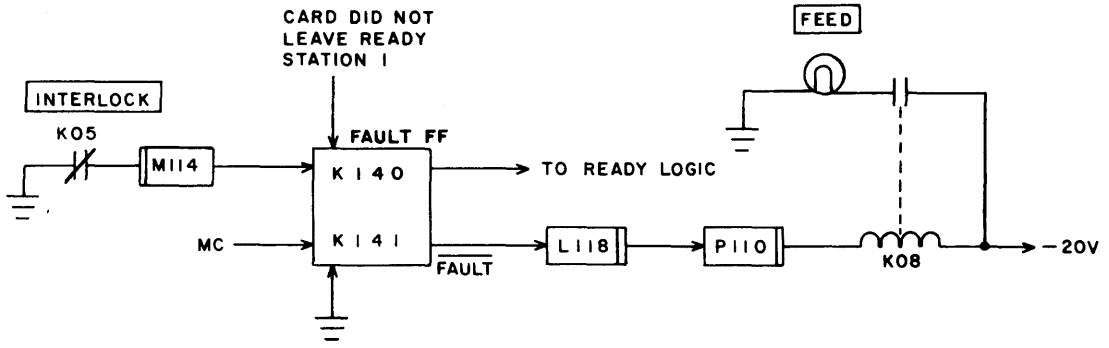


Ready Station Logic Figure 5

Fault Logic

The Feed indicator lamp on the operator control panel lights whenever a fault condition exists. The fault flip-flop, shown in figure 6, is set when an interlock is open or when a card does not leave ready station 1 at the proper time. If the fault flip-flop is set, L118 provides a -16 volt d-c potential to relay puller P110. P110 then conducts to ground and the feed relay, K08, is energized by the -20 volt d-c potential. The energized K08 relay drops relay K03, causing the motor power to shut down.

A fault condition also causes the fault flip-flop to disable the AND-gate to B132 (figure 1), producing a card punch not-ready condition.



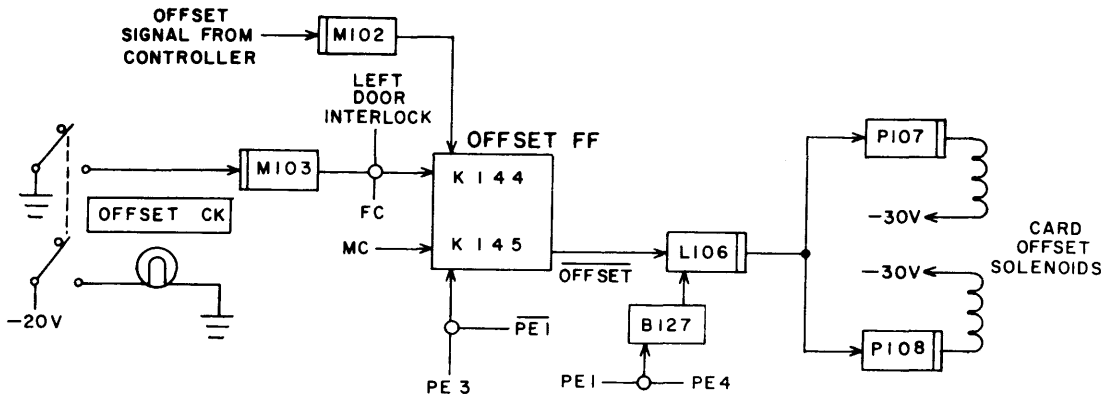
Fault Logic Figure 6

Card Offset Logic

The card offset solenoid signal is a 30 volt d-c, 600 milliampere pulse. If the controller is programmed to do so, it sends an offset signal to input card M102 to set the offset flip-flop (figure 7). L106 then provides a -16 volt d-c potential to relay pullers P107 and P108, causing the relay pullers to conduct to ground. The card offset solenoids are energized at time 4 of the timing chain and de-energized at time 5 by the -30 volt d-c potential. The offset mechanism is actuated in this manner and deflects the card to an offset position before it arrives in the output stacker tray.

The PE1 flip-flop is cleared by the fifth PI pulse. This clears the offset flip-flop, causing the offset solenoids to be dropped.

An offset ck toggle switch on the maintenance panel provides a means for checking the card offset operation. During normal operation, M103 produces a "0" to the AND-gate of K144. M103 switches to a "1" when the Offset ck toggle switch is turned on, enabling the AND-gate and setting the offset flip-flop.

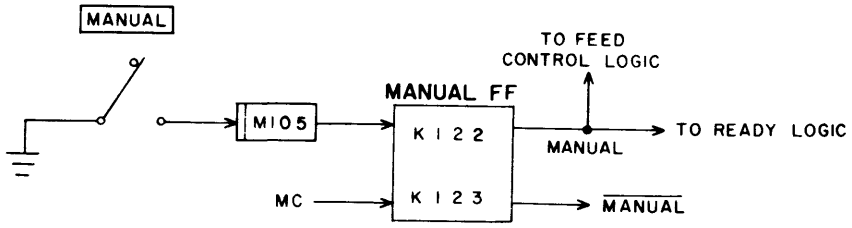


Card Offset Logic Figure 7

Manual Logic

The Manual toggle switch is used in conjunction with other switches on the maintenance panel to test various logic circuits. Input card M105 switches to "1" when the Manual toggle switch is closed. The "1" sets the manual flip-flop, shown in figure 8, disabling the AND-gate to B132 (figure 1). A card punch not-ready condition exists whenever the Manual toggle switch is closed, stopping on-line operation.

The manual signal is a mode condition which enables maintenance personnel to actuate the run logic and manually feed cards through the card punch.

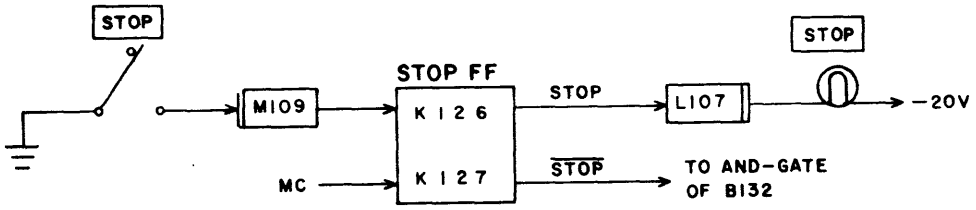


Manual Logic Figure 8

Stop Logic

Card feeding can be stopped by depressing the Stop pushbutton on the operator control panel. A ground signal causes input card M109, shown in figure 9, to switch to a "1" which sets the stop flip-flop. The "0" from K126 of the stop flip-flop disables the AND-gate to B132, clearing the ready flip-flop and preventing the feed control logic from being set by the controller. The Stop indicator lamp lights when the stop flip-flop is set.

The stop flip-flop remains in the set state until cleared by depressing the Ready pushbutton.

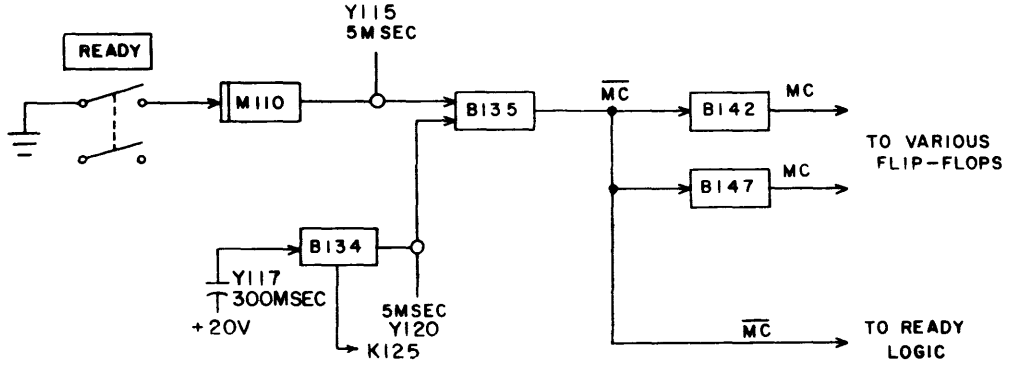


Stop Logic Figure 9

Master Clear Logic

All flip-flops in the card punch logic section are cleared by depressing the Ready pushbutton on the operator control panel (the ready flip-flop may set again when the Ready pushbutton is released). The master clear signal breaks the AND-gate to B132 (figure 1) which clears the ready flip-flop. A 5 millisecond delay, caused by Y115, eliminates any noise in the master clear logic.

Circuit card B134, shown in figure 10, is used to master clear the logic circuits when the power supply is turned on. The "1" output from B134 lasts for approximately 300 milliseconds until Y117 charges, causing B134 to switch to "0".



Master Clear Logic Figure 10

TIMING LOGIC

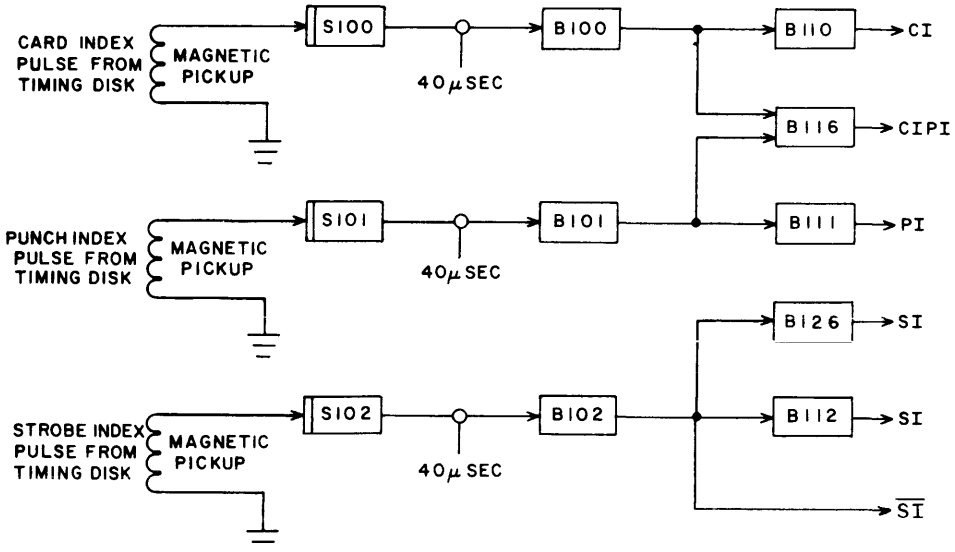
Card Index Logic

Two card index (CI) pulses are generated by the transport every 240 milliseconds from a timing disk. CI pulses provide the timing required for starting row operations. The timing disk operates in conjunction with the magnetic pickup shown in figure 11. One of the CI pulses is coincident with the punch index (PI) pulse and denotes the beginning of a card cycle. The CI pulse not coincident with the PI pulse denotes the end of a card cycle and occurs approximately 206 milliseconds after the coincident pulses.

The irregular pulses from the timing disk are applied to circuit card S100 where they are converted to square waves with logic level voltages. After a delay of 40 microseconds, the square wave pulses are inverted and applied to various logic circuits in the card punch.

Punch Index Logic

Sixteen punch index (PI) pulses are generated every 240 milliseconds by a one-point timing disk which is mounted on the 4000 rpm eccentric shaft. Sixteen pulses occur during each machine cycle. The first PI pulse is coincident with the CI pulse and denotes the beginning of a card cycle. PI 3 is the first punch magnet energize time. Each PI pulse thereafter, for the next twelve, is the beginning of punch magnet energize time (the 7.1 millisecond period during which the punch magnets pull the interposer arms). The actual driving of the punch die is determined by the punch eccentric.
The irregular PI pulses from the timing disk are applied to circuit card S101, as shown in figure 11, where they are converted to square waves with logic level voltages. After a delay of 40 microseconds, the square wave pulses are inverted and applied to various logic circuits.



Card Index, Punch Index and Strobe Index Logic Figure 11

Picker Enable Logic

Cards are picked, one at a time, from the bottom of the input hopper by two self-aligning knives which are attached to the carriage. The carriage is actuated by a cam reset linkage which is controlled by a solenoid-actuated interposer. The Pick Enable FF's provide the necessary timing for:

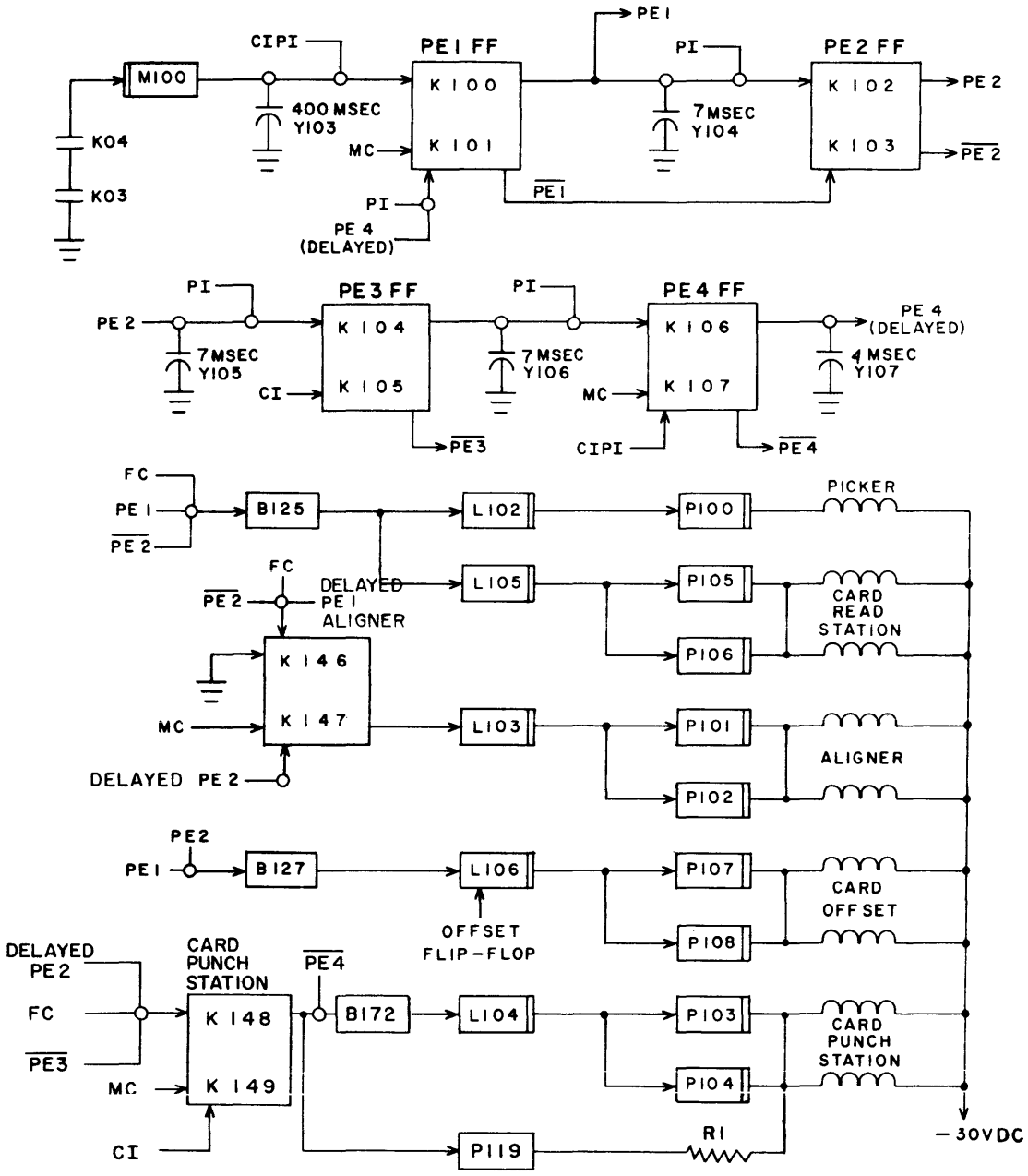
1. Energizing the solenoids
2. Clearing the following FF's:
    a. Lockout
    b. Resume

Picker Enable FF's PE1, PE2, PE3, PE4, shown in Figure 12, set and clear continuously. After the motor is running and relays K03 and K04 have been energized, a 400ms delay holds the pulses until the motor comes up to speed. Although the Picker Enable FF's are free-running when the motor is up to speed, the solenoids are not energized unless the Feed Control FF is set.

The PE1 FF is set by the first coincident C1 and P1 pulses. The PE2 FF is set by the second P1 pulse which occurs 15ms later. The third P1 pulse sets PE3 and the fourth P1 pulse sets PE4. The PE1 FF is cleared by the fifth P1 pulse which, in turn, clears the PE2 FF. PE3 is cleared by the C1 pulse, which occurs just prior to the fifteenth P1 pulse. This indicates the end of punch and read operations for the twelve row card. The second coincident C1 and P1 pulses clear PE4 at the start of the next cycle.

Solenoid Logic

The picker and card read station solenoids, shown in Figure 12, are energized from the time PE1 is set, until PE2 sets (providing the Feed Control FF is set). This interval is 15ms at the start of each punch cycle. The aligner solenoids are energized 7ms after PE1 sets, and remain energized until 7ms after PE2 sets. The card punch station solenoids are energized 7ms after PE2 sets and remain energized until end of card CI pulse occurs. The card offset solenoids are energized from the time PE4 is set until PE1 clears (providing the Offset FF is set). The output cards convert the standard logic voltages to levels suitable for operating the relay pullers. The solenoids are energized by the -30 volt d-c potential when the relay pullers conduct to ground.



Picker Enable and Solenoid Logic Figure 12

Strobe Index Logic

Strobe Index (SI) pulses are generated every 15 milliseconds by the same timing disk which generates PI pulses (a second magnetic pickup is used). SI pulses generally occur 7.5 milliseconds after PI pulses.

Essentially, the third through fourteenth SI pulses indicate that the check-read brushes have made contact with the segmented plate for each of the twelve rows and it is time to strobe the brushes. The check-read brushes are strobed for approximately 2ms with a maximum current of 10 ma.

NOTE: The strobe index magnetic pickup should be adjusted until the SI pulse occurs just past the center of the read brush make time. Delay Y114 should be adjusted for a 2ms read timing pulse.

Arcing and burning of brush contacts is eliminated because current is not applied while the brushes are making or breaking contact.

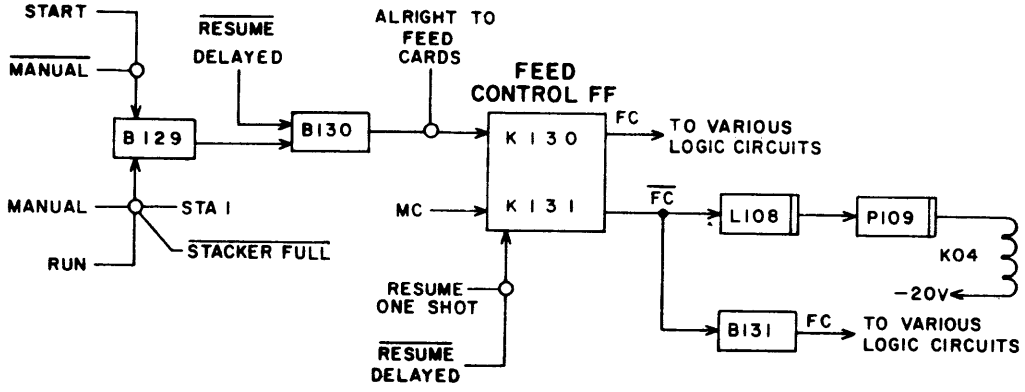
Feed Control Logic

The feed control flip-flop is set when the start signal from the controller is present and manual operation is not selected, or when manual operation is selected and the Run toggle switch on the maintenance panel is closed. In the latter case, the controller is disabled and the feed control flip-flop is continually set and cleared to permit maintenance checks by free-running cards through the card punch. Refer to figure 13.

The feed control flip-flop is used to: (1) enable the clear sides of the lockout, resume and station 1-2 flip-flops, (2) set the fault and punch flip-flops, and (3) partially enable the AND-gates to L122 and B125 in the card counter and solenoid logic circuits, respectively.

The feed control flip-flop is cleared when the resume pulse comes up at the end of a punch cycle. This causes delay relay K04 to be dropped.

NOTE: Delay K04 drops during the 2 to 60 second time interval following de-energize time.



Feed Control Logic Figure 13

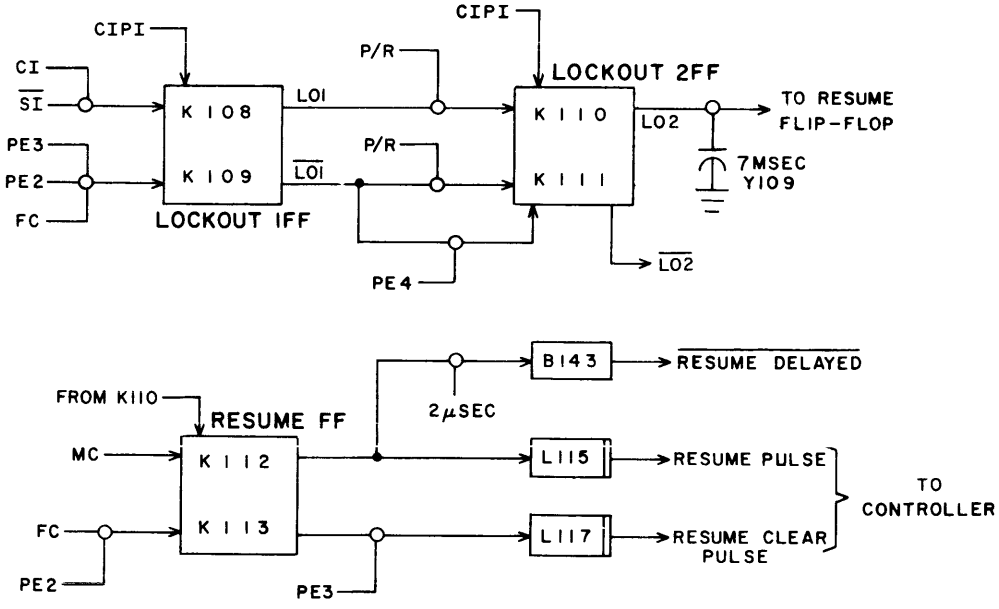
Lockout and Resume Logic

The lockout flip-flops determine: (1) which twelve of the sixteen PI pulses are to be used for generating punch timing and (2) which twelve of the sixteen SI pulses are to be used for generating read timing.

Both lockout flip-flops, shown in figure 14, are set at the first coincident CI and PI pulses. Lockout 1 must be cleared prior to enabling a read timing pulse and lockout 2 must be cleared prior to enabling a punch timing pulse. Lockout 1 is cleared when the PE2 and PE3 flip-flops are set. This occurs at the third PI pulse, 30 milliseconds after CI PI time. Lockout 2 is cleared at the same time by lockout 1. The same pulse also sets the punch timing flip-flop (K114).

After the twelfth row has been punched, the check-read brushes are strobed and the AND-gate to K108 prevents lockout 1 from setting while the strobe is in progress. A second CI pulse occurs after the twelfth row has been read, setting the lockout 1 and 2 flip-flops. The generation of punch timing and read timing pulses is now impossible because the punch timing and read timing flip-flop set inputs have been disabled.

The resume flip-flop is set by a delayed L02 pulse. It then notifies the controller that the card punch is at the end of an operation. When the lockout 1 and 2 flip-flops have cleared, the resume flip-flop clears and a resume clear signal is sent to the controller.



Punch and Read Timing Logic Figure 14

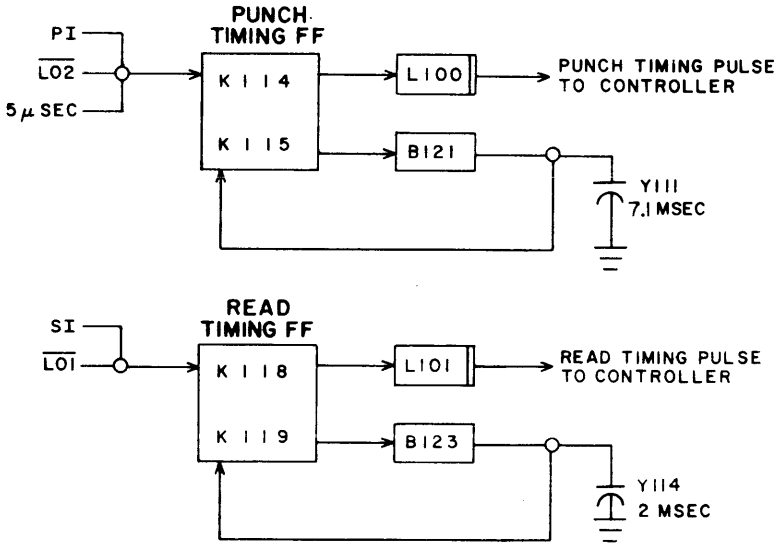
Punch and Read Timing Logic

The third PI pulse cleared LO2, by setting PE3 flip-flop and set the punch timing flip-flop at K114 (figure 15). When the punch timing flip-flop is set, B121 switches to "1". After a delay of 4.5 to 8 milliseconds (the duration of the punch timing pulse), Y111 goes to "1" and clears the punch timing flip-flop.

NOTE: The delay circuit, Y111, should be set for a nominal delay of 7.1 milliseconds.

The third through fourteenth SI pulses set the read timing flip-flop at K118. When the read timing flip-flop is set, B123 switches to a "1". After a delay of 1.2 to 2.2 milliseconds, Y114 goes to "1" and clears the read timing flip-flop. This delay determines the duration of each of the twelve read timing pulses.

NOTE: The delay circuit, Y114, should be set for a nominal delay of 2 milliseconds.



Punch and Read Timing Logic Figure 15

SEQUENCE OF OPERATION

The following is a logical sequence of operation for a complete card punching operation.

I. Power On:

1. Close main circuit breaker (CB-1)
2. Close main power switch
3. K-2 energizes
4. K-7 energizes
5. K-5 energizes
6. K-1 energizes

II. Card Punching Operation:

1. Press motor power switch
2. Start Signal to Set Feed Control F/F
3. K-4 energizes
4. K-6 energizes
5. K-3 energizes to Start Drive Motor
6. Card Index Pulse to Clear PE-3
7. Punch Index Pulse to C1 P1

    a. Set Pick Enable 1 F/F
    b. Clear Pick Enable 4 F/F
    c. Set lockout F/F's 1 and 2
    d. Set Resume F/F (Initially set on POMC)
    e. Energize picker solenoid, and read station solenoids
    f. Set Aligner F/F
    g. Energize aligner solenoids

8. Punch Index Pulse 2.

    a. Set Pick Enable 2 F/F
    b. Clear Resume F/F
    c. Drop Picker and Read Station solenoids
    d. Drop Aligner solenoids
    e. Set Punch Station F/F
    f. Clear Single Pick F/F

9. Punch Index Pulse 3.

    a. Set Pick Enable 3 F/F
    b. Clear Lockout F/F's 1 and 2
    c. Send Resume Clear to controller
    d. Set Punch Timing F/F
    e. Set Read Timing F/F

10. Punch Index Pulse 4.

    a. Set Pick Enable 4 F/F
    b. Off-set circuit is enabled at this time if selected by the controller.

11. Punch Index Pulse 5.

    a. Clear Pick Enable 1 and 2 F/F's
    b. Clear Off Set F/F
    c. Resume clear pulse to controller drops

12. Punch Timing F/F sets and clears on each successive punch index pulse for remaining rows to be punched.
13. Read Timing F/F sets and clears on each successive strobe index pulse for remaining rows to be read.
14. Card index pulse (End of Card) after Row 12.

    a. Set Lockout F/F's 1 and 2
    b. Clear Pick Enable 3 F/F
    c. Clear Punch Station F/F
    d. Set Resume F/F to punch resume to controller
    e. Clear Feed Control F/F
    f. K-4, K-6, K-3 de-energize turning off the drive motor.

15. Set Ready F/F when cards are positioned in card ready stations 1 and 2.

TABLE 1 COMMUNICATION LINES

CONTROLLER TO CARD PUNCH		CARD PUNCH TO CONTROLLER	
Start Line	Enables card feeding - In the Auto. mode one card is fed for each start pulse.	Ready	Indicates to controller that the punch is ready for on-line operation.
Punch Lines	Eighty lines (one for each interposer solenoid) energize the interposer solenoid to punch.	Punch Timing	7 msec timing pulses indicate the punch solenoids may be pulsed by the controller to punch.
Offset Line	Sets the offset flip flop to energize the offset mechanism and offset a card prior to its arrival in the output stacker. The card is offset approximately 1/4 inch.	Read Timing	2 msec timing pulses indicate information is on the output lines and may be sampled by the controller.
		Check Read	Eighty lines carry read information to the controller.
		Not Fail to Feed	Signal indicates a card is in the punch ready station.
		Resume	Indicates card punch is between punch cycles.
		Resume Clear	Sent to the controller for 30 msec at the beginning of a punch cycle.

RELAY SEQUENCING

The cabinet wiring assembly contains the relays that control power distribution and provide the correct power-on sequencing.

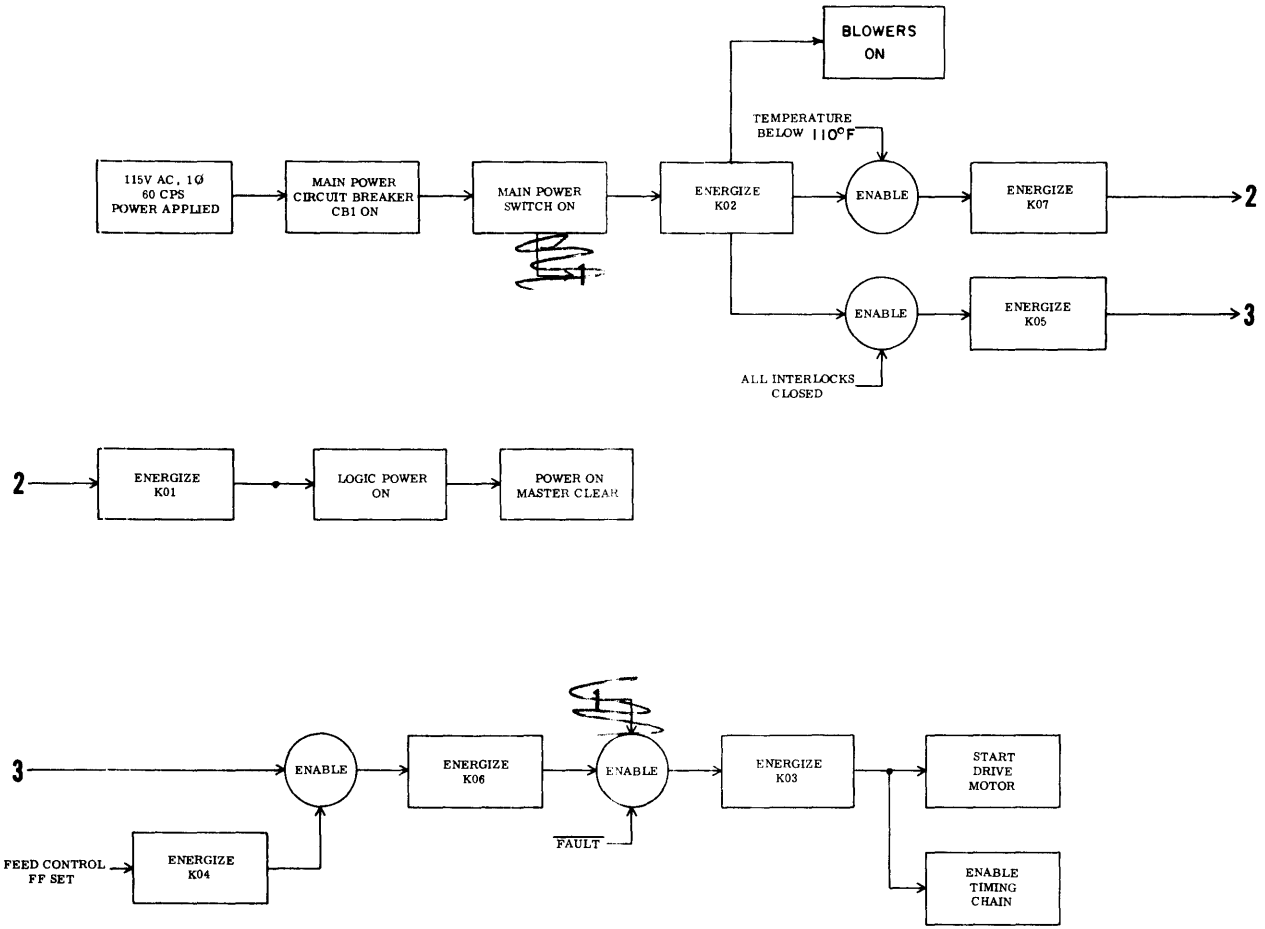
Main circuit breaker CBI closes the service lines to the power supply and distribution system. Assume that all circuit breakers are closed during the following sequence of events.

1. Connect the card punch to a convenient 115 volt, 60 cycle single phase power outlet.

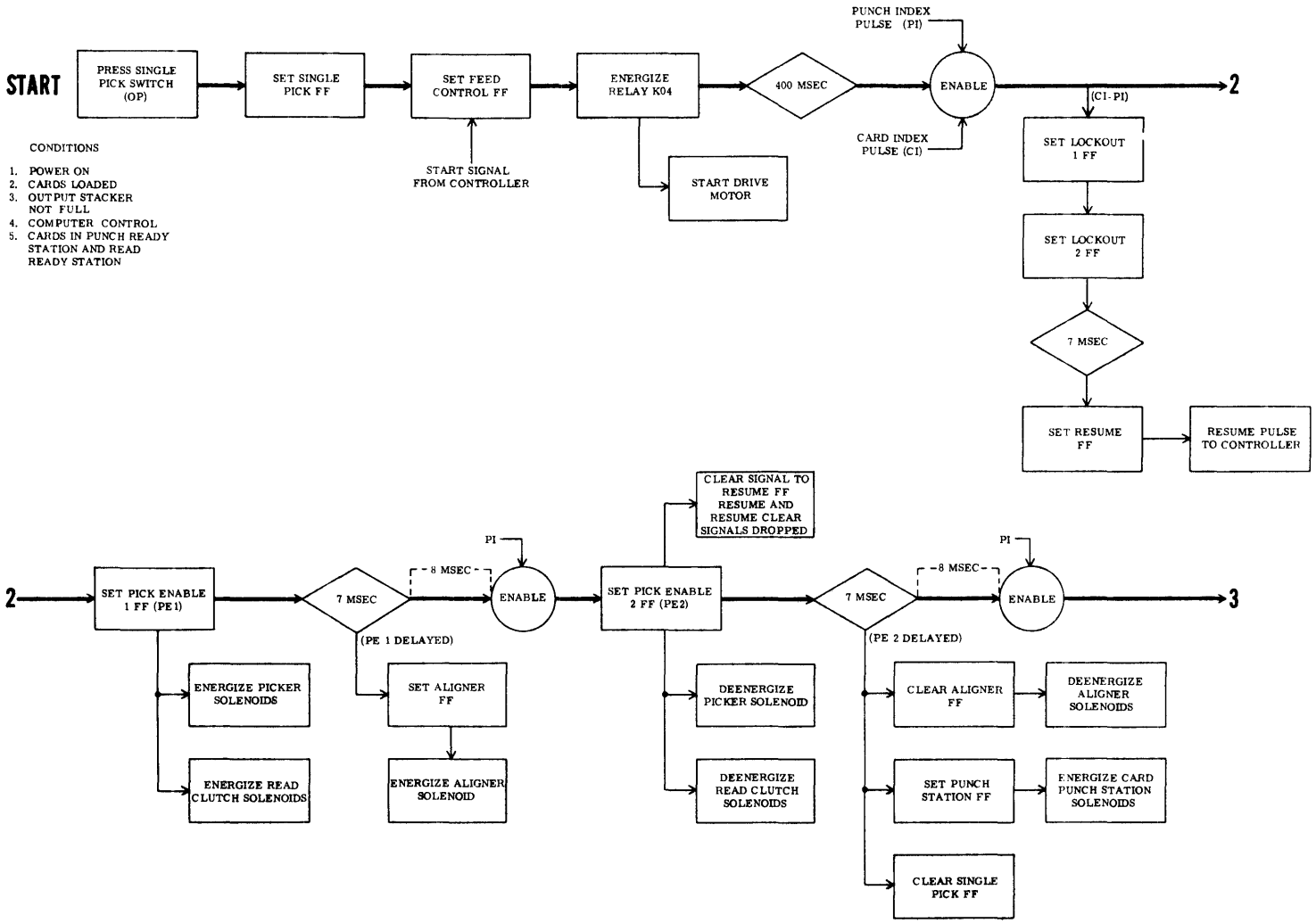
2. Depress the Main Power pushbutton on the operator control panel. The 24 volt a-c potential from transformer T1 causes the Main Power indicator lamp to light and energizes relay K02. Relay K02 will turn on the blowers. Relay K07 is in turn energized when K02 is energized (provided the chassis temperature is less than 110°F). Relay K01 is in turn energized when the K07 is energized. The 115 volt, 60 cycle, single phase power is then applied to the power supply. If the punch head, hood and right cabinet doors are closed relay K05 is energized when relay K02 is energized. The Interlock indicator lamp should not be lit.

3. Depress the Motor Power pushbutton on the operator control panel. The Motor Power indicator lamp lights, indicating that the K03 circuit is enabled.

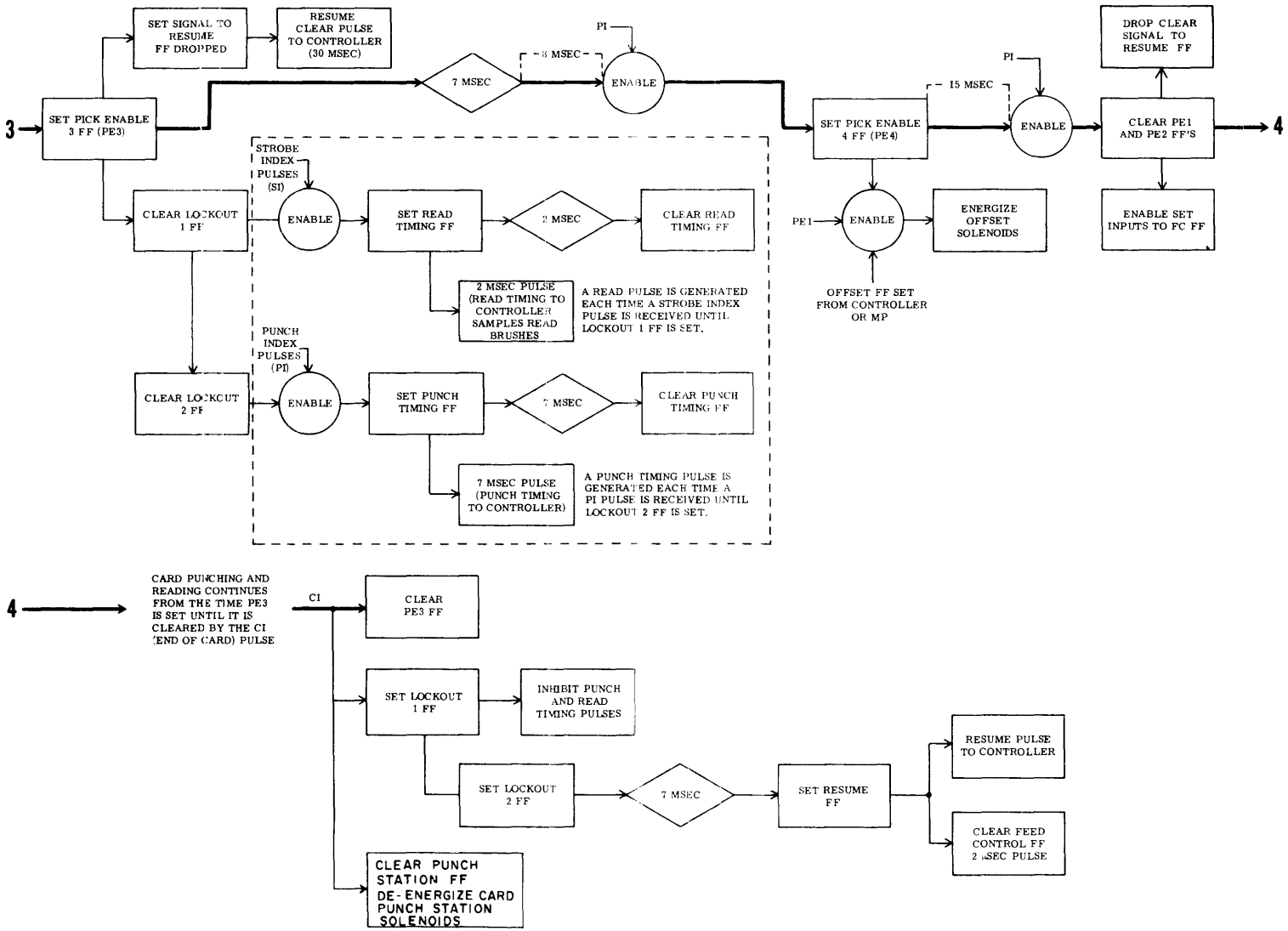
4. A start signal causes relay K04 to energize which, in turn, energizes relay K06. With relay K06 energized, the -30 volt d-c potential from the power supply is applied to the punch magnets and solenoids. Relay K08 is energized if a fault condition exists. With relay K06 energized and K08 de-energized, relay K03 becomes energized and supplies 115 volt, 60 cycle, single phase power to the drive motor.



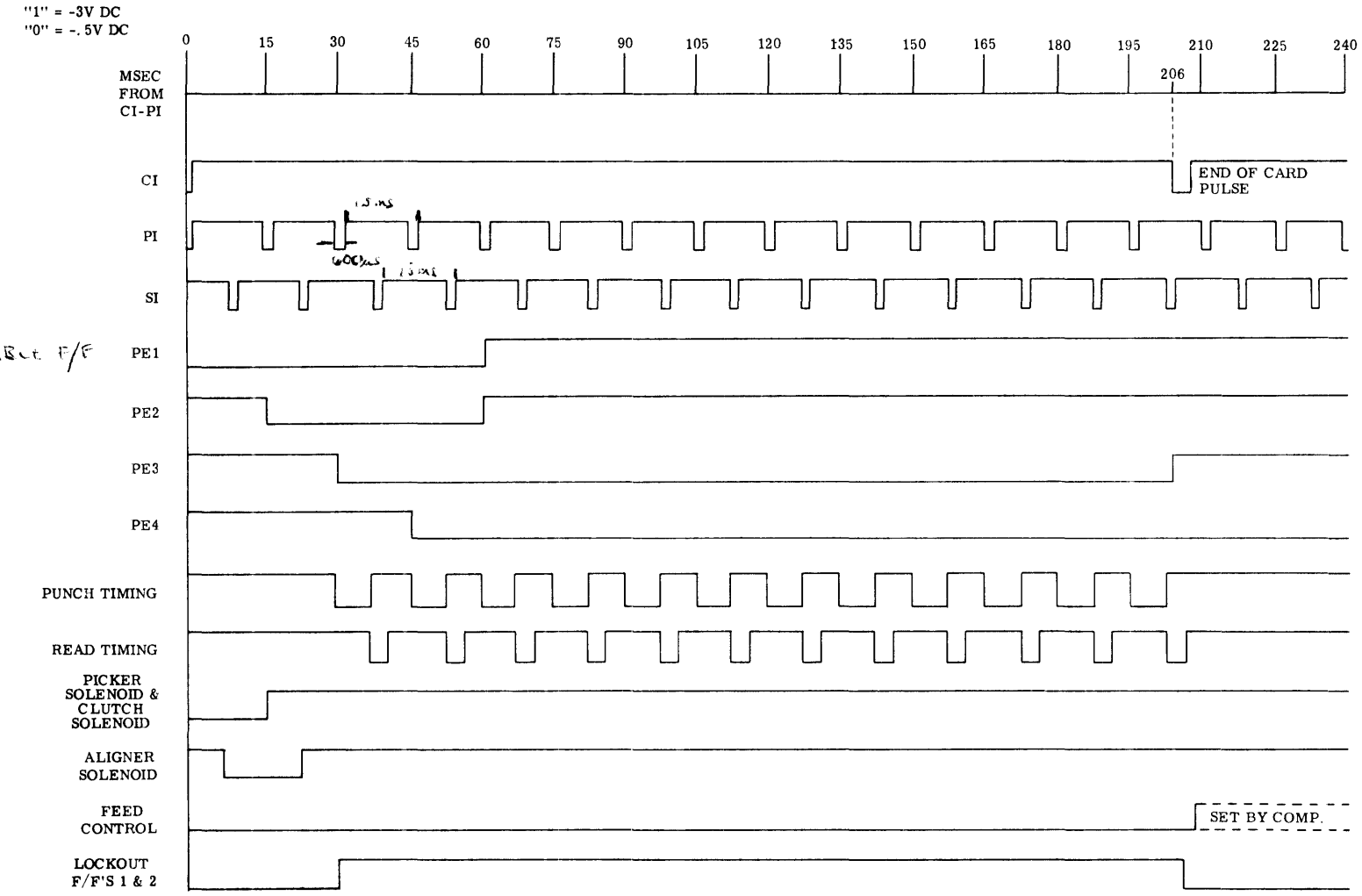
Relay Sequencing - Flow Chart



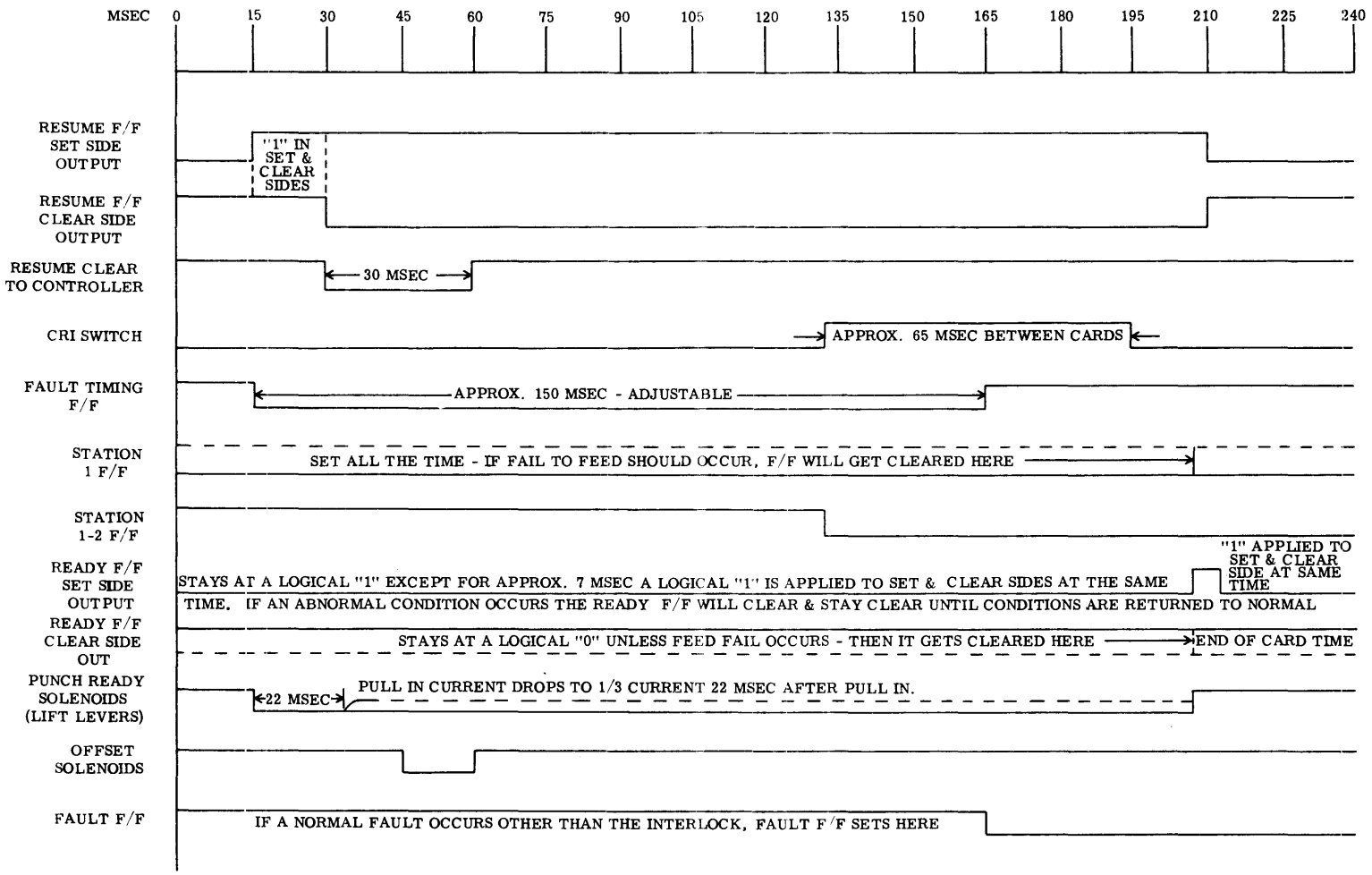
Operation Flow Chart (Part 1 of 2)



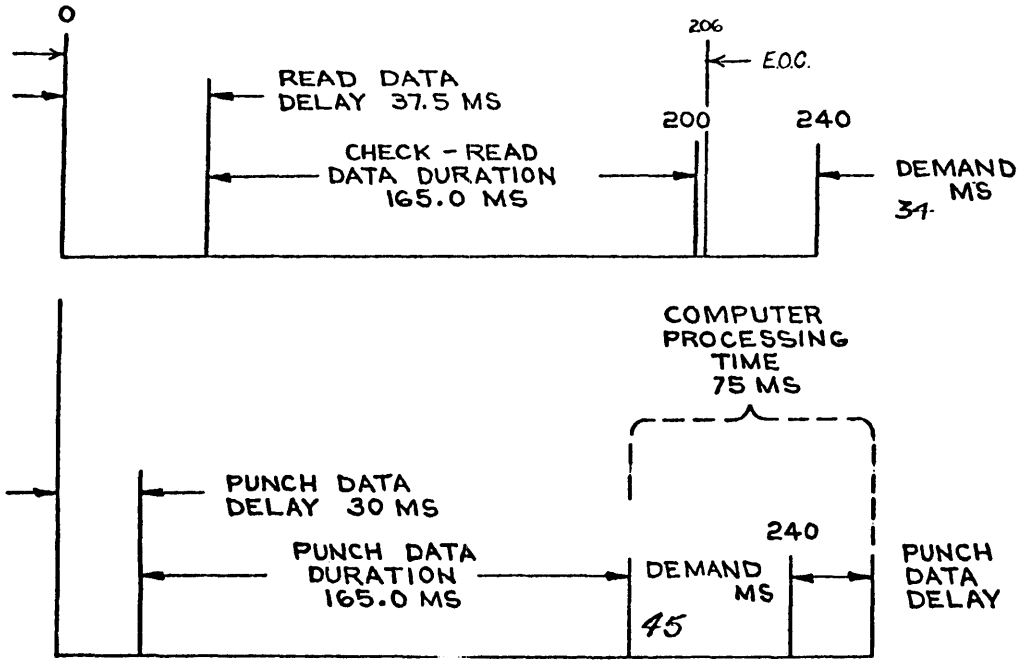
Operation Flow Chart (Part 2 of 2)



Timing Diagram (Part 1 of 2)

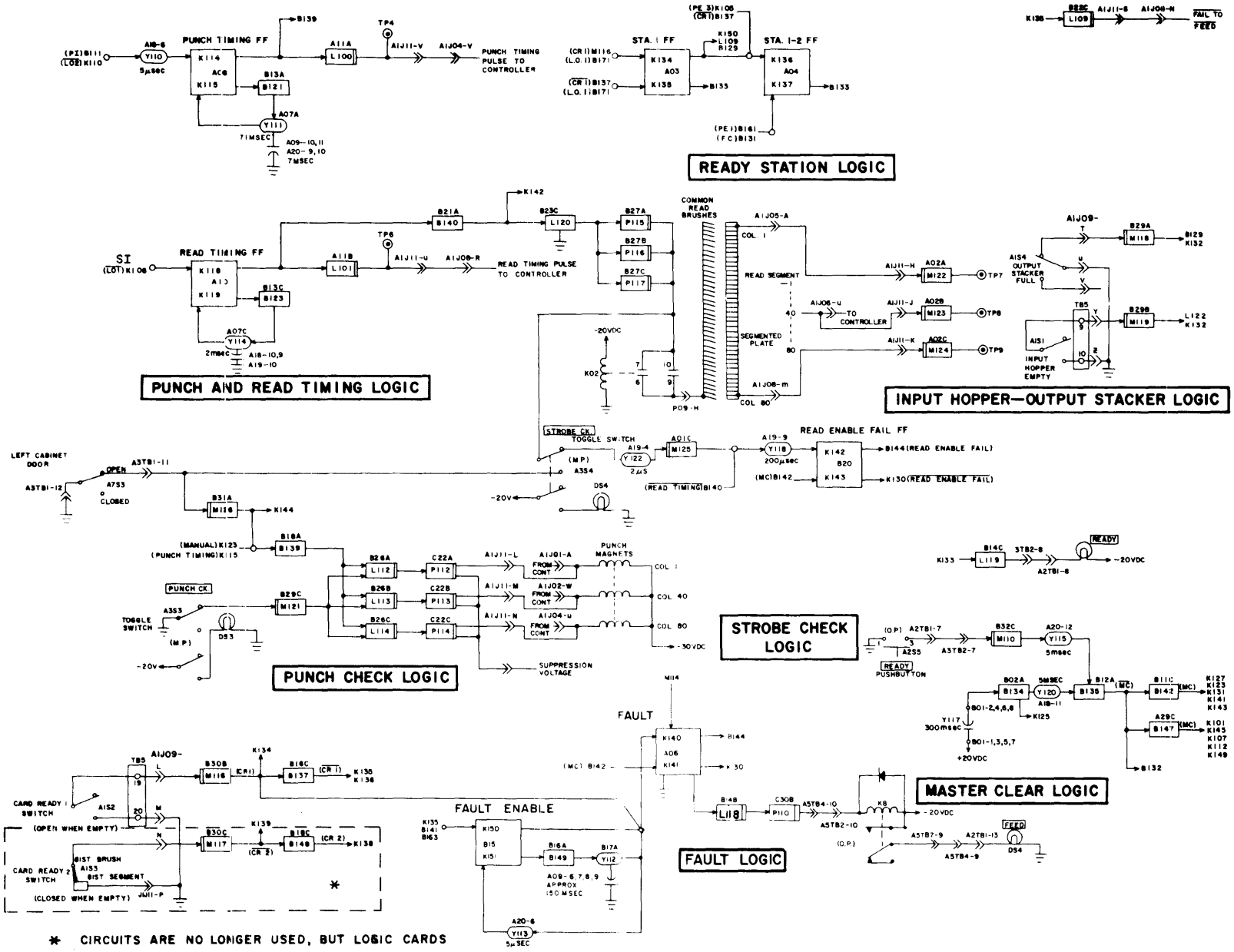


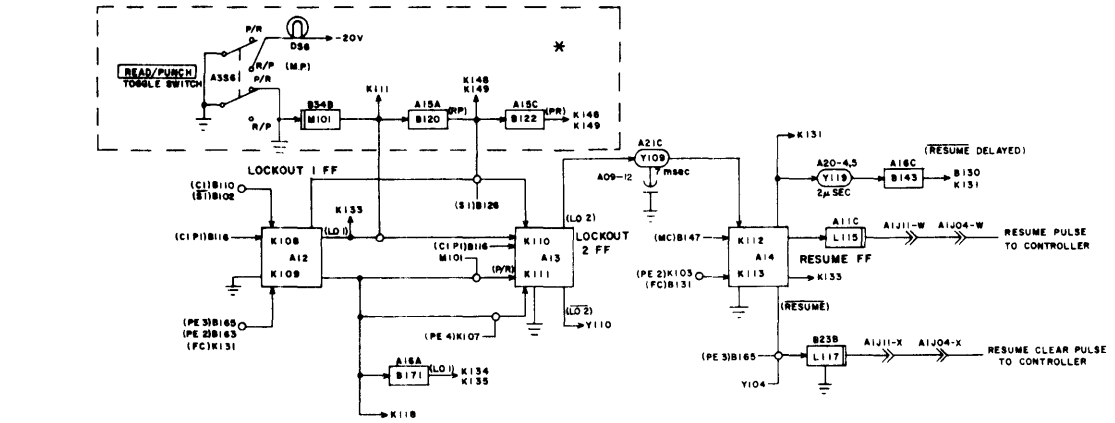
Timing Diagram (Part 2 of 2)



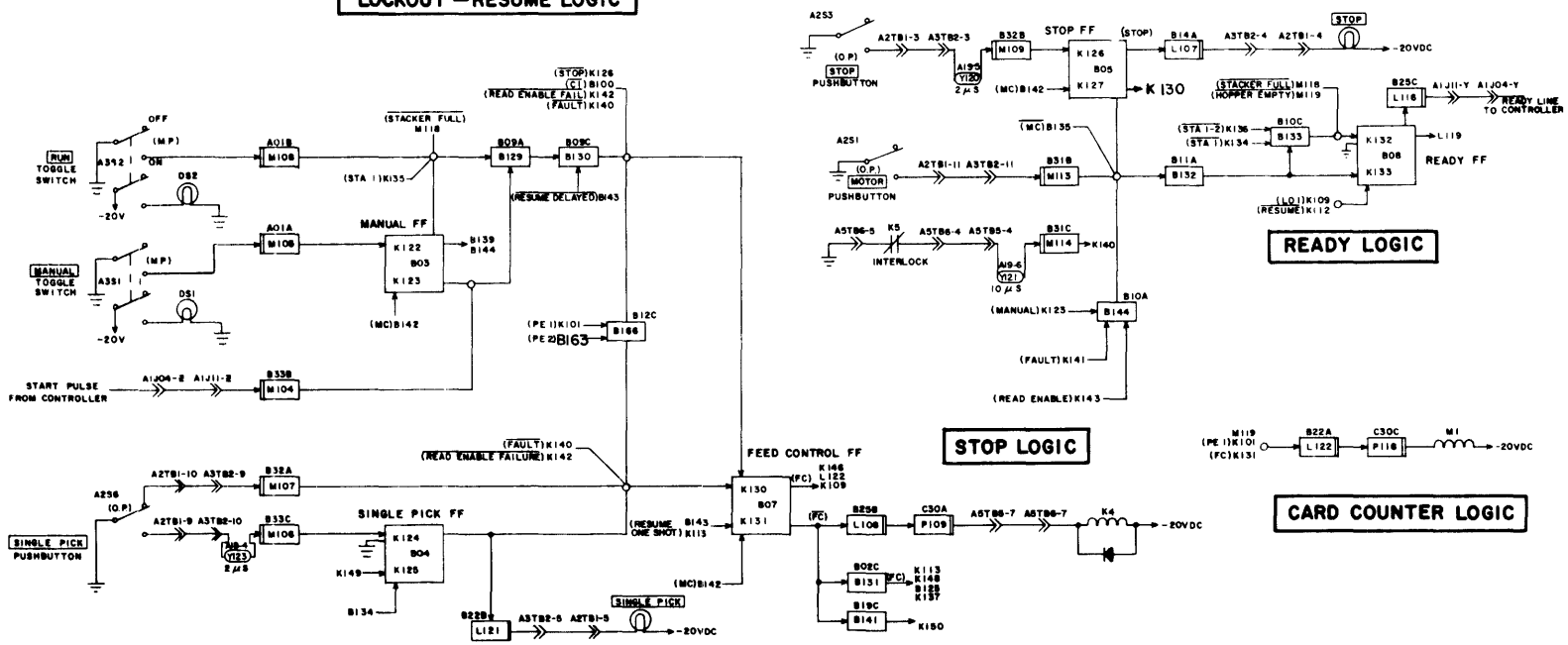
250 CPM - 240 MS / CARD

TIMING DIAGRAM


READY STATION LOGIC
PUNCH AND READ TIMING LOGIC
INPUT HOPPER—OUTPUT STACKER LOGIC
STROBE CHECK LOGIC
PUNCH CHECK LOGIC
MASTER CLEAR LOGIC
FAULT LOGIC
PUNCH TIMING FF
STA. 1 FF
STA. 1-2 FF
READ TIMING FF
READ ENABLE FAIL FF
FAULT
FAULT ENABLE
PUNCH TIMING PULSE TO CONTROLLER
READ TIMING PULSE TO CONTROLLER
COMMON READ BRUSHES
SEGMENTED PLATE
PUNCH MAGNETS
SUPPRESSION VOLTAGE
CARD READY 1 SWITCH
CARD READY 2 SWITCH
* CIRCUITS ARE NO LONGER USED, BUT LOGIC CARDS ARE STILL PRESENT IN THE CARD PUNCH.



LOCKOUT — RESUME LOGIC



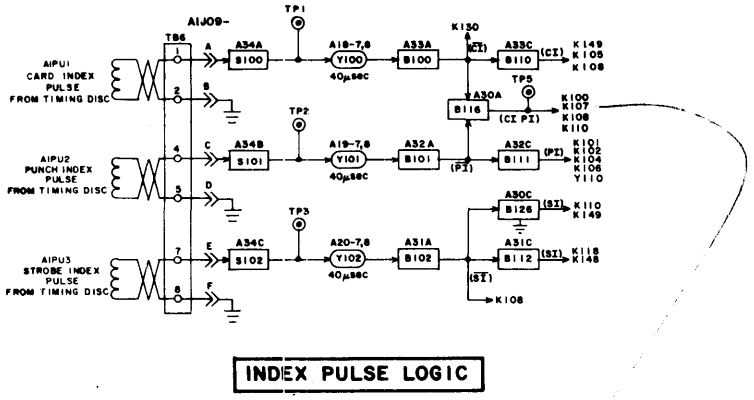
FEED CONTROL LOGIC

READY LOGIC

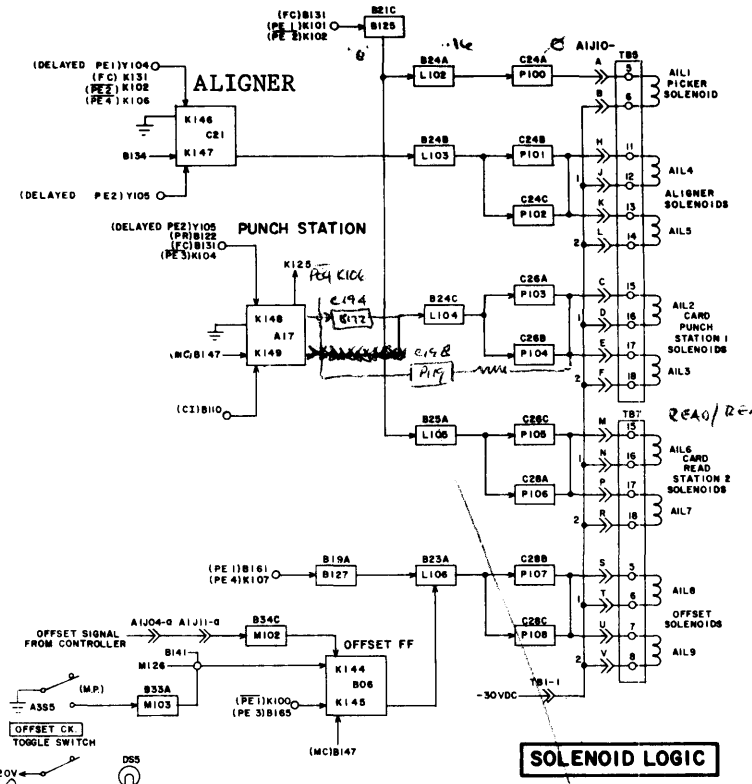
STOP LOGIC

CARD COUNTER LOGIC

* CIRCUIT IS NO LONGER USED, BUT LOGIC CARDS ARE STILL PRESENT IN THE CARD PUNCH.



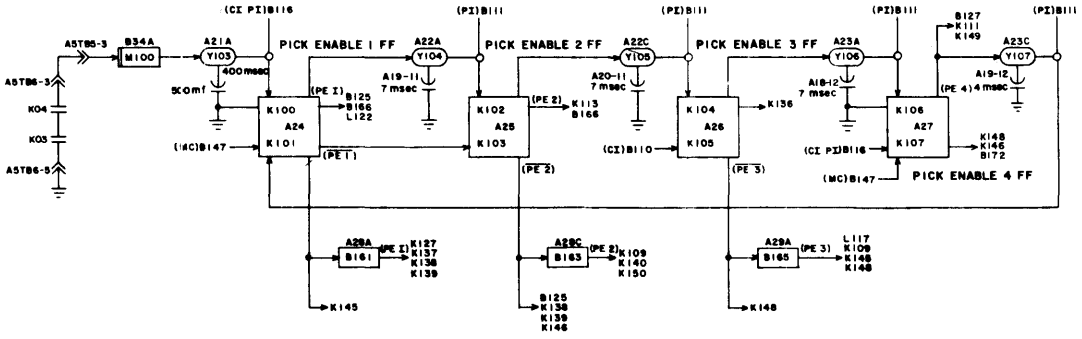
INDEX PULSE LOGIC



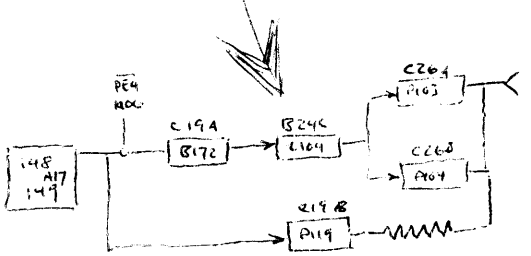
SOLENOID LOGIC

CARD OFFSET LOGIC

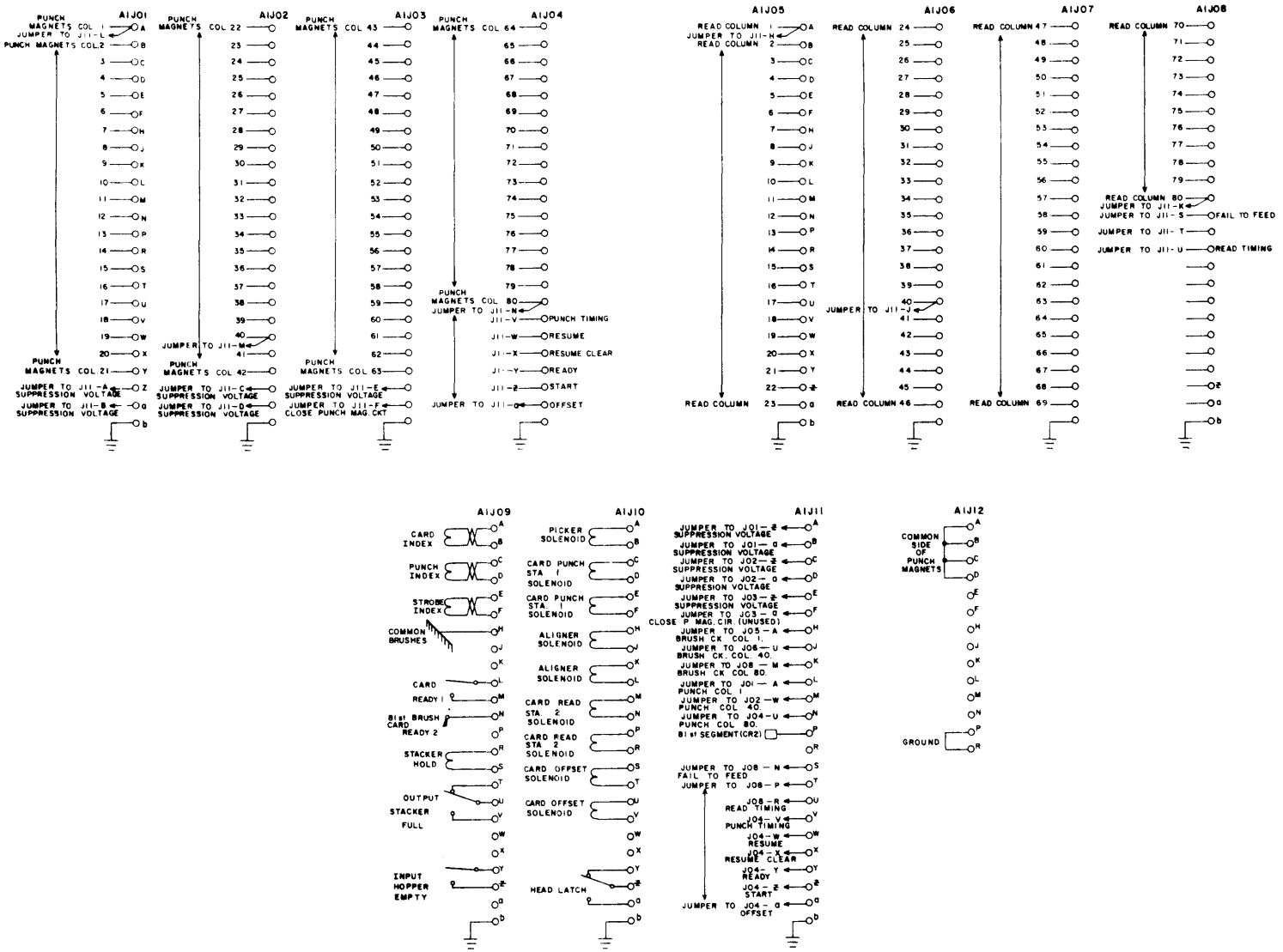
ALLOWS MOTOR TO EVEN OUT SPEED



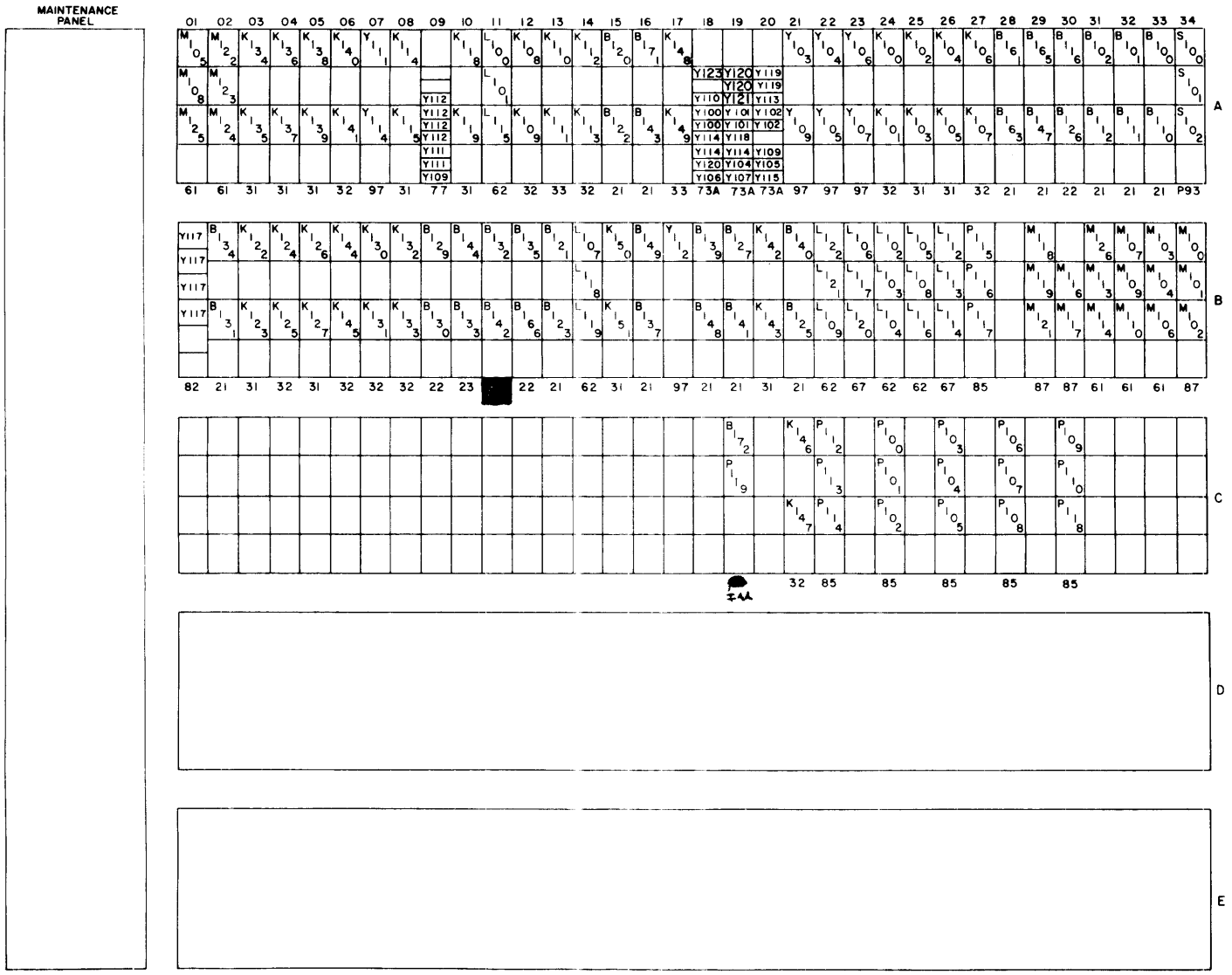
PICKER ENABLE LOGIC

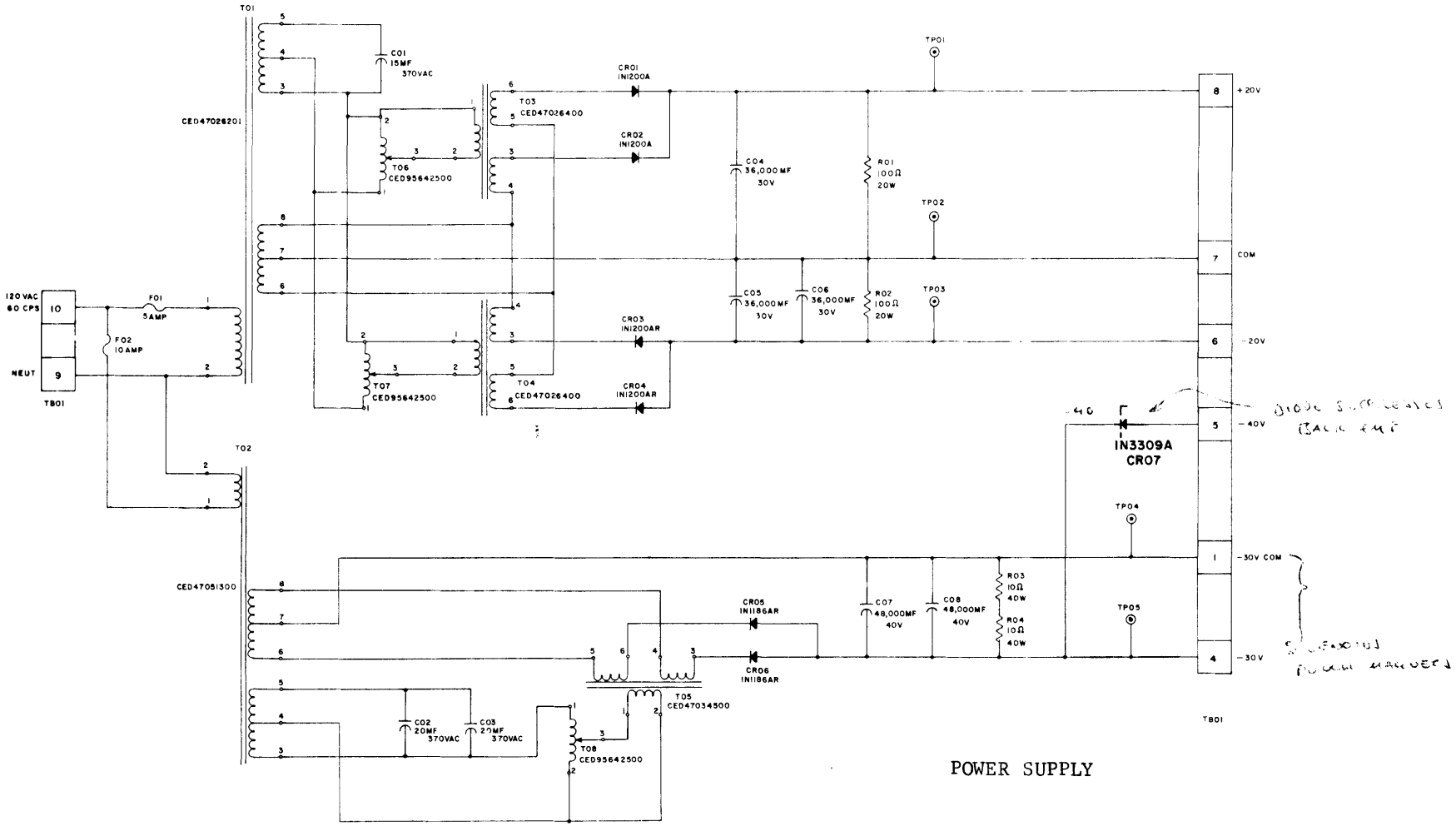


C19 IAA


A1J01
PUNCH MAGNETS COL 1
JUMPER TO J11-L
PUNCH MAGNETS COL 2
PUNCH MAGNETS COL 21
JUMPER TO J11-A
SUPPRESSION VOLTAGE
JUMPER TO J11-B
SUPPRESSION VOLTAGE
A1J02
PUNCH MAGNETS COL 22
JUMPER TO J11-M
PUNCH MAGNETS COL 42
JUMPER TO J11-C
SUPPRESSION VOLTAGE
JUMPER TO J11-D
SUPPRESSION VOLTAGE
A1J03
PUNCH MAGNETS COL 43
PUNCH MAGNETS COL 63
JUMPER TO J11-E
SUPPRESSION VOLTAGE
JUMPER TO J11-F
CLOSE PUNCH MAG. CKT
A1J04
PUNCH MAGNETS COL 64
PUNCH MAGNETS COL 80
JUMPER TO J11-N
J11-V PUNCH TIMING
J11-W RESUME
J11-X RESUME CLEAR
J11-Y READY
J11-Z START
JUMPER TO J11-a OFFSET
A1J05
READ COLUMN 1
JUMPER TO J11-H
READ COLUMN 2
READ COLUMN 23
A1J06
READ COLUMN 24
JUMPER TO J11-J
READ COLUMN 46
A1J07
READ COLUMN 47
READ COLUMN 69
A1J08
READ COLUMN 70
READ COLUMN 80
JUMPER TO J11-K
JUMPER TO J11-S FAIL TO FEED
JUMPER TO J11-T
JUMPER TO J11-U READ TIMING
A1J09
CARD INDEX
PUNCH INDEX
STROBE INDEX
COMMON BRUSHES
CARD READY 1
81st BRUSH CARD READY 2
STACKER HOLD
OUTPUT STACKER FULL
INPUT HOPPER EMPTY
A1J10
PICKER SOLENOID
CARD PUNCH STA. 1 SOLENOID
CARD PUNCH STA. 1 SOLENOID
ALIGNER SOLENOID
ALIGNER SOLENOID
CARD READ STA. 2 SOLENOID
CARD READ STA. 2 SOLENOID
CARD OFFSET SOLENOID
CARD OFFSET SOLENOID
HEAD LATCH
A1J11
JUMPER TO J01-Z SUPPRESSION VOLTAGE
JUMPER TO J01-a SUPPRESSION VOLTAGE
JUMPER TO J02-Z SUPPRESSION VOLTAGE
JUMPER TO J02-a SUPPRESSION VOLTAGE
JUMPER TO J03-Z SUPPRESSION VOLTAGE
JUMPER TO J03-a CLOSE P. MAG. CIR (UNUSED)
JUMPER TO J05-A BRUSH CK. COL. 1.
JUMPER TO J06-U BRUSH CK. COL. 40.
JUMPER TO J08-M BRUSH CK. COL. 80.
JUMPER TO J01-A PUNCH COL. 1
JUMPER TO J02-W PUNCH COL. 40.
JUMPER TO J04-U PUNCH COL. 80.
81st SEGMENT (CR2)
JUMPER TO J08-N FAIL TO FEED
JUMPER TO J08-P
J08-R READ TIMING
J04-V PUNCH TIMING
J04-W RESUME
J04-X RESUME CLEAR
J04-Y READY
J04-Z START
JUMPER TO J04-a OFFSET
A1J12
COMMON SIDE OF PUNCH MAGNETS
GROUND

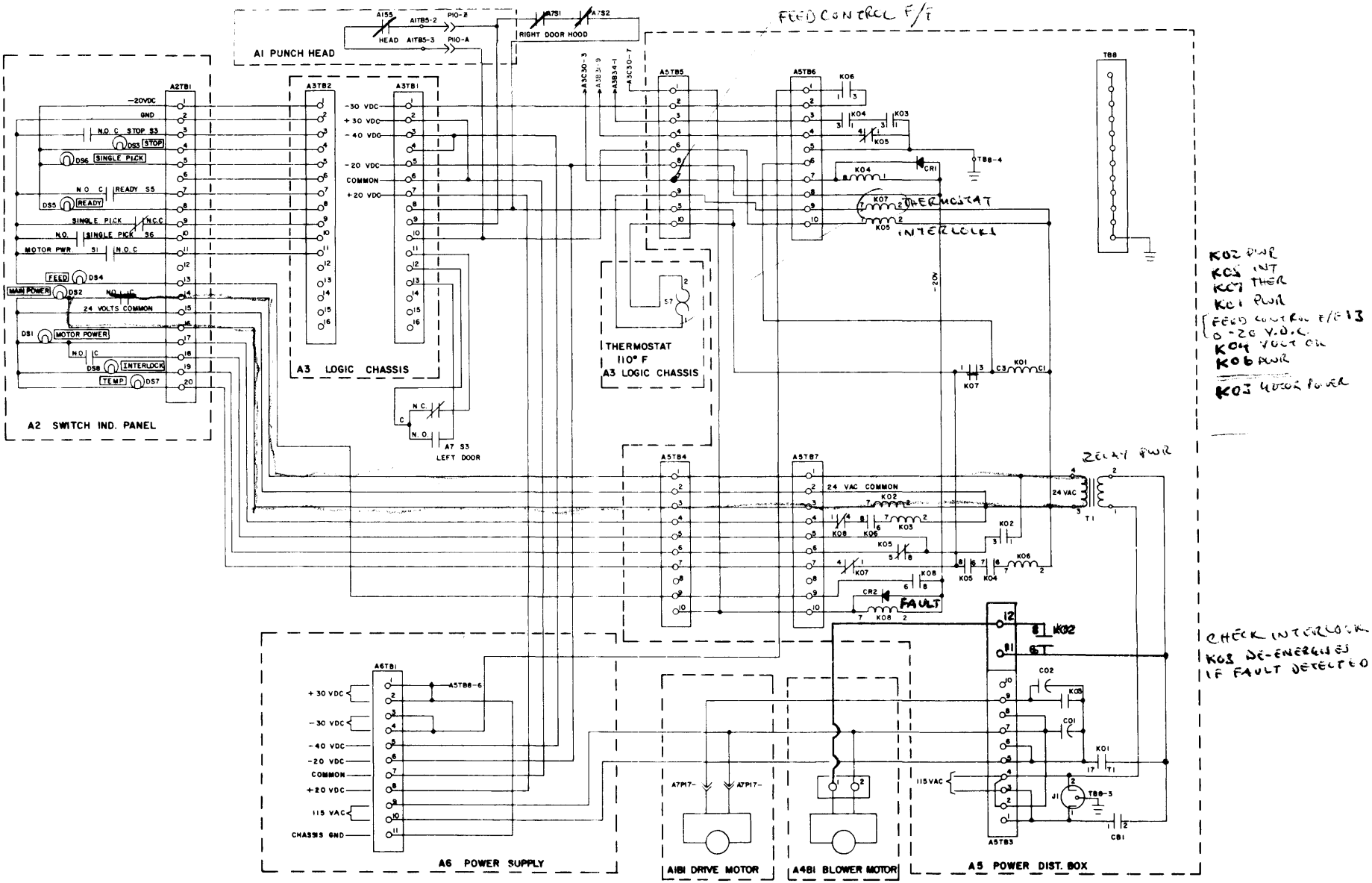
CARD PLACEMENT CHART





POWER SUPPLY

S/N 63 AND ABOVE



POWER SUPPLY DISTRIBUTION

PRACTICAL APPLICATION EXERCISE

A. Set up the machine to run standard 80 column cards

1. Using the Single Pick Switch, position cards until the punch indicates a Ready condition. Open the punch and observe the position of each card in the channel. Close the punch and continue with the next step.
2. Using the Manual and Run Switches, observe the action of the machine as it feeds cards at the rate of 250 cards per minute. At random, use the Off-set Check Switch and observe the offset action of the cards in the Output Stacker Tray.
3. Using the Manual, Run, and Punch Check Switches, observe the action of the machine as it feeds cards at the rate of 250 cards per minute. Columns 1, 40, and 80 should be punched as a test pattern on the card. This pattern is used primarily to check the registration of punches on the card.
4. Restore the machine to normal operation.

PRACTICAL APPLICATION EXERCISES

EXERCISE I: COMPONENT LOCATION

1. Reference: 415 Punched Card Equipment Training Manual

2. Equipment: 415 Card Punch

3. Procedure: Open the top and side covers of the machine. Also, remove the front panel for access to the logic chassis. Then make a careful study of the general construction of the machine. Use pages 4-7 thru 4-17 as a guide to locate all parts.

   a. Physically locate and identify the following:

Component	Location	Function
Main Circuit Breaker		
Main Power Switch		
Motor Power Switch		
Feed Indicator		
Stop Switch		
Single Pick Switch		
Ready/Master Clear Switch		
Temperature Indicator		
Interlock Indicator		
Interlocks (3)		
Left Hand Door Interlock		
Manual Switch		
Run Switch		
Punch Check Switch		
Strobe Check Switch		
Off-set Switch		
Drive Motor (1/3 H.P.)		

Component	Location	Function
Cabinet Cooling Blower		
Gear Train and Drive Belts		
Input Hopper		
Picker Mechanism		
Input Hopper Empty Switch		
Punch Ready and Aligner Station		
Transport Pinch Rollers		
80 Column Guide Plate		
Row Indexing Mechanism		
CI Timing Disk and Magnetic Pickup		
Punch Head Assembly		
PI/SI Timing Disk and Magnetic Pickup		
Check-Read Ready Assembly		
Read Brush Assembly		
CR1 Switch		
Read Segment Assembly		
Offset Assembly		
Stacker Disk Assembly		
Output Stacker		
Output Stacker Full Switch		
Power Supply		
Relay Panel		
Chad Basket		
Thermostat		
Logic Chassis		
Anti-Jam Mechanism		

EXERCISE II: MECHANICAL ADJUSTMENTS

1. Reference: 415 Reference Manual

2. Equipment: 415 Card Punch

3. Procedure: The following adjustments are to famiarize the trainee with the 415 Card Punch and to allow the trainee to gain enough experience to provide reliable maintenance of the 415 in the field.

   NOTE: Refer to Chapter 5 of the Reference Manual for the procedures to be followed for each adjustment listed below.

   a. Input Hopper
      1. Card Clearance
      2. Card Throat
      3. Card Throat Roller
   b. Pinch Rollers
   c. Card Aligner
   d. Row Indexing Mechanism
   e. Solenoid Bank
   f. Check Read Station Feed Roller Timing
   g. Check Read Station Clutch Setting
   h. Read Station and Brush Removal and Replacement
   i. Read Strobe Adjustment
   j. Off-Set Roller Timing
   k. Off-Set Mechanism
   l. Stacker Fingers

m. Punch Transport Timing

4. Upon completion of the adjustments, load a stack of blank cards in the Input Hopper and position the cards, using the Single Pick Switch, until the punch indicates a Ready condition. Open the punch and carefully observe the position of the cards in both ready stations. It should be noted that any skew in the card position could cause incorrect punching or reading of the cards OR/AND a jam condition. Close the punch and continue if the cards are positioned correctly.
5. Punch the test pattern on several cards, using the Manual, Run, and Punch Check Switches to insure that the registration on the punched cards is correct. If incorrect, determine what corrections should be made and do them.
6. This completes the exercise.

STUDY QUESTIONS

1. The CDC 415 Card Punch is capable of punching cards:

   a. at demand rates up to 200 CPM in 300 micro-second card cycles.

   b. at demand rates up to 250 CPM in 600 milli-second card cycles.

   c. at 240 CPM.

   d. at demand rates up to 250 CPM in 240 milli-second card cycles.

2. In CDC format cards are oriented in the Input Hopper:

   a. Row 12-first-face-up.

   b. Row 9-first-face-down.

   c. Row 12-first-face-down.

   d. Any position desired by the programmer.

3. The punching method used by the 415 is:

   a. Column Binary with all rows being punched simultaneously.

   b. Column Binary with each column punched separately.

   c. A row at a time for 12 rows in the Column Binary Mode.

   d. A row at a time for 12 rows in the Row Binary Mode.

4. The actual time to punch or read 12 rows of data from an 80 column card is:

   a. 240 ms

   b. 200 ms

   c. 165 ms

   d. 206 ms

5. With the Main Power Switch closed the drive motor in the punch will start when the Motor Power Switch is closed. No other switches are closed.

   a. True

   b. False

6. Under no circumstances can cards be fed in the 415 with the Stop Switch closed and the Stop Indicator lit.

   a. True

   b. False

7. During a continuous mode of operation with the drive motor running if an interlock were momentarily opened and closed:

   a. a fault condition would be created stopping the drive motor until the interlock was closed again starting the drive motor.

   b. a fault condition would be created keeping the drive motor stopped after the interlock was closed again.

   c. it would not interrupt a continuous punching operation.

   d. feed indicator would light indicating a fault condition, but the punching operation would continue.

8. A Punch Ready condition exists when:

   a. Station #1 F/F is set.

   b. Station #1 and Station #1-2 F/Fs are set.

   c. Station #1, 1-2, and 2 F/Fs are set.

   d. when a Master Clear pulse is present.

9. The 415 will give a Punch Ready condition when:

   a. a card is positioned in the Punch Ready Station.

   b. a card is positioned in the Check-Read Ready Station.

   c. when the Punch Resume signal is sent to the card punch controller.

   d. cards are positioned in the Punch Ready and the Check-Read Ready station.

10. Malfunction Condition: K-06 solenoid winding is open, the probable results would be:

    a. an immediate $\overline{\text{Punch Ready}}$ condition is sent to the controller.

    b. the punch magnet solenoids would not energize and the drive motor would run continuously.

    c. punch magnet solenoids would not energize and the drive motor would stop.

    d. the drive motor would stop and the Fault F/F would set causing the Feed Indicator to light.

11. Malfunction Condition: Columns 1, 40, and 80 cannot be punched on the cards when the Manual, Run, and Punch Check Switches are closed. A probable cause would be:

    a. Columns 1, 40 and 80 are punched by the 415 when used with its associated punch controller.

    b. Strobe Index pulse would come up at the wrong time causing incorrect reading of the card.

    c. the Fault F/F is set when this combination of switches is set.

    d. Left Cabinet Door Switch is in the closed position.

12. When the Fault F/F is set, which of the following conditions exists?

    a. Punch is $\overline{\text{Ready}}$, Feed Indicator is lit, Drive motor runs continuously.

    b. K-8 energized, drive motor is stopped, punch indicates a Ready condition as long as cards are placed in the Input Hopper.

    c. Feed Indicator is lit, $\overline{\text{Punch Ready}}$ signal is sent to the controller, drive motor is stopped, controller is unable to re-select the 415.

    d. Drive motor is stopped, Ready F/F is cleared, K-8 de-energized.

13. Malfunction Condition: The Single Pick Switch is pressed and released with the following results: Single Pack F/F remains set, drive motor runs continuously, no cards are fed into the machine. A probable cause would be:

    a. Card Index and Punch Index are out of time.

    b. Punch Resume signal failed to reach the punch controller.

    c. An interlock on the cabinet has been left open.

    d. Card Index and Strobe Index pulses are out of time.

14. The Suppression voltage sent from the 415 to the card punch controller is used to prevent damage to the punch magnet selection circuit in the card punch controller when the punch magnet is de-energized.

    a. True

    b. False

15. With the Run/Manual Switches on, the output stacker full of cards, and the Stacker Full switch in the On position, K-6 will remain energized after the drive motor stops.

    a. True

    b. False

16. A grounded read brush (Strobe Check Switch Off) will:

    a. have no effect in a normal Read operation.

    b. prevent cards from being fed in the 415.

    c. cause the Feed Indicator to light.

    c. cause the Punch Resume signal to the controller.

CHAPTER V

3245 CARD PUNCH CONTROLLER

CHAPTER V

3245 CARD PUNCH CONTROLLER

INTRODUCTION

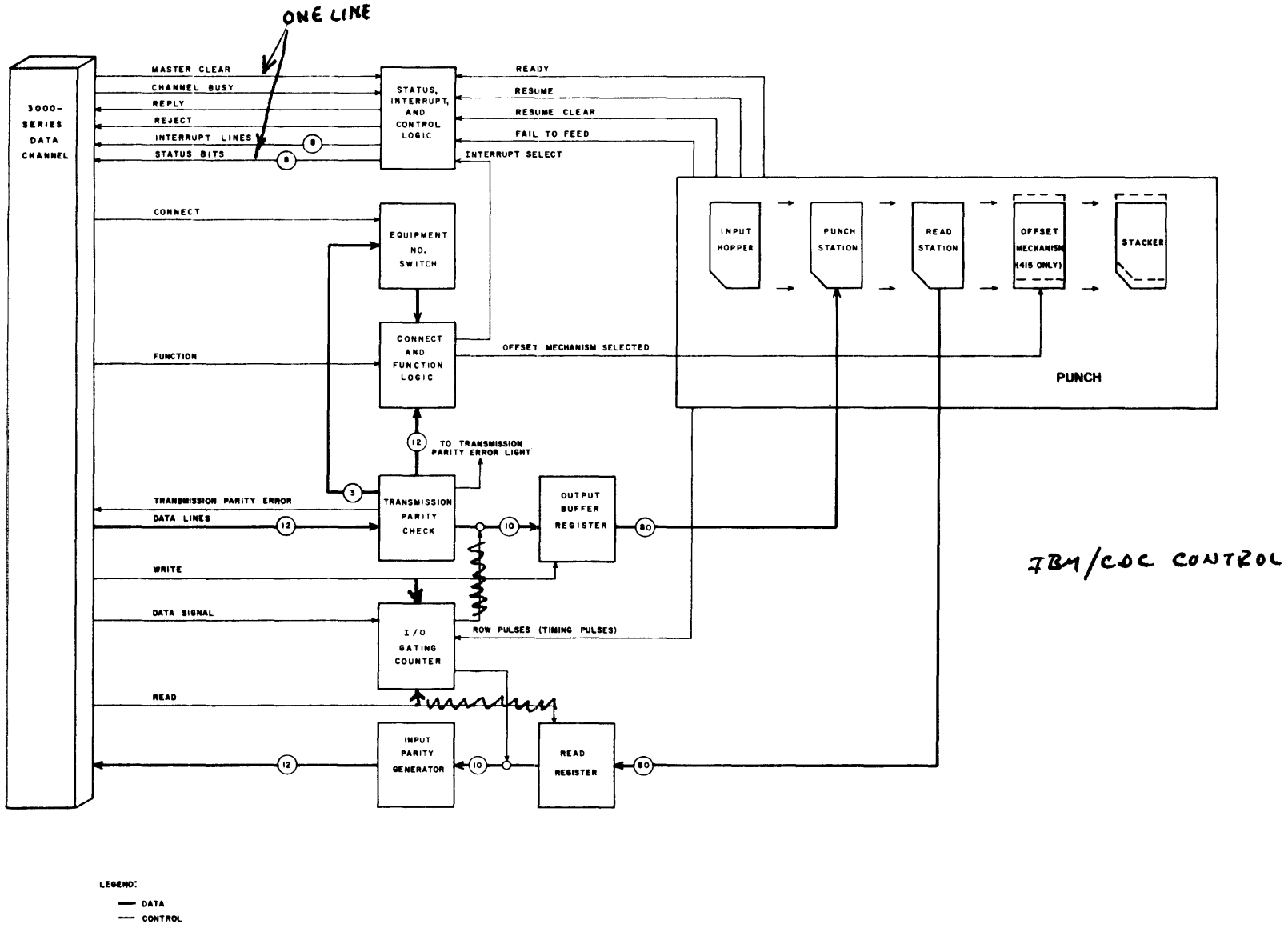
The 3245 Card Punch Controller acts as an interface to synchronize the 3200 computer with the 415 Card Punch during the punching and reading of data on the card. The logic components of the 3245 can be mounted in the 3200 main frame or separately in a peripheral controller cabinet.

The 3245 is connected for a punch and/or read operation when bit positions 9, 10, and 11 of the connect code match the numerical setting of the equipment switch. Prior to the punch operation, the 3200 computer can sense the status of the 3245/415 combination. It should be pointed out that cards must be positioned in the Punch Ready and Read Ready stations in the 415 before the card punch is in the Ready condition.

The function codes for the 3245 are used to offset selected cards in the Output Stacker or select interrupt conditions. If a function is attempted while the controller is busy a Reject Signal is sent to the data channel clearing the function code from the data lines.

Card motion for the punch operation in the 415 is initiated when the Write, Data, and Channel Busy signals are received by the controller. For the 12 rows on the card the punch generates 12 Punch Timing pulses with each pulse being in time with each card row as it passes beneath the punch dies. As each row is positioned, the Punch Timing pulse is sent to the controller allowing the Output Buffer Register to be loaded. Wherever a bit is stored in the register the appropriate punch magnet is energized. Once the register is loaded with a row the mechanics of the 415 perforate the card, then advance the card to position the next row for punching.

The Read Station in the 415 is utilized to read the data from the card, an eighty (80) column row at a time, and transfer it to the Read Register in the 3245, then onto the data channel for comparison. The comparison is made with the data stored in the computer memory in order to check for punch errors. The data that is being read was punched on the previous cycle, not on the current punch cycle. Once loaded into the Read Register, the data is transferred to the data channel in eight (8) twelve bit bytes, high order two bits being ignored.
After the card has been punched and read it passes in front of the Offset mechanism in the 415. If the card is to be denoted from the rest the Offset mechanism, if selected to offset by a function code, will cause the card to be offset from the other cards in the output stacker.
At the completion of the punch cycle the 415 and 3245 logic components are cleared in preparation for reselection for another punch operation.



FUNCTIONAL BLOCK DIAGRAM

CHARACTERISTICS

1.	Card Punch Cycle	240 ms
2.	Card Punch Speed	Up to 250 CPM
3.	Punch Time Per Row	7.1 ms pulse every 15 ms
4.	Read Time Per Row	2 ms pulse every 15 ms
5.	Buffer Load Time	300 u/s
6.	Card Placement	9-edge-first-face-down
7.	Punching Method	Row Binary

SWITCHES AND INDICATORS

Name	S/I*	Action
Equipment Designator Switch (Control A)	S	Designates code number selection for the controller.
Power	I	Indicates d-c voltage applied to logic.
Reserve	I	Indicates that unit has been connected by the data channel.
Parity	I	Indicates a parity error in transmission from the data channel to the controller. Turned off by M.C., Connect or Function signal.
Not Ready	I	Indicates a Not Ready condition in the punch - such as stacker full, hopper empty, etc.
Fail to Feed	I	Indicates a card failed to feed from hopper to pre-punch station; also causes Punch Not Ready condition - turned off by manually advancing cards from hopper.

CARD PUNCH AND CONTROLLER PREPARATION

1. Place cards in hopper face down with row 9 facing in the direction of card feed.
2. Turn 3245 and Punch Main Power switches on. Power On lights will come on. Check chip box to see if it is empty.
3. M. C. from computer.
4. Push single Pick button on punch to advance cards into the Punch Ready and Read Ready Stations. Ready indicator will light when cards are positioned. Punch Not Ready light and Fail to Feed light on controller should go out.
5. The 3245 and punch are now ready for control by the computer program.

CONNECT CODE

Connect Punch Equipment N(000)

The upper order three bits of the Connect code must match the setting of the Equipment Number switch for the controller. If the controller can be connected to the channel a Reply is returned to the channel, otherwise nothing happens. Once a channel is connected to the controller it has the punch reserved until a Master Clear occurs or until a new Connect code is issued to a different controller on the same data channel.

Operation	Code	Action
Connect:	N000	
Function:	0003	Select Offset Stacker
	0005	Clear
	0020	Interrupt on Ready and Not Busy
	0021	Release Interrupt on Ready and Not Busy
	0022	Interrupt on End of Operation
	0023	Release Interrupt on End of Operation
	0024	Interrupt on Abnormal End of Operation
	0025	Release Interrupt on Abnormal End of Operation

FUNCTION CODES

Offset Stacker (0003)

This code will offset the card which was read on the previous cycle. The card will be offset before entering the stacker. At the end of each punch cycle the offset stacker selection is cleared.

Interrupt on Ready and Not Busy (0020)

This code allows an interrupt to be sent to the computer via the data channel when a new operation can be started. Usually the interrupt is interpreted as signalling the completion of a manual operation. The punch is ready if (1) cards are in the hopper, punch, and read stations, and (2) the stacker is not full. The controller becomes Not Busy at the end of a punch cycle if the data channel is not busy.

Interrupt on End of Operation (0022)

The interrupt will occur when (1) all information has been transferred, the channel is no longer busy, and the punching or reading of correct record is complete or (2) if punch becomes Not Ready at the end of a punch cycle even though the channel remains active.

Interrupt on Abnormal End of Operation (0024)

The interrupt will occur at the end of a punch cycle when one of the following conditions exists: (1) feed failure or (2) punch not ready. (If interrupt on End of Operation is selected, it will also occur simultaneously with the Abnormal Interrupt.)

STATUS RESPONSE CODES

Status Responses:	XXX1	Punch Ready
	XXX3	Punch Busy
	X1XX	Fail to Feed
	X2XX	Interrupt - Ready and Not Busy
	X4XX	Interrupt - End of Operation
	1XXX	Interrupt - Abnormal End of Operation

Information is constantly available on these lines when the controller is connected to a data channel.

Punch Ready (XXX1)

The punch is ready when it can be used by the data channel. This involves several conditions including: (1) stacker not full, (2) cards present in hopper, Punch-Ready and Read-Ready stations.

Upon pressing the Punch Stop switch, the punch becomes Not Ready at the end of the current punch cycle. In this case the punch is made Ready by pushing the Ready switch (this does not advance cards). Once ready, the punch remains continuously ready until one of the aforementioned conditions arises to prevent further operation. The punch will become Not Ready only at the end of a card cycle.

Punch Busy (XXX2)

The controller is busy when the data channel is busy or the punch is busy. The channel becomes busy upon initiation of a Write or Read operation although actual punching or reading has not yet begun.

Fail to Feed (X1XX)

A feed failure means that when a punch cycle was initiated, a card did not feed from the hopper into the pre-punch station.

Interrupt Due to Ready and Not Busy (X2XX)

This bit indicates that Interrupt on Ready and Not Busy (0020) was selected and the Ready and Not Busy conditions now exist.

Interrupt Due to End of Operation (X4XX)

This bit indicates that Interrupt on End of Operation (0022) was selected and the End of Operation condition now exists.

Interrupt Due to Abnormal End of Operation (1XXX)

This bit indicates that Interrupt on Abnormal End of Operation was selected and the condition now exists.

PROGRAM CONCEPTS

Card Punching equipment is perhaps one of the hardest pieces of I/O equipment on a computer system to operate from the software standpoint. Once the utility routine for the card punch is written then all that is necessary is to "call up" this routine to handle the punch operation.

Card Punch operations have two lines of thought in the industry today, one being the hardware point of view the other being the software point of view.

The hardware point of view says the controller must contain a core buffer memory with at least 80 addressable locations. Each memory address will store a 12 bit data word. The information to be punched on cards is transferred from the computer to the controller memory. The data, after being loaded in the memory, will represent the data as it is to appear in the column form on the card. The card punch can punch a row at a time, therefore the memory in the controller is unloaded a row at a time, punched on the card until all 12 rows are complete. In other words, we are loading the controller memory column by column and unloading it row by row with the end result being the information punched on the card the same way it appeared loaded in memory.

The software point of view says the controller does not need a core buffer memory. The data to be punched on the card must be transferred a row at a time to the controller from the computer as each new row in the card punch is positioned in the punching station. The assembly of the data must be done under program control in the computer with the end result being the desired data appearing on the card in the column format.

There are good and bad things to be said of both methods. The 3245 follows the software point of view primarily because it is less expensive and also because it affords the programmer greater versatility in its use.

Assembly of the data in core memory for a punching operation must follow certain conditions:

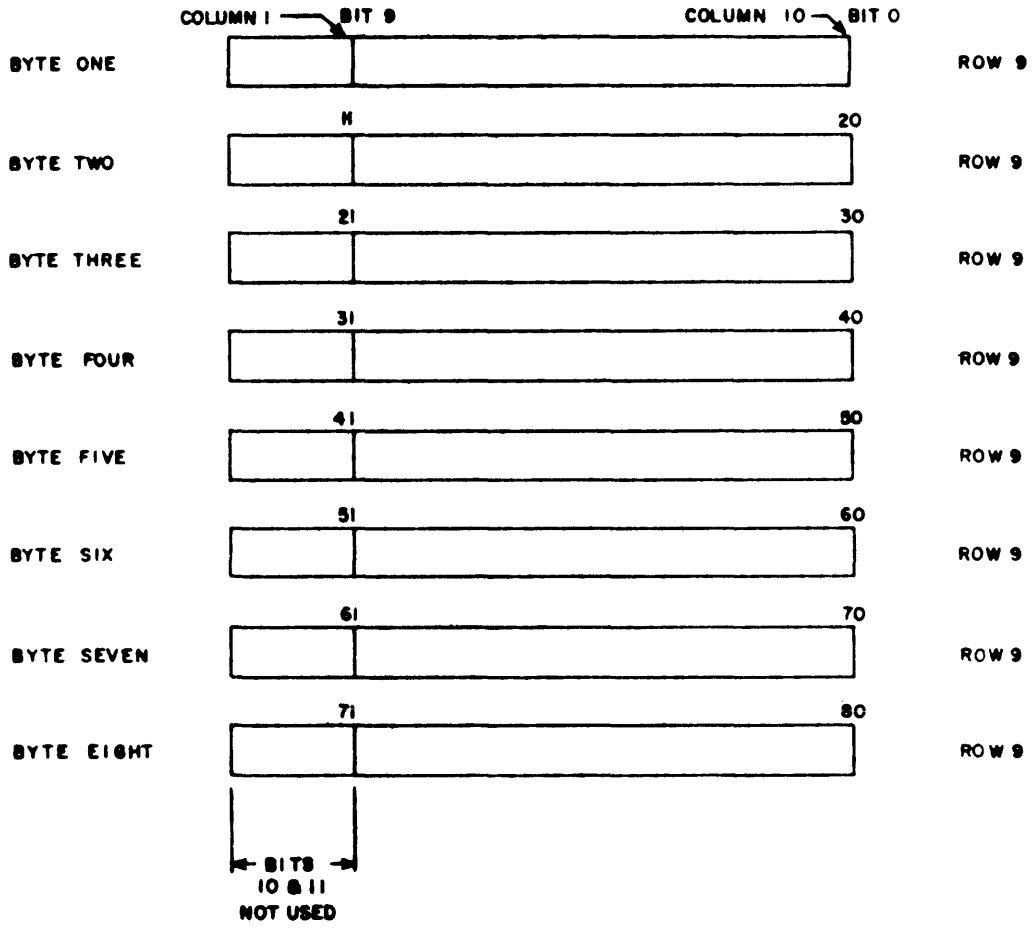
1. Each card row, beginning with Row 9, is divided into eight 12-bit bytes with bit positions 2^{11} and 2^{10} of each data byte being disregarded.

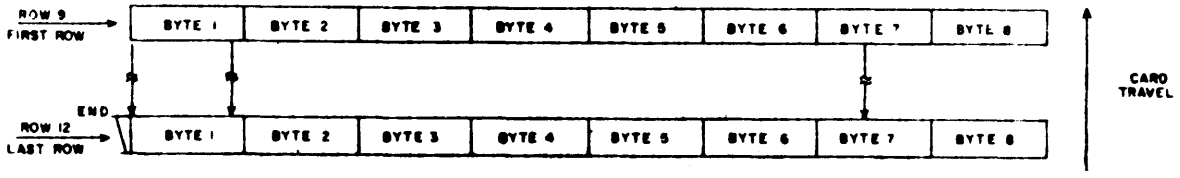
2. Each group of eight 10-bit bytes transferred must follow within 15 ms of the previous group, since a new row is positioned on the punch station every 15 ms.

3. Cards are oriented in the card punch 9 Row-first-face-down for feeding in the machine.

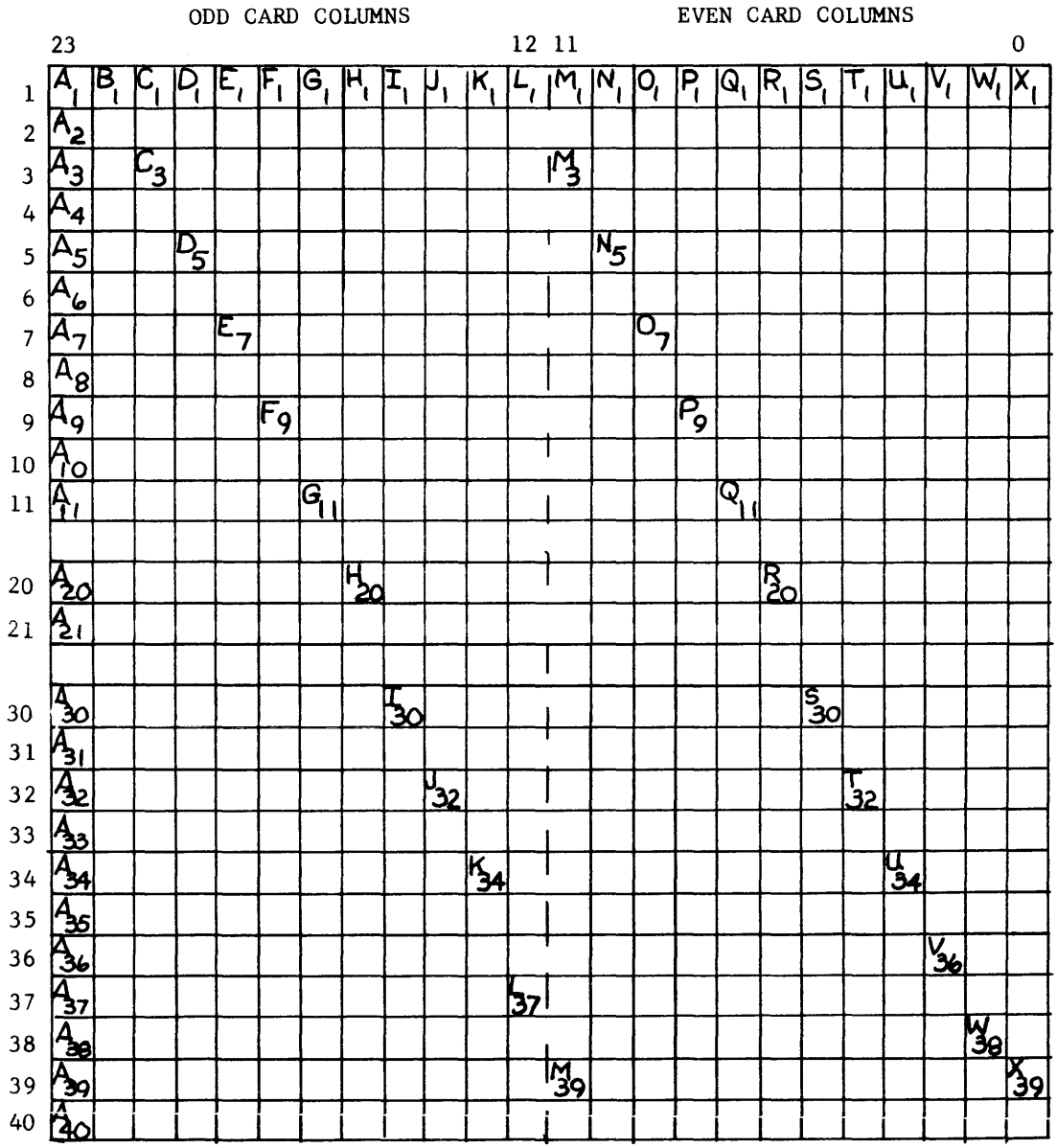
The first byte is punched in columns 1 through 10, bit 9 as column 1, bit 0 as column ten. This sequence is followed for the remaining bytes of that card row, the eighth byte being punched in columns 71 through 80. When the eight bytes of data for row nine have been transferred to the punch, the data channel may initiate a read cycle and input eight bytes of data from row nine of the card punched on the previous cycle. Reading of a card takes place one card cycle after the punching of that card because the punch station and read station are separated by the width of one card. The bit/column arrangement for reading is the same as explained above for punching.

The above sequence of punching 8 bytes, followed by the optional reading of 8 bytes, may be continued twelve times for each card cycle, i.e., one per card row. If the program does not require checking, the data Read portion of the sequence may be eliminated. Likewise, the data Write portion of the sequence may be eliminated if only reading is desired.

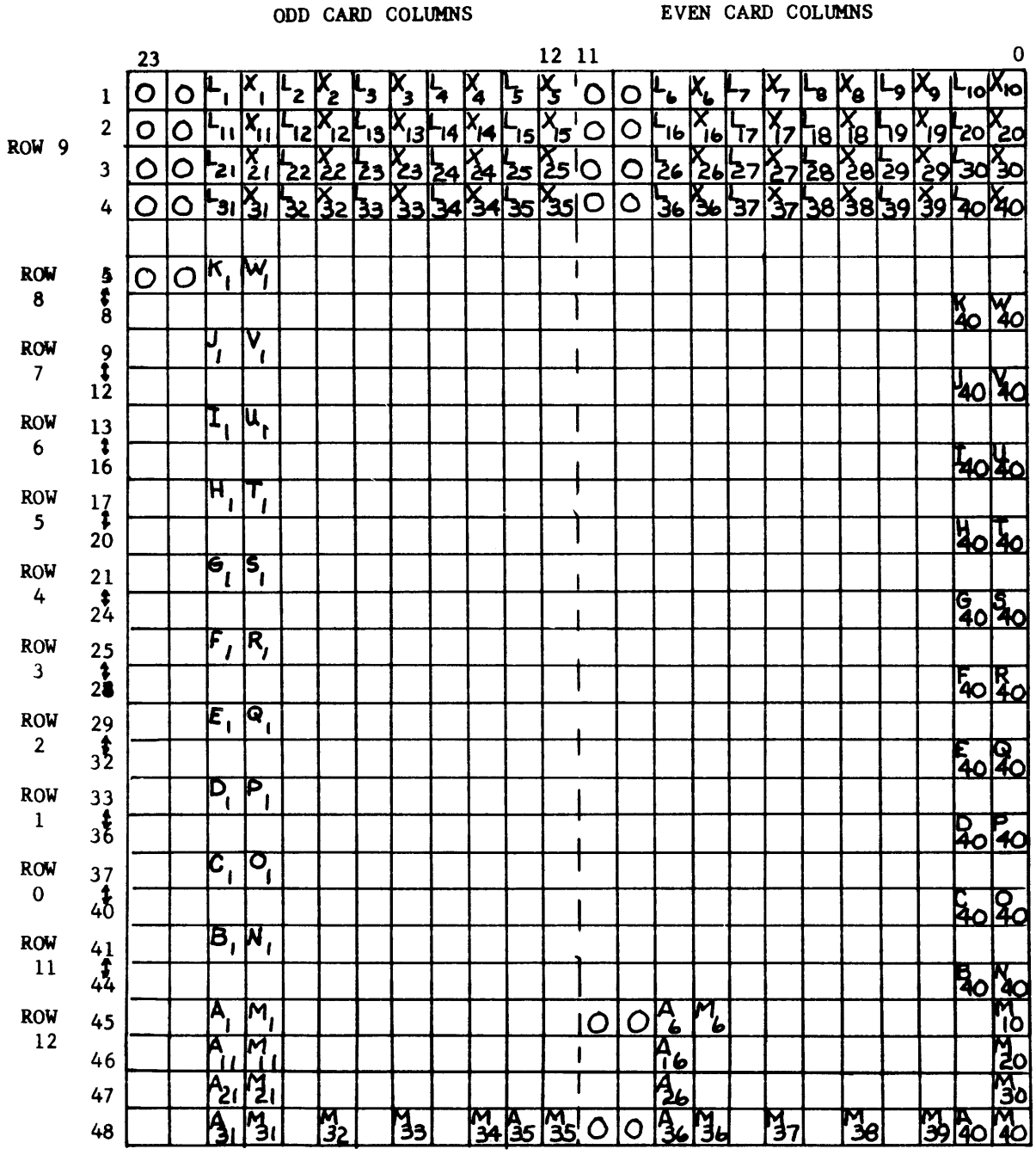




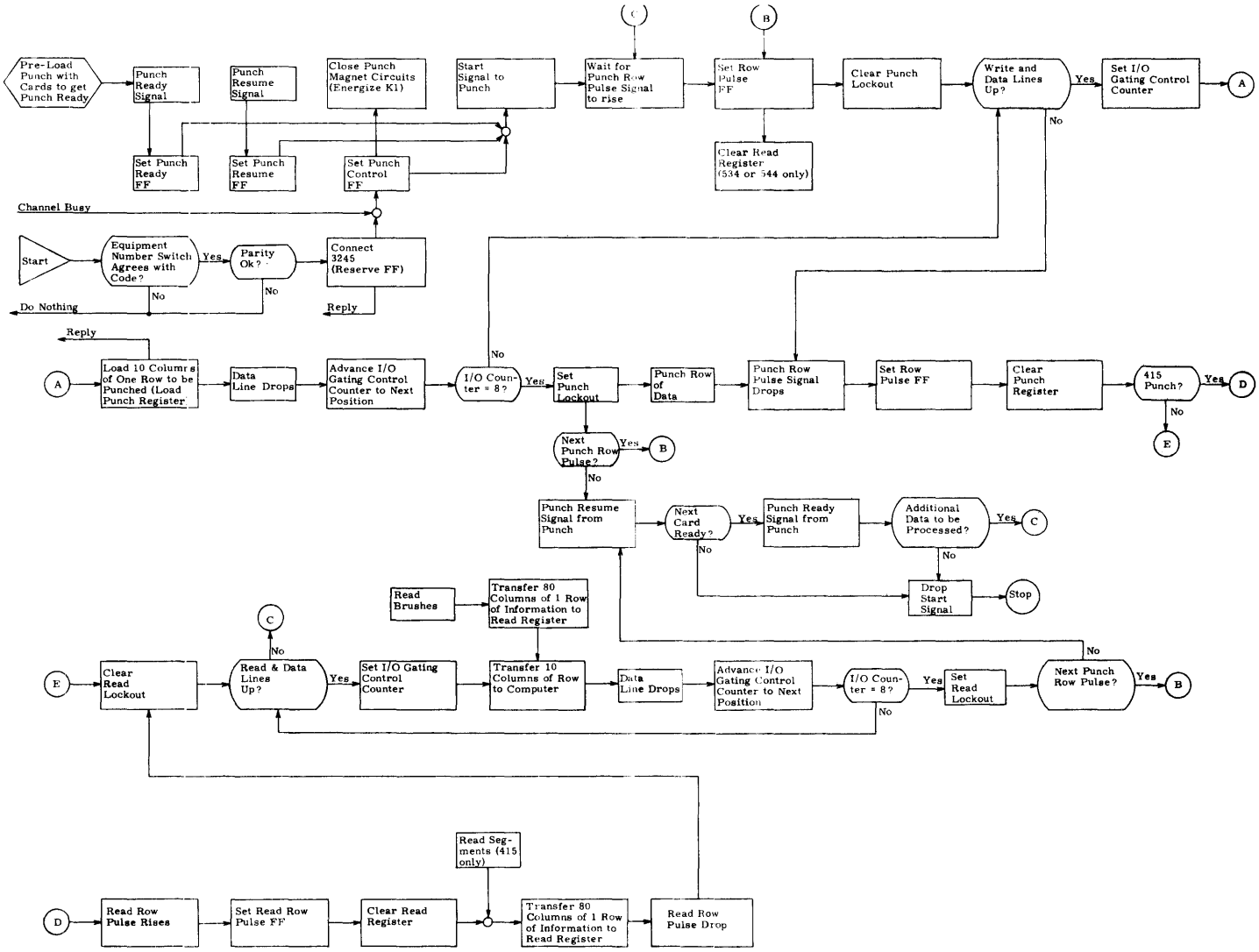
Punch Format For Each Row To Be Punched On The Card



DATA STORED IN MEMORY AS IT IS TO APPEAR ON THE CARD



DATA ASSEMBLED IN MEMORY FOR TRANSFER TO THE 3245 CONTROLLER FOR A PUNCHING OPERATION.


Pre-Load Punch with Cards to get Punch Ready
Punch Ready Signal
Punch Resume Signal
Close Punch Magnet Circuits (Energize K1)
Start Signal to Punch
Wait for Punch Row Pulse Signal to rise
Set Row Pulse FF
Clear Punch Lockout
Write and Data Lines Up?
Yes
No
Set I/O Gating Control Counter
A
B
C
Set Punch Ready FF
Set Punch Resume FF
Set Punch Control FF
Clear Read Register (534 or 544 only)
Channel Busy
Start
Equipment Number Switch Agrees with Code?
Yes
No
Parity Ok?
No
Connect 3245 (Reserve FF)
Reply
Do Nothing
Reply
A
Load 10 Columns of One Row to be Punched (Load Punch Register
Data Line Drops
Advance I/O Gating Control Counter to Next Position
I/O Counter = 8?
No
Yes
Set Punch Lockout
Punch Row of Data
Punch Row Pulse Signal Drops
Set Row Pulse FF
Clear Punch Register
415 Punch?
Yes
No
D
E
Next Punch Row Pulse?
Yes
B
No
Punch Resume Signal from Punch
Next Card Ready?
Yes
No
Punch Ready Signal from Punch
Additional Data to be Processed?
Yes
C
No
Drop Start Signal
Stop
Read Brushes
Transfer 80 Columns of 1 Row of Information to Read Register
C
No
E
Clear Read Lockout
Read & Data Lines Up?
Yes
Set I/O Gating Control Counter
Transfer 10 Columns of Row to Computer
Data Line Drops
Advance I/O Gating Control Counter to Next Position
I/O Counter = 8?
Yes
No
Set Read Lockout
Next Punch Row Pulse?
Yes
B
No
Read Segments (415 only)
D
Read Row Pulse Rises
Set Read Row Pulse FF
Clear Read Register
Transfer 80 Columns of 1 Row of Information to Read Register
Read Row Pulse Drop

FLOW CHART

SEQUENCE OF OPERATION

Master Clear or Power On M.C. (C001, C003, C004 all have a "1" output)

1. Clear P.E. FF, K020/021
2. Set Punch Lockout FF, A126/127
3. Set Read Lockout FF, E000/001
4. Clear Row Pulse FF, S500/501
5. Set $\overline{\text{Row Pulse}}$ FF, S502/503
6. Set Resume FF, S504/505
7. Clear Punch Control Busy FF, S506/507

NOTE: When the Row Pulse FF sets, C512 and C513 provide a 4 usec output:

a. Set A100/101
b. Clear A102/103 through A116/117

Since the Reserve FF, K010/011 will be cleared, a master clear should be performed prior to any Connect or Function.

CONNECT

1. R013 connect signal to "1", connect code plus parity bit.
2. Check parity.
3. Compare Bits 2^9, 2^{10}, 2^{11} of connect code to equipment select switch.

   a. If compare all inputs to J041 will be "0".

4. Set K010/011 (Reserve F/F) if compare and no parity error.

NOTE: It will clear if ~~compare~~ or parity error.

   a. J039 to "1", enabling status to the channel.

5. After 2u/sec set K014/015 (Reply) if connected and send reply to the channel via T013.
6. Channel receives reply and drops connect signal and code.

   a. J040 to "1"

      1. Clear K014/015 (Reply)
      2. Clear K018/019 (Good Parity)

NOTE: If parity error; K020/021 (Parity Error)
K010/011 (Reserve) will <u>not</u> set and no response will be sent back to the channel.
If $\overline{\text{compare}}$ on equipment code; clear K010/011
(Reserve)...and K016/017
(Reject)...can <u>not</u> be set.
There will be no reponse to the channel from this equipment.

FUNCTION

1. R014 to "1" (Function Signal)...function code plus parity bit enters the controller.
2. Check Parity

    a. If parity OK, Set K018/019 (Good Parity)...
    b. If parity error, Set K020/021 (Parity Error)...

3. If Parity OK and connected, set K012/013 (Function)

    a. J047 to "1"..,enables function code translators to the function code F/F's...
    b. If punch control busy (S527 = "1") set K016/017 (Reject) and send reject back to channel (T014)

NOTE: After 2 u/sec, the Reply F/F (K014/015) will set and a reply will be sent to the channel but the channel will have already processed the reject.

4. When the channel receives the reply or reject signal, it drops function signal and code

    a. J040 to "1"..., Clear: K014/015 (Reply)
    K016/017 (Reject)
    K018/019 (Parity OK)
    and K012/013 (Function)

NOTE: If Parity error on function, Parity Error F/F (K020/021) Sets, A Parity Error signal is sent to the channel The Function F/F (K012/013) can not set, and no response will be sent to the channel. If Punch Control Busy (S527 = "1" - send reject to the channel.

WRITE (PUNCH)

Initial conditions: Punch is ready (cards in hopper, punch station, and read station) M506 has a "1" out
Punch Resume is up, M502 and M505 = "1"
Ready F/F (S520/521) is set

1. Channel signals sent to 3245 are:
Write (R017), Ch Busy (R020), Data (R015)

    a. Set Punch Control Busy (S506/507)
    1. Energize "K1"

    b. L606 to -16V, P581 to Ov, send start signal to the 415
    Wait 1st Row Pulse

2. Punch resume (M502 to "0") drops before Row 9 comes up.
3. Row Pulse (M503 = "1") Resume Clear (M501 = "1")

    a. Clear Resume (S504/505)

        1. Drop Start Pulse to 415.

    b. Set Row Pulse (S500/501).

        1. C512 and C513 = 1's for 4 us to initiate I/O gating counter. Set A100/101, clear all other FF's in the counter.

    c. Clear $\overline{\text{Row Pulse}}$ (S502/503).

        1. C502 through C511 = 1's, which enables the feedback loops in the Output Buffer Register.

    d. Clear Punch Lockout (A126/127), S501 and S508 = 4 usec "1" Pulse.

        1. A145 = "1", enabling data sig into "A124". Wait Data Signal (R015).

4. Data Signal (R015); and Data plus parity.

    a. Parity is checked.
    b. Data (lower 10 bits) is sent to Output Buffer Register.
    c. Data Signal causes A124 to = "0" output if Punch Lockout FF, A126/127, is clear.

        1. After 2 usec delay set A102/103, A150 and A151 = 1's = PT 1.

5. PT 1 causes data bits 2^0 to 2^9 to be enabled into the 1st 10 bits of the Output Buffer Register.

    a. A123 = "1" if $\overline{\text{Punch Lockout}}$ (Write.connected).
    b. J080 = "0".
    c. After 2 usec set Reply (K014/015) and send reply to channel.

6. When channel receives reply it drops the Data signal (R015 = "0").

    a. J040 = 1

        1. Clear Reply (K014/015).
        2. Clear Parity OK (K018/019).
        3. A124 to "1", Set A104/105, which clears A100/101. This drops the PT 1 translation.

7. Second Data Signal (R015 = 1) A125 - "1".
   Set A106/107 which clears A102/103.

   a. Generate PT 2.
   b. Transfer 2nd Byte to Output Buffer Register.
   c. A123 sets Reply (K014/015), send reply.
   d. Channel drops data signal.
      1. Clear Reply (K014/015) and Parity OK (K018/019).
      2. A124 = 1 set A108/109 which clears A104/105.
         This drops the PT 2 translation.

8. PT 3 (A108/109 Sets, A110/111 Sets)
9. PT 4 (A112/113 Set, A114/115 Set)
   When 4th Data Signal drops: Set A116/117, which sets A110/111, which clears A112/113.
10. PT 5 (A100/101 Set, A102/103 Set, A119 = "1")
11. PT 6 (A104/105 Set, A106/107 Set, A119 = "1")
12. PT 7 (A108/109 Set, A110/111 Set, A119 = "1")
13. PT 8 (A112/113 Set, A114/115 Set, A119 = "1")
    When the 8th Data Signal drops

    a. Set Punch Lockout (A126/127).

NOTE: This prevents the next Data Signal from advancing the counter.

      1. A129 = "1", this forces the PT 8 translation to = "0".

         The Buffer Register now contains 80 bits and the entire transfer has taken approximately 300 usec and the 415 will punch the row.

14. Row Pulse drops (M503 = "0").

    a. Set $\overline{\text{Row Pulse}}$ (S502/503).

       1. C502 to C500 = "0", clearing the Output Buffer Register.

    b. Clear Row Pulse (S500/501).

READ (PUNCH CHECK)

1. Can be done when the Punch Row Pulse drops (M503 = 0).

   a. When the Row Pulse drops for Row 9 of the 2nd card, it is possible to do a Read operation on Row 9 of the 1st card if desired.
   b. When Row 9, Card 2 was punched, Row 9 card #1 was over the Read Station and the information was transferred to the Read Register. Read Timing came up causing M508 to output a 2ms 1. This set read row pulse FF S530/531 which cleared the Read Register prior to receiving the Row Data. If a punch were present, a ground would be applied to the M-- card feeding a Read Register FF causing it to set the corresponding FF.
   c. C512 and C513 = 1 setting A100/101 and clearing the other FF's in the counter.
   d. Clear Read Lockout (E000/001).

2. If a Read Signal comes up (R018) E004 = 1.

   a. Pulse A124 if Read Feature Enable is present and the Data Signal (J035) = 1.
   b. Set A102/103

      1. E010 = "1" and E011 = "1" and this causes a translation of RT 1.
      2. Enable column 1 through 10 to the channel data lines.
      3. The output of the Parity Generator E113 will be transferred to T012.

   c. E003 = "1"
      1. Set reply (K014/015) and send reply to the channel.

3. Channel Drops Data Signal.

   a. J040 = "1"

      1. Clear Reply (K014/015).
      2. A124 = "1"
         This sets A104/105 which clears A100/101 and drops the translation of RT 1.

4. The preceding action will take place for the remaining transfers of Bytes 2 through 8.

5. When the 8th Data Signal drops, Read Lockout (E000/001) sets preventing any more data transfers to the channel.

NOTE: When the next Row Pulse comes up, Row 8, Card 2 can be punched. When the next Row Pulse drops, Row 8, Card 1 can be read.

6. After punching Row 12, Punch Resume comes up (M502 = 1) and M505 = "1".

   a. After 1 usec set Resume (S504/505)

      1. S518 = 0 for 4 usec
      2. S505 and S515 = 1 for 4 usec

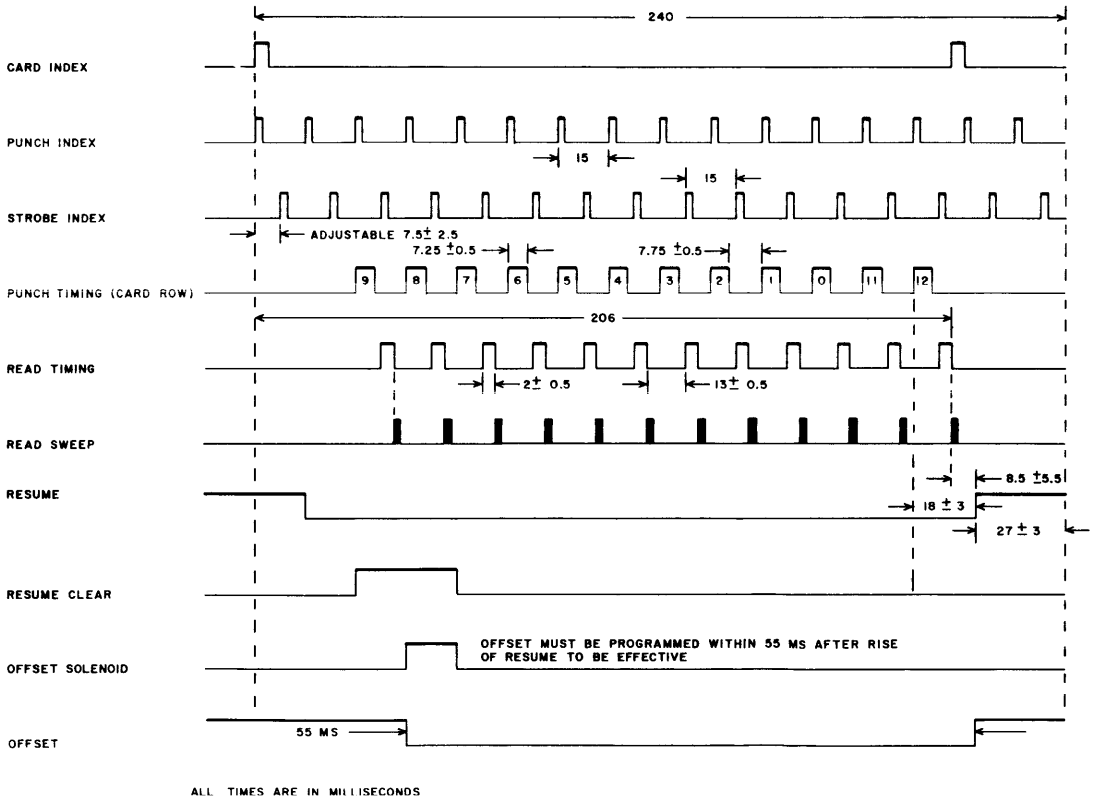
7. If Channel $\overline{\text{Busy}}$ clear Punch Control Busy (S506/507).

   a. De-energize K1.
   b. Open contacts 6-7.

8. S518 cause C004 to = "1" for 4 usec.

   a. Set Punch Lockout (A126/127).
   b. Set Read Lockout (E000/001).

415 CARD PUNCH TIMING



ALL TIMES ARE IN MILLISECONDS

FUNCTIONAL BLOCK DIAGRAM

The CONTROL DATA* 3245 Card Punch Controller receives data in 12-bit bytes and assembles eight bytes into an 80 column row for punching one card row. The controller uses only the lower 10 bits of each byte for punching. The process is repeated for each row on that card.

The punch generates 12 punch timing pulses (punch row pulses) which correspond to the 12 rows on a card. Each pulse is coincident with the time that one card row is directly above the punch die. Each row on the card has a maximum capacity of 80 bits. When the punch has a card in position to punch a row, the punch timing pulse is received in the controller. This allows the data to be transferred from the data channel to the Output Buffer register which in turn energizes the applicable punch magnets. The data channel transfers eight 12-bit bytes to the controller but after parity is checked only the lower 10 bits are positioned in the OBR.

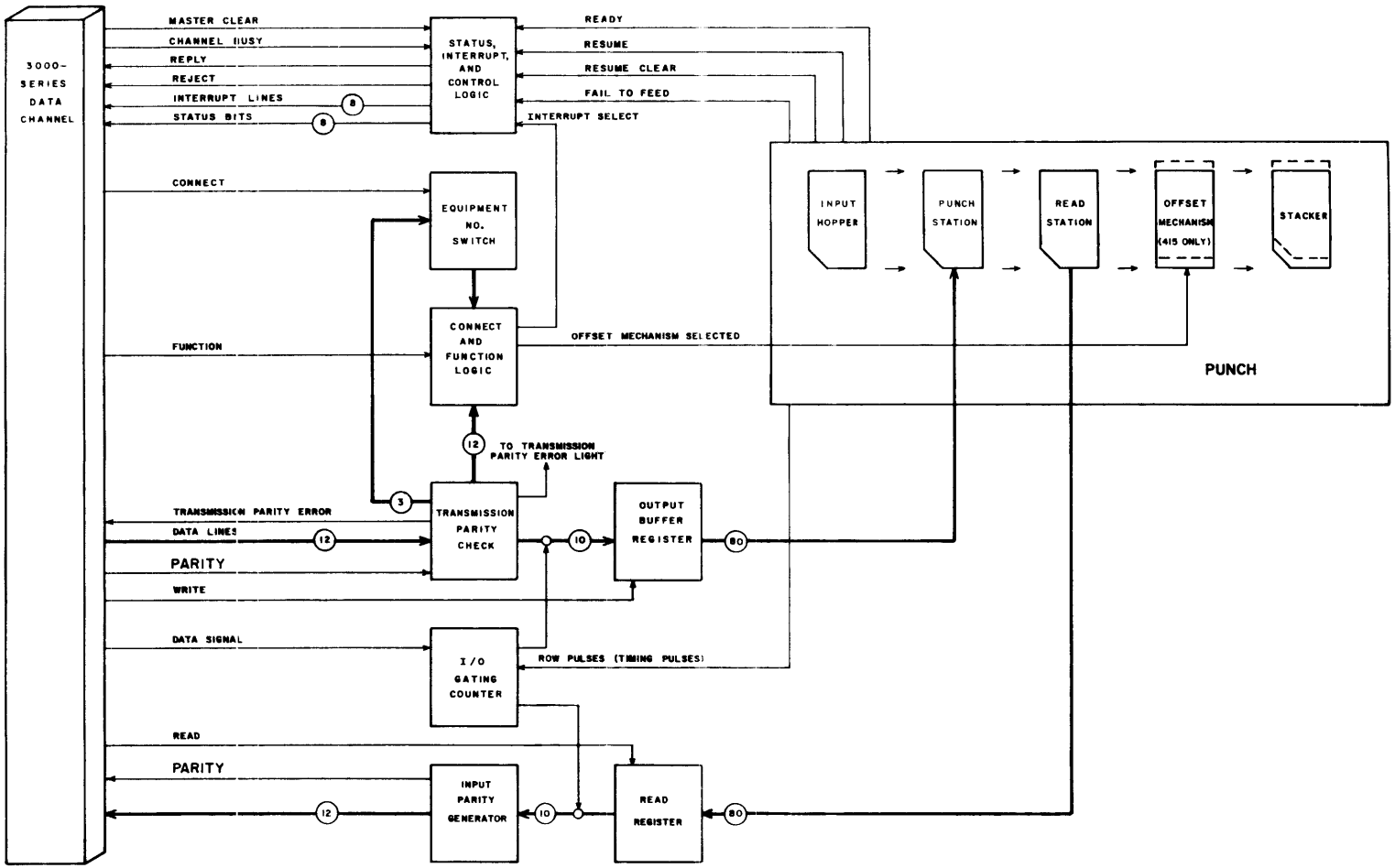
The data signal rises and falls eight times for every punch timing pulse to fill the 80-bit row.

The position of each byte as it is received in the OBR is controlled by the I/O Gating counter. When the counter reaches time eight (signifying that eight data bytes have been accepted into the OBR), a Punch Lockout is set which prevents further output data transmission until the next punch row pulse is received.

If the Read portion of the punch is used, an 80-bit row is read and transferred to the Read register. The row is then divided into eight 10-bit bytes. Each byte is checked for parity and a parity bit is generated if needed. The I/O Gating Counter gates each byte to the data channel on the rise of each Data signal. When the I/O Gating Counter reaches time eight (signifying that the eight data bytes have been transferred to the data channel) a Read Lockout is set which prevents further input data transmission until the next Read Row Pulse is received.

The punching of a card row is followed by the reading of the same row on the previous card. This is due to the construction of the punch that puts the read station one card width behind the punch station.

*Registered trademark of Control Data Corporation



FUNCTIONAL BLOCK DIAGRAM

TERM	LOCATION	PAGE	DEFINITION
A123	B30C	27	Reply on Write
E003	D01A	27	Reply on Read
J000 ↓ J004	K18B ↓ K21B	25	Function Translation ↓ Function Translation
J070 ↓ J075	I01A ↓ I01C	25	Function Translation ↓ Function Translation
K019	I14	25	Good Parity
K021	I15	25	Parity Error
S506	B35	33	Punch Control $\overline{\text{Busy}}$
S515	B29A	33	$\overline{\text{Resume}}$
S517	B29C	33	Resume
S521	B24	33	Ready
S524	B27A	33	Fail to Feed
S527	R28C	33	Punch Control Busy

CONNECT

When the Connect signal is received at the controller and the N portion of the Connect code agrees with the setting of the Equipment Number switch J041 enables the setting of the Reserve FF, providing there has been no transmission parity error. Setting the Reserve FF turns on the Reserve light on the control panel. After two usec, the Reply FF is set, sending a Reply signal to the data channel, thereby dropping the Connect signal. If the code does not agree, or if there is a parity error, the Reserve FF is cleared. (The controller does not send a Reject during a Connect oper.).

FUNCTION

When the Function signal and a function code are received by the controller, the code is sent to the function translators. If the translation yields an acceptable code, Punch Control (S506) is not busy, and there is no parity error, the Function FF and one of the Select FFs are set. (The only functions this controller responds to are the three interrupts and the Offset. The Offset function is explained below.) Two usec after Function FF has been set, a reply is sent to the data channel.

Note that sending a Reply is not predicated on the validity of a function code. Any code that has correct parity provokes a reply, even though the function specified may not be performed. If, during a Function signal, the Punch Control is busy, S527 immediately sets the Reject FF.

INTERRUPT

An interrupt code sets one of the Select FFs. When the selected condition occurs the appropriate Interrupt FF is set, turning on the interrupt transmitter and turning on the Status line indicating the condition to the data channel.

The Interrupt on Abnormal End of Operation occurs at the end of a punch cycle if the Ready FF (S520/521) has been cleared. The Ready FF can be cleared as a result of the punch going Not Ready, or a Feed Failure.

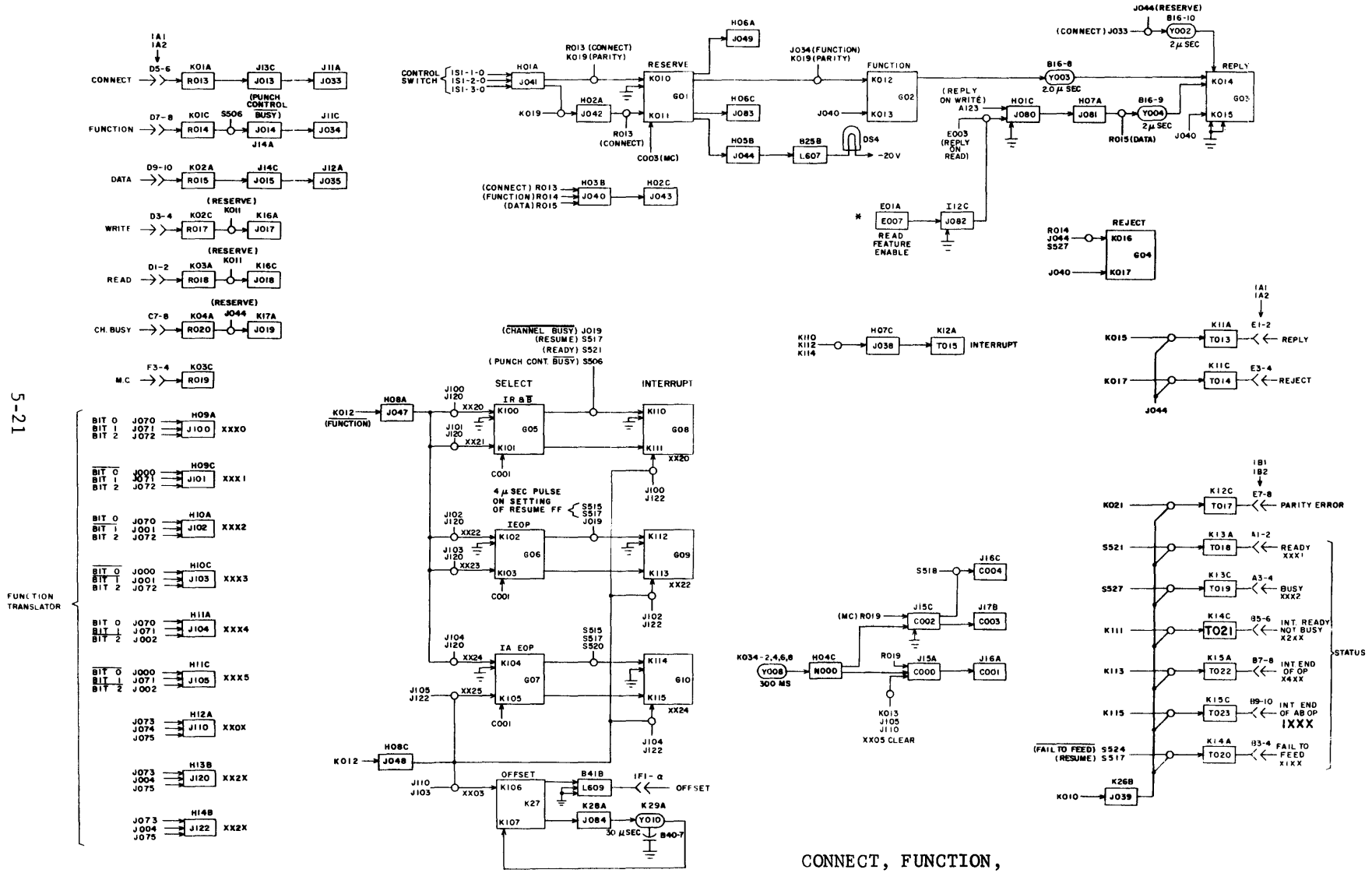
OFFSET

In the 415 Punch the programmer may at the end of any card punch cycle select the Offset function if he desires that the card which has just passed the Read station be offset before it enters the stacker. However, when offsetting a card the following limitations are inherent in the logic and must be observed.

- The function is rejected until the controller becomes Not Busy.
- After the controller becomes Not Busy, the function must be issued within 55 ms to be effective. If not, the controller still accepts the function, but the card may be only partially offset or not at all.

STATUS LINES

The Status lines indicate 1) the condition of the interrupts if they have occurred, 2) if the punch is ready or busy, and 3) if there has been a feed failure in the punch.



* THIS CARD IS PRESENT ONLY WHEN THE READ FEATURE HAS BEEN PURCHASED BY THE USER.

TERM	LOCATION	PAGE	DEFINITION
J009	K24A	25	Data Bit 9
J010	K24C	25	Data Bit 10
J011	K25A	25	Data Bit 11
J 41	Ho1A	21	Reserve Input
R009	K09A	25	Data Bit 9
R010	K09C	25	Data Bit 10
R011	K10A	25	Data Bit 11
T015	K12A	21	Interrupt

EQUIPMENT NUMBER SWITCH

The Equipment Number switch has 5 sections. Three of these sections are connected to bits 9, 10, and 11 of the data cable, and translate the Equipment portion of the Connect code to determine if the controller should be connected to the data channel. The other two sections determine which of eight Interrupt lines in the control cable transmit to the computer I/O module any Interrupt signal generated by the controller.

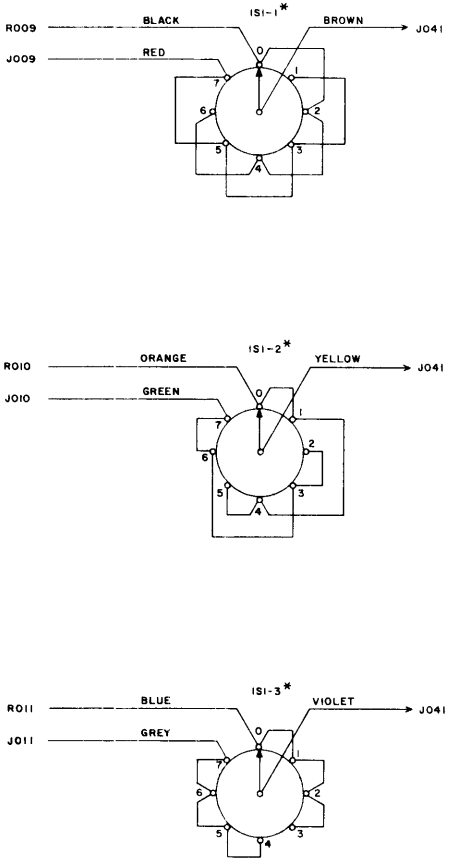
CONNECT

The R--- and J--- leads to sections 1, 2, 3 of the switch represent the true and inverted states, respectively, of the upper three bits of the Connect code. If the switch setting matches the code, the BROWN, YELLOW and VIOLET leads all present "0's" to J041. Then, if there is no Parity Error, the Reserve FF is set. Because the switch has eight positions, as many as eight controllers may be physically attached to one data channel.

INTERRUPT

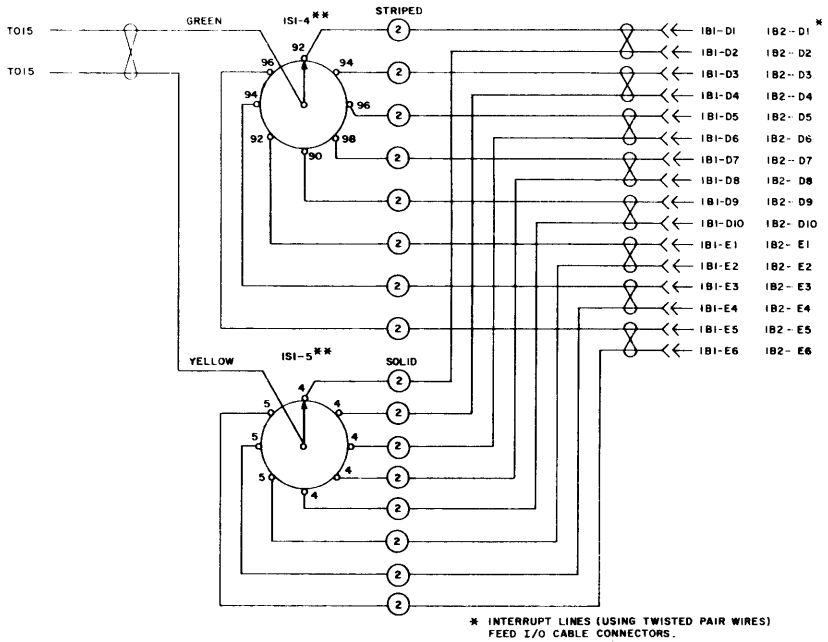
Upon the appearance of a previously selected interrupt condition, transmitter T015 produces outputs such that the GREEN wire is at -0.25 vdc, and the YELLOW wire is at +0.25 vdc. These voltages, representing the "1" state, are passed on to one of the eight twisted-pair Interrupt lines, depending upon the setting of the switch.

CONTROL A



* ON SWITCH SECTIONS 1, 2, AND 3, NUMBERING REFERS TO SWITCH POSITION, NOT PIN NUMBERS.

** ON SWITCH SECTIONS 4 AND 5, NUMBERING REFERS TO COLOR CODE OF WIRES.



* INTERRUPT LINES (USING TWISTED PAIR WIRES) FEED I/O CABLE CONNECTORS.

EQUIPMENT NUMBER SWITCH

TERM	LOCATION	PAGE	DEFINITION
C003	J17B	21	Master Clear
E060 ↓ E079	C30A ↓ C31C	29 29	Gated Outputs from Read Register
J018	K16C	21	Read
J040	H03B	21	Connect, Function, Data
J043	H02C	21	Connect, Function, Data

PARITY

The Output Parity Check checks every transmission from the data channel, (Connect, Function, Data) before it is processed by the controller.

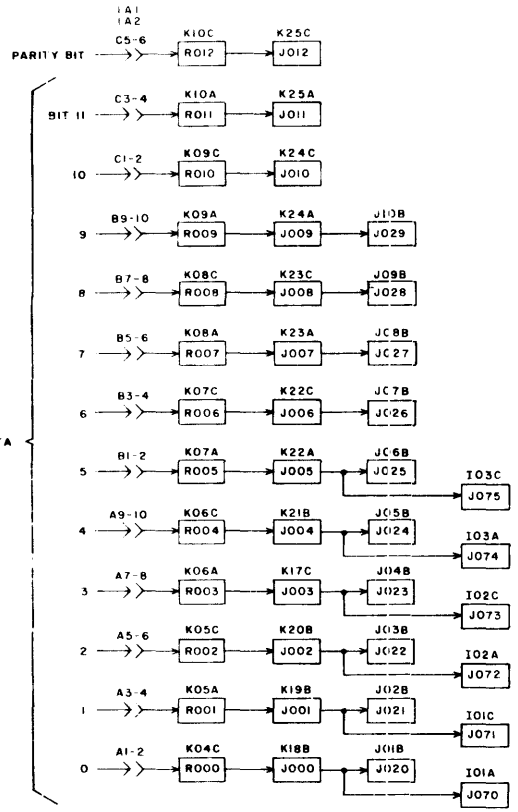
On a Connect, parity is checked and if an error occurs the Connect code is ignored, and a Parity Error is indicated.

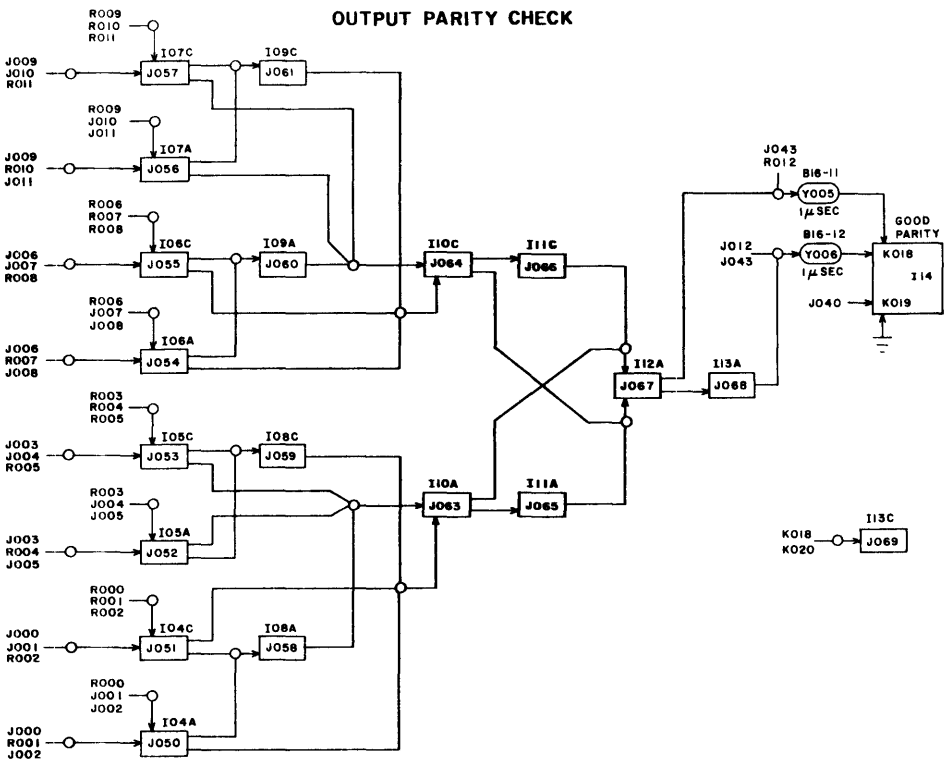
On a Function, parity is checked and if an error occurs the Function is not accepted and the Parity Error FF is set.

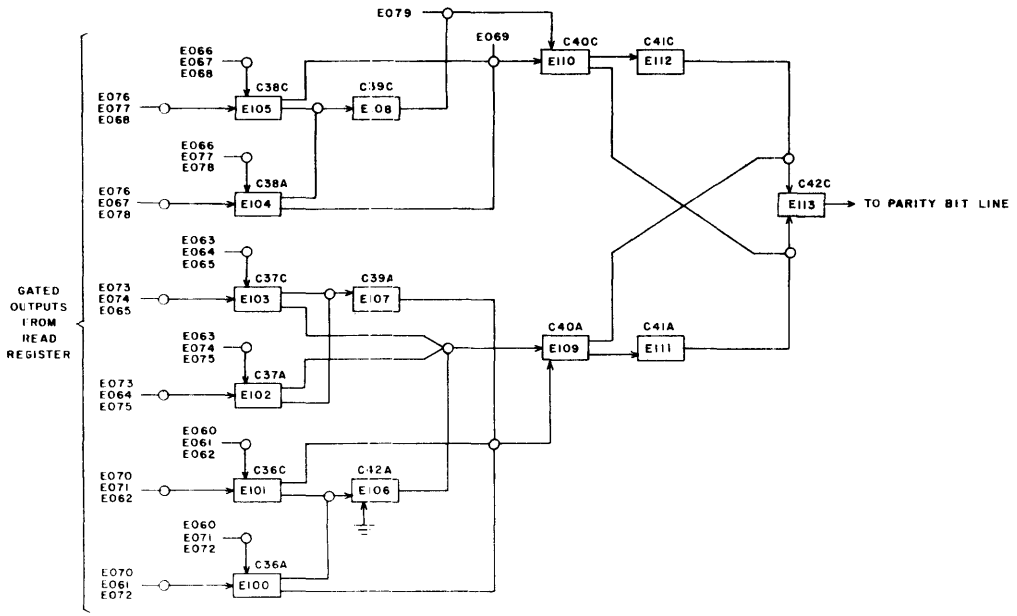
When writing, the 12-bit data byte is received from the data channel along with the parity bit. The data bits are put through the translator and checked along with the parity bit to see that odd parity is maintained. If an error occurs the Parity Error FF is set turning on the Parity Error light and energizing the Parity Error status line to the data channel. When the byte is transferred to the punch the upper two data bits are ignored as is the parity bit. (See Output Buffer Register Table, page 5-31).

When reading, the Input Parity Generator checks each 10-bit byte for parity and generates a parity bit, if needed, to maintain odd parity. The parity bit is transferred to the data channel along with the 10-bit byte.

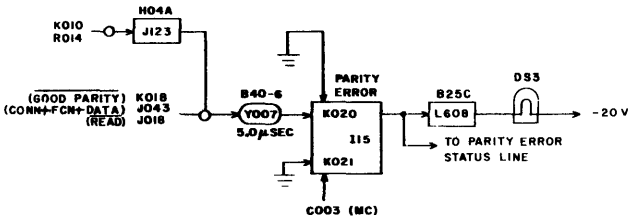
The inverter J069 is used to inhibit the I/O Gating Counter in case there is neither a Good Parity or a Parity Error. This prevents the possible transmission of erroneous information in the event of a malfunction in the Parity Check network.







INPUT PARITY GENERATOR



PARITY

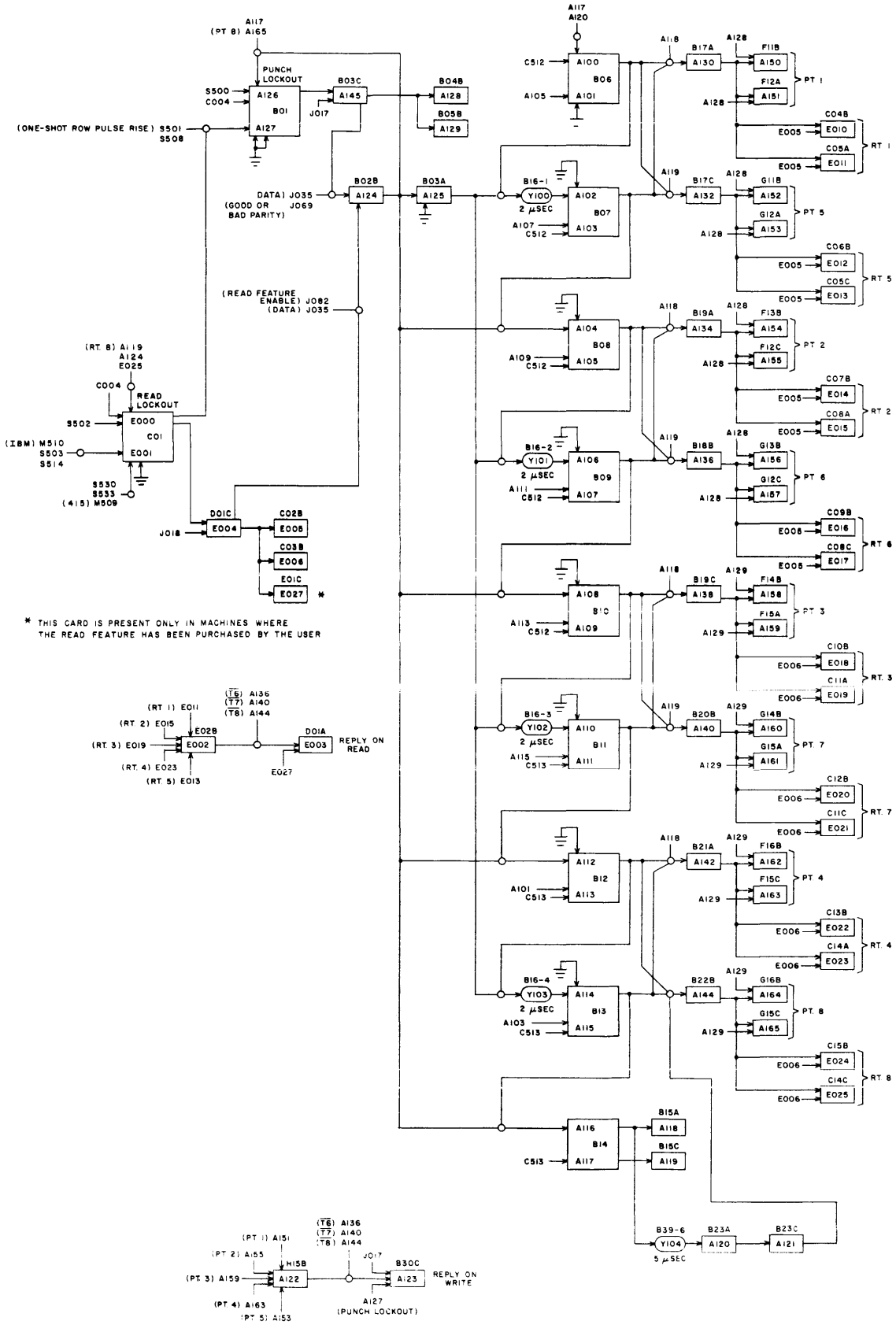
TERM	LOCATION	PAGE	DEFINITION
C004	J16C	21	Master Clear
C512	B24A	33	Row Pulse
C513	B24C	33	Row Pulse
J017	K16A	21	$\overline{\text{Write}}$
J018	K16C	21	$\overline{\text{Read}}$
J035	J12A	21	Data
J069	I13C	25	Good or Bad Parity
J082	I12C	21	$\overline{\text{Read Feature Enable}}$
M510	K32B	33	IBM Punch
S500 S501	> B38	33	Row Pulse FF
S502 S503	> B37	33	$\overline{\text{Row Pulse FF}}$
S508	B33B	33	Row Pulse
S514	B31C	33	$\overline{\text{Row Pulse}}$

INPUT/OUTPUT GATING COUNTER

The counter is used for both reading and writing. Let us assume the 3245 is cleared by a Power Up Master Clear. This sets both the Read Lockout FF and the Punch Lockout FF. The punch generates a Punch Row pulse and then a Read Row pulse for each row of data.* When the first Punch Row pulse is received the Punch Lockout FF is cleared and all the FFs in the counter are cleared except A100/101 which is set. This puts the counter into the starting position. At the rise of the data signal inverter A125 goes to a "1" and after 2 usec A103 goes to a "1". This makes the gate to A130 and Punch Time 1 (P.T.1) is signalled. A reply is returned after a 2 usec delay which in turn drops the data signal. This makes A124 to a "1" and FF A105 to a "1" advancing the counter to position #2. When the next data signal appears, after 2 usec A107 goes to a "1" gating P.T.2. The counter repeats this process until after time 4, when the data signal drops, A117 goes to a "1". This inverts A101 to a "1" and clears A113. The counter then repeats for punch times 5-8. At P.T. 8 the Punch Lockout FF is set and remains set until the rise of the next Punch Row pulse.

The data signal rises and falls eight times for every Punch Row pulse, gating each 10-bit byte to the selected magnets. (See Output Buffer Register, page 5-31).

If the Read portion is selected, after the Punch Row pulse drops the Read Row pulse appears. This clears the Read Lockout FF allowing the counter to operate in the same manner as above except that the 80-bit row read from the punch into the Read register is divided into eight 10-bit bytes under the control of the I/O Counter. At Read Time 8, the Read Lockout FF is set signifying that the eight bytes have been transferred to the data channel. The Read Lockout FF remains set until the next Read Row pulse is received.

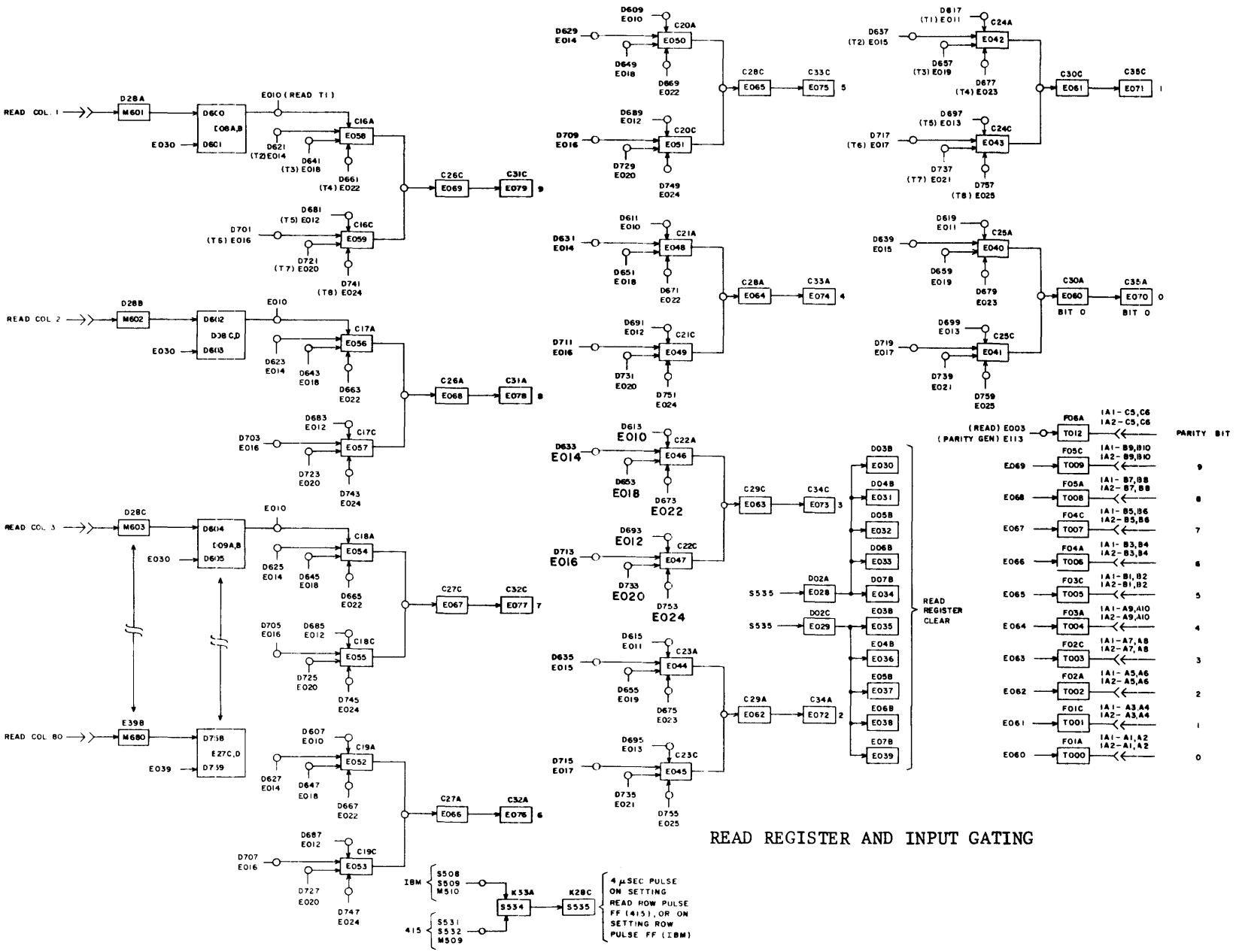

PUNCH LOCKOUT
(ONE-SHOT ROW PULSE RISE)
DATA) J035 (GOOD OR BAD PARITY)
J069
(READ FEATURE ENABLE) J082
(DATA) J035
READ LOCKOUT
(IBM) M510
(415) M509
REPLY ON READ
REPLY ON WRITE
2 μSEC
5 μSEC
PT 1
PT 2
PT 3
PT 4
PT 5
PT 6
PT 7
PT 8
RT 1
RT 2
RT 3
RT 4
RT 5
RT 6
RT. 7
RT. 8
* THIS CARD IS PRESENT ONLY IN MACHINES WHERE THE READ FEATURE HAS BEEN PURCHASED BY THE USER

TERM	LOCATION	PAGE	DEFINITION
E003	D01A	27	Reply on Read
E113	C42C	25	Parity Generator
E010 ↓	C04B ↓	27	Read Times ↓
E025	C14C	27	Read Times
M509	K32A	33	415 Punch
M510	K32B	33	IBM Punch
S508	B33B	33	Row Pulse
S509	F10A	33	Row Pulse
S531	K30	33	Read Row Pulse
S532	K31A	33	Read Row Pulse

READ REGISTER AND INPUT GATING

The Read Register receives the 80 bits of information from the Read Station. The data is then transferred, in eight 10-bit bytes, to the data channel. Column 1 of the row read is bit 9 and column 10 is bit 0, column 11 is bit 9 of the next byte and column 20 is bit 0 again.

A 4 usec pulse from S535 clears the Read Register FFs, D600/601 through D758/759. When using the 415, this pulse is generated when the Read Timing pulse sets the Read Row Pulse FF. For the IBM punches, the pulse is generated by the setting of the Row Pulse FF. Transfer of the eight bytes is controlled by the I/O Gating Counter. Transmitter cards T000 through T009 deliver the data proper, and T012 adda a parity bit if needed to maintain odd parity. The parity generator is shown on page 5-25.



READ REGISTER AND INPUT GATING

Col. #	Bit	Read M6-- Sym.	Read M6-- Loc.	Read Register Sym.	Read Register Loc.	Gate Sym.	Gate Loc.	E04- Sym.	E04- Loc.	Reg. Clear Sym.	Reg. Clear Loc.
1	9	M601	D28A	D600/D601	D08AB	E010	C04B	E058	C16A	E030	D03B
	8		B		CD			E056	C17A		
	7		C		D09AB			E054	C18A		
	6		D29A		CD			E052	C19A		
	T1 5		B					E050	C20A		
	4		C			E010	C04B	E048	C21A		
	3		D30A			E010	C04B	E046	C22A		
	2		B			E011	C05A	E044	C23A	E030	D03B
	1		C			E011	C05A	E042	C24A	E031	D04B
10	0	M610	D31A	D618/D619		E011	C05A	E040	C25A		
	9		B			E014	C07B				
	8		C								
	7		D32A								
	6		B								
	T2 5		C								
	4		D33A			E014	C07B			E031	D04B
	3		B			E014	C07B			E032	D05B
	2		C			E015	C08A				
	1		D34A			E015	C08A				
20	0	M620	B	D638/D639		E015	C08A				
	9		C			E018	C10B				
	8		D35A								
	7		B								
	6		C							E032	D05B
	T3 5		D36A							E033	D06B
	4		B			E018	C10B				
	3		C			E018	C10B				
	2		D37A			E019	C11A				
	1		B			E019	C11A				
30	0	M630	C	D658/D659		E019	C11A				
	9		D38A			E022	C13B				
	8		B							E033	D06B
	7		C							E034	D07B
	6		D39A								
	T4 5		B								
	4		C			E022	C13B				
	3		D40A			E022	C13B				
	2		B			E023	C14A				
	1		C			E023	C14A				
40	0	M640	D41A	D678/D679	D27CD	E023	C14A			E034	D07B

Col. #	Bit	Read M6-- Sym.	Read M6-- Loc.	Read Register Sym.	Read Register Loc.	Gate Sym.	Gate Loc.	E04- Sym.	E04- Loc.	Reg. Clear Sym.	Reg. Clear Loc.
41	9	M641	D41B	D680/D681	E08AB	E012	C06B	E059	C16C	E035	E03B
	8		C		CD			E057	C17C		
	7		D42A					E055	C18C		
	6		B					E053	C19C		
	T5 5		C					E051	C20C		
	4		E28A			E012	C06B	E049	C21C		
	3		B			E012	C06B	E047	C22C		
	2		C			E013	C05C	E045	C23C	E035	E03B
	1		E29A			E013	C05C	E043	C24C	E036	E04B
50	0	M650	B	D698/D699		E013	C05C	E041	C25C		
	9		C			E016	C09B				
	8		E30A								
	7		B								
	6		C								
	T6 5		E31A								
	4		B			E016	C09B			E036	E04B
	3		C			E016	C09B			E037	E05B
	2		E32A			E017	C08C				
	1		B			E017	C08C				
60	0	M660	C	D718/D719		E017	C08C				
	9		E33A			E020	C12B				
	8		B								
	7		C								
	6		E34A							E037	E05B
	T7 5		B							E038	E06B
	4		C			E020	C12B				
	3		E35A			E020	C12B				
	2		B			E021	C11C				
	1		C			E021	C11C				
70	0	M670	E36A	D738/D739		E021	C11C				
	9		B			E024	C15B				
	8		C							E038	E06B
	7		E37A							E039	E07B
	6		B								
	T8 5		C								
	4		E38A			E024	C15B				
	3		B			E024	C15B				
	2		C			E025	C14C				
	1		E39A			E025	C14C				
80	0	M680	B	D758/D759	E27CD	E025	C14C			E039	E07B

READ REGISTER TABLE

The Read Register table shows which column of the card row is read into which FF of the **Read Register.** It also gives the gating terms and the locations of all these cards.

Punch

Col. #	Bit	Data Sym.	Data Loc.	Gate Sym.	Gate Loc.	B5-- Sym.	B5-- Loc.	L5-- Sym.	L5-- Loc.	P5-- Sym.	P5-- Loc.	Clear Sym.	Clear Loc.
1	9	J029		A150		B501	F17A	L501	H16A	P501	I16A	C502	F37B
2	8	J028				02	C		H16B		I16B		
3	7	J027				03	F18A		H16C		I16C		
4	6	J026				04	C				I18A		
5	5	J025				05	F19A				I18B		
6	4	J024				06	C				I18C		
7	3	J023		A150		07					I20A		
8	2	J022		A151		08					I20B	C502	F37B
9	1	J021				09					I20C	C503	F38B
10	0	J020		A151		10							
11	9	J029		A154		B511		L511		P511			
	8												
	7												
	6												
	5												
	4											C503	F38B
	3			A154								C504	F39B
	2			A155									
	1												
	0	J020		A155									
21	9	J029		A158		B521		L521		P521			
	8												
	7												
	6											C504	F39B
	5											C505	F40B
	4												
	3			A158									
	2			A159									
	1												
	0	J020		A159									
31	9	J029		A162		B531		L531		P531			
	8											C505	F40B
	7											C506	F41B
	6												
	5												
	4												
	3			A162									
	2			A163									
	1												
	0	J020		A163			F36C		H29A		I42A	C506	F41B

SEE PAGE 7

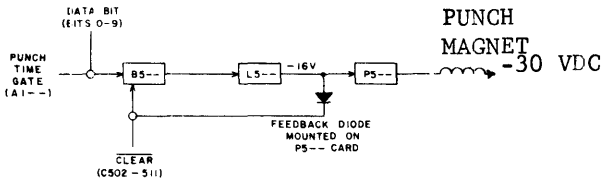
SEE PAGE 9

Punch

Col. #	Bit	Data Sym.	Data Loc.	Gate Sym.	Gate Loc.	B5-- Sym.	B5-- Loc.	L5-- Sym.	L5-- Loc.	P5-- Sym.	P5-- Loc.	Clear Sym.	Clear Loc.
41	9	J029		A152		B541	G17A	L541	H29B	P541	I42B	C507	G37B
	8						C				I42C		
	7						G18A				J18A		
	6						C				J18B		
	5										J18C		
	4										J20A		
	3			A152									
	2			A153								C507	G37B
	1											C508	G38B
	0	J020		A153									
51	9	J029		A156		B551		L551		P551			
	8												
	7												
	6												
	5												
	4											C508	G38B
	3			A156								C509	G39B
	2			A157									
	1												
	0	J020		A157									
61	9	J029		A160		B561		L561		P561			
	8												
	7												
	6											C509	G39B
	5											C510	G40B
	4												
	3			A160									
	2			A161									
	1												
	0	J020		A161									
71	9	J029		A164		B571		L571		P571			
	8											C510	G40B
	7											C511	G41B
	6												
	5												
	4												
	3			A164									
	2			A165									
	1												
	0	J020		A165		B580	G36C	L580	H42B	P580	J42B	C511	G41B

SEE PAGE 7

SEE PAGE 9



OUTPUT BUFFER REGISTER

TERM	LOCATION	PAGE	DEFINITION
0003	J17B	21	Master Clear
J044	H05B	21	Reserve
J083	H06C	21	Reserve
R020	K04A	21	Channel Busy

PUNCH CIRCUIT TIMING

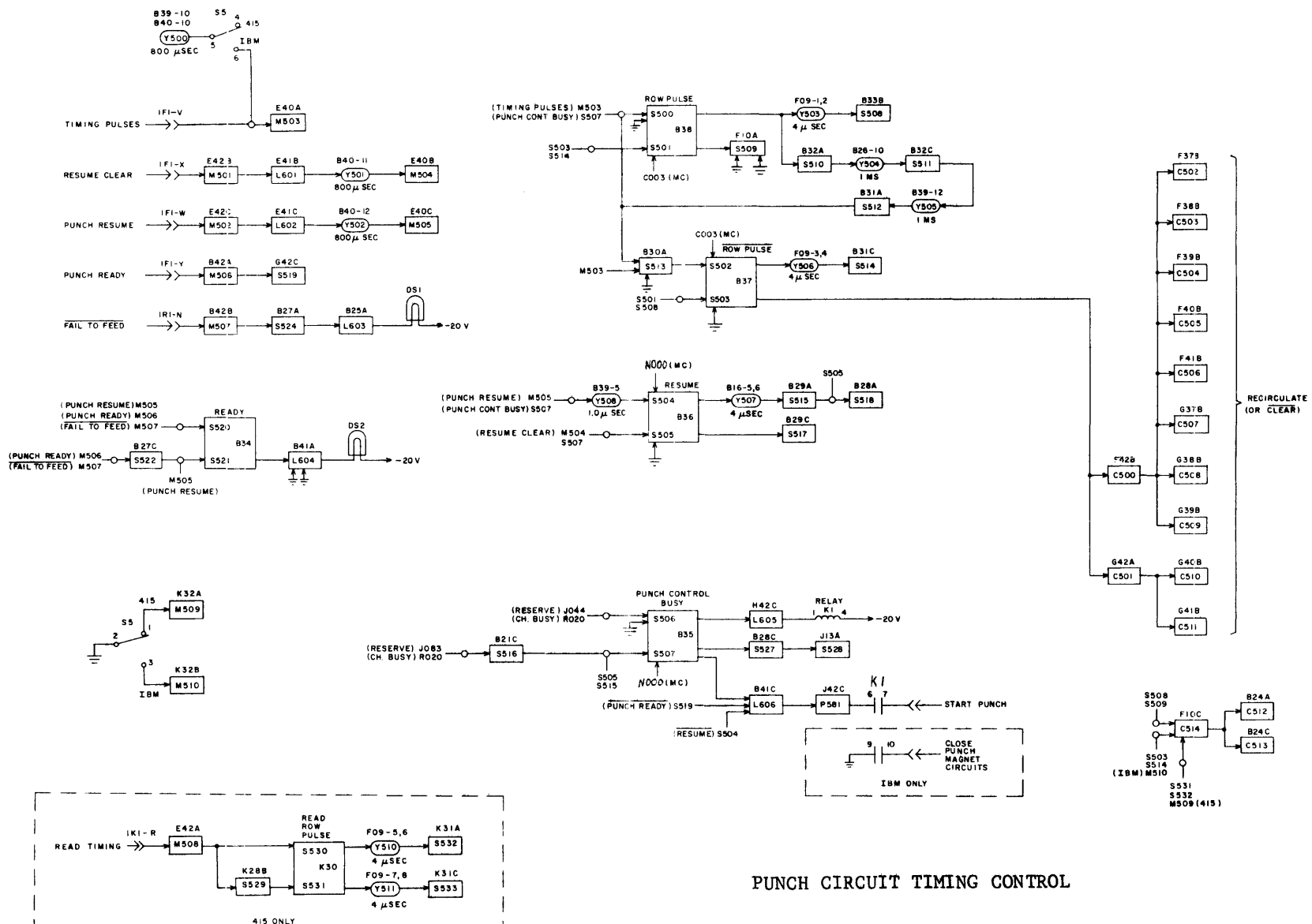
The Punch Circuit Timing* is controlled by pulses generated by the punch. When starting originally, a Master Clear sets the Resume FF and clears the Punch Control Busy FF; also the Row Pulse FF is set and the Row Pulse FF is cleared. When the Channel Busy signal is received from the data channel, the Punch Control Busy FF is set, energizing relay K1 and closing the Punch Magnet circuits. If the static Punch Ready signal is present (generated by the punch being made ready), the punch starts and a series of punch timing pulses are generated.

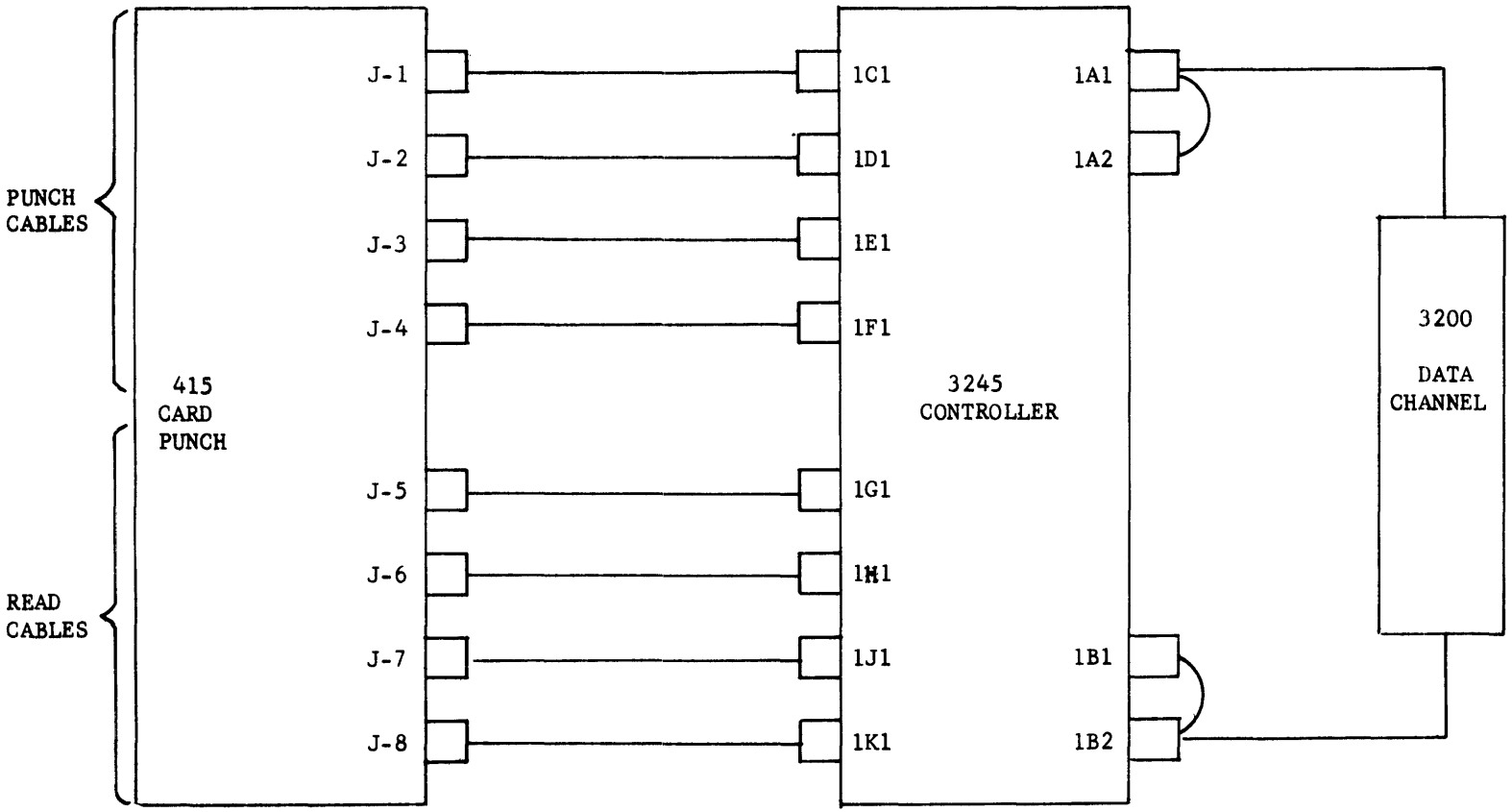
NOTE

The 415 punch generates separate timing pulses for Punch and Ready. One set of pulses from the IBM units is used for both Punch and Read. To distinguish the two operations, pulses which initiate punching or reading a card are called punch timing pulses and read timing pulses, even though, strictly speaking, the IBM punches do not generate them separately. A punch timing pulse always sets the Row Pulse FF. Read operations in IBM units are initiated by setting the Row Pulse FF; for the 415, a read operation is initiated by setting the Read Row Pulse FF.

When the first punch timing pulse is received, the Row Pulse FF is set and a 4 usec pulse clears the Row Pulse FF. This allows the Recirculate inverters to enable the bit recirculation gates in each stage of the Output Buffer Register. The Recirculate inverters hold the punch magnets closed until all the eight bytes for one row are received and the punch has processed the row of data. When the timing pulse drops the Row Pulse FF is set and the Row Pulse FF is cleared. The delay on the Row Pulse FF is used for noise suppression and to inhibit spurious timing pulses from the punch cam.

The above sequence continues for all twelve rows on the card. The Resume Clear is generated some time during the punch cycle. This clears the Resume FF, which drops the Start signal to the punch, but the punch is already rotating and completes one card cycle, generating the twelve pulses before it latches up. When all the Row Pulses for the first card are passed and the Punch Resume signal comes up again, the Resume FF is set and the controller is ready for the next punch operation. The controller stops the punch at the end of a punch cycle if the punch goes not ready, or if the Resume signal is not received from the punch, or if the Channel Busy signal is dropped.


PUNCH CIRCUIT TIMING CONTROL
TIMING PULSES
RESUME CLEAR
PUNCH RESUME
PUNCH READY
FAIL TO FEED
READ TIMING
800 μSEC
IBM
415 ONLY
IBM ONLY
CLOSE PUNCH MAGNET CIRCUITS
START PUNCH
RECIRCULATE (OR CLEAR)
-20 V



CABLE IDENTIFICATION

PUNCH CABLES

Pin	1C1	1D1	1E1	1F1
A	Punch Col. 1	Punch Col. 22	Punch Col. 43	Punch Col. 64
B	2	23	44	65
C	3	24	45	66
D	4	25	46	67
E	5	26	47	68
F	6	27	48	69
H	7	28	49	70
J	8	29	50	71
K	9	30	51	72
L	10	31	52	73
M	11	32	53	74
N	12	33	54	75
P	13	34	55	76
R	14	35	56	77
S	15	36	57	78
T	16	37	58	79
U	17	38	59	80
V	18	39	60	Punch Timing (Row) Pulses
W	19	40	61	Punch Resume
X	20	41	62	Punch Resume Clear
Y	21	42	63	523 Ready
Z	Suppression	Suppression	Suppression	Start Punch
a	Suppression	Suppression	Close Punch Magnets	Start Punch Common
b	GND	GND	GND	GND

READ CABLES

Pin	1G1	1H1	1J1	1R1
A	Read Col. 1	Read Col 24	Read Col. 47	Read Col. 70
B	2	25	48	71
C	3	26	49	72
D	4	27	50	73
E	5	28	51	74
F	6	29	52	75
H	7	30	53	76
J	8	31	54	77
K	9	32	55	78
L	10	33	56	79
M	11	34	57	80
N	12	35	58	Fail to FEED
P	13	36	59	Offset Stacker
R	14	37	60	
S	15	38	61	
T	16	39	62	
U	17	40	63	
V	18	41	64	
W	19	42	65	
X	20	43	66	
Y	21	44	67	
Z	22	45	68	
a	23	46	69	
b	GND	GND	GND	GND

3245 Card Punch Controller

Study Questions

1. Consider an output to the 415 from the 3245. What is the proper sequence of events starting after a connect in the 3245 regarding the functions listed below?

    1. Row Pulse
    2. Punch Resume Clear Signal
    3. Punch Resume Signal
    4. Punch Control (Busy) FF sets
    5. Data Signal
    6. Reply
    7. Punch Time #1

2. What causes the Punch Lockout FF A^{126}_{127} to set?

    a. When A^{112}_{113} sets.
    b. When A^{108}_{109} clears.
    c. When we get PT8.
    d. When the 8th Data Pulse drops.

3. What purpose does setting A116/117 serve?

    a. Enables the Reply Signal for each Data Signal stepping the gating control.
    b. Enables PT5 through PT8.
    c. Enables RT1 through RT4.
    d. Enables setting of the Read Lockout FF E^{000}_{001}.
    e. More than one of the above is correct.

4. Malfunction: Open input to A120. What times would be missing?

   a. PT-1 only.

   b. PT-1 through PT-8.

   c. PT-4 through PT-8.

   d. PT-5 through PT-8.

5. During Data Channel output to the 415 punch the counter in the 3245 cycles

   a. PT-1 through PT-8 for each card.

   b. PT-1 through PT-4 for each row pulse.

   c. PT-1 through PT-8 for each card row.

   d. PT-1 for the first row; PT-2 for the second row, etc.

6. The word transfer from Data Channel to the 3245 consists of:

   a. Eight 10-bit words with 2^1 and 2^0 bit positions dropped in the computer for each row.

   b. Eight 12-bit words with 2^{11} and 2^{10} dropped prior to being stored in the buffer register for each row.

   c. Two 40-bit words with each word dropping the upper 8-bit positions for each row.

   d. Eight 12-bit words with the 8th word losing the 2^3 through 2^0-bit position.

7. During the read cycle for each row in the 415 the 3245 Read Register receives the eight 10-bit words in a column binary word format.

   a. True

   b. False

8. With the Read Feature Enable (E007) removed information can be read back to the data channel via 3245 for a Punch Error Check.

   a. True

   b. False

9. The Start Signal to the 415 from the 3245 must be present until after the last row on the card is punched, then it can be dropped.

   a. True

   b. False

   Briefly state why you chose the answer you did in regard to circuit action.

10. Briefly describe the logic action of the 3245 if a Parity Error were to occur on a connect operation.

11. Briefly describe the logic action of the 3245 if a Fail to Feed signal comes from the 415.

12. The status lines to the Data Channel are enabled for a status check after a Connect has been completed.

   a. True

   b. False

13. The Function Translator will examine the connect code to determine if connect code matches the equipment switch setting during a Connect Operation.

   a. True

   b. False

APPENDIX A

STUDY QUESTION ANSWERS

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STUDY QUESTION ANSWERS

CHAPTER I

1. a
2. c
3. c
4. a,c,d
5. b
6. d
7. b
8. d
9. c
10. b
11. c
12. d
13. A COMPUTER, WITHOUT A PROGRAM, IS A HIGH SPEED MORON
14. b

CHAPTER II

1. b
2. c
3. b
4. b
5. c
6. c
7. c
8. b
9. c
10. b
11. b
12. b
13. c
14. b
15. b
16. b
17. b
18. c
19. b
20. b
21. a
22. b
23. c
24. d
25. b
26. a
27. a
28. c
29. a
30. c
31. b
32. b
33. a
34. b
35. a

CHAPTER III

1. No. A function cannot be performed while the data channel is busy reading or writing.
2. a
3. b
4. b
5. b
6. a
7. b
8. c
9. d
10. b
11. b
12. b
13. a
14. d
15. c
16. d
17. c
18. a

CHAPTER IV

1. d.
2. b.
3. d.
4. c.
5. b.
6. b.
7. b.
8. b.
9. d.
10. c.
11. d.
12. c.
13. a.
14. a.
15. b.
16. b.

CHAPTER V

1. 3,4,2,1,5,7,6
2. d.
3. e. (b&d)
4. d.
5. c.
6. b.
7. b.
8. b.
9. b.
10. Set the Parity Error F/F, No Connect, No Reply.
11. Ready F/F will not set, start pulse cannot be sent to punch.
12. a.
13. b.