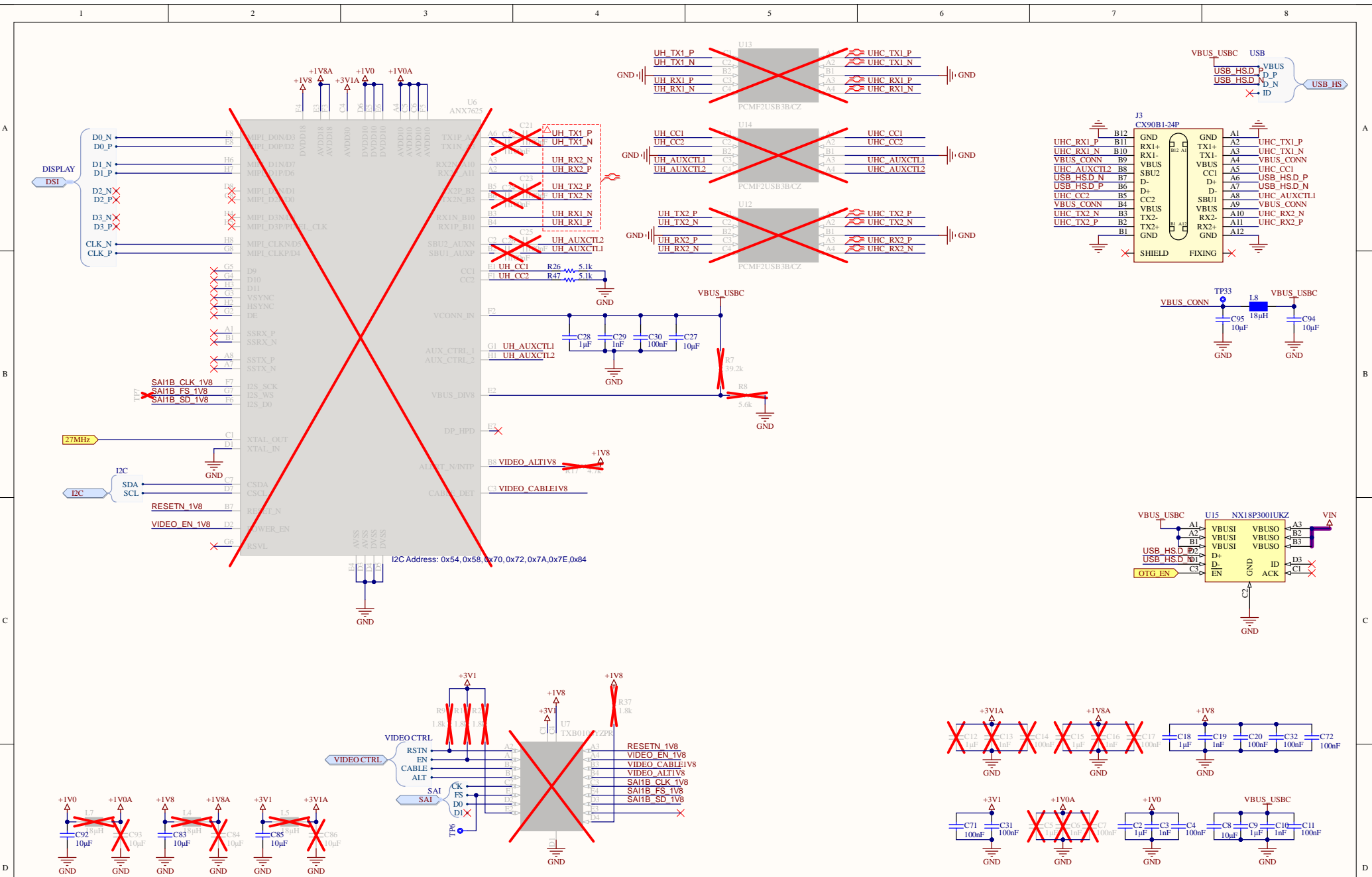


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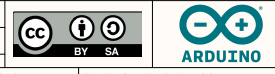
<b>Title: PortentaH7</b>				
ID: SL-ABX00045				
Date: 9/6/2021	Time: 5:35:53 PM	Sheet 1 of 10		
File: TopView.SchDoc		Author: Arturo Guadalupi		RevAuthor: Dario Pennisi

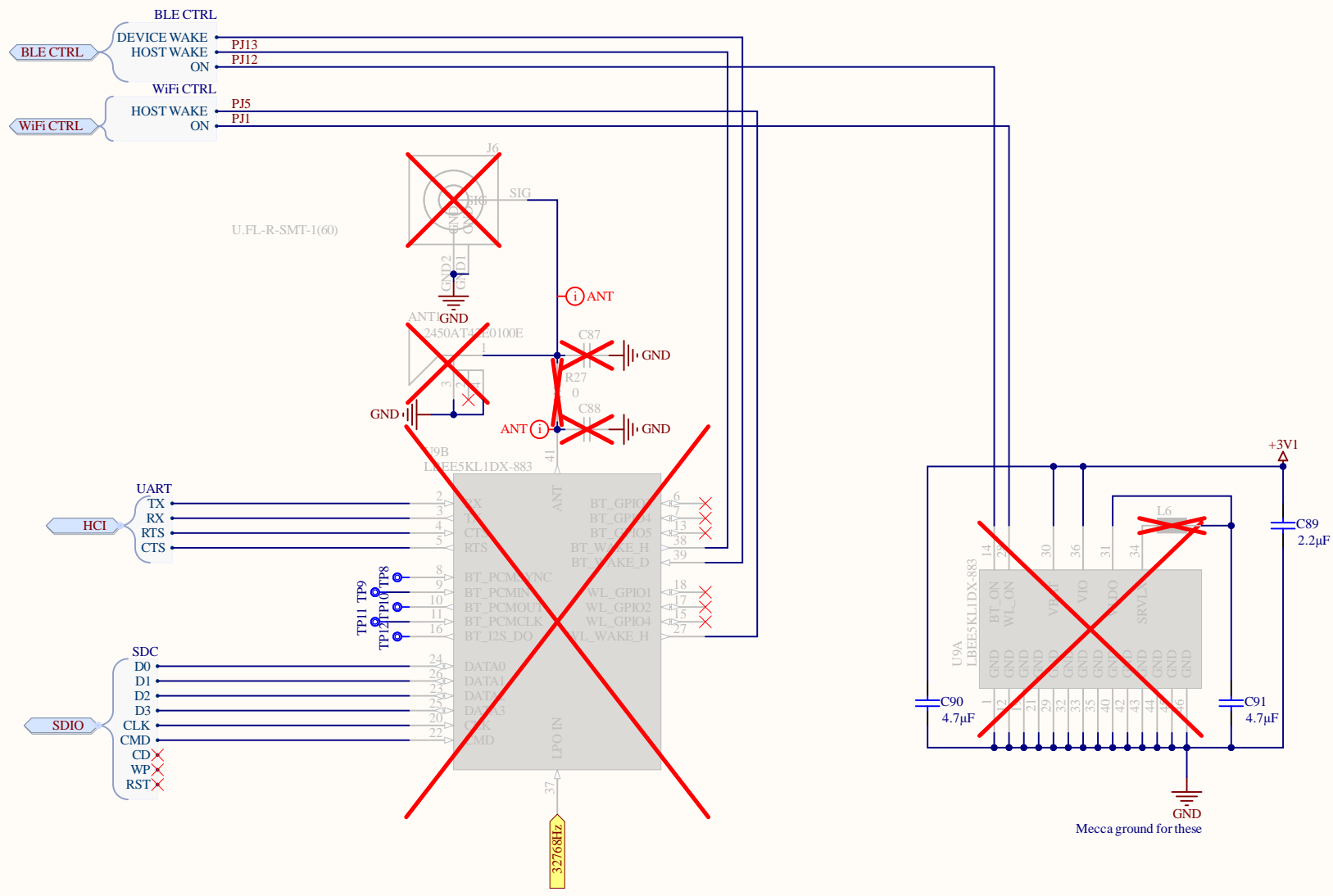




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Title: <b>PortentaH7</b>		Revision: 4.0	
ID: <b>SL-ABX00045</b>		Sheet 3 of 10	
Date: 9/6/2021	Time: 5:35:56 PM	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi
File: Video_SchDoc			

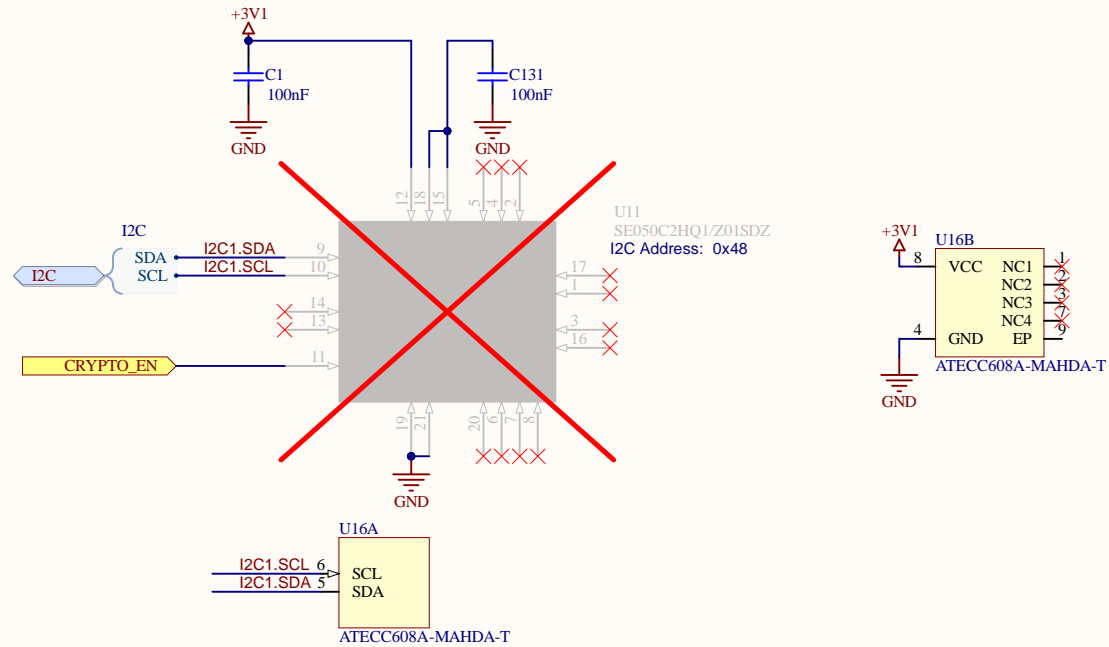






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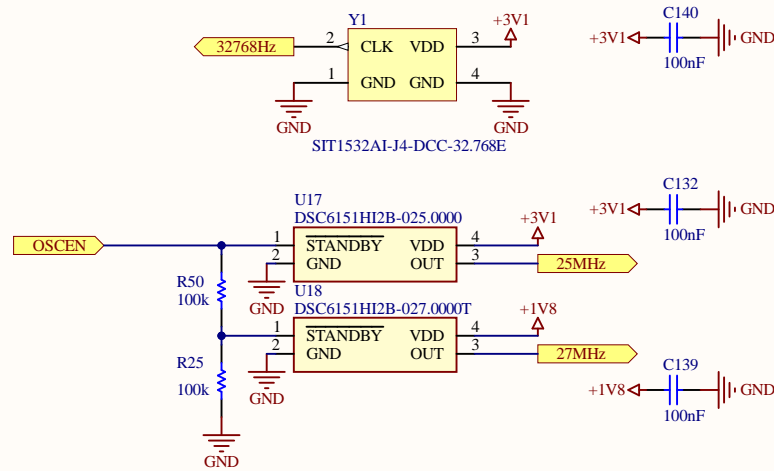
<b>Title: PortentaH7</b>				
<b>ID: SL-ABX00045</b>		Revision: 4.0		
Date: 9/6/2021	Time: 5:35:57 PM	Sheet 4 of 10		
File: LBEE5KLDX.SchDoc		Author: Arturo Guadalupi		RevAuthor: Dario Pennisi







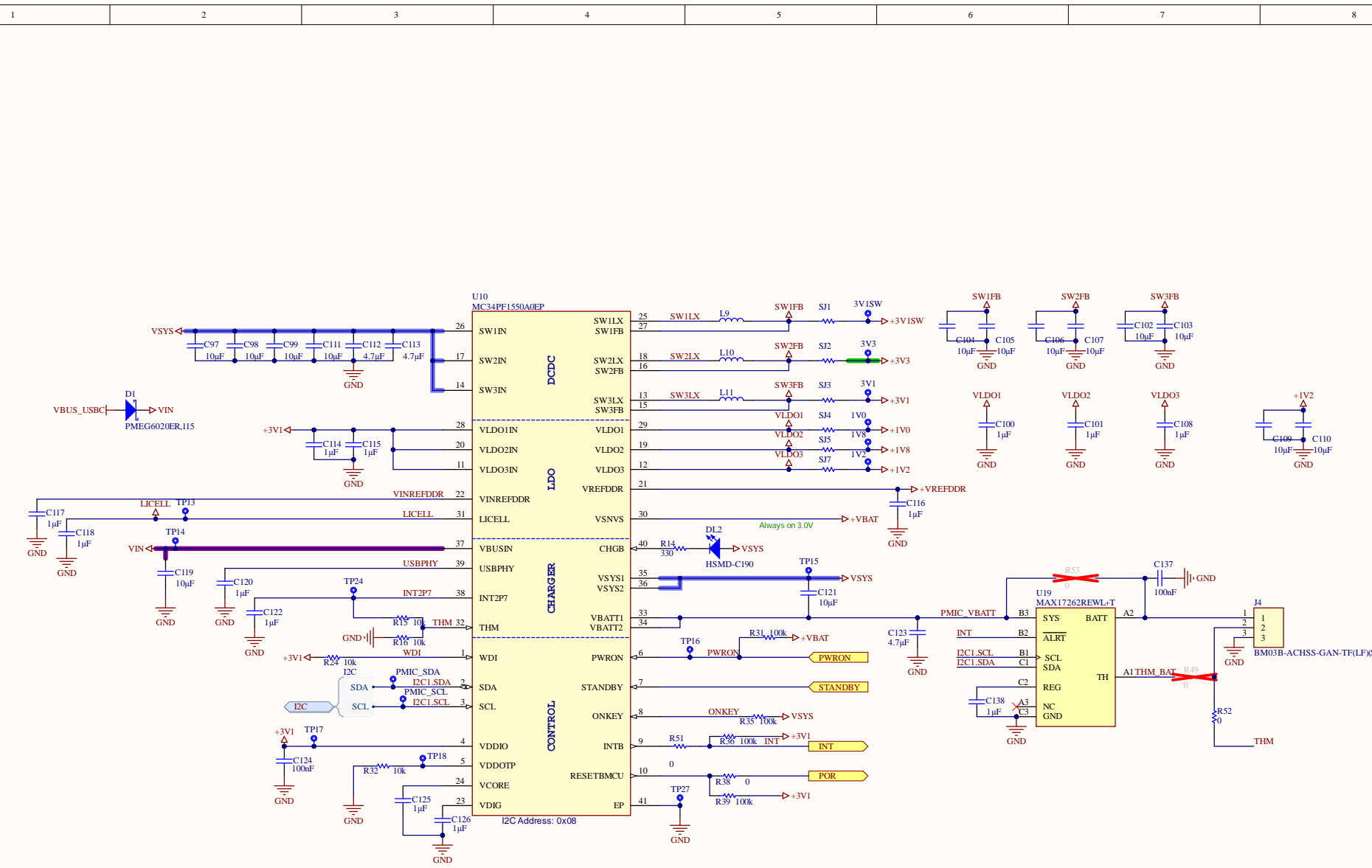
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<b>Title: PortentaH7</b>		 	
<b>ID: SL-ABX00045</b>			
Date: 9/6/2021	Time: 5:35:58 PM	Sheet 5 of 10	
File: Cryptochip_SchDoc		Author: ArturoGuadalupi	RevAuthor: Dario Pennisi



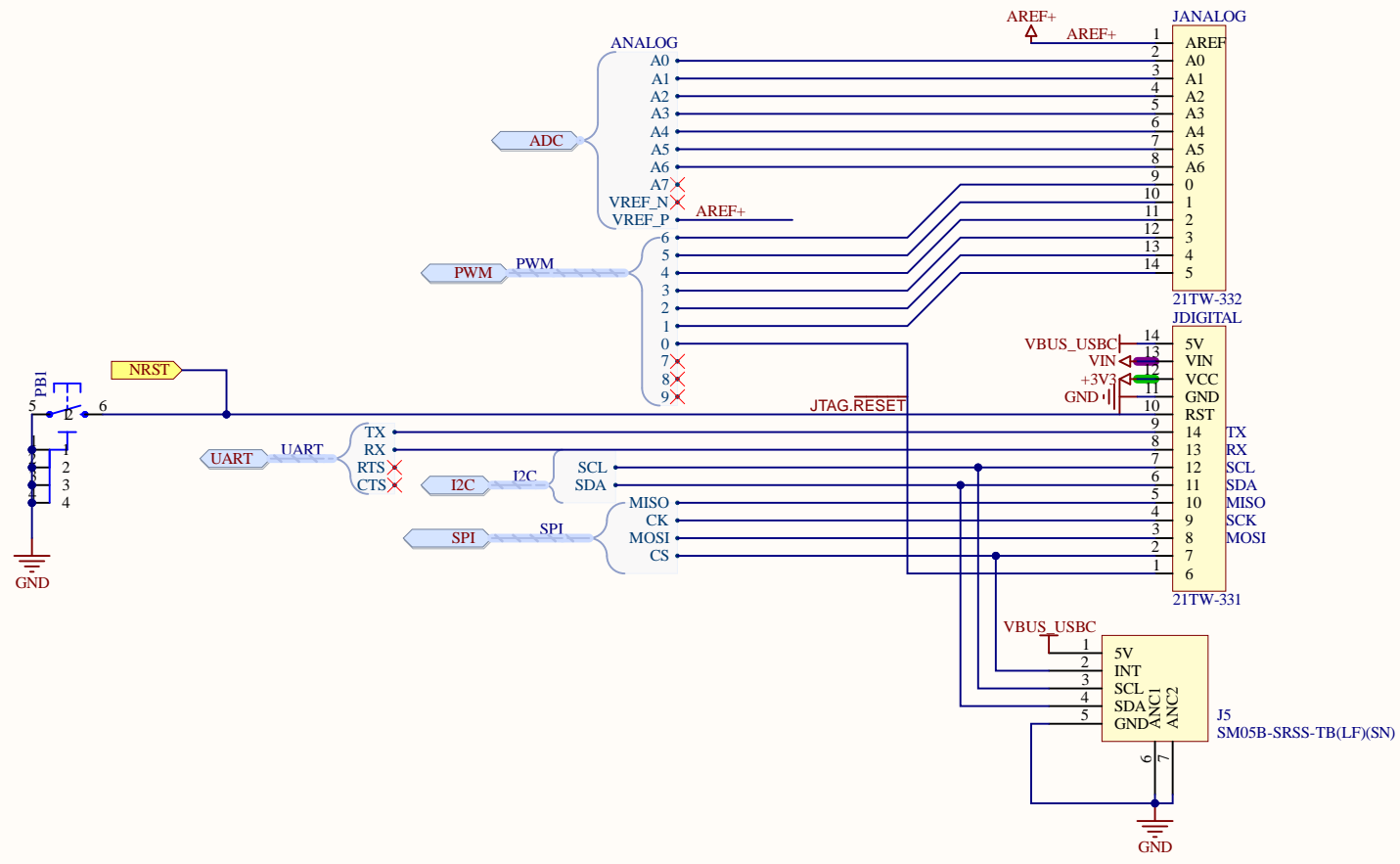
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<b>Title: PortentaH7</b>		 	
ID: SL-ABX00045			
Date: 9/6/2021	Time: 5:35:59 PM	Sheet 6 of 10	
File: Oscillators.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi





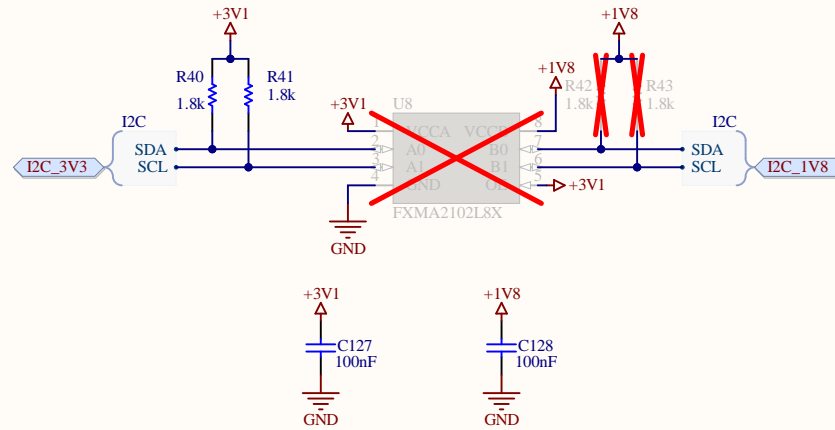
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Title: <b>PortentaH7</b>		Revision: 4.0			
ID: <b>SL-ABX00045</b>	Date: 9/6/2021	Time: 5:36:00 PM	Sheet 7 of 10		
File: PowerSchDoc	Author: Arturo Guadalupi		RevAuthor: Dario Pennisi		





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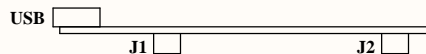
<b>Title: PortentaH7</b>		 	
ID: SL-ABX00045			
Date: 9/6/2021	Time: 5:36:01 PM	Sheet 8 of 10	
File: MKR.SchDoc	Author: Arturo Guadalupi	RevAuthor: Dario Pennisi	



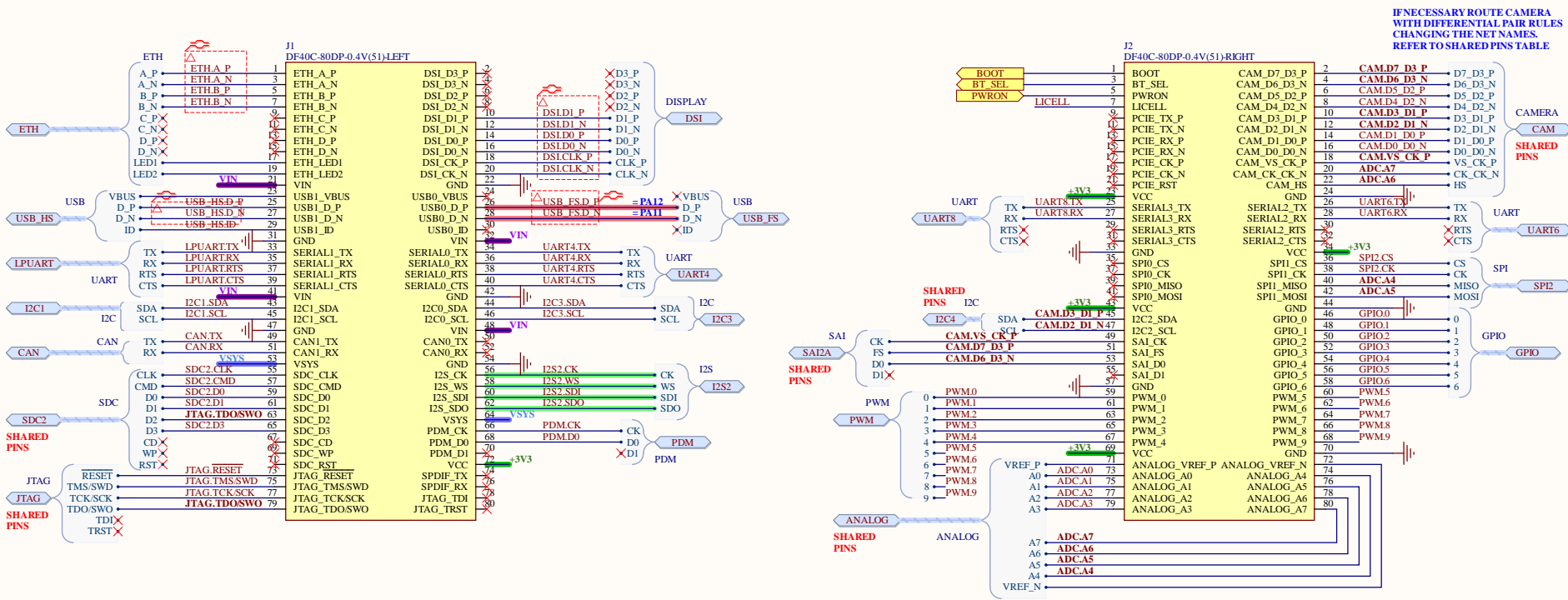
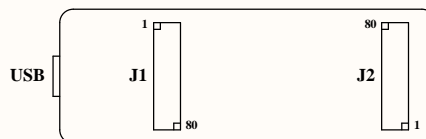
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<b>Title: PortentaH7</b>		 	
<b>ID: SL-ABX00045</b>			
Date: 9/6/2021	Time: 5:36:02 PM	Sheet 9 of 10	
File: I2CLevelShifter.SchDoc		Author: Arturo Guadalupi	RevAuthor: Dario Pennisi

Board side view:



Board BOTTOM view:



IF NECESSARY ROUTE CAMERA WITH DIFFERENTIAL PAIR RULES CHANGING THE NET NAMES. REFER TO SHARED PINS TABLE

SHARED PINS TABLE

NET	BUS 1	BUS 2
JTAG.TDOSWO	JTAG	SDC2
CAM.D2_D1_N	CAM	I2C4
CAM.D3_D1_P	CAM	I2C4
CAM.VS_CK_P	CAM	SAI2A
CAM.D6_D3_N	CAM	SAI2A
CAM.D7_D3_P	CAM	SAI2A
ADC.A6	CAM	ANALOG
ADC.A7	CAM	ANALOG
ADC.A4	CAM	ANALOG
ADC.A5	CAM	ANALOG

POWER NETS TABLE

NET	TYPE	RANGES	DESCRIPTION
VIN	PORTENTA INPUT	4.1V to 6V.	Default 3.3V, PMIC (U10) programmable output.
+3V3	PORTENTA OUTPUT	1.1V to 3.3V in steps, max 1A.	Default 3.3V, PMIC (U10) programmable output.
VSYS	PORTENTA RESERVED OUTPUT	RESERVED, DO NOT USE 3.5V to 4.2V, max 600mA.	Default 4.2V, PMIC (U10) programmable output which is also the input voltage of the bucks inside the PMIC itself.
LICELL	PORTENTA INPUT	Coinc cell max 3.6V, max 46uA.	Max 4uA with PMIC (U10) in coin cell mode, max 46uA with PMIC in standby/suspend mode.

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Title: <b>HD Connectors</b>		Revision: 4.0	
ID: SL-ABX00045		Sheet 10 of 10	
Date: 9/6/2021	Time: 5:36:03 PM	Author: Arturo Guadalupi	
File: HDConn_SchDoc		RevAuthor: Dario Pennisi	

