A PENNWELL PUBLICATION

# COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

JULY 1981

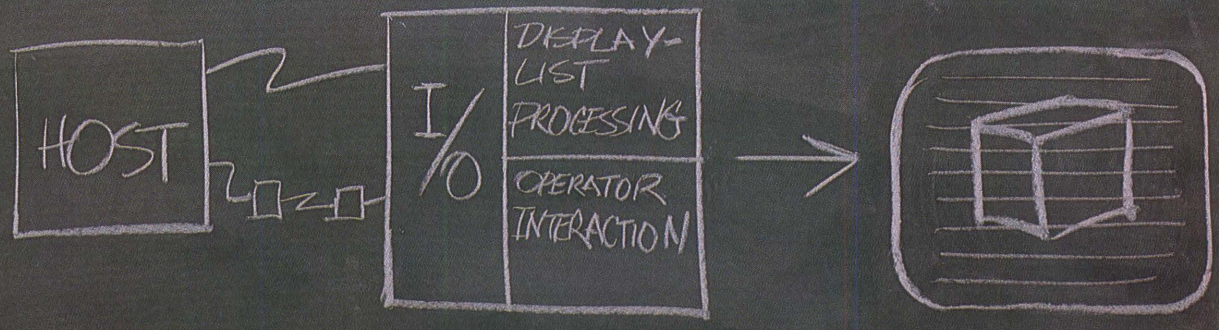
**LOW COST ALTERNATIVE TO HAMMING CODES CORRECTS MEMORY ERRORS**

**VIRTUAL MEMORY EXTENSION FOR AN EXISTING MINICOMPUTER**

**SPECIAL REPORT ON COMPUTER GRAPHICS**

# THE MEGATEK DIFFERENCE:

# REMOTE WORKSTATIONS




Whizzard 6200 raster-scan, line-drawing terminals are working remote workstations – fast, interactive, intelligent.

The Megatek difference starts with host-computer software. Wand 6200 is a computer-independent, Core-compatible Fortran package which organizes graphic information for maximum communication-line efficiency. Image segments can be dynamically extended, changed to a different color or line type, scaled, translated, or blinked with just a few simple commands.

Whizzard 6200 terminals can also be programmed with hundreds of graphic subroutines (e.g., the image of a bolt head). Instead of reconstructing such "instances" each time they are needed, the host computer simply transmits a subroutine ID number.

Swiftly interacting with the host computer at the "action" end of the communication line is an intelligent Whizzard 6200 memory-management I/O interface which maps subroutines, segments, and attribute information into a 64K-byte display-list memory (expandable to 128K bytes).

The final step, from memory to screen, is nearly instantaneous. Powered by a 32-bit proprietary processor, the Whizzard 6200 "graphics engine" processes display-list data into raster images at an average rate of 200 nanoseconds per pixel. Text can be displayed in eight hardware-generated character sizes. Twelve-bit vector coordinates (4096 x 4096 virtual display space) can be scaled up to 8X with full retention of fine-line detail. Images can be "Rasterized" into full-resolution hardcopy.

Monochrome or color, 512 x 512 or 1024 x 1024, every member of the Whizzard 6200 family is a complete graphics workstation, including desk, display monitor, keyboard, joystick, and optional data tablet. And all are upwardly mobile – up to the Whizzard 7200 series of 3D rotation-and-scaling raster/vector terminals.

**The more you know about graphics, the more you lean toward Megatek.**

There is a Megatek difference. See it, believe it. Call or write: Megatek Corporation, 3931 Sorrento Valley Blvd., San Diego, CA 92121. 714/455-5590. TWX 910-337-1270.

MEGATEK

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**See Us at Siggraph Booth #607**

**CIRCLE 1 ON INQUIRY CARD**

# When you ask some people about backup — they back off.

And for good reason. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8" 40 MByte disk drive (Model 7300) and an 80 MByte 14" Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼" cartridge recorder (Model 6450), and Model 6809, ½" Data Streamer Tape Transport.

Kennedy was the first to utilize the ¼" 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

We won't back off.

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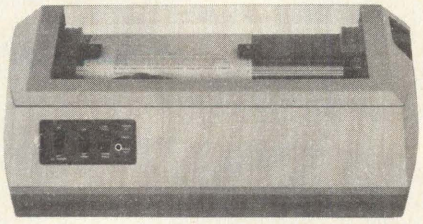
CIRCLE 2 ON INQUIRY CARD

# Four new printer ideas from the matrix printer leader

## ONE

**New 40 x 18 matrix Dual purpose printer:** The new T-1805 serial printer uses a unique 40 x 18 matrix dot pattern for high quality correspondence printing; or, flip a switch, it uses a 7 x 9 matrix for high speed data processing printing. In the high speed mode it turns out reports at time-saving throughput rates up to 200 lines per minute. In the reduced speed correspondence mode, its pivoting print head lays down an overlapping dot array to create high quality characters that look like they came from an office typewriter.



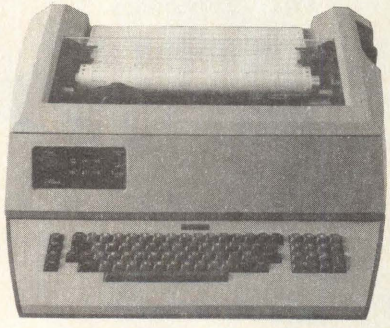
## TWO

**Line printer offers business graphics and more:** The T-3000 line printer is more application extensive than ever. This 300 line per minute multi-font machine now prints business graphics, subscripts, superscripts and customer defined special characters. This in addition to double high character printing. And to further its flexibility, characters can be loaded downstream from a host computer on command. Any number of character sets can be changed or interchanged on the fly. No printer stoppage. No wasted time.

For remote applications, the T-3000 even offers a communications adapter for long distance link-up with the host computer.

## THREE

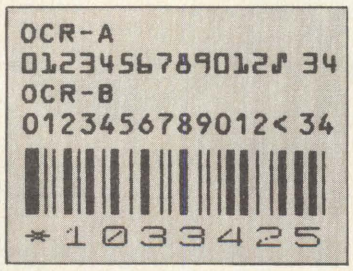
**New enhancement! DEC LA-120 compatible:** The versatile T-1612 teleprinter can now conform to the same function codes as the DEC LA-120. That means it's a simple swap to upgrade to the feature packed, lower priced T-1612. Remember, the T-1612 teleprinter offers the same functional features as the LA-120, plus extras like nine-needle print capability for true descenders and underlining, two-color red and black printing and forms handling bonuses like the Auto Front Feed for pre-cut forms and the Quick Tear for fast and easy forms removal.



## FOUR

**Low cost bar code, OCR printing:** Here's the economy answer to high quality bar code printing. And OCR-A and OCR-B printing. And data processing printing good enough for correspondence printing. And as a bonus, highly efficient and cost effective forms handling. Its the M-Series of serial matrix printers. With models in 80, 132 or 184 column widths.

Print two forms simultaneously! Some models can be equipped with dual tractor sets to handle two different forms sets in tandem. For example, print bar code labels and a summary sheet in one operation.

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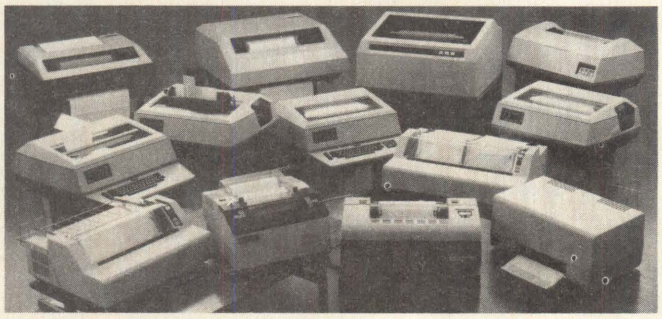

CIRCLE 3 ON INQUIRY CARD

# COMPUTER DESIGN®

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

JULY 1981

VOLUME 20, NUMBER 7


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Cover Artist: Darcy Gerbarg; cover was prepared on the Ampex Video Art (AVA) system, introduced by Ampex Corp, Redwood City, Calif in 1980 at the National Association of Broadcasters Convention. It was first utilized by the CBS network in New York City, Nov 1980, to create graphics for the presidential election-night coverage.


**Editorial Review Board**
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Gary W. Palmer
Joseph E. Bryden


## SPECIAL REPORT ON COMPUTER GRAPHICS


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Focusing on increased emphasis on higher resolutions, "souped up" arithmetic and data handling, and larger, lower cost memories, this year's "Special Report on Computer Graphics" presents a collection of five feature articles that points the way as computer graphics comes of age


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LOW COST ALTERNATIVE TO HAMMING CODES CORRECTS MEMORY ERRORS 143

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When memory accounts for a large part of product cost, or when throughput is critical, horizontal and vertical parity scheme detects and corrects errors at less expense than do Hamming codes

VIRTUAL MEMORY EXTENSION FOR AN EXISTING MINICOMPUTER 151

**by Peter D. Vogt**

Extensions to minicomputer architecture capitalize on low cost, high speed memory, and memory support chips



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ABP



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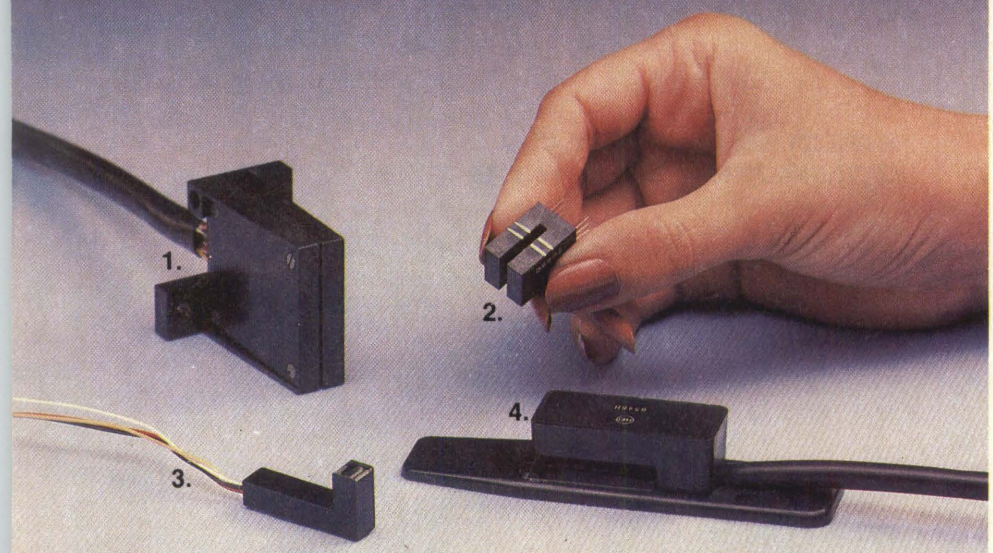


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HEI supplies a wide range of optoelectric devices as well as hand-fed card readers and a family of light pens. HEI has optoelectronic solutions for your design needs.

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**CIRCLE 4 ON INQUIRY CARD**



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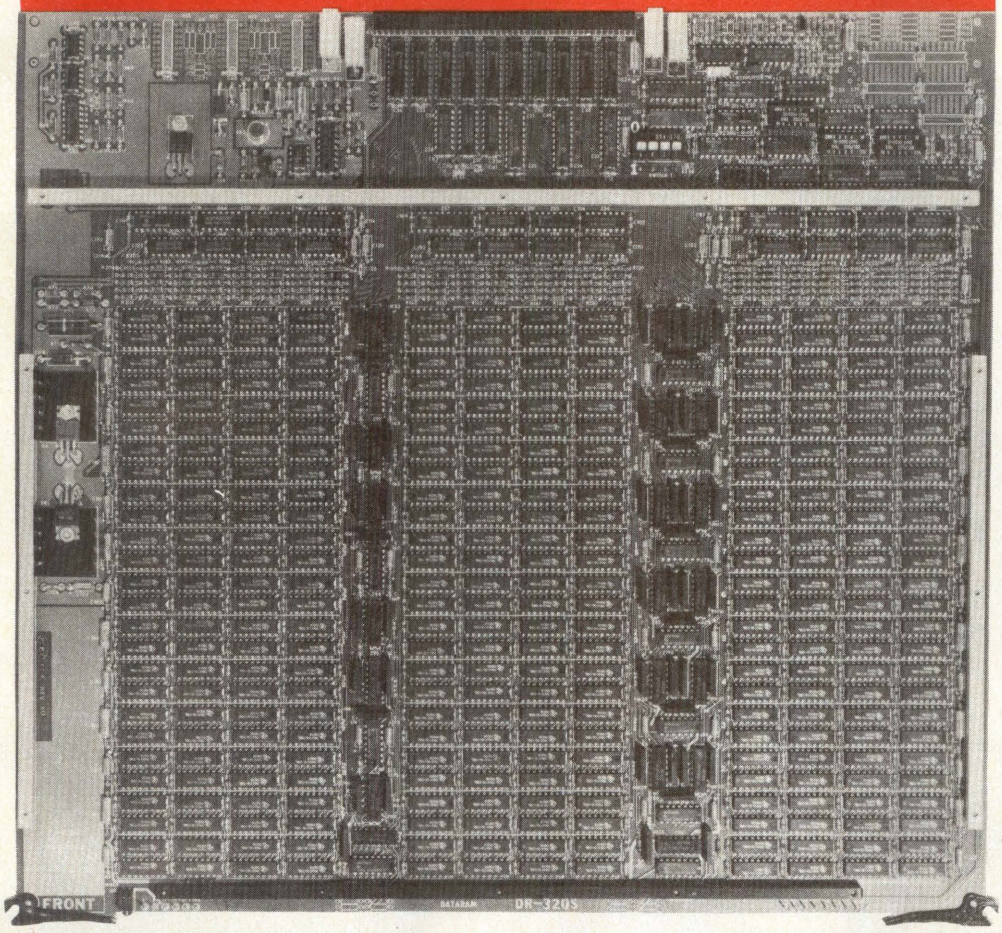
*(TM)

# 512KB ADD-IN FOR PERKIN-ELMER 3200




- **Memory capacity up to twice the comparable P-E storage module**
- **Substantial price savings**
- **Compatible with Perkin-Elmer 3220 and 3240**
- **256KB and 512KB configurations**
- **LED indicators to aid troubleshooting**
- **Test points available**
- **Switch-selectable address selection**
- **Address up to 4.0MB**

Dataram Corporation introduces another first for users of Perkin-Elmer minicomputers — the 512KB DR-320S semiconductor ADD-IN, the first 3200 Series-compatible semiconductor ADD-IN to be offered by an independent memory manufacturer.

The DR-320S continues the Dataram tradition of providing Perkin-Elmer compatible products at the industry's lowest cost/bit. Products that are not only compatible, but which offer additional features.

For example, the 512KB DR-320S, which occupies only one slot, offers twice the memory capacity of the comparable 256KB Storage Module (Model 35-694) available from Perkin-Elmer. The DR-320S operates in conjunction with the Perkin-Elmer Memory Interface Board contained in the host 3200 Series minicomputer.

The DR-320S is internally configured as a 128K x 39 bit (32 data + 7 ECC) memory to provide the 512KB capacity. A 256KB version of the DR-320S is also available. The DR-320S employs 16K RAMs having a 150 nsec access time to meet the speed requirements of the 3200 Series minicomputer. Tri-state receivers and drivers are used to transfer data between the DR-320S and the memory interface board.

In addition to 3200 series memory products, Dataram also offers core memory modules for older Perkin-Elmer/Interdata machines as well as BULK MEMORY Disk Emulation Systems for the full family of Perkin-Elmer minicomputers.

I'd like to learn more about Perkin-Elmer compatible memory:

☐ 3200 Series ☐ Disk Emulation ☐ Other

☐ Please send information.

☐ Please have a salesman contact me.

Name _____

Title _____ Phone _____

Company _____

Address _____

City _____

State _____ Zip _____

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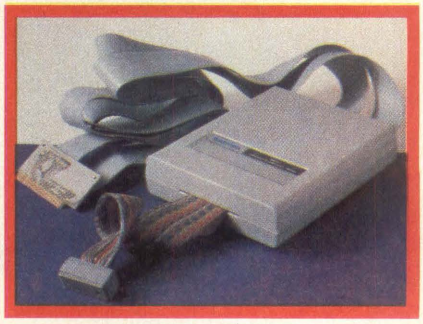
**CIRCLE 5 ON INQUIRY CARD**

# 16 bits of information

**1. Self-contained and upward compatible.** The 8550 Microcomputer Development Lab is the single-user member of the new 8500 Modular MDL Series, which also includes the 8560 multi-user system and the 8540 Advanced Integration Unit for the host computer environment. The 8550 is a complete microcomputer design tool, covering both software development and integration into the prototype. The 8550 can also be used as a station on Tek's forthcoming 8560 multi-user system.

**2. Real-Time Emulation.** Takes the concept of emulation to a new performance level. Advanced circuitry eliminates the need for wait states during program execution and debugging. The emulator processor now functions in real-time, with its operation totally transparent to the user.



**3. Multi-Vendor Chip Support.** The 8550 MDL supports 26 chips in all. The broadest support available anywhere, covering a wide range of vendors. With microcomputers as well as microprocessors. The ultimate in design flexibility.

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# on the new 8550 MDL.

**4. 16-bit Support.** You'll be able to choose from an entire new generation of 16-bit processors. Tektronix has the high performance tools to make it possible. Assembler support is available now for the 16-bit chips listed below. The TMS 9900 and SBP 9900 are fully supported with emulation today. Real-Time Emulation and Pascal support will be available in stages for the 68000, Z8000 and 8086 beginning the third quarter of 1981.

| | |
|---|---|
| **68000** | **TMS 9900** |
| **Z8000** | **SBP 9900** |
| **8086** | |

**5. 16-bit Trigger Trace Analysis.** Gives you highly sophisticated triggering ability for selective snapshots of full-speed code execution on the prototype bus. Up to four data acquisition triggers can be combined in a wide variety of ways. Bus cycle resolution to 8 MHz.

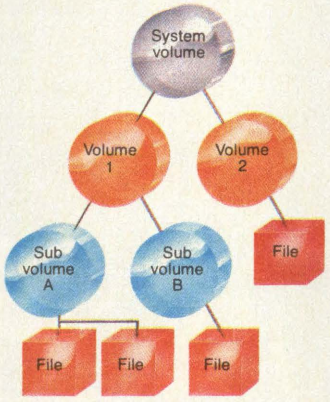
**6. 8-bit Support.** Besides the most up-to-date microprocessor coverage, you can also take advantage of extensive 8-bit microcomputer support. All 8-bit chip support includes real-time emulation.

| | | |
|---|---|---|
| **6800** | **8048** | **3870** |
| **6802** | **8039** | **3872** |
| **6808** | **8039-6** | **3874** |
| **Z80A** | **8035** | **3876** |
| **8080A** | **8021** | **F8** |
| **8085A** | **8022** | **1802** |
| **8049** | **8041A** | **6500/1** |

**7. 8-bit Real-Time Analysis.** An optional Real-Time Prototype Analyzer lets you extract both bus and hardware logic at full operating speeds. You capture 48-bit words for storage in a 128-word memory. Two triggers for precise data acquisition.

**8. Split-Bus Architecture.** The 8550 uses one processor and bus for system operation, and another for real-time emulation. This architecture assures that the emulator processor is denied access to system memory, preventing the possibility of a system crash during prototype program execution.

**9. Tree-Like File Structure.** Combines ease of use, rapid access and in-depth organization. Allows files to be arranged in a predetermined hierarchy that best supports your current situation. A flexible tool that supports filing situations from very simple to extremely complex.




**10. Advanced CRT-Oriented Editor.** Gives you the quickest path possible to perform many editing operations. Lets you use screen-oriented editing as well as line-oriented editing. Up and down scrolling capabilities give you a total window on all of your code.

**11. Macro Assembly.** The most powerful assembler software available today in a development system. Lets you employ user-defined constructs and library resources. A conditional assembly feature allows sophisticated user manipulation of code at assembly time.

**12. Pascal Compiler.** Available in true compiler form, producing executable object code. Pascal's structured format allows a modular approach to programming. With extensions designed specifically for microcomputer development, Tektronix Pascal is ideal for the "top-down" method of product development.

**13. MDL/$\mu$ Compiler.** Tektronix' advanced form of Basic, with many extensions for microcomputer development. Often the quickest route from concept to fully developed code.

**14. Transportable Emulators and Software.** If you need to expand to a multi-user design environment, your 8550 can be incorporated as a workstation in an 8560 multi-user system. Source code and emulator modules can be readily transferred to the Tektronix 8560 system. If you move to a host environment, your 8550 emulator modules are totally compatible with the new Tektronix 8540 Advanced Integration Unit.

**15. Worldwide Service.** For service support, 36 centers around the globe. You get fast on-site service no matter where you are — without waiting weeks for parts or repairs.

**16. Full Tektronix Support.** Training, documentation, applications engineering. Nobody does it like Tektronix. An entire series of classes on microcomputer design, from high-level language to hardware/software integration. Applications engineers are available worldwide to assist you.

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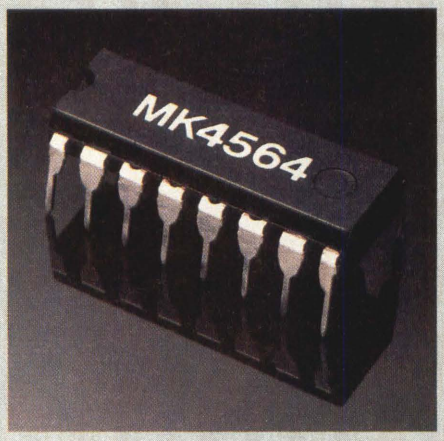
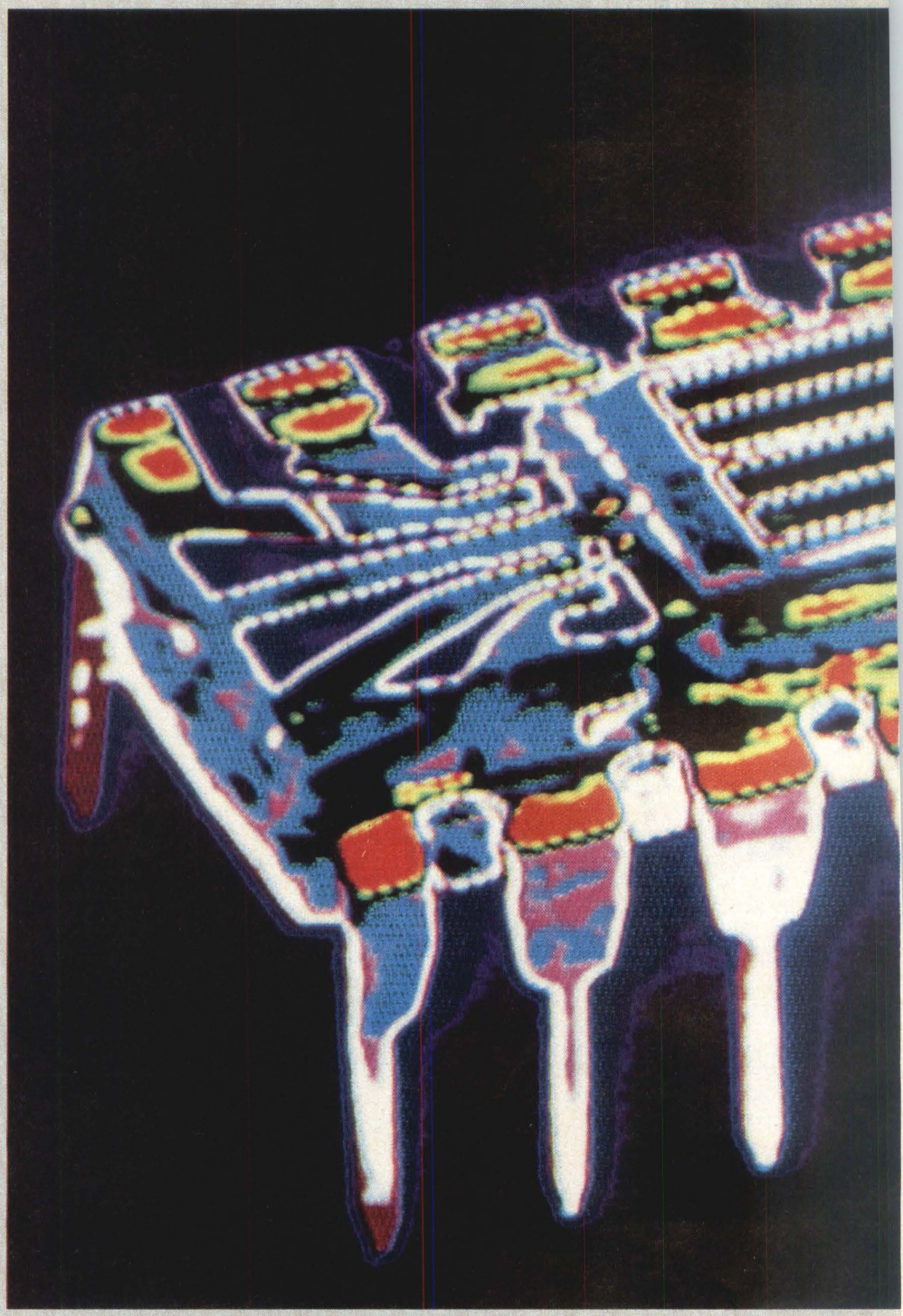



Fact: The Mostek 64K RAM is here. Utilizing our Scaled POLY 5 process technology, this new generation VLSI memory represents the cumulative expertise of the same people who already have three impressive industry standard memories to their credit. Standards that include the MK4096 4K RAM, as well as its second generation counterpart, the MK4027. And more recently, the MK4116 16K dynamic RAM.

Fact: The MK4564 is not, however, a simple scaling of the MK4116. On the contrary, it's an entirely new approach to MOS memory design. One that demanded fresh, innovative ideas to maximize signal strength, yet minimize differential noise, sense amplifier offset and substrate voltage excursions, to name just a few. How we mastered these challenges with new circuitry, new layout techniques and new process technology is why our 64K RAM is so highly



*Science showing science: New advances in photographic densitometry*

# Introducing the Mostek 64K RAM. An innovative yet realistic approach significantly enhances manufacturability.

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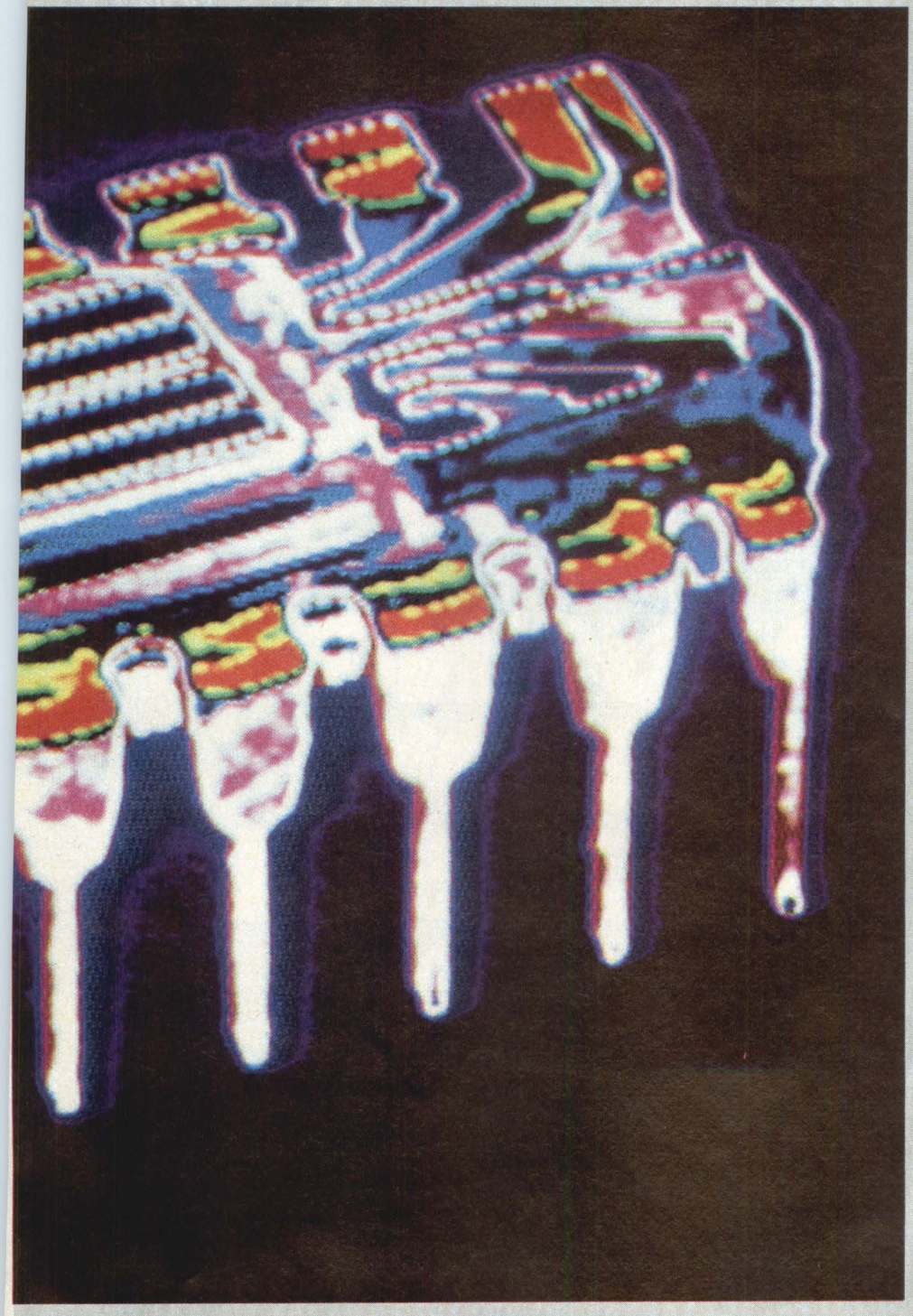

*provide inside view of the Mostek 64K RAM.*

manufacturable. And why it provides such wide operating margins both internally and to the system user.

Fact: The MK4564 has all the performance characteristics you would expect from the industry's memory leader. Organized 65,536 words this single supply, 5-volt NMOS memory features fast access time and low power dissipation; just 300mW active and 22mW standby. Refresh characteristics have been chosen to maintain compatibility with other Mostek dynamic RAMs. To simplify user interface, a pin 1 on-chip refresh version, designated MK4164, is also available. Pinout for both, of course, is JEDEC-approved.

Fact: There are some very detailed reasons why the MK4564 is so highly manufacturable. Why it's so reliable. And why we fully expect it to become the standard by which other 64K RAMs will be measured. To find out what those reasons are, send for the 64K RAM brochure that explains them. In terms of science, not science fiction. Write Mostek, 1215 West Crosby Road, Carrollton, Texas 75006. Or call (214) 323-6000. In Europe, contact Mostek Brussels 762.18.80.

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CIRCLE 8 ON INQUIRY CARD

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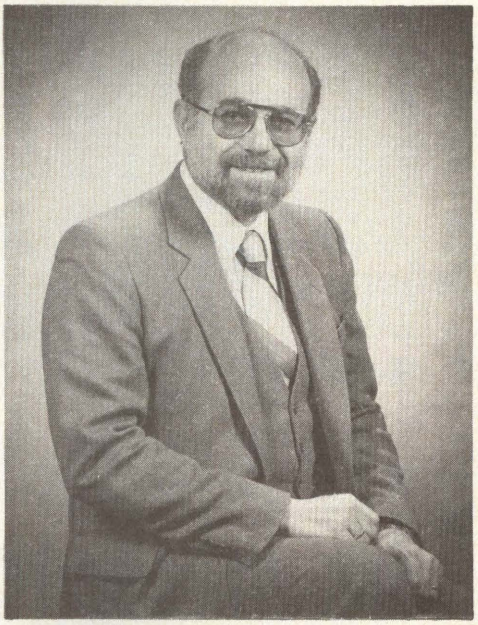
CIRCLE 9 ON INQUIRY CARD

# EDITORIAL



*Last month we mailed an editorial survey to a selected sample of subscribers in order to obtain a baseline for selecting future editorial material. If you received one of these surveys in the mail, I urge you to help us and your fellow engineers by taking some of your valuable time to complete and return the survey as soon as possible.*

*The next step in* Computer Design*'s development program is to broaden our contributor and reviewer base. The editorial content of any publication that purports to be a technical book should reflect the next generation and state-of-the-art thinking that is taking place right now in our industry. A publication such as ours ultimately must decide whether it will merely report events as they are heard or provide significant technical information in the form of in-depth articles.* Computer Design *has always opted for the latter. As it is impossible for any publication to maintain a staff of writers whose technical competence is on a par with those of you who are on the front lines of applied digital systems technology, we intend to expand our ranks of editorial contributors in order to continue providing you with in-depth current material.*

*Needless to say, having an article published in a technical periodical such as* Computer Design *is a personal achievement that goes well on your resume, contributes to your professional growth, and helps promote your company as a stimulating and up-to-date place to work. If you are interested in finding out how to become one of our contributors, please circle 754 in the "Editorial Score Card" box of our Inquiry Card, and we will send you a copy of our* Author's Guide.

Saul B. Dinman
Editor

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CIRCLE 11 ON INQUIRY CARD

# CALENDAR

## CONFERENCES

**AUG 3-5—Pattern Recognition and Image Processing,** Sheraton Hotel, Dallas, Tex. INFORMATION: PRIP, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

**AUG 3-7—ACM (Assoc for Computing Machinery) Siggraph '81,** Dallas, Tex. INFORMATION: Dr Anthony Lucido, Intercomp, 1201 Dairy Ashford, Houston, TX 77079. Tel: 713/497-8400

**AUG 5-7—SYMSAC '81 (Assoc for Computing Machinery),** Snowbird Ski Resort, Salt Lake City, Ut. INFORMATION: Prof B. F. Caviness, Dept of Mathematical Sciences, Rensselaer Polytechnic Inst, Troy, NY 12181. Tel: 518/270-6731

**AUG 11-14—Electronics '81,** Mexico City, Mexico. INFORMATION: Franc D. Manzolillo, Proj Mgr, Rm 6015, U.S. Department of Commerce, Washington, DC 20230. Tel: 202/377-2991

**AUG 12-15—NYCE (New York Computer Expo),** Sheraton Centre, New York, NY. INFORMATION: NYCE, 110 Charlotte Pl, Englewood Cliffs, NJ 07632. Tel: 201/569-8542

**AUG 18-21—VLSI (Very Large Scale Integration) '81 Internat'l Conf,** University of Edinburgh, Edinburgh, Scotland. INFORMATION: Secretariat, VLSI '81 Internat'l Conf, 26 Albany St, Edinburgh EH1 3QH, Scotland

**AUG 24-28—IFAC (Internat'l Federation for Automatic Control) World Congress,** Kyoto, Japan. INFORMATION: IFAC '81 Secretariat, Kinki Hatsumei Ctr, 14 Kawahara-cho, Yoshida, Sakyo-ku, Kyoto 606, Japan

**AUG 24-28—Internat'l Joint Conf on Artificial Intelligence,** Vancouver, British Columbia, Canada. INFORMATION: Richard Rosenberg, Computer Science Dept, U of British Columbia, Vancouver, BC V6T 1W5, Canada. Tel: 604/228-3061

**AUG 25-28—1981 Internat'l Conf on Parallel Processing,** Shanty Creek Lodge, Bellaire, Mich. INFORMATION: Dr M. T. Liu, Dept of Computer and Information Science, Ohio State U, Columbus, OH 43210. Tel: 614/422-1837

**AUG 26-29—Nat'l Small Computer Show,** New York Coliseum, New York, NY. INFORMATION: Nat'l Small Computer Show, 110 Charlotte Pl, Englewood Cliffs, NJ 07632. Tel: 201/569-8542

**SEPT 1-3—FOC '81 WEST (Internat'l Fiber Optics and Communications Expo),** Hyatt Regency Embarcadero, San Francisco, Calif. INFORMATION: Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

**SEPT 8-9—Internat'l Conf on Computer Hardware Description Languages and Their Applications,** Kaiserslautern University, Federal Republic of Germany. INFORMATION: Prof Melvin Breuer, Dept of Electrical Engineering, USC, Los Angeles, CA 90007. Tel: 213/743-2308

**SEPT 14-17—Software Info '81 (The Nat'l Software Package Conf and Expo),** Merchandise Mart Expocenter, Chicago, Ill. INFORMATION: Software Info, 1730 N Lynn St, Suite 400, Arlington, VA 22209. Tel: 703/521-6209

**SEPT 14-18—COMPCON FALL '81,** Capital Hilton Hotel, Washington, DC. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

**SEPT 14, OCT 1, OCT 27, AND OCT 29—Invitational Computer Conf:** Newton, Mass; Minneapolis, Minn; Valley Forge, Pa; AND Washington, DC, area. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

**SEPT 15-17—WESCON '81,** Brooks Hall and Civic Auditorium, San Francisco, Calif. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

**SEPT 21-23—Federal Computer Conf,** Sheraton Washington Hotel, Washington, DC. INFORMATION: Federal Education Programs, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181

**OCT 5-8—Electronics Test and Measurement Conf, Hyatt Regency,** Chicago, Ill. INFORMATION: Dona Atwood, Registrar, Electronics Test and Measurement Conf, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

**OCT 12-14—Conf on Local Computer Networks,** Hilton Inn, Minneapolis, Minn. INFORMATION: Dr Abe Franck, Gen'l Chm, UCC, U of Minnesota, 227 Experimental Engineering, 208 Union St SE, Minneapolis, MN 55455

**OCT 19-23—JEMIMA (Japan Electric Measuring Instruments Manufacturers' Assoc) Internat'l Exhibition,** Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: 19th JEMIMA Internat'l Exhibition, Secretariat of the Administration Committee, 1-9-10, Toranomon, Minato-ku, Tokyo 105, Japan. Tel: 03/502-0601, X4

**OCT 19-23—SYSTEMS '81 (Computer Systems and Their Application),** Munich, West Germany. INFORMATION: Kallman Associates, 30 Journal Sq, Jersey City, NJ 07306. Tel: 201/653-3304

**OCT 27-29—Data Communications Sym,** Mexico City, Mexico. INFORMATION: Dr Wushow Chou, Gen'l Chm, Seventh Data Communications Sym—1981, PO Box 5490, North Carolina State U, Raleigh, NC 27650

**OCT 27-29—Internat'l Test Conf, Franklin Plaza Hotel,** Philadelphia, Pa. INFORMATION: Louis J. Sobotka, Program Chm, 1981 Internat'l Test Conf, Bell Laboratories, PO Box 830, Allentown, PA 18105. Tel: 215/439-6198

**OCT 28-30—Sym on Foundations of Computer Science,** Nashville, Tenn. INFORMATION: Prof R. Book, Dept of Mathematics, U of California, Santa Barbara, CA 93106

**NOV 5, 12, AND 17—Invitational Computer Conferences,** Amsterdam, The Netherlands; Paris, France; AND Milan, Italy. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

**NOV 9-12—IECI '81 (Internat'l Conf and Exhibition on Industrial Control and Instrumentation),** Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: LeRoy Bushart, FMC, 328 Brokaw Rd, Santa Clara, CA 95052. Tel: 408/289-3871

## SEMINARS

**AUG 24-27—Software Design, Reliability, and Testing,** Sheraton Motor Inn, Lexington, Mass. INFORMATION: Prof Donald D. French, Inst for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: 617/964-1412

**SEPT 7-8—Microprocessor Workshop on Microprocessor Applications,** Liverpool University, Liverpool, England. INFORMATION: Dr M. J. Taylor, Microprocessor Workshop, Computer Laboratory, University of Liverpool, PO Box 147, Liverpool L69 3BX, England

## SHORT COURSES

**SEPT 2-4, 9-11, AND 21-25—Computer Communication Systems and Networks, The American and Russian Methods in Linear Programming and Applications, AND Structured Programming and Software Engineering,** George Washington U, Washington, DC. INFORMATION: Dir, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

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CIRCLE 12 ON INQUIRY CARD

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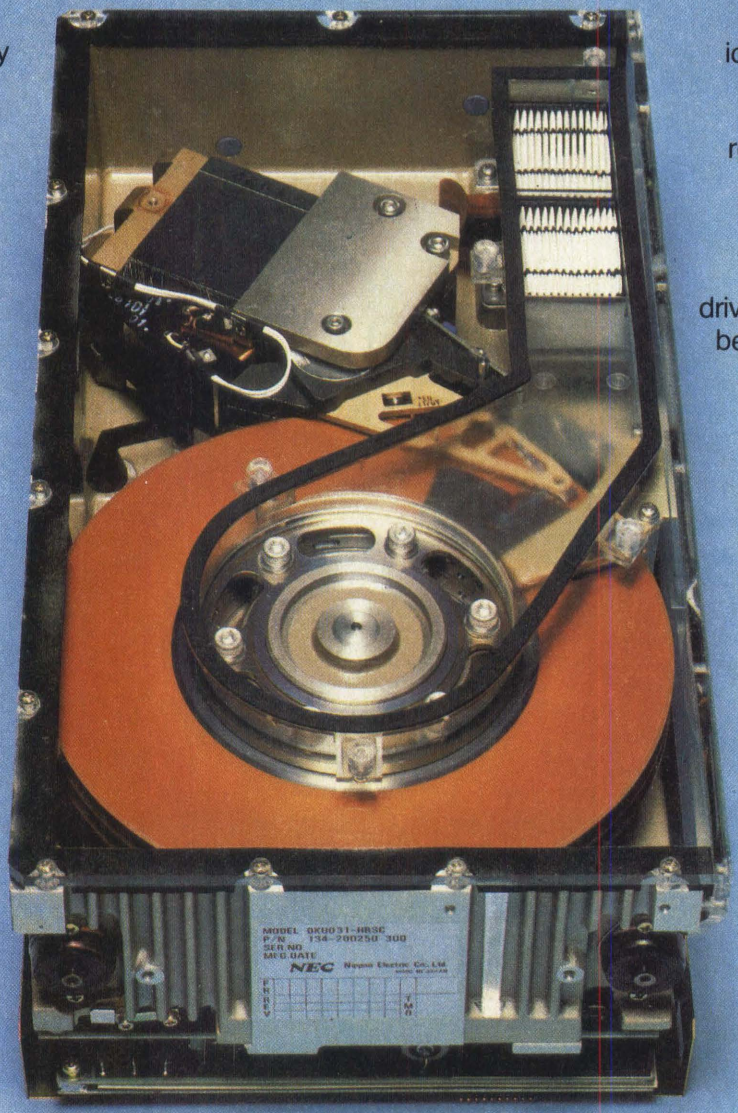


The D2200 family is ideally suited to medium and heavy volume interactive business applications that require frequent disk access, as in virtual memory, database access and data communications operations.

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CIRCLE 13 ON INQUIRY CARD

# Serial Interface Autodialer Protocol

**Al Wedgman**

**Universal Data Systems**
**500 Bradford Dr**
**Huntsville, AL 35805**

In a world of increasing technical complexity, data communications systems are becoming easier to understand and to implement. Much of this progress can be attributed to modern modems that are less expensive than earlier models and offer greatly simplified access to the public telephone network. With a minimum amount of homework a user can assemble a satisfactory data communications network even if he or she has relatively little knowledge of the circuits and components that make up the various network elements.

One of the more common manifestations of this new situation in data communication networks is their mix and match characteristic. Users feel quite secure in buying a CPU from one vendor, modems from another, and terminals from several different suppliers. The situation would be chaotic if it were not for the acceptance of some "standards." Organizations such as the EIA, CCITT, and even the federal government have helped to establish common practices in pinouts, cables and connectors, interface designs, and basic communications protocols.

However, the existing cluster of standards has somehow bypassed an aspect of data communications that is growing rapidly: there is no commonly accepted practice for organizing the data stream that provides call origination in a serial format to be used to control an automatic dialer. Serial input autodialer data adapt easily to a common format, and we have found no situations where this proposed "standard" protocol works a hardship on users.

## Basic Network Configurations

The simplest data communications network consists of the PSTN, at each end of which is a modem (DCE) and a terminal (DTE), as shown in Fig 1. To initiate a call, a person lifts the telephone off hook, dials the desired number, talks to the answering party at the other end and then, by common agreement, both parties switch their modems into the circuit. After the data have been exchanged, both parties switch back to voice mode, say farewell, and hang up their telephones.

The automatic answering modem is one step up from this elementary network. No human intervention is required at the answering end. The modem

## Terminology

Acronyms and abbreviations are used in the accompanying discussion to help shorten sentences that might otherwise be clumsy. The reader is asked to tolerate the following terms used in describing the proposed interface protocol:

| | |
|---|---|
| ACU | Automatic Calling Unit, sometimes called an autodialer. This product converts digital bit streams into signals that are the equivalent of manually dialing a telephone number. |
| DTE | Data Terminal Equipment. This can refer to a keyboard and CRT terminal or can imply a CPU if that is where the command information originates. In this discussion DTE means the device that originates and/or uses the data, as opposed to devices that merely switch or convert data. |
| DCE | Data Communications Equipment. Here the term means a modem. This is a side-by-side arrangement of a transmitter and receiver. The transmitter accepts digital inputs and converts them into tones that can travel over telephone lines. The receiver accepts tone inputs and converts them back into digital signals. Modems also have some network control functions. |
| PSTN | Public Switched Telephone Network, also known as DDD. This is the big system that includes the telephone on your desk, the telephone on somebody else's desk, and all the apparatus in between. To be perfectly accurate, PSTN does not include the PBX installed in an office, but for purposes of this discussion, that fine point is immaterial. |
| Bits/s | Bits Per Second. This refers to the actual transfer rate of the digital pulse stream and is not always the same as the baud rate. Note that commands between DTE and ACU need not run at the same speed as information between one DTE and another DTE at a remote location. |
| Strap | Straps are internal switches and jumpers provided by manufacturers of DTEs, ACUs, and DCEs. The term stems from an early practice of making changes by rerouting wires (straps) from one terminal block screw to another. Strap options allow one device to serve several kinds of applications by making proper connections or settings when the equipment is installed. |
| RS-232-C | An interface standard sanctioned by the Electronics Industries Association (EIA) that closely defines voltages and pinouts used to exchange signals for data communications purposes. It is used in serial data situations. RS-232-C describes the mechanical and electrical details of interconnection but does not define the makeup of the digital bit stream it accommodates. |

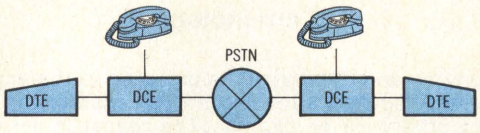


Fig 1 Simple data communications network. Manual switches on each modem (DCE) select between talk and data modes. To place call, modem is switched to talk and user dials desired number. Once other end answers both operators switch their modems to data mode and establish signal path for terminals (DTEs). When call is over both operators switch to talk again and hang up their telephones

itself senses the ring of the telephone, picks up the call, switches in the terminal, allows data to flow, and then electrically puts the phone back on the hook when the originating party terminates the call.

Adding an ACU to the network provides full automation. A call can be initiated by some preprogrammed event; the ACU reacts to a command from the DTE by taking the telephone off hook, waits for a dial tone, calls a number defined by the DTE program, and, when the other end answers, transfers communications to the DTE.

The ACU must be capable of at least three functions that have little to do with the dialing of a number. It must be able to wait for and recognize a dial tone, hang up the phone if the called number cannot be reached, and take itself out of the circuit once communication has been established. Many ACUs also provide automatic redial capability that, in effect, keeps trying to reach a number after a busy signal has been received.

In the type of network under discussion here, the ACU and DCE are functionally positioned in parallel [Fig 2(a)]. They both access the telephone line, and they both access the DTE. Both units usually contain hardware provisions to prevent a condition where they are both turned on at the same time. When the ACU is operating the DCE is totally transparent to the network, and when the DCE is operating the ACU is transparent.

### Established Practice

When data communications engineers first tackled automatic calling, they assumed that dialing commands would issue from the DTE in a parallel format. This is easy to accomplish with only four data lines and a binary coded decimal (BCD) format. Early computers had extra communications ports, one of which was reserved solely to command the ACU. An additional port had to be used to exchange the data once communication was established [Fig 2(b)]. The interface protocol adopted for parallel ACU operation was, and is, called RS-366. The important fact to remember about RS-366 is that it requires a dedicated port on the DTE that does nothing but control the ACU.

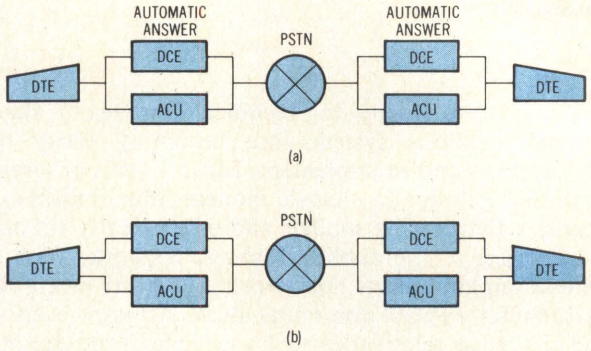


Fig 2 Automatic data communications network. Serial dialing (a) needs only one port from DTE, while parallel dialing (b) requires two. Both ends of circuit have automatic dialers and automatic answering modems. Either terminal can place call in response to program control, and modem at other end will pick up call and establish data communications. No telephone sets are shown because they are not needed. However, modems have modular sockets to connect telephones if required for voice communication whenever there is no data communication call

### A Newer Way

Smaller computers and many terminals now in use have only a single communications port that is configured for RS-232-C type communications. RS-232-C provides several communications channels for network control and housekeeping functions, but there is only a single 2-way path for exchanging the real traffic of a data communications network. Obviously, RS-232-C cannot support parallel input BCD dialing commands because it does not provide the necessary four data lines.

If one of today's smaller DTE devices is going to be used for both data transactions *and* ACU commands, a format must be developed that is capable of differentiating between command and all other information. Also, in today's environment of mixing components from several vendors, all serial input asynchronous ACUs must be able to recognize and execute the same protocol.

### Defining the ACU Command Bit Stream

The protocol must conform to standard ASCII because most small computers use ASCII and existing

*(continued on page 24)*

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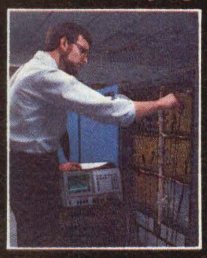

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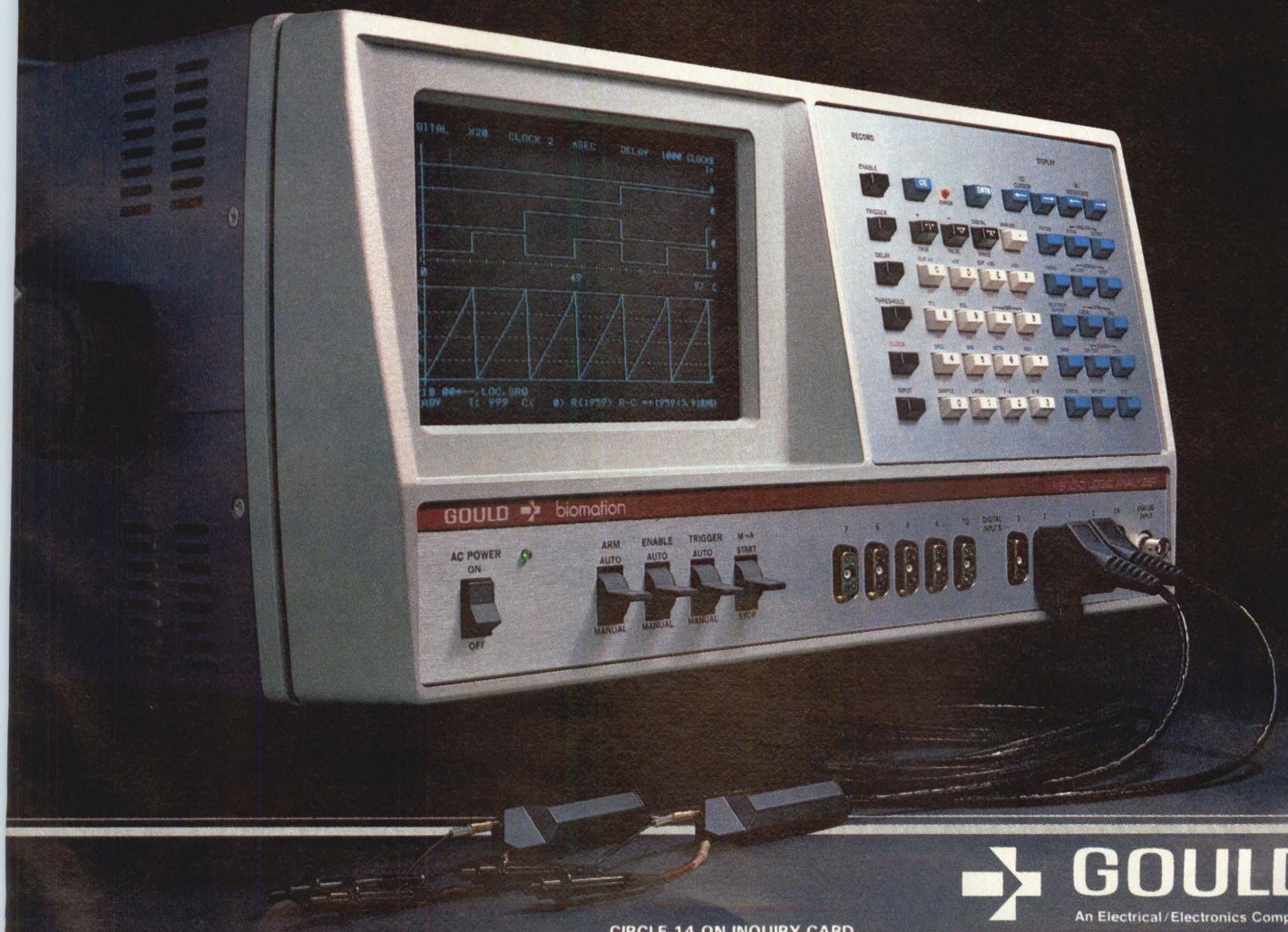


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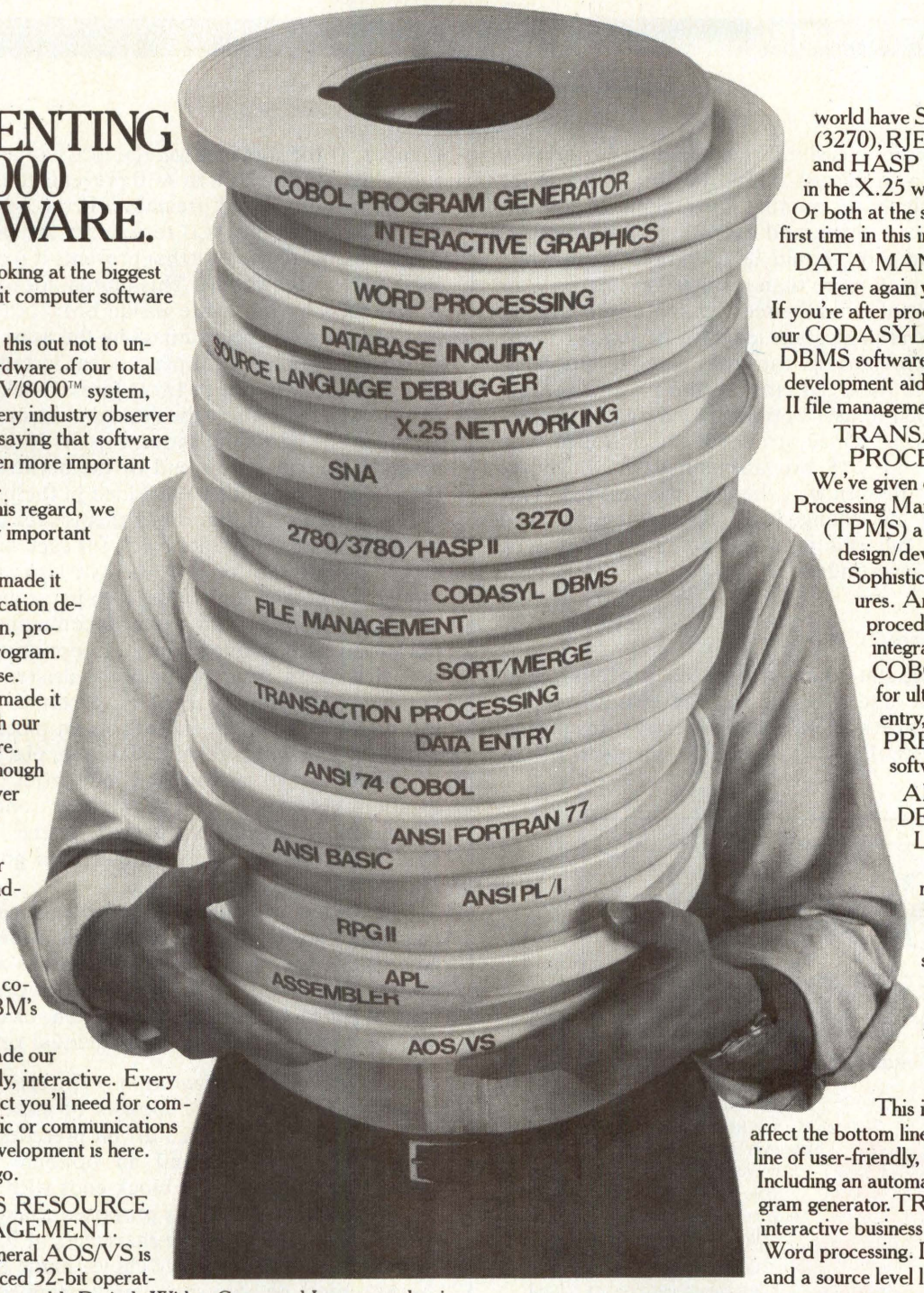


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**CIRCLE 16 ON INQUIRY CARD**

software handles it easily. From a human engineering point of view, a person should be able to assign or change a telephone number by making a conventional keyboard entry, and execution of all required control commands should be as simple as possible: preferably by no more than a single keystroke.

Serial data offer unlimited flexibility in character length and overall message length. The standard proposed here provides the user with enough options to accommodate most systems we have seen, and the ACU is adapted to user options by making the proper strap selections. Once strapped and installed, the ACU, DCE, and DTE are all limited to whichever character bit pattern that the user has selected. This pattern can be changed by reprogramming and restrapping, but this is not something that can be done in a few seconds.

### How the Protocol Works

In a no traffic state the ACU and DCE are idling, and the telephone line is on hook. The DTE causes the ACU to recognize a telephone number by transmitting a block of data that always precedes the digits of the number. If for some reason the DCE happens to be in use, a signal from DCE to ACU prevents the ACU from recognizing this fixed preamble. If the DCE is not in use, as soon as the ACU recognizes the preamble it sends a signal to the DCE that prevents it from becoming a part of the circuit. This mutual lockout feature is provided by hardware inside both DCE and ACU and need not be programmed by the user.

Where there are multiple modem installations the protocol contains one or two address blocks that first identify the rack where the desired modem is installed and then the particular modem itself. If there is only a single modem at this end of the network, the address blocks need not be included in the protocol.

Next, the actual dial digits themselves are sent to the ACU, using a separate block for each digit. In addition to digits 0 through 9, the ACU also recognizes a tandem command that causes it to pause and wait for another dial tone, and a pause command of fixed duration that is defined by a strap option. Unless the ACU detects an error, it loads the desired telephone number into internal registers. Upon receiving the last digit block and an end of format block, the ACU seizes the line, waits for the dial tone, places the call, and waits for an answerback tone from the remote location. As soon as the answerback tone is recognized, the ACU transfers control of the line to the modem, drops out of the circuit, and goes into an idling state.

In addition to being able to accept some control signals from the DTE, the ACU can send several status advisories back to the DTE. The user has a choice of placing every part of this sequence under program control for truly automatic operation, or of controlling the process sequentially by manual keystrokes.

*Character Block Configuration*—The central portion of each character block consists of either seven or eight information bits. A start bit precedes the information bit sequence, and an optional parity bit follows it. The character block ends with either one or two stop bits. With this proposed character block format, the users will have characters of 9, 10, 11, or 12 bits in length. For every choice made by the user the ACU must be correspondingly strapped so that it will recognize the meaning of each bit it detects.

*Overall Control*—The system can operate under STX control (explained below) or under RTS control, which means that the presence or absence of a request to send (RTS) signal will enable/disable the dialer. This consideration is more important in the way the DTE commands an abort than for any other part of the process, and is further discussed under the paragraph dealing with the abort command.

*Control Characters from the DTE*—There are three required control commands. The DTE must generate

*(continued on page 26)*

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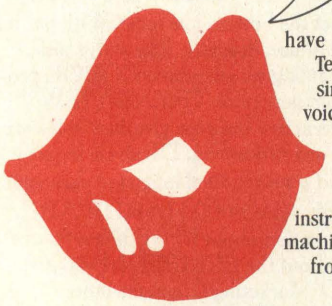

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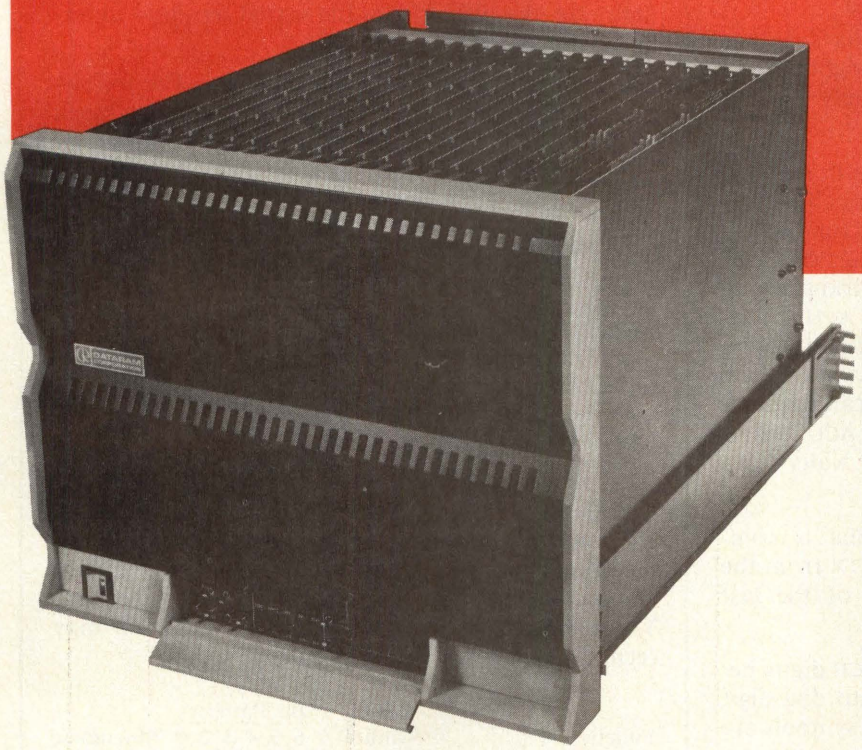

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**CIRCLE 17 ON INQUIRY CARD**

Start Format, End Format, and Abort Call commands, configured as follows:

| Function | Bit Pattern 7 6 5 4 3 2 1 | Mnemonic |
|---|---|---|
| Start Format | 0 0 0 0 0 1 0 | STX |
| End Format | 0 0 0 0 0 1 1 | ETX |
| Abort Call | 0 0 0 0 1 0 0 | EOT |

In this discussion and all following the character has been stripped of start, stop, parity, and eighth information bits. The ACU interpreter reads only the first seven information bits.

*Abort Command from the DTE before the DCE Enters Data Mode*—The DTE may terminate a call at any time before the receipt of an answerback tone brings the DCE into the data mode. If the ACU is strapped for STX control, abort is commanded by transmitting ETX and then EOT from the DTE. If the ACU is configured for RTS control, abort is commanded by allowing RTS to go low (off). Once a call has been completed and the DCE is in data mode, call termination is handled by the DCE. Any time the ACU is commanded to abort, it resets all logic and waits for a new command sequence.

*Redial Command from the DTE*—Redial is commanded by transmitting STX and then ETX from the DTE to the ACU. This causes a retry of the last telephone number sent to the ACU.

*Dial Digit Characters from the DTE*—ASCII digits between 0 and 9 are translated directly into dial digit characters. Additionally, four keystroke symbols are used to communicate vital information:

| ASCII Keystroke | Bit Pattern 7 6 5 4 3 2 1 | ACU Interpretation |
|---|---|---|
| 0 | 0 1 1 0 0 0 0 | Dial Digit 0 |
| 1 | 0 1 1 0 0 0 1 | Dial Digit 1 |
| 2 | 0 1 1 0 0 1 0 | Dial Digit 2 |
| 3 | 0 1 1 0 0 1 1 | Dial Digit 3 |
| 4 | 0 1 1 0 1 0 0 | Dial Digit 4 |
| 5 | 0 1 1 0 1 0 1 | Dial Digit 5 |
| 6 | 0 1 1 0 1 1 0 | Dial Digit 6 |
| 7 | 0 1 1 0 1 1 1 | Dial Digit 7 |
| 8 | 0 1 1 1 0 0 0 | Dial Digit 8 |
| 9 | 0 1 1 1 0 0 1 | Dial Digit 9 |
| : | 0 1 1 1 0 1 0 | Tandem (option) |
| ; | 0 1 1 1 0 1 1 | Pause (option) |
| < | 0 1 1 1 1 0 0 | EON (option) |
| ? | 0 1 1 1 1 1 1 | Last Digit |

Tandem is a command that causes the dialer to wait for another dial tone before going on with the number sequence. Pause is strap selected for 1.28, 2.56, or 5.12 seconds. EON is a special purpose command that causes the ACU to transfer network control to the modem without waiting for any other events.

On receipt of EON the modem jumps into data mode and takes over the line.

*Data Exchange Rate between DTE and ACU*—Because the serial autodialer is an asynchronous device it is capable of a wide range of exchange rates. Strap options provide rates of 75, 110, 134.5, 150, 300, 600, 1200, 2400, 4800, and 9600 bits/s. The command data rate can differ from the actual terminal to terminal rate across the network.

*Block Sequence Format from the DTE*—The following block sequence must be observed. Where a block is designated as optional, the system components must be strapped correspondingly.

| Block Content | Comment |
|---|---|
| Start Format (STX) | Mandatory |
| Chassis Address | Optional |
| DCE Address | Optional |
| Dial Digits | As many blocks as are needed, to a maximum of 25 blocks |
| End of Number | Optional (ASCII:< ) |
| Last Digit | Mandatory (ASCII: ?) |
| End of Format (ETX) | Mandatory |

Note: STX is generated by typing Control/B and ETX by Control/C

*Response Characters from the ACU*—In addition to receiving commands from the DTE the ACU can also communicate certain information back to the DTE. Those who have worked with RS-366 protocol may recognize some of the mnemonics:

| Function | ASCII Symbol | Bit Pattern 7 6 5 4 3 2 1 | Mnemonic |
|---|---|---|---|
| Data Line Occupied | D | 1 0 0 0 1 0 0 | DLO |
| Call Origin Status | C | 1 0 0 0 0 1 1 | COS |
| Abandon Call, Retry | A | 1 0 0 0 0 0 1 | ACR |
| Busy (Remote) | B | 1 0 0 0 0 1 0 | BUSY |
| Character Error | E | 1 0 0 0 1 0 1 | ERROR |

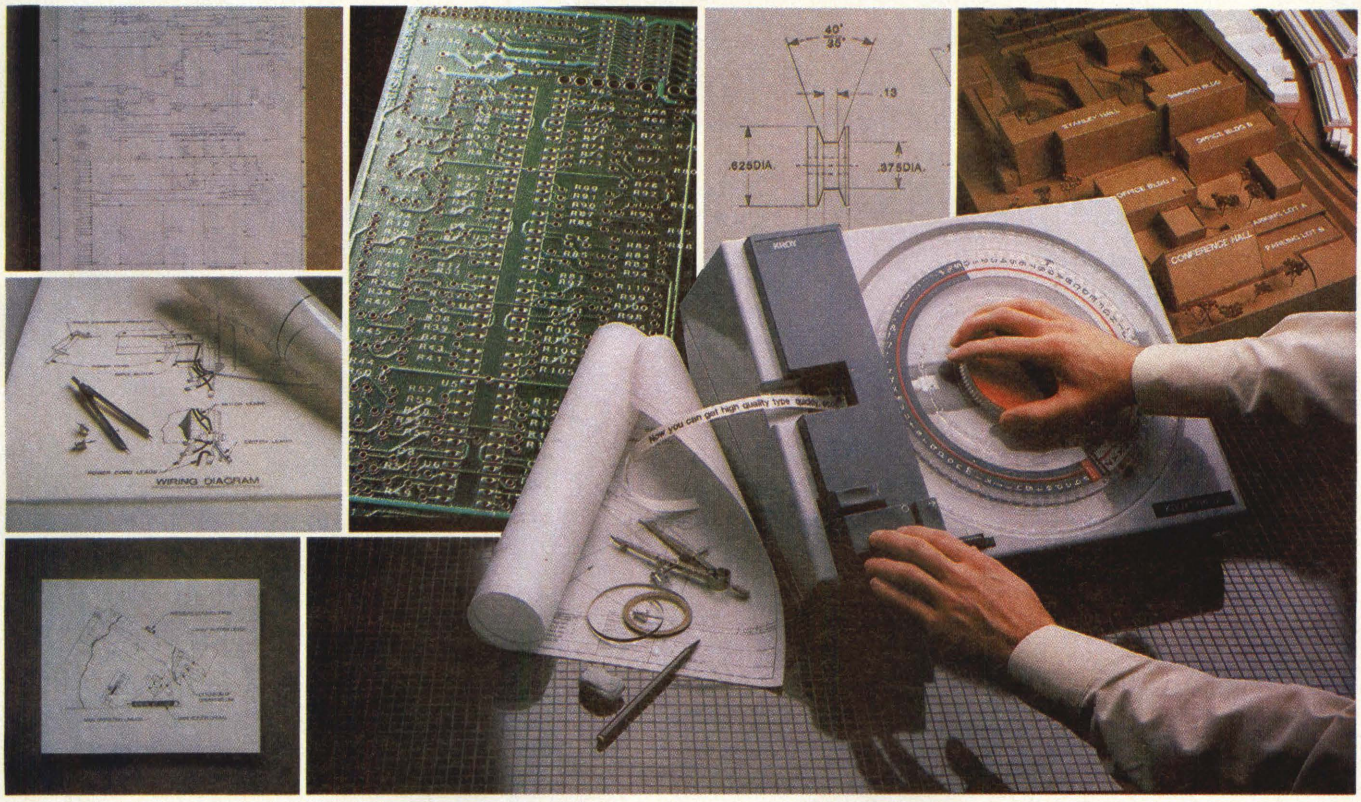
Response Personality of the ACU:

| Condition | Signal | Action Taken |
|---|---|---|
| Call is completed normally | (COS) "C" | DSR turned on |
| Remote end busy | (BUSY) "B" | CTS turned off |
| Call cannot be completed | (ACR) "A" | CTS turned off |
| DCE off hook | (DLO) "D" | CTS turned off |
| Data error detected | (ERROR) "E" | |
| Abort command received | "E" | ACU resets logic, goes back to idle |

### Example of Complete Command Protocol

The illustrative example that follows shows a dial command sequence from DTE to ACU. The start, parity, and stop bits have been stripped away and only the seven significant information bits are

*(continued on page 31)*

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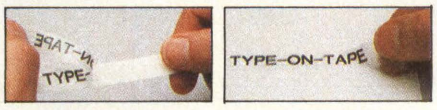


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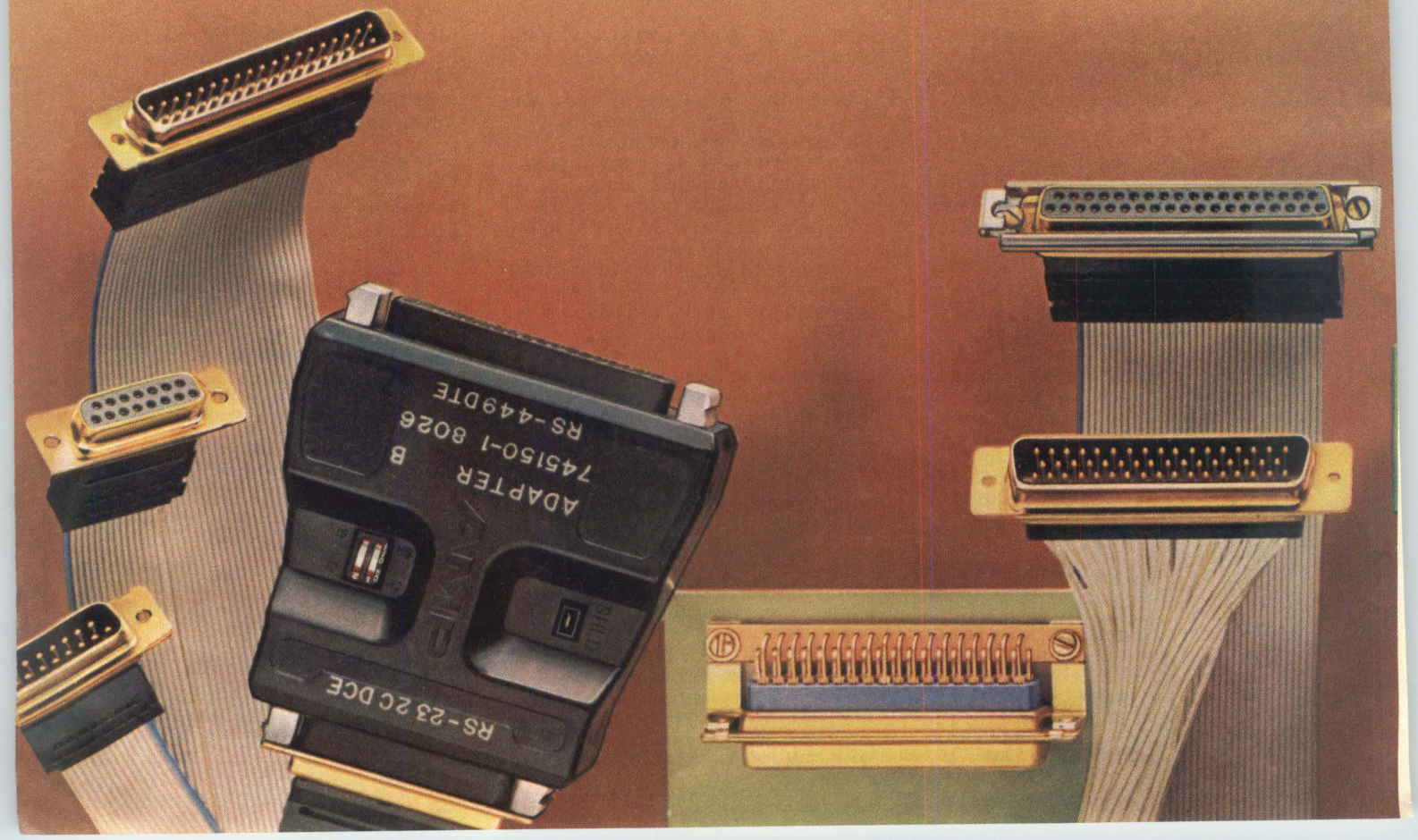

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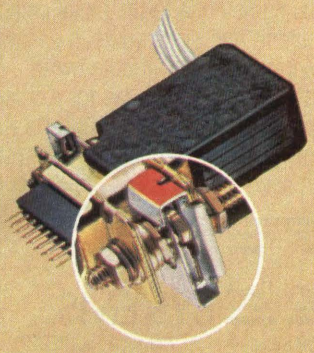

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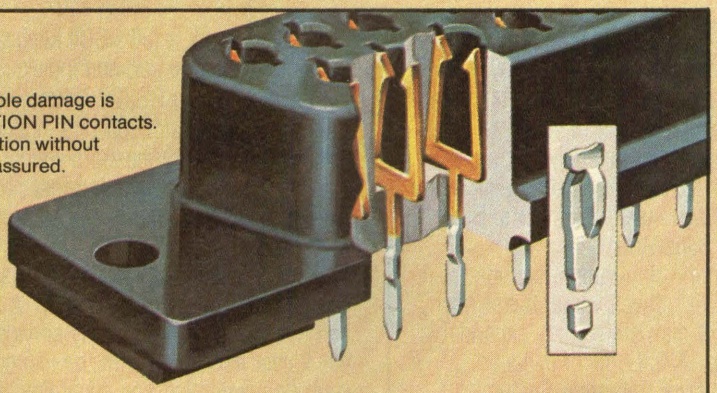

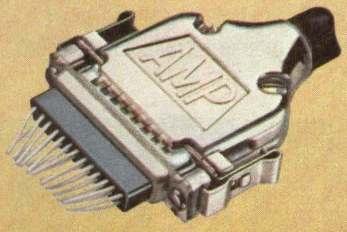


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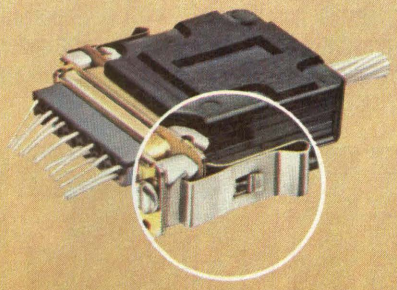

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shown. The number being called is that of Universal Data Systems, Huntsville, Ala, 1-205/837-8100. To illustrate the sequence further, it is assumed that a PBX system calls for the user to first dial the digit 8 for a long distance line, and to wait for a second dial tone before continuing with the actual phone number:

| Block | ASCII Keystroke | Function | Bit Pattern 7 6 5 4 3 2 1 |
|---|---|---|---|
| 1 | Control/B (STX) | Start Format | 0 0 0 0 0 1 0 |
| 2 | 8 | Access LD line | 0 1 1 1 0 0 0 |
| 3 | : | Wait for new dialtone | 0 1 1 1 0 1 0 |
| 4 | 1 | Dial Digit 1 | 0 1 1 0 0 0 1 |
| 5 | 2 | Dial Digit 2 | 0 1 1 0 0 1 0 |
| 6 | 0 | Dial Digit 0 | 0 1 1 0 0 0 0 |
| 7 | 5 | Dial Digit 5 | 0 1 1 0 1 0 1 |
| 8 | 8 | Dial Digit 8 | 0 1 1 1 0 0 0 |
| 9 | 3 | Dial Digit 3 | 0 1 1 0 0 1 1 |
| 10 | 7 | Dial Digit 7 | 0 1 1 0 1 1 1 |
| 11 | 8 | Dial Digit 8 | 0 1 1 1 0 0 0 |
| 12 | 1 | Dial Digit 1 | 0 1 1 0 0 0 1 |
| 13 | 0 | Dial Digit 0 | 0 1 1 0 0 0 0 |
| 14 | 0 | Dial Digit 0 | 0 1 1 0 0 0 0 |
| 15 | ? | Last Digit | 0 1 1 1 1 1 1 |
| 16 | Control/C (ETX) | End Format | 0 0 0 0 0 1 1 |

In the example given, if the installation had multiple modems served by a single ACU, it is possible that block 2 might have contained a modem address, and all other blocks would have been displaced by one block.

### Dialing Options

ACUs can be purchased for use with older sequential pulse rotary dial networks or with the newer Touch Tone[R] dialer networks. Most units are not field convertible from one type to another. The user must ascertain the dialing method at each location when ordering ACUs for remote terminals. A sequential pulse dialer will work on a Touch Tone network, but the reverse is not true.

### Access to the Public Switched Telephone Network

ACUs are now available with direct-connect capability, registered under FCC Docket 19528, Part 68 Rules. These units are usually identified by the letters DC somewhere on their type designation and can be plugged directly into the modular socket provided by the telephone company. These sockets can be either "permissive" or "programmable" and the ACU purchase order must specify the type of connector required. If the ACU is not registered for direct-connect operation, it must be used in conjunction with a registered Data Access Arrangment (DAA).

### Summary

Serial input dialing commands are easy to program and easy for a terminal operator to manipulate. The proposed protocol assumes that interfacing will be from a standard RS-232-C interface port. The protocol offers the latitude necessary to accommodate the user's choice of parity, length of information bit stream, and even the stop pattern. ACUs designed to accept this proposed format are easily strapped to accept the options selected by the user.

There is no reason for the small system user to be denied the convenience of automatic dialing in a data communications network. Serial ACUs impose no penalty on communications port traffic; when considered from a functional point of view, they offer the same benefits as older parallel-input ACUs designed to meet the RS-366 protocol.

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All **GIMIX** Boards have gold plated bus connectors, and are burned in and 100% tested before shipping.

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For further info on the best in 6809 Hardware, contact:

**GIMIX** inc.
*The Company that delivers Quality Electronic products since 1975.*
**1337 WEST 37th PLACE, CHICAGO, IL 60609**
**(312) 927-5510 • TWX 910-221-4055**

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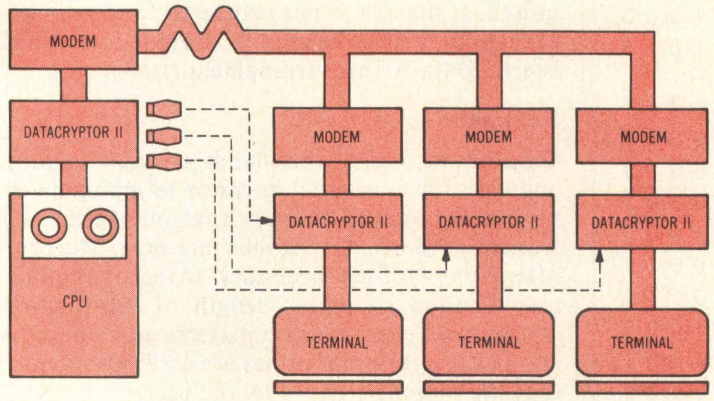
**MICROWARE**
Microware Systems Corp.
5835 Grand Avenue, Des Moines, Iowa 50304
(515) 279-8844 • TWIX 910-520-2535

## Encryption system uses protocol transparent technology to protect data




Typical Datacryptor II configuration. Master keys are generated and copied into modules. Each module is transported to its remote location

Datacryptor II uses a protocol independent encryption technique that enciphers and deciphers data at rates to 9600 bits/s, half- and full-duplex, synchronous or asynchronous, on dial-up or leased point to point or multipoint lines. Introduced by Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166, the system operates without regard to communications discipline or methodology. Units used to encrypt the aggregate of a multiplexer may also be used on a low speed asynchronous dial-up line.

The device uses the self-synchronizing single-bit cipher feedback mode in accordance with the NBS data encryption standard (DES) algorithm. Encrypting data on a bit rather than on a character basis avoids problems with protocols, provides freedom from hardware and software restraints, and delays point to point transmission by only a single-bit time.

A 2-level key hierarchy is used in the key management system: a master key and a working key. The former is used to encrypt and decrypt transmission of the working keys as they are downloaded. The working keys encrypt and decrypt the user's transmitted data and are never stored or transmitted in plain text. Both keys are automatically generated in a random fashion to avoid "weak" keys and remain unknown to the user.

Three standard components make up the system: master datacryptor, remote datacryptor, and master key module. The master unit performs all key management functions. Master keys may be generated or copied into master key modules through operation of two front panel pushbutton switches. Duplicate modules are encoded by the master key and physically transported to the remote site. (See Figure.) The remote datacryptor reads the master key from the modules and decrypts downline working key messages transmitted by the master unit.

Optional asynchronous speeds range from 50 to 9600 bits/s with asynchronous character sizes of 5, 6, 7, 8, or 9, plus 1, 1.5, or 2 stop bits. No internal strapping is required. An anti-tamper interlock switch, dual-key access control, and secure desktop or rack mounting provide physical security. NICAD battery backup protects the working key and associated security codes for a minimum of 1000 hours in the event of a power failure.

**Circle 321 on Inquiry Card**

## Board level Ethernet controller provides physical, data link control interface

Ethernet communications controller iSBC 550 is a 2-board set that provides the physical and data link control interface called for by the joint specification published by Intel, Digital Equipment Corp, and Xerox (*Computer Design,* Mar 1981, pp 12-20). It is manufactured by Intel Corp, OEM Microcomputer Systems Group, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123, and is compatible with the entire line of MULTIBUS™-interconnected single board computer products.

In the Ethernet local area network concept, packet-switched messages are transmitted over a 50-Ω coaxial cable at a 10M-bit/s data rate. The first two layers in the network's architecture are the physical link and data link control layers. These layers are the least application-specific and therefore lend themselves to implementation in hardware and firmware.

The controller provides the 10M-bit/s serial and electrical interface to an Ethernet transceiver. The board uses an 8-bit iAPX 88/10 (8088) microprocessor plus

*(continued on page 38)*

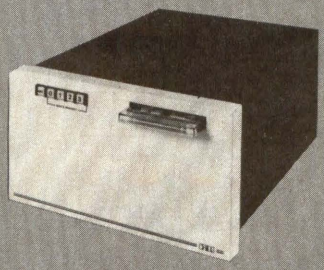
# Build your own DEC system with CRDS...

## MF-211

10½" Enclosure for LSI 11/23 System with built-in RX02 equivalent floppy disk system. Available with or without processor and memory.

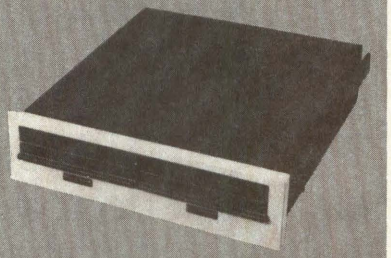
## HD-11/T

20.8 Megabyte Winchester disk software equivalent to 4 RL01 units. Optional cartridge tape backup.



## FD-311

RX02 equivalent dual floppy system, single or double sided. Includes bootstrap loader, self-tester, formatter and diagnostic diskette.



## MB-211

5¼" enclosure with 8 quad slot backplane. Front panel console with switches for Enable/Halt, Boot/Init and Line Time Clock.

# Complete software compatibility at a savings!

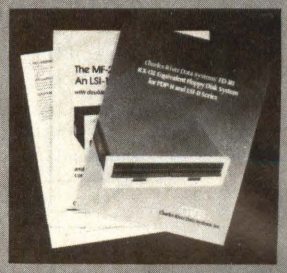
With CRDS, you can configure your own DEC system and be assured of complete software compatibility. Each of the above systems is provided with slides for rack mounting or can be used in desk top applications. All DEC LSI 11 based modules and associated software packages are available through CRDS, if desired.

**Attractive Packaging**
Careful attention is given the CRDS repertoire of enclosures in assuring you an attractive yet comfortable blending of product in the DEC environment.

**Significant Savings**
Flexibility of procurement plus attractive OEM schedules allows you to optimize dollar savings in configuring your CRDS system. Use the time tested technique. Compare.

**Warranty and Maintenance**
A 90 day warranty is offered with your CRDS system. In the event of malfunction, by use of provided diagnostic routines, the defective submodule is normally found within minutes. After verification with the CRDS Maintenance Department, a replacement for your defective module will be promptly forwarded.

**Call or write** for a comprehensive literature package and prices.



CRDS

**Charles River Data Systems, Inc.** 4 Tech Circle, Natick, MA 01760 Tel. (617) 655-1800 TWX (710) 386-0523

**CIRCLE 21 ON INQUIRY CARD**

# SHUGART A REVOLUT

Choice.

If you've been looking at disk drives for desktop systems, you may have thought you had only one choice: take it or leave it.

Not any more. Now you can get everything you need from a single source. And get the added convenience of doing business with one company.

Say you want a reliable, entry-level drive, but cost is critical. The ideal choice? Our SA400, the original Minifloppy.™

Or maybe you need more capacity, but you don't want to give up low cost. Try our double-sided Minifloppy, the SA450.

Then too, you may want to move up to even higher speeds and capacities — up to a megabyte — in a Minifloppy-size package. For that, choose our 96-TPI SA410 single-sided or SA460 double-sided drives.

But what if your desktop system demands the high performance and reliability of a

# INTRODUCES IONARY IDEA.

Winchester? Then specify our new 5.25-inch fixed disk drive, the SA600. It's got ten times the throughput of a floppy, and capacities from 3.33 to 10 megabytes. And by teaming it with a Minifloppy, you get duplicate file backup too.

Now *that's* choice. Which means you get just the right combination of cost and capacity for your application. And in the desktop market, that's a revolutionary idea.

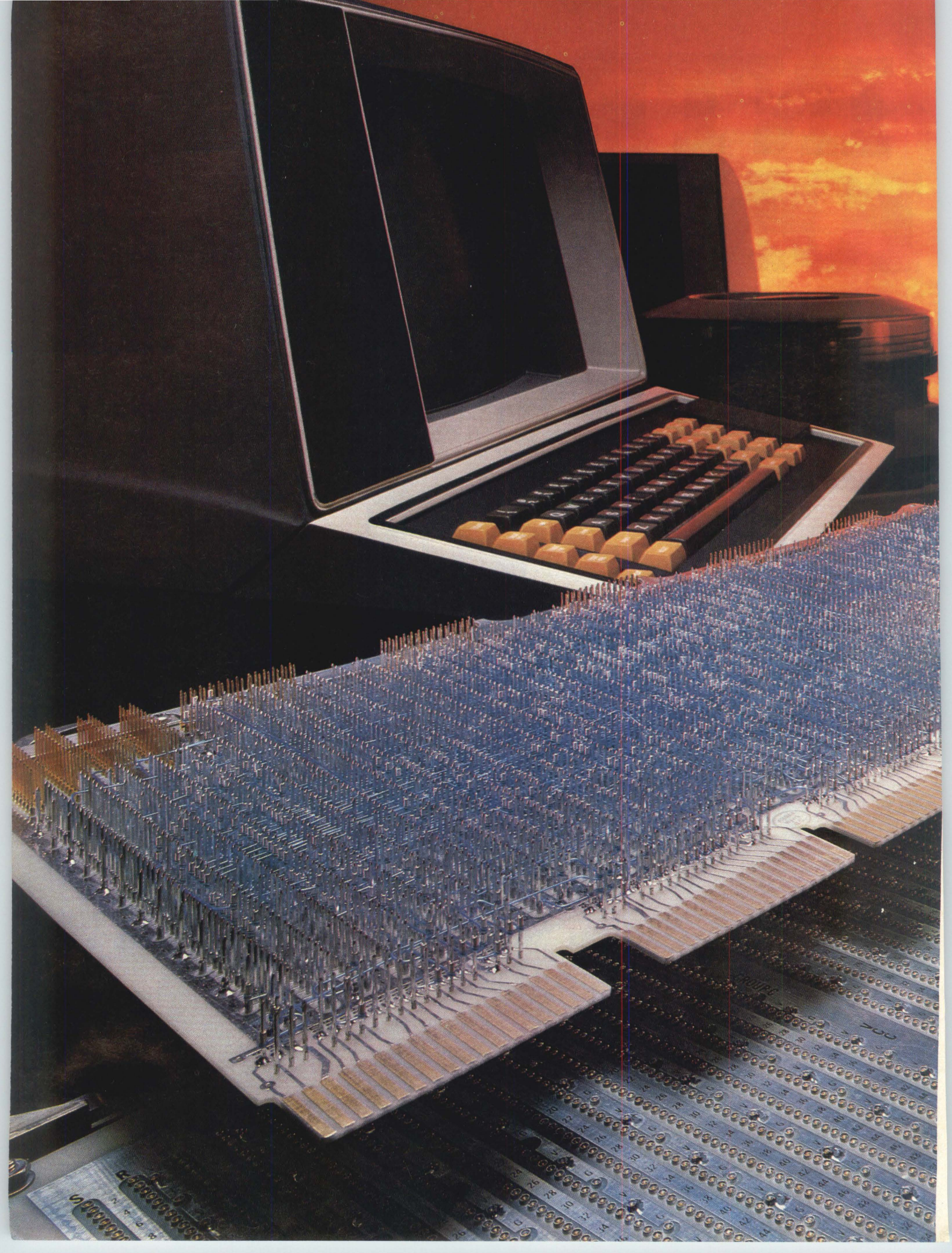
To find out more about your desktop alternatives, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, CA 94086. Telephone (408) 733-0100. Or Hamilton/Avnet, authorized distributor.

**Shugart**

Right from the very start.

Sales and Service: Sunnyvale CA, Costa Mesa CA, Minneapolis MN, Richardson TX, Framingham MA, Landing NJ, Atlanta GA, Toronto Ontario, Paris France, Munich Germany.

CIRCLE 22 ON INQUIRY CARD



# The many interfaces of Augat.

Augat wire wrap* interface panels make it easy to connect with the big names in the minicomputer industry. Digital Equipment Corporation, Data General, Intel, Motorola, Prolog, Zilog, Texas Instruments and all the rest.

First, because our inventory of chassis and bus compatible IC pluggable panels is the most extensive in the business. We have patterned boards and boards with universal columns which accept IC's of all sizes. In fact, there's one to match the specifications of virtually any minicomputer on the market today.

Second, because Augat interface panels give you the time- and money-saving advantages of wire wrap. Their inherent flexibility lets you get your design to the market faster. A strategic advantage and a head start on sales and profits. Logic and wiring changes are quick and inexpensive at any design stage—pre-production, production, even in the field.

What's more, the natural heat dissipation of wire wrap posts keeps IC surfaces cooler for longer chip life and greater reliability. And since in most cases the high planar density of panels easily offsets the pin extension, you get greater volume density as well.

Need a custom panel for a special application? No problem. Augat engineers are ready to help. They'll put their years of experience to work and come up with a board that meets your requirements exactly.

The many interfaces of Augat. They're the fastest, easiest way to interface the minicomputer industry. Get all the details from your Augat distributor, or write Augat, Interconnection Systems Division, 40 Perry Avenue, P.O. Box 779, Attleboro, MA 02703. Tel: 617-222-2202. TWX: 710. 391.0644. In Europe, Augat SA—Fresnes, France. Tel: 668.30.90. Telex: 201.227 AUG-SAF.

AUGAT®

Augat interconnection products, Isotronics microcircuit packaging, and Alco Subminiature switches.

*Registered trademark of Gardner Denver Company.

CIRCLE 23 ON INQUIRY CARD

8k bytes of EPROM. The EPROM is preprogrammed with data link control software to meet the Ethernet specification and the MULTIBUS message exchange (iMMX) interface. 16k bytes of dynamic RAM and a separate 8k bytes of static RAM are included for DMA to support high speed communications. The boards are identical in size to all iSBC compatible boards and will fit into any iSBC chassis. The controller works with any component based system that supports the MULTIBUS interprocessor protocol.

Cable access and actual transmission and reception of the Manchester coded message signals on the cable are handled by the physical link control layer. The controller implements all Ethernet specifications except for the actual transmission hardware.

Arranging the message in the specified frame sequence and appending the 32-bit cyclic redundancy check value is done by the data link layer. This layer also handles carrier sense multiple access/collision detection (CSMA/CD) that enforces one-at-a-time cable access and the handling of error conditions when collisions do occur.

The controller offers users a means to implement Ethernet control quickly in an iSBC-based prototype. Applications programs for Ethernet-connectable prototypes are developed in the same way as programs for any iSBC based system. The controller is designed to work in a realtime multitasking environment (iRMX). Application programs executed by iSBC CPU boards will pass messages to the Ethernet controller with the support of the MULTIBUS message exchange software (iMMX 800).

**Circle 322 on Inquiry Card**


# Give Your Present CPU Video I/O Capability

## This Board Makes Real Time Digitized Imaging Possible... Economically

In 17 msec. the image above was viewed by a camera, stored in memory, retrieved, and displayed in pseudo-color. This VG-120 board made it possible.

Put sight in your present system by mating your computer with our VG-120 Video Graphics Boards that can digitize and display information from standard video cameras for Intel's MULTIBUS™ and DEC'S Q-BUS™ systems.

A VG-120 couples easily to your display. Inputs and outputs are RS-170 compatible, with up to 8 bits flash A/D inputs. It stores up to 768 H x 512 V x 16 bits in black-and-white or pseudo-color.

For as little as $3,000, you can bring sight to your system. Call today for details.

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670 Main St., Reading, MA 01867
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## Interface enables 1M-baud DMA transfers between Intel microprocessors

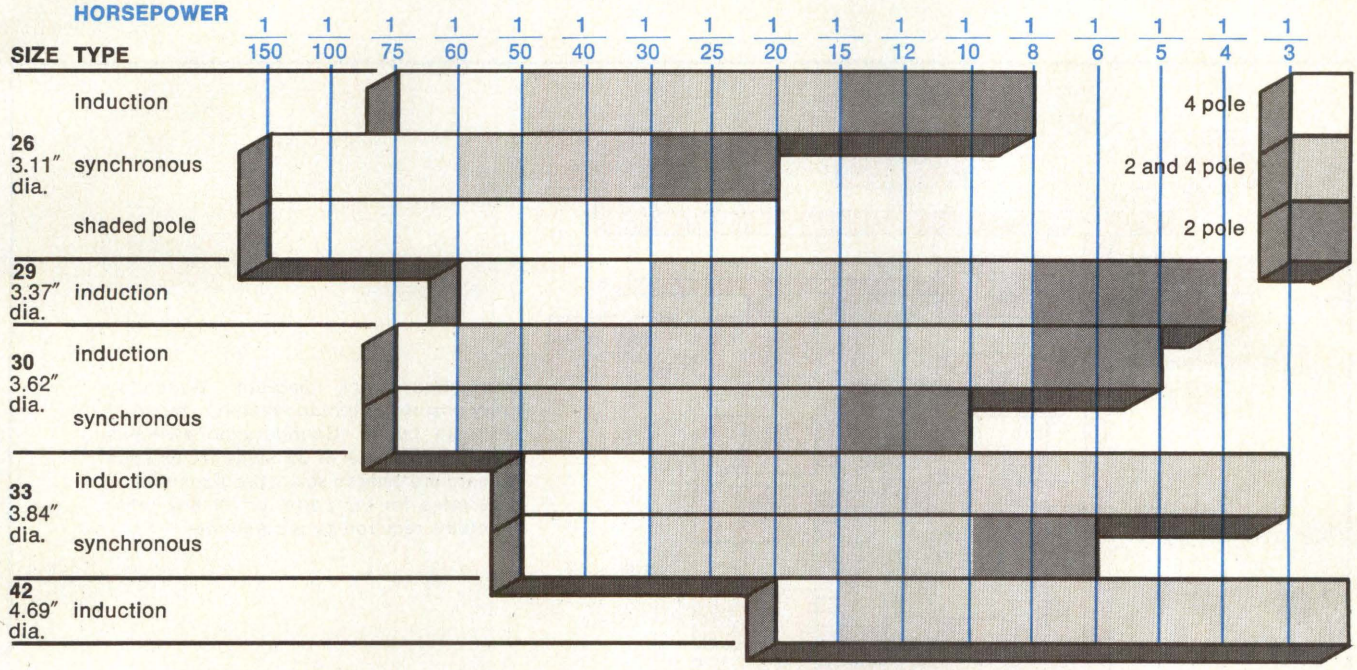
MULTIBUS compatible interface model 11-0080 Megalink from Computrol Corp, 15 Ethan Allen Hwy, Ridgefield, CT 06877, permits DMA block transfers between as many as 255 Intel iSBC/System 80 and 86 microprocessors at a 1M-baud rate over a single coaxial cable up to 32,000 ft (9754 m) in length.

Communications protocol is HDLC. Protocol and control functions are implemented in hardware and onboard EPROM and require no program intervention. Network protocol can be polled, token pass, or all peer contention. The interface onboard microprocessor handles all link operations including network polling, automatic retry on error, and communications control independently of host processor.

An integral, wide dynamic range, 1M-baud coaxial cable modem enables operation at any point on the cable without need for gain adjustments. Provisions for carrier control permit half-duplex point to point and multidrop party line operation on a single cable. The circuit is packaged on a standard 6.75 x 12″ (17 x 30.5 cm) board that plugs directly into iSBC/80-86 card cages.

**Circle 323 on Inquiry Card**

# The right motor for you



How can you design the right AC motor into your new equipment? Check the speed-HP envelopes above, then ask Robbins & Myers for exactly what you need. You will get precisely the speed, performance, features, and long life you require. Superior manufacturing technology then yields consistent motors from production lot to lot.

This approach differs from motor manufacturers who may force you into their standards rather than match your application needs. It's one reason Robbins & Myers motor customers return again and again; the motors help them build a trouble-free reputation. Request catalog D-1120 from Electric Motor Division, Robbins & Myers, Inc., 1345 Lagonda Ave., Springfield, OH 45501. Tel. 513-327-3329.

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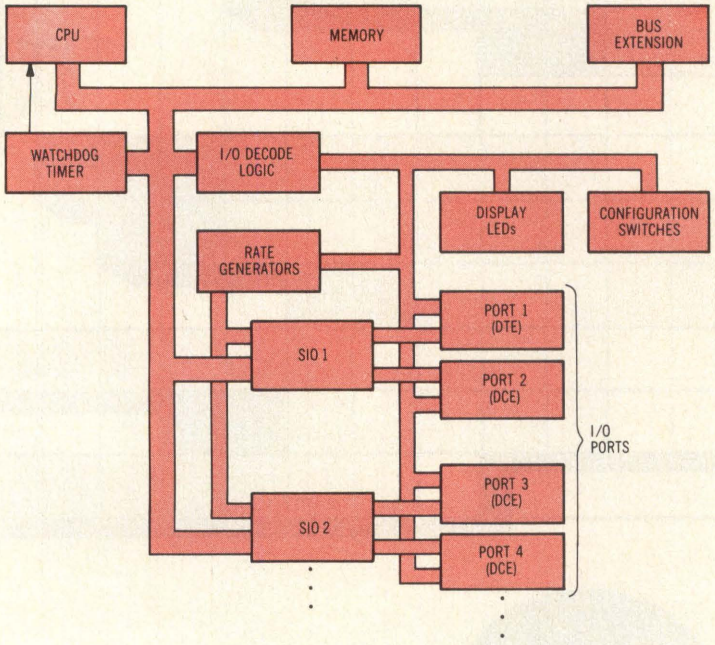
CIRCLE 25 ON INQUIRY CARD

## Microcomputer system designed specifically for data communication applications




OrangeBox block diagram. Watchdog timer ensures automatic restart in event of software failure. Configuration switches on 4 DIPs for total of 32 switches on each PC card are used to select program modes, data rates for I/O ports, or for any other functions required by programmer

Designed for data communications applications using both synchronous and asynchronous protocols, the Micro30 OrangeBox™ line of communications processors implements a broad range of communications controllers and front-end devices in conjunction with user-developed software. The processor, from Micom Systems, Inc, 20151 Nordhoff St, Chatsworth, CA 91311, is packaged as a standalone unit having 2 to 18 communications interfaces. It is also available in a rackmount version.

The device is organized as a single self-contained PC card module that contains a Z80A microcomputer, EPROM and RAM memory, and up to six I/O ports. Incorporation of the Z80A permits use of the complete instruction set and capabilities. Memory includes 16k bytes of 4116 dynamic RAM and sockets for up to four 2732 or 2764 EPROMs for as much as 32k bytes of EPROM space.

Associated Z80A programmable serial I/O (SIO) ICs provide a range of synchronous and asynchronous I/O functions that include interface control, CRC and parity generation and checking, flag and zero insertion and deletion, and sync character insertion. The SIO can be programmed to interrupt on error conditions, changes in interface control lead state, and changes in buffer status.

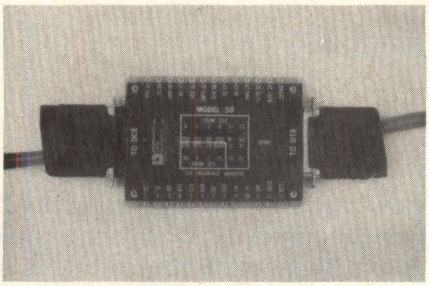
A programmable rate generator offers 13 independent data rates from 50 to 9600 bits/s, or external clocking can be used on most ports. The rate generator output can also be used for a realtime clock function. Time-sensitive or time of day functions may also be obtained from a derivative of the 50/60-Hz power line frequency.

Each model of the processor has one EIA RS-232-C interface configured as DTE with male connector and one optional interface configured as DCE with female connector. Additional models are available having from 2 to 16 DCE interfaces.

Options include a built-in LSI synchronous modem module for 2400-, 4800-, or 9600-bit/s operation, and synchronous support for DCE interfaces.

**Circle 324 on Inquiry Card**

## Compact interface monitor is transparent to codes and line disciplines



DTE/DCE line interface monitor. Spare LED allows any other EIA signal to be monitored by patching desired line into spare LED circuit

EIA interface monitor model 50 provides access to all 25 conductors of the RS-232-C/V.24 interface between modem and terminal. It is installed inline at the data interface, does not affect data flow, requires no external power, and has no

*(continued on page 42)*

# THE LATEST ADVANCE IN VIDEO GRAPHIC HARD COPY RECORDING FROM HONEYWELL

VGR 4000, Honeywell's new and advanced video graphic recorder, provides fast, crisp, 8½ x 11" hard copies on dry silver paper from most CRT's and other video sources.

White-on-black or black-on-white images are as simple as flipping a switch. With options, images can be produced having up to 16 shades of grey or even more.

An innovative processing technique eliminates the need for large heated platens. This allows the recorder to run cool, consuming very little energy.

The VGR 4000 is the only recorder on the market available with a self-contained test-pattern generator providing a choice of formats for proper copy verification.

Rugged, yet cleanly designed for easy operation, the compact VGR 4000 can be used on a desk top or rack-mounted, taking up only 7" of front panel space.

Honeywell's VGR 4000 is the latest advance in video-input hard-copy reproduction systems, built by the people with the most fiber-optic CRT recorder experience in the field.

To get the whole story on the VGR 4000 and how it can meet your needs, call Durke Johnson at 303/773-4700. Or write Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

**WE'LL SHOW YOU A BETTER WAY.**

**Honeywell**

HON-6-631

CIRCLE 26 ON INQUIRY CARD

moving parts. The device, a product of International Data Sciences, Inc, 7 Wellington Rd, Lincoln, RI 02865, uses 12 LED indicators to monitor line conditions of the most common EIA signals: TD, RD, RTS, CTS, DSR, DCD, TC, RC, DTR, SQ, RI, and BUSY. Numbered and labeled test points provide access to all 25 conductors of the interface to allow connection of instruments for further analysis.

The unit is a PCB assembly housed in an anodized aluminum case measuring 4.5 x 3 x 0.5″ (11.4 x 7.6 x 1.3 cm) and may be permanently interconnected or temporarily installed to verify proper activity at the signal interface. D-type 25-pin connectors mounted at each end of the monitor case and clearly marked for proper polarity provide the DTE/DCE interface. The case carries an EIA/CCITT modem-terminal interface chart that lists all pertinent designations of the 25 conductors.

**Circle 325 on Inquiry Card**


# WE PRICED OURSELVES RIGHT INTO BUSINESS.

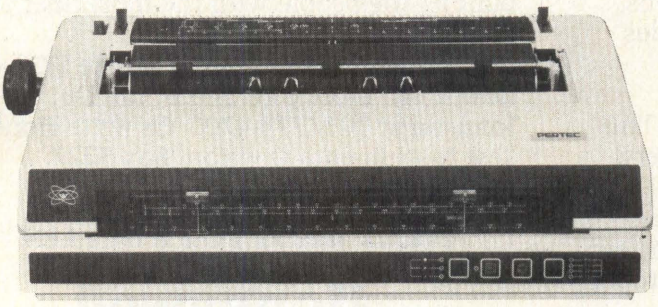
At about half the cost of most daisywheel printers, the Pertec Stylist 360™ is making quite an impression.

Not simply because of the price, but because of the technology behind it. In fact, feature for feature, it outperforms printers costing twice as much.

Now if we can do this with a printer today, imagine what we'll do tomorrow.

For more information, write Pertec Computer Corporation, Peripherals Division, 21111 Erwin Street, Woodland Hills, CA 91367.

PERTEC PERIPHERALS Perfecting Technology



PERTEC 360 STYLIST PRINTER

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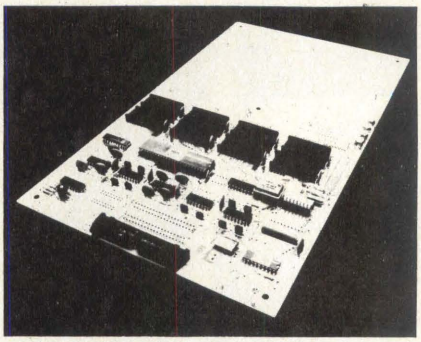
## Kit aids designers of X.25-related circuitry and development systems

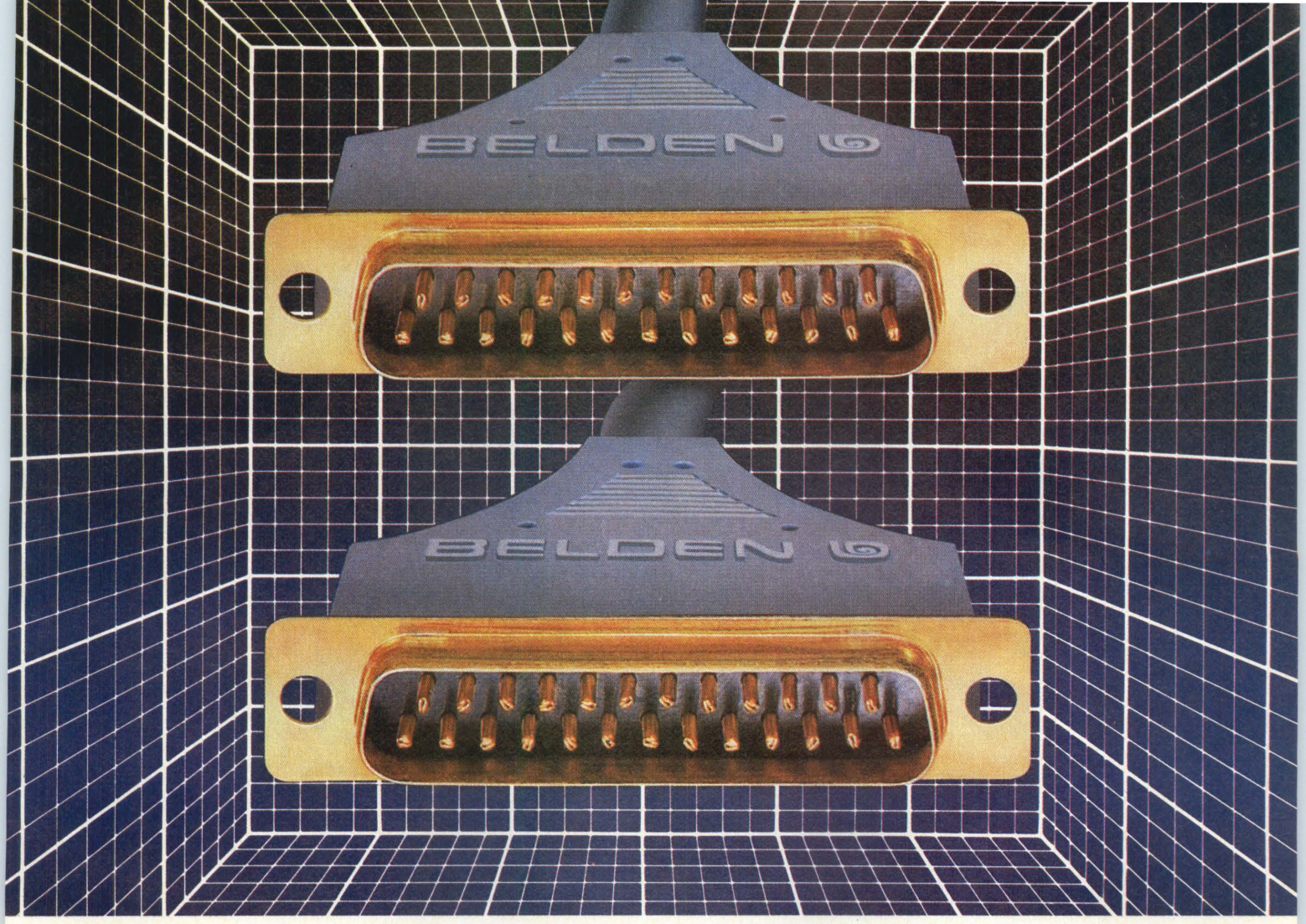


Design aid for X.25 circuitry. Levels 1, 2, and memory functions are premounted. Large open board area allows designer to prototype other X.25-related circuits

Architecture for X.25 Level 1 (serial I/O interface), Level 2 (logical link), and memory interface are predesigned into the board of the X.25 PAC-KIT, allowing the designer to construct Level 3 software for network control, develop a bus or other interface for specific equipment, or analyze Level 1 and Level 2 procedures. The kit has been developed by Western Digital Corp, Telecommunications Div, 3128 Red Hill Ave, Box 2180, Newport Beach, CA 92663.

The kit enables integration into any development system, laboratory microprocessor, or host system, and is designed to save time in creating X.25 circuitry for specific hardware and dedicated network applications. Heart of the design aid is the company's WD2501 link level controller subsystem that provides transparent, automatic, and unsupervised control for executing Level 2 link access procedures. The 8 x 14″ (20.3 x 35.6-cm) vector board also includes an RS-423 interface, a crystal and baud rate generator, DMA interface, RAM/ROM/EPROM sockets, and a large wirewrap area for prototyping. The kit comes with assembly instructions and an operations manual.

**Circle 326 on Inquiry Card**

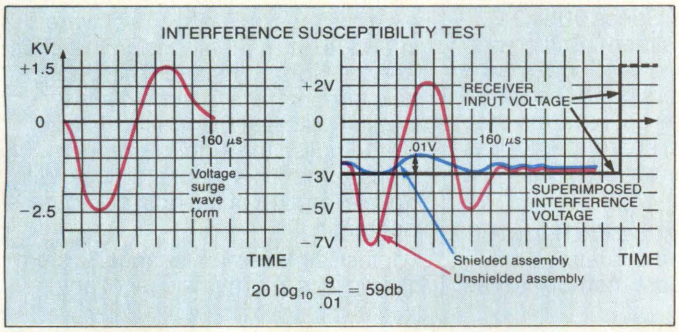



# One of these cable assemblies can cut your interference levels 59 db.

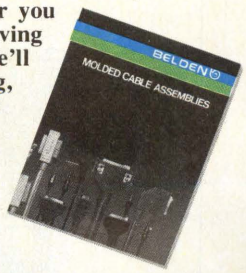
**Both meet RS-232-C specifications. Both are made by Belden using rugged materials and proven designs.**

**But one is shielded. One is not. And that can make a big difference in critical data communications applications.**

**Although RS-232-C standards do not specifically call for shielded interconnect devices, our research indicates that cable *and* connector shielding is required to insure the signal integrity of the assembly. In fact, transfer impedance, leakage current power spectrum, electrostatic discharge and interference susceptibility tests at Belden all demonstrate the value of Belden totally shielded connector-cable assemblies over nonshielded assemblies.**




**With a complete line of rugged and highly reliable standard molded connector designs including GPIB, and complete custom design capabilities, we can make exactly what you need, when you need it. And show you ways to increase performance without increasing costs. Whenever you have a shielding need or a question involving interconnect devices, contact Belden. We'll share our experience. For a free catalog, write Belden Corporation, Interconnect Systems Operation, 105 Wolfpack Rd., Gastonia, NC 28052. Phone: (704) 865-4513.**




**BELDEN**

***Coming through...***

*with new ideas for moving electrical energy*

**CIRCLE 28 ON INQUIRY CARD**

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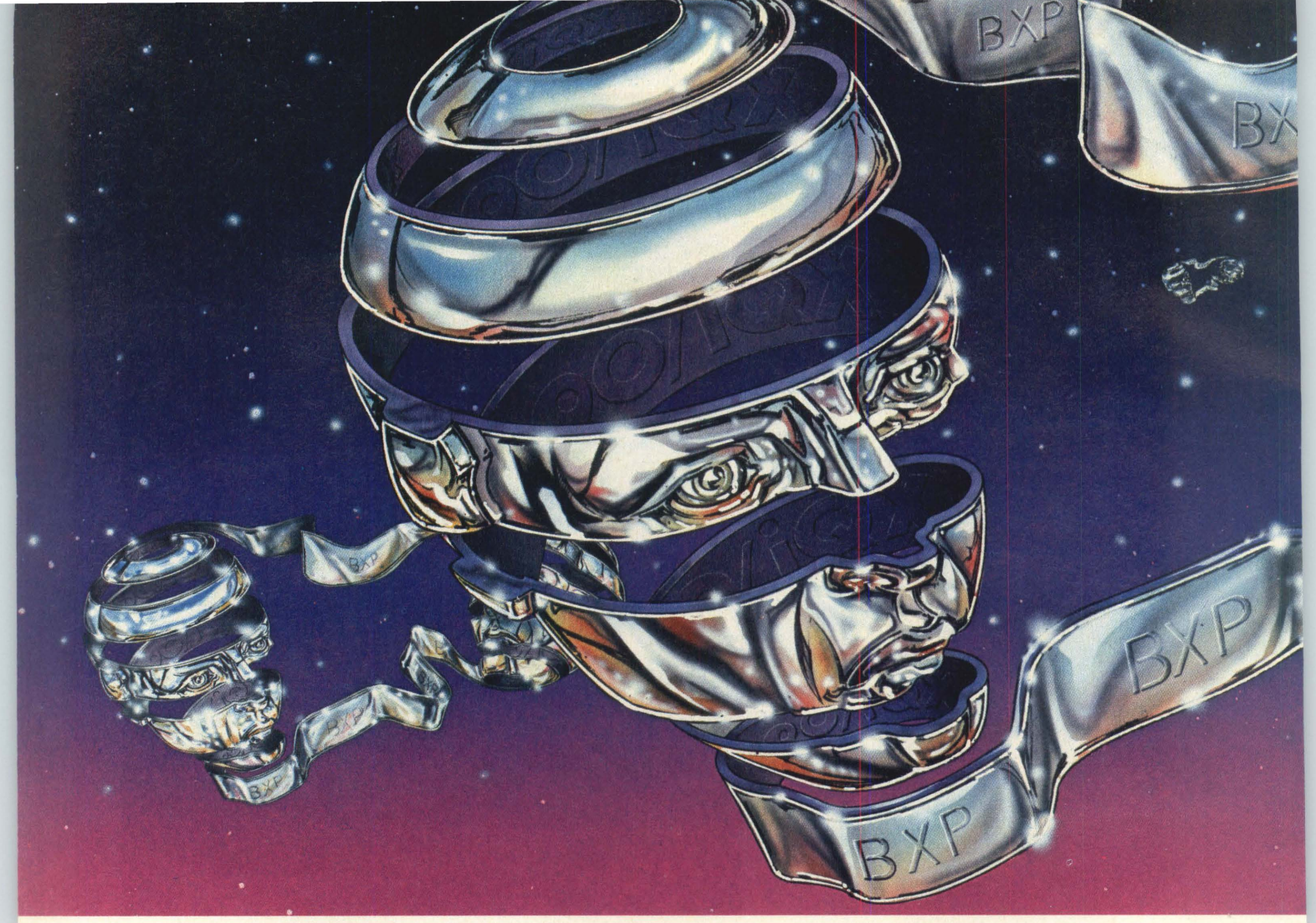


# Intel's Series 90/iQX. The memory

**Intel's new Series 90/iQX is the first standard Intelligent Memory System to offer continuous operation and high maintainability at low cost.**

Now, for the first time, OEMs can design systems with built-in protection against errors, downtime, and excessive maintenance costs. How? With Intel's new Series 90/iQX.

*Series 90/iQX Intelligent Memory System*

The iQX controller adds the intelligence of an iAPX 86 microcomputer to the standard Series 90 Memory System. Intelligence that monitors memory operation directly, detects and corrects errors, runs local or remote diagnostics, and reallocates memory space as required. All without burdening the host system.

## Fault-tolerant operation

Hard errors or soft, Series 90's iQX controller uncovers them. Soft errors are simply "scrubbed" and corrected. In case of hard errors or device failure, the controller routes data around the problem, allocating spare memory as needed. It then logs the error for future reference.

With protection like this, the Series 90 system will continue operating uninterrupted until all spare memory is filled.

And thanks to the iQX's memory status reporting, your customer will know well in advance of memory resource problems. Which not only improves data integrity, but increases reliability and reduces maintenance dramatically.

## Instant diagnostics

To keep users continually apprised of conditions within their memory system, the iQX controller provides easy access to its complete diagnostic file. Information can be accessed by the host system either automatically via a simple message-driven software interface, or manually, using the iQX's Service Communicator. This detachable terminal allows technicians to instantly retrieve diagnostic data in plain English through a compact, alphanumeric keyboard/display. With no interruption of the host computer's operation.

For fast, simple maintenance, system diagnostics inform the user of any

# machine with non-stop intelligence.

errors it has tracked—soft or hard, correctable or avoidable—and their precise location by row and column.

Many problems can also be solved using the iQX's memory tasking capability to move data blocks as required. Then too, the iQX monitors the system's power supply and signals a warning if voltages drop critically. As a final, double protection, the iQX controller even diagnoses its own operation continuously.

## Diagnosing from a distance

To reduce maintenance costs for remote systems and networks, iQX diagnostics can be accessed over phone lines through a single diagnostic station. By being able to analyze problems from afar, you'll eliminate unnecessary service visits and shorten those that are required. And since one diagnostic station can easily serve up to 150 installations, the set-up and ongoing diagnostic costs are contained as well.

## Consider the economics

The iQX's protection features offer important economic advantages for systems OEMs. Because of the increased demand for fault tolerance in today's marketplace, systems equipped with iQX capability add significant value to your products. In fact, many applications simply could not be justified economically *without* such self-healing and remote maintenance. Now, through Intel's leadership in 16-bit microprocessing, the Series 90/iQX brings you this capability at an incremental price only nominally above that of ECC alone.

In sum, iQX gives your systems state-of-the art fault protection, reduced maintenance costs, and therefore increased value. Best of all, Intel is delivering Series 90 systems with iQX right now. For detailed information, return the coupon to Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080. For hot line service, call (800) 538-1876.

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CIRCLE 29 ON INQUIRY CARD

## BRIEFS

**Software package links Data General minicomputers to UNIVAC mainframes**—Data communciations software that allows NOVA and ECLIPSE minicomputers to connect to UNIVAC mainframes using the NTR RJE protocol has been introduced by Gamma Technology, Inc, 2452 Embarcadero Way, Palo Alto, CA 94303. NTR workstation software supports all std protocol features including multiple I/O streams, console, full-duplex operation, space compression, and remote operator control over output peripherals. The software interfaces to Data General's RTOS, RDOS, and AOS. Under AOS, jobs may be entered from any user console, full I/O queuing facilities are available, and multiple workstations communications protocols can be run concurrently.

**Circle 327 on Inquiry Card**

**Processor links dumb terminals to 3270 devices**—Designed to enable "dumb" terminals to communicate with equipment in the IBM 3270 environment, C-80 terminal controller/concentrator allows dial access from remote sites. The processor has been introduced by Alanthus Data Communications Corp, 6011 Executive Blvd, Rockville, MD 20852. It can maintain simultaneous data link connections with two separate host mainframes or networks. TTY-compatible to 3270 protocol conversion capability is said to cut traditional CRT workstation costs by as much as 75%. The processor can work with as many as 25 terminals or workstations. Workstations can operate with the controller located up to 1000′ (305 m) distant with the integral RS-422 interface; RS-232 interface is also standard. Data rates to 19.2k bits/s can be accommodated. Add-in of processing power, additional memory, and applications software is enabled by modular design.

**Circle 328 on Inquiry Card**

**Software brings electronic mail to Apple users**—Owners of Apple II desktop computers can transmit charts, graphs, correspondence, and entire programs to other Apple computers over std telephone lines using the Micro-Courier software package from Microcom, 89 State St, Boston, MA 02109. A menu driven program guides the user in plain English. Transmissions can be sent automatically enabling use of lower nighttime telephone rates. Use of the software package is said to enable transmission of 1k words of text in one minute for less than $0.25 as against a comparable TWX™ message cost of $4.32.

**Circle 329 on Inquiry Card**

**Viewdata software package conforms to Prestel standards**—ViewMax viewdata software package comes separately or as a complete ready to run viewdata system when combined with the CLASSIC minicomputer hardware. It is available from Modular Computer Systems, Inc, PO Box 6099, 1650 W McNab Rd, Ft Lauderdale, FL 33310. The company's std operating system MAX IV supports the system and enables combining ViewMax with other applications. The package conforms precisely to Prestel standards as an information storage and retrieval medium. Additional features simplify creation, editing, and maintenance of viewdata text and graphics. Menu selection and editing facilities are std and a bulk update feature supports both incoming and outgoing updates. System pricing ranges from a single processor system to a maximum of 256 ports. The software is sold with an indefinite life. Availability is scheduled for Sept 1981.

**Circle 330 on Inquiry Card**

**4800-bit/s modem added to Bell compatible series**—A new addition to the 5000 Series of Bell compatible modems from Codex Corp, 20 Cabot Blvd, Mansfield, MA 02048, the 5208R 4800-bit/s modem is compatible with Bell 208A and 208B and can operate over both dial-up and leased lines. The device features microprocessor controlled adaptive equalization and a compromise equalizer to reduce errors. A wide range of fault isolation and error detection functions are included. Line connection is via an integral RJ-11C interface.

**Circle 331 on Inquiry Card** □

**A new long-life alternative to trackballs**

With this new X-Y controller all you do is slide your fingertip in the desired direction.

Then 3600 solid-state sensors embedded in a tough plastic block along with VLS hybrid circuitry detect the presence, motion, and direction of motion of your fingertip on the Touch Graphics™surface, producing X- and Y- digital control signals for all graphics applications.

The result is a cost-effective alternative to trackballs, light pens, thumb wheels, etc.

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This is a new micro-proximity touch-sensing technology you should know about. Call now for sales literature on this and other control devices.

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# POWER-ONE
# D.C. POWER SUPPLIES

## Our customers select their favorite models

The choice wasn't easy. Not with 105 open frame linears and a full switcher line to choose from. Still, the top models of the past year — proudly pictured below — have been named.

Actually, this is a statement of Power-One's most popular D.C. power supplies — as determined by our customers. Obviously, applications vary widely, from small floppies and micro-computers to large main-frame systems.

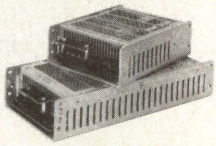
But one thing they all have in common. They're built by Power-One. Which means the most reliable power supplies available, at the lowest cost possible.

So take a look at our entire line. Send for our new 1981 Catalog and Facilities Brochure for details.

### Switchers

- Hi-Tech Design
- High Efficiency - 75% min.
- Compact/Light Weight
- 115/230 VAC Input
- 20 msec Hold-up
- Totally Enclosed Packaging
- Two Year Warrantee
- 24 Hour Burn-in

### SINGLE OUTPUT

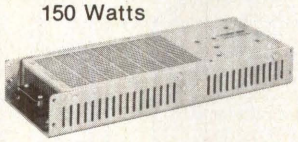


5V to 24V Models

SD, 60W : $115.00
SF, 100W : $170.00
SK, 200W : $250.00

### MULTIPLE OUTPUT

150 Watts



5V @ 20A
12V @ 5A
-12V @ 3A
5V to 24V @ 3.5A
User Selectable

SHQ-150W : $295.00

### QUME PRINTER SUPPLY

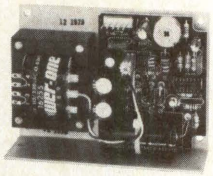
5V @ 10A
±15V @ 4.5A/16A Peak

SP305 : $345.00

### Disk-Drive

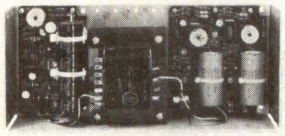
- Powers Most Popular Drives
- 7 "Off the Shelf" Models
- Powers Drives & Controller
- UL & CSA Recognized
- 115/230 VAC Input

### 5¼" FLOPPY SUPPLIES



CP340, 1 Drive : $44.95
CP323, Up to 4 Drivers : $74.95

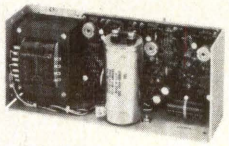
### 8.0" FLOPPY SUPPLIES



CP205, 1 Drive : $69.95
CP206, 2 Drives : $91.95
CP162, Up to 4 Drives : $120.00

### WINCHESTER SUPPLIES

2 Models to Power any Manufacturer's Drive

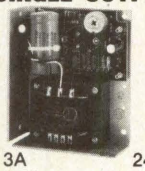


CP379, CP384 : $120.00

### Open-Frame Linear

- Industry Standard Packages
- 115/230 VAC Input
- ±.05% Regulation
- Two Year Warrantee
- UL & CSA Recognized
- Industry's Best Power/Cost Ratio

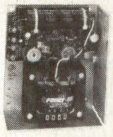
### SINGLE OUTPUT



5V @ 3A
12V @ 1.7A
15V @ 1.5A
24V @ 1.2A
28V @ 1.0A
250V @ 0.1A

HB Series : $24.95

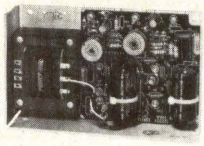
### SINGLE OUTPUT



5V @ 6A
12V @ 3.4A
15V @ 3.0A
24V @ 2.4A
28V @ 2.0A
48V @ 1.0A

HC Series : $44.95 to $49.95

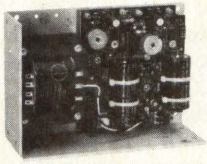
### DUAL OUTPUT



±12V @ 1.0A or
±15V @ 0.8A

HAA15-0.8 : $39.95

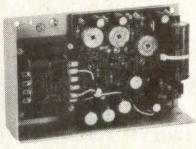
### DUAL OUTPUT



±12V @ 1.7A or
±15V @ 1.5A

HBB15-1.5 : $49.95

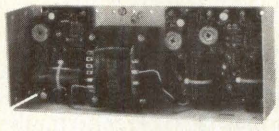
### TRIPLE OUTPUT



5V @ 2A
±9V to ±15V @ 0.4A

HTAA-16W : $49.95

### TRIPLE OUTPUT



5V @ 3A
±12V @ 1A or
±15V @ 0.8A

HBAA-40W : $69.95

### POWER FAIL MONITORS

- Indicates pending system power loss.
- Monitors AC line and DC outputs.
- Allows for orderly data-save procedures

PFM-1 : $24.95 PFM-2 : $39.95

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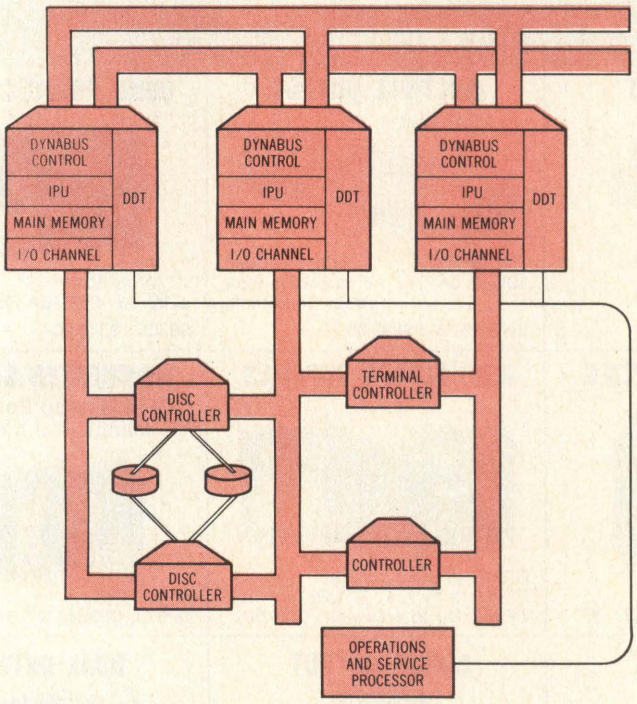
CIRCLE 31 ON INQUIRY CARD

## 32-bit data access architecture supports I/O intensive transaction processing




Architecture of Tandem NonStop II system is made up of multiple, independent processors all interconnected by Dynabus. Dual-ported I/O controllers allow each controller to be connected to two different processors. Separate operations and service processor provides entire system with operating and maintenance support

NonStop II™, a fault tolerant, network oriented computer system, fits online transaction processing applications that require hundreds of interactive terminals and communications lines. The multiple processor computer system, announced by Tandem Computers Inc, 19333 Vallco Pkwy, Cupertino, CA 95014, extends the NonStop™ architecture designed for continuous system operation and data integrity.

Key to implementing the system's extended virtual address space which places up to 1G bytes of data per processor under control of the operating system is a 32-bit data access architecture. Systems are modularly expandable from 2 to 16 processors with a fully expanded system addressing up to 16G bytes of virtual memory.

Architecturally the system is composed of multiple independent processors. Dual-ported I/O controllers allow each controller to be connected to two different processors. A separate operations and service processor provides the entire system with operating and maintenance support. Each processor module is an autonomous computer system with its own memory, power supplies, diagnostic facilities, and I/O capabilities.

Each processor module includes an instruction processing unit (IPU), main memory, Dynabus interface unit, I/O processor, and diagnostic data transceiver (DDT) processor. The instruction processing unit is a microcoded processor that uses stack architecture to provide efficient implementation of high level languages.

The IPU is implemented using Schottky TTL and has a microinstruction cycle time of 100 ns. The basic set of 242 machine instructions provides stack operations, 16-, 32-, and 64-bit integer arithmetic, and byte oriented functions such as scanning and comparing strings. It also supports 32-bit extended addressing. The optional floating point instruction set provides 43 instructions for high speed scientific calculations.

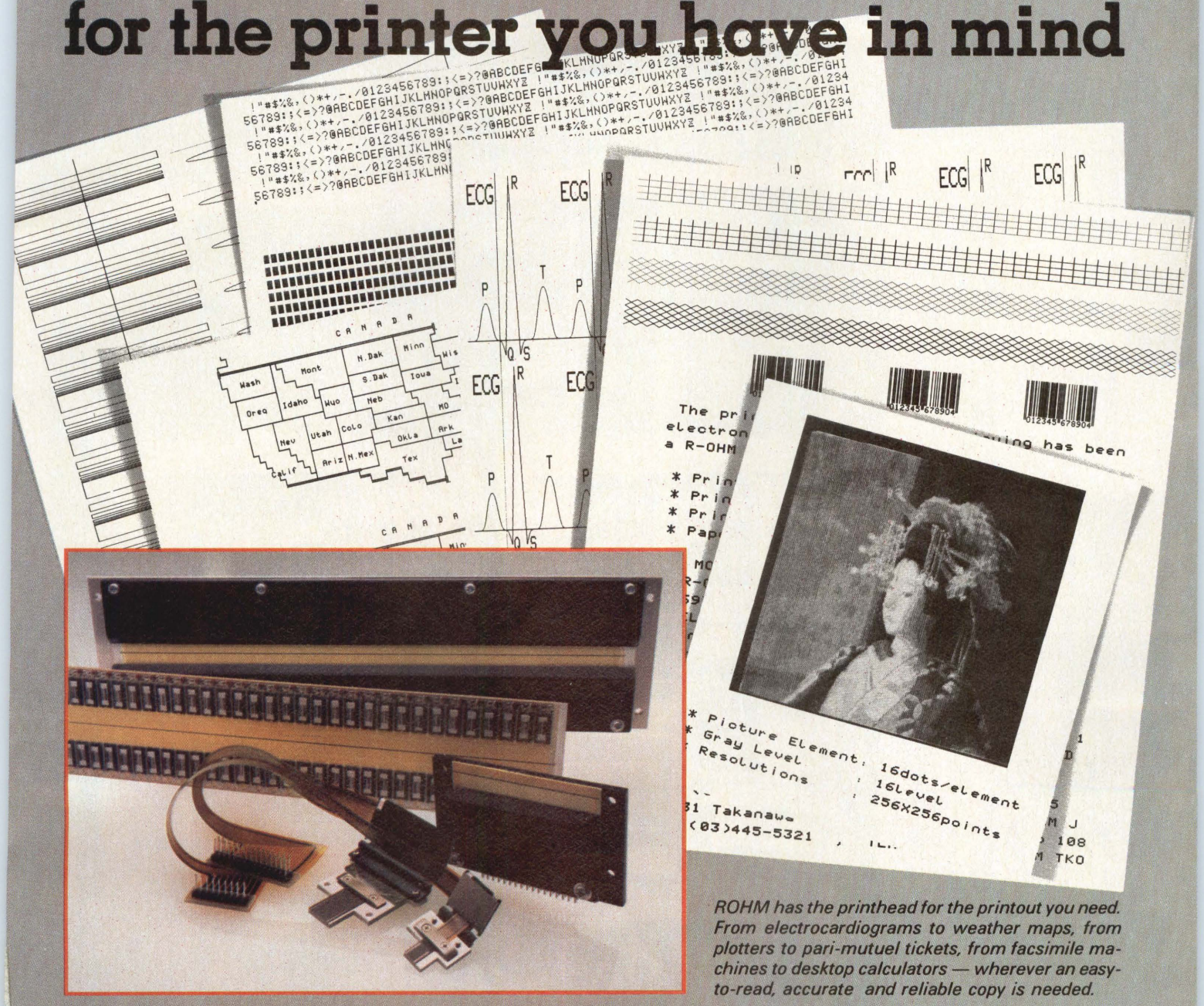
Instruction sets are implemented in microcode located in a high speed control store. The control store has 8k 32-bit words of loadable storage and 1k words of read-only storage. The IPU features a 2-stage pipeline that allows it to fetch the next instruction while it executes the current instruction.

Extended 32-bit addressing mode, used primarily by the operating system, allows access to the entire virtual memory space. Efficient virtual to physical address translations are accommodated by 1024 map registers residing in high speed 32-ns access bipolar RAMs.

Each processor module contains a separate processor dedicated to I/O operations. Because the I/O processor operates independently from the IPU, transfers are efficient and require a minimum of IPU intervention. Every I/O device controller is buffered, allowing transfers between main memory and the controller buffer to occur at full memory speed. The high speed I/O channels use burst multiplexed direct memory access to provide transfer rates of up to 5M bytes/s; thus the aggregate burst I/O rate of a fully configured 16 processor system is 80M bytes/s.

All processors are interconnected by the Dynabus. This provides two independent high speed (up to 13M bytes/s/bus) communications paths among the system's processors, with a potential communications bandwidth of up to 26M bytes/s. Transfers over the bidirectional bus use a multiplexed packet interleaved protocol to maintain high speeds. Messages ae sent in 16-byte packets and can be up to 32k bytes in length. Each packet is protected by a checksum with automatic retransmission if an error is detected. Using the Dynabus rather than the I/O channels for interprocessor communication improves system performance and leaves the I/O channels available to application programs. **Circle 350 on Inquiry Card**

# ROHM has a thermal printhead for the printer you have in mind




*ROHM has the printhead for the printout you need. From electrocardiograms to weather maps, from plotters to pari-mutuel tickets, from facsimile machines to desktop calculators — wherever an easy-to-read, accurate and reliable copy is needed.*

ROHM has developed a complete line of standard printheads for all types of thermal printing requirements. These high speed, high resolution line and serial printheads set new standards for reproduction quality and reliability and are available now to meet your specific applications.

ROHM line printheads are available with print widths to 10 inches, densities to 8 dots/mm (200 dots/inch) and line print speeds to 2 mS. Drive circuits, shift registers and diode matrices are mounted in IC form on the substrate to keep things simple, save space and improve reliability (MDLBF is $100 \times 10^6$). These units come ready to install, complete with heat sink and platen guide and with all connections terminated in a standard edge connector.

For serial applications we offer a full line of heads that achieve print speeds of 120 to 150 cps and life expectancies of 150 million characters or more.

These standard configurations can be customized to match your specific requirements. For more information, contact:

**ROHM CORPORATION**
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(714) 546-7750, TWX: 910-595-1721
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ROHM

CIRCLE 137 ON INQUIRY CARD

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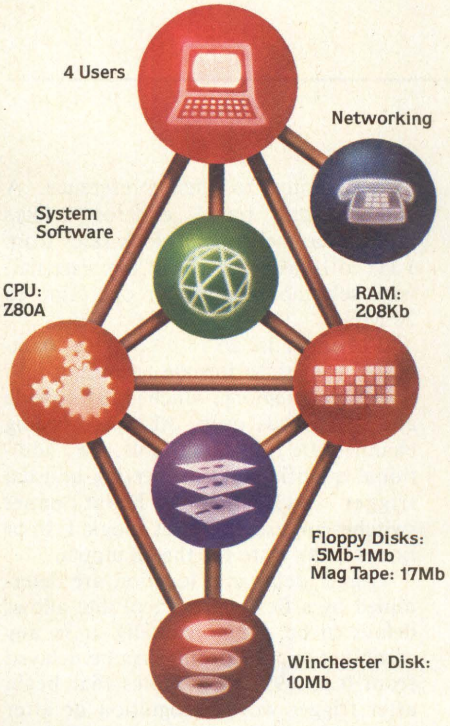
# BUMPER CROP

## 8-inch Winchester Multi-User Systems. Now In Volume- $8,500.

Altos is delivering the cream of the crop with their new 8-inch multi-user Winchester disk systems. They're freshly packed with the quality features you expect from Altos, and at a price you expect from Altos, too—just $8,500.

Pick from two fully integrated systems, each packaged in our new compact, stylish cabinet suitable for either rack mount or table top applications. You get 10 MBytes of reliable on-line storage in our 8-inch Winchester drives. Then for system back-up storage, you can select from either 8-inch, single or double-sided floppy drives (ACS8000-10 and -10D) or a ¼-inch magnetic tape drive (ACS8000-10/MTU). And for powerful performance, all of these Z80A*based systems come complete with 208K of RAM and 6 programmable serial ports, ready to support four users.




SYSTEMS PICTURED:

| | |
|---|---|
| ACS8000-10 (10Mb HD + 1 floppy) | $ 8,500 |
| ACS8000-10/MTU (10Mb HD + DEI Mag Tape) | $10,990 |

Here's the most bountiful selection of systems and capacities in the field from the company that knows how to deliver quality systems in the volumes that OEMs need to stay competitive.

And Altos supports these systems with a broad software selection including the three industry standard operating systems—CP/M, multi-user MP/M** and OASIS†. These operating systems support seven high level programming languages: BASIC, FORTRAN, COBOL, PASCAL, APL, PL/1 and C. Also available are comprehensive communications packages: ASYNC—Altos-to-Altos, BISYNC—Altos-to-mainframe and full networking with CP/NET. All are designed to run on a high speed 800 Kilobaud networking channel—standard with every system.

The ACS8000-10 Winchester systems join our growing family of field-proven products. In just three years, more than 8,000 systems have been shipped to an OEM customer-base.

Get to market fast. Harvest your 8-inch Winchester system direct from the heart of Silicon Valley. Call or write today for specific product information and OEM pricing. Altos Computer Systems. 2360 Bering Drive, San Jose, CA 95131, (408) 946-6700, Telex 171562 ALTOS SNJ.

## Packed with Fresh Ideas

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COMPUTER SYSTEMS

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CIRCLE 139 ON INQUIRY CARD

## 4½-digit intelligent multimeter offers full complement of facilities

As a multimeter, the portable 6504 offers a 5-range measurement of dc and ac voltage and current, with true rms ac sensing, and 6-range measurement of resistance. Basic accuracy of ±0.03% ±2 digits and wideband ac frequency response (to 20 kHz) place it in the forefront of its class. The intelligent instrument, developed by Weston Instruments, Inc, 614 Frelinghuysen Ave, Newark, NJ 07114, has automatic self-checking routines to make operating procedures accurate and foolproof. The few pushbutton keys required for computation control are grouped with the instrument's range and function controls and large LCD readout display on a panel measuring 8.5 x 3″ (21.6 x 7.6 cm).

Any combination of six basic computing modes is selectable by panel pushbutton keys: filter, null, scale/offset, percent deviation, max/min monitoring, and hi/lo limits. All measurements are scaled by the frontend circuits to ±4-V full-scale, and are applied to a dual-slope A-D converter. All inputs to the converter are first routed through a gain controlled preamplifier. Current measurements are made by converting current to voltage via range switching current shunts. For dc current measurements, the resulting dc voltage is routed directly to the preamplifier. For ac current measurements, the ac voltage developed across the current shunts is first applied to an ac converter and from there to the preamplifier.

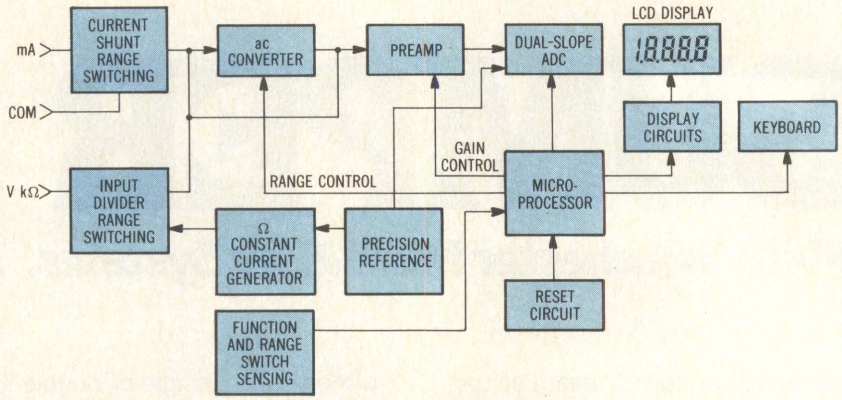
Voltage inputs are fed to an input divider for scaling. Scaled dc voltages are then applied to the preamplifier. Ac voltages are first routed to the ac converter as described for ac current operation.

Resistance is converted to dc voltage by a constant current generator that sinks a known value of current through the resistance in accordance with the selected range. The constant current generator derives its reference from the A-D converter reference. The precise input divider resistance is used as a reference resistance in the constant current generator.

All measurements and resulting displays are controlled by the microprocessor. In addition to displaying numeric readings and stored values, the LCD readout provides a man/machine interface that maintains continuous communications with the operator through its self-diagnostic ability and 8-word prompting vocabulary. Computing modes in use are also displayed, and flashing symbols distinguish between stored register values and realtime readings; a flashing data signal appears when data entry is required.

A rechargeable battery that enables complete instrument operation for up to 8 hours without ac power is a standard option. Also optional is an IEEE 488 interface bus that permits the instrument to be used with automatic test and data acquisition systems. A series of probes is also available to extend measurement capabilities and utility of the unit.

**Circle 366 on Inquiry Card**




Weston's 4½ digit multimeter model 6504 provides wide ac bandwidth in both average and rms sensing modes. All measurements and displays are controlled by internal microprocessor which also supplies intelligence for prompting and result computation

## 16-channel logic analyzers operate to 20 MHz to aid microcomputer development

The 16-channel LA-1020 logic analyzer and LA-1025 digital system analyzer from B&K-Precision, Dynascan Corp, 6460 W Cortland St, Chicago, IL 60635, monitor logic activity in complex digital circuits under test, and process and display captured data to permit rapid analysis of circuit activity. Designed for use in the design and development of microcomputers and microcomputer based products, the instruments present data in both state and time domains.

State data are formatted in binary, octal, decimal, or hexadecimal codes on the integral 12-digit LED display. Timing diagrams of 16 channels by 16 words can be displayed externally on most conventional oscilloscopes. Clock pulses and cursor are also displayed on the scope, permitting both hardware and software designers to display information in a format suited to their preference. A single front panel control selects internal, asynchronous clock rates from 1 Hz to 10 MHz or one of two external, edge selectable clocks for operation to 20 MHz.

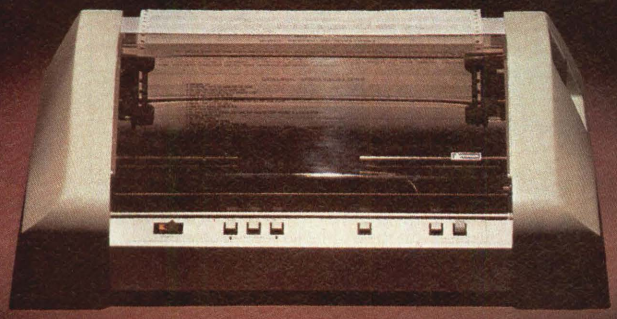
Both units use an 18-bit pattern recognition trigger to initiate recording into the system memory, which is 16 bits wide and 250 words deep. All 16 recording channels are fully qualifiable. Two additional qualifiers aid in meeting unusual trigger requirements. Front panel switches are used to select a logic 1, 0, or DON'T CARE state for the 18 inputs.

Trigger delay and location are determined by a flexible protocol that allows delays to be set individually or in any combination. Recording can be delayed from 0 to 999 clock pulses that begin after trigger word recognition or after the last event delay occurrence. Trigger word location may be established anywhere within the 250-word memory,

*(continued on page 48f)*

# The important plus in matrix printers:

# grafixPLUS.™



Since their introduction in mid-1980, the Anadex high-resolution DP-9500 Series matrix printers have set new standards for printer quality and performance. All models feature the rugged Anadex 9-wire print head that combines long life with resolutions of 72 dots/inch vertical and up to 75 dots/inch horizontal. With this kind of resolution, fineline graphics (under data source control) and razor sharp characters are pluses built into every printer.

**Performance Plus**

The full standard ASCII 96 character set, with descenders and underlining of all upper and lower case letters, is printed bi-directionally, with up to 5 crisp copies, at speeds up to 200 CPS. Models DP-9500 and DP-9501 offer 132/158/176 and 132/165/198/220 columns respectively. Print densities are switch- or data-source selectable from 10 to 16.7 characters/inch. All characters can be printed double-width under communications command.

**Interface Plus**

Standard in all models are the three ASCII compatible interfaces (Parallel, RS-232-C, and Current Loop). Also standard is a sophisticated communications interface to control Vertical Spacing, Form Length and Width, Skip-Over Perforation, Auto Line Feed, X-On/Off, and full point-to-point communications.

**Features Plus**

As standard, each model features forms width adjustment from 1.75 to 15.6 inches, shortest-distance sensing, full self-test, 700 character FIFO buffer (with an additional 2048 characters, optional), and a quick-change, 6 million character life ribbon.

**Quality Plus**

Beyond the built-in performance of the grafixPLUS series printers, the engineered-in quality and support are equally important. The result? Approval of both UL and FCC, Class A; operating noise levels under 65dbA; and a nationwide service organization second to none.

To see for yourself why the grafixPLUS printers offer more pluses for your printing dollar, contact us today.

Anadex®
the plus in printers

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CIRCLE 140 ON INQUIRY CARD

# Now RCA CMOS bursts into color.

## New video interface Microboard has all you need to design a custom terminal.

**For the first time; a CMOS Microboard with:**

- up to 128 user-programmable characters
- 8 programmable colors, or
- black and white display
- audio output for tones or white noise
- parallel input port for keyboard
- graphics and motion
- NTSC and PAL versions.

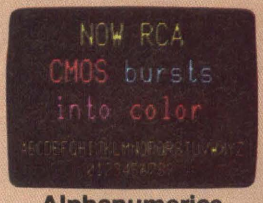
**So you can:**

- program graphs, charts, messages
- get any combination of sounds
- add a keyboard for human interaction
- use it with any RCA Microboard computer
- use our optional programming design aid, the VIS interpreter (CDP 18S835).

**Plus,** you get all the advantages of CMOS, making it ideal for industrial controls.

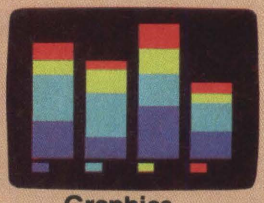
For more information on the CDP18S661, contact any RCA Solid State sales office or appointed distributor. Or contact RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Hong Kong. Sao Paulo, Brazil.

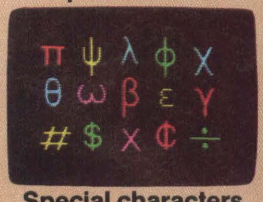
**Or call Microsystems Marketing toll-free (800) 526-3862.**



Alphanumerics.

Color.


Graphics.


Special characters.

Overlay.

Programmed sound.

**Another reason to switch to CMOS.**

RCA

48f

CIRCLE 141 ON INQUIRY CARD




providing pre-, post-, and variable pre/post trigger recording.

An event pulse output provided by the analyzers increases versatility. The event output of one analyzer can be connected to the qualifier input of a second unit, expanding the system to 32 channels at speeds up to 10 MHz.

The LA-1025 offers added signature analysis capability. Circuits are tested using a data probe and control pod which connect directly to the logic analyzer. Signatures are displayed in the most widely used industry coding for modified hexadecimal format. The unit is also capable of recording the occurrence of unstable or abnormal signatures.

The units are interfaced to the circuit under test through two TTL compatible model LP-1 probes; LP-2 probes are available for use with CMOS circuits. The optional model LP-3 increases trigger capability by adding 16 qualifiers.

**Circle 367 on Inquiry Card**

## Daisywheel printers improve output quality using direct drive mechanism

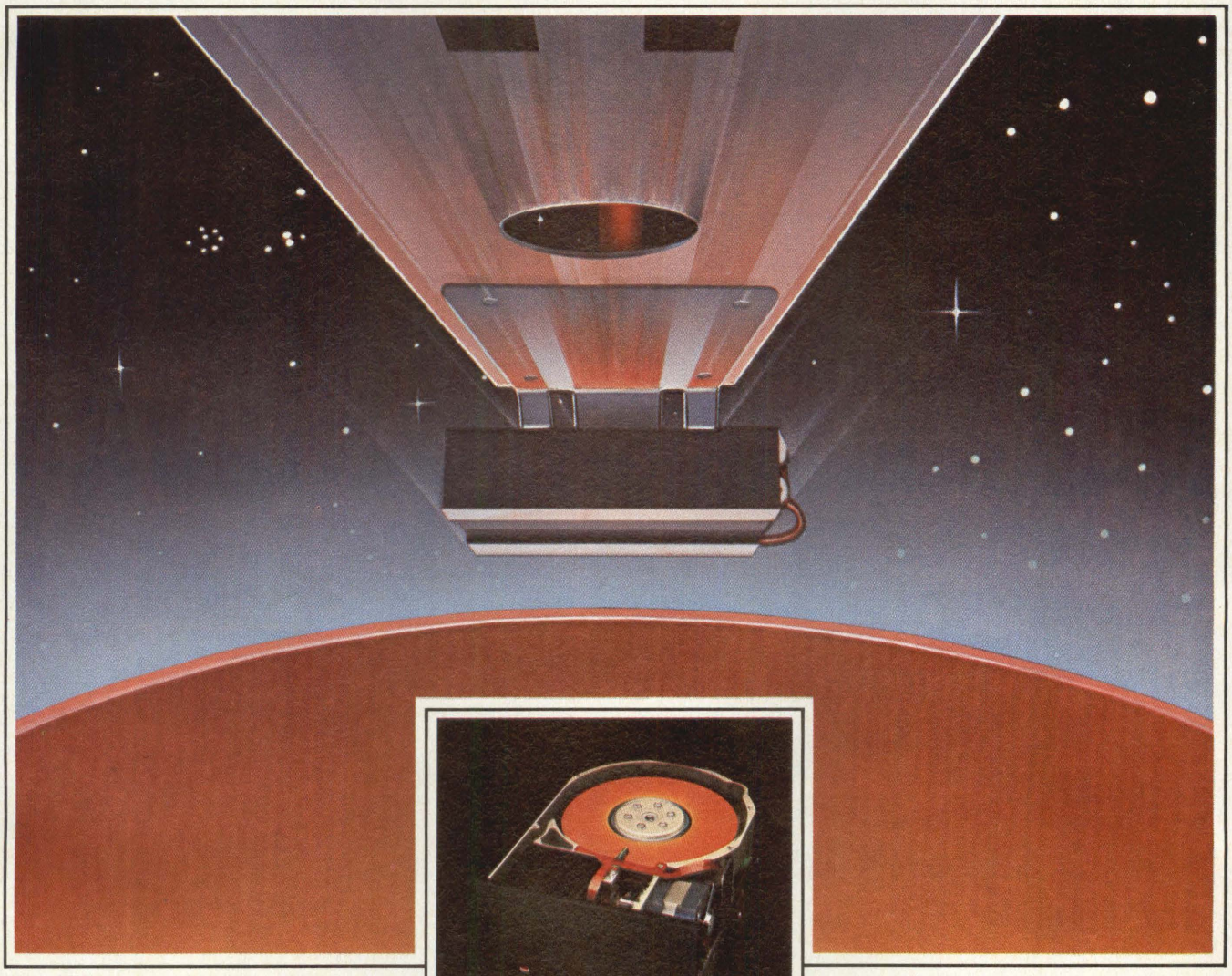
Sprint 7™ letter quality printer and Sprint 9 printing data terminal replace the steel drive cable and pulleys customarily used in daisywheel printers with a MicroDrive™ mechanism to offer better print accuracy and reliability. An important part of this innovation from Qume Corp, 2350 Qume Dr, San Jose, CA 95150, is a direct drive system using a custom drive belt made of DuPont Kevlar®, that reduces chassis stress and results in longer life and superior print quality.

The units offer print speeds of 45 or 55 chars/s. Improvements over earlier models include 30% fewer parts, an internal power supply, and simplified service access. MTBF has been increased to 3000 hours, and acoustic noise level has been reduced to 65 dBA maximum.

The terminal version uses the industry standard RS-232-C interface to plug directly into most minicomputers, and provides all current word processing functions. It offers a superset of the Sprint 5 command set with enhancements that include automatic logic seeking bidirectional printing.

**Circle 368 on Inquiry Card**

# Thin is in!



**Seagate Technology announces another first. The inventor of the 5¼-inch micro-Winchester™ now brings you thin film heads and 12.76 megabytes on just two platters — double the capacity of current ferrite head drives.**

**The new ST512 micro-Winchester** with thin film heads stores 10202 bits per inch and doubles the number of tracks from 612 to 1224. Increased bit packing permits recording closer to the disc center and eliminates the need for write precompensation.

**No change in form factor or interfacing.** The ST512 doubles storage capacity without changing your system configuration. Size and shape exactly match Minifloppy and ST506 micro-Winchester. Just as important, the ST512 uses the same recording format, 5 MBits/sec. data transfer rate and DC voltages. You can use the same interface and power supply.

**Think what ST512 could do for your system.** Perform interactive, on-line jobs without being disc limited. Offer faster random access to inventories and other long listings. Run prompt-driven tutorials and other large disc-based programs. Share storage resources in local networks. Serve faster 16 and 32-bit machines. In short, provide faster access to more storage in less space.

For complete specifications, circle our readers' service number. To order an evaluation unit, write, telex or phone.

**Seagate Technology**

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East Coast Sales Office: P.O. Box 137 Allamuchy, New Jersey 07820 (201) 852-6184

**"Turning the tide in fixed disc technology"**

™micro-Winchester is a trademark of Seagate Technology

CIRCLE 142 ON INQUIRY CARD

# GET A CLEAR HONEST IMAGE THE HITACHI WAY!

Computer data and graphic displays never looked better, brighter, sharper.

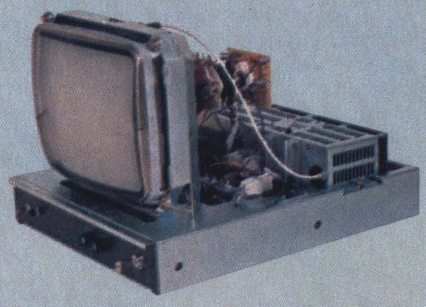
New Hitachi high resolution in-line RGB color monitors utilize wide video bandwidth and a 0.31 mm spacing between triad pairs. The result? A trio-dot density **twice that of conventional monitors!**

**Look at these advanced features**

Adjustment-free convergence, single PCB configuration, video amplifier bandwidth from 50 Hz to 25 MHz. Flexible frequencies range from 15 to 18 KHz horizontal and 50 to 60 Hz vertical. Monitors provide high contrast and brightness from black matrix and 85% light transmission tubes. Can any other maker match these advantages?

**Variety of Screens**

You can select from a wide choice of screens to meet your specific application needs: Normal phosphor; long persistence phosphor to virtually eliminate flickering, or medium resolution versions for most ambient light situations.



**Unsurpassed performance**

Long time convergence stability is assured due to self convergent in-line guns and **single PCB reliability.** Operator controls include power on/off, degauss, brightness, contrast.

Call or write for more information.

**Hitachi America, Ltd.**

100 California Street, San Francisco, Calif. 94111 Tel: (415) 981-7871
**New Jersey Office:** 6 Pearl Court, Allendale, N.J. 07401 Tel: (201) 825-8000

CIRCLE 143 ON INQUIRY CARD

# THE BROADEST LINE OF MINICOMPUTER STORAGE SYSTEMS IN THE WORLD.

# DATUM MADE 'EM.

Made 'em available to you. So that you can get the increased performance you've been looking for.

How many times have you wondered where you can get the kind of storage that would really enhance your computer performance? And how many times have you wondered why you couldn't get that from the original manufacturer?

Well, when it comes to minicomputer storage systems, you won't find a more reliable source than Datum.

## WE'D LIKE YOU TO MEET OUR FAMILY.

One of the greater limitations of the minicomputer is memory capacity. That's because as a "smaller computer," the mini has very real limitations on the amount of resident memory. And that's why a company like Datum is dedicated to the development of reliable nonresident memory products. Our outstanding product family includes several standouts that make minicomputers more manageable.

Our clan includes controllers, drives and integrated systems. Our tape/disk controllers and tape/disk drives could make all the difference for your minicomputer. And they're compatible with DEC, Data General, HP, IBM Series 1, Interdata and Sperry Univac systems.

What's more, when you're in the market for minicomputer storage, you don't have to shop around, piecemeal. Because our family has it. All of it. We're price competitive and interested in doing volume business both large and small.

## NOW MEET THE WHOLE FAMILY.

To tell the truth, there's more to our family than just product. There's people, too.

Our people provide you with excellent service from start to finish. From sales and application/technical support to on-site installation. And our maintenance program services all Datum products. Nobody serves you like the people from Datum.

## WE MAKE TRANSPARENT CLAIMS.

Datum products are software transparent. That means, when you buy from Datum, your purchase will be totally compatible with your present system. As well as your future system, should performance requirements change.

And it won't require you to turn your operation upside down. There's no point in making a capital investment that won't cooperate.

In fact, Datum is the expert in minicomputer storage products. So when your computer system needs its performance increased, don't call a general practitioner. Call a specialist. Because we can diagnose your application requirements, prescribe a solution and come up with the cure better than just about anybody else.

But what's so unusual about that? After all we're specialists. The minicomputer storage specialists.

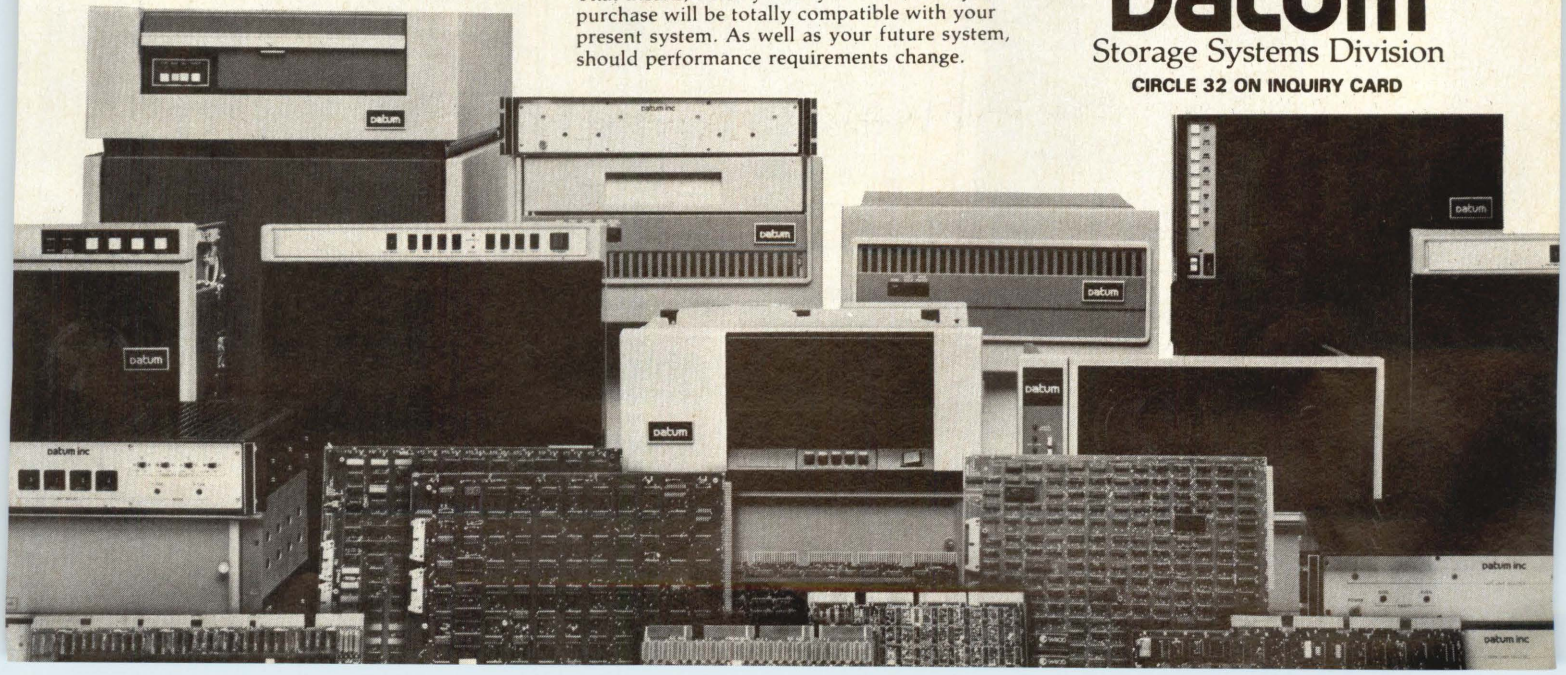
Why not call us today for a free checkup?

Datum, Inc., Corporate Headquarters: 1363 South State College Blvd., Anaheim, California 92806. Telephone: (714) 533-6333, Ext. 207, TWX: (910) 592-1289, Telex: 68-5579.

**Toll Free: 800/854-4600** (Outside California)

**datum**
Storage Systems Division

**CIRCLE 32 ON INQUIRY CARD**



# DEC does not offer these products for your PDP-11. Only Able does.

## THE ABLE GENERAL-PURPOSE SERIES

Provides a wide range of practical and exclusive solutions to problems facing the PDP-11 user.

QNIVERTER™ opens the wonders of the UNIBUS world to PDP-11/23 & LSI users, or lets Q-bus devices be compatible with any PDP-11.

### QNIVERTER™

(Q-BUS TO UNIBUS CONVERTER OR UNIBUS TO Q-BUS CONVERTER)

**INSTALLS IN:** LSI-11, LSI-11/23, PDP-11/03 and PDP-11/23 via quad-width card. **APPLICATIONS:** Allows Unibus-compatible controllers and memories to be used with LSI computer systems, or LSI-based peripherals to be used with PDP-11 computer systems. **FEATURES:** Supports features of LSI-11/23 including the full 128K address capability.

REBUS™ meets or exceeds all DB11 performance specifications, fits *in-line* with UNIBUS cable using *no additional* backplane space.

### REBUS™

(BUS REPEATER – DB11 REPLACEMENT)

**INSTALLS IN:** All PDP-11's; without using any additional backplane space. **MECHANICAL:** One dual-width card plugs into the same pair of connectors as the Unibus extension cable which is then plugged into the REBUS connectors. **COMPATIBILITY:** Allows for 18 additional bus loads and 50 foot bus extension. Requires no software changes. Bus cycle time unaffected for devices on CPU side of REBUS – increased by 250 nsec max. for devices on outboard side.

BUSLINKS, unlike the DEC DL11-W, are software compatible with the original DA11-B driver.

### BUSLINK/UNI, LSI OR U TO Q

(CPU TO CPU LINK: UNIBUS TO UNIBUS, UNIBUS TO Q-BUS OR Q-BUS TO Q-BUS)

**INSTALLS IN:** All PDP-11's and/or LSI-11's via pairs of hex-width, hex/quad-width, or quad-width cards and supplied cables. **APPLICATION:** Provides full DA11-B (Unibus or Q-bus link) compatibility on single cards. BUSLINK operates at DA11-B transfer rates over distance of up to 50 feet. **OPERATING ADVANTAGE:** Requires only one card per CPU to effect link at minimal bus loading vs. full system unit per computer.

EMULOADER™ boots all the latest peripheral devices and provides the only fixed console emulator for early PDP-11's.

### EMULOADER™

(ODT/BOOTSTRAP LOADER REPLACEMENT)

**INSTALLS IN:** PDP-11/05, -11/10, -11/35, -11/40, -11/45, -11/50 and -11/55. **MECHANICAL:** Dual width card replaces standard Unibus termination; requires no additional backplane space. **OPERATING ADVANTAGE:** Provides fixed console emulator (ODT) and bootstrap loaders for DL11, PC11, RF11, RK06, RK11, RP04/05/06, RP11, RS03/04, RX11, TC11, TM11 and TU16. **SPECIAL FEATURE:** Performs memory diagnostic each time a boot operation is done from ODT.

DUAL I/O™ provides two full DR11-B DMA interfaces but takes half the space and exhibits only one bus load.

### DUAL I/O™

(GENERAL INTERFACE-DR11-C REPLACEMENT)

**INSTALLS IN:** All PDP-11's; in any SPC slot via quad-width card. **APPLICATION:** Dual I/O is equivalent to two (2) DR11-C's and provides the logic for program-controlled parallel transfer of 16-bit data between two (2) external user devices and a Unibus system. **OPERATING ADVANTAGE:** Provides user the hardware/software equal to a dual DR11-C in one-half the space and one-half the bus loading of DR11-C's.

INTERLINK provides DMA interface and can function as one side of a high-speed, half-duplex BUSLINK.

### INTERLINK/UNI

(DR11-B AND ½DA11-B REPLACEMENT)

**INSTALLS IN:** All PDP-11's in any SPC slot via hex-width card. **APPLICATIONS:** Provides full DR11-B (DMA INTERFACE) and one side of DA11-B (UNIBUS LINK) capability on a single card. **OPERATING ADVANTAGES:** Requires only one hex-width card in each computer to effect link vs. full four-slot system unit per computer. Exhibits one bus load. Directly software transparent as a DR11-B replacement or when expanded to DA11-B equivalency.

Every product is designed exclusively for implementation in PDP-11 and LSI-11 computers. Each is software compatible to the diagnostic level and sells for less but does more than the competitive product it is intended to replace. Ask for more information. We'll tell you all about the *general-purpose* series as well as our *special memory* and *communications* products, all of which currently ship within 30 days ARO. Remember, we have a veritable store of DEC computer enhancements. They are all unique, and they all help you get more out of your present computer.

## Able, the computer experts

ABLE COMPUTER, 1751 Langley Avenue, Irvine, California 92714. (714) 979-7030. TWX 910-595-1729.

ABLE COMPUTER-EUROPE, 74/76 Northbrook Street, Newbury, Berkshire, England RG13 1AE. (0635) 32125. TELEX 848507 HJULPHG.

CIRCLE 33 ON INQUIRY CARD

## Prototype text to speech system has unlimited English vocabulary

Model TTS-X is a complete standalone unlimited speech peripheral device. Developed by Telesensory Speech Systems, 3408 Hillview Ave, PO Box 10099, Palo Alto, CA 94304, this system consists of 2 wirewrap and 10 printed circuit boards mounted in a card cage. Components mounted on these boards include one 8085 and two LSI-11 microcomputers, RAM, and programmable digital signal processor chips. The card cage, power supply, speaker, and tape cartridge are packaged in an enclosure with external user controls mounted on the front panel; RS-232-C connectors used for I/O are on the back panel.

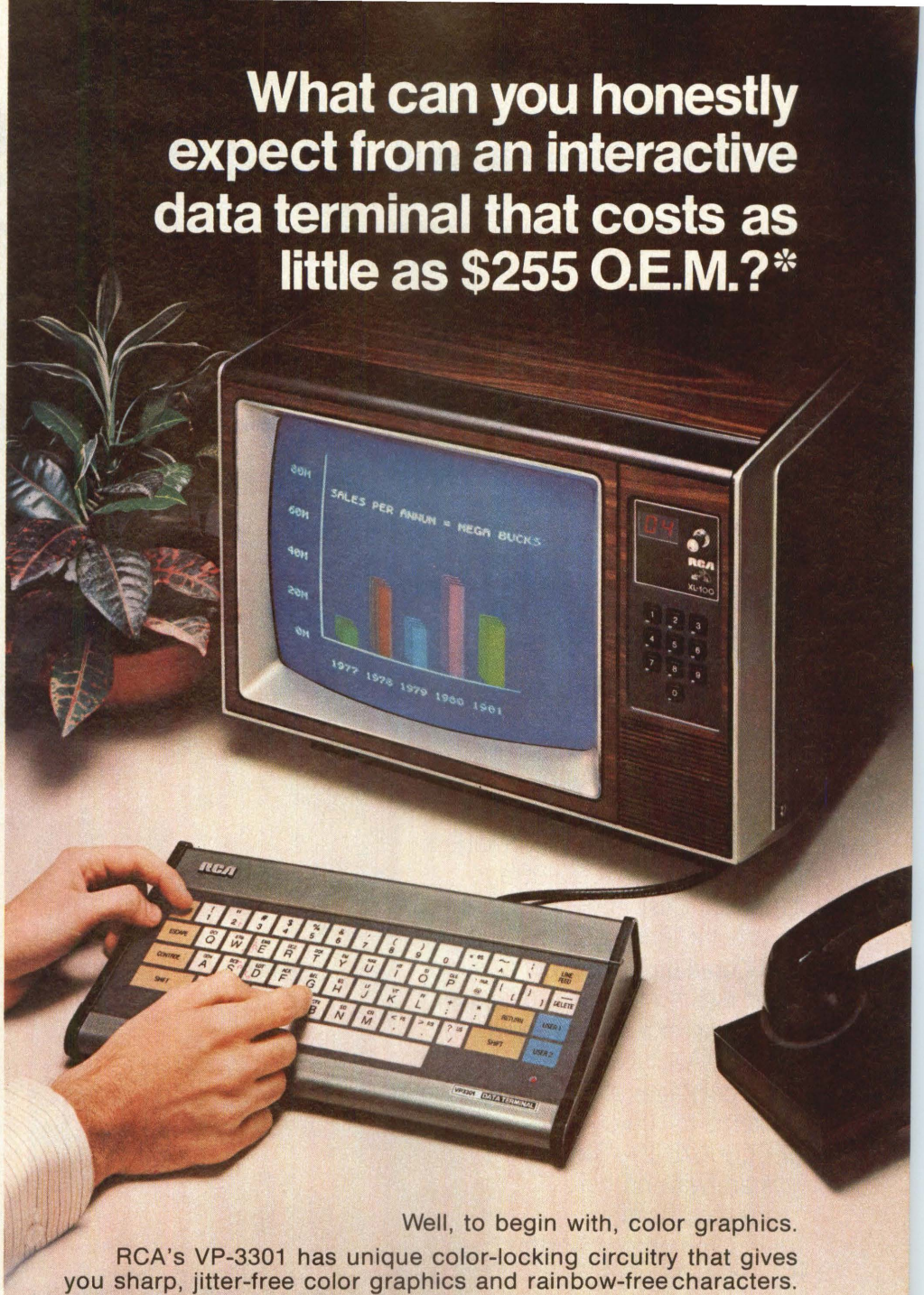
The system receives full words as strings of characters in ASCII format. These words are spoken in either lexical, prosodic, or spell mode. In lexical mode each word is pronounced with full normal stress (based on the lexical stress rules for words) without regard to the surrounding words. Prosodic mode more closely resembles human speech in conversation; an entire phrase is analyzed before speech begins, and each word is stressed with relationship to the surrounding words. Spell mode names each character in the input string. Mode of operation is selected by ASCII input control characters.

Incorporating a dictionary of 1500 exceptional words, the device speaks an unlimited English vocabulary. The dictionary contains words that are most common in the English language and those that do not follow the typical phonetic rules of the language. Along with this dictionary is a set of algorithms that convert other words to phonemes. A phonetic synthesis subsystem converts the resulting phoneme, stress, and duration data to speech parameters which drive the proprietary PDSP synthesizer to create synthetic speech.

If operated in lexical or prosodic mode, the system can speak indefinitely at a maximum rate of 200 words/min. Speech rate is controlled from a front panel switch. Text input is an ASCII format at 1200 baud based on RS-232-C specifications. The external user's control consists of variable speech rates between 50 and 200 words/min, and volume control. Power requirements are 110 V, 60 Hz, 4 to 5 A.

**Circle 351 on Inquiry Card**


# What can you honestly expect from an interactive data terminal that costs as little as $255 O.E.M.?*




Well, to begin with, color graphics.

RCA's VP-3301 has unique color-locking circuitry that gives you sharp, jitter-free color graphics and rainbow-free characters.

Plus much more: Microprocessor control. Resident and programmable character set. Reverse video. State-of-the-art LSI video control. 20 and 40 character formats. RS232C and 20 mA current loop. Six baud rates. Eight data formats. ASCII encoding. Light-touch flexible-membrane key switches for reliability and long life. CMOS circuitry and a spill-proof, dust-proof keyboard for hostile environments.

The VP-3301 can be used with a 525-line color or monochrome monitor or a standard TV set through an RF modulator.** It serves a wide variety of industrial, educational, business and individual applications including communication with time sharing and data base networks.

All this—for as little as $255. And it's made by RCA. So get the whole story about the surprising VP-3301 today. Write RCA MicroComputer Marketing, New Holland Avenue, Lancaster, PA 17604. Or call toll-free: 800-233-0094.

**Model VP-3303 with *built-in* RF modulator—$270. O.E.M.
*Quantity price. Monitor and modem not included.

RCA

CIRCLE 34 ON INQUIRY CARD

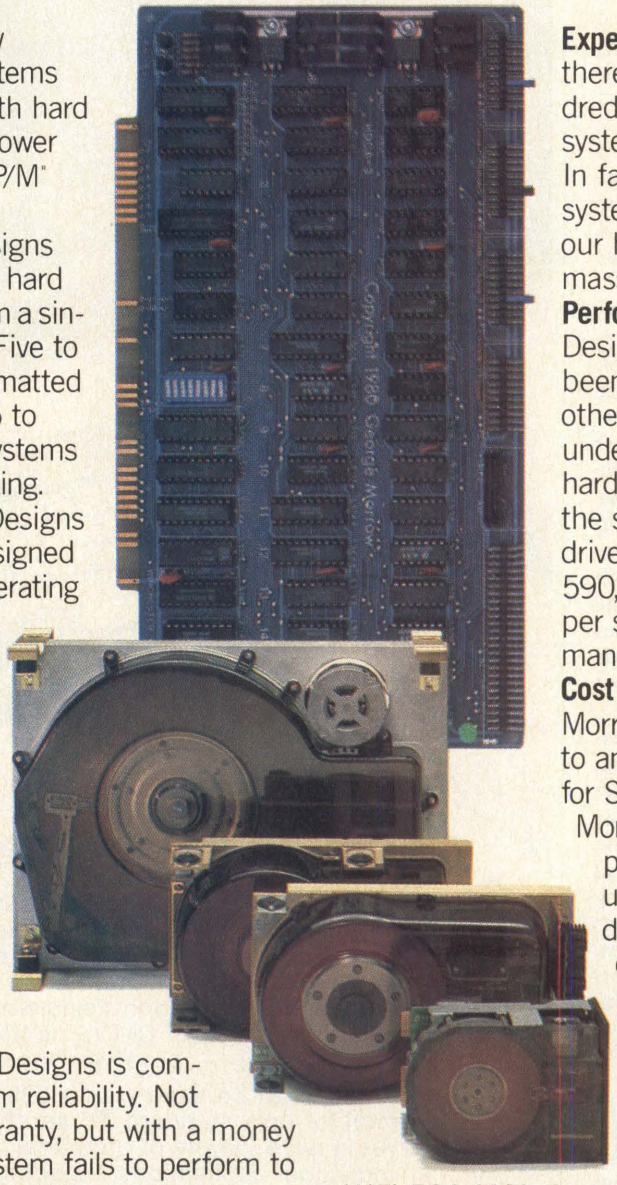
# MORROW DESIGNS

## Leading edge technology in hard disk systems.

**Complete systems.** Morrow Designs hard disk subsystems are delivered complete with hard disk, controller, cabinet, power supply, fan, cables and CP/M* 2.2 operating system.

**Widest range.** Morrow Designs offers the widest range of hard disk systems available from a single supplier. 5¼," 8," 14." Five to over 100 megabytes of formatted hard disk storage. $2,995 to $19,980. Cost effective systems that work. And keep working.

**S-100 and more.** Morrow Designs hard disk systems are designed for use with the CP/M operating system. Available software packages allow our systems to run on any IEEE696/S-100 Standard system with no hardware modification. Plus, Cromemco,† North Star,** Vector Graphics, Godbout, Dynabyte, Exidy,†† IMSAI, Micromation, Processor Technology and California Computer Systems.



**Reliable systems.** Morrow Designs is committed to hard disk system reliability. Not simply with a 90-day warranty, but with a money back guarantee. If our system fails to perform to specification, send it back. We'll send back your money.

**Experience.** As of April, 1981, there were over fifteen hundred Morrow Designs hard disk systems successfully installed. In fact, over 200 independent systems integrators now use our hard disks to solve their mass storage problems.

**Performance answers.** Morrow Designs hard disk systems have been benchmarked against all other systems. None is faster under CP/M. Morrow Designs hard disks operate at 10 times the speed of a floppy disk drive. Transfer rates range from 590,000 bytes to 900,000 bytes per second. That kind of performance can become addictive.

**Cost effective answers.** Compare Morrow prices and performance to anything presently available for S-100 systems. You'll find Morrow's price/megabyte/performance ratio to be unmatched. Leadership in disk systems technology earned us leadership in price/performance. And that may have earned us a call from you. Circle the Reader Service Number for our full line data sheets. Can't wait? Call us at (415) 524-2101. And yes, OEM quantity prices are available. **LOOK TO MORROW FOR ANSWERS.**

*CP/M is a trademark of Digital Research.
**Northstar is a trademark of North Star Computers, Inc.
†Cromemco is a trademark of Cromemco, Inc.
††Exidy is a trademark of Exidy Corporation.

**MORROW DESIGNS**

5221 Central Avenue, Richmond, CA 94804
(415) 524-2101

**CIRCLE 35 ON INQUIRY CARD**

## 10M-byte removable cartridge subsystem based on flexible media

ALPHA 10, a 10M-byte removable cartridge storage subsystem, is based on a technique for high density recording on flexible media. The unit, developed by Iomega Corp, 4646 S 1500 West, Suite 160, Ogden, UT 84403, includes disc drive, integrated controller, and 10M-byte flexible media cartridge. The subsystem package, including controller, fits in the envelope of a standard 8″ (20-cm) flexible disc drive.

A media stabilization system is used to enable the flexible media to fly close to the head, resulting in high density noncontact recording. Embedded servo and parity sector error correction further enhance the high density and data reliability achieved with the technology.

Competing favorably with Winchester products in the same capacity range, the unit's average access time of 35 ms is achieved by a simple PCB rotary actuator. A brushless dc drive motor spins the media at 1500 r/min resulting in a 1.1M-byte/s transfer rate.

**Circle 352 on Inquiry Card**

## I/O subsystem provides 64M-bytes buffer memory, streaming data channels

An enhanced I/O subsystem provides up to 8M words (64M bytes) of buffer memory, dual high performance channels for streaming data to central memory, and support for online magnetic tape. Developed by Cray Research Inc, 1440 Northland Dr, Mendota Heights, MN 55120, the unit meets the high throughput demands of the CRAY I/S supercomputer.

The I/O subsystem, with its multiple I/O processors, acts as a data concentrator for input to the CPU and distributes output from the CPU. In this role, it handles I/O for a variety of frontend computer systems and for peripheral devices such as disc units and user supplied magnetic tapes. An integral part of models S/1200 through S/4400, the I/O subsystem is composed of two to four I/O processors, buffer memory, disc control units (DCU-4s), optional block multiplexer control units (BMC-4s), three CRT consoles, and peripheral expander and maintenance peripherals.

The I/O processors all interconnect with each other and with buffer memory. Connecting to the CPU, to one to three frontend computer systems, and to maintenance peripherals via a peripheral expander, the master I/O processor handles communications protocol with other mainframes.

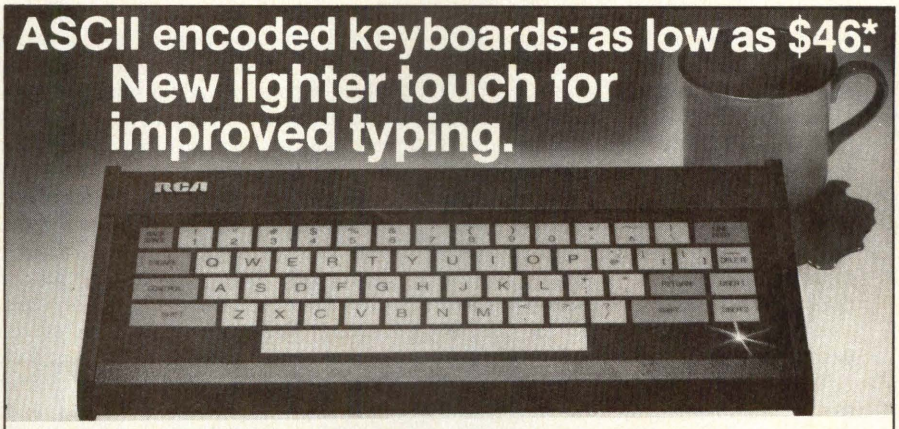
A second processor, the buffer I/O processor controls system disc storage and moves data between buffer memory and central memory and the CPU. This processor contains one to four DCU-4 disc controllers, each of which independently controls up to four DD-29 disc storage units. Each disc unit has a capacity of 600M bytes.

Optional third and fourth I/O processors each may support up to 16 additional disc units for a maximum system capacity of 28.8G bytes. As an alternative, one optional processor may contain 1 to 4 block multiplexer controllers. Each BMC-4 consists of four channels. Controller units for peripheral devices such as magnetic tape units may be connected to these block multiplexer channels.

Buffer memory is a solid state secondary storage unit, consisting of either 1M or 8M 64-bit words, that is accessible to all I/O processors in the subsystem. I/O processors connect to the buffer memory through internal channels capable of transfer rates of over 800M bits/s. Bandwidths of approximately 1250M and 2500M bits/s are possible between buffer memory and up to four I/O processors, depending on the number of banks (8 or 16) in the buffer memory.

**Circle 353 on Inquiry Card**


**ASCII encoded keyboards: as low as $46.* New lighter touch for improved typing.**




RCA VP-600 series ASCII keyboards are available in two formats. You can choose either a 58-key typewriter format. Or a 74-key version which includes an additional 16-key calculator-type keypad. Both can be ordered with parallel or serial output.

These keyboards, redesigned for lighter key activation and improved typing capability, feature modern flexible membrane key switches with contact life rated at greater than 5 milion operations. Plus two key rollover circuitry. A finger positioning overlay. And an on-board tone generator that gives aural key press feedback.

The unitized keyboard surface is spillproof and dustproof. This plus high noise immunity CMOS circuitry makes these boards particularly suited for use in hostile environments.

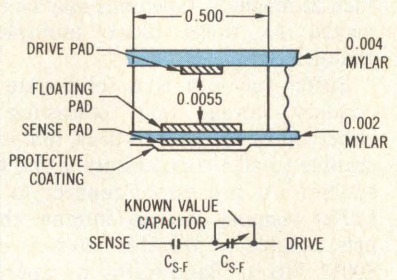
Parallel output keyboards have 7-bit buffered,TTL compatible output. Serial output keyboards have RS 232C compatible, 20mA current loop and TTL compatible asynchronous outputs with 6 selectable baud rates. All operate from 5 V DC, excluding implementation of RS 232C.

For more information contact RCA Customer Service, New Holland Avenue, Lancaster, PA 17604.
**Or call our toll-free number: 800-233-0094.**
*OEM price. Also available less case.

RCA

CIRCLE 36 ON INQUIRY CARD

## Full travel membrane keyboards seal switching elements within sandwich




Micro Switch's full travel membrane keyboard eliminates problems of stray capacitance by use of floating pad capacitor plates. Fixed capacitor formed between sense and float pads defines closed key capacitance; variable capacitor between drive and float pads senses key actuation

Using variations of membrane technology, sealed, full travel capacitance and contact keyboards and a flat touch panel keyboard protect the signal generating elements with unusual sealing and venting procedures. Micro Switch, a Honeywell Div, 11 W Spring St, Freeport, IL 61032, designed the keyboards for use in low cost terminals being introduced for industrial, commercial, and home applications. The combination of sealing, capacitor design, and shielding makes for an electronic unity that permits close tolerances, reduces impact of stray capacitance, simplifies circuit design, and improves overall reliability.

The sealed capacitance keyboard virtually eliminates unpredictable signal generation due to dust and moisture. Its patentable capacitive network provides the keyboard with superior overall performance characteristics.

Membrane keyboards are constructed from thin sheets of polyester film. Polymer ink networks of pads and connecting lines have been screened onto two of the Mylar sheets. These two plastic sheets are separated by a spacer sheet with cutouts corresponding to contact pad locations. Depressing a keytop brings the two screened ink networks together to generate appropriate signals.

Venting the keyboards relieves internal pressure built up during storage at temperature extremes or through multiple key actuation. Full travel keyboards use a 6-layer sealing sandwich for internal venting. This permits full sealing against fluids, moisture, and dirt. Arranged top to bottom, drive layer, spacer sheet, sense layer, pocket spacer sheet, flexible diaphragm, and second spacer sheet are bonded with adhesives to form the sealed unit. Total thickness of the sandwich is about 32 mils (0.8 mm). Air pressure changes in the switch cavities cause air to interchange through small holes in the sense layer to larger pockets in the first pocket spacer sheet. The diaphragm between pocket spacer sheets then flexes to normalize the pressure in the switch cavities.

The problem of stray capacitance has been minimized by using floating pad capacitor plates that fit between the normal screened on drive and sense pads. Drive pads (one per key) are inked onto the bottom of the top sheet of Mylar. Float and sense pads (one per key) are inked onto the upper and lower surfaces of the third layer of Mylar, with the float pads on top so that one float pad comes between every drive and sense pad. The three pads form two separate capacitors: a fixed capacitor between the sense and float pads, which accurately defines the closed key capacitance, and a variable capacitor between drive and float pads, which senses key actuation. During key actuation, the drive pad is pushed down through a hole in the spacer sheet toward the float pad, increasing the variable capacitance. The change in capacitance is detected by the sense circuit before the drive pad reaches the float pad. This permits electrical and physical overtravel with no bounce or teasing. Drive and sense lines are connected to the printed circuit board electronics. This combination of variable and fixed capacitors produces a predictable and reliable capacitive coupling.

To eliminate stray capacitance and electrical noise in the closely spaced membrane, the conventional method of driving is inverted. All unused drive lines are therefore grounded and act as a shield. All unused sense lines are also grounded. Grounding is accomplished by a scanning chip in conjunction with a microprocessor, effectively prohibiting any interaction between key stations and significantly reducing the impact of electrical noise.

The hard contact keyboard is offered as a wired-only unit and as an encoded keyboard with 2-key rollover option. Both capacitance and contact keyboards offer standard or low profile key modules that meet European standards and provide operators with firm tactile response. Since sensing elements are found within the membrane layers, the key actuator module has been simplified. It consists of housing, actuating plunger, return (compression spring), and snap spring, which provides the definite hysteresis between operate and release points that prevents teasing and ensures positive contact.

The flat touch panel keyboard is made up of only three membrane layers; venting takes place through channels formed in the spacer and lower circuit layers. A snap disc in each position offers tactile feedback and protection of the switching area against actuation by sharp objects.

**Circle 354 on Inquiry Card**

## Micro-Winchester based desktop computer offers system development tools

Model XP/3 features a 5M-byte micro-Winchester hard disc for storage of system programs and data, plus a 900k-byte double-sided GCR (group code recording) minifloppy drive for I/O and backup. This enables the system, from Commercial Computer Inc, 7884 12th Ave S, Minneapolis, MN 55420, to provide high capacity, fast access, low cost storage with easy backup.

Compared with the industry standard minifloppy, the micro-Winchester stores 30 times as much data, accesses data twice as fast (170 ms average), and transfers data 20 times faster (5M bits/s). Standard system features include Z80 microprocessor, 64k of RAM (standard), a 1920-char CRT with antiglare amber screen, serial communications channel, and a Centronics-compatible parallel printer interface. Options include up to two additional 5M-byte micro-Winchester disc drives in their own cabinet and a selection of dot matrix and daisywheel printers.

The unit is supported by the CP/M operating system, with Microsoft BASIC (interpreter and compiler), FORTRAN, and COBOL available, as well as the Wordstar word processing system. Also offered are a group of software development tools that allow the OEM to interactively define and generate end-user business software. Metasoftware™ produces business packages in highly structured BASIC source code that can easily be modified to add specialized tasks.

**Circle 355 on Inquiry Card**

# HOW TO COPY THE MICROPOLIS 8" RIGID DISK DRIVE.

It's bound to happen sooner or later. Someone will decide to copy our 8" rigid disk drive. It happens to all industry-standard products.

So we're going to save someone the trouble and tell exactly how we built our 8" drive. But we're not worried. Because, frankly, we don't think anyone else will want to go to the trouble we did to give you such a product.

First of all, our family of 8" rigid disk drives (9 to 45 megabytes) comes with features you simply can't find in the competition's products. Such as our low-cost intelligent controller board, designed to allow swift integration into your existing system.

In addition to low power dissipation and fastest access time, we also included a Quartz-locked, direct-drive, brushless DC motor. We gave our rigid disk a braking mechanism, too. It extends the life of the disk by not allowing the head to act as the brake. That's a longer disk life for you, and a higher MTBF in the critical clean area. Next, we included our balanced rotary voice coil positioner, which, together with the closed-loop servo, absolutely protects against unexpected jolts, bumps, and shocks during write operations which might otherwise result in off-track writing.

We enclosed the heads, platters, and positioner assembly in a sealed clean area. No other drive has all active components outside the clean area, for easy access and maintenance. So we can offer the longest drive warranty in the business.

All this adds up to unprecedented quality, reliability, and stability. And our 8" rigid disk fits into the exact same space as an 8" floppy drive—they even use the same screw holes.

So if you want the best 8" rigid disk drive, call us. We deliver.

If you want to try and copy it, good luck. You'll need it.

MICROPOLIS™

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Chatsworth, California 91311
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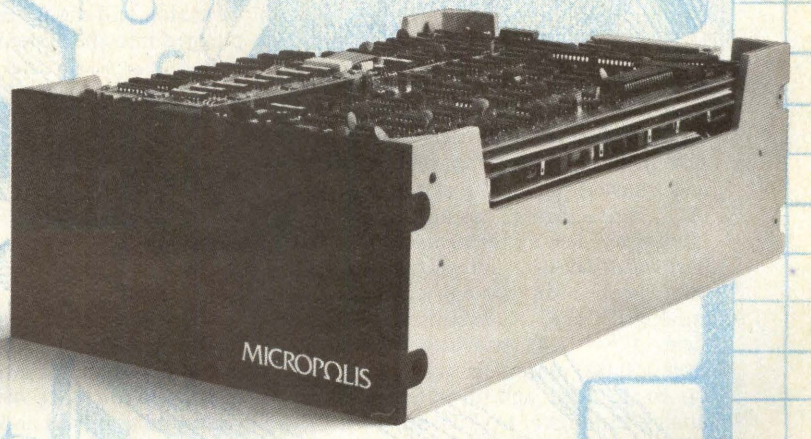


## Emulating computer gives TD-830 and UTS-400 users remote processing capabilities

Software enhancements for systems based on Unique™ minicomputers give users of Burroughs TD-830 and Univac UTS-400 networks economical remote processing capabilities similar to 3270 emulator operations in IBM networks. Announced by Data Communications Corp, 3000 Directors Row, Memphis, TN 38131, the systems allow concurrent multi-user operations including data collection, transaction processing, database inquiry, word processing, and 3270 emulation with local format storage capability.

Burroughs and Univac users who want to upgrade remote processing capabilities can install the Data General Corp computer based systems in standalone or host cluster configurations to save controller and communications line costs. Local format storage features reduce host mainframe involvement and increase remote functionality while maintaining compatibility with host network protocol. In addition, the systems provide access to the Cylix™ message switching network, a private communications network that has FCC approval to operate satellite communications equipment in an enhanced, shared usage data communications network.

**Circle 356 on Inquiry Card**

## FORTRAN programmable data acquisition system handles 1000 I/O channels

FOCUS 5000™ (FORTRAN Controllable Universal System) accommodates over 1000 I/O channels and meets accuracy requirements for gathering, manipulating, and transmitting analog and digital data in manufacturing, monitoring, and laboratory testing environments. The hardware/software integrated realtime data acquisition system, offered by Analogic Corp, Audubon Rd, Wakefield, MA 01880, provides a speed of over 100,000 measurements/s, accuracy up to 16 bits, and over 85 types of analog and digital I/O boards.

The system incorporates the ANDS5400 data acquisition system with the ANDS7000 controller and software to increase user productivity. Programmable in FORTRAN, the system implements ANALIB™, a sophisticated call package with a library of over 35 calls including I/O, timing/synchronization, Boolean algebra, and engineering subroutines, and provides comprehensive exerciser, diagnostic, and self-test packages.

High speed simplifies both integration and operation of realtime installations. When connected directly to transducers and receivers in the installation, the system will acquire, condition, and measure analog and digital signals at rates up to 100,000 samples/s. It will also process acquired signals in its self-contained computer, make decisions and transmit analog and/or digital signals based on the processed results, and display selected information all under program control.

Architecture of the system delivers the accuracy level and channel capacity to meet expanding needs. Application programs are tailored to the installation. Programs can read data from or write data to any implemented I/O channel, enabling a complete closed loop control system to be established from the keyboard alone. The architecture also provides realtime synchronization capability as well as I/O capability for high speed data acquisition with 16-bit resolution on as many as 1000 channels.

Specialized multichannel analog input cards available include strain gauge completion/measurement cards, thermocouple measurement cards with electronic cold junction compensation, and RTD measurement cards. Analog input full-scale ranges from ±10 mV to ±100 V are available, as well as 150-dB common mode rejection ratio and 300-V rms common mode isolation. Any mix of analog and digital card types may be plugged into the system.

**Circle 357 on Inquiry Card**

## Small computer system merges data and word processing capabilities

Both data processing and word processing operations merge are handled by the B 93 small business computer. The integrated system, offered by Burroughs Corp, Detroit, MI 48232, manages a variety of terminals and keyboard workstations, enabling computing capability to be placed where work originates, or where access to the programs or files is required.

The English language word management system software allows word processing operations to run in parallel with or to be combined with computer application programs. While some workstation operators are performing business data processing tasks, others may be extracting information from computer files. A terminal in the local network can be designated as both a data entry/inquiry station and as an operator control display, allowing users to place control of the computer where it is most effective, and the processor to be located where most convenient.

Housed in a single cabinet, the CPU has a 2-MHz cycle time. Basic memory is 256k bytes, expandable to 512k bytes. A 4k-byte memory is provided for a cold and warm start maintenance test routine. The system provides 8 I/O channels for up to 3 disc controllers and up to 4 data communications channels. Up to two line printers may be attached. These may be 48-char printers with speeds up to 650 lines/min, 64-char set printers with speeds up to 600 lines/min, or word processing letter quality printers. Five disc storage options are provided.

Data communications capabilities include asynchronous, synchronous, and bisynchronous modes. Speeds can range up to 38.4 baud on leased, switched, or 2-wire direct connect lines. The network definition language compiler allows fast implementation and reconfiguration of networks, and the message processing language compiler provides interfacing of user programs to the data communications network.

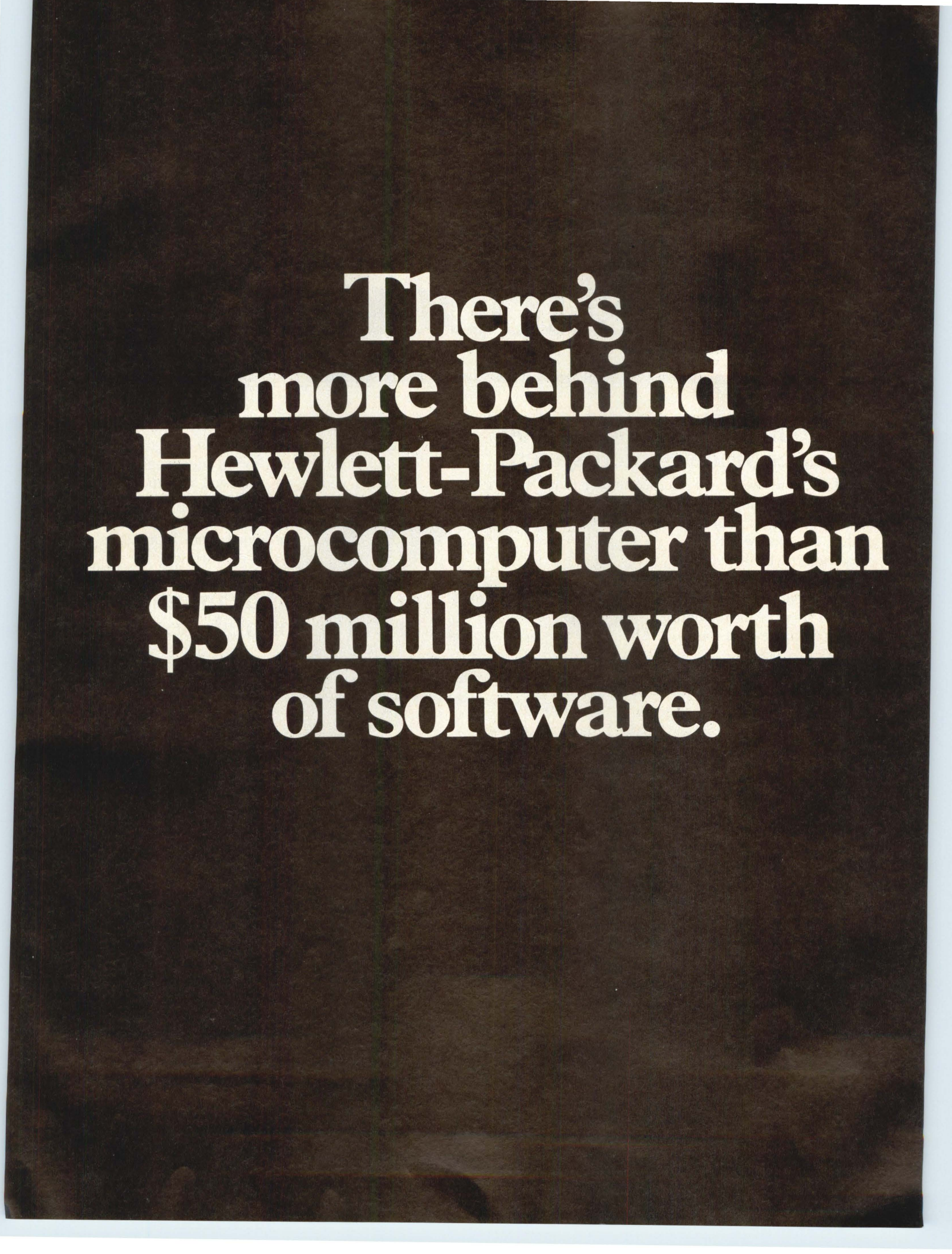
**Circle 358 on Inquiry Card**

## ECL based processor boosts scanning speed of data entry machine

Recognition speed of the Data Entry Machine based on optical recognition technology has been increased 300% with an ECL based processor capable of executing 6M instructions/s. Developed by Kruzeweil Computer Products, 33 Cambridge Pkwy, Cambridge, MA 02142, the system recognizes and converts to digital signals common typefaces and fonts, automating text and data entry into computer systems.

The scanner camera in the unit is capable of seeing several text lines at

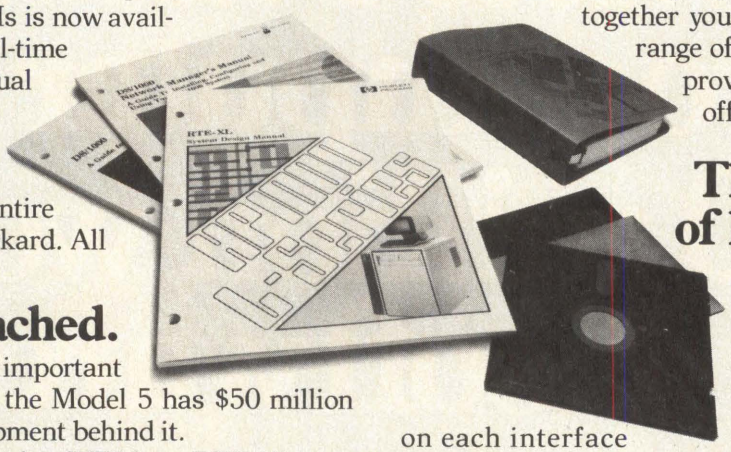
*(continued on page 62)*


There's
more behind
Hewlett-Packard's
microcomputer than
$50 million worth
of software.

# Full system support.

## Announcing the new HP 1000 L-Series Model 5 microsystem.

The same two-board microcomputer that's becoming so popular with OEMs is now available as an integrated, real-time system—complete with dual minifloppies, 128K bytes of memory, your choice of interactive terminals *and* full support for the entire system from Hewlett-Packard. All for under $10,000.




## All strings attached.

Software is the most important part of any system, and the Model 5 has $50 million worth of software development behind it.

You can start with either RTE-L or RTE-XL, our powerful multi-programming, multi-user operating systems. Their modular construction lets you build the real-time computing environment your applications programs demand—programs you can develop in Assembler, FORTRAN 4X and BASIC. And our HP DSN networking software makes it simple to put low-cost computing wherever you need it.

Data base management on a microcomputer? With our IMAGE DBMS, you've got a powerful tool for simple and efficient data management. And you can easily picture the possibilities offered by our GRAPHICS/1000 software. Like our other software packages, these are all upwardly compatible throughout the entire HP 1000 line, giving you an easy growth path to even higher performance.

## Configure it out for yourself.

The Model 5 is completely modular, so you can virtually design a system yourself. Hard disks and other peripherals can be plugged in directly. And thanks to a 60% reduction in memory costs, you can go all the way to 1/2 megabyte of memory for an additional $2000.

Whether you buy a packaged system, or put one together yourself, you can get HP's full range of customer support services, provided from more than 170 offices worldwide.

## The ins and outs of high-speed I/O.

In designing the Model 5, we used an advanced distributed intelligence architecture that puts a separate LSI I/O processor board on each interface. This means each processor has its own direct channel to the entire 1/2-megabyte memory. (We used state-of-the-art 64K RAMs to put the 512K bytes of memory onto just one board.) With the CPU free to concentrate on computation, you get significantly increased throughput and exceptional performance.

If you'd like a hands-on demonstration, just contact your local HP sales office listed in the White Pages. Or for more information, and our new OEM catalog, write to Joe Schoendorf, Hewlett-Packard, Dept. 12107, 11000 Wolfe Road, Cupertino, CA 95014.

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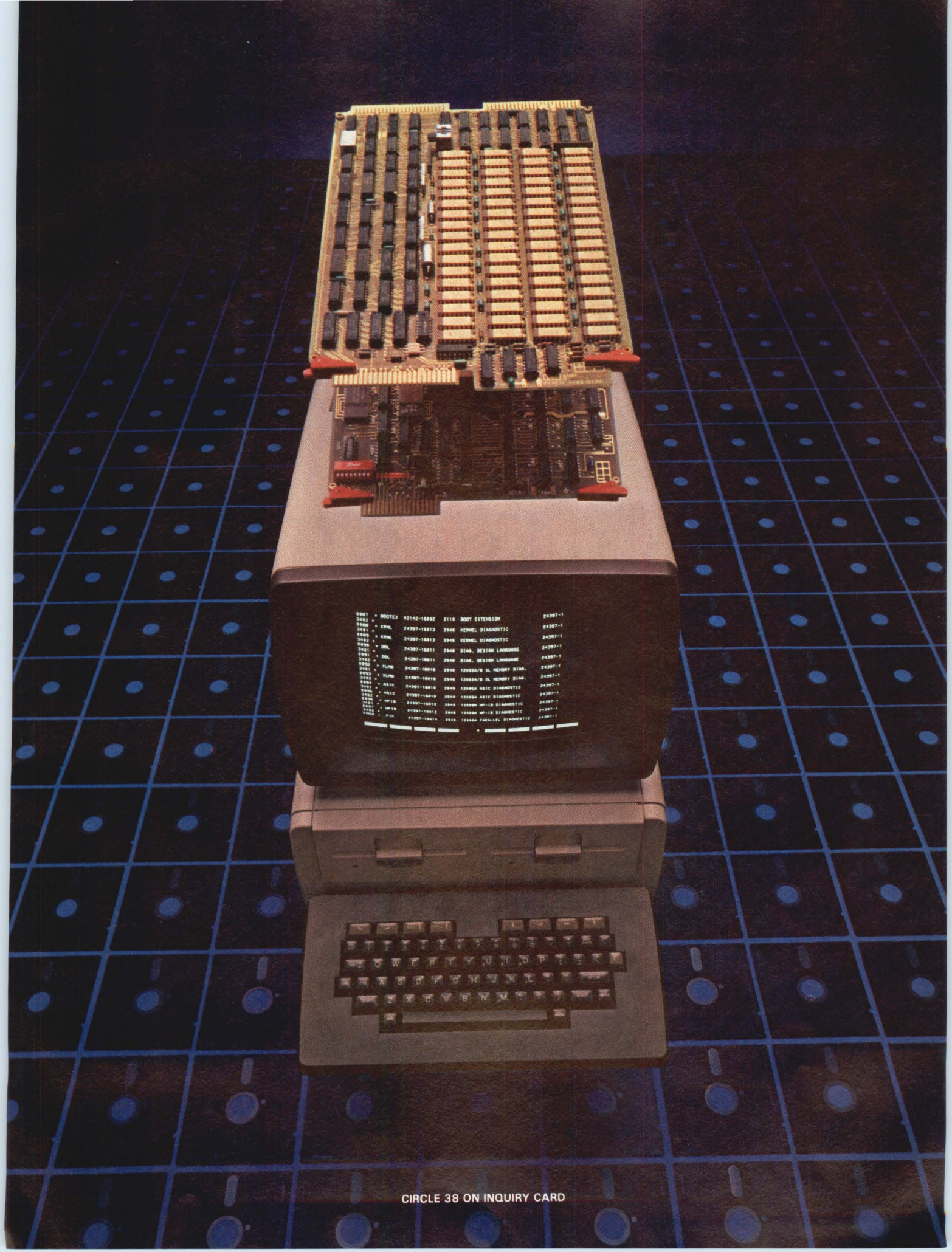
*Prices U.S.A. OEM quantities of 100 units. Prices subject to change without notice.*




CIRCLE 38 ON INQUIRY CARD

# ONLY ONE OF THESE COMPACT DISK DRIVES DELIVERS BOTH 25 YEARS OF MEDIA EXPERIENCE AND THE ANSI INTERFACE.

# THE ONE FROM 3M.

# INTRODUCING 3M BRAND COMPACT DISK DRIVES.

A new family of 8" Winchester drives offers you a unique combination of features—features that pay off in high-quality performance, reliability, and product migration. 3M designed and built these drives so that the features would be right for OEM applications—starting with the media itself.

## 1 WHAT MAKES THESE 3M DRIVES DIFFERENT FROM EVERY OTHER WINCHESTER IN THE WORLD?

Scotch® Brand media. An industry leader for over 25 years. Its proven performance is the cornerstone of our new fixed disk drives. The medium is critical—it's *precisely* where super-reliable data storage should start.

One guarantee of this performance is the thoroughly proven surface lubricant called Lubyte™. Lubyte helps protect against head crashes, loss of data and computer system downtime.

## 2 COMBINED WITH ANSI INTERFACE: HIGH PERFORMANCE OFF-THE-SHELF.

By using the ANSI interface, these Compact Disk Drives let you take full advantage of state-of-the-art technology for both low-cost design *and* high performance. The standard makes a disk drive's interconnection to its controller easier. 3M has made sure that the new drives deliver the flexibility you need to support specific systems and applications.

The ANSI interface is microprocessor-based, and works efficiently at high data rates. The result: 3M drives are easy on customers' equipment overhead.

## 3 MIGRATION FROM 10 TO 60 MEGABYTES AND BEYOND.

The third benefit the 3M Compact Disk Drive family gives you is the migration needed to keep up with user demands. Migration that won't dead-end your customers, or cost them an arm and a leg to obtain.

The 3M 8431 drive offers a total unformatted capacity of 10 megabytes on a single disk, with 8649 BPI and an average track density of 219 TPI. The 3M 8432, with two disks, delivers 20 megabytes, with the same bit and track density. The 3M 8533 offers 60 megabytes on three disks, with track density increased to 693 TPI. Modularly expandable, the drives offer you and your customers cost-effective increases in capacity from 10 to 240 megabytes.

## 4 THE "SUPER-CLEAN" AIR SYSTEM.

Because reliability is so critical to the operation of a sealed-environment disk drive, the drives have a specially-engineered super-clean air system (patent pending). A cast aluminum deck, for example, separates the heads and media from the motors: a feature that helps make 3M's super-clean air system distinct from ordinary systems. Air is cleaned to 10 particles per cubic foot/minute or less.

## 5 AND OTHER OUTSTANDING FEATURES.

Like microprocessor-controlled rotary actuators (patent pending), drive modularity, data separation and direct track addressing, and low power consumption. Right now, these new drives are the only ones that give you *all* of these features in one 8" Winchester package. It's time to evaluate them against the competition. For complete information write to:

Compact Disk Drives
Marketing, Data
Recording Products
Division/3M,
223-5N, 3M
Center, St. Paul,
MN 55144.

3M Hears You...

3M

CIRCLE 39 ON INQUIRY CARD

once on most material. While the format control software in the previous system selected one of these text lines to track and recognize, the multiline format controller (MLFC) used in this version tracks and recognizes all text lines in view of the camera simultaneously, doubling or tripling basic scanning speed. Processing multiple lines simultaneously requires equivalently greater computer processing power.

Therefore, the MAX computer used is about four times faster than its predecessor, being able to process about 5.88M instructions/s (MIPS), versus 1.47M. Together, the MLFC and the processor provide a basic speed improvement of between 50% and 300%, depending on the type of material being scanned.

Operator speed has been addressed by making available a 40,000-word English dictionary lexicon. By using English spelling context, 80% to 90% of potential operator interventions are eliminated. The enhanced data entry machine also incorporates a document feed and a redesigned workstation that eases paper handling. The unit is capable of storing 25 training sets online. Options include 9-track magnetic tape, document feeder, asynchronous or bisynchronous communication, a disc file management system, and a secondary editing terminal.

**Circle 359 on Inquiry Card**

## Factory data collection system enhances productivity in small to large networks

System 7300 provides operational performance advantages over conventional data acquisition and management systems, reducing clerical efforts on the factory floor by more than 50% and delivering input accuracies of better than 99% under ideal conditions and better than 85% in harsh environments. Overall, the system, announced by Identicon Corp, 1 Kenwood Cir, Franklin, MA 02038, improves manufacturing productivity by providing high system availability through rugged terminals that can be positioned between every two workers.

Using a fault tolerant architecture, the distributed processing system features an intelligent frontend processor and a variety of modular components such as concentrator modules, tape and disc storage devices, local multiplexers, and a range of data collection terminals. In addition, tightly coupled networking techniques provide complete formatting and communications functions, 2-way high speed data links, downline loading from host computers, data verification, editing, buffering, and error monitoring.

System modules are linked by the Identicomm$^{R}$ communications network which allows data to travel at 3000 bytes/s in both clockwise and counterclockwise directions over two independent data links or channels. By also providing for direct 2-way communications between the system and the host, this network permits extensive data formatting and communications protocol capabilities. Jumper selectable parity and data transmission rates up to 9600 baud are possible.

If a single module or data link fails, data acquisition devices attached to it are still available. Typically two modules are linked to the host. If a data link to the host fails, it is automatically detected by the second module and all data are transmitted via the remaining link to the host. If both links fail, data may be stored internally using optional disc and/or tape drives that accept information until communications links are restored.

The system uses bar code reading devices for data acquisition. Up to 2500 data input terminals may be added to a network configuration. Model 7321 data collection system control modules provide the direct physical link to host computers. Model 7322 data collection concentrator modules are linked directly to the control modules to form the basic system. Data entry stations are then organized into data acquisition nodes by the model 6035 data collection multiplexer.

**Circle 360 on Inquiry Card**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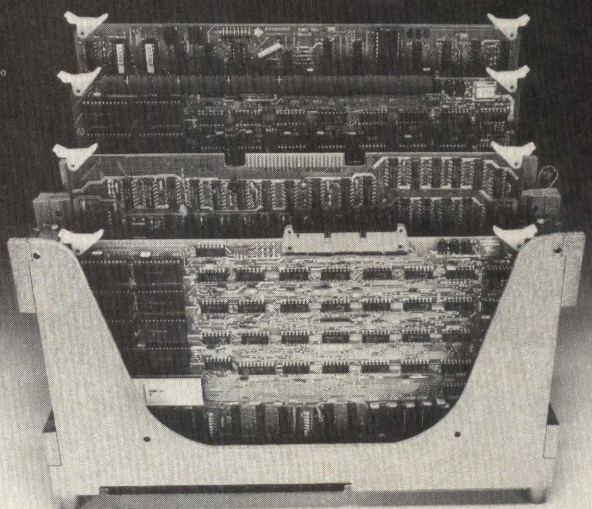

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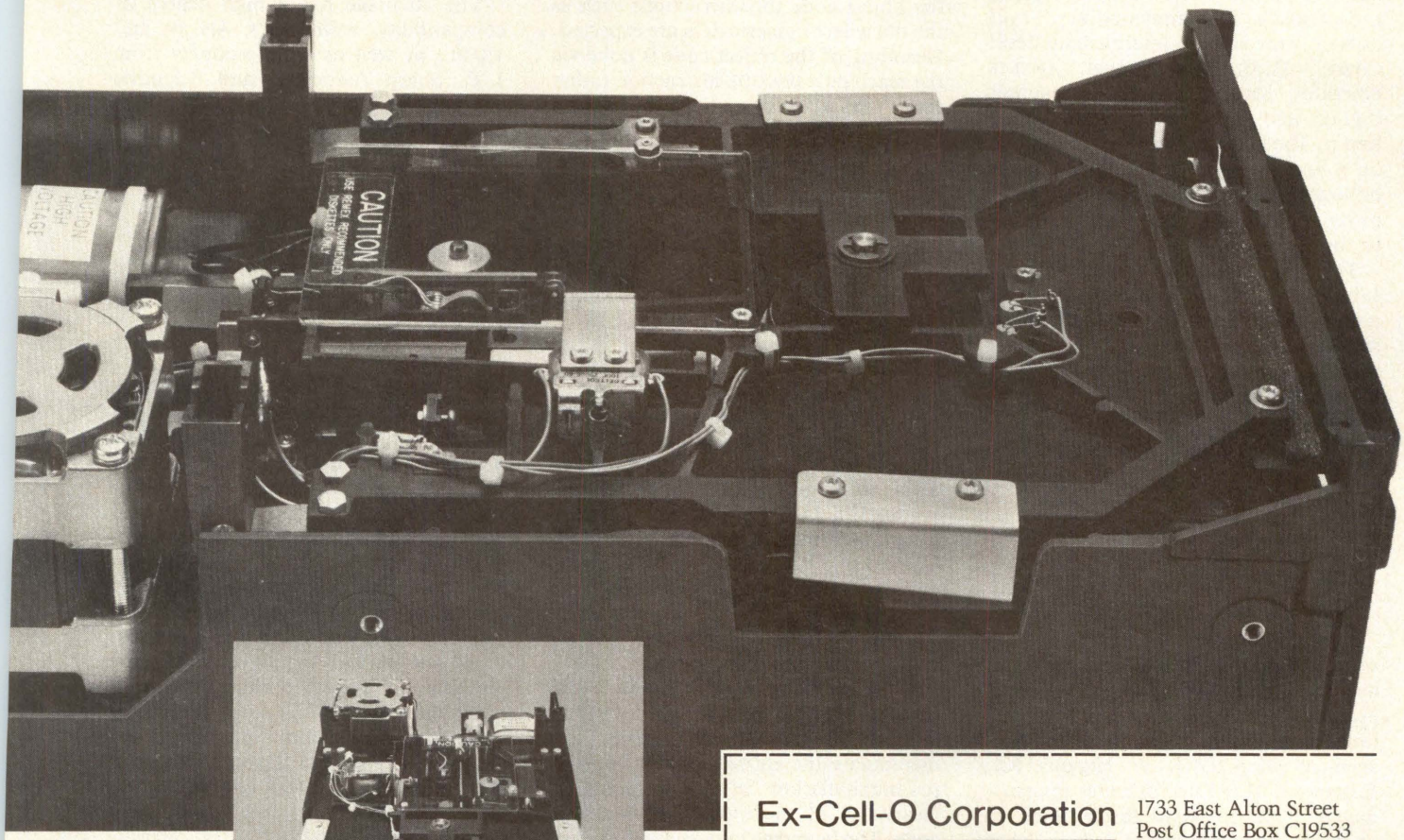
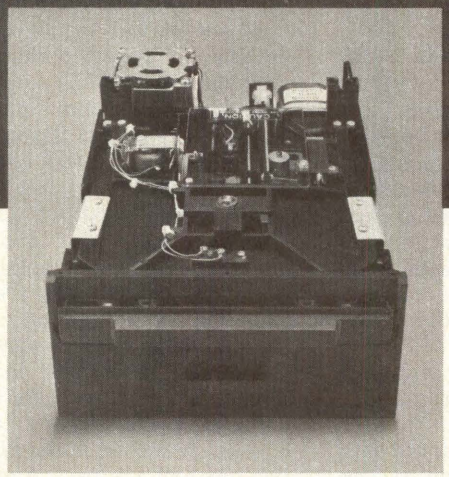
# Remex Dual Head Floppy Disk Drives.

## No Extravagant Claims. Just Performance.




*Remex RFD4000 Dual Head Flexible Disk Drive*



*Remex RFD2000 Single Head Flexible Disk Drive*

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## SOFTWARE

### Machine independent compilers run on 16/32-bit computers

A field tested family of machine independent compilers share a common optimizer and allow a common code generator. All phases of the compilers, except the code generator, are machine independent. Introduced by Language Processors, Inc, 254 Trapelo Rd, Belmont, MA 02178, the seven compilers are ANSI-74 low-intermediate level COBOL, ANSI-74 high-intermediate level COBOL, Draft ANSI Pascal, ANSI-78 FORTRAN, ANSI full PL/I, ANSI subset G PL/I, and IBM System/3-compatible RPG II. The language family will compile on a host machine that supports 16-bit or larger integers and provides 64k bytes or more of directly addressable memory to the compilers.

The entire family is written in ANSI subset G PL/I. Identical technology, data representation conventions, and a common intermediate language have been used in implementation.

**Circle 361 on Inquiry Card**

### Software language release improves execution speed, adds instructions

RPL-81 (Realtime Processor Language) has been improved through increased execution speed and additional instructions. The package from Systems Management Inc, 10400 W Higgins Rd, Rosemont, IL 60018, executes approximately 30% to 40% faster than its predecessor in programs having large arithmetic instructions. More efficient and structured programming is possible using the added IF..THEN..ELSE, FOR..NEXT, and square root function.

Speed improvement has been achieved in two ways. All data stored in the input buffer (% buffer) are not stored sequentially as in previous releases. Instead, a pointer approach allows direct reference to data. In addition, all other buffers have a last used pointer that keeps track of the last attribute referenced. Subsequent references to attributes ahead of the last used attribute start the data scan at that point, rather than at the beginning of the buffer. This reduces data reference time considerably, especially on large file items. The % buffer has an absolute limit of 250 attributes whether referenced directly or indirectly. An execution time fatal error message will be generated if this limit is exceeded.

Numeric data are stored in binary, rather than in string format in the % buffer attributes. In addition, the compiler stores numbers in binary format in the object code for instructions such as the IFN where numeric data are expected. Decoding of the object code is done via the machine's DECODE instruction rather than via a software routine as on previous releases.

**Circle 362 on Inquiry Card**

### 32-bit APL operates under AOS/VS to minimize user programming

The high level programming language and development tool APL (A Programming Language) has been added to 32-bit software available for the Eclipse MV/8000™. Offered by Data General Corp, Information Systems Div, 4400 Computer Dr, Westboro, MA 01581, the language operates under AOS/VS (advanced operating system/virtual storage) to minimize user programming and increase programmer productivity.

Workspaces may have up to 512M bytes of storage. This lets users organize a large file as a single array and manipulate the entire array as opposed to manipulation of array segments. Nearly all of the interpreter is shared code. The language may be used interactively for program development and execution or may be run in a batch mode where user intervention is not required. Up to 25 interactive APL terminals can be supported simultaneously.

The software combines the virtues of a compiler and an interpreter. APL-defined functions and lines entered for immediate execution are compiled into pseudocode for interpretation on an abstract, array oriented APL machine. Pseudocode is decompiled to make the source code available for function editing or error reports; compilation/decompilation is totally transparent to the user. A typical application can be developed 5 to 10 times faster in APL than in FORTRAN or COBOL.

A system formatting function formats a single array or list of arrays for quick generation of complex reports. An exception handling feature allows errors and other exceptional conditions to be intercepted and dealt with under program control, eliminating the need for user intervention.

The language has a high degree of compatibility with IBM's APL.SV and VSAPL, as well as with products from I. P. Sharp Associates and Scientific Timesharing Corp.

**Circle 363 on Inquiry Card**

### Software tools cut time and cost of generating documentation

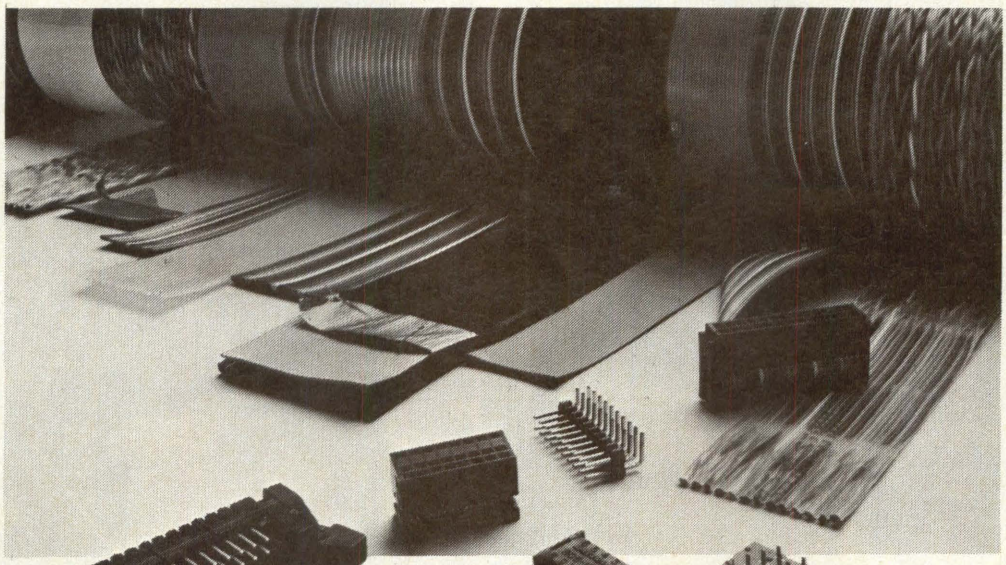
Increasing costs of technical documentation and a pending shortage of skilled programmers motivated development of a series of software tools, each designed to produce a specific section of a technical reference manual. The main goal for Applied Business Systems, 4350 Upper Soda Rd, Dunsmuir, CA 96025, in developing the packages was to simplify and accelerate preparation of technical manuals to save time and decrease costs.

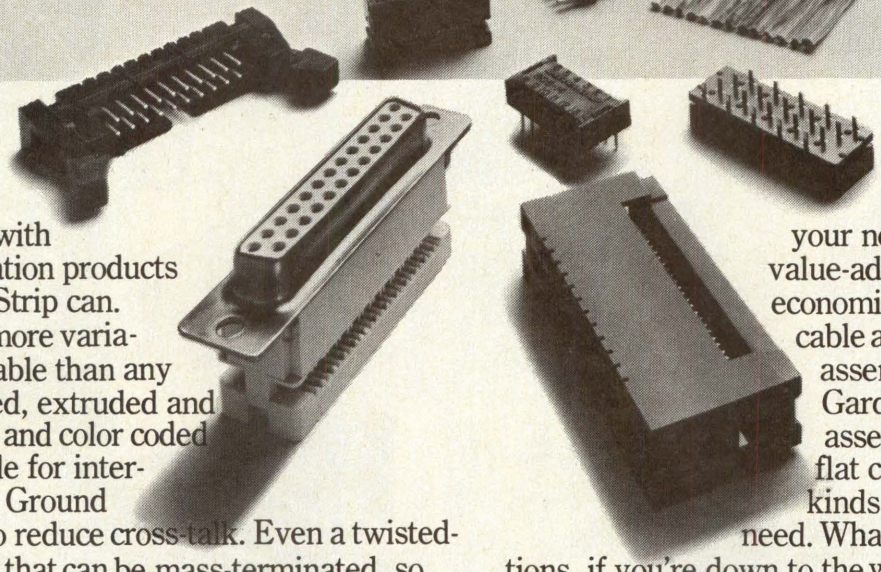
DOC-MASTER support packages simplify the documentation burden of programming organizations. Individual packages and functions performed are REPORT-DEF, report layouts; SCREEN-DEF, screen layouts; FILE-DEF, file definitions; ENTRY-DEF, screen data entry specifications; SPEC-DEF, technical program data and information; SYMBOL-DEF, program symbol tables; and FLOW-DEF, flow charts. SCRIPT-MASTER is a word processing system for freeform text development and maintenance.

Although defined as documentation tools, the packages can be used in preparation of reports and screen layouts, as well as in the system definition phase of a project. A major benefit is that reference materials are maintained on magnetic media for subsequent recall, modification, and reuse.

**Circle 364 on Inquiry Card**

# When you're down to the wire:





Nobody can support you with mass termination products like Spectra-Strip can.

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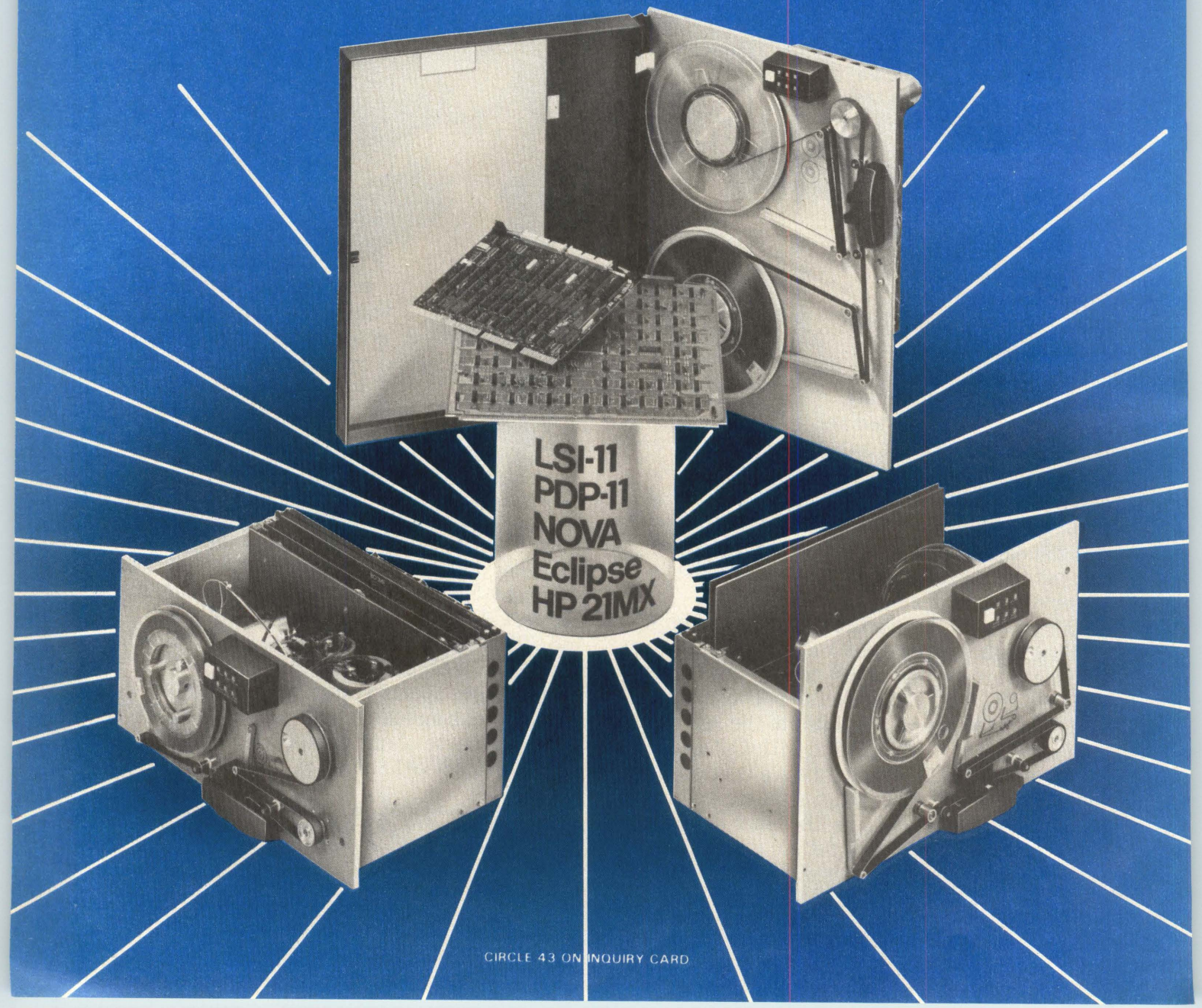



CIRCLE 43 ON INQUIRY CARD

## TECH REVIEW

## SOFTWARE

### Process control software increases configuration possibilities

MAXPAC, a software system that supports monitoring and control of industrial processes, provides data acquisition and system alarm capabilities that allow operators to control a process by exception, utilizing stations enhanced by color graphic and trend displays. The system, offered by Modular Computer Systems, Inc, 1650 W McNab Rd, Fort Lauderdale, FL 33310, uses an interactive fill in the blanks definition of the process data base. Data are acquired from the MODACS III process interface in a distributed environment, or from distributed systems offered by various instrumentation companies.

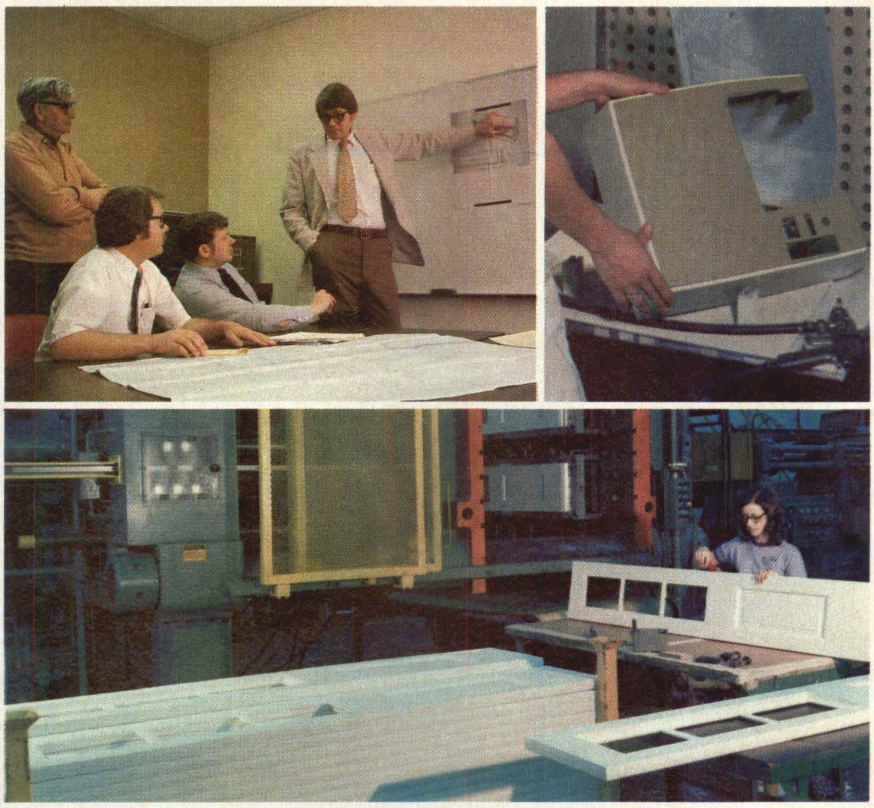
The system executes as tasks under the MAX IV multitasking realtime operating system and provides easy to use interfaces to the data base for user coded FORTRAN programs. MAXNET distributed resource sharing extensions of MAX IV are used to achieve distributed data acquisition, as well as interconnection with other in-plant computers.

System designers can interactively build process diagrams using MIRAGE, the color CRT screen management portion of the software system. Pictures are drawn using shapes, bars, lines, and characters placed anywhere on the screen. Realtime displays are composed of these static pictures plus dynamic elements obtained from the process data base.

The executive portion of the software system provides the operator interface by supporting a system of keyboards and semigraphic color displays. Each keyboard can control up to four color displays. Keyboards include function keys that can be assigned any command or set of commands at the time the system is configured.

A comprehensive reporting capability permits historical data to be requested for any point or group of points. These data may then be output in tabular form or as trend displays, functionally replacing stripchart recorders. Alarms are reported and logged as they occur on any designated logical device. Point reviews may be requested for any point or group of points that have bad sensors, are off scan, have alarm suppressed, or are in alarm.

**Circle 365 on Inquiry Card**

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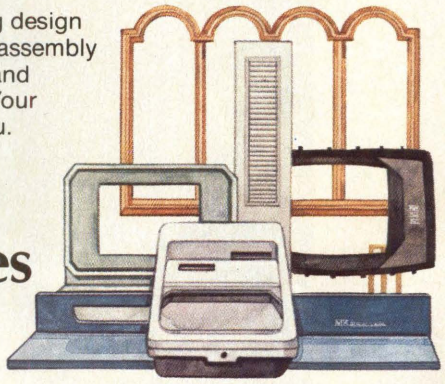

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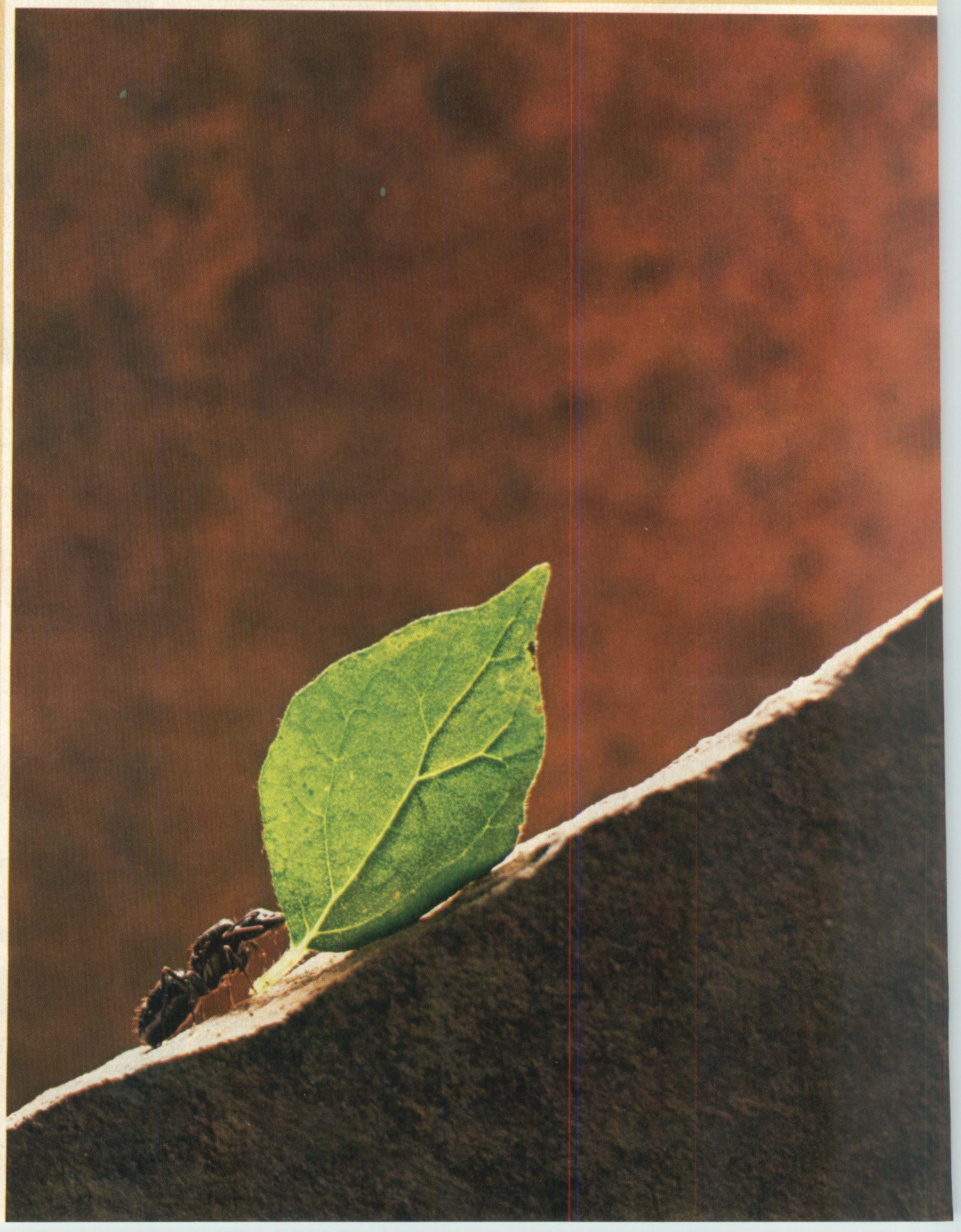

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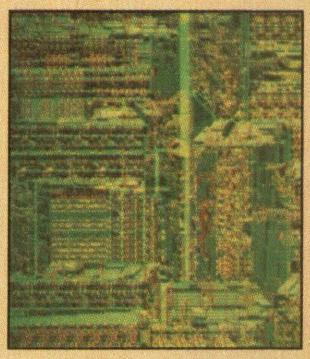

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**CIRCLE 46 ON INQUIRY CARD**

# 3-Level Data Acquisition System Monitors Sewage Treatment

It is often the case that distributed systems are assembled by user organizations through interfacing subsystems obtained from various sources. For example, an existing onsite mainframe might be utilized as the host to a subsystem of distributed processors acquired from an outside supplier. The advantage of this kind of system synthesis lies in the flexibility offered to the user to implement existing equipment. However, the user is faced with the problems of interfacing the diverse equipment. Alternately, a multilevel distributed system can be obtained in its entirety, all the way from a central host to remote sensors and actuators. The advantage here lies in the complete, integrated design of the system, with interfaces and communications built in from the outset.

Dealing with a supplier prepared to fulfill either of these approaches, the East Bay Discharge Authority (EBDA), 2651 Grant Ave, San Lorenzo, CA 94580, chose the latter approach and acquired a 3-level multilayered system from Process Control Equipment Co (PROCO), 14494 Wicks Blvd, San Leandro, CA 94577. EBDA is a consortium that oversees the treatment of sewage at five northern California plants and the discharge of the effluent, via a single "super sewer" system, into San Francisco Bay. The 3-level data acquisition system is used to monitor various parameters of the effluent in order to establish whether it is within acceptable limits with regard to pollution, toxicity, and overall environmental impact.

### System Overview

The EBDA system, mapped in Fig 1, shows four sewage treatment facilities, located in San Leandro, Oro Loma, Hayward, and Alvarado, and remote elements of the control network positioned in pump stations at or near each of these plants. All of these plants empty their effluents into a single central conduit 12′ (3.7 m) in diameter. In San Leandro, a dechlorination plant reduces the chlorine content introduced into the effluent in the treatment plants, in order to avoid adverse chemical effects upon marine life when the effluent is discharged into the bay. The system monitors this plant as well as a sampling station where a tributary system, under the jurisdiction of the Livermore-Amador Valley Waste Management Association (LAVWMA), empties into the super sewer.

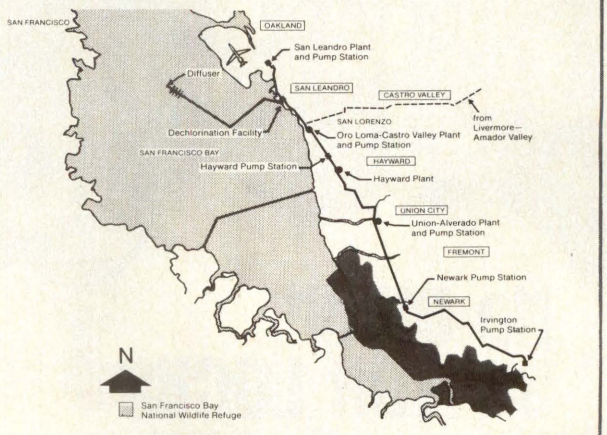


Fig 1 Super sewer network. Local treatment centers discharge into common pipeline. California State requirements on effluent levels in San Francisco Bay require realtime monitoring

Four parameters must be maintained within specified limits in order to meet State of California requirements. The qualities being tested are chlorine residual, acidity (pH level), turbidity, and biological oxygen demand (BOD)—an indirect measure of microbe contamination based on oxygen levels in the water. The principal purposes of EBDA are to monitor these critical parameters and to measure flow rates out of the various stations in order to determine billing rates to be assessed from participating agencies. Secondary functions relate to monitoring the status of the sewer system by such factors as pump operation, sump levels, and line pressure.

### A 3-Level System

Figs 2, 3, and 4 show the elements of the data acquisition system. High level supervision and human interface are provided at the single, level III central station (Fig 2). Computer Automation, Naked Mini Div,

*(continued on page 72)*

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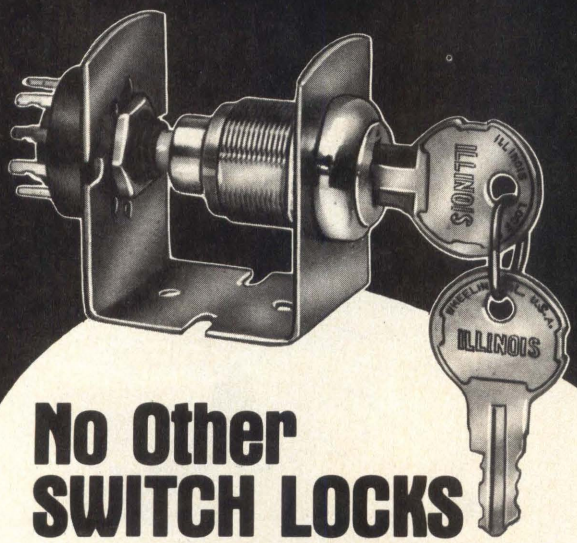


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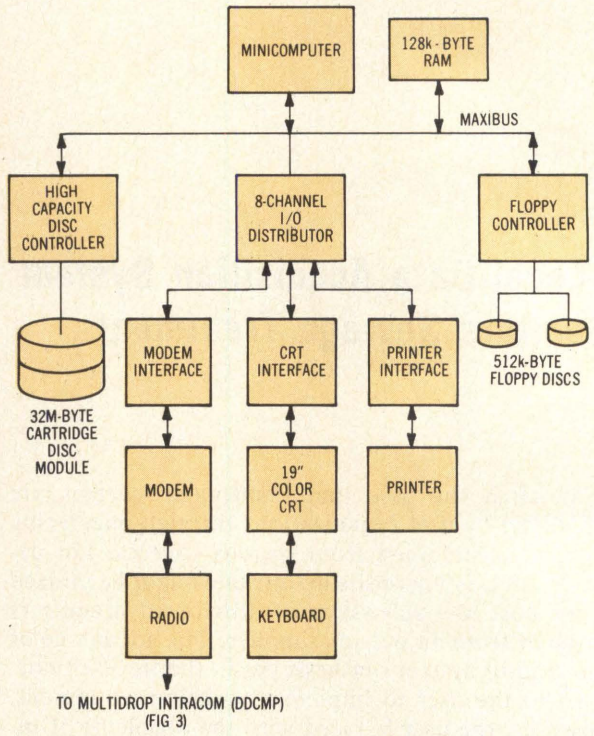


Fig 2 Level III central stations. Human interface and supervisory control are maintained from this site

18651 Von Karman, Irvine, CA 92713, is the supplier of several elements of this station, including a 16-bit 4/30 minicomputer, 128k bytes of random access memory (RAM), a disc drive controller, a floppy disc controller, and an 8-channel input/output (I/O) distributor, all interfaced to the Maxibus 16-bit bus. The I/O distributor interfaces to peripherals by means of various specialized versions of "intelligent cables," also from Naked Mini, each of which incorporates a microprogrammed picoprocessor™.

Peripherals utilized in the level III station include a 32M-byte cartridge disc module, model 9448 from Control Data Corp, Box O, Minneapolis, MN 55440, two 256k-byte floppy disc drives, model SA801 from Shugart Assoc, 435 Oakmead Pkwy, Sunnyvale, CA 94086, a 19″ (48-cm) color cathode ray tube (CRT) terminal with all printed circuit boards (PCBs) and microprocessors built into the keyboard, from Aydin Controls, 414 Commerce Dr, Fort Washington, PA 19034, and a 703 impact matrix printer having a 180-char/s max speed from Centronics Data Computer Corp, Wall St, Hudson, NH 03051.

*(continued on page 74)*

# Dependable Switchers...

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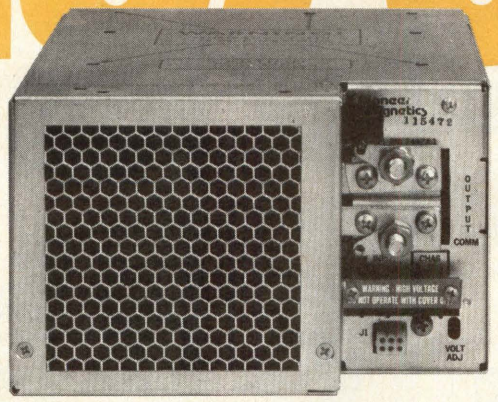

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| PM2497A | 200A | 100A | 100A 120A 150A | 60A | 50A | 45A | 33A | 27A | 16A | 12A | 5"X8"X11" |
| PM2500A | | 200A | 200A | 85A | 70A | 60A | 45A | 40A | 24A | 19A | 5"X8"X11" |
| PM2498B | 400A | 300A | 200A 300A | 120A | 100A | 90A | 66A | 54A | 32A | 25A | 5"X16"X11" |
| PM2501 | 400A | 300A | 300A | 120A | 100A | 90A | 66A | 54A | 32A | 25A | 5"X8"X11" |
| PM2502 | 500A | 450A | 450A | 180A | 150A | 125A | 90A | 80A | 47A | 35A | 5"X16"X11" |

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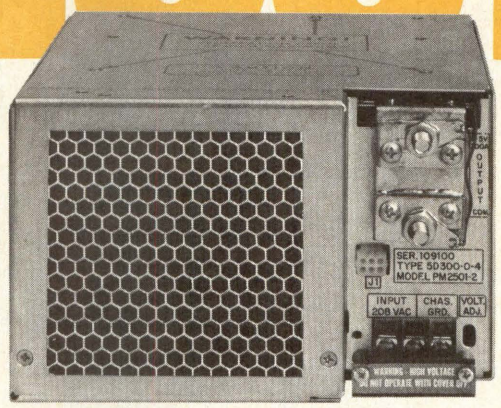

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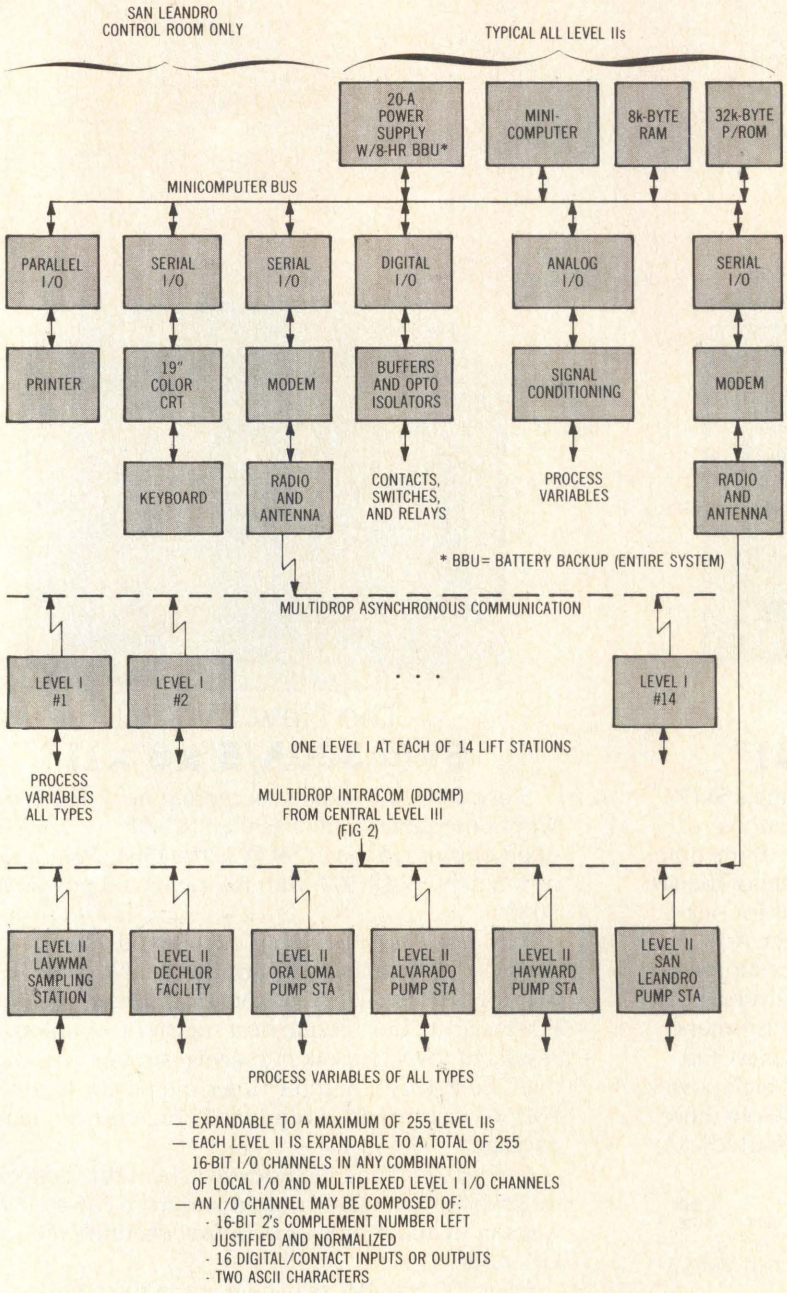


Fig 3 Levels I and II. One of seven level II sites (San Leandro control room) has expanded capabilities for personnel to utilize CRT terminal and printer

Immediately below this central station in the system hierarchy are the level II remote installations (Fig 3). Four of these are located at pump stations in or near the sewage treatment plants; one is located at the dechlorination facility, one at the LAVWMA sampling station, and one at the San Leandro control room. Each of these is based on the 16-bit Naked Mini 4/04 (Scout) minicomputer from Computer Automation. As shown in Fig 3, every level II installation includes 8k bytes of RAM, 32k bytes of programmable read only memory (P/ROM), and digital, analog, and serial I/O cards, all connected to the Scout bus. In the specific case of the San Leandro control room, provision is made for personnel to interact with the system by means of a CRT terminal and printer identical to those at level III.

*(continued on page 78)*



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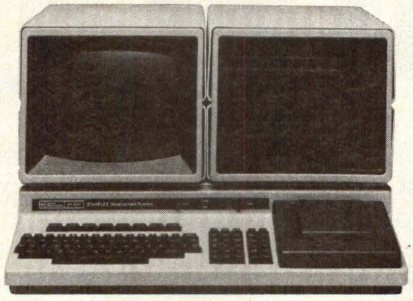

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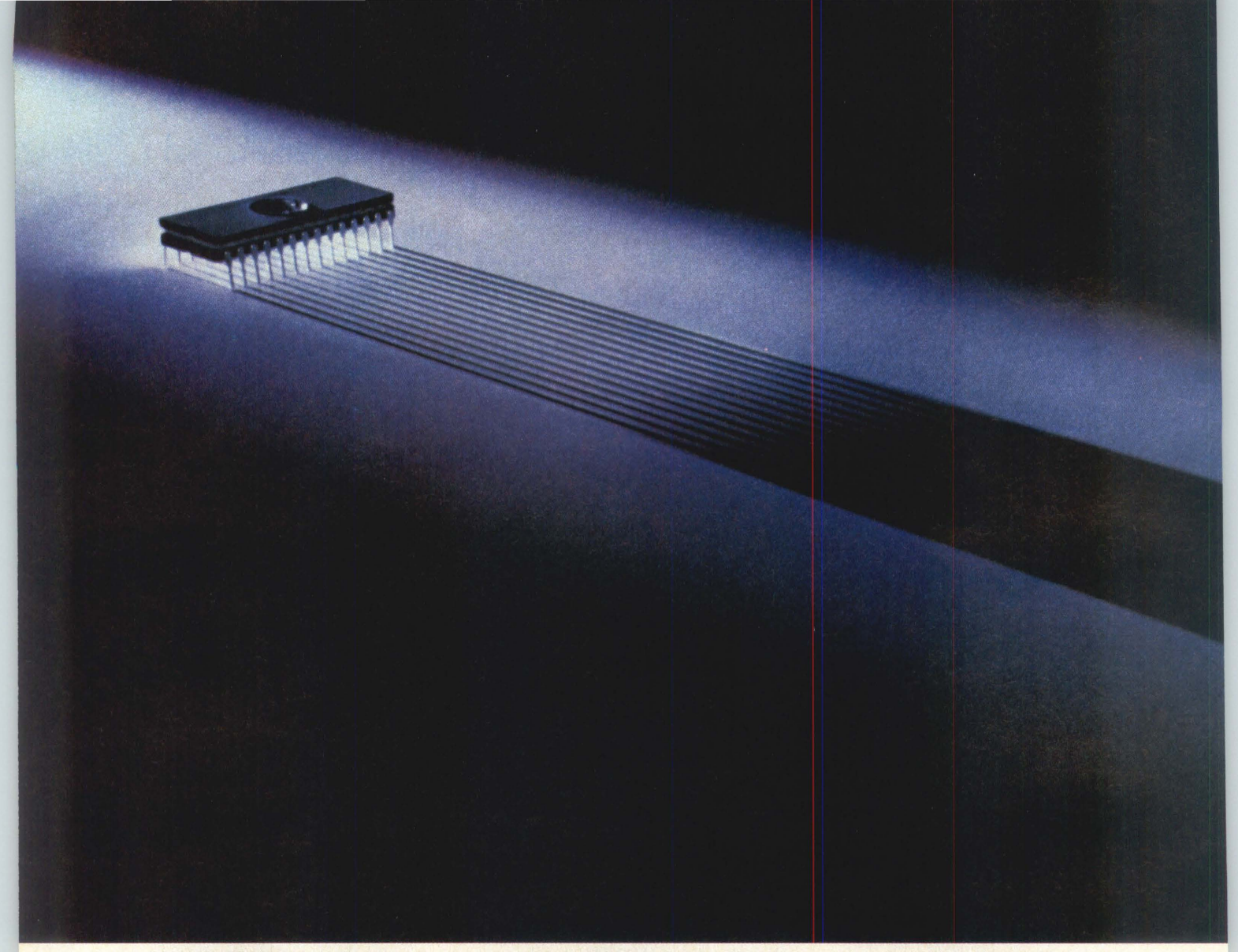

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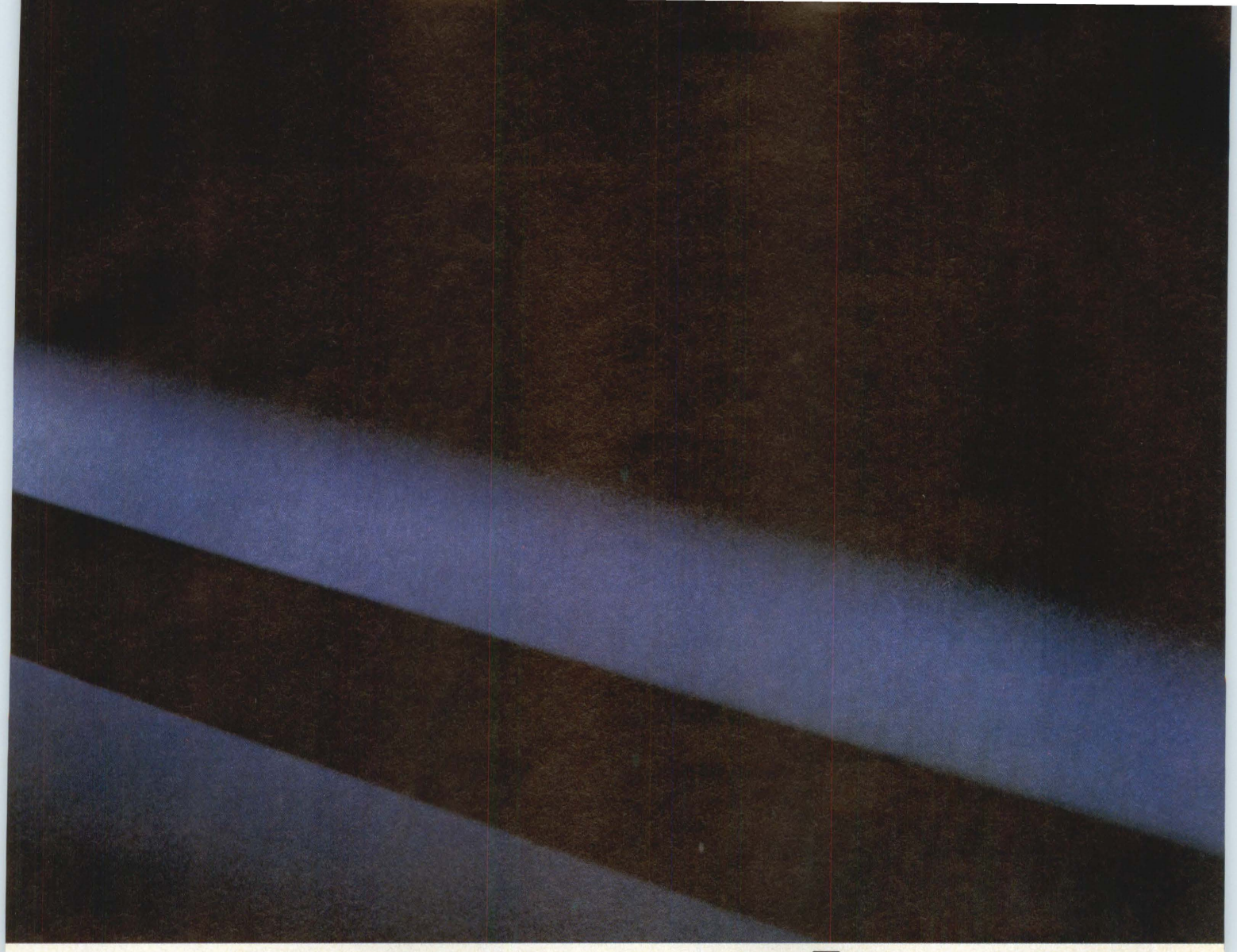

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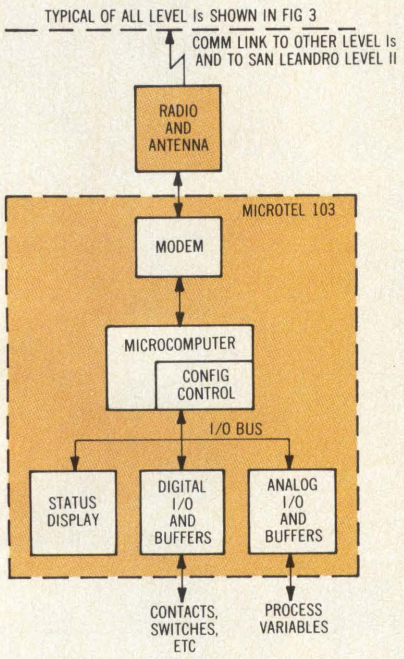



Fig 4 Detail of typical level I site. Control loop can pass through all levels

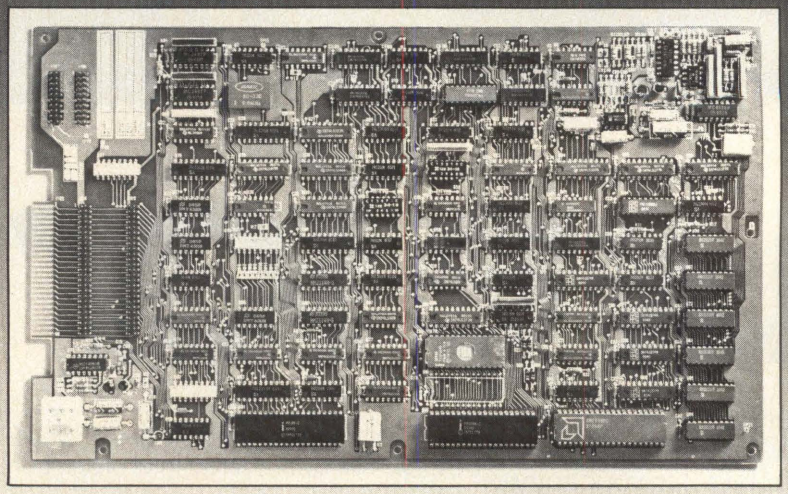
Level II installations carry out data collection from local sensors at their various stations, carry out calculations based on these inputs, and pass data up to level III. All level IIs communicate with one another and with the level III central station over a multidrop network that utilizes the DDCMP protocol originated by Digital Equipment Corp (DEC), 146 Main St, Maynard, MA 01754. This asynchronous communications link uses radio transmission and has a half-duplex transmission rate from 100 to 19.2k bits/s. The architecture enables all stations to monitor all activities concurrently.

Each level II is expandable to 255 16-bit I/O channels in any combination of local I/O and multiplexed level I I/O channels (Fig 4). However, at this time, only the expanded level II installation at the San Leandro control room is being configured to utilize level I inputs. The 14 level I elements reporting to the control room will not be monitoring the EBDA system, but will perform an independent task, monitoring the San Leandro City local sewage system. Nevertheless, these data, too, will be processed by the system as a whole.

The level I remote units, containing sensors, digitizers, and hardwired multiplexers, collect data,

*(continued on page 80)*


# INTRODUCING
## THE SMS WINCHESTER PLUS FLOPPY DISK CONTROLLER



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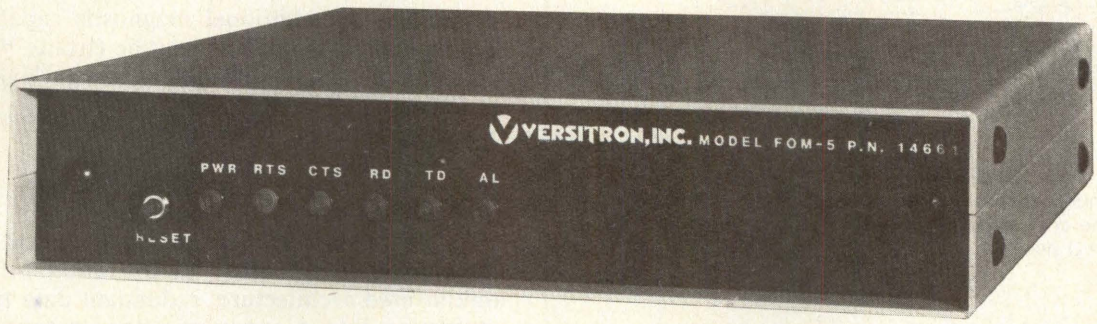
# fiber optic modem for local data distribution




## multiplexes control signals along with the data

Fiber optic modems are ideally suited for many local data distribution applications since they offer several inherent advantages over conventional hard-wired systems. These include immunity from rf and magnetic signals, increased bandwidth, and a significant improvement in the security of the data link.

Versitron's FOM-5 fiber optic modem (one of a family of fiber optic modems) not only provides the basic advantage of fiber optics, but also offers several unique system operating features that makes it ideal for local data distribution applications.

**Multiplexes Control Signals** — Three separate control signals in each direction are multiplexed with the data over the fiber optic link. This provides a fully interactive hand-shaking sequence with the FOM-5 functioning as a truly transparent device at both ends of the link.

**Increased Throughput and Range** — The FOM-5 operates full duplex over a fiber optic cable pair at synchronous rates of 50 or 56 kbps and asynchronous rates up to 14 kbps; with an operating range of 1 kilometer.

**Intrusion Alarm** — The receive circuitry continuously monitors the receive data for the presence of the multiplexer sync signal generated by the remote unit. Loss of this signal will cause an audible alarm condition and block further data transmission at both local and the remote modems. After verifying that the link is still secure, the system may be reset from either the local or remote unit.

**Plug-In Compatibility** — The FOM-5 has DSU/V35 or RS-232/MIL-188 interfaces. Pre-cut and terminated fiber optic cables are also available from Versitron.

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CIRCLE 52 ON INQUIRY CARD

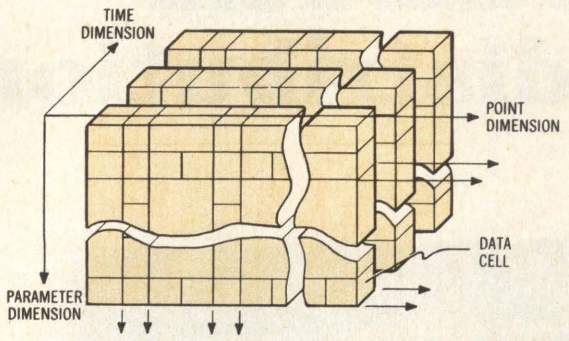


Fig 5 Data base is organized as 3-dimensional array, containing data elements in each cell of cube. Dimensions are time or scan interval, parameter type, and analog or digital I/O point

digitize those data, and transmit them, via a multidrop line, to the higher processing node. Message packets utilize a packed ASCII format with 8-bit cyclic redundancy check (CRC).

This distributed architecture is a customized version of the Microtel system developed by the system supplier, utilizing a software package designated as Procon. In the EBDA configuration, the system is presently operating in an open loop mode, with data acquisition as its primary function, although it also provides supervisory outputs to initiate such actions as local area alarm enunciators. However, it could readily be assigned closed loop functions to control system operating parameters, such as flow rates from pumping stations or chlorination rates, as a function of the sensor inputs. I/O capabilities include analog, digital, contact/digital input, relay output, single-loop non-indicating and indicating proportional integral derivation (PID) controllers, differential gap controllers, relay logic boards, RS-232-C compatible peripherals, and local operator interfaces and process display panels.

### Additional Features

The system's data base is organized as a 3-dimensional array, with time interval, parameter type, and I/O points as the dimensions (Fig 5). This data base is protected from loss due to power failure because it is maintained at both level II and level III.

Each level II has the capability for expansion to include a CRT terminal and a printer, as at the San Leandro facility described above. Furthermore, the system as a whole can be expanded to include additional level II units. (The inherent capability of the Microtel system, as described by its developer, allows up to 255 level IIs, for a total of more than 65,000 I/O channels.)

The Scout minicomputers monitor all points 24 hours a day and are polled by the central computer. A control loop, rather than being restricted to level I or II, can optionally be passed through all levels or closed anywhere in the system. Built-in diagnostics allow immediate isolation of any malfunctioning device. As an additional diagnostic capability, the Scouts contain a self-test routine (Isolite™) resident on circuit boards, resulting in a red light switching on to indicate a defective board.

### Summary

The distributed data acquisition system utilized by EBDA achieves flexibility of operation through its multilayered architecture, redundant data base, and integration into a communications network. These capabilities are resulting in an efficient, automated data gathering operation in which the sewage treatment functions of a widespread suburban complex are monitored and anaylzed. Furthermore, the modularity of the system provides easy expansion in scope and in functions handled, with ready adaptability to closed loop operation should requirements arise.

EBDA would not be feasible without an automatic monitoring system. The widely separated sites would require either an employee and office at each site or a few field service personnel traveling between sites, and neither of these options would be economically feasible. Nor would the sewage system be able to meet its requirements with a single site at the outfall, since responsibility for problems could not be identified with particular facilities. Given these strictures, and given that the project could not operate without going into violation, were data not available, a distributed system becomes a necessary approach.

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**High 710** **Average 711** **Low 712**

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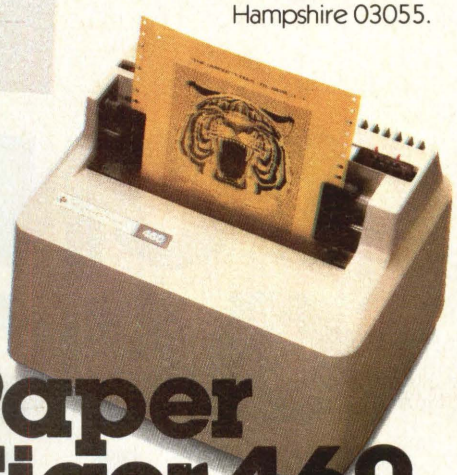

## Paper Tiger 460

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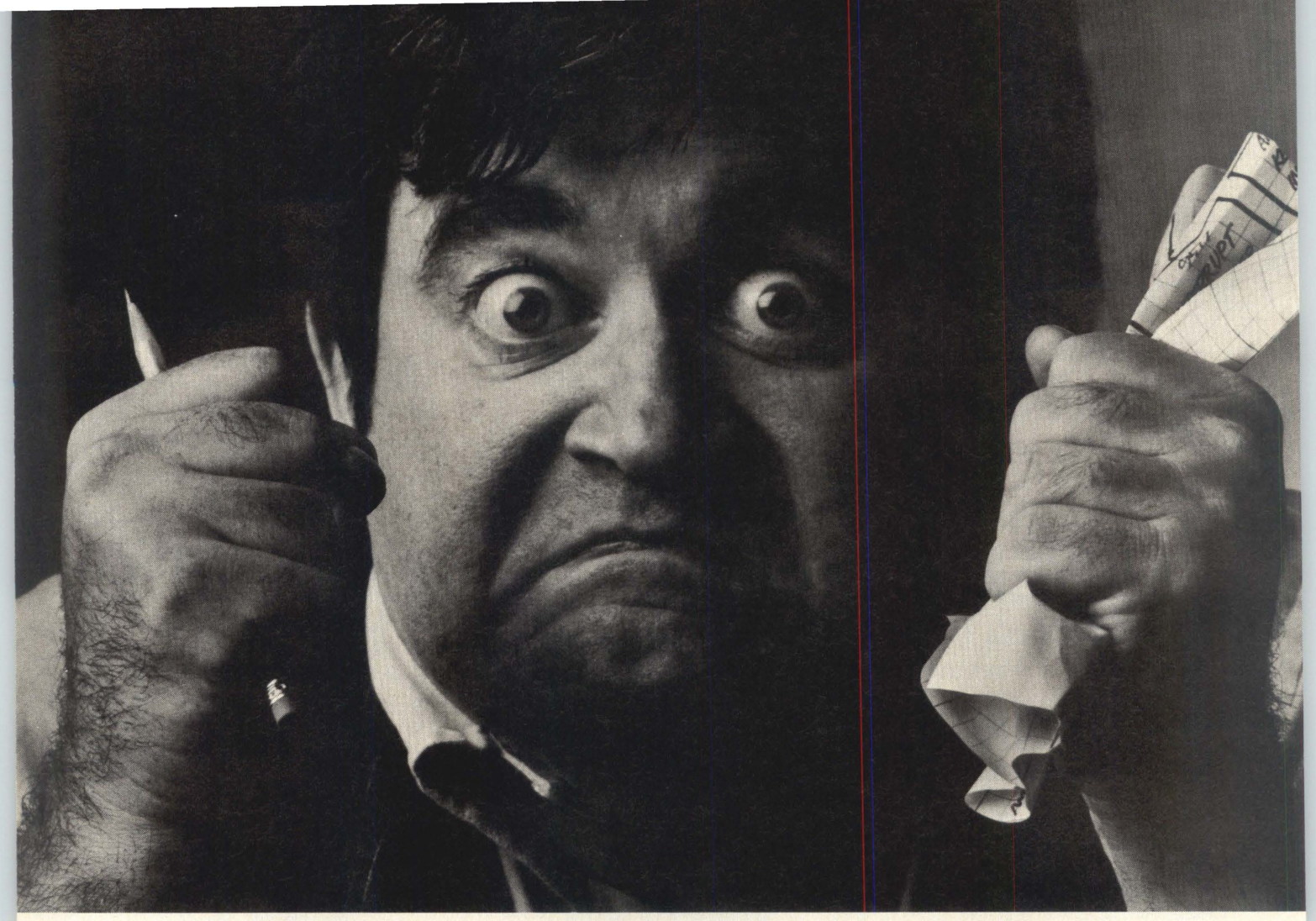
CIRCLE 53 ON INQUIRY CARD



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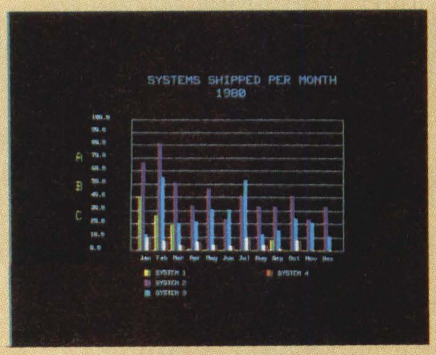
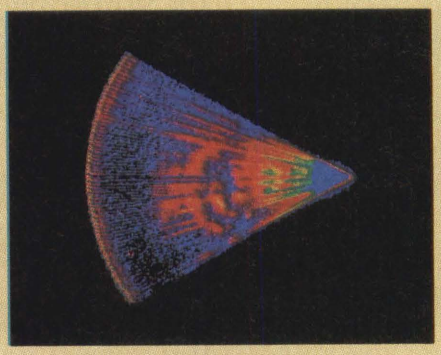
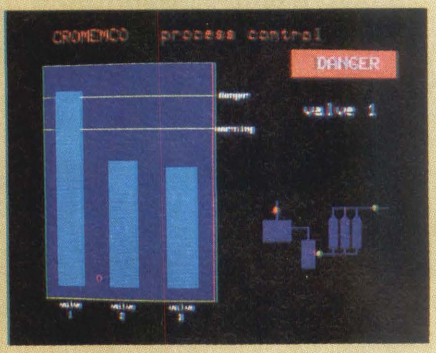



Management Information Display



Ultrasonic heart sector scan




Process Control

# Get the professional color display that has BASIC/FORTRAN simplicity

## LOW-PRICED, TOO

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The resolution surpasses that of a color TV picture.

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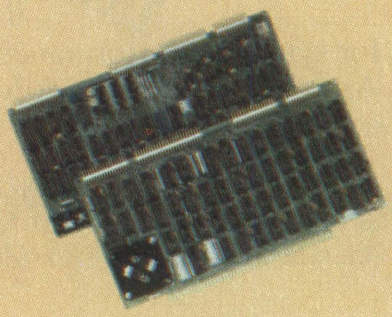
Besides its high resolution and low price, the new SDI lets you control with optional Cromemco software packages that use simple BASIC- and FORTRAN-like commands.

Pick any of 16 colors (from a 4096-color palette) with instructions like DEFCLR (c, R, G, B). Or obtain a circle of specified size, location, and color with XCIRC (x, y, r, c).

*U.S. Pat. No. 4121283



Model SDI High-Resolution Color Graphics Interface

## HIGH RESOLUTION

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

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## CONTACT YOUR REP NOW

The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

The SDI has still more features that you should be informed about. So contact your Cromemco representative now and see all that the SDI will do for you.

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**CIRCLE 55 ON INQUIRY CARD**

A PENNWELL PUBLICATION

# COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

JULY 1981

## SPECIAL REPORT ON COMPUTER GRAPHICS

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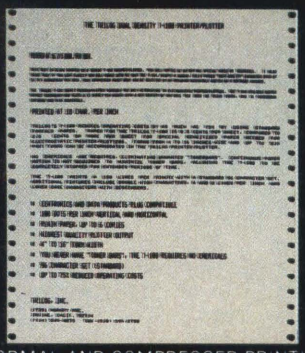
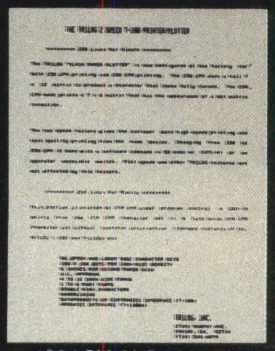
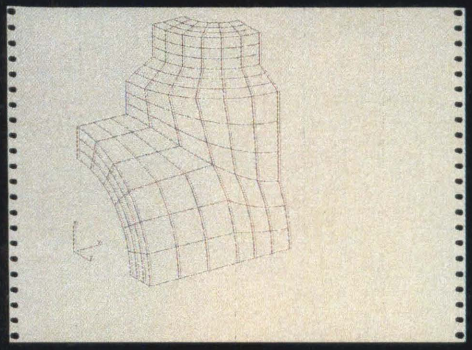


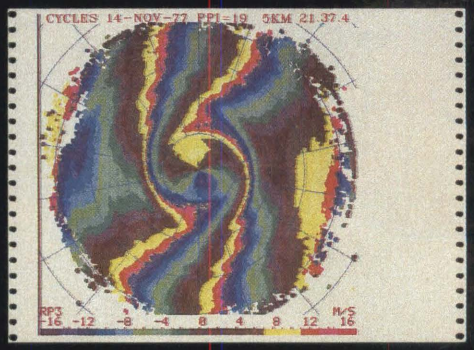
NORMAL AND COMPRESSED PRINTING



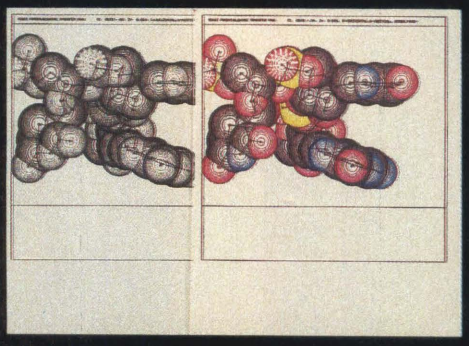
150 LPM AND 250 LPM



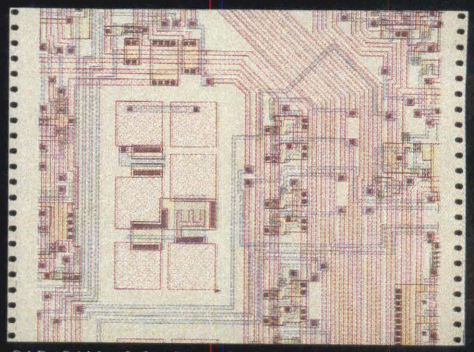
HI RES. STRESS ANALYSIS (PDA Eng.)




RADAR WEATHER MAPPING



SCIENTIFIC: MOLECULAR STRUCTURE (MIT)



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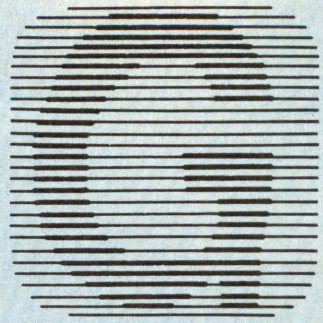


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Combining refresh and storage display technologies presents the designer with some interesting problems and design choices

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Multiple memory organization technique provides image overlay functions and multichannel display drive

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*Photo of actual CRT display.

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## *RASTER DISPLAYS... FOR THOSE WHO DEMAND PERFORMANCE.*

CIRCLE 57 ON INQUIRY CARD

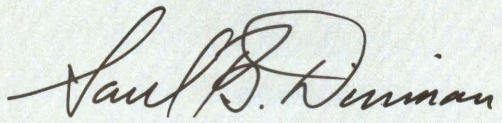
# INTRODUCTION

*This year seems to have produced a bumper crop of graphics display terminals, and the floor of NCC was "atwinkle" with many of the new offerings from domestic as well as off-shore suppliers. The number of graphics units on display was somewhat reminiscent of the days when VDU prices finally intersected those of the all but forgotten KSR33. With the advent of Star Wars, CAT Scanners, and Landsat derived topological maps, it's clear that the upper ends of graphics technology know no absolute bounds. The trend exhibited at NCC, however, was without question on lower cost units with higher resolution and color capability.*

*There were also signs of an emerging marketplace for personal computing products aimed at the business professional. The concept of the executive's terminal is coming on strong. Using graphics to condense and conceptually present what used to take mountains of reports and perhaps even a staff statistician to digest into a non-ulcerous display for the executive is an exciting idea. Freestanding graphics systems with impressive computing storage and communications capabilities are arriving on the scene with increasing frequency. Would that there were only half the number of software products arriving at the same time.*

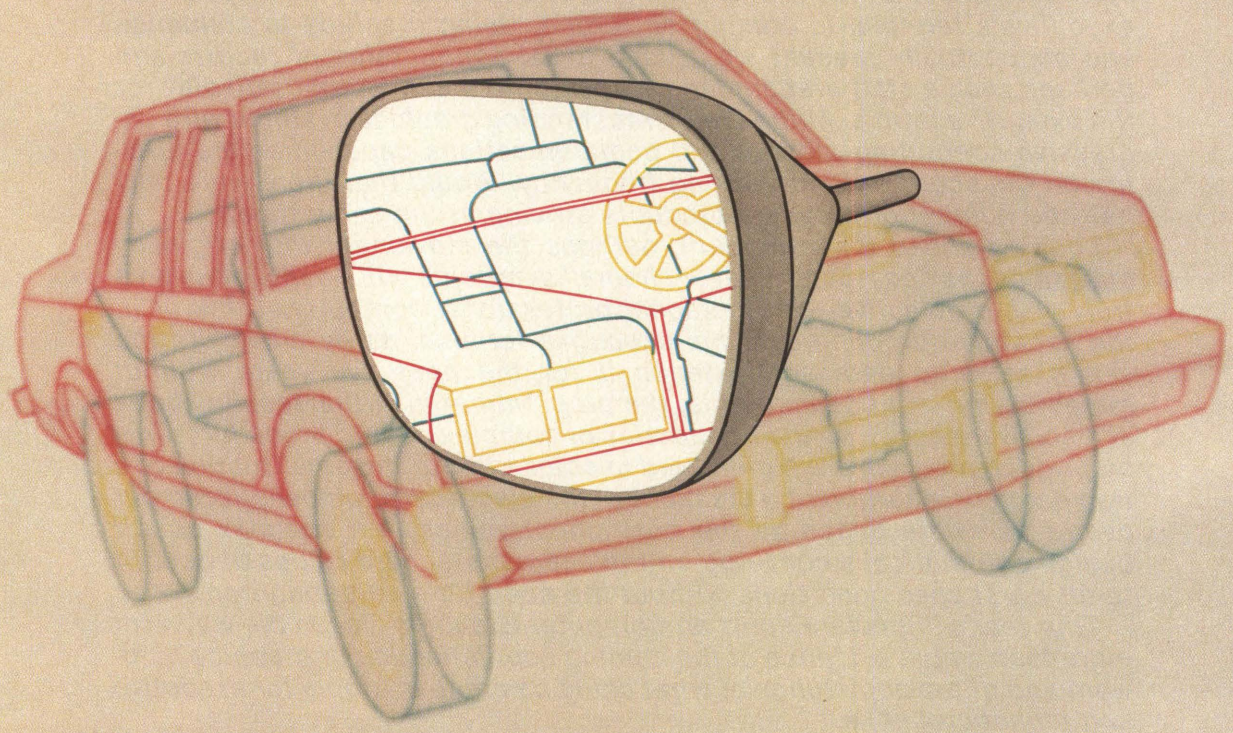
*Looking ahead for a moment, perhaps the movement that originally started as the "computer in every home" syndrome will finally focus on a truly viable objective—the personal professional computer. Think of it: the executive drooling over his executive terminal as he curve fits the year's sales to date and extends it for the next five years without remembering what a curve fit is; the programmer in virtual insulin shock at a software bench as the boundaries of complex nested procedures in a bug-ridden program are highlighted in color without the construction of a trap patch or insertion of a breakpoint; the electrical engineer spaced out over a hardware bench as the component values in a complex circuit design automatically converge on the nearest standard values of best fit to all worst case conditions without the need for a soldering iron.*

*This year's "Special Report on Computer Graphics" leads the way with more than ample evidence of the coming sophistication of graphics hardware and of the beginnings of what could be creative utopia for executive and technocrat alike.*



Saul B. Dinman
Editor

# The advantage of Raytheon's penetration color CRT is perfectly clear.



Readability. Legibility. Clarity. However you describe it, the extraordinary high resolution of the Raytheon Beam-Penetration Color CRT is really what puts things into focus. Especially in computer colorgraphic systems that combine graphic and alphanumeric display data.

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RAYTHEON

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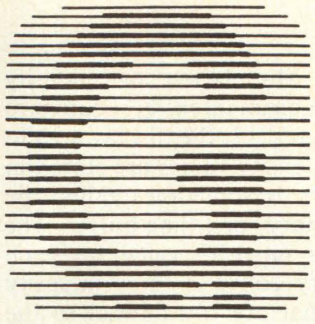

*LSI memory and processor elements now facilitate the full potential of raster graphics techniques*

# Raster graphics: expanding its frontiers

Computer graphics had its true commercial beginnings in the small X-Y plotters of the early 1960s. Plotter technology soon extended to line drawing displays based on cathode ray tubes and refresh vector hardware. Later, vendors introduced random scan storage tubes, which made computer graphics more affordable. Using these displays, it was necessary to store only the endpoint coordinates of picture line segments, holding memory requirements to a minimum and eliminating the need to refresh the display continuously.

Simultaneously, an image processing technology developed along its own evolutionary path. Instead of dealing with lines, image processing was based on arrays of individual picture elements, or pixels. Digital information defining the intensity or color of each pixel was stored in a random access memory and used to generate a television type, raster scan display.

Image data generally originated at a camera or an array of sensors. Computers sometimes processed the data before initial viewing. After viewing, data processing techniques were used to alter the contrast or color, or perform more sophisticated procedures such as correlation, convolution, and digital filtering, in order to derive new information from the image data or gain additional insight. Unfortunately, raster displays required considerable memory, which was relatively expensive until recently.

Today, low cost semiconductor memories and advanced large scale integrated circuitry have made raster displays economically feasible. High resolution displays and the use of gray scale and color essentially eliminate the objectionable staircase effect that appears when low resolution raster systems display line vectors. Microprocessor based architectures can alternate selected display elements at full video rates. Current generation systems combine the full-color, pixel by pixel control of image processing technology with the line drawing capabilities of vector graphics technology in a single display system.

## Raster configurations

Raster graphics system configurations vary between two extremes. At one end of the spectrum, a remote central host computer performs all graphics computation and modeling functions, as well as display formatting and viewing algorithm computations. A dedicated, standalone system performs all graphics processing at the other extreme. However, most configurations fall between these extremes and distribute the graphics processing load between a host computer and either an in-

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telligent terminal or a graphics display processor, thereby offloading the host significantly.

The intelligent graphics terminal concept is generally limited to alphanumeric graphics and the rudimentary vector graphics capabilities needed for business applications, process control, low level computer aided design or manufacturing, and educational applications. The more flexible and powerful alternative uses a separate graphics display processor, such as the Lexidata System 3400. In this kind of system, the raster scan display is refreshed continuously by reading a digital memory that contains a representation or map of the desired image, including the intensity or color of each pixel in the display.

The electron beam pattern of the cathode ray tube (CRT) is a major distinguishing feature of the raster scan display device. The beam begins at the upper left corner of the screen and sweeps across to the right, forming one scan line. It then moves rapidly back to the left and slightly downward to start the next scan line. This process repeats until the entire screen is swept, at which time the beam returns to the upper left corner to begin a new scan. An image forms on the screen when the intensity of the beam varies during the scan. Intensity variations are timed so that the beam is at the fullest intensity level when it passes over a spot intended to be bright, and at the lowest intensity level when it passes over a dark spot.

Initially, the timing for raster scan displays corresponded to broadcast television standards set by the Federal Communications Commission (FCC), which required a visible vertical resolution of 480 lines and a horizontal scan line of approximately 512 pixels, with an additional timing limitation such that the color could not change more than about 200 times on a scan line. FCC standards also required scanning the entire screen 30 times each second. However, a display scanned at this rate would appear to flicker objectionably. To reduce flicker, the scan is interlaced. Each frame is generated in two passes, called fields. The first pass generates all even-numbered scan lines. The second field generates the odd-numbered lines. Each field takes 1/60 s, giving the effect of a 60-Hz refresh rate, which is fast enough for the eye to perceive a steady image.

At the low resolution of commercial television, interlacing is a suitable process only because the broadcast images to be displayed do not differ markedly from one scan line to the next. This is rarely the case with computer graphics, however. For example, if an application calls for a picture with many horizontal lines spaced a uniform number of lines apart, the even- and odd-numbered fields can have markedly different intensities and flicker will become easily perceptible. Instead of following the FCC standard, most successful computer aided design/computer aided manufacturing (CAD/CAM) installations use noninterlaced scans with a 60-Hz refresh rate or higher resolution displays with long persistence phosphors.

A typical raster graphics display system includes a minicomputer, a graphics display processor, and a CRT monitor. Basic elements of the graphics processor include the display controller, the bit map memory, the lookup table, and the video circuits with their digital to analog converters (DACs). Modulation or intensity values determine the electron beam intensity required to produce an image as the beam scans the display area to refresh the picture. These intensity values are stored in the bit map memory, which is sometimes called the image memory, display memory, or frame buffer. The display controller reads the intensity value for each pixel. Video output circuitry converts these intensity values to analog voltages that are transmitted to the beam intensity amplifier where they drive the monitor display.

### Video lookup tables

Lookup tables specify colors or levels of gray scale under program control. When the display controller reads the intensity (Z-axis) values stored in the frame buffer, it does not convert these directly into analog values, but instead uses them as offsets into a lookup table. The value stored at a referenced address in the lookup table contains three or four fields, interpreted as voltages to drive the red, green, and blue guns of a color monitor and, sometimes, an optional monochrome monitor. The maximum number of entries in the lookup table equals the number of different intensity levels that can appear in the bit map entry for each pixel, usually from 8 to 4096.

In bit map memory, every pixel with the same binary intensity value has the same color definition. The lookup table word referenced by this intensity value is a set of weighted quantities, in binary format, each directly proportional to the intensity of a CRT beam directed toward the phosphor dot or triad at the pixel coordinates. If lookup table quantities are 8-bit values, either the red, green, or blue color gun can have any of 256 intensities, for a total of $2^{24}$ or about 16M different colors, each defined by a lookup table value. The number of colors that can be displayed simultaneously from this vast palette depends on the number of lookup table entries, which in turn depends on the number of bits assigned to each pixel in the bit map. With n bits/pixel, a bit map entry can address any of $2^n$ lookup table entries, each defining one color. For example, with 12 bits/pixel, lookup table data can designate up to 4096 of the 16M colors.

Since the lookup table is considerably smaller than the frame buffer, it can be altered much faster, usually at the refresh rate of the display. Lookup table speed and versatility are critical performance features. For example, changes to a high speed lookup table can create animation or motion effects even when the image in the bit map remains constant. To place a foreground object into motion relative to its background, a composite image is formed that consists of superimposed frames, each showing the object in one position of the animation sequence, and each designating a different "color" for the object. The lookup table maps one of the many foreground object colors to the true display color, and maps all other foreground objects to the background color. Then, changing only two lookup table entries merges a visible foreground object into the background, where it cannot be seen, and exposes the hidden object in the next frame of the animation sequence.

## Future Trends for Graphics Displays and Systems

| | |
|---|---|
| 1981 | Business graphics applications—mostly low resolution color raster—begin to increase |
| | CAD/CAM systems begin almost total conversion to raster; only exceptions are high end systems involving rotation |
| | Noticeable improvements in graphics monitors result from faster and more reliable electronics, new phosphors, higher bandwidths, and easier convergence |
| 1982 | Low cost CAD/CAM systems using black and white and color raster displays begin to proliferate |
| | Application software becomes a critical element for the success of turnkey graphics system vendors |
| | Satellite processors connected to large mainframes become more common in CAD/CAM |
| | Business graphics using high resolution displays begin to grow rapidly. Users become accustomed to graphics software and new input/output (I/O) devices |
| | Graphic arts applications implement high resolution raster, first in black and white and then in color |
| | Intelligence of local graphics terminals increases, offloading graphics functions. Graphics processing tasks are divided in new and innovative ways |
| | Advanced raster systems develop sophisticated rotation capabilities |
| 1983 | Large computer mainframe companies begin to threaten the position of turnkey companies that lack software and customer support |
| | A new generation of CAD/CAM systems involving substantial computational processing and higher resolution is introduced |
| | Spatial and relational concepts in graphics data bases appear in commercial products |
| | Initial graphics exchange standard (IGES) interfaces and database structures become accepted |
| | New generation of high resolution monitors (2k x 2k) is introduced |
| | Very large scale integration applied to raster displays lowers costs |
| 1984 | New high resolution international television standards are introduced |
| | Low resolution graphics terminal market decreases rapidly |
| | I/O devices providing natural interaction with graphics displays become common |
| 1985 | High resolution digital technologies compete with raster display systems |
| | Facsimile, electronic mail, graphics processing, and data processing are combined into integrated systems |

### Bit map memory

Each location in bit map memory holds the intensity value that corresponds to one pixel on the display. A minicomputer can access the bit map memory to read or write this pixel map, thereby altering the displayed image. Frequently, the display controller includes a zoom option that can replicate pixels to give the effect of enlarging a region within an image. If an image consists of a sequence of frames and the zoom feature is used to enlarge each frame to fill the display, viewing each of the enlarged frames in quick succession produces an animation effect. If bit map locations exceed the number of pixels on the display, scroll and pan options can provide a movable window by reading only a user selectable segment of the bit map.

To preserve a direct correspondence between pixels on the display and bits in the bit map, the bit map is viewed as a set of memory planes, each containing one bit for every pixel. Using this terminology, a system that displays 4096 colors simultaneously will need 12 memory planes, each containing as many bits as there are pixels in a display. Each memory plane contributes one bit to form the lookup table offset associated with a pixel.

#### Bit plane extraction and density slicing

The process of building a lookup table offset by taking one bit from each memory plane in the bit map is called bit plane extraction. Density slicing is a 3-dimensional variation on this theme. With density slicing, the image stored in the bit map is considered to be a monochrome image in three dimensions; the color values are interpreted as Z-axis data. In a sense, the normal X- and Y-axis coordinates form a plane parallel to the CRT screen, and the CRT display shows a cross-section of the image, an arbitrary slice whose depth and thickness depend only on the number of memory planes. Using prioritized memory planes, hardware rearranges 2-dimensional slices stored on different memory planes to construct a 3-dimensional image.

#### Transparency and pseudo-color mixing

Two related techniques called transparency and pseudo-color mixing are especially useful for computer aided design applications in integrated circuit and printed circuit board layout work. Using transparency, different images stored on separate memory planes seem to exist on translucent sheets of colored cellophane. Wherever the two images overlap, their separate colors combine to create a blended hue. Pseudo-color mixing replaces the spectral combination of two colors with a distinctive, arbitrary hue that emphasizes the overlap region.

Lookup tables are also used to load gradations in gray scale value, called ramps. A predetermined algorithm can vary color or gray scale as a function of pixel position for each level of intensity. Then, 3-dimensional images can include reflections and shadows that simulate lighting effects. For example, a ramp that varies the gray scale from very dark through an intermediate intensity to a very light shade can be used to simulate

highlights on a 3-dimensional object whose surfaces vary in distance from a light source.

### Additional raster features

Although lookup table performance enhancements are among the most powerful features of raster graphics systems, expanded bit map capacity is becoming an equally attractive option and can be used in several ways. If the bit map contains a larger image than will fit on the display screen, information can be scrolled vertically or panned horizontally with no need to rewrite bit map data. A double-buffered bit map can be used to assemble one complete frame of information while another frame is being displayed. Then, switching from one section of the bit map to another achieves high speed changing of displayed data. Sequential pictures can be stored and reviewed rapidly in cinematic sequence, or alternative solutions to a design problem can be toggled onto the display for quick comparison.

Other raster graphics features include selective blinking by pixel, by memory plane, or by intensity (color). Some systems allow graphics or text overlays that can be added, removed, or changed without affecting the underlying information. Character generators produce text at high speed to increase performance, and multiple-image sources use auxiliary high speed input ports. Multiple-input systems have the significant potential to combine photographic data with tentative design data, or to combine new data with previously recorded data. For example, business charts from past financial reporting periods can be recorded on videotape and later combined on the display screen with current period charts generated by the computer. It has also been suggested that background patterns or images might serve as a visual analog of background music, relieving tedium and helping to maintain the operator's attention. Many possible applications involve a combination of graphics and image processing techniques, a dual approach that is becoming more and more popular.

### Conclusion

Technological advancements in both the computer industry and large scale integration of electronic circuits are converging to make raster graphics the dominant display technique of the 1980s. Large scale integration has caused the price of digital memories to decline sharply. Hardware function generators are now available to perform the highly repetitive tasks that characterize most visual display programs. Control and timing functions can be accomplished by versatile and inexpensive microprocessors. The full potential of raster graphics is now within the reach of computer system designers. All of the major benefits offered by the raster scan technique, including photographic detail, selective updating, unlimited range of colors, and cinematic animation, are now economically feasible.

The basic display device for raster graphics is the CRT monitor—a non-broadcast version of the standard television receiver. Decades of mass production experience have refined the receiver, CRT, and raster scan circuits to a high level of reliability and cost effectiveness. Most important, CRTs and monitors are still evolving as commercial products and significant developments can be expected during the next few years. Higher resolutions and increased color capabilities are mandating faster scanning monitors and more precise convergence systems. Self-converging inline CRTs are the subject of substantial research and development, and may become the next generation of high resolution monitors. Ultimately, the availability of 2048- and 4096-line raster scan monitors will eliminate all reasonable concern about resolution and staircase effect.

Questions of technology aside, the human factor remains perhaps the most important variable in every graphics display system design. The two practical purposes of a graphics system are to communicate information to a human operator and to facilitate the operator's response to the displayed information. Features available in raster graphics systems can best achieve these goals.

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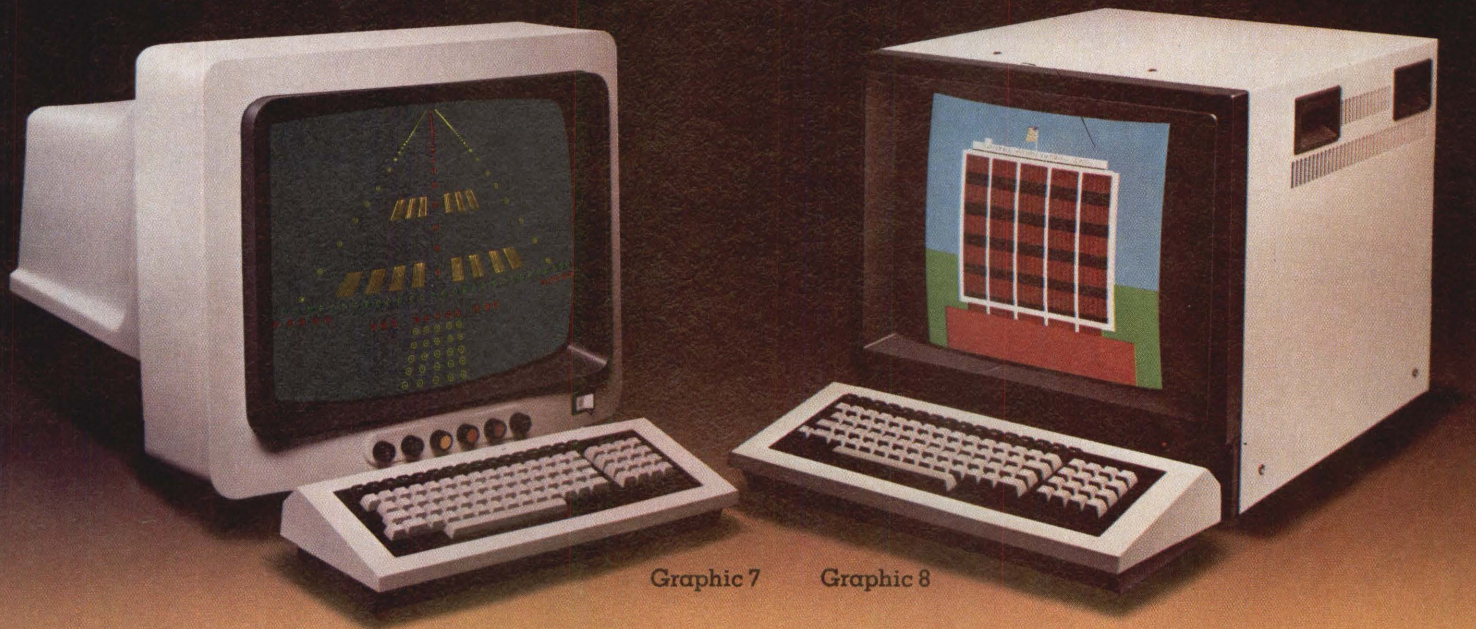

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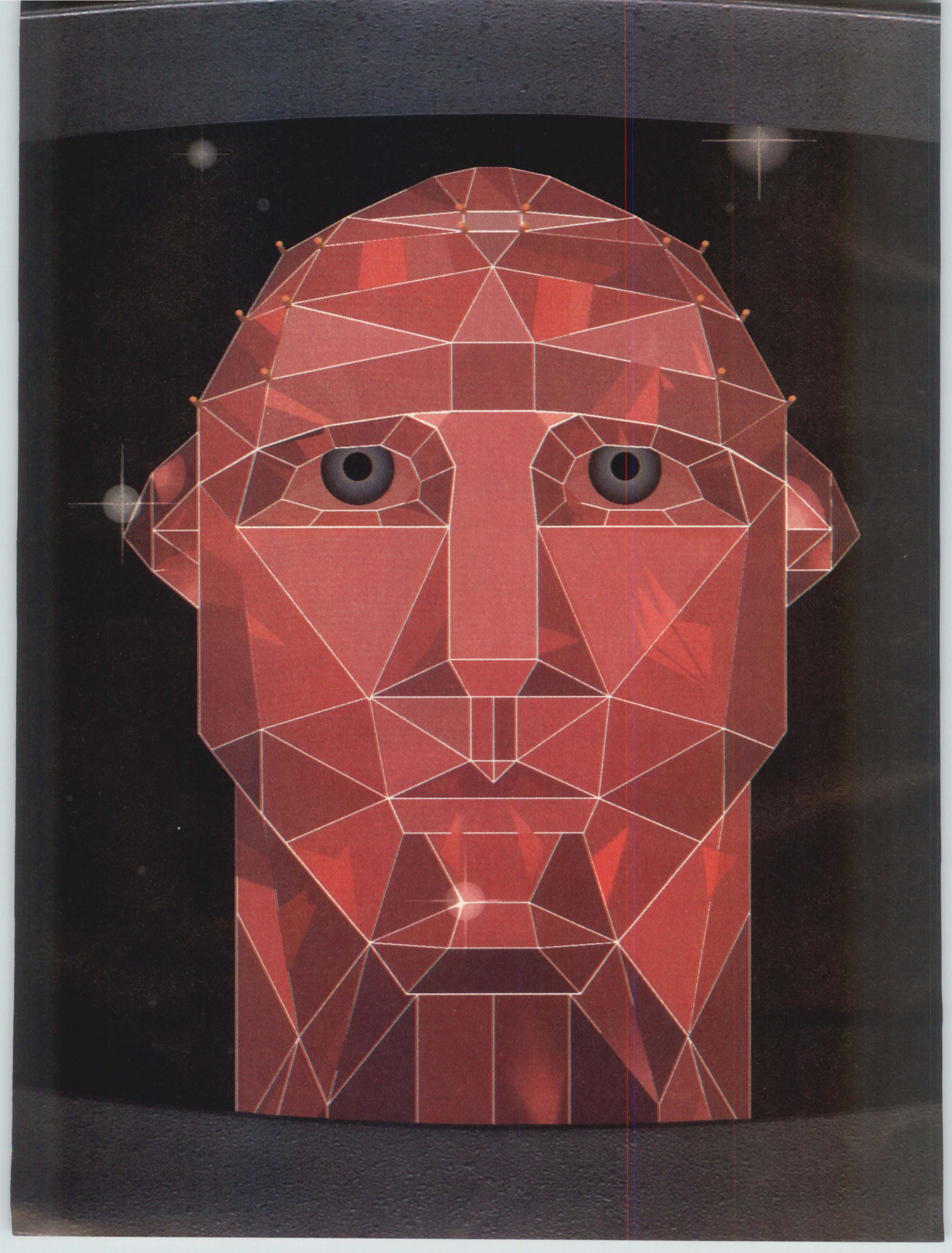

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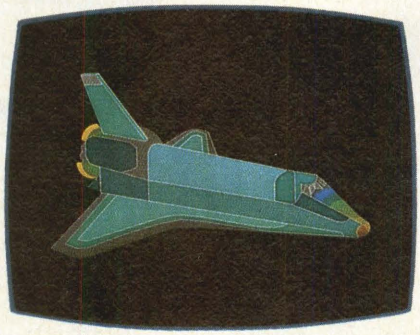

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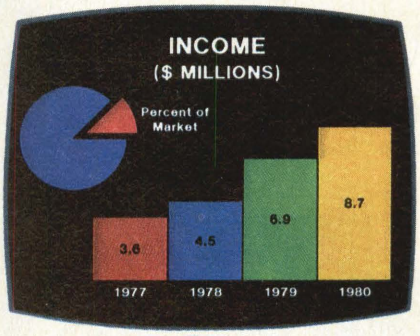


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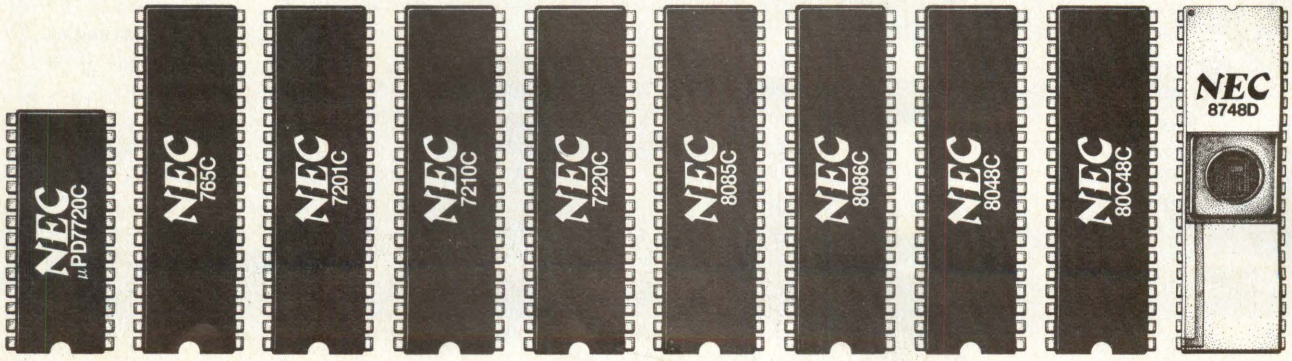

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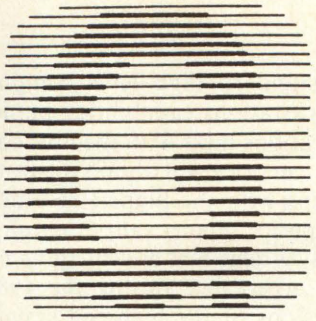

*Shaped by increased demands for high resolution and sophisticated processing capabilities, future systems extend graphics frontiers*

# Trends in CAD/CAM graphics technology

It is no secret that the graphics segment of the computer marketplace is the fastest growing portion of the industry. With independent suppliers scrambling as fast as some of the computer companies to enter the graphics field, it is no wonder that a compounded annual growth rate of more than 35% is predicted over the five-year period from 1979 to 1984. In dollars, this amounts to an increase from the $1 billion in shipments of 1979 to at least $4.5 billion by 1984. In units, this is an increase from 69,000 to 454,000 graphics terminals.

In the 1980s computer graphics is likely to expand in three primary areas: the high-end systems required for sophisticated computer aided design and computer aided manufacturing (CAD/CAM) and multifunction applications; the emerging intermediate or mid-level systems used for broad, general purpose needs; and the new low-end systems, which will provide basic but unsophisticated graphics functions for business and management information applications. Although the low-end business graphics area of the marketplace is receiving much of the current publicity, the market segment comprising CAD/CAM applications is by far the largest part of the graphics industry in terms of dollar volume. Thus, it is in the CAD/CAM area that most of the major technological advances are likely to occur.

The CAD/CAM market probably will benefit most from advances in technology because it is here that the quickest and most cost-effective productivity gains can be made. The reason is that CAD/CAM systems generally are used for automating design, drafting, engineering, and manufacturing tasks. Large savings in time and improvements in productivity are the benefits of using such systems. More lead time becomes available for new product development. Savings result from engineering analysis performed in simulation rather than in trial and error manufacturing, and better quality designs result from greater dimensional accuracy. A more efficient use of materials and a relief in the shortage of skilled manpower also become possible.

### From storage tube to dynamic line drawing

A trend toward ever-increasing levels of sophistication characterizes the development of graphics in CAD/CAM applications. In the past, the storage tube was the most commonly used graphics display in CAD/CAM systems because it was low in cost and provided high resolution and high display density. Eventually, however, a tradeoff for that low cost became necessary because storage tube terminals did not offer multiple colors, were slow

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in drawing screen images, and, perhaps most important, limited dynamic interaction between the operator and the terminal for online design and analysis tasks. The nature of the storage tube requires that once a drawing has been made on the screen the entire picture be redrawn if any part of it is to be changed. Although engineers can draw high resolution designs, their inability to interact dynamically with the screen image and to change it easily for design analysis greatly slows down the design process.

High performance stroke refresh and color raster refresh graphics systems provide interaction and dynamics but usually cost more than storage tube terminals—from $25,000 to more than $100,000. This situation is changing dramatically, however. Of all the terminals shipped in 1979, one-third were high performance displays and two-thirds were medium or low cost storage tube or raster scan displays. Over the next few years, there could be subtle changes in this ratio. One-third of the total could still be high performance, high cost displays, but there will be a noticeable difference in the volume of work that can be done with the new types of terminals. These will gradually replace today's mid-range units to provide new levels of capability for a broad range of engineering needs.

Sophisticated high-end systems costing $25,000 to $40,000 or more will always be required. These systems provide 3-dimensional graphics capabilities with color display, dynamic transformation, and support for a wide variety of sophisticated peripheral devices. They will offer distributed intelligence at the user level and programmability using standard high level computer languages, as well as workstations capabilities employing high speed communications links with the host computer. Users who pay the top price will obtain the fastest and most dynamic systems with the highest resolution available to create the superior quality output required.

The mid-range graphics systems that are emerging now will find ever-increasing acceptance during the 1980s. These will be limited versions of the high-end systems, providing perhaps 75% of their functionality for users who do not need extreme sophistication but want some of their important features. Mid-range systems will offer high quality graphics capabilities but will be priced in the $10,000 to $25,000 range. The key to their acceptance is that they will provide excellent interactive and dynamic features with some local intelligence at this lower price. They may well serve as introductory or beginning systems for first-time users of graphics who want to add this capability to their existing computer systems.

The newest field for graphics is the low-end market, where a large variety of graphics terminals will eventually become available. These units will offer fewer colors with less resolution—perhaps 512 x 512 pixels or less— and comparatively slow picture update rates. Intended for business graphics, management information, process control and monitoring, and applications requiring less sophistication, they will have the advantage of low cost—under $10,000 within the coming year and as low as $5,000 or slightly less by 1983. Such systems will be limited in functionality and will usually consist of just a display tube and keyboard.

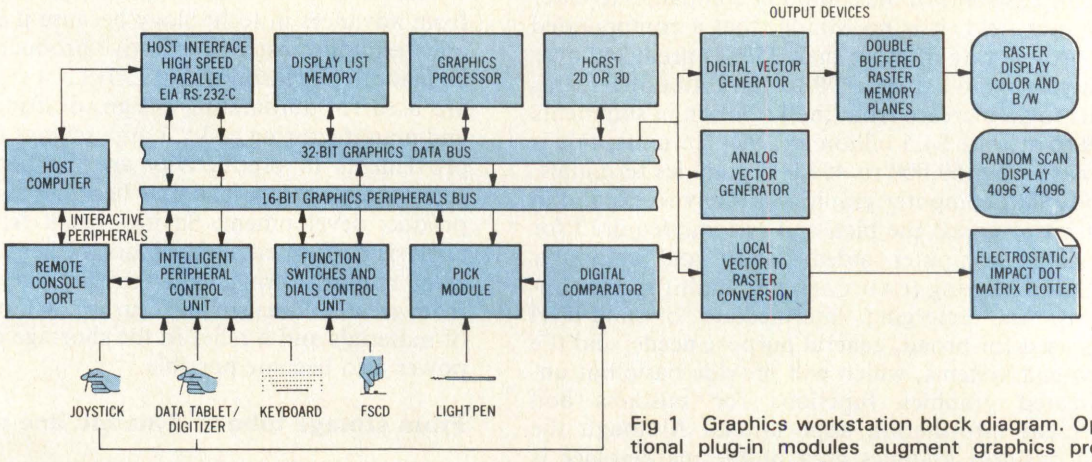


Fig 1 Graphics workstation block diagram. Optional plug-in modules augment graphics processor, host computer interface, and vector memory in CAD oriented "graphics engine" that can drive either raster displays or stroke refresh displays

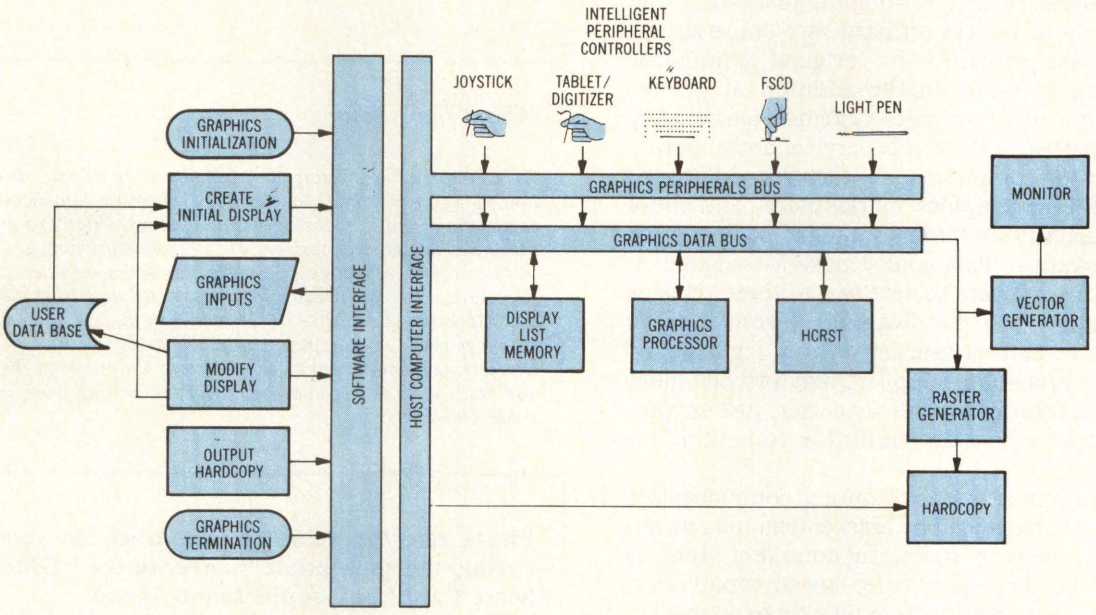


Fig 2 Customizable hardware/software interface. Adaptable operating system and extensible application programs outperform highly specialized, dedicated systems because engineers can tailor their design aids to particular project requirements

## Hardware development

Advances in the semiconductor industry make developments in computer graphics systems possible. Now that 64k and higher density random access memories are available, more memory can be placed in the system. The results are the capacity for larger displays, a reduced computing load on the host, more colors, and better screen resolution. The availability of 16- and 32-bit microcomputers will promote the development of highly sophisticated graphics workstations. Special purpose graphics chip sets will provide more power for less money as well. High production volumes and the resulting economies of scale will only lower prices further, making graphics available to even more users.

An example of this trend is the Graphics Engine™, which consists of a host interface, a display list memory, and a graphics processsor, all capable of driving both raster and stroke refresh displays. To this basic engine may be added various options, in terms of processing power and choice of input and output peripheral devices (Fig 1).

## Software development

In parallel with hardware developments, graphics suppliers will be providing better operating and application software systems in larger quantities (Fig 2). This will tend to encourage the users themselves—not just original equipment manufacturers—to acquire and implement their own graphics systems. Packaged systems will still be sold for specific applications, such as printed circuit board design, but as the user community becomes more familiar with and competent in graphics system implementation, more people will tend to select and configure their own hardware systems and either buy and modify or write their own application software.

Software will also be compatible across the board, thanks to the growing acceptance of the CORE (computer-oriented reporting efficiency) guidelines established by SIGGRAPH. A few hardware manufacturers currently follow these guidelines and make their software usable on all hardware offered. More will follow this trend in the future because it will cease to be merely a nice thing to do—it will become a market requirement. In addition, so-called "universal" software systems which are computer and device independent, such as Megatek's Template™ package, will offer graphics programming capability both to users who have never written applications programs for graphics systems and to those who want sophisticated graphics with minimal software development. These software systems will tend to advance the use of graphics as well because of their portability and device independence.

## Conclusion

Combining the hardware and software trends, the graphics industry will tend to more closely parallel the minicomputer industry of five to eight years ago. The emphasis is likely to be less on hardware and user application software provided by original equipment manufacturers, and more on the addition of greater value by the suppliers of graphics systems—particularly in the form of software, customer service, and support. More of the major computer manufacturers will make new entries into the graphics marketplace, and more graphics software will be sold as standard packages for end user applications. This could cause a shakeout in the graphics industry over the next two to three years as the exclusive suppliers of hardware are forced to leave the business or to concentrate on narrow segments of the market. The remaining suppliers may provide more across-the-board solutions for the end user, just as computer manufacturers now do within the computing industry itself.

Just as the more successful computer companies are those who have stayed ahead of market demands by anticipating needs, the truly successful computer graphics companies will be those that offer broad capabilities. They will be the ones able to adapt quickly to advancing technological developments and offer new products that make use of custom large scale integration to offer more graphics capabilities at lower costs. And they will be the ones who develop new and more extensive graphics software systems for broad use by large numbers of users.


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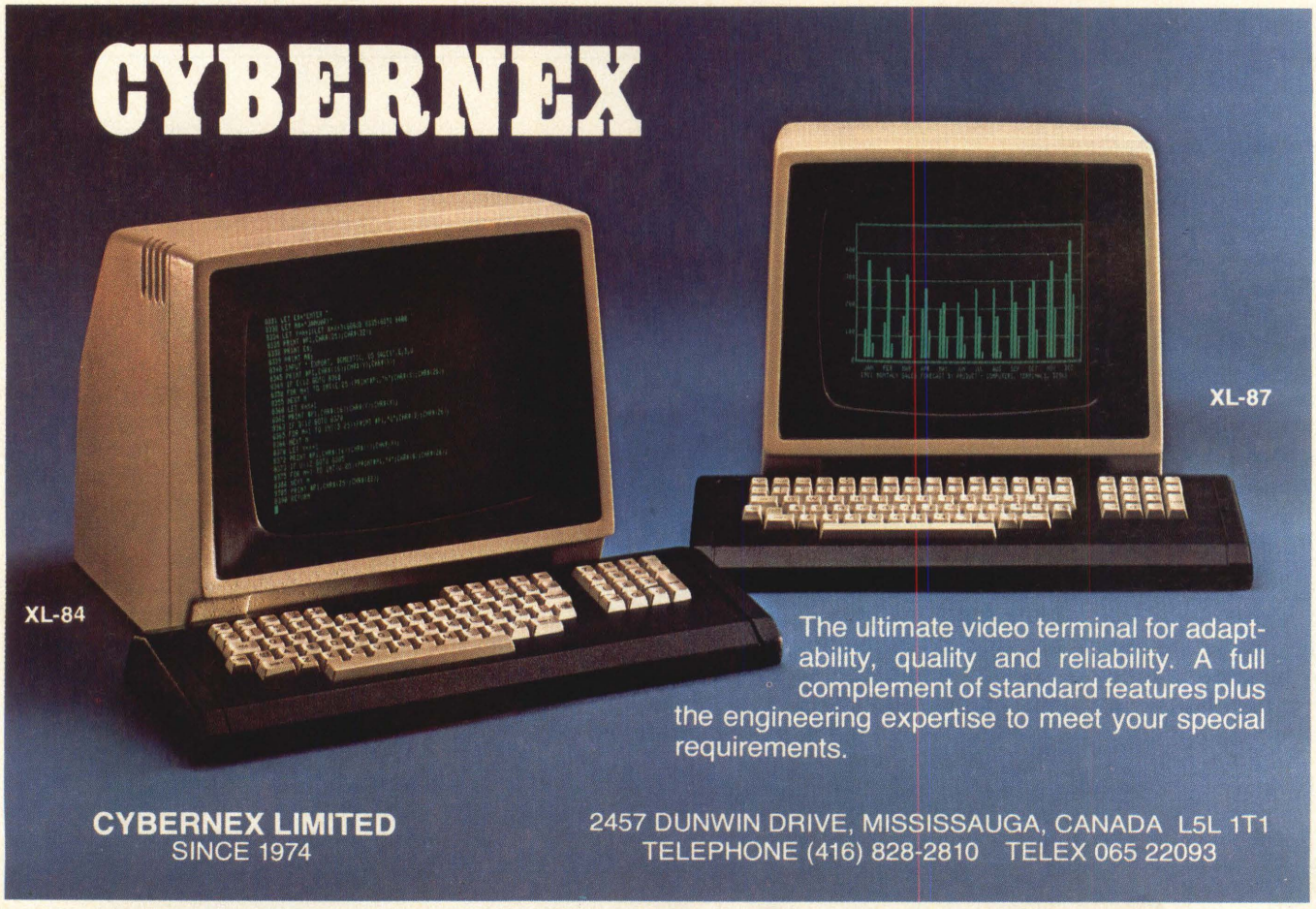

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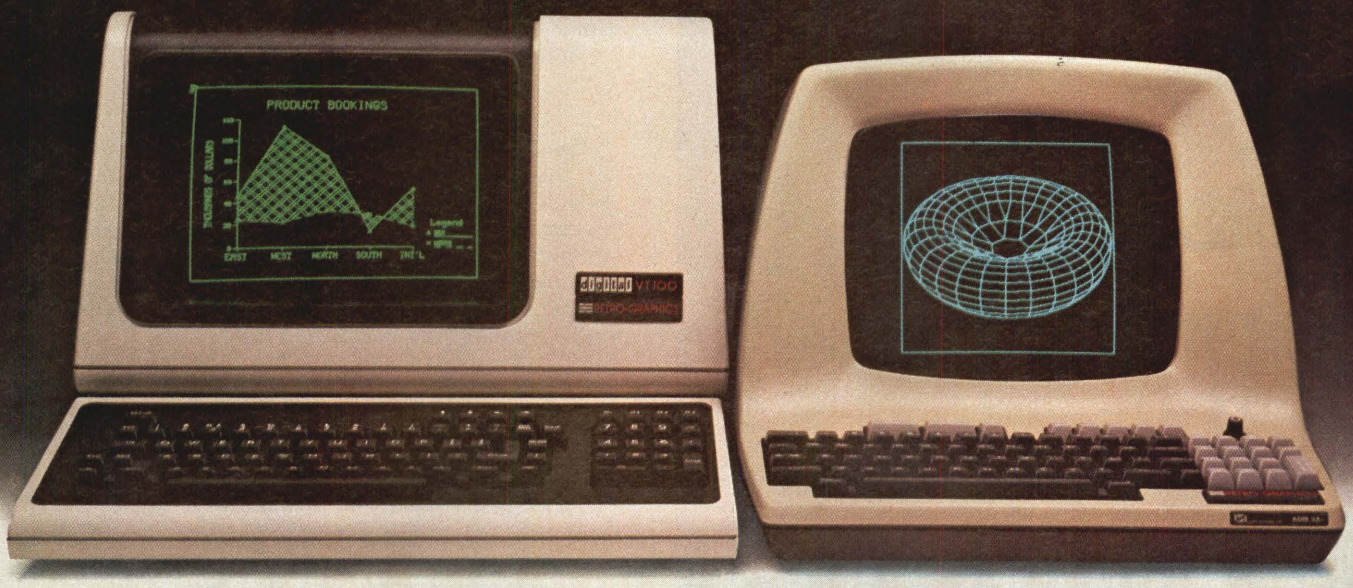


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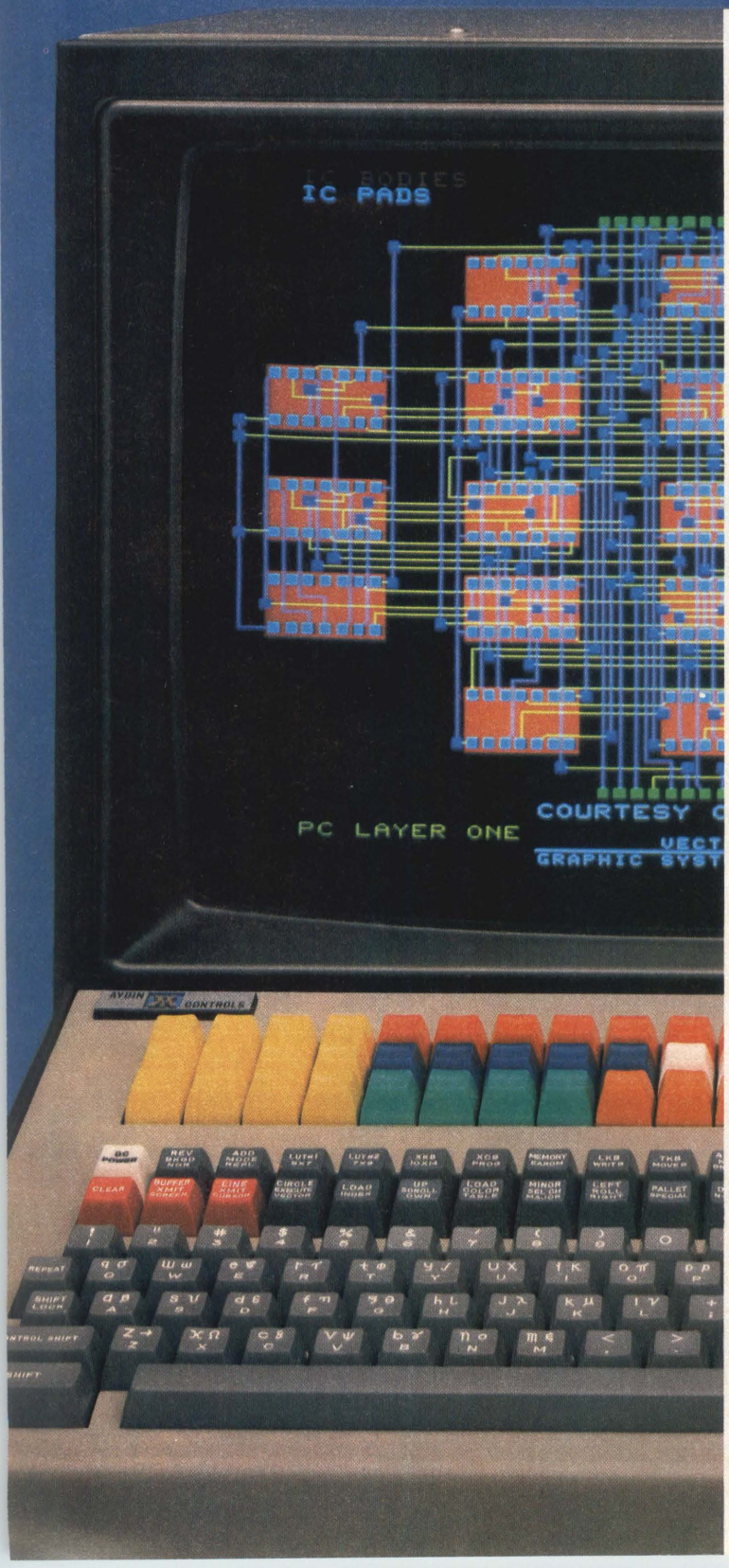


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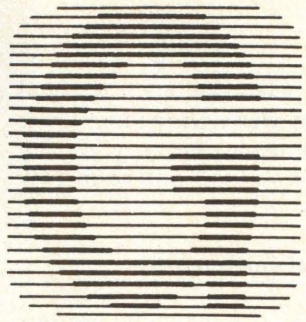

*Multimicroprocessors facilitate the use of both storage display and raster scan technology in a graphics display that offers 4096 x 4096 resolution without increased memory requirements*

# Powerful graphics tool combines refresh and storage capabilities

There are two main display technologies in widespread use: direct view storage displays and raster scan displays. Direct view storage tubes are a special type of cathode ray tube that was first used in laboratory storage oscilloscopes. Electrons impinging on their bistable phosphor excite the phosphor to the background, unwritten state. The phosphor emits very little light in this condition. To write on a direct view storage tube screen, a focused beam of electrons is directed to the desired screen point. The written points, excited by these accelerated electrons, continue to glow and emit light after the beam stops writing. The image remains visible until the entire screen is erased by rapidly placing it in a totally positive state, then discharging it back to the background state.

Raster scan displays, on the other hand, are essentially like a black and white television cathode ray tube (CRT). The beam constantly scans the face of the CRT, usually in horizontal lines; it is this horizontal line spacing that defines much of the resolution of the display. The display is generated by turning the Z-axis beam on to illuminate the line points that make up the display image. Raster scan display resolution is generally acceptable for alphanumeric displays. In fact, raster displays offer distinct advantages for applications such as word processing, because characters, lines, or blocks of text can be inserted or deleted without erasing the display. But the resolution of a raster scan display becomes a limiting factor in applications that involve graphics. The typical raster display is limited to 512 x 512 displayable points, regardless of processor or data resolution. This is especially critical for vectors that are angled across the screen, where the staircase effect is most visible. (See Fig 1.)

Another raster display characteristic is the rate at which the screen information is refreshed. The raster tube does not retain information written to it; it must be rewritten at least 30 times/s to maintain the display without flicker. This requires at least one bit of memory to support each point of the display, or over 250k bits of memory to refresh a 512 x 512 picture element display, and high speed logic to constantly rewrite the display.

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### Storage displays do not have to store

Direct view storage tubes (DVSTs) have some distinct advantages, especially in graphics applications, and a few disadvantages as well—tradeoffs that designers must evaluate as a part of the design cycle. The primary advantage is, of course, resolution; DVSTs offer the highest resolution available. All vectors are drawn from endpoint to endpoint, not approximated on a display matrix as in raster scan displays. A typical 11″ (28-cm) storage display can have 1024 x 1024 addressable points and 1024 x 780 displayable points. A 19″ (48-cm) display can have 16 times as many points available. But supporting a raster display with equivalent resolution would consume almost 17M bits, if such a display device were available. The highest resolution currently

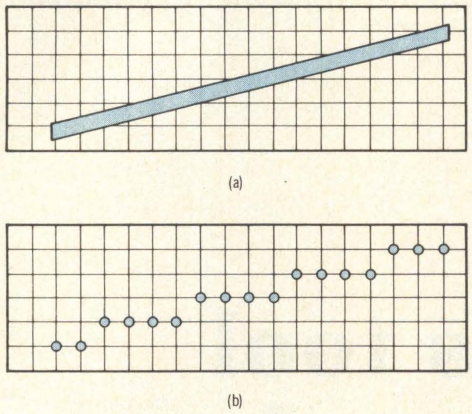


Fig 1 DVST versus raster display. When drawing vector between two endpoint addresses, DVST (a) deflects writing beam in a straight line, creating precise high resolution trace. Raster display (b) can only approximate line by activating predesignated pixels, leading to staircase effect

available is 1024 x 1024 picture elements (pixels), which requires more than 1M bits of memory to support, in monochrome.

A storage display requires far less memory for display support. Once information is written to the display, it remains there without further attention, as long as power is applied to the CRT. While this has the advantage of reduced memory overhead and display control circuitry, there is a drawback. If one part of the picture needs to be changed, even a small part, the entire display must be erased and redrawn. Selective changes, possible on raster displays, are not possible on a stored display.

The 4054 graphics system is a standalone desktop computer with a 19″ DVST display and standard resolution of 4096 x 4096 points. By adding the dynamic graphics option, refreshed, dynamic graphics become a part of the 4054, with the same high resolution. To create such capabilities, the interaction of the CRT phosphors with the writing electron beam must change. That interaction has been studied in detail, in order to achieve the high resolutions available today. Storage displays have improved as writing beam intensity and speed have become more tightly controllable. The questions of how fast to move the beam across the screen and how fast to accelerate the electrons can be looked at with new perspective. The question grows from "How do we maintain 4096 x 4096 resolution?" to "How can we maintain the same resolution without storing, so that the display elements can be moved around the screen?"

In adding refresh capabilities to the display, some vector memory will be required, along with faster display circuitry. But only the pixels that are not stored need be refreshed to remain in view. Once stored, the segments are dropped from the display memory, freeing memory and reducing the refresh load on the display processor.

### Storage and refresh – best of both worlds

Storage is a function of charge, defined as the product of writing beam current density and dwell time, the length of time the beam stays on a position. So, in order to write without storing, there are two possible avenues: the time or the beam current can be reduced. And a further choice occurs if the designer chooses dwell time reduction to achieve non-stored displays. Dwell time can be dropped by increasing the rate of change of charge current to the beam deflection amplifiers, thereby moving the beam across the target faster. Or, pulse width modulation techniques can be used to chop the beam current, turning the beam on and off rapidly.

The best choice combines two of these elements to create a bright but non-storing graphic display. One factor is reduced beam current to reduce the energy directed at the CRT target phosphor. The other element is faster beam deflection. In storage mode, the 4054 writing beam moves at 15k cm/s. When operating in refresh mode, however, the deflection speed is increased to 45k cm/s. This increased speed also limits the energy directed to the phosphor by reducing the time in the charge equation but has an added benefit: the faster deflection allows more refreshed vectors to be displayed

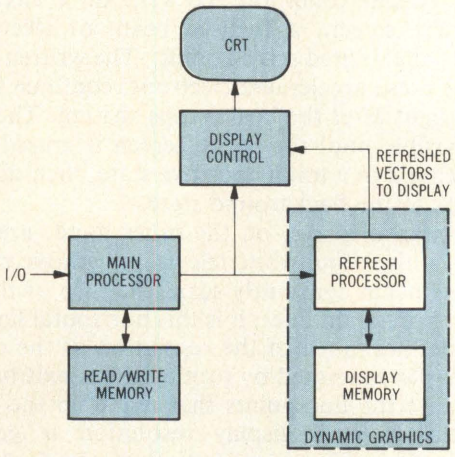


Fig 2 Combined system block diagram. With dynamic graphics, main processor is bypassed by refresh processor to repeatedly draw refreshed vectors on display

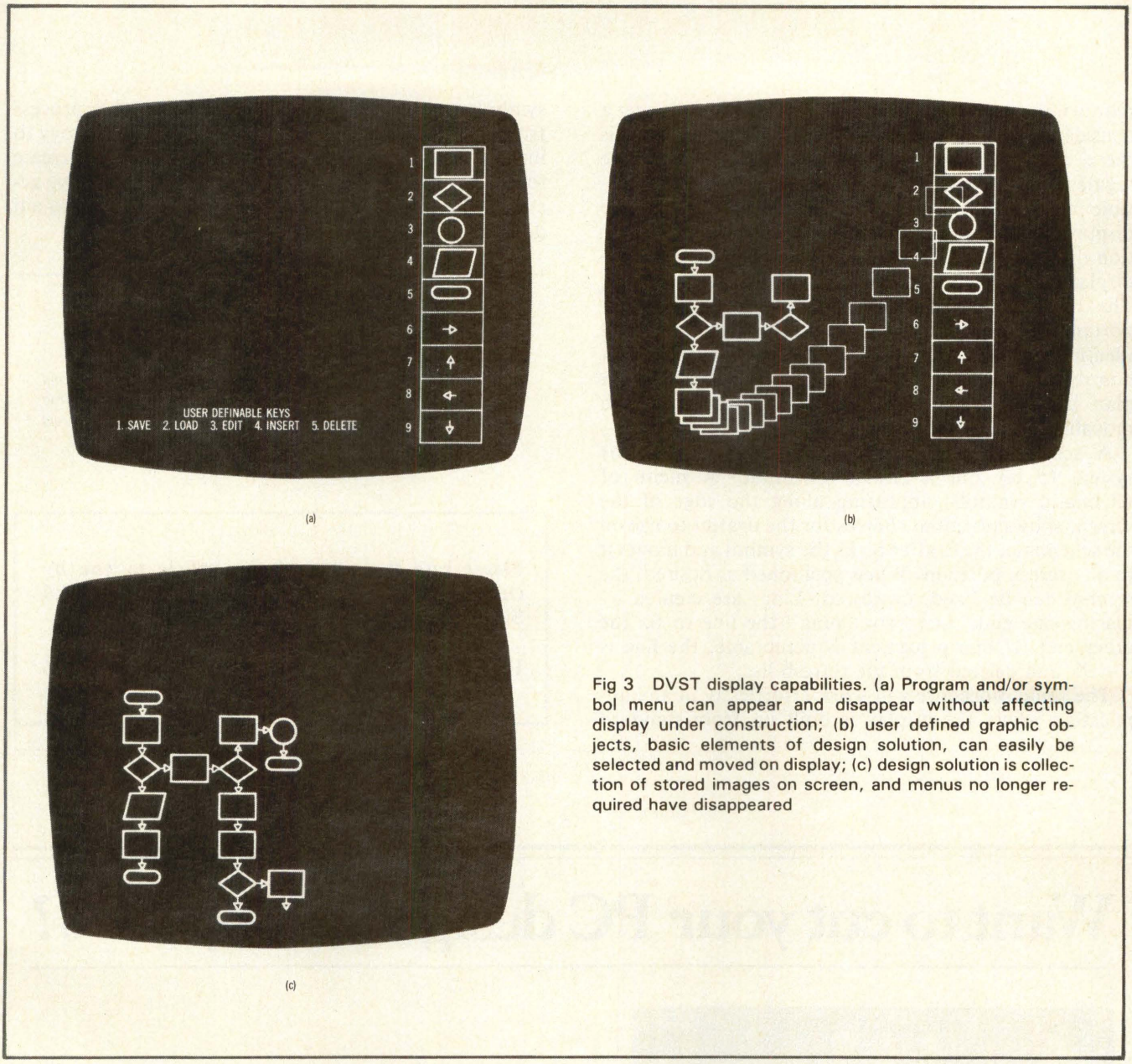


Fig 3 DVST display capabilities. (a) Program and/or symbol menu can appear and disappear without affecting display under construction; (b) user defined graphic objects, basic elements of design solution, can easily be selected and moved on display; (c) design solution is collection of stored images on screen, and menus no longer required have disappeared

without flicker. And vectors can be moved, added, or deleted individually, without erasing and redrawing the display.

In light of the increased vector processing, another factor is important to consider: the 4054 is a desktop computer first, with a high resolution graphic display included. So it is likely that the refreshed display will be in response to calculations from a BASIC program—analyzing the flex and stresses on beams, for instance, or routing an etched circuit board run in its ideal location. Therefore, it is imperative that the display, which requires continual vector rewrite for refresh, do so with a minimum of impact on the system processor.

For the dynamic graphics option, a second dedicated microprocessor was chosen as the solution (Fig 2). This processor is activated when dynamic graphics are needed. Vectors to be refreshed are captured by the high speed display processor and placed in display memory. The system processor no longer needs to handle those vectors; the microprocessor reads them from the display list and rewrites them to the display. At the same time, a signal to the display board tells it to reduce writing beam current and increase deflection speed. Adding the dedicated microprocessor means that the 4054's main bit slice processor is only slightly involved in refreshing the display. The system processor is then free to run its BASIC program performing calculations and adding to or subtracting from the refresh display list as the program dictates.

## Conclusion

Adding the flexibility of refreshed, or non-stored, dynamic displays to a DVST provides a powerful and versatile tool. Added capability of dynamic graphics overcomes the reservation that the whole screen must be

redrawn if even a small part changes. This is no longer a consideration. The high resolution of the storage tube is there, along with the ability to move vectors or picture segments on the screen without storing them. The possible applications for such high resolution dynamic display capabilities are numerous. Almost any application that benefits from the high resolution of a storage display can reap added benefits from dynamic graphics. The combination of display capabilities is especially important, for instance, in areas that rely on output that is identical to the screen display. From etched circuit boards to aerospace, from architectural design to floor plan layouts, the design task is simplified through movable graphics segments. (See Fig 3.)

A schematic drafter, for example, might use the system to lay out a circuit schematic. A menu of schematic symbols, appearing along the edge of the screen, shows potential choices for the drafter to use on the schematic; the drafter picks the symbol and moves it to any screen position. When positioned as desired, the symbol can be fixed, or stored. Lines are created by placing one end, then "stretching" the line to fix the other end. If line placement is acceptable, the line is stored, and deleted from the refresh list.

The same procedure will work effortlessly in any application where the display is built up from standard symbols or components, reducing the graphic process from days to hours. By extending storage technology to include refresh capabilities, DVST designers can create tools for other designers—tools that work quickly, accurately, and productively—thus enabling design to aid design.

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*Terence M. Davis is the editor of* TEKniques, *the applications library newsletter serving users of Tektronix 4050 series graphic computing systems. A technical writer at Tektronix, Mr Davis holds a BA in English from Portland State University.*

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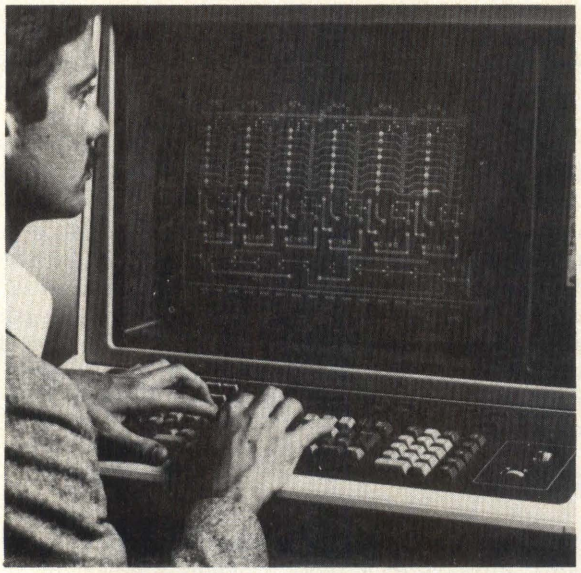

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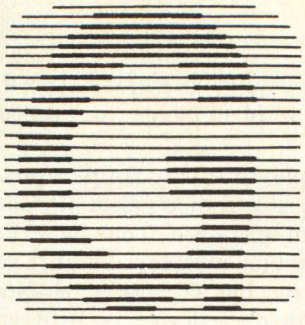

*Bit slice and PLA technology provide a powerful graphics processing system with the characteristics of a general purpose computer*

# Graphics and imaging system offloads host computer

To be viable in today's market, a high performance graphics and imaging system must remove some of the load from the host computer, which is already overburdened with the complexity of systems tasks. At the same time, the graphics system must provide a high level of interaction between the user and the display to meet the rising demands of current applications. The graphics system itself must contain the hardware required for ultrafast processing, as well as programs for interaction; in other words, it must be an advanced design, special purpose computer with the characteristics of a general purpose processor.

One such computer, called an advanced display computer (ADC), has been designed as the central processor for the G-6000 raster graphics display series. Although the initial series offering is described as an ideal computer aided design/computer aided manufacturing (CAD/CAM) configuration, the ADC promises even more important implications for the industry.

As a bit mapped raster scan system, the G-6000 retains the inherent benefits of raster including moderate cost, a wide range of selectable color hues, continuous shading capability, and the ability to display a large number of vectors. At the same time, the raster system is, by definition, memory intensive. The location of each picture element (pixel) must be written into memory individually. In a 1024 by 1280 system, this means 1,310,720 memory locations/plane. Obviously, increasing the number of functions and the speed with which such functions are performed is a formidable task in raster graphics.

ADC architecture enables instruction execution times as low as 160 ns with byte transfer rates to 3 MHz—believed to be more than twice the speed of the nearest raster competitor and comparing favorably with more expensive strokewriter systems. In addition, the ADC provides for more than 140 mnemonic instructions through the central processor and a 39-mnemonic instruction set in the graphics controller. It attains speed and flexibility in a single graphics processor that can exceed the performance which, until now, has required three separate processors to handle host interface, interactive input/output (I/O), and graphics displays.

Principal elements of the ADC are a central processing unit including program memory; a graphics controller; the host computer interface; and a multi-active system I/O bus. Each subsystem was designed to meet the requirements of high speed graphics application to complete many jobs rapidly. In so doing, the ADC overcomes the speed throughput limitations encountered with single-chip, off-the-shelf microprocessors. (See the Figure.)

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## Bit slice/PLA architecture

Architecture of the central processor combines a bipolar, bit slice arithmetic logic unit (ALU) with a

"direct decoding" programmable logic array (PLA). While other systems have used bit slice design for graphics generation, the ADC employs it for computational processes, which contributes significantly to the exceptional speed of the computer. Choice of bit slice over off-the-shelf 16-bit (or even 32-bit) microcomputers was an essential design decision. General purpose microcomputers necessarily provide a number of addressing modes that are not required for graphics applications and that slow processing speed. In a 16-bit integer division instruction, for example, a 68000 microprocessor might require 15.9 μs to perform the task, while the ADC processor, designed primarily for graphics computation, requires only 4.08 μs.

PLAs were selected for their high speed instruction decoding capability. Whereas the use of traditional microcode programmable read only memory (P/ROM) requires a first level of "code cracking" to shrink the number of bits per instruction to a manageable size (entry of a 16-bit instruction into P/ROM would require 65,535 memory locations for decoding), the wider 16-bit input word of the PLA eliminates the need for instruction parsing. The PLA can perform complete decoding in 25 ns, and makes possible the execution of many instructions in one cycle time (160 ns).

### Resident data storage

To put more of the host computer characteristics into the graphics system also requires substantial program data storage. Graphics displays employ extensive data lists which describe, in encoded form, various graphic entities such as vectors, circles, areas, and characters. In the past, most raster graphics systems did not have the capacity to store large data lists and, hence, the host computer was required to take on this burden. The ADC provides for this by containing up to 128k bytes of data and program storage. Standard configuration offers 8k words of P/ROM and 16k words of random access memory (RAM), while optional 64k memory chips extend the RAM capacity to 56k words. Future options will extend capacity to as high as 1M words. The large memory resident in the system further impacts its speed. Increased interactivity and modifications to data attributes such as scale, translate, and rotate are possible at high speed because there is no time delay while modifications are made in the host and then communicated to the display.

### Powerful instruction set

To implement its speed and capacity, the ADC offers a set of more than 140 instructions. Among these is a powerful block transfer capability that allows the transfer of up to 64k words with a single command at speeds as high as 3 MHz. Routing of the block transfer may be between the external host and the ADC computer memory, between the computer memory and graphics refresh memory, or between the external host and the refresh memory. This flexibility makes it possible to load an image into refresh memory at memory speed. For example, a 640 x 512 x 16-pixel image can take as little as 500 ms to load.

In addition, blocks of display list data can be stored on a graphics system peripheral and then paged into the ADC memory at high speed. In operation, it can have the effect of an even larger computer memory. Because of the system's bus structure, the block transfer of data from an I/O device to any other I/O device, or between memory and a device, can be accomplished without any special I/O control logic. Among the system's other instructions are both multiply and divide commands that can be performed in under 4 μs; single- and double-operand; extended branches/calls/returns; programmed flags; multiple shifts; stack operation; programmable traps; and interrupt service.

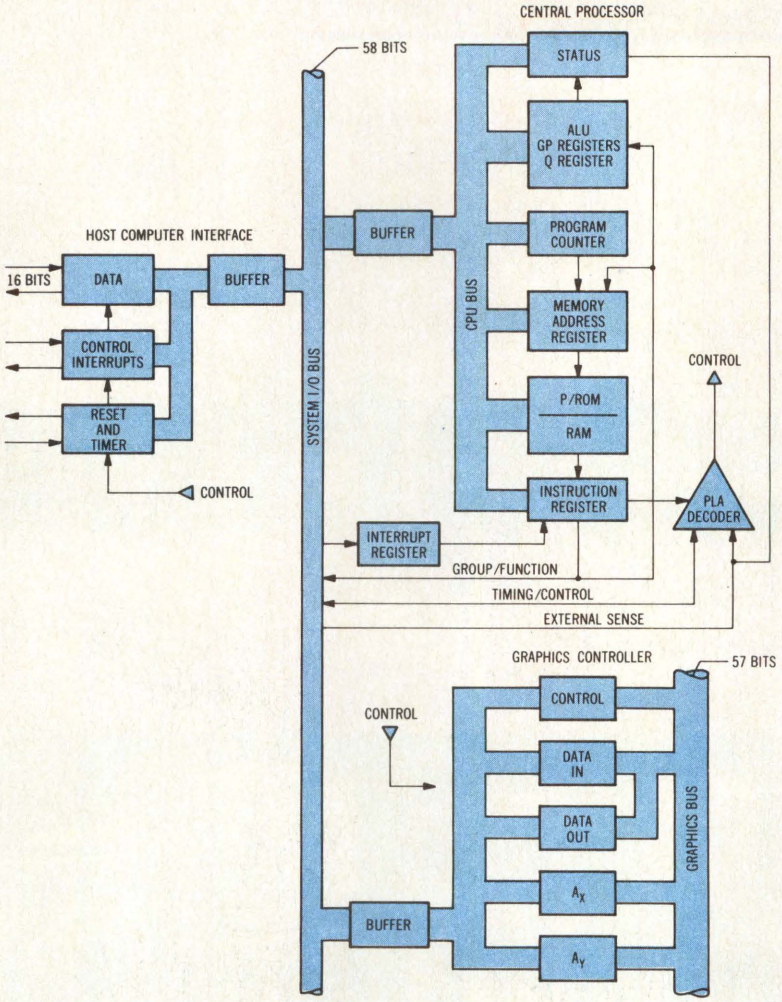
The interrupt service includes 16 automatically vectored, priority selectable interrupts with masking capability. These have an automatic trap response that stores the current contents of the program counter and status register and replaces the information in these registers with predefined values. Interrupt speed is 1.4 μs. In addition to the interrupt lines, the ADC also has 16 external sense inputs that provide a lower level event flagging at a slower speed. This large number of event flagging lines is extremely useful and effective in large multistation interactive graphics and imaging systems.

### Multi-active system I/O bus

One interesting design feature of the ADC is the I/O bus structure. As can be seen in the block diagram, the computer actually employs a separate host CPU bus and graphics bus, both of which access the system I/O bus independently. Much of the system's speed and flexibility can be attributed to this design. Other features of the controller are interrupt on a memory address error for dynamic window clipping and 39 instructions, including automatic X,Y update, repeat operation mode, block transfers, and automatic packing and unpacking of data words.

### Host computer interface

The host computer interface separates the system I/O bus from the computer interface. It is cabled to an interface board at the host computer. The 16-bit I/O bus allows easy adaptation to the I/O structure of most major minicomputers, and supports block transfers at high speed when a standard direct memory access interface is present in the host computer. The computer interface has a 3-state buffered data path with bidirectional interrupts and simple handshaking signals. A built-in watchdog timer can reset the system if a function is not completed within a given time. To meet diversified requirements, the system I/O bus is designed to allow fast, simple interfacing to an array of I/O devices such as discs, printers, array processors, and even additional hosts.




Block diagram of advanced display computer. Central processor and graphics controller interact with one another and host computer interface via system I/O bus

## Software

Software currently available for the G-6000 includes a graphics operating system resident in the 8k P/ROM. This operating system consists of an executive monitor and a number of subroutines that provide the basic operations. The system performs 2-dimensional transformations, absolute and relative addressing, and a full range of primitive constructs including point, vector, circle, arc, and rectangle. Other instructions include polygon fill, alphanumerics, multiple raster writing modes, incremental vector, multicursor tracking, fast image write, and system control functions including color/monochrome lookup tables, hardware scroll and zoom, double-buffered refresh memory, overlays, and interactive peripheral device control.


*About the Authors:*

*Dan Jones has managed the Applications Engineering Group at Genisco Computers for two years. An electrical engineering graduate of the University of California at Los Angeles where he specialized in radio communications and radar, Mr Jones later worked with missile guidance radar at Raytheon, and in Supervisory Control and Data Acquisition (SCADA) at Wescom before joining Genisco.*

*John Fletcher has been with Genisco Computers for three years. Coming to the company with over twelve years of experience in computer graphics products, Mr Fletcher was recently appointed Product Marketing Manager. He is responsible for marketing programs of computer graphics terminals and new product development.*



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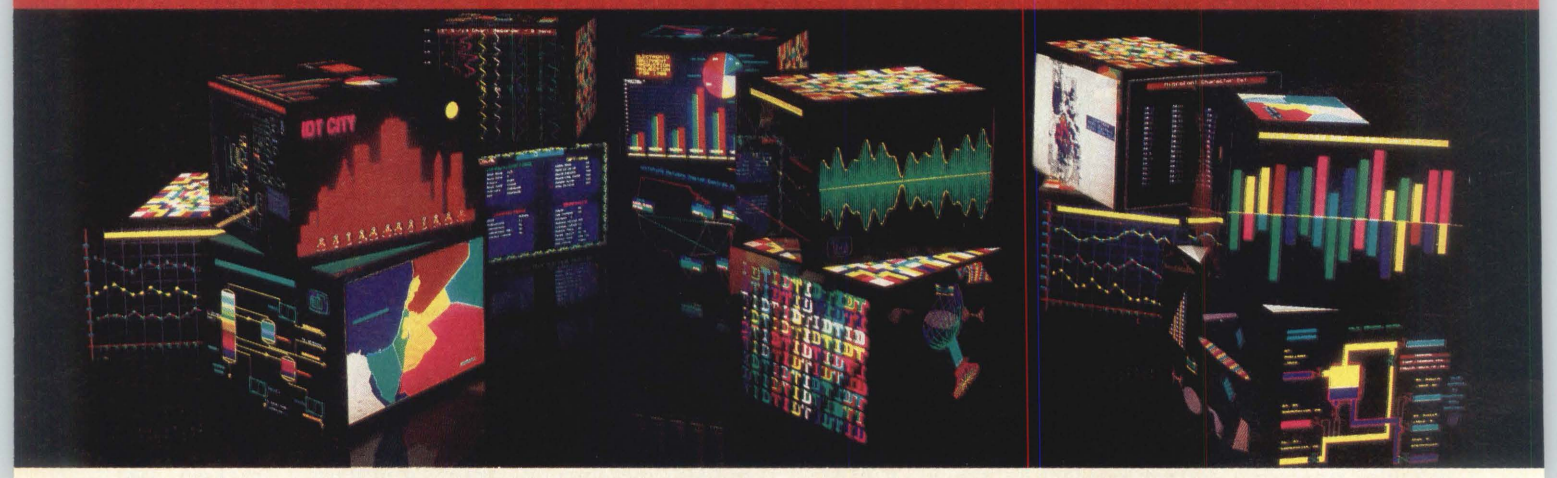
# Pacesetter.

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PRODUCT TECHNOLOGY

# Memory organization and high speed processor facilitate unique image display capabilities

The IP8500 image display and processing system is intended for remote sensing, nondestructive testing, 3-dimensional computer graphics, or any application calling for high resolution color, multi-image monochrome, or pseudocolor displays. Compatible with Digital Equipment Corp (DEC)* PDP-11 or VAX systems, the IP8500 can be interfaced to most popular minicomputers and features advanced concepts in pipeline processing and high speed data transfers from a host computer memory or directly from disc. Each of its up to 20 512 x 512 x 8-bit memories features integer zoom, pan, and independent intensity transformation tables. Optionally, the system can be equipped for distributed processing or standalone operation. A variety of interactive devices is available, including trackball, joystick, and lightpen. A single system can support 4 color or 12 monochrome users.

### System features

Each image display and processing system (IDPS) may have up to 20 image memories with 16 assigned to display channel output and 4 used as scratch channels for arithmetic operations or temporary image storage. A full system can store a 1024 x 1024 x 32-bit image with graphics and alphanumerics and display a 512 x 512 image window. Each memory module consists of 256k bytes of metal oxide semiconductor random access memory (MOS RAM), input and ouput (I/O) selection logic, zoom control, output address registers for X and Y pan (scroll) control, and a selectable intensity transformation table that can be loaded as a block of 256 bytes or altered on a byte by byte basis. A module stores 512 elements by 512 lines, with each pixel consisting of 8 bits of data, and has 5 control registers accessed by the host computer.

From 1 to 4 display channels of from 1 to 16 memories each can be supported, interfaced to a video control and video output capable of driving a red/green/blue (RGB) color monitor with three composite video signals. In addition, each display channel can have an optional alphanumeric overlay generator for producing annotation over the image window as well as in the margins on either side of the image window, and a cursor generator with its associated joystick, trackball, or lightpen.

Each display channel can be configured as a single 512 x 512 x 8-bit monochrome or pseudocolor display, a 1024 x 1024 x 24-bit (8 bits for each primary color) display, a 2048 x 2048 x 8-bit display with a 512 x 512 image window or any subset of the above that is an integral combination of the 512 x 512 image memories. In addition, each display channel includes a set of logic to configure image memories into a display channel; select and control overlay memory, cursors, and alphanumerics; and provide video output for an RGB monitor. Any or all of the 16 image memories can be selected as inputs. Image data are then modified by a lookup table (LUT) of 256 x 8 bits with the table's 8-bit output transformed into an analog video signal by an 8-bit digital to analog converter (DAC). Each of the three outputs has four selectable 256 x 8-bit LUTs controlled by

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**Kendall Dinwiddie**
DeAnza Systems, Incorporated
118 Charcot Ave, San Jose, CA 95131

register selection, split memory register, or overlay memory control.

All overlay functions (cursor, alphanumerics, and overlay memory) can be enabled or disabled in the video output control (VOC), which also contains the logic to select the visual appearance of the overlay functions. When the VOC selects a memory channel (512 x 512 x 8 bits) as overlay, the 8 bits of this memory plus the two cursor generators are summed as the 10-bit address, with the cursors being the two most significant bits, of a 1024 x 16-bit overlay function table (LUT).

These 16 bits are divided into three groups of 5 bits, each controlling an individual video output (red, green, and blue). The 16th bit is gated with a blink clock to achieve a blink (on/off) of the overlay, cursor, or alphanumeric function. (The other three groups of 5 bits each are identical.) The most significant bit is an on/off control and the least significant 4 bits form a 16 intensity level replacement of the selected image channel. Overlay and cursor priority can be controlled by loading the overlay LUT with the desired data; the relative priority of the alphanumeric overlay can be selected with a control bit in the VOC.

### System options

The IDPS can be optionally equipped with a separate alphanumeric overlay generator, as previously discussed, for each video output control to a maximum of four. Each alphanumeric generator includes a 2k-byte ASCII storage memory and 64-char (uppercase) read only memory (ROM) character generator. The characters, formed on the fly from the ASCII code stored in memory, are formatted on the screen as 80 chars/line by 25 lines. The characters have a 5-element by 14-line font in an 8-element by 20-line matrix. Two control bits included in the 8-bit byte defining a character specify the character color and reversed background. A control bit in the VOC can inhibit the background matrix so that only the font data are visible on the screen.

Another option is the high speed pipeline digital video processor (DVP) that operates on a combination of 512 x 512 x 8-bit memories and allows realtime (one frame time) operations such as multiply, add, subtract, compare, and reciprocal divides. The DVP performs 16-bit fixed point arithmetic operations to facilitate such operations as convolution, correlation, edge detection, edge enhancement, image merge, and many other normally used image enhancement algorithms at speeds up to 7880k operations/s. The DVP contains four 8-bit realtime multipliers, a 36-bit arithmetic logic unit (ALU), a 32-bit shifter, and four 8-bit test ALUs structured in a pipeline to provide realtime arithmetic functions on 512 x 512 x 8-bit arrays. This input to the DVP can come from any of the image memories, 3 possible 8-bit video digitizers, or 12 function table outputs from the VOC. A 4096 x 16-bit programmable function table is also implemented in the DVP feedback loop to perform special 16-bit table functions on the data in real time. A comparator for testing the minimum and maximum values in one frame time is logically positioned between the arithmetic section and the shifters and function table to provide output clamping to selectable limits for 8- or 16-bit unsigned magnitude or 2's complement numbers. Input selection provides for 64 bits of simultaneous input variables (8 sets of 8 bits) and 32 bits of output. Output can be routed to four 512 x 512 x 8-bit image memories simultaneously.

Each display channel can also be equipped with a dual cursor generator with independent X and Y position register that can be altered by the interactive device connected to it (joystick, trackball, or lightpen) or by the host CPU. The visible cursors have eight 1-dimensional forms consisting of full-screen horizontal and vertical (pixel) pairs and full-screen crosshairs. All 1-dimensional modes can be solid or dashed (or dot where X and Y intersect); 2-dimensional modes consisting of outline or solid boxes defined by a cursor pair are selectable, and the two cursors may be programmed by the user to contain any special form that can be contained in the 64 x 64 programmable matrix. When used in the programmable matrix mode, position 32, 32 becomes the target element.

### Data transfers

In the standard IDPS, data transfers to and from the display are accomplished either through a single data register or through a data window assigned in 512-word blocks as UNIBUS memory address with up to 256 blocks for a total of 128k words. A third, optional method interfaces the display system to most computers through a direct memory access (DMA) control board at a transfer rate of 1.5M bytes/s.

The basic transfer mode is initialized on power-up and is used for data being transferred via the data register, located in user I/O space on a DEC PDP-11 UNIBUS. This mode is useful for single-word transfers of data or commands. The data window mode allocates up to 256 512-word pages of DEC UNIBUS memory to allow DMA to the image memory. The DMA mode of transfer is accomplished with an optional DMA interface card that contains the word count and address registers and allows block transfers up to 65k bytes of data.

*About the Author:*

*Kendall Dinwiddie is product manager of Image Products at DeAnza Systems, Incorporated, in San Jose, California. He has been involved in minicomputer system design, most recently as manager of Software Development. He holds a BSME from California Institute of Technology and an MSME from Stanford University.*

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**High 740** **Average 741** **Low 742**

# DAWN OF THE EVANS & SUTHERLAND PS 300

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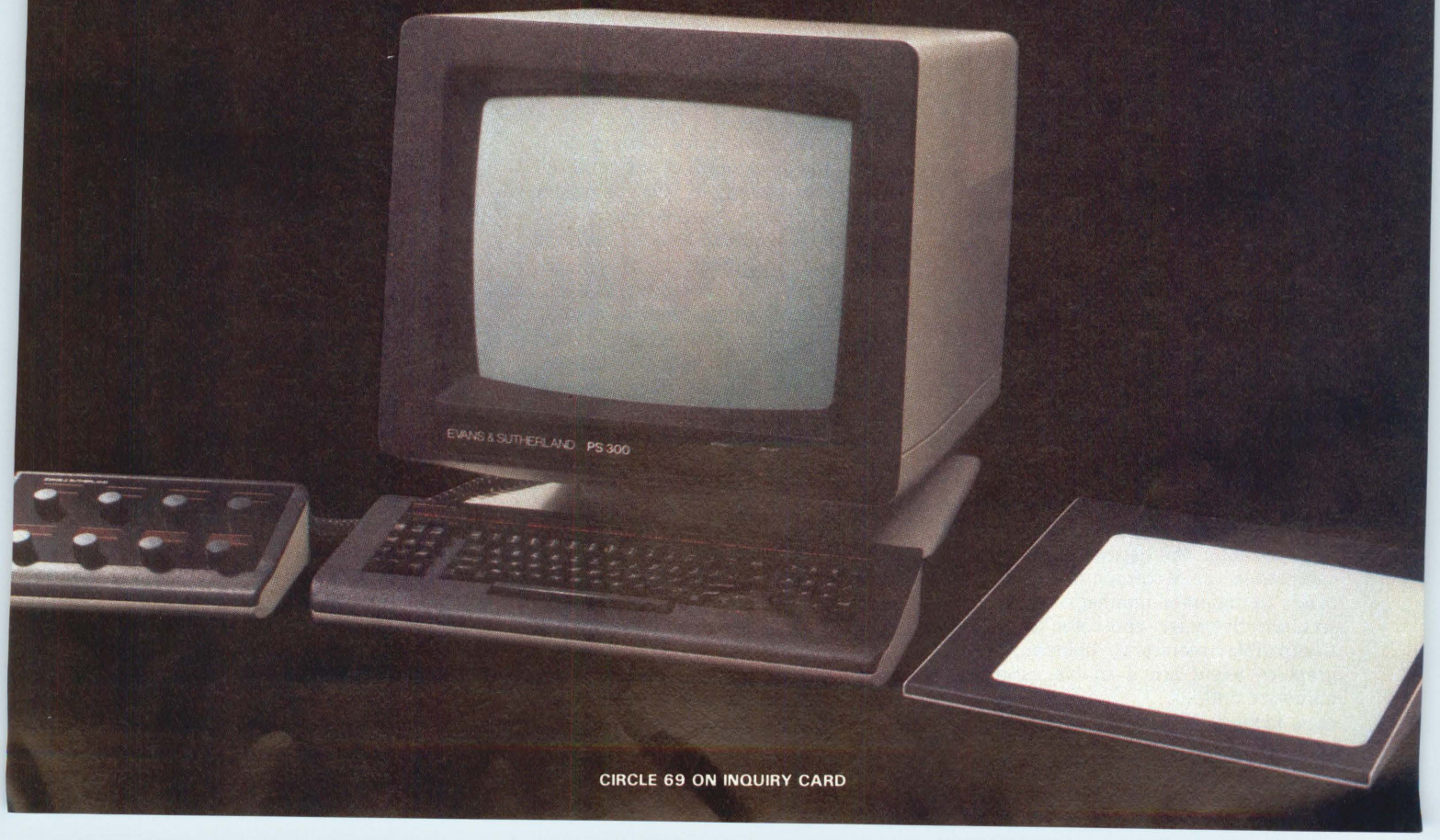


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## GRAPHICS SOFTWARE

### HP 1000 adds graphics capability, supports graphics peripherals

GRAPHICS/1000-II software is used by HP 1000 realtime computers to increase support for a range of graphics peripherals, and to add interactive and 3-dimensional design capabilities. The software, developed by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, initially includes a device independent graphics library (DGL) and an advanced graphics package-3D (AGP-3).

DGL is a 2-dimensional package that enables the use of different graphics peripherals by means of a common set of commands, without programming changes. It requires minimal memory space and system overhead. The package is made up of graphics subroutines that may be called from FORTRAN, Pascal, and Assembly language programs. A 3-dimensional package that builds on DGL to enable users to communicate interactively with graphics peripherals, AGP-3 is made up of a set of subroutines that are called from user programs and a workstation program that processes graphics commands concurrently with a user program.

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### Graphics interface/software allow S-100 computers to emulate 4010 terminals

A graphics interface and software package, available from Cambridge Development Laboratory, 36 Pleasant St, Watertown, MA 02172, enables S-100 microcomputers to emulate Tektronix 4010 series terminals. The raster scan Tektronix emulator provides 640 x 512 raster graphics in black and white, gray tones, or color. All hardware is S-100 bus compatible. CP/M compatible software offers an unlimited number of character sets, selective erase, and color selection. Compatible monitors, lightpen, and graphics BASIC are available as other hardware options.

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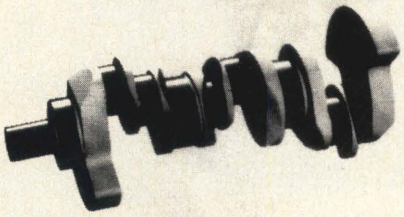
### Graphics system provides 3-dimensional description of solid objects

System uses simple rules to automatically combine elementary geometric solids such as cones, cylinders, and spheres to design solid mechanical parts. GMSOLID software is being developed by Dr John W. Boyse of General Motors Corp Research Laboratories in Warren, Michigan, and a team of engineers from the manufacturing and engineering staff.

In a paper presented earlier this year to the Congress of the Society of Automotive Engineers, Dr Boyse said, "Our graphics system provides a complete 3-dimensional computer model of a mechanical part. This is a significant technical advance over the current system that represents surfaces with a network of lines like a wire mesh.



"GMSOLID provides for a complete 3-dimensional description of the solid object to be stored in the computer memory," he said, "and is exactly what we need to significantly accelerate the design and manufacture of chassis, power train, and component parts. Because the object is stored as a solid, properties such as volume, weight, and moments of inertia can be calculated; and hidden line removal when displaying pictures of the part is automatic."

Programming was designed for maximum ease of use by the design engineer, with particular attention paid to the human factors aspects of the software. Working with lightpen, the engineer chooses from a menu on the bottom portion of the screen showing primitive solids needed and the combining operation used to shape them. A key to the system's interactive capability is the speed of the display response. Pictures are built up in seconds compared to the minutes needed by other systems.

### Graphics software adds blanking system, improved character generation

DISSPLA[R] software from Integrated Software Systems Corp, 4186 Sorrento Valley Blvd, G, San Diego, CA 92121, has been updated to include a blanking system that eliminates confusing and overlapping lines, curves, or annotation on high quality charts and graphs. This revision also provides improved character generation and type selection for annotation and other text portions of graphics presentations, a virtual storage system that reduces memory requirements, extended mapping capabilities, and other quality enhancing features.

Graphics elements such as horizontal and vertical bars, curve symbol markers, pie charts with exploded segments, shaded curve areas, and high resolution characters may be protected from intrusion by other figure elements through the blanking system. This system also allows the user to create blanked areas within perspective drawing projections with blanked areas automatically conforming to the perspective.

Text treatment features include improved spacing of characters in annotation, including compensation for optical illusions, Helvetica-like shaded type fonts, call-up of hardware characters to take advantage of built-in intelligence in the graphics output device, and European character sets. Similar to a virtual memory operating system, the virtual storage system records data on disc instead of in main memory; these data are then paged into real memory as required, reducing program size and optimizing memory resources.

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### Color graphics software facilitates image development

Slidemaster provides an added level of user oriented convenience to the company's high resolution graphics system that can be used to display color or black and white images with up to 756 x 482-point resolution on a high quality RGB monitor. The package, from Cromemco Inc, 280 Bernardo Ave, Mountain View, CA 94043, facilitates development of graphics for business statistics, illustration, and for medical imaging, circuit design, or architectural drawings.

*(continued on page 120)*

# Image processing systems
# Modular graphic display systems
# Frame buffers–Television monitors

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All systems are available in both U.S. and European versions, with plug-compatible interfaces to most minicomputers (including DEC, Data General and PRIME). Proven system designs ensure reliability, and an expanded FORTRAN library and driver package makes operation easy.

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With the software, a user at a workstation with graphics capability and a digitizing tablet and pen can create images interactively. Users can choose from more than 75 design functions listed on a menu on the digitizing tablet. Pictures being created appear on the monitor. Images may be stored on or retrieved from disc by pressing the pen to the tablet. Graphics and text being generated can be erased, changed, moved, enlarged, or manipulated in various ways. The menu provides pen and brush selections, color pallet, capability to generate circles, ellipses, lines, text, and zoom and pan functions.

Depending on the hardware configuration, users can build up to six full 48k images at once, moving parts of any one to another. Backup buffers reduce the possibility of unrecoverable errors, allowing users to have from one to six images in RAM for instant recall; hundreds more can be stored on disc.

**Circle 404 on Inquiry Card**

## Package offers full device independent graphics support for PDP-11 systems

A DI-3000 version tailored for DEC PDP-11 computer systems has been announced by Precision Visuals, Inc, 250 Arapahoe, Boulder, CO 80302. Running on any PDP-11 system with at least 128k words of main memory, the software is compatible with FORTRAN IV PLUS versions 2 and 3 under RSX-11M, RSX-11M-PLUS, and IAS operating systems. All graphics devices available with DI-3000 are supported through standard device drivers customized for the target operating system.

The system is implemented as a collection of intercommunicating tasks. This design, coupled with modular overlay structures, provides support for multiple, concurrent graphics devices and maximizes address space available to an application program. The software is an integrated package of FORTRAN callable subroutines that offers full-color, 3-D area fill and patterning, snapshot debugging, and picture library features.

**Circle 405 on Inquiry Card**

## Software adds 2-D, 3-D graphics to Apple II computers

Multidimensional graphics capability for Apple II computers is offered by Apple-Graphics II from Apple Computer Inc, 10260 Bandley Dr, Cupertino, CA 95014. Designed to help software OEMs and private software developers prepare computer programs that require the generation of 2- and 3-dimensional graphics, the program enables computer users to see a multidimensional object from any angle.

In addition to its multidimensional capability, the package enables users to call up a full-screen view of any portion of a drawing, with no degradation of picture quality, for detailed study. For demanding applications requiring high resolution hard copy, the software supports device independent graphics protocol. Programs using the system can be written in UCSD Pascal and FORTRAN.

**Circle 406 on Inquiry Card**

## Automated electrical control design system software produces accurate drawings

To aid designers in producing accurate, detailed ladder and zone electrical drawings, Electrical Control Design System (ECDS) software, provided by Autotrol Technology Corp, 12500 N Washington St, Denver, CO 80233, works with the AD/380 automated design and drafting system. Using the software, a user can automatically set and monitor the numbering of wires and jumpers, annotate the drawing with cross-referencing data, and generate wire lists as a post-process function to verify proper connections. The system also automates accounting for elements of split devices using an auto-interactive or post-processing mode. These functions are accomplished through implementation of exclusive associate function capabilities within the system that enable the user to develop a fully associative data base.

Static and dynamic refresh capabilities allow graphic entities to be visualized in context with their surroundings prior to making them a permanent part of the drawing. A designer can select, rotate, and reposition an electrical symbol until the proper placement is found.

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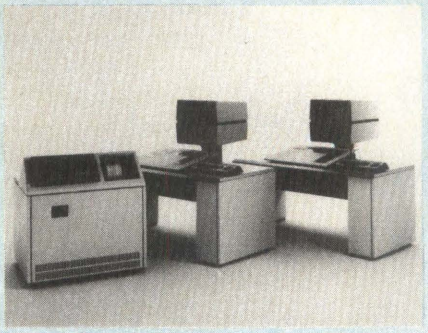
# CAD/CAM

## Multi-application turnkey CAD/CAM system supplies performance and function



The Designer™ M offers high level performance of large scale systems at moderate price levels. The medium scale system is available from Computervision Corp, 201 Burlington Rd, Bedford, MA 01730, in packaged versions for automated design and manufacture in the areas of printed circuit design, cartography, and integrated circuit design.

All applications packages except the integrated circuit design package are subsets of the company's CADDS3 software and are supported by one common data base. The system consists of CGP-80 processor with fixed media disc and magnetic tape drive, two Instaview M raster scan interactive workstations, graphics operating system, system console, and one application software package. A maximum of three tasks, two interactive and one batch, is supported simultaneously.

**Circle 408 on Inquiry Card**

## CAD system offers 3 to 20 times more operator productivity

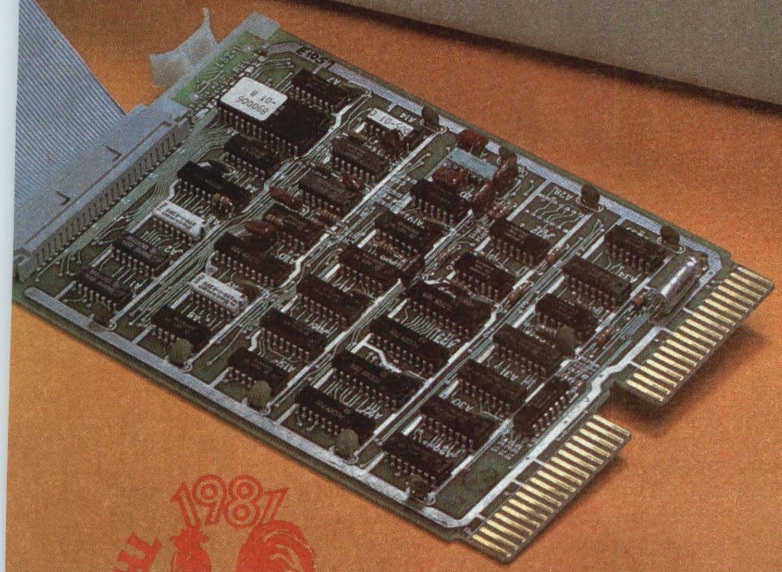
EasyDraf$^2$, a low cost standalone computer aided drafting system, increases productivity in trained operators from 3 to 20 times. The system, according to AM International, Bruning Div, 1900 Avenue of the Stars, Los Angeles, CA 90067, is priced to provide an entry level system for small- or medium-sized firms.

The processing unit is a HP 9845T desktop computer that contains 318k

*(continued on page 122)*

# WHICH IS IT?

## A NEW 8" DISK SYSTEM FROM DEC, OR A WINC™ CONTROLLER FROM AED?



Truth is, the dual 8" Winchester disk drive you see neatly packaged in a 5¼" high DEC look-alike cabinet is available only from AED. But used with our WINC 08 controller, it's fully compatible with either your LSI-11 or PDP-11. The Q-Bus®/UNIBUS® compatible WINC 08 controller is completely software transparent to DEC's RL02 system, and provides up to 41.6 megabytes of data storage. That's four times as much storage capacity as DEC's RL02 gives you—in just half the space. Plus you get all the speed and reliability of Winchester technology. And the price/performance ratio is unbeatable!

As an alternative, LSI-11 users may wish to specify AED's WINC 08/F controller. This comprises one 8" Winchester disk drive together with one 8" floppy disk drive mounted side by side in the same DEC-styled cabinet, to provide a total capacity of 21 MBs. The Q-Bus interface cards, provided with the WINC controller, plug into your computer, while the controller mounts directly into the Winchester chassis.

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bytes of memory, interactive keyboard, and monochromatic CRT display. A tape cartridge drive provides automatic program setup when the unit is turned on, and a built-in thermal printer prepares check prints. Two online flexible disc drives supply mass storage capabilities. Higher capacity Winchester drives are optional.

The companion graphics tablet serves for entering drawing information. A movable cursor on the CRT screen is manipulated by sliding a corresponding handheld puck across the graphics tablet. Four buttons on the puck allow command entry. Interactive questions and answers between computer and drafters provide a means of entering drawing information into the system.

A plotter prepares high quality, multicolor engineering and architectural drawings on standard materials. Plotting at 60-cm/s max velocity with 4-G acceleration, the plotter uses as many as eight different colored pens, and interchanges them according to programmed instructions, without operator intervention.

**Circle 409 on Inquiry Card**

## Standalone CAD system useful as starter system or graphics preprocessor

Interactive Grafics Digitizer (IGD), a low cost, standalone turnkey CAD system, announced by GTCO Corp, 1055 First St, Rockville, MD 20850, is suited to small- and medium-size graphics database applications. Used as a starter system or graphics preprocessor, the system is limited in speed, storage, and display resolution but offers the accuracy of larger systems.

Menu driven software allows graphics data entry, editing, storage, analysis, zooming, windowing, and overlaying of images. As a graphics input preprocessing system, it can be used in circuit analysis, mechanical design, and numerical control data verification applications.

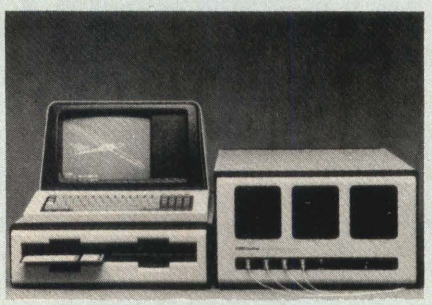
The basic system consists of a standard 8080 based Micro Digi-Pad 11 x 17″ (28 x 43-cm) tablet with 0.001″ (0.025-mm) resolution and 16-button cursor; two Z80 microprocessors; a multifunction tabletop console that includes 96k user addressable bytes of RAM; two minifloppies totaling 320k bytes of storage; 9″ (23-cm) CRT with 512 x 256 resolution and 24 lines of 80 char/line text; full 128-char ASCII keyboard with cursor control keys and 12-key pad for numeric data entry or function control; 4 RS-232-C ports (110 to 9600 baud); 4 parallel I/O ports; and video port for optional printer or monitor. Options include digitizer tablets up to 42 x 60″ (107 x 152-cm) GPIB and DMA interfaces; additional RAM, Winchester disc; remote CRT monitor; plotter; modem; standard or video printer; and high resolution CRT.

P/ROM firmware provides interacting digitizing functions, including metric and other conversions; calculator; length, area, and volume accumulation and multiplier; normalizing, scaling, rotation, axis offset, chart shifting, event counter; and digitizing modes including point, line, vector distances, delta X-Y distance, and gridding.

The system's FORTRAN based GRAFIC software can create vector images from keyboard commands. The operator can perform realtime editing of images to window an area, zoom in, selectively erase elements, position text, overlay images, output images to a plotter, or output alphanumeric data to a printer. Message prompts and a help menu make the system easy to use.

**Circle 410 on Inquiry Card**

## Microcomputer based analyzer offers high speed animation



A desktop analyzer designed to meet demands of sophisticated requirements, the MicroModal™ was developed by GenRad, Vibration Analysis Div, 2855 Bowers Ave, Santa Clara, CA 95051, as a moderately priced microcomputer based analyzer for use in computer aided design and engineering. The system provides high speed animation on a 12″ (30-cm) screen and stores 1M bytes of data on flexible media. Software is written in question and answer format for easy use.

The technique reduces development times and is helpful in locating and correcting structural problems, such as dynamic weaknesses or lightly damped modes, which are major causes of vibration, noise, and fatigue in mechanical equipment. The portable unit offers two channels for accurate frequency response measurements of baseband data to 25 kHz. Optional 4-channel capability allows faster data collection on single-axis surveys or while measuring responses along three axes. Data are sampled and collected simultaneously on all channels.

Selectable resolution allows discrimination between two closely spaced signals. Standard resolution is selectable up to 800 lines/frequency band. Optional resolutions range as high as 3200 lines.

Operator controls display size, animation rate, perspective, and viewing angle on the screen. Realtime rotation, expansion, and translation of structural mode shapes allow more complete understanding of complex structures.

The system is available with software for rotating machinery vibration analysis, structural simulation using software developed by Structural Dynamics Research Corp, or with special programs using the optional GenRad Time Series Language[R].

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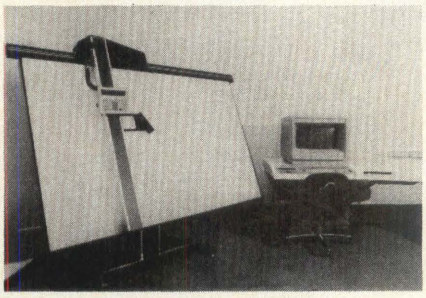
## PC artwork production eased with CAD system features



PC 800 model 2 offers display and digitizing capabilities for efficient production of PC artwork. Following the PC 800, The Gerber Scientific Instrument Co, Inc, PO Box 305, Hartford, CT 06101, has incorporated a number of design changes which further increases PC design productivity.

The system is configured around the model 8100 console, which features a large screen video display that measures 8.75 x 17.5″ (22.23 x 44.5 cm)—doubling the viewing area previously available with equivalent resolution. The digitizer is designed with controls that have been human engineered for smoother operation. Also available for online operation are high resolution photoplotters with a wide range of specifications.

**Circle 412 on Inquiry Card**

# A Brilliant New Graphics Terminal from Genisco

Raster brilliance, contrast and erasability. Z-8001 intelligence plus programmability. All in a desk top, high resolution (1024 x 792), monochrome, graphics terminal ticketed at a low $10,000*

Genisco's G-1000 is the low cost graphics terminal you've been holding your purchase order for. It is the first direct raster replacement for the Tektronix 4014-1** terminal—plug to plug and software compatible. But, at the same time, the on-board Z-8001 microprocessor plus 16K words each of RAM and PROM let you develop your own programs at your pace while your system is up and running on existing software (like PLOT-10).

Because the G-1000 is a bit map raster scan device it can do things a storage tube can't approach—like provide easy viewing in normal room light, and allow erasure of any portion of the screen without altering or redrawing the rest of the display. Genisco has equipped the G-1000 with all the quality features—60Hz noninterlaced refresh for flicker free viewing, a large 19 inch display, a detachable keyboard with cursor joystick. And, an optional alphanumeric overlay eliminates the need to use a second terminal. The unit supports a selection of I/O equipment including graph tablet and hard copy devices. With all that and the Z-8001 intelligence, the list of future capabilities is virtually open-ended.

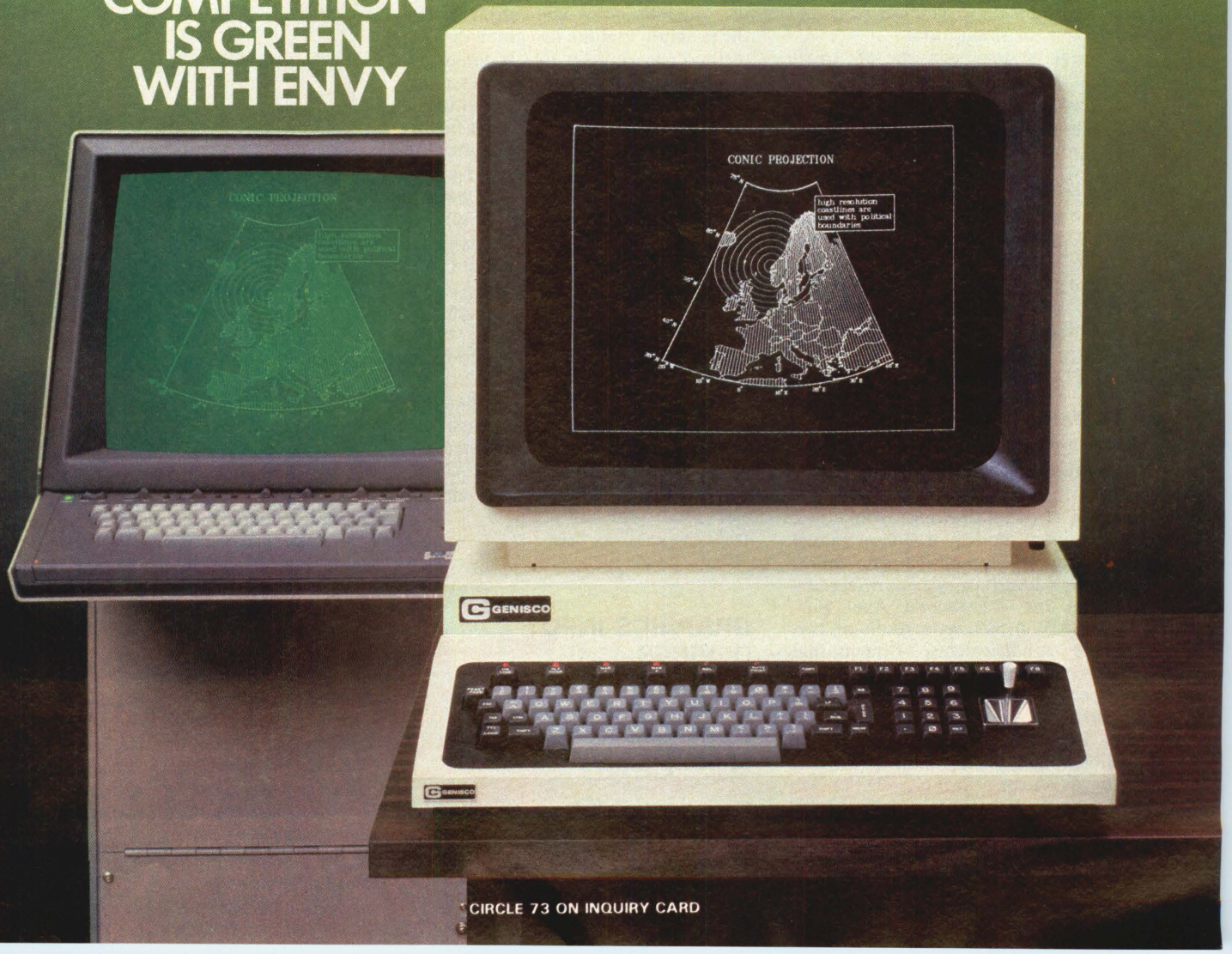
Take a look at Genisco's new G-1000—the 4014-1 replacement and a whole lot more.

Call or write for more information to Genisco Computers Corporation, 3545 Cadillac Avenue, Costa Mesa, California 92626. (714) 556-4916.

*Price varies according to quantity.
**Trademark of Tektronix
Graphics software from ISSCO Graphics.

**Genisco**

## THE COMPETITION IS GREEN WITH ENVY




CIRCLE 73 ON INQUIRY CARD

## CAD/CAM

### Microprocessor based system reduces turnaround time for NC operations

Significant productivity increases in numerically controlled engraving of individual type and composed graphic designs, and in milling of molds and dies, are offered by the 8200 CAD/CAM system. The microprocessor based system, developed by Microtex, 80 Trowbridge St, Cambridge, MA 02138, is priced 50% lower than conventional equipment built around minicomputers.

Combining traditional job functions with a full-color computer graphics workstation, the turnkey system bypasses repetitive manual design tasks such as drafting, paste-up, typesetting, layout, and part replication. Designs made using the system are immediately translated into NC machine code for direct transmission to a milling machine, laser cutter, or similar tool.

A basic system consists of 16-bit microprocessor with up to 256k bytes of high speed memory, 40M bytes of online disc storage, and a high performance, high resolution color graphics station. Operating system and applications software are provided. Interactive system software allows users to tailor size, scale, and configuration of design elements. Minor redesigns, replications, or scaling of existing designs can be accomplished rapidly.

**Circle 413 on Inquiry Card**

### CAD system capabilities increased by software enhancements

Creation of detail drawings from either 3-dimensional models or 2-dimensional representations is simplified and requires less time on CAD/CAM systems offered by Applicon Inc, 32 Second Ave, Burlington, MA 01803, as a result of two software enhancements. Dimensional enhancements include dual dimensioning—performed by pushing a button—automatic conversion of dimensions from English standards to metric or fractional, and display of either or both standards on the drawing.

Steps in the transfer process have been automated through a concept comparable to a "snapshot." This feature duplicates any view generated with the system and files it for future use. Associated text is automatically positioned so that it does not interfere with the geometry of the detail drawing. Other features include 1-step automatic updating of baseline dimensioning, bilateral tolerancing, and automatic generation of featured control blocks, architectural arrowheads, and an ISO/DIN standard diameter symbol. The system can perform chainline as well as baseline dimensioning.

**Circle 414 on Inquiry Card**

### 3250 emulating graphics display system supports 32 terminals

A graphics display system that emulates IBM 3250 class equipment, the VG 8250, developed by Vector General, 21300 Oxnard St, Woodland Hills, CA 91367, supports CADAM (Computer Graphics Augmented Design and Manufacturing), a CAD and CAM programming system developed by Lockheed Corp. Resident in a System/370 or compatible system, the program uses the IBM graphics access method (GAM) driver that is designed to support IBM 2250 and 3250 class systems.

The system enables display stations to be deployed throughout a user's facility; as many as 12 remote display sites may be located up to 3 mi (5 km) from the host computer. Channel speed of up to 1.2M bytes/s and operation of selector, block multiplexer, or byte multiplexer in real mode produce a system that can effectively support 32 terminals. 3M-bit/s communication line allows eight terminals at a site to be supported without degradation in display station response at those sites.

Other features include a handheld tablet/digitizer, maintenance/data management supervisor, twice as much refresh memory, continuous rotation and scaling of characters, and an electrostatic plotter option.

**Circle 415 on Inquiry Card**

## GRAPHICS INPUT DEVICES

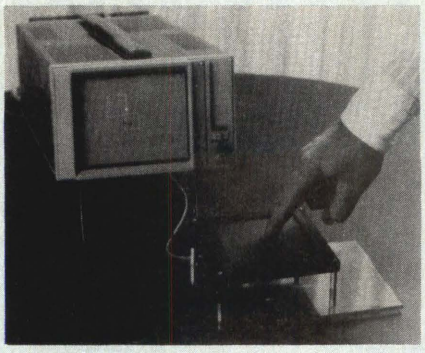
### Table digitizer has readout speed of 200 points/s

Converting engineering drawings and other graphics into digital data, high accuracy HICOMSCAN accommodates input formats from 11 x 11″ (28 x 28 cm) up to 48 x 36″ (122 x 91 cm) in size. The unit, developed by Hitachi America Ltd, 449 Alaska Ave, Torrance, CA 90503, uses an electronic stylus pen and/or cursor to accurately scan drawings for instant conversion into digital data.

Digitized data are output directly to a host computer or can be held within system memory, with visual display, for later transmission. Inherent stability is provided by an electromagnetic induction technique that makes the unit insensitive to external disturbances such as temperature, humidity, vibration, and electrical interference. Resolution is 0.001″ (0.025 mm), accuracy is ±0.005″ (0.127 mm), and readout speed is 200 points/s. Interfaces include parallel, RS-232-C, and GPIB.

**Circle 416 on Inquiry Card**

### Touch-sensitive X-Y controller replaces trackball



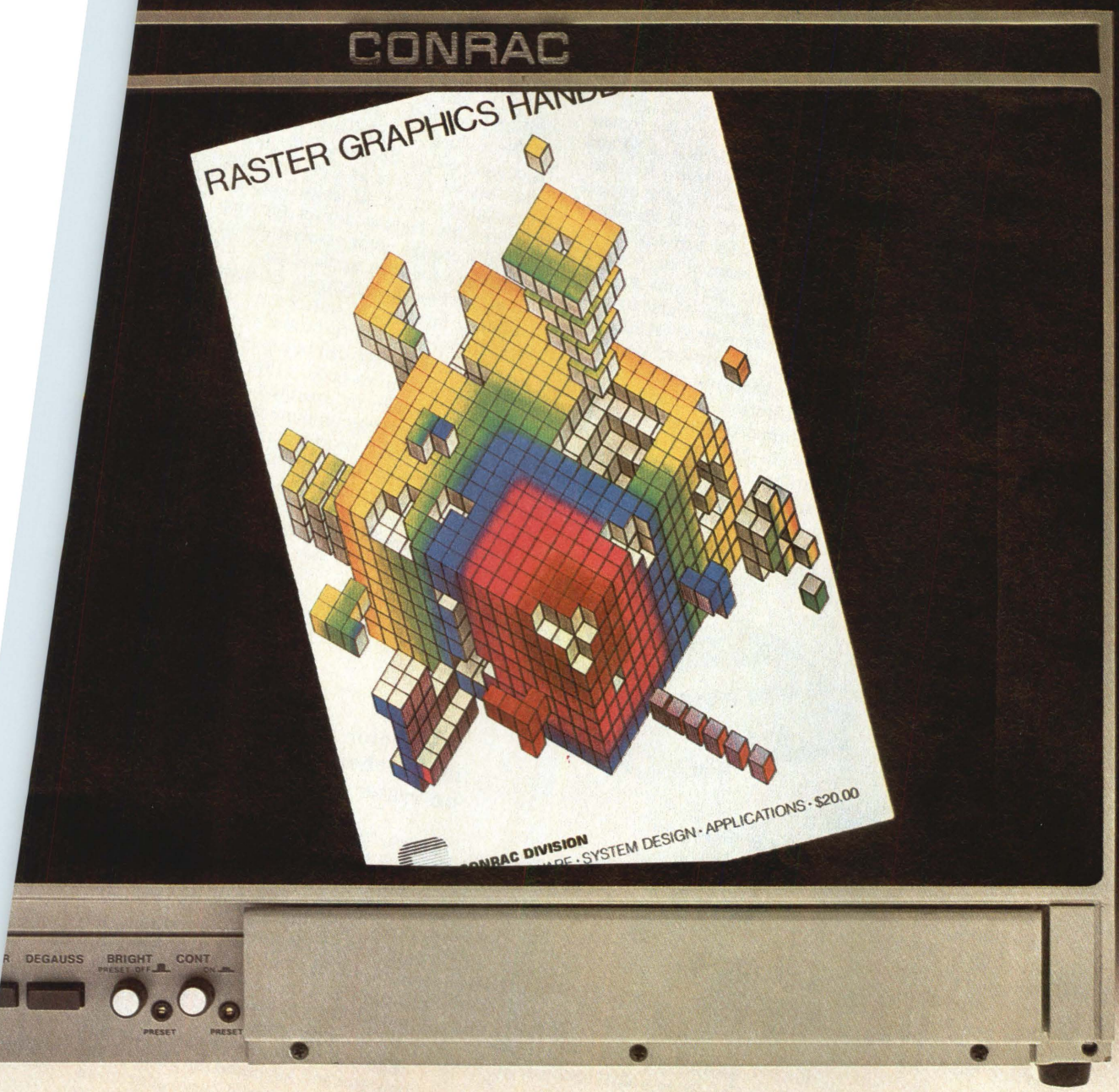
TouchGraphic operates using microproximity, high speed solid state sensing technology on both X and Y axes. Developed by TASA, Inc, 2346 Walsh Ave, Santa Clara, CA 95051, the unit can be used to replace trackball assemblies, as well as joysticks, lightpens, and field plotters.

A standard 2-dimensional positioning and tracking unit is 4 x 4″ (10 x 10 cm) in size; larger sizes can be provided. The entire positioner is only 0.5″ (1.27-cm) thick. Completely environmentally encapsulated, the units are rugged and chemically resistant.

To operate, the user simply moves a finger across the surface. Sensors embedded under the surface detect the presence, motion, and direction of the operator's hand. For slewing quickly to distant positions, the tablet can be wiped as fast as 60″ (152 cm)/s or can be moved one step at a time, even in high resolution systems.

**Circle 417 on Inquiry Card**

# See the picture that inspired the book.




There are three must-see pictures this year. All from Conrac.

They are everything you would expect from the authors of the informative text on raster graphics. And then some.

See the 7100 series for high performance color, accelerated display speed and exceptional contrast that come with Conrac's precision in-line gun CRT, wide-band video amplifier and selectable horizontal scan frequencies.

See the 7200 series for all that—plus the extra resolution and sharpness that comes with the 7200's high density shadow-mask CRT.

And for the ultimate in high-resolution black and white, see the picture you get with the 2400 series from Conrac.

You may love the book—but wait till you see the picture.

**Conrac Division**
Conrac Corporation
600 North Rimsdale Avenue
Covina, California 91722
Telephone (213) 966-3511 Telex: 67-0437

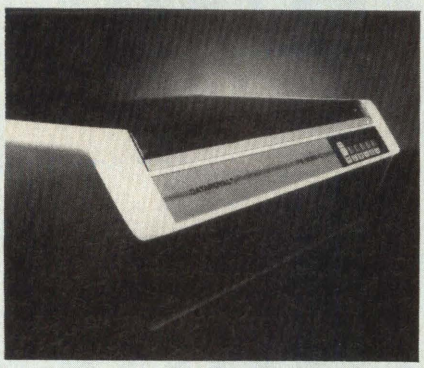
**Conrac Elektron, GmbH**
Postfach 60, Industriestrasse 18
D 6992 Weikersheim
Federal Republic of Germany
Telefon 0 79 34/70 71 Telex: 07 4231 elecon

**See Us at Siggraph, Booth 741**

**CIRCLE 74 ON INQUIRY CARD**

## GRAPHICS PRINTERS

### 165-char/s printer handles complex printing and communications protocols



The 165-char/s IPS-5000-C provides increased programmable memory, graphics, international character sets, print-style selection, and other features to handle complex printing applications. An open-ended DMA architecture, provided in the unit by Dataroyal Inc, 235 Main Dunstable Rd, Nashua, NH 03060, offers the potential for unlimited memory expansion for use either to add printing features or to handle complex communications protocol.

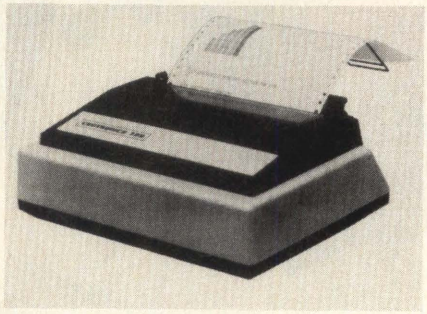
Standard memory consists of up to 12k EPROM and 4k RAM. Print speeds are 165-chars/s at 10 chars/in (3.9/cm), and 285 chars/s at 17.2 chars/in (6.7/cm). A 500-char FIFO buffer is provided and selectable 6- or 8-line/in (2.4 or 3.1/cm) spacing is offered. Available in 80- and 136-col versions, the unit bidirectionally prints a 96-char USASCII set in a 9 x 9 dot matrix, with true descending characters and underlining, using a ribbon cartridge. MTBF is 1500 operating hours at 100% duty cycles. The standard graphics package uses full-pin dots with full-dot definition.

**Circle 418 on Inquiry Card**

### Printer produces pin addressable graphics with 74 x 72 dot/in resolution

Producing correspondence printing for text and data processing, plus graphics, the model 739 is designed to meet needs of small businesses. Standard features provided in the unit by Centronics Data Computer Corp, Hudson, NH 03051, include pin addressable graphics with resolution of 74 dots/in (29/cm) horizontal by 72 dots/in (28/cm) vertical, monospaced print speed of 100 chars/s, and an acoustical top cover that improves single-sheet paper loading and minimizes average printer noise level.

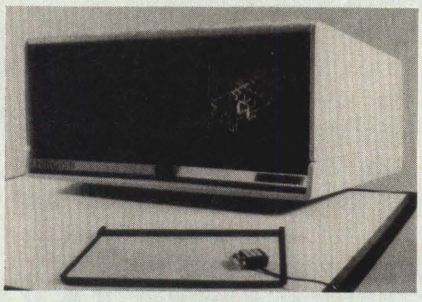
The printer produces 7 x 8 dot matrix characters with true underline at 10 and 16.5 chars/in (3.9 and 6.5/cm) for standard data processing tasks and generates N x 9 dot matrix proportional characters with true descenders for text editing applications. Under manual or software control, the printer performs half-line steps, both forward and reverse to create super- and subscripts. Additional features include a software controlled top of form and self-test capacity. Right margin justification, expanded print, and proportional character spacing are also provided. It is available in Centronics parallel and serial models, with serial versions including a standard 2k buffer suitable for screen dump applications.



**Circle 419 on Inquiry Card**

## GRAPHICS SYSTEMS

### Color graphics system offers high resolution on dual screens



A high resolution, flicker-free color graphics system, offered by Intergraph Corp, 1 Madison Industrial Pk, Huntsville, AL 35807, includes a 16-bit microcomputer and features dual 19″ (48-cm) raster screens, one color and one monochrome, which have 1280 x 1024-pixel resolution. Each screen can display full 2- and 3-dimensional graphics, plus operator prompts and messages, with independent hardware pan, zoom, and drag for both screens.

Users can select 8 active colors for simultaneous display from a palette of 4096 colors. Color associations for elements being displayed are stored in the display system and are dynamically translated to actual colors at display time. This feature allows the user to rapidly change color associations as appropriate for each application.

A keyboard and choice of digitizing tablets, menus, and cursors are offered to complete a workstation configuration. Workstations can be directly linked at distances up to 6000′ (1829 m) from the central site or operated at remote locations over telecommunications lines. A total system provides the ability to create, manipulate, display, and plot any form of graphics information and to simultaneously manage attribute data associated with the graphics.

**Circle 420 on Inquiry Card**

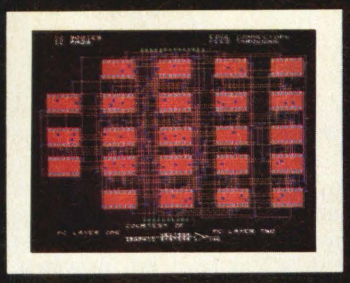
### Multicolor graphics system mixes character sizes on raster screen

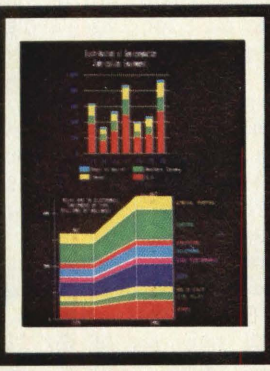
TERRELATOR™ improves legibility of displays by using a patented character generator that enables large and small characters and symbols to be mixed arbitrarily. Together with low profile keyboard and optional track ball for cursor control, the system, developed by ASEA, Electronics Div, S-721 83 Västeräs, Sweden, helps to ease the work of control room operators.

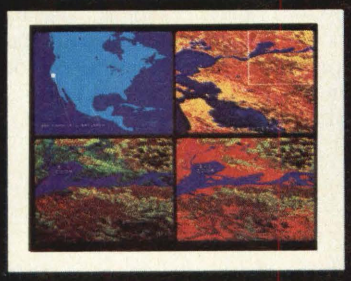
The unit display generator consists of computer and keyboard interfaces, character generator, trend curve generation, and VDU display channels. There are two interface ports: one for the primary computer and one for the backup computer. The computers are connected via high speed serial interfaces that enable the display generators to be connected in point to point or multipoint configurations. Data transfer between computer and display generator occurs at up to 250k bits/s, allowing display updates to be transmitted in less than 0.1 s.

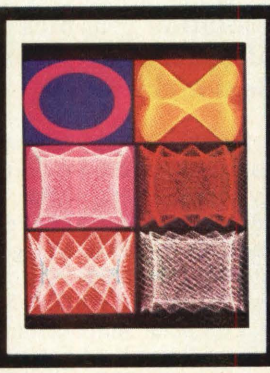
Trend curve generation provides an effective means of displaying up to 16

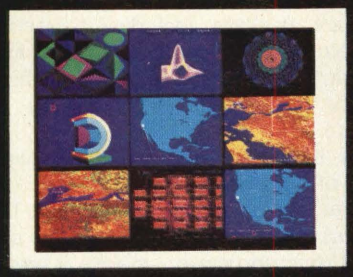
*(continued on page 128)*











Microfiche

Overhead Projection Transparency

Slide

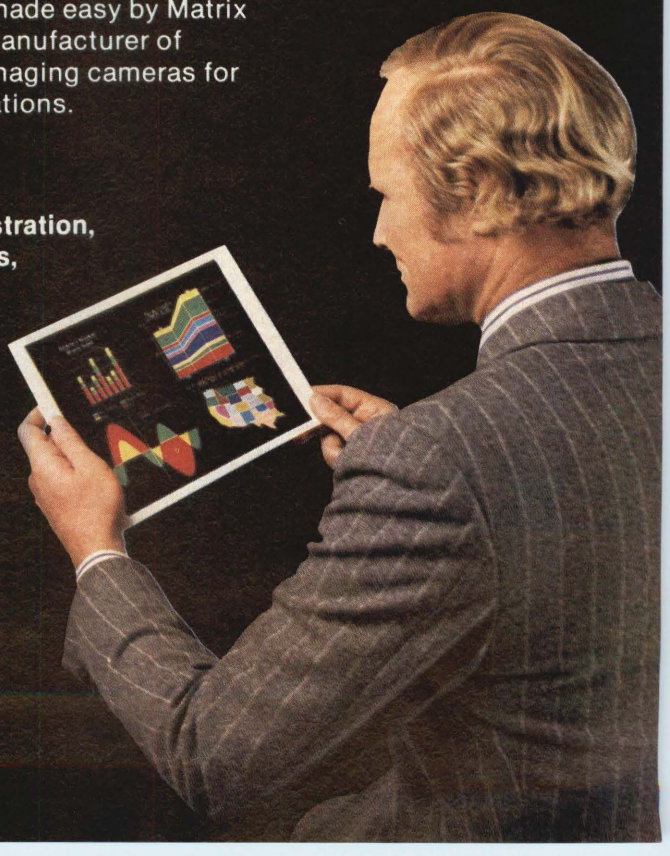
# Color Graphics Hard Copy... Made Easy

The Matrix Color Graphic Camera System converts the output of any raster scan computer color terminal into brilliant, high resolution photographic hard copy. Both line and continuous tone images can be made with accurate, bright, saturated colors.

Our system does what no other instrument can do — it produces instant, on-the-spot results with Polaroid® 8 x 10 film, 8 x 10 color transparencies for backlit displays and overhead projection, 35mm color slides, 60 image color microfiche, and 16mm/35mm color animation films. All with one camera system. It also allows recording of multiple image formats. Related and sequential images can be recorded in orderly arrays, on a single sheet of 8 x 10 instant print film. The resultant ease of comparison and analysis is unmatched. The system is also fully modular and field upgradable. . . you purchase only the capability that you need now.

Microprocessor based electronics provide many automation, self-calibration, self-diagnosis and remote control functions. Color graphics hard copy made easy by Matrix Instruments, the leading manufacturer of precision electro-optical imaging cameras for diagnostic medical applications.

**For more information, film samples, or a demonstration, contact Matrix Instruments, 230 Pegasus Avenue, Northvale, New Jersey 07647. Telephone (201) 767-1750 Or call toll-free: (800) 526-0274.**



**# MATRIX INSTRUMENTS**

**CIRCLE 75 ON INQUIRY CARD**

Hard copy shown reduced from original 8" x 10", slide, and microfiche films.
Multiple images recorded on a single sheet of film.
"Polaroid" is a registered trademark of the Polaroid Corporation.

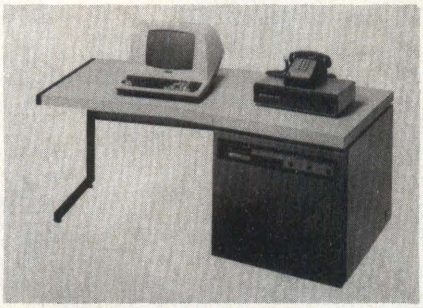
channels of trend data. Any curve or any part of the curve can be presented in any of 8 or 16 colors, depending on use of the color/blink attribute bits. Curves can also be filled with color down to the baseline.

The display generator can be equipped with up to three independent display channels. Data transfer into or out of the display generator or other functions internal to the display generator do not interrupt refresh of the display. A built-in zoom function permits an arbitrary quarter of the display to be enlarged to occupy the entire screen.

The video monitor is a 20″ (51-cm) RGB high resolution shadow mask CRT that provides about four times as many dots as a standard resolution CRT. Displays are designed directly from the keyboard with the system checking the logic connection points of symbols. Each symbol, regardless of size, needs only one character code, reducing the amount of data to be transmitted. Up to three parallel VDUs and four keyboards can be connected to the system, and up to four online computers can be used.

**Circle 421 on Inquiry Card**

### Plotting workstation offers remote graphics manipulation



Supporting remote job entry, electrostatic plotting/printing, and graphics manipulation, the 444 remote plotting workstation accepts unsorted vectors as well as sorted vector, compressed raster, raster, and print data formats. Emulating HASP multileave remote workstations, the system, developed by Versatec, 2805 Bowers Ave, Santa Clara, CA 95051, provides IBM software and system protocol compatibility without requiring modification of the operating system.

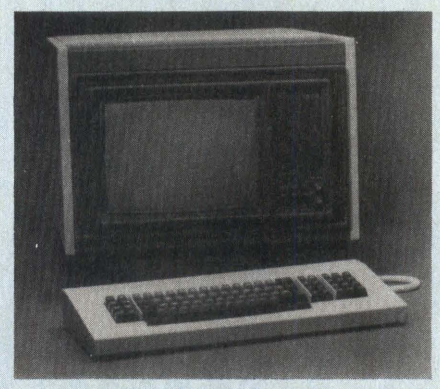
Workstation components include microprocessor with 64k bytes of memory, CRT display, 24M-byte disc, and bipolar algorithmic processor designed specifically to perform vector sorting and raster generation. The system will support any two of the company's printer/plotters in any mix of paper widths.

A console with CRT display and keyboard provides host command input and response, sign-on inquiry, cancel, and queue control. Menus enable users to define plot parameters, create canned sequences, and perform graphics manipulation. Data received in Versatec Random Format (VRF) can be scaled, translated, windowed, mirrored, and rotated in 1-degree increments. Multiple copies can be produced without re-sorting data. The system can generate up to 15 font styles and assign pen numbers to create different line styles and widths. Data are received over dial-up or leased lines at speeds of 2400 to 9600 bits/s.

**Circle 422 on Inquiry Card**

## GRAPHICS TERMINALS

### Color CRT terminal displays graphics data using 9 x 12 matrix



MVI-7 from Colorgraphic Communications Corp, Suite 105, 2379 John Glenn Dr, Atlanta, GA 30341, has a 13″ (33-cm) preconverged high resolution color CRT. Colors include red, green, blue, white, yellow, turquoise, and pink. The display has 1920 alphanumeric characters in a 24-line by 80-col format with 720 by 288 graphic resolution. Graphics data can be displayed by using any portion or all of the 9- x 12-char matrix. In addition to the full ASCII character set, each unit has 1280 user-defined programmable symbols on a single plane.

The detached keyboard provides 87 keys. There are 8 for editing and special functions plus 24 programmable function keys. Standard video attributes include blink, highlight, foreground and background color, and underscore. Users can view two pages of data by horizontal or vertical scrolling with a scroll buffer of 80 chars x 48 lines, 160 x 24, or 140 x 32.

Standard emulation package includes DEC VT 100 and VT 52, IBM 3101, Hazeltine 1500, Lear Siegler ADM3, and ADDS. Selectable baud rates are in the 110- to 19,200-baud range. Standard communications interfaces included with each unit are RS-232-C, RS-422, and current loop plus an auxiliary serial output port.

**Circle 423 on Inquiry Card**

### High resolution graphics terminal features self-reliant architecture

Basic interface of the IM-1 intelligent terminal uses a full RS-232-C I/O port. The universally compatible terminal, from Form & Substance, Inc, 875 Westlake Blvd, Suite 213, Westlake Village, CA 91361, interfaces to mini- and microcomputers including Alpha Micro, DEC LSI-11, Computer Automation NM/4, and S-100 computers. A complementary software package includes interactive X-Y plotting, 3-D contour plotting, and pie charts. In addition to producing high quality images, the unit is easy to operate.

The high resolution terminal is capable of drawing crisp character or graphic images at high speed on a 15″ (38-cm) green phosphor screen. Its onboard microprocessor makes it completely independent, supporting its own RAM and P/ROM, interrupt structure, lightpen interface, and resident software.

Graphics primitive software, resident in P/ROM, offers standard terminal emulation and a basic package that includes draw and erase, complement and read, and point and plot character, as well as draw, erase, and complement line. Optional primitive software allows separate user definable regions for graphics and ASCII data such as draw circle and curve, and selection of terminal region and graphics region size.

*(continued on page 130)*

# Computer Graphics Hardcopy for Every Application... Worldwide

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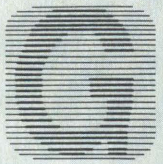
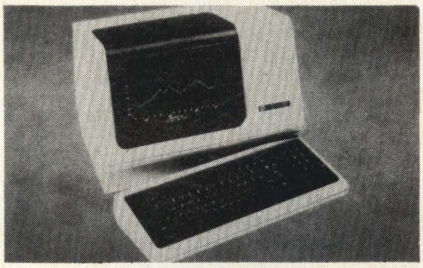
CIRCLE 76 ON INQUIRY CARD



Resolution is 512 x 484; text is displayed on 39 lines of 85 characters. Lightpen interface, 20-MHz monitor, keyboard with IBM Selectric layout, and RS-232 serial interface to the host computer are standard.

**Circle 424 on Inquiry Card**

## Color graphics terminal serves as VT 100 replacement



ID-100, a low cost serial communicating, ASCII terminal, is able to portray 8-color, character and symbol graphic images. The video color character graphics terminal, offered by ID Systems Corp, PO Box 393, Dublin, OH 43017, can function as a high performance 80- or 132-character/line replacement for the DEC VT-100.

The high resolution (0.31-mm pitch) color monitor has a housing and keyboard that are the same as those of the VT-100. Communications are supported at up to 19.2k baud with optional instant picture or forms retrieval from internal memories. The unit is plug to plug and fully software compatible with the VT-100.

**Circle 425 on Inquiry Card**

## Graphics terminal adds color with VT-100 compatibility

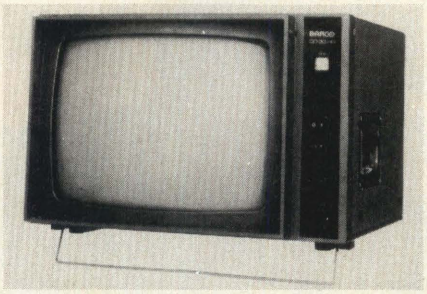
A 80/132-col, 8-color display terminal, ColorScan 10 is VT-100 compatible with added high resolution color. Announced by Datamedia Corp, 7401 Central Hwy, Pennsauken, NJ 08109, the unit offers a high quality crisp display in 132-col format at an affordable price. It has a built-in line ruling set, and 8 colors for both foreground and background information.

The eight displayable colors include red, blue, green, cyan, magenta, yellow, black, and white. These colors are displayed on a nonglare 12″ (30-cm) screen in either an 80- or 132-col x 24-line format. The unit's detachable typewriter style keyboard has a separate numeric pad for operator convenience. Additional features include split screen, regional scrolling, smooth scrolling, and double-high/wide characters.

**Circle 426 on Inquiry Card**

# GRAPHICS MONITORS

## Color display monitors offer high resolution shadow mask tube



CD-33B HIR and CD-51B HIR monitors offer 13 and 19″ (33- and 48-cm) PIL tubes that lower cost and eliminate the need for operator convergence adjustments. The units introduced by Elector, 5128 Calle del Sol, Santa Clara, CA 95050, are equipped with a high resolution 0.31-mm dot screen shadow mask inline gun picture tube that permits extremely sharp definition of characters and graphics. Picture bandwidth is 7 MHz with RGB input (looped through). The monitors can be rackmounted or used with attached tiltup stand that raises easily for desktop display.

**Circle 427 on Inquiry Card**

## Standalone graphics generator uses TV monitor for display

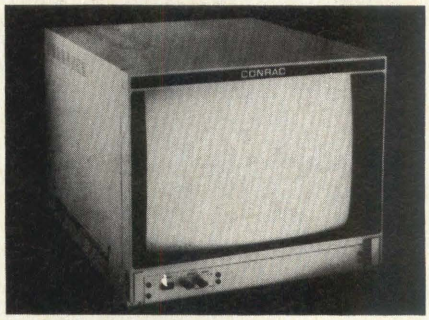
Adding graphics capability to any computer via its RS-232 port, the RG-B1 is a smart standalone graphics generator that accepts high level commands from a host computer and displays text and graphics on a standard 525-line TV monitor. Providing 512 H x 480 V resolution, the generator, designed by Raster Graphics, PO Box 23334, Tigard, OR 97223, accepts high level display opcodes from the host computer to generate circles, ASCII characters, point to point draw, and rectangular fill.

Display opcodes are downloaded from the host to the generator and stored in its 2k RAM buffer. After loading, they are processed by the generator's internal processor to create graphics shapes that are stored in its refresh memory. Contents of refresh memory are formatted into a composite TV signal and output at a connector on the rear panel for connection to a 525-line TV monitor.

Data may be uploaded to the host or downloaded from the host in either binary or Intel hex format. A software monitor allows use from a keyboard when the generator is in manual mode.

**Circle 428 on Inquiry Card**

## Modular raster scan monochrome display adapts to application




A high resolution raster scan monochrome display, the 19″ (48-cm) model 2400 is designed for applications such as computer generated images, medical diagnostics, military command/control, CAD/CAM, and document viewing. Modular design of the monitor, offered by the Conrac Div of Conrac Corp, 600 N Rimsdale Ave, Covina, CA 91722, permits selection of only those features needed for an application.

Features include wideband video amplifier, preset calibration controls, dynamic focus, optional CRT phosphors, and adjustable horizontal scan frequency. Switchable horizontal scan frequency allows the customer to set a frequency. Video characteristics include 60-Hz to 35-MHz video signal bandwidth, 15-ns rise time, and field distortion of less than 1% line.

The unit is available in cabinet, naked, or rack slide versions. Other options are dual-video input, inverted video, external sync, separate horizontal and vertical drive, differential input, and optional CRT phosphors. G

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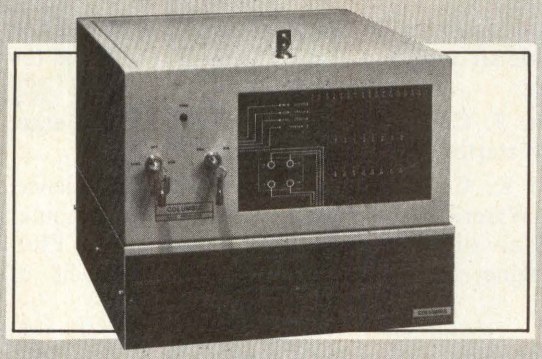
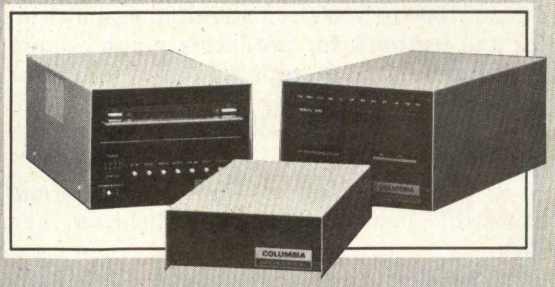


**Multi-User Multi-Tasking Multi-Processor System**
Affordable, upgradeable and expandable distributed processing is a reality with our new DC-1000 system. By simply adding satellite processor boards, our modular architecture allows for servicing up to 16 users, while creating a complete CP/M environment for each user; allowing full and fast execution of standard, unmodified CP/M programs. A master processor manages interaction of resources such as printers, floppy and Winchester disks, and data communication lines, at such speeds that a user is unaware others are sharing these peripherals.

**Standalone Computer System With Graphics**
With a Model 900 Commander Microcomputer, you don't need a separate graphics terminal . . . it's built in. You can display bar charts, histograms and complex point-to-point plots. And, because this Commander has an independent processor controlling the display, graphics can be handled without interrupting primary computing tasks. So . . . don't buy a graphics terminal . . . select a Columbia Data Products' Model 900 with the fullest I/O complement today, including RS-232, parallel, DMA and IEEE Bus controllers.

**Floppy and Winchester Disk Based Computer Systems**
Commander Series FX and MX computer systems let you connect your dumb terminal into a powerful distributed processing system. With these floppy disk based Z80A computers, you can perform a vast array of computer tasks using high-level language programs (such as BASIC, PASCAL, COBOL, and FORTRAN). Expandable versions are also available offering high performance Winchester disk storage and multi-user capability with up to 5 users sharing a 256K Z80A processor system running under CP/M and MP/M.




**Intelligent RS-232 Storage Systems**
These microprocessor-controlled data storage products offer cost effective storage with trade offs between capacity and access speed. In addition to the standard storage capabilities, these high-speed tape units, mini-floppy disks and data buffer units provide intelligent data handling, improved file management and editing as well as ease of operation . . . locally or remotely. Each data storage product is fully compatible with RS-232C/CCITT V.24 bus standards for data rates up to 19,200 baud.

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# SIGGRAPH/81

## Dallas Convention Center
## Dallas, Texas, August 3 to 7

Most of the diverse technological phases as well as applications of computer graphics—interactive systems, raster graphics, image synthesis, modeling, user/computer interface, software, and standards—will be subjects of courses and technical program sessions at the eighth annual conference on computer graphics and interactive techniques. Additionally, SIGGRAPH/81, sponsored by the Association for Computing Machinery, will include a wide range of product presentations: graphics input devices, interactive vector and raster displays, hardcopy output devices, and software support packages for turnkey applications such as computer aided design/computer aided manufacturing (CAD/CAM) and image processing.

Doug Green of Texas A&M University and Tony Lucido of Intercomp Resource Development and Engineering are cochairmen of SIGGRAPH/81. Henry Fuchs of the University of North Carolina is technical program chairman and Ingrid Carlbom of Schlumberger-Doll Research organized the series of courses. For full details on registering for SIGGRAPH/81, write to SIGGRAPH/81, Conference Office, 1 Illinois Center, 111 E Wacker Dr, Chicago, IL 60601.

## Courses

Eighteen courses—both introductory level tutorials with emphasis on fundamentals and principles, and advanced level, special topic seminars—will be conducted. The degree of technical content varies; some courses are overviews of broad subjects, others are intended only for engineers and computer scientists with technical backgrounds. The following is a partial listing and description of those courses.

### 2-day courses/August 3 and 4

#### Introduction to computer graphics

This tutorial will provide managers and technical people with a conceptual introduction to graphics hardware and software. Although it is not a course in graphics programming, mathematical and programming backgrounds will be helpful to attendees. Included in the discussion are vector and raster display systems, graphics input hardware, interaction techniques, human factors, organization and content of graphics packages, and visible surface processing, as well as current trends in computer graphics. In addition to this, the discussion will provide an overview of the technical sessions at the conference.

Chairman: J. C. Beatty, Prof of Computer Science, Univ of Waterloo, Waterloo, Ontario

Lecturers: K. C. Booth, Prof of Computer Science, Univ of Waterloo; L. Matthies, Dept of Computer Science, Univ of Waterloo; and M. Wein, Div of Electrical Engineering, National Research Council of Canada

#### Introduction to computer aided design

Intended for decision makers, managers, and potential users in a number of application fields, this seminar will deal with commercially available CAD systems. Introducing general principles and key topics, the lecturers will cover general structure and uses of CAD systems, interconnection of different CAD systems, engineering analysis that can be performed on parts defined by CAD systems, numerically controlled machining, how to buy a CAD system, solid modeling, and a discussion of what the near-term future holds for CAD users.

Chairman: B. Herzog, President, Herzog Associates, Inc, Boulder, Colo

Lecturers: S. H. Chasen, Lockheed Georgia Co, Marietta, Ga; R. Heilman, Battelle, Columbus, Ohio; and H. Voelker, Dir, Production Automation Project, Univ of Rochester, Rochester, NY

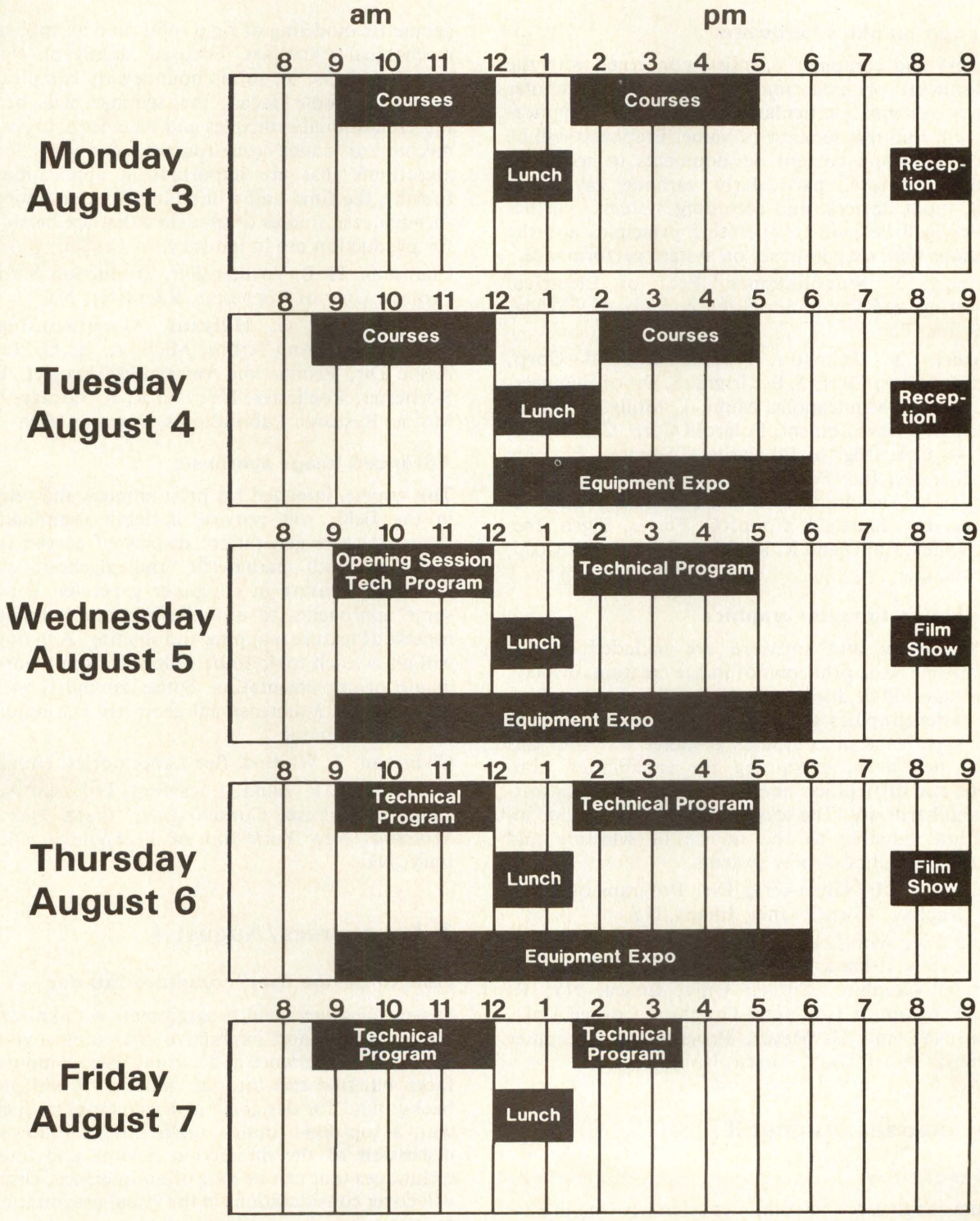
#### Low cost graphics

This course will cover the application of low cost interactive computer graphics hardware ranging in price from less than $1000 to $3000. In addition, graphics input devices and methods for producing graphics hard copy will be discussed. The seminar is appropriate for engineers, scientists, managers, and analysts in industry, government, and education with no previous graphics experience.

Chairman: R. L. Phillips, Prof of Computer, Information, and Control Engineering, Univ of Michigan, Ann Arbor, Mich

Lecturers: T. DeFanti, Prof of Information Engineering, Univ of Illinois at Chicago Circle, Chicago, Ill; H. L. Loats, Jr, Vice President of ECO Systems International, Inc, Gamgrills, Md; and P. Roper, Dir of Software Development, Eyring Research Institute, Provo, Utah

# Conference at a Glance



# SIGGRAPH/81

### Computer graphics hardware

Engineers and computer scientists concerned with the establishment or extension of interactive computer graphics systems, particularly for CAD/CAM applications, will find this seminar of value. Emphasis will be on principles and current developments in computer graphics products, particularly cathode ray tubes (CRTs), input devices, and recording systems. Further attention will be paid to operating principles and the limitations hardware imposes on system performance.

Chairman: J. Staudhammer, Prof of Electrical Engineering and Computer Science, Univ of Florida, Gainesville, Fla

Lecturers: N. Johnson, Vector General Corp, Woodland Hills, Calif; J. E. Grimaldi, Dir of Engineering, Dicomed, Minneapolis, Minn; T. Milligan, Mgr of Applications Development, Polaroid Corp, Cambridge, Mass; D. Cole, Mgr of Educational Services, Floating Point Systems, Inc, Portland, Ore; R. M. Dunn, Vice President of Development and Engineering, Summagraphics, Inc, Fairfield, Conn; G. Foster, Eigen, Inc, Grass Valley, Calif; and R. Keithley, PrintaColor Corp, Norcross, Ga

### Introduction to raster graphics

Both hardware and software are included in this tutorial. The basic principles of image creation, display, and storage will be discussed along with examples of existing raster graphics systems. Professionals with little or no experience in computer graphics will find this tutorial helpful in explaining the capabilities, constraints, and difficulties inherent in raster graphics software and hardware. The session should also provide information valuable to the novice in selecting and evaluating graphics display systems.

Chairman: D. P. Greenberg, Dir, Program of Computer Graphics, Cornell Univ, Ithaca, NY

Lecturers: V. Woolf, Program of Computer Graphics, Cornell Univ, Ithaca, NY; J. Friedberg, Program of Computer Graphics, Cornell Univ, Ithaca, NY; R. Cook, Program of Computer Graphics, Cornell Univ, Ithaca, NY; and G. Meyer, Program of Computer Graphics, Cornell Univ, Ithaca, NY

## 1-day courses/August 3

### Solid modeling

Graduate engineers and computer scientists who are active in CAD/CAM research and system development, as well as CAD/CAM users who require a better foundation in principles, will find this seminar of interest. It will summarize the current state of knowledge in the geometric modeling of rigid solids and its application to mechanical CAD/CAM. Focused mainly on "unsculptured" objects, ie, solids bounded by complex collections of simple faces, the seminar will deal with representational principles and schemes appropriate for mechanical solids (one-fourth), and functions and algorithms that are important in applications (one-fourth); the final half will address system design issues through case studies of modelers that are being readied for production use in industry.

Chairman: H. B. Voelker, Dir, Production Automation Project, Univ of Rochester, Rochester, NY

Lecturers: R. C. Hillyard, Manufacturing Data Systems, Inc, Ann Arbor, Mich; A. A. G. Requicha, Assoc Dir, Production Automation Project, Univ of Rochester, Rochester, NY; and R. F. Sarraga, General Motors Research Laboratories, Warren, Mich

### Advanced image synthesis

This course, intended for programmers and researchers in the field, will provide in-depth examinations of shaded picture generation: display of curved surfaces, including both parametric and algebraic surfaces; causes of aliasing in computer generated images and some approaches to anti-aliasing; and computational aspects of texture mapping and shading. A limited scope will allow each topic to be followed from theory to the details of implementation. Some familiarity with raster graphics and 3-dimensional geometry is a requisite for full understanding.

Chairman: T. Whitted, Bell Laboratories, Holmdel, NJ

Lecturers: J. F. Blinn, Lucasfilm, Ltd, San Anselmo, Calif; E. Feibush, Cornell Univ, Ithaca, NY; and L. Williams, New York Inst of Technology, Old Westbury, NY

## 1-day courses/August 4

### How to design user/computer interfaces

Systems designers and programmers with knowledge of basic graphics and interactive computing but without substantial experience in designing user/computer interfaces will find this tutorial valuable. It will provide a background for designers of user/computer interfaces, with a top-down design methodology followed by a discussion of the interaction devices and interaction techniques that can be part of an interface. Discussions will cover considerations in the visual presentation of information, such as coding, searching, and structure, as well as design criteria that can be used to evaluate existing or proposed user interfaces. Available software

*(continued on page 136)*

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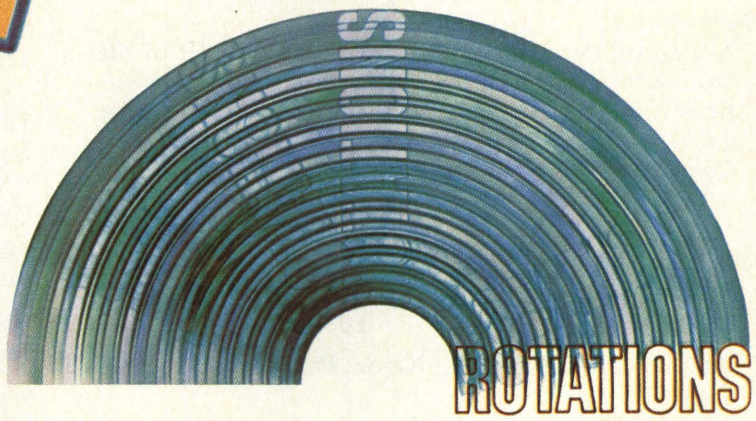
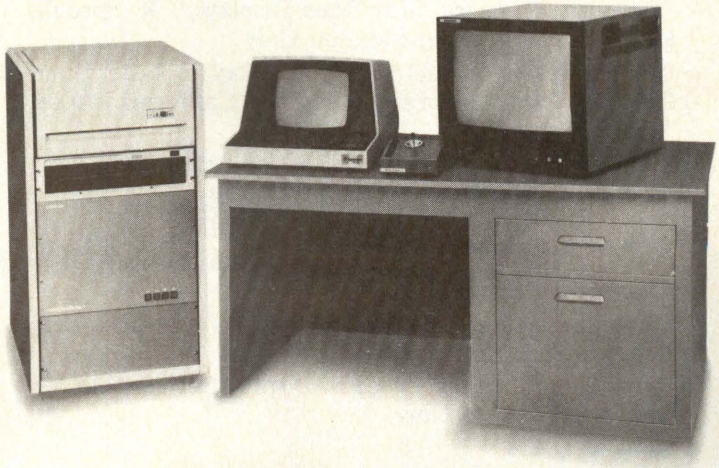


CIRCLE 78 ON INQUIRY CARD

tools for implementing user/computer interfaces will also be described.

Chairman and Lecturer: J. D. Foley, Prof of Electrical Engineering and Computer Science, George Washington Univ, Washington, DC

**State of the art in image synthesis**

This seminar will consist of several short informal talks describing recent developments in complex image synthesis. The talks will concentrate on aspects of the process that do not ordinarily appear in published papers. Exact content will be flexible until the time of the conference to allow last minute developments to be included. The seminar will appeal mostly to researchers in the field, but some of the presentations could be appreciated by a general audience.

Chairman: J. F. Blinn, Lucasfilm, Ltd, San Anselmo, Calif

Lecturers: T. Whitted, Bell Laboratories, Holmdel, NJ; D. Em, independent artist, Los Angeles, Calif; D. Lundin, New York Inst of Technology, Old Westbury, NY; and R. Schumacker, Evans and Sutherland Computer Corp, Salt Lake City, Utah

## Technical program

A total of 15 sessions will be presented as part of the SIGGRAPH/81 technical program, starting with the official conference opening on Wednesday, August 5, at 9 am. Most of the remaining sessions of interest to *Computer Design* readers are summarized below.

### Wednesday, August 5

**Theory and algorithms I** **10:45 am-12:00 noon**

Chairman: J. Warnock, Xerox Palo Alto Research Center

"Filtering Edges for Gray Scale Displays," R. Sproull and S. Gupta, Carnegie-Mellon Univ

"Filtering High Quality Text for Display on Raster Scan Devices," J. T. Kajiya and M. Ullner, California Inst of Technology

"A Visible Polygon Reconstruction Algorithm," S. Sechrest and D. Greenberg, Cornell Univ

**Theory and algorithms II** **1:30-2:30 pm**

Chairman: K. Booth, Univ of Waterloo

"Contour Filling in Raster Graphics," T. Pavlidis, Bell Laboratories

"Shading of Regions of Vector Display Devices," D. T. Lee, Northwestern Univ

"Frame to Frame Coherence and the Hidden Surface Computation: Constraints for a Convex World," H. Hubschman and S. W. Zucker, McGill Univ

**Graphics hardware** **2:45-3:45 pm**

Chairman: M. Wozny, Rensselaer Polytechnic Inst

"Parallel Processing Image Synthesis and Anti-Aliasing," R. Weinberg, Cray Research Inc

"A Frame Buffer System with Enhanced Functionality," F. C. Crow, and M. W. Howard, Ohio State Univ

"VLSI Parallel Processing for Raster Scan Displays," S. Gupta, Carnegie-Mellon Univ

**Custom VLSI chips for graphics** **4:00-5:15 pm**

Panel discussion of new VLSI oriented designs for high performance graphic processors

Panelists: J. Clark, Stanford Univ; H. Fuchs, Univ of North Carolina at Chapel Hill; and T. Whitted, Bell Laboratories

### Thursday, August 6

**Interaction techniques** **9:00-10:30 am**

Chairman: R. Baecker, Univ of Toronto and Human Computing Resources Corp

"Effective Use of Color in Computer Graphics," J. R. Truckenbrod, Northern Illinois Univ

"Tablet Based Valuators that Provide One, Two, or Three Degrees of Freedom," K. B. Evans, P. P. Tanner, and M. Wein, National Research Council

"A Methodology for the Specification of Graphical User Interfaces," M. Green, Univ of Toronto

"Gaze Orchestrated Dynamic Windows," R. A. Bolt, Massachusetts Inst of Technology

**Video panel session on interactive systems** **10:45 am-12:00 noon**

Chairman: R. Baecker, Univ of Toronto and Human Computing Resources Corp

Panelists will show videotapes illustrating user interfaces of interactive systems and comment on techniques used.

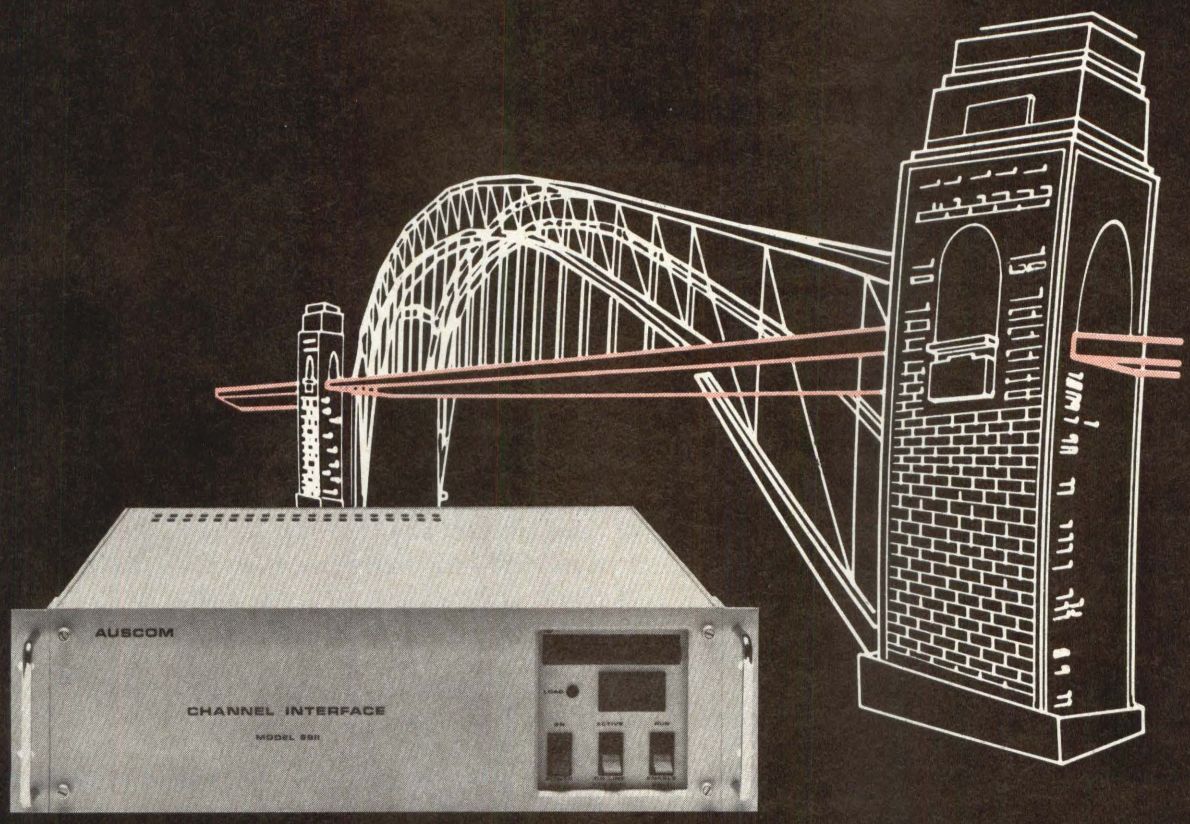
**Graphics software and languages** **1:30-2:30 pm**

Chairman: R. Puk, Megatek Corp

"The George Washington University Core System Implementation," J. D. Foley and P. A. Wenner, George Washington Univ

"GRAMPS—A Graphics Language Interpreter for Realtime Interactive 3-Dimensional Picture Editing and Animation," T. J. O'Donnell and A. J. Olson, Lawrence Berkeley Laboratory

*(continued on page 138)*

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"An Attribute Binding Model," M. T. Garrett, Applied Graphics, Inc

**CAD/CAM** **2:45-3:45 pm**

Chairman: R. Riesenfeld, University of Utah

"An Application of Color Graphics to the Display of Surface Curvature," J. C. Dill, General Motors Research Laboratory

"SAMMIE—A Computer Aid for Man/Machine Modeling," N. Schofield and E. C. Kingsley, Compeda Ltd; and K. Case, Univ of Nottingham, England

"Variational Geometry in Computer Aided Design," V. C. Lin, D. C. Gossard, and R. A. Light, Massachusetts Inst of Technology

**Presidents' forum** **4:00-5:15 pm**

Chairman: L. N. Johnson, Vector General

The presidents of key computer graphics companies will discuss contemporay business and technical issues.

Panelists: D. C. Evans, President and Chairman of the Board, Evans & Sutherland Computer Corp; W. Huelskoetter, President, Dicomed Corp; and R. Zaphiropoulos, President, Versatec Corp, Xerox, Inc


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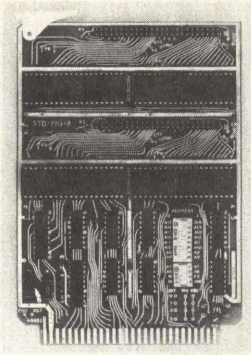

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## Friday, August 7

**Applications (concurrent session)** **8:30-10:30 am**

Chairman: C. Machover, Machover Associates

"An Integrated System for Creating and Presenting Complex Computer Based Documents," S. Feiner, Brown Univ; S. Nagy, Hungarian Academy of Science; and A. van Dam, Brown Univ

"Towards a Laboratory Instrument for Motion Analysis," R. Baecker, Univ of Toronto; W. Reeves, Lucasfilm, Ltd; and D. Miller, Micom, Ltd

"DATAPLOT—An Interactive High Level Language for Graphics, Non-Linear Fitting, Data Analysis, and Mathematics," J. J. Filliben, National Bureau of Standards

"Creating Repeating Hyperbolic Patterns," D. Dunham and J. Lingren, Univ of Minnesota; and D. Witte, Univ of Chicago

"Austere C3 Graphics," P. De Shaxo and R. Todd, the MITRE Corp

"Two Aspects of Domain Designing: $C^{\infty}$ Curve Rendering and Blended Map Projections," A. P. Rockwood and T. W. Jensen, Evans and Sutherland Computer Corp

**Panel on standards (concurrent session)** **8:30-10:30 am**

Chairman: P. Bono, Naval Underwater Systems Center

Members of ANSI Committee X3H3 will present current issues of the standardization effort and describe avenues of attack and proposed solutions. Topics include graphics functionality, programmers' minimal interface, virtual device interface, and Metafile.

Panelists: R. Puk, Megatek Corp; T. Reed, Los Alamos Laboratory; M. Skall, National Bureau of Standards; and T. Wright, ISSCO

**Raster graphics I** **1:30-2:30 pm**

Chairman: J. Beatty, Univ of Waterloo

"A Software Test Bed for the Development of 3-D Raster Graphics," T. Whitted and D. Weimer, Bell Laboratories

"A Method of Interactively Analyzing 3-D CAD Surface Models on a Color Video Display," P. R. Atherton, General Electric Co

"3-D Graphics and the Wave Theory," H. P. Moravec, Carnegie-Mellon Univ

**Raster graphics II** **2:45-3:45 pm**

Chairman: T. Whitted, Bell Laboratories

"A Lens and Aperture Camera Model for Synthetic Image Generation," M. Potmesel and I. Chakravarty, Rensselaer Polytechnic Inst

"Reflectance Models for Computer Graphics," R. L. Cook and K. Torrance, Cornell Univ

"Water Waves and Islands in the Sunset," N. Max, Lawrence Livermore Laboratory □

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So whether you're buying or building a CRT display, look for something more than just another pretty face. Look for the best in CRT's: Panasonic. Panasonic Company, Electronics Components Division/Electron Tube Marketing, One Panasonic Way, Secaucus, NJ 07094; (201) 348-5278.

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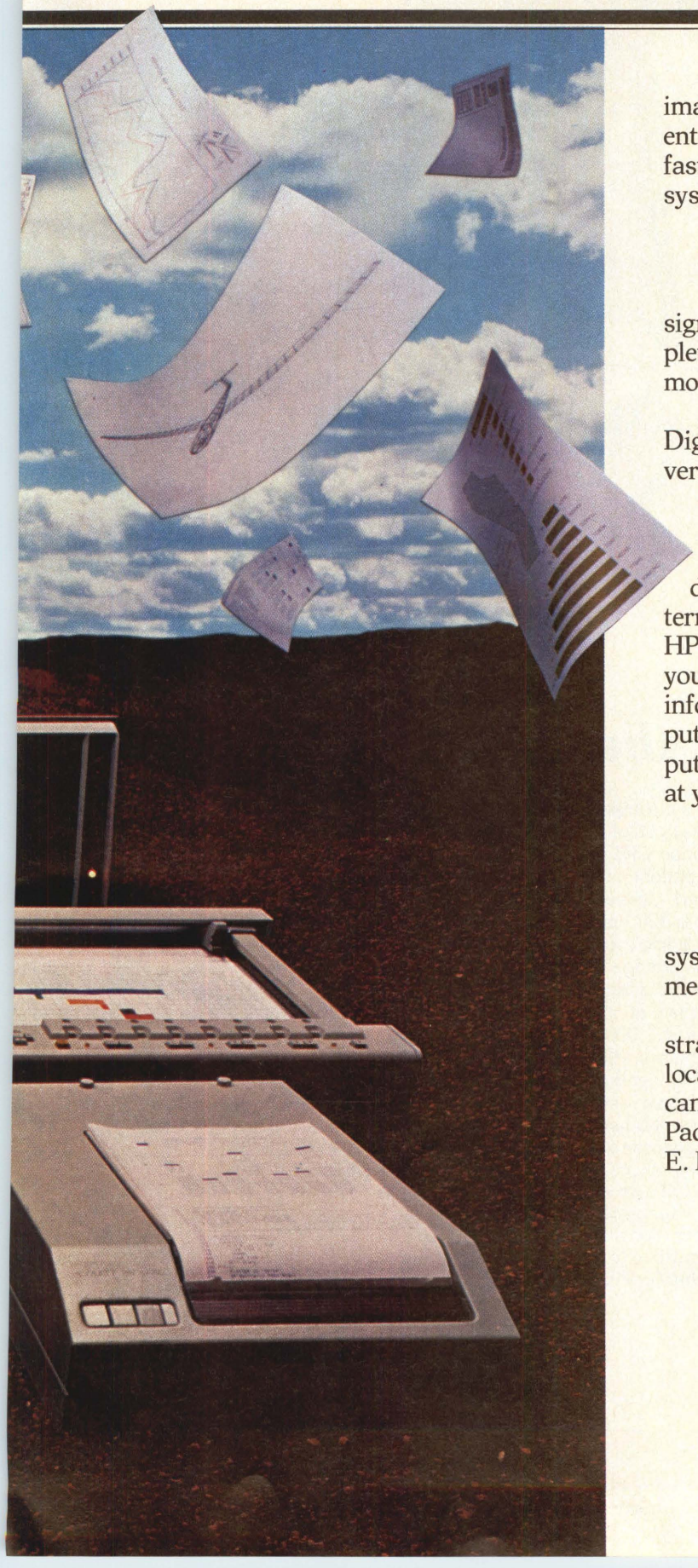

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FEATURE

*Adding horizontal parity bit and vertical parity words to discrete blocks of memory provides a lower cost, higher speed alternative to Hamming codes*

# Low cost alternative to Hamming codes corrects memory errors

As technology advances, computer memories become more dense and more affordable for small, low cost systems. Many freestanding terminals today have more memory capacity than entire systems that were considered large a few years ago. With this increased memory capacity and the inherent soft failure rate of high density memory chips, memory error correction is crucial, even in low cost products.

Memory error correction usually leads to a discussion of Hamming error correction codes. Hamming codes, however, add considerable overhead to the memory system cost, and degrade the memory cycle time significantly. For instance, to protect an 8-bit data word, 5 Hamming bits are required; 6 bits protect a 16-bit data word, and so on—adding 1 error correction bit for each power of 2 that the data word increases. This process accomplishes double-error detection with single-error correction, but errors involving more than 2 bits per word may not be detected. Codes must be generated and stored on each write cycle, and regenerated and checked on each read cycle. Hamming error correction codes represent 20% to 60% of the memory component cost and can degrade memory efficiency by as much as 25%. In low cost systems where memory is a large part of the product cost, or where throughput is critical, the addition of Hamming error correction can make a product noncompetitive in its market. This article describes an economical alternative to Hamming codes that is both efficient and effective in detecting and correcting soft failures in computer memories.

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## Horizontal and Vertical Parity

For double-bit error detection and single-bit correction, Hamming codes may be superior; but for smaller systems, the horizontal and vertical parity method is more practical and economical. This method of detecting and correcting errors is less expensive than Hamming codes and more efficient in terms of memory cycle degradation; it uses a combination of software/firmware and hardware logic. For error detection, at least one parity bit per memory word is required. Since this horizontal parity is either standard or an option on most memory systems, the only additional hardware requirement is logic for vertical parity words.

Errors are detected by the horizontal parity, which identifies the failed word by trapping the central processing unit (CPU) to a firmware routine that uses the vertical parity word to identify failed bits. The vertical odd parity word is the cumulative exclusive OR of blocks of words in memory; every memory write operation updates one vertical parity word. When the horizontal parity detects an error on a read operation, the firmware must save the pertinent vertical parity word, then recalculate the cumulative exclusive OR of all memory

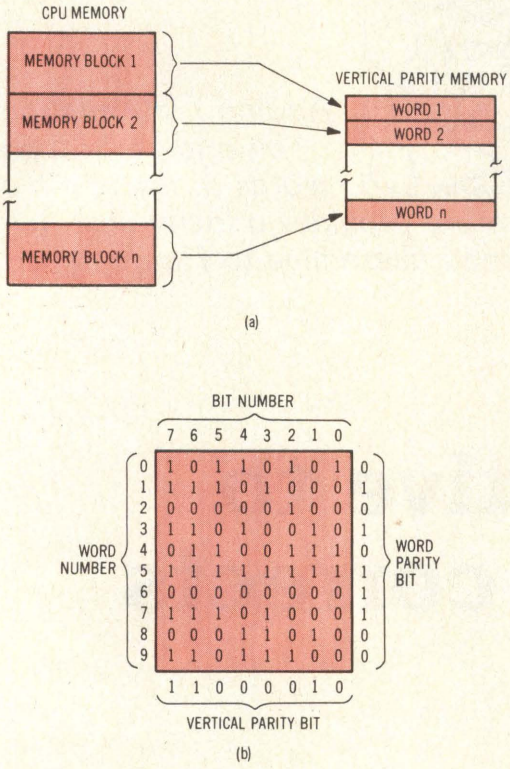



Fig 1 CPU memory. Memory is partitioned into blocks so that each vertical parity memory word represents exclusive OR of one block (a). Word parity detects errors and indicates word in error. Software or firmware uses vertical parity word for block in error to calculate correction data (b)

words in that block except that of the failed word. This result, exclusive ORed with the pertinent vertical parity word, produces the correct data to be stored in the failed location.

Fig 1 shows a memory block with 8 bits/word. For simplicity, the block in this example has only 10 words, although the actual number of words in a memory block is unimportant. Assume that on a read operation, word 3 changed from 11010010 to 11010110 (bit 2 in error). The CPU will trap to the firmware error correction routine that will: read the current vertical parity word 11000010 from the vertical parity memory; calculate the exclusive OR of all words except word 3; exclusive OR the result, 00010000, with 11000010, to produce 11010010, which is the original content of word 3; correct the content of word 3; and restore the vertical parity word.

Fig 2 shows the logical flow for the firmware correction routine. More than one horizontal parity bit per word would improve the error detection capability. All errors detectable by horizontal parity are correctable. While the primary target for this method is the single-bit soft failure, all single- and multiple-bit errors are correctable in a single memory word. If two or more words are simultaneously in error in a single block, correction cannot be accomplished; however, since the firmware error correction routine accesses all memory words, multiple words in error would be detected.

The possibility of multiple-word errors should be considered. Most memory error correction schemes only address single-bit errors. Hamming codes are generally designed for single-error correction with double-error detection. This means that any number of simultaneous errors in memory is correctable as long as no two bits in the same word are in error.

In 16k-bit memory chips, the worst case for soft (or correctable) errors should not exceed 10 failures/$10^6$ hours per chip. In a 128k-byte memory, the mean time between failures would be 65.10 days (assuming 24 hours/day, 7 days/week). But even at twice this rate, or one failure per month, the danger of two simultaneous errors is negligible. The software system can prevent memory failures from accumulating by periodically executing a low priority routine that reads from each memory location, thus detecting and allowing

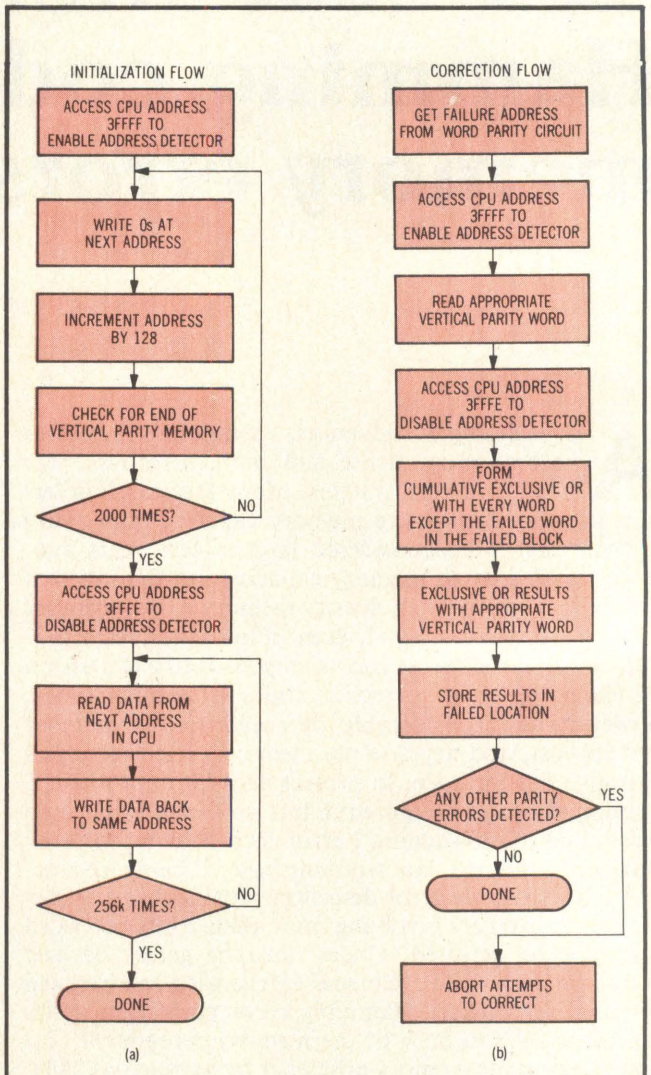



Fig 2 Initialization and correction. Flowcharts represent logical sequence followed by software or firmware to initialize vertical parity memory (a) and correct errors (b). Vertical parity memory is separate from CPU memory and is completely accessible by CPU. Write flow shows the effect of CPU write on vertical parity circuitry

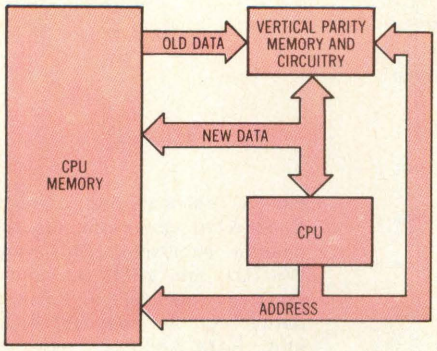



Fig 3 Vertical parity circuitry. Address and data from CPU are received by vertical parity circuitry, as well as "old data" from CPU memory locations being addressed. All additional hardware logic is contained in vertical parity memory and circuitry block

correction of errors during noncritical times. Recalculating and checking the vertical parity in a low priority routine would enhance this method. Then, errors that normal parity and Hamming codes would not find can be detected, although these failures could not be corrected since the failed word could not be identified.

## Vertical parity implementation

Fig 3 shows the vertical parity circuit relationship to the CPU and the CPU memory. The vertical parity circuit contains a memory that is the same width (in bits) as the CPU memory word without its parity bits, and should be static random access memory (RAM) for reliability unless it, too, is protected by parity. CPU memory is partitioned into blocks so that each word of the vertical parity memory represents the cumulative exclusive OR of one block of CPU memory. Then the length of the CPU memory block is determined by dividing the CPU memory length by the vertical parity memory length. Long blocks increase the possibility of multiple errors occurring simultaneously in a single block. Cost and safety of critical data must be considered to determine the optimum block size. Memory failure rate and the value of the data to be protected are the most important factors affecting this tradeoff.

In a byte-wide 256k-byte CPU memory and a byte-wide 2k-byte vertical parity memory, the CPU blocks are 128 bytes each. There would be a vertical parity word for every 128 bytes of CPU memory. During a write operation, the 11 most significant bits (MSBs) of the address are used to select the proper vertical parity word to be updated. In this example, the hardware cost overhead consists of the vertical parity logic, in addition to a single 16k memory chip.

The vertical parity circuitry must be implemented so that each write operation updates one word of the vertical parity memory to reflect the new vertical parity of the CPU memory block that was addressed. In the same example, adding a second 2k-byte chip to the vertical parity memory would reduce the memory block sizes to 64 bytes each. For small memories, such as in freestanding terminals, a CPU memory of 64k bytes and a vertical parity memory of one 2k-byte chip would provide block sizes of 32 bytes each. These short blocks would be desirable where the data to be protected are critical or where there is no convenient reload device.

### Initialization of the Vertical Parity

The initialization operation is a firmware or software routine that sets the vertical parity words to the cumulative exclusive OR of all data blocks in memory. Initialization should be performed anytime the validity of the vertical parity is in question, such as at power-up, after power interrupts, at load time, and after processor hardware failures. Initialization can be accomplished in two ways. One is to zero the vertical parity words, then store 0 (or any fixed value) in every memory location. This could be done prior to loading the system. The second initialization method can be used when the memory contains valid data. It simply consists of zeroing the vertical parity memory, then performing a read/write on every memory location.

### Vertical Parity Memory Logic

Fig 4 shows a block diagram of a vertical parity memory and associated logic. This example assumes an 8-bit

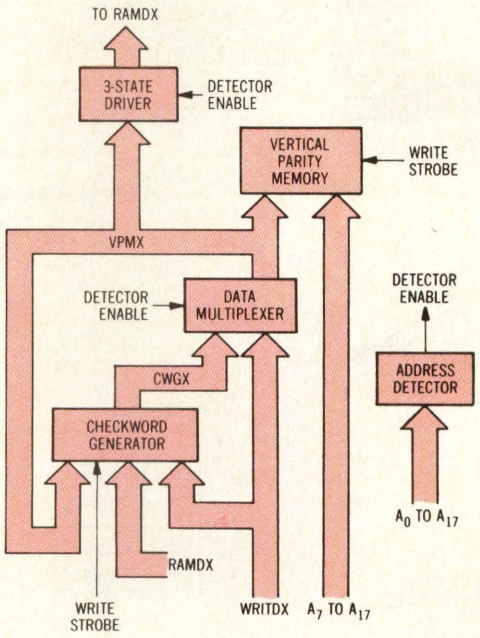
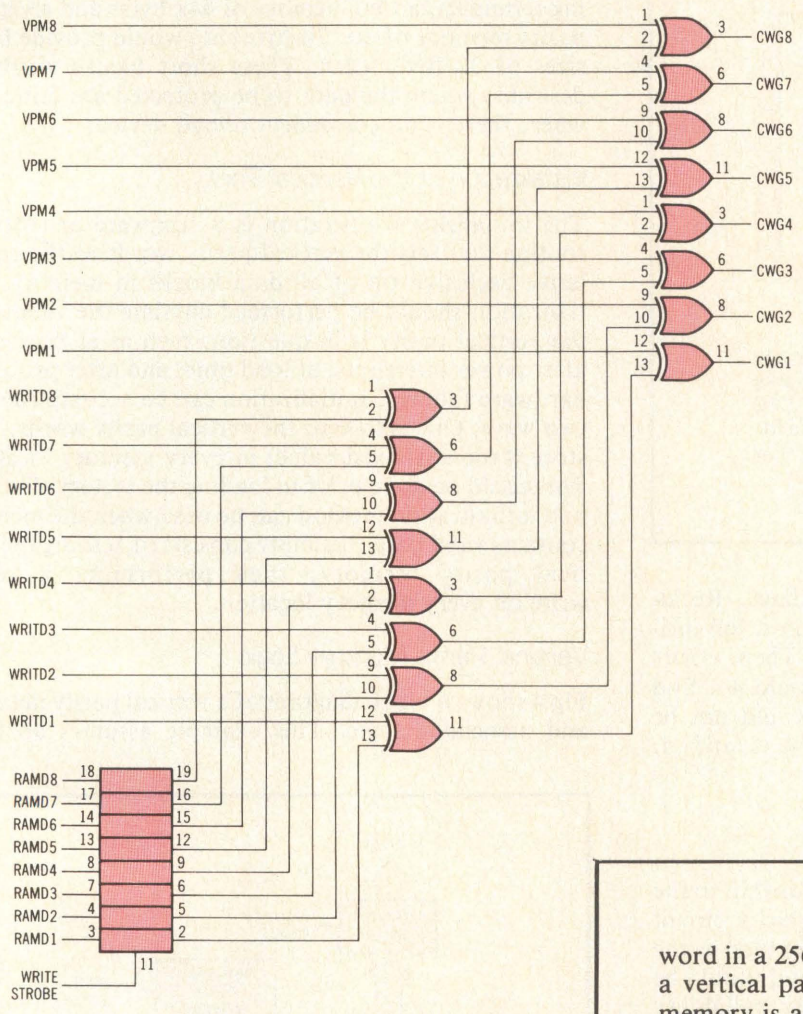
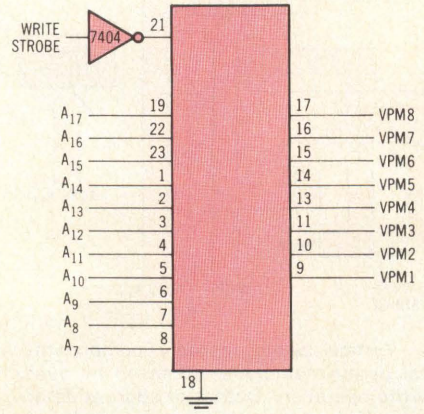



Fig 4 Vertical parity memory components. Vertical parity memory is accessed by every CPU write operation. Output of address detector determines whether access is to write initialization data or update vertical parity data. Read operations access vertical parity memory only if previous CPU instruction enabled address detector by sending address 3FFFF. Detector is disabled by sending address 3FFFE




CHECKWORD GENERATOR

(a)




VERTICAL PARITY MEMORY ARRAY

(b)

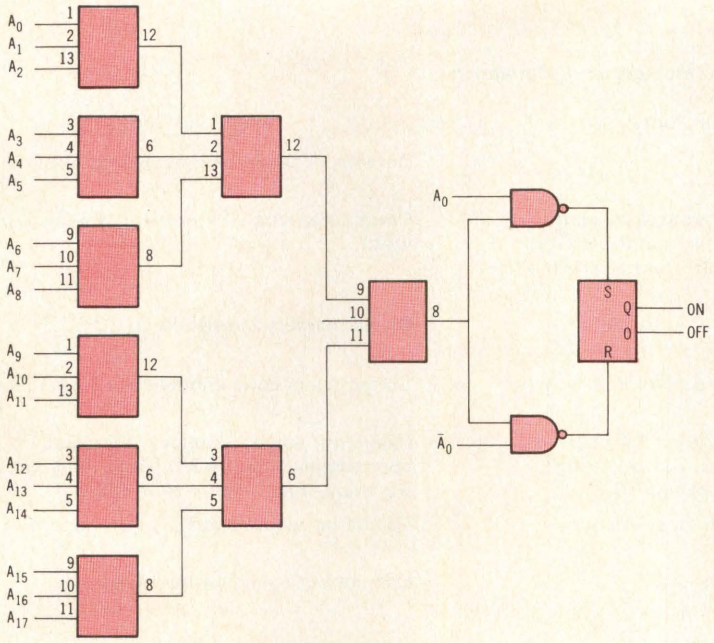
Fig 5 Vertical parity memory logic. Checkword generator (a) is two successive exclusive ORs using RAMD*X*, WRITD*X*, and VPM*X* as input to produce updates to vertical parity memory. Vertical parity memory array (b) is 2k by 8-bit static RAM. Address detector (c) is latched on when it detects all address bits equal to 1; it is latched off when it detects all address bits except $A_0$ equal to 1. Data multiplexer (d) is enabled by write strobe, and gates either write data from CPU or vertical parity from checkword generator. 3-state driver (e) gates VPM*X* to CPU data bus when address detector is on

*—Logic design by Walter Smith, NCR Corporate Engineering*

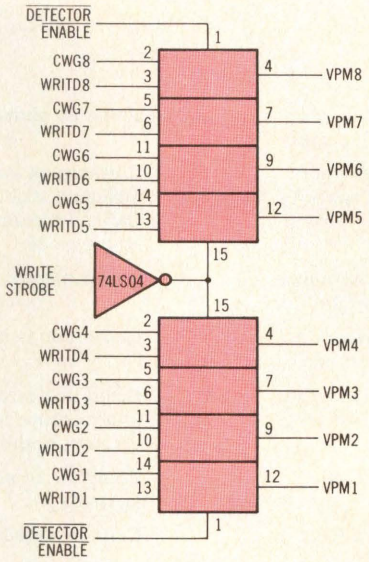
word in a 256k-word memory with 18 address lines, and a vertical parity memory of 2k words. When the CPU memory is addressed, the 11 MSBs are presented to the vertical parity memory. These, along with the write strobe, select 1 of the 2k vertical parity words and make the data (VPM*X*) available to the checkword generator and the 3-state driver. At the same time, the CPU data at the location to be written into (RAMD*X*) become available. Since this is a write operation, the write data (WRITD*X*) are already available at the checkword generator.

On some systems, it may be necessary to delay the write strobe to the CPU memory long enough for the new vertical parity word to be generated, but since the vertical parity memory is separate from the CPU memory, the two write operations can occur simultaneously. This delay (if necessary) is the only time penalty caused by the circuit. Use of Hamming codes would require a similar delay but of much longer duration because the codes take longer to generate and would reside in the CPU memory. In addition to the write delay, Hamming codes also cause a delay on each read operation, since the codes must be generated for each read to detect errors. The read delay is shorter than the write delay because the data would not necessarily need to be written back to memory.

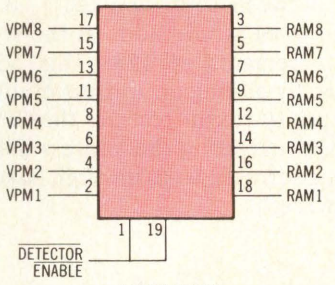
The vertical parity memory array, checkword generator, address detector, data multiplexer, and 3-state




ADDRESS DETECTOR
(c)




DATA MULTIPLEXER
(d)




3-STATE DRIVER
(e)

driver, all shown in Fig 4, are illustrated in Fig 5 with implementation in standard low power Schottky logic chips. The *checkword generator* is a 3-way exclusive OR, triggered by the write strobe. [See Fig 5(a).] RAMD*X*, exclusive ORed with WRITD*X*, is exclusive ORed with VPM*X* to generate CWG*X*, which goes to the data multiplexer. CWG*X* is the updated vertical parity word to be stored.

For initialization it is necessary to write known data (ie, zeroes) to the *vertical parity memory* [Fig 5(b)]; and for error correction it is necessary to read the contents of specific words. This is the function of the address detector, data multiplexer, and 3-state driver. The *address detector* [Fig 5(c)] is activated and generates a signal when it detects address 256k minus 1 (3FFFF)*. It is deactivated when it detects address 256k minus 2 (3FFFE). Thus, under software or firmware control, the vertical parity memory can be read and written without disturbing the CPU memory.

The address detector prevents the use of the last two words of the CPU memory. The *data multiplexer* receives CWG*X*, WRITD*X*, and the output of the address detector. During a write operation when the address detector is disabled, CWG*X* is gated and a vertical parity word is updated. When the detector is enabled, WRITD*X* is gated and a vertical parity word is initialized. [See Fig 5(d).] The 3-state driver receives VPM*X* and the output of the address detector [Fig 5(e)]. During a read, the VPM*X* is gated to RAMD*X* if the detector is enabled. When the detector is disabled, read operations in the CPU are undisturbed by the vertical parity circuitry. Output of the address detector must be input to the CPU memory to inhibit CPU data when the 3-state driver is gating vertical parity memory data. The preceding examples are shown using low power Schottky logic chips, but the entire logic for a byte-wide memory could be implemented in a single 40-pin large scale integration (LSI) custom chip. Additional chips could be combined to accommodate memories with larger words.

When directly addressing the vertical parity memory, the firmware should access the first word by using an

*Addresses are expressed in hexadecimal

**Memory Error Correction**

| | Vertical Parity | Hamming Codes |
|---|---|---|
| Detection Capability | Same as parity | Detects all single- and double-bit errors |
| Correction Capability | Corrects all errors detectable by parity, including multiple errors in a single word. Cannot correct multiple word errors in a single block | Corrects all single-bit errors in any memory word |
| Performance Degradation | Slows memory speed 0% to 2% | Slows memory speed 9% to 20% |
| Correction Method | Correction is done by software or firmware | Correction is done immediately by hardware |
| Component Cost | Using low power Schottky: 14 chips, approximate total $35. Using LSI logic: 2 chips, approximate total $20 | Using low power Schottky: 66 chips, approximate total $532. Using LSI logic: 66 chips, approximate total $382 |
| Ease of Implementation | Could be an add-on to most memory systems | To add-on requires redesign of memory |
| Hard Failures | Cannot correct hard failures | Can correct single-bit hard failures |

address between 00000 and 0007F. An address between 00040 and 000FF would address the second word, and so on, in increments of 128. This addressing could be simplified by adding an address multiplexer in which the vertical parity circuit receives the CPU memory address. Then after activating the address detector, the 2k bytes could be addressed 00000 through 00007F, which is normal for software.

## Summary

The frequency of soft memory failures increases with the density of the memory chips. When compared with the Hamming code method, vertical parity offers a low cost, easy to implement solution to correcting soft failures on most memory systems. Even though it is time-consuming to correct errors with this method, a 1-second interrupt is preferable to a reload or loss of critical data. The Table, "Memory Error Correction," compares the two methods and shows advantages and disadvantages of each. For the purpose of this comparison, a byte-wide 256k-byte CPU memory and a byte-wide 2k-byte vertical parity memory are assumed; the CPU memory in the example uses 16k-bit memory chips and has 1 bit/byte of word parity. The component cost for the Hamming method could be greatly reduced by multiplexing the memory into 32-bit words. While this would further degrade the memory performance by causing a read before each write to memory, it would reduce the number of additional memory chips that store the codes by 81%. The cost would then be approximately $256 for low power Schottky and $95 for LSI logic.

*About the Author:*

*Lee Edwards, a computer systems engineer for NCR Corporation, is currently project leader for the Total Reporting Accounting and Communications System (NCR TRACS). He discovered the error correction method discussed in this article while researching cost-effective methods of error correction in point of sales terminals. Mr Edwards holds a BS/BA degree in mathematics from the University of Texas at Austin.*

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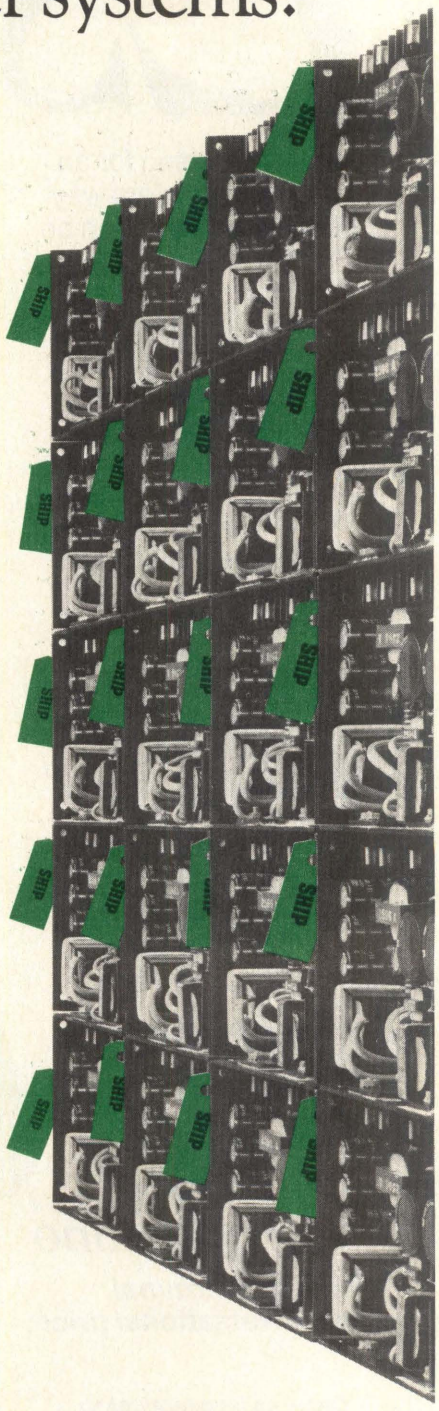


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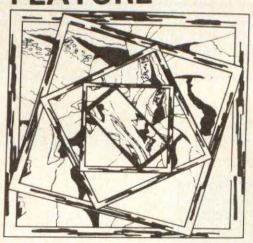

*Memory management add-on maps limited address space into larger virtual range, detects and corrects errors, and gives memory protection without changing CPU architecture*

# Virtual memory extension for an existing minicomputer

Demand for higher performance minicomputers has increased exponentially over the past decade as their prices have declined. Increases in "raw" processor speed, however, are not the complete answer to this challenge. To meet user needs effectively, designers must consider memory and software characteristics as well as applications requirements. Faster memories and increased use of direct memory access controllers have begun to use up the available bandwidth on the typical minicomputer memory bus. In addition, the logical memory space that the program can address directly and the physical amount of memory that can be attached to the system have become limiting factors in many applications.

Development software for minicomputers also has become increasingly complex, often requiring hardware enhancements to support the more sophisticated features. For example, the use of multitasking as a tool for breaking a complex task into an array of simpler tasks makes hardware support of synchronization primitives desirable for intertask communication. In addition, systems with a realtime control application running in the foreground and a potentially "hostile" development system running in the background require hardware protection mechanisms to ensure uninterrupted realtime service, even when software errors are encountered in the development software.

Perhaps the most complex class of software systems to be placed on a minicomputer to date is a general purpose, multi-user, timesharing system, providing multiple virtual program environments, with realtime and batch processing capability. Traditional minicomputers may offer memory mapping support, but generally do not provide the hardware support for protection and the page fault recovery required for an operating system of this type. The computer architecture of the NAKED MINI[R] 4, evolutionary product of the ALPHA 16 computer introduced in 1971, has been enhanced to accommodate these high level support features. Having evolved through the LSI-1, -2 and -3 computers, this minicomputer family comprises several software- and interface-compatible 16-bit minicomputers that differ only in performance and optional instruction set mix. Program resources consist of a 64k-word (128k-byte) address space; four general registers (two of which can be used for indexing); a stack pointer register; a stack limit register; and a status register.

## Extensions

The virtual memory support extension to the architecture was realized with four system components: the NM 4/95 central processing unit (CPU), the memory

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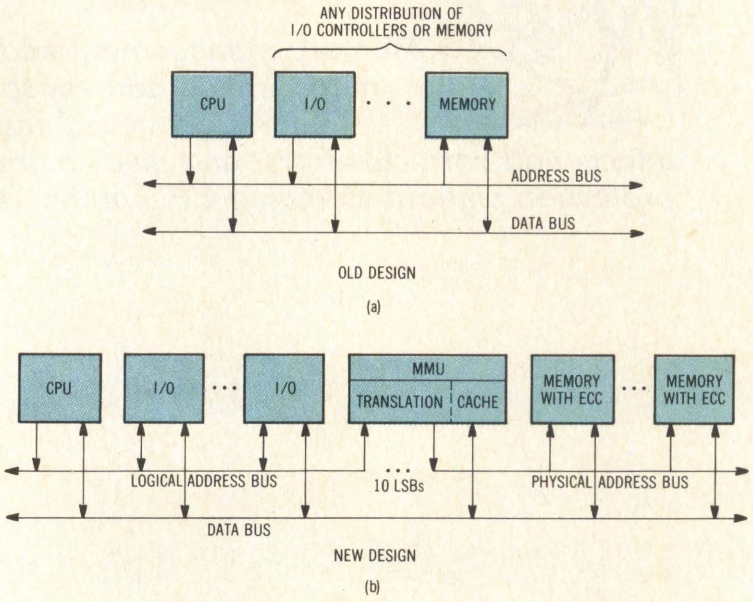



Fig 1 Extensions to architecture. Memory mapping for processor and DMA memory transfers is accomplished by splitting bus and inserting memory management unit (MMU), which translates logical addresses from processor and DMA controllers on one side of bus into physical addresses for memories on other side of bus

management unit (MMU), a 256k-byte memory with error correction, and a split version of the MAXI-BUS™ backplane. Fig 1(b) compares the relationships of these components to the original system configuration in Fig 1(a). The main difference between these two interconnection schemes is the logical split in the system bus, between the CPU and the system memory, which separates the bus into a logical address side and a physical address side.

The MMU bridges this split and translates a 16-bit logical address on one side of the bus into a 22-bit physical address on the other side. A straightforward mechanical implementation is possible because of the flexibility of the original motherboard system configuration. The standard motherboard duplicates MAXI-BUS signals on both sides of each slot in the chassis. Each slot accepts a pair of half-card products or a single full-card product. Thus, minor rewiring of the motherboard allows the full-card MMU to access both the logical and physical sides of the bus. Also, this unique location within the system permits a cache memory to be inserted.

## System protection

Each of the four system components enhances the original architecture and contributes to virtual memory support. To solve the architectural problem of foreground/background protection and multiple virtual environments, a user/system mode is added. This capability is implemented by including in the status register a protection bit which is saved and restored as part of the process context. When the protection bit is set to user mode, a user process is trapped if it attempts to execute privileged instructions, such as halt, input/output, context switch, or any instruction that attempts to change privileged bits in the status register (including the protection bit).

In user mode, the process is also prohibited from delaying interrupts for more than a fixed length of time. One of the subtlest examples of interrupts being masked by a program occurs when a multilevel, indirect memory reference is coded incorrectly. During multilevel indirection, the most significant bit of an indirect address specifies whether it is the address of the final operand or the address of yet another indirect address. The NM 4 architecture allows this feature, but does not limit the number of levels to which it can be taken, nor does it allow interrupts during the instruction. If the indirection goes through too many levels (or loops endlessly), a time-out occurs and the system traps the process.

Keeping a user process from executing potentially disruptive instructions is little protection if the process has access to the system address space. This final protection is implemented by putting in the status register a user/system map control bit, which selects either the system map or one of several user maps. The bit is protected from user modification and is overridden in the system map mode during interrupt and trap handling. A context save instruction is added; this instruction saves the entire context of the user process and loads a new context for the system process.

The user context is saved in the system address space, not in the user address space. This technique allows more efficient access to the context block by the system process and system independence of the user address space mapping. A group of locations specified by the context pointer, a new register added to the architecture, stores the user context. When a system process is saved in order to service an interrupt, the context save instruction pushes a partial context onto the system stack instead of a complete context into a context block. Therefore, multilevel interrupts are serviced with a minimum of context switching overhead.

Access to the user space by the system process is accomplished with the addition of the load from user space and the store to user space instructions. Other instructions added to support more complex features of the system are a pair of semaphore instructions for interprocess synchronization and a class of double-linked, list-manipulation instructions.

## Virtual memory

With the protection mechanisms just described, a user process can be mapped into an area of memory and run without being able to "escape" from its environment except through traps to the system process. The entire 128k-byte address space now is available to the user process because the system process no longer occupies user memory space. In a timesharing system where many user environments are being processed concurrently, the amount of memory required to keep each user mapped would be prohibitively expensive. Secondary storage, such as discs, can be used as a cheaper storage area for the user processes that cannot fit into the main memory. A scheduling algorithm can move the user environments back and forth between main memory and the disc as the machine cycles through the user processes. This procedure is referred to as swapping.

Swapping an entire user environment is wasteful because it is likely that only a small portion of the memory is needed for any short execution period. Only those pieces of memory that are needed should be brought in from the disc and mapped into the user environment. The NM 4/95 divides the user environment into 64 equal-sized pieces called pages, and swaps individual pages instead of the entire environment. Then, the system can vary the number of pages of the user environment that are in main memory or in secondary storage as the needs of the user task change. Once a required page is brought into main memory by the system, the user process resumes. This represents a true virtual memory system in that a user can assume at any given time that the entire address space is available, even when only a fraction of the space is actually available in main memory.

When a user process attempts to access a page that is not in main memory, the MMU aborts the memory cycle and informs the processor of the unsuccessful attempt. This action is referred to as a page fault. The NM 4/95 system is able to "back up" any instruction that causes a page fault, and reexecute the instruction using a page fault recovery procedure. The processor and MMU cooperate to save the information required by the page fault recovery routines. Firmware in the processor guarantees that the values of the registers saved in the context block are correct and need not be repaired by the software. This feature requires the firmware to ensure that register contents are not changed until after all the memory references of the instruction have been completed successfully. An example of how this restriction could be violated is the multi-register push instruction. The push instruction might have been implemented to advance the stack pointer as each register is stored, but then, if a page fault occurred, the pointer would be incorrect when the instruction was restarted.

## Addressing and mapping

One solution to the problem of page fault recovery is to use a temporary register as the stack pointer and to update the stack pointer after the last push operation is complete. The MMU remembers the correct program pointer and the fault address when a page fault is detected. Recovery software interrogates the MMU to acquire the program pointer and the fault address. The fault address is used to determine which page needs to be swapped in, and the program pointer is the process restart address.

The primary function of the MMU is to map the 16-bit logical address generated by the processor or direct memory access (DMA) controllers into the 22-bit physical address, decoded by the memories, which directly addresses 8M bytes of main memory. Address translation is accomplished using the page number of the logical address as an index into a 64-entry translation table or map. Each entry in the table specifies the page number of the corresponding physical address.

The processor can select either of two active maps: the system map, and one of several user maps. The MMU contains 16 maps: map 0 always is the system map, and a user map number register specifies which one of the 16 maps is the active user map. The active user map number can be switched with a single privileged I/O instruction. The processor also can switch from the system map to the user map between memory references, as is done during the load from user space instruction. DMA transfers are not restricted to the active system map and user map. The MMU detects DMA transfers and uses the map specified by the DMA map number register.

## Memory protection

In addition to the translation data contained in each map entry, there is also protection control information and access status information. The protection control field establishes four protection levels for each page: no access, read only, data only, and unrestricted access. The MMU traps the process if any protection violations are encountered and supplies fault information to the recovery software. The read-only protection level can be used to protect pure code segments. Thus, the segment

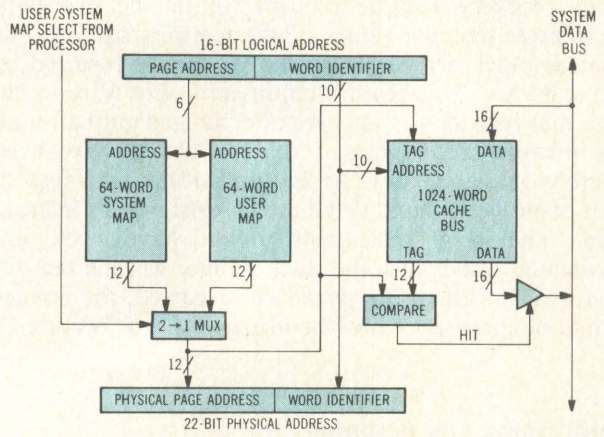



Fig 2 Memory management unit. MMU translates logical addresses into physical addresses. Signal from processor selects user map or system map, providing fast map switch for interrupt and trap handling. Because least significant address bits are not translated, high speed cache memory can be addressed in parallel with address translation, more than compensating for performance penalties

can be shared by two or more processes and still maintain protection. The data-only protection level is useful during program development because it allows the MMU to trap a runaway program at the first attempt to fetch an instruction from a data page.

The access status information recorded for each entry in the map indicates whether the page has never been accessed, accessed but not modified, or modified. This feature—coupled with protection, mapping, page fault recovery, and memory access control—allows the NM 4 architecture to be used for a full, hardware-supported virtual memory application. A working set is that portion of a user virtual address space that is mapped into main memory. With the information saved by the processor and MMU, the application software needed to handle a page fault and manage the user's working set can be quite simple. The system process usually limits the working set to a few pages. As the user process changes its location in memory, pages from the working set are moved to disc, and other pages are swapped into memory to replace them. By identifying the least frequently used pages, the "modified" access bits help to determine which pages should be swapped out to disc.

At the beginning of each time slice of a user process, the access bits for each page in the working set are reset. When a page fault occurs, the access bits are examined, and unmodified pages that have not been accessed are the first to be removed from the working set. No disc transfers are required to remove an unmodified page because a copy of the page already exists on the disc. Modified pages that have not been accessed recently are eligible for swapping, followed by modified pages that have been accessed recently.

The disadvantage of adding mapping to an architecture is that the address translation increases memory access time, slowing down the processor. However, because of the logical split in the NAKED MINI bus between the processor with DMA controllers and the main memory, a cache can be inserted. The cache is placed physically on the MMU printed circuit board, but it is located logically on the translated side of the map. It compensates for the time lost during translation; in fact, a system with the map and cache combination performs faster than a system without either component.

As shown in Fig 2, the cache is accessed in parallel with address translation, giving the memory system an average access time of only 115 ns. Because the 10 least significant bits of the logical address need not be translated, they are available at the beginning of a memory cycle. By using a high speed RAM that has a depth of 1k ($2^{10}$) or less, the cache access and address translation are completed at the same time. The output of the cache is compared with the 12 high-order bits of the physical address; if they match, the cache data are returned to the processor within 50 ns. By caching physical memory addresses instead of logical addresses, the cache never needs to be cleaned because of a translation table change.

DMA transfers, such as disc input/output, are not repetitive and are detrimental to cache performance. Therefore, the cache senses and ignores DMA references. The exception to this rule is one in which a write operation would invalidate a cache entry; in this case, the cache updates its entry to ensure valid data. The cache is a write-through type, and main memory always has the latest copy of the data.

If the cache does not have the data desired, or if the memory reference is a write, the translated address is passed to the main memory and a reference is initiated. Each main memory board also has a cache (Fig 3). This

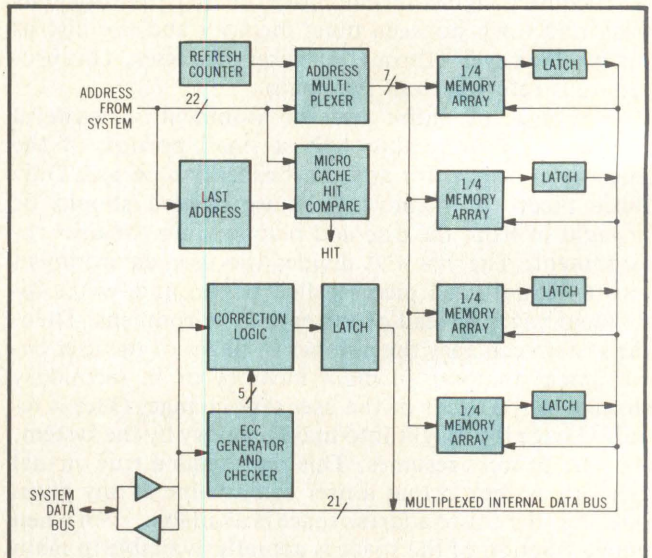
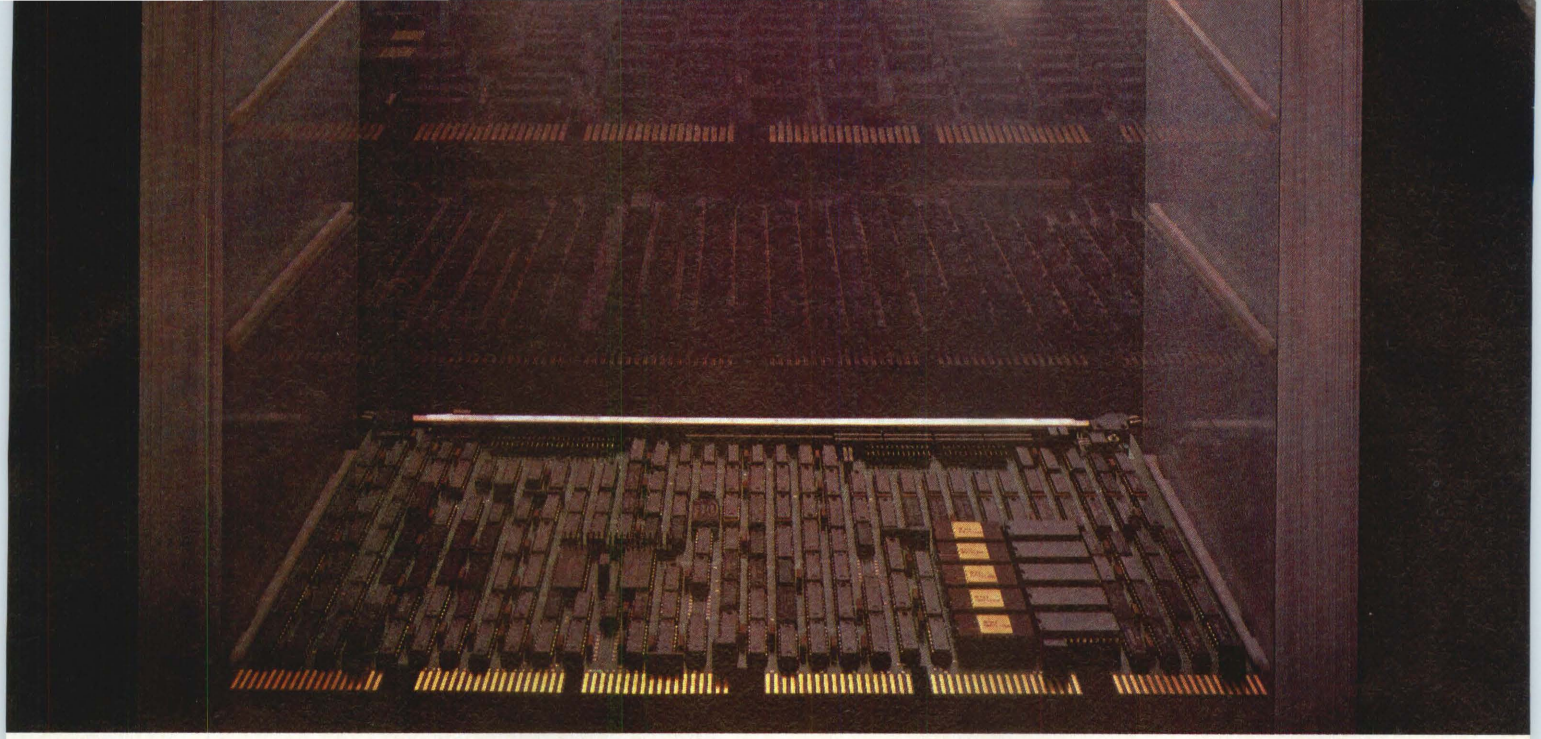



Fig 3 Look-around cache. Internal memory organization provides access to 4-word block of data during read operations. All four words are latched, and, if subsequent read operation requests one of these words, it is returned immediately without another memory cycle. Microcache performs well for sequential memory access, as is typical of DMA transfers



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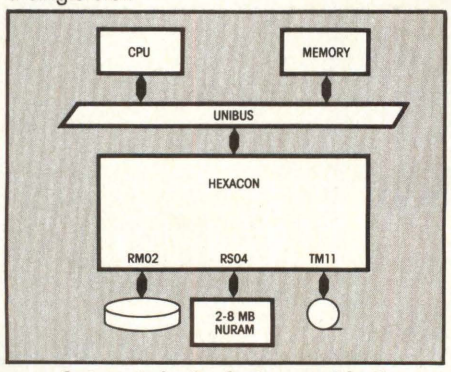


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smaller one is a 4-word (8-byte) look-around cache that holds a 4-word block of data. During a memory read, the memory accesses four words in parallel and latches the words in the cache. The words are a group of memory locations with addresses that differ only by the 2 least significant bits. If a subsequent read occurs from one of these locations, the proper word is immediately returned to the processor (or DMA controller).

The look-around cache functions well during sequential data accesses and complements the main cache, which functions well for repetitive accesses. DMA block read operations benefit greatly from the look-around cache. DMA write transfers, as well as CPU writes, are enhanced by a fast write capacity on each memory board. The fast write compatibility is accomplished by latching the address/data lines and acknowledging the memory transfer. The memory cycle continues internal to the memory board, while allowing the bus to be used for the next memory access.

## System reliability

Many features have been added to improve the integrity of the memory system. On power-up, translation is turned off, and the logical addresses pass directly onto the physical address lines, with the most significant lines forced to zero. By using input/output instructions, the system can make the translation table appear in the top 1k of the system address space. Then, it can be tested with a memory diagnostic to ensure its integrity before it is loaded with translation data and turned on.

An undetected failure in a map location could redirect a memory write into an area of physical memory outside a particular logical address space. In this case, a protect violation would occur. Checking parity across the translation data prohibits this unacceptable situation. Upon detection of a failure, this checking mode initiates a system trap before any memory modification occurs. In some cases, failure in one of the maps can be recovered by loading another map and restarting the preempted program. Maintenance personnel then would be notified of the degraded performance.

Parity also is maintained across the entire cache data and tag fields. If an error is detected, the cache simply does not respond, and a reference is made to main memory. Thus, cache errors are transparent to the running process. Software can periodically poll an MMU error. A cache hit indicator, when used with cache control bits, allows a software diagnostic to verify the cache update and hit logic. If the cache is of questionable integrity, it can be disabled by software or by a manual switch on the board.

All memories on the system contain error check and correction (ECC) logic. The method used is single-error correction and partial double-error detection. It is less expensive than full double-error detection but has the potential shortcoming of not detecting all double-bit errors. A memory refresh technique all but eliminates this problem. With this technique, it is possible to sweep through every memory location to correct single-bit errors, instead of refreshing just the rows of a memory array to prevent loss. Each row is accessed often enough to prevent data loss, and the entire memory is corrected every 2 s. This clean-sweep technique corrects soft memory errors, even those in seldom used memory locations. It keeps the single-bit errors from accumulating into double-bit errors that can never be corrected and that might even go undetected.

When an error is corrected, a light emitting diode flashes on the rear of the board, and a signal is generated. The MMU latches this signal and informs the software that a bad memory exists. If the error frequency increases, a memory diagnostic can be run to identify the fault board. Special instructions are added that give the software diagnostic access to the ECC code bits. By reading and writing the ECC code, the diagnostic can test the error detection and correction circuitry. The ability to write the ECC code allows the detection of single-bit errors even while the memory is correcting errors. By remapping memory pages, a low priority, self-diagnostic program can use idle CPU time continuously to verify system integrity.

*About the Author:*

*Peter Vogt is a senior design engineer in Computer Automation's NAKED MINI Division. Prior to joining Computer Automation in 1975, he worked at Collins Radio. He holds a BSEE in computer engineering from California State University at Long Beach.*

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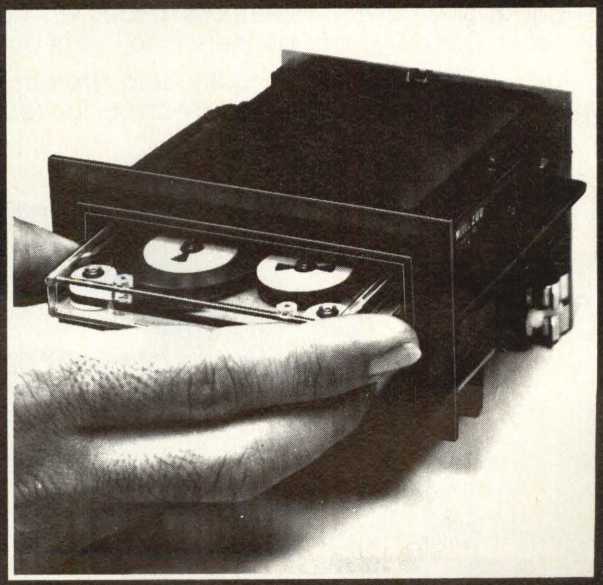

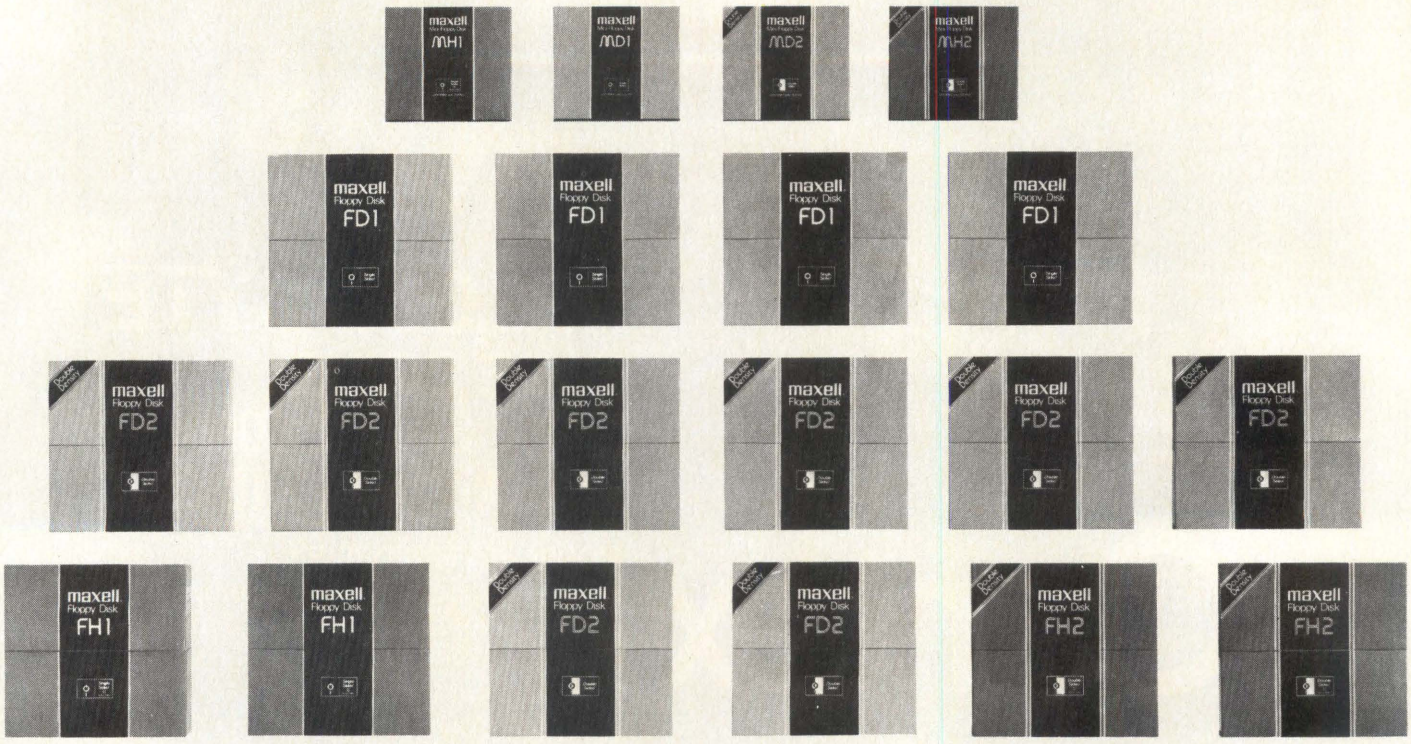


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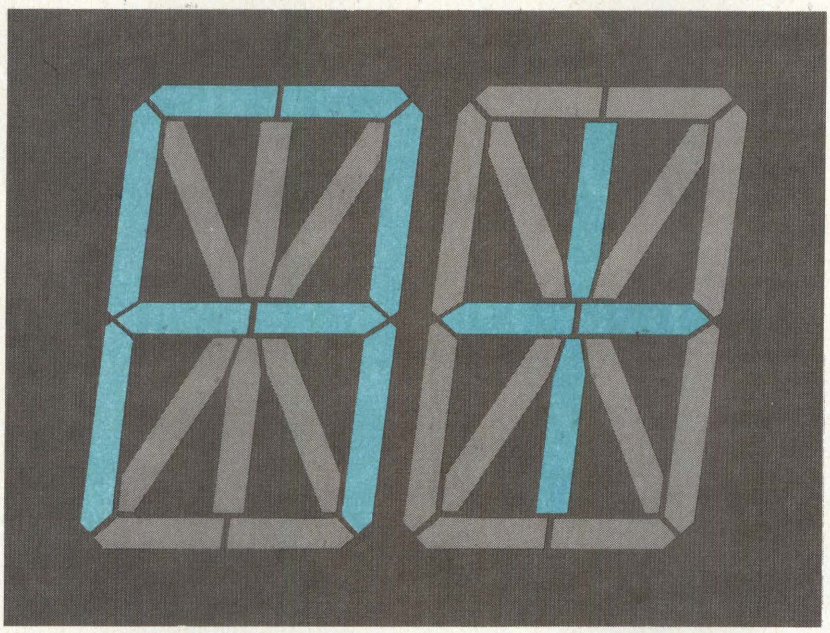

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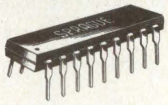

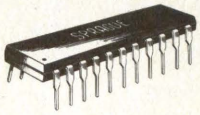

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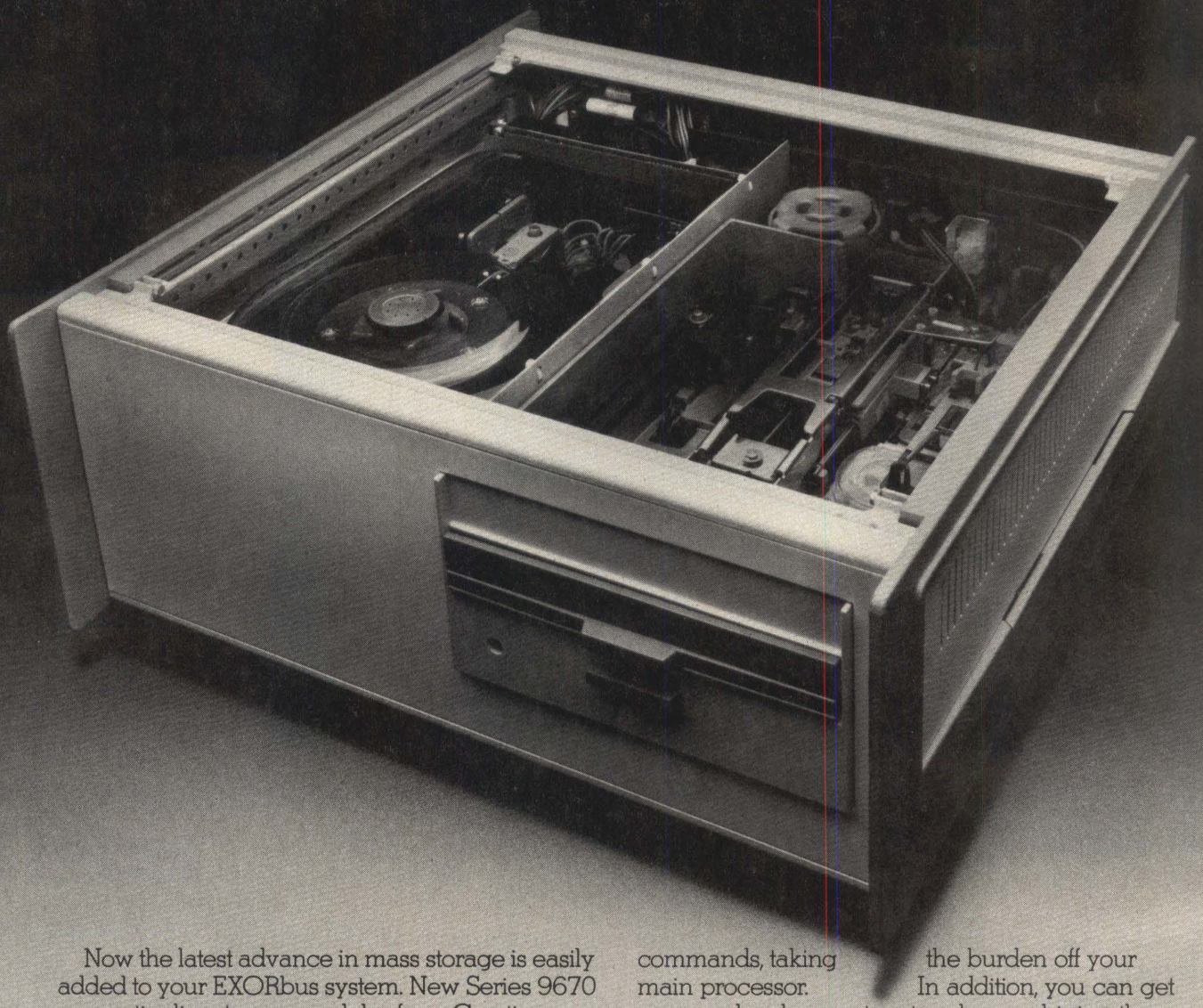

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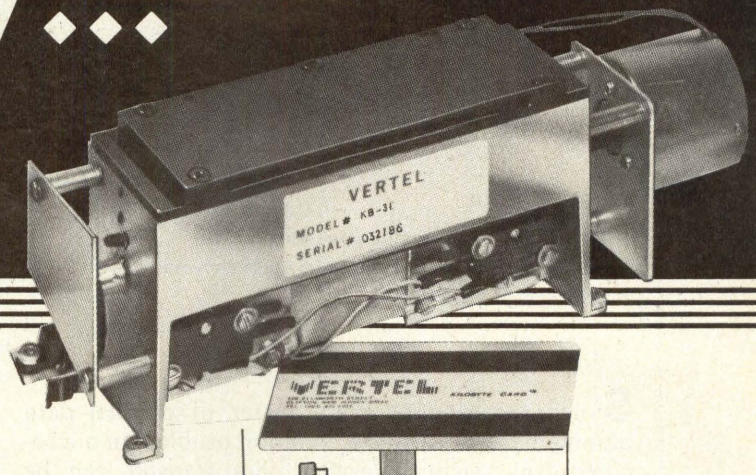


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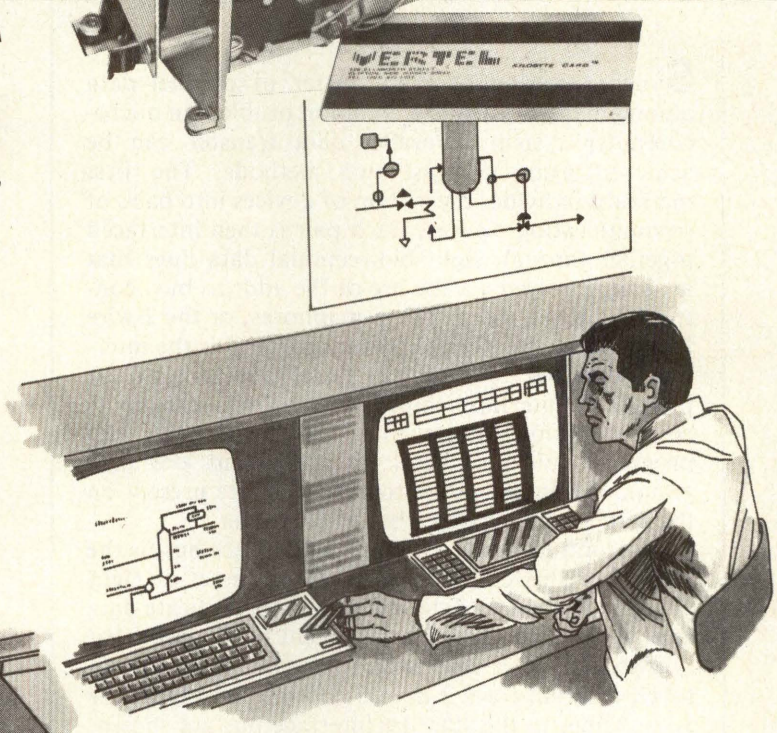

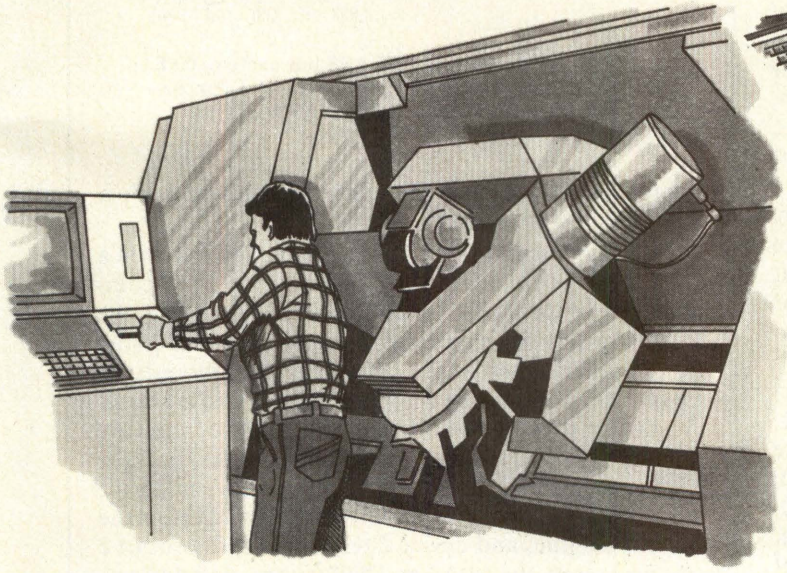

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# Interfacing Fundamentals: Bused Flags

**Peter R. Rony**

**Department of Chemical Engineering**
**Virginia Polytechnic Institute and State University**
**Blacksburg, VA 24061**

Synchronization of the transfer of parallel data among many devices is a common problem in microcomputer systems. Parallel data transfer can be achieved using at least two methods. The first method subdivides the system of devices into pairs of communicating devices. Each pair is then interfaced together through eight bidirectional data lines that are synchronized via the use of the address bus, control bus, flags, interrupts, semaphores, or the 2-wire handshake. One example of this method is the interfacing to the 8080A central processing unit of the peripheral interface chips—the 8251 programmable communication interface, 8253 interval timer, 8255 programmable peripheral interface, and 8259 programmable interrupt controller—that are present on the Intel SBC 80/20 single-board computer.

A second method, the IEEE 488 interface bus, is the subject of this column; it uses a single set of eight bused bidirectional data lines that communicate data among all of the devices, plus eight bused flags that synchronize such communication. Fig 1 provides a block diagram for a 3-device system. Only 11 of the 16 bus lines in the IEEE 488 interface bus are shown. The other five IEEE 488 signals—IFC, ATN, SRQ, REN, and EOI—are not essential to this discussion. DIO1 through DIO8 are bused bidirectional data lines; there is nothing unusual or special about their behavior. Between each device and the DIO1 to DIO8 interface bus lines are eight sets of receivers and drivers, that is, eight IEEE 488 bus transceivers. Either 3-state or open-collector drivers are used; for further details, consult the IEEE Std 488-1978 document.[1]

The three bus lines that synchronize the bidirectional data transfer are the interesting aspect of Fig 1. These bus lines participate in the 3-wire handshake protocol, and are called NDAC (not data accepted), NRFD (not ready for data), and DAV (data available). All three are based on the principle of the *bused flag*. In most articles on the IEEE 488 bus, the existence of bused flags is assumed to be understood, and attention is directed instead to hardware [large scale integration (LSI) chip sets], to state diagrams, and to the timing diagrams and flowcharts that summarize the characteristics of the 3-wire handshake.[2-12] Since the concept of a bused flag is one of the important ideas contained within the IEEE 488 standard, it is

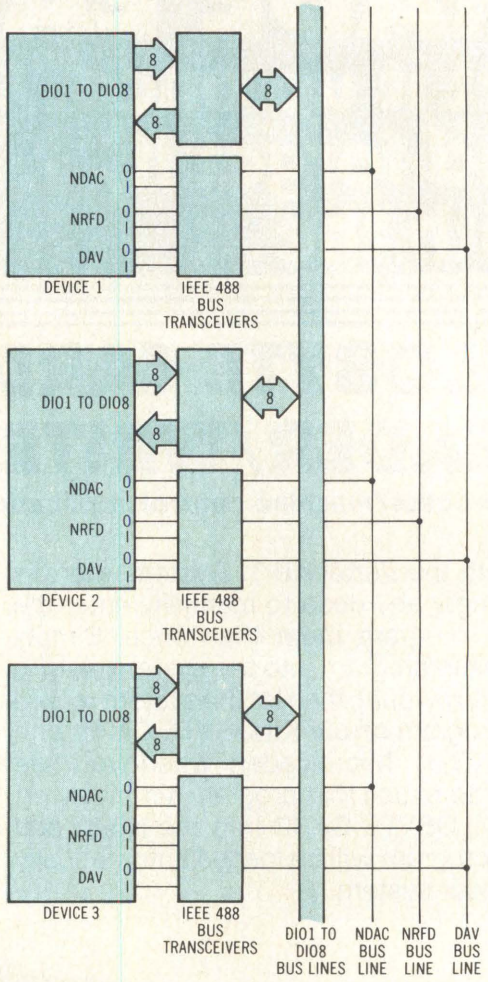
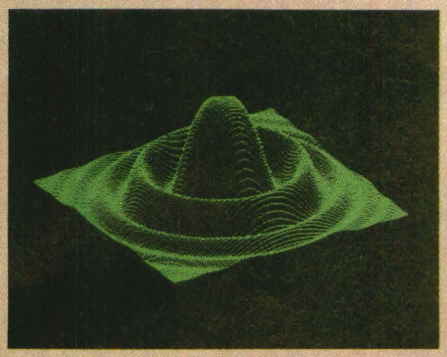



Fig 1 Three-device IEEE 488 bus system. IEEE 488 bus transceivers provide critical link between each device and IEEE 488 bus

appropriate to discuss the characteristics of such a flag and how it is used.

It is again useful to make the distinction between a flag and a semphore in the context of a pair of communicating devices. As discussed previously,[13] the state of a flag is set or reset by one device and tested by the other, whereas the state of a semaphore is set by one device, reset by the other, and tested by both. According to these definitions, NDAC, NRFD, and DAV appear to possess semaphore characteristics, but it is easy to be misled. In Fig 1, for example, when device 1 outputs data to device 2, device 1 sets and resets the DAV signal line, and device 2 tests it. In turn, device 2 sets and resets the NDAC and NRFD lines, and device 1 tests them. The direction of communication can be changed, however, and device 2 can output data to device 1. In such a situation, device 2 now sets and resets the DAV signal line, and device 1 tests it; also, device 1 sets and resets the NDAC and NRFD signal lines, and device 2 tests them. Thus, the DAV, NDAC,

*(continued on page 164)*



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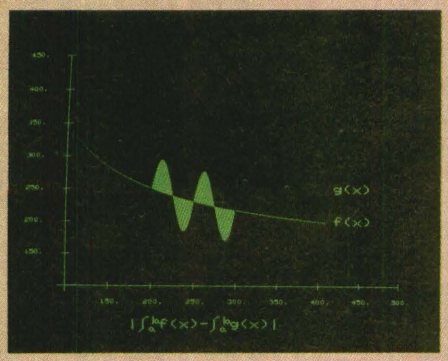

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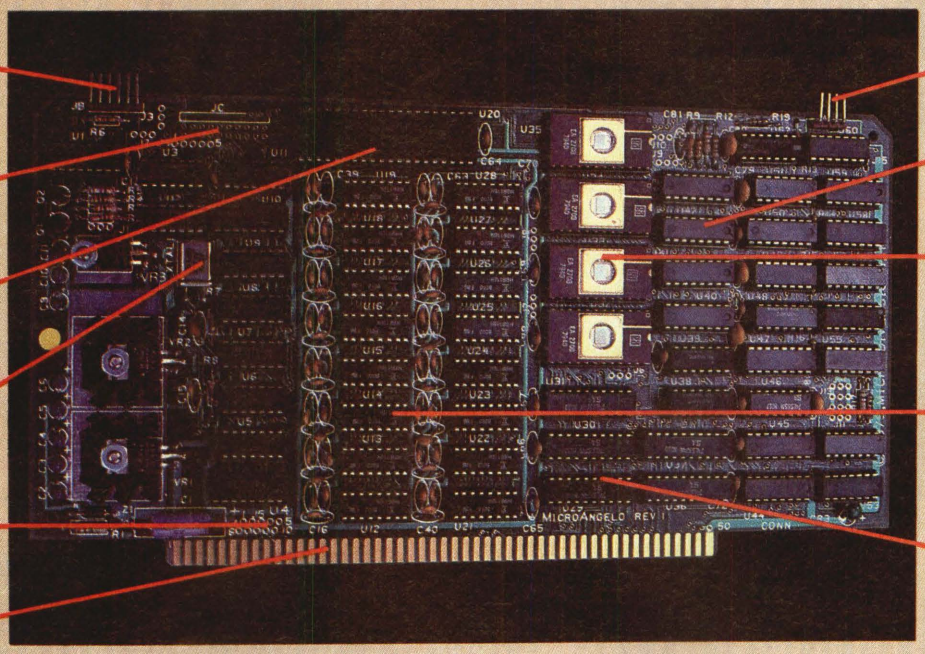


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and NRFD signal lines may be set, reset, and tested by both devices. Are they semaphores? Our suggested answer is that they are not. Recall that bidirectional data transfer between two devices required two semaphores, one for each direction; for the transfer of data in a given direction, both devices tested the appropriate semaphore.[14] Such is not the case with the IEEE 488 bus system depicted in Fig 1.

For the transfer of a single byte of data in one direction, DAV, NDAC, and NRFD act as flags. Consider the interface diagram for the NDAC bus line (Fig 2). Open-collector busing is used, as required by the IEEE 488 standard, with a 3-k Ω resistor tied to 5 V and a 6.2-k Ω resistor tied to ground.[1] Each of the three devices communicates with the NDAC bus line via a single transceiver, which is a combination of an inverter as a receiver (R) and an open-collector inverter as a bus driver (D). Each device outputs (O) its NDAC flag state, and inputs (I) the status of the NDAC bus line. The NDAC bus line possesses the wire-ORed negative-logic convention that is characteristic of open-collector busing.

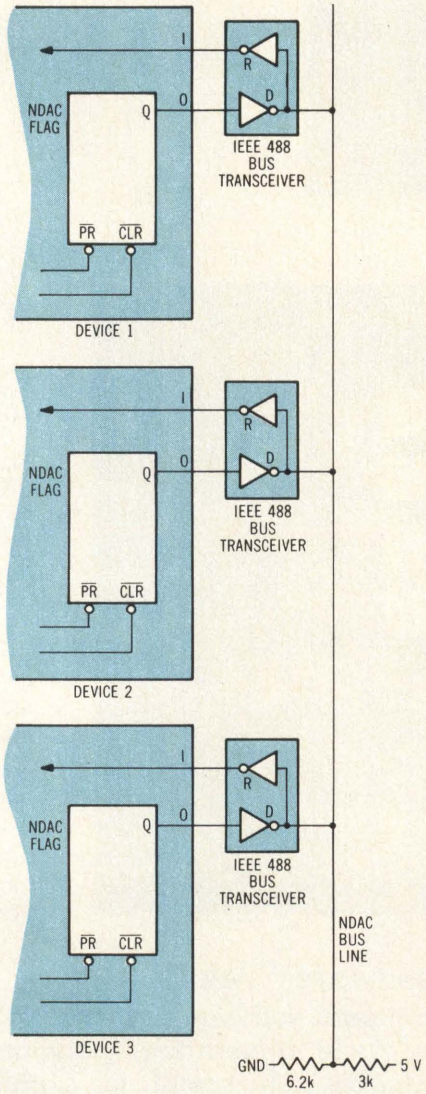


Fig 2 Three-device IEEE 488 NDAC bus line. Each of three NDAC flags requires separate IEEE 488 bus transceiver. NDAC bus line is open-collector, with 6.2-k Ω resistor connected to ground and 3.0-k Ω resistor connected to 5 V

It is easy to confuse the coded logic state with the electrical signal level on either side of the IEEE 488 bus transceiver shown in Fig 2. Fig 3 assists the interpretation. On the left of the bus transceiver, positive transistor-transistor logic (TTL) is employed for the NDAC flag, with GND potential corresponding to logic 0 (false) and 5 V corresponding to logic 1 (true). To the right of the transceiver, a negative-logic bus is employed, with the low (L) electrical state ($\leq$0.8 V) corresponding to logic 1* (true), and the high (H) electrical state ($\geq$2.0 V) corresponding to logic 0* (false). The asterisk (*) represents states coded in negative logic. Interconversion between positive TTL logic and the negative-logic bus is accomplished with inverters.

A truth table for the NDAC bus line summarizes the logic relationships between the three TTL NDAC flags and the NDAC bus line in Fig 2. The logic states for the NDAC flag for device X have the following meanings:

0 (False) Device X has accepted current data from DIO1 to DIO8

1 (True) Device X has not accepted current data from DIO1 to DIO8

The logic states for the NDAC bus line have the following meanings:

0* (False) All of the devices have accepted current data from DIO1 to DIO8

1* (True) Not all of the devices have accepted current data from DIO1 to DIO8

If any NDAC flag in Fig 2 is at true, the NDAC bus line is pulled true to indicate that all of the devices have not accepted data from DIO1 to DIO8.

The interface diagram for the NRFD bus line is identical to that for the NDAC line in Fig 2; compare

*(continued on page 166)*

**NDAC Bus Line Truth Table**

| NDAC Flag Device 3 | NDAC Flag Device 2 | NDAC Flag Device 1 | NDAC Bus Line |
|---|---|---|---|
| 0 | 0 | 0 | 0* |
| 0 | 0 | 1 | 1* |
| 0 | 1 | 0 | 1* |
| 0 | 1 | 1 | 1* |
| 1 | 0 | 0 | 1* |
| 1 | 0 | 1 | 1* |
| 1 | 1 | 0 | 1* |
| 1 | 1 | 1 | 1* |

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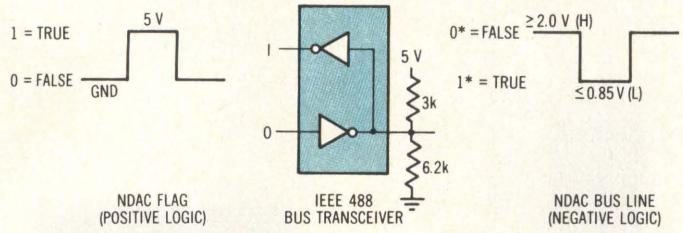


Fig 3 Summary of NDAC flag and bus line logic. At device level, positive logic is used frequently. At bus level, negative logic is required by IEEE Std 488-1978. Asterisk (*) refers to bus line logic

the NRFD truth table. Logic states for the NRFD flag for device X have the following meanings:

0 (False) Device X is ready for the next data byte from DIO1 to DIO8

1 (True) Device X is not ready for the next data byte from DIO1 to DIO8

The logic states for the NRFD bus line have the following meanings:

0* (False) All of the devices are ready for the next data byte from DIO1 to DIO8

1* (True) All of the devices are not ready for the next data byte from DIO1 to DIO8

If any NRFD flag is true, the NRFD bus line is pulled true, thus indicating that all of the devices are not ready for the next data byte from DIO1 to DIO8.

The interface diagram for the DAV signal is identical to that in Fig 2, but the truth table for the DAV bus line is different from the DAV and NRFD tables. Logic states of the DAV flag for device X have the following meanings:

0 (False) Device X does not have data available for DIO1 to DIO8

1 (True) Device X has current data available for DIO1 to DIO8

Logic states for the DAV bus line have the following meanings:

0* (False) None of the devices has data available for DIO1 to DIO8

1* (True) A single device has current data available for DIO1 to DIO8

Observe that only one device at a time is permitted to output data to DIO1 to DIO8. Four of the entries in the DAV truth table are not allowed by the IEEE 488 standard.

To summarize the information provided here for NDAC, NRFD, and DAV, it is appropriate to consider the 3-wire handshake timing diagram. (See Fig 4.) A single device in Fig 1 is assumed to be the source of data, or *talker*, and one of the other two devices is assumed to be an acceptor of data, or *listener*. The remaining device is assumed to be inactive. Fig 4 differs from the 3-wire handshake diagrams given in other articles[5-12] in one significant respect: the timing diagrams for the talker and listener TTL flag signals are provided in addition to the timing diagrams for the DAV, NRFD, and NDAC open-collector bus lines. Defining two types of data will aid the discussion of Fig 4: "current" data, which are data being transmitted during the current handshake cycle, and "next" data, which are data to be transmitted during the next handshake cycle. The reason for making such a distinction is that the state of the NRFD bus

*(continued on page 168)*

**NRFD Bus Line Truth Table**

| NRFD Flag Device 3 | NRFD Flag Device 2 | NRFD Flag Device 1 | NRFD Bus Line |
|---|---|---|---|
| 0 | 0 | 0 | 0* |
| 0 | 0 | 1 | 1* |
| 0 | 1 | 0 | 1* |
| 0 | 1 | 1 | 1* |
| 1 | 0 | 0 | 1* |
| 1 | 0 | 1 | 1* |
| 1 | 1 | 0 | 1* |
| 1 | 1 | 1 | 1* |

**DAV Bus Line Truth Table**

| DAV Flag Device 3 | DAV Flag Device 2 | DAV Flag Device 1 | DAV Bus Line | Comments |
|---|---|---|---|---|
| 0 | 0 | 0 | 1* | No output data available |
| 0 | 0 | 1 | 0* | Output data available (from device 1) |
| 0 | 1 | 0 | 0* | Output data available (from device 2) |
| 0 | 1 | 1 | — | Not allowed |
| 1 | 0 | 0 | 0* | Output data available (from device 3) |
| 1 | 0 | 1 | — | Not allowed |
| 1 | 1 | 0 | — | Not allowed |
| 1 | 1 | 1 | — | Not allowed |

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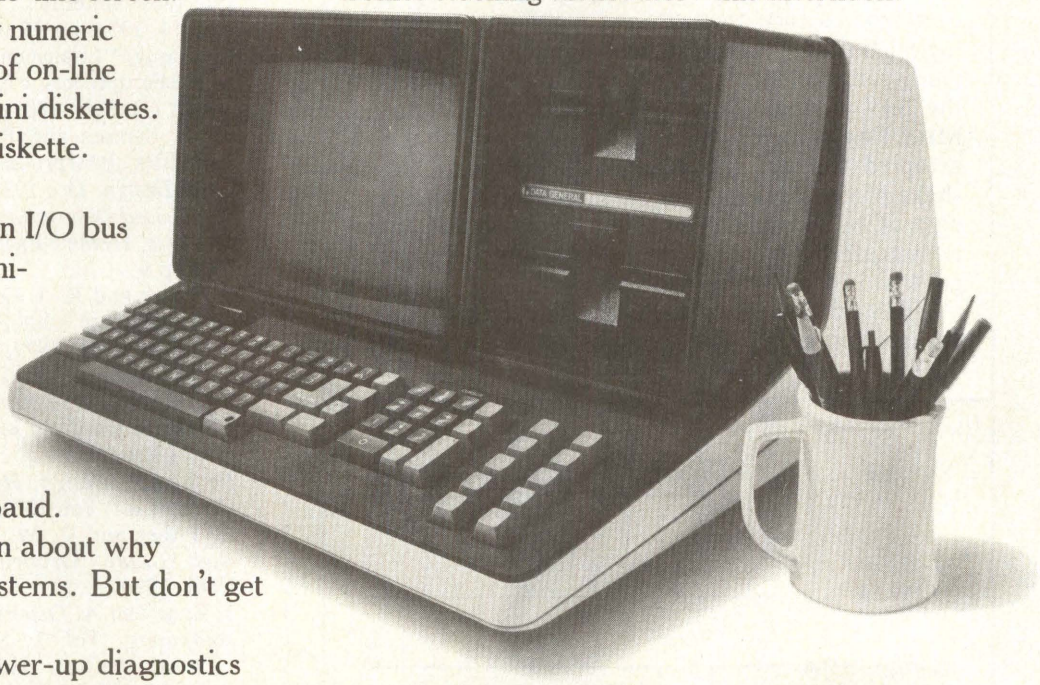

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line, after it has become true (logic 1*), applies to the next data byte, whereas the state of the NDAC bus line, while the DAV bus line is true (logic 1*), applies to the current data byte.

Initially, the talker in Fig 4 is not outputting data (DAV is false) and the listener is not ready for (NRFD is true) and has not accepted (NDAC is true) the next data byte. The talker outputs the current data byte to DIO1 to DIO8; detects the NRFD = logic 0* (false) condition; and sets its DAV flag to logic 1 (true). The listener detects the DAV = logic 1* (true) condition; sets its NRFD flag to logic 0 (true) to indicate that it is not ready for the next data byte; at its own rate, accepts the current data byte from the DIO1 to DIO8 bus; and resets its NDAC flag to logic 0 (false). The talker detects the NDAC = logic 0* (false) condition; resets its DAV flag to logic 0 (false); tests to determine whether more data must be output; outputs the next data byte to DIO1 to DIO8; and waits until NRFD = logic 0* (false), which indicates that the listener is ready for this "next" data byte. The listener detects the DAV = logic 0* (false) condition and sets its NDAC flag to logic 1 (true) to indicate that it has not accepted the next data byte. With the 3-wire handshake protocol, each listener can accept and process data at its own rate. The rate at which output data are transferred from talker to one or more listeners is governed by the slowest listener.

With positive and negative signals or buses, positive and negative mnemonics and signal conventions, the occasional absence of true/false labels on 3-wire handshake timing diagrams, the use of high/low instead of true/false as labels on some timing diagrams, and the use of diagrams that are not identical to, or the complement of, the diagrams given in the IEEE Std 488-1978 document, it is no surprise that engineers often have difficulty in learning the basic characteristics of the IEEE 488 bus. One useful reference on the subject is the introductory text by Fisher and Jensen.[10]

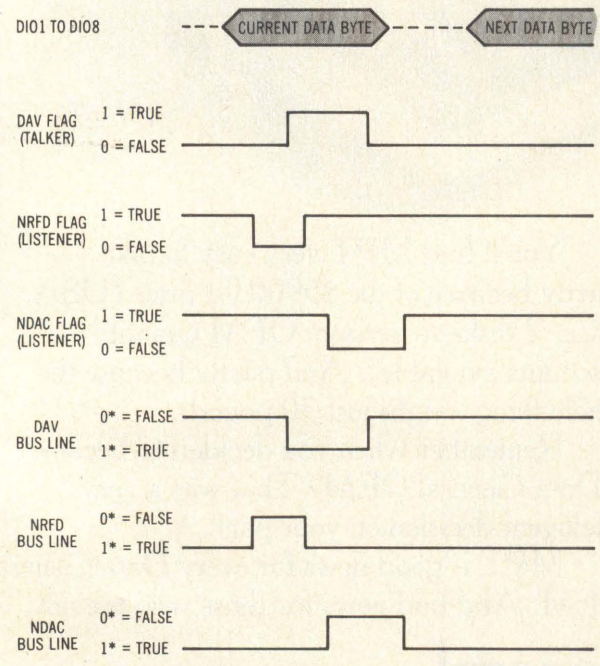


Fig 4 Three-wire handshake timing diagram. Positive logic is assumed for flags, and negative logic is required for bus lines

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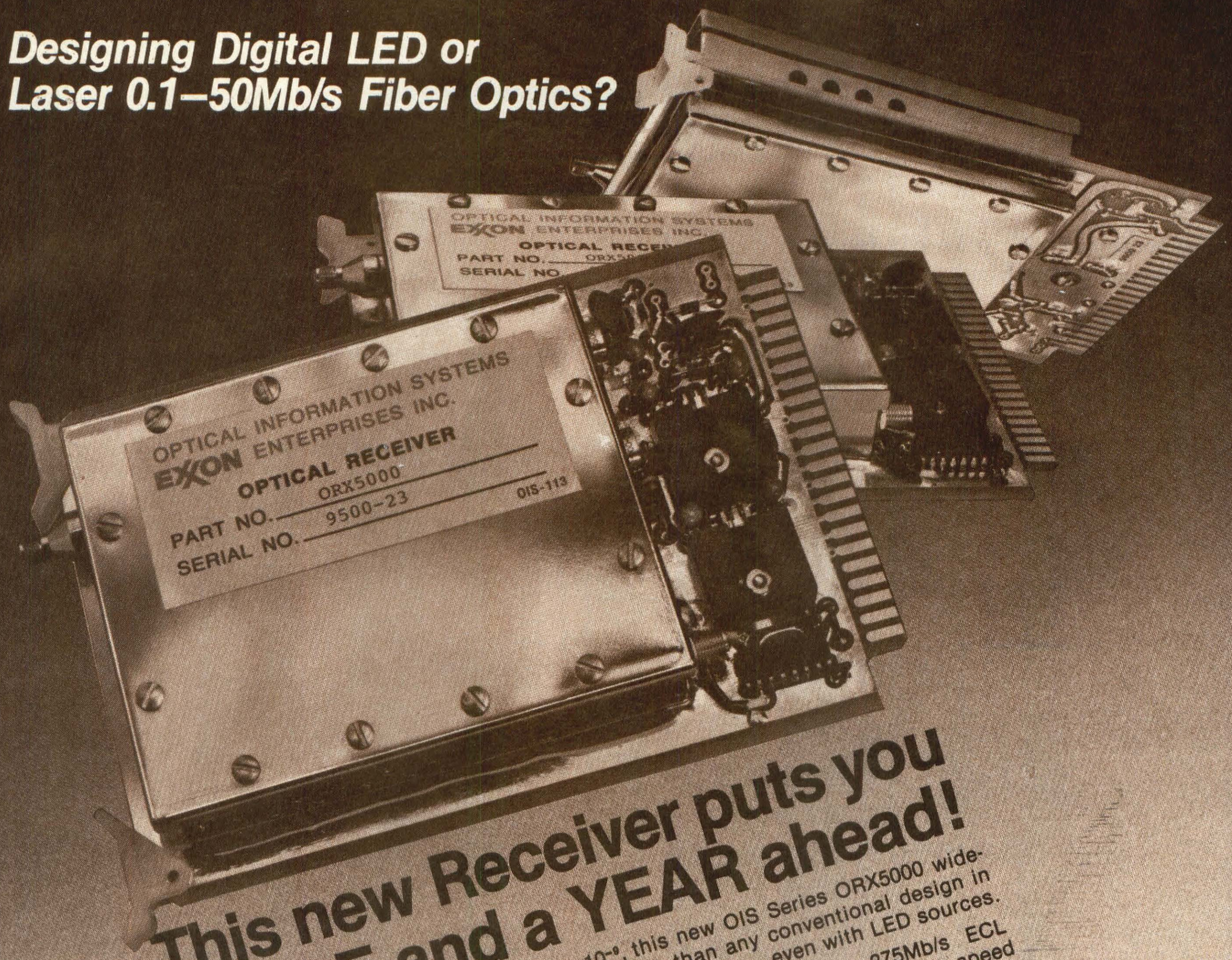


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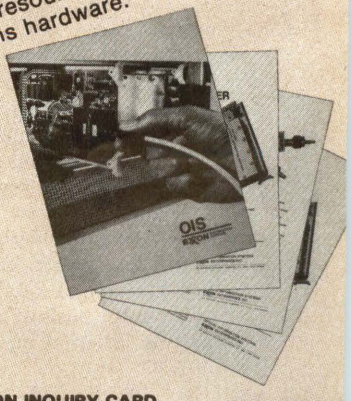


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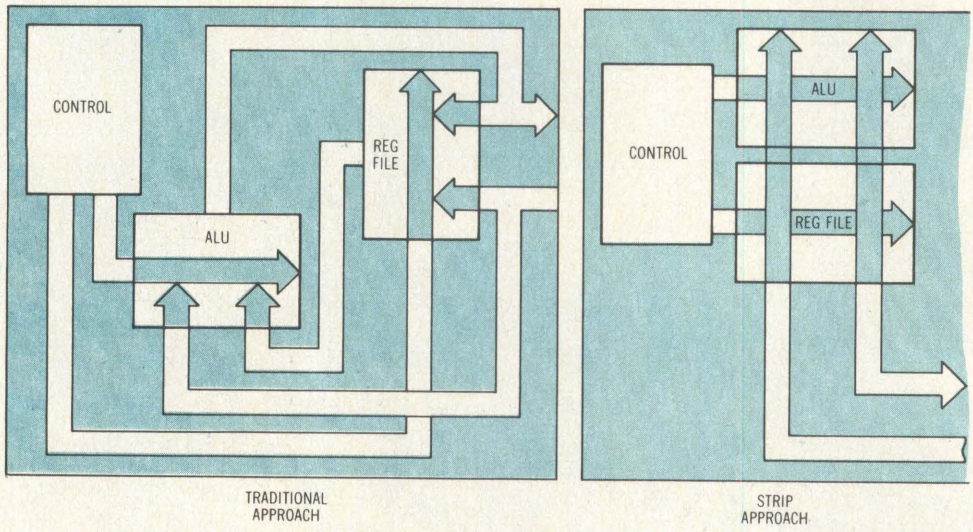


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*(continued on page 173)*

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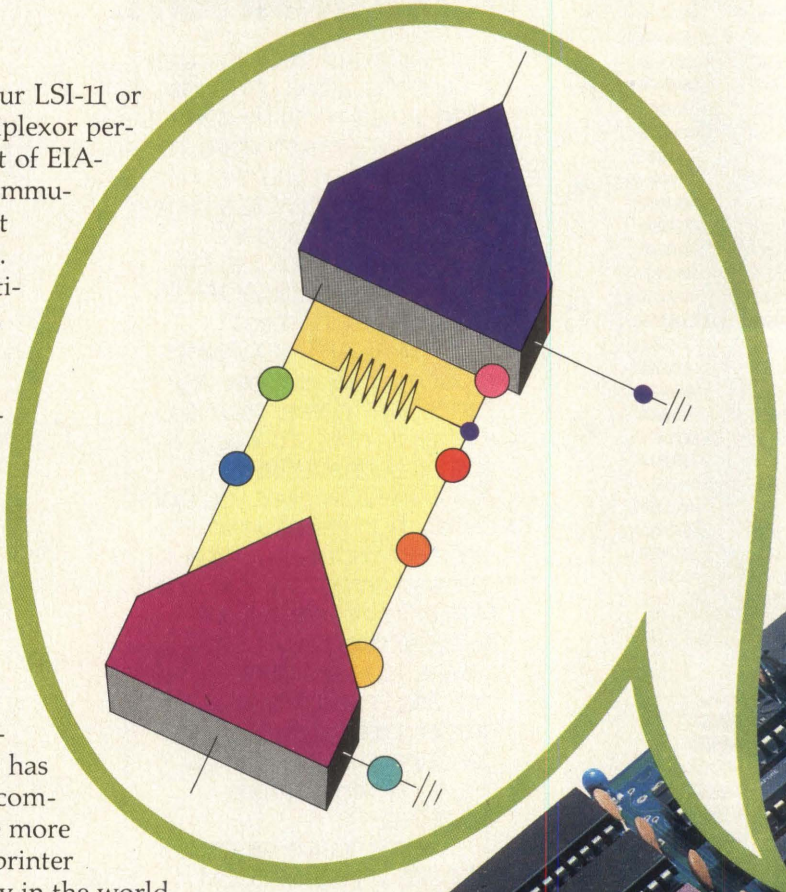

Now you can have it all for your LSI-11 or PDP*-11 system! Full DZ11 multiplexor performance with the added benefit of EIA-RS-422 long line capability—communicates at distances to 3000 feet (914.4m) at rates to 19.2K baud. What's more, MDB's DZ11 multiplexors let you combine RS-422 with EIA-RS-232 in any combination up to a total of eight lines on a single board. Or combine RS-232 with current loop in the same way. Eight and sixteen channel RS-232 DZ11 multiplexors are also available. No more doubling up on boards, distribution boxes, rack space or price. You see the results in your system's performance and cost.

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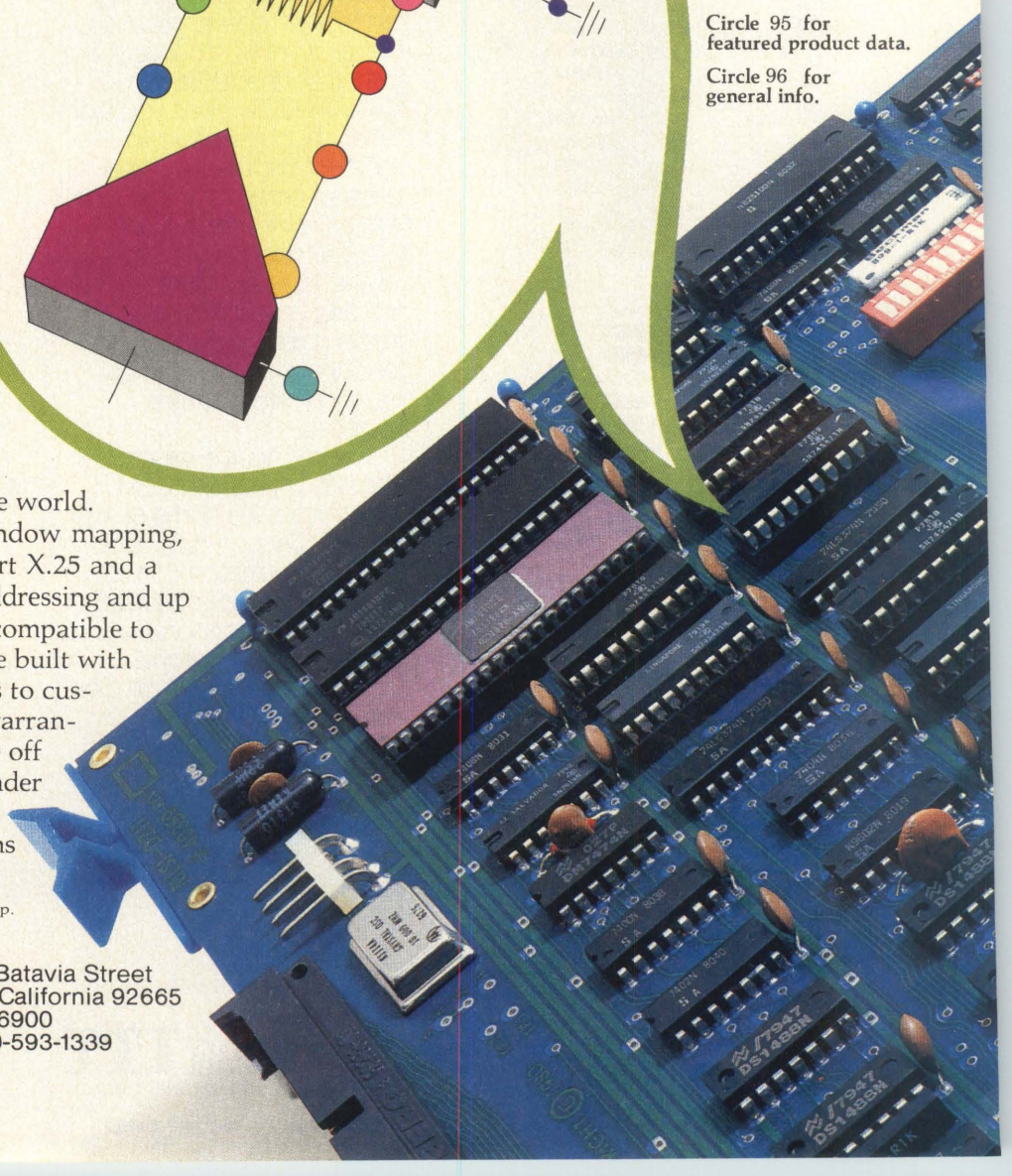
Circle 95 for featured product data.

Circle 96 for general info.



MDB SYSTEMS INC.

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addressing mode instructions, can manipulate onchip I/O ports and external peripheral device registers. This ability eliminates the need to use an accumulator as an intermediary. Specified bits can be set, cleared, and tested with single instructions.

Model TMS7000 is a "ROMless" version of the microcomputer chip; it contains a CPU, 128 bytes of RAM, and I/O onchip. TMS7020 provides CPU, 128 bytes of RAM, 2k bytes of ROM, and I/O onchip; the same features with 4k bytes of onchip RAM are provided by TMS7040. All three versions can be accessed up to 64k bytes of address space through memory expansion modes.

**Circle 460 on Inquiry Card**

## Logic modules offered for LSI-11 microcomputers

Two logic modules for Digital Equipment Corp's LSI-11 microcomputer family, the P03 parity controller and the BT03 bootstrap/terminator, are offered by Dataram Corp, Princeton Rd, Cranbury, NJ 08512. The parity controller provides parity error detection up to 2M words and operates with any LSI-11 compatible memory module that provides the necessary 18-bit word length. The dual-board bootstrap/terminator offers space for a 32 x 16-bit P/ROM array and provides bootstrap programs for a variety of LSI-11 peripheral controllers.

The control and status register (CSR) contained in the parity controller has a switch-selectable address range of 172100 to 172136. Contents of the CSR are displayed continuously on LED indicators mounted on the rear edge of the controller.

Compatible with the Q-bus protocol, the controller requires 5 V at 1.5 A and operates in systems with up to 4M bytes of memory storage. The unit measures 0.46 x 8.9 x 5.18" (1.17 x 22.6 x 13.16 cm) and fits into the LSI-11 chassis using one dual PCB slot. Operating temperature is 0 to 55 °C.

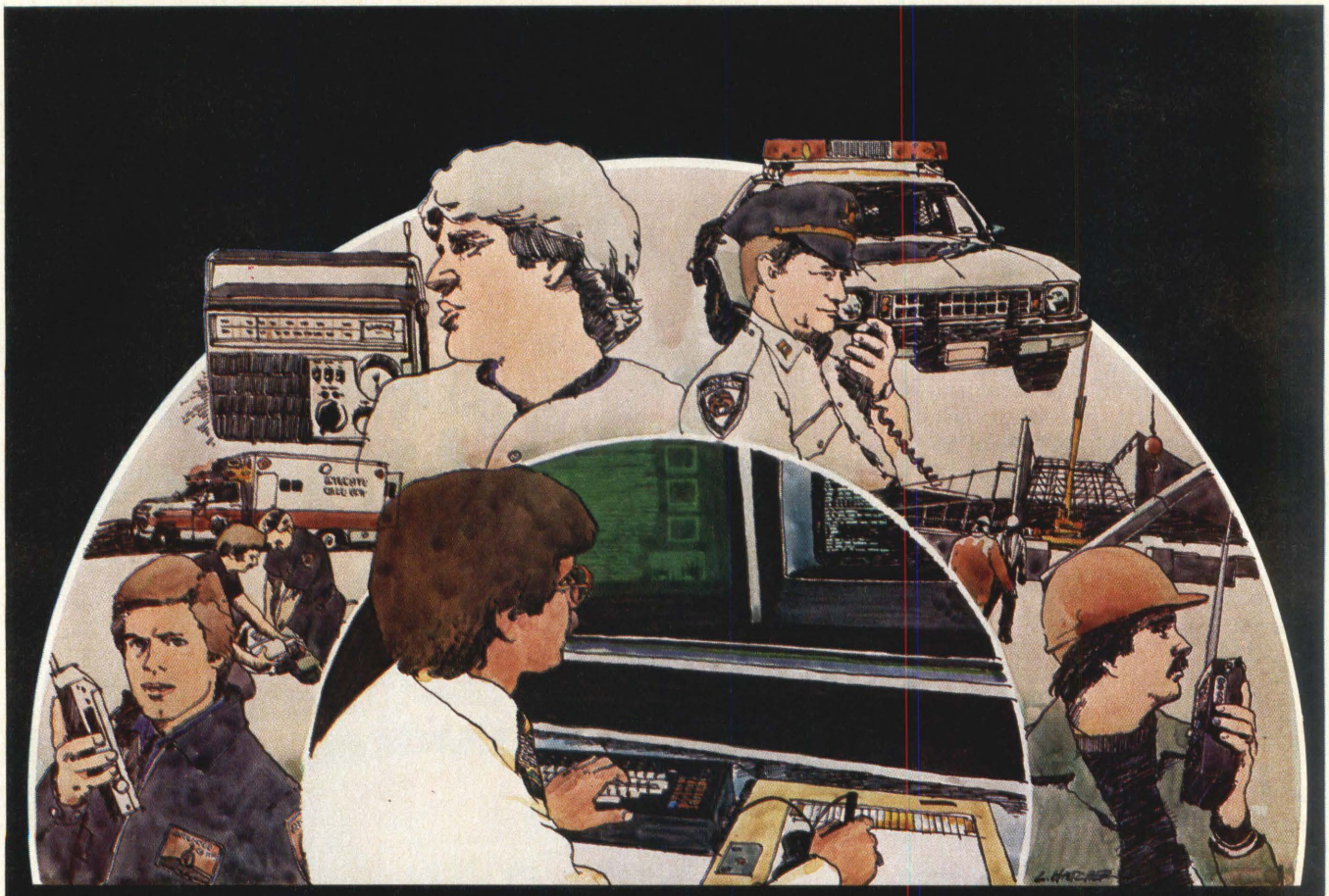
A dual board that provides space for a 32 x 16-bit P/ROM array, the bootstrap/terminator can be provided without P/ROMs to allow population with user designed P/ROMs. The unit is also offered with any one of five P/ROM sets designed to provide specific bootstrap routines.

The unit's P/ROM array can be located in one of two switch-selectable address ranges in the upper 4k-byte I/O address bank. Circuitry is provided that performs the same functions as the programmable line time circuitry on DEC's KPV11 clock module. LSI-11 bus terminators are optional. Power requirements are 5 V at 0.75 A with terminations.

Designed to fit into the LSI-11 backplane using one dual slot, the board measures 0.46 x 8.9 x 5.18" (1.17 x 22.6 x 13.16 cm) and weighs 5.6 oz (0.16 kg). It is compatible with DEC's RLV11 cartridge disc system, TU58 DECtape II cartridge tape system, TM11 compatible tape systems, RKV11 compatible cartridge disc systems, and the company's BC-212 Bulk Core and BS-212 Bulk Semi disc emulation systems.

**Circle 461 on Inquiry Card**

CIRCLE 136 ON INQUIRY CARD



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For information about Spectrum Control and EMC technology, write: Spectrum Control, Inc., 8061 Avonia Rd., Fairview, PA 16415. Call: 814-474-1571.

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*Making technology compatible with technology.*

## Single-board Winchester disc controller is Multibus compatible

MSC-9205 Multibus compatible single-board disc drive controller is based on the MSC 9000 series module that provides up to 75% of all the circuitry needed for 5.25 and 8″ (13.34- and 20-cm) Winchester disc drive controllers. Offered by Microcomputer Systems Corp, 432 Lakeside Dr, Sunnyvale, CA 94086, the controller uses a MOS microprocessor, ROM, and semicustom LSI circuitry to reduce the number of chips needed for a complete disc control system from approximately 200 to less than 25.

The controller supports 20-bit addressing, 8- or 16-bit DMA data transfer, DMA command transfer, and 8080 and 8086 compatibility. Features include alternate sectoring on each track, variable interleaving, 22-bit error detection and 11-bit error correction, data separation, automatic position verification, and automatic re-try. The 9000 series module includes control, data buffering, and error correction functions, while other circuitry on the host-resident single board provides host and disc interface functions.

**Circle 462 on Inquiry Card**

## Personal business computer offered in briefcase sized package

Osborne I, a personal computer for business professionals, is a totally integrated microcomputer system in a portable carrying case. Offered by Osborne Computer Corp, 26500 Corporate Ave, Hayward, CA 94545, the 64k Z80A based system performs a large number of straightforward tasks using industry standard operating systems and programming languages.

Standard hardware features include a 5″ (13-cm) monitor that provides a 52-character window on a 128-character line. The screen displays 24 rows implemented in 4k x 9-bit RAM. Upper- and lowercase characters with underlining, two screen intensities, and graphics capabilities are provided. IEEE-488 and RS-232-C interfaces, the Supercalc electronic calculator, and a standard typewriter keyboard plus numeric pad are included as well.

Two single-density, single-sided floppy disc drives provide approximately 100k bytes of storage each. Of the 64k bytes of RAM, 4k bytes are used by the screen, leaving 60k bytes available to the programmer. System software is held in ROM in a separate address space.

System software includes the CP/M® operating system and a CP/M compatible electronic worksheet. The system uses two BASIC programming languages: CBASIC and MBASIC. WordStar word processing system with MailMerge is provided as well.

Hardware options include double-density, double-sided floppy disc drives; a 9″ (23-cm) monitor that reproduces the 5″ (13-cm) display; a 12″ (30-cm) monitor providing an 80-column display; modem electronics; and an acoustic coupler. An optional battery pack provides three to five hours of operation away from an electrical outlet.

**Circle 463 on Inquiry Card**

## Emulator, analyzer aid 16-bit microcomputer system development

An emulator for the Zilog Z8000 microprocessor family, and Trigger Trace Analyzer supply added debugging capability for 16-bit microcomputer systems. The hardware/software integration tools, available from Tektronix, Inc, PO Box 500, Beaverton, OR 97077, provide full-speed, completely transparent eumulation of Z8001A and Z8002A chips and advanced logic analysis for 16-bit microprocessors, respectively.

The Trigger Trace Analyzer (TTA) has four channels, each with a 16-bit counter, that can count triggers, time, or provide delays. Channels are composed of identical word recognizers that will trigger on address, data, and control signal information, or combinations of these. Four external triggers tie in other design tools such as logic analyzers and oscilloscopes. Eight external probe inputs and one BNC input are available to the word recognizers. Triggering capabilities for address and data comparators include "equal to," "not equal to," "don't care," "ranging," and "range exclusion." The external probe input comparator provides "equal to" and "don't care" triggering, while the control signal comparator has "equal to" capability.

For realtime tracing, the TTA has a 255-word x 62-signal acquisition trace memory that samples address, data, external probe, and control line information from the emulator. The trace memory accepts up to 24 address signals, up to 16 data signals, up to 14 emulator dependent signals, and 8 external probe signals. The TTA has 8-MHz (125-ns) bus cycle resolution for word recognizers and acquisition trace memory. Maximum clock rate for counting or timing is 5 MHz.

Features include the ability to qualify storage in the acquisition trace memory, a microcomputer specific user interface for 16-bit emulators, definition of an additional breakpoint for the emulator by each trigger, consecutive event detection, and sequential triggering detection. The TTA is compatible with both the 8550 single-user microcomputer development lab (see *Computer Design,* Jan 81, p 159) and the 8540 integration unit scheduled for introduction later this year.

The Z8000 emulator, with Z8001A and Z8002A probes, offers full-speed, completely transparent emulation of both chips at up to 6 MHz, with no wait states. The full 48M-byte addressing range (6 address spaces of 8M bytes each for the Z8001A and 6 address spaces of 64k bytes each for the Z8002A) is supported by the emulator. For debugging, two emulation breakpoints are contained in the emulator along with symbolic debug. The emulator can disassemble instructions in the segmented or nonsegmented mode and detect prototype clock failures.

Features include memory mapping and memory write protection, both with 4k-byte resolution; a low profile hybrid microprocessor probe; prototype I/O that is directly accessible from the terminal with read and write commands; qualified program tracing, and complete support of "refresh" and "busreq" while the emulator is not running. The emulator is compatible with the TTA. Intel 8086 and Motorola 68000 emulators will be avaialable later this year.

**Circle 464 on Inquiry Card**

# LSI-11 USERS

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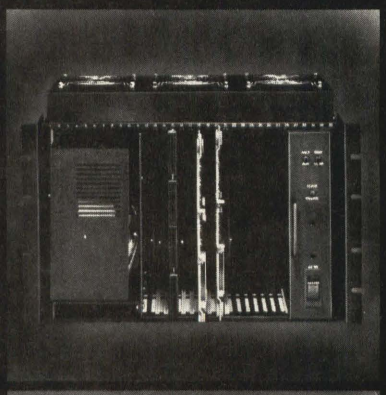

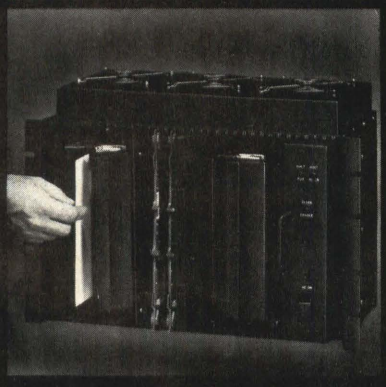

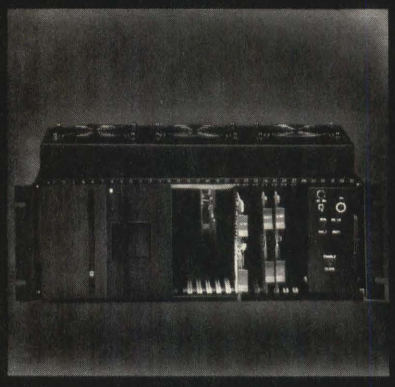

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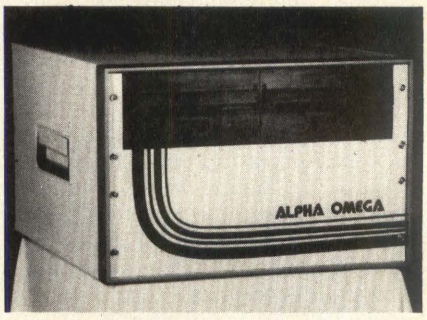
## Microcomputer system is designed for industrial process control




Industrial process control microcomputer system. Product of Alpha Omega Computer Systems, STD BUS Little Computer utilizes multiple processors dedicated to specific tasks and operating at optimum speed

A microcomputer system designed specifically for industrial process control applications, the Little Computer is available from Alpha Omega Computer Systems, Inc, 875 NW Grant Ave, Corvallis, OR 97330. Using the STD BUS, the system can utilize multiple processors, each dedicated to a specific task and operating at optimum speed.

Special application cards available for the system include a 4-MHz Z80 processor card, 64k-byte memory, disc controller, 4-channel serial I/O, 24-h clock card with onboard battery backup, 16-channel ADC and a 48-line parallel I/O card. A video display card, Winchester controller, and a DAC will be available in the future. The system can use up to four 8″ (20-cm) Shugart floppy disc drives for a total storage capacity of 1M characters.

The system is programmable in a variety of languages. Widely used operating systems can be added easily, allowing program development in high level languages such as BASIC, COBOL, FORTRAN, and C.

A typical system configuration includes two 0.25M-byte floppy disc drives, printer, console, 64k bytes of memory mapped RAM, and six empty card slots. These slots can be used to add additional serial I/O, parallel I/O, time of day battery backup clock, an additional disc controller, or an additional 64k bytes of memory.

**Circle 465 on Inquiry Card**

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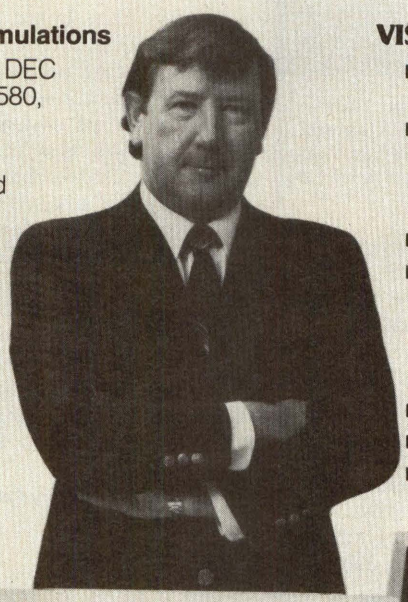

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**CIRCLE 99 ON INQUIRY CARD**

## Bit slice development system offers logic state analyzer capabilities

Bit slice development system. Advanced Micro Devices' AmSYS 29/10 features integrated logic analyzer and reduces debug time by emulating critical parts of target system

Complete hardware and software tools for the development of microprogrammed target systems are provided by the AmSYS29/10 development system from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. The system features an integrated logic analyzer and offers symbolic development of microcode, high speed control store emulator, target system clock control, and logic state monitoring.

During hardware and software integration, the system reduces debug time by emulating critical parts of the target system. A writable control store replaces control/store P/ROM with high speed RAM, and clock control logic adds breakpoint and single-step capability. A single-card microprogram sequencer is provided as an evaluation vehicle for microprogram familiarization and software module testing. When combined with the writable control store and clock control logic, the microprogram sequencer forms a complete microprogrammed controller for testing and debugging prototype hardware.

The system's AMDASM meta-assembler supports microcode development. The meta-assembler allows definition of a mnemonic instruction set for any microinstruction format.

Support is provided for an optional Am29/6310 high speed trace unit with logic state analyzer capabilities. This unit allows tracking of microinstructions and the many bus paths inside complex bit slice architecture. The high speed trace option performs real-time event and count measurements to 10 MHz on a 48-bit wide sample. Up to 256 time and data samples can be stored, and each sample can be expanded to 128 bits. Multiple 48-bit wide triggers provide event based controls. The eight triggers are general purpose and can be nested to qualify data for storage or add up to eight breakpoints to the clock control logic.

The system processor is composed of an 8-bit microprocessor board, 64k bytes of RAM, and a single/double-density floppy disc controller board. It provides an interface to a CRT console, supports microprogram development software, and directs the microprogrammed controller and high speed trace option. The board also contains four RS-232 serial ports and a parallel printer interface. All peripherals are optional.

A single Am96/1064 board containing 64k bytes of dynamic RAM and auto-refresh provides memory support. A separate chassis contains two 8″ (20-cm) floppy disc drives. The controller detects and matches the density of the IBM format compatible diskettes in each drive.

The microprogram support software package handles microprogram development and controls emulation and trace hardware. The package runs under the standard AMDOS29 disc operating system, along with an editor, an 8080/8085/Z80 relocatable macro assembler, and file handler.

**Circle 466 on Inquiry Card**

## Single-board controller interfaces Winchester discs to LSI-11 computers

SC02 single-board controller interfaces a variety of 8 and 14″ (20- and 36-cm), small to medium capacity hard disc drives with Digital Equipment Corp's LSI-11 computers. The controller, offered by Emulex Corp, 2001 E Deere Ave, Santa Clara, CA 92705, uses the standard SMD interface and supports one or two disc drives.

Features include two selectable bus register start locations, selectable bus addressing, two selectable vector addresses, and a 32-bit error correcting code provision. An edge-mounted LED provides activity, error, and status display under microprogram control. Onboard slide switches allow selection of program controlled operating and configuration options. Sockets are supplied for installing bus terminator resistors plus P/ROM chips for execution up to a 512-word bootstrap program. Also included onboard is a BDV-11 compatible, software controllable line time clock. All control functions reside in one quad-size PCB that occupies a single Q-bus slot on the LSI-11.

Two models emulate specific DEC subsystems. SC02/A emulates the RP11E controller combined with multiple RP02 and RP03 disc drives to support all types of drives having capacities from 8M to 160M bytes. The SC02/C emulates the RK611 controller combined with multiple RK06 and RK07 drives to support cartridge module drives that have both fixed and removable media and capacities from 16M to 96M bytes, plus other drives for which the RK06/07 provides a convenient capacity.

**Circle 467 on Inquiry Card**

## Power supply offered for microprocessor based systems in Europe

Microprocessor based systems aimed at international markets can be powered with the XL200-3501 200-W open frame switching power supply from Boschert, Inc, 384 Santa Trinita Ave, Sunnyvale, CA 94086. The supply complies with Verband Deutscher Elektronika (VDE) requirements, providing a general purpose power supply for small business computers and other microprocessor based systems in Europe.

The supply has jumper selectable input voltage ranges of 95 to 130 Vac and 190 to 265 Vac, at frequencies from 47 to 440 Hz. It supplies up to 200 W of total power on four outputs. The 5-V primary output delivers 5 to 25 A at total regulation within ±1% and combined noise and ripple within ±2%. Standard −5-, 12-, and −12-V auxiliary outputs each provide 0.5 to 4 A with total regulation of ±9% and combined noise and ripple of ±2%.

Minimum output voltage time is 16 ms at maximum load and nominal input voltage. Protective features include short circuit protection, overvoltage protection, and power foldback. Overtemperature protection is offered by a thermal switch, and power fail detection is optional.

Operating temperature range is 0 to 50 °C without forced air cooling, and 0 to 70 °C with forced air cooling. The supply measures 15 x 6.0 x 2.75″ (38 x 15.2 x 7.0 cm), and weighs 4 lb (1.82 kg). It has been improved under VDE 0730 safety and is designed to meet VDE 0871 electrical noise specifications.

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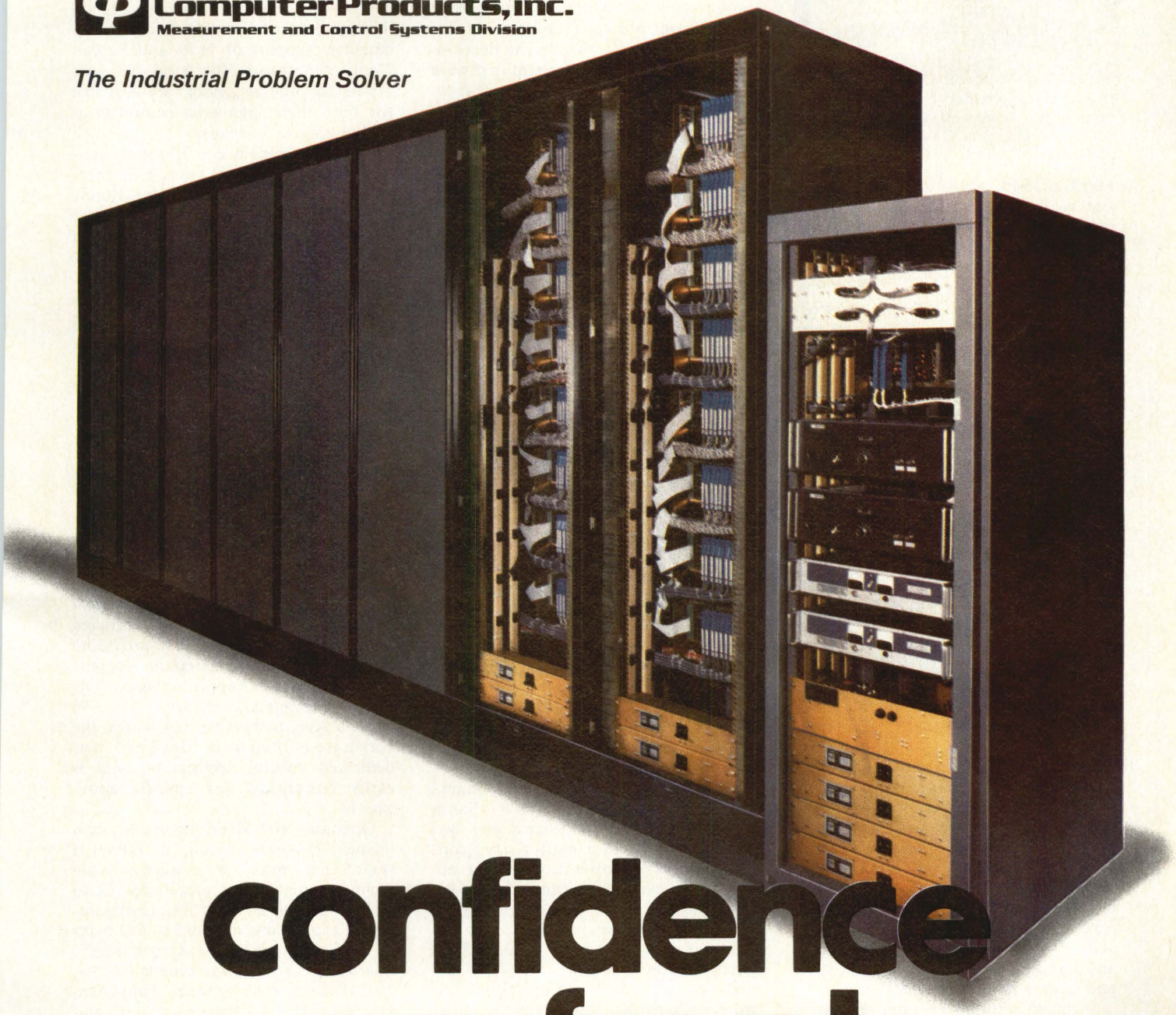


# confidence up front

## Computer system combines UCSD Pascal and Q-bus

16-bit, stack oriented computer system. Offered by Advanced Digital Products, PDQ-3 incorporates Q-bus and executes UCSD Pascal Version III.0 P-code

PDQ-3, a 16-bit stack oriented computer system from Advanced Digital Products, 7584 Trade St, San Diego, CA 92121, features direct execution of UCSD Pascal Version III.0 P-code. UCSD Pascal offers a high degree of software portability and reduced software development and maintenance. The system also incorporates the Q-bus, permitting the addition of a variety of peripherals.

A realtime clock interval timer, multiplexed CRT and serial printer interface, DMA floppy disc controller, and bootstrap loader from floppy or hard disc are features of the CPU module. The module is contained on a 8.5 x 10″ (21.6 x 25-cm) multilayer printed circuit board.

**Circle 469 on Inquiry Card**

## Universal development station supports over 40 microprocessors

Phoenix 3 universal microprocessor development station stores 2.5M bytes of program and data and supports high productivity software development for more than 40 microprocessors. The system, from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051, supports 6800, 9900, 8080A, Z80, 802X, 803X, and 804X families, 6502, 1802, and 2650 microprocessors, 68000, Z8000, and 8086; and the company's S2000, S2200, and S2300 families.

Included in the system are a microprocessor based computer, 64k-byte RAM, 12″ (30-cm) CRT, full ASCII keyboard and keypad, a 5.25″ (13.34-cm) disc drive, two double-sided, double-density 8″ (20-cm) drives (total of 2.5M bytes), and three RS-232-C interfaces. The Pascal based AMIX executive operating system supplies screen editor (EDWARD), utilities, and assemblers for the S2000, S2200, 6800, and 9900 microprocessors. The same editor is used for every supported microprocessor, increasing programmer productivity by reducing learning time for different projects. EDWARD includes cues and prompts to prevent development errors and inadvertent software destruction, and to allow recovery from errors.

Hardware options include Ariel, an RS-232-C compatible universal EPROM programmer/ROM simulator, and Delphi, a universal in-circuit emulation module that supports the S6800, S6802, 6801, 6809, Z80, 8021, 8048, 8080, 8085, and 8041 microprocessors. Most RS-232-C compatible printers can also be used with the system.

**Circle 470 on Inquiry Card**

## Development system offers high level language support, added memory

A microprocessor based development system for system designers using high level languages and requiring the support of future 16-bit processors, Starplex II offers both hardware and software support for a variety of microprocessor products. With additional RAM and high level language support, the system gives users three times the performance of the Starplex I disc oriented development system (see *Computer Design,* Sept 78, p 150).

Available from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, the system uses two Z80A processors in a master/slave configuration. The master processor has access to 64k bytes of RAM and controls the operating system. The slave processor, which controls user programs, also has 64k bytes of RAM, for a total of 128k bytes of system RAM.

A spooled printer allows the user to print while simultaneously editing, compiling, assembling, or performing any other development system work. The programmed function keyboard has eight uppercase and eight lowercase function keys that can be programmed to provide access to a total of 16 functions usable in a command system mode or by an application program running on the system. A system resident debugger does not occupy any user space in memory and can be called up at any time during program execution.

FORTRAN and BASIC can be used on the system with optional high level language support of PL/M and Pascal. Code generators for 8080/8085 and Z80/NSC800 8-bit processors are available for both these high level compilers as well as a CP/M interface.

A typical system configuration consists of two Z80A based CPUs; 128k bytes of RAM; 1M byte of 8″ (20-cm) floppy disc storage (two drives); video monitor and keyboard; and the disc based operating system with debugger, text editor, assembler, and linker. FORTRAN, BASIC, utilities and diagnostics, and the universal programmer interface for P/ROMs and PLAs are included as well.

**Circle 471 on Inquiry Card**

## Single-board computer provides support logic and power supply onboard

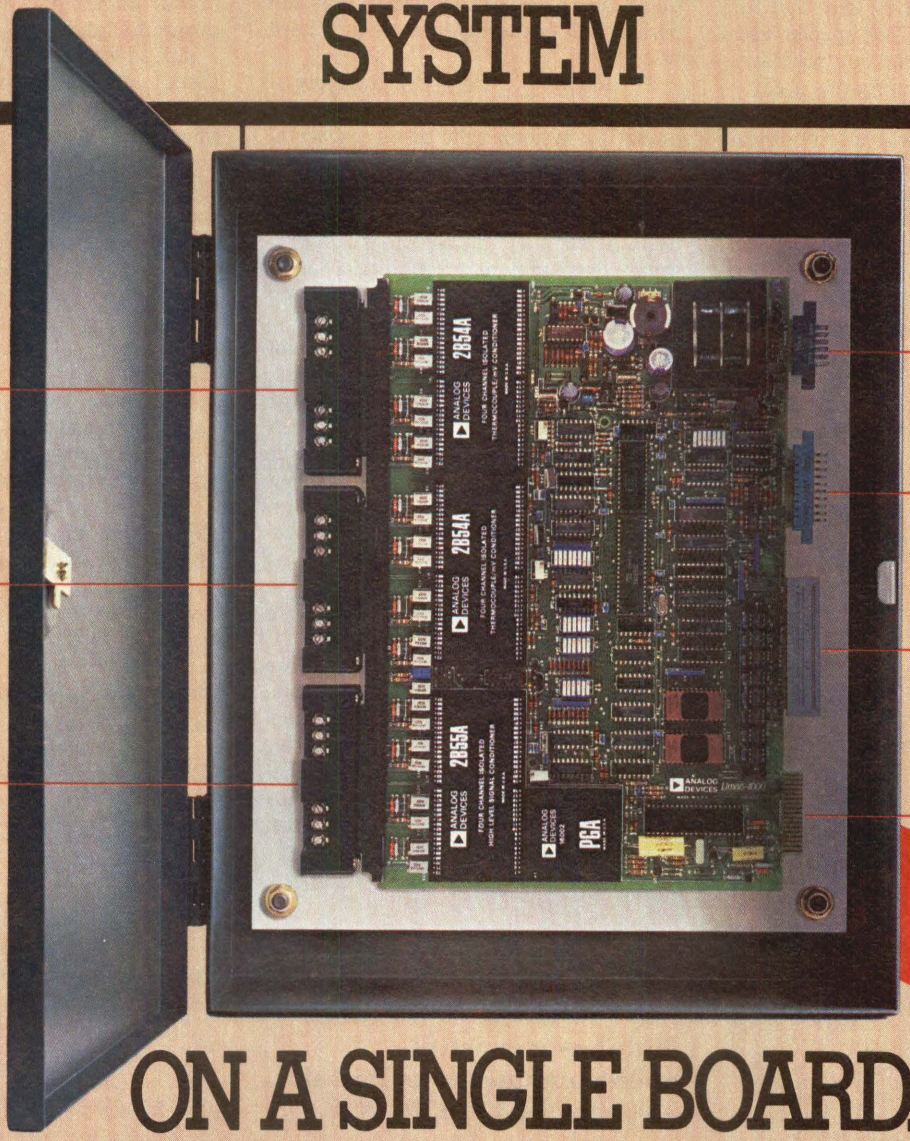
CPU-1 single-board computer allows designers to concentrate on their overall application, rather than on detailed microcomputer design, by providing basic microcomputer circuitry, support logic, and power supply onboard. Offered by Pragmatic Designs, Inc, 950 Benicia Ave, Sunnyvale, CA 94086, the 8085-based board is designed for dedicated control applications and is easily customized for specific applications.

Operating at 3 MHz, the basic system includes 256 bytes of RAM, 22 I/O lines, a serial I/O port, a programmable counter/timer, and 2 sockets for 1k to 4k bytes of EPROM. This basic configuration is expandable onboard to 512 bytes of RAM, 44 I/O lines, and 2 clock timers. EPROM type is jumper selectable for 2708, 2716, 2758, or TMS 2716 EPROMs. The system also provides both power-on reset and manual reset buttons, and supports the 8085 vectored interrupt structure.

System power supply rectifiers, filters, and regulators are on the PC board; only

*(continued on page 182)*

# THE FIRST COMPLETE SENSOR-BASED MEASUREMENT AND CONTROL SYSTEM

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μMAC-4000 is a fully integrated, pre-calibrated, intelligent system, complete with sensor signal conditioning, multiplexing, A/D conversion, digital I/O and serial communications to any host computer. Its on-board microcomputer unburdens the host CPU by performing sensor linearization, scaling and conversion to engineering units, and limit checking.

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ANALOG DEVICES

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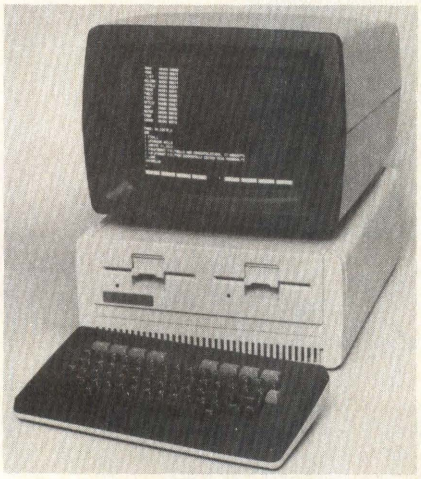
an external transformer is required to complete a single-board system. A special PC board area is laid out for wirewrapping or soldering special user functions. System I/O and control traces are bused to pads adjoining this area.

Application programs for the system can be developed using any 8080/8085 development system. The board also works with the company's DBM-I debug memory card. A connector and logic to utilize the memory card's hardware trap facility are provided and a trap LED shows the trap latch state during debugging. Programs for the target application can be developed using a larger host computer. When development is complete, the EPROMs can be programmed and installed in the computer for normal system operation.

**Circle 472 on Inquiry Card**

## Realtime microcomputer system provides software power of minicomputer system



Realtime computer system. Desktop HP 1000 model 5, from Hewlett-Packard Co, includes HP 1000 L-series microcomputer, dual-disc drives, CRT, and keyboard

Model 5 combines the HP 1000 L series microcomputer (see *Computer Design*, Dec 80, p 142) with dual 270k-byte minifloppy disc drives, CRT, and keyboard in a desktop package for hardware OEMs and software houses developing systems around a small computer. Offered by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, the system offers the software power of a minicomputer, plus a variety of I/O interfaces and peripherals including printers and hard discs.

The microsystem supports a variety of HP 1000 software, including two realtime operating systems: the RTE-L excecute-only system for up to 64k bytes of memory, and the RTE-XL expanded memory operating system for up to 512k bytes of memory that provides full program development capabilities. Both operating systems are multi-user and multitasking.

Languages available on the system include HP Pascal, FORTRAN, ASSEMBLER, or BASIC. Optional software includes the company's Distributed Systems Network (DSN) software for linking the microsystem in a local or global computer network and IMAGE/1000 for database management. For applications requiring graphics, the system supports graphics peripherals and GRAPHICS/1000-II, the company's graphics software with 3-dimensional capabilities.

Three integrated terminal tops are offered for the system: the 2621A low cost terminal, the 2624 block mode terminal with user definable soft keys and forms generating set, and the 2626A multiple-workspace, split screen terminal. A built-in thermal printer can be specified for all three terminals.

**Circle 473 on Inquiry Card**

## Multibus compatible microcomputer runs Pascal, ANSI standard FORTRAN 77

A Multibus compatible microcomputer, CTS-300 processes full ANSI standard FORTRAN 77 and Pascal software under its UNIX-like MERLIN operating system to allow programs written for large computers to be run without change. Offered by Codata Systems Corp, 285 N Wolfe Rd, Sunnyvale, CA 94086, the microcomputer can also be used to write programs for large system use.

An M68000 CPU, 256k bytes of high speed cache memory, and intelligent high speed control devices are provided on one Multibus card. Approaching large mainframe operating speeds, the CPU operates at 8 MHz, without wait states. Compiler speeds of up to 7000 lines/min are possible.

The system directly addresses up to 1.5M bytes of memory without segmentation. Since the CPU and software impose no addressing restrictions, the microcomputer can run programs up to 1.5M bytes in length. Differentiation between code and data is dynamic and optional, therefore there is no limit on a FORTRAN array size or Pascal procedure.

Included in the system are built-in floppy and Winchester disc drives, CRT, and an independent keyboard. A screen oriented editor and a 68000 assembler and linker that allow Pascal and FORTRAN to be linked to assembly language are also included.

**Circle 474 on Inquiry Card**

## Memory expansion system increases RAM capacity, speeds disc transfers

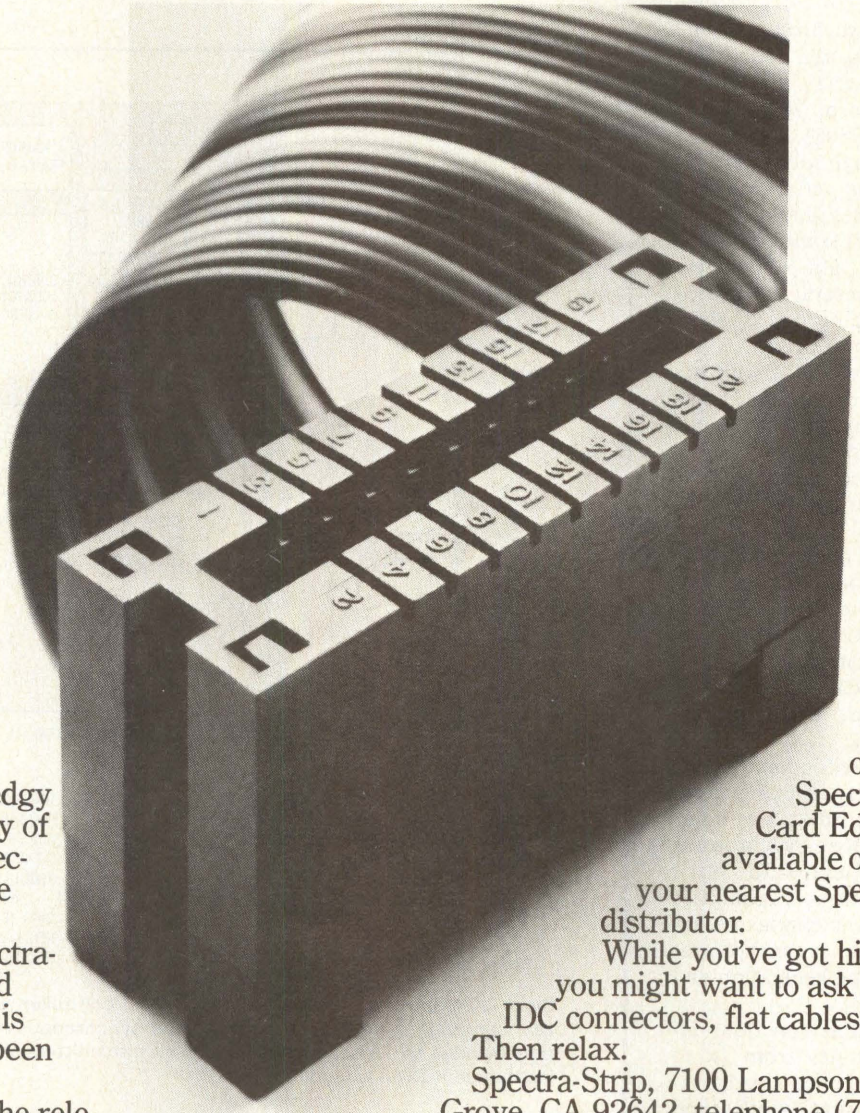
Axlon 256 increases storage capacity of the Atari 800 computer from 48k bytes of RAM to 256k bytes. Offered by Axlon Inc, 170 N Wolfe Rd, Sunnyvale, CA 94086, the memory expansion system is plug compatible with the computer and includes all interface hardware. No modifications are required.

A modified DOS is included; the system is loaded from the disc and is ready to run. Disc transfer time is increased from 756 bytes/s to 128,000 bytes/s. Designed as an extension of the Atari bus structure, the system allows 80-col card units or hard disc controllers to interface with the computer.

Two 32k-byte RAMCRAM modules are provided with the system. Additional modules can be added until the full 256k-byte capacity is achieved. Atari RAM modules can be added as well.

**Circle 475 on Inquiry Card**

# Advantedge



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## Multiprotocol serial controller supports three communication protocols

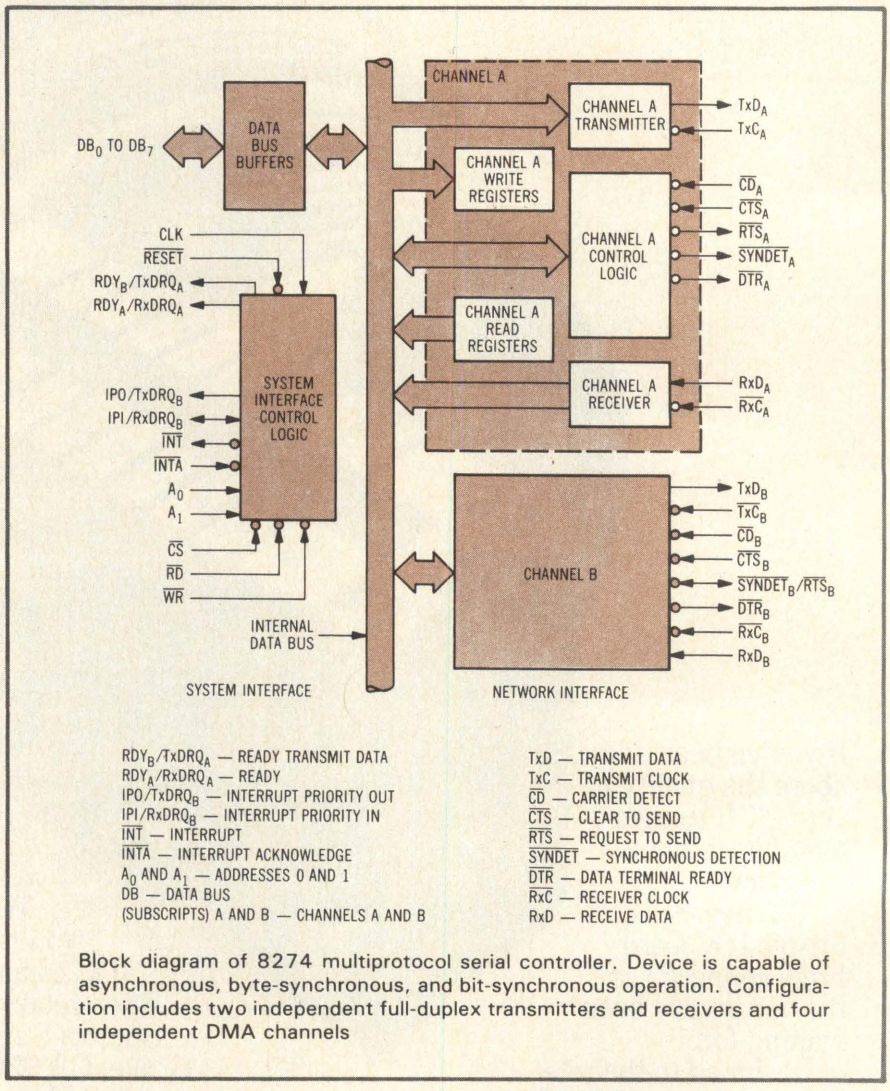
Supporting asynchronous, byte-synchronous, and bit-synchronous communications techniques, the 880k-baud 8274 multiprotocol serial controller (MPSC), from Intel Corp, 2625 Walsh Ave, Santa Clara, CA 95051, is designed for multiple protocol high speed applications. Two independent serial receiver/transmitter channels are implemented. Designed to be compatible with the company's MCS-85, iAPX-86, and -88 families, the device supports several microprocessor interfaces including polled, wait, interrupt driven, and DMA driven. A full 1M-baud data rate is available with the 8274-2. Manufactured using the company's HMOS technology, the MPSC is implemented in a 40-pin package.

Asynchronous protocols can be programmed for 5- to 8-bit characters; odd, even, or no parity; and 1, 1.5, or 2 stop bits, with the detection of framing, overrun, and parity errors. In the bit-synchronous mode, the device is compatible with IBM's SDLC and the International Standards Organization's HDLC protocols. Features include flag generation and recognition, 8-bit address recognition, automatic zero-bit insertion, automatic cyclic redundancy check (CRC) generation and checking, and compatibility with the CCITT X.25 international standard. Byte-synchronous operation is compatible with IBM's Bisync. Byte-synchronous capabilities include 1- or 2-byte sync characters, internal or external character synchronization, and automatic CRC generation and checking.

General programmable functions include clock-rate multiples from 1x to 64x, combinations of polled, ready, interrupt, and DMA handshake modes, and assignments of four DMA handshake channels to the two transmitters and two receivers. For multichannel applications, several MPSCs can be connected in an interrupt daisy chain, with priorities determined by position in the chain. Priorities can also be dynamically controlled with standard priority controllers.

The MPSC to microprocessor system interface can be configured in several ways. Basic interface types are polled, wait, interrupt driven, or direct memory access driven. Polled operation is accomplished by repetitively reading the status of the MPSC, and making decisions based on that status. The MPSC can be polled at any time. Wait operation allows slightly faster data throughput for the MPSC by manipulating the ready input to the microprocessor. Block read or write operations to the MPSC are started by the microprocessor. The MPSC deactivates its RDY signal if it is not ready to transmit the new byte, or if reception of a new byte is not completed.

Interrupt driven operation is accomplished via an internal or external interrupt controller. When the MPSC requires service, it sends an interrupt request signal to the microprocessor, which responds with an interrupt acknowledge signal. Upon receiving the acknowledge, the internal or external interrupt controller vectors the microprocessor to a service routine in which the transaction occurs. DMA operation is accomplished with an external DMA controller. When the MPSC needs a data transfer, it requests a DMA cycle from the DMA controller. The DMA controller then takes control of the bus and simultaneously does a read from the MPSC and a write to memory or vice versa.




Block diagram of 8274 multiprotocol serial controller. Device is capable of asynchronous, byte-synchronous, and bit-synchronous operation. Configuration includes two independent full-duplex transmitters and receivers and four independent DMA channels

**Circle 440 on Inquiry Card**

# CARTS & CRAFTS

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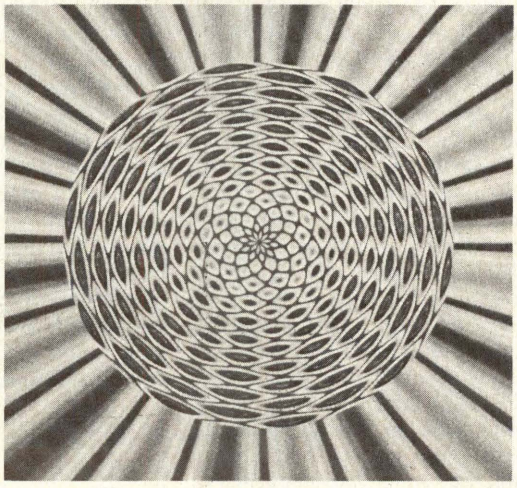
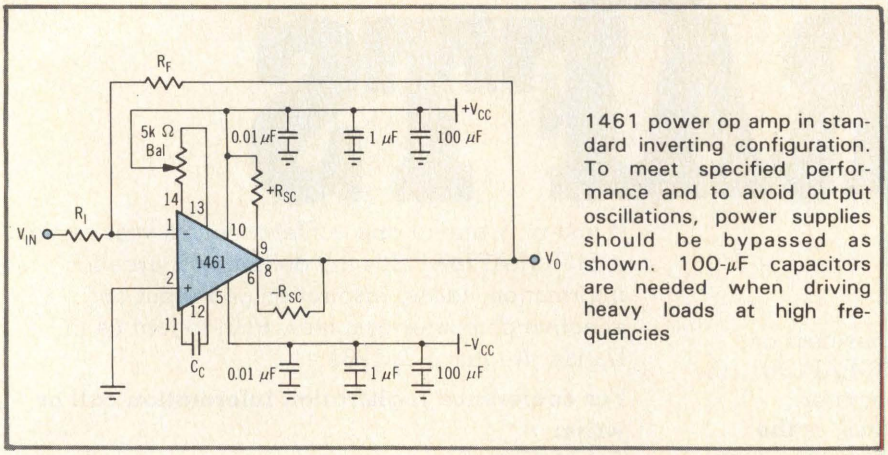


Computer graphic by M. Thompson, M. Schecter

# SIGGRAPH/81

CIRCLE 103 ON INQUIRY CARD

## Power op amp implemented with VMOS output stage




1461 power op amp in standard inverting configuration. To meet specified performance and to avoid output oscillations, power supplies should be bypassed as shown. 100-μF capacitors are needed when driving heavy loads at high frequencies

Claimed to be the first power op amp with V-groove power MOSFETs in the output stage, the recently announced 1461 is a high speed, high power, FET-input, VMOS device. The FET input limits typical bias currents to ±10 pA. A bipolar gain stage provides a minimum 100 dB of open loop gain. Manufactured by Teledyne Philbrick, Allied Drive at Rte 128, Dedham, MA 02026, the device operates from ±15- to ±45-V supplies and has output voltages up to ±30 V and output currents up to ±600 mA. The VMOS output stage eliminates the safe operating area restrictions and secondary breakdown problems that typically plague power op amps. The ability to handle high output currents at any voltage eliminates the normally intricate problems caused by driving capacitive or inductive loads. Thermal runaway is not exhibited. Performance characteristics include 100-dB open loop gain, 1-GHz gain-bandwidth product, and 1200-V/μs slew rate.

Packaged in a 14-pin DIP, the device has "ears" for easy mounting on heat sinks. Compensation is accomplished with a single external capacitor. Two external resistors are optional for current limiting. The standard part is specified for 0 to 70 °C operation. For high reliability military/aerospace applications, it is available specified for −55 to 125 °C operation with MIL-STD-883 screening.

Three external add-ons, a compensation capacitor, and two optional current limiting resistors make the device a versatile amplifier. With the proper compensation capacitor, a 15-MHz bandwidth up to closed loop gains of 50 can be maintained. Output current is internally limited to approximately ±750 mA. Users may select two external resistors to further limit maximum positive and negative current excursions; the only limitation on the output is imposed by a maximum allowable junction temperature of 150 °C.

Applications for the part are seen in video yoke drivers and distribution amplifiers, high speed ATE pin drivers, high accuracy audio amplification, and the driving of inductive and capacitive loads. The device is shown in a standard inverting amplifier configuration in the Figure. This configuration includes a compensation capacitor, current limiting resistors, and an offset adjusting potentiometer.

**Circle 441 on Inquiry Card**

## Performance of programmable array logic circuits improved

Recent PAL® series 20 programmable array logic circuits are faster and require less power than previous models. The propagation delay and setup time of the PAL16L8, PAL16R8, PAL16R6, and PAL16R4 have been reduced from 40 to 35 ns. Registered circuits for performing sequential functions, the supply current of these "medium" devices has also been lowered from 225 to 180 mA.

The speed of smaller PALs, designed to perform combinational functions, has also been improved. The delay and setup time has also been reduced from 40 to 35 ns without a change in current requirements. These devices include the PAL10H8, PAL12H8, PAL14H4, PAL16H2, PAL10L8, PAL12L6, PAL14L4, and PAL16L2. The PAL16C1 continues to operate at 40 ns. These improvements in power and speed apply to 20-pin commercial versions. Improved specifications for military versions are expected the second half of 1981. All devices come in 30-mil (0.76-mm) SKINNYDIP™ packages.

Manufactured by Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, the devices use an advanced Schottky TTL process and bipolar P/ROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flipflops with a reduction in chip count. The fusible links are blown to configure AND and OR gates. Complex interconnections that previously required time-consuming layout are "lifted" from PC board etch and placed on silicon where they can be modified during prototype checkout or production.

The family is programmed on conventional P/ROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to give the user a proprietary circuit that is difficult to copy.

**Circle 442 on Inquiry Card**

## Op amp eliminates crossover distortion

LH0101, a power operational amplifier, outputs up to 5 A. Voltage range is ±20 V at 10 V/μs. Full power bandwidth is 300 kHz with 40-W output. Gain bandwidth product is 5 MHz. These characteristics make the part well suited for use in servo applications such as disc head position controls and gyroscopic platform controls, where high speeds and high power are essential. The op amp is manufactured by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051.

*(continued on page 188)*

# Single vendor graphics support...

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SYSTEMS Graphics Support Platform provides you with three key elements —graphics support software featuring Template ™, CONCEPT/32 minicomputers and support for a wide range of graphics devices. Our single vendor graphics support is the best approach to meet your computer graphics requirements.

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1981

CIRCLE 104 ON INQUIRY CARD

Crossover distortion has been eliminated through a new circuit technique that alters commutation of the output current from the source transistors to the sinking transistors. This is accomplished by a separate output circuit that controls the transition region and eliminates the heavy quiescent currents normally associated with Class AB output stages. The result is a total harmonic distortion of 0.008%, and an undetectable crossover distortion.

Power DACs built with conventional op amps have difficulty attempting to force a zero output voltage. The crossover results in a deadband, which causes the output impedance to rise and the gain to drop. With the LH0101, output impedance is maintained below 1 Ω when there is no load. Inductive and capacitive loads can also be handled.

Thermal feedback can also cause problems in conventional power op amps. For example, at dc the temperature gradients caused by changing conditions in the output devices can shift the input offset to reduce, increase, or even invert the effective gain. With this device the specified 150 μV/W is due entirely to temperature rise and is not dependent on the output state. Both the common mode rejection and the power supply rejection of the device are 100 dB, and dc gain is a minimum of 50,000.

It comes in an 8-pin, TO-3 package and is available from stock in four grades, including prime and standard electricals, and commercial and military temperature ranges. 883B versions are available.

## Programmable quad and low noise op amps announced

Two operational amplifiers were recently announced by Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040. RC4149 is a programmable quad op amp. RC/RM5532 is a high performance dual low noise op amp. With programmable ac and dc characteristics, 4149 consists of four high-gain, compensated, low power amplifiers. 5532 is claimed to provide better noise performance and output drive capability and higher small-signal and power bandwidths than standard dual op amps.

A single external resistor selection on 4149 allows the user to program the supply current, slew rate, gain bandwidth product, and input noise of three amplifiers. With another resistor selection, the user can independently adjust the ac and dc characteristics of the fourth amplifier.

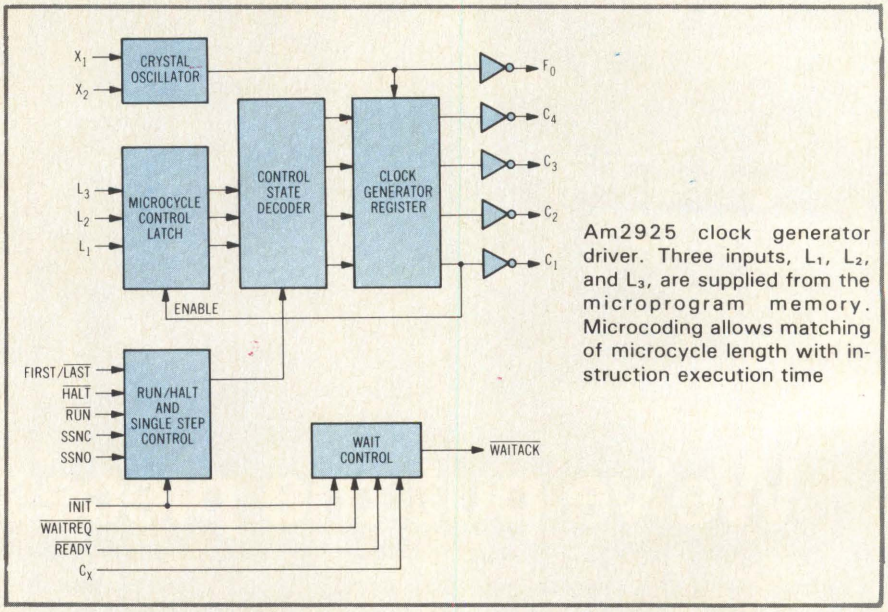
4149-2 allows the user to independently adjust the ac and dc characteristics of the dual amplifiers with two resistor selections. This results in two different ac and dc characteristics in a single package. 4149-3 is for applications that require identical ac and dc characteristics from all four amplifiers. The user can program the current for all four amplifiers from pin 8. This leaves pin 9 available to adjust op amp "C" to zero offset with the addition of a variable resistor.

5532 has a wide supply voltage range of ±3 to ±20 V, a power bandwidth of 140 kHz, a small-signal bandwidth of 10 MHz and a slew rate of 8 V/μs. It is especially suited for such applications as high quality audio equipment, instrumentation, control circuits, and telecommunication channel amplifiers. It is internally compensated for gains of one or more.

Except for the two programming pins, 4149 has the same pinout as most of the popular quad op amps, and is a plug-in replacement for the 146 series. 5532 is available in either plastic or ceramic dual inline packages or a TO-99 metal can.

**Circle 443 on Inquiry Card**

## General purpose clock generator/driver




Am2925 clock generator driver. Three inputs, $L_1$, $L_2$, and $L_3$, are supplied from the microprogram memory. Microcoding allows matching of microcycle length with instruction execution time

Am2925 is a single-chip, general purpose clock generator and microcycle length controller. The microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length and generates four different clock output waveforms. Since the machine cycle is no longer determined by the slowest instruction, microcycle length control allows the designer to improve system throughput. By selecting the appropriate clock length, each microcycle can be tailored to the instruction time required. Am2900 based designs can be made as much as 30% faster by replacing present fixed microcycle clocks with the recently announced part from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. The device is packaged in a 0.3" (7.6-mm) 24-pin DIP.

A block diagram of the device is shown in the Figure. A crystal-controlled onchip oscillator can be driven at frequencies up to 32 MHz, providing a 32-ns oscillator period. A buffered oscillator output is also provided. The device decodes three inputs, $L_1$, $L_2$ and $L_3$, latched into the microcycle control latch, to determine a microcycle length of 3 to 10 oscillator periods. These inputs are normally supplied from

*(continued on page 191)*

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**Nominal Capacity @ 68°F:**

| | | |
|---|---|---|
| 20 | Hour Rate ( .28 ampere to 5.25 volts) | 5.5 ampere hours |
| 10 | Hour Rate ( .53 ampere to 5.10 volts) | 5.3 ampere hours |
| 5 | Hour Rate ( .96 ampere to 4.95 volts) | 4.8 ampere hours |
| 1½ | Hour Rate (2.80 ampere to 5.25 volts) | 4.2 ampere hours |
| 1 | Hour Rate (3.50 ampere to 4.50 volts) | 3.5 ampere hours |

**Physical Size (± .05 inches):**

| | |
|---|---|
| Length | 6.00 inches |
| Width | 1.34 inches |
| Height | 3.70 inches |
| Height (including terminals) | 3.90 inches |
| Volume (excluding terminals) | 29.7 cubic inches |
| Weight | 2.7 pounds |

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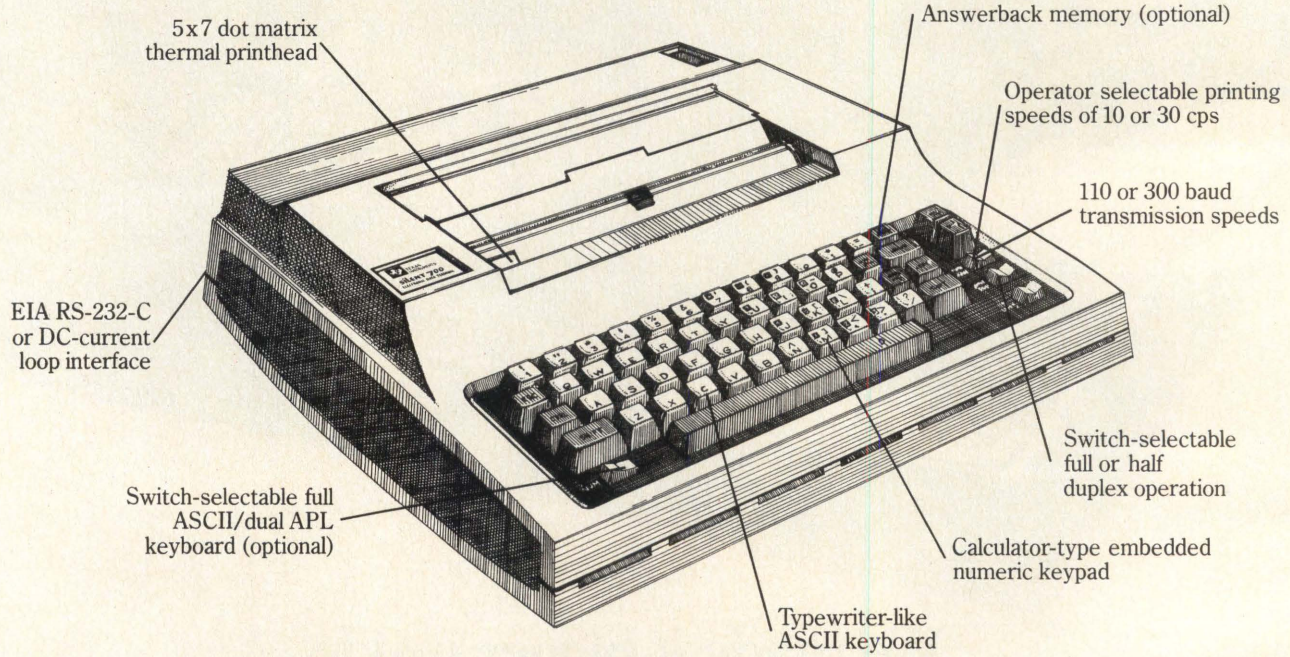
CIRCLE 105 ON INQUIRY CARD

# The Silent Commander.

## 743 KSR

### Keyboard Send-Receive Data Terminal




TI's *Silent 700** Model 743 KSR Data Terminal can help you take command of your data entry application needs today. The compact 743 offers a variety of easy-to-use standard features and options, and is an ideal input/output console. And with virtually silent thermal printing, the low-cost 743 leads the way for efficiency and reliability. The field-proven 743 is also available as a Receive-Only model. With either 743, you can depend on high-quality *Silent 700* performance.

TI is dedicated to producing quality, innovative products like the Model 743 KSR Data Terminal. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 743 terminals, contact the TI sales office nearest you, or write Texas Instruments Incorporated, P.O. Box 202145, Dallas, Texas 75220, or phone (713) 373-1050. In Canada, write Texas Instruments Incorporated, 41 Shelley Rd., Richmond Hill, Ontario L4C 5G4, or phone (416) 884-9181.

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TEXAS INSTRUMENTS
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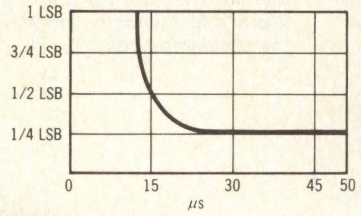
CIRCLE 106 ON INQUIRY CARD

the microprogram memory and are microcoded to match the microcycle length to the instruction execution time. The four "C" outputs have the same timing regardless of the microcycle length: $C_1$ is low only on the last oscillator period for each microcycle, $C_2$ is low on the last two oscillator periods, $C_3$ has a 50% duty cycle, and $C_4$ is low only on the first oscillator period.

The system control inputs provide for halting the clock outputs ($\overline{\text{HALT}}$) on the first or last oscillator period (FIRST/$\overline{\text{LAST}}$) of a microcycle. In the halt mode, SSNO and SSNC provide single-step control so that a single microcycle step will occur. The $\overline{\text{WAITREQ}}$ input can initiate a wait, but the wait timing input $C_X$ determines when the wait will occur. The $\overline{\text{WAITACK}}$ output indicates that the system clocks are halted in the wait mode. A separate $\overline{\text{READY}}$ input takes the chip out of the wait mode. Lastly, an $\overline{\text{INIT}}$ input overrides all other control inputs and allows the clocks to free run.

**Circle 444 on Inquiry Card**

## 12-bit successive approximation A-D converter



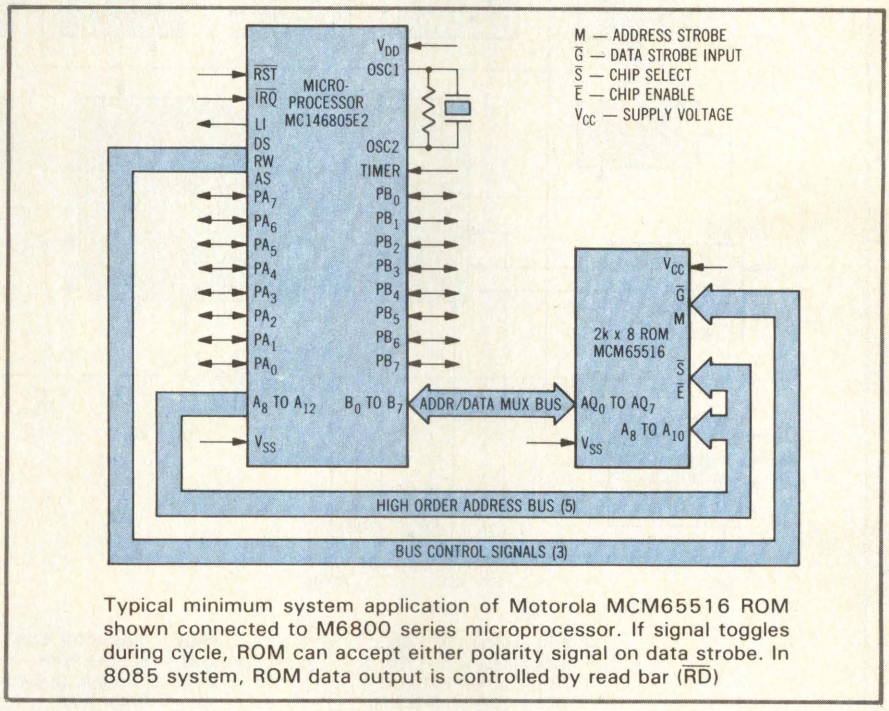

Linearity error as a function of conversion time (normalized) of AD5200 12-bit ADC. External clock of 260 kHz will yield 50-μs conversion time. Increasing clock frequency will decrease conversion time; linearity error, however, will increase

A second source for the industry standard 5200 series 12-bit analog to digital converters is now available. The recently announced AD5200, from Analog Devices, Route 1 Industrial Park, Norwood, MA 02062, is a hybrid design. MSI, linear monolithic chips, and active laser trimming of high-stability and thin-film resistors are used in the design of this adjustment free converter. Potentiometers are not required for calibration. A monolithic 12-bit feedback DAC is incorporated to lower the chip count and increase reliability.

Linearity of ±½ LSB is guaranteed over the operating temperature range. The converters are available in two input voltage ranges; ±5 V (AD5201/AD5204) and ±10 V (AD5202/AD5205). They can also be ordered with an internal buried zener reference or with an external reference for improved absolute accuracy. AD5200 converters come in two performance grades; the "B" is specified from −25 to 85 °C and the "T" is specified from −55 to 125 °C. "B" and "T" grades are also available processed to MIL-STD-883 level B requirements. All units are packaged in a 24-pin, hermetically sealed, ceramic DIP.

**Circle 445 on Inquiry Card**

## CMOS 2048 x 8 ROM designed for multiplex bus systems




Typical minimum system application of Motorola MCM65516 ROM shown connected to M6800 series microprocessor. If signal toggles during cycle, ROM can accept either polarity signal on data strobe. In 8085 system, ROM data output is controlled by read bar ($\overline{\text{RD}}$)

Designed for multiplex bus systems, a recently released ROM is fabricated in silicon gate CMOS technology. Manufactured by Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721, MCM65516 is mask programmable and organized 2048 bytes by 8 bits. Low power operation is from a single 5-V supply. The memory is compatible with CMOS microprocessors that share address and data lines.

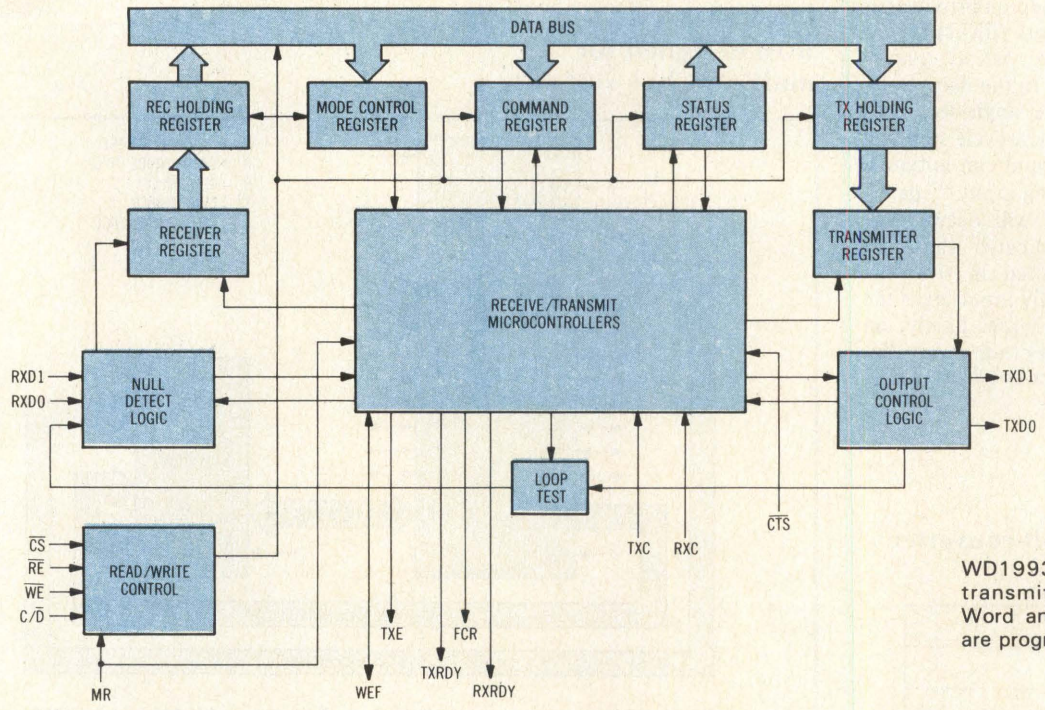
Compatibility of the versatile device is enhanced by allowing user selection of the active levels of pins 13, 14, 16, and 17. Pin 17 allows the user to choose active high, active low, or a third option of programming termed the "MOTEL" (MOTorola-intEL) mode. If the "MOTEL" mode is selected, direct compatibility with either the Motorola MC146805E2 or Intel 8085 type microprocessor series is provided. In the "MOTEL" operation the ROM can accept either polarity signal on the data strobe input as long as the signal toggles during the cycle.

The CMOS ROM shares address and data lines and, therefore, is compatible with the majority of CMOS microprocessors in the industry. Package size is reduced from 24 pins for standard NMOS ROMs to 18 pins because of the multiplexed bus approach. It is designed to provide low active and standby currents. The active power dissipation of 150 mW (at $V_{CC}$ = 5 V, freq = 1 MHz) and standby power of 250 μW (at $V_{CC}$ = 5 V) add up to low power for battery operation. Access time is 430 ns for the -43 and 550 ns for the -55.

A typical connection with the Motorola MC146805E2 CMOS microprocessor (M6800 series) is shown in the Figure. The data strobe (DS) on the microprocessor controls the output of data from the ROM.

**Circle 446 on Inquiry Card**

## Receiver/transmitter handles Arinc 429 protocol over 8-bit bus




WD1993 Arinc 429 receiver/transmitter configuration. Word and character lengths are programmable

WD1993, an avionic receiver/transmitter, is designed to handle Arinc 429 protocol digital data transmission. Word length is programmable from one to eight characters of 5, 6, 7, or 8 bits. Parallel data are converted into a serial data stream during transmission and serial to parallel during reception. The device is packaged in a 28-pin plastic or ceramic package and is available in commercial, industrial, and military temperature ranges.

From Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663, the bus-oriented MOS/LSI device contains a local loop-back test mode of operation controlled by the loop test enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped back" into the receiver input. The REN and TEN control bits must also be active (1) and the $\overline{CTS}$ input must be low. The status and output flags operate normally.

A block diagram of the WD1993 is shown in the Figure. Communication between the WD1993 and the controlling CPU occurs via the 8-bit data bus through the bus transceivers. There are two accessible data registers, which buffer, transmit, and receive data. They are the transmit holding register and the receive holding register. There is a parallel-to-serial shift register and a serial-to-parallel shift register (serial in/parallel out).

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status, or holding registers by activating the appropriate control lines: chip select ($\overline{CS}$), read enable ($\overline{RE}$), write enable ($\overline{WE}$), and control or data select (C/$\overline{D}$). Internal control is achieved through two internal microcontrollers, one for transmit and one for receive. The control registers, null detect logic, and various counters provide inputs to the microcontrollers. The microcontrollers generate the necessary control signals to send and receive serial data according to the Arinc 429-1 protocol.

**Circle 447 on Inquiry Card**

## 12-bit hybrid DAC line has 3-μs output, and 300-ns input, settling times

A recently announced line of hybrid 12-bit digital to analog converters provides maximum output settling times of 3 μs and maximum current settling times of 300 ns. Pin compatible with DAC-85 and DAC-87, the devices allow a choice of voltage or current output models with either 12-bit binary or 3-digit BCD coding. The DAC-685 from Datel Intersil, 11 Cabot Blvd, Mansfield, MA 02048, is available in two models. The "C" and "R" suffix models operate over the 0 to 70 °C and −25 to 85 °C temperature ranges, respectively. DAC-687 M is specified for −55 to 125 °C operation and is available with MIL-STD-883, class B screening.

Digital inputs of the DAC-685/687 series are TTL and CMOS compatible. Digital input current is 10 μA. Voltage outputs are pin-programmable with ranges of 0 to 5 V, 0 to 10 V, ±2.5 V, ±5 V, and ±10 V. Current output models have pin-programmable outputs of 0 to −2 mA, ±1 mA for binary coded versions, and 0 to −1.25 mA for BCD versions.

Gain tempco is ±20 ppm/°C, offset tempco is ±10 ppm/°C, and differential nonlinearity tempco is ±2 ppm/°C. The devices operate from ±15- and 5-V supplies with a maximum power dissipation of 770 mW.

**Circle 448 on Inquiry Card**

## Flat op amps and quad comparator introduced

Three 8-pin and one 14-pin operational amplifiers and a 14-pin low power quad comparator have been developed as hybrid ICs to help circuit designers meet high density board problems. Both the 8-pin and the 14-pin Miniflats from NEC Electron, Inc, 252 Humboldt Ct, Sunnyvale, CA 94086, have a lead pitch of 1.25 mm and are 1.5 mm thick. The 8-pin version is 5 mm wide. The 14-pin IC is 10 mm wide.

Some of the benefits of the linear Miniflats are soldering by reflowing, which results in easier handling; improved integration because wiring is needed only on one side of the mounting board; and reduced labor costs because Miniflats are suited to automatic mounting. Designations are μPC741G, the 8-pin general purpose amp; μPC1458G, the 8-pin dual general purpose amp; μPC4558G, the 8-pin high performance dual op amp; μPC324G, the 14-pin low power quad amp, and μPC339G, the 14-pin low power quad comparator.

**Circle 449 on Inquiry Card**

## Voice synthesizer chip uses partial auto correlation

A recently released LSI voice synthesizer chip can speak in female or male voices and is capable of synthesizing up to 63 words in about 20 s. Designated MN6401, the device uses the PARCOR (Partial Auto Correlation) system developed by Nippon Telephone and Telegraph Corp. The device is available from the Electronic Components Div of Panasonic Co, One Panasonic Way, Secaucus, NJ 07094.

The chip includes a built-in 32k ROM, operates from a single 5-Vdc power supply, has a maximum power consumption of 0.1 W (20-mA current drain), audio output of 1.0 V peak-to-peak maximum, bit rate of 1.2k to 5.4k bits/s, sampling frequency of 10 kHz, and a fundamental frequency of 200 kHz. TTL compatible, the circuit is packaged in a 28-pin DIL plastic case. In applications requiring more memory, the user can connect an external ROM. A speech speed control with six different settings is included. The chip can be operated either by manual or remote (computer) control.

Synthetic voice quality is influenced by the length of the sound time, which is determined by the data receiving method. Relationship between voice time, number of expressions, and the voice quality factor, when the 32k-bit inner ROM is utilized, is shown in the Table.

**Circle 450 on Inquiry Card**

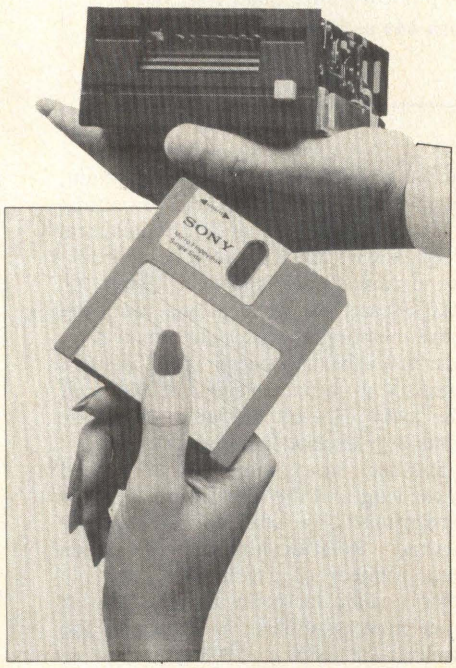
**Factors Influencing Voice Synthesis**

| Frame Length[2] / Bit Distribution | | 20 ms | | | | 10 ms | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit Rate (bits/s) | | Voice Time[1] (s) | Expressions | Bit Rate (bits/s) | | Voice Time (s) | Expressions |
| Type | Bit Frame | Min | Max | | | Min | Max | | |
| High range pitch Changeable type | 55 | About 1500 | 2750 | 21 | 30 | About 3000 | 5500 | 10 | 16 |
| Standard type | 54 | About 1500 | 2700 | 22 | 31 | About 3000 | 5400 | 11 | 16 |
| Long time type | 43 | About 1200 | 2150 | 27 | 39 | About 2400 | 4300 | 14 | 20 |

[1]Voice time and number of expressions are calculated on the min bit rate and assumption of 0.7 s/word

[2]Voice analysis (synthesis) space is called a "frame." The length (in units of time) is called the "frame length." A frame of 10 ms has a better voice/quality than that of 20 ms; however, the memory quantity will be shorter

# 3.5″ disc doubles floppy capacity in one-fourth the space




Large storage capacity and miniature size have been combined in the Micro Floppydisk drive introduced by Sony Corp of America at the 1981 National Computer Conference. Memory capacity of one side of the 3.5″ (8.9-cm) disc is 437.5k bytes. The disc is rated as having 2 times the storage capacity, 1.47 times the recording density, 27% of the volume, and 56% of the weight of the 5.25″ (13.34-cm) minidisc. Dimensions of the drive are 4″ (10.2 cm) wide by 5.1″ (13 cm) deep by 2″ (5.1 cm) high. It weighs only 1.7 lb (771 g).

### Design features

Designed for memory storage in personal and business computers as well as text editors, the disc is constructed of a material developed to achieve increased recording density; whereas a conventional 5.25″ disc has 48 tracks/in (19/cm), the 3.5″ disc has a density of 135 tracks/in (53/cm). The magnetic medium is protected by a hard plastic shell, and a metal guard can be slipped over the disc opening to keep the material free from dust, dirt, and fingerprints when the disc is not in use. This guard also prevents the disc from being inserted improperly; if the disc is inserted upside down, backwards, or with the disc guard closed, it will be automatically ejected.

The rigid disc shell also reduces friction between the moving disc and its stationary envelope. A metal centerpiece ensures proper centering. The drive motor is a specially designed direct drive flat disc motor that is said to be smaller, to have fewer parts, to be more stable and more reliable, to consume less power, and to provide better performance than other comparable motors. Other key features are 1-touch disc load/unload, fast transfer rate, write protect circuitry, and activity light. I/O signals are compatible with standard specification floppy discs.

### Specifications

Unformatted capacity ratings for single- and double-density recording, respectively, are 218.8k and 437.5k bytes/disc. Respective formatted capacities are 161.2k and 322.5k bytes/disc, 2.3k and 4.6k bytes/track, and 256 and 512 bytes/sector, with 9 sectors/track. Transfer rates, respectively, are 250k and 500k bits/s. For both densities, average latency is 50 ms and access times are 15 ms track to track, 365 ms avg, 15 ms settling, and 50 ms head load.

Rotational speed is 600 r/min and track density is 135/in (53/cm) for 70 tracks. Recording densities are 3805 bits/in (1498/cm) single and 7610 bits/in (2996/cm) double. Single-density encoding is FM (frequency modulation); double-density encoding is MFM (modified frequency modulation).

Error rates are predicted to be $1/10^9$ bits read for soft read, $1/10^{12}$ bits read for hard read, and $1/10^6$ seeks. MTTR (mean time to repair) is 30 min and component life is rated at 5 yr.

Voltage requirements are 12 Vdc ± 5% at 0.4 A typ and 5 Vdc ± 5% at 0.6 A typ. Power dissipation is 7.5 W continuous, 3.3 W standby. Environmental specifications are 40 to 113 °F (5 to 45 °C) ambient temperature at 20% to 80% relative humidity and 85 °F (29 °C) max wet bulb.

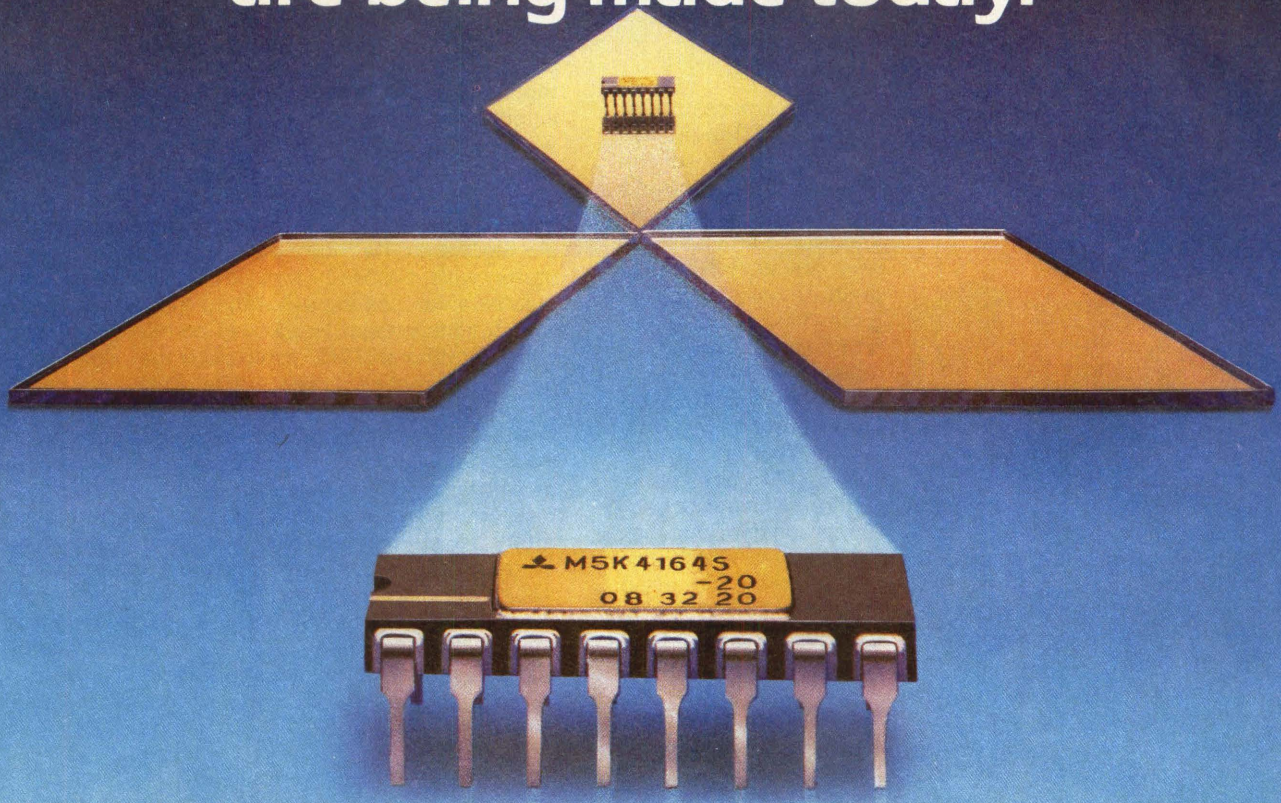
### Price and delivery

Single-unit price for the Micro Floppydisk drive is approximately $600; OEM discounts will be available. Deliveries will begin this month (July). Sony Corp of America, Data Products Div, 15 Essex Rd, Paramus, NJ 07652. Tel: 201/368-5000.

**For additional information circle 199 on Inquiry Card.**

# THE MITSUBISHI 64K RAM:

# The memories of tomorrow are being made today.

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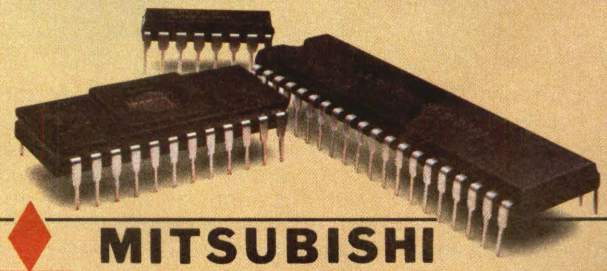

**Semiconductor Division**

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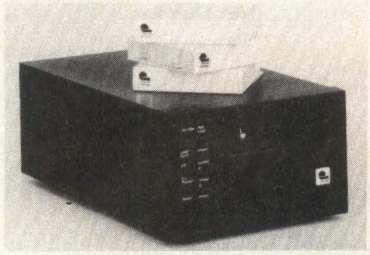
1230 Oakmead Parkway
Sunnyvale, California 94086
(408) 730-5900 TWX 910-339-9549

**MITSUBISHI ELECTRONICS**

CIRCLE 107 ON INQUIRY CARD

## 80M-byte tape cartridge drive offers fast data access as Winchester backup unit

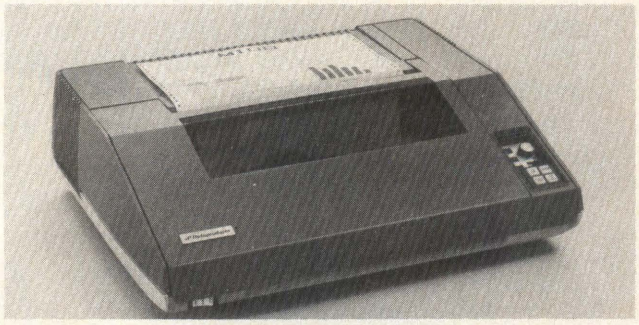
A low cost, high capacity, high speed direct access tape drive with the form factor of an 8" (20-cm) floppy drive, model 2000 supplies the high data rate and random access capability of a disc drive as well as the high capacity and removable low cost media of a tape drive. A user can transfer a bit, byte, block, or 80M-byte file without the start/stop and tape/disc synchronization problems associated with streaming tape units. The unit stores 100 times as much data, transfers data 15 times faster, and offers better access times than a floppy disc. Data are written on or read from a 0.5" (1.3-cm) tape cartridge that is manually inserted into the front of the drive. Each cartridge provides storage of up to 80M bytes of formatted data in a 4.87 x 4.87 x 1" (12.37 x 12.37 x 2.5-cm) package. Cartridges are fully enclosed to protect the tape media. Data are organized in blocks with direct access capability to any record in any block. Conceptually the unit appears to be a 32-head disc with 615 cylinders, with access characteristics that are similar to those of small Winchester discs.



Unlike reel type drives where the magnetic tape moves past read/write heads during read and write, the magnetic tape is held stationary while read/write heads are rotated longitudinally along the selected track for reading and writing, and transversely for seeking tracks. Tape from the cartridge is automatically fed from the supply reel around a semicircular tape guide and onto a takeup reel. A pair of diametrically opposed read/write heads offset by 16 tracks are mounted on a rotary scanner driven by a brushless dc motor with a closed loop servo. Motion of the scanner creates an air bearing separating the rotating surface from the stationary tape. Heads can be moved across the tape while rotating at 3200 r/min such that each head encompasses 16 tracks (32 total). After a block is written, tape is moved so that a succession of these 32-track blocks is written down the length of the tape within the cartridge. Each track allows for a formatted capacity of 4096 bytes, or a total of 131k bytes for each tape position (block). Read/write data are transferred from/to rotating heads via a rotary transformer. Rotational speed and incremental track to track movement of heads are coordinated to enable track switching in 9.4 ms. Drive electronics accommodate data rates of 4M to 5M bits/s. Average latency is 10 ms. Block to block moves require less than 250 ms. A full tape can be streamed at an average sustained data rate of 200k bytes/s. **Pragma Data Systems, Inc,** 610 Palomar Ave, Sunnyvale, CA 94086.

Circle 200 on Inquiry Card

## Matrix printer produces high density output using vertical column 14-wire printhead



Offering high resolution output with graphics, the M-100 uses a vertical column 14-wire printhead to achieve higher density characters than comparably priced matrix units. In addition, optional raster graphics capability provides full control over every dot. The printhead allows use of a 9 x 9 matrix representation of all alphanumeric characters, with true descenders for lowercase letters, capability for printing sub- and superscripts, and underlining at any position in the output. The printhead also permits solid black areas to be produced, important in applications involving OCR or UPC barcode characters and increasing representational contrast of graphics output for easier interpretation. Units can provide special symbols and characters with all accents required for international alphabets. Character sets are user programmable and can be changed online by downloading character representations from mainframe to internal memory.

The printer provides 140-char/s speeds, yielding 56 lines/min on 132-col formats, and 86 lines/min on 80-col lines. Bidirectional logic seeking print routines combine with the ability to slew over blank areas at accelerated speeds to improve throughput. Parallel interface units offer 1 line, and serial interface versions up to 2k bytes of RAM buffer to reduce CPU overhead. Registration and forms control have been improved to meet stringent alignment necessary for high quality graphics. Sound level emissions have been reduced to less than 65 dBa in typ applications. A 2-digit status display, built-in self-test, choice of front, bottom, or rear forms feed, and snap-in ribbon cassettes are also included. Units are designed to provide 6G impacts over 2.5 years of typical operation. **Dataproducts Corp,** 6200 Canoga Ave, Woodland Hills, CA 91365.

Circle 201 on Inquiry Card

# If You Use Back Planes...

## You need the Innovation and Imagination of TRW Cinch Connectors' "Creative Technology"

When you need back planes, you need back planes designed to do your specific job. That's where TRW Cinch Connectors' Creative Technology comes in. We sit down with you and customize your back planes to do exactly what you want. We provide a variety of connector centers, and TRW Cinch Connectors' reliability is unchallenged.

If your telecommunications, computer or military packaging applications require the following types of back planes, consider TRW Cinch Connectors as your primary source:

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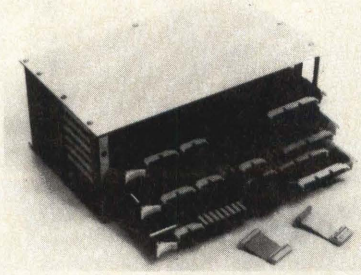
CIRCLE 108 ON INQUIRY CARD

**TRW CINCH CONNECTORS**

### Microcomputer based data acquisition system contains ROM-resident control software

Offered as integrated board set or packaged computer, MIDAX DT302 series offers a low cost solution in applications such as industrial process control, machine control, and automated test and measurement. The Multibus-compatible data acquisition and control system includes DTFIRM, a ROM resident firmware package, that provides support for all analog and digital I/O functions as well as a resident system debugger. Standard features include 8085A CPU with 40k memory, 16 A-D input channels with 12-bit resolution and software gain selection, 4 DAC outputs with 12-bit resolution, 2 serial I/O ports, 48 digital I/O lines, counter timer, and frequency I/O measurement. A floating point math processor is optional.

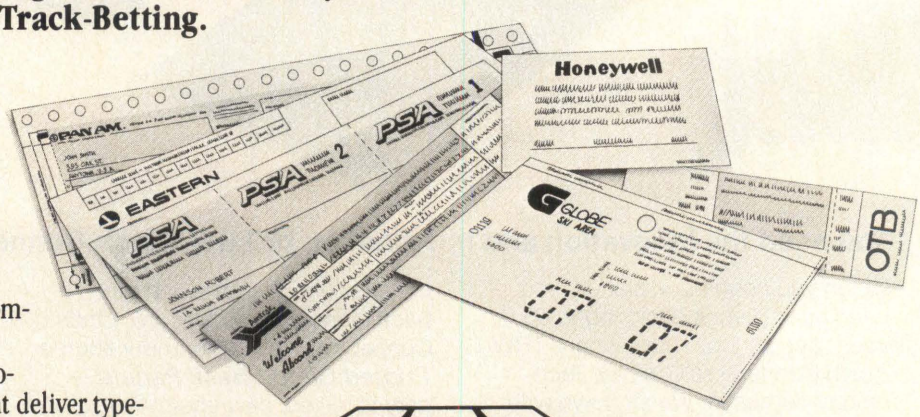


Model DT302 measures high level analog input signals with software selectable full scale ranges of 0 to 1.25, 0 to 2.5, 0 to 5, and 0 to 10 V unipolar, and ±1.25, ±2.5, ±5, and ±10 V bipolar. Standard resolution is 12 bits with ±0.03% system accuracy. System throughput is 35 kHz. Measuring low level, wide range analog input signals with software selectable full scale ranges of 0 to 20 mV, 0 to 100 mV, 0 to 1 V, and 0 to 10 V unipolar, and ±20 mV, ±100 mV, ±1 V, and ±10 V bipolar, the DT304 provides 12-bits standard resolution with ±0.01% system accuracy. System throughput rate varies up to 35 kHz. Model DT305 measures low level, wide range analog input signals with high common mode input isolation up to ±250 Vdc and 166-dB (at 60-Hz) noise rejection. Full scale input ranges are resistor selectable between 10 mV to 10 V FSR, unipolar or bipolar. Standard resolution is 12 bits with ±0.03% system accuracy. All versions feature 4- to 20-mA current loop I/O as an optional interface on all channels. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752.

Circle 202 on Inquiry Card


# OUR SPECIAL PRINTERS SATISFY SOME VERY SPECIAL CUSTOMERS:

**NCR, Eastman Kodak, Ford, Westinghouse, TRW, Honeywell, American Airlines, TWA, Amtrak, Raytheon Data Systems, N.Y.C. Off-Track-Betting.**

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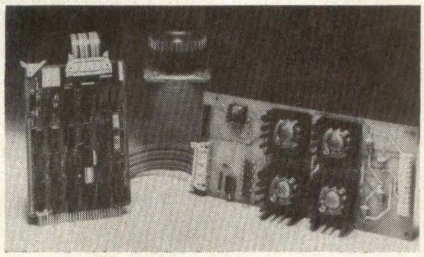
## CIRCUIT COMPONENTS AND SUBASSEMBLIES

### STD BUS STEPPER MOTOR CONTROLLER



Stepper motor controller card 7911/SMC with appropriate power driver card provides STD bus with complete programmable unipolar or bipolar stepper drive system and minimizes software and hardware overheads. Program defined step rate, direction, and number of steps function automatically. Features include automatic up or down ramping, up to 30k-step/s stepping rate, and 65,535-step counter. 7911/USD unipolar and 7911/BSD bipolar stepper drivers are currently available. The controller is completely STD bus compatible and provides any processor with capability for incremental motion control. **Matrix Corp,** 1639 Green St, Raleigh, NC 27603.

**Circle 203 on Inquiry Card**

### PID LOOP CONTROLLER

Dedicated multiloop controller with graphics CRT terminal is offered in 12-, 16-, or 20-cascadable P/PI/PID loop configurations. Operators need only enter required control parameters using graphics terminal. Std features include CRT loop status display in engineering units, tuning display for system setup, high/low alarming on CRT, and anti-reset windup/proportional bandlimit/deadband/polarity control. **Control Logic, Inc,** 9 Tech Circle, Natick, MA 01760.

**Circle 204 on Inquiry Card**

## DATA TERMINALS

### MULTI-USER INTELLIGENT TERMINALS

Diskette based CDX-68/24 and disc based CDX-68/44 intelligent terminals use an OS-9 operating system patterned after Bell Labs' UNIX to allow concurrent execution of a variety of programs by multiple users. The terminals support a variety of communications protocols including 3270, 2780/3780, and TTY. The 2M-byte diskette memory of the CDX-68/24 is expandable to 4M bytes and the 10M-byte disc of the model 44 can be expanded to 40M bytes. The terminals support a wide variety of peripherals, communications, and applications development tools. **Codex Corp,** 20 Cabot Blvd, Mansfield, MA 02048.

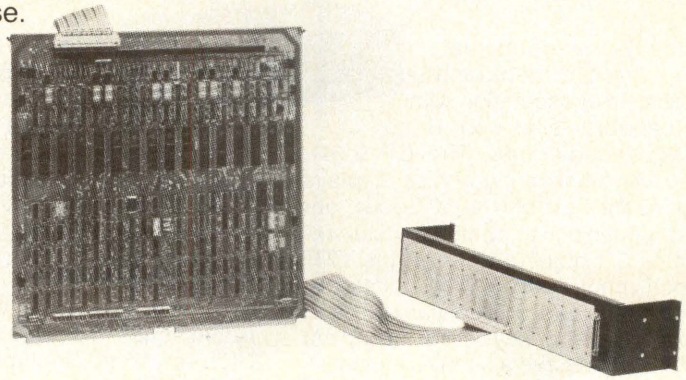
**Circle 205 on Inquiry Card**


# ECLIPSE/NOVA* USERS...

## Meet Our NEWEST Mux!

### Custom Systems' Model 420 Programmable Terminal Interface (PTI):

- Eliminates need for comm. chassis.
- Operates in any Nova 3, Nova 4, or Eclipse.
- Includes 'plug-and-go' distribution panel.



The PTI (16 programmable channels) is software-compatible with Data General's ALM programming format. Unlike DG's multiplexers, however, the PTI supports CTS, can be switched on demand to operate RS232 or 20 MA terminals, and comes complete with a 16-port distribution panel. Best of all, it sells for only $2200!

Call or write today for more information.

**CUSTOM SYSTEMS INC**
6850 Shady Oak Road
Eden Prairie, Minnesota 55344
Telephone: (612) 941-9480 Telex: 290975

*Trademark of Data General Corporation

CIRCLE 110 ON INQUIRY CARD

## DATA TERMINALS

### VIDEO DISPLAY TERMINAL

Features added to ADM 31 intermediate terminal include programmable function keys, 25th line for terminal status, smooth scroll, X-ON and X-OFF, cursor on/off, and horizontal split screen. Std features include 2 full 1920-char pages of memory, block mode operation, complete editing capability, function keys, visual attributes, business graphics, self-test, typewriter tab stops, formatting, and protected fields. 12″ (30-cm) diagonal CRT screen displays 25 lines of 80 chars in upper- and lowercase. **Lear Siegler, Inc, Data Products Div,** 714 N Brookhurst St, Anaheim, CA 92803.

Circle 206 on Inquiry Card


NEW!

**Real-time three-dimensional graphics representation.**

**The GP-6-3D sonic digitizer. Only from Science Accessories.**

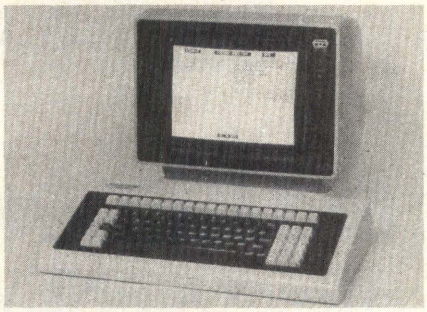
Finally, low-cost, real-time, three-dimensional graphics representation with the capabilities of coordinate measuring devices: The GP-6-3D. Used with intelligent graphics displays such as the Tektronix 4050 Series, our three-dimensional sonic digitizer re-creates 3D objects right on the CRT screen, tracing up to 100 points per second. Instead of painstaking hand calculation and keyboard input, the GP-6-3D can have a simple geometric form on your CRT screen for viewing from any angle in a matter of seconds. And the system can allow the simultaneous calculation of volumes, center of gravity, and surface areas, all in real-time.

Our GP-6-3D is being widely applied in engineering design, human motion analysis, medicine, and other fields where three-dimensional objects must be duplicated, studied, and measured. It's even capable of 0.01 cm resolution. If so many diverse applications can utilize three-dimensional digitizing, maybe you can, too. Write and see. We're Science Accessories Corporation, 970 Kings Highway West, Southport, CT 06490, (203) 255-1526.

SAC® SCIENCE ACCESSORIES CORPORATION

**See Us at the Siggraph Show, Dallas, August 3-7, Booth 904**


### INTELLIGENT COLOR ALPHANUMERIC TERMINAL



CTM-300 is a serially interfaced (RS-232-C) ASCII terminal with an 8-color CRT display. Std format is 80 chars x 25 lines; it is user programmable to other formats. Firmware executes intelligent commands and conforms to ANSI X3.64 std; users may customize terminal functions from host computer through program downloading. Programs are downloaded into the unit's 2k RAM user memory for execution by its Z80A CPU. In combination with the 18 user-definable keys, this allows easy adaptation of the unit to the application. The keyboard, which contains terminal intelligence, offers typewriter layout and provides a numeric keypad as well as user-definable keys. Keyboard is cable connected to the monitor for maximum operator comfort. Std features include lightpen interface, printer interface, and American/European standard for power and video. **Matrox Electronic Systems, Ltd,** 5800 Andover Ave, Montreal, Quebec H4T 1H4, Canada.

Circle 207 on Inquiry Card

## DATA TERMINALS

### 1200-BAUD PORTABLE TERMINAL

Miniterm model 2300 is a lightweight 1200-baud unit with a 160-char/s bidirectional thermal printer. Std features include 6 user-definable soft function keys, battery protected RAM, 80- or 132-col printing, a simplified command mode to set terminal configuration, switch-selectable 300/1200-baud communications, and true upper- and lowercase printing with descenders. Printing speed of 120 chars/s is achieved in full-duplex, 1200-baud operating environments, compatible with Vadic 3400 modems. Provision for up to 8k bytes of user available ROM permits creation of special application terminals by OEMs. A high resolution printer/plotter option offers over 8000 dots/in² (1240/cm²), multiple communication options include switch-selectable acoustic coupler/data jack, and soft function keys for automatic log-on and interactive prompting. **Computer Devices, Inc,** 25 North Ave, Burlington, MA 01803.

**Circle 208 on Inquiry Card**

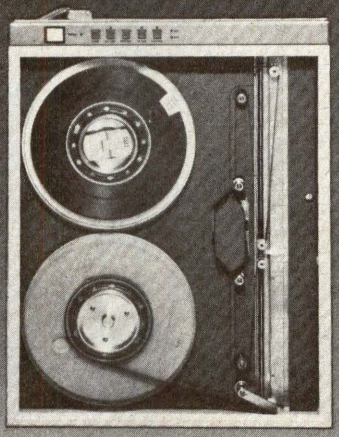
### TOUCH INPUT DISPLAY TERMINAL

Using scanning infrared beam technology, the Dialogue TouchTerm 80™ provides a high speed, safe, and reliable method for the user to interact with the host computer. The unit responds to a simple touch on the surface of the display, eliminating the need for typing skills or for special command languages. A detached keyboard, brightness control, descenders on lowercase letters, and nonglare keytops and display minimize body and eye strain. Terminal features are initiated by user-defined escape codes to avoid conflict with existing software. These soft codes provide for audible feedback to the operator where the application demands it: point mode, stream mode, and set stylus size among others. Continuous self-diagnostics assure the user of error-free operation. Stylus size may be varied by the program. Up to 1920 targets can be located anywhere on the screen. The keyboard has fast repeat action keys that enable rapid data entry, and a numeric pad. Separate keys control movement of switch-selectable cursor. Data format is 24 lines x 80 chars plus an 80-char status line. **Ampex Corp, Memory Products Div,** 200 N Nash St, El Segundo, CA 90245.

**Circle 209 on Inquiry Card**


$6985.
COMPLETE
TAPE SYSTEM

The 75ips TDX Series II complete with embedded microformatter and interface to PDP-11/VAX, LSI-11, NOVA/ECLIPSE, RS-232, IEEE-488 or Dual Buffered I/O. $6985-800 bpi/NRZ or $7885-NRZ/PE Dual Density in single unit quantity. Contact us today.



TDX PERIPHERALS
Division of GAW Control Corp.
150 New York Avenue, Halesite, NY 11743
(516) 423-3232

CIRCLE 112 ON INQUIRY CARD

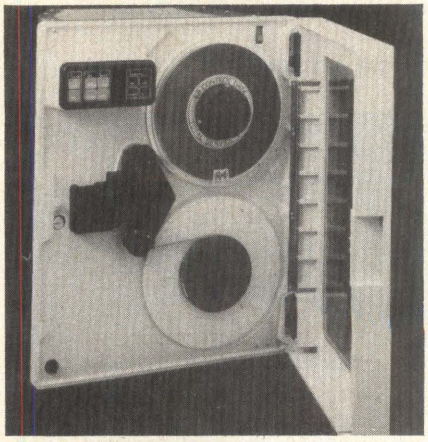
## MEMORIES

### HARD DISC SYSTEM

File Controller III interfaces with up to 8 OP-1 Display Computer systems, each with its own Disc Controller III, which in turn interface up to 2 CDC 9448-96 Phoenix 96M-byte hard disc drives; each computer system then has access to any disc drive with priorities assigned by the file controller. 8 ports are provided as 4 fully buffered pairs. Each pair consists of 2 parallel connected ports and accommodates up to 200′ (60 m) of cable. Max system cable length is 800′ (240 m). **Ontel Corp,** 250 Crossways Park Dr, Woodbury, NY 11797.

**Circle 210 on Inquiry Card**

### STREAMING TAPE TRANSPORT



Using data streaming techniques, magnetic tape transport CDC 92180 is designed for use with minicomputer and microcomputer systems. The transport serves as backup for medium capacity fixed disc drives and as a general purpose transport. A formatted reel to reel transport that uses 0.5″ (1.3-cm) magnetic tape with a density of 1600 bits/in (630/cm), it records and reads 9-track PE format at a speed of 100″ (254 cm)/s when operated as a streaming device, and at 12.5″ (32 cm)/s in start/stop mode. Its design incorporates a 13″ (33-cm) tape path, air bearings, and distributed edge guides to control tape movement and to ensure reliability of data and longer tape life. Built-in diagnostic capability allows operators to identify faults and perform routine maintenance functions. **Control Data Corp,** Box 0, Minneapolis, MN 55440.

**Circle 211 on Inquiry Card**


# ORIGIN OF THE SPECIES.

Fourteen years ago, Pertec® set the industry standard in mini-computer tape drives. Since then, a lot of other companies have followed with copies of their own—good copies.

Even so, our innovations continued and we still remain the number one independent tape drive manufacturer.

Evidently, people realize that there's just no substitute for the original.

For more information, write Pertec Computer Corporation, Peripherals Division, 21111 Erwin Street, Woodland Hills, CA 91367.

PERTEC PERIPHERALS Perfecting Technology

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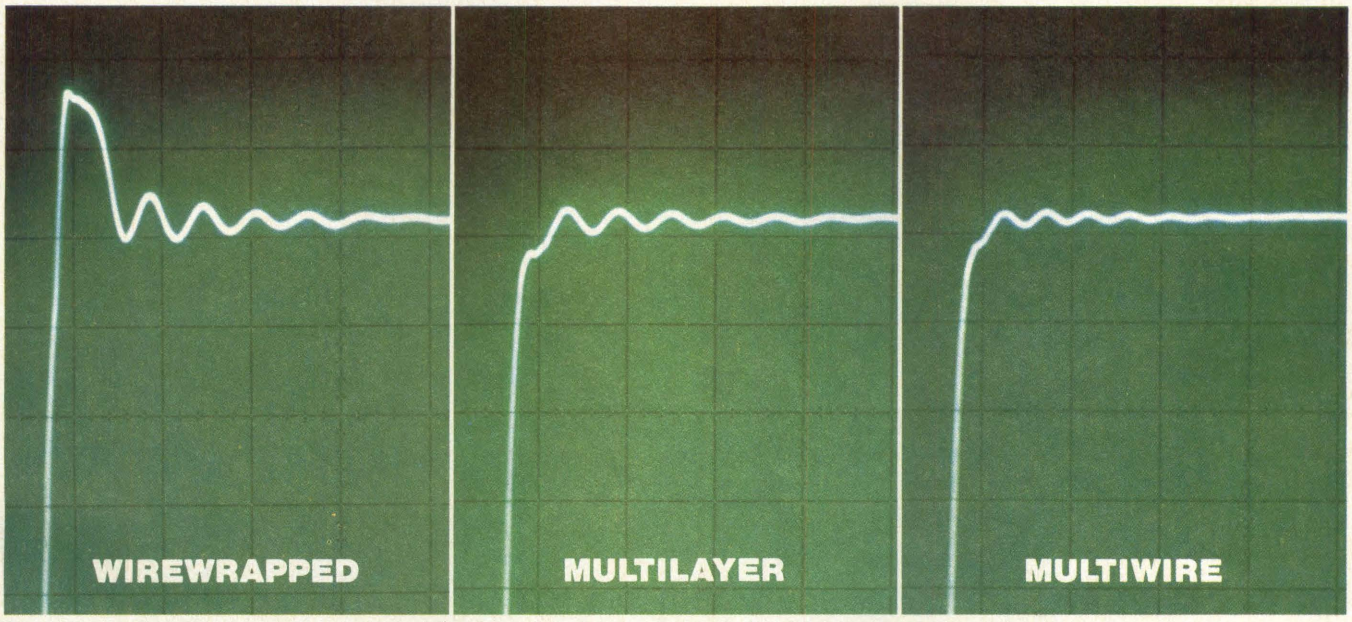
### 4M-BYTE FIXED HEAD DISC DRIVE

Model 990 offers 10 times greater access speed than moving head drives through interchangeable Disc Cells, fixed head disc cartridges. Cartridges contain drive spindle, Winchester type media, and read/write head assemblies. They are interchangeable within models, self-cooling, and sealed against contaminants. MTTR for the units is specified as 15 min; MTBF as 10k hours. Soft data error rate is 1 in $10^{11}$; hard error rate is 1 in $10^{13}$. Average access time is 12.5 ms at 2400 r/min and 8.5 ms at 3600 r/min. **Dataflux Corp,** 1050 Stewart Dr, Sunnyvale, CA 94086.

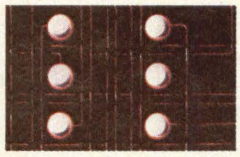
**Circle 212 on Inquiry Card**

# Multiwire* Optimizes ECL.

## These traces tell the story.




Wirewrapped and multilayer circuit boards can handle the high speeds of emitter-coupled logic. But Multiwire does it better. With Multiwire, *board impedance is precisely controlled* to meet circuit specs and is *consistent from signal to signal and board to board.* The problem of signal reflections with wirewrapped and multilayer requires the use of discrete series-damping and terminating resistors. Multiwire reduces design problems,



A typical example of the circuit density achievable with Multiwire circuit boards.

provides consistent electrical characteristics, and results in lower cost and better circuit performance. Add to that other Multiwire advantages: less design time, shorter lead times, easy circuit changes, reduced inspection costs, and higher production yields. The choice is obvious. Multiwire is the way to go. Write or call today for details.

Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307

MULTIWIRE DIVISION
KOLLMORGEN CORPORATION

*Multiwire is a U.S. registered trademark for the Kollmorgen Corporation discrete wired circuit boards.

CIRCLE 114 ON INQUIRY CARD

## MEMORIES

### SOLID STATE STORAGE SYSTEM

Maxiram-15 attaches to I/O bus of DEC's PDP-15 or -9 computers, replacing RF15 controller and RS09 fixed head disc drive. Completely compatible with the rotating devices, system features no moving parts, zero latency, storage capacity equivalent to from 1 to 8 RS09 drives, and core or semiconductor storage module. Unit includes power supply, blower assemblies, and controller in 19" (48-cm) rackmounted chassis. Capacity is from 0.25M to 2M 18-bit words. **Imperial Technology**, 831 S Douglas St, El Segundo, CA 90245.

**Circle 213 on Inquiry Card**


# TOUGH LITTLE TAPE SYSTEM

# SETS-1

A 23-megabit digital tape system for airborne and other severe environments

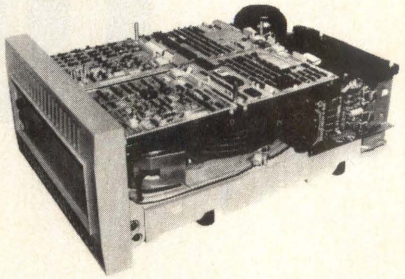
Meeting MIL-E-16400, 5400 and 4158, SETS-1 is a compact digital tape system which stores 23 megabits of data at 1600 bits per inch on 300 feet of ¼-inch magnetic tape. It has bidirectional read/write on 4 tracks with a 192K bit-per-second transfer rate.

SETS-1 consists of a compact drive module coupled to a removable, hermetically sealed tape module. It's being used right now by the Army and Air Force for bulk storage and data gathering from tanks, aircraft and remote sites. Also as a data entry device for mission loaders, communications and fire control systems.

**Phone or write for details today.**

**Severe Environment Systems Company**
A Subsidiary of Electronic Memories & Magnetic Corporation
P.O. Box 668 • Chatsworth, CA 91311 • Telephone: (213) 998-9090 • TELEX 69-1404

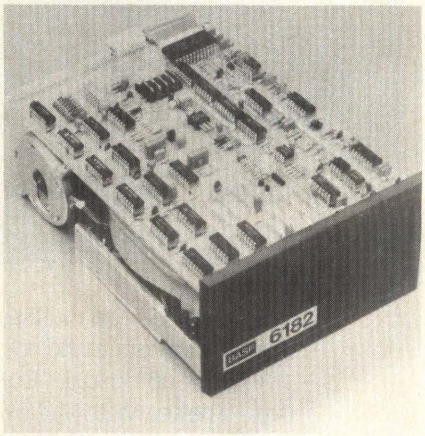

### 14" WINCHESTER DISC DRIVE



Sapphire 160 consists of disc module, drive motor, electronics, and power supply arranged on a common base plate; its modular design allows drive to be mounted into frame of host system. Unit provides up to 160M bytes of storage capacity, 6400 bits/in (2520/cm), and 600 tracks/in (236/cm), in environments that are not air-conditioned. Op temp is 10 to 40 °C. Unit measures 9.8 x 16.5 x 24.4" (24.9 x 41.9 x 62.0 cm) and weighs 88 lb (40 kg). **Tecstor,** 16161 Gothard Ave, Huntington Beach, CA 92647.

**Circle 214 on Inquiry Card**

### 5.25" FIXED DISC DRIVE SERIES




The 6180 series of 5.25" (13.34-cm) fixed disc drives includes model 6182 with 2 discs and 6M-byte unformatted capacity (5M-byte formatted), and model 6183 with 3 discs and 10M-byte capacity (7.5M-byte formatted). Drives have 2-ms track to track access time, 100-ms avg data access time, and 5M-bit/s transfer rate. Track density is 254 tracks/in (100 tracks/cm) and bit density is 7690 bits/in (3028 bits/cm). **BASF Systems Corp,** Crosby Dr, Bedford, MA 01730.

**Circle 215 on Inquiry Card**

Edward H. Budd, President, The Travelers Corporation

Employers. Would you like to increase production? Cut down on absenteeism? Reduce industrial accidents?

We think you can if you start a physical fitness and health program for your employees.

Over 400 companies like Boeing, Chase Manhattan Bank, The Travelers Corporation, Phillips Petroleum, Kimberly Clark, Prudential Insurance and Xerox are already doing it. So can you at very low cost — by providing a place to exercise or jog, a running track, bicycle racks and showers. You can give or share the time for fitness. Encourage exercise before or after work.

To find out how *you* can start a fitness and health program in *your* company write: Employee Fitness, Washington, D.C. 20201

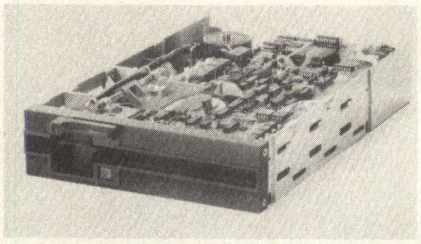
**President's Council on Physical Fitness and Sports.**

## ENERGY FOR AMERICA - IT COMES FROM EXERCISE

## MEMORIES

### HALF-HEIGHT FLOPPY DRIVE

Two Thinline drives install in the cabinet space taken by one full-size floppy drive. Height of the drive is only 2.3" (5.8 cm), and the weight is just 7 lb (3 kg). Units feature an efficient dc brushless spindle motor, eliminating the need to make voltage changes for European use. They can be turned on and off by control signals from the interface, reducing wear on the diskette as well as the drive. The drive incorporates the firm's patented double-sided head, eliminating the need for a head load solenoid. Head positioning is accomplished by a band driven carriage that is virtually frictionless, thereby increasing positioning accuracy. Track to track access time is only 3 ms. Model TM 848-1 reads and writes 0.6M bytes (double-density, IBM format) on one side of the disc; model TM 848-2 writes 1.2M bytes using both sides. **Tandon Corp,** 20320 Prairie St, Chatsworth, CA 91311.



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# Multiperipherals For Your Multibus

MULTIWAYS

Need large disk capacity for your Multibus system? Xylogics has what you need.

**Multi Disks**
- CDC Hawk (10 MB)
- CDC cartridge modules (32-96 MB)
- CDC storage modules (80-300 MB)
- CDC Lark (8 MB/8 MB)
- BASF (24 MB)
- NEC (20-80 MB)

**Multi Interfaces**
Choice of Xylogics **Peripheral Processors** for either storage module or Diablo 44B interface.

**Multi Benefits**
- Bit-slice control technology
- Compatible with INTEL, NATIONAL 80/20, 86/12
- SMD configurations of up to four drives in any mix of storage capacities
- Fast delivery
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The Reason is Xylogics
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## SOFTWARE

### COBOL COMPILER

An enhanced ANSI '74 standard version for DEC's RT-11 and RSTS/E operating systems, RJ-11 COBOL consists of compiler, runtime system, and supporting programs designed to run on a PDP-11 using RT-11 or RSTS/E. Utility programs are provided to print file contents or program results, sort files, update files, print file details, and extend files. RJ-11 COBOL will run on any PDP-11 with at least 16k-word main memory, a console terminal, and a std floppy or cartridge mass storage device. **ECC Systems,** 315 Goodman's Hill Rd, Sudbury, MA 01776.

Circle 217 on Inquiry Card

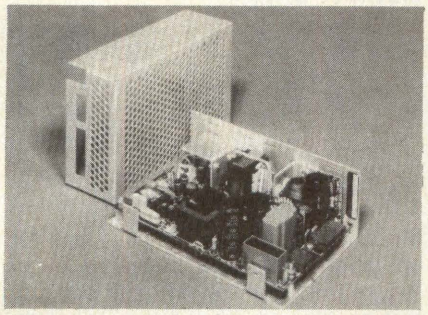
### COMPILER AND RUNTIME LIBRARY

A superset of BNF notation, PL/C language has been implemented to boost productivity in development of programming language compilers, human language translators, program language converters, machine language translators and disassemblers, and interpreters for complex command languages. The compiler provides rapid implementation of complex syntactical analysis algorithms, fast code generation, and facility for inline user assembler language code. **MRD Systems Inc,** PO Box 147, Spring Valley, MN 55975.

Circle 218 on Inquiry Card

## POWER SUPPLIES AND REGULATORS

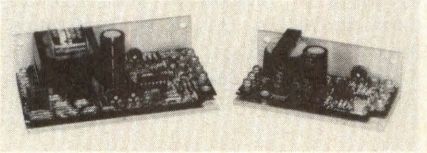
### VDE AND FCC APPROVED MULTIPLE-OUTPUT SWITCHER



VDE-50 series open frame 50-W regulated supplies meet all VDE 0730 safety standards, and have a built-in emi filtering system that meets VDE 0871/6.78 level A spec and FCC spec 20780. Dc outputs are 5 V at 6 A, 12 or 15 V at 1.0 A, and −12 or −15 V at 1.0 A. Line regulation is ±0.2% max at 90 to 132 Vac or 180 to 264 Vac, 47- to 440-Hz input. Overall regulation of 5-V primary output is ±1%. Overall regulation of the other outputs is ±4% from 20% to 100% of max rated load, line regulation over input voltage range, and centering. Units feature voltage protection on the 5-V output, soft start, short circuit protection on all outputs, reverse voltage, overload, and brownout protection. Noise and ripple are less than 1% peak to peak on any output. Hold-up time is 20 ms min. Typ efficiency is 70%. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.

**Circle 219 on Inquiry Card**

### POWER FAIL MONITORS



PFM-1 and -2 monitor system ac input power, providing a TTL compatible indication of reduced line conditions and transients, plus complete power outages. PFM-1 provides power fail detection for all foreign and domestic ac applications. PFM-2 adds phase shifting circuitry to detect ac power loss occurring at any point on the input sine wave and an external dc sense capability that allows users to monitor any external dc output voltage from 5 to 48 V. **Power-One, Inc,** Power One Dr, Camarillo, CA 93010.

**Circle 220 on Inquiry Card**

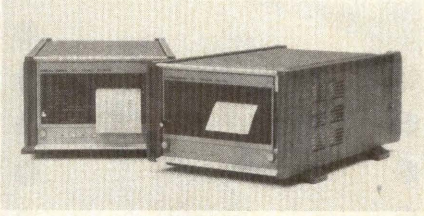
### LINEAR VOLTAGE REGULATOR

LM117M/217M and 317M adjustable 3-terminal regulators are capable of supplying in excess of 0.5 A over an output range of 1.2 to 37 V. The devices are easy to use and require only 2 external resistors to set the desired output voltage. Internal current limiting, thermal shutdown, and safe area compensation make them virtually failure proof. The devices serve various applications including local oncard regulation. They also make a simple adjustable switching regulator and a programmable output regulator. By connecting a fixed resistor between the adjustment and output, the devices can be used as a precision current regulator. Available in TO-66 and TO-220 cases, the devices are offered in 0 to 125 °C, −25 to 150 °C, and −55 to 150 °C temp ranges. The TO-220 plastic package is available only in the lower temp range. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

**Circle 221 on Inquiry Card**

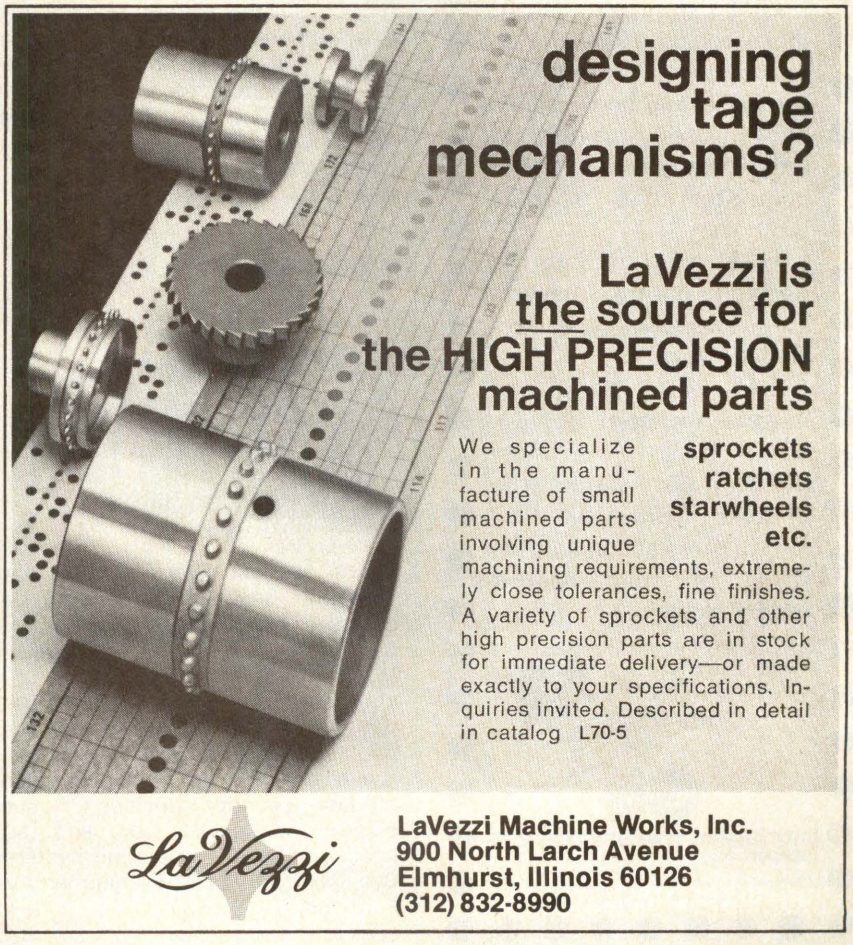
## PRINTERS/PLOTTERS

### THERMAL PRINTERS/PLOTTERS

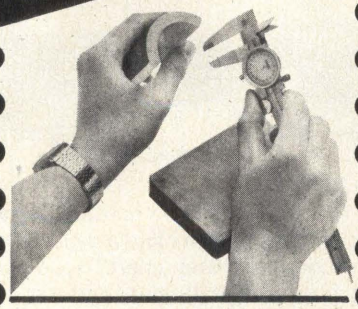


Models 1001 and 1002 feature list and text printing formats and a digital plotting function. "Step chart" type plotting from a digital input, and IEEE 488 interface are std. Available with or without time clock, models offer 20-col, 2.5-line/s thermal printing capability with full 64-char ASCII alphanumeric character set. A 20-col BCD interface is optional, and can be installed in addition to the GPIB interface. **Racal-Dana Instruments, Inc,** 18912 Von Karman Ave, Irvine, CA 92713.

**Circle 222 on Inquiry Card**

# Computer Hardware Designers!



## GM ceramic magnets meet tough specs!

GM ceramic magnets give you better dimensional accuracy, functional flexibility and environmental reliability.

GM magnets hold dimensional tolerances to computer hardware accuracies and have a stable non-outgassing coating to satisfy the critical needs of computer disc storage technology.

GM coated, tight-tolerance ceramic magnets are available as either arcs or flat blocks.

GM delivers the quality magnets you need yet stays within budget. For more information, circle the number below for our informative catalog and the name of your nearest representative.

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an ESMARK Company

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(214) 296-4711 ■ Telex 79-1634 • GENOX

CIRCLE 119 ON INQUIRY CARD


# PRODUCTS

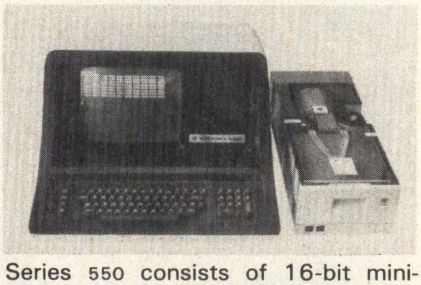
## COMPUTERS AND COMPUTER SYSTEMS

### ENTRY LEVEL MINICOMPUTER

MARK III, a 16-bit mini with 64k bytes of memory uses the main processor to supply intelligence for peripheral controllers, thereby eliminating separate interface and intelligence for each individual controller. A combined CPU/memory board with an integrated power supply is also provided with a connector for a std Pico-N software protection device. The peripheral interface board consists of multiplexer, disc controller, and streamer tape drive interfaces. They connect with the CPU/memory board via the backplane. The built-in disc controller interfaces with 1 or 2 drives with a std SMC/CMD specification. It is also compatible with SMD interfaced Winchester drives. Up to 4 streamer tape drives may interface to the PIB using a single ribbon cable. The unit has an asynchronous DMA multiplexer capability consisting of 4 ports that are independently strappable to 9600 baud. The ports have modem interface capabilities and can be connected to a line printer and/or a variety of terminals. Fully compatible with the IRIS operating system, the unit implements the std instruction set in 600 ns. **Point 4 Data Corp,** 2569 McCabe Way, Irvine, CA 92714.

**Circle 223 on Inquiry Card**

### MINICOMPUTER SYSTEMS

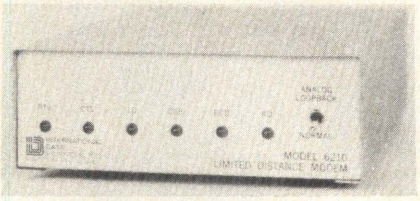


Series 550 consists of 16-bit minicomputer, 64k bytes of memory, disc controller capable of driving CDC 9455 Lark module drives, printer controller (parallel or serial), and a second asynchronous port for an additional CRT. 550-ns CPU has Data General compatible instruction set, and an adapter is available on the CPU board to accommodate security devices. System operates under IRIS, IOS, BITS, BLIS/COBOL, and MICOS operating systems. **Bytronix Corp,** 2701 E Chapman Ave, Fullerton, CA 92631.

**Circle 224 on Inquiry Card**

## DATA COMMUNICATIONS

### ASYNCHRONOUS LIMITED DISTANCE MODEM



Model 6201 modem is designed for operation over telco or private 2- or 4-wire unloaded twisted-pair conductors at rates to 9600 bits/s. It can be used in local data distribution up to 7 mi (11 km) with #26 AWG wire. Strap selection provides for constant or controlled RTS, high/low transmit level, 2- or 4-wire operation, and normal or high receiver impedance. A pulse modulation scheme varies transmit signal polarity on balanced lines. Interface is EIA RS-232-C/CCITT V.24. 20-mA current loop interface is available. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865.

**Circle 225 on Inquiry Card**

### SYNCHRONOUS SHORT-HAUL DATA SET

Limited distance data set DS547 operates up to 6 mi (9.7 km) at selectable rates from 1200 to 19.2k bits/s and meets all requirements of CCITT 43401 specification. The set may be used in full-duplex, half-duplex (4-wire), or multidrop configurations, and is RS-232-C compatible. D-A loopback is incorporated, as is internal lightning protection at transmission cable terminals. **Develcon Electronics Inc,** 200 North St, Doylestown, PA 18901.

**Circle 226 on Inquiry Card**

### COMPACT 9600-BIT/s MODEM

Designed to support high speed point to point applications or to act as a backbone link in standalone multiplexer applications, DataComm 9600 provides 9600-bit/s synchronous transmission over 4-wire unconditioned voice grade lines. Fallback rates of 7200 or 4800 bits/s handle continued operations over severely degraded circuits. **General DataComm Industries, Inc,** One Kennedy Ave, Danbury, CT 06810.

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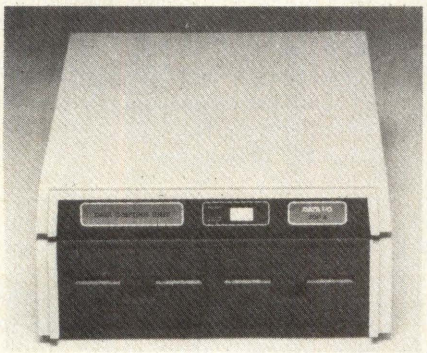
## MISCELLANEOUS

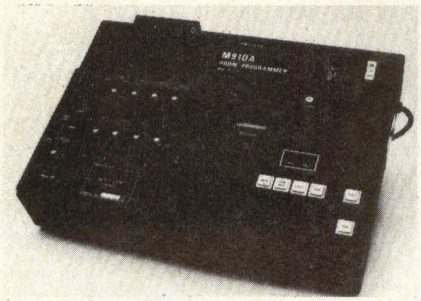
### PRODUCTION P/ROM PROGRAMMING SYSTEM



P/ROM and logic device programming system combines a diskette based data control unit (DCU), production programmer, and handler UniPak to address the whole sequence of tasks associated with device programming for production. The data control unit has 1 or 2 disc drives to provide readily accessible online storage for programming data. A single 5.25" (13.34-cm) floppy diskette can store 82k bytes of 8-bit programming data, enough for 41 (2716 type) EPROMs. The DCU's built-in directory files programming data patterns under user specified part numbers. With 3 RS-232-C I/O ports, the unit can serve up to 3 programmers. It works as a slave in connection with the production programmer; the interactive command set gives the operator control of both instruments from the programmer's front panel. **Data I/O Corp,** Box 308, Issaquah, WA 98027.

**Circle 228 on Inquiry Card**

### PRODUCTION P/ROM PROGRAMMER



M910A P/ROM control unit allows user to repeatedly BLANK CHECK, DUPLICATE, or COMPARE P/ROMs with a single keystroke. Unit can program over 450 different devices, including P/ROMs, PLAs®, and microprocessors that contain P/ROMs. With gang personality modules, unit duplicates up to 8 devices simultaneously and performs testing of P/ROMs, including high/low $V_{CC}$ tests with rated loads and tests for shorts. Features include lighted pass, fail, and function indicators, and audio signals for pass and fail. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940. **Circle 229 on Inquiry Card**

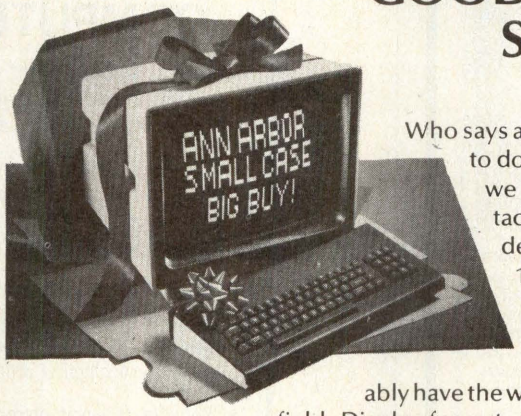
### SPEECH SYNTHESIZER

To produce speech, serial data are input through the RS-232 interface of the ASCII VOCALIZER I. The unit vocalizes any words or characters contained in its vocabulary and ignores all others. The std vocabulary is 200 words, expandable to 800. The synthesizer contains an internal amplifier and loudspeaker and responds to commands to set output loudness levels and to flush the internal buffer for emergency messages. Operating speed ranges from 110 to 19.2k baud. A vocabulary generator unit and EBCDIC model are also available. **Micro Communications, Inc,** 1509 Government St, Suite 214, Mobile, AL 36604. **Circle 230 on Inquiry Card**

### SPEECH SYNTHESIZER MICROCIRCUIT AND BOARD

TDS90 speech synthesizer microcircuit and TDS910 board make up a system that allows the spoken word to be converted into a small number of speech parameters, stored in P/ROMs, and subsequently reproduced as speech. The synthesizer board contains the microcircuit, sockets for 3 speech memories, and an audio power amplifier for driving a speaker. Three interfaces include switch closure, 2-wire serial ASCII, and parallel binary with handshake. A std vocabulary ROM is available. **Stynetic Systems, Inc,** Flowerfield, Bldg 1, St James, NY 11780. **Circle 231 on Inquiry Card**


# GOOD CRT'S COME IN SMALL PACKAGES




Who says a CRT terminal has to be big and bulky to do a good job? At Ann Arbor Terminals, we offer a full 15-inch screen *and* detached keyboard as standard on all our desktop terminals. And the case is only 14" wide by 15" high by 13.6" deep. We're known throughout the industry for our high quality and reliability. On top of this, we probably have the widest range of available options in the field. Display formats from 256 to 4800 characters. Foreign language character sets. Special command sets. Custom keyboards. Editing, protected fields and block transmit.

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# LITERATURE

### Snap Action Switches

Catalog details complete line of snap action switches, and provides glossary and selection guide. **Cherry Electrical Products Corp,** Waukegan, Ill.
**Circle 281 on Inquiry Card**

### Keyboards

Brochure describing 10-, 12-, and 16-station encoded and non-encoded keyboards contains specs and dimensional diagrams. **ITT Datanetics Corp,** Fountain Valley, Calif.
**Circle 282 on Inquiry Card**

### Logic Development System

Universal, multi-user 64000 system for software and hardware development is subject of 32-p company journal illustrated with block diagrams, displays, and tables. **Hewlett-Packard Co,** Palo Alto, Calif.
**Circle 283 on Inquiry Card**

### Telecommunications Devices

Catalog covering video, voice, and data transmission system components describes over 80 items, and includes specs, photos, and reference sources for each. **GTE Lenkurt Inc,** San Carlos, Calif. **Circle 284 on Inquiry Card**

### Microminiature IC Packages

Applications brochure features spec selection guide, tabulated reliability evaluation, and circuit diagrams, as well as mounting, power dissipation, and cost effectiveness outline. **Signetics Corp,** Sunnyvale, Calif.
**Circle 285 on Inquiry Card**

### Microcomputer Software

Catalog lists over 50 media formats, CP/M compatible disc operating systems, hard disc integration modules, and word processing systems. **Lifeboat Associates,** New York, NY.
**Circle 286 on Inquiry Card**

### Test and Measurement Instruments

Oscilloscopes, data test equipment, counters and counters/timers, pulse generators, and TV test equipment are described in full catalog illustrated with specs, photos, graphs, and dimensional and timing diagrams. **Philips Test & Measuring Instruments, Inc,** Mahwah, NJ.
**Circle 287 on Inquiry Card**

### Uninterruptible Power Systems

Full specs are given for 750-VA and 15k-VA models in booklet featuring photos and flow diagrams. **Clary Corp,** San Gabriel, Calif.
**Circle 288 on Inquiry Card**

### Switching Power Supplies

Short form catalog tabulates electrical and mechanical specs on ac-dc and dc-dc supplies, and illustrates pin and socket configurations. **Power General,** Canton, Mass. **Circle 289 on Inquiry Card**


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RESEARCH REPORT

## OEM MINI/MICRO COMPUTER MARKETS

- Traces the evolution of the mini/microcomputer markets, and discusses the current market structure as it relates to the development of board level versus system products.
- Analyzes the current and future OEM mini, micro, and maxi computer markets, and evaluates the key technological factors affecting the future market, with expected trends in channels of distribution and product support.
- Reviews current semiconductor technology trends impacting the mini/microcomputer markets, and considers the Silicon Valley views on packaging, maintainability and software for future mini/microcomputer products.
- Provides ten-year projections for mini, micro and maxi computers, with a review of current and expected future strategies of leading suppliers.
- 170 pages; 22 exhibits; published March 1981; price $985.00.

For free descriptive literature and a detailed table of contents, contact:

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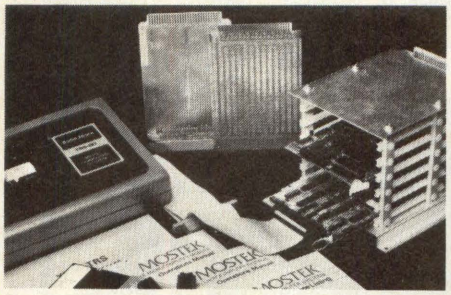

### STD BUS PROTOTYPE PACKAGE

The TRS-PROTO Package permits STD BUS Z80 Systems to be developed using a TRS-80 for all editing, assembling, and bulk storage. It includes the Mostek CPU2 card and Debug O.S., and is available for $895 as shown ($1050 for 4.0 MHz). A full catalog of STD BUS products from Mostek and other manufacturers is also available.

Contact **QC MICROSYSTEMS,** 9861 Chartwell Dr., Dallas, TX 75243, (214) 343-1282.

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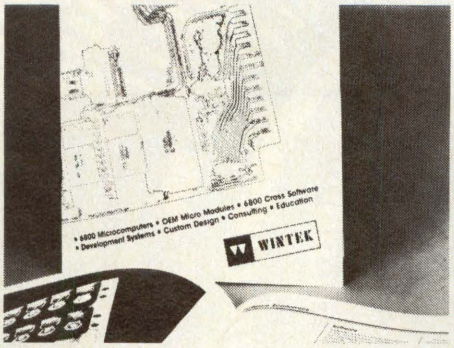


### FREE MICROPROCESSOR CATALOG

40 page catalog of 6800 single board computers, interface modules, SPRINT 68 control computer/development system, WIZRD multitasking DOS, assemblers, compilers, BASIC, cross assemblers, cross compilers, custom engineering, OEM applications software.

**WINTEK CORP.,** 1801 South Street, Lafayette, IN 47904; 317-742-8428.

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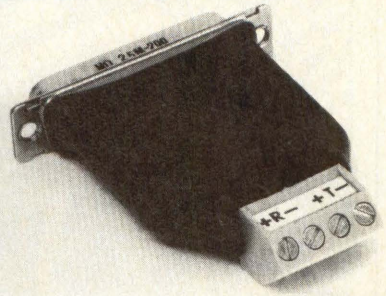


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**CIRCLE 527**

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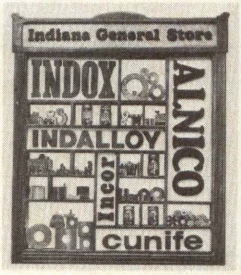


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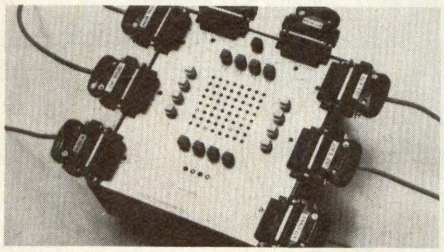

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**CIRCLE 529**

### ARE YOU PROGRAMMING AN INTEL MCS-48 FAMILY CHIP?

Cross assembler for Intel MCS-48 family of single chip microprocessors allows you to turn your single disk Heath H89 computer into a development system with the simple addition of an EPROM programmer. The program, in Microsoft BASIC, accepts named source file as input from diskette, logs error messages and output listing to either printer or CRT, and creates sequential hex address-opcode array as named file on diskette for subsequent downloading to EPROM programmer RAM. Use of popular Microsoft BASIC enables adapting this program to many other personal computers. Source listing plus user implementation documentation available for $95.00 from **INFORMATION ASSOCIATES,** PO Box 40713, Tucson, AZ 85717.

**CIRCLE 530**

### HEWLETT PACKARD 9845B/C & 9835A BINARY UTILITY PROGRAMS

Binary programs to enhance program editing capabilities and provide new keyboard commands are now available. ● **SEARCH & REPLACE** Provides a program-global facility to change names of labels, functions, variables and subprograms on BASIC programs in memory. ● **SYMBOL FINDER** Searches BASIC program for identifiers and reports defining line number and all occurrences. ● **MEMORY MAPPER** Prints memory map to help programmers write BASIC programs which execute faster and use less memory. ● **CROSS REFERENCE** An invaluable aid in preparing documentation. Produces a cross reference table to show all identifiers and line numbers where they occur. ● **DUMP ALPHA** Copies the CRT display to the internal printer or an external hardcopy device. ● **COMMENT STRIPPER** Removes comments from BASIC programs to reduce memory requirements and improve execution speed. ● **OEMSEC** Enciphers BASIC programs to prevent listing, tracing or interrogation of program variables. Insures that algorithms and trade secrets embodied in programs remain secure. ● **NODUP** Prevents duplication of the program media. Works with tape, floppy, or hard disc based systems.

**STRUCTURED SOFTWARE SYSTEMS, INC.,** Box 1072, Irick Road, Mt. Holly, NJ 08060. (609)267-1616

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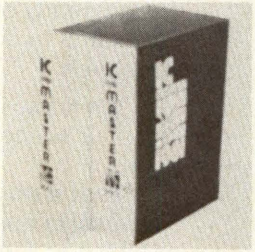
*IC MASTER*

*$82.50*

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**INTERNATIONAL MARKETING GROUP,** 17401 Irvine Blvd., Suite K, Tustin, CA 92680 (714) 832-5005

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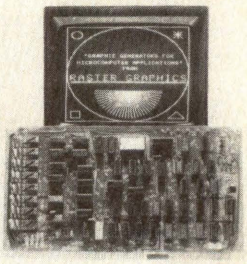


### GRAPHICS BOARD

The RG-SBC-GG1 256H x 240V Graphics Generator contains a hardware vector generator, two 256H x 240V refresh memories, and produces a high quality composite TV signal for use with a standard 525 line TV monitor. Ideal for games or moving displays. Includes manual for $395 ea. Manual only $20.

**RASTER GRAPHICS,** P O Box 23334, Tigard, Oregon, 97223. Tel. (503)620-2241.

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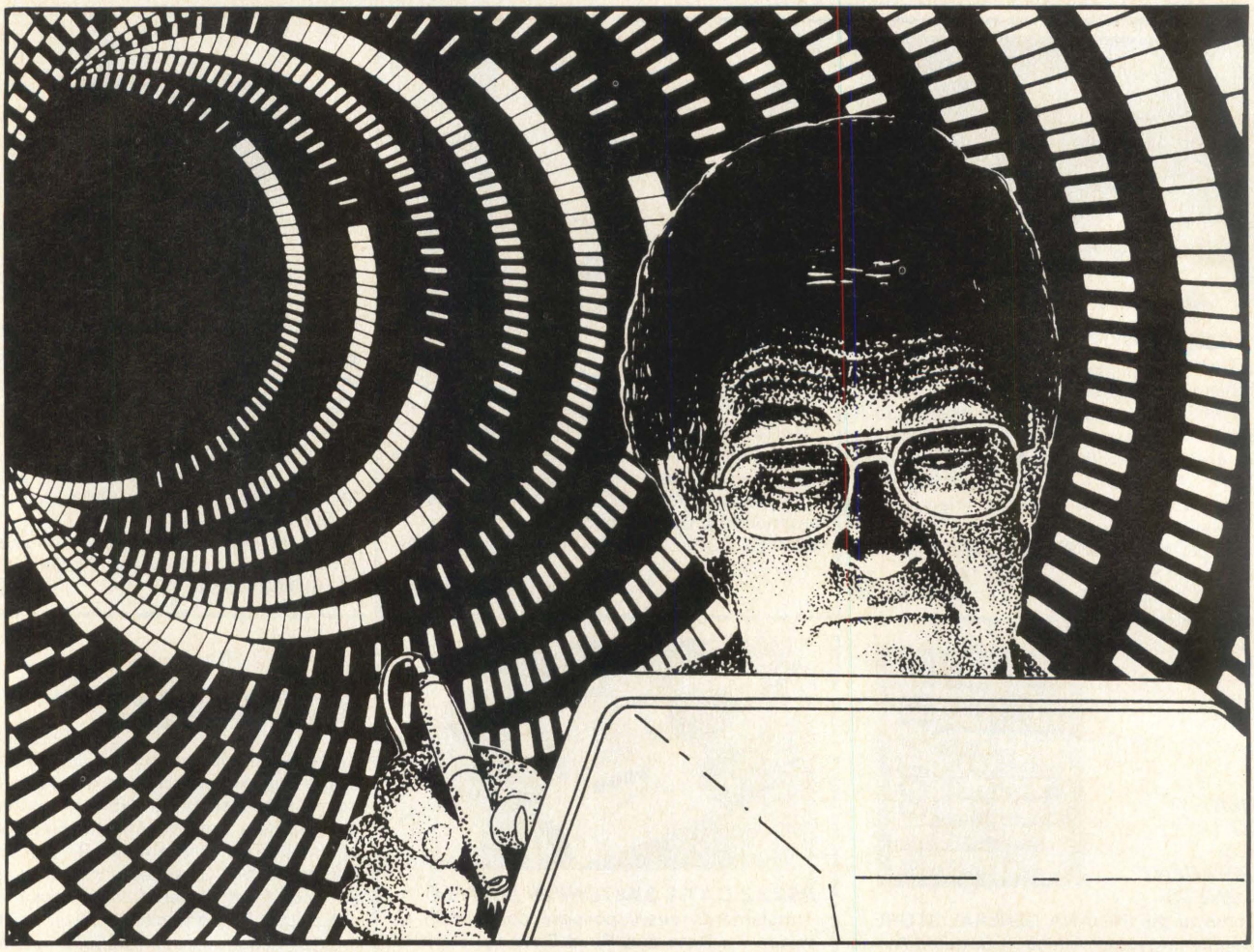

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## VOICE PROCESSING PRODUCTS MARKET

Frost & Sullivan has completed a 191-page report on the Voice Processing Market. An analysis and 10-year sales forecast in number of units, unit price and dollar sales are furnished for various product types in these voice processing categories: medium- and low-priced speaker dependent voice data entry; speaker dependent voice data entry; and low- and medium-priced voice response systems. An evaluation is made of voice data entry and response systems used separately or in combination. A state of the art description is provided for the various voice processing products. A questionnaire survey of those presently using and considering the use of voice processing equipment was one of the data gathering approaches, and the results are tabulated and interpreted. The industry structure is investigated, company profiles are provided, and company market shares are determined by major product category with future company market shares presented. The project director has headed a number of Frost & Sullivan reports in the small business computer, data entry and distributed data processing products market.

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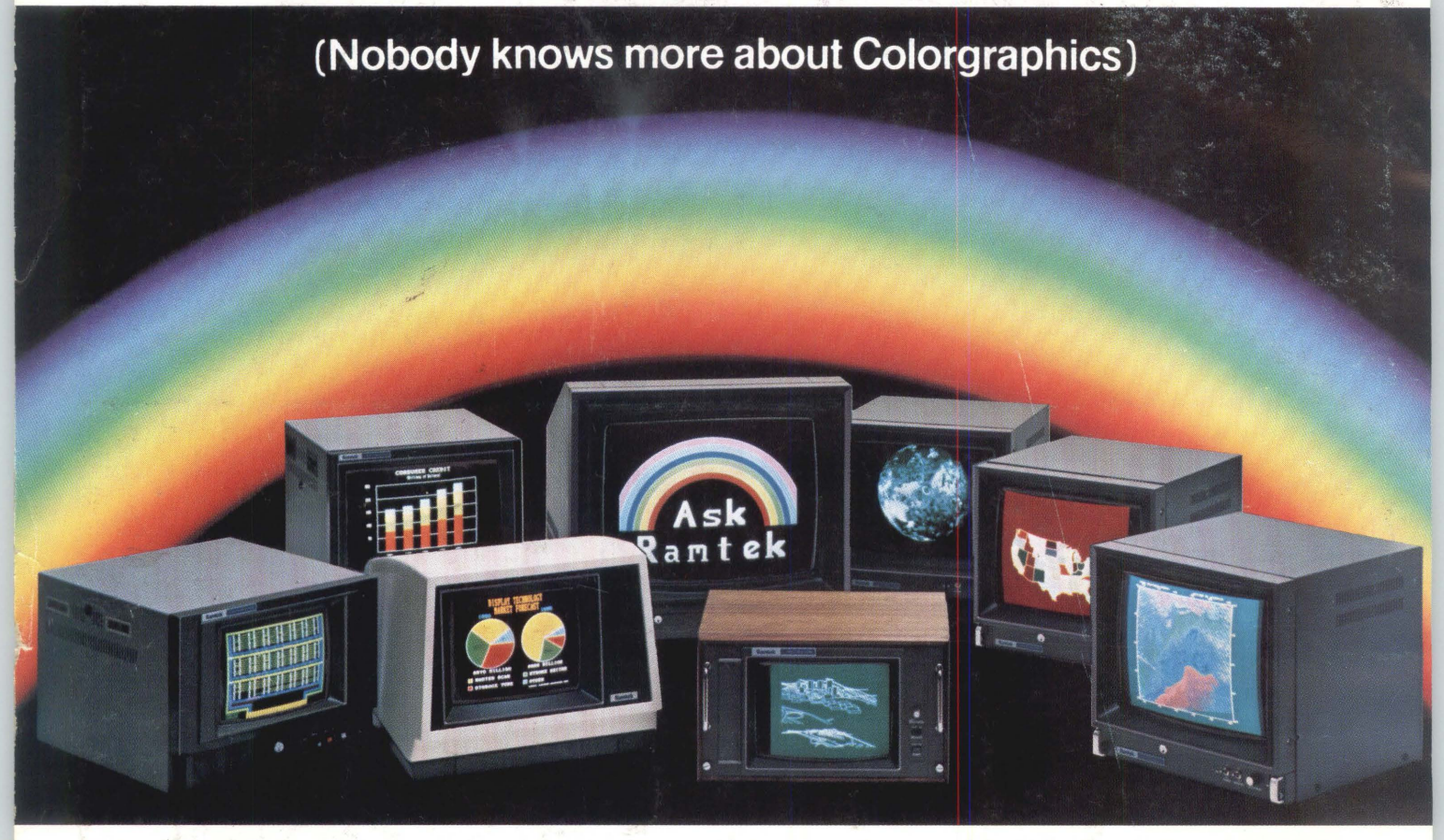


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